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EFM32GG940 Errata, Chip rev. D

F1024/F512

0 1 2 3 4

This document describes errata for the latest revision of EFM32GG940 devices.

ENERGY micro

1 Errata

This document contains information on the errata of the latest revision of this device. For errata on older revisions, please refer to the errata history for the device. The device datasheet explains how to identify chip revision, either from package marking or electronically.

In addition to the errata noted below, the errata for the ARM Cortex-M3 r2p1 (www.arm.com) also applies to this device.

1.1 Chip revision D

Table 1.1. Erratas

ID	Title/Problem	Effect	Fix/Workaround
ADC1	**Offset in ADC Temperature Sensor Calibration DataData** The ADC temperature sensor calibration value stored in the Device Information (DI) Page has an offset.	For devices with PROD_REV values of 16 or 17, the ADC0_TEMP_0_READ_1V25 register of the Device Information Page has an offset of 112. Using this value for calculating the absolute temperature gives an approximately 18 degrees too high value. Relative temperature measurements (temperature changes) are not affected by this offset.	For devices with PROD_REV values of 16 or 17, use ADC0_TEMP_0_READ_1V25 - 112 instead of ADC0_TEMP_0_READ_1V25 when calculating the temperature.
BURTC1	**BURTC LPMODE entry** Entering LPMODE with LPCOMP=7 causes counter error.	Counting error occurs if overflow on 7 LSBs happens when entering LPMODE with LPCOMP=7. This results in the counter value being 256 less than it should be after the error. The error accumulates.	Avoid using LPMODE with LPCOMP=7.
BU5	**LFXO missing cycles during IOVDD rampings** LFXO missing cycles during IOVDD ramping when used in combination with Backup mode.	When IOVDD is ramped, the DC-level of the XTAL signal changes, resulting in missed LFXO cycles and possible glitches on the LFXO clock.	Set PRESC in BURTC_CTRL to greater then 0 when ramping IOVDD in combination with Backup mode to avoid glitches on the LFXO clock.
BU6	**Current leakage in Backup mode**	In Backup mode, when VDD > BU_VIN + 0.7, current will leak from VDD.	To avoid leakage, exit Backup mode before VDD exceeds the voltage where the leakage start by configuring the threshold in EMU_BUACT.
CMU4	**LFXO boost buffer current setting** LFXO boost buffer current must be disabled	LFXO will not work properly with LFXOBUFCUR in CMU_CTRL set.	Do not set LFXOBUFCUR in CMU_CTRL.
CMU5	**LFXO startup at high temperature**	For devices with PROD_REV = 16, LFXO may have startup issues with low capacitance crystals when using the default LFXO configuration.	Make this line of code part of your starup code, typically in the start of main(): *((volatile uint32_t*) 0x400c80C0) = (*((volatile uint32_t*) 0x400c80C0) & ~(1<<6)) | (1<<4);.

ID	Title/Problem	Effect	Fix/Workaround
	LFXO does not start at high temperature with default configuration.		
DI1	**Flash Page Size** The MEM_INFO_PAGE_SIZE value stored in Device Information (DI) Page is incorrect.	For devices with PROD_REV values lower than 18, the MEM_INFO_PAGE_SIZE register value in the Device Information Page is incorrect.	Use fixed flash page size of 4k bytes.
LES3	**AUXHFRCO and LESENSE** LESENSE will not work properly at low AUXHFRCO frequencies.	LESENSE will not work properly when used with the AUXHFRCO running at the 1 or 7 MHz band.	Do not use a AUXHFRCO frequency band of 1 or 7 MHz when used in combination with LESENSE.
PRS1	**Edge detect on GPIO/ACMP** Edge detect on peripherals with asynchronous edges might be missed.	When using edge detect in PRS on signals from ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC edges can be missed.	Do not use edge detect on ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC.
USART1	**USART AUTOTX continues to transmit even with full RX buffer** USART AUTOTX continues to transmit even with full RX buffer.	When AUTOTX in USARTn_CTRL or AUTOTXEN in USARTn_TRIGCTRL is set, the USART will continue to transmit data even after the RX buffer is full. This may cause the RX buffer to overflow if the data is not read out in time.	No known workaround.
USB3	**HNP Sequence fails if A-Device connects after 3.4ms** HNP Sequence fails if A-Device connects after 3.4ms.	The B-Device core waits for less amount of time (3.4ms) and signals HNP fail and reverts back to Peripheral. HNP sequence fails if A-Device connects after 3.4ms.	No known workaround.
USB4	**USB A-Device delays the HNP switch back process** Disconnecting the D+ lines only occur after 200ms, making the HNP switch back delayed.	The A-Device core delays the HNP switch back process. As per the USB-OTG 2.0 specification, the B-Device on the other side of USB either should wait for disconnect from A-Device or should switch to Peripheral mode and wait for A-Device to issue reset. Hence, there is no significant impact on actual operation.	No known workaround.
USB5	**B-Device as Host driving K-J pairs during reset** A-Device misinterprets the K-J pairs as Suspend, after switching to High Speed mode.	If B-Device as Host on the other side of USB drives K-J pairs for more than 200ms during USB reset, the A-Device core exits peripheral state causing HNP process to fail. There is no significant impact since normally the host drives USB reset for lesser time than 200ms.	No known workaround.

2 Revision History

2.1 Revision 0.60

June 5th, 2012

Added ADC1.

Added DI1.

2.2 Revision 0.50

April 24th, 2012

Added BU6.

Added CMU4.

Added CMU5.

Added LES3.

Removed Erratas not valid for chip revision.

2.3 Revision 0.30

January 13th, 2012

Added USART1.

2.4 Revision 0.20

January 6th, 2012

Added CMU3.

Added CUR3.

Added CUR4.

Added USB7.

Added USB8.

Added MSC1.

Updated PRS1.

Removed Erratas not valid for chip revision.

2.5 Revision 0.10

November 4th, 2011

Initial preliminary release.

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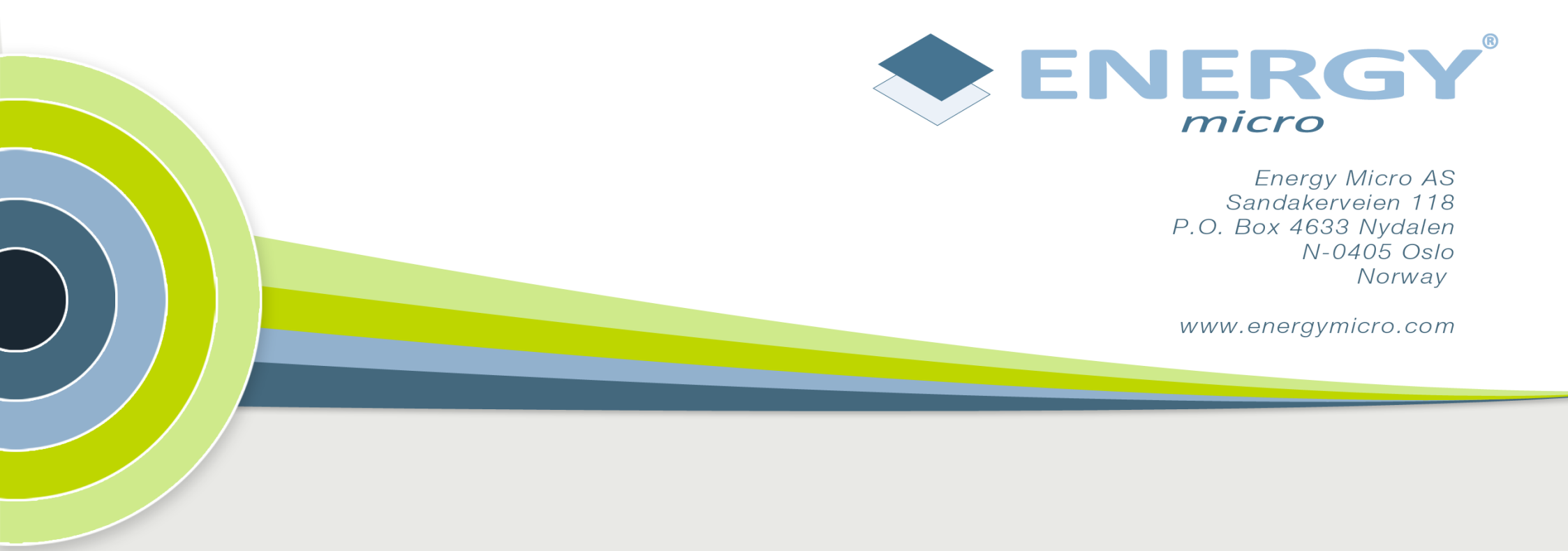

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