EFM32

... the world's most energy friendly microcontrollers

# EFM32GG842 Errata, Chip rev. D

*F1024/F512*

This document describes errata for the latest revision of EFM32GG842 devices.

ARM ZERO TINY GECKO LEOPARD GIANT WONDER

SILICON LABS

# 1 Errata

This document contains information on the errata of the latest revision of this device. For errata on older revisions, please refer to the errata history for the device. The device datasheet explains how to identify chip revision, either from package marking or electronically.

In addition to the errata noted below, the errata for the ARM Cortex-M3 r2p1 (www.arm.com) also applies to this device.

## 1.1 Chip revision D

***Table 1.1. Erratas***

| ID | Title/Problem | Effect | Fix/Workaround |
|---|---|---|---|
| ADC_E116 | **Offset in ADC Temperature Sensor Calibration DataData**<br><br>The ADC temperature sensor calibration value stored in the Device Information (DI) Page has an offset. | For devices with PROD_REV values of 16 or 17, the ADC0_TEMP_0_READ_1V25 register of the Device Information Page has an offset of 112. Using this value for calculating the absolute temperature gives an approximately 18 degrees too high value. Relative temperature measurements (temperature changes) are not affected by this offset. | For devices with PROD_REV values of 16 or 17, use ADC0_TEMP_0_READ_1V25 - 112 instead of ADC0_TEMP_0_READ_1V25 when calculating the temperature. |
| ADC_E117 | **TIMEBASE not wide enough**<br><br>For 48 MHz ADC clock, the ADC_CTRL_TIMEBASE is not wide enough. | For ADC warm-up, the user is required to set the ADC_CTRL_TIMEBASE to the number of ADC clock cycles in 1 µs. As this register is only 5 bits wide, it does not support frequencies above 32 MHz. | If an ADC clock above 32 MHz is required, the acquistion time should be increased to also account for too short warmup-time. |
| AES_E101 | **BYTEORDER does not work in combination with DATASTART/XORSTART**<br><br>When the BYTEORDER bit in AES_CTRL is set, an encryption or decryption should not be started through DATASTART or XORSTART. | If BYTEORDER is used in combination with DATASTART or XORSTART, the AES data and key are interpreted in the wrong order. | Do not use BYTEORDER in combination with DATASTART or XORSTART. |
| AES_E102 | **AES_STATUS_RUNNING set one cycle late with BYTEORDER set**<br><br>When the BYTEORDER bit in AES_CTRL is set, AES_STATUS_RUNNING is set one cycle late. | If BYTEORDER is used, it will take one cycle for the AES_STATUS_RUNNING flag to be set. This means that polling this status flag should be postponed at least one cycle after starting encryption/decryption. | If polling the AES_STATUS_RUNNING is preferred, insert a No Operation assembly instruction (NOP()) before starting to poll the status flag. |
| BURTC_E101 | **BURTC LPMODE entry** | Counting error occurs if overflow on 7 LSBs happens when entering LPMODE with LPCOMP=7. This results in the | Avoid using LPMODE with LPCOMP=7. |

| ID | Title/Problem | Effect | Fix/Workaround |
|---|---|---|---|
| | Entering LPMODE with LPCOMP=7 causes counter error. | counter value being 256 less than it should be after the error. The error accumulates. | |
| BURTC_E102 | **BURTC_CNT read error**<br><br>Software reads from BURTC_CNT might fail when LPMODE is activated | When LPMODE is active (i.e. BURTC_STATUS_LPMODEACT is high), software reads might result in wrong value being read from BURTC_CNT. | Before reading BURTC_CNT, disable LPMODE and wait for BURTC_STATUS_LPMODEACT to be cleared before reading BURTC_CNT. |
| BU_E105 | **LFXO missing cycles during IOVDD rampings**<br><br>LFXO missing cycles during IOVDD ramping when used in combination with Backup mode. | When IOVDD is ramped, the DC-level of the XTAL signal changes, resulting in missed LFXO cycles and possible glitches on the LFXO clock. | Set PRESC in BURTC_CTRL to greater then 0 when ramping IOVDD in combination with Backup mode to avoid glitches on the LFXO clock. |
| BU_E106 | **Current leakage in Backup mode** | In Backup mode, when VDD > BU_VIN + 0.7, current will leak from VDD. | To avoid leakage, exit Backup mode before VDD exceeds the voltage where the leakage start by configuring the threshold in EMU_BUACT. |
| CMU_E112 | **LFXO boost buffer current setting**<br><br>LFXO boost buffer current must be disabled | LFXO will not work properly with LFXOBUFCUR in CMU_CTRL set. | Do not set LFXOBUFCUR in CMU_CTRL. |
| CMU_E113 | **LFXO startup at high temperature**<br><br>LFXO does not start at high temperature with default configuration. | For devices with PROD_REV = 16, LFXO may have startup issues with low capacitance crystals when using the default LFXO configuration. | Make this line of code part of your starup code, typically in the start of main(): *((volatile uint32_t*) 0x400c80C0) = (*((volatile uint32_t*) 0x400c80C0) & ~(1<<6)) \| (1<<4);. |
| CMU_E114 | **Chip not waking up from EM2 when using prescaled non-HFRCO oscillator as HFCLK**<br><br>Chip not waking up from EM2 when using prescaled non-HFRCO oscillator as HFCLK. | When the chip is running from any other prescaled oscillator than HFRCO as HFCLK and HFRCO disabled the chip will not wake-up from EM2. | Before entering EM2, clear CMU_CTRL_HFCLKDIV or enable HFRCO by setting CMU_OSCENCMD_HFRCOEN and wait until CMU_STATUS_HFRCORDY is set. |
| DI_E101 | **Flash Page Size**<br><br>The MEM_INFO_PAGE_SIZE value stored in Device Information (DI) Page is incorrect. | For devices with PROD_REV values lower than 18, the MEM_INFO_PAGE_SIZE register value in the Device Information Page is incorrect. | Use fixed flash page size of 4k bytes. |
| DMA_E101 | **EM2 with WFE and DMA** | In EM2, when sleeping with WFE (Wait for Event), an interrupt from the DMA will not wake up the system. | Use WFI (Wait for Interrupt) or EM1 instead. |

| ID | Title/Problem | Effect | Fix/Workaround |
|---|---|---|---|
| | WFE does not work for the DMA in EM2. | | |
| LES_E103 | **AUXHFRCO and LESENSE**<br><br>LESENSE will not work properly at low AUXHFRCO frequencies. | LESENSE will not work properly when used with the AUXHFRCO running at the 1 or 7 MHz band. | Do not use a AUXHFRCO frequency band of 1 or 7 MHz when used in combination with LESENSE. |
| PRS_E101 | **Edge detect on GPIO/ACMP**<br><br>Edge detect on peripherals with asynchronous edges might be missed. | When using edge detect in PRS on signals from ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC edges can be missed. | Do not use edge detect on ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC. |
| USART_E112 | **USART AUTOTX continues to transmit even with full RX buffer**<br><br>USART AUTOTX continues to transmit even with full RX buffer. | When AUTOTX in USARTn_CTRL or AUTOTXEN in USARTn_TRIGCTRL is set, the USART will continue to transmit data even after the RX buffer is full. This may cause the RX buffer to overflow if the data is not read out in time. | No known workaround. |

## 1.2 Older Revisions

Erratas for older revisions can be found at the Silicon Laboratories Norway AS homepage:

www.energymicro.com/downloads/errata-archive

# 2 Revision History

## 2.1 Revision 0.80

August 21st, 2013

Added ADC_E117.

Added AES_E102.

Updated disclaimer, trademark and contact information.

## 2.2 Revision 0.70

July 30th, 2013

Added AES_E101.

Added BURTC_E102.

Added CMU_E114.

Added DMA_E101.

Updated errata naming convention.

## 2.3 Revision 0.60

June 5th, 2012

Added ADC1.

Added DI1.

## 2.4 Revision 0.50

April 24th, 2012

Added BU6.

Added CMU4.

Added CMU5.

Added LES3.

Removed Erratas not valid for chip revision.

## 2.5 Revision 0.40

January 19th, 2012

Updated CUR5.

## 2.6 Revision 0.30

January 13th, 2012

Added USART1.

## 2.7 Revision 0.20

January 6th, 2012

Added CMU3.

Added CUR3.

Added CUR5.

Added MSC1.

Updated PRS1.

Removed Erratas not valid for chip revision.

## 2.8 Revision 0.10

November 4th, 2011

Initial preliminary release.

# A Disclaimer and Trademarks

## A.1 Disclaimer

*Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.*

## A.2 Trademark Information

Silicon Laboratories Inc., Silicon Laboratories, the Silicon Labs logo, Energy Micro, EFM, EFM32, EFR, logo and combinations thereof, and others are the registered trademarks or trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.

# B Contact Information

**Silicon Laboratories Inc.**
400 West Cesar Chavez
Austin, TX 78701

Please visit the Silicon Labs Technical Support web page:
http://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

# Table of Contents

# List of Tables

silabs.com


ZERO
ARM Cortex-M0+
TINY
ARM Cortex-M3
GECKO
ARM Cortex-M3
LEOPARD
ARM Cortex-M3
GIANT
ARM Cortex-M3
WONDER
ARM Cortex-M4