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EFM32GG900 Errata History

F1024/F512



This document describes known errata for all revisions of EFM32GG900 devices.



1 Errata History

1.1 Errata Overview

Table 1.1 (p. 2) shows which erratum is applicable for each revision. The device datasheet explains how to identify chip revision, either from package marking or electronically.

In addition to the errata noted below, the errata for the ARM Cortex-M3 r2p1 (www.arm.com) also applies to all revisions of this device.

Table 1.1. Errata Overview

Erratum ID	Rev. D
ADC_E116	X
ADC_E117	X
AES_E101	X
AES_E102	X
BU_E105	X
BU_E106	X
BURTC_E101	X
BURTC_E102	X
CMU_E112	X
CMU_E113	X
CMU_E114	X
DI_E101	X
DMA_E101	X
EBI_E103	X
LES_E103	X
PRS_E101	X
USART_E112	X

Erratum ID	Rev. D
USB_E103	X
USB_E104	X
USB_E105	X
USB_E109	X
USB_E110	X

1.2 EFM32GG900 Errata Descriptions

Table 1.2. EFM32GG900 Errata Descriptions

ID	Title/Problem	Effect	Fix/Workaround
ADC_E116	Offset in ADC Temperature Sensor Calibration Data The ADC temperature sensor calibration value stored in the Device Information (DI) Page has an offset.	For devices with PROD_REV values of 16 or 17, the ADC0_TEMP_0_READ_1V25 register of the Device Information Page has an offset of 112. Using this value for calculating the absolute temperature gives an approximately 18 degrees too high value. Relative temperature measurements (temperature changes) are not affected by this offset.	For devices with PROD_REV values of 16 or 17, use ADC0_TEMP_0_READ_1V25 - 112 instead of ADC0_TEMP_0_READ_1V25 when calculating the temperature.
ADC_E117	TIMEBASE not wide enough For 48 MHz ADC clock, the ADC_CTRL_TIMEBASE is not wide enough.	For ADC warm-up, the user is required to set the ADC_CTRL_TIMEBASE to the number of ADC clock cycles in 1 µs. As this register is only 5 bits wide, it does not support frequencies above 32 MHz.	If an ADC clock above 32 MHz is required, the acquisition time should be increased to also account for too short warmup-time.
AES_E101	BYTEORDER does not work in combination with DATASTART/XORSTART When the BYTEORDER bit in AES_CTRL is set, an encryption or decryption should not be started through DATASTART or XORSTART.	If BYTEORDER is used in combination with DATASTART or XORSTART, the AES data and key are interpreted in the wrong order.	Do not use BYTEORDER in combination with DATASTART or XORSTART.
AES_E102	AES_STATUS_RUNNING set one cycle late with BYTEORDER set When the BYTEORDER bit in AES_CTRL is set,	If BYTEORDER is used, it will take one cycle for the AES_STATUS_RUNNING flag to be set. This means that polling this status flag should be postponed at least one cycle after starting encryption/decryption.	If polling the AES_STATUS_RUNNING is preferred, insert a No Operation assembly instruction (NOP()) before starting to poll the status flag.

ID	Title/Problem	Effect	Fix/Workaround
	AES_STATUS_RUNNING is set one cycle late.		
BU_E105	LFXO missing cycles during IOVDD rampings LFXO missing cycles during IOVDD ramping when used in combination with Backup mode.	When IOVDD is ramped, the DC-level of the XTAL signal changes, resulting in missed LFXO cycles and possible glitches on the LFXO clock.	Set PRESC in BURTC_CTRL to greater than 0 when ramping IOVDD in combination with Backup mode to avoid glitches on the LFXO clock.
BU_E106	Current leakage in Backup mode	In Backup mode, when VDD > BU_VIN + 0.7, current will leak from VDD.	To avoid leakage, exit Backup mode before VDD exceeds the voltage where the leakage starts by configuring the threshold in EMU_BUACT.
BURTC_E101	BURTC LPMODE entry Entering LPMODE with LPCOMP=7 causes counter error.	Counting error occurs if overflow on 7 LSBs happens when entering LPMODE with LPCOMP=7. This results in the counter value being 256 less than it should be after the error. The error accumulates.	Avoid using LPMODE with LPCOMP=7.
BURTC_E102	BURTC_CNT read error Software reads from BURTC_CNT might fail when LPMODE is activated	When LPMODE is active (i.e. BURTC_STATUS_LPMODEACT is high), software reads might result in wrong value being read from BURTC_CNT.	Before reading BURTC_CNT, disable LPMODE and wait for BURTC_STATUS_LPMODEACT to be cleared before reading BURTC_CNT.
CMU_E112	LFXO boost buffer current setting LFXO boost buffer current must be disabled	LFXO will not work properly with LFXOBUFCUR in CMU_CTRL set.	Do not set LFXOBUFCUR in CMU_CTRL.
CMU_E113	LFXO startup at high temperature LFXO does not start at high temperature with default configuration.	For devices with PROD_REV = 16, LFXO may have startup issues with low capacitance crystals when using the default LFXO configuration.	Make this line of code part of your startup code, typically in the start of main(): <code>*((volatile uint32_t*) 0x400c80c0) = (*((volatile uint32_t*) 0x400c80c0) & ~(1<<6)) (1<<4);</code> .
CMU_E114	Chip not waking up from EM2 when using prescaled non-HFRCO oscillator as HFCLK Chip not waking up from EM2 when using prescaled non-HFRCO oscillator as HFCLK.	When the chip is running from any other prescaled oscillator than HFRCO as HFCLK and HFRCO disabled the chip will not wake-up from EM2.	Before entering EM2, clear CMU_CTRL_HFCLKDIV or enable HFRCO by setting CMU_OSCENCMD_HFRCOEN and wait until CMU_STATUS_HFRCORDY is set.
DI_E101	Flash Page Size	For devices with PROD_REV values lower than 18, the MEM_INFO_PAGE_SIZE register value in the Device Information Page is incorrect.	Use fixed flash page size of 4k bytes.

ID	Title/Problem	Effect	Fix/Workaround
	The MEM_INFO_PAGE_SIZE value stored in Device Information (DI) Page is incorrect.		
DMA_E101	EM2 with WFE and DMA WFE does not work for the DMA in EM2.	In EM2, when sleeping with WFE (Wait for Event), an interrupt from the DMA will not wake up the system.	Use WFI (Wait for Interrupt) or EM1 instead.
EBI_E103	Page mode read in D16A16ALE mode Page mode read in D16A16ALE mode skips RDSETUP stage for page mode accesses.	Page mode read in D16A16ALE mode skips RDSETUP stage for page mode accesses, making the read process go directly from ADDRSETUP to RDPA.	To compensate for the missing hold time related to the ALE address latch, the HALFALE field in EBI_ADDRTIMING can be enabled providing a 1/2 cycle hold time.
LES_E103	AUXHFRCO and LESENSE LESENSE will not work properly at low AUXHFRCO frequencies.	LESENSE will not work properly when used with the AUXHFRCO running at the 1 or 7 MHz band.	Do not use a AUXHFRCO frequency band of 1 or 7 MHz when used in combination with LESENSE.
PRS_E101	Edge detect on GPIO/ACMP Edge detect on peripherals with asynchronous edges might be missed.	When using edge detect in PRS on signals from ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC edges can be missed.	Do not use edge detect on ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC.
USART_E112	USART AUTOTX continues to transmit even with full RX buffer USART AUTOTX continues to transmit even with full RX buffer.	When AUTOTX in USARTn_CTRL or AUTOTXEN in USARTn_TRIGCTRL is set, the USART will continue to transmit data even after the RX buffer is full. This may cause the RX buffer to overflow if the data is not read out in time.	No known workaround.
USB_E103	HNP Sequence fails if A-Device connects after 3.4ms HNP Sequence fails if A-Device connects after 3.4ms.	The B-Device core waits for less amount of time (3.4ms) and signals HNP fail and reverts back to Peripheral. HNP sequence fails if A-Device connects after 3.4ms.	No known workaround.
USB_E104	USB A-Device delays the HNP switch back process Disconnecting the D+ lines only occur after 200ms, making the HNP switch back delayed.	The A-Device core delays the HNP switch back process. As per the USB-OTG 2.0 specification, the B-Device on the other side of USB either should wait for disconnect from A-Device or should switch to Peripheral mode and wait for A-Device to issue reset. Hence, there is no significant impact on actual operation.	No known workaround.
USB_E105	B-Device as Host driving K-J pairs during reset	If B-Device as Host on the other side of USB drives K-J pairs for more than 200ms during USB reset, the A-Device core	No known workaround.

ID	Title/Problem	Effect	Fix/Workaround
	A-Device misinterprets the K-J pairs as Suspend, after switching to High Speed mode.	exits peripheral state causing HNP process to fail. There is no significant impact since normally the host drives USB re-set for lesser time than 200ms.	
USB_E109	Missing GINTSTS.SessReq Interrupt with USB_PCGCCTL.STOPPCLK = 1 A Host-initiated Suspend, followed by a Host Disconnect and Host Connect will not result in a SessReq interrupt.	When USB_PCGCCTL.STOPPCLK is set and the device is acting as a B-peripheral, a Host-initiated Suspend, followed by a Host Disconnect and Host Connect will not result in a SessReq interrupt.	If this is an expected use-case, USB_PCGCCTL.STOPPCLK should not be set. USB_PCGCCTL.GATEHCLK can still be used to save power.
USB_E110	Unexpected HCINTn.ChHltd interrupt In some cases the HCINTn.ChHltd interrupt might be wrongly set.	In some cases an unexpected HCINTn.ChHltd interrupt might be received from another endpoint from which it has not set the HCCHARn.CHDis, HCINTn.XactErr, HCINTn.BblErr, HCINTn.DataTglErr or HCINTn.XferComplete interrupt.	If such an interrupt is received, the application must re-enable the channel for which it received the unexpected HCINTn.ChHltd interrupt.

2 Revision History

2.1 Revision 1.00

Aug 8th, 2014

Initial release.

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B Contact Information

Silicon Laboratories Inc.

400 West Cesar Chavez

Austin, TX 78701

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