EFM32®

... the world's most energy friendly microcontrollers

EFM32G800 DATASHEET

F128

- **ARM Cortex-M3 CPU platform**
  - High Performance 32-bit processor @ up to 32 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 20 nA @ 3 V Shutoff Mode
  - 0.6 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.9 µA @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 45 µA/MHz @ 3 V Sleep Mode
  - 180 µA/MHz @ 3 V Run Mode, with code executed from flash
- **128 KB Flash**
- **16 KB RAM**
- **90 General Purpose I/O pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 16 asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **8 Channel DMA Controller**
- **8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Hardware AES with 128/256-bit keys in 54/75 cycles**
- **Timers/Counters**
  - 3× 16-bit Timer/Counter
    - 3×3 Compare/Capture/PWM channels
    - Dead-Time Insertion on TIMER0
  - 16-bit Low Energy Timer
  - 1× 24-bit Real-Time Counter
  - 3× 8-bit Pulse Counter
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- **Integrated LCD Controller for up to 4×40 segments**
  - Voltage boost, adjustable contrast and autonomous animation
- **External Bus Interface for up to 4x64 MB of external memory mapped space**
- **Communication interfaces**
  - 3× Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA
    - Triple buffered full/half-duplex operation
  - 1× Universal Asynchronous Receiver/Transmitter
  - 2× Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - I^2C Interface with SMBus support
    - Address recognition in Stop Mode
- **Ultra low power precision analog peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter
    - 8 single ended channels/4 differential channels
    - On-chip temperature sensor
  - 12-bit 500 ksamples/s Digital to Analog Converter
    - 2 single ended channels/1 differential channel
  - 2× Analog Comparator
    - Capacitive sensing with up to 16 inputs
  - Supply Voltage Comparator
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **2-pin Serial Wire Debug interface**
  - 1-pin Serial Wire Viewer
- **Pre-Programmed UART Bootloader**
- **Temperature range -40 to 85 ºC**
- **Single power supply 1.98 to 3.8 V**
- **Delivered as full wafer**

32-bit ARM Cortex-M0+, Cortex-M3 and Cortex-M4 microcontrollers for:

- Energy, gas, water and smart metering
- Health and fitness applications
- Smart accessories
- Alarm and security systems
- Industrial and home automation

ARM ZERO TINY GECKO LEOPARD GIANT WONDER

SILICON LABS

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32G800 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (ºC)	Package
EFM32G800F128G-D-D1I	128	16	32	1.98 - 3.8	-40 - 85	Wafer

Visit **www.silabs.com** for information on global distributors and representatives.

2 System Summary

The EFM32G800 products are delivered in wafer form, but are otherwise identical to the EFM32G890 packaged parts. Please refer to the EFM32G890 datasheet for additional information.

3 Pinout and Package

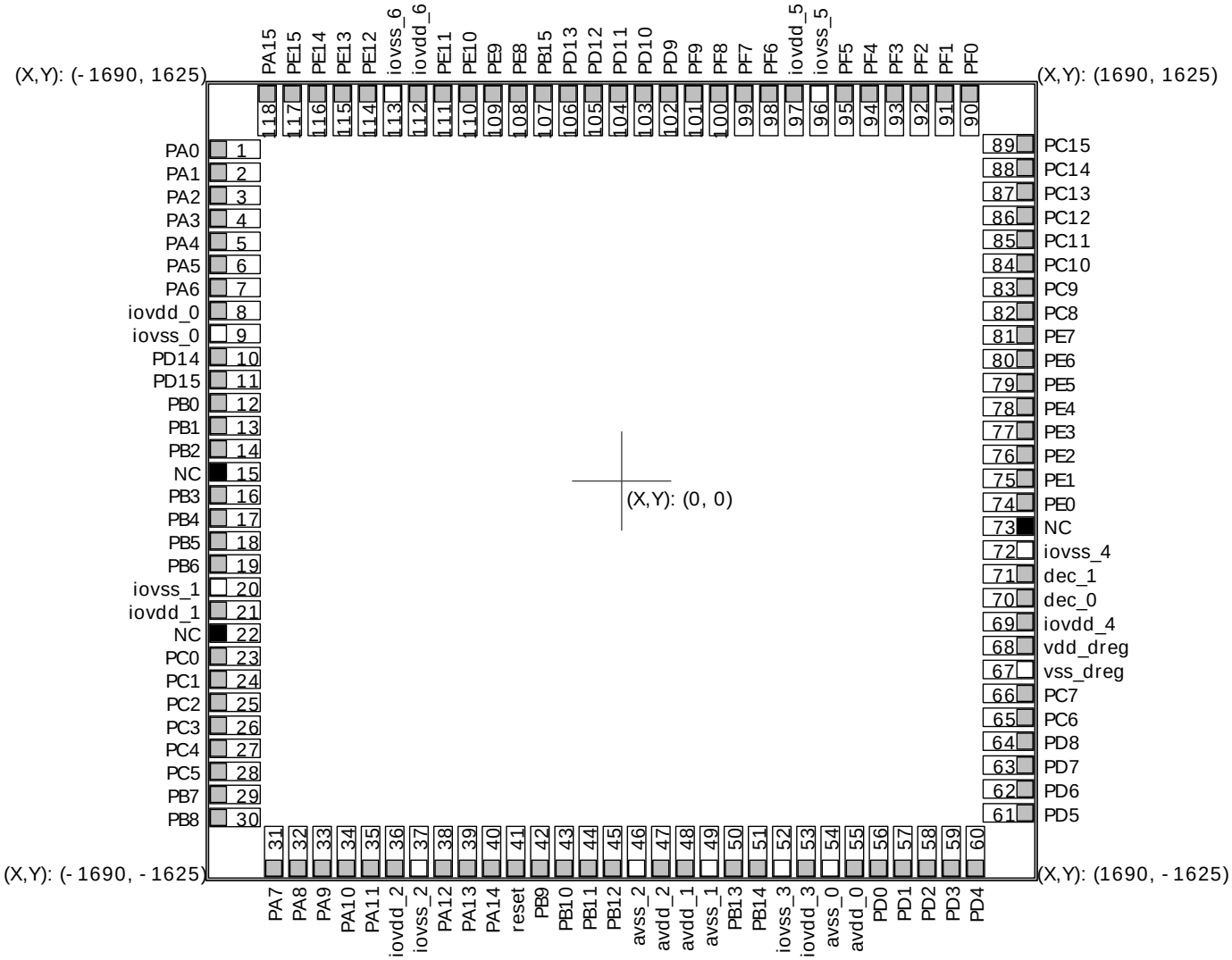
Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32G800.

3.1 Padout

The *EFM32G800* padout is shown in Figure 3.1 (p. 4) and Table 3.1 (p. 5). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pad are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 3.1. EFM32G800 Padout (top view, not to scale)



The pad coordinates represent the center of the pad opening relative to the die center.

Table 3.1. Device Padout

Wafer Pads and Coordinates				Pad Alternate Functionality / Description				
Pad #	Pad Name	X [µm]	Y [µm]	Analog	EBI	Timers	Commu-nication	Other
1	PA0	-1640.0	1350.0	LCD_SEG13	EBI_AD09 #0	TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1	-1640.0	1256.2	LCD_SEG14	EBI_AD10 #0	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2	-1640.0	1162.5	LCD_SEG15	EBI_AD11 #0	TIM0_CC2 #0/1		CMU_CLK0 #0
4	PA3	-1640.0	1068.8	LCD_SEG16	EBI_AD12 #0	TIM0_CDTI0 #0	U0_TX #2	
5	PA4	-1640.0	975.0	LCD_SEG17	EBI_AD13 #0	TIM0_CDTI1 #0	U0_RX #2	
6	PA5	-1640.0	881.2	LCD_SEG18	EBI_AD14 #0	TIM0_CDTI2 #0	LEU1_TX #1	
7	PA6	-1640.0	787.5	LCD_SEG19	EBI_AD15 #0		LEU1_RX #1	
8	IOVDD_0	-1640.0	693.8	Digital IO power supply 0.				
9	IOVSS_0	-1640.0	600.0	Digital IO ground 0.				
10	PD14	-1640.0	506.2				I2C0_SDA #3	
11	PD15	-1640.0	412.5				I2C0_SCL #3	
12	PB0	-1640.0	318.8	LCD_SEG32		TIM1_CC0 #2		
13	PB1	-1640.0	225.0	LCD_SEG33		TIM1_CC1 #2		
14	PB2	-1640.0	131.2	LCD_SEG34		TIM1_CC2 #2		
15	NC	-1640.0	37.5	Do not connect.				
16	PB3	-1640.0	-56.2	LCD_SEG20		PCNT1_S0IN #1	US2_TX #1	
17	PB4	-1640.0	-150.0	LCD_SEG21		PCNT1_S1IN #1	US2_RX #1	
18	PB5	-1640.0	-243.8	LCD_SEG22			US2_CLK #1	
19	PB6	-1640.0	-337.5	LCD_SEG23			US2_CS #1	
20	IOVSS_1	-1640.0	-431.2	Digital IO ground 1.				
21	IOVDD_1	-1640.0	-525.0	Digital IO power supply 1.				
22	NC	-1640.0	-618.8	Do not connect.				
23	PC0	-1640.0	-712.5	ACMP0_CH0		PCNT0_S0IN #2	US1_TX #0	
24	PC1	-1640.0	-806.2	ACMP0_CH1		PCNT0_S1IN #2	US1_RX #0	
25	PC2	-1640.0	-900.0	ACMP0_CH2			US2_TX #0	
26	PC3	-1640.0	-993.8	ACMP0_CH3			US2_RX #0	
27	PC4	-1640.0	-1087.5	ACMP0_CH4		LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0	
28	PC5	-1640.0	-1181.2	ACMP0_CH5		LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
29	PB7	-1640.0	-1275.0	LFXTAL_P			US1_CLK #0	
30	PB8	-1640.0	-1368.8	LFXTAL_N			US1_CS #0	
31	PA7	-1415.0	-1575.0	LCD_SEG35				
32	PA8	-1316.6	-1575.0	LCD_SEG36		TIM2_CC0 #0		
33	PA9	-1218.2	-1575.0	LCD_SEG37		TIM2_CC1 #0		
34	PA10	-1119.8	-1575.0	LCD_SEG38		TIM2_CC2 #0		
35	PA11	-1021.4	-1575.0	LCD_SEG39				
36	IOVDD_2	-923.0	-1575.0	Digital IO power supply 2.				
37	IOVSS_2	-824.6	-1575.0	Digital IO ground 2.				
38	PA12	-726.2	-1575.0	LCD_BCAP_P		TIM2_CC0 #1		

Wafer Pads and Coordinates				Pad Alternate Functionality / Description				
Pad #	Pad Name	X [µm]	Y [µm]	Analog	EBI	Timers	Commu-nication	Other
39	PA13	-627.9	-1575.0	LCD_BCAP_N		TIM2_CC1 #1		
40	PA14	-529.5	-1575.0	LCD_BEXT		TIM2_CC2 #1		
41	RESETn	-431.1	-1575.0	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
42	PB9	-332.7	-1575.0					
43	PB10	-234.3	-1575.0					
44	PB11	-135.9	-1575.0	DAC0_OUT0		LETIM0_OUT0 #1		
45	PB12	-37.5	-1575.0	DAC0_OUT1		LETIM0_OUT1 #1		
46	AVSS_2	60.9	-1575.0	Analog ground 2.				
47	AVDD_2	159.3	-1575.0	Analog power supply 2.				
48	AVDD_1	257.7	-1575.0	Analog power supply 1.				
49	AVSS_1	356.1	-1575.0	Analog ground 1.				
50	PB13	454.5	-1575.0	HFXTAL_P			LEU0_TX #1	
51	PB14	552.9	-1575.0	HFXTAL_N			LEU0_RX #1	
52	IOVSS_3	651.2	-1575.0	Digital IO ground 3.				
53	IOVDD_3	749.6	-1575.0	Digital IO power supply 3.				
54	AVSS_0	848.0	-1575.0	Analog ground 0.				
55	AVDD_0	946.4	-1575.0	Analog power supply 0.				
56	PD0	1044.8	-1575.0	ADC0_CH0		PCNT2_S0IN #0	US1_TX #1	
57	PD1	1143.2	-1575.0	ADC0_CH1		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	
58	PD2	1241.6	-1575.0	ADC0_CH2		TIM0_CC1 #3	US1_CLK #1	
59	PD3	1340.0	-1575.0	ADC0_CH3		TIM0_CC2 #3	US1_CS #1	
60	PD4	1438.4	-1575.0	ADC0_CH4			LEU0_TX #0	
61	PD5	1640.0	-1350.0	ADC0_CH5			LEU0_RX #0	
62	PD6	1640.0	-1252.8	ADC0_CH6		LETIM0_OUT0 #0	I2C0_SDA #1	
63	PD7	1640.0	-1155.6	ADC0_CH7		LETIM0_OUT1 #0	I2C0_SCL #1	
64	PD8	1640.0	-1058.3					CMU_CLK1 #1
65	PC6	1640.0	-961.1	ACMP0_CH6			LEU1_TX #0 I2C0_SDA #2	
66	PC7	1640.0	-863.9	ACMP0_CH7			LEU1_RX #0 I2C0_SCL #2	
67	VSS_DREG	1640.0	-766.7	Ground for on-chip voltage regulator.				
68	VDD_DREG	1640.0	-669.4	Power supply for on-chip voltage regulator.				
69	IOVDD_4	1640.0	-572.2	Digital IO power supply 4.				
70	DEC_0	1640.0	-475.0	Decouple output for on-chip voltage regulator.				
71	DEC_1	1640.0	-377.8	Decouple output for on-chip voltage regulator.				
72	IOVSS_4	1640.0	-280.6	Digital IO ground 4.				
73	NC	1640.0	-183.3	Do not connect.				
74	PE0	1640.0	-86.1			PCNT0_S0IN #1	U0_TX #1	
75	PE1	1640.0	11.1			PCNT0_S1IN #1	U0_RX #1	

Wafer Pads and Coordinates				Pad Alternate Functionality / Description				
Pad #	Pad Name	X [µm]	Y [µm]	Analog	EBI	Timers	Commu-nication	Other
76	PE2	1640.0	108.3					ACMP0_O #1
77	PE3	1640.0	205.6					ACMP1_O #1
78	PE4	1640.0	302.8	LCD_COM0			US0_CS #1	
79	PE5	1640.0	400.0	LCD_COM1			US0_CLK #1	
80	PE6	1640.0	497.2	LCD_COM2			US0_RX #1	
81	PE7	1640.0	594.4	LCD_COM3			US0_TX #1	
82	PC8	1640.0	691.7	ACMP1_CH0		TIM2_CC0 #2	US0_CS #2	
83	PC9	1640.0	788.9	ACMP1_CH1		TIM2_CC1 #2	US0_CLK #2	
84	PC10	1640.0	886.1	ACMP1_CH2		TIM2_CC2 #2	US0_RX #2	
85	PC11	1640.0	983.3	ACMP1_CH3			US0_TX #2	
86	PC12	1640.0	1080.6	ACMP1_CH4				CMU_CLK0 #1
87	PC13	1640.0	1177.8	ACMP1_CH5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
88	PC14	1640.0	1275.0	ACMP1_CH6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	
89	PC15	1640.0	1372.2	ACMP1_CH7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1
90	PF0	1415.0	1575.0			LETIM0_OUT0 #2		DBG_SWCLK #0/1
91	PF1	1313.0	1575.0			LETIM0_OUT1 #2		DBG_SWDIO #0/1
92	PF2	1210.9	1575.0	LCD_SEG0	EBI_ARDY #0			ACMP1_O #0 DBG_SWO #0
93	PF3	1108.9	1575.0	LCD_SEG1	EBI_ALE #0	TIM0_CDTI0 #2		
94	PF4	1006.9	1575.0	LCD_SEG2	EBI_WEn #0	TIM0_CDTI1 #2		
95	PF5	904.8	1575.0	LCD_SEG3	EBI_REn #0	TIM0_CDTI2 #2		
96	IOVSS_5	802.8	1575.0	Digital IO ground 5.				
97	IOVDD_5	700.7	1575.0	Digital IO power supply 5.				
98	PF6	598.7	1575.0	LCD_SEG24		TIM0_CC0 #2	U0_TX #0	
99	PF7	496.7	1575.0	LCD_SEG25		TIM0_CC1 #2	U0_RX #0	
100	PF8	394.6	1575.0	LCD_SEG26		TIM0_CC2 #2		
101	PF9	292.6	1575.0	LCD_SEG27				
102	PD9	190.6	1575.0	LCD_SEG28	EBI_CS0 #0			
103	PD10	88.5	1575.0	LCD_SEG29	EBI_CS1 #0			
104	PD11	-13.5	1575.0	LCD_SEG30	EBI_CS2 #0			
105	PD12	-115.6	1575.0	LCD_SEG31	EBI_CS3 #0			
106	PD13	-217.6	1575.0					
107	PB15	-319.6	1575.0					
108	PE8	-421.7	1575.0	LCD_SEG4	EBI_AD00 #0	PCNT2_S0IN #1		
109	PE9	-523.7	1575.0	LCD_SEG5	EBI_AD01 #0	PCNT2_S1IN #1		
110	PE10	-625.7	1575.0	LCD_SEG6	EBI_AD02 #0	TIM1_CC0 #1	US0_TX #0	BOOT_TX
111	PE11	-727.8	1575.0	LCD_SEG7	EBI_AD03 #0	TIM1_CC1 #1	US0_RX #0	BOOT_RX
112	IOVDD_6	-829.8	1575.0	Digital IO power supply 6.				

Wafer Pads and Coordinates				Pad Alternate Functionality / Description				
Pad #	Pad Name	X [µm]	Y [µm]	Analog	EBI	Timers	Commu-nication	Other
113	IOVSS_6	-931.9	1575.0	Digital IO ground 6.				
114	PE12	-1033.9	1575.0	LCD_SEG8	EBI_AD04 #0	TIM1_CC2 #1	US0_CLK #0	
115	PE13	-1135.9	1575.0	LCD_SEG9	EBI_AD05 #0		US0_CS #0	ACMP0_O #0
116	PE14	-1238.0	1575.0	LCD_SEG10	EBI_AD06 #0		LEU0_TX #2	
117	PE15	-1340.0	1575.0	LCD_SEG11	EBI_AD07 #0		LEU0_RX #2	
118	PA15	-1442.0	1575.0	LCD_SEG12	EBI_AD08 #0			

3.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 3.2 (p. 8). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 3.2. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5				Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6				Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7				Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2			Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12				Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3			Analog comparator ACMP1, digital output.
ADC0_CH0	PD0				Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1				Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2				Analog to digital converter ADC0, input channel number 2.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ADC0_CH3	PD3				Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2	PC12			Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8			Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD00	PE8				External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9				External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10				External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11				External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12				External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13				External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14				External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15				External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15				External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0				External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2				External Bus Interface (EBI) Hardware Ready Control input.
EBI_CS0	PD9				External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10				External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11				External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12				External Bus Interface (EBI) Chip Select output 3.
EBI_REn	PF5				External Bus Interface (EBI) Read Enable output.
EBI_WEn	PF4				External Bus Interface (EBI) Write Enable output.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
HFXTAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	I2C0 Serial Data input / output.
LCD_BCAP_N	PA13				LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12				LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14				LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4				LCD driver common line number 0.
LCD_COM1	PE5				LCD driver common line number 1.
LCD_COM2	PE6				LCD driver common line number 2.
LCD_COM3	PE7				LCD driver common line number 3.
LCD_SEG0	PF2				LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3				LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4				LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5				LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8				LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9				LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10				LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11				LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12				LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13				LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14				LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15				LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG12	PA15				LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG13	PA0				LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1				LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2				LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3				LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4				LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5				LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG19	PA6				LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LCD_SEG20	PB3				LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG21	PB4				LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG22	PB5				LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG23	PB6				LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5.
LCD_SEG24	PF6				LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG25	PF7				LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG26	PF8				LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG27	PF9				LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG28	PD9				LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG29	PD10				LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG30	PD11				LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG31	PD12				LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG32	PB0				LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG33	PB1				LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG34	PB2				LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG35	PA7				LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG36	PA8				LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG37	PA9				LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG38	PA10				LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG39	PA11				LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6			LEUART1 Receive input.
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1		Pulse Counter PCNT0 input number 1.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
PCNT1_S0IN	PC4	PB3			Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4			Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.
TIM0_CC0	PA0	PA0	PF6	PD1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0		Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1		Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2		Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10		Timer 2 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15	UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX	PC3	PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3			USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

3.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32G800* is shown in Table 3.3 (p. 13). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 3.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	-	-	-	-	-	-	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

3.4 Bonding Instructions

All pads should be bonded out, with the exception of the pads labeled “NC” and listed as “Do not connect” in Table 3.1 (p. 5) . Gold bond wires are recommended for these devices.

Both voltage regulator output decouple pads (DEC_0, DEC_1) must be bonded out and electrically connected on the PCB. In the packaged devices, both of these pads are bonded to a single DECOUPLE pin.

3.5 Wafer Description

Table 3.4. Wafer and Die Information

Parameter	Value
Device Family	EFM32G (Gecko)
Wafer Diameter	8 in
Die Dimensions (Outer edge of seal ring)	3380 µm × 3250 µm
Wafer Thickness (No backgrind)	725 µm ±15 µm (28.54 mil ±1 mil)
Wafer Identification	Notch
Scribe Street Width	80 µm × 80 µm
Die Per Wafer [1]	Contact sales for information
Passivation	Standard
Wafer Packaging Detail	Wafer Jar
Bond Pad Dimensions	65 µm (parallel to die edge) × 66 µm
Bond Pad Pitch Minimum	81 µm
Maximum Processing Temperature	250°C
Electronic Die Map Format	.txt

[1]Note: This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).

3.5.1 Environmental

Bare silicon die are susceptible to mechanical damage and may be sensitive to light. When bare die must be used in an environment exposed to light, it may be necessary to cover the top and sides with an opaque material.

For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx.

3.6 Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18 - 24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).

3.7 Failure Analysis (FA) Guidelines

Certain conditions must be met for Silicon Laboratories to perform Failure Analysis on devices sold in wafer form.

- In order to conduct failure analysis on a device in a customer-provided package, Silicon Laboratories must be provided with die assembled in an industry standard package that is pin compatible with existing packages Silicon Laboratories offers for the device. Initial response time for FA requests that meet these requirements will follow the standard FA guidelines for packaged parts.
- If retest of the entire wafer is requested, Silicon Laboratories must be provided with the whole wafer. Silicon Laboratories cannot retest any wafers that have been sawed, diced, backgrind or are on tape. Initial response time for FA requests that meet these requirements will be 3 weeks.

4 Chip Marking, Revision and Errata

4.1 Errata

Please see the errata document for EFM32G800 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:
http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

5 Revision History

5.1 Revision 1.90

May 22nd, 2015

Added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

Corrected EM2 current consumption condition in Electrical Characteristics section.

Added AUXHFRCO to block diagram and Electrical Characteristics.

Updated HFRCO table in the Electrical Characteristics section.

Updated EM0, EM2, EM3, and EM4 maximum current specifications in the Electrical Characteristics section.

Updated the Output Low Voltage maximum for sinking 20 mA with VDD = 3.0 V in the Electrical Characteristics section.

Updated the Input Leakage Current maximum in the Electrical Characteristics section.

Updated the minimum and maximum frequency specifications for the LFRCO, HFRCO, and AUXHFRCO in the Electrical Characteristics section.

Updated the maximum current consumption of the HFRCO in the Electrical Characteristics section.

Updated the maximum current consumption of the HFRCO in the Electrical Characteristics section.

Added some minimum ADC SNR, SNDR, and SFDR specifications in the Electrical Characteristics section.

Added some minimum and maximum ADC offset voltage, DNL, and INL specifications in the Electrical Characteristics section.

Added maximum DAC current specifications in the Electrical Characteristics section.

Added maximum ACMP current and maximum and minimum offset voltage specifications in the Electrical Characteristics section.

Added maximum VCMP current and updated typical VCMP current specifications in the Electrical Characteristics section.

Updated references to energyAware Designer to Configurator.

5.2 Revision 1.10

December 12th, 2014

Added recommendation to use gold bond wire.

5.3 Revision 1.00

October 15th, 2014

Initial release.

A Disclaimer and Trademarks

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Table of Contents

List of Figures

List of Tables

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