K82 Sub-Family Reference Manual

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MK82FN256VLQ15, MK82FN256CAx15

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Chapter 1
About This Manual

1.1 Audience

This reference manual is intended for system software and hardware developers and applications programmers who want to develop products with this device. It assumes that the reader understands operating systems, microprocessor system design, and basic principles of software and hardware.

1.2 Organization

This manual has two main sets of chapters.

1. Chapters in the first set contain information that applies to all components on the chip.
2. Chapters in the second set are organized into functional groupings that detail particular areas of functionality.
   - Examples of these groupings are clocking, timers, and communication interfaces.
   - Each grouping includes chapters that provide a technical description of individual modules.

1.3 Module descriptions

Each module chapter has two main parts:

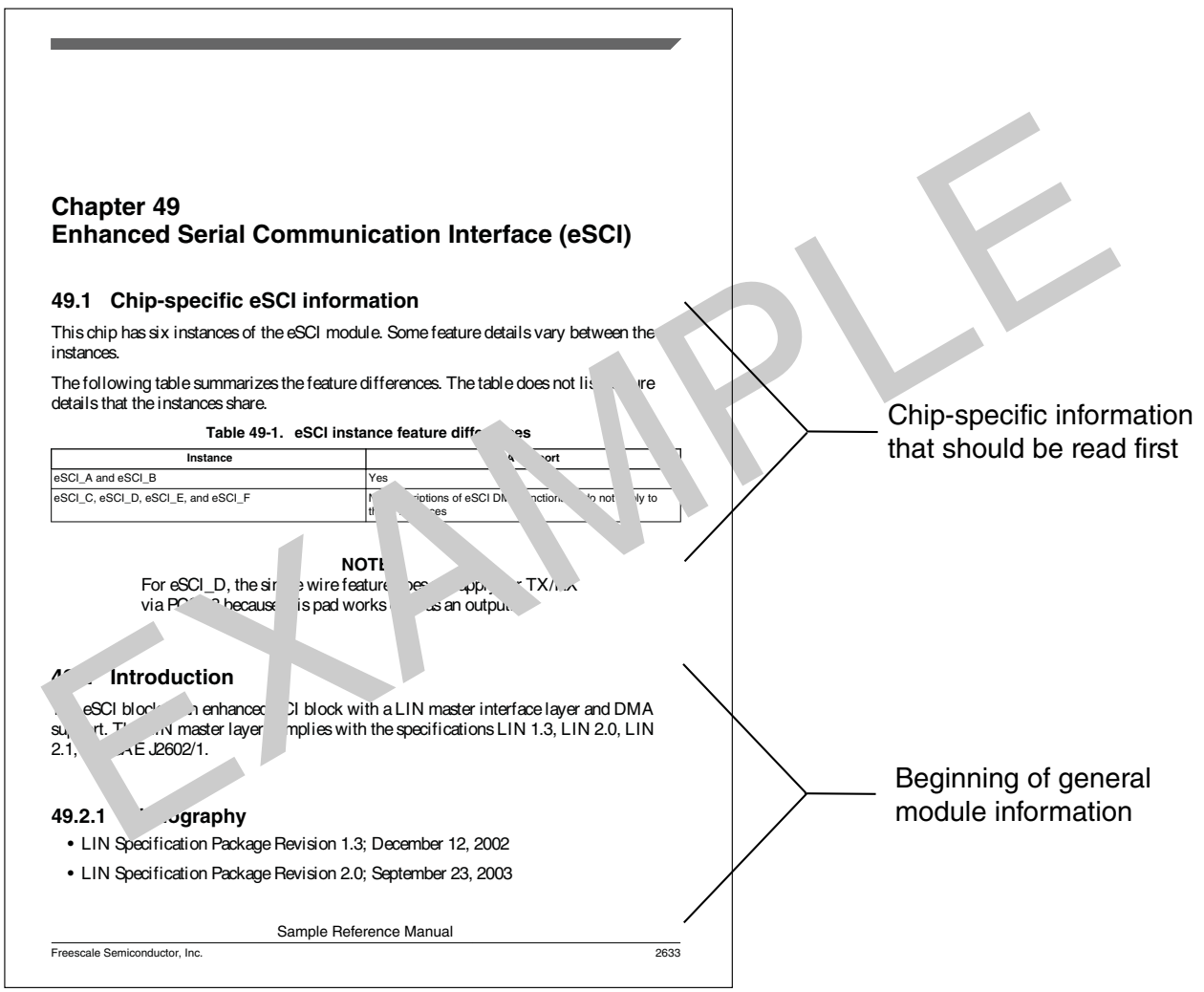
- **Chip-specific:** The first section, *Chip-specific [module name] information*, includes the number of module instances on the chip and possible implementation differences between the module instances, such as differences in FIFO depths or the number of

channels supported. It may also include functional connections between the module instances and other modules. Read this section *first* because its content is crucial to understanding the information in other sections of the chapter.

- **General:** The subsequent sections provide general information about the module, including its signals, registers, and functional description.

NOTE

If there is a conflict between the chip-specific module information (first section) and the general module information (subsequent sections), the chip-specific information supersedes the general information.



Chapter 49
Enhanced Serial Communication Interface (eSCI)

49.1 Chip-specific eSCI information

This chip has six instances of the eSCI module. Some feature details vary between the instances.

The following table summarizes the feature differences. The table does not li re details that the instances share.

Table 49-1. eSCI instance feature diff es

Instance	ort
eSCI_A and eSCI_B	Yes
eSCI_C, eSCI_D, eSCI_E, and eSCI_F	N iptions of eSCI DM nctio o not ly to th ces

NOTE
For eSCI_D, the si e wire feature oes upp TX/RX via PC 2 becaus is pad works as an output

Introduction

eSCI blo n enhanced CI block with a LIN master interface layer and DMA su rt. Th N master layer mplies with the specifications LIN 1.3, LIN 2.0, LIN 2.1, AE J2602/1.

49.2.1 ography

- LIN Specification Package Revision 1.3; December 12, 2002
- LIN Specification Package Revision 2.0; September 23, 2003

Sample Reference Manual
Freescale Semiconductor, Inc. 2633

EXAMPLE

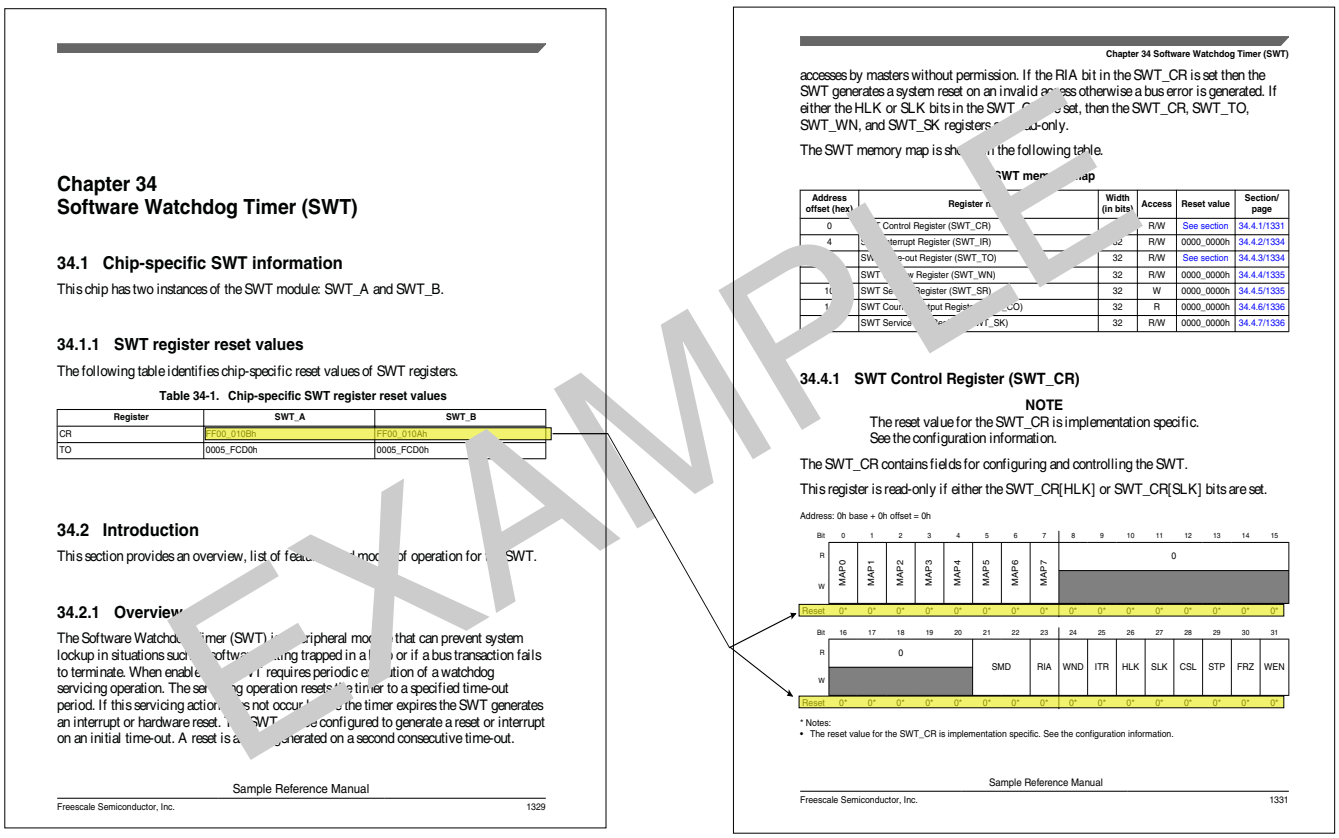
Chip-specific information that should be read first

Beginning of general module information

Figure 1-1. Example: chapter chip-specific information and general module information

1.3.1 Example: chip-specific information that supersedes content in the same chapter

The example below shows chip-specific information that supersedes general module information presented later in the chapter. In this case, the chip-specific register reset values supersede the reset values that appear in the register diagram.



Chapter 34
Software Watchdog Timer (SWT)

34.1 Chip-specific SWT information

This chip has two instances of the SWT module: SWT_A and SWT_B.

34.1.1 SWT register reset values

The following table identifies chip-specific reset values of SWT registers.

Table 34-1. Chip-specific SWT register reset values

Register	SWT_A	SWT_B
CR	FF00_010Bh	FF00_010Ah
TO	0005_FCD0h	0005_FCD0h

34.2 Introduction

This section provides an overview, list of fea... mo... of operation for ... SWT.

34.2.1 Overview

The Software Watchd... imer (SWT) i... ripheral mo... that can prevent system lockup in situations suc... softw... ing trapped in a l... or if a bus transaction fails to terminate. When enable... T requires periodic e... tion of a watchdog servicing operation. The se... g operation resets ... timer to a specified time-out period. If this servicing actio... s not occur ... the timer expires the SWT generates an interrupt or hardware reset. ... SWT ... e configured to generate a reset or interrupt on an initial time-out. A reset is a... enerated on a second consecutive time-out.

Sample Reference Manual

Freescale Semiconductor, Inc. 1329

Chapter 34 Software Watchdog Timer (SWT)

accesses by masters without permission. If the RIA bit in the SWT_CR is set then the SWT generates a system reset on an invalid a... ss otherwise a bus error is generated. If either the HLK or SLK bits in the SWT_C... set, then the SWT_CR, SWT_TO, SWT_WN, and SWT_SK registers ... d-only.

The SWT memory map is sh... n the following table.

SWT mem... ap

Address offset (hex)	Register n...	Width (in bits)	Access	Reset value	Section/ page
0	... Control Register (SWT_CR)		R/W	See section	34.4.1/1331
4	... terrupt Register (SWT_IR)	...2	R/W	0000_0000h	34.4.2/1334
	SW... e-out Register (SWT_TO)	32	R/W	See section	34.4.3/1334
	SWT ... w Register (SWT_WN)	32	R/W	0000_0000h	34.4.4/1335
10	SWT Se... egister (SWT_SR)	32	W	0000_0000h	34.4.5/1335
1...	SWT Coun... tput Regis... CO)	32	R	0000_0000h	34.4.6/1336
	SWT Service ... T_SK)	32	R/W	0000_0000h	34.4.7/1336

34.4.1 SWT Control Register (SWT_CR)

NOTE
The reset value for the SWT_CR is implementation specific.
See the configuration information.

The SWT_CR contains fields for configuring and controlling the SWT.

This register is read-only if either the SWT_CR[HLK] or SWT_CR[SLK] bits are set.

Address: 0h base + 0h offset = 0h

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	MAP0	MAP1	MAP2	MAP3	MAP4	MAP5	MAP6	MAP7	0							
W																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

Bit	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0					SMD	RIA	WND	ITR	HLK	SLK	CSL	STP	FRZ	WEN	
W																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- The reset value for the SWT_CR is implementation specific. See the configuration information.

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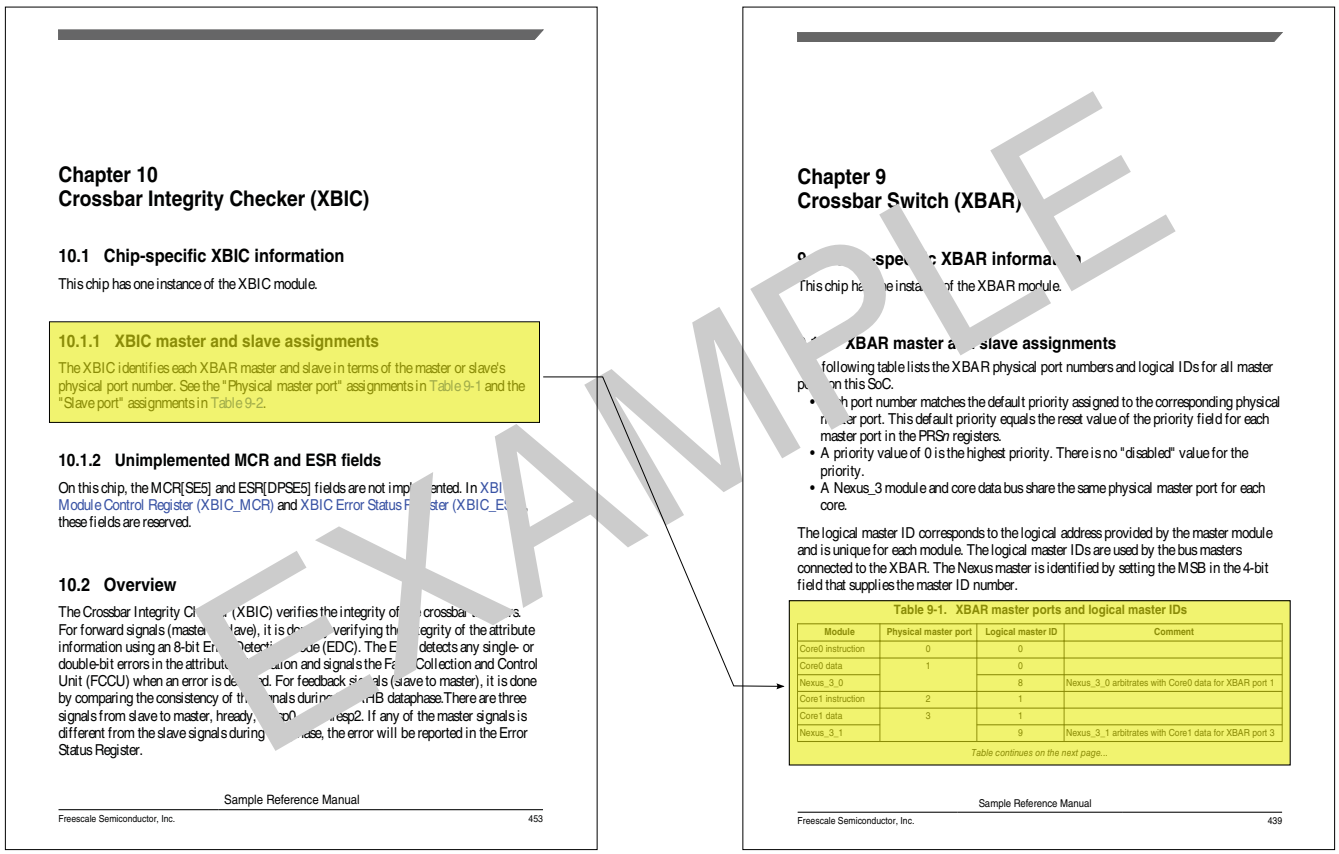
EXAMPLE

Figure 1-2. Example: chip-specific information that supersedes content in the same chapter

1.3.2 Example: chip-specific information that refers to a different chapter

The chip-specific information below refers to another chapter's chip-specific information. In this case, read both sets of chip-specific information before reading further in the chapter.



Chapter 10
Crossbar Integrity Checker (XBIC)

10.1 Chip-specific XBIC information

This chip has one instance of the XBIC module.

10.1.1 XBIC master and slave assignments

The XBIC identifies each XBAR master and slave in terms of the master or slave's physical port number. See the "Physical master port" assignments in Table 9-1 and the "Slave port" assignments in Table 9-2.

10.1.2 Unimplemented MCR and ESR fields

On this chip, the MCR[SE5] and ESR[DPSE5] fields are not implemented. In XBI Module Control Register (XBIC_MCR) and XBIC Error Status Register (XBIC_E these fields are reserved.

10.2 Overview

The Crossbar Integrity Ch (XBIC) verifies the integrity of crossba s. For forward signals (maste lave), it is d verifying th egrity of the attribute information using an 8-bit Er Detecti ue (EDC). The E detects any single- or double-bit errors in the attribut tion and signals the Fa Collection and Control Unit (FCCU) when an error is de d. For feedback si ls (slave to master), it is done by comparing the consistency of th nals duri HB dataphase.There are three signals from slave to master, hready, so0 esp2. If any of the master signals is different from the slave signals during ase, the error will be reported in the Error Status Register.

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Chapter 9
Crossbar Switch (XBAR)

9 -spe c XBAR informa n

This chip ha e insta of the XBAR module.

XBAR master a slave assignments

following table lists the XBAR physical port numbers and logical IDs for all master p on this SoC.

- h port number matches the default priority assigned to the corresponding physical r er port. This default priority equals the reset value of the priority field for each master port in the PRSn registers.
- A priority value of 0 is the highest priority. There is no "disabled" value for the priority.
- A Nexus_3 module and core data bus share the same physical master port for each core.

The logical master ID corresponds to the logical address provided by the master module and is unique for each module. The logical master IDs are used by the bus masters connected to the XBAR. The Nexus master is identified by setting the MSB in the 4-bit field that supplies the master ID number.

Table 9-1. XBAR master ports and logical master IDs

Module	Physical master port	Logical master ID	Comment
Core0 instruction	0	0	
Core0 data	1	0	
Nexus_3_0		8	Nexus_3_0 arbitrates with Core0 data for XBAR port 1
Core1 instruction	2	1	
Core1 data	3	1	
Nexus_3_1		9	Nexus_3_1 arbitrates with Core1 data for XBAR port 3

Table continues on the next page...

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EXAMPLE

Figure 1-3. Example: chip-specific information that refers to a different chapter

1.4 Register descriptions

Module chapters present register information in:

- Memory maps including:
  - Addresses
  - The name and acronym/abbreviation of each register
  - The width of each register (in bits)
  - Each register's reset value
  - The page number on which each register is described
- Register figures
- Field-description tables
- Associated text

The register figures show the field structure using the conventions in the following figure.

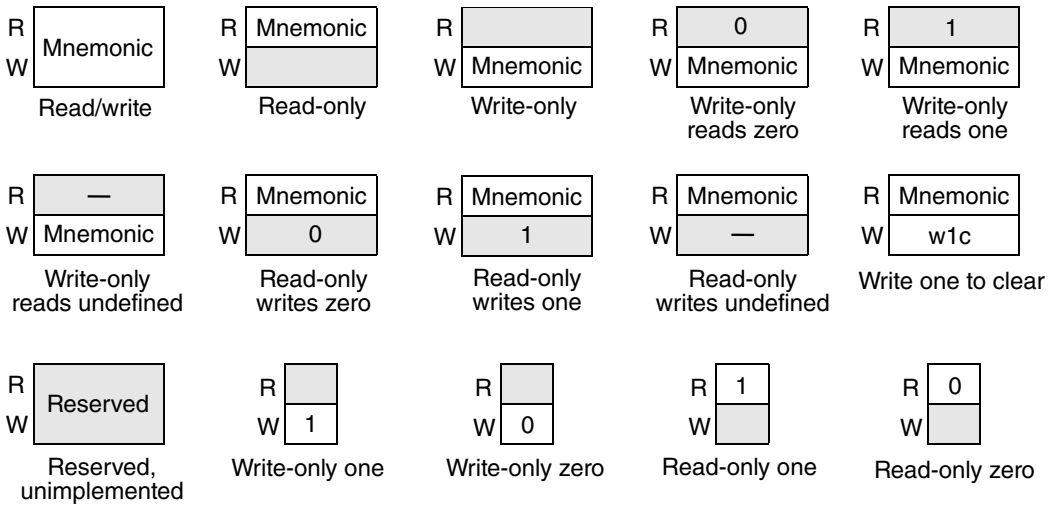


Figure 1-4. Register figure conventions

1.5 Conventions

1.5.1 Numbering systems

The following suffixes identify different numbering systems:

This suffix	Identifies a
b	Binary number. For example, the binary equivalent of the number 5 is written 101b. In some cases, binary numbers are shown with the prefix *0b*.
d	Decimal number. Decimal numbers are followed by this suffix only when the possibility of confusion exists. In general, decimal numbers are shown without a suffix.
h	Hexadecimal number. For example, the hexadecimal equivalent of the number 60 is written 3Ch. In some cases, hexadecimal numbers are shown with the prefix *0x*.

1.5.2 Typographic notation

The following typographic notation is used throughout this document:

Example	Description
placeholder, x	Items in italics are placeholders for information that you provide. Italicized text is also used for the titles of publications and for emphasis. Plain lowercase letters are also used as placeholders for single letters and numbers.
`code`	Fixed-width type indicates text that must be typed exactly as shown. It is used for instruction mnemonics, directives, symbols, subcommands, parameters, and operators. Fixed-width type

Table continues on the next page...

Example	Description
	is also used for example code. Instruction mnemonics and directives in text and tables are shown in all caps; for example, BSR.
SR[SCM]	A mnemonic in brackets represents a named field in a register. This example refers to the Scaling Mode (SCM) field in the Status Register (SR).
REVNO[6:4], XAD[7:0]	Numbers in brackets and separated by a colon represent either: • A subset of a register's named field For example, REVNO[6:4] refers to bits 6–4 that are part of the COREREV field that occupies bits 6–0 of the REVNO register. • A continuous range of individual signals of a bus For example, XAD[7:0] refers to signals 7–0 of the XAD bus.

1.5.3 Special terms

The following terms have special meanings:

Term	Meaning
asserted	Refers to the state of a signal as follows: • An active-high signal is asserted when high (1). • An active-low signal is asserted when low (0).
deasserted	Refers to the state of a signal as follows: • An active-high signal is deasserted when low (0). • An active-low signal is deasserted when high (1). In some cases, deasserted signals are described as *negated*.
reserved	Refers to a memory space, register, field, or programming setting. Writes to a reserved location can result in unpredictable functionality or behavior. • Do not modify the default value of a reserved programming setting, such as the reset value of a reserved register field. • Consider undefined locations in memory to be reserved.
w1c	Write 1 to clear: Refers to a register bitfield that must be written as 1 to be "cleared."

Chapter 2
Introduction

2.1 Overview

This chapter provides high-level descriptions of the modules available on the devices covered by this document.

2.2 Block Diagram

The below figure shows a top-level block diagram of the device.

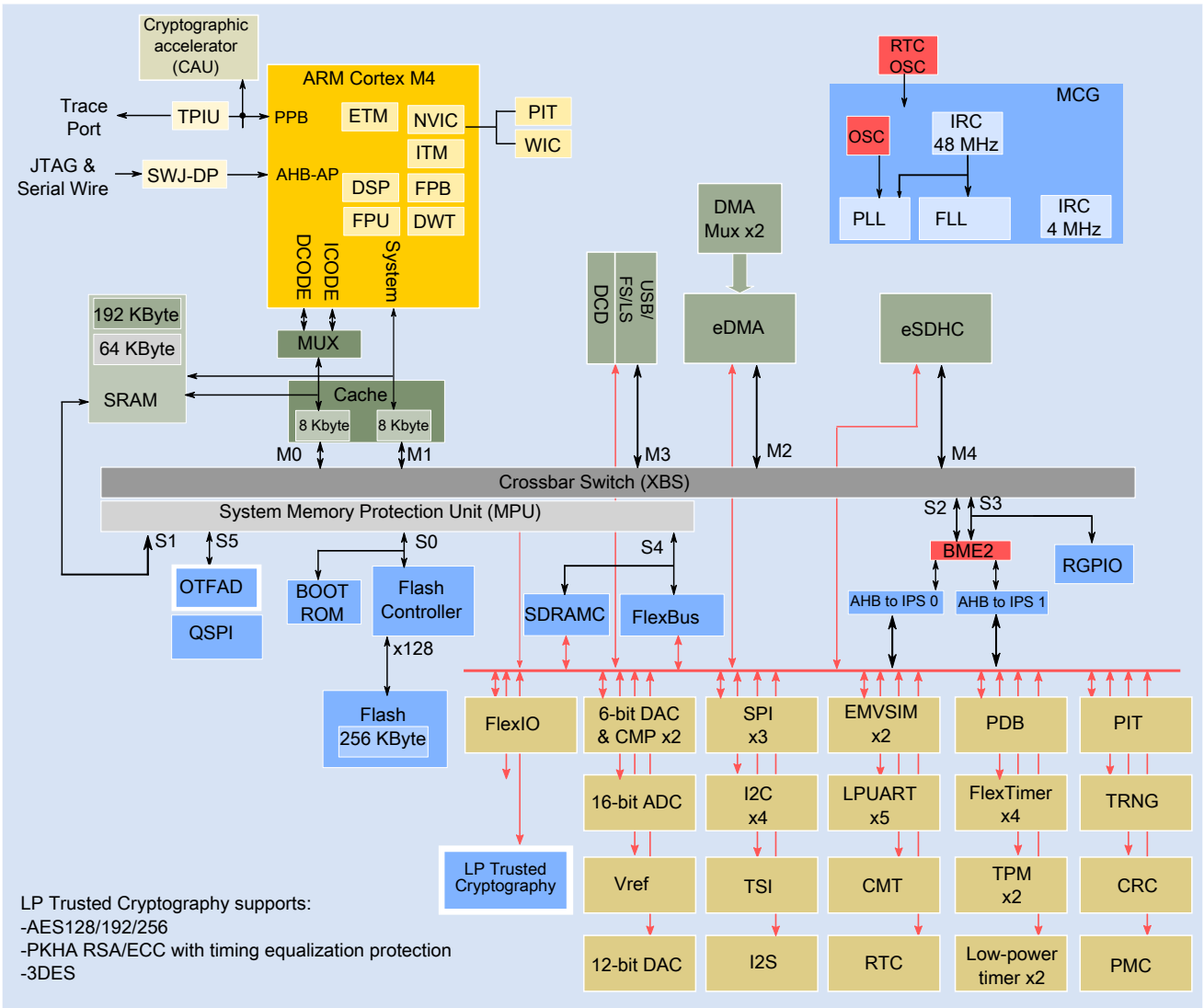


Figure 2-1. K82 Block Diagram

2.3 Module Functional Categories

The modules on this device are grouped into functional categories. The following sections describe the modules assigned to each category in more detail.

Table 2-1. Module functional categories

Module category	Description
ARM® Cortex®-M4 based core	• 32-bit MCU core from ARM's Cortex-M based class adding DSP instructions and single-precision floating point unit based on ARMv7 architecture with 8 kB of cache in some devices
System	• System integration module

Table continues on the next page...

Table 2-1. Module functional categories (continued)

Module category	Description
	• Power management and mode controllers • Multiple power modes available based on high speed run, run, wait, stop, and power-down modes • Low-leakage wakeup unit • Miscellaneous control module • Crossbar switch • Memory protection unit • Peripheral bridge • Bit Manipulation Engine (BME2) • Direct memory access (DMA) controller with multiplexer to increase available DMA requests. DMA can handle transfers in VLPS mode • External watchdog monitor • Watchdog

Memories	• Internal memories include:
	  • Program flash memory
	  • SRAM
	  • Cache memory
	• SDRAM memory controller
	• 32-byte System Register File
	• 128-byte VBAT register file
	• Flexbus
	• Quad Serial Peripheral Interface
	• 32 KB Boot ROM

Clocks	• Multiple clock generation options available from internally- and externally-generated clocks • System oscillator to provide clock source for the MCU • RTC oscillator to provide clock source for the RTC • 48 MHz Internal Reference Clock
Security	• Cyclic Redundancy Check module for error detection • Hardware encryption, along with a random number generator • On-the-Fly AES Decryption Engine (OTFAD)
Analog	• High speed analog-to-digital converter • Comparator • Digital-to-analog converter • Internal voltage reference • Bandgap voltage reference
Timers	• Programmable delay block • FlexTimers • Low Power Timer/PWM • Periodic interrupt timer • Low power timer • Carrier modulator transmitter • Independent real time clock

Communications	• USB FS OTG controller
	  • Built-in FS/LS transceiver
	  • USB device charger detect
	• USB voltage regulator
	• Serial peripheral interface (SPI)
	• Inter-integrated circuit (I^2C)
	• Low Power Universal Asynchronous Receiver Transmitter (LPUART)
	• Secured Digital host controller
	• Integrated interchip sound (I^2S)

Table continues on the next page...

Table 2-1. Module functional categories (continued)

Module category	Description
	• FlexIO • EMVSIM (ISO-7816) Module
Human-Machine Interfaces (HMI)	• General purpose input/output controller • Capacitive touch sense input interface enabled in hardware

2.3.1 ARM® Cortex®-M4 Core Modules

The following core modules are available on this device.

Table 2-2. Core modules

Module	Description
ARM Cortex-M4	The ARM Cortex-M4 is a member of the Cortex M Series of processors targeting microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments. The Cortex M4 processor is based on the ARMv7 Architecture and Thumb®-2 ISA and is upward compatible with the Cortex M3, Cortex M1, and Cortex M0 architectures. Cortex M4 improvements include an ARMv7 Thumb-2 DSP (ported from the ARMv7-A/R profile architectures) providing 32-bit instructions with SIMD (single instruction multiple data) DSP style multiply-accumulates and saturating arithmetic.
Floating point unit (FPU)	A single-precision floating point unit (FPU) that is compliant to the *IEEE Standard for Floating-Point Arithmetic* (IEEE 754).
NVIC	The ARMv7-M exception model and nested-vectored interrupt controller (NVIC) implement a relocatable vector table supporting many external interrupts, a single non-maskable interrupt (NMI), and priority levels. The NVIC replaces shadow registers with equivalent system and simplified programming. The NVIC contains the address of the function to execute for a particular handler. The address is fetched via the instruction port allowing parallel register stacking and look-up. The first sixteen entries are allocated to ARM internal sources with the others mapping to MCU-defined interrupts.
AWIC	The primary function of the Asynchronous Wake-up Interrupt Controller (AWIC) is to detect asynchronous wake-up events in stop modes and signal to clock control logic to resume system clocking. After clock restart, the NVIC observes the pending interrupt and performs the normal interrupt or event processing.
Debug interfaces	Most of this device's debug hardware is based on the ARM CoreSight™ architecture. Four debug interfaces are supported: • IEEE 1149.1 JTAG • IEEE 1149.7 JTAG (cJTAG) • Serial Wire Debug (SWD) • ARM Real-Time Trace Interface

2.3.2 System Modules

The following system modules are available on this device.

Table 2-3. System modules

Module	Description
System integration module (SIM)	The SIM includes integration logic and several module configuration settings.
System mode controller	The SMC provides control and protection on entry and exit to each power mode, control for the Power management controller (PMC), and reset entry and exit for the complete MCU.
Power management controller (PMC)	The PMC provides the user with multiple power options. different modes are supported that allow the user to optimize power consumption for the level of functionality needed. Includes power-on-reset (POR) and integrated low voltage detect (LVD) with reset (brownout) capability and selectable LVD trip points.
Low-leakage wakeup unit (LLWU)	The LLWU module allows the device to wake from low leakage power modes (LLS and VLLS) through various internal peripheral and external pin sources.
Miscellaneous control module (MCM)	The MCM includes integration logic
Crossbar switch (XBS)	The XBS connects bus masters and bus slaves, allowing all bus masters to access different bus slaves simultaneously and providing arbitration among the bus masters when they access the same slave.
Freescale Memory protection unit (MPU)	The MPU provides memory protection and task isolation. It concurrently monitors all bus master transactions for the slave connections.
Peripheral bridges	The peripheral bridge converts the crossbar switch interface to an interface to access a majority of peripherals on the device.
DMA multiplexer (DMAMUX)	The DMA multiplexer selects from many DMA requests down to a smaller number for the DMA controller.
Direct memory access (DMA) controller	The DMA controller provides programmable channels with transfer control descriptors for data movement via dual-address transfers for 8-, 16-, 32- and 128-bit data values.
External watchdog monitor (EWM)	The EWM is a redundant mechanism to the software watchdog module that monitors both internal and external system operation for fail conditions.
Software watchdog (WDOG)	The WDOG monitors internal system operation and forces a reset in case of failure. It can run from an independent 1 KHz low power oscillator with a programmable refresh window to detect deviations in program flow or system frequency.
Bit Manipulation Engine2 (BME2)	The second-generation BME2 provides hardware support for atomic read-modify-write operations to the peripheral address space.

2.3.3 Memories and Memory Interfaces

The following memories and memory interfaces are available on this device.

Table 2-4. Memories and memory interfaces

Module	Description
Flash memory	Program flash memory — non-volatile flash memory that can execute program code
Flash memory controller	Manages the interface between the device and the on-chip flash memory.
SRAM	Internal system RAM. Partial SRAM kept powered in LLS2 and VLLS2 low leakage mode.

Table continues on the next page...

Table 2-4. Memories and memory interfaces (continued)

Module	Description
SRAM controller	Manages simultaneous accesses to system RAM by multiple master peripherals and core.
Local memory controller	Manages simultaneous accesses to system RAM by multiple master peripherals and core. Controls cache which improves system performance by providing single-cycle access to the instruction and data pipelines.
System register file	32-byte register file that is accessible during all power modes and is powered by VDD.
VBAT register file	128-byte register file that is accessible during all power modes and is powered by VBAT.
FlexBus	External bus interface with multiple independent, user-programmable chip-select signals that can interface with external SRAM, PROM, EPROM, EEPROM, flash, and other peripherals via 8-, 16- and 32-bit port sizes. Configurations include multiplexed or non-multiplexed address and data buses using 8-bit, 16-bit, 32-bit, and 16-byte line-sized transfers.
SDRAM Controller	Interface to store and retrieve data from an external SDRAM. Supports glue-less interface to SDR DRAM devices with up to 32-bit wide data and 16MB per chip select. Note that not all packages or pinouts support 32-bit wide data. See Signal Multiplexing Introduction for more information.
Quad Serial Peripheral Interface	The Quad Serial Peripheral Interface (QuadSPI) block acts as an interface to one single or two external serial flash devices, each with up toeight bidirectional data lines.
32 KB Boot ROM	Provisions the internal flash or QSPI with an embedded firmware image during manufacturing, or at any time during the life of the device. It does this by acting as a slave device, and listening to various peripheral ports where a master can start communication

2.3.4 Clocks

The following clock modules are available on this device.

Table 2-5. Clock modules

Module	Description
Multi-clock generator (MCG)	The MCG provides several clock sources for the MCU that include: • Phase-locked loop (PLL) — Voltage-controlled oscillator (VCO) • Frequency-locked loop (FLL) — Digitally-controlled oscillator (DCO) • Internal reference clocks — Can be used as a clock source for other on-chip peripherals
48 MHz Internal Reference Clock (IRC48M)	The IRC48M provides an internally generated clock source. Clock Recovery circuitry uses the incoming USB data stream to adjust the internal oscillator and enables the internal oscillator to meet the requirements for USB clock tolerance.
System oscillator	The system oscillator, in conjunction with an external crystal or resonator, generates a reference clock for the MCU.

Table continues on the next page...

Table 2-5. Clock modules (continued)

Module	Description
Real-time clock oscillator	The RTC oscillator has an independent power supply and supports a 32 kHz crystal oscillator to feed the RTC clock. Optionally, the RTC oscillator can replace the system oscillator as the main oscillator source.

2.3.5 Security and Integrity modules

The following security and integrity modules are available on this device:

Table 2-6. Security and integrity modules

Module	Description
Cryptographic acceleration unit (CAU)	Supports the following algorithms: • DES • 3-DES • AES • SHA-1 and SHA-256 • MD5 Via simple C calls to optimized security functions provided by Freescale.
LP Trusted Cryptography (LTC)	LTC is hardware block that supports the following algorithms: Supports DES, 3DES, AES, MD5 algorithms
True Random number generator (TRNG)	A hardware entropy source which can be used to seed a software random number generator.
Cyclic Redundancy Check (CRC)	Hardware CRC generator circuit using 16/32-bit shift register. Error detection for all single, double, odd, and most multi-bit errors, programmable initial seed value, and optional feature to transpose input data and CRC result via transpose register.
On-the-Fly AES Decryption Engine (OTFAD)	Hardware module supporting AES128 counter mode decryptions on external flash data fetched by the QuadSPI.

2.3.6 Analog modules

The following analog modules are available on this device:

Table 2-7. Analog modules

Module	Description
16-bit analog-to-digital converters (ADC)	16-bit successive-approximation ADC
Analog comparators	Compares two analog input voltages across the full range of the supply voltage.
6-bit digital-to-analog converters (DAC)	64-tap resistor ladder network which provides a selectable voltage reference for applications where voltage reference is needed.
12-bit digital-to-analog converters (DAC)	Low-power general-purpose DAC, whose output can be placed on an external pin or set as one of the inputs to the analog comparator or ADC.

Table continues on the next page...

Table 2-7. Analog modules (continued)

Module	Description
Voltage reference (VREF)	Supplies an accurate voltage output that is trimmable in 0.5 mV steps. The VREF can be used in medical applications, such as glucose meters, to provide a reference voltage to biosensors or as a reference to analog peripherals, such as the ADC, DAC, or CMP.

2.3.7 Timer modules

The following timer modules are available on this device:

Table 2-8. Timer modules

Module	Description
Programmable delay block (PDB)	• 16-bit resolution • 3-bit prescaler • Positive transition of trigger event signal initiates the counter • Supports two triggered delay output signals, each with an independently-controlled delay from the trigger event • Outputs can be OR'd together to schedule two conversions from one input trigger event and can schedule precise edge placement for a pulsed output. This feature is used to generate the control signal for the CMP windowing feature and output to a package pin if needed for applications, such as critical conductive mode power factor correction. • Continuous-pulse output or single-shot mode supported, each output is independently enabled, with possible trigger events • Supports bypass mode • Supports DMA
Flexible timer modules (FTM)	• Selectable FTM source clock, programmable prescaler • 16-bit counter supporting free-running or initial/final value, and counting is up or up-down • Input capture, output compare, and edge-aligned and center-aligned PWM modes • Operation of FTM channels as pairs with equal outputs, pairs with complimentary outputs, or independent channels with independent outputs • Deadtime insertion is available for each complementary pair • Generation of hardware triggers • Software control of PWM outputs • Up to 4 fault inputs for global fault control • Configurable channel polarity • Programmable interrupt on input capture, reference compare, overflowed counter, or detected fault condition • Quadrature decoder with input filters, relative position counting, and interrupt on position count or capture of position count on external event • DMA support for FTM events
Low Power TPM (TPM)	• Two channel timer which supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. • The counter, compare and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes. • DMA support

Table continues on the next page...

Table 2-8. Timer modules (continued)

Module	Description
Periodic interrupt timers (PIT)	• Four general purpose interrupt timers • Interrupt timers for triggering ADC conversions • 32-bit counter resolution • DMA support
Low-power timer (LPTimer)	• Selectable clock for prescaler/glitch filter of 1 kHz (internal LPO), 32.768 kHz (external crystal), or internal reference clock • Configurable Glitch Filter or Prescaler with 16-bit counter • 16-bit time or pulse counter with compare • Interrupt generated on Timer Compare • Hardware trigger generated on Timer Compare

Carrier modulator timer (CMT)	• Four CMT modes of operation:
	  • Time with independent control of high and low times
	  • Baseband
	  • Frequency shift key (FSK)
	  • Direct software control of CMT_IRO pin
	• Extended space operation in time, baseband, and FSK modes
	• Selectable input clock divider
	• Interrupt on end of cycle with the ability to disable CMT_IRO pin and use as timer interrupt
	• DMA support

Real-time clock (RTC)	• Independent power supply, POR, and 32 kHz Crystal Oscillator • 32-bit seconds counter with 32-bit Alarm • 16-bit Prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm

2.3.8 Communication interfaces

The following communication interfaces are available on this device:

Table 2-9. Communication modules

Module	Description
FlexIO	Supports a wide range of protocols including, but not limited to: • UART • I2C • SPI • I2S • Camera IF • LCD RGB • PWM / Waveform generation Functions in STOP/VLPS modes DMA support
USB OTG (low-/full-speed)	USB 2.0 compliant module with support for host, device, and On-The-Go modes. Includes an on-chip transceiver for full and low speeds.

Table continues on the next page...

Table 2-9. Communication modules (continued)

Module	Description
USB Device Charger Detect (USBDCD)	The USBDCD monitors the USB data lines to detect a smart charger meeting the USB Battery Charging Specification Rev1.2. This information allows the MCU to better manage the battery charging IC in a portable device.
USB voltage regulator	Up to 5 V regulator input typically provided by USB VBUS power with 3.3 V regulated output that powers on-chip USB subsystem, capable of sourcing 120 mA to external board components.
Serial peripheral interface (SPI)	Synchronous serial bus for communication to an external device
Inter-Integrated Circuit (I^2C)	Allows communication between a number of devices. Also supports the System Management Bus (SMBus) Specification, version 2.
EMVSIM (ISO-7816) Module	Allows communication on ISO-7816
Low Power Universal asynchronous receiver/transmitter (LPUART)	Asynchronous serial bus communication interface with programmable 8- or 9-bit data format
Secure Digital host controller (SDHC)	Interface between the host system and the SD, SDIO, MMC, or CE-ATA cards. The SDHC acts as a bridge, passing host bus transactions to the cards by sending commands and performing data accesses to/from the cards. It handles the SD, SDIO, MMC, and CE-ATA protocols at the transmission level.
I^2S	The I^2S is a full-duplex, serial port that allows the chip to communicate with a variety of serial devices, such as standard codecs, digital signal processors (DSPs), microprocessors, peripherals, and audio codecs that implement the inter-IC sound bus (I^2S) and the Intel® AC97 standards

2.3.9 Human-machine interfaces

The following human-machine interfaces (HMI) are available on this device:

Table 2-10. HMI modules

Module	Description
General purpose input/output (GPIO)	All general purpose input or output (GPIO) pins are capable of interrupt and DMA request generation. Configurable slew rate on all output pins. High drive configurable option on 8 pins (PTB0, PTB1, PTD4, PTD5, PTD6, PTD7, PTC3, and PTC4).
Capacitive touch sense input (TSI)	Contains up to 16 channel inputs for capacitive touch sensing applications. Operation is available in low-power modes via interrupts.

2.4 Orderable part numbers

The following table summarizes the part numbers of the devices covered by this document.

Table 2-11. Orderable part numbers summary

Freescale part number	CPU frequency	Pin count	Package	Total flash memory	Program flash	SRAM	GPIO
MK82FN256VDC15	150 MHz	121	XFBGA	256 kB	256 kB	256 kB	87
MK82FN256CAx15[1]	150 MHz	121	WLCSP	256 kB	256 kB	256 kB	87
MK82FN256VLL15	150 MHz	100	LQFP	256 kB	256 kB	256 kB	66
MK82FN256VLQ15[2]	150 MHz	144	LQFP	256 kB	256 kB	256 kB	102

1. The 121-pin WLCSP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Please visit freescale.com/KPYW for more details.
2. The 144-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Please visit freescale.com/KPYW for more details.

Chapter 3
Core Overview

3.1 Introduction

The ARM Cortex M4 is a member of the Cortex M Series of processors targeting microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments. The Cortex M4 processor is based on the ARMv7 Architecture and Thumb®-2 ISA and is upward compatible with the Cortex M3, Cortex M1, and Cortex M0{+} architectures. Cortex M4 improvements include an ARMv7 Thumb-2 DSP (ported from the ARMv7-A/R profile architectures) providing 32-bit instructions with SIMD (single instruction multiple data) DSP style multiply-accumulates and saturating arithmetic. There are approximately 90 instructions added to the previous ARMv7-M instruction set.

3.1.1 Buses, interconnects, and interfaces

The ARM Cortex-M4 core has four buses as described in the following table.

Bus name	Description
Instruction code (ICODE) bus	The ICODE and DCODE buses are muxed. This muxed bus is called the CODE bus and is connected to the crossbar switch via a single master port. In addition, the CODE bus is also tightly coupled to the lower half of the system RAM (SRAM_L).
Data code (DCODE) bus	
System bus	The system bus is connected to a separate master port on the crossbar. In addition, the system bus is tightly coupled to the upper half system RAM (SRAM_U).
Private peripheral (PPB) bus	The PPB provides access to these modules: • ARM modules such as the NVIC, ETM, ITM, DWT, FBP, and ROM table • Freescale Miscellaneous Control Module (MCM) • Memory-Mapped Cryptographic Acceleration Unit (MMCAU)

3.1.2 System Tick Timer

The System Tick Timer's clock source is always the core clock, FCLK. This results in the following:

- The CLKSOURCE bit in SysTick Control and Status register is always set to select the core clock.
- Because the timing reference (FCLK) is a variable frequency, the TENMS bit in the SysTick Calibration Value Register is always zero.
- The NOREF bit in SysTick Calibration Value Register is always set, implying that FCLK is the only available source of reference timing.

3.1.3 Debug facilities

This device has extensive debug capabilities including run control and tracing capabilities. The standard ARM debug port that supports JTAG and SWD interfaces. Also the cJTAG interface is supported on this device.

3.1.4 Caches

This device includes two 8 KB of combined data/ instructions caches to minimize the performance impact of memory access latencies: one for the system bus and one for I/D bus.

Features of each cache are:

- 2-way set associative
- 4 word lines
- Lines can be individually flushed
- Entire cache can be flushed at once

3.1.4.1 Low Power

The caches are powered down in LLS and VLLSx modes. The caches need to be flushed before being powered down. This affects the time it takes for the system to go into the new mode but not the wakeup time.

3.1.4.2 Control

For control purposes the cache can be in one of these states:

1. Write Back /Write Allocate (WBWA)

2. Write Through (WT)
3. Non-Cachable (NC)

For each defined region there are 2 bits allocated in the control register that determines the cache state for the memory region associated with this section. The user can only "lower" the cache attribute, given the fixed relationship of WBWA > WT > NC - so, you can demote a WBWA region to either WT or NC, you can demote a WT space to NC. In order to change the state upwards a system reset is required.

The 1GB space allocated to the DRAM and FlexBus is split in 16 MB regions and 2 bits assigned to the control state of each region. A total of 128 bits, distributed in four 32-bit registers is used for this control.

3.1.5 Core privilege levels

The ARM documentation uses different terms than this document to distinguish between privilege levels.

If you see this term...	it also means this term...
Privileged	Supervisor
Unprivileged or user	User

3.2 Interrupt priority levels

This device supports 16 priority levels for interrupts. Therefore, in the NVIC each source in the IPR registers contains 4 bits. For example, IPR0 is shown below:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IRQ3				0	0	0	0	IRQ2				0	0	0	0	IRQ1				0	0	0	0	IRQ0				0	0	0	0
W																																

3.3 Non-maskable interrupt

The non-maskable interrupt request to the NVIC is controlled by the external $\overline{\text{NMI}}$ signal. The pin the $\overline{\text{NMI}}$ signal is multiplexed on, must be configured for the $\overline{\text{NMI}}$ function to generate the non-maskable interrupt request.

3.4 Interrupt channel assignments

The interrupt source assignments are defined in the following table.

- Vector number — the value stored on the stack when an interrupt is serviced.
- IRQ number — non-core interrupt source count, which is the vector number minus 16.

The IRQ number is used within ARM's NVIC documentation.

Table 3-2. Interrupt vector assignments

Address	Vector	IRQ[1]	NVIC non-IPR register number [2]	NVIC IPR register number [3]	Source module	Source description
ARM Core System Handler Vectors						
0x0000_0000	0	–	–	–	ARM core	Initial Stack Pointer
0x0000_0004	1	–	–	–	ARM core	Initial Program Counter
0x0000_0008	2	–	–	–	ARM core	Non-maskable Interrupt (NMI)
0x0000_000C	3	–	–	–	ARM core	Hard Fault
0x0000_0010	4	–	–	–	ARM core	MemManage Fault
0x0000_0014	5	–	–	–	ARM core	Bus Fault
0x0000_0018	6	–	–	–	ARM core	Usage Fault
0x0000_001C	7	–	–	–	—	—
0x0000_0020	8	–	–	–	—	—
0x0000_0024	9	–	–	–	—	—
0x0000_0028	10	–	–	–	—	—
0x0000_002C	11	–	–	–	ARM core	Supervisor call (SVCall)
0x0000_0030	12	–	–	–	ARM core	Debug Monitor
0x0000_0034	13	–	–	–	—	—
0x0000_0038	14	–	–	–	ARM core	Pendable request for system service (PendableSrvReq)
0x0000_003C	15	–	–	–	ARM core	System tick timer (SysTick)
Non-Core Vectors						
0x0000_0040	16	0	0	0	DMA	DMA channel 0, 16 transfer complete
0x0000_0044	17	1	0	0	DMA	DMA channel 1, 17 transfer complete
0x0000_0048	18	2	0	0	DMA	DMA channel 2, 18 transfer complete
0x0000_004C	19	3	0	0	DMA	DMA channel 3, 19 transfer complete
0x0000_0050	20	4	0	1	DMA	DMA channel 4, 20 transfer complete
0x0000_0054	21	5	0	1	DMA	DMA channel 5, 21 transfer complete
0x0000_0058	22	6	0	1	DMA	DMA channel 6, 22 transfer complete

Table continues on the next page...

Table 3-2. Interrupt vector assignments (continued)

Address	Vector	IRQ[1]	NVIC non-IPR register number [2]	NVIC IPR register number [3]	Source module	Source description
0x0000_005C	23	7	0	1	DMA	DMA channel 7, 23 transfer complete
0x0000_0060	24	8	0	2	DMA	DMA channel 8, 24 transfer complete
0x0000_0064	25	9	0	2	DMA	DMA channel 9, 25 transfer complete
0x0000_0068	26	10	0	2	DMA	DMA channel 10, 26 transfer complete
0x0000_006C	27	11	0	2	DMA	DMA channel 11, 27 transfer complete
0x0000_0070	28	12	0	3	DMA	DMA channel 12, 28 transfer complete
0x0000_0074	29	13	0	3	DMA	DMA channel 13, 29 transfer complete
0x0000_0078	30	14	0	3	DMA	DMA channel 14, 30 transfer complete
0x0000_007C	31	15	0	3	DMA	DMA channel 15, 31 transfer complete
0x0000_0080	32	16	0	4	DMA	DMA error interrupt channels 0-31
0x0000_0084	33	17	0	4	MCM or RDC	MCM or RDC interrupt
0x0000_0088	34	18	0	4	Flash memory	Command complete
0x0000_008C	35	19	0	4	Flash memory	Read collision
0x0000_0090	36	20	0	5	Mode Controller	Low-voltage detect, low-voltage warning, high-voltage detect
0x0000_0094	37	21	0	5	LLWU	Low Leakage Wakeup NOTE: The LLWU interrupt must not be masked by the interrupt controller to avoid a scenario where the system does not fully exit stop mode on an LLS recovery.
0x0000_0098	38	22	0	5	WDOG or EWM	Both watchdog modules share this interrupt
0x0000_009C	39	23	0	5	TRNG	True Randon Number Generator
0x0000_00A0	40	24	0	6	I2C0	—
0x0000_00A4	41	25	0	6	I2C1	—
0x0000_00A8	42	26	0	6	SPI0	Single interrupt vector for all sources
0x0000_00AC	43	27	0	6	SPI1	Single interrupt vector for all sources
0x0000_00B0	44	28	0	7	I2S0	Transmit
0x0000_00B4	45	29	0	7	I2S0	Receive
0x0000_00B8	46	30	0	7	LPUART0	Single interrupt vector for LPUART sources
0x0000_00BC	47	31	0	7	LPUART1	Single interrupt vector for LPUART sources
0x0000_00C0	48	32	1	8	LPUART2	Single interrupt vector for LPUART sources
0x0000_00C4	49	33	1	8	LPUART3	Single interrupt vector for LPUART sources
0x0000_00C8	50	34	1	8	LPUART4	Single interrupt vector for LPUART sources
0x0000_00CC	51	35	1	8	—	—

Table continues on the next page...

Table 3-2. Interrupt vector assignments (continued)

Address	Vector	IRQ[1]	NVIC non-IPR register number [2]	NVIC IPR register number [3]	Source module	Source description
0x0000_00D0	52	36	1	9	— > >	—
0x0000_00D4	53	37	1	9	EMVSIM0	EMVSIM single interrupt source
0x0000_00D8	54	38	1	9	EMVSIM1	EMVSIM single interrupt source
0x0000_00DC	55	39	1	9	ADC0	—
0x0000_00E0	56	40	1	10	CMP0	—
0x0000_00E4	57	41	1	10	CMP1	—
0x0000_00E8	58	42	1	10	FTM0	Single interrupt vector for all sources
0x0000_00EC	59	43	1	10	FTM1	Single interrupt vector for all sources
0x0000_00F0	60	44	1	11	FTM2	Single interrupt vector for all sources
0x0000_00F4	61	45	1	11	CMT	—
0x0000_00F8	62	46	1	11	RTC	Alarm interrupt
0x0000_00FC	63	47	1	11	RTC	Seconds interrupt
0x0000_0100	64	48	1	12	PIT	Channel 0
0x0000_0104	65	49	1	12	PIT	Channel 1
0x0000_0108	66	50	1	12	PIT	Channel 2
0x0000_010C	67	51	1	12	PIT	Channel 3
0x0000_0110	68	52	1	13	PDB	—
0x0000_0114	69	53	1	13	USBFS OTG	—
0x0000_0118	70	54	1	13	USBFS Charger Detect	—
0x0000_011C	71	55	1	13	—	
0x0000_0120	72	56	1	14	DAC0	—
0x0000_0124	73	57	1	14	MCG	—
0x0000_0128	74	58	1	14	Low Power Timer	Single interrupt vector for LPTMR0 and LPTMR1
0x0000_012C	75	59	1	14	Port control module	Pin detect (Port A)
0x0000_0130	76	60	1	15	Port control module	Pin detect (Port B)
0x0000_0134	77	61	1	15	Port control module	Pin detect (Port C)
0x0000_0138	78	62	1	15	Port control module	Pin detect (Port D)
0x0000_013C	79	63	1	15	Port control module	Pin detect (Port E)
0x0000_0140	80	64	2	16	Software	Software interrupt [4]
0x0000_0144	81	65	2	16	SPI2	Single interrupt vector for all sources
0x0000_0148	82	66	2	16	—	—
0x0000_014C	83	67	2	16	—	—
0x0000_0150	84	68	2	17	—	—
0x0000_0154	85	69	2	17	—	—
0x0000_0158	86	70	2	17	FlexIO	—

Table continues on the next page...

Table 3-2. Interrupt vector assignments (continued)

Address	Vector	IRQ[1]	NVIC non-IPR register number [2]	NVIC IPR register number [3]	Source module	Source description
0x0000_015C	87	71	2	17	FTM3	Single interrupt vector for all sources
0x0000_0160	88	72	2	18	—	—
0x0000_0164	89	73	2	18	—	—
0x0000_0168	90	74	2	18	I2C2	—
0x0000_016C	91	75	2	18	—	—
0x0000_0170	92	76	2	19	—	—
0x0000_0174	93	77	2	19	—	—
0x0000_0178	94	78	2	19	—	—
0x0000_017C	95	79	2	19	—	—
0x0000_0180	96	80	2	20	—	—
0x0000_0184	97	81	2	20	SDHC	—
0x0000_0188	98	82	2	20	—	—
0x0000_018C	99	83	2	20	—	—
0x0000_0190	100	84	2	21	—	—
0x0000_0194	101	85	2	21	—	—
0x0000_0198	102	86	2	21	—	—
0x0000_019C	103	87	2	21	TSI0	—
0x0000_01A0	104	88	2	22	TPM1	—
0x0000_01A4	105	89	2	22	TPM2	—
0x0000_01A8	106	90	2	22	—	—
0x0000_01AC	107	91	2	22	I2C3	—
0x0000_01B0	108	92	2	23	—	—
0x0000_01B4	109	93	2	23	—	——
0x0000_01B8	110	94	2	23	—	—
0x0000_01BC	111	95	2	23	—	—
0x0000_01C0	112	96	3	24	—	—
0x0000_01C4	113	97	3	24	—	—
0x0000_01C8	114	98	3	24	—	—
0x0000_01CC	115	99	3	24	—	—
0x0000_01D0	116	100	3	25	QSPI0	Single interrupt vector for all sources
0x0000_01D4	117	101	3	25	—	—
0x0000_01D8	118	102	3	25	—	—
0x0000_01DC	119	103	3	25	—	—
0x0000_01E0	120	104	3	26	LTC	LP Trusted Cryptography
0x0000_01E4	121	105	3	26	—	—
0x0000_01E8	122	106	3	26	—	—

1. Indicates the NVIC's interrupt source number.

2. Indicates the NVIC's ISER, ICER, ISPR, ICPR, and IABR register number used for this IRQ. The equation to calculate this value is: IRQ div 32
3. Indicates the NVIC's IPR register number used for this IRQ. The equation to calculate this value is: IRQ div 4
4. This interrupt can only be pended or cleared via the NVIC registers.

3.5 AWIC overview

The primary function of the AWIC block is to detect asynchronous wake-up events in stop modes and signal to clock control logic to resume system clocking. After clock restart, the NVIC observes the pending interrupt and performs the normal interrupt or event processing.

3.6 Wake-up sources

The device uses the following internal and external inputs to the AWIC module.

Table 3-3. AWIC Partial Stop, Stop and VLPS Wake-up Sources

Wake-up source	Description
Available system resets	$\overline{\text{RESET}}$ pin and WDOG when LPO is its clock source, and JTAG
Low-voltage detect	Power Mode Controller
High-voltage detect	Power Mode Controller
Low-voltage warning	Power Mode Controller
Pin interrupts	Port Control Module - Any enabled pin interrupt is capable of waking the system
ADCx	The ADC is functional when using internal clock source
CMPx	Since no system clocks are available, functionality is limited, trigger mode provides wakeup functionality with periodic sampling
I^2C	Address match wakeup
LPUART	Functional when using clock source which is active in Stop and VLPS modes
USB FS/LS Controller	Wakeup
FlexIO	Functional when using clock source which is active in Stop and VLPS modes
LPTMR	Functional when using clock source which is active in Stop, VLPS and LLS/VLLS modes
RTC	Functional in Stop/VLPS modes
SDHC	Wakeup
I^2S (SAI)	Functional when using an external bit clock or external master clock
TPM	Functional when using clock source which is active in Stop and VLPS modes
TSI0	Wakeup
NMI	Non-maskable interrupt

Chapter 4
Memories and Memory Interfaces

4.1 Flash memory types

This device contains the following types of flash memory:

- Program flash memory — non-volatile flash memory that can execute program code

4.2 Flash Memory Sizes

The devices covered in this document contain:

- 1 block 256 kB of program flash consisting of 4 kB sectors

4.3 Flash Security

How flash security is implemented on this device is described in Chip Security.

4.4 Flash Modes

The flash memory is always configured in NVM normal. There are no operating conditions in which the flash is configured for NVM special mode.

4.5 Erase All Flash Contents

An Erase All Flash Blocks operation can be launched by software through a series of peripheral bus writes to flash registers. In addition the entire flash memory may be erased external to the flash memory from the SWJ-DP debug port by setting DAP_CONTROL[0]. DAP_STATUS[0] is set to indicate the mass erase command has been accepted. DAP_STATUS[0] is cleared when the mass erase completes.

4.6 FTF_FOPT Register

The flash memory's FTF_FOPT register allows the user to customize the operation of the MCU at boot time. See FOPT boot options for details of its definition.

4.7 SRAM sizes

This device contains SRAM tightly coupled to the ARM Cortex-M4 core. The on-chip SRAM is split into SRAM_L and SRAM_U regions where the SRAM_L and SRAM_U ranges form a contiguous block in the memory map anchored at address 0x2000_0000. As such:

- SRAM_L is anchored at address 0x2000_0000 and occupies the space below this address, that is, addresses less than 0x2000_0000.
- SRAM_U is anchored at address 0x2000_0000 and occupies the space at and above this beginning address, that is, addresses greater than or equal to 0x2000_0000.

NOTE

Misaligned accesses across the 0x2000_0000 boundary are not supported in the ARM Cortex-M4 architecture.

The amount of SRAM for the devices covered in this document is shown in the following table(s).

SRAM Sizes for ORDERABLE Part Numbers

Device	SRAM (KB)	SRAM_L size (KB)	SRAM_U size (KB)	Address Range
MK82FN256VDC15	256 kB	64 kB	192 kB	0x1FFF_0000-0x2002_FFFF

Table continues on the next page...

Device	SRAM (KB)	SRAM_L size (KB)	SRAM_U size (KB)	Address Range
MK82FN256CAx15[1]	256 kB	64 kB	192 kB	0x1FFF_0000-0x2002_FFFF
MK82FN256VLL15	256 kB	64 kB	192 kB	0x1FFF_0000-0x2002_FFFF
MK82FN256VLQ15[2]	256 kB	64 kB	192 kB	0x1FFF_0000-0x2002_FFFF

1. The 121-pin WLCSP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Please visit freescale.com/KPYW for more details.
2. The 144-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Please visit freescale.com/KPYW for more details.

4.8 SRAM accesses

The SRAM is split into two logical arrays that are 32-bits wide.

- SRAM_L — Accessible by the code bus of the Cortex-M4 core and by the backdoor port.
- SRAM_U — Accessible by the system bus of the Cortex-M4 core and by the backdoor port.

The backdoor port makes the SRAM accessible to the non-core bus masters (such as DMA).

The following figure illustrates the SRAM accesses within the device.

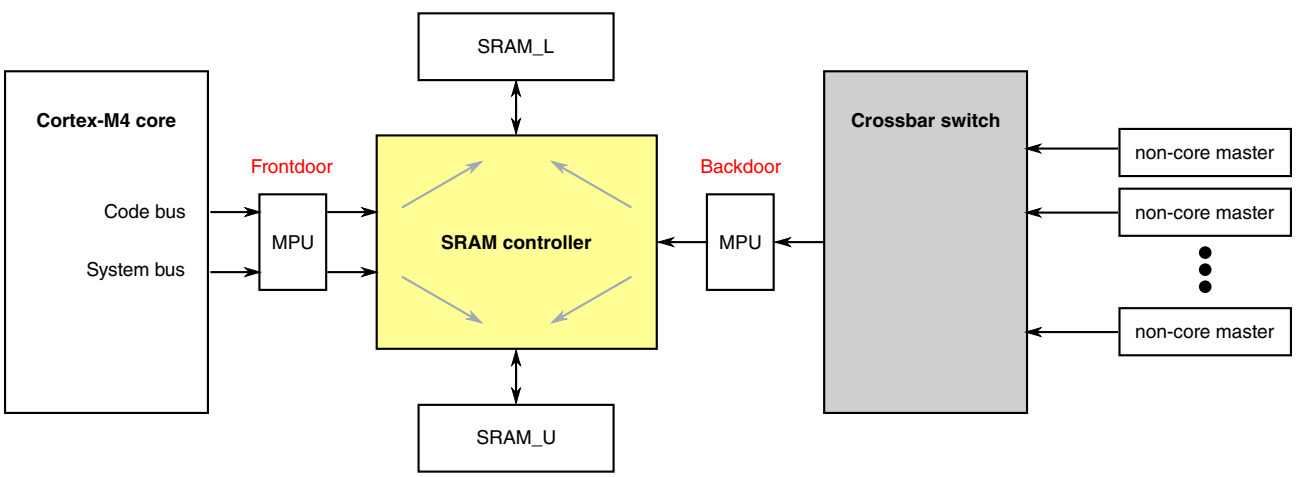


Figure 4-1. SRAM access diagram

The following simultaneous accesses can be made to different logical regions of the SRAM:

- Core code and core system
- Core code and non-core master system
- Core system and non-core master code

4.9 SRAM retention in low power modes

The SRAM is retained down to LLS3 and VLLS3 mode.

In LLS2 and VLLS2 the 32 kB region of SRAM_U based at 0x2000_0000 is powered. Optionally the 32KB region of SRAM_L ending at 0x1FFF_FFFF can be powered on, enabled by setting STOPCTRL[RAM2PO]. These regions (or partitions) of SRAM are labeled as follows:

- RAM1: the 32 kB region of SRAM_U always powered in VLLS2 and LLS2
- RAM2: the additional 32 KB region of SRAM_L optionally powered in VLLS2/ LLS2
- RAM3: the rest of system RAM

In VLLS1 and VLLS0 no SRAM is retained; however, the 32-byte register file is available.

4.10 QuadSPI memory interface

This device contains a QSPI controller which can interface with external flash devices to expand the storage size. With the QSPI controller enabled, the external flash can be mapped to a 128 MB system address range 0x6800_0000 to 0x6FFF_FFFF and can be read directly just like on-chip memory. For the flash space which exceeds above range, it can be read in through a 16 words QSPI FIFO located at system address 0x6700_0000. QSPI is not available when the system enters STOP modes, Compute Operation mode, LLSx and VLLSx modes.

4.11 System Register file

This device includes a 32-byte register file that is powered in all power modes.

Also, it retains contents during low-voltage detect (LVD) events and is only reset during a power-on reset.

4.12 VBAT register file

This device includes a 128-byte register file that is powered in all power modes and is powered by VBAT.

It is only reset during VBAT power-on reset.

Chapter 5
Memory Map

5.1 Introduction

This device contains various memories and memory-mapped peripherals which are located in one 32-bit contiguous memory space. This chapter describes the memory and peripheral locations within that memory space.

5.2 System memory map

The following table shows the high-level device memory map. This map provides the complete architectural address space definition for the various sections. Based on the physical sizes of the memories and peripherals, the actual address regions used may be smaller.

The system memory map includes multiple aliased address spaces that are intended for specific purposes.

- There are three aliased address spaces that are mapped into the ICode regions (address < 0x2000_0000) for code sections that normally reside in the system address space (address >= 0x2000_0000). The FlexBus address space is located in the system region of the memory map, but a subset of this space is aliased so it appears in the ICode region so instructions mapped into this space can be executed with maximum performance. The SDRAM Controller and QuadSPI have a similar mapping structure.
- There is an aliased region that maps a system address space to the Program flash section. This is complementary to the previous FlexBus example. Flash region aliasing is specifically intended for references to read-only data coefficients in the

flash while still preserving a full Harvard memory organization in the processor core supporting concurrent instruction fetches (for example, from RAM) and data accesses (from flash via the aliased space).

- The bitbanding functionality supported by the processor core uses aliased regions that map to the basic RAM and peripheral address spaces. This functionality maps each 32-bit word of the aliased address space to a unique bit in the underlying RAM or peripheral address space to support single-bit insert and extract operations from the processor.

Table 5-1. K82 System memory map

System 32-bit Address Range	Destination Slave	Access
0x0000_0000-0x03FF_FFFF [1]	Program flash and read-only data (Includes exception vectors in first 1024 bytes)	All masters
0x0400_0000-0x07FF_FFFF[2]	QSPI0 (Aliased area) Mapped to the same access space of 0x6800_0000 to 0x6BFF_FFFF	Cortex-M4 core (M0) only
0x0800_0000-0x0FFF_FFFF	SDRAM (Aliased area) Mapped to the same access space of 0x8800_0000-0x8FFF_FFFF	Cortex-M4 core (M0) only
0x1000_0000-0x17FF_FFFF	Reserved	—
0x1800_0000-0x1BFF_FFFF	FlexBus (Aliased Area) Mapped to the same access space of 0x9800_0000-0x9BFF_FFFF	Cortex-M4 core (M0) only
0x1C00_0000-0x1C00_7FFF	ROM	All masters
0x1C00_8000-0x1DFF_FFFF	Reserved	—
0x1E00_8000-0x1FFF_FFFF[3]	Tightly Coupled Memory Lower (TCML) SRAM_L: Lower SRAM (ICODE/ DCODE)	All masters
0x2000_0000-0x200F_FFFF[3]	Tightly Coupled Memory Upper (TCMU) SRAM_U: Upper SRAM bitband region	All masters
0x2100_0000-0x21FF_FFFF	Reserved	—
0x2200_0000-0x23FF_FFFF	Aliased to TCMU SRAM bitband	Cortex-M4 core only
0x2400_0000-0x2FFF_FFFF	Reserved	—
0x3000_0000-0x33FF_FFFF	Flash Data Alias	Cortex-M4 (M1) core only
0x3400_0000-0x3FFF_FFFF	Reserved	—
0x4000_0000-0x4007_FFFF	Bitband region for AIPS0	Cortex-M4 core & DMA
0x4008_0000-0x400F_EFFF	Bitband region for AIPS1	Cortex-M4 core & DMA
0x400F_F000-0x400F_FFFF	Bitband region for GPIO	Cortex-M4 core & DMA
0x4010_0000-0x41FF_FFFF	Reserved	—
0x4200_0000-0x43FF_FFFF	Aliased to AIPS and GPIO bitband	Cortex-M4 core only
0x4400_0000-0x5FFF_FFFF	Bit Manipulation Engine (BME2) access to AIPS0 peripheral slots 0-127 and AIPS1 peripheral slots 0-123	Cortex-M4 core & DMA
0x6000_0000-0x66FF_FFFF	FlexBus (External Memory - Write-back)	All masters

Table continues on the next page...

Table 5-1. K82 System memory map (continued)

System 32-bit Address Range	Destination Slave	Access
0x6700_0000-0x677F_FFFF	QuadSPI0 Rx Buffer	All masters
0x6780_0000-0x67FF_FFFF	Reserved	—
0x6800_0000-0x6FFF_FFFF[2]	QSPI0 (External Memory)	All masters
0x7000_0000-0x7FFF_FFFF	SDRAM (External Memory - Write-back)	All masters
0x8000_0000-0x87FF_FFFF	SDRAM (External Memory - Write-through)	All masters
0x8800_0000-0x8FFF_FFFF	SDRAM (External Memory - Write-through)	All masters
0x9000_0000-0x97FF_FFFF	Reserved	—
0x9800_0000-0x9FFF_FFFF	FlexBus (External Memory - Write-through)	All masters
0xA000_0000-0xDFFF_FFFF	FlexBus (External Peripheral - Not executable)	All masters
0xE000_0000-0xE00F_FFFF	Private Peripherals	Cortex-M4 core only
0xE010_0000-0xFFFF_FFFF	Reserved	—

1. This map provides the complete architectural address space definition for the flash. Based on the physical sizes of the memories implemented for a particular device, the actual address regions used may be smaller. See Flash Memory Sizes for details.
2. Debug access is available only in the aliased QuadSPI memory region. (Breakpoints are not supported in the main QuadSPI memory region.)
3. This range varies depending on amount of SRAM implemented for a particular device. See SRAM sizes for details.

NOTE

1. Access rights to AIPS-Lite peripheral bridges and general purpose input/output (GPIO) module address space is limited to the core and DMA.
2. ARM Cortex-M4 core access privileges also includes accesses via the debug interface.

5.3 Flash Memory Map

The flash memory and the flash registers are located at different base addresses as shown in the following figure. The base address for each is specified in System memory map.

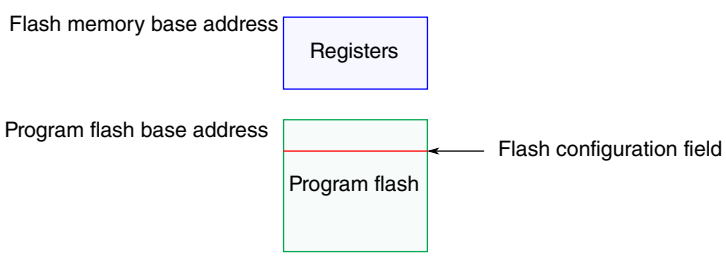


Figure 5-1. Flash memory map

The on-chip Flash is implemented in a portion of the allocated Flash range to form a contiguous block in the memory map beginning at address 0x0000_0000. See Flash Memory Sizes for details of supported ranges.

Accesses to the flash memory ranges outside the amount of Flash on the device causes the bus cycle to be terminated with an error followed by the appropriate response in the requesting bus master. Read collision events in which flash memory is accessed while a flash memory resource is being manipulated by a flash command also generates a bus error response.

5.4 Flash Access Control Introduction

The Flash Access Control (FAC) is a Freescale or third-party configurable memory protection scheme optimized to allow end users to utilize software libraries while offering programmable restrictions to these libraries. The flash memory is divided into equal size segments that provide protection to proprietary software libraries. The protection of these segments is controlled as the FAC evaluates of the access rights for each transaction routed to the on-chip flash memory. Configurability allows an increasing number of protected segments while supporting two levels of vendors adding their proprietary software to a device.

Flash access control aligns to the three privilege levels supported by ARM Cortex-M family products where the most secure state - supervisor/privileged-secure - aligns to the execute-only and supervisor-only access control. The unsecure state of user-non-secure aligns to no access control states set, and the mid-level state where user-secure aligns to using the access control of execute-only.

Control for this protection scheme is implemented in Program Once NVM locations and is configurable through Program Once flash command operations. The NVM locations controlling FAC are unaffected by Erase All Blocks flash command and debug interface initiated mass erase operations.

NOTE

The FAC protection scheme has eight XACC and eight SACC registers to control up to 64 segments. For program flash sizes 128KB or less, the memory is divided into 32 segments, controlled by the four lower-order XACC and SACC registers.

5.5 SRAM memory map

The on-chip RAM is split in two regions: SRAM_L and SRAM_U. The RAM is implemented such that the SRAM_L and SRAM_U ranges form a contiguous block in the memory map. See SRAM Configuration for details.

Accesses to the SRAM_L and SRAM_U memory ranges outside the amount of RAM on the device causes the bus cycle to be terminated with an error followed by the appropriate response in the requesting bus master.

5.6 Peripheral bridge (AIPS-Lite0 and AIPS-Lite1) memory maps

The peripheral memory map is accessible via two slave ports on the crossbar switch in the 0x4000_0000–0x400F_FFFF region. The device implements two peripheral bridges (AIPS-Lite 0 and 1):

- AIPS-Lite0 covers 512 KB
- AIPS-Lite1 covers 496 KB plus 4 KB assigned to the general purpose input/output module (GPIO) and 12 KB reserved (4K in 3 spaces)

AIPS-Lite0 is connected to crossbar switch slave port 2, and is accessible at locations 0x4000_0000–0x4007_FFFF.

The two regions associated with this space are:

- A 128 KB region, partitioned as 32 spaces, each 4 KB in size and reserved for on-platform peripheral devices. The AIPS controller generates unique module enables for all 32 spaces.
- A 384 KB region, partitioned as 96 spaces, each 4 KB in size and reserved for off-platform modules. The AIPS controller generates unique module enables for all 96 spaces.

AIPS-Lite1 and the general purpose input/output (GPIO) module share the connection to crossbar switch slave port 3. The AIPS-Lite1 is accessible at locations 0x4008_0000–0x400F_BFFF. 12 KB is reserved at 0x400F_C000 - 0x400F_EFFF. The general purpose input/output module is accessible in a 4 KB region at 0x400F_F000–0x400F_FFFF. Its direct connection to the crossbar switch provides master access without incurring wait states associated with accesses via the AIPS-Lite controllers.

NOTE

The BME2 functionality is available for the 512 KB of AIPS0 and 496 KB of AIPS1; it is not available for the GPIO.

Modules that are disabled via their clock gate control bits in the SIM registers disable the associated AIPS slots. Access to any address within an unimplemented or disabled peripheral bridge slot results in a transfer error termination.

For programming model accesses via the peripheral bridges, there is generally only a small range within the 4 KB slots that is implemented. Accessing an address that is not implemented in the peripheral results in a transfer error termination.

5.6.1 Peripheral Bridge 0 (AIPS-Lite 0) Memory Map

Table 5-2. Peripheral bridge 0 slot assignments

System 32-bit base address	Slot number	Module
0x4000_0000	0	Peripheral bridge 0 (AIPS-Lite 0)
0x4000_1000	1	—
0x4000_2000	2	—
0x4000_3000	3	—
0x4000_4000	4	Crossbar switch
0x4000_5000	5	—
0x4000_6000	6	—
0x4000_7000	7	—
0x4000_8000	8	DMA controller
0x4000_9000	9	DMA controller transfer control descriptors
0x4000_A000	10	—
0x4000_B000	11	—
0x4000_C000	12	FlexBus
0x4000_D000	13	System MPU
0x4000_E000	14	—
0x4000_F000	15	SDRAMC
0x4001_0000	16	—
0x4001_1000	17	—
0x4001_2000	18	—
0x4001_3000	19	—
0x4001_4000	20	—
0x4001_5000	21	—
0x4001_6000	22	—
0x4001_7000	23	—

Table continues on the next page...

Table 5-2. Peripheral bridge 0 slot assignments (continued)

System 32-bit base address	Slot number	Module
0x4001_8000	24	—
0x4001_9000	25	—
0x4001_A000	26	—
0x4001_B000	27	—
0x4001_C000	28	—
0x4001_D000	29	—
0x4001_E000	30	—
0x4001_F000	31	Flash memory controller
0x4002_0000	32	Flash memory
0x4002_1000	33	DMA channel mutiplexer
0x4002_2000	34	—
0x4002_3000	35	—
0x4002_4000	36	—
0x4002_5000	37	—
0x4002_6000	38	—
0x4002_7000	39	—
0x4002_8000	40	—
0x4002_9000	41	—
0x4002_A000	42	—
0x4002_B000	43	—
0x4002_C000	44	SPI 0
0x4002_D000	45	SPI 1
0x4002_E000	46	—
0x4002_F000	47	I2S (SSI/SAI) 0
0x4003_0000	48	—
0x4003_1000	49	—
0x4003_2000	50	CRC
0x4003_3000	51	—
0x4003_4000	52	—
0x4003_5000	53	USB0 DCD
0x4003_6000	54	Programmable delay block (PDB)
0x4003_7000	55	Periodic interrupt timers (PIT)
0x4003_8000	56	FlexTimer (FTM) 0
0x4003_9000	57	FlexTimer (FTM) 1
0x4003_A000	58	FlexTimer (FTM) 2[1]
0x4003_B000	59	Analog-to-digital converter (ADC) 0
0x4003_C000	60	—
0x4003_D000	61	Real-time clock (RTC)
0x4003_E000	62	VBAT register file

Table continues on the next page...

Table 5-2. Peripheral bridge 0 slot assignments (continued)

System 32-bit base address	Slot number	Module
0x4003_F000	63	DAC0[2]
0x4004_0000	64	Low-power timer 0 (LPTMR0)
0x4004_1000	65	System register file
0x4004_2000	66	—
0x4004_3000	67	—
0x4004_4000	68	Low-power timer 1 (LPTMR1)
0x4004_5000	69	Touch sense interface (TSI0)
0x4004_6000	70	—
0x4004_7000	71	SIM low-power logic
0x4004_8000	72	System integration module (SIM)
0x4004_9000	73	Port A multiplexing control
0x4004_A000	74	Port B multiplexing control
0x4004_B000	75	Port C multiplexing control
0x4004_C000	76	Port D multiplexing control
0x4004_D000	77	Port E multiplexing control
0x4004_E000	78	—
0x4004_F000	79	—
0x4005_0000	80	—
0x4005_1000	81	—
0x4005_2000	82	Software watchdog
0x4005_3000	83	—
0x4005_4000	84	—
0x4005_5000	85	—
0x4005_6000	86	—
0x4005_7000	87	—
0x4005_8000	88	—
0x4005_9000	89	—
0x4005_A000	90	—
0x4005_B000	91	—
0x4005_C000	92	—
0x4005_D000	93	—
0x4005_E000	94	—
0x4005_F000	95	—
0x4006_0000	96	—
0x4006_1000	97	External watchdog
0x4006_2000	98	Carrier modulator timer (CMT)
0x4006_3000	99	—
0x4006_4000	100	Multi-purpose Clock Generator (MCG)
0x4006_5000	101	System oscillator (OSC)

Table continues on the next page...

Table 5-2. Peripheral bridge 0 slot assignments (continued)

System 32-bit base address	Slot number	Module
0x4006_6000	102	I2C 0
0x4006_7000	103	I2C 1
0x4006_8000	104	—
0x4006_9000	105	—
0x4006_A000	106	—
0x4006_B000	107	—
0x4006_C000	108	—
0x4006_D000	109	—
0x4006_E000	110	—
0x4006_F000	111	—
0x4007_0000	112	—
0x4007_1000	113	—
0x4007_2000	114	USB OTG FS/LS
0x4007_3000	115	2C2D (Analog comparator (CMP) / 6-bit digital-to-analog converter (DAC))
0x4007_4000	116	Voltage reference (VREF)
0x4007_5000	117	—
0x4007_6000	118	—
0x4007_7000	119	—
0x4007_8000	120	—
0x4007_9000	121	—
0x4007_A000	122	—
0x4007_B000	123	—
0x4007_C000	124	Low-leakage wakeup unit (LLWU)
0x4007_D000	125	Power management controller (PMC)
0x4007_E000	126	System Mode controller (SMC)
0x4007_F000	127	Reset Control Module (RCM)

1. FTM2 is also available in AIPS1
2. DAC0 is also available in AIPS1

5.6.2 Peripheral Bridge 1 (AIPS-Lite 1) Memory Map

Table 5-3. Peripheral bridge 1 slot assignments

System 32-bit base address	Slot number	Module
0x4008_0000	0	Peripheral bridge 1 (AIPS-Lite 1)
0x4008_1000	1	—
0x4008_2000	2	—

Table continues on the next page...

Table 5-3. Peripheral bridge 1 slot assignments (continued)

System 32-bit base address	Slot number	Module
0x4008_3000	3	—
0x4008_4000	4	—
0x4008_5000	5	—
0x4008_6000	6	—
0x4008_7000	7	—
0x4008_8000	8	—
0x4008_9000	9	—
0x4008_A000	10	—
0x4008_B000	11	—
0x4008_C000	12	—
0x4008_D000	13	—
0x4008_E000	14	—
0x4008_F000	15	—
0x4009_0000	16	—
0x4009_1000	17	—
0x4009_2000	18	—
0x4009_3000	19	—
0x4009_4000	20	—
0x4009_5000	21	—
0x4009_6000	22	—
0x4009_7000	23	—
0x4009_8000	24	—
0x4009_9000	25	—
0x4009_A000	26	—
0x4009_B000	27	—
0x4009_C000	28	—
0x4009_D000	29	—
0x4009_E000	30	—
0x4009_F000	31	—
0x400A_0000	32	True Random number generator (TRNG)
0x400A_1000	33	—
0x400A_2000	34	—
0x400A_3000	35	—
0x400A_4000	36	—
0x400A_5000	37	—
0x400A_6000	38	—
0x400A_7000	39	—
0x400A_8000	40	—
0x400A_9000	41	—

Table continues on the next page...

Table 5-3. Peripheral bridge 1 slot assignments (continued)

System 32-bit base address	Slot number	Module
0x400A_A000	42	—
0x400A_B000	43	—
0x400A_C000	44	SPI 2
0x400A_D000	45	—
0x400A_E000	46	—
0x400A_F000	47	—
0x400B_0000	48	—
0x400B_1000	49	eSDHC
0x400B_2000	50	—
0x400B_3000	51	—
0x400B_4000	52	—
0x400B_5000	53	—
0x400B_6000	54	—
0x400B_7000	55	—
0x400B_8000	56	FlexTimer (FTM) 2[1]
0x400B_9000	57	FlexTimer (FTM) 3
0x400B_A000	58	—
0x400B_B000	59	—
0x400B_C000	60	—
0x400B_D000	61	—
0x400B_E000	62	—
0x400B_F000	63	—
0x400C_0000	64	—
0x400C_1000	65	—
0x400C_2000	66	—
0x400C_3000	67	—
0x400C_4000	68	LPUART0
0x400C_5000	69	LPUART1
0x400C_6000	70	LPUART2
0x400C_7000	71	LPUART3
0x400C_8000	72	—
0x400C_9000	73	TPM1
0x400C_A000	74	TPM2
0x400C_B000	75	—
0x400C_C000	76	12-bit digital-to-analog converter (DAC) 0[2]
0x400C_D000	77	—
0x400C_E000	78	—
0x400C_F000	79	—
0x400D_0000	80	—

Table continues on the next page...

Table 5-3. Peripheral bridge 1 slot assignments (continued)

System 32-bit base address	Slot number	Module
0x400D_1000	81	LP Trusted Cryptography (LTC)
0x400D_2000	82	—
0x400D_3000	83	—
0x400D_4000	84	EMVSIM0
0x400D_5000	85	EMVSIM1
0x400D_6000	86	LPUART4
0x400D_7000	87	—
0x400D_8000	88	—
0x400D_9000	89	—
0x400D_A000	90	QSPI0
0x400D_B000	91	—
0x400D_C000	92	—
0x400D_D000	93	—
0x400D_E000	94	—
0x400D_F000	95	FlexIO0
0x400E_0000	96	—
0x400E_1000	97	—
0x400E_2000	98	—
0x400E_3000	99	—
0x400E_4000	100	—
0x400E_5000	101	—
0x400E_6000	102	I2C2
0x400E_7000	103	I2C3
0x400E_8000	104	—
0x400E_9000	105	—
0x400E_A000	106	—
0x400E_B000	107	—
0x400E_C000	108	—
0x400E_D000	109	—
0x400E_E000	110	—
0x400E_F000	111	—
0x400F_0000	112	—
0x400F_1000	113	—
0x400F_2000	114	—
0x400F_3000	115	—
0x400F_4000	116	—
0x400F_5000	117	—
0x400F_6000	118	—
0x400F_7000	119	—

Table continues on the next page...

Table 5-3. Peripheral bridge 1 slot assignments (continued)

System 32-bit base address	Slot number	Module
0x400F_8000	120	—
0x400F_9000	121	—
0x400F_A000	122	—
0x400F_B000	123	—
0x400F_C000	124	Not an AIPS-Lite slot. Reserved
0x400F_D000	125 [3]	Not an AIPS-Lite slot. Reserved
0x400F_E000	126 [3]	Not an AIPS-Lite slot. Reserved
0x400F_F000	127 [3]	Not an AIPS-Lite slot. The 32-bit general purpose input/output module that shares the crossbar switch slave port with the AIPS-Lite is accessed at this address.

1. FTM2 is also available in AIPS0
2. DAC0 is also available in AIPS0
3. Last 4 slots of AIPS1 (124-127) cannot be accessed through BME2 on this device.

5.7 Private Peripheral Bus (PPB) memory map

The PPB is part of the defined ARM bus architecture and provides access to select processor-local modules. These resources are only accessible from the core; other system masters do not have access to them.

Table 5-4. PPB memory map

System 32-bit Address Range	Resource
0xE000_0000–0xE000_0FFF	Instrumentation Trace Macrocell (ITM)
0xE000_1000–0xE000_1FFF	Data Watchpoint and Trace (DWT)
0xE000_2000–0xE000_2FFF	Flash Patch and Breakpoint (FPB)
0xE000_3000–0xE000_DFFF	Reserved
0xE000_E000–0xE000_EFFF	System Control Space (SCS) (for NVIC and FPU)
0xE000_F000–0xE003_FFFF	Reserved
0xE004_0000–0xE004_0FFF	Trace Port Interface Unit (TPIU)
0xE004_1000–0xE004_1FFF	Embedded Trace Macrocell (ETM)
0xE004_2000–0xE004_2FFF	Reserved
0xE004_3000–0xE004_3FFF	Reserved
0xE004_4000–0xE007_FFFF	Reserved
0xE008_0000–0xE008_0FFF	Miscellaneous Control Module (MCM)
0xE008_1000–0xE008_1FFF	Memory Mapped Cryptographic Acceleration Unit (MMCAU)
0xE008_2000–0xE008_2FFF	Cache Controller
0xE008_3000–0xE00F_EFFF	Reserved
0xE00F_F000–0xE00F_FFFF	ROM Table - allows auto-detection of debug components

Chapter 6
Clock Distribution using MCG

6.1 Introduction

The MCG module controls which clock source is used to derive the system clocks. The clock generation logic divides the selected clock source into a variety of clock domains, including the clocks for the system bus masters, system bus slaves, and flash memory. The clock generation logic also implements module-specific clock gating to allow granular shutoff of modules.

The primary clocks for the system are generated from the MCGOUTCLK clock. The clock generation circuitry provides several clock dividers that allow different portions of the device to be clocked at different frequencies. This allows for trade-offs between performance and power dissipation.

Various modules, such as the USB OTG Controller, have module-specific clocks that can be generated from the IRC48MCLK or MCGPLLCLK or MCGFLLCLK clock. The SDRAM controller is a specific case, since it can take its clock from either PLL (system or SDRAM). In addition, there are various other module-specific clocks that have other alternate sources. Clock selection for most modules is controlled by the SOPT registers in the SIM module.

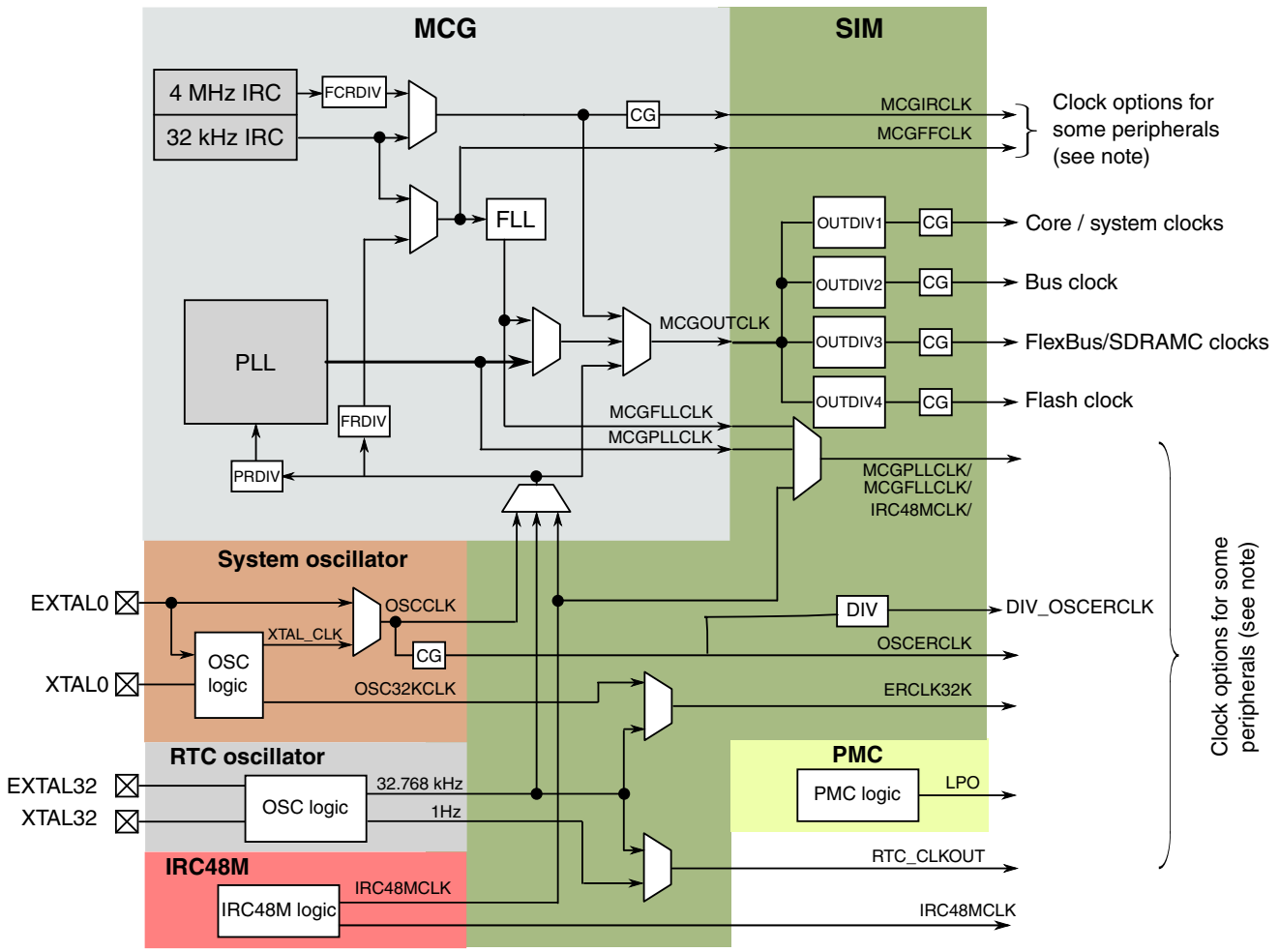
6.2 Programming model

The selection and multiplexing of system clock sources is controlled and programmed via the MCG module. The setting of clock dividers and module clock gating for the system are programmed via the SIM module. Reference those sections for detailed register and bit descriptions.

6.3 High-Level device clocking diagram

The following system oscillator, MCG, and SIM module registers control the multiplexers, dividers, and clock gates shown in the below figure:

	OSC	MCG	SIM
Multiplexers	MCG_C*x*	MCG_C*x*	SIM_SOPT1, SIM_SOPT2
Dividers	—	MCG_C*x*	SIM_CLKDIV*x*
Clock gates	OSC_CR	MCG_C1	SIM_SCGC*x*



CG — Clock gate

Note: See subsequent sections for details on where these clocks are used.

Figure 6-1. Clocking diagram

6.4 Clock definitions

The following table describes the clocks in the previous block diagram.

Clock name	Description
Core clock	MCGOUTCLK divided by OUTDIV1 clocks the ARM Cortex-M4 core
System clock	MCGOUTCLK divided by OUTDIV1 clocks the crossbar switch and bus masters directly connected to the crossbar.
Bus clock	MCGOUTCLK divided by OUTDIV2 clocks the bus slaves and peripheral (excluding memories)
FlexBus clock	MCGOUTCLK divided by OUTDIV3 clocks the external FlexBus interface
Flash clock	MCGOUTCLK divided by OUTDIV4 clocks the flash memory
MCGIRCLK	MCG output of the slow or fast internal reference clock
MCGFFCLK	MCG output of the slow internal reference clock or a divided MCG external reference clock.
MCGOUTCLK	MCG output of either IRC, MCGFLLCLK , MCGPLLCLK or MCG's external reference clock that sources the core, system, bus, FlexBus, and flash clock. It is also an option for the debug trace clock.
MCGFLLCLK	MCG output of the FLL. MCGFLLCLK may clock some modules.
MCGPLLCLK	MCG output of the PLL. MCGFLLCLK or MCGPLLCLK may clock some modules.
MCG external reference clock	Input clock to the MCG sourced by the system oscillator (OSCCLK) or RTC oscillator
IRC48MCLK	Internal 48 MHz oscillator that can be used as a reference to the MCG and also may clock some on-chip modules.
OSCCLK	System oscillator output of the internal oscillator or sourced directly from EXTAL
OSCERCLK	System oscillator output sourced from OSCCLK that may clock some on-chip modules
OSC32KCLK	System oscillator 32kHz output
ERCLK32K	Clock source for some modules that is chosen as OSC32KCLK or the RTC clock.
RTC clock	RTC oscillator output for the RTC module
LPO	PMC 1kHz output

6.4.1 Device clock summary

The following table provides more information regarding the on-chip clocks.

Table 6-1. Clock Summary

Clock name	HS Run mode clock frequency	Run mode clock frequency	VLPR mode clock frequency	Clock source	Clock is disabled when…
MCGOUTCLK	Up to 150 MHz	Up to 120 MHz	Up to 4 MHz	MCG	In all stop modes except for partial stop modes and during PLL locking when MCGOUTCLK derived from PLL.
MCGFLLCLK	Up to 100 MHz	Up to 100 MHz	N/A	MCG	MCG clock controls do not enable. Overriding forced disable in all low powers modes (including STOP and VLPx modes).
MCGPLLCLK	Up to 150 MHz	Up to 150 MHz	N/A	MCG	MCG clock controls do not enable, in Stop mode but PLLSTEN=0, or in VLPS, LLS and VLLSx modes
Core clock	Up to 150 MHz	Up to 120 MHz	Up to 4 MHz	MCGOUTCLK clock divider	In all wait and stop modes
System clock	Up to 150 MHz	Up to 120 MHz	Up to 4 MHz	MCGOUTCLK clock divider	In all stop modes and Compute operation
Bus clock	Up to 75 MHz	Up to 60 MHz	Up to 4 MHz	MCGOUTCLK clock divider	In all stop modes except for partial STOP2 mode, and Compute Operation
FlexBus clock (FB_CLK)	Up to 75 MHz	Up to 60 MHz	Up to 4 MHz	MCGOUTCLK clock divider	In all stop modes or FlexBus disabled
Flash clock	Up to 25 MHz	Up to 25 MHz	Up to 1MHz in BLPE, Up to 800KHz in BLPI	MCGOUTCLK clock divider	In all stop modes except for partial STOP2 mode
Internal reference (MCGIRCLK)	Up to 4 MHz IRC oscillator	Up to 4 MHz IRC oscillator	Up to 4 MHz IRC oscillator	MCG	MCG_C1[IRCLKEN] cleared, Stop or VLPS mode and MCG_C1[IREFSTEN] cleared, or LLS/ VLLS mode
External reference (OSCERCLK)	Up to 50 MHz (bypass), 30-40 kHz, or 3-32 MHz (crystal)	Up to 50 MHz (bypass), 30-40 kHz, or 3-32 MHz (crystal)	Up to 16 MHz (bypass), 30-40 kHz (low-range crystal) or Up to 16 MHz (high-range crystal)	System OSC	System OSC's OSC_CR[ERCLKEN] cleared, or Stop mode and OSC_CR[EREFSTEN] cleared

Table continues on the next page...

Table 6-1. Clock Summary (continued)

Clock name	HS Run mode clock frequency	Run mode clock frequency	VLPR mode clock frequency	Clock source	Clock is disabled when...
External reference 32kHz (ERCLK32K)	30-40 kHz	30-40 kHz	30-40 kHz	System OSC or RTC OSC depending on SIM_SOPT1[OSC32KSEL]	System OSC's OSC_CR[ERCLKEN] cleared or RTC's RTC_CR[OSCE] cleared
Internal 48 MHz clock (IRC48MCLK)	48 MHz	48 MHz	N/A	IRC48M	USB, MCG or SIM control does not enable and QSPI does not select it. Overriding forced disable in VLPS, LLSx, VLLSx.
RTC_CLKOUT	1 Hz or 32 kHz	1 Hz or 32 kHz	1 Hz or 32 kHz	RTC clock	Clock is disabled in LLS and VLLSx modes
LPO	1 kHz	1 kHz	1 kHz	PMC	in VLLS0
USB FS clock	48 MHz	48 MHz	N/A	MCGPLLCLK, IRC48MCLK or MCGFLLCLK with fractional clock divider, or USB_CLKIN	USB FS OTG is disabled in all Stop Modes and Compute Operation mode
I^2S master clock	Up to 75 MHz	Up to 60 MHz	Up to 12.5 MHz	System clock , MCGPLLCLK, IRC48MCLK, OSCERCLK with fractional clock divider, or I2S_CLKIN	I^2S is disabled
SDHC clock	Up to 150 MHz	Up to 120 MHz	Up to 4 MHz	System clock, MCGPLLCLK/ MCGFLLCLK, or OSCERCLK	SDHC is disabled
LPUART clock	Up to 75 MHz	Up to 75 MHz	Up to 16 MHz	MCGIRCLK, IRC48MCLK, OSCERCLK, or MCGPLLCLK/ MCGFLLCLK	SIM_SOPT2[LPUARTSRC] is cleared
FlexIO clock	Up to 150 MHz	Up to 120 MHz	Up to 16 MHz	System clock, MCGIRCLK, IRC48MCLK, OSCERCLK, or MCGPLLCLK/ MCGFLLCLK	FlexIO is disabled

Table continues on the next page...

Table 6-1. Clock Summary (continued)

Clock name	HS Run mode clock frequency	Run mode clock frequency	VLPR mode clock frequency	Clock source	Clock is disabled when...
EMVSIM clock	Up to 75 MHz	Up to 75 MHz	Up to 8 MHz	MCGIRCLK, IRC48MCLK, OSCERCLK, or MCGPLLCLK/ MCGFLLCLK	SIM_SOPT2[EMVSIMSRC] is cleared
TPM clock	Up to 75 MHz	Up to 75 MHz	Up to 16 MHz	MCGIRCLK, IRC48MCLK, OSCERCLK, or MCGPLLCLK/ MCGFLLCLK	SIM_SOPT2[LPTPMSRC] is cleared
TRACE clock	Up to 150 MHz	Up to 120 MHz	Up to 4 MHz	System clock or MCGOUTCLK	Trace is disabled
QSPI clocking	Up to 100 MHz [1]	Up to 100 MHz	Up to 4 MHz	MCGPLL2XCLK, MCGPLLCLK/ MCGFLLCLK, IRC48MHZ, MCGIRCLK or OSCERCLK	QSPI is disabled in all stop modes and Compute Operation

1. QuadSPI clocks are limited to 75 MHz in dual data rate (DDR) configurations for both RUN and HSRUN modes.

6.5 Internal clocking requirements

The clock dividers are programmed via the SIM module's CLKDIV registers. Each divider is programmable from a divide-by-1 through divide-by-16 setting. The following requirements must be met when configuring the clocks for this device:

1. The core and system clock frequencies must be 150 MHz or slower in HSRUN, 120MHz or slower in RUN.
2. The bus clock frequency must be programmed to 75 MHz or slower in HSRUN, 60 MHz or slower in RUN, and an integer divide of the core clock. The core clock to bus clock ratio is limited to a max value of 8.

NOTE

Flash erase and programming operations are not allowed in HSRUN modes

3. The flash clock frequency must be programmed to 25 MHz or less, less than or equal to the bus clock, and an integer divide of the core clock. The core clock to flash clock ratio is limited to a max value of 8.

4. The FlexBus clock frequency must be programmed to be less than or equal to the bus clock frequency. The FlexBus also has pad interface restrictions that limits the maximum frequency. For this device the FlexBus maximum frequency is 75 MHz. The core clock to FlexBus clock ratio is limited to a max value of 8.
5. Since SDRAMC and FlexBus both use CLKOUT, the same restrictions apply to the SDRAM controller as stated for the FlexBus clock.
6. The QuadSPI clock must be 75 MHz or less in DDR (dual) mode and 100 MHz or less in SDR (single) mode.

The following are a few of the more common clock configurations for this device:

6.5.1 Clock divider values after reset

Each clock divider is programmed via the SIM module's CLKDIV*n* registers. The flash memory's FTF_FOPT[LPBOOT] bit controls the reset value of the core clock, system clock, bus clock, and flash clock dividers as shown below:

FTF_FOPT [LPBOOT]	Core/system clock	Bus clock	FlexBus clock	Flash clock	Description
0	0x7 (divide by 8)	0x7 (divide by 8)	0xF (divide by 16)	0xF (divide by 16)	Low power boot
1	0x0 (divide by 1)	0x0 (divide by 1)	0x1 (divide by 2)	0x1 (divide by 2)	Fast clock boot

This gives the user flexibility for a lower frequency, low-power boot option. The flash erased state defaults to fast clocking mode, since where the low power boot (FTF_FOPT[LPBOOT]) bit resides in flash is logic 1 in the flash erased state.

To enable the low power boot option program FTF_FOPT[LPBOOT] to zero. During the reset sequence, if LPBOOT is cleared, the system is in a slow clock configuration. Upon any system reset, the clock dividers return to this configurable reset state.

6.5.2 VLPR mode clocking

The clock dividers cannot be changed while in VLPR mode. They must be programmed prior to entering VLPR mode to guarantee:

- the core/system, FlexBus, and bus clocks are less than or equal to 4 MHz, and
- the flash memory clock is less than or equal to 1 MHz

NOTE

When the MCG is in BLPI and clocking is derived from the Fast IRC, the clock divider controls, MCG_SC[FCRDIV] and

SIM_CLKDIV1[OUTDIV4], must be programmed such that the resulting flash clock nominal frequency is 800 kHz or less. In this case, one example of correct configuration is MCG_SC[FCRDIV]=000b and SIM_CLKDIV1[OUTDIV4]=0100b, resulting in a divide by 5 setting.

6.6 Clock Gating

The clock to each module can be individually gated on and off using the SIM module's SCGC*x* registers. These bits are cleared after any reset, which disables the clock to the corresponding module to conserve power. Prior to initializing a module, set the corresponding bit in SCGC*x* register to enable the clock. Before turning off the clock, make sure to disable the module.

Any bus access to a peripheral that has its clock disabled generates an error termination.

6.7 Module clocks

The following table summarizes the clocks associated with each module.

Table 6-2. Module clocks

Module	Bus interface clock	Internal clocks	I/O interface clocks
Core modules			
ARM Cortex-M4 core	System clock	Core clock	—
NVIC	System clock	—	—
DAP	System clock	—	—
ITM	System clock	—	—
ETM	System clock	TRACE clock	TRACE_CLKOUT
cJTAG, JTAGC	—	—	JTAG_CLK
System modules			
DMA	System clock	—	—
DMA Mux	Bus clock	—	—
Port control	Bus clock	LPO	—
Crossbar Switch	System clock	—	—
Peripheral bridges	System clock	Bus clock, Flash clock	—
MPU	System clock	—	—
LLWU, PMC, SIM, RCM	Flash clock	LPO	—
Mode controller	Flash clock	—	—

Table continues on the next page...

Table 6-2. Module clocks (continued)

Module	Bus interface clock	Internal clocks	I/O interface clocks
MCM	System clock	—	—
EWM	Bus clock	LPO	—
Watchdog timer	Bus clock	LPO	—
Clocks			
MCG	Flash clock	MCGOUTCLK, MCGPLLCLK, MCGFLLCLK, MCGIRCLK, OSCERCLK	—
OSC	Bus clock	OSCERCLK	—
IRC48M	—	IRC48MCLK	—
Memory and memory interfaces			
Flash Controller	System clock	Flash clock	—
Flash memory	Flash clock	—	—
FlexBus	System clock	—	CLKOUT
SDRAM controller	System clock	—	CLKOUT
QSPI controller	System clock	QSPI clock	QSPIx_SCK
Security			
CRC	Bus clock	—	—
MMCAU	System clock	—	—
TRNG	Bus clock	—	—
LTC Encryption Engine	System clock	—	—
Analog			
ADC	Bus clock	OSCERCLK, IRC48MCLK	—
CMP	Bus clock	—	—
DAC	Bus clock	—	—
VREF	Flash clock	—	—
Timers			
TPM	Bus clock	TPM clock	TPM_CLKIN0, TPM_CLKIN1
PDB	Bus clock	—	—
FlexTimers	Bus clock	MCGFFCLK	FTM_CLKINx
PIT	Bus clock	—	—
LPTMR	Flash clock	LPO, OSCERCLK, MCGIRCLK, ERCLK32K	—
CMT	Bus clock	—	—
RTC	Flash clock	EXTAL32	—
Communication interfaces			
USB FS OTG	System clock	USB FS clock	—
USB DCD	Bus clock	—	—
DSPI	Bus clock	—	DSPI_SCK
I^2C	Bus clock	—	I2C_SCL
LPUART	Bus clock	LPUART clock	—

Table continues on the next page...

Table 6-2. Module clocks (continued)

Module	Bus interface clock	Internal clocks	I/O interface clocks
SDHC	System clock	SDHC clock	SDHC_DCLK
I^2S	Bus clock	I^2S master clock	I2S_TX_BCLK, I2S_RX_BCLK
EMVSIM	Bus clock	EMVSIM clock	—
FlexIO	Bus clock	FlexIO clock	—
Human-machine interfaces			
GPIO	Platform clock	—	—
TSI	Flash clock	—	—

6.7.1 PMC 1-kHz LPO clock

The Power Management Controller (PMC) generates a 1-kHz clock that is enabled in all modes of operation, including all low power modes except VLLS0. This 1-kHz source is commonly referred to as LPO clock or 1-kHz LPO clock.

6.7.2 IRC 48MHz clock

The integrated 48 MHz internal reference clock source (IRC48MCLK) is available in High Speed Run, Run, WAIT and Stop modes of operation. IRC48MCLK is also available in Compute Only, PSTOP2 and PSTOP1 modes of operation when entered from Run mode. IRC48MCLK is forced disabled when the MCU transitions into VLPS , LLSx, and VLLSx low power modes.

NOTE

IRC48MCLK is not forced disabled in Stop modes and should be disabled by software prior to Stop entry unless it is required. IRC48MCLK is not forced disabled in VLPR and should be disabled by software prior to VLPR entry.

IRC48MCLK is enabled via the following control settings while operating in these modes:

- USB Control register enables — enabled when USB_CLK_RECOVER_IRC_EN[IRC_EN]=1
- or MCG Control register selects IRC48 MHz clock — enabled when MCG_C7[OSCSEL]=10
- or SIM Control register selects IRC48 MHz clock — enabled when SIM_SOPT2[PLLFLLSEL]=11

In USB Device applications, the IRC48M block can be enabled in USB Clock Recovery mode in which the internal IRC48M oscillator is tuned to match the clock extracted from the incoming USB data stream. This functionality provides the capability of generating a high precision 48MHz clock source without requiring an on-chip PLL or an associated off-chip crystal circuit.

The IRC48MCLK is also available for use as:

- An oscillator reference to the MCG - from which core, system, bus, and flash clock sources can be derived
- an ADC alternate clock source
- clock source for LPUART communications
- clock source for I2S/SAI communications

6.7.3 WDOG clocking

The WDOG may be clocked from two clock sources as shown in the following figure.

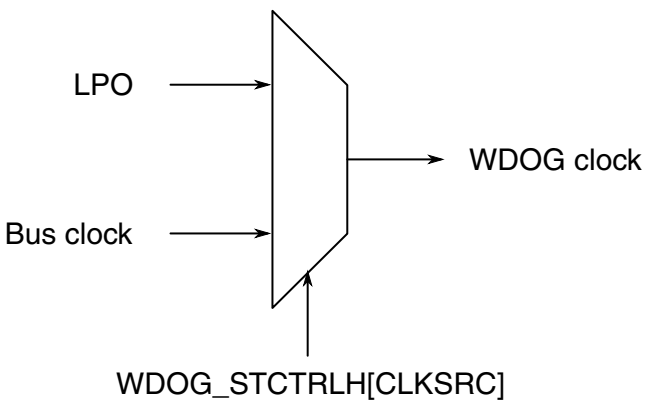


Figure 6-2. WDOG clock generation

6.7.4 Debug trace clock

The debug trace clock source can be clocked as shown in the following figure.

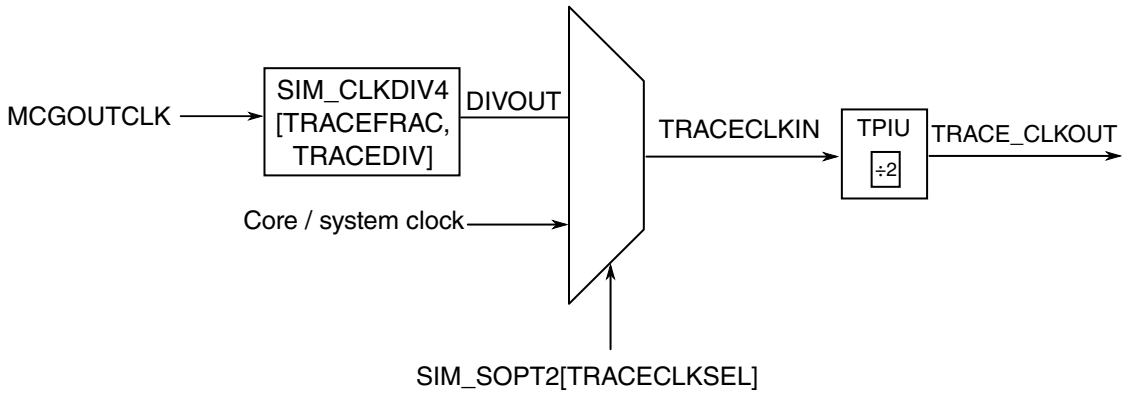


Figure 6-3. Trace clock generation

NOTE

The trace clock frequency observed at the TRACE_CLKOUT pin will be half that of the selected clock source.

6.7.5 PORT digital filter clocking

The digital filters in each of the PORT*x* modules the PORTD module can be clocked as shown in the following figure.

NOTE

In stop mode, the digital input filters are bypassed unless they are configured to run from the 1 kHz LPO clock source.

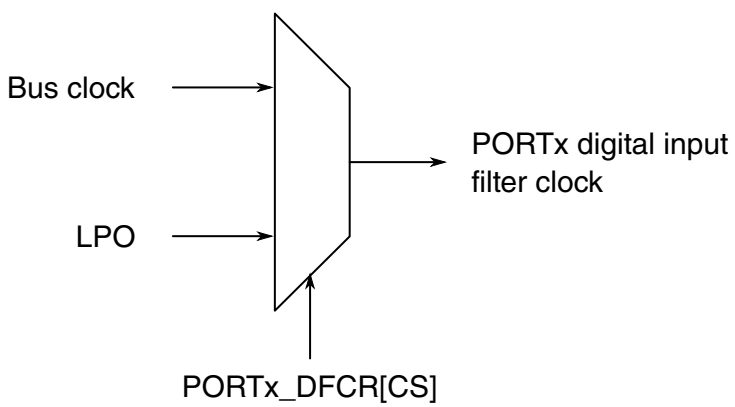


Figure 6-4. PORTx digital input filter clock generation

6.7.6 LPTMR clocking

The prescaler and glitch filters in each of the LPTMR*x* modules can be clocked as shown in the following figure.

NOTE

The chosen clock must remain enabled if the LPTMR*x* is to continue operating in all required low-power modes.

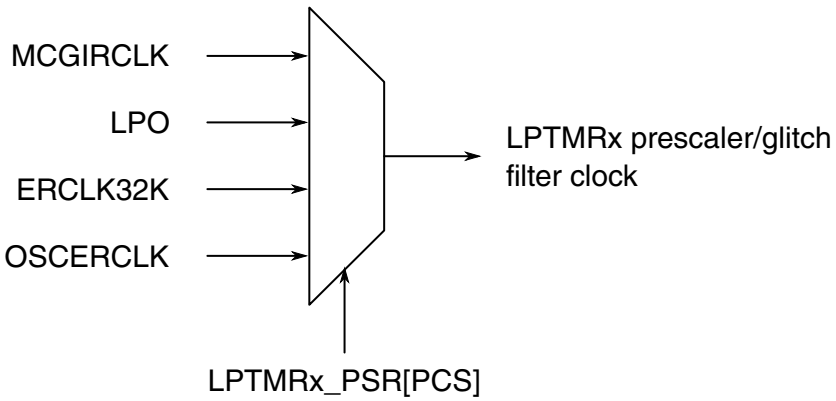


Figure 6-5. LPTMRx prescaler/glitch filter clock generation

6.7.7 TPM clocking

The counter for the TPM modules have a selectable clock as shown in the following figure.

NOTE

The chosen clock must remain enabled if the TPM*x* is to continue operating in all required low-power modes.

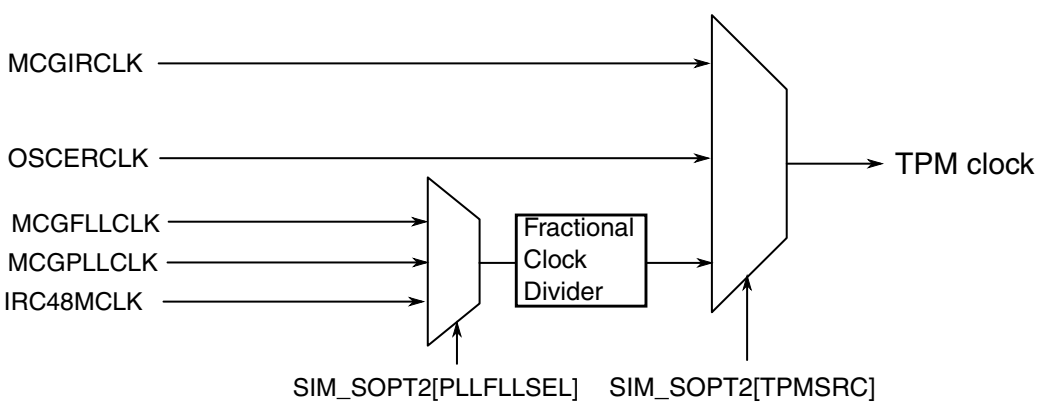


Figure 6-6. TPM clock generation

6.7.8 SDHC clocking

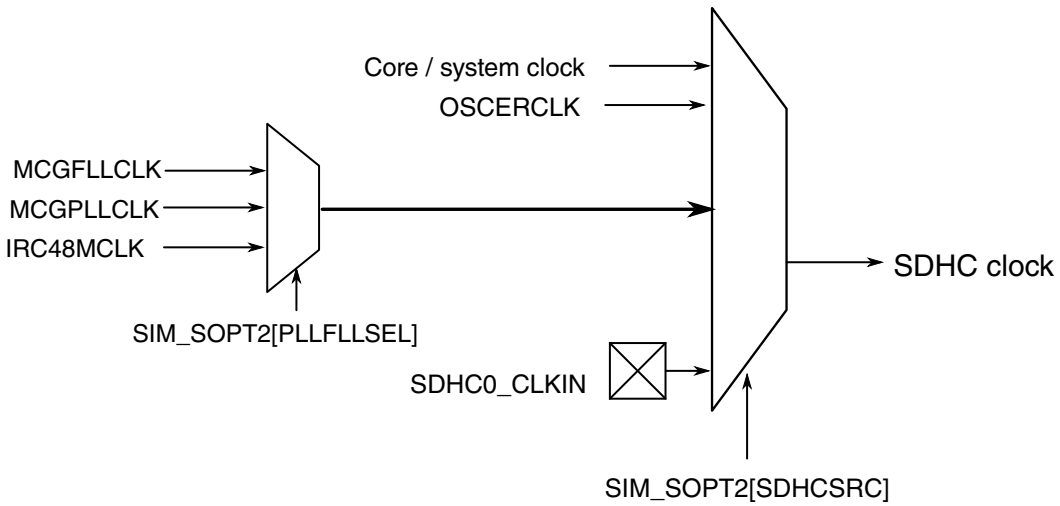


Figure 6-7. SDHC clock generation

6.7.9 USB FS OTG Controller clocking

The USB FS OTG controller is a bus master attached to the crossbar switch. As such, it uses the system clock.

NOTE

For the USB FS OTG controller to operate, the minimum system clock frequency is 20 MHz.

The USB OTG controller also requires a 48 MHz clock. The clock source options are shown below.

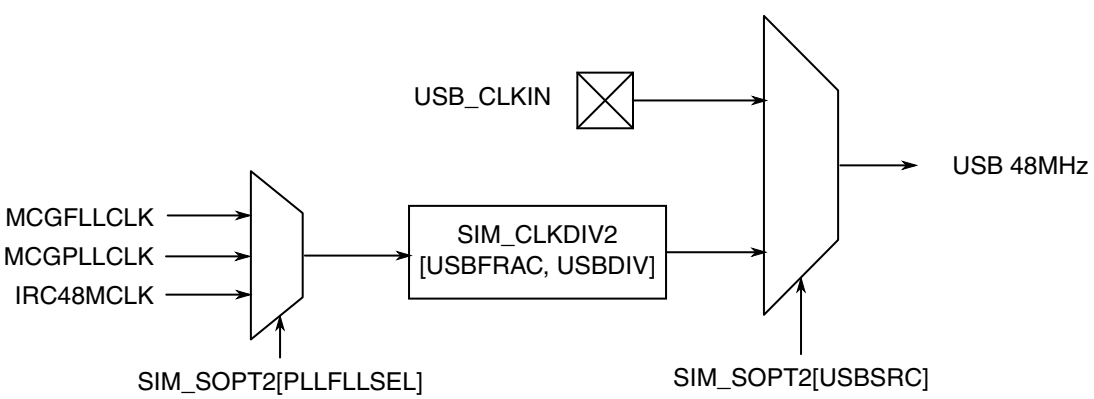


Figure 6-8. USB 48 MHz clock source

NOTE

The MCGFLLCLK does not meet the USB jitter specifications for certification. The IRC48MCLK is only usable as a USB clock source in USB Device operation with the USB Clock Recover function enabled.

6.7.10 LPUART clocking

Each LPUART module has a selectable clock as shown in the following figure.

NOTE

The chosen clock must remain enabled if the LPUART is to continue operating in all required low-power modes.

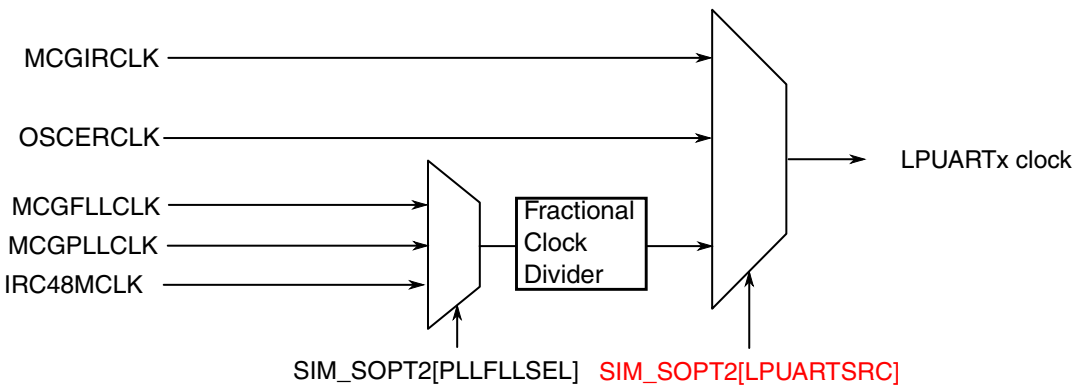


Figure 6-9. LPUART clock generation

6.7.11 I²S/SAI clocking

The audio master clock (MCLK) is used to generate the bit clock when the receiver or transmitter is configured for an internally generated bit clock. The audio master clock can also be output to or input from a pin. The transmitter and receiver have the same audio master clock inputs.

Each SAI peripheral can control the input clock selection, pin direction and divide ratio of one audio master clock.

The I²S/SAI transmitter and receiver support asynchronous bit clocks (BCLKs) that can be generated internally from the audio master clock or supplied externally. The module also supports the option for synchronous operation between the receiver and transmitter product or between two separate I²S/SAI peripherals.

The transmitter and receiver can independently select between the bus clock and the audio master clocks to generate the bit clock.

The MCLK and BCLK source options appear in the following figure.

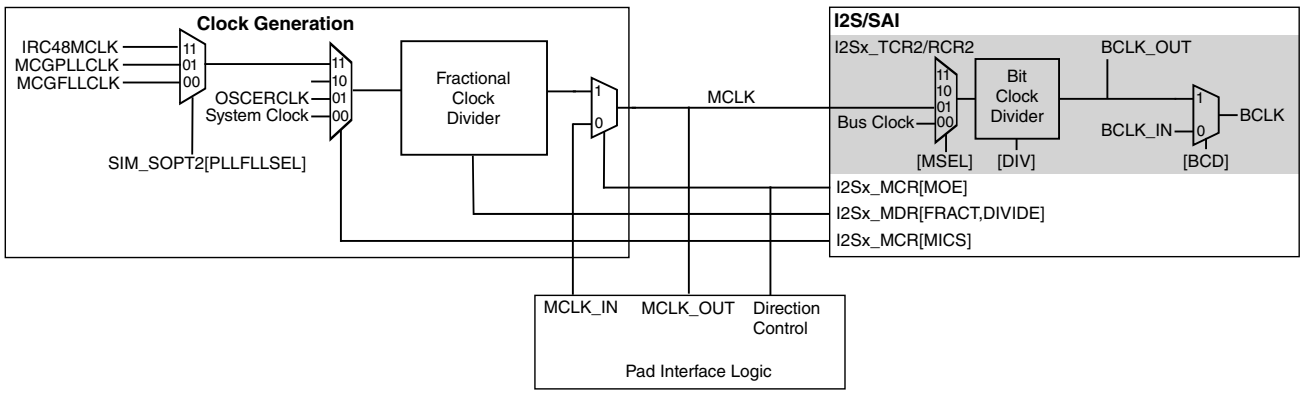


Figure 6-10. I²S/SAI clock generation

6.7.12 QuadSPI clocking

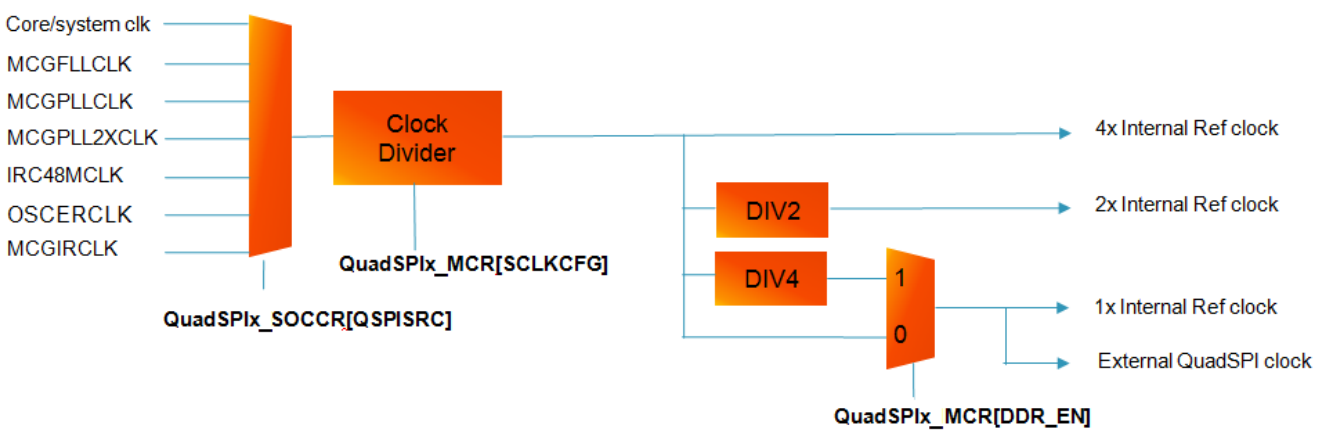


Figure 6-11. QuadSPI clock generation

DDR mode of the QuadSPI requires a 4x, 2x, and 1x internal reference clock. In DDR mode, the clock divider output is used as the 4x internal reference clock. The 2x and 1x clocks are divided down from that clock.

To generate the maximum 75Mhz flash frequency supported in DDR mode, MCGPLL2XCLK should be 300MHz with QuadSPIx_MCR[SCLKCFG]=0 to generate the 4x internal clock required.

In SDR mode, the 4x and 2x internal clocks are not used, and the Div 4 divider is bypassed.

6.7.13 LP Trusted Cryptography (LTC) clocking

LTC is clocked from the system clock.

6.7.14 TRNG clocking

TRNG is clocked from the bus clock.

6.7.15 FlexIO clocking

The FlexIO timers and shifters have a selectable clock as shown in the following figure.

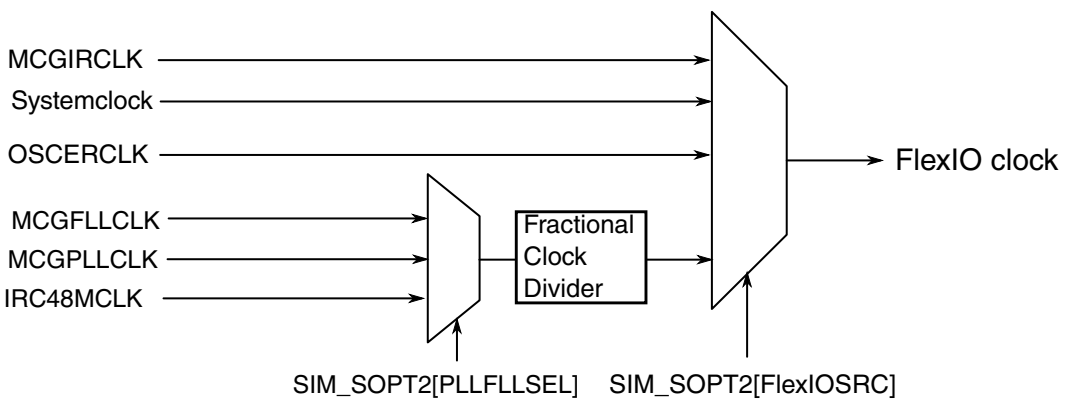


Figure 6-12. FlexIO clock generation

NOTE

The chosen clock must remain enabled if FlexIO is to continue operation in required low-power modes.

6.7.16 EMVSIM clocking

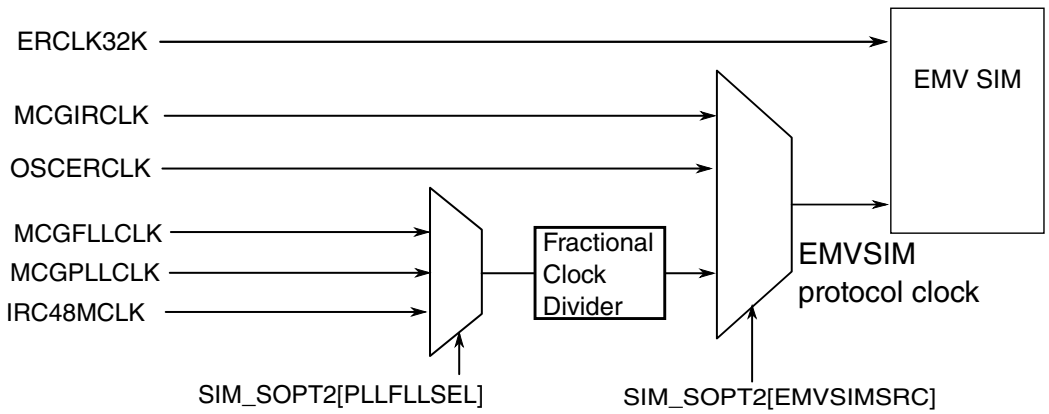


Figure 6-13. EMVSIM clock generation

Chapter 7
Reset and Boot

7.1 Introduction

The following reset sources are supported in this MCU:

Table 7-1. Reset sources

Reset sources	Description
POR reset	• Power-on reset (POR)
System resets	• External pin reset (PIN) • Low-voltage detect (LVD) • Computer operating properly (COP) watchdog reset • Low leakage wakeup (LLWU) reset • Multipurpose clock generator loss of clock (LOC) reset • Multipurpose clock generator loss of lock (LOL) reset • Stop mode acknowledge error (SACKERR) • Software reset (SW) • Lockup reset (LOCKUP) • MDM DAP system reset
Debug reset	• JTAG reset • nTRST reset

Each of the system reset sources has an associated bit in the system reset status (SRS) registers. See the Reset Control Module for register details.

The MCU exits reset in functional mode where the CPU is executing code. See Boot options for more details.

7.2 Reset

This section discusses basic reset mechanisms and sources. Some modules that cause resets can be configured to cause interrupts instead. Consult the individual peripheral chapters for more information.

7.2.1 Power-on reset (POR)

When power is initially applied to the MCU or when the supply voltage drops below the power-on reset re-arm voltage level (V_{POR}), the POR circuit causes a POR reset condition.

As the supply voltage rises, the LVD circuit holds the MCU in reset until the V_{DD} supply has risen above the LVD low threshold (V_{LVDL}). The POR and LVD bits in SRS0 register are set following a POR.

It is required that V_{DDIO} is powered up after V_{DD}, and powered down prior to V_{DD} power down. In other words, V_{DDIO} cannot be powered when V_{DD} is off.

7.2.2 System reset sources

Resetting the MCU provides a way to start processing from a known set of initial conditions. System reset begins with the on-chip regulator in full regulation and system clocking generation from an internal reference. When the processor exits reset, it performs the following:

- Reads the start SP (SP_main) from vector-table offset 0
- Reads the start PC from vector-table offset 4
- LR is set to 0xFFFF_FFFF

The on-chip peripheral modules are disabled and the non-analog I/O pins are initially configured as disabled. The pins with analog functions assigned to them default to their analog function after reset.

During and following a reset, the JTAG pins have their associated input pins configured as:

- TDI in pull-up (PU)
- TCK in pull-down (PD)
- TMS in PU

and associated output pin configured as:

- TDO with no pull-down or pull-up

Note that the nTRST signal is initially configured as disabled, however once configured to its JTAG functionality its associated input pin is configured as:

- nTRST in PU

7.2.2.1 External pin reset (PIN)

On this device, $\overline{\text{RESET}}$ is a dedicated pin. This pin is open drain and has an internal pullup device. Asserting $\overline{\text{RESET}}$ wakes the device from any mode. During a pin reset, the RCM's SRS0[PIN] bit is set.

7.2.2.1.1 $\overline{\text{RESET}}$ pin filter

The $\overline{\text{RESET}}$ pin filter supports filtering from both the 1 kHz LPO clock and the bus clock. RCM_RPFC[RSTFLTSS], RCM_RPFC[RSTFLTSRW], and RCM_RPFW[RSTFLTSEL] control this functionality; see the RCM chapter. The filters are asynchronously reset by Chip POR. The reset value for each filter assumes the $\overline{\text{RESET}}$ pin is negated.

For all stop modes where LPO clock is still active (Stop, VLPS, LLS, VLLS3, VLLS2, and VLLS1), the only filtering option is the LPO-based digital filter. The filtering logic either switches to bypass operation or has continued filtering operation depending on the filtering mode selected. When entering VLLS0, the $\overline{\text{RESET}}$ pin filter is disabled and bypassed.

The LPO filter has a fixed filter value of 3. Due to a synchronizer on the input data, there is also some associated latency (2 cycles). As a result, 5 cycles are required to complete a transition from low to high or high to low.

7.2.2.2 Low-voltage detect (LVD)

The chip includes a system for managing low voltage conditions on the V_{DD} domain to protect memory contents and control MCU system states during supply voltage variations. The system consists of a power-on reset (POR) circuit and an LVD circuit with a user-selectable trip voltage. The LVD system is always enabled in hsrun, normal run, wait, or stop mode. The LVD system is disabled when entering VLPx, LLS, or VLLSx modes.

The LVD can be configured to generate a reset upon detection of a low voltage condition by setting the PMC's LVDSC1[LVDRE] bit to 1. The low voltage detection threshold is determined by the PMC's LVDSC1[LVDV] field. After an LVD reset has occurred, the LVD system holds the MCU in reset until the supply voltage has risen above the low voltage detection threshold. The RCM's SRS0[LVD] bit is set following either an LVD reset or POR.

NOTE

V_{DDIO} domain does not contain LVD circuit.

7.2.2.3 Computer operating properly (COP) watchdog timer

The computer operating properly (COP) watchdog timer (WDOG) monitors the operation of the system by expecting periodic communication from the software. This communication is generally known as servicing (or refreshing) the COP watchdog. If this periodic refreshing does not occur, the watchdog issues a system reset. The COP reset causes the RCM's SRS0[WDOG] bit to set.

7.2.2.4 Low leakage wakeup (LLWU)

The LLWU module provides the means for a number of external pins, the $\overline{\text{RESET}}$ pin, and a number of internal peripherals to wake the MCU from low leakage power modes. The LLWU module is functional only in low leakage power modes.

- In LLS mode, only the $\overline{\text{RESET}}$ pin via the LLWU can generate a system reset.
- In VLLSx modes, all enabled inputs to the LLWU can generate a system reset.

After a system reset, the LLWU retains the flags indicating the input source of the last wakeup until the user clears them.

NOTE

Some flags are cleared in the LLWU and some flags are required to be cleared in the peripheral module. Refer to the individual peripheral chapters for more information.

7.2.2.5 Multipurpose clock generator loss-of-clock (LOC)

The MCG module supports an external reference clock.

If the C6[CME] bit in the MCG module is set, the clock monitor is enabled. If the external reference falls below f_{loc_low} or f_{loc_high}, as controlled by the C2[RANGE] field in the MCG module, the MCU resets. The RCM's SRS0[LOC] bit is set to indicate this reset source.

NOTE

To prevent unexpected loss of clock reset events, all clock monitors should be disabled before entering any low power modes, including VLPR and VLPW.

7.2.2.6 MCG loss-of-lock (LOL) reset

The MCG includes a PLL loss-of-lock detector. The detector is enabled when configured for PEE and lock has been achieved. If the MCG_C8[LOLRE] bit in the MCG module is set and the PLL lock status bit (MCG_S[LOLS0]) becomes set, the MCU resets. The RCM_SRS0[LOL] bit is set to indicate this reset source.

NOTE

This reset source does not cause a reset if the chip is in any stop mode.

7.2.2.7 Stop mode acknowledge error (SACKERR)

This reset is generated if the core attempts to enter stop mode, but not all modules acknowledge stop mode within 1025 cycles of the 1 kHz LPO clock.

A module might not acknowledge the entry to stop mode if an error condition occurs. The error can be caused by a failure of an external clock input to a module.

7.2.2.8 Software reset (SW)

The SYSRESETREQ bit in the NVIC application interrupt and reset control register can be set to force a software reset on the device. (See ARM's NVIC documentation for the full description of the register fields, especially the VECTKEY field requirements.) Setting SYSRESETREQ generates a software reset request. This reset forces a system reset of all major components except for the debug module. A software reset causes the RCM's SRS1[SW] bit to set.

7.2.2.9 Lockup reset (LOCKUP)

The LOCKUP gives immediate indication of seriously errant kernel software. This is the result of the core being locked because of an unrecoverable exception following the activation of the processor’s built in system state protection hardware.

The LOCKUP condition causes a system reset and also causes the RCM's SRS1[LOCKUP] bit to set.

7.2.2.10 MDM-AP system reset request

Set the system reset request bit in the MDM-AP control register to initiate a system reset. This is the primary method for resets via the JTAG/SWD interface. The system reset is held until this bit is cleared.

Set the core hold reset bit in the MDM-AP control register to hold the core in reset as the rest of the chip comes out of system reset.

7.2.3 MCU Resets

A variety of resets are generated by the MCU to reset different modules.

7.2.3.1 VBAT POR

The VBAT POR asserts on a VBAT POR reset source. It affects only the modules within the VBAT power domain: RTC and VBAT Register File. These modules are not affected by the other reset types.

7.2.3.2 POR Only

The POR Only reset asserts on the POR reset source only. It resets the PMC and System Register File.

The POR Only reset also causes all other reset types (except VBAT POR) to occur.

7.2.3.3 Chip POR not VLLS

The Chip POR not VLLS reset asserts on POR and LVD reset sources. It resets parts of the SMC and SIM. It also resets the LPTMR.

The Chip POR not VLLS reset also causes these resets to occur: Chip POR, Chip Reset not VLLS, and Chip Reset (including Early Chip Reset).

7.2.3.4 Chip POR

The Chip POR asserts on POR, LVD, and VLLS Wakeup reset sources. It resets the Reset Pin Filter registers and parts of the SIM and MCG.

The Chip POR also causes the Chip Reset (including Early Chip Reset) to occur.

7.2.3.5 Chip Reset not VLLS

The Chip Reset not VLLS reset asserts on all reset sources except a VLLS Wakeup that does not occur via the RESET_b pin. It resets parts of the SMC, LLWU, and other modules that remain powered during VLLS mode.

The Chip Reset not VLLS reset also causes the Chip Reset (including Early Chip Reset) to occur.

7.2.3.6 Early Chip Reset

The Early Chip Reset asserts on all reset sources. It resets only the flash memory module. It negates before flash memory initialization begins ("earlier" than when the Chip Reset negates).

7.2.3.7 Chip Reset

Chip Reset asserts on all reset sources and only negates after flash initialization has completed and the RESET_b pin has also negated. It resets the remaining modules (the modules not reset by other reset types).

7.2.4 Reset Pin

For all reset sources except a VLLS Wakeup that does not occur via the $\overline{\text{RESET}}$ pin, the $\overline{\text{RESET}}$ pin is driven low by the MCU for at least 128 bus clock cycles and until flash initialization has completed.

After flash initialization has completed, the $\overline{\text{RESET}}$ pin is released, and the internal Chip Reset negates after the $\overline{\text{RESET}}$ pin is pulled high. Keeping the $\overline{\text{RESET}}$ pin asserted externally delays the negation of the internal Chip Reset.

7.2.5 Debug resets

The following sections detail the debug resets available on the device.

7.2.5.1 JTAG reset

The JTAG module generate a system reset when certain IR codes are selected. This functional reset is asserted when EXTEST, HIGHZ and CLAMP instructions are active. The reset source from the JTAG module is released when any other IR code is selected. A JTAG reset causes the RCM's SRS1[JTAG] bit to set.

7.2.5.2 nTRST reset

The nTRST pin causes a reset of the JTAG logic when asserted. Asserting the nTRST pin allows the debugger to gain control of the TAP controller state machine (after exiting LLS or VLLSx) without resetting the state of the debug modules.

The nTRST pin does not cause a system reset.

7.2.5.3 Resetting the Debug subsystem

Use the CDBGRSTREQ bit within the SWJ-DP CTRL/STAT register to reset the debug modules. However, as explained below, using the CDBGRSTREQ bit does not reset all debug-related registers.

CDBGRSTREQ resets the debug-related registers within the following modules:

- SWJ-DP
- AHB-AP
- ETM
- TPIU
- MDM-AP (MDM control and status registers)

CDBGRSTREQ does not reset the debug-related registers within the following modules:

- CM4 core (core debug registers: DHCSR, DCRSR, DCRDR, DEMCR)
- FPB
- DWT
- ITM
- NVIC
- Crossbar bus switch[1]
- AHB-AP[1]
- Private peripheral bus[1]

1. CDBGRSTREQ does not affect AHB resources so that debug resources on the private peripheral bus are available during System Reset.

7.3 Boot

This section describes the boot sequence, including sources and options.

7.3.1 Boot sources

Based on the source selections in FOPT, the device boots initially to internal Flash or internal BOOT ROM. If BOOT ROM, the device executes in boot loader mode or proceeds with a secondary boot to a QSPI device connected to QSPI0 which can be optionally an encrypted image that can be decrypted by the OTFAD module.

7.3.2 Boot options

Because this device has BOOT ROM and no dedicated BOOT mode pin, the device's functional mode is controlled by the BOOT ROM reading the flash option boot source selection located within FOPT register.

7.3.3 FOPT boot options

The flash option register (FOPT) in the flash memory module allows the user to customize the operation of the MCU at boot time. The register contains read-only bits that are loaded from the NVM's option byte in the flash configuration field. The user can reprogram the option byte in flash to change the FOPT values that are used for subsequent resets. For more details on programming the option byte, refer to the flash memory chapter.

The MCU uses the FOPT register bits to configure the device at reset as shown in the following table.

NOTE

Reserved bits in the option byte should be left in their default erased state of logic 1. FOPT[7:0] = 0x00 is not a valid

configuration. FOPT register is written to 0xFF if the contents of NVM's option byte in the flash configuration field is 0x00.

Table 7-2. Flash Option Register Bit Definitions

Bit Num	Field	Value	Definition
7-6	BOOTSRC_SEL	Boot Source Selection: these bits select the boot sources if boot pin option bit BOOTPIN_OPT = 1	
		00	Boot from Internal Flash
		01	Reserved
		10	Boot from ROM, configure QSPI0, and enter boot loader mode. See Boot sequence for more information
		11	Boot from ROM and enter boot loader mode. See Boot sequence for more information.
5	FAST_INIT	Select initialization speed on POR, VLLSx, and any system reset.	
		0	Slower initialization. The Flash initialization will be slower with the benefit of reduced average current during this time. The duration of the recovery will be controlled by the clock divider selection determined by the LPBOOT setting.
		1	Fast Initialization. The Flash has faster recoveries at the expense of higher current during these times.
4-3	Reserved	Reserved for future expansion.	
2	NMI_DIS	Enable/disable control for the NMI function.	
		0	NMI interrupts are always blocked. The associated pin continues to default to NMI pin controls with internal pullup enabled.
		1	NMI pin/interrupts reset default to enabled.
1	BOOTPIN_OPT	External pin selects boot options	
		0	Force Boot from ROM with update if BOOTCFG0 asserted, where BOOTCFG0 is the boot config function which is muxed with NMI pin. The RESET pin should be enabled when this option is selected.
		1	Boot source configured by FOPT[7:6] (BOOTSRC_SEL) bits
0	LPBOOT	Control the reset value of OUTDIVx values in SIM_CLKDIV1 register. Larger divide value selections produce lower average power consumption during POR, VLLSx recoveries and reset sequencing and after reset exit.	
		0	Low-power boot: OUTDIVx values in SIM_CLKDIV1 register are auto-configured at reset exit for higher divide values that produce lower power consumption at reset exit. • Core and system clock divider (OUTDIV1) and bus clock divider (OUTDIV2) are 0x7 (divide by 8) • Flash clock divider (OUTDIV4) and FlexBus clock divider (OUTDIV3) are 0xF (divide by 16)
		1	Normal boot: OUTDIVx values in SIM_CLKDIV1 register are auto-configured at reset exit for higher frequency values that produce faster operating frequencies at reset exit. • Core and system clock divider (OUTDIV1) and bus clock divider (OUTDIV2) are 0x0 (divide by 1) • Flash clock divider (OUTDIV4) and FlexBus clock divider (OUTDIV3) are 0x1 (divide by 2)

7.3.4 Boot sequence

At power up, the on-chip regulator holds the system in a POR state until the input supply is above the POR threshold. The system continues to be held in this static state until the internally regulated supplies have reached a safe operating voltage as determined by the LVD. The Mode Controller reset logic then controls a sequence to exit reset.

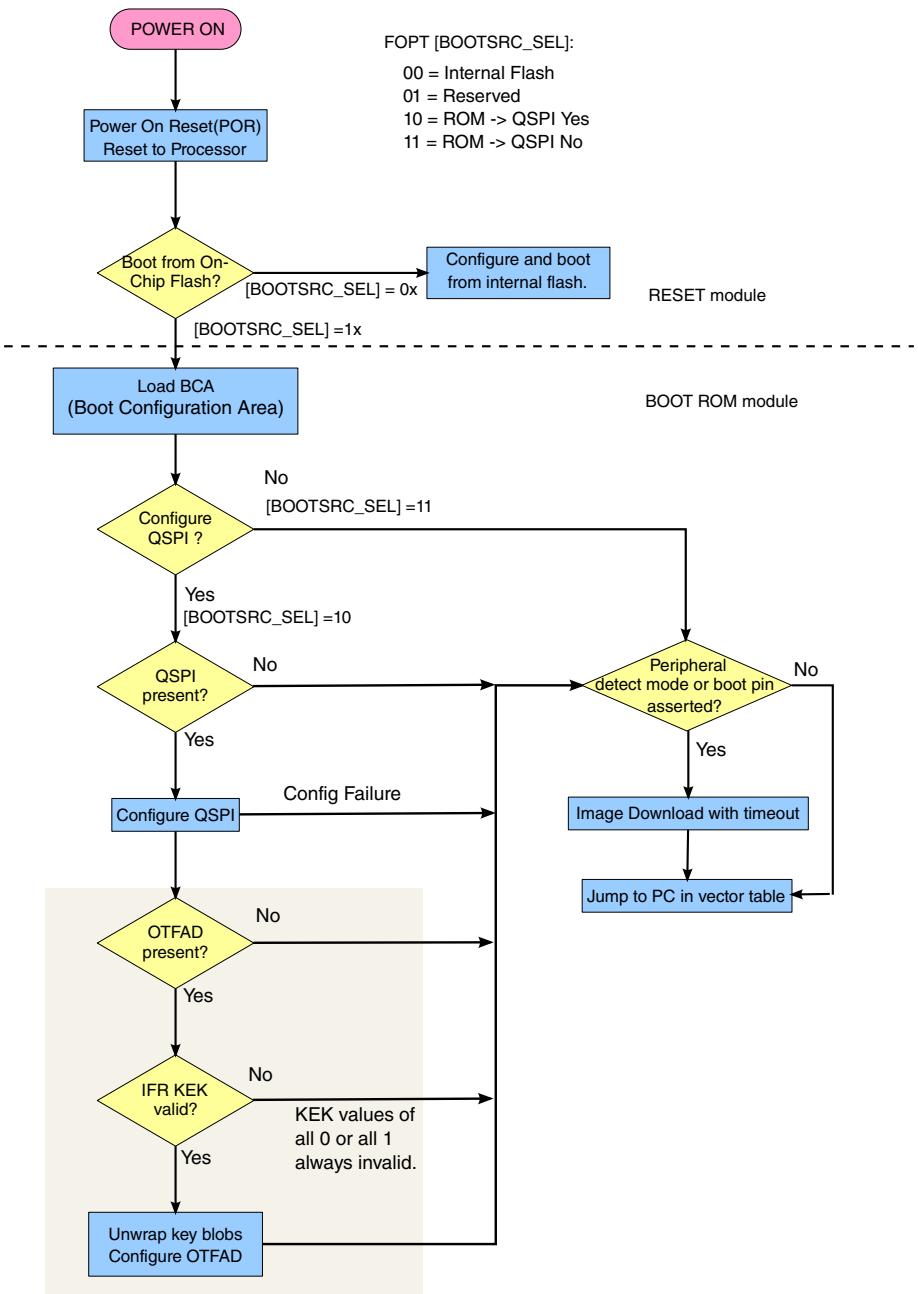


Figure 7-1. Boot Flow For Devices with QSPI and OTFAD

1. A system reset is held on internal logic, the $\overline{\text{RESET}}$ pin is driven out low, and the MCG is enabled in its default clocking mode.
2. Required clocks are enabled (Core Clock, System Clock, Flash Clock, and any Bus Clocks that do not have clock gate control reset to disabled).
3. The system reset on internal logic continues to be held, but the Flash Controller is released from reset and begins initialization operation while the Reset Control logic continues to drive the $\overline{\text{RESET}}$ pin out low.
4. Early in reset sequencing the NVM option byte is read and stored to the Flash Memory module's FOPT register. Based on the following values, the corresponding actions are taken:
   a. If the LPBOOT bit is programmed for an alternate clock divider reset value, the system/core clock is switched to a slower clock speed.
   b. If the FAST_INIT bit is programmed clear, the Flash initialization switches to slower clock resulting longer recovery times.
   c. If the BOOTPIN_OPT bit is set, the boot source of the device is determined by BOOTSRC_SEL field.
   d. The BOOTSRC_SEL field determines if the device boots from internal flash, directly from the internal ROM to allow bootloading of firmware, or configuring the QSPI to allow booting from QSPI device.
5. When Flash Initialization completes, the $\overline{\text{RESET}}$ pin is released. If $\overline{\text{RESET}}$ continues to be asserted (an indication of a slow rise time on the $\overline{\text{RESET}}$ pin or external drive in low), the system continues to be held in reset. Once the $\overline{\text{RESET}}$ pin is detected high, the Core clock is enabled and the system is released from reset.
6. If the BOOTSRC_SEL bits indicate a boot from internal flash, when the system exits reset, the processor sets up the stack, program counter (PC), and link register (LR). The processor reads the start SP (SP_main) from vector-table offset 0. The core reads the start PC from vector-table offset 4. LR is set to 0xFFFF_FFFF. What happens next depends on the NMI input and the FOPT[NMI_DIS] field in the Flash Memory module:
   - If the NMI input is high or the NMI function is disabled in the NMI_DIS field, the CPU begins execution at the PC location.
   - If the NMI input is low and the NMI function is enabled in the NMI_DIS field, this results in an NMI interrupt. The processor executes an Exception Entry and reads the NMI interrupt handler address from vector-table offset 8. The CPU begins execution at the NMI interrupt handler.

Subsequent system resets follow this same reset flow.

Chapter 8
Kinetis ROM Bootloader

8.1 Chip-Specific Information

This device has various peripherals supported by the Kinetis ROM Bootloader.

Table 8-1. Kinetis Bootloader Peripheral Pinmux

Peripheral	Instance	Port	GPIO	Alt
LPUART	0	LPUART0_RX	PTB16	3
		LPUART0_TX	PTB17	3
	1	LPUART1_RX	PTC3	3
		LPUART1_TX	PTC4	3
	2	LPUART2_RX	PTD2	3
		LPUART2_TX	PTD3	3
I2C	0	I2C0_SCL	PTB2	2
		I2C0_SDA	PTB3	2
I2C	1	I2C1_SCL	PTC10	2
		I2C1_SDA	PTC11	2
SPI	0	SPI0_PCS0	PTA14	2
		SPI0_SCK	PTA15	2
		SPI0_SOUT	PTA16	2
		SPI0_SIN	PTA17	2
SPI	1	SPI1_PCS0	PTD4	7
		SPI1_SCK	PTD5	7
		SPI1_SOUT	PTD6	7
		SPI1_SIN	PTD7	7
QuadSPI	0	QSPI0A_DATA3	PTE0	5
		QSPI0A_SCLK	PTE1	5
		QSPI0A_DATA0	PTE2	5
		QSPI0A_DATA2	PTE3	5
		QSPI0A_DATA1	PTE4	5
		QSPI0A_SS0_B	PTE5	5

Table continues on the next page...

Table 8-1. Kinetis Bootloader Peripheral Pinmux (continued)

Peripheral	Instance	Port	GPIO	Alt
		QSPI0A_SS1_B	PTE7	7
		QSPI0A_DQS	PTE11	7
		QSPI0B_DATA3	PTE6	5
		QSPI0B_SCLK	PTE7	5
		QSPI0B_DATA0	PTE8	5
		QSPI0B_DATA2	PTE9	5
		QSPI0B_DATA1	PTE10	5
		QSPI0B_SS0_B	PTE11	5
		QSPI0B_DQS [1]	PTE12	5
		QSPI0B_SS1_B [1]	PTE13	5
CRC		Status pin	PTA11	1

1. Only available on the 144LQFP package.

NOTE

Not all QuadSPI pins are supported in all packages, so refer the pinout section for detailed information.

8.2 Introduction

The Kinetis bootloader is the program residing in the on-chip read-only memory (ROM) of a Kinetis microcontroller device. There is hardware logic in place at boot time that either starts execution of an embedded image available on the internal flash memory, or starts the execution of the Kinetis Bootloader from on-chip ROM. When booting from ROM, the bootloader can optionally jump to an application in the external Quad SPI flash memory.

The Kinetis Bootloader's main task is to provision the internal flash (or external Quad SPI flash) memory with an embedded firmware image during manufacturing, or at any time during the life of the Kinetis device. The Kinetis Bootloader does the provisioning by acting as a slave device, and listening to various peripheral ports where a master can start communication.

For the Kinetis device, the Kinetis Bootloader can interface with USB, I2C, SPI, and LPUART peripherals in slave mode and respond to the commands sent by a master (or host) communicating on one of those ports. The host/master can be a firmware-download application running on a PC or an embedded host communicating with the Kinetis Bootloader. Regardless of the host/master (PC or embedded host), the Kinetis Bootloader always uses a command protocol to communicate with that host/master. Commands are

provided to write to memory (internal flash or external Quad SPI flash memory or RAM), erase flash, and get/set bootloader options and property values. The host application can query the set of available commands.

On start-up, the bootloader reads optional configuration parameters from a fixed area on flash called the bootloader configuration area (BCA). These parameters can be modified by the write memory command or by downloaded flash image. BCA parameters include configuration data such as enabled peripherals, peripheral-specific settings, etc.

This chapter describes Kinetis Bootloader features, functionality, command structure and which peripherals are supported.

Features supported by the Kinetis Bootloader in Kinetis ROM:

- Supports USB, I2C, SPI, and LPUART peripheral interfaces
- Automatic detection of the active peripheral
- Ability to disable any peripheral
- LPUART peripheral implements autobaud
- Common packet-based protocol for all peripherals
- Packet error detection and retransmission
- Flash-resident configuration options
- Fully supports internal flash security, including ability to mass erase or unlock security via the backdoor key
- Protection of RAM used by the bootloader while it is running
- Provides command to read properties of the device, such as flash and RAM size
- Multiple options for executing the bootloader either at system start-up or under application control at runtime. The ability to configure the QuadSPI interface is based on a configuration block located in the external QuadSPI.

Table 8-2. Commands supported by the Kinetis Bootloader in ROM

Command	Description	When flash security is enabled, then this command is
Call	Runs user application code and returns control to bootloader	Not supported
Execute	Run user application code that never returns control to the bootloader	Not supported
FillMemory	Fill a range of bytes in flash with a word pattern	Not supported
FlashEraseAll	Erase the entire flash array	Not supported
FlashEraseRegion	Erase a range of sectors in flash	Not supported
WriteMemory	Write data to memory	Not supported
ReadMemory	Read data from memory	Not supported
FlashProgramOnce	Writes data provided in a command packet to a specified range of bytes in the program once field	Not supported

Table continues on the next page...

Table 8-2. Commands supported by the Kinetis Bootloader in ROM (continued)

Command	Description	When flash security is enabled, then this command is
FlashReadOnce	Returns the contents of the program once field by given index and byte count	Not supported
FlashReadResource	Returns the contents of the IFR field or Flash firmware ID, by given offset, byte count and option	Not supported
ConfigureQuadSpi	Configure the QuadSPI with a programmed configuration block	Supported
FlashSecurityDisable	Attempt to unlock flash security using the backdoor key	Supported
GetProperty	Get the current value of a property	Supported
ReceiveSbFile	Receive an SB file (which is generated by the elftosb tool)	Supported if the SB file is encrypted. See the SB File Decryption Support section for more details.
Reset	Reset the chip	Supported
SetProperty	Attempt to modify a writable property	Supported
FlashEraseAllUnsecure	Erase the entire flash array, including protected sectors	Supported

8.3 Functional Description

The following sub-sections describe the Kinetis Bootloader in K82F ROM functionality.

8.3.1 Memory Maps

While executing, the Kinetis Bootloader uses ROM and RAM memory.

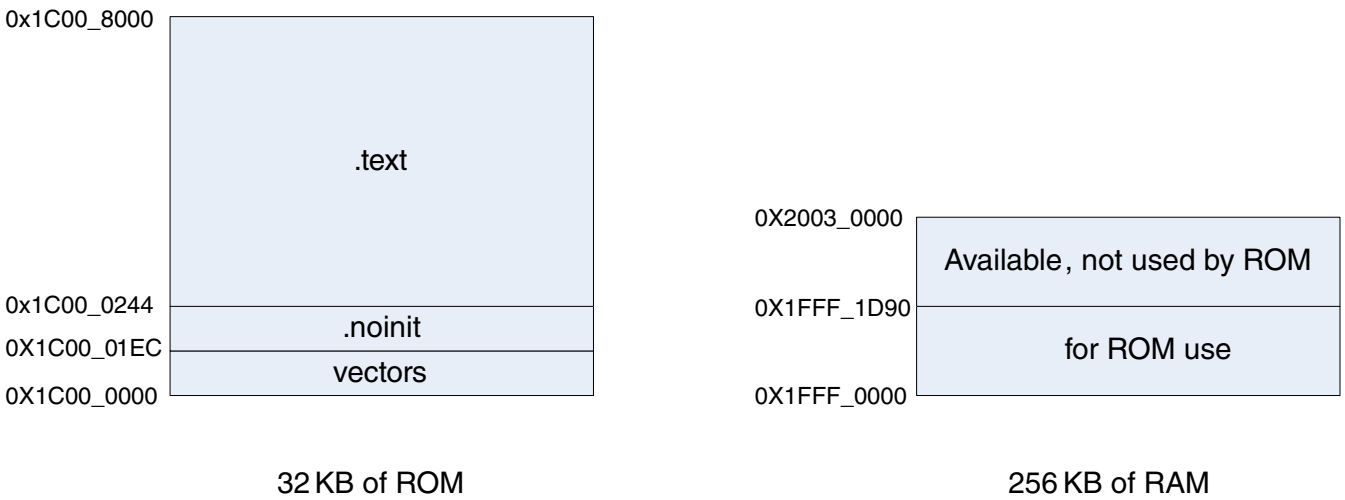


Figure 8-1. Kinetis Bootloader ROM/RAM Memory Maps

8.3.2 The Kinetis Bootloader Configuration Area (BCA)

The Kinetis Bootloader reads data from the Bootloader Configuration Area (BCA) to configure various features of the bootloader. The BCA resides in flash memory at offset 0x3C0, and provides all of the parameters needed to configure the Kinetis Bootloader operation. For uninitialized flash, the Kinetis Bootloader uses a predefined default configuration. A host application can use the Kinetis Bootloader to program the BCA for use during subsequent initializations of the bootloader.

Table 8-3. Configuration Fields for the Kinetis Bootloader

Offset	Size (bytes)	Configuration Field	Description
0x00 - 0x03	4	tag	Magic number to verify bootloader configuration is valid. Must be set to 'kcfg'.
0x04 - 0x07	4	crcStartAddress	Start address for application image CRC check. To generate the CRC, refer to the CRC chapter. If the bits are all set then Kinetis bootloader by default will not perform any CRC check.
0x08 - 0x0B	4	crcByteCount	Byte count for application image CRC check. If the bits are all set then Kinetis bootloader by default will not perform any CRC check.
0x0C - 0x0F	4	crcExpectedValue	Expected CRC value for application CRC check. If the bits are all set then Kinetis bootloader by default will not perform any CRC check.
0x10	1	enabledPeripherals	Bitfield of peripherals to enable.

Table continues on the next page...

Table 8-3. Configuration Fields for the Kinetis Bootloader (continued)

Offset	Size (bytes)	Configuration Field	Description
			bit 0 LPUART bit 1 I2C bit 2 SPI bit 4 USB Kinetis bootloader will enable the peripheral if corresponding bit is set to 1.
0x11	1	i2cSlaveAddress	If not 0xFF, used as the 7-bit I2C slave address. If 0xFF, defaults to 0x10 for I2C slave address
0x12 - 0x13	2	peripheralDetectionTimeout	Timeout in milliseconds for active peripheral detection. If 0xFFFF, defaults to 5 seconds.
0x14 - 0x15	2	usbVid	Sets the USB Vendor ID reported by the device during enumeration. If 0xFFFF, it defaults to 0x15A2.
0x16- 0x17	2	usbPid	Sets the USB Product ID reported by the device during enumeration.
0x18 - 0x1B	4	usbStringsPointer	Sets the USB Strings reported by the device during enumeration. Default string values are described in the USB peripheral section.
0x1C	1	clockFlags	See Table 8-5, clockFlags Configuration Field
0x1D	1	clockDivider	Inverted value of the divider to use for core and bus clocks when in high speed mode
0x1E	1	bootFlags	If bit 0 is cleared, then Kinetis bootloader will jump to either Quad SPI Flash or internal flash image depending on FOPT BOOTSRC_SEL bits. If the bit is set, then Kinetis bootloader will prepare for host communication over serial peripherals.
0x1F	1	pad byte	N/A
0x20	4	MMCAU configuration pointer	A pointer to the MMCAU configuration structure in memory. See the encryption section for details.
0x24	4	keyblob data pointer	A pointer to the keyblob data in memory. See the encryption section for details.
0x28	8	Reserved	-
0x30	4	qspiConfigBlockPointer	A pointer to the QSPI config block in internal flash array.
0x34	12	Reserved	-

NOTE

The flash sector containing the BCA should not be located in the execute-only region, because the Kinetis bootloader cannot read an execute-only region.

The first configuration field 'tag' is a tag value or magic number. The tag value must be set to 'kcfg' for the bootloader configuration data to be recognized as valid. If tag-field verification fails, then the Kinetis Bootloader assumes that the flash is not initialized and uses a predefined default configuration. The tag value is treated as a character string, so bytes 0-3 must be set as shown in the table.

Table 8-4. tag Configuration Field

Offset	tag Byte Value
0	'k' (0x6B)
1	'c' (0x63)
2	'f' (0x66)
3	'g' (0x67)

The flags in the clockFlags configuration field are enabled if the corresponding bit is cleared (0).

Table 8-5. clockFlags Configuration Field

Bit	Flag	Description
0	HighSpeed	Enable high speed mode (i.e., 48 MHz).
1 - 7	Reserved	

8.3.3 Start-up Process

Any of the following conditions will force the hardware to start the Kinetis Bootloader:

- BOOTSRC_SEL field of FOPT register is set to either 0b11 or 0b10. This forces the ROM to run out of reset.
- The BOOTCFG0 pin is asserted. The pin must be configured as BOOTCFG0 by setting the BOOTPIN_OPT bit of FOPT to 0.
- A user applications running on flash or RAM calls into the Kinetis Bootloader entry point address in ROM, to start Kinetis Bootloader execution.

The BOOTSRC_SEL bits (FOPT register, FOPT [7:6]) determine the boot source. The FOPT register is located in the flash configuration field at address 0x40D in the flash memory array. For a complete list of options, see the Boot options section in the Reset

and Boot chapter. If BOOTSRC_SEL is set to 0b11 or 0b10, then the device will boot to ROM out of reset. Flash memory defaults to all 1s when erased, so a blank chip will automatically boot to ROM.

The BOOTCFG0 pin is shared with the NMI pin, with NMI being the default usage. Regardless of whether the NMI pin is enabled or not, the NMI functionality is disabled if the ROM is executed out of reset, for as long as the ROM is running.

When the ROM is executed out of reset, vector fetches from the CPU are redirected to the ROM's vector table in ROM memory at offset 0x1C00_0000. This ensures that any exceptions will be handled by the ROM.

After the Kinetis Bootloader has started, the following procedure starts bootloader operations:

1. The RCM_MR [FORCEROM] bits are set, so that the device will reboot back into the ROM if/when the device is reset.
2. Initializes the bootloader's .data and .bss sections.
3. Reads bootloader configuration data from flash at address 0x3C0. The configuration data is only used if the tag field is set to the expected 'kcfg' value. If the tag is incorrect, then the configuration values are set to default, as if the data was all 0xFF bytes.
4. Clocks are configured. See the Clock Configuration section.
5. If BOOTSRC_SEL is set to 0b10, then the QSPI0 interface is configured by reading the configuration block from the base address of the external QuadSPI, or from the address pointed by the qspiConfigBlockPointer in the BCA.
6. Enabled peripherals are initialized.
7. The bootloader waits for communication to begin on a peripheral.
   - If detection times out, then the bootloader jumps to the user application in flash. See Bootloader Exit state section.
   - If communication is detected, then all inactive peripherals are shut down, and the command phase is entered.

NOTE

The flash sector containing the vector table should not be located in the execute-only region, because the Kinetis bootloader cannot read the PC and SP addresses in an execute-only region.

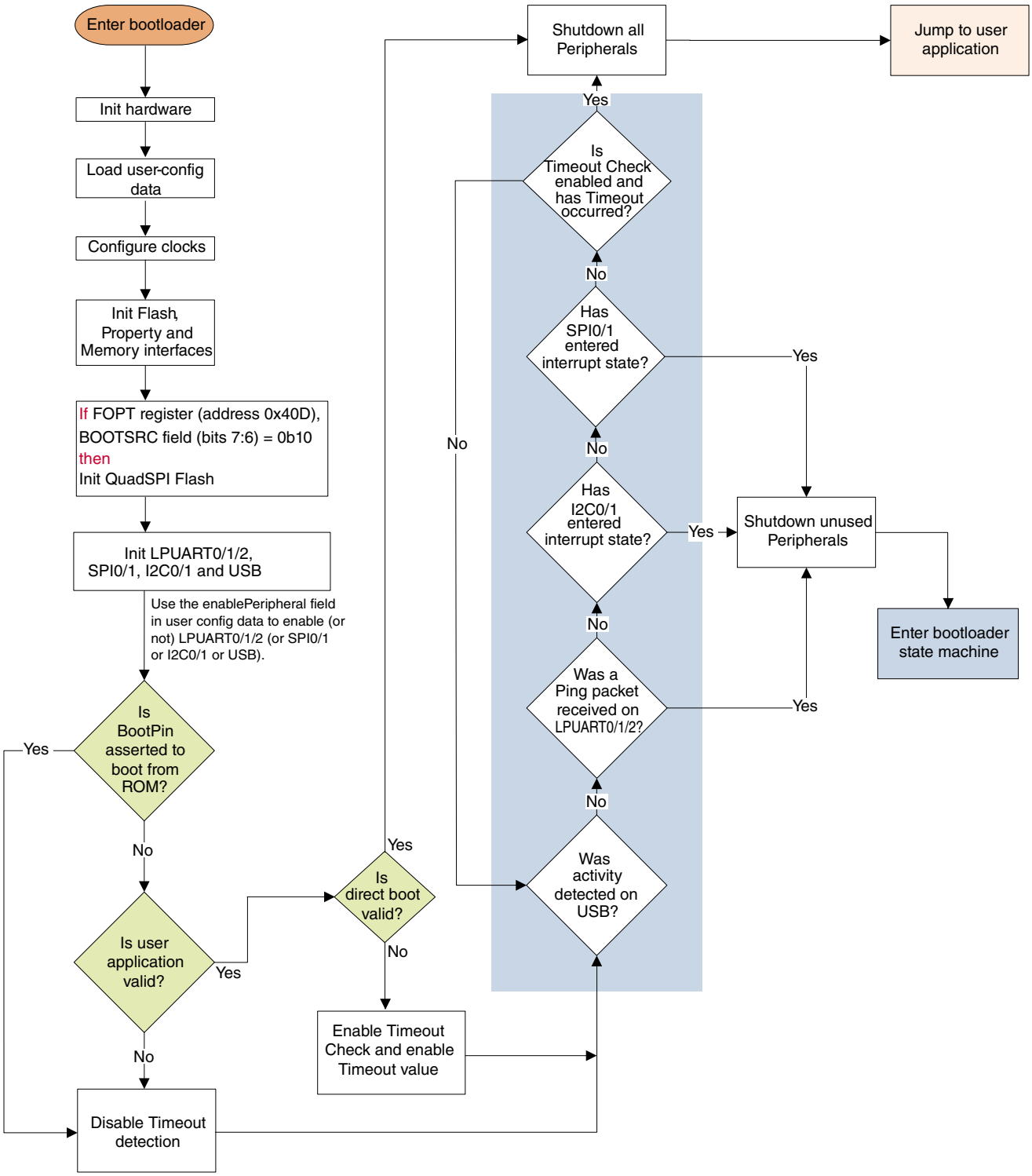


Figure 8-2. Kinetis Bootloader Start-up Flowchart

8.3.4 Clock Configuration

By default, the bootloader does not modify clocks. The Kinetis Bootloader in ROM will use the clock configuration of the chip out of reset unless the clock configuration bits in the FOPT register are cleared, or if a USB peripheral is enabled.

- Alternate clock configurations are supported, by setting fields in the Bootloader Configuration Area (BCA) shown in Table 8-3.
- If the HighSpeed flag of the clockFlags configuration value is cleared, or if a USB peripheral is enabled, the bootloader will enable the internal 48 MHz reference clock.
- In high speed mode, the core and bus clock frequencies are determined by the clockDivider configuration value.
- The core clock divider is set directly from the inverted value of the clockDivider unless a USB peripheral is enabled. If a USB peripheral is enabled and the inverted value of the clockDivider is greater than 2, then the value is reduced to 2, in order to keep the CPU clock above 20 MHz.
- The bus clock divider is set to 1, unless the resulting bus clock frequency would be greater than the maximum supported value. In this case, the bus clock divider is increased until the bus clock frequency is at or below the maximum.
- Note that the maximum baud rate of serial peripherals is related to the core and bus clock frequencies. To achieve the desired baud rates, high speed mode should be enabled in BCA.

8.3.5 Bootloader Entry Point

The Kinetis Bootloader provides a function (runBootloader) that a user application can call, to run the bootloader.

To get the address of the entry point, the user application reads the word containing the pointer to the bootloader API tree at offset 0x1C of the bootloader's vector table. The vector table is placed at the base of the bootloader's address range, which for the ROM is 0x1C00_0000. Thus, the API tree pointer is at address 0x1C00_001C.

The bootloader API tree is a structure that contains pointers to other structures, which have the function and data addresses for the bootloader. The bootloader entry point is always the first word of the API tree.

The prototype of the entry point is:

```
void run_bootloader(void * arg);
```

The arg parameter is currently unused, and is intended for future expansion (for example, passing options to the bootloader). To ensure future compatibility, a value of NULL should be passed for arg.

Example code to get the entry pointer address from the ROM and start the bootloader.

NOTE

This entry must be called in supervisor (privileged) mode.

```
// Variables

uint32_t runBootloaderAddress;

void (*runBootloader)(void * arg);


// Read the function address from the ROM API tree.

runBootloaderAddress = **(uint32_t **)(0x1c00001c);

runBootloader = (void (*)(void * arg))runBootloaderAddress;


// Start the bootloader.

runBootloader(NULL);
```

8.3.6 Bootloader Protocol

This section explains the general protocol for the packet transfers between the host and the Kinetis Bootloader. The description includes the transfer of packets for different transactions, such as commands with no data phase and commands with incoming or outgoing data phase. The next section describes various packet types used in a transaction.

Each command sent from the host is replied to with a response command.

Commands may include an optional data phase:

- If the data phase is **incoming** (from host to bootloader), then the data phase is part of the **original command**.
- If the data phase is **outgoing** (from bootloader to host), then the data phase is part of the **response command**.

NOTE

In all protocols (described in the next subsections), the Ack sent in response to a Command or Data packet can arrive at any time *before, during, or after* the Command/Data packet has processed.

8.3.6.1 Command with no data phase

The protocol for a command with no data phase contains:

- Command packet (from host)
- Generic response command packet (to host)

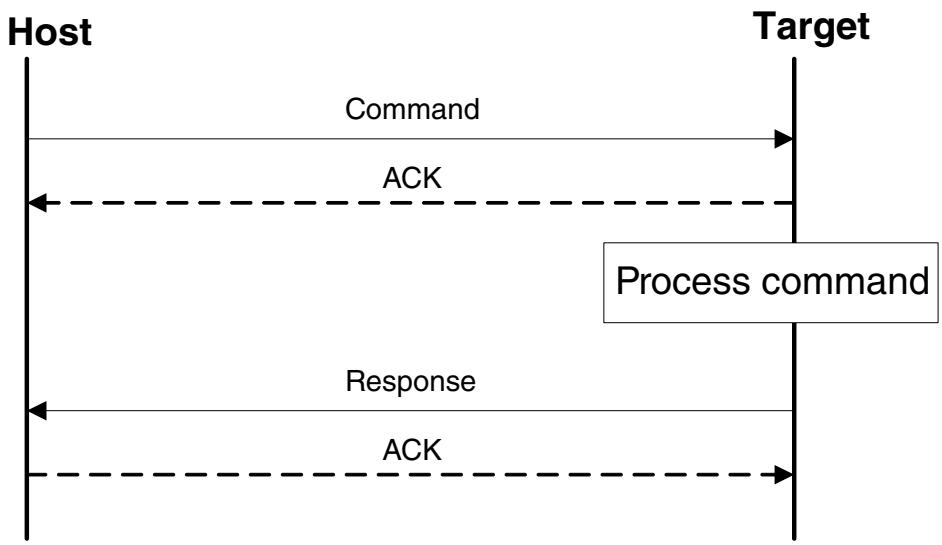


Figure 8-3. Command with No Data Phase

8.3.6.2 Command with incoming data phase

The protocol for a command with an incoming data phase contains:

- Command packet (from host)
- Generic response command packet (to host)
- Incoming data packets (from host)
- Generic response command packet (to host)

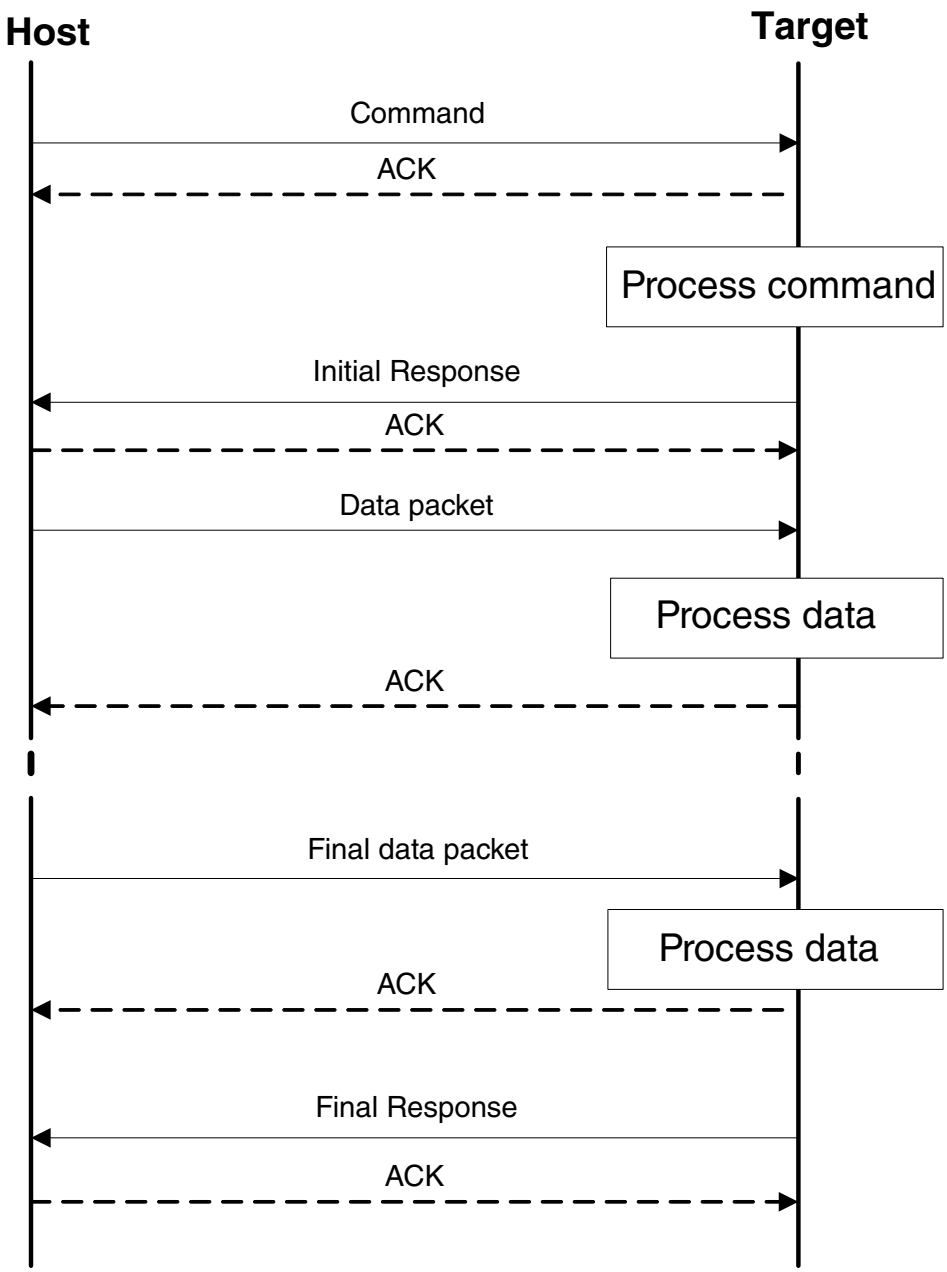


Figure 8-4. Command with incoming data phase

NOTE

- The host may not send any further packets while it (the host) is waiting for the response to a command.
- If the Generic Response packet prior to the start of the data phase does not have a status of kStatus_Success, then the data phase is aborted.
- Data phases may be aborted by the receiving side by sending the final Generic Response early with a status of

kStatus_AbortDataPhase. The host may abort the data phase early by sending a zero-length data packet.
- The final Generic Response packet *sent after the data phase* includes the status for the entire operation.

8.3.6.3 Command with outgoing data phase

The protocol for a command with an outgoing data phase contains:
- Command packet (from host)
- ReadMemory Response command packet (to host) (kCommandFlag_HasDataPhase set)
- Outgoing data packets (to host)
- Generic response command packet (to host)

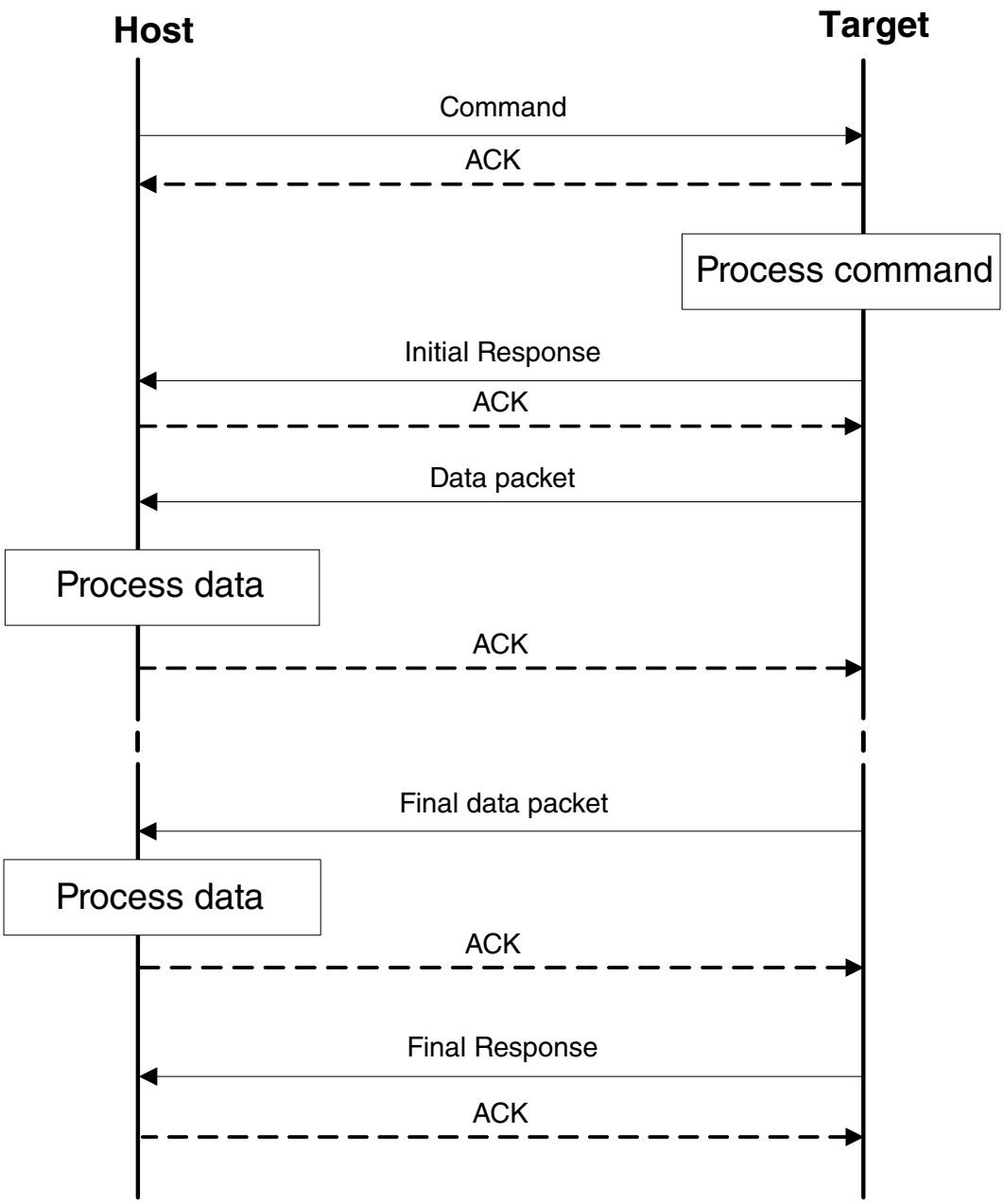


Figure 8-5. Command with outgoing data phase

NOTE

- For the outgoing data phase sequence above, the data phase is really considered part of the response command.
- The host may not send any further packets while it (the host) is waiting for the response to a command.
- If the ReadMemory Response command packet prior to the start of the data phase does not contain the kCommandFlag_HasDataPhase flag, then the data phase is aborted.

- Data phases may be aborted by the host sending the final Generic Response early with a status of kStatus_AbortDataPhase. The sending side may abort the data phase early by sending a zero-length data packet.
- The final Generic Response packet *sent after the data phase* includes the status for the entire operation.

8.3.7 Bootloader Packet Types

The Kinetis Bootloader device works in slave mode. All data communication is initiated by a host, which is either a PC or an embedded host (note that QuadSPI is treated like a storage device, like flash). The Kinetis Bootloader device is the target, which receives a command or data packet. All data communication between host and target is packetized.

NOTE

The term "target" refers to the "Kinetis Bootloader device."

There are 6 types of packets used in the device:

- Ping packet
- Ping Response packet
- Framing packet
- Command packet
- Data packet
- Response packet

All fields in the packets are in little-endian byte order.

8.3.7.1 Ping packet

The Ping packet is the first packet sent from a host to the target (Kinetis Bootloader), to establish a connection on a selected peripheral. For a LPUART peripheral, the Ping packet is used to determine the baudrate. A Ping packet must be sent before any other communications. In response to a Ping packet, the target sends a Ping Response packet.

Table 8-6. Ping Packet Format

Byte #	Value	Name
0	0x5A	start byte
1	0xA6	ping

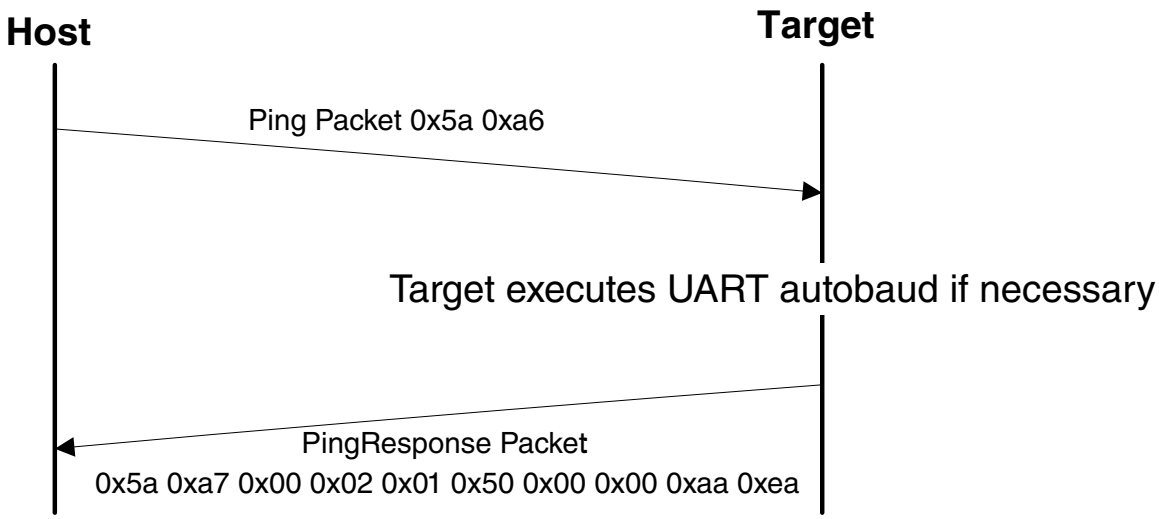


Figure 8-6. Ping Packet Protocol Sequence

8.3.7.2 Ping Response Packet

The target (Kinetis Bootloader) sends a Ping Response packet back to the host after receiving a Ping packet. If communication is over a LPUART peripheral, the target uses the incoming Ping packet to determine the baud rate before replying with the Ping Response packet. Once the Ping Response packet is received by the host, the connection is established, and the host starts sending commands to the target (Kinetis Bootloader).

Table 8-7. Ping Response Packet Format

Byte #	Value	Parameter
0	0x5A	start byte
1	0xA7	Ping response code
2		Protocol bugfix
3		Protocol minor
4		Protocol major
5		Protocol name = 'P' (0x50)
6		Options low
7		Options high
8		CRC16 low
9		CRC16 high

8.3.7.3 Framing Packet

The framing packet is used for flow control and error detection, and it (the framing packet) wraps command and data packets as well.

The framing packet described in this section is used for serial peripherals including LPUART, I2C and SPI. The USB HID peripheral does not use framing packets. Instead, the packetization inherent in the USB protocol itself is used. Please refer to the USB peripheral section for details.

Table 8-8. Framing Packet Format

Byte #	Value	Parameter	
0	0x5A	start byte	
1		packetType	
2		length_low	Length is a 16-bit field that specifies the entire command or data packet size in bytes.
3		length_high	
4		crc16_low	This is a 16-bit field. The CRC16 value covers entire framing packet, including the start byte and command or data packets, but does not include the CRC bytes. See the CRC16 algorithm after this table.
5		crc16_high	
6 . . .n		Command or Data packet payload	

A special framing packet that contains only a start byte and a packet type is used for synchronization between the host and target.

Table 8-9. Special Framing Packet Format

Byte #	Value	Parameter
0	0x5A	start byte
1	0xA*n*	packetType

The Packet Type field specifies the type of the packet from one of the defined types (below):

Table 8-10. packetType Field

packetType	Name	Description
0xA1	kFramingPacketType_Ack	The previous packet was received successfully; the sending of more packets is allowed.
0xA2	kFramingPacketType_Nak	The previous packet was corrupted and must be re-sent.
0xA3	kFramingPacketType_AckAbort	Data phase is being aborted.
0xA4	kFramingPacketType_Command	The framing packet contains a command packet payload.
0xA5	kFramingPacketType_Data	The framing packet contains a data packet payload.

Table continues on the next page...

Table 8-10. packetType Field (continued)

packetType	Name	Description
0xA6	kFramingPacketType_Ping	Sent to verify the other side is alive. Also used for UART autobaud.
0xA7	kFramingPacketType_PingResponse	A response to Ping; contains the framing protocol version number and options.

This device uses the Cyclic Redundancy Check module (CRC) to perform the CRC algorithm. See the CRC chapter for more details.

8.3.7.4 Command packet

The command packet carries a 32-bit command header and a list of 32-bit parameters.

Table 8-11. Command Packet Format

Command Packet Format (32 bytes)										
Command Header (4 bytes)				28 bytes for Parameters (Max 7 parameters)						
Tag	Flags	Rsvd	Param Count	Param1 (32-bit)	Param2 (32-bit)	Param3 (32-bit)	Param4 (32-bit)	Param5 (32-bit)	Param6 (32-bit)	Param7 (32-bit)
byte 0	byte 1	byte 2	byte 3							

Table 8-12. Command Header Format

Byte #	Command Header Field	
0	Command or Response tag	The command header is 4 bytes long, with these fields.
1	Flags	
2	Reserved. Should be 0x00.	
3	ParameterCount	

The header is followed by 32-bit parameters up to the value of the ParameterCount field specified in the header. Because a command packet is 32 bytes long, only 7 parameters can fit into the command packet.

Command packets are also used by the target to send responses back to the host. As mentioned earlier, command packets and data packets are embedded into framing packets for all of the transfers.

Table 8-13. Commands that are supported

Command	Name
0x01	FlashEraseAll

Table continues on the next page...

Table 8-13. Commands that are supported (continued)

Command	Name
0x02	FlashEraseRegion
0x03	ReadMemory
0x04	WriteMemory
0x05	FillMemory
0x06	FlashSecurityDisable
0x07	GetProperty
0x08	ReceiveSBFile
0x09	Execute
0x10	FlashReadResource
0x11	ConfigureQuadSpi
0x0A	Call
0x0B	Reset
0x0C	SetProperty
0x0D	FlashEraseAllUnsecure
0x0E	FlashProgramOnce
0x0F	FlashReadOnce

Table 8-14. Responses that are supported

Response	Name
0xA0	GenericResponse
0xA7	GetPropertyResponse (used for sending responses to GetProperty command only)
0xA3	ReadMemoryResponse (used for sending responses to ReadMemory command only)
0xAF	FlashReadOnceResponse (used for sending responses to FlashReadOnce command only)
0xB0	FlashReadResourceResponse (used for sending responses to FlashReadResource command only)

Flags: Each command packet contains a Flag byte. Only bit 0 of the flag byte is used. If bit 0 of the flag byte is set to 1, then data packets will follow in the command sequence. The number of bytes that will be transferred in the data phase is determined by a command-specific parameter in the parameters array.

ParameterCount: The number of parameters included in the command packet.

Parameters: The parameters are word-length (32 bits). With the default maximum packet size of 32 bytes, a command packet can contain up to 7 parameters.

8.3.7.5 Data packet

The data packet carries just the data, either host sending data to target, or target sending data to host. The data transfer direction is determined by the last command sent from the host. The data packet is also wrapped within a framing packet, to ensure the correct packet data is received.

The contents of a data packet are simply the data itself. There are no other fields, so that the most data per packet can be transferred. Framing packets are responsible for ensuring that the correct packet data is received.

8.3.7.6 Response packet

The responses are carried using the same command packet format wrapped with framing packet data. Types of responses include:

- GenericResponse
- GetPropertyResponse
- ReadMemoryResponse
- FlashReadOnceResponse
- FlashReadResourceResponse

GenericResponse: After the Kinetis Bootloader has processed a command, the bootloader will send a generic response with status and command tag information to the host. The generic response is the last packet in the command protocol sequence. The generic response packet contains the framing packet data and the command packet data (with generic response tag = 0xA0) and a list of parameters (defined in the next section). The parameter count field in the header is always set to 2, for status code and command tag parameters.

Table 8-15. GenericResponse Parameters

Byte #	Parameter	Descripton
0 - 3	Status code	The Status codes are errors encountered during the execution of a command by the target (Kinetis Bootloader). If a command succeeds, then a kStatus_Success code is returned. Table 8-61, Kinetis Bootloader Status Error Codes, lists the status codes returned to the host by the Kinetis Bootloader for K82F ROM.
4 - 7	Command tag	The Command tag parameter identifies the response to the command sent by the host.

GetPropertyResponse: The GetPropertyResponse packet is sent by the target in response to the host query that uses the GetProperty command. The GetPropertyResponse packet contains the framing packet data and the command packet data, with the command/response tag set to a GetPropertyResponse tag value (0xA7).

The parameter count field in the header is set to greater than 1, to always include the status code and one or many property values.

Table 8-16. GetPropertyResponse Parameters

Byte #	Value	Parameter
0 - 3		Status code
4 - 7		Property value
. . .		. . .
		Can be up to maximum 6 property values, limited to the size of the 32-bit command packet and property type.

ReadMemoryResponse: The ReadMemoryResponse packet is sent by the target in response to the host sending a ReadMemory command. The ReadMemoryResponse packet contains the framing packet data and the command packet data, with the command/response tag set to a ReadMemoryResponse tag value (0xA3), the flags field set to kCommandFlag_HasDataPhase (1).

The parameter count set to 2 for the status code and the data byte count parameters shown below.

Table 8-17. ReadMemoryResponse Parameters

Byte #	Parameter	Descripton
0 - 3	Status code	The status of the associated Read Memory command.
4 - 7	Data byte count	The number of bytes sent in the data phase.

FlashReadOnceResponse: The FlashReadOnceResponse packet is sent by the target in response to the host sending a FlashReadOnce command. The FlashReadOnceResponse packet contains the framing packet data and the command packet data, with the command/response tag set to a FlashReadOnceResponse tag value (0xAF), and the flags field set to 0. The parameter count is set to 2 plus *the number of words* requested to be read in the FlashReadOnceCommand.

Table 8-18. FlashReadOnceResponse Parameters

Byte #	Value	Parameter
0 – 3		Status Code

Table continues on the next page...

Table 8-18. FlashReadOnceResponse Parameters (continued)

4 – 7		Byte count to read
…		…
		Can be up to 20 bytes of requested read data.

The FlashReadResourceResponse packet is sent by the target in response to the host sending a FlashReadResource command. The FlashReadResourceResponse packet contains the framing packet data and command packet data, with the command/response tag set to a FlashReadResourceResponse tag value (0xB0), and the flags field set to kCommandFlag_HasDataPhase (1).

Table 8-19. FlashReadResourceResponse Parameters

Byte #	Value	Parameter
0 – 3		Status Code
4 – 7		Data byte count

8.3.8 Bootloader Command API

All Kinetis Bootloader command APIs follow the command packet format that is wrapped by the framing packet, as explained in previous sections.

- For a list of commands supported by the Kinetis Bootloader in K82F ROM, see Table 8-2, Commands supported.
- For a list of status codes returned by the Kinetis Bootloader in K82F ROM, see Table 8-61, Kinetis Bootloader Status Error Codes.

NOTE

All the examples in this section depict byte traffic on serial peripherals that use framing packets. USB HID transactions use the USB HID report packets instead of the serial framing packets shown in this section. Please refer to the HID reports section for details of the USB HID packet structure.

8.3.8.1 Call command

The Call command will execute a function that is written in memory at the address sent in the command. The address needs to be a valid memory location residing in accessible flash (internal or external) or in RAM. The command supports the passing of one 32-bit

argument. Although the command supports a stack address, at this time the call will still take place using the current stack pointer. After execution of the function, a 32-bit return value will be returned in the generic response message.

Table 8-20. Parameters for Call Command

Byte #	Command
0 - 3	Call address
4 - 7	Argument word
8 - 11	Stack pointer

Response: The target (Kinetis Bootloader) will return a GenericResponse packet with a status code either set to the return value of the function called or set to kStatus_InvalidArgument (105).

8.3.8.2 ConfigureQuadSPI command

The ConfigureQuadSPI command will configure the QuadSPI device using a pre-programmed configuration image. The parameters passed in the command are the QuadSPI memory ID, which should always be 1 for the current release of the bootloader, and then the memory address from which the configuration data can be loaded from. Options for loading the data can be a scenario where the configuration data is written to a RAM or flash location and then this command will direct the bootloader to use the data at that location to configure the QuadSPI.

Table 8-21. Parameters for ConfigureQuadSPI Command

Byte #	Command
0 – 3	Flash Memory ID (Should always be 1)
4 – 7	Configuration block address

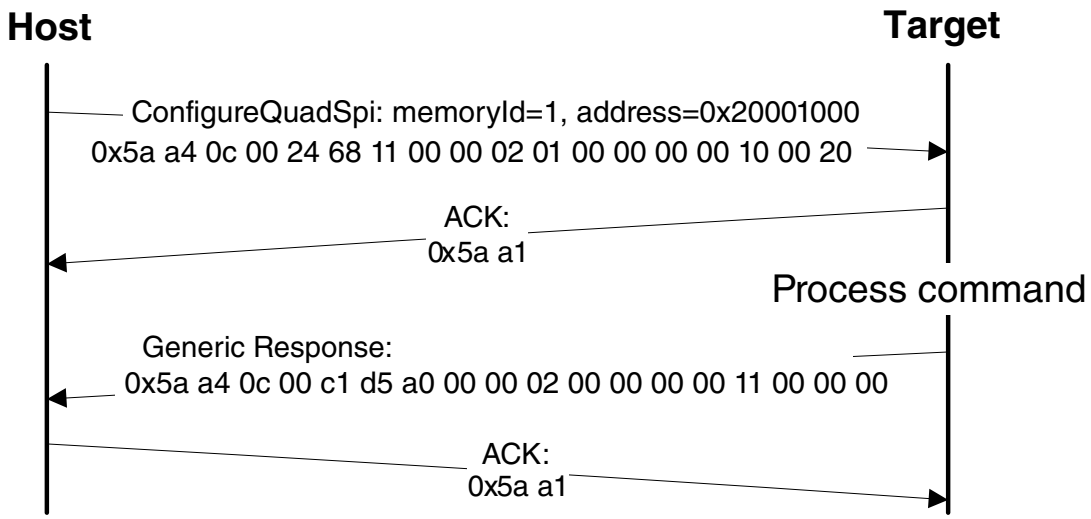


Figure 8-7. Protocol Sequence for Configure QuadSPI Command

Response: The target (Kinetis Bootloader) will return a GenericResponse packet with a status code either set to kStatus_Success upon successful execution of the command, or set to an appropriate error code.

8.3.8.3 ReceiveSBFile command

The ReceiveSBFile command (ReceiveSbFile) will start the transfer of an SB file to the target. The command only specifies the size in bytes of the SB file that will be sent in the data phase. The SB file will be processed as it is received by the bootloader.

Table 8-22. Parameters for ReceiveSBFile Command

Byte #	Command
0 - 3	Byte count

Data Phase: The Receive SB file command has a data phase; the host will send data packets until the number of bytes of data specified in the byteCount parameter of the Receive SB File command are received by the target.

Response: The target (Bootloader) will return a GenericResponse packet with a status code set to the kStatus_Success upon successful execution of the command, or set to an appropriate error code.

8.3.8.4 Execute command

The execute command results in the bootloader setting the program counter to the code at the provided jump address, R0 to the provided argument, and a Stack pointer to the provided stack pointer address. Prior to the jump, the system is returned to the reset state.

The Jump address, function argument pointer, and stack pointer are the parameters required for the Execute command.

Table 8-23. Parameters for Execute Command

Byte #	Command
0 - 3	Jump address
4 - 7	Argument word
8 - 11	Stack pointer address

The Execute command has no data phase.

Response: Before executing the Execute command, the target (Kinetis Bootloader) will validate the parameters and return a GenericResponse packet with a status code either set to kStatus_Success or an appropriate error status code.

8.3.8.5 Reset command

The Reset command will result in bootloader resetting the chip.

The Reset command requires no parameters.

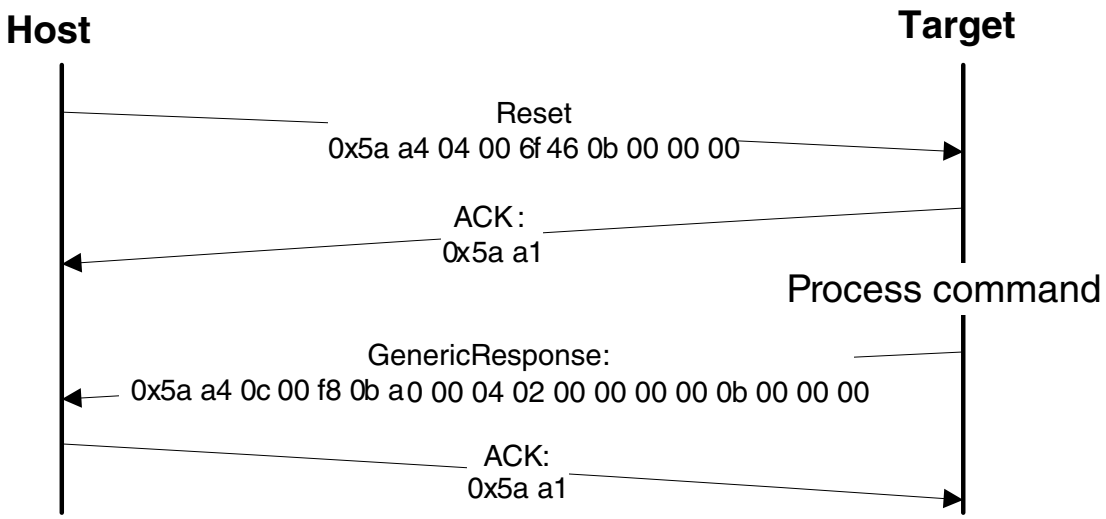


Figure 8-8. Protocol Sequence for Reset Command

Table 8-24. Reset Command Packet Format (Example)

Reset	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4, kFramingPacketType_Command
	length	0x04 0x00
	crc16	0x6F 0x46
Command packet	commandTag	0x0B - reset
	flags	0x00
	reserved	0x00
	parameterCount	0x00

The Reset command has no data phase.

Response: The target (Kinetis Bootloader) will return a GenericResponse packet with status code set to kStatus_Success, before resetting the chip.

8.3.8.6 GetProperty command

The GetProperty command is used to query the bootloader about various properties and settings. Each supported property has a unique 32-bit tag associated with it. The tag occupies the first parameter of the command packet. The target returns a GetPropertyResponse packet with the property values for the property identified with the tag in the GetProperty command.

Properties are the defined units of data that can be accessed with the GetProperty or SetProperty commands. Properties may be read-only or read-write. All read-write properties are 32-bit integers, so they can easily be carried in a command parameter.

For a list of properties and their associated 32-bit property tags supported by the Kinetis Bootloader in K82F ROM, see Table 8-56.

The 32-bit property tag is the only parameter required for GetProperty command.

Table 8-25. Parameters for GetProperty Command

Byte #	Command
0 - 3	Property tag
4 - 7	External memory identifier, which is only valid when using the GetProperty command for an external memory

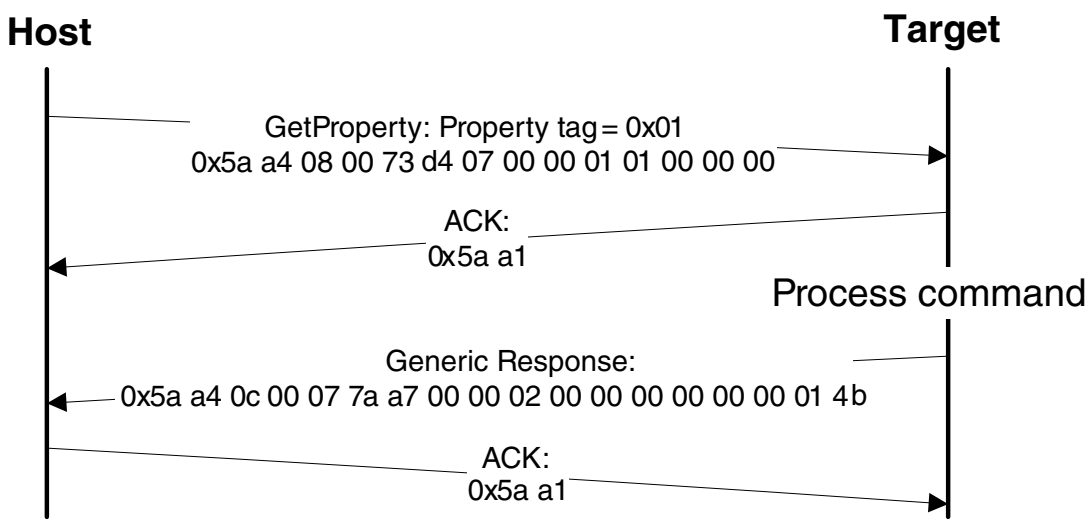


Figure 8-9. Protocol Sequence for GetProperty Command

Table 8-26. GetProperty Command Packet Format (Example)

GetProperty	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4, kFramingPacketType_Command
	length	0x08 0x00
	crc16	0x73 0xD4
Command packet	commandTag	0x07 – GetProperty
	flags	0x00
	reserved	0x00
	parameterCount	0x01
	propertyTag	0x00000001 - CurrentVersion

The GetProperty command has no data phase.

Response: In response to a GetProperty command, the target will send a GetPropertyResponse packet with the response tag set to 0xA7. The parameter count indicates the number of parameters sent for the property values, with the first parameter showing status code 0, followed by the property value(s). The next table shows an example of a GetPropertyResponse packet.

Table 8-27. GetProperty Response Packet Format (Example)

GetPropertyResponse	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4, kFramingPacketType_Command
	length	0x0c 0x00 (12 bytes)
	crc16	0x07 0x7a
Command packet	responseTag	0xA7
	flags	0x00
	reserved	0x00
	parameterCount	0x02
	status	0x00000000
	propertyValue	0x0000014b - CurrentVersion

8.3.8.7 SetProperty command

The SetProperty command is used to change or alter the values of the properties or options in the Kinetis Bootloader ROM. However, the SetProperty command can only change the value of properties that are writable—see Table 8-56, Properties used by Get/SetProperty Commands. If you try to set a value for a read-only property, then the Kinetis Bootloader will return an error.

The property tag and the new value to set are the 2 parameters required for the SetProperty command.

Table 8-28. Parameters for SetProperty Command

Byte #	Command
0 - 3	Property tag
4 - 7	Property value

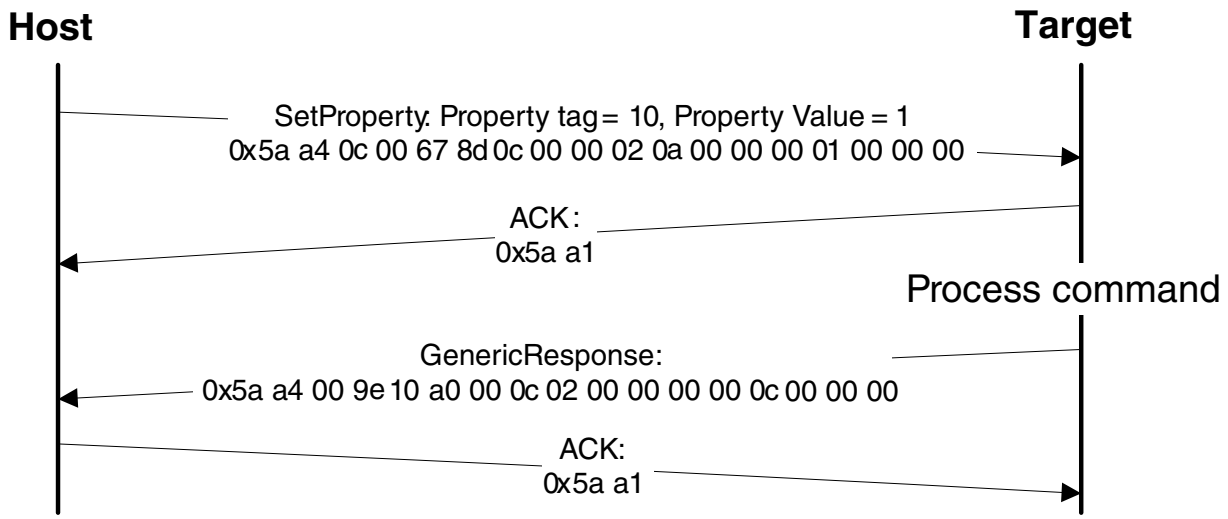


Figure 8-10. Protocol Sequence for SetProperty Command

Table 8-29. SetProperty Command Packet Format (Example)

SetProperty	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4, kFramingPacketType_Command
	length	0x0C 0x00
	crc16	0x67 0x8D
Command packet	commandTag	0x0C – SetProperty with property tag 10
	flags	0x00
	reserved	0x00
	parameterCount	0x02
	propertyTag	0x0000000A - VerifyWrites
	propertyValue	0x00000001

The SetProperty command has no data phase.

Response: The target (Kinetis Bootloader) will return a GenericResponse packet with one of following status codes:

Table 8-30. SetProperty Response Status Codes

Status Code
kStatus_Success
kStatus_ReadOnly
kStatus_UnknownProperty
kStatus_InvalidArgument

8.3.8.8 FlashEraseAll command

The FlashEraseAll command performs an erase of the entire flash memory or of QuadSPI memory (if that is the case). If any flash regions are protected, then the FlashEraseAll command will fail and return an error status code. Executing the FlashEraseAll command will release flash security if it (flash security) was enabled, by setting the FTFA_FSEC register. However, the FSEC field of the flash configuration field is erased, so unless it is reprogrammed, the flash security will be re-enabled after the next system reset. The Command tag for FlashEraseAll command is 0x01 set in the commandTag field of the command packet.

The FlashEraseAll command requires no parameters.

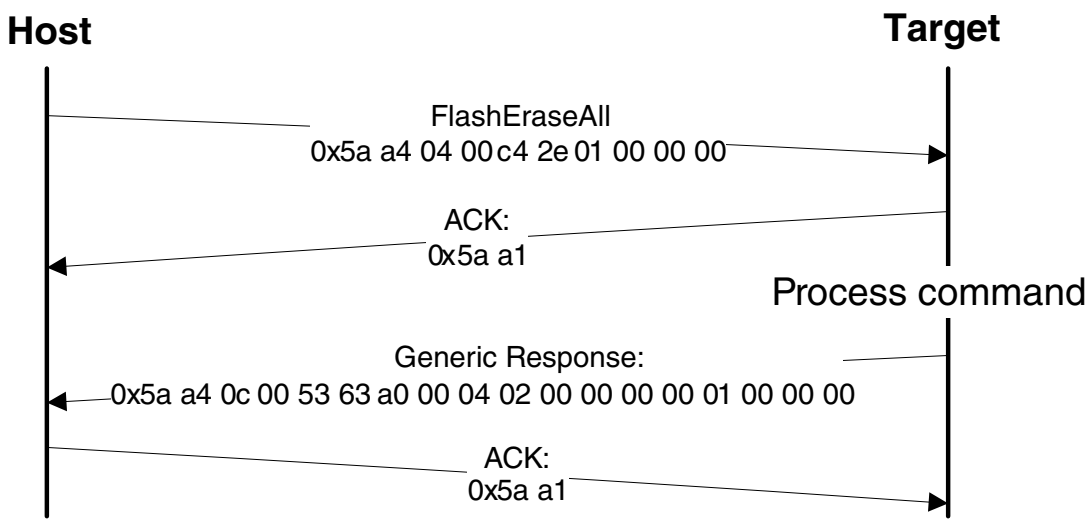


Figure 8-11. Protocol Sequence for FlashEraseAll Command

Table 8-31. FlashEraseAll Command Packet Format (Example)

FlashEraseAll	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4, kFramingPacketType_Command
	length	0x04 0x00
	crc16	0xC4 0x2E
Command packet	commandTag	0x01 - FlashEraseAll
	flags	0x00
	reserved	0x00
	parameterCount	0x00

The FlashEraseAll command has no data phase.

Response: The target (Kinetis Bootloader) will return a GenericResponse packet with status code either set to kStatus_Success for successful execution of the command, or set to an appropriate error status code.

8.3.8.9 FlashEraseRegion command

The FlashEraseRegion command performs an erase of one or more sectors of the flash memory or a specified range of flash within the connected SPI flash devices.

The start address and number of bytes are the 2 parameters required for the FlashEraseRegion command. The start and byte count parameters must be , or the FlashEraseRegion command will fail and return kStatus_FlashAlignmentError (0x101). If the region specified does not fit in the flash memory space, the FlashEraseRegion command will fail and return kStatus_FlashAddressError (0x102). If any part of the region specified is protected, the FlashEraseRegion command will fail and return kStatus_MemoryRangeInvalid (0x10200).

Table 8-32. Parameters for FlashEraseRegion Command

Byte #	Parameter
0 - 3	Start address
4 - 7	Byte count

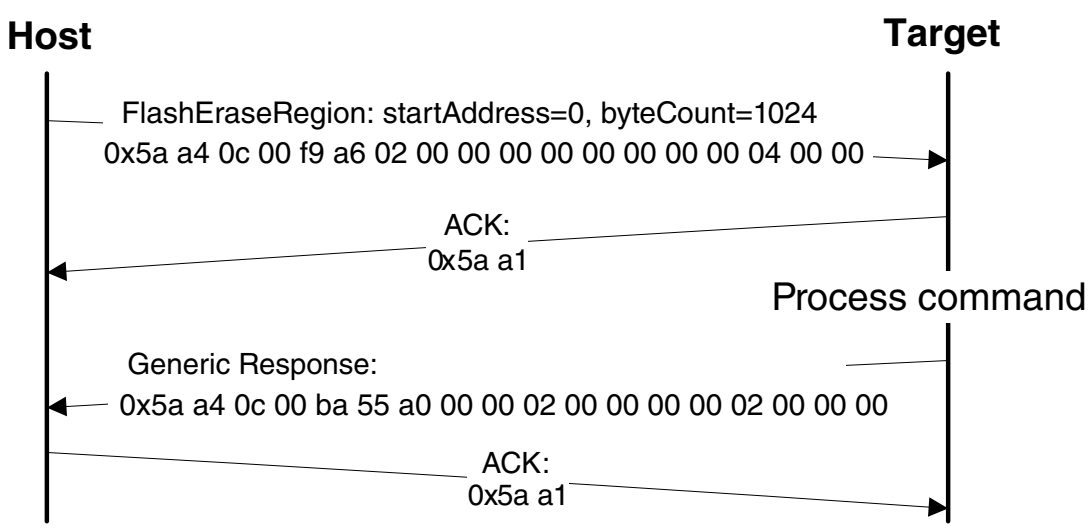


Figure 8-12. Protocol Sequence for FlashEraseRegion Command

Table 8-33. FlashEraseRegion Command Packet Format (Example)

FlashEraseRegion	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4, kFramingPacketType_Command
	length	0x0C 0x00
	crc16	0xF9 0x A6
Command packet	commandTag	0x02, kCommandTag_FlashEraseRegion
	flags	0x00
	reserved	0x00
	parameterCount	0x02
	startAddress	0x00 0x00 0x00 0x00 (0x0000_0000)
	byte count	0x00 0x04 0x00 0x00 (0x400)

The FlashEraseRegion command has no data phase.

Response: The target (Kinetis Bootloader) will return a GenericResponse packet with one of following error status codes.

Table 8-34. FlashEraseRegion Response Status Codes

Status Code
kStatus_Success (0x0)
kStatus_MemoryRangeInvalid (0x10200)
kStatus_FlashAlignmentError (0x101)
kStatus_FlashAddressError (0x102)
kStatus_FlashAccessError (0x103)
kStatus_FlashProtectionViolation (0x104)
kStatus_FlashCommandFailure (0x105)

8.3.8.10 FlashEraseAllUnsecure command

The FlashEraseAllUnsecure command performs a mass erase of the flash memory, including protected sectors. Flash security is immediately disabled if it (flash security) was enabled, and the FSEC byte in the flash configuration field at address 0x40C is programmed to 0xFE. However, if the mass erase enable option in the FSEC field is disabled, then the FlashEraseAllUnsecure command will fail.

The FlashEraseAllUnsecure command requires no parameters.

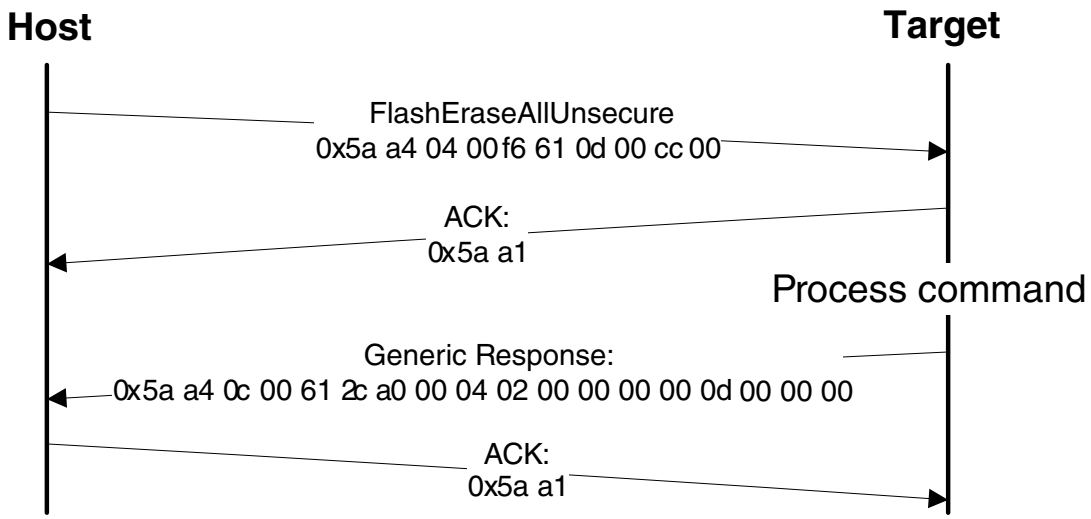


Figure 8-13. Protocol Sequence for FlashEraseAll Command

Table 8-35. FlashEraseAllUnsecure Command Packet Format (Example)

FlashEraseAllUnsecure	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4, kFramingPacketType_Command
	length	0x04 0x00
	crc16	0xF6 0x61
Command packet	commandTag	0x0D - FlashEraseAllUnsecure
	flags	0x00
	reserved	0x00
	parameterCount	0x00

The FlashEraseAllUnsecure command has no data phase.

Response: The target (Kinetis Bootloader) will return a GenericResponse packet with status code either set to kStatus_Success for successful execution of the command, or set to an appropriate error status code.

8.3.8.11 FlashProgramOnce command

The FlashProgramOnce command writes data (that is provided in a command packet) to a specified range of bytes in the program once field. Special care must be taken when writing to the program once field.

- The program once field only supports programming once, so any attempted to reprogram a program once field will get an error response.
- Writing to the program once field requires the byte count to be 4-byte aligned or 8-byte aligned.

The FlashProgramOnce command uses 3 parameters: index, byteCount, data.

Table 8-36. Parameters for FlashProgramOnce Command

Byte #	Command
0 - 3	Index of program once field
4 - 7	Byte count (must be evenly divisible by 4)
8 - 11	Data
12 - 16	Data

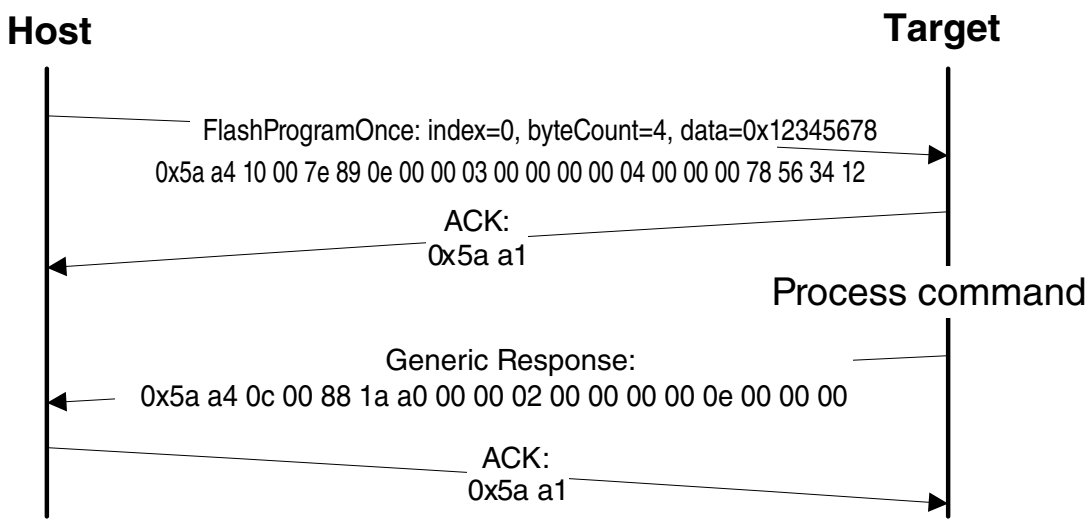


Figure 8-14. Protocol Sequence for FlashProgramOnce Command

Table 8-37. FlashProgramOnce Command Packet Format (Example)

FlashProgramOnce	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4, kFramingPacketType_Command
	length	0x10 0x00
	crc16	0x7E4 0x89
Command packet	commandTag	0x0E – FlashProgramOnce
	flags	0
	reserved	0
	parameterCount	3
	index	0x0000_0000

Table continues on the next page...

Table 8-37. FlashProgramOnce Command Packet Format (Example) (continued)

FlashProgramOnce	Parameter	Value
	byteCount	0x0000_0004
	data	0x1234_5678

Response: upon successful execution of the command, the target (Kinetis Flashloader) will return a GenericResponse packet with a status code set to kStatus_Success, or to an appropriate error status code.

8.3.8.12 FlashReadOnce command

The FlashReadOnce command returns the contents of the program once field by given index and byte count. The FlashReadOnce command uses 2 parameters: index and byteCount.

Table 8-38. Parameters for FlashReadOnce Command

Byte #	Parameter	Description
0 - 3	index	Index of the program once field (to read from)
4 - 7	byteCount	Number of bytes to read and return to the caller

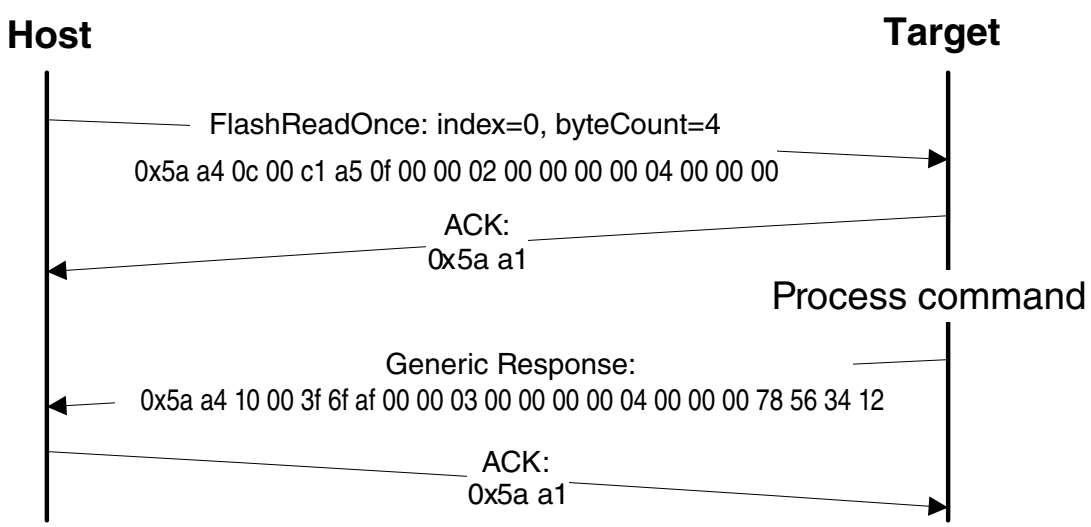


Figure 8-15. Protocol Sequence for FlashReadOnce Command

Table 8-39. FlashReadOnce Command Packet Format (Example)

FlashReadOnce	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4
	length	0x0C 0x00
	crc	0xC1 0xA5
Command packet	commandTag	0x0F – FlashReadOnce
	flags	0x00
	reserved	0x00
	parameterCount	0x02
	index	0x0000_0000
	byteCount	0x0000_0004

Table 8-40. FlashReadOnce Response Format (Example)

FlashReadOnce Response	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4
	length	0x10 0x00
	crc	0x3F 0x6F
Command packet	commandTag	0xAF
	flags	0x00
	reserved	0x00
	parameterCount	0x03
	status	0x0000_0000
	byteCount	0x0000_0004
	data	0x1234_5678

Response: upon successful execution of the command, the target (Kinetis Flashloader) will return a FlashReadOnceResponse packet with a status code set to kStatus_Success, a byte count and corresponding data read from Program Once Field upon successful execution of the command, or will return with a status code set to an appropriate error status code and a byte count set to 0.

8.3.8.13 FlashReadResource command

The FlashReadResource command returns the contents of the IFR field or Flash firmware ID, by given offset, byte count, and option. The FlashReadResource command uses 3 parameters: start address, byteCount, option.

Table 8-41. Parameters for FlashReadResource Command

Byte #	Parameter	Command
0 - 3	start address	Start address of specific non-volatile memory to be read
4 - 7	byteCount	Byte count to be read
8 - 11	option	0: IFR 1: Flash firmware ID

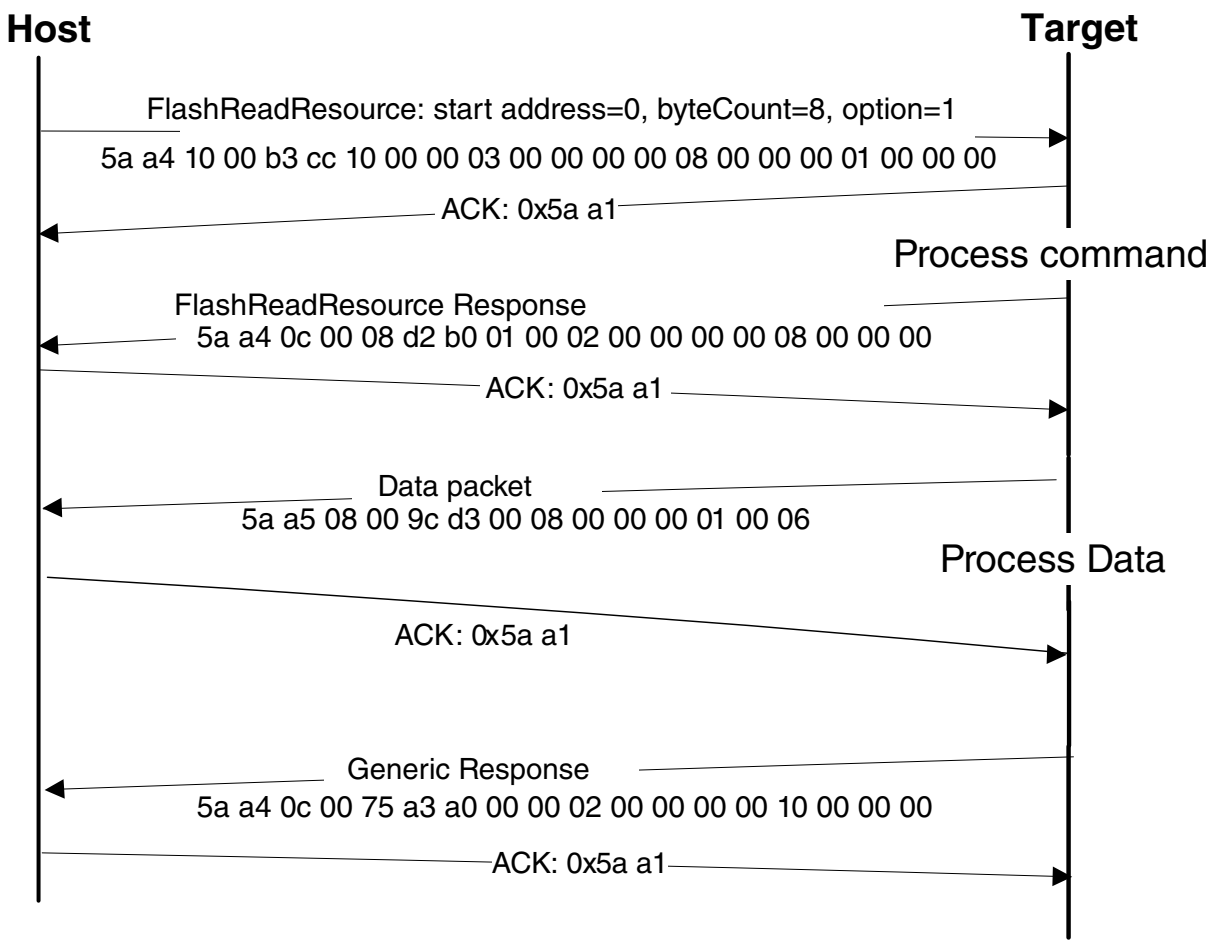


Figure 8-16. Protocol Sequence for FlashReadResource Command

Table 8-42. FlashReadResource Command Packet Format (Example)

FlashReadResource	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4
	length	0x10 0x00
	crc	0xB3 0xCC
Command packet	commandTag	0x10 – FlashReadResource
	flags	0x00

Table continues on the next page...

Table 8-42. FlashReadResource Command Packet Format (Example) (continued)

FlashReadResource	Parameter	Value
	reserved	0x00
	parameterCount	0x03
	startAddress	0x0000_0000
	byteCount	0x0000_0008
	option	0x0000_0001

Table 8-43. FlashReadResource Response Format (Example)

FlashReadResource Response	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4
	length	0x0C 0x00
	crc	0xD2 0xB0
Command packet	commandTag	0xB0
	flags	0x01
	reserved	0x00
	parameterCount	0x02
	status	0x0000_0000
	byteCount	0x0000_0008

Data phase: The FlashReadResource command has a data phase. Because the target (Kinetis Bootloader) works in slave mode, the host must pull data packets until the number of bytes of data *specified in the byteCount parameter of FlashReadResource command* are received by the host.

8.3.8.14 FlashSecurityDisable command

The FlashSecurityDisable command performs the flash security disable operation, by comparing the 8-byte backdoor key (provided in the command) against the backdoor key stored in the flash configuration field (at address 0x400 in the flash).

The backdoor low and high words are the only parameters required for FlashSecurityDisable command.

Table 8-44. Parameters for FlashSecurityDisable Command

Byte #	Command
0 - 3	Backdoor key low word

Table continues on the next page...

Table 8-44. Parameters for FlashSecurityDisable Command (continued)

Byte #	Command
4 - 7	Backdoor key high word

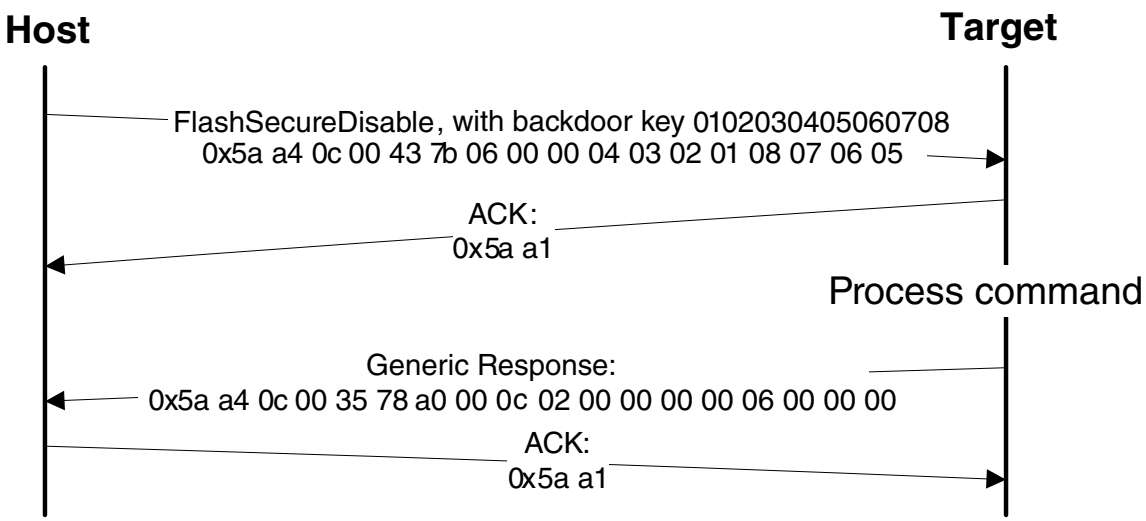


Figure 8-17. Protocol Sequence for FlashSecurityDisable Command

Table 8-45. FlashSecurityDisable Command Packet Format (Example)

FlashSecurityDisable	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4, kFramingPacketType_Command
	length	0x0C 0x00
	crc16	0x43 0x7B
Command packet	commandTag	0x06 - FlashSecurityDisable
	flags	0x00
	reserved	0x00
	parameterCount	0x02
	Backdoorkey_low	0x04 0x03 0x02 0x01
	Backdoorkey_high	0x08 0x07 0x06 0x05

The FlashSecurityDisable command has no data phase.

Response: The target (Kinetis Bootloader) will return a GenericResponse packet with a status code either set to kStatus_Success upon successful execution of the command, or set to an appropriate error status code.

8.3.8.15 FillMemory command

The FillMemory command fills a range of bytes in memory with a data pattern. It follows the same rules as the WriteMemory command. The difference between FillMemory and WriteMemory is that a data pattern is included in FillMemory command parameter, and there is no data phase for the FillMemory command, while WriteMemory does have a data phase.

Table 8-46. Parameters for FillMemory Command

Byte #	Command
0 - 3	Start address of memory to fill
4 - 7	Number of bytes to write with the pattern • The start address should be 32-bit aligned. • The number of bytes must be evenly divisible by 4.
8 - 11	32-bit pattern

- To fill with a byte pattern (8-bit), the byte must be replicated 4 times in the 32-bit pattern.
- To fill with a short pattern (16-bit), the short value must be replicated 2 times in the 32-bit pattern.

For example, to fill a byte value with 0xFE, the word pattern would be 0xFEFEFEFE; to fill a short value 0x5AFE, the word pattern would be 0x5AFE5AFE.

Special care must be taken when writing to flash.

- First, any flash sector written to must have been previously erased with a FlashEraseAll, FlashEraseRegion, or FlashEraseAllUnsecure command.
- Writing to flash requires the start address to be .
- If the VerifyWrites property is set to true, then writes to flash will also perform a flash verify program operation.

When writing to RAM, the start address need not be aligned, and the data will not be padded.

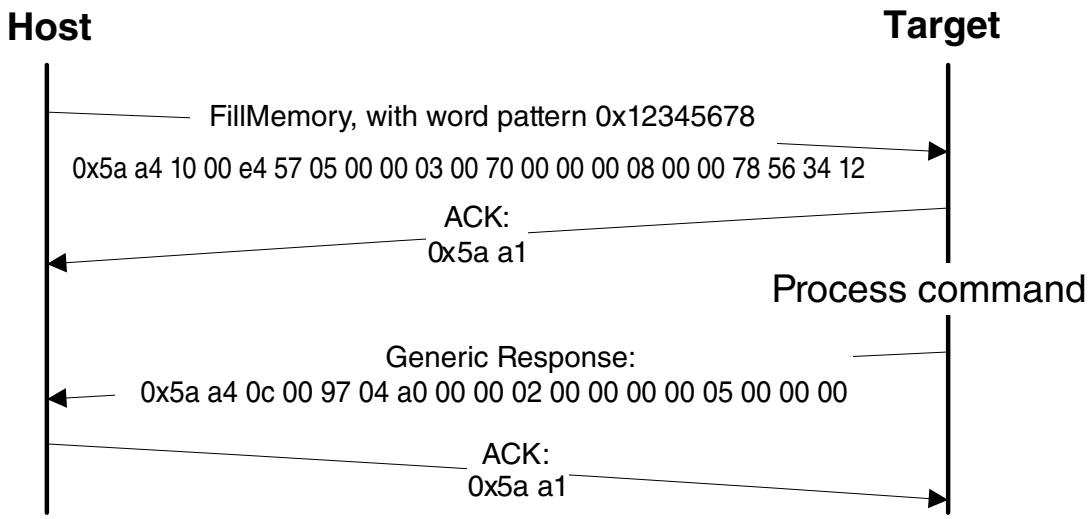


Figure 8-18. Protocol Sequence for FillMemory Command

Table 8-47. FillMemory Command Packet Format (Example)

FillMemory	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4, kFramingPacketType_Command
	length	0x10 0x00
	crc16	0xE4 0x57
Command packet	commandTag	0x05 – FillMemory
	flags	0x00
	Reserved	0x00
	parameterCount	0x03
	startAddress	0x00007000
	byteCount	0x00000800
	patternWord	0x12345678

The FillMemory command has no data phase.

Response: upon successful execution of the command, the target (Kinetis Flashloader) will return a GenericResponse packet with a status code set to kStatus_Success, or to an appropriate error status code.

8.3.8.16 WriteMemory command

The WriteMemory command writes data provided in the data phase to a specified range of bytes in memory (flash or RAM or QuadSPI memory). However, if flash protection is enabled, then writes to protected sectors will fail.

Special care must be taken when writing to flash.

- First, any flash sector written to must have been previously erased with a FlashEraseAll, FlashEraseRegion, or FlashEraseAllUnsecure command.
- Writing to flash requires the start address to be 4-byte aligned ([1:0] = 00).
- The byte count will be rounded up to a multiple of , and the trailing bytes will be filled with the flash erase pattern (0xff).
- If the VerifyWrites property is set to true, then writes to flash will also perform a flash verify program operation.

When writing to RAM, the start address need not be aligned, and the data will not be padded.

The start address and number of bytes are the 2 parameters required for WriteMemory command.

Table 8-48. Parameters for WriteMemory Command

Byte #	Command
0 - 3	Start address
4 - 7	Byte count

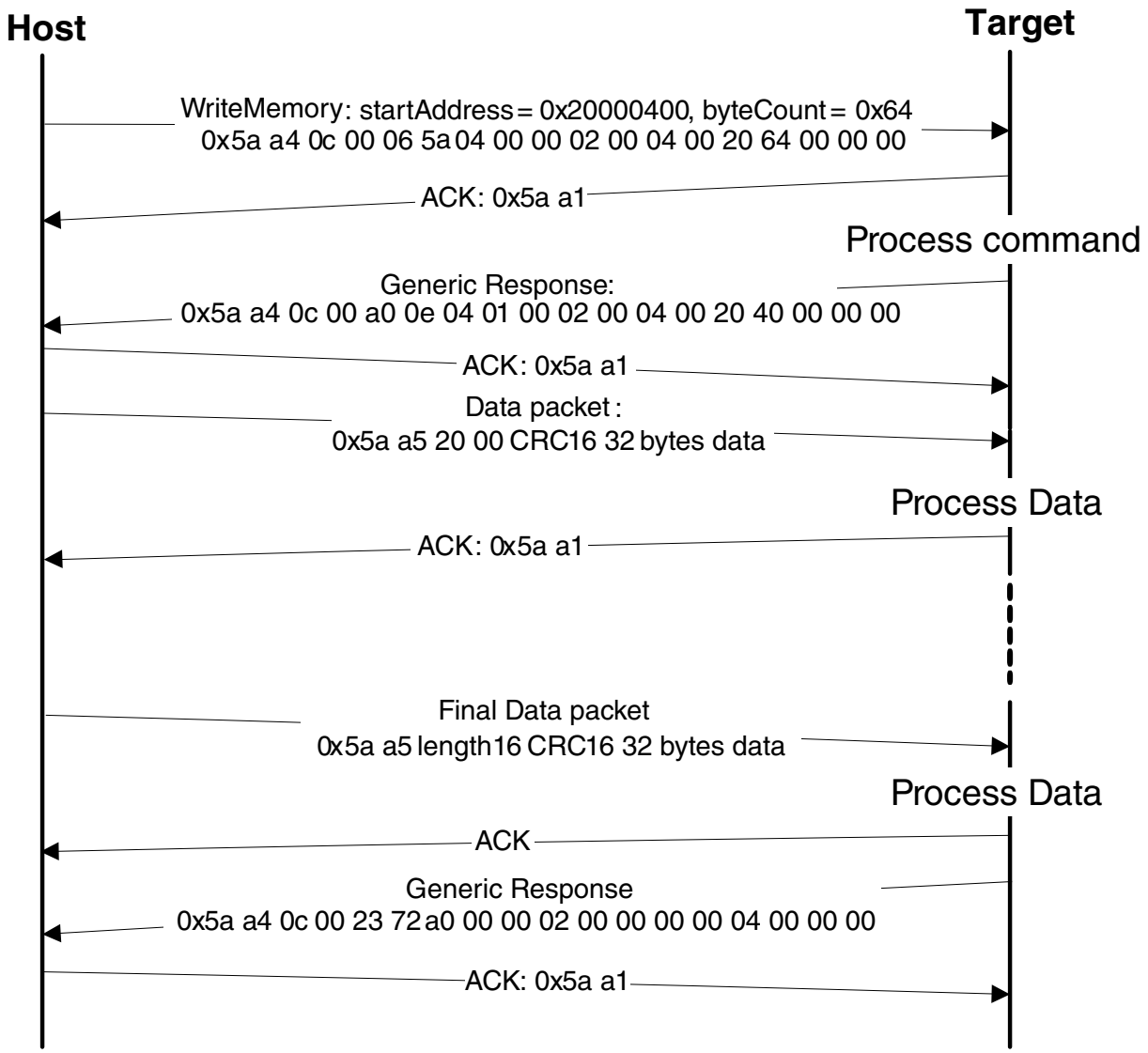


Figure 8-19. Protocol Sequence for WriteMemory Command

Table 8-49. WriteMemory Command Packet Format (Example)

WriteMemory	Parameter	Value
Framing packet	start byte	0x5A
	packetType	0xA4, kFramingPacketType_Command
	length	0x0C 0x00
	crc16	0x06 0x5A
Command packet	commandTag	0x04 - writeMemory
	flags	0x00
	reserved	0x00
	parameterCount	0x02
	startAddress	0x20000400
	byteCount	0x00000064

Data Phase: The WriteMemory command has a data phase; the host will send data packets until the number of bytes of data specified in the byteCount parameter of the WriteMemory command are received by the target.

Response: The target (Kinetis Bootloader) will return a GenericResponse packet with a status code set to kStatus_Success upon successful execution of the command, or to an appropriate error status code.

8.3.8.17 Read memory command

The ReadMemory command returns the contents of memory at the given address, for a specified number of bytes. This command can read any region of memory accessible by the CPU and not protected by security.

The start address and number of bytes are the 2 parameters required for ReadMemory command.

Table 8-50. Parameters for read memory command

Byte	Parameter	Description
0-3	Start address	Start address of memory to read from
4-7	Byte count	Number of bytes to read and return to caller

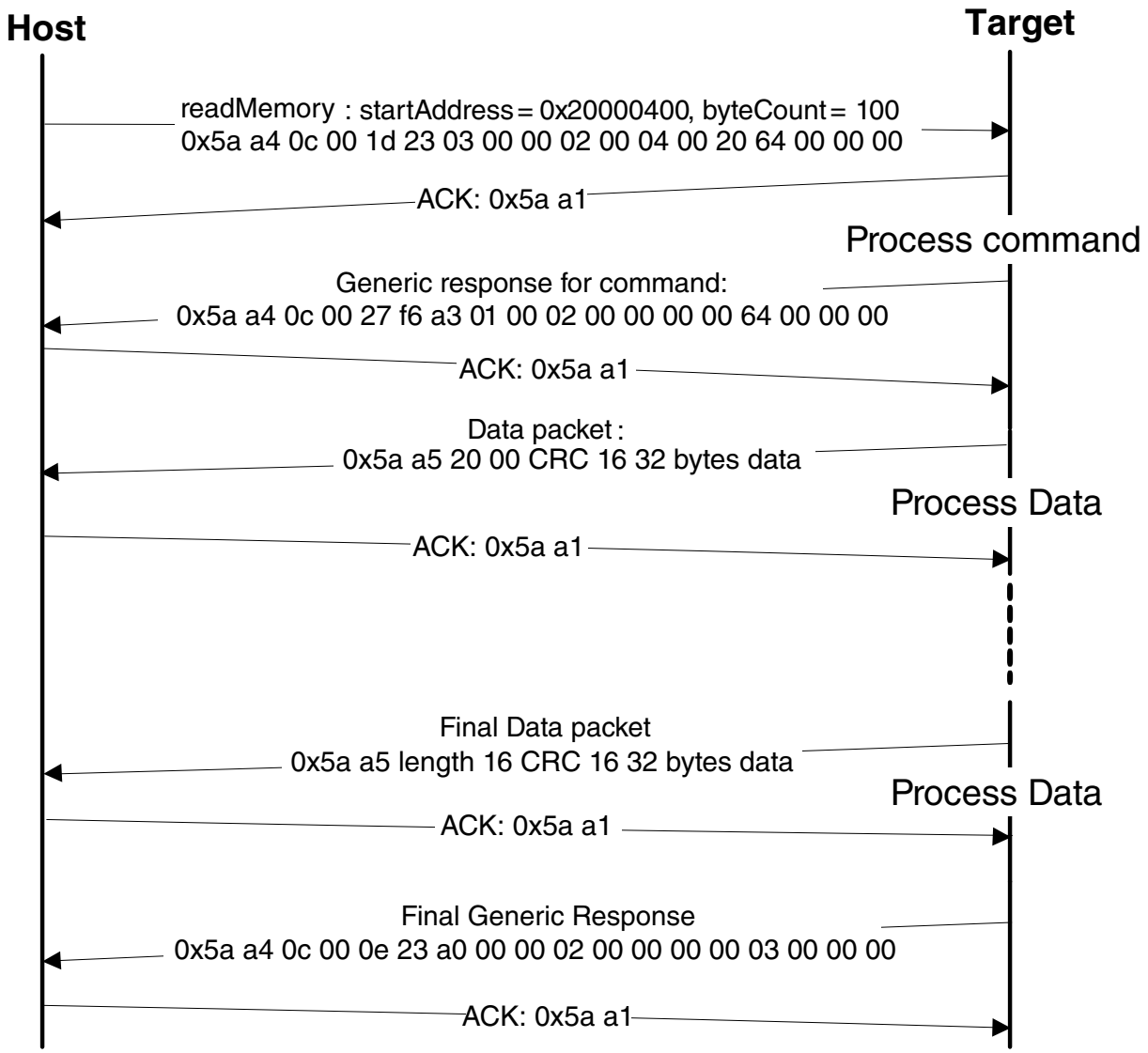


Figure 8-20. Command sequence for read memory

ReadMemory	Parameter	Value
Framing packet	Start byte	0x5A0xA4,
	packetType	kFramingPacketType_Command
	length	0x0C 0x00
	crc16	0x1D 0x23
Command packet	commandTag	0x03 - readMemory
	flags	0x00
	reserved	0x00
	parameterCount	0x02
	startAddress	0x20000400
	byteCount	0x00000064

Data Phase: The ReadMemory command has a data phase. Since the target (Kinetis Bootloader) works in slave mode, the host need pull data packets until the number of bytes of data specified in the byteCount parameter of ReadMemory command are received by host.

Response: The target (Kinetis Bootloader) will return a GenericResponse packet with a status code either set to kStatus_Success upon successful execution of the command, or set to an appropriate error status code.

8.3.9 Bootloader Exit state

The Kinetis Bootloader tries to reconfigure the system back to the reset state in the following situations:

- After completion of an Execute command, but before jumping to the specified entry point.
- After a peripheral detection timeout, but before jumping to the application entry point.

8.4 Peripherals Supported

This section describes the peripherals supported by the Kinetis ROM Bootloader. To use an interface for bootloader communications, the peripheral must be enabled in the BCA, as shown in Table 8-3. If the BCA is invalid (such as all 0xFF bytes), then all peripherals will be enabled by default.

8.4.1 I2C Peripheral

The Kinetis Bootloader in ROM supports loading data into flash via the I2C peripheral, where the I2C peripheral serves as the I2C slave. A 7-bit slave address is used during the transfer.

Customizing an I2C slave address is also supported. This feature is enabled if the Bootloader Configuration Area (BCA) (shown in Table 8-3) is enabled (tag field is filled with ‘kcfg’) and the i2cSlaveAddress field is filled with a value other than 0xFF. 0x10 is used as the default I2C slave address.

The maximum supported I2C baud rate depends on corresponding clock configuration field in the BCA. Typical supported baud rate is 400 kbps with factory settings. Actual supported baud rate may be lower or higher than 400 kbps, depending on the actual value of the clockFlags and the clockDivider fields.

Because the I2C peripheral serves as an I2C slave device, each transfer should be started by the host, and each outgoing packet should be fetched by the host.

- An incoming packet is sent by the host with a selected I2C slave address and the direction bit is set as write.
- An outgoing packet is read by the host with a selected I2C slave address and the direction bit is set as read.
- 0x00 will be sent as the response to host if the target is busy with processing or preparing data.

The following flow charts demonstrate the communication flow of how the host reads ping packet, ACK and response from the target.

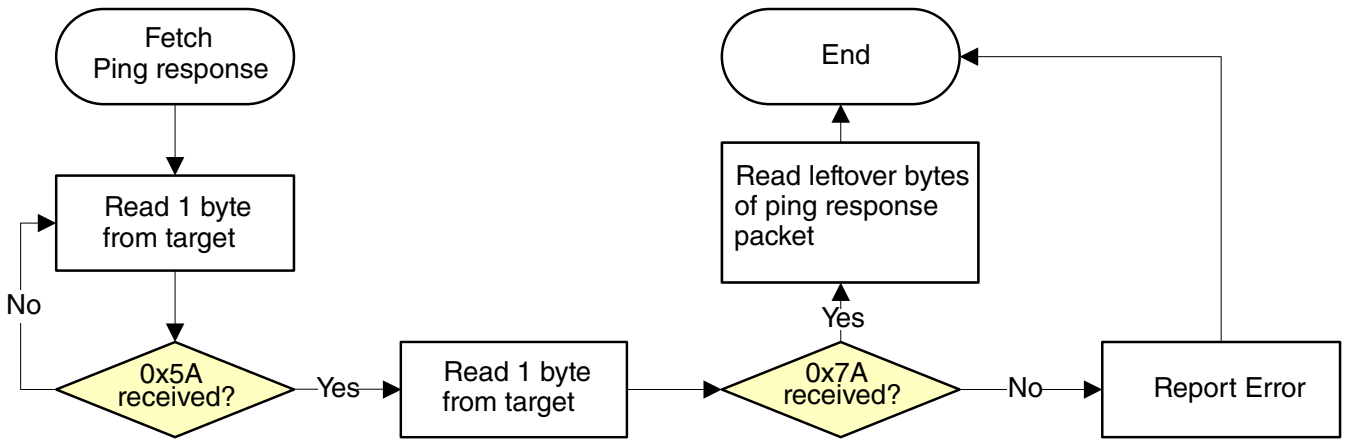


Figure 8-21. Host reads ping response from target via I2C

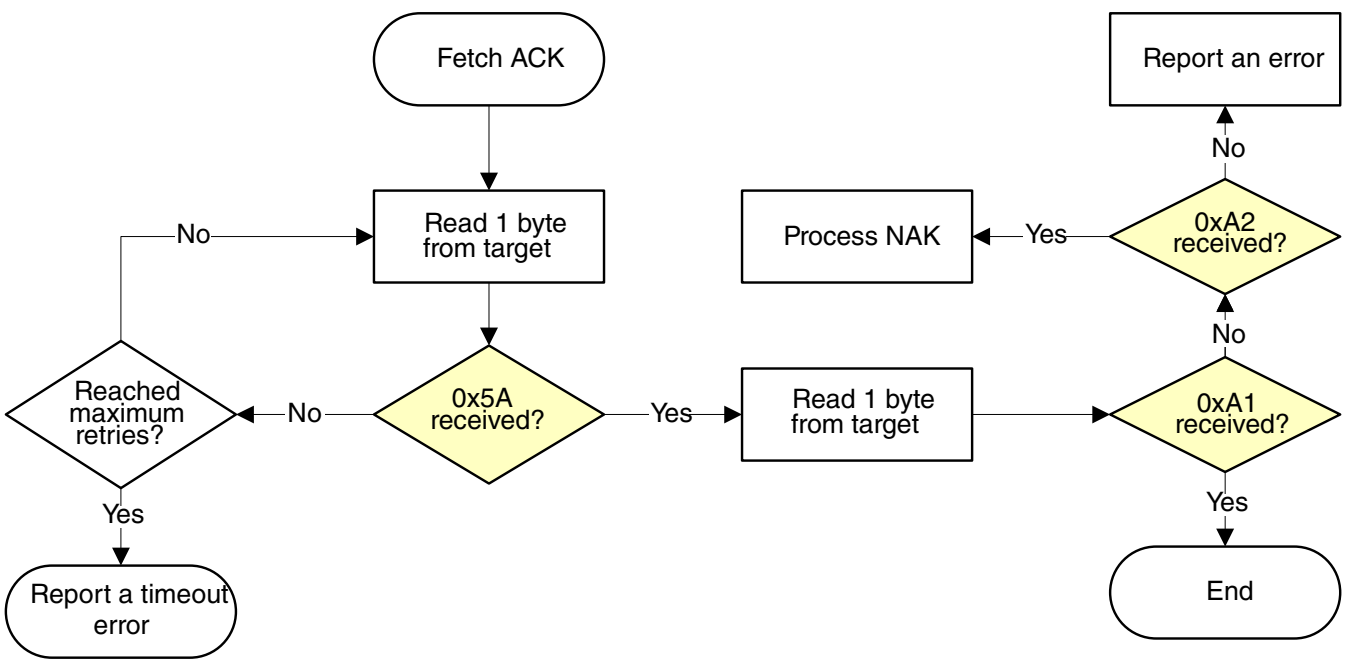


Figure 8-22. Host reads ACK packet from target via I2C

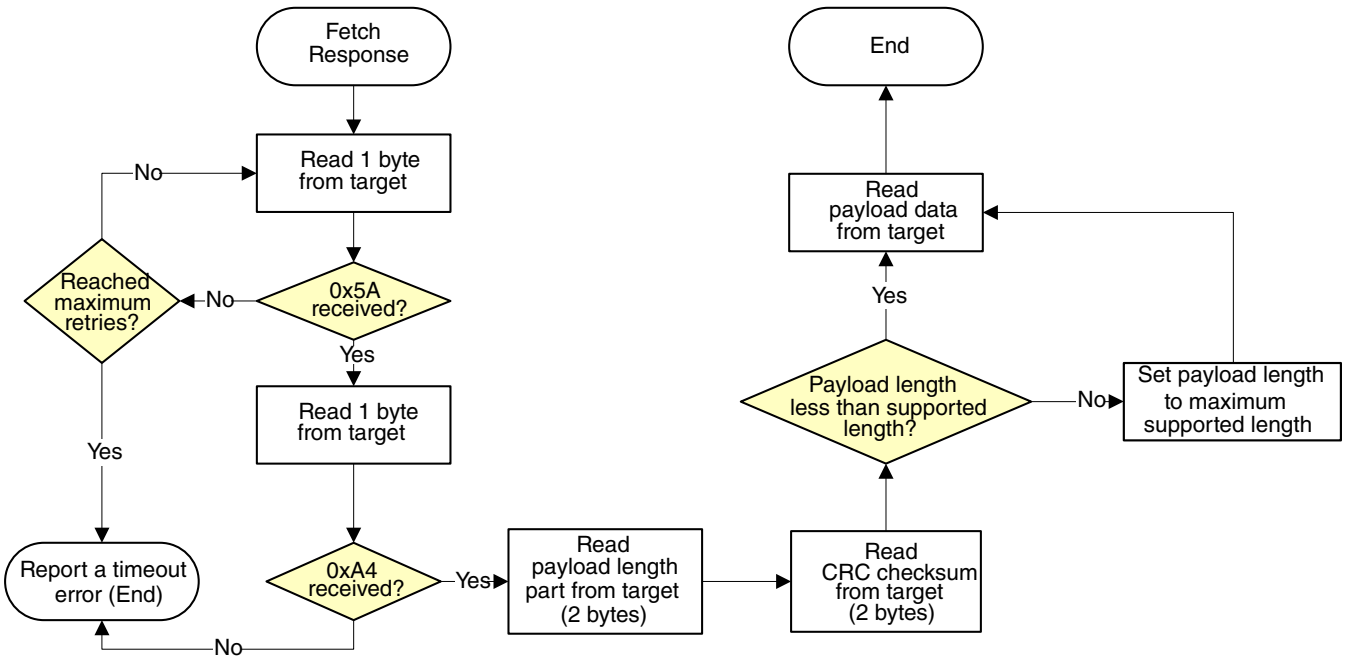


Figure 8-23. Host reads response from target via I2C

8.4.2 SPI Peripheral

The Kinetis Bootloader in K82F ROM supports loading data into flash via the SPI peripheral, where the SPI peripheral serves as a SPI slave.

Maximum supported baud rate of SPI depends on the clock configuration fields in the Bootloader Configuration Area (BCA) shown in Table 8-3. The typical supported baud rate is 400 kbps with the factory settings. The actual baud rate is lower or higher than 400 kbps, depending on the actual value of the clockFlags and clockDivider fields in the BCA.

The SPI peripheral uses the following bus attributes:

- Clock Phase = 1 (Second Edge)
- Clock Polarity = 1 (Active Low)

Because the SPI peripheral in K82F ROM serves as a SPI slave device, each transfer should be started by the host, and each outgoing packet should be fetched by the host.

The transfer on SPI is slightly different from I2C:

- Host will receive 1 byte after it sends out any byte.
- Received bytes should be ignored when host is sending out bytes to target
- Host starts reading bytes by sending 0x00s to target
- The byte 0x00 will be sent as response to host if target is under the following conditions:

- Processing incoming packet
- Preparing outgoing data
- Received invalid data

The SPI bus configuration is:

- Phase = 1; data is sampled on rising edges
- Polarity = 1; idle is high
- MSB is transmitted first

For any transfer where the target does not have actual data to send, the target (slave) is responsible for ensuring that 0x00 bytes will be returned to the host (master). The host uses framing packets to identify real data and not "dummy" 0x00 bytes (which do not have framing packets).

The following flowcharts demonstrate how the host reads a ping response, an ACK and a command response from target via SPI.

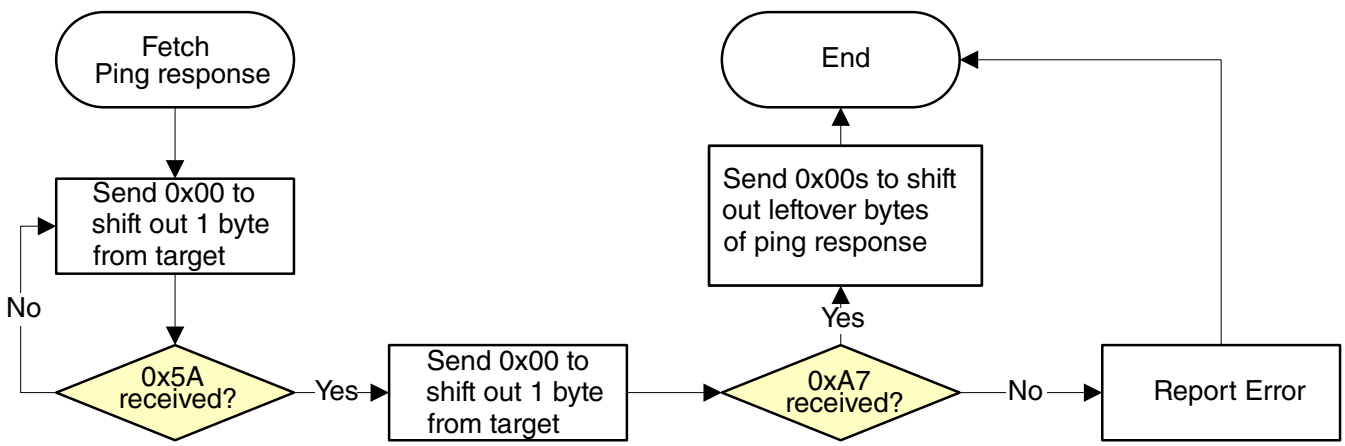


Figure 8-24. Host reads ping packet from target via SPI

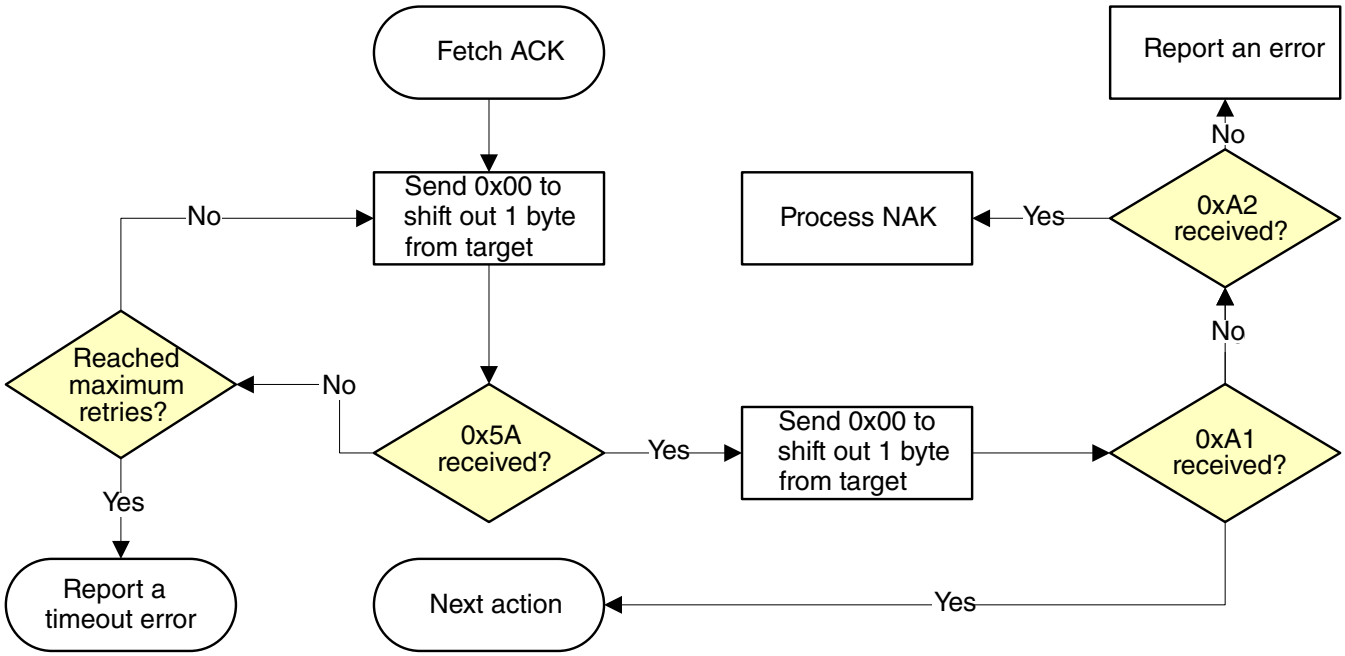


Figure 8-25. Host reads ACK from target via SPI

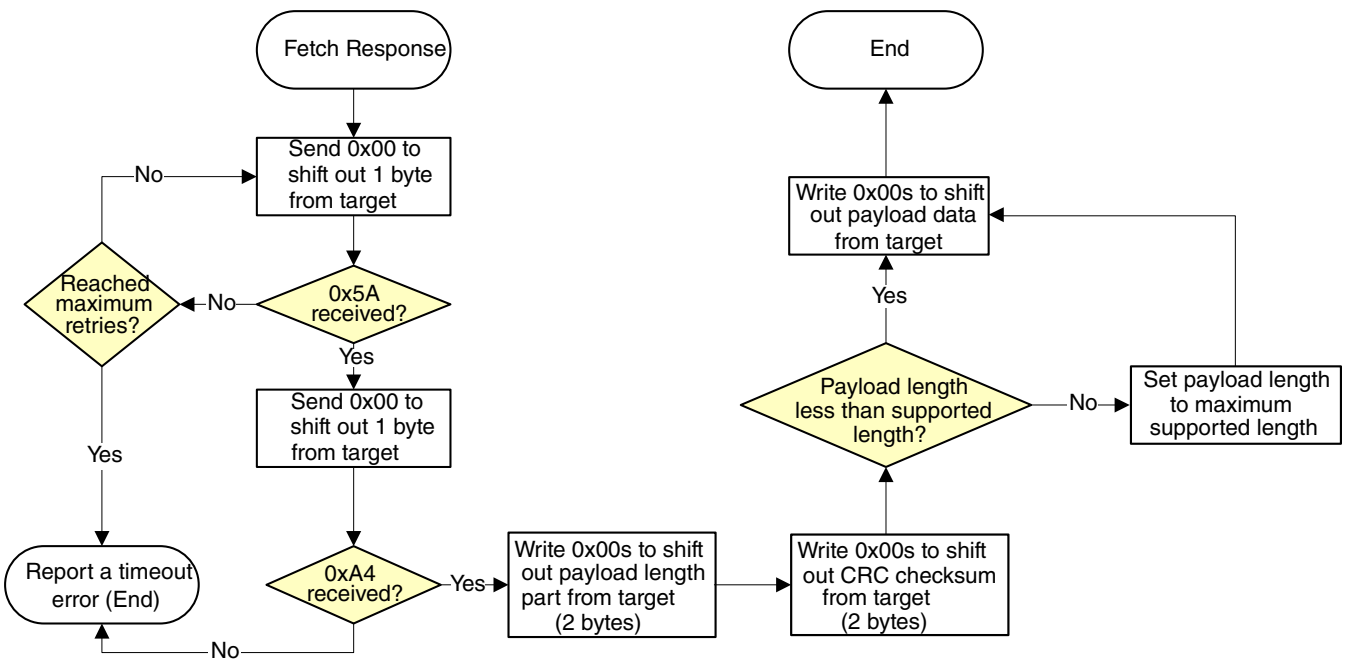


Figure 8-26. Host reads response from target via SPI

8.4.3 QuadSPI Peripheral

The Kinetis Bootloader supports read, write, and erase external SPI flash devices (QuadSPI memory) via the QuadSPI module. It supports booting directly to external SPI flash and XIP in QuadSPI memory. Before accessing external SPI flash devices, the QuadSPI module must be configured properly, using the QSPI configuration block.

8.4.3.1 QSPI configuration block

The QSPI config block (QCB) provides many configuration parameters, which are intended to support many types of serial flash. All fields in the QSPI config block must be configured according to the specific flash device provided by your specific vendor, and all of them are related to the configuration for registers in the QuadSPI module. Also see the QuadSPI chapter.

NOTE

To correctly configure the QuadSPI, **all *unused* QuadSPI configuration fields should be set to 0**.

Table 8-51. Configuration fields in QSPI config block

Offset	Size (bytes)	Configuration Field	Description
0x00 – 0x03	4	tag	A magic number to verify whether the QSPI config block (QCB) is valid. Must be set to ‘kqcf’ [31:24] - ‘f’ (0x66) [23:16] - ‘c’ (0x63) [15: 8] - ‘q’(0x71) [7: 0] - ‘k’(0x6B)
0x04 – 0x07	4	version	Version number of the QSPI config block [31:24] - name: must be 'Q' (0x51) [23:16] - major: must be 1 [15: 8] - minor: must be 0 [7: 0] - bugfix: must be 0
0x08 – 0x0b	4	lengthInBytes	Size of QSPI config block, in bytes Must be 512
0x0c – 0x0f	4	dqs_loopback	Enable DQS loopback support 0 DQS loopback is disabled 1 DQS loopback is enabled, the DQS loopback mode is determined by subsequent ‘***dqs_loopback_internal***’ field
0x10 – 0x1b	12	-	Reserved

Table continues on the next page...

Table 8-51. Configuration fields in QSPI config block (continued)

Offset	Size (bytes)	Configuration Field	Description
0x1c – 0x1f	4	device_mode_config_en	Configure work mode Enable for external SPI flash devices 0 Disabled - ROM will not configure work mode of external flash devices. 1 Enabled - ROM will configure work mode of external flash devices, based on “device_cmd” and the LUT entry indicated by” write_cmd_ipcr”.
0x20 – 0x23	4	device_cmd	Command to configure the work mode of external flash devices. Effective only if “device_mode_config_en” is set to 1. It also depends on your specific external SPI flash device.
0x24 – 0x27	4	write_cmd_ipcr	IPCR pointed to LUT index for quad mode enablement Value = index << 24
0x28 – 0x2b	4	word_addressable	Word Addressable 0 Byte-addressable serial flash mode 1 Word-addressable serial flash mode
0x2c – 0x2f	4	cs_hold_time	Serial flash CS hold time, in number of flash clock cycles
0x30 – 0x33	4	cs_setup_time	Serial flash CS setup time, in number of flash clock cycles
0x34 – 0x37	4	sflash_A1_size	Size of external flash connected to ports of QSPI0A and QSPI0A_CS0, in bytes
0x38 – 0x3b	4	sflash_A2_size	Size of external flash connected to ports of QSPI0A and quadSPI0A_CS1, in bytes sflash_A2_size field must be set to 0 if the serial flash device is not present.
0x3c – 0x3f	4	sflash_B1_size	Size of external flash connected to ports of QSPI0B and quadSPI0B_CS0, in bytes sflash_B1_size field must be set to 0 if the serial flash device is not present.
0x40 – 0x43	4	sflash_B2_size	Size of external flash connected to ports of QSPI0B and quadSPI0B_CS1, in bytes sflash_B2_size field must be set to 0 if the serial flash device is not present.
0x44 – 0x47	4	sclk_freq	Frequency of QuadSPI serial clock 1 0 Low frequency (24 MHz) 1 Mid frequency (48 MHz) 2 High frequency (96 MHz)
0x48 – 0x4b	4	busy_bit_offset	Busy bit offset in status register of Serial flash [31:16] : 0 - Busy flag in status register is 1 when flash devices are busy.

Table continues on the next page...

Table 8-51. Configuration fields in QSPI config block (continued)

Offset	Size (bytes)	Configuration Field	Description
			1 - Busy flag in status register is 0 when flash devices are busy. [15:0]: The offset of busy flag in status register; valid range is 0 - 31.
0x4c – 0x4f	4	sflash_type	Type of serial flash 0 Single mode 1 Dual mode 2 Quad mode 3 Octal mode
0x50 – 0x53	4	sflash_port	Port enablement for QuadSPI module 0 Only pins for QSPI0A are enabled 1 Pins for both QSPI0A and QSPI0B are enabled
0x54 – 0x57	4	ddr_mode_enable	Enable DDR mode 0 DDR mode is disabled 1 DDR mode is enabled
0x58 – 0x5b	4	dqs_enable	Enable DQS 0 DQS is disabled 1 DQS is enabled
0x5c – 0x5f	4	parallel_mode_enable	Enable Parallel Mode 0 Parallel mode is disabled 1 Parallel mode is enabled[1]
0x60 – 0x63	4	portA_cs1	Enable QuadSPI0A_CS1 0 QuadSPI0A_CS1 is disabled 1 QuadSPI0A_CS1 is enabled portA_cs1 field must be set to 1 if sflash_A2_size is not equal to 0.
0x64 – 0x67	4	portB_cs1	Enable QuadSPI0B_CS1 0 QuadSPI0B_CS1 is disabled 1 QuadSPI0B_CS1 is enabled portB_cs1 field must be set to 1 if sflash_B2_size is not equal to 0.
0x68 – 0x6b	4	fsphs	Full Speed Phase selection for SDR instructions 0 Select sampling at non-inverted clock 1 Select sampling at inverted clock
0x6c – 0x6f	4	fsdly	Full Speed Delay selection for SDR instructions 0 One clock cycle delay 1 Two clock cycles delay.
0x70 – 0x73	4	ddrsmp	DDR sampling point

Table continues on the next page...

Table 8-51. Configuration fields in QSPI config block (continued)

Offset	Size (bytes)	Configuration Field	Description
			Valid range: 0 - 7
0x74 – 0x173	4	look_up_table	Look-up-table for sequences of instructions
0x174 – 0x177	4	column_address_space	Column Address Space Defines the width of the column address
0x178 – 0x17b	4	config_cmd_en	Enable additional configuration command 0 Additional configuration command is not needed 1 Additional configuration command is needed
0x17c – 0x18b	16	config_cmds	IPCR arrays for each connected SPI flash All fields must be set to 0 if config_cmd_en is not asserted.
0x18c - 0x19b	16	config_cmds_args	Command arrays needed to be transferred to external spi flash All fields must be set to 0 if config_cmd_en is not asserted.
0x19c – 0x19f	4	differential_clock_pin_enable	Enable differential flash clock pin 0 Differential flash clock pin is disabled 1 Differential flash clock pin is enabled
0x1a0 – 0x1a3	4	flash_CK2_clock_pin_enable	Enable Flash CK2 Clock pin 0 Flash CK2 Clock pin is disabled 1 Flash CK2 Clock pin is enabled
0x1a4 – 0x1a7	4	dqs_inverse_sel	Select clock source for internal DQS generation 0 Use 1x internal reference clock for DQS generation 1 Use inverse 1x internal reference clock for DQS generation
0x1a8 – 0x1ab	4	dqs_latency_enable	DQS Latency Enable 0 DQS latency disabled 1 DQS feature with latency included enabled
0x1ac – 0x1af	4	dqs_loopback_internal	DQS loopback from internal DQS signal or DQS Pad 0 DQS loopback is sent to DQS pad first and then looped back to QuadSPI 1 DQS loopback from internal DQS signal directly
0x1b0 – 0x1b3	4	dqs_phase_sel	Select Phase Shift for internal DQS generation 0 No Phase shift 1 Select 45° phase shift 2 Select 90° phase shift 3 Select 135° phase shift
0x1b4 – 0x1b7	4	dqs_fa_delay_chain_sel	Delay chain tap number selection for QuadSPI0A DQS Valid range: 0 - 63

Table continues on the next page...

Table 8-51. Configuration fields in QSPI config block (continued)

Offset	Size (bytes)	Configuration Field	Description
0x1b8 – 0x1bb	4	dqs_fb_delay_chain_sel	Delay chain tap number selection for QuadSPI0B DQS Valid range: 0 - 63
0x1bc – 0x1c3	8	-	Reserved
0x1c4 – 0x1c7	4	page_size	Page size of external SPI flash.[1] Page size of all SPI flash devices must be the same
0x1c8 – 0x1cb	4	sector_size	Sector size of external SPI flash.[1] Sector size of all SPI flash devices must be the same.
0x1cc - 0x1cf	4	timeout_milliseconds	Timeout in terms of milliseconds. 0 Timeout check is disabled. **NOTE:** If the time that the external SPI device is busy is more than this timeout value, then the QuadSPI driver returns a timeout.
0x1d0 – 0x1d3	4	ips_cmd_second_divider	Second divider for IPs command based on QSPI_MCR[SCLKCFG]; the maximum value of QSPI_MCR[SCLKCFG] depends on the specific device.
0x1d4 – 0x1d7	4	need_multi_phase	0 Only 1 phase is necessary to access external flash devices 1 Multiple phases are necessary to erase/program external flash devices
0x1d8 – 0x1db	4	is_spansion_hyperflash	0 External flash devices is not in the Spansion Hyperflash family 1 External flash devices is in the Spansion Hyperflash family
0x1dc – 0x1df	4	pre_read_status_cmd_address_offset[2]	Additional address for the PreReadStatus command. Set this field to 0xFFFF FFFF if it is not required.
0x1e0 – 0x1e3	4	pre_unlock_cmd_address_offset[2]	Additional address for PreWriteEnable command. Set this field to 0xFFFF FFFF if it is not required.
0x1e4 – 0x1e7	4	unlock_cmd_address_offset[2]	Additional address for WriteEnable command. Set this field to 0xFFFF FFFF if it is not required.
0x1e8 – 0x1eb	4	pre_program_cmd_address_offset[2]	Additional address for PrePageProgram command. Set this field to 0xFFFF FFFF if it is not required.
0x1ec – 0x1ef	4	pre_erase_cmd_address_offset[2]	Additional address for PreErase command. Set this field to 0xFFFF FFFF if it is not required.
0x1f0 – 0x1f3	4	erase_all_cmd_address_offset[2]	Additional address for EraseAll command. Set this field to 0xFFFF FFFF if it is not required.
0x1f4 – 0x1ff	12	-	Reserved

1. If parallel mode is enabled, then page size and sector size must be twice the actual size.
2. These fields are effective only if “need_multi_phase” field is set to 1.

8.4.3.2 Look-up-table

The look-up table (LUT) is a part of the QCB, and contains sequences for instructions, such as read and write instructions. The Kinetis Bootloader defines LUT entries to support erase, program and read operations.

NOTE

The sequence in each LUT entry is target-specific. See the datasheet or reference manual of the corresponding serial flash device.

Table 8-52. Look-up table entries for bootloader

Index	Field	Description
0	Read	Sequence for read instructions
1	WriteEnable	Sequence for WriteEnable instructions
2	EraseAll	Sequence for EraseAll instructions
3	ReadStatus	Sequence for ReadStatus instructions
4	PageProgram	Sequence for Page Program instructions
6	PreErase[1]	Sequence for Pre-Erase instructions
7	SectorErase	Sequence for Sector Erase
8	Dummy	Sequence for dummy operation if needed. For example, if continuous read is configured in index 0, then the dummy LUT should be configured to force the external SPI flash to exit continuous read mode. If a dummy operation is not required, then this LUT entry must be set to 0.
9	PreWriteEnable[1]	Sequence for Pre-WriteEnable instructions
10	PrePageProgram[1]	Sequence for Pre-PageProgram instructions
11	PreReadStatus[1]	Sequence for Pre-ReadStatus instructions

1. If these LUT entries are are not required, then they are allowed to be used for other purposes.

8.4.3.3 Configure QuadSPI module

The Kinetis Bootloader is able to access external SPI devices via the QuadSPI module, but only after the QuadSPI module is configured. There are 2 ways to configure the QuadSPI module:

- Configure QuadSPI module at runtime
- Configure QuadSPI module at start-up

Table 8-53. Configuring the QuadSPI module

Configure QuadSPI at	Procedure	Clock updates during QuadSPI module configuration
runtime	1. Use a WriteMemory command to program the QCB to either a region of RAM or internal flash. 2. Use the ConfigQuadSPI command to configure the QuadSPI module with the QCB that was programmed before. 3. After the above operations, the QuadSPI module has been set to an expected mode specified by the QCB, so the Kinetis bootloader is now able to access all connected SPI flash devices.	**If QuadSPI module is configured at runtime:** The System Core clock will not be updated if the QuadSPI module is configured at runtime; only QUADSPI_MCR [SCLKCFG] is updated according to sclk_freq field within the QCB. In this case, the clock source for QuadSPI module is MCGFLL , (QUADSPI0_SOCCR [QSPISRC] equals 4).
start-up	The steps of configuring QuadSPI at startup is based on the runtime procedure, if the QCB is not present at address 0 of the 1st external SPI flash device. 1. Configure the QuadSPI module at runtime (procedure above). 2. Erase the 1st sector of the 1st connected external SPI flash device using the FlashEraseRegion command. 3. Program the QCB to address 0 of the 1st connected external SPI flash device using the WriteMemory command. **NOTE:** For some types of SPI flash devices (like Spansion Hyperflash) which do not support basic reads (0x03) with 24-bit addresses, an alternative is available: for this step, program the QCB to internal flash, set the “qspiConfigBlockPointer” in the BCA to the start address of QCB, and program the BCA to 0x3c0. 4. Update BOOTSRC_SEL field (bits [7:6]) in FOPTregister at the address 0x40D to “0b’10”, which means "boot from ROM with QuadSPI configured". 5. Reset the target. 6. After start-up, ROM code reads the QCB from address 0 of the external SPI flash and then configures the QuadSPI according to the QCB. 7. Now, the Kinetis Bootloader is able to access all connected SPI flash devices. The QuadSPI module will be configured automatically out of reset, if the QCB is already present and the BOOTSRC_SEL field (bits [7:6]) in FOPTregister at the address 0x40D equals to “0’b10”.	**If QuadSPI module is configured at start-up:** The System Core clock will be updated to 96 MHz, if the QuadSPI module is configured at start-up. In this case, the clock source of the QuadSPI module switches to MCGFLL. The corresponding registers are updated with the values listed in the table *Register value updates when the QuadSPI module is configured at start-up*.

NOTE

The user application boot from QuadSPI in XIP mode should not change the QuadSPI source clock from what ROM has configured (as shown in the previous table); otherwise a hard fault may occur. However, the QuadSPI source clocks (listed in

the next table) can be changed successfully, if the application avoids shutting down the QSPI clock during clock switching; for example, if the clock switch related codes are relocated in either internal flash or SRAM.

Table 8-54. Register value updates when the QuadSPI module is configured at start-up

Register	Field	Value	Description
MCG_C7	OSCSEL	2	IRC48M is chosen as external reference clock
MCG_C2	RANGE	2	
MCG_C1	FRDIV	6	Combined with MCG_C2[RANGE] to divide IRC48M with 1280
MCG_C4	DMX32	0	
MCG_C4	DRST_DRS	3	Combined with MCG_C4[DMX32] to multiply divided clock with 2560, then MCGOUT clock is equal to 96 MHz.
MCG_C6	PLLS	0	Disable PLL
MCG_C1	IREFS	0	Switch to external reference clock
SIM_CLKDIV1	OUTDIV1	0	
SIM_CLKDIV1	OUTDIV2	1	
SIM_CLKDIV1	OUTDIV3	1	
SIM_CLKDIV1	OUTDIV4	3	
QUADSPII0_SOCCR	QSPISRC	1	MCGFLL clock is selected as the clock source for QuadSPI module

8.4.3.4 Access external SPI flash devices using QuadSPI module

The Kinetis Bootloader supports access to external SPI flash devices using the following commands:

- **Flash-erase-all:** This command can erase all SPI flash devices defined in the QCB. For example, if “flash-erase-all 1”, the 1 represents the source of the erasure command is QuadSPI memory.
- **Flash-erase-region:** This command can erase a specified range of flash within connected SPI flash devices. For example “flash-erase-region 0x68000000 0x10000”.
- **Write-memory:** The Kinetis Bootloader calls the Write-memory command to program specified data to a given region of connected SPI flash devices. For example, “write-memory 0x68001000 led_demo.bin”.
- **Read-memory:** The Kinetis Bootloader calls the Read-memory command to read data from a given region of connected SPI flash devices. For example, “read-memory 0x68000000 1024 temp.bin”.

These commands return error codes.

Table 8-55. Status Error Codes for accessing QuadSPI memory

Error Code	Value	Description
kStatus_Success	0	Operation succeeded without error
kStatus_QspiFlashSizeError	400	Size of external SPI flash is invalid
kStatus_QspiFlashAlignmentError	401	Start Address for program is not page-aligned
kStatus_QspiFlashAddressError	402	The address is invalid
kStatus_QspiFlashCommandFailure	403	The operation failed
kStatus_QspiNotConfigured	405	QSPI module is not successfully configured
kStatus_QspiCommandNotSupported	406	The command is not supported under certain modes
kStatus_QspiCommandTimeout	407	The time that the external SPI device is busy more than the timeout value (timeout_milliseconds).
kStatus_QspiWriteFailure	408	QSPI module cannot perform a program command at the current clock frequency

8.4.3.5 Boot directly from QuadSPI

The Kinetis Bootloader supports booting directly from QuadSPI. To boot directly from QuadSPI, the following conditions must be met:

- The bootFlags field in BCA is set to 0xFE, which means "boot directly from QuadSPI".
- The BOOTSRC_SEL field (bits [7:6]) in the FOPT register at address 0x40D is set to “0’b10”, which means "boot from ROM with QuadSPI configured".
- User application is valid.
- QuadSPI configuration block (QCB) is valid
- CRC check passed if the CRC check feature is enabled.

8.4.4 LPUART Peripheral

The Kinetis Bootloader integrates an autobaud detection algorithm for the LPUART peripheral, thereby providing flexible baud rate choices.

Autobaud feature: If LPUART*n* is used to connect to the bootloader, then the LPUART*n*_RX pin must be kept high and not left floating during the detection phase in order to comply with the autobaud detection algorithm. After the bootloader detects the ping packet (0x5A 0xA6) on LPUART*n*_RX, the bootloader firmware executes the autobaud sequence. If the baudrate is successfully detected, then the bootloader will send a ping packet response [(0x5A 0xA7), protocol version (4 bytes), protocol version options (2 bytes) and crc16 (2 bytes)] at the detected baudrate. The Kinetis Bootloader then enters a loop, waiting for bootloader commands via the LPUART peripheral.

NOTE

The data bytes of the ping packet must be sent continuously (with no more than 80 ms between bytes) in a fixed LPUART transmission mode (8-bit data, no parity bit and 1 stop bit). If the bytes of the ping packet are sent one-by-one with more than 80 ms delay between them, then the autobaud detection algorithm may calculate an incorrect baud rate. In this case, the autobaud detection state machine should be reset.

Supported baud rates: The baud rate is closely related to the MCU core and system clock frequencies. Typical baud rates supported are 9600, 19200, 38400, 57600, and 115200. Of course, to influence the performance of autobaud detection, the clock configuration in BCA can be changed.

Packet transfer: After autobaud detection succeeds, bootloader communications can take place over the LPUART peripheral. The following flow charts show:

- How the host detects an ACK from the target
- How the host detects a ping response from the target
- How the host detects a command response from the target

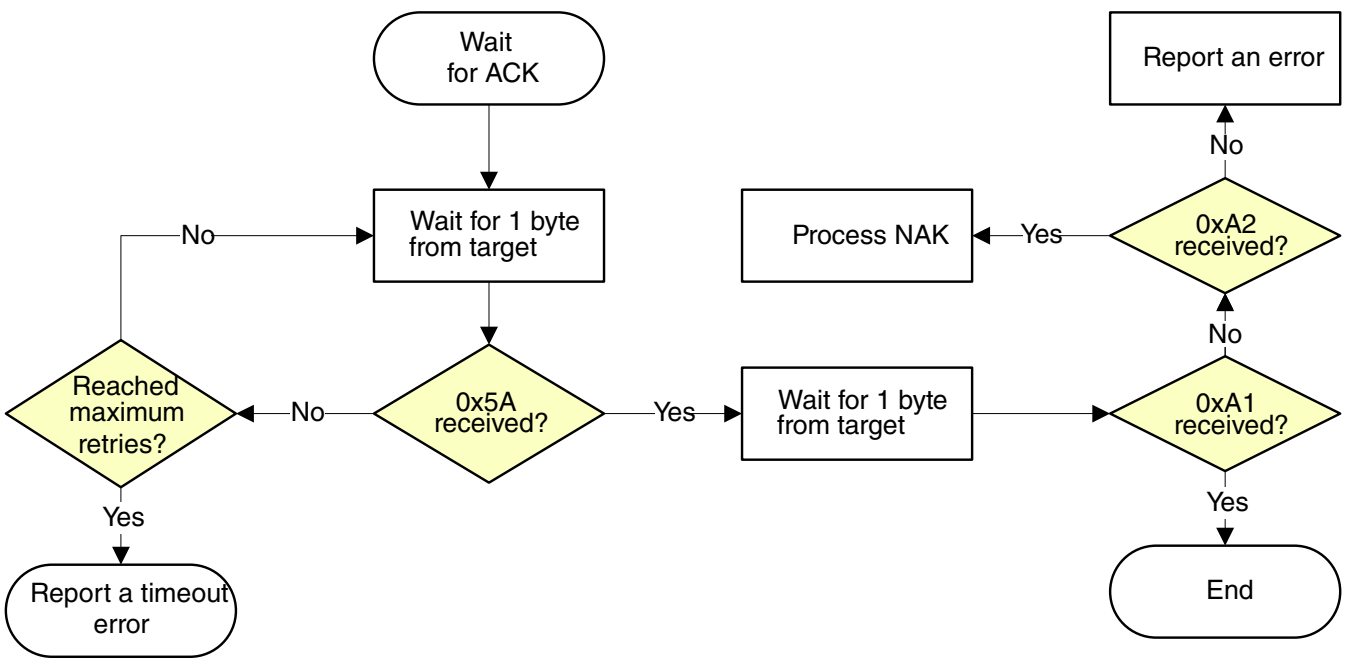


Figure 8-27. Host reads an ACK from target via LPUART

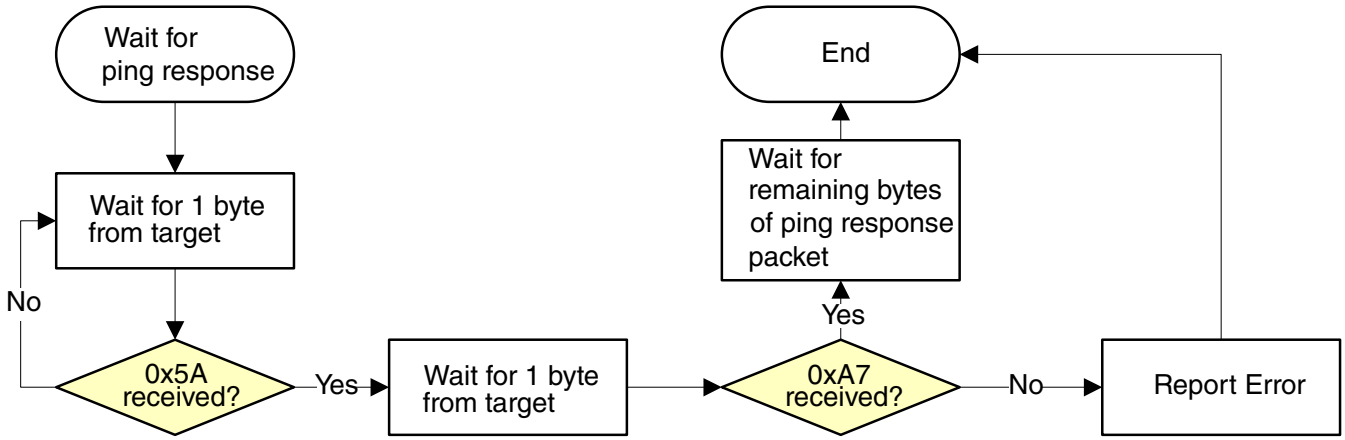


Figure 8-28. Host reads a ping response from target via LPUART

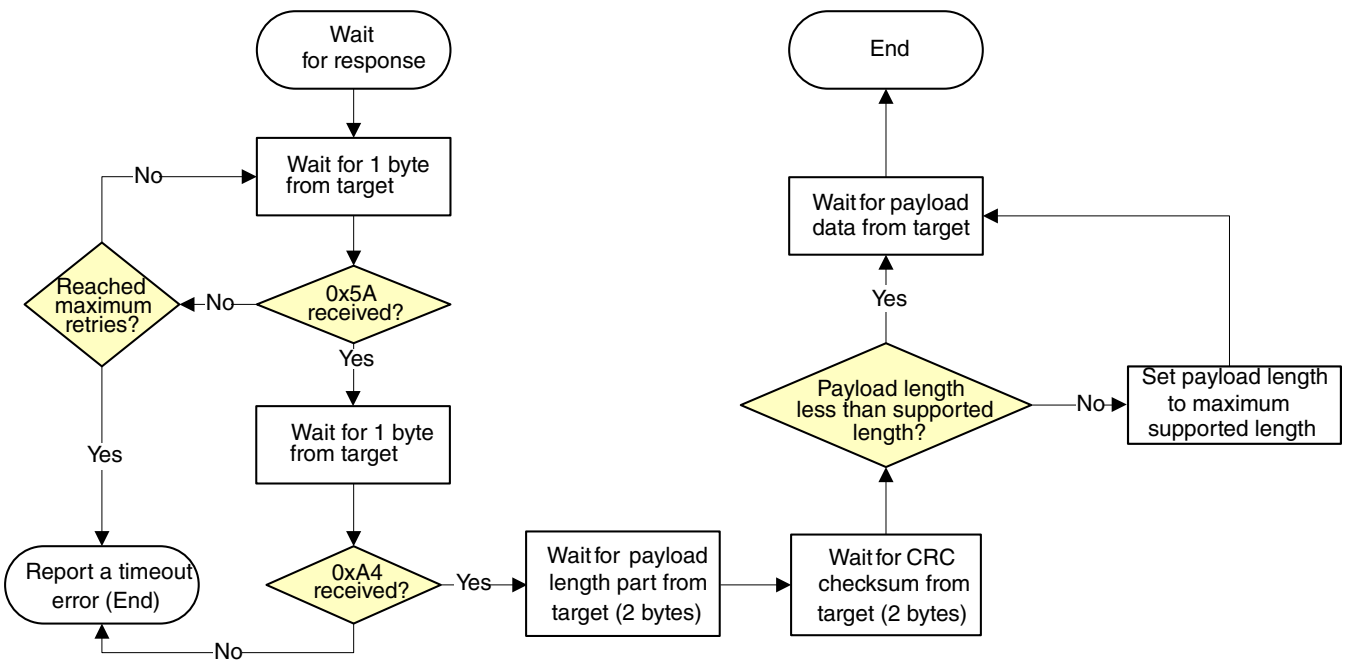


Figure 8-29. Host reads a command response from target via LPUART

8.4.5 USB peripheral

The Kinetis Bootloader in the ROM supports loading data into flash via the USB peripheral. The target is implemented as a USB HID class.

USB HID does not use framing packets; instead the packetization inherent in the USB protocol itself is used. The ability for the device to NAK Out transfers (until they can be received) provides the required flow control; the built-in CRC of each USB packet provides the required error detection.

8.4.5.1 Clock configuration

The K82F ROM supports the crystal-less USB feature. If the USB peripheral is enabled, then the ROM enables the 48-MHz IRC. The ROM also enables the USB clock recovery feature (by setting USB_CLK_RECOVER_CTRL[CLOCK_RECOVER_EN] to 1 and USB_CLK_RECOVER_IRC_EN[IRC_EN] to 1).

8.4.5.2 Device descriptor

The Kinetis ROM configures the default USB VID/PID/Strings as below:

Default VID/PID:

- VID = 0x15A2
- PID = 0x0073

Default Strings:

- Manufacturer [1] = "Freescale Semiconductor Inc."
- Product [2] = "Kinetis Bootloader"

You can customize the USB VID/PID/Strings with the Bootloader Configuration Area (BCA) of the flash. See Table 8-3. For example, the USB VID and PID can be customized by writing the new VID to the usbVid(BCA + 0x14) field and the new PID to the usbPid(BCA + 0x16) field of the BCA in flash. To change the USB strings, you need to prepare a structure (like the one shown below) in the flash, and then write the address of the g_languages structure to the usbStringsPointer(BCA + 0x18) field of the BCA.

```
g_languages = { USB_STR_0,
sizeof(USB_STR_0),
(uint_16)0x0409,
(const uint_8 **)g_string_descriptors,
g_string_desc_size};
the USB_STR_0, g_string_descriptors and g_string_desc_size are defined as below.
USB_STR_0[4] =    {0x02,
0x03,
0x09,
0x04
};
g_string_descriptors[4] =
{ USB_STR_0,
USB_STR_1,
USB_STR_2,
USB_STR_3};
g_string_desc_size[4] =
{ sizeof(USB_STR_0),
sizeof(USB_STR_1),
sizeof(USB_STR_2),
sizeof(USB_STR_3)};
```

You can make your own structure of USB_STR_1, USB_STR_2, USB_STR_3:

- USB_STR_1 is used for the manufacturer string.
- USB_STR_2 is used for the product string.
- USB_STR_3 is used for the serial number string.

By default, the 3 strings are defined as below:

```
USB_STR_1[] =
{  sizeof(USB_STR_1),
USB_STRING_DESCRIPTOR,
'F',0,
'r',0,
'e',0,
'e',0,
's',0,
'c',0,
'a',0,
'l',0,
'e',0,
' ',0,
'S',0,
'e',0,
'm',0,
'i',0,
'c',0,
'o',0,
'n',0,
'd',0,
'u',0,
'c',0,
't',0,
'o',0,
'r',0,
' ',0,
'I',0,
'n',0,
'c',0,
'.',0
};

USB_STR_2[] =
{  sizeof(USB_STR_2),
USB_STRING_DESCRIPTOR,
'M',0,
'K',0,
' ',0,
'M',0,
'a',0,
's',0,
's',0,
' ',0,
'S',0,
't',0,
'o',0,
'r',0,
'a',0,
'g',0,
'e',0
};

USB_STR_3[] =
{  sizeof(USB_STR_3),
USB_STRING_DESCRIPTOR,
'0',0,
'1',0,
```

```
'2',0,
'3',0,
'4',0,
'5',0,
'6',0,
'7',0,
'8',0,
'9',0,
'A',0,
'B',0,
'C',0,
'D',0,
'E',0,
'F',0
};
```

8.4.5.3 Endpoints

The HID peripheral uses 3 endpoints:

- Control (0)
- Interrupt IN (1)
- Interrupt OUT (2)

The Interrupt OUT endpoint is optional for HID class devices, but the Kinetis Bootloader uses it as a pipe, where the firmware can NAK send requests from the USB host.

8.4.5.4 HID reports

There are 4 HID reports defined and used by the bootloader USB HID peripheral. The report ID determines the direction and type of packet sent in the report; otherwise, the contents of all reports are the same.

Report ID	Packet Type	Direction
1	Command	OUT
2	Data	OUT
3	Command	IN
4	Data	IN

For all reports, these properties apply:

Usage Min	1
Usage Max	1
Logical Min	0

Table continues on the next page...

Logical Max	255
Report Size	8
Report Count	34

Each report has a maximum size of 34 bytes. This is derived from the minimum bootloader packet size of 32 bytes, plus a 2-byte report header that indicates the length (in bytes) of the packet sent in the report.

NOTE

In the future, the maximum report size may be increased, to support transfers of larger packets. Alternatively, additional reports may be added with larger maximum sizes.

The actual data sent in all of the reports looks like:

0	Report ID
1	Packet Length LSB
2	Packet Length MSB
3	Packet[0]
4	Packet[1]
5	Packet[2]
	...
N+3-1	Packet[N-1]

This data includes the Report ID, which is required if more than one report is defined in the HID report descriptor. The actual data sent and received has a maximum length of 35 bytes. The Packet Length header is written in little-endian format, and it is set to the size (in bytes) of the packet sent in the report. This size does not include the Report ID or the Packet Length header itself. During a data phase, a packet size of 0 indicates a data phase abort request from the receiver.

8.5 Get/SetProperty Command Properties

This section lists the properties of the GetProperty and SetProperty commands.

Table 8-56. Properties used by Get/SetProperty Commands, sorted by Value

Property	Writable	Tag Value	Size	Descripion
CurrentVersion	No	01h	4	Current bootloader version.
AvailablePeripherals	No	02h	4	The set of peripherals supported on this chip.

Table continues on the next page...

Table 8-56. Properties used by Get/SetProperty Commands, sorted by Value (continued)

Property	Writable	Tag Value	Size	Descripion
FlashStartAddress	No	03h	4	Start address of program flash.
FlashSizeInBytes	No	04h	4	Size in bytes of program flash.
FlashSectorSize	No	05h	4	The size in bytes of one sector of program flash. This is the minimum erase size.
FlashBlockCount	No	06h	4	Number of blocks in the flash array.
AvailableCommands	No	07h	4	The set of commands supported by the bootloader.
CRCCheckStatus	No	08h	4	The status of the application CRC check.
VerifyWrites	Yes	0Ah	4	Controls whether the bootloader will verify writes to flash. VerifyWrites feature is enabled by default. 0 - No verification is done. 1 - Enable verification.
MaxPacketSize	No	0Bh	4	Maximum supported packet size for the currently active peripheral interface.
ReservedRegions	No	0Ch	16	List of memory regions reserved by the bootloader. Returned as value pairs (<start-address-of-region>, <end-address-of-region>). • If HasDataPhase flag is not set, then the Response packet parameter count indicates the number of pairs. • If HasDataPhase flag is set, then the second parameter is the number of bytes in the data phase.
RAMStartAddress	No	0Eh	4	Start address of RAM
RAMSizeInBytes	No	0Fh	4	Size in bytes of RAM
SystemDeviceId	No	10h	4	Value of the Kinetis System Device Identification register.
FlashSecurityState	No	11h	4	Indicates whether Flash security is enabled 0 - Flash security is disabled 1 - Flash security is enabled
UniqueDeviceId	No	12h	16	Unique device identification, value of Kinetis Unique Identification registers (16 for K series devices, 12 for KL series devices)
FacSupport	No	13h	4	FAC (Flash Access Control) support flag 0 - FAC not supported 1 - FAC supported
FlashAcessSegmentSize	No	14h	4	The size in bytes of 1 segment of flash
FlashAcessSegmentCount	No	15h	4	FAC segment count (The count of flash access segments within the flash model.)
FlashReadMargin	Yes	16h	4	The margin level setting for flash erase and program verify commands. 0 = Normal 1 = User (default) 2 = Factory

Table continues on the next page...

Table 8-56. Properties used by Get/SetProperty Commands, sorted by Value (continued)

Property	Writable	Tag Value	Size	Descripion
QspiInitStatus	No	17h	4	The result of the QSPI and OTFAD initialization process during startup. 405 - QSPI is not initialized 0 - QSPI is initialized
ExternalMemoryAttributes	No	19h	24	List of attributes supported by the specified memory Id (1=QuadSpi0). See description for the return value in the section ExternalMemoryAttributes Property.

8.5.1 Property Definitions

Get/Set property definitions are provided in this section.

8.5.1.1 CurrentVersion Property

The value of this property is a 4-byte structure containing the current version of the bootloader.

Table 8-57. Fields of CurrentVersion property:

Bits	[31:24]	[23:16]	[15:8]	[7:0]
Field	Name = 'K' (0x4B)	Major version	Minor version	Bugfix version

8.5.1.2 AvailablePeripherals Property

The value of this property is a bitfield that lists the peripherals supported by the bootloader and the hardware on which it is running.

Table 8-58. Peripheral bits:

Bit	[31:7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Peripheral	Reserved	Reserved	Reserved	USB HID	Reserved	SPI Slave	I2C Slave	LPUART

If the peripheral is available, then the corresponding bit will be set in the property value. All reserved bits must be set to 0.

8.5.1.3 AvailableCommands Property

This property value is a bitfield with set bits indicating the commands enabled in the bootloader. Only commands that can be sent from the host to the target are listed in the bitfield. Response commands such as GenericResponse are excluded.

The bit number that identifies whether a command is present is the command's tag value minus 1. 1 is subtracted from the command tag because the lowest command tag value is 0x01. To get the bit mask for a given command, use this expression:

```
mask = 1 << (tag - 1)
```

Table 8-59. Command bits:

Bit	[31:17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Command	Reserved	ConfigureQuadSPI	FlashReadResource	FlashReadOnce	FlashProgramOnce	FlashEraseAllUnsecure	SetProperty	Reset	Call	Execute	ReceiveSBFile	GetProperty	FlashSecurityDisable	FillMemory	WriteMemory	ReadMemory	FlashEraseRegion	FlashEraseAll

8.5.1.4 ExternalMemoryAttributes Property

The value returned by this property is a 24-byte data structure containing available external memory attributes: start address, total size in KB, page size, sector size, and block size. Below is the breakdown of 24-byte structure:

Table 8-60. Fields of ExternalMemoryAttributes property:

Field Offset	Field Description
0 - 3	The value returned is a bitmap showing the supported attributes for the external memory, with the corresponding bit-field set. 0x00000001 - start address 0x00000002 - total size 0x00000004 - page size 0x00000008 - sector size 0x00000010 - block size
4 - 7	Start address of external memory
8 - 11	Total size of external memory in terms of kilobytes

Table continues on the next page...

Table 8-60. Fields of ExternalMemoryAttributes property: (continued)

Field Offset	Field Description
12 - 15	Page size of external memory in terms of bytes
16 - 19	Sector size of external memory in terms of bytes
20 - 23	Block size of external memory in terms of bytes

8.6 SB File Decryption Support

The bootloader supports the loading and flashing of applications using an encrypted SB file format. Using the ReceiveSbFile command, the host can send an SB file that contains various commands and data that will be executed on the Kinetis bootloader (the target). An unencrypted SB file can be flashed to the target only when flash security is disabled. When flash security is enabled, all memory writes and reads are disabled, with the exception being an encrypted SB file that can be sent to the target. The SB file is decrypted using an AES-128 style key (16 bytes). Before you send the encrypted file, the key must be written to the target using the FlashProgramOnce command. The SB key begins at offset 0x30 in the program once registers.

For example, to program a key of 000102030405060708090A0B0C0D0E0F:

- FlashProgramOnce to index 0x30 with 4 bytes of 0x03020100
- FlashProgramOnce to index 0x31 with 4 bytes of 0x07060504
- FlashProgramOnce to index 0x32 with 4 bytes of 0x0B0A0908
- FlashProgramOnce to index 0x33 with 4 bytes of 0x0F0E0D0C

If no key is programmed in these registers, then an attempt is made to decrypt the file using an all-zero key.

8.6.1 Decryption using MMCAU

The MMCAU code must flashed to the device memory in a separate step. The location of MMCAU initialization, encryption, and decryption functions does not matter, as long as it is on accessible memory. The provided functions are expected to have the following prototypes:

```
    void mmcau_aes_init(unsigned int* key, unsigned int* keySchedule, unsigned int* rcon);
    void mmcau_aes_encrypt(unsigned int* in, unsigned int* key, unsigned int* keySchedule,
unsigned int* out);
    void mmcau_aes_decrypt(unsigned int* in, unsigned int* key, unsigned int* keySchedule,
unsigned int* out);
```

NOTE

The mmCAU software library source code can be downloaded from Freescale.com.

In order to decrypt an encrypted SB file using the MMCAU peripheral, the following information must be provided:

- The Bootloader Configuration Area (BCA) contains a pointer to an MMCAU set-up structure. The location in the configuration area (relative to the BCA) is at offset 0x20, as shown in the BCA layout in this document. The pointer is a little endian memory location that contains the following structure:

```
        typedef struct mmcau_function_info
{
    uint32_t tag;
    uint32_t length;
    uint32_t aes_init_start;
    uint32_t aes_encrypt_start;
    uint32_t aes_decrypt_start;
} mmcau_function_info_t;
```

  For decryption to work properly, the mmcau_function_info structure must contain valid values for all the fields in this structure:
  a. The tag field must equal 'kcau'.
  b. The length field must equal the size of the total length of the aes_init, aes_encrypt, and aes_decrypt functions. All of these function must be in a contiguous region of memory that fits within 1280 bytes. All code in the functions must be relocatable.
  c. aes_init_start contains the memory location of the aes_init function.
  d. aes_encrypt_start contains the memory location of the aes_encrypt function.
  e. aes_decrypt_start contains the memory location of the aes_decrypt function.
- The MMCAU information structure and the actual MMCAU functions do not need to be in contiguous memory.
- Freescale has a ready-to-use library that contains these functions, but this library needs to be rebuilt to be compatible with the prototypes above. Specifically, the rcon variable needs to be passed into the functions, to make the code relocatable.

After an encrypted SB file starts to be received by the bootloader, the information for setting up the MMCAU is retrieved and the decryption process begins.

- If the information is incorrect or if the functions do not meet the above requirements, then the bootloader can become unresponsive, so be sure that everything is correctly implemented as above.
- If there is a recoverable error, then the bootloader will return a relevant error code.

If everything is operating properly, then the exact same response will be received as though the bootloader was receiving an unencrypted file via the ReceiveSbFile command.

8.6.2 Decryption using LTC

SB file decryption is performed by the LTC module; see the LTC chapter for more details.

8.6.3 Decryption of an Encrypted Application Image via OTFAD

The OTFAD module supports on-the-fly decryption (using AES-CTR-128) of an encrypted program image, as opposed to using the ReceiveSbFile command (which will decrypt and store the image plaintext on the device). The OTFAD allows you to store an encrypted image on the external QSPI device, and it will be decrypted and executed on the fly. For the decryption to work properly, there are several steps that must be performed to properly provision the OTFAD.

The application will consist of 2 parts:

- One application part (with the initialization vectors, bootloader configuration, and the OTFAD setup information) resides on internal flash that will be used by the bootloader.
- The second application part will be the encrypted application image that will be stored on the external QSPI.

After these images are properly created, these images must be written to their respective memory addresses on the device using the bootloader. Upon reset and if everything is configured correctly, the application should be running just like any normal unencrypted application would be. The steps for creating these application images are:

- Create the Internal Flash Image
- Create the Keyblob
- Create the External QSPI Image
- Encrypt the QSPI Section Image

8.6.3.1 Create the Internal Flash Image

The image *that will be written to internal flash* contains several key pieces:

- The normal initialization vectors for the application that will be written to address 0 in the flash. Most importantly these initialization vectors must contain a valid application reset vector and stack pointer.
- The bootloader configuration at address 0x3C0. There are 2 fields in this structure that are used in this process.

- The 1st field is the bootFlags field, in which bit 0 is the flag to indicate "direct boot." When the direct boot flag (bit 0) is set, it instructs the bootloader to jump directly to the application image. When bootFlags field is programmed to 0xFE, the bootloader will perform any secondary configuration that is listed within this section, and jump to the application using the initialization vectors at address 0.
- The 2nd field is the keyblob data pointer field. The keyblob data pointer field is a little endian value that contains the address to the keyblob data structure (which is used to initialize the OTFAD). If no value is provided in the keyblob data pointer field, then the bootloader will attempt configuration using the default address of 0x410. If no keyblob structure is present, then OTFAD will not be initialized and there will be no decryption of the image. The keyblob and OTFAD are only necessary if the image is encrypted.

- The Flash Configuration Area that starts at address 0x400 must contain the flags necessary to boot to ROM, because the bootloader is what configures the OTFAD and decryption. Specifically, the FOPT[BOOTSRC_SEL] field located in the byte (at 0x40D) must be set to 10b, to boot to ROM and configure the QSPI.

8.6.3.2 Create the Keyblob

The keyblob structure is used to initialize the OTFAD, and can contain up to 4 different keys for 4 different data regions in the external QSPI. The keyblob is decrypted using AES-128 ECB encryption. The key for this data must be written using the FlashProgramOnce command, and at the initial register offset of 0x20. For example, to program a key of 000102030405060708090A0B0C0D0E0F for the keyblob encryption key (KEK):

```
FlashProgramOnce to index 0x20 with 4 bytes of 0x0F0E0D0C
FlashProgramOnce to index 0x21 with 4 bytes of 0x0B0A0908
FlashProgramOnce to index 0x22 with 4 bytes of 0x07060504
FlashProgramOnce to index 0x23 with 4 bytes of 0x03020100
```

If the keyblob decryption or structure is either not programmed or fails to properly deserialize, then any image on the external QSPI will not be decrypted.

The keyblob consists of 4 structures of key information in the following format:

```
typedef struct KeyBlob
{
 unsigned char key[kAesKeySizeBytes];       // 16 bytes, 128-bits, KEY[A15...A00]
 unsigned char ctr[kCtrSizeBytes];          // 8 bytes, 64-bits, CTR[C7...C0]
 unsigned int srtaddr;                      // region start, STRADDR[31 - 10]
 unsigned int endaddr;                      // region end, ENDADDR[31 - 10] + flags
R0,ADE,VLD
                                            // end of 32-byte area covered by CRC
 unsigned int zero_fill;                    // zeros
```

```
        unsigned int key_blob_crc32;                // crc32 over 1st 32-bytes
                                                    // end of 40 byte (5*64-bit) key blob data
        unsigned char expanded_wrap_data[8];        // 8 bytes, used for wrap expanded data
                                                    // end of 48 byte (6*64-bit) wrap data
        unsigned char unused_filler[16];            // unused fill to 64 bytes
       } keyblob_t;
```

Each of these entries should be encrypted use the AES-128 Key Wrap algorithm (found at http://csrc.nist.gov/groups/ST/toolkit/documents/kms/key-wrap.pdf)

The individual entries contain important information for the OTFAD decryption process. Because the OTFAD uses the AES-128-CTR algorithm to decrypt an image, the OTFAD needs several pieces of information:

- **AES-128 key value**
- **AES-128 counter value:** This is normally a 16-byte field, but the OTFAD uses only an 8-byte counter field and then additionally uses the address information of the region that it is decrypting, to form the rest of the 16-byte counter.
- The **start address of the application section** for which this key information is relevant.
- The **end address of the application section** for which this key information is relevant.

For example, here is a keyblob structure in raw memory format with the following information:

- A key of 000102030405060708090A0B0C0D0E0F
- An intial counter value of 0123456789ABCDEF
- A start address of 0x68000000
- An end address of 0x68FFFFFF

```
        0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0a, 0x0b, 0x0c, 0x0d,
0x0e, 0x0f
        0x01, 0x23, 0x45, 0x67, 0x89, 0xab, 0xcd, 0xef, 0x00, 0x00, 0x00, 0x68, 0xfb, 0xff,
0xff, 0x68
        0x00, 0x00, 0x00, 0x00, 0x7f, 0xb1, 0x2d, 0xd1, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
0x00, 0x00
        0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
0x00, 0x00
```

After running the AES-128 Key Wrap algorithm on this structure with a KEK of 00000000000000000000000000000001 :

```
        0x20, 0x40, 0xee, 0x75, 0xe5, 0x42, 0xc9, 0x63, 0x49, 0x29, 0x26, 0xd5, 0x81, 0xdd,
0x5a, 0xed,
        0xa3, 0x5d, 0xf2, 0x82, 0xc3, 0x82, 0xe9, 0xfc, 0xae, 0x55, 0x62, 0x60, 0xdd, 0x83,
0xfa, 0x42,
        0x8a, 0x7c, 0x59, 0x6e, 0xd8, 0x59, 0xd5, 0xc2, 0xf1, 0xd2, 0x64, 0xe7, 0x01, 0x5a,
0x08, 0x1b,
        0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
0x00, 0x00,
```

8.6.3.3 Create the External QSPI Image

The image that is written to the external QSPI memory contains 2 or more important sections of data:

- **QSPI configuration block:** which is read from the QSPI base address (0x68000000). The QSPI configuration structure contains information for configuring the specific QSPI part: the structure is read by the bootloader, and then used to configure the QSPI driver. This information must always be unencrypted. See the QSPI section. For certain types of external SPI flash devices which do not support basic read (0x03) command with 24-bit address, the QSPI configuration block should be placed in internal flash.
- **Application data sections:** The application data sections can be encrypted or unencrypted, but the previously described keyblob for the memory region *that the data section is located in* must match.

8.6.3.4 Encrypt the QSPI Section Image

If an encrypted application image is located on the QSPI, then the image is assumed be encrypted using the AES-128-CTR standard. When encrypting the image, the following steps must be taken:

- The AES-128 key used to encrypt the image must match the keyblob's section key for the memory range that the image will be written to.
- The AES-128 counter value is created using an 8-byte initial counter, a 4-byte XOR of the 1st and 2nd 4 bytes of the initial counter, then the 4-byte memory address from the base address where the section will be located at. For example:
  - Initial 8-byte counter: 0123456789ABCDEF
  - 4-byte XOR of the initial counter : 01234567 ^ 89ABCDEF = 88888888
  - Memory address that the image will be written to: 0x68001000
  - Resulting counter value = 0123456789ABCDEF8888888868001000
- When encrypting the image, the counter value must increment by 16 for each successive block of data.
- The data *that is to be encrypted* must be rearranged, in order to be compatible with the OTFAD. For example, to properly shift a 16-byte block of data on a host PC program:

```
uint32_t block[4] = { 0x4917b580, 0x60084817, 0x48184917, 0xbf1c1a42 };

block[0] = endian_reverse(block[0]);
```

```
block[1] = endian_reverse(block[1]);
block[2] = endian_reverse(block[2]);
block[3] = endian_reverse(block[3]);
// block = {0x80b51749, 0x17480860, 0x17491848, 0x421a1cbf};

word_swap(block[0], block[1]);
word_swap(block[2], block[3]);
// block = {0x17480860, 0x80b51749, 0x421a1cbf, 0x17491848};

// key = 000102030405060708090A0B0C0D0E0F
// counter = 0123456789ABCDEF8888888868001000
encrypt(block, 16, block);
// block = {0x8adc1fc9, 0xd63dd732, 0x143aa1e7, 0xa88bba26};

word_swap(block[0], block[1]);
word_swap(block[2], block[3]);
// block = {0xd63dd732, 0x8adc1fc9, 0xa88bba26, 0x143aa1e7};

block[0] = endian_reverse(block[0]);
block[1] = endian_reverse(block[1]);
block[2] = endian_reverse(block[2]);
block[3] = endian_reverse(block[3]);
// block = {0x32d73dd6, 0xc91fdc8a, 0x26ba8ba8, 0xe7a13a14};
```

8.6.4 CRC-32 Check on Application Data

Using CRC-32 and a given address range, the ROM bootloader supports performing an application integrity check. To properly configure this functionality, the following fields in the bootloader configuration area must be set:

- Set crcStartAddress to the start address that should be used for the CRC check.
- Set crcByteCount to the number of bytes to run the CRC check on, from the start address.
- Set crcExpectedValue to the value that the CRC calculation should result in.

Considerations:

- If all of the above fields are unset (all 0xFF bytes for crcStartAddress, crcByteCount, and crcExpectedValue), then the ROM bootloader returns kStatus_AppCrcCheckInvalid.
- If any one of the above fields are set (crcStartAddress, crcByteCount, and crcExpectedValue), then the ROM bootloader checks if the given address range of the application is valid and if the application just resides in internal flash or external QSPI flash:
  - If false, then the bootloader returns kStatus_AppCrcCheckOutOfRange.
  - If true, then the CRC check occurs. If the CRC check fails, then the bootloader returns kStatus_AppCrcCheckFailed; if the CRC check succeeds, then it returns kStatus_AppCrcCheckPassed.

- If the bootloader returns kStatus_AppCrcCheckOutOfRange or kStatus_AppCrcCheckFailed, then an external pin will also be asserted, to indicate CRC check failure.
- Only if kStatus_AppCrcCheckPassed is returned, will the application be jumped to; otherwise the bootloader will stay active, and wait for further commands.

- The CRC32 algorithm in ROM uses a polynomial (0x04C1_1DB7), and the initial seed is 0xFFFF_FFFF.

8.7 Kinetis Bootloader Status Error Codes

This section describes the status error codes that the Kinetis Bootloader returns to the host.

Table 8-61. Kinetis Bootloader Status Error Codes, sorted by Value

Error Code	Value	Description
kStatus_Success	0	Operation succeeded without error.
kStatus_Fail	1	Operation failed with a generic error.
kStatus_ReadOnly	2	Requested value cannot be changed because it is read-only.
kStatus_OutOfRange	3	Requested value is out of range.
kStatus_InvalidArgument	4	The requested command's argument is undefined.
kStatus_Timeout	5	A timeout occurred.
kStatus_FlashSizeError	100	Not used.
kStatus_FlashAlignmentError	101	Address or length does not meet required alignment.
kStatus_FlashAddressError	102	Address or length is outside addressable memory.
kStatus_FlashAccessError	103	The FTFA_FSTAT[ACCERR] bit is set.
kStatus_FlashProtectionViolation	104	The FTFA_FSTAT[FPVIOL] bit is set.
kStatus_FlashCommandFailure	105	The FTFA_FSTAT[MGSTAT0] bit is set.
kStatus_FlashUnknownProperty	106	Unknown Flash property.
kStatus_FlashEraseKeyError	107	The key provided does not match the programmed flash key.
kStatus_FlashRegionExecuteOnly	108	The area of flash is protected as execute only.
kStatus_I2C_SlaveTxUnderrun	200	I2C Slave TX Underrun error.
kStatus_I2C_SlaveRxOverrun	201	I2C Slave RX Overrun error.
kStatus_I2C_AribtrationLost	202	I2C Arbitration Lost error.
kStatus_SPI_SlaveTxUnderrun	300	SPI Slave TX Underrun error.
kStatus_SPI_SlaveRxOverrun	301	SPI Slave RX Overrun error.
kStatus_SPI_Timeout	302	SPI tranfser timed out.
kStatus_SPI_Busy	303	SPI instance is already busy performing a transfer.
kStatus_SPI_NoTransferInProgress	304	Attempt to abort a transfer when no transfer was in progress.
kStatus_QspiFlashSizeError	400	The detected flash size is incorrect.
kStatus_QspiFlashAlignmentError	401	The address that is being written to is not properly aligned.

Table continues on the next page...

Table 8-61. Kinetis Bootloader Status Error Codes, sorted by Value (continued)

Error Code	Value	Description
kStatus_QspiFlashAddressError	402	The QSPI address is invalid.
kStatus_QspiFlashCommandFailure	403	The QSPI command failed.
kStatus_QspiFlashUnknownProperty	404	The property is not supported.
kStatus_QspiNotConfigured	405	The QSPI has not been configured.
kStatus_QspiCommandNotSupported	406	The operation is not supported.
kStatus_QspiCommandTimeout	407	The time that external SPI devices are busy is more than the specified timeout value.
kStatus_QspiWriteFailure	408	The QSPI module cannot perform a program command at the current clock frequency.
kStatus_UnknownCommand	10000	The requested command value is undefined.
kStatus_SecurityViolation	10001	Command is disallowed because flash security is enabled.
kStatus_AbortDataPhase	10002	Abort the data phase early.
kStatus_Ping	10003	Internal: received ping during command phase.
kStatusRomLdrSectionOverrun	10100	The loader has finished processing the SB file.
kStatusRomLdrSignature	10101	The signature of the SB file is incorrect.
kStatusRomLdrSectionLength	10102	The section length in chunks is invalid.
kStatusRomLdrUnencryptedOnly	10103	An encrypted SB file has been sent and decryption support is not available.
kStatusRomLdrEOFReached	10104	The end of the SB file has been reached.
kStatusRomLdrChecksum	10105	The checksum of a command tag block is invalid.
kStatusRomLdrCrc32Error	10106	The CRC-32 of the data for a load command is incorrect.
kStatusRomLdrUnknownCommand	10107	An unknown command was found in the SB file.
kStatusRomLdrIdNotFound	10108	There was no bootable section found in the SB file.
kStatusRomLdrDataUnderrun	10109	The SB state machine is waiting for more data.
kStatusRomLdrJumpReturned	10110	The function that was jumped to by the SB file has returned.
kStatusRomLdrCallFailed	10111	The call command in the SB file failed.
kStatusRomLdrKeyNotFound	10112	A matching key was not found in the SB file's key dictionary to unencrypt the section.
kStatusRomLdrSecureOnly	10113	The SB file sent is unencrypted and security on the target is enabled.
kStatusRomLdrResetReturned	10114	The SB file reset operation has unexpectedly returned.
kStatusMemoryRangeInvalid	10200	Memory range conflicts with a protected region.
kStatus_UnknownProperty	10300	The requested property value is undefined.
kStatus_ReadOnlyProperty	10301	The requested property value cannot be written.
kStatus_InvalidPropertyValue	10302	The specified property value is invalid.
kStatus_AppCrcCheckPassed	10400	CRC check is valid and passed.
kStatus_AppCrcCheckFailed	10401	CRC check is valid but failed.
kStatus_AppCrcCheckInactive	10402	CRC check is inactive.
kStatus_AppCrcCheckInvalid	10403	CRC check is invalid, because the BCA is invalid or the CRC parameters are unset (all 0xFF bytes).
kStatus_AppCrcCheckOutOfRange	10404	CRC check is valid but addresses are out of range.

Chapter 9
Power Management

9.1 Introduction

This chapter describes the various chip power modes and functionality of the individual modules in these modes.

9.2 Clocking modes

Information found here describes the various clocking modes supported on this device.

9.2.1 Partial Stop

Partial Stop is a clocking option that can be taken instead of entering Stop mode and is configured in the SMC Stop Control Register (SMC_STOPCTRL). The Stop mode is only partially entered, which leaves some additional functionality alive at the expense of higher power consumption. Partial Stop can be entered from either Run mode or VLP Run mode.

When configured for PSTOP2, only the core and system clocks are gated and the bus clock remains active. The bus masters and bus slaves clocked by the system clock enter Stop mode, but the bus slaves clocked by bus clock remain in Run (or VLP Run) mode. The clock generators in the MCG and the on-chip regulator in the PMC also remain in Run (or VLP Run) mode. Exit from PSTOP2 can be initiated by a reset, an asynchronous interrupt from a bus master or bus slave clocked by the system clock, or a synchronous interrupt from a bus slave clocked by the bus clock. If configured, a DMA request (using the asynchronous DMA wakeup) can also be used to exit Partial Stop for the duration of a DMA transfer before the device is transitioned back into PSTOP2.

When configured for PSTOP1, both the system clock and bus clock are gated. All bus masters and bus slaves enter Stop mode, but the clock generators in the MCG and the on-chip regulator in the PMC remain in Run (or VLP Run) mode. Exit from PSTOP1 can be initiated by a reset or an asynchronous interrupt from a bus master or bus slave. If configured, an asynchronous DMA request can also be used to exit Partial Stop for the duration of a DMA transfer before the device is transitioned back into PSTOP1.

PSTOP1 is functionally similar to Stop mode, but offers faster wake-up at the expense of higher power consumption. Another benefit is that it keeps all of the MCG clocks enabled, which can be useful for some of the asynchronous peripherals that can remain functional in Stop modes.

9.2.2 DMA Wakeup

The DMA can be configured to wake the device on a DMA request whenever it is placed in Stop mode. The wake-up is configured per DMA channel and is supported in Compute Operation, PSTOP, STOP, and VLPS low power modes.

When a DMA wake-up is detected in PSTOP, STOP or VLPS then the device will initiate a normal exit from the low power mode. This can include restoring the on-chip regulator and internal power switches, enabling the clock generators in the MCG, enabling the system and bus clocks (but not the core clock) and negating the stop mode signal to the bus masters and bus slaves. The only difference is that the CPU will remain in the low power mode with the CPU clock disabled.

During Compute Operation, a DMA wake-up will initiate a normal exit from Compute Operation. This includes enabling the clocks and negating the stop mode signal to the bus masters and bus slaves. The core clock always remains enabled during Compute Operation.

Since the DMA wakeup will enable the clocks and negate the stop mode signals to all bus masters and slaves, software needs to ensure that bus masters and slaves that are not involved with the DMA wake-up and transfer remain in a known state. That can be accomplished by disabling the modules before entry into the low power mode or by setting the Doze enable bit in selected modules.

Once the DMA request that initiated the wake-up negates and the DMA completes the current transfer, the device will transition back to the original low-power mode. This includes requesting all non-CPU bus masters to enter Stop mode and then requesting bus slaves to enter Stop mode. In STOP and VLPS modes the MCG and PMC would then also enter their appropriate modes.

NOTE

If the requested DMA transfer cannot cause the DMA request to negate then the device will remain in a higher power state until the low power mode is fully exited.

An enabled DMA wake-up can cause an aborted entry into the low power mode, if the DMA request asserts during the stop mode entry sequence (or reentry if the request asserts during a DMA wakeup) and can cause the SMC to assert its Stop Abort flag. Once the DMA wake-up completes, entry into the low power mode will restart.

An interrupt that occurs during a DMA wake-up will cause an immediate exit from the low power mode (this is optional for Compute Operation) without impacting the DMA transfer.

A DMA wake-up can be generated by either a synchronous DMA request or an asynchronous DMA request. Not all peripherals can generate an asynchronous DMA request in stop modes, although in general if a peripheral can generate synchronous DMA requests and also supports asynchronous interrupts in stop modes, then it can generate an asynchronous DMA request.

9.2.3 Compute Operation

Compute Operation is an execution or compute-only mode of operation that keeps the CPU enabled with full access to the SRAM and Flash read port, but places all other bus masters and bus slaves into their stop mode. Compute Operation can be enabled in either Run mode, High Speed Run mode or VLP Run mode.

NOTE

Do not enter any stop mode without first exiting Compute Operation.

Because Compute Operation reuses the stop mode logic (including the staged entry with bus masters disabled before bus slaves), any bus master or bus slave that can remain functional in stop mode also remains functional in Compute Operation, including generation of asynchronous interrupts and DMA requests. When enabling Compute Operation in Run mode, module functionality for bus masters and slaves is the equivalent of STOP mode. When enabling Compute Operation in VLP Run mode, module functionality for bus masters and slaves is the equivalent of VLPS mode. The MCG, PMC, SRAM and Flash read port are not affected by Compute Operation, although the Flash register interface is disabled.

During Compute Operation, the AIPS peripheral and external memory (FlexBus, SDRAM controller) space and QSPI is disabled and attempted accesses generate bus errors. The private peripheral bus (PPB) remains accessible during Compute Operation, including the MCM, System Control Space (SCS) (for NVIC and FPU), MMCAU and SysTick. Although access to the GPIO registers is supported, the GPIO port data input registers do not return valid data since clocks are disabled to the Port Control and Interrupt modules. By writing to the GPIO port data output registers, it is possible to control those GPIO ports that are configured as output pins.

Compute Operation is controlled by the CPO register in the MCM, which is only accessible to the CPU. Setting or clearing the CPOREQ bit in the MCM initiates entry or exit into Compute Operation. Compute Operation can also be configured to exit automatically on detection of an interrupt, which is required in order to service most interrupts. Only the core system interrupts (exceptions, including NMI and SysTick) and any edge sensitive interrupts can be serviced without exiting Compute Operation.

When entering Compute Operation, the CPOACK status bit indicates when entry has completed. When exiting Compute Operation in Run mode, the CPOACK status bit negates immediately. When exiting Compute Operation in VLP Run mode, the exit is delayed to allow the PMC to handle the change in power consumption. This delay means the CPOACK bit is polled to determine when the AIPS peripheral space can be accessed without generating a bus error.

The DMA wakeup is also supported during Compute Operation and causes the CPOACK status bit to clear and the AIPS peripheral space to be accessible for the duration of the DMA wakeup. At the completion of the DMA wakeup, the device transitions back into Compute Operation.

9.2.4 Peripheral Doze

Several peripherals support a Peripheral Doze mode, where a register bit can be used to disable the peripheral for the duration of a low-power mode. The flash memory can also be placed in a low-power state during Peripheral Doze via a register bit in the SIM.

Peripheral Doze is defined to include all of the modes of operation listed below.

- The CPU is in Wait mode.
- The CPU is in Stop mode, including the entry sequence and for the duration of a DMA wakeup.
- The CPU is in Compute Operation, including the entry sequence and for the duration of a DMA wakeup.

Peripheral Doze can therefore be used to disable selected bus masters or slaves for the duration of WAIT or VLPW mode. It can also be used to disable selected bus slaves immediately on entry into any stop mode (or Compute Operation), instead of waiting for the bus masters to acknowledge the entry as part of the stop entry sequence. Finally, it can be used to disable selected bus masters or slaves that should remain inactive during a DMA wakeup.

If the flash memory is not being accessed during WAIT and PSTOP modes, then the Flash Doze mode can be used to reduce power consumption, at the expense of a slightly longer wake-up when executing code and vectors from flash. It can also be used to reduce power consumption during Compute Operation when executing code and vectors from SRAM.

9.2.5 Clock Gating

To conserve power, the clocks to most modules can be turned off using the SCGCx registers in the SIM module. These bits are cleared after any reset, which disables the clock to the corresponding module. Prior to initializing a module, set the corresponding bit in the SCGCx register to enable the clock. Before turning off the clock, make sure to disable the module. For more details, refer to the clock distribution and SIM chapters.

9.3 Power Modes Description

The power management controller (PMC) provides multiple power options to allow the user to optimize power consumption for the level of functionality needed.

Depending on the stop requirements of the user application, a variety of stop modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. The following table compares the various power modes available.

For Run and VLPR mode there is a corresponding wait and stop mode. Wait modes are similar to ARM® sleep modes. Stop modes (VLPS, STOP) are similar to ARM sleep deep mode. The very low power run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

Stop mode entry is not supported directly from HSRUN and requires transition to Run prior to an attempt to enter a stop mode.

The three primary modes of operation are run, wait and stop. The WFI instruction invokes both wait and stop modes for the chip. The primary modes are augmented in a number of ways to provide lower power based on application needs.

Table 9-1. Chip power modes

Chip mode	Description	Core mode	Normal recovery method
Normal run	Default mode out of reset; on-chip voltage regulator is on.	Run	-
High Speed run	Allows maximum performance of chip. In this state, the MCU is able to operate at a faster frequency compared to normal run mode.	Run	-
Normal Wait - via WFI	Allows peripherals to function while the core is in sleep mode, reducing power. NVIC remains sensitive to interrupts; peripherals continue to be clocked.	Sleep	Interrupt
Normal Stop - via WFI	Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection. NVIC is disabled; AWIC is used to wake up from interrupt; peripheral clocks are stopped.	Sleep Deep	Interrupt
VLPR (Very Low Power Run)	On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. Reduced frequency Flash access mode (1 MHz); LVD off; internal oscillator provides a low power 4 MHz source for the core, the bus and the peripheral clocks.	Run	-
VLPW (Very Low Power Wait) -via WFI	Same as VLPR but with the core in sleep mode to further reduce power; NVIC remains sensitive to interrupts (FCLK = ON). On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency.	Sleep	Interrupt
VLPS (Very Low Power Stop)-via WFI	Places chip in static state with LVD operation off. Lowest power mode with ADC and pin interrupts functional. Peripheral clocks are stopped, but LPTimer, RTC, CMP , TSI, DAC can be used. NVIC is disabled (FCLK = OFF); AWIC is used to wake up from interrupt. On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. All SRAM is operating (content retained and I/O states held).	Sleep Deep	Interrupt
LLS3 (Low Leakage Stop3)	State retention power mode. Most peripherals are in state retention mode (with clocks stopped), but LLWU, LPTimer, RTC, CMP , TSI, DAC can be used. NVIC is disabled; LLWU is used to wake up. **NOTE:** The LLWU interrupt must not be masked by the interrupt controller to avoid a scenario where the system does not fully exit stop mode on an LLS recovery. All SRAM is operating (content retained and I/O states held).	Sleep Deep	Wakeup Interrupt[1]
LLS2 (Low Leakage Stop2)	State retention power mode. Most peripherals are in state retention mode (with clocks stopped), but LLWU, LPTimer, RTC, CMP , TSI, DAC can be used. NVIC is disabled; LLWU is used to wake up. **NOTE:** The LLWU interrupt must not be masked by the interrupt controller to avoid a scenario where the system does not fully exit stop mode on an LLS recovery. A portion of SRAM_U remains powered on (content retained and I/O states held).	Sleep Deep	Wakeup Interrupt[1]

Table continues on the next page...

Table 9-1. Chip power modes (continued)

Chip mode	Description	Core mode	Normal recovery method
VLLS3 (Very Low Leakage Stop3)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP , TSI, DAC can be used. NVIC is disabled; LLWU is used to wake up. SRAM_U and SRAM_L remain powered on (content retained and I/O states held).	Sleep Deep	Wakeup Reset[2]
VLLS2 (Very Low Leakage Stop2)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP , TSI, DAC can be used. NVIC is disabled; LLWU is used to wake up. SRAM_L is powered off. A portion of SRAM_U remains powered on (content retained and I/O states held).	Sleep Deep	Wakeup Reset[2]
VLLS1 (Very Low Leakage Stop1)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP , TSI, DAC can be used. NVIC is disabled; LLWU is used to wake up. All of SRAM_U and SRAM_L are powered off. The 32-byte system register file and the 128-byteVBAT register file remain powered for customer-critical data.	Sleep Deep	Wakeup Reset[2]
VLLS0 (Very Low Leakage Stop 0)	Most peripherals are disabled (with clocks stopped), but LLWU and RTC can be used. NVIC is disabled; LLWU is used to wake up. All of SRAM_U and SRAM_L are powered off. The 32-byte system register file and the 128-byte VBAT register file remain powered for customer-critical data. The POR detect circuit can be optionally powered off.	Sleep Deep	Wakeup Reset[2]
BAT (backup battery only)	The chip is powered down except for the VBAT supply. The RTC and the 128-byte VBAT register file for customer-critical data remain powered.	Off	Power-up Sequence

1. Resumes normal run mode operation by executing the LLWU interrupt service routine.
2. Follows the reset flow with the LLWU interrupt flag set for the NVIC.

9.4 Entering and exiting power modes

The WFI instruction invokes wait and stop modes for the chip. The processor exits the low-power mode via an interrupt. The Nested Vectored Interrupt Controller (NVIC) describes interrupt operation and what peripherals can cause interrupts.

NOTE

The WFE instruction can have the side effect of entering a low-power mode, but that is not its intended usage. See ARM documentation for more on the WFE instruction.

Recovery from VLLSx is through the wake-up Reset event. The chip wake-ups from VLLSx by means of reset, an enabled pin or enabled module. See the table "LLWU inputs" in the LLWU configuration section for a list of the sources.

The wake-up flow from VLLSx is through reset. The wakeup bit in the SRS registers in the RCM is set indicating that the chip is recovering from a low power mode. Code execution begins; however, the I/O pins are held in their pre low power mode entry states, and the system oscillator and MCG registers are reset (even if EREFSTEN had been set before entering VLLSx). Software must clear this hold by writing a 1 to the ACKISO bit in the Regulator Status and Control Register in the PMC module.

NOTE

To avoid unwanted transitions on the pins, software must re-initialize the I/O pins to their pre-low-power mode entry states *before* releasing the hold.

If the oscillator was configured to continue running during VLLSx modes, it must be re-configured before the ACKISO bit is cleared. The oscillator configuration within the MCG is cleared after VLLSx recovery and the oscillator will stop when ACKISO is cleared unless the register is re-configured.

The IRC48MCLK is not forced disabled in Stop modes and should be disabled by software prior to Stop mode entry unless it is required. The IRC48MCLK is not forced disabled in VLPR and should be disabled by software prior to VLPR entry.

The SDRAM controller should be idle before entering any stop modes. This idle state can be achieved under any one of the following conditions:

- SDRAM controller has never been used
- SDRAM controller has been used, but there is no active command and refresh is not enabled (SDRAM_AC0[RE] = 0 and SDRAM_AC1[RE] = 0)
- SDRAM controller has been used, and the last command was a self-refresh command (SDRAM_CTRL[IS] = 1)

9.5 Power mode transitions

The following figure shows the power mode transitions. Any reset always brings the chip back to the normal run state. In run, wait, and stop modes active power regulation is enabled. The VLPx modes offer a lower power operating mode than normal modes. VLPR and VLPW are limited in frequency. The LLS and VLLSx mode(s) are the lowest power stop modes based on amount of logic or memory that is required to be retained by the application.

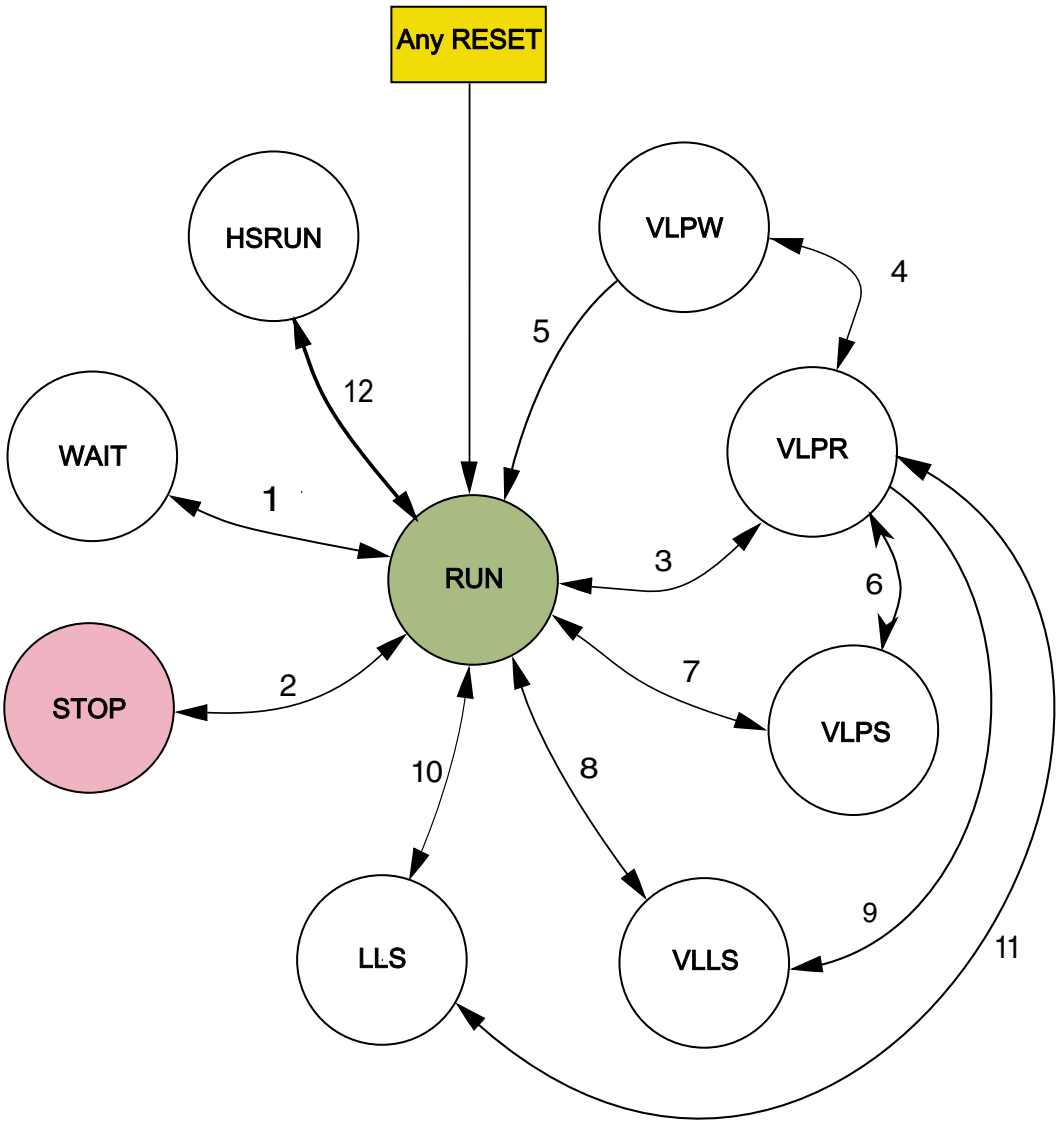


Figure 9-1. Power mode state transition diagram

9.6 Power modes shutdown sequencing

When entering stop or other low-power modes, the clocks are shut off in an orderly sequence to safely place the chip in the targeted low-power state. All low-power entry sequences are initiated by the core executing an WFI instruction. The ARM core's outputs, SLEEPDEEP and SLEEPING, trigger entry to the various low-power modes:

- System level wait and VLPW modes equate to: SLEEPING & $\overline{\text{SLEEPDEEP}}$
- All other low power modes equate to: SLEEPING & SLEEPDEEP

When entering the non-wait modes, the chip performs the following sequence:

- Shuts off Core Clock and System Clock to the ARM Cortex-M4 core immediately.
- Polls stop acknowledge indications from the non-core crossbar masters (DMA), supporting peripherals (SPI, PIT, TRNG) and the Flash Controller for indications that System Clocks, Bus Clock and/or Flash Clock need to be left enabled to complete a previously initiated operation, effectively stalling entry to the targeted low power mode. When all acknowledges are detected, System Clock, Bus Clock and Flash Clock are turned off at the same time.
- MCG and Mode Controller shut off clock sources and/or the internal supplies driven from the on-chip regulator as defined for the targeted low power mode.

In wait modes, most of the system clocks are not affected by the low power mode entry. The Core Clock to the ARM Cortex-M4 core is shut off. Some modules support stop-in-wait functionality and have their clocks disabled under these configurations.

The debugger modules support a transition from stop, wait, VLPS, and VLPW back to a halted state when the debugger is enabled. This transition is initiated by setting the Debug Request bit in MDM-AP control register. As part of this transition, system clocking is re-established and is equivalent to normal run/VLPR mode clocking configuration.

9.7 Flash Program Restrictions

The flash memory on this device should not be programmed or erased while operating in High Speed Run or VLPR power modes.

9.8 Module Operation in Low Power Modes

The following table illustrates the functionality of each module while the chip is in each of the low power modes. The standard behavior is shown with some exceptions for Compute Operation (CPO) and Partial Stop2 (PSTOP2).

(Debug modules are discussed separately; see Debug in Low Power Modes.) Number ratings (such as 2 MHz and 1 Mbit/s) represent the maximum frequencies or maximum data rates per mode. Also, these terms are used:

- FF = Full functionality. In VLPR and VLPW the system frequency is limited, but if a module does not have a limitation in its functionality, it is still listed as FF.
- Async operation = Fully functional with alternate clock source, provided the selected clock source remains enabled
- static = Module register states and associated memories are retained.
- powered = Memory is powered to retain contents.
- low power = Memory is powered to retain contents in a lower power state

- OFF = Modules are powered off; module is in reset state upon wakeup. For clocks, OFF means disabled.
- wakeup = Modules can serve as a wakeup source for the chip.

Table 9-2. Module operation in low power modes

Modules	VLPR	VLPW	Stop	VLPS	LLSx	VLLSx
Core modules						
NVIC	FF	FF	static	static	static	OFF
System modules						
Mode Controller	FF	FF	FF	FF	FF	FF
LLWU[1]	static	static	static	static	FF	FF[2]
Regulator	low power	low power	ON	low power	low power	low power in VLLS2/3, OFF in VLLS0/1
LVD	disabled	disabled	ON	disabled	disabled	disabled
Brown-out Detection	ON	ON	ON	ON	ON	ON in VLLS1/2/3, optionally disabled in VLLS0[3]
DMA	FF Async operation in CPO	FF	Async operation	Async operation	static	OFF
Watchdog	FF	FF	FF	FF	static	OFF
EWM	FF static in CPO	static	static FF in PSTOP2	static	static	OFF
Clocks						
1kHz LPO	ON	ON	ON	ON	ON	ON in VLLS1/2/3, OFF in VLLS0
System oscillator (OSC)	OSCERCLK max of 16 MHz crystal	OSCERCLK max of 16 MHz crystal	OSCERCLK optional	OSCERCLK max of 16 MHz crystal	limited to low range/low power	limited to low range/low power in VLLS1/2/3, OFF in VLLS0
MCG	4 MHz IRC	4 MHz IRC	static - MCGIRCLK optional ; PLL optionally on but gated	static - MCGIRCLK optional (4 MHz IRC only).	static - no clock output	OFF
Core clock	4 MHz max	OFF	OFF	OFF	OFF	OFF
Platform clock	4 MHz max	4 MHz max	OFF	OFF	OFF	OFF
System clock	4 MHz max OFF in CPO	4 MHz max	OFF	OFF	OFF	OFF
Bus clock	4 MHz max OFF in CPO	4 MHz max	OFF 60 MHz max in PSTOP2 from RUN	OFF	OFF	OFF

Table continues on the next page...

Table 9-2. Module operation in low power modes (continued)

Modules	VLPR	VLPW	Stop	VLPS	LLSx	VLLSx
			4 MHz max in PSTOP2 from VLPR			
Memory and memory interfaces						
Flash	1 MHz max access - no program/erase No register access in CPO	low power	low power	low power	OFF	OFF
System RAM (SRAM_U and SRAM_L) [-1]	low power	low power	low power	low power	low power in LLS3, partial in LLS2	low power in VLLS3, partial in VLLS2; otherwise OFF
Cache	low power	low power	low power	low power	low power	OFF
VBAT Register file[6]	powered	powered	powered	powered	powered	powered
System Register files	powered	powered	powered	powered	powered	powered
SDRAM controller	FF, disabled in CPO	FF	Low power	Low power	Low power	OFF
FlexBus	FF, disabled in CPO	FF	static	static	static	OFF
QSPI	FF, static in CPO	FF	static [7]	static	static	OFF
Communication interfaces						
USB FS/LS	static, wakeup on resume	static, wakeup on resume	static, wakeup on resume	static, wakeup on resume	static	OFF
USB DCD	FF	FF	static	static	static	OFF
USB Voltage Regulator	optional	optional	optional	optional	optional	optional
LPUART	4 Mbps Async operation in CPO	4 Mbps	Async operation FF in PSTOP2	Async operation	static	OFF
SPI	1 Mbit/s (slave) 2 Mbit/s (master) static in CPO	1 Mbit/s (slave) 2 Mbit/s (master)	static FF in PSTOP2	static	static	OFF
I^2C	200 kbit/s static, address match wakeup in CPO	200 kbit/s	static, address match wakeup FF in PSTOP2	static, address match wakeup	static	OFF
I^2S	FF Async operation in CPO	FF	Async operation with external clock[8] FF in PSTOP2	FF with external clock[8]	static	OFF

Table continues on the next page...

Table 9-2. Module operation in low power modes (continued)

Modules	VLPR	VLPW	Stop	VLPS	LLSx	VLLSx
SDHC	FF	FF	wakeup	wakeup	static	OFF
EMVSIM	FF	FF	static	static	static	OFF
FLEXIO	FF	FF	Async operation FF in PSTOP2	Async operation	static	OFF
Security						
CRC	FF static in CPO	FF	static	static	static	OFF
TRNG	FF static in CPO	static	static	static	static	OFF
LTC	FF, static in CPO	FF	static	static	static	OFF
Timers						
FTM	FF static in CPO	FF	static FF in PSTOP2	static	static	OFF
TPM	FF	FF	Async operation FF in PSTOP2	Async operation	static	OFF
PIT	FF static in CPO	FF	static FF in PSTOP2	static	static	OFF
PDB	FF static in CPO	FF	static FF in PSTOP2	static	static	OFF
LPTMR	FF	FF	Async operation FF in PSTOP2	Async operation	Async operation	Async operation[9]
RTC - 32kHz OSC[6]	FF Async operation in CPO	FF	Async operation FF in PSTOP2	Async operation	Async operation[10]	Async operation[10]
CMT	FF static in CPO	FF	static FF in PSTOP2	static	static	OFF
Analog						
16-bit ADC	FF ADACK and ALTCLK clocks only in CPO	FF	ADACK, ALTCLK, and ALTCLK2 clocks only FF in PSTOP2	ADACK and ALTCLK clocks only	static	OFF
CMP[11]	FF HS or LS compare in CPO	FF	HS or LS compare FF in PSTOP2	HS or LS compare	LS compare	LS compare in VLLS1/2/3, OFF in VLLS0
6-bit DAC	FF static in CPO	FF	static FF in PSTOP2	static	static	static, OFF in VLLS0
VREF	FF	FF	FF	FF	static	OFF
12-bit DAC	FF	FF	static	static	static	static

Table continues on the next page...

Table 9-2. Module operation in low power modes (continued)

Modules	VLPR	VLPW	Stop	VLPS	LLSx	VLLSx
	static in CPO		FF in PSTOP2			
Human-machine interfaces						
GPIO	FF GPIO write only in CPO	FF	static output, wakeup input FF in PSTOP2	static output, wakeup input	static, pins latched	OFF, pins latched
TSI0	FF Async operation in CPO	Async operation	Async operation [12] FF in PSTOP2	Async operation [12]	Async operation [12]	Async operation [12]

1. Using the LLWU module, the external pins available for this chip do not require the associated peripheral function to be enabled. It only requires the function controlling the pin (GPIO or peripheral) to be configured as an input to allow a transition to occur to the LLWU.
2. Since LPO clock source is disabled, filters will be bypassed during VLLS0
3. The SMC_STOPCTRL[PORPO] bit in the SMC module controls this option.
4. 32 kB of SRAM_U block is in low power when MCU is in low power modes LLS2 and VLLS2. 32 kB of SRAM_L block is optionally left powered on in low power modes LLS2 and VLLS2 via configuration of the SMC_STOPCTRL[RAM2PO]. The remaining System RAM is OFF in LLS2 and VLLS2.
5. 32 kB of SRAM_U block is in low power when MCU is in low power modes LLS2 and VLLS2. 32 kB of SRAM_L block is optionally left powered on in low power modes LLS2 and VLLS2 via configuration of the SMC_STOPCTRL[RAM2PO]. The remaining System RAM is OFF in LLS2 and VLLS2.
6. These components remain powered in BAT power mode.
7. the QSPI module may require specific instructions to enter low power prior to the MCU entering low power.
8. Use an externally generated bit clock or an externally generated audio master clock (including EXTAL).
9. System OSC and LPO clock sources are not available in VLLS0. Pulse counting is available in all modes.
10. RTC_CLKOUT is not available.
11. CMP in stop or VLPS supports high speed or low speed external pin to pin or external pin to DAC compares. CMP in LLSx or VLLSx only supports low speed external pin to pin or external pin to DAC compares. Windowed, sampled & filtered modes of operation are not available while in stop, VLPS, LLSx, or VLLSx modes.
12. TSI wakeup from all low power modes is limited to a single selectable pin.

NOTE

Modules that are functional in Stop mode are supported during Compute operation

Chapter 10
Flash Security Measures & Module Interactions

10.1 Introduction

This device implements security based on the mode selected from the flash module. The following sections provide an overview of flash security and details the effects of security on non-flash modules.

10.2 Flash Security

The flash module provides security information to the MCU based on the state held by the FSEC[SEC] bits. The MCU, in turn, confirms the security request and limits access to flash resources. During reset, the flash module initializes the FSEC register using data read from the security byte of the flash configuration field.

NOTE

The security features apply only to external accesses via debug. CPU accesses to the flash are not affected by the status of FSEC.

In the unsecured state all flash commands are available to the programming interfaces (JTAG), as well as user code execution of Flash Controller commands. When the flash is secured (FSEC[SEC] = 00, 01, or 11), programmer interfaces are only allowed to launch mass erase operations and have no access to memory locations.

Further information regarding the flash security options and enabling/disabling flash security is available in the Flash Memory Module.

10.3 Security Interactions with other Modules

The flash security settings are used by the SoC to determine what resources are available. The following sections describe the interactions between modules and the flash security settings or the impact that the flash security has on non-flash modules.

10.3.1 Security interactions with FlexBus and SDRAM controller

When flash security is enabled, SIM_SOPT2[FBSL] enables/disables off-chip accesses through the FlexBus and the SDRAM interfaces. The FBSL bitfield also has an option to allow opcode and operand accesses or only operand accesses.

10.3.2 Security Interactions with Debug

When flash security is active the JTAG port cannot access the memory resources of the MCU. Boundary scan chain operations work, but debugging capabilities are disabled so that the debug port cannot read flash contents.

Although most debug functions are disabled, the debugger can write to the Flash Mass Erase in Progress bit in the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command. A mass erase via the debugger is allowed even when some memory locations are protected.

When mass erase is disabled, mass erase via the debugger is blocked.

Chapter 11
Debug

11.1 Introduction

This device's debug is based on the ARM coresight architecture and is configured in each device to provide the maximum flexibility as allowed by the restrictions of the pinout and other available resources.

Four debug interfaces are supported:

- IEEE 1149.1 JTAG
- IEEE 1149.7 JTAG (cJTAG)
- Serial Wire Debug (SWD)
- ARM Real-Time Trace Interface(1-pin asynchronous mode only)

The basic Cortex-M4 debug architecture is very flexible. The following diagram shows the topology of the core debug architecture and its components.

11.2 Cortex-M4 Debug Topology with CAU

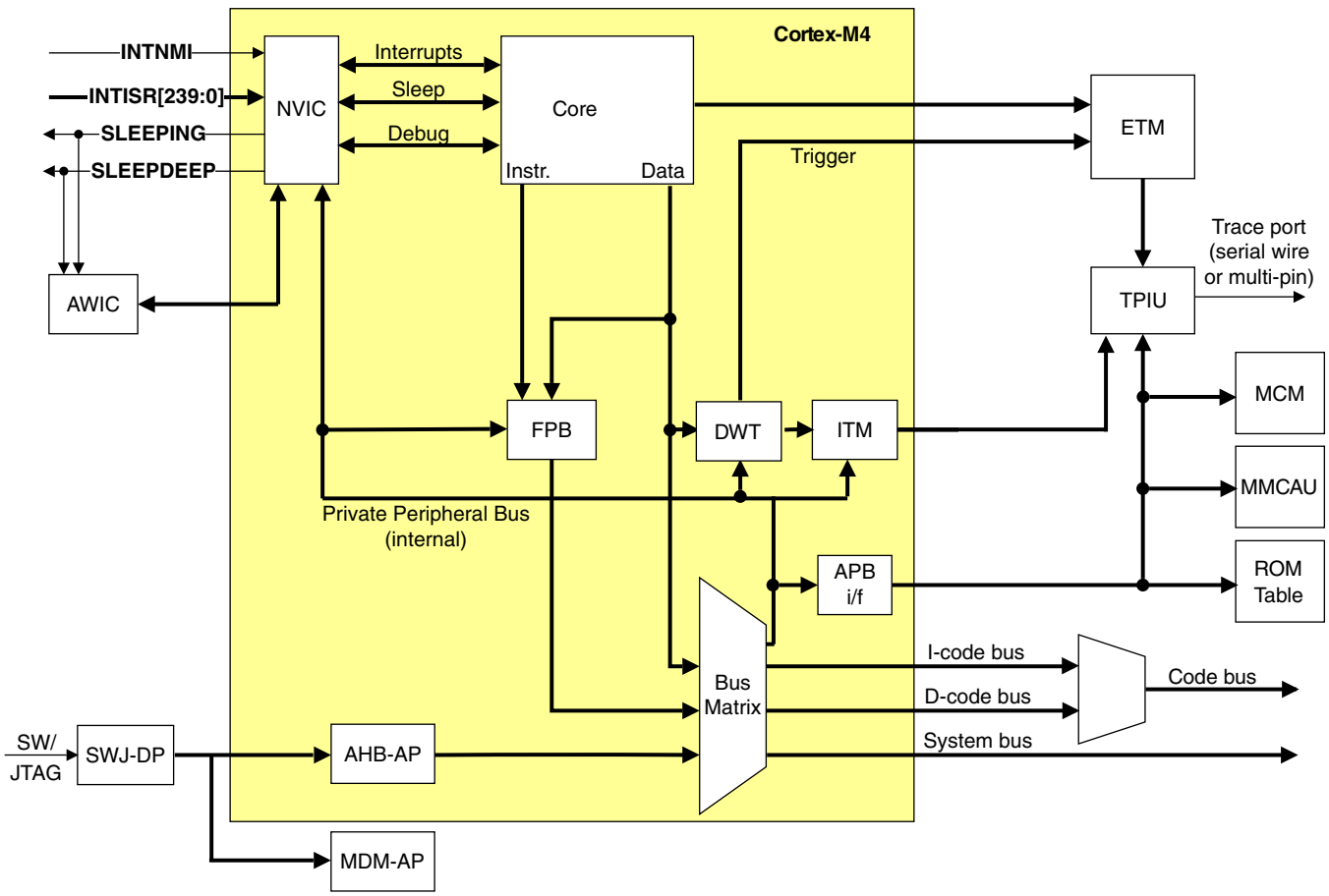


Figure 11-1. Cortex-M4 Debug Topology with CAU

11.3 Debug Components

The following table presents a brief description of each one of the debug components.

Table 11-1. Debug Components Description

Module	Description
SWJ-DP+ cJTAG	Modified Debug Port with support for SWD, JTAG, cJTAG
AHB-AP	AHB Master Interface from JTAG to debug module and SoC system memory maps
MDM-AP	Provides centralized control and status registers for an external debugger to control the device.
ROM Table	Identifies which debug IP is available.
Core Debug	Singlestep, Register Access, Run, Core Status

Table continues on the next page...

Table 11-1. Debug Components Description (continued)

Module	Description
ETM (Embedded Trace Macrocell)	ETMv3.5 Architecture
ITM	S/W Instrumentation Messaging + Simple Data Trace Messaging + Watchpoint Messaging
DWT (Data and Address Watchpoints)	4 data and address watchpoints
FPB (Flash Patch and Breakpoints)	The FPB implements hardware breakpoints and patches code and data from code space to system space. The FPB unit contains two literal comparators for matching against literal loads from Code space, and remapping to a corresponding area in System space. The FPB also contains six instruction comparators for matching against instruction fetches from Code space, and remapping to a corresponding area in System space. Alternatively, the six instruction comparators can individually configure the comparators to return a Breakpoint Instruction (BKPT) to the processor core on a match, so providing hardware breakpoint capability.
TPIU (Trace Port Inteface Unit)	Synchronous Mode (5-pin) = TRACE_D[3:0] + TRACE_CLKOUT Synchronous Mode (3-pin) = TRACE_D[1:0] + TRACE_CLKOUT Asynchronous Mode (1-pin) = TRACE_SWO (available on JTAG_TDO)

11.3.1 References

For more information on ARM debug components, see these documents:

- ARMv7-M Architecture Reference Manual
- ARM Debug Interface v5.1
- ARM CoreSight Architecture Specification
- ARM ETM Architecture Specification v3.5

11.4 The Debug Port

The configuration of the cJTAG module, JTAG controller, and debug port is illustrated in the following figure:

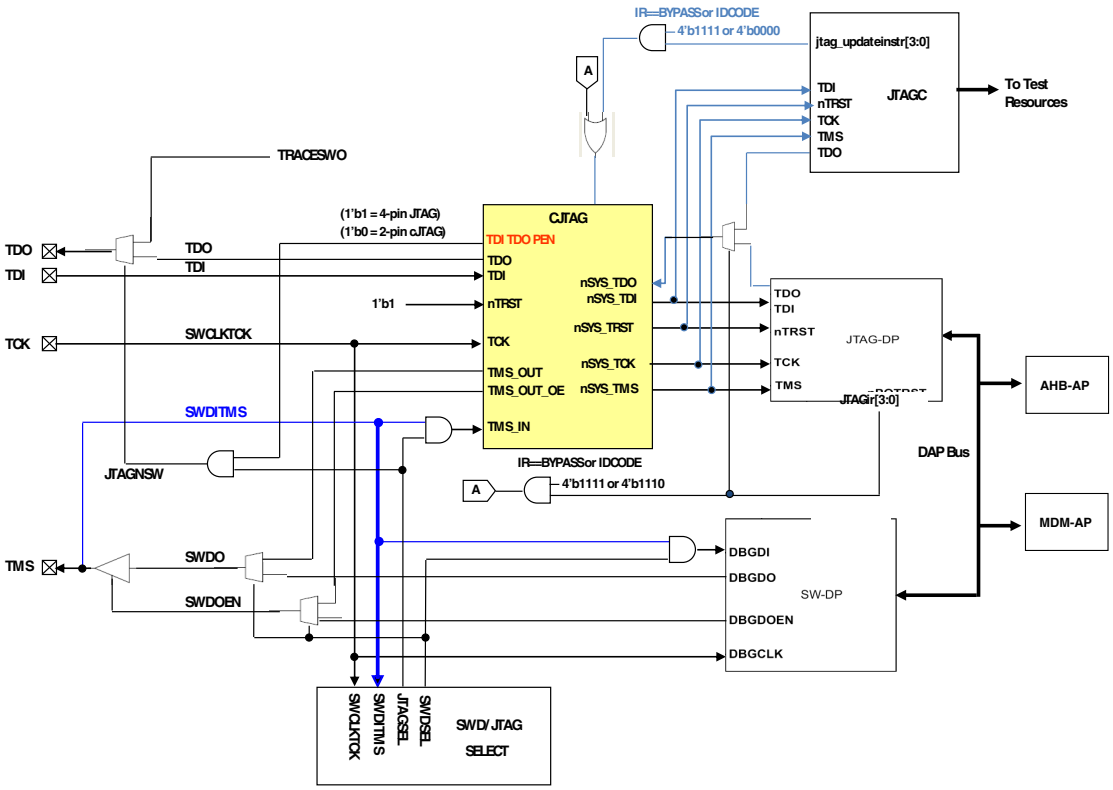


Figure 11-2. Modified Debug Port

The debug port comes out of reset in standard JTAG mode and is switched into either cJTAG or SWD mode by the following sequences. Once the mode has been changed, unused debug pins can be reassigned to any of their alternative muxed functions.

11.4.1 JTAG-to-SWD change sequence

1. Send more than 50 TCK cycles with TMS (SWDIO) =1
2. Send the 16-bit sequence on TMS (SWDIO) = 0111_1001_1110_0111 (MSB transmitted first)
3. Send more than 50 TCK cycles with TMS (SWDIO) =1

NOTE

See the ARM documentation for the CoreSight DAP Lite for restrictions.

11.4.2 JTAG-to-cJTAG change sequence

1. Reset the debug port

2. Set the control level to 2 via zero-bit scans
3. Execute the Store Format (STFMT) command (00011) to set the scan format register to 1149.7 scan format

11.5 Debug Port Pin Descriptions

The debug port pins default after POR to their JTAG functionality with the exception of JTAG_TRST_b and can be later reassigned to their alternate functionalities. In cJTAG and SWD modes JTAG_TDI and JTAG_TRST_b can be configured to alternate GPIO functions.

Table 11-2. Debug port pins

Pin Name	JTAG Debug Port		cJTAG Debug Port		SWD Debug Port		Internal Pull-up\Down
	Type	Description	Type	Description	Type	Description	
JTAG_TMS/ SWD_DIO	I/O	JTAG Test Mode Selection	I/O	cJTAG Data	I/O	Serial Wire Data	Pull-up
JTAG_TCLK/ SWD_CLK	I	JTAG Test Clock	I	cJTAG Clock	I	Serial Wire Clock	Pull-down
JTAG_TDI	I	JTAG Test Data Input	-	-	-	-	Pull-up
JTAG_TDO/ TRACE_SWO	O	JTAG Test Data Output	O	Trace output over a single pin	O	Trace output over a single pin	N/C
JTAG_TRST_b	I	JTAG Reset	I	cJTAG Reset	-	-	Pull-up

11.6 System TAP connection

The system JTAG controller is connected in parallel to the ARM TAP controller. The system JTAG controller IR codes overlay the ARM JTAG controller IR codes without conflict. Refer to the IR codes table for a list of the available IR codes. The output of the TAPs (TDO) are muxed based on the IR code which is selected. This design is fully JTAG compliant and appears to the JTAG chain as a single TAP. At power on reset, ARM's IDCODE (IR=4'b1110) is selected.

11.6.1 IR Codes

Table 11-3. JTAG Instructions

Instruction	Code[3:0]	Instruction Summary
IDCODE	0000	Selects device identification register for shift
SAMPLE/PRELOAD	0010	Selects boundary scan register for shifting, sampling, and preloading without disturbing functional operation
SAMPLE	0011	Selects boundary scan register for shifting and sampling without disturbing functional operation
EXTEST	0100	Selects boundary scan register while applying preloaded values to output pins and asserting functional reset
HIGHZ	1001	Selects bypass register while three-stating all output pins and asserting functional reset
CLAMP	1100	Selects bypass register while applying preloaded values to output pins and asserting functional reset
ARM_IDCODE	1110	ARM JTAG-DP Instruction
BYPASS	1111	Selects bypass register for data operations
Factory debug reserved	0101, 0110, 0111, 1101	Intended for factory debug only
ARM JTAG-DP Reserved	1000, 1010, 1011, 1110	These instructions will go the ARM JTAG-DP controller. Please look at ARM JTAG-DP documentation for more information on these instructions.
Reserved [1]	All other opcodes	Decoded to select bypass register

1. The manufacturer reserves the right to change the decoding of reserved instruction codes in the future

11.7 JTAG status and control registers

Through the ARM Debug Access Port (DAP), the debugger has access to the status and control elements, implemented as registers on the DAP bus as shown in the following figure. These registers provide additional control and status for low power mode recovery and typical run-control scenarios. The status register bits also provide a means for the debugger to get updated status of the core without having to initiate a bus transaction across the crossbar switch, thus remaining less intrusive during a debug session.

It is important to note that these DAP control and status registers are not memory mapped within the system memory map and are only accessible via the Debug Access Port (DAP) using JTAG, cJTAG, or SWD. The MDM-AP is accessible as Debug Access Port 1 with the available registers shown in the table below.

Table 11-4. MDM-AP Register Summary

Address	Register	Description
0x0100_0000	Status	See MDM-AP Status Register

Table continues on the next page...

Table 11-4. MDM-AP Register Summary (continued)

0x0100_0004	Control	See MDM-AP Control Register
0x0100_00FC	ID	Read-only identification register that always reads as 0x001C_0000

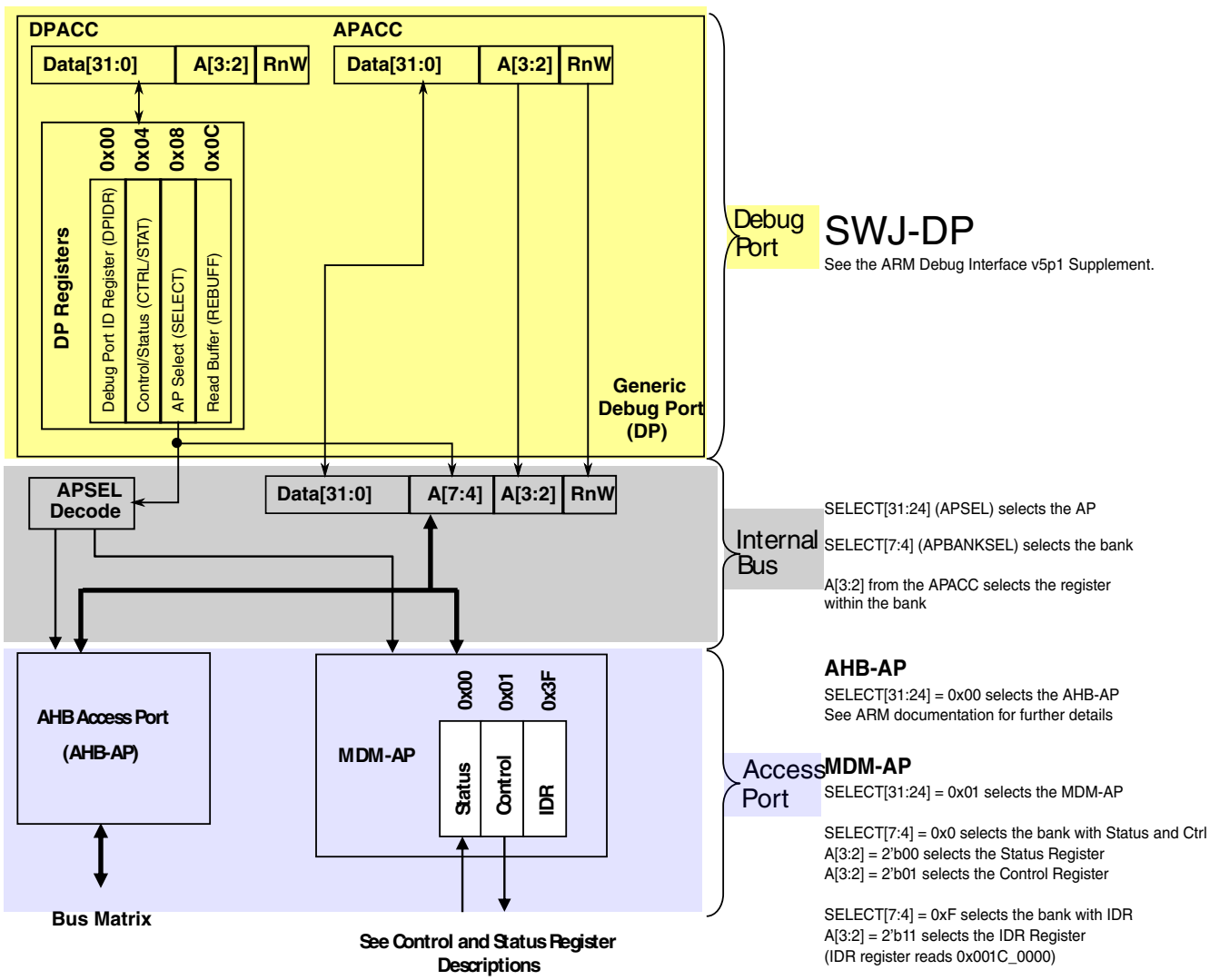


Figure 11-3. MDM AP Addressing

11.7.1 MDM-AP Control Register

Table 11-5. MDM-AP Control register assignments

Bit	Name	Secure[1]	Description
0	Flash Mass Erase in Progress	Y	Set to cause mass erase. Cleared by hardware after mass erase operation completes.

Table continues on the next page...

Table 11-5. MDM-AP Control register assignments (continued)

Bit	Name	Secure[1]	Description
			When mass erase is disabled (via MEEN and SEC settings), the erase request does not occur and the Flash Mass Erase in Progress bit continues to assert until the next system reset.
1	Debug Disable	N	Set to disable debug. Clear to allow debug operation. When set it overrides the C_DEBUGEN bit within the DHCSR and force disables Debug logic.
2	Debug Request	N	Set to force the Core to halt. If the Core is in a stop or wait mode, this bit can be used to wakeup the core and transition to a halted state.
3	System Reset Request	N	Set to force a system reset. The system remains held in reset until this bit is cleared.
4	Core Hold Reset	N	Configuration bit to control Core operation at the end of system reset sequencing. 0 Normal operation - release the Core from reset along with the rest of the system at the end of system reset sequencing. 1 Suspend operation - hold the Core in reset at the end of reset sequencing. Once the system enters this suspended state, clearing this control bit immediately releases the Core from reset and CPU operation begins.
5	VLLSx Debug Request (VLLDBGREQ)	N	Set to configure the system to be held in reset after the next recovery from a VLLSx mode. This bit holds the system in reset when VLLSx modes are exited to allow the debugger time to re-initialize debug IP before the debug session continues. The Mode Controller captures this bit logic on entry to VLLSx modes. Upon exit from VLLSx modes, the Mode Controller will hold the in reset until VLLDBGACK is asserted. The VLLDBGREQ bit clears automatically due to the POR reset generated as part of the VLLSx recovery.
6	VLLSx Debug Acknowledge (VLLDBGACK)	N	Set to release a system being held in reset following a VLLSx recovery This bit is used by the debugger to release the system reset when it is being held on VLLSx mode exit. The debugger re-initializes all debug IP and then assert this control bit to allow the Mode Controller to release the from reset and allow CPU operation to begin. The VLLDBGACK bit is cleared by the debugger or can be left set because it clears automatically due to the POR reset generated as part of the next VLLSx recovery.
7	LLS, VLLSx Status Acknowledge	N	Set this bit to acknowledge the DAP LLS and VLLS Status bits have been read. This acknowledge automatically clears the status bits. This bit is used by the debugger to clear the sticky LLS and VLLSx mode entry status bits. This bit is asserted and cleared by the debugger.
8	Timestamp Disable	N	Set this bit to disable the 48-bit global trace timestamp counter during debug halt mode when the core is halted. 0 The timestamp counter continues to count assuming trace is enabled and the ETM is enabled. (default)

Table continues on the next page...

Table 11-5. MDM-AP Control register assignments (continued)

Bit	Name	Secure[1]	Description
			1 The timestamp counter freezes when the core has halted (debug halt mode).
9 – 31	Reserved for future use	N	

1. Command available in secure mode

11.7.2 MDM-AP Status Register

Table 11-6. MDM-AP Status register assignments

Bit	Name	Description
0	Flash Mass Erase Acknowledge	The Flash Mass Erase Acknowledge bit is cleared after any system reset. The bit is also cleared at launch of a mass erase command due to write of Flash Mass Erase in Progress bit in MDM AP Control Register. The Flash Mass Erase Acknowledge is set after Flash control logic has started the mass erase operation. When mass erase is disabled (via MEEN and SEC settings), an erase request due to seting of Flash Mass Erase in Progress bit is not acknowledged.
1	Flash Ready	Indicate Flash has been initialized and debugger can be configured even if system is continuing to be held in reset via the debugger.
2	System Security	Indicates the security state. When secure, the debugger does not have access to the system bus or any memory mapped peripherals. This bit indicates when the part is locked and no system bus access is possible.
3	System Reset	Indicates the system reset state. 0 System is in reset 1 System is not in reset
4	Reserved	
5	Mass Erase Enable	Indicates if the MCU can be mass erased or not 0 Mass erase is disabled 1 Mass erase is enabled
6	Backdoor Access Key Enable	Indicates if the MCU has the backdoor access key enabled. 0 Disabled 1 Enabled
7	LP Enabled	Decode of LPLLSM control bits to indicate that VLPS, LLS, or VLLSx are the selected power mode the next time the ARM Core enters Deep Sleep. 0 Low Power Stop Mode is not enabled 1 Low Power Stop Mode is enabled

Table continues on the next page...

Table 11-6. MDM-AP Status register assignments (continued)

Bit	Name	Description
		Usage intended for debug operation in which Run to VLPS is attempted. Per debug definition, the system actually enters the Stop state. A debugger should interpret deep sleep indication (with SLEEPDEEP and SLEEPING asserted), in conjuntion with this bit asserted as the debugger-VLPS status indication.
8	Very Low Power Mode	Indicates current power mode is VLPx. This bit is not 'sticky' and should always represent whether VLPx is enabled or not. This bit is used to throttle JTAG TCK frequency up/down.
9	LLS Mode Exit	This bit indicates an exit from LLS mode has occurred. The debugger will lose communication while the system is in LLS (including access to this register). Once communication is reestablished, this bit indicates that the system had been in LLS. Since the debug modules held their state during LLS, they do not need to be reconfigured. This bit is set during the LLS recovery sequence. The LLS Mode Exit bit is held until the debugger has had a chance to recognize that LLS was exited and is cleared by a write of 1 to the LLS, VLLSx Status Acknowledge bit in MDM AP Control register.
10	VLLSx Modes Exit	This bit indicates an exit from VLLSx mode has occurred. The debugger will lose communication while the system is in VLLSx (including access to this register). Once communication is reestablished, this bit indicates that the system had been in VLLSx. Since the debug modules lose their state during VLLSx modes, they need to be reconfigured. This bit is set during the VLLSx recovery sequence. The VLLSx Mode Exit bit is held until the debugger has had a chance to recognize that a VLLS mode was exited and is cleared by a write of 1 to the LLS, VLLSx Status Acknowledge bit in MDM AP Control register.
11 – 15	Reserved for future use	Always read 0.
16	Core Halted	Indicates the Core has entered debug halt mode
17	Core SLEEPDEEP	Indicates the Core has entered a low power mode
18	Core SLEEPING	SLEEPING==1 and SLEEPDEEP==0 indicates wait or VLPW mode. SLEEPING==0 and SLEEPDEEP==1 indicates stop or VLPS mode.
19 – 31	Reserved for future use	Always read 0.

11.8 Debug Resets

The debug system receives the following sources of reset:

- JTAG_TRST_b from an external signal. This signal is optional and may not be available in all packages.
- Debug reset (CDBGRSTREQ bit within the SWJ-DP CTRL/STAT register) in the TCLK domain that allows the debugger to reset the debug logic.
- TRST asserted via the cJTAG escape command.
- System POR reset

Conversely the debug system is capable of generating system reset using the following mechanism:

- A system reset in the DAP control register which allows the debugger to hold the system in reset.
- SYSRESETREQ bit in the NVIC application interrupt and reset control register
- A system reset in the DAP control register which allows the debugger to hold the Core in reset.

11.9 AHB-AP

AHB-AP provides the debugger access to all memory and registers in the system, including processor registers through the NVIC. System access is independent of the processor status. AHB-AP does not do back-to-back transactions on the bus, so all transactions are non-sequential. AHB-AP can perform unaligned and bit-band transactions. AHB-AP transactions bypass the FPB, so the FPB cannot remap AHB-AP transactions. SWJ/SW-DP-initiated transaction aborts drive an AHB-AP-supported sideband signal called HABORT. This signal is driven into the Bus Matrix, which resets the Bus Matrix state, so that AHB-AP can access the Private Peripheral Bus for last ditch debugging such as read/stop/reset the core. AHB-AP transactions are little endian.

The MPU includes default settings and protections for the Region Descriptor 0 (RGD0) such that the Debugger always has access to the entire address space and those rights cannot be changed by the core or any other bus master.

For a short period at the start of a system reset event the system security status is being determined and debugger access to all AHB-AP transactions is blocked. The MDM-AP Status register is accessible and can be monitored to determine when this initial period is completed. After this initial period, if system reset is held via assertion of the RESET pin, the debugger has access via the bus matrix to the private peripheral bus to configure the debug IP even while system reset is asserted. While in system reset, access to other memory and register resources, accessed over the Crossbar Switch, is blocked.

11.10 ITM

The ITM is an application-driven trace source that supports printf style debugging to trace Operating System (OS) and application events, and emits diagnostic system information. The ITM emits trace information as packets. There are four sources that can

generate packets. If multiple sources generate packets at the same time, the ITM arbitrates the order in which packets are output. The four sources in decreasing order of priority are:

1. Software trace -- Software can write directly to ITM stimulus registers. This emits packets.
2. Hardware trace -- The DWT generates these packets, and the ITM emits them.
3. Time stamping -- Timestamps are emitted relative to packets. The ITM contains a 21-bit counter to generate the timestamp. The Cortex-M4 clock or the bitclock rate of the Serial Wire Viewer (SWV) output clocks the counter.
4. Global system timestamping. Timestamps can optionally be generated using a system-wide 48-bit count value. The same count value can be used to insert timestamps in the ETM trace stream, allowing coarse-grain correlation.

11.11 Core Trace Connectivity with ETM

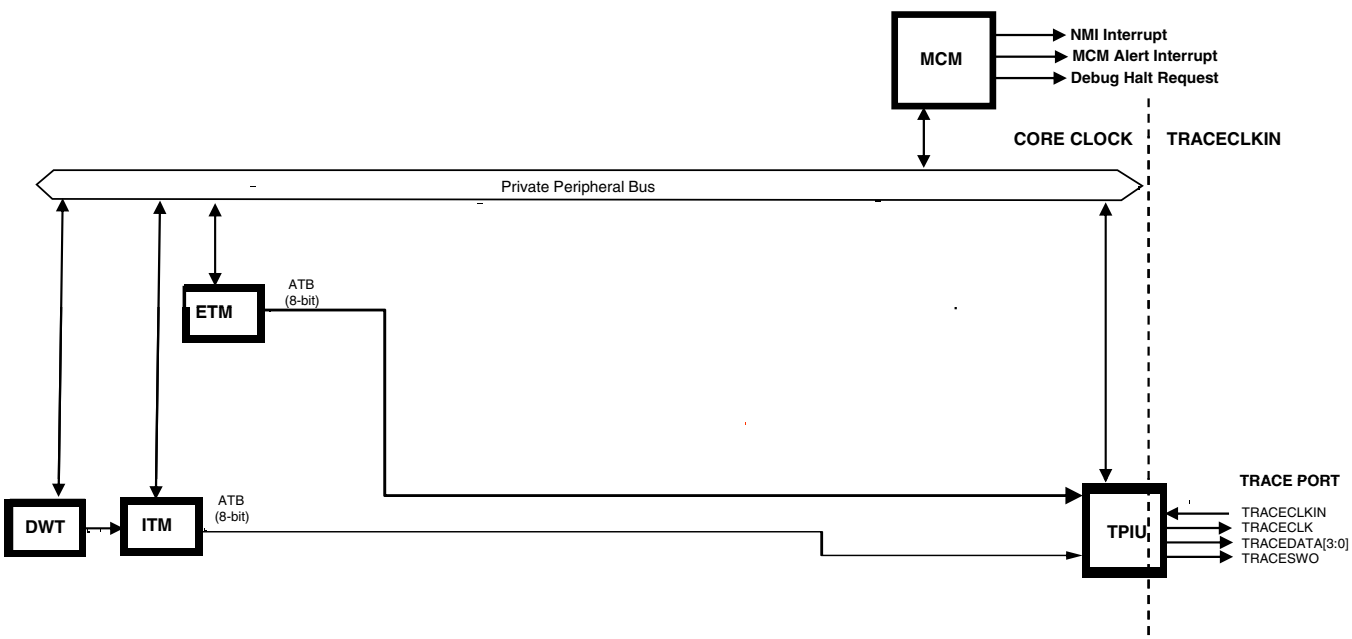


Figure 11-4. Core Trace Connectivity with ETM only

The figure above assumes the device contains an ETM.

The following combinations paths are supported:

1. ETM -> TPIU(4 pin or 2 pin parallel)
2. ITM->TPIU(1 pin SWO, 2 pin or 4 pin parallel)
3. ETM & ITM -> TPIU

11.12 Embedded Trace Macrocell v3.5 (ETM)

The Cortex-M4 Embedded Trace Macrocell (ETM-M4) is a debug component that enables a debugger to reconstruct program execution. The CoreSight ETM-M4 supports only instruction trace. You can use it either with the Cortex-M4 Trace Port Interface Unit (M4-TPIU).

The main features of an ETM are:

- Tracing of 16-bit and 32-bit Thumb instructions
- Four EmbeddedICE watchpoint inputs
- Trace Start/Stop block with EmbeddedICE inputs
- One reduced function counter
- Two external inputs
- 24-byte FIFO queue
- Global timestamping

11.13 TPIU

The TPIU acts as a bridge between the on-chip trace data from the Embedded Trace Macrocell (ETM) and the Instrumentation Trace Macrocell (ITM), with separate IDs, to a data stream, encapsulating IDs where required, that is then captured by a Trace Port Analyzer (TPA). The TPIU is specially designed for low-cost debug.

11.14 DWT

The DWT is a unit that performs the following debug functionality:

- It contains four comparators that you can configure as a hardware watchpoint, an ETM trigger, a PC sampler event trigger, or a data address sampler event trigger. The first comparator, DWT_COMP0, can also compare against the clock cycle counter, CYCCNT. The second comparator, DWT_COMP1, can also be used as a data comparator.
- The DWT contains counters for:
  - Clock cycles (CYCCNT)
  - Folded instructions
  - Load store unit (LSU) operations
  - Sleep cycles

- CPI (all instruction cycles except for the first cycle)
- Interrupt overhead

NOTE

An event is emitted each time a counter overflows.

- The DWT can be configured to emit PC samples at defined intervals, and to emit interrupt event information.

11.15 Debug in Low Power Modes

In low power modes in which the debug modules are kept static or powered off, the debugger cannot gather any debug data for the duration of the low power mode. In the case that the debugger is held static, the debug port returns to full functionality as soon as the low power mode exits and the system returns to a state with active debug. In the case that the debugger logic is powered off, the debugger is reset on recovery and must be reconfigured once the low power mode is exited.

Power mode entry logic monitors Debug Power Up and System Power Up signals from the debug port as indications that a debugger is active. These signals can be changed in RUN, VLPR, WAIT and VLPW. If the debug signal is active and the system attempts to enter stop or VLPS, FCLK continues to run to support core register access. In these modes in which FCLK is left active the debug modules have access to core registers but not to system memory resources accessed via the crossbar.

With debug enabled, transitions from Run directly to VLPS are not allowed and result in the system entering Stop mode instead. Status bits within the MDM-AP Status register can be evaluated to determine this pseudo-VLPS state. Note with the debug enabled, transitions from Run--> VLPR --> VLPS are still possible but also result in the system entering Stop mode instead.

In VLLS mode all debug modules are powered off and reset at wakeup. In LLS mode, the debug modules retain their state but no debug activity is possible.

NOTE

When using cJTAG and entering LLS mode, the cJTAG controller must be reset on exit from LLS mode.

Going into a VLLSx mode causes all the debug controls and settings to be reset. To give time to the debugger to sync up with the HW, the MDM-AP Control register can be configured hold the system in reset on recovery so that the debugger can regain control and reconfigure debug logic prior to the system exiting reset and resuming operation.

11.15.1 Debug Module State in Low Power Modes

The following table shows the state of the debug modules in low power modes. These terms are used:

- FF = Full functionality. In VLPR and VLPW the system frequency is limited, but if a module does not have a limitation in its functionality, it is still listed as FF.
- static = Module register states and associated memories are retained.
- OFF = Modules are powered off; module is in reset state upon wakeup.

Table 11-7. Debug Module State in Low Power Modes

Module	STOP	VLPR	VLPW	VLPS	LLS	VLLSx
Debug Port	FF	FF	FF	OFF	static	OFF
AHB-AP	FF	FF	FF	OFF	static	OFF
ITM	FF	FF	FF	OFF	static	OFF
ETM	FF	FF	FF	OFF	static	OFF
TPIU	FF	FF	FF	OFF	static	OFF
DWT	FF	FF	FF	OFF	static	OFF

11.16 Debug & Security

When security is enabled (FSEC[SEC] != 10), the debug port capabilities are limited in order to prevent exploitation of secure data. In the secure state the debugger still has access to the MDM-AP Status Register and can determine the current security state of the device. In the case of a secure device, the debugger also has the capability of performing a mass erase operation via writes to the MDM-AP Control Register. In the case of a secure device that has mass erase disabled (FSEC[MEEN] = 10), attempts to mass erase via the debug interface are blocked.

Chapter 12
Signal Multiplexing and Signal Descriptions

12.1 Signal Multiplexing Introduction

To optimize functionality in small packages, pins have several functions available via signal multiplexing. This chapter illustrates which of this device's signals are multiplexed on which external pin.

The Port Control block controls which signal is present on the external pin. Reference that chapter to find which register controls the operation of a specific pin.

12.2 Signal Multiplexing Integration

This section summarizes how the module is integrated into the device. For a comprehensive description of the module itself, see the module's dedicated chapter.

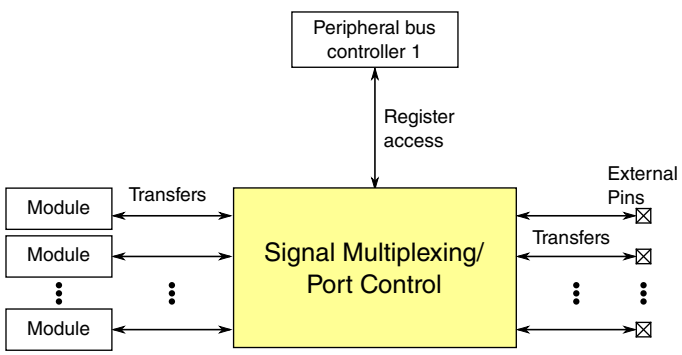


Figure 12-1. Signal multiplexing integration

Table 12-1. Reference links to related information

Topic	Related module	Reference
Full description	Port control	Port control
System memory map		System memory map

Table continues on the next page...

Table 12-1. Reference links to related information (continued)

Topic	Related module	Reference
Clocking		Clock Distribution
Register access	Peripheral bus controller	Peripheral bridge

12.2.1 Port control and interrupt module features

- 32-pin ports

NOTE

Not all pins are available on the device. See the following section for details.

- Each 32-pin port is assigned one interrupt.

Table 12-2. Ports summary

Feature	Port A	Port B	Port C	Port D	Port E
Pull select control	Yes	Yes	Yes	Yes	Yes
Pull select at reset	PTA1/PTA2/PTA3/ PTA4/PTA5=Pull up, Others=Pull down	Pull down	Pull down	Pull down	Pull down
Pull enable control	Yes	Yes	Yes	Yes	Yes
Pull enable at reset	PTA0/PTA1/PTA2/ PTA3/ PTA4=Enabled; Others=Disabled	Disabled	Disabled	Disabled	Disabled
Slew rate enable control	Yes	Yes	Yes	Yes	Yes
Slew rate enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Passive filter enable control	PTA4=Yes; Others=No	No	No	No	No
Passive filter enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Open drain enable control	Yes	Yes	Yes	Yes	Yes
Open drain enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Drive strength enable control	No	PTB0/PTB1 only	PTC3/PTC4 only	PTD4/PTD5/PTD6/ PTD7 only	Yes
Drive strength enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled

Table continues on the next page...

Table 12-2. Ports summary (continued)

Feature	Port A	Port B	Port C	Port D	Port E
Pin mux control	Yes	Yes	Yes	Yes	Yes
Pin mux at reset	PTA0/PTA1/PTA2/ PTA3/PTA4=ALT7; Others=ALT0	ALT0	ALT0	ALT0	ALT0
Lock bit	Yes	Yes	Yes	Yes	Yes
Interrupt and DMA request	Yes	Yes	Yes	Yes	Yes
Digital glitch filter	No	No	No	Yes	No

NOTE

Port E has separate power domain to support QSPI flash

12.2.2 Clock gating

The clock to the port control module can be gated on and off using the SCGC5[PORTx] bits in the SIM module. These bits are cleared after any reset, which disables the clock to the corresponding module to conserve power. Prior to initializing the corresponding module, set SCGC5[PORTx] in the SIM module to enable the clock. Before turning off the clock, make sure to disable the module. For more details, refer to the clock distribution chapter.

12.2.3 Signal multiplexing constraints

1. A given peripheral function must be assigned to a maximum of one package pin. Do not program the same function to more than one pin.
2. To ensure the best signal timing for a given peripheral's interface, choose the pins in closest proximity to each other.

12.3 Pinout

12.3.1 K82 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

The 144-pin LQFP and 121-WLCSP packages for this product are not yet available, however they are included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
x	—	H6	K9	NC	NC	NC								
—	—	—	G8	ADC0_SE16	ADC0_SE16	ADC0_SE16								
—	—	A11	—	NC	NC	NC								
—	—	J6	—	NC	NC	NC								
—	—	J4	—	NC	NC	NC								
1	1	B1	C10	PTE0	DISABLED		PTE0	SPI1_PCS1	LPUART1_TX	SDHC0_D1	QSPI0A_DATA3	I2C1_SDA	RTC_CLKOUT	
2	2	C2	D9	PTE1/LLWU_P0	DISABLED		PTE1/LLWU_P0	SPI1_SCK	LPUART1_RX	SDHC0_D0	QSPI0A_SCLK	I2C1_SCL	SPI1_SIN	
3	3	C1	D10	PTE2/LLWU_P1	DISABLED		PTE2/LLWU_P1	SPI1_SOUT	LPUART1_CTS_b	SDHC0_DCLK	QSPI0A_DATA0		SPI1_SCK	
4	4	D2	B11	PTE3	DISABLED		PTE3	SPI1_PCS2	LPUART1_RTS_b	SDHC0_CMD	QSPI0A_DATA2		SPI1_SOUT	
5	5	F7	F6	VSS	VSS	VSS								
6	6	E5	F7	VDDIO_E	VDDIO_E	VDDIO_E								
7	7	D1	C11	PTE4/LLWU_P2	DISABLED		PTE4/LLWU_P2	SPI1_SIN	LPUART3_TX	SDHC0_D3	QSPI0A_DATA1			
8	8	E2	E8	PTE5	DISABLED		PTE5	SPI1_PCS0	LPUART3_RX	SDHC0_D2	QSPI0A_SS0_B	FTM3_CH0	USB0_SOF_OUT	
9	9	E1	E9	PTE6/LLWU_P16	DISABLED		PTE6/LLWU_P16	SPI1_PCS3	LPUART3_CTS_b	I2S0_MCLK	QSPI0B_DATA3	FTM3_CH1	SDHC0_D4	
10	10	F3	E10	PTE7	DISABLED		PTE7	SPI2_SCK	LPUART3_RTS_b	I2S0_RXD0	QSPI0B_SCLK	FTM3_CH2	QSPI0A_SS1_B	
11	11	F2	D11	PTE8	DISABLED		PTE8	I2S0_RXD1	SPI2_SOUT	I2S0_RX_FS	QSPI0B_DATA0	FTM3_CH3	SDHC0_D5	
12	12	F1	E11	PTE9/LLWU_P17	DISABLED		PTE9/LLWU_P17	I2S0_TXD1	SPI2_PCS1	I2S0_RX_BCLK	QSPI0B_DATA2	FTM3_CH4	SDHC0_D6	
13	13	G2	F8	PTE10/LLWU_P18	DISABLED		PTE10/LLWU_P18	I2C3_SDA	SPI2_SIN	I2S0_TXD0	QSPI0B_DATA1	FTM3_CH5	SDHC0_D7	
14	14	G1	F9	PTE11	DISABLED		PTE11	I2C3_SCL	SPI2_PCS0	I2S0_TX_FS	QSPI0B_SS0_B	FTM3_CH6	QSPI0A_DQS	
15	—	—	—	PTE12	DISABLED		PTE12		LPUART2_TX	I2S0_TX_BCLK	QSPI0B_DQS	FTM3_CH7	FXIO0_D2	QSPI0A_DATA3
16	—	—	—	PTE13	DISABLED		PTE13		LPUART2_RX		QSPI0B_SS1_B	SDHC0_CLKIN	FXIO0_D3	QSPI0A_SCLK
17	15	—	F10	VDDIO_E	VDDIO_E	VDDIO_E								
18	16	—	F11	VSS	VSS	VSS								

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
19	—	—	—	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	LPUART2_TX	FTM_CLKIN0		FTM0_FLT3	FXIO0_D4	QSPI0A_DATA0
20	—	—	—	PTE17/LLWU_P19	ADC0_SE5a	ADC0_SE5a	PTE17/LLWU_P19	SPI0_SCK	LPUART2_RX	FTM_CLKIN1		LPTMR0_ALT3/LPTMR1_ALT3	FXIO0_D5	QSPI0A_DATA2
21	—	—	—	PTE18/LLWU_P20	ADC0_SE6a	ADC0_SE6a	PTE18/LLWU_P20	SPI0_SOUT	LPUART2_CTS_b	I2C0_SDA			FXIO0_D6	QSPI0A_DATA1
22	—	—	—	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	LPUART2_RTS_b	I2C0_SCL			FXIO0_D7	QSPI0A_SS0_B
23	16	H3	F11	VSS	VSS	VSS								
24	17	H2	G11	USB0_DP	USB0_DP	USB0_DP								
25	18	H1	H11	USB0_DM	USB0_DM	USB0_DM								
26	19	J1	G10	VOUT33	VOUT33	VOUT33								
27	20	J2	H10	VREGIN	VREGIN	VREGIN								
28	21	—	G9	NC	NC	NC								
29	—	K2	J10	ADC0_DP0	ADC0_DP0	ADC0_DP0								
30	—	K1	K10	ADC0_DM0	ADC0_DM0	ADC0_DM0								
31	—	J3	J11	ADC0_DP3	ADC0_DP3	ADC0_DP3								
32	—	K3	K11	ADC0_DM3	ADC0_DM3	ADC0_DM3								
33	22	F5	H8	VDDA	VDDA	VDDA								
34	23	G5	H9	VREFH	VREFH	VREFH								
35	24	G6	J9	VREFL	VREFL	VREFL								
36	25	F6	J8	VSSA	VSSA	VSSA								
37	26	L2	—	ADC0_DP1	ADC0_DP1	ADC0_DP1								
38	27	L1	—	ADC0_DM1	ADC0_DM1	ADC0_DM1								
39	28	L3	L11	VREF_OUT/CMP1_IN5/CMP0_IN5/ADC0_SE22	VREF_OUT/CMP1_IN5/CMP0_IN5/ADC0_SE22	VREF_OUT/CMP1_IN5/CMP0_IN5/ADC0_SE22								
40	29	K4	L10	DAC0_OUT/CMP1_IN3/ADC0_SE23	DAC0_OUT/CMP1_IN3/ADC0_SE23	DAC0_OUT/CMP1_IN3/ADC0_SE23								
42	30	K5	H7	RTC_WAKEUP_B	RTC_WAKEUP_B	RTC_WAKEUP_B								
43	31	L4	L9	XTAL32	XTAL32	XTAL32								
44	32	L5	L8	EXTAL32	EXTAL32	EXTAL32								
45	33	K6	K8	VBAT	VBAT	VBAT								
46	34	—	G7	VDD	VDD	VDD								
47	35	—	F6	VSS	VSS	VSS								

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
48	—	H5	L7	PTA20	DISABLED		PTA20	I2C0_SCL	LPUART4_TX	FTM_CLKIN1	FXIO0_D8	EWM_OUT_b	TPM_CLKIN1	
49	—	J5	K7	PTA21/ LLWU_P21	DISABLED		PTA21/ LLWU_P21	I2C0_SDA	LPUART4_RX		FXIO0_D9	EWM_IN		
50	36	L7	J7	PTA0	JTAG_TCLK/ SWD_CLK	TSI0_CH1	PTA0	LPUART0_CTS_b	FTM0_CH5		FXIO0_D10	EMVSIM0_CLK	JTAG_TCLK/ SWD_CLK	
51	37	H8	J6	PTA1	JTAG_TDI	TSI0_CH2	PTA1	LPUART0_RX	FTM0_CH6	I2C3_SDA	FXIO0_D11	EMVSIM0_IO	JTAG_TDI	
52	38	J7	K6	PTA2	JTAG_TDO/ TRACE_SWO	TSI0_CH3	PTA2	LPUART0_TX	FTM0_CH7	I2C3_SCL	FXIO0_D12	EMVSIM0_PD	JTAG_TDO/ TRACE_SWO	
53	39	H9	L6	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	LPUART0_RTS_b	FTM0_CH0		FXIO0_D13	EMVSIM0_RST	JTAG_TMS/ SWD_DIO	
54	40	J8	H6	PTA4/ LLWU_P3	NMI_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1		FXIO0_D14	EMVSIM0_VCCEN	NMI_b	
55	41	K7	H5	PTA5	DISABLED		PTA5	USB0_CLKIN	FTM0_CH2		FXIO0_D15	I2S0_TX_BCLK	JTAG_TRST_b	
56	—	L10	G6	VDD	VDD	VDD								
57	—	K10	F5	VSS	VSS	VSS								
58	—	—	—	PTA6	DISABLED		PTA6	I2C2_SCL	FTM0_CH3	EMVSIM1_CLK	CLKOUT		TRACE_CLKOUT	
59	—	—	—	PTA7	ADC0_SE10	ADC0_SE10	PTA7	I2C2_SDA	FTM0_CH4	EMVSIM1_IO			TRACE_D3	
60	—	—	—	PTA8	ADC0_SE11	ADC0_SE11	PTA8		FTM1_CH0	EMVSIM1_PD		FTM1_QD_PHA/ TPM1_CH0	TRACE_D2	
61	—	—	—	PTA9	DISABLED		PTA9		FTM1_CH1	EMVSIM1_RST		FTM1_QD_PHB/ TPM1_CH1	TRACE_D1	
62	—	J9	L5	PTA10/ LLWU_P22	DISABLED		PTA10/ LLWU_P22	I2C2_SDA	FTM2_CH0	EMVSIM1_VCCEN	FXIO0_D16	FTM2_QD_PHA/ TPM2_CH0	TRACE_D0	
63	—	H7	L4	PTA11/ LLWU_P23	DISABLED		PTA11/ LLWU_P23	I2C2_SCL	FTM2_CH1		FXIO0_D17	FTM2_QD_PHB/ TPM2_CH1		
64	42	K8	K5	PTA12	DISABLED		PTA12		FTM1_CH0	TRACE_CLKOUT	FXIO0_D18	I2S0_TXD0	FTM1_QD_PHA/ TPM1_CH0	
65	43	L8	J5	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		FTM1_CH1	TRACE_D3	FXIO0_D19	I2S0_TX_FS	FTM1_QD_PHB/ TPM1_CH1	
66	44	K9	L3	PTA14	DISABLED		PTA14	SPI0_PCS0	LPUART0_TX	TRACE_D2	FXIO0_D20	I2S0_RX_BCLK	I2S0_TXD1	
67	45	L9	K4	PTA15	DISABLED		PTA15	SPI0_SCK	LPUART0_RX	TRACE_D1	FXIO0_D21	I2S0_RXD0		
68	46	J10	J4	PTA16	DISABLED		PTA16	SPI0_SOUT	LPUART0_CTS_b	TRACE_D0	FXIO0_D22	I2S0_RX_FS	I2S0_RXD1	

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
69	47	H10	K3	PTA17	DISABLED		PTA17	SPI0_SIN	LPUART0_RTS_b		FXIO0_D23	I2S0_MCLK		
70	48	E6	L2	VDD	VDD	VDD								
71	49	G7	K2	VSS	VSS	VSS								
72	50	L11	L1	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0			TPM_CLKIN0	
73	51	K11	K1	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1/ LPTMR1_ALT1	TPM_CLKIN1	
74	52	J11	J1	RESET_b	RESET_b	RESET_b								
75	—	—	—	PTA24	DISABLED		PTA24	EMVSIM0_CLK				FB_A29		
76	—	—	—	PTA25	DISABLED		PTA25	EMVSIM0_IO				FB_A28		
77	—	—	—	PTA26	DISABLED		PTA26	EMVSIM0_PD				FB_A27		
78	—	—	—	PTA27	DISABLED		PTA27	EMVSIM0_RST				FB_A26		
79	—	—	—	PTA28	DISABLED		PTA28	EMVSIM0_VCCEN				FB_A25		
80	—	H11	J2	PTA29	DISABLED		PTA29					FB_A24		
81	53	G11	J3	PTB0/ LLWU_P5	ADC0_SE8/ TSI0_CH0	ADC0_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0		SDRAM_CAS_b	FTM1_QD_PHA/ TPM1_CH0	FXIO0_D0	
82	54	G10	H2	PTB1	ADC0_SE9/ TSI0_CH6	ADC0_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1		SDRAM_RAS_b	FTM1_QD_PHB/ TPM1_CH1	FXIO0_D1	
83	55	G9	H1	PTB2	ADC0_SE12/ TSI0_CH7	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	LPUART0_RTS_b		SDRAM_WE	FTM0_FLT3	FXIO0_D2	
84	56	G8	H3	PTB3	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	LPUART0_CTS_b		SDRAM_CS0_b	FTM0_FLT0	FXIO0_D3	
85	—	B11	H4	PTB4	DISABLED		PTB4	EMVSIM1_IO			SDRAM_CS1_b	FTM1_FLT0		
86	—	C11	G1	PTB5	DISABLED		PTB5	EMVSIM1_CLK				FTM2_FLT0		
87	—	F11	G2	PTB6	DISABLED		PTB6	EMVSIM1_VCCEN			FB_AD23/ SDRAM_D23			
88	—	E11	G3	PTB7	DISABLED		PTB7	EMVSIM1_PD			FB_AD22/ SDRAM_D22			
89	—	D11	G4	PTB8	DISABLED		PTB8	EMVSIM1_RST	LPUART3_RTS_b		FB_AD21/ SDRAM_D21			

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
90	57	E10	G5	PTB9	DISABLED		PTB9	SPI1_PCS1	LPUART3_CTS_b		FB_AD20/SDRAM_D20			
91	58	D10	F1	PTB10	DISABLED		PTB10	SPI1_PCS0	LPUART3_RX	I2C2_SCL	FB_AD19/SDRAM_D19	FTM0_FLT1	FXIO0_D4	
92	59	C10	F2	PTB11	DISABLED		PTB11	SPI1_SCK	LPUART3_TX	I2C2_SDA	FB_AD18/SDRAM_D18	FTM0_FLT2	FXIO0_D5	
93	60	L6	F5	VSS	VSS	VSS								
94	61	E7	G6	VDD	VDD	VDD								
95	62	B10	E1	PTB16	TSI0_CH9	TSI0_CH9	PTB16	SPI1_SOUT	LPUART0_RX	FTM_CLKIN0	FB_AD17/SDRAM_D17	EWM_IN	TPM_CLKIN0	
96	63	E9	F3	PTB17	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	LPUART0_TX	FTM_CLKIN1	FB_AD16/SDRAM_D16	EWM_OUT_b	TPM_CLKIN1	
97	64	D9	F4	PTB18	TSI0_CH11	TSI0_CH11	PTB18		FTM2_CH0	I2S0_TX_BCLK	FB_AD15/SDRAM_A23	FTM2_QD_PHA/TPM2_CH0	FXIO0_D6	
98	65	C9	E2	PTB19	TSI0_CH12	TSI0_CH12	PTB19		FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_PHB/TPM2_CH1	FXIO0_D7	
99	66	F10	D1	PTB20	DISABLED		PTB20	SPI2_PCS0			FB_AD31/SDRAM_D31	CMP0_OUT	FXIO0_D8	
100	67	F9	E3	PTB21	DISABLED		PTB21	SPI2_SCK			FB_AD30/SDRAM_D30	CMP1_OUT	FXIO0_D9	
101	68	F8	E4	PTB22	DISABLED		PTB22	SPI2_SOUT			FB_AD29/SDRAM_D29		FXIO0_D10	
102	69	E8	D2	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28/SDRAM_D28		FXIO0_D11	
103	70	B9	C1	PTC0	ADC0_SE14/TSI0_CH13	ADC0_SE14/TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG	USB0_SOF_OUT	FB_AD14/SDRAM_A22	I2S0_TXD1	FXIO0_D12	
104	71	D8	D3	PTC1/LLWU_P6	ADC0_SE15/TSI0_CH14	ADC0_SE15/TSI0_CH14	PTC1/LLWU_P6	SPI0_PCS3	LPUART1_RTS_b	FTM0_CH0	FB_AD13/SDRAM_A21	I2S0_TXD0	FXIO0_D13	
105	72	C8	C2	PTC2	ADC0_SE4b/CMP1_IN0/TSI0_CH15	ADC0_SE4b/CMP1_IN0/TSI0_CH15	PTC2	SPI0_PCS2	LPUART1_CTS_b	FTM0_CH1	FB_AD12/SDRAM_A20	I2S0_TX_FS		
106	73	B8	B1	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	LPUART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK		
107	74	—	E5	VSS	VSS	VSS								
108	75	—	G6	VDD	VDD	VDD								

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
109	76	A8	A1	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	LPUART1_ TX	FTM0_CH3	FB_AD11/ SDRAM_ A19	CMP1_OUT		
110	77	D7	B2	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2/ LPTMR1_ ALT2	I2S0_RXD0	FB_AD10/ SDRAM_ A18	CMP0_OUT	FTM0_CH2	
111	78	C7	C3	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_ EXTRG	I2S0_RX_ BCLK	FB_AD9/ SDRAM_ A17	I2S0_MCLK	FXIO0_D14	
112	79	B7	A2	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB0_ SOF_OUT	I2S0_RX_ FS	FB_AD8/ SDRAM_ A16		FXIO0_D15	
113	80	A7	B3	PTC8	CMP0_IN2	CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK	FB_AD7/ SDRAM_ A15		FXIO0_D16	
114	81	D6	D4	PTC9	CMP0_IN3	CMP0_IN3	PTC9		FTM3_CH5	I2S0_RX_ BCLK	FB_AD6/ SDRAM_ A14	FTM2_FLT0	FXIO0_D17	
115	82	C6	A3	PTC10	DISABLED		PTC10	I2C1_SCL	FTM3_CH6	I2S0_RX_ FS	FB_AD5/ SDRAM_ A13		FXIO0_D18	
116	83	C5	C4	PTC11/ LLWU_P11	DISABLED		PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7	I2S0_RXD1	FB_RW_b		FXIO0_D19	
117	84	B6	B4	PTC12	DISABLED		PTC12		LPUART4_ RTS_b	FTM_ CLKIN0	FB_AD27/ SDRAM_ D27	FTM3_FLT0	TPM_ CLKIN0	
118	85	A6	A4	PTC13	DISABLED		PTC13		LPUART4_ CTS_b	FTM_ CLKIN1	FB_AD26/ SDRAM_ D26		TPM_ CLKIN1	
119	86	A5	D5	PTC14	DISABLED		PTC14		LPUART4_ RX		FB_AD25/ SDRAM_ D25		FXIO0_D20	
120	87	B5	C5	PTC15	DISABLED		PTC15		LPUART4_ TX		FB_AD24/ SDRAM_ D24		FXIO0_D21	
121	88	—	F6	VSS	VSS	VSS								
122	89	—	E6	VDD	VDD	VDD								
123	—	D5	A5	PTC16	DISABLED		PTC16		LPUART3_ RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_ 16_BLS15_ 8_b/ SDRAM_ DQM2			
124	90	C4	B5	PTC17	DISABLED		PTC17		LPUART3_ TX		FB_CS4_b/ FB_TSIZ0/ FB_BE31_ 24_BLS7_ 0_b/			

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
											SDRAM_DQM3			
125	—	B4	A6	PTC18	DISABLED		PTC18		LPUART3_RTS_b		FB_TBST_b/ FB_CS2_b/ FB_BE15_8_BLS23_16_b/ SDRAM_DQM1			
126	—	A4	B6	PTC19	DISABLED		PTC19		LPUART3_CTS_b		FB_CS3_b/ FB_BE7_0_BLS31_24_b/ SDRAM_DQM0	FB_TA_b		
127	91	D4	C6	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	LPUART2_RTS_b	FTM3_CH0	FB_ALE/ FB_CS1_b/ FB_TS_b		FXIO0_D22	
128	92	D3	D6	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	LPUART2_CTS_b	FTM3_CH1	FB_CS0_b		FXIO0_D23	
129	93	C3	D7	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	LPUART2_RX	FTM3_CH2	FB_AD4/ SDRAM_A12		I2C0_SCL	
130	94	B3	A7	PTD3	DISABLED		PTD3	SPI0_SIN	LPUART2_TX	FTM3_CH3	FB_AD3/ SDRAM_A11		I2C0_SDA	
131	95	A3	B7	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	LPUART0_RTS_b	FTM0_CH4	FB_AD2/ SDRAM_A10	EWM_IN	SPI1_PCS0	
132	96	A2	C7	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	LPUART0_CTS_b	FTM0_CH5	FB_AD1/ SDRAM_A9	EWM_OUT_b	SPI1_SCK	
133	97	B2	A8	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	LPUART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0	SPI1_SOUT	
134	98	—	F6	VSS	VSS	VSS								
135	99	—	E7	VDD	VDD	VDD								
136	100	A1	B8	PTD7	DISABLED		PTD7	CMT_IRO	LPUART0_TX	FTM0_CH7	SDRAM_CKE	FTM0_FLT1	SPI1_SIN	
137	—	A10	A9	PTD8/ LLWU_P24	DISABLED		PTD8/ LLWU_P24	I2C0_SCL				FB_A16	FXIO0_D24	
138	—	A9	C8	PTD9	DISABLED		PTD9	I2C0_SDA				FB_A17	FXIO0_D25	
139	—	E4	B9	PTD10	DISABLED		PTD10					FB_A18	FXIO0_D26	
140	—	E3	A10	PTD11/ LLWU_P25	DISABLED		PTD11/ LLWU_P25	SPI2_PCS0				FB_A19	FXIO0_D27	
141	—	F4	D8	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0			FB_A20	FXIO0_D28	
142	—	G3	C9	PTD13	DISABLED		PTD13	SPI2_SOUT				FB_A21	FXIO0_D29	
143	—	G4	B10	PTD14	DISABLED		PTD14	SPI2_SIN				FB_A22	FXIO0_D30	
144	—	H4	A11	PTD15	DISABLED		PTD15	SPI2_PCS1				FB_A23	FXIO0_D31	

12.3.2 K82 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

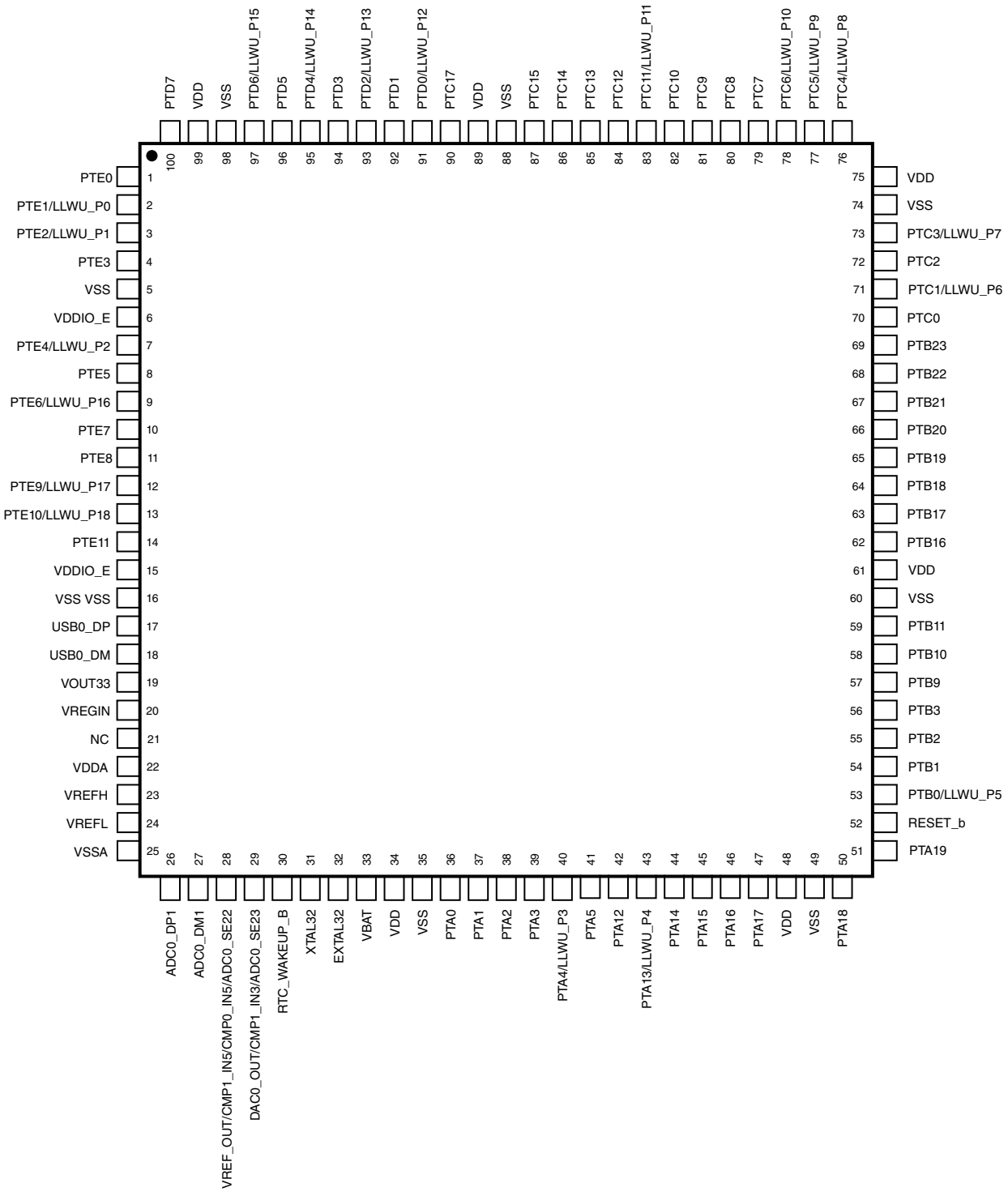


Figure 12-2. K82 100 LQFP Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	PTC19	PTC14	PTC13	PTC8	PTC4/ LLWU_P8	PTD9	PTD8/ LLWU_P24	NC	A
B	PTE0	PTD6/ LLWU_P15	PTD3	PTC18	PTC15	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	PTB4	B
C	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTD2/ LLWU_P13	PTC17	PTC11/ LLWU_P11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	PTB5	C
D	PTE4/ LLWU_P2	PTE3	PTD1	PTD0/ LLWU_P12	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6	PTB18	PTB10	PTB8	D
E	PTE6/ LLWU_P16	PTE5	PTD11/ LLWU_P25	PTD10	VDDIO_E	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	PTE9/ LLWU_P17	PTE8	PTE7	PTD12	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	PTB6	F
G	PTE11	PTE10/ LLWU_P18	PTD13	PTD14	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	USB0_DM	USB0_DP	VSS	PTD15	PTA20	NC	PTA11/ LLWU_P23	PTA1	PTA3	PTA17	PTA29	H
J	VOUT33	VREGIN	ADC0_DP3	NC	PTA21/ LLWU_P21	NC	PTA2	PTA4/ LLWU_P3	PTA10/ LLWU_P22	PTA16	RESET_b	J
K	ADC0_DM0	ADC0_DP0	ADC0_DM3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	RTC_ WAKEUP_B	VBAT	PTA5	PTA12	PTA14	VSS	PTA19	K
L	ADC0_DM1	ADC0_DP1	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22	XTAL32	EXTAL32	VSS	PTA0	PTA13/ LLWU_P4	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 12-3. K82 121 XFBGA Pinout Diagram

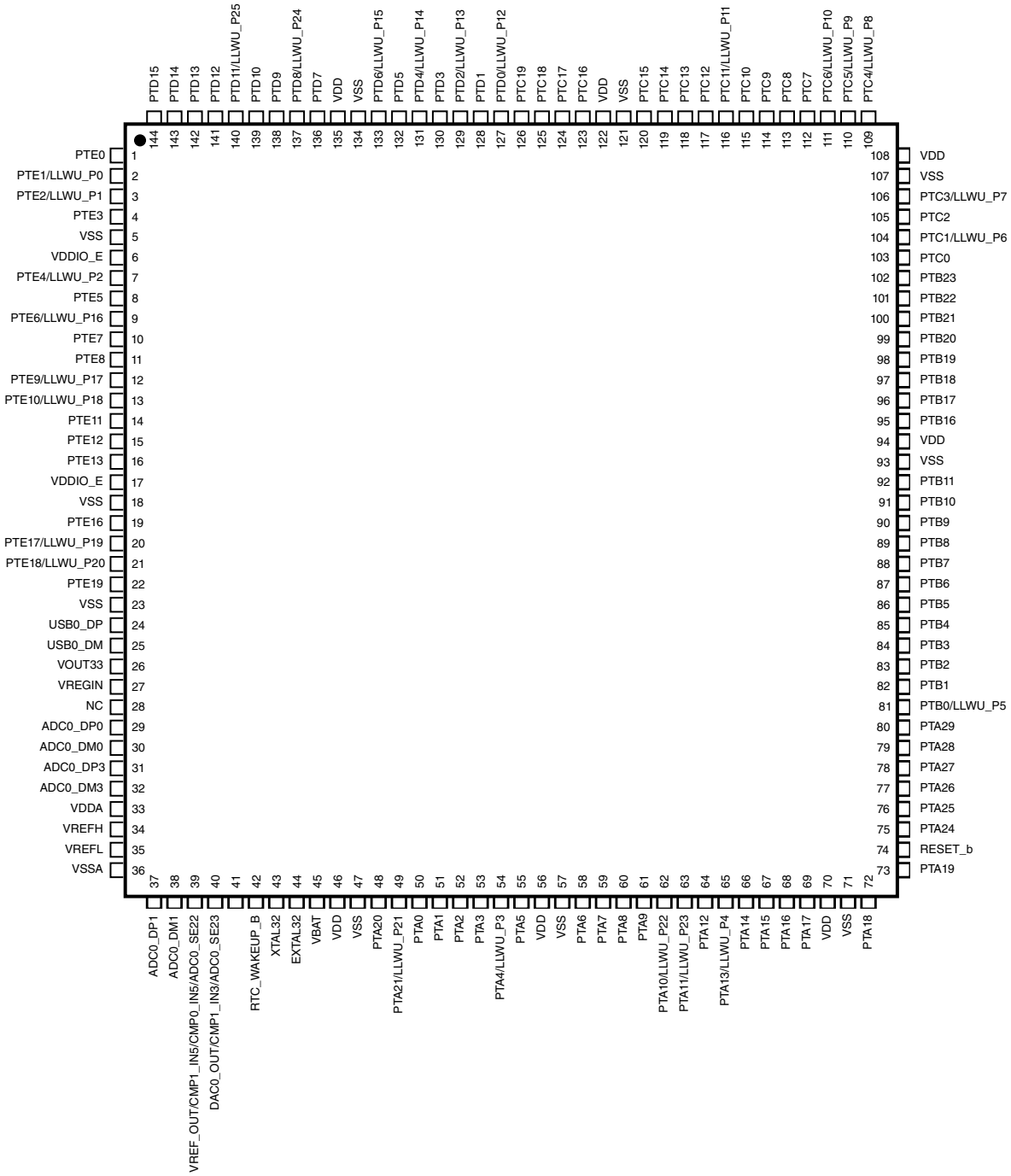


Figure 12-4. K82 144 LQFP Pinout Diagram

NOTE

The 144-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTC4/ LLWU_P8	PTC7	PTC10	PTC13	PTC16	PTC18	PTD3	PTD6/ LLWU_P15	PTD8/ LLWU_P24	PTD11/ LLWU_P25	PTD15	A
B	PTC3/ LLWU_P7	PTC5/ LLWU_P9	PTC8	PTC12	PTC17	PTC19	PTD4/ LLWU_P14	PTD7	PTD10	PTD14	PTE3	B
C	PTC0	PTC2	PTC6/ LLWU_P10	PTC11/ LLWU_P11	PTC15	PTD0/ LLWU_P12	PTD5	PTD9	PTD13	PTE0	PTE4/ LLWU_P2	C
D	PTB20	PTB23	PTC1/ LLWU_P6	PTC9	PTC14	PTD1	PTD2/ LLWU_P13	PTD12	PTE1/ LLWU_P0	PTE2/ LLWU_P1	PTE8	D
E	PTB16	PTB19	PTB21	PTB22	VSS	VDD	VDD	PTE5	PTE6/ LLWU_P16	PTE7	PTE9/ LLWU_P17	E
F	PTB10	PTB11	PTB17	PTB18	VSS VSS	VSS VSS VSS VSS	VDDIO_E	PTE10/ LLWU_P18	PTE11	VDDIO_E	VSS VSS	F
G	PTB5	PTB6	PTB7	PTB8	PTB9	VDD VDD VDD	VDD	ADC0_SE16	NC	VOUT33	USB0_DP	G
H	PTB2	PTB1	PTB3	PTB4	PTA5	PTA4/ LLWU_P3	RTC_ WAKEUP_B	VDDA	VREFH	VREGIN	USB0_DM	H
J	RESET_b	PTA29	PTB0/ LLWU_P5	PTA16	PTA13/ LLWU_P4	PTA1	PTA0	VSSA	VREFL	ADC0_DP0	ADC0_DP3	J
K	PTA19	VSS	PTA17	PTA15	PTA12	PTA2	PTA21/ LLWU_P21	VBAT	NC	ADC0_DM0	ADC0_DM3	K
L	PTA18	VDD	PTA14	PTA11/ LLWU_P23	PTA10/ LLWU_P22	PTA3	PTA20	EXTAL32	XTAL32	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 12-5. K82 121 WLCSP Pinout Diagram

NOTE

The 121-pin WLCSP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

12.4 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

12.4.1 Core Modules

Table 12-3. JTAG Signal Descriptions

Chip signal name	Module signal name	Description	I/O
JTAG_TMS	JTAG_TMS/ SWD_DIO	JTAG Test Mode Selection	I/O
JTAG_TCLK	JTAG_TCLK/ SWD_CLK	JTAG Test Clock	I
JTAG_TDI	JTAG_TDI	JTAG Test Data Input	I
JTAG_TDO	JTAG_TDO/ TRACE_SWO	JTAG Test Data Output	O
JTAG_TRST	JTAG_TRST_b	JTAG Reset	I

Table 12-4. SWD Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SWD_DIO	JTAG_TMS/ SWD_DIO	Serial Wire Data	I/O
SWD_CLK	JTAG_TCLK/ SWD_CLK	Serial Wire Clock	I

Table 12-5. TPIU Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TRACE_CLKOUT	TRACECLK	Trace clock output from the ARM CoreSight debug block	O
TRACE_D[3:2]	TRACEDATA	Trace output data from the ARM CoreSight debug block used for 5-pin interface	O
TRACE_D[1:0]	TRACEDATA	Trace output data from the ARM CoreSight debug block used for both 5-pin and 3-pin interfaces	O
TRACE_SWO	JTAG_TDO/ TRACE_SWO	Trace output data from the ARM CoreSight debug block over a single pin	O

12.4.2 System Modules

Table 12-6. System Signal Descriptions

Chip signal name	Module signal name	Description	I/O
$\overline{\text{NMI}}$	—	Non-maskable interrupt	I

Table continues on the next page...

Table 12-6. System Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
		NOTE: Driving the NMI signal low forces a non-maskable interrupt, if the NMI function is selected on the corresponding pin.	
RESET	—	Reset bi-directional signal	I/O
VDD	—	MCU power	I
VSS	—	MCU ground	I

Table 12-7. EWM Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EWM_IN	EWM_in	EWM input for safety status of external safety circuits. The polarity of EWM_in is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low.	I
EWM_OUT	EWM_out	EWM reset out signal	O

Table 12-8. EMVSIM0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EMVSIM0_CLK	CLK	Smart Card Clock	O
EMVSIM0_IO	IO	Smart Card IO	I/O
EMVSIM0_PD	PD	Smart Card Presence Detect	I
EMVSIM0_RST	RST	Smart Card Reset	O
EMVSIM0_VCCEN	VCCEN	Smart Card Voltage Enable	O

Table 12-9. EMVSIM1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EMVSIM1_CLK	CLK	Smart Card Clock	O
EMVSIM1_IO	IO	Smart Card IO	I/O
EMVSIM1_PD	PD	Smart Card Presence Detect	I
EMVSIM1_RST	RST	Smart Card Reset	O
EMVSIM1_VCCEN	VCCEN	Smart Card Voltage Enable	O

12.4.3 Clock Modules

Table 12-10. OSC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL0	EXTAL	External clock/Oscillator input	I
XTAL0	XTAL	Oscillator output	O

Table 12-11. RTC OSC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL32	EXTAL32	32.768 kHz oscillator input	I
XTAL32	XTAL32	32.768 kHz oscillator output	O

12.4.4 Memories and Memory Interfaces

Table 12-12. FlexBus Signal Descriptions

Chip signal name	Module signal name	Description	I/O
CLKOUT	FB_CLK	FlexBus Clock Output	O
FB_A[29:16]	FB_A[29:16]	Address Bus When FlexBus is used in a multiplexed configuration, this bus is not used.	O
FB_AD[31:0] [1]	FB_AD31 - FB_AD0	This is the address and data bus, FB_AD. The number of byte lanes carrying the data is determined by the port size associated with the matching chip-select. The full 32-bit address is driven on the first clock of a bus cycle (address phase). After the first clock, the data is driven on the bus (data phase). During the data phase, the address is driven on the pins not used for data. For example, in 16-bit mode, the lower address is driven on FB_AD15–FB_AD0, and in 8-bit mode, the lower address is driven on FB_AD23–FB_AD0.	I/O
$\overline{\text{FB_CS}}$[5:0] [2]	$\overline{\text{FB_CS5}}$–$\overline{\text{FB_CS0}}$	General Purpose Chip-Selects—Indicate which external memory or peripheral is selected. A particular chip-select is asserted when the transfer address is within the external memory's or peripheral's address space, as defined in CSAR[BA] and CSMR[BAM].	O
$\overline{\text{FB_BE31_24_BLS7_0}}$, $\overline{\text{FB_BE23_16_BLS15_8}}$, $\overline{\text{FB_BE15_8_BLS23_16}}$,	$\overline{\text{FB_BE_31_24}}$ $\overline{\text{FB_BE_23_16}}$ $\overline{\text{FB_BE_15_8}}$ $\overline{\text{FB_BE_7_0}}$	Byte Enables—Indicate that data is to be latched or driven onto a specific byte lane of the data bus. CSCR[BEM] determines if these signals are asserted on reads and writes or on writes only. For external SRAM or flash devices, the $\overline{\text{FB_BE}}$ outputs should be connected to individual byte strobe signals.	O

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Table 12-12. FlexBus Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
FB_BE7_0_BLS31_24[3]			
FB_OE	FB_OE	Output Enable—Sent to the external memory or peripheral to enable a read transfer. This signal is asserted during read accesses only when a chip-select matches the current address decode.	O
FB_R/W	FB_R/W	Read/Write—Indicates whether the current bus operation is a read operation (FB_R/W high) or a write operation (FB_R/W low).	O
FB_TS/ FB_ALE	FB_TS	Transfer Start—Indicates that the chip has begun a bus transaction and that the address and attributes are valid. An inverted FB_TS is available as an address latch enable (FB_ALE), which indicates when the address is being driven on the FB_AD bus. FB_TS/FB_ALE is asserted for one bus clock cycle. The chip can extend this signal until the first positive clock edge after FB_CS asserts. See CSCR[EXTS] and Extended Transfer Start/Address Latch Enable.	O
FB_TSIZ[1:0]	FB_TSIZ1–FB_TSIZ0	Transfer Size—Indicates (along with FB_TBST) the data transfer size of the current bus operation. The interface supports 8-, 16-, and 32-bit operand transfers and allows accesses to 8-, 16-, and 32-bit data ports. • 00b = 4 bytes • 01b = 1 byte • 10b = 2 bytes • 11b = 16 bytes (line) For misaligned transfers, FB_TSIZ1–FB_TSIZ0 indicate the size of each transfer. For example, if a 32-bit access through a 32-bit port device occurs at a misaligned offset of 1h, 8 bits are transferred first (FB_TSIZ1–FB_TSIZ0 = 01b), 16 bits are transferred next at offset 2h (FB_TSIZ1–FB_TSIZ0 = 10b), and the final 8 bits are transferred at offset 4h (FB_TSIZ1–FB_TSIZ0 = 01b). For aligned transfers larger than the port size, FB_TSIZ1–FB_TSIZ0 behave as follows: • If bursting is used, FB_TSIZ1–FB_TSIZ0 are driven to the transfer size. • If bursting is inhibited, FB_TSIZ1–FB_TSIZ0 first show the entire transfer size and then show the port size. For burst-inhibited transfers, FB_TSIZ1–FB_TSIZ0 change with each FB_TS assertion to reflect the next transfer size. For transfers to port sizes smaller than the transfer size, FB_TSIZ1–FB_TSIZ0 indicate the size of the entire transfer on the first access and the size of the current port transfer on subsequent transfers. For example, for a 32-bit write to an 8-bit port, FB_TSIZ1–FB_TSIZ0 are 00b for the first transaction and 01b for	O

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Table 12-12. FlexBus Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
		the next three transactions. If bursting is used for a 32-bit write to an 8-bit port, FB_TSIZ1–FB_TSIZ0 are driven to 00b for the entire transfer.	
FB_TA[4]	FB_TA	Transfer Acknowledge—Indicates that the external data transfer is complete. When FB_TA is asserted during a read transfer, FlexBus latches the data and then terminates the transfer. When FB_TA is asserted during a write transfer, the transfer is terminated. If auto-acknowledge is disabled (CSCR[AA] = 0), the external memory or peripheral drives FB_TA to terminate the transfer. If auto-acknowledge is enabled (CSCR[AA] = 1), FB_TA is generated internally after a specified number of wait states, or the external memory or peripheral may assert external FB_TA before the wait-state countdown to terminate the transfer early. The chip deasserts FB_CS one cycle after the last FB_TA is asserted. During read transfers, the external memory or peripheral must continue to drive data until FB_TA is recognized. For write transfers, the chip continues driving data one clock cycle after FB_CS is deasserted. The number of wait states is determined by CSCR or the external FB_TA input. If the external FB_TA is used, the external memory or peripheral has complete control of the number of wait states. **Note:** External memory or peripherals should assert FB_TA only while the FB_CS signal to the external memory or peripheral is asserted. The CSPMCR register controls muxing of FB_TA with other signals. When the CSPMCR register does not allow fb_ta control, auto-acknowledge must be used (CSCR[AA] =1'b1); otherwise the bus may hang.	I
FB_TBST	FB_TBST	Transfer Burst—Indicates that a burst transfer is in progress as driven by the chip. A burst transfer can be 2 to 16 beats depending on FB_TSIZ1–FB_TSIZ0 and the port size. **Note:** When a burst transfer is in progress (FB_TBST = 0b), the transfer size is 16 bytes (FB_TSIZ1–FB_TSIZ0 = 11b), and the address is misaligned within the 16-byte boundary, the external memory or peripheral must be able to wrap around the address.	O

1. FB_AD[23:21] not available on 100-LQFP devices.
2. FB_CS3not available on 100-LQFP devices.
3. FB_BE7_0_BLS31_24not available on 100-LQFP devices.
4. FB_TAnotavailable on 100-LQFP devices.

Table 12-13. SDRAM SDR Controller Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SDRAM_RAS	SRAS	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. SRAS should be connected to the corresponding SDRAM SRAS.	O

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Table 12-13. SDRAM SDR Controller Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
SDRAM_CAS	SCAS	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. SCAS should be connected to the corresponding SDRAM SCAS.	O
SDRAM_WE	DRAMW	DRAM read/write. Asserted for write operations and negated for read operations.	O
SDRAM_A[23:9]	SDRAM_A [23:9]	SDRAM address bus output	O
SDRAM_D[31:0]	SDRAM_D [31:0]	SDRAM data bus	I/O
SDRAM_CS[1:0]	SDRAM_CS[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the controller. One SDRAM_CS signal selects one SDRAM block and connects to the corresponding CS signals.	O
SDRAM_CKE	SCKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode in which operations are suspended or capable of entering self-refresh mode.	O
SDRAM_DQM[3:0]	BS[3:0]	SDRAM byte selects BS[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or data qualifier masks) of the SDRAMs.	O

Table 12-14. QSPI signal description

Chip Signal Name	Module SIgnal Name	Description	I/O
QSPI0A_SS0_B	PCSFA1	Peripheral Chip Select Flash A1	O
QSPI0A_SS1_B	PCSFA2	Peripheral Chip Select Flash A2	O
QSPI0B_SS0_B	PCSFB1	Peripheral Chip Select Flash B1	O
QSPI0B_SS1_B	PCSFB2	Peripheral Chip Select Flash B2	O
QSPI0A_SCLK	SCKFA	Serial Clock Flash A	O
QSPI0B_SCLK	SCKFB	Serial Clock Flash B	O
QSPI0B_DATA3 QSPI0B_DATA2 QSPI0B_DATA1 QSPI0B_DATA0 QSPI0A_DATA3 QSPI0A_DATA2 QSPI0A_DATA1 QSPI0A_DATA0	IOFA[7:0]	Serial I/O Flash A	I/O
QSPI0B_DATA3 QSPI0B_DATA2 QSPI0B_DATA1 QSPI0B_DATA0	IOFB[3:0]	Serial I/O Flash B	I/O

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Table 12-14. QSPI signal description (continued)

Chip Signal Name	Module SIgnal Name	Description	I/O
QSPI0A_DQS	DQSFA	Data Strobe signal Flash A	I
QSPI0B_DQS	DQSFB	Data Strobe signal Flash B	I

12.4.5 Analog

Table 12-15. ADC 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ADC0_DP[3:0]	DADP3–DADP0	Differential Analog Channel Inputs	I
ADC0_DM[3:0]	DADM3–DADM0	Differential Analog Channel Inputs	I
ADC0_SEn	AD*n*	Single-Ended Analog Channel Inputs	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VREFL	V_{REFSL}	Voltage Reference Select Low	I
VDDA	V_{DDA}	Analog Power Supply	I
VSSA	V_{SSA}	Analog Ground	I

Table 12-16. CMP 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
CMP0_IN[5:0]	IN[5:0]	Analog voltage inputs	I
CMP0_OUT	CMPO	Comparator output	O

NOTE

There is no CMP0_IN[4] coming from pad.

Table 12-17. CMP 1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
CMP1_IN[5:0]	IN[5:0]	Analog voltage inputs	I
CMP1_OUT	CMPO	Comparator output	O

NOTE

There is no CMP1_IN[2] and CMP1_IN[4] coming from pad

Table 12-18. DAC 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
DAC0_OUT	—	DAC output	O

Table 12-19. VREF Signal Descriptions

Chip signal name	Module signal name	Description	I/O
VREF_OUT	VREF_OUT	Internally-generated Voltage Reference output	O

12.4.6 Timer Modules

Table 12-20. FTM 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FTM_CLKIN[1:0]	EXTCLK	External clock. FTM external clock can be selected to drive the FTM counter.	I
FTM0_CH[7:0]	CHn	FTM channel (n), where n can be 7-0	I/O
FTM0_FLT[3:0]	FAULTj	Fault input (j), where j can be 3-0	I

Table 12-21. FTM 1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FTM_CLKIN[1:0]	EXTCLK	External clock. FTM external clock can be selected to drive the FTM counter.	I
FTM1_CH[1:0]	CHn	FTM channel (n), where n can be 7-0	I/O
FTM1_FLT0	FAULTj	Fault input (j), where j can be 3-0	I
FTM1_QD_PHA	PHA	Quadrature decoder phase A input. Input pin associated with quadrature decoder phase A.	I
FTM1_QD_PHB	PHB	Quadrature decoder phase B input. Input pin associated with quadrature decoder phase B.	I

Table 12-22. FTM 2 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FTM_CLKIN[1:0]	EXTCLK	External clock. FTM external clock can be selected to drive the FTM counter.	I
FTM2_CH[1:0]	CHn	FTM channel (n), where n can be 7-0	I/O
FTM2_FLT0	FAULTj	Fault input (j), where j can be 3-0	I

Table continues on the next page...

Table 12-22. FTM 2 Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
FTM2_QD_PHA	PHA	Quadrature decoder phase A input. Input pin associated with quadrature decoder phase A.	I
FTM2_QD_PHB	PHB	Quadrature decoder phase B input. Input pin associated with quadrature decoder phase B.	I

Table 12-23. FTM 3 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FTM_CLKIN[1:0]	EXTCLK	External clock. FTM external clock can be selected to drive the FTM counter.	I
FTM3_CH[7:0]	CHn	FTM channel (n), where n can be 7-0	I/O
FTM3_FLT0	FAULTj	Fault input (j), where j can be 3-0	I

Table 12-24. CMT Signal Descriptions

Chip signal name	Module signal name	Description	I/O
CMT_IRO	CMT_IRO	Infrared Output	O

Table 12-25. PDB 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
PDB0_EXTRG	EXTRG	External Trigger Input Source If the PDB is enabled and external trigger input source is selected, a positive edge on the EXTRG signal resets and starts the counter.	I

Table 12-26. LPTMR 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR0_ALT[3:1]	LPTMR0_ALT*n*	Pulse Counter Input pin	I
LPTMR1_ALT[3:1]	LPTMR0_ALT*n*	Pulse Counter Input pin	I

Table 12-27. RTC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
VBAT	—	Backup battery supply for RTC and VBAT register file	I
RTC_CLKOUT	RTC_CLKOUT	1 Hz square-wave output or OSCERCLK	O

Table 12-28. TPM 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	EXTCLK	External clock. FTM external clock can be selected to drive the FTM counter.	I
TPM0_CH[5:0]	CHn	FTM channel (n), where n can be 7-0	I/O

Table 12-29. TPM 1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM1_CH[1:0]	TPM_CHn	TPM channel (n = 1 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

12.4.7 Communication Interfaces

Table 12-30. USB FS OTG Signal Descriptions

Chip signal name	Module signal name	Description	I/O
USB0_DM	usb_dm	USB D- analog data signal on the USB bus.	I/O
USB0_DP	usb_dp	USB D+ analog data signal on the USB bus.	I/O
USB_CLKIN	—	Alternate USB clock input	I
USB_SOF_OUT	—	USB start of frame signal. Can be used to make the USB start of frame available for external synchronization.	O

Table 12-31. USB VREG Signal Descriptions

Chip signal name	Module signal name	Description	I/O
VOUT33	reg33_out	Regulator output voltage	O
VREGIN	reg33_in	Unregulated power supply	I

Table 12-32. SPI 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SPI0_PCS0	PCS0/$\overline{SS}$	Peripheral Chip Select 0 (O)	I/O

Table continues on the next page...

Table 12-32. SPI 0 Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
SPI0_PCS[3:1]	PCS[1:3]	Peripheral Chip Selects 1–3	O
SPI0_PCS4	PCS4	Peripheral Chip Select 4	O
SPI0_PCS5	PCS5/ $\overline{\text{PCSS}}$	Peripheral Chip Select 5 /Peripheral Chip Select Strobe	O
SPI0_SIN	SIN	Serial Data In	I
SPI0_SOUT	SOUT	Serial Data Out	O
SPI0_SCK	SCK	Serial Clock (O)	I/O

Table 12-33. SPI 1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SPI1_PCS0	PCS0/$\overline{\text{SS}}$	Peripheral Chip Select 0 (O)	I/O
SPI1_PCS[3:1]	PCS[1:3]	Peripheral Chip Selects 1–3	O
SPI1_SIN	SIN	Serial Data In	I
SPI1_SOUT	SOUT	Serial Data Out	O
SPI1_SCK	SCK	Serial Clock (O)	I/O

Table 12-34. SPI 2 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SPI2_PCS0	PCS0/$\overline{\text{SS}}$	Peripheral Chip Select 0 (O)	I/O
SPI2_PCS1	PCS[1:3]	Peripheral Chip Selects 1–3	O
SPI2_SIN	SIN	Serial Data In	I
SPI2_SOUT	SOUT	Serial Data Out	O
SPI2_SCK	SCK	Serial Clock (O)	I/O

Table 12-35. I^2C 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
I2C0_SCL	SCL	Bidirectional serial clock line of the I^2C system.	I/O
I2C0_SDA	SDA	Bidirectional serial data line of the I^2C system.	I/O

Table 12-36. I^2C 1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
I2C1_SCL	SCL	Bidirectional serial clock line of the I^2C system.	I/O
I2C1_SDA	SDA	Bidirectional serial data line of the I^2C system.	I/O

Table 12-37. I²C 2 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
I2C2_SCL	SCL	Bidirectional serial clock line of the I²C system.	I/O
I2C2_SDA	SDA	Bidirectional serial data line of the I²C system.	I/O

Table 12-38. I²C 3 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
I2C3_SCL	SCL	Bidirectional serial clock line of the I²C system.	I/O
I2C3_SDA	SDA	Bidirectional serial data line of the I²C system.	I/O

Table 12-39. LPUART0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPUART0_CTS_b	CTS	Clear to Send	I
LPUART0_RTS_b	RTS	Request to send	O
$\overline{\text{LPUART0_TX}}$	TXD	Transmit Data	O
$\overline{\text{LPUART0_RX}}$	RXD	Receive Data	I

Table 12-40. LPUART1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPUART1_CTS_b	CTS	Clear to Send	I
LPUART1_RTS_b	RTS	Request to send	O
$\overline{\text{LPUART1_TX}}$	TXD	Transmit Data	O
$\overline{\text{LPUART1_RX}}$	RXD	Receive Data	I

Table 12-41. LPUART2 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPUART2_CTS_b	CTS	Clear to Send	I
LPUART2_RTS_b	RTS	Request to send	O
$\overline{\text{LPUART2_TX}}$	TXD	Transmit Data	O
$\overline{\text{LPUART2_RX}}$	RXD	Receive Data	I

Table 12-42. LPUART3 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPUART3_CTS_b	CTS	Clear to Send	I
LPUART3_RTS_b	RTS	Request to send	O
LPUART3_TX	TXD	Transmit Data	O
LPUART3_RX	RXD	Receive Data	I

Table 12-43. LPUART4 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPUART4_CTS_b	CTS	Clear to Send	I
LPUART4_RTS_b	RTS	Request to send	O
LPUART4_TX	TXD	Transmit Data	O
LPUART4_RX	RXD	Receive Data	I

Table 12-44. SDHC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SDHC0_CLKIN	—	SDHC clock input	I
SDHC0_DCLK	SDHC_DCLK	Generated clock used to drive the MMC, SD, SDIO or CE-ATA cards.	O
SDHC0_CMD	SDHC_CMD	Send commands to and receive responses from the card.	I/O
SDHC0_D0	SDHC_D0	DAT0 line or busy-state detect	I/O
SDHC0_D1	SDHC_D1	8-bit mode: DAT1 line 4-bit mode: DAT1 line or interrupt detect 1-bit mode: Interrupt detect	I/O
SDHC0_D2	SDHC_D2	4-/8-bit mode: DAT2 line or read wait 1-bit mode: Read wait	I/O
SDHC0_D3	SDHC_D3	4-/8-bit mode: DAT3 line or configured as card detection pin 1-bit mode: May be configured as card detection pin	I/O
SDHC0_D4	SDHC_D4	DAT4 line in 8-bit mode Not used in other modes	I/O
SDHC0_D5	SDHC_D5	DAT5 line in 8-bit mode Not used in other modes	I/O
SDHC0_D6	SDHC_D6	DAT6 line in 8-bit mode Not used in other modes	I/O
SDHC0_D7	SDHC_D7	DAT7 line in 8-bit mode Not used in other modes	I/O

Table 12-45. I²S0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
I2S0_MCLK	SAI_MCLK	Audio Master Clock. The master clock is an input when externally generated and an output when internally generated.	I/O
I2S0_RX_BCLK	SAI_RX_BCLK	Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
I2S0_RX_FS	SAI_RX_SYNC	Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
I2S0_RXD	SAI_RX_DATA[1:0]	Receive Data. The receive data is sampled synchronously by the bit clock.	I
I2S0_TX_BCLK	SAI_TX_BCLK	Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
I2S0_TX_FS	SAI_TX_SYNC	Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
I2S0_TXD	SAI_TX_DATA[1:0]	Transmit Data. The transmit data is generated synchronously by the bit clock and is tristated whenever not transmitting a word.	O

Table 12-46. FlexIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FXIO0_Dn(n=0...31)	"FXIO_D"	"Bidirectional FlexIO Shifter and Timer pin inputs/outputs"	I/O

12.4.8 Human-Machine Interfaces (HMI)

Table 12-47. GPIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
PTA[31:0][1]	PORTA31–PORTA0	General-purpose input/output	I/O
PTB[31:0][1]	PORTB31–PORTB0	General-purpose input/output	I/O
PTC[31:0][1]	PORTC31–PORTC0	General-purpose input/output	I/O
PTD[31:0][1]	PORTD31–PORTD0	General-purpose input/output	I/O
PTE[31:0][1]	PORTE31–PORTE0	General-purpose input/output	I/O

1. The available GPIO pins depends on the specific package. See the signal multiplexing section for which exact GPIO signals are available.

Table 12-48. TSI 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TSI0_CH[15:0]	TSI_IN[15:0]	TSI pins. Switchable driver that connects directly to the electrode pins TSI[15:0] can operate as GPIO pins	I/O

Chapter 13
Port Control and Interrupts (PORT)

13.1 Introduction

13.2 Overview

The Port Control and Interrupt (PORT) module provides support for port control, digital filtering, and external interrupt functions.

Most functions can be configured independently for each pin in the 32-bit port and affect the pin regardless of its pin muxing state.

There is one instance of the PORT module for each port. Not all pins within each port are implemented on a specific device.

13.2.1 Features

The PORT module has the following features:

- Pin interrupt
  - Interrupt flag and enable registers for each pin
  - Support for edge sensitive (rising, falling, both) or level sensitive (low, high) configured per pin
  - Support for interrupt or DMA request configured per pin
  - Asynchronous wake-up in low-power modes
  - Pin interrupt is functional in all digital pin muxing modes
- Digital input filter on selected pins
  - Digital input filter for each pin, usable by any digital peripheral muxed onto the pin
  - Individual enable or bypass control field per pin

- Selectable clock source for digital input filter with a five bit resolution on filter size
- Functional in all digital pin multiplexing modes

- Port control
  - Individual pull control fields with pullup, pulldown, and pull-disable support
  - Individual drive strength field supporting high and low drive strength
  - Individual slew rate field supporting fast and slow slew rates
  - Individual input passive filter field supporting enable and disable of the individual input passive filter
  - Individual open drain field supporting enable and disable of the individual open drain output
  - Individual mux control field supporting analog or pin disabled, GPIO, and up to six chip-specific digital functions
  - Pad configuration fields are functional in all digital pin muxing modes.

13.2.2 Modes of operation

13.2.2.1 Run mode

In Run mode, the PORT operates normally.

13.2.2.2 Wait mode

In Wait mode, PORT continues to operate normally and may be configured to exit the Low-Power mode if an enabled interrupt is detected. DMA requests are still generated during the Wait mode, but do not cause an exit from the Low-Power mode.

13.2.2.3 Stop mode

In Stop mode, the PORT can be configured to exit the Low-Power mode via an asynchronous wake-up signal if an enabled interrupt is detected.

In Stop mode, the digital input filters are bypassed unless they are configured to run from the LPO clock source.

13.2.2.4 Debug mode

In Debug mode, PORT operates normally.

13.3 External signal description

The table found here describes the PORT external signal.

Table 13-1. Signal properties

Name	Function	I/O	Reset	Pull
PORTx[31:0]	External interrupt	I/O	0	-

NOTE

Not all pins within each port are implemented on each device.

13.4 Detailed signal description

The table found here contains the detailed signal description for the PORT interface.

Table 13-2. PORT interface—detailed signal description

Signal	I/O	Description	
PORTx[31:0]	I/O	External interrupt.	
		State meaning	Asserted—pin is logic 1. Negated—pin is logic 0.
		Timing	Assertion—may occur at any time and can assert asynchronously to the system clock. Negation—may occur at any time and can assert asynchronously to the system clock.

13.5 Memory map and register definition

Any read or write access to the PORT memory space that is outside the valid memory map results in a bus error. All register accesses complete with zero wait states.

PORT memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4004_9000	Pin Control Register n (PORTA_PCR0)	32	R/W	See section	13.5.1/252
4004_9004	Pin Control Register n (PORTA_PCR1)	32	R/W	See section	13.5.1/252
4004_9008	Pin Control Register n (PORTA_PCR2)	32	R/W	See section	13.5.1/252
4004_900C	Pin Control Register n (PORTA_PCR3)	32	R/W	See section	13.5.1/252
4004_9010	Pin Control Register n (PORTA_PCR4)	32	R/W	See section	13.5.1/252
4004_9014	Pin Control Register n (PORTA_PCR5)	32	R/W	See section	13.5.1/252
4004_9018	Pin Control Register n (PORTA_PCR6)	32	R/W	See section	13.5.1/252
4004_901C	Pin Control Register n (PORTA_PCR7)	32	R/W	See section	13.5.1/252
4004_9020	Pin Control Register n (PORTA_PCR8)	32	R/W	See section	13.5.1/252
4004_9024	Pin Control Register n (PORTA_PCR9)	32	R/W	See section	13.5.1/252
4004_9028	Pin Control Register n (PORTA_PCR10)	32	R/W	See section	13.5.1/252
4004_902C	Pin Control Register n (PORTA_PCR11)	32	R/W	See section	13.5.1/252
4004_9030	Pin Control Register n (PORTA_PCR12)	32	R/W	See section	13.5.1/252
4004_9034	Pin Control Register n (PORTA_PCR13)	32	R/W	See section	13.5.1/252
4004_9038	Pin Control Register n (PORTA_PCR14)	32	R/W	See section	13.5.1/252
4004_903C	Pin Control Register n (PORTA_PCR15)	32	R/W	See section	13.5.1/252
4004_9040	Pin Control Register n (PORTA_PCR16)	32	R/W	See section	13.5.1/252
4004_9044	Pin Control Register n (PORTA_PCR17)	32	R/W	See section	13.5.1/252
4004_9048	Pin Control Register n (PORTA_PCR18)	32	R/W	See section	13.5.1/252
4004_904C	Pin Control Register n (PORTA_PCR19)	32	R/W	See section	13.5.1/252
4004_9050	Pin Control Register n (PORTA_PCR20)	32	R/W	See section	13.5.1/252
4004_9054	Pin Control Register n (PORTA_PCR21)	32	R/W	See section	13.5.1/252
4004_9058	Pin Control Register n (PORTA_PCR22)	32	R/W	See section	13.5.1/252
4004_905C	Pin Control Register n (PORTA_PCR23)	32	R/W	See section	13.5.1/252
4004_9060	Pin Control Register n (PORTA_PCR24)	32	R/W	See section	13.5.1/252
4004_9064	Pin Control Register n (PORTA_PCR25)	32	R/W	See section	13.5.1/252
4004_9068	Pin Control Register n (PORTA_PCR26)	32	R/W	See section	13.5.1/252
4004_906C	Pin Control Register n (PORTA_PCR27)	32	R/W	See section	13.5.1/252
4004_9070	Pin Control Register n (PORTA_PCR28)	32	R/W	See section	13.5.1/252
4004_9074	Pin Control Register n (PORTA_PCR29)	32	R/W	See section	13.5.1/252
4004_9078	Pin Control Register n (PORTA_PCR30)	32	R/W	See section	13.5.1/252
4004_907C	Pin Control Register n (PORTA_PCR31)	32	R/W	See section	13.5.1/252
4004_9080	Global Pin Control Low Register (PORTA_GPCLR)	32	W (always reads 0)	0000_0000h	13.5.2/255
4004_9084	Global Pin Control High Register (PORTA_GPCHR)	32	W (always reads 0)	0000_0000h	13.5.3/255
4004_90A0	Interrupt Status Flag Register (PORTA_ISFR)	32	w1c	0000_0000h	13.5.4/256

Table continues on the next page...

PORT memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4004_90C0	Digital Filter Enable Register (PORTA_DFER)	32	R/W	0000_0000h	13.5.5/256
4004_90C4	Digital Filter Clock Register (PORTA_DFCR)	32	R/W	0000_0000h	13.5.6/257
4004_90C8	Digital Filter Width Register (PORTA_DFWR)	32	R/W	0000_0000h	13.5.7/257
4004_A000	Pin Control Register n (PORTB_PCR0)	32	R/W	See section	13.5.1/252
4004_A004	Pin Control Register n (PORTB_PCR1)	32	R/W	See section	13.5.1/252
4004_A008	Pin Control Register n (PORTB_PCR2)	32	R/W	See section	13.5.1/252
4004_A00C	Pin Control Register n (PORTB_PCR3)	32	R/W	See section	13.5.1/252
4004_A010	Pin Control Register n (PORTB_PCR4)	32	R/W	See section	13.5.1/252
4004_A014	Pin Control Register n (PORTB_PCR5)	32	R/W	See section	13.5.1/252
4004_A018	Pin Control Register n (PORTB_PCR6)	32	R/W	See section	13.5.1/252
4004_A01C	Pin Control Register n (PORTB_PCR7)	32	R/W	See section	13.5.1/252
4004_A020	Pin Control Register n (PORTB_PCR8)	32	R/W	See section	13.5.1/252
4004_A024	Pin Control Register n (PORTB_PCR9)	32	R/W	See section	13.5.1/252
4004_A028	Pin Control Register n (PORTB_PCR10)	32	R/W	See section	13.5.1/252
4004_A02C	Pin Control Register n (PORTB_PCR11)	32	R/W	See section	13.5.1/252
4004_A030	Pin Control Register n (PORTB_PCR12)	32	R/W	See section	13.5.1/252
4004_A034	Pin Control Register n (PORTB_PCR13)	32	R/W	See section	13.5.1/252
4004_A038	Pin Control Register n (PORTB_PCR14)	32	R/W	See section	13.5.1/252
4004_A03C	Pin Control Register n (PORTB_PCR15)	32	R/W	See section	13.5.1/252
4004_A040	Pin Control Register n (PORTB_PCR16)	32	R/W	See section	13.5.1/252
4004_A044	Pin Control Register n (PORTB_PCR17)	32	R/W	See section	13.5.1/252
4004_A048	Pin Control Register n (PORTB_PCR18)	32	R/W	See section	13.5.1/252
4004_A04C	Pin Control Register n (PORTB_PCR19)	32	R/W	See section	13.5.1/252
4004_A050	Pin Control Register n (PORTB_PCR20)	32	R/W	See section	13.5.1/252
4004_A054	Pin Control Register n (PORTB_PCR21)	32	R/W	See section	13.5.1/252
4004_A058	Pin Control Register n (PORTB_PCR22)	32	R/W	See section	13.5.1/252
4004_A05C	Pin Control Register n (PORTB_PCR23)	32	R/W	See section	13.5.1/252
4004_A060	Pin Control Register n (PORTB_PCR24)	32	R/W	See section	13.5.1/252
4004_A064	Pin Control Register n (PORTB_PCR25)	32	R/W	See section	13.5.1/252
4004_A068	Pin Control Register n (PORTB_PCR26)	32	R/W	See section	13.5.1/252
4004_A06C	Pin Control Register n (PORTB_PCR27)	32	R/W	See section	13.5.1/252
4004_A070	Pin Control Register n (PORTB_PCR28)	32	R/W	See section	13.5.1/252
4004_A074	Pin Control Register n (PORTB_PCR29)	32	R/W	See section	13.5.1/252
4004_A078	Pin Control Register n (PORTB_PCR30)	32	R/W	See section	13.5.1/252
4004_A07C	Pin Control Register n (PORTB_PCR31)	32	R/W	See section	13.5.1/252
4004_A080	Global Pin Control Low Register (PORTB_GPCLR)	32	W (always reads 0)	0000_0000h	13.5.2/255

Table continues on the next page...

PORT memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4004_A084	Global Pin Control High Register (PORTB_GPCHR)	32	W (always reads 0)	0000_0000h	13.5.3/255
4004_A0A0	Interrupt Status Flag Register (PORTB_ISFR)	32	w1c	0000_0000h	13.5.4/256
4004_A0C0	Digital Filter Enable Register (PORTB_DFER)	32	R/W	0000_0000h	13.5.5/256
4004_A0C4	Digital Filter Clock Register (PORTB_DFCR)	32	R/W	0000_0000h	13.5.6/257
4004_A0C8	Digital Filter Width Register (PORTB_DFWR)	32	R/W	0000_0000h	13.5.7/257
4004_B000	Pin Control Register n (PORTC_PCR0)	32	R/W	See section	13.5.1/252
4004_B004	Pin Control Register n (PORTC_PCR1)	32	R/W	See section	13.5.1/252
4004_B008	Pin Control Register n (PORTC_PCR2)	32	R/W	See section	13.5.1/252
4004_B00C	Pin Control Register n (PORTC_PCR3)	32	R/W	See section	13.5.1/252
4004_B010	Pin Control Register n (PORTC_PCR4)	32	R/W	See section	13.5.1/252
4004_B014	Pin Control Register n (PORTC_PCR5)	32	R/W	See section	13.5.1/252
4004_B018	Pin Control Register n (PORTC_PCR6)	32	R/W	See section	13.5.1/252
4004_B01C	Pin Control Register n (PORTC_PCR7)	32	R/W	See section	13.5.1/252
4004_B020	Pin Control Register n (PORTC_PCR8)	32	R/W	See section	13.5.1/252
4004_B024	Pin Control Register n (PORTC_PCR9)	32	R/W	See section	13.5.1/252
4004_B028	Pin Control Register n (PORTC_PCR10)	32	R/W	See section	13.5.1/252
4004_B02C	Pin Control Register n (PORTC_PCR11)	32	R/W	See section	13.5.1/252
4004_B030	Pin Control Register n (PORTC_PCR12)	32	R/W	See section	13.5.1/252
4004_B034	Pin Control Register n (PORTC_PCR13)	32	R/W	See section	13.5.1/252
4004_B038	Pin Control Register n (PORTC_PCR14)	32	R/W	See section	13.5.1/252
4004_B03C	Pin Control Register n (PORTC_PCR15)	32	R/W	See section	13.5.1/252
4004_B040	Pin Control Register n (PORTC_PCR16)	32	R/W	See section	13.5.1/252
4004_B044	Pin Control Register n (PORTC_PCR17)	32	R/W	See section	13.5.1/252
4004_B048	Pin Control Register n (PORTC_PCR18)	32	R/W	See section	13.5.1/252
4004_B04C	Pin Control Register n (PORTC_PCR19)	32	R/W	See section	13.5.1/252
4004_B050	Pin Control Register n (PORTC_PCR20)	32	R/W	See section	13.5.1/252
4004_B054	Pin Control Register n (PORTC_PCR21)	32	R/W	See section	13.5.1/252
4004_B058	Pin Control Register n (PORTC_PCR22)	32	R/W	See section	13.5.1/252
4004_B05C	Pin Control Register n (PORTC_PCR23)	32	R/W	See section	13.5.1/252
4004_B060	Pin Control Register n (PORTC_PCR24)	32	R/W	See section	13.5.1/252
4004_B064	Pin Control Register n (PORTC_PCR25)	32	R/W	See section	13.5.1/252
4004_B068	Pin Control Register n (PORTC_PCR26)	32	R/W	See section	13.5.1/252
4004_B06C	Pin Control Register n (PORTC_PCR27)	32	R/W	See section	13.5.1/252
4004_B070	Pin Control Register n (PORTC_PCR28)	32	R/W	See section	13.5.1/252
4004_B074	Pin Control Register n (PORTC_PCR29)	32	R/W	See section	13.5.1/252
4004_B078	Pin Control Register n (PORTC_PCR30)	32	R/W	See section	13.5.1/252

Table continues on the next page...

PORT memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4004_B07C	Pin Control Register n (PORTC_PCR31)	32	R/W	See section	13.5.1/252
4004_B080	Global Pin Control Low Register (PORTC_GPCLR)	32	W (always reads 0)	0000_0000h	13.5.2/255
4004_B084	Global Pin Control High Register (PORTC_GPCHR)	32	W (always reads 0)	0000_0000h	13.5.3/255
4004_B0A0	Interrupt Status Flag Register (PORTC_ISFR)	32	w1c	0000_0000h	13.5.4/256
4004_B0C0	Digital Filter Enable Register (PORTC_DFER)	32	R/W	0000_0000h	13.5.5/256
4004_B0C4	Digital Filter Clock Register (PORTC_DFCR)	32	R/W	0000_0000h	13.5.6/257
4004_B0C8	Digital Filter Width Register (PORTC_DFWR)	32	R/W	0000_0000h	13.5.7/257
4004_C000	Pin Control Register n (PORTD_PCR0)	32	R/W	See section	13.5.1/252
4004_C004	Pin Control Register n (PORTD_PCR1)	32	R/W	See section	13.5.1/252
4004_C008	Pin Control Register n (PORTD_PCR2)	32	R/W	See section	13.5.1/252
4004_C00C	Pin Control Register n (PORTD_PCR3)	32	R/W	See section	13.5.1/252
4004_C010	Pin Control Register n (PORTD_PCR4)	32	R/W	See section	13.5.1/252
4004_C014	Pin Control Register n (PORTD_PCR5)	32	R/W	See section	13.5.1/252
4004_C018	Pin Control Register n (PORTD_PCR6)	32	R/W	See section	13.5.1/252
4004_C01C	Pin Control Register n (PORTD_PCR7)	32	R/W	See section	13.5.1/252
4004_C020	Pin Control Register n (PORTD_PCR8)	32	R/W	See section	13.5.1/252
4004_C024	Pin Control Register n (PORTD_PCR9)	32	R/W	See section	13.5.1/252
4004_C028	Pin Control Register n (PORTD_PCR10)	32	R/W	See section	13.5.1/252
4004_C02C	Pin Control Register n (PORTD_PCR11)	32	R/W	See section	13.5.1/252
4004_C030	Pin Control Register n (PORTD_PCR12)	32	R/W	See section	13.5.1/252
4004_C034	Pin Control Register n (PORTD_PCR13)	32	R/W	See section	13.5.1/252
4004_C038	Pin Control Register n (PORTD_PCR14)	32	R/W	See section	13.5.1/252
4004_C03C	Pin Control Register n (PORTD_PCR15)	32	R/W	See section	13.5.1/252
4004_C040	Pin Control Register n (PORTD_PCR16)	32	R/W	See section	13.5.1/252
4004_C044	Pin Control Register n (PORTD_PCR17)	32	R/W	See section	13.5.1/252
4004_C048	Pin Control Register n (PORTD_PCR18)	32	R/W	See section	13.5.1/252
4004_C04C	Pin Control Register n (PORTD_PCR19)	32	R/W	See section	13.5.1/252
4004_C050	Pin Control Register n (PORTD_PCR20)	32	R/W	See section	13.5.1/252
4004_C054	Pin Control Register n (PORTD_PCR21)	32	R/W	See section	13.5.1/252
4004_C058	Pin Control Register n (PORTD_PCR22)	32	R/W	See section	13.5.1/252
4004_C05C	Pin Control Register n (PORTD_PCR23)	32	R/W	See section	13.5.1/252
4004_C060	Pin Control Register n (PORTD_PCR24)	32	R/W	See section	13.5.1/252
4004_C064	Pin Control Register n (PORTD_PCR25)	32	R/W	See section	13.5.1/252
4004_C068	Pin Control Register n (PORTD_PCR26)	32	R/W	See section	13.5.1/252
4004_C06C	Pin Control Register n (PORTD_PCR27)	32	R/W	See section	13.5.1/252

Table continues on the next page...

PORT memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4004_C070	Pin Control Register n (PORTD_PCR28)	32	R/W	See section	13.5.1/252
4004_C074	Pin Control Register n (PORTD_PCR29)	32	R/W	See section	13.5.1/252
4004_C078	Pin Control Register n (PORTD_PCR30)	32	R/W	See section	13.5.1/252
4004_C07C	Pin Control Register n (PORTD_PCR31)	32	R/W	See section	13.5.1/252
4004_C080	Global Pin Control Low Register (PORTD_GPCLR)	32	W (always reads 0)	0000_0000h	13.5.2/255
4004_C084	Global Pin Control High Register (PORTD_GPCHR)	32	W (always reads 0)	0000_0000h	13.5.3/255
4004_C0A0	Interrupt Status Flag Register (PORTD_ISFR)	32	w1c	0000_0000h	13.5.4/256
4004_C0C0	Digital Filter Enable Register (PORTD_DFER)	32	R/W	0000_0000h	13.5.5/256
4004_C0C4	Digital Filter Clock Register (PORTD_DFCR)	32	R/W	0000_0000h	13.5.6/257
4004_C0C8	Digital Filter Width Register (PORTD_DFWR)	32	R/W	0000_0000h	13.5.7/257
4004_D000	Pin Control Register n (PORTE_PCR0)	32	R/W	See section	13.5.1/252
4004_D004	Pin Control Register n (PORTE_PCR1)	32	R/W	See section	13.5.1/252
4004_D008	Pin Control Register n (PORTE_PCR2)	32	R/W	See section	13.5.1/252
4004_D00C	Pin Control Register n (PORTE_PCR3)	32	R/W	See section	13.5.1/252
4004_D010	Pin Control Register n (PORTE_PCR4)	32	R/W	See section	13.5.1/252
4004_D014	Pin Control Register n (PORTE_PCR5)	32	R/W	See section	13.5.1/252
4004_D018	Pin Control Register n (PORTE_PCR6)	32	R/W	See section	13.5.1/252
4004_D01C	Pin Control Register n (PORTE_PCR7)	32	R/W	See section	13.5.1/252
4004_D020	Pin Control Register n (PORTE_PCR8)	32	R/W	See section	13.5.1/252
4004_D024	Pin Control Register n (PORTE_PCR9)	32	R/W	See section	13.5.1/252
4004_D028	Pin Control Register n (PORTE_PCR10)	32	R/W	See section	13.5.1/252
4004_D02C	Pin Control Register n (PORTE_PCR11)	32	R/W	See section	13.5.1/252
4004_D030	Pin Control Register n (PORTE_PCR12)	32	R/W	See section	13.5.1/252
4004_D034	Pin Control Register n (PORTE_PCR13)	32	R/W	See section	13.5.1/252
4004_D038	Pin Control Register n (PORTE_PCR14)	32	R/W	See section	13.5.1/252
4004_D03C	Pin Control Register n (PORTE_PCR15)	32	R/W	See section	13.5.1/252
4004_D040	Pin Control Register n (PORTE_PCR16)	32	R/W	See section	13.5.1/252
4004_D044	Pin Control Register n (PORTE_PCR17)	32	R/W	See section	13.5.1/252
4004_D048	Pin Control Register n (PORTE_PCR18)	32	R/W	See section	13.5.1/252
4004_D04C	Pin Control Register n (PORTE_PCR19)	32	R/W	See section	13.5.1/252
4004_D050	Pin Control Register n (PORTE_PCR20)	32	R/W	See section	13.5.1/252
4004_D054	Pin Control Register n (PORTE_PCR21)	32	R/W	See section	13.5.1/252
4004_D058	Pin Control Register n (PORTE_PCR22)	32	R/W	See section	13.5.1/252
4004_D05C	Pin Control Register n (PORTE_PCR23)	32	R/W	See section	13.5.1/252
4004_D060	Pin Control Register n (PORTE_PCR24)	32	R/W	See section	13.5.1/252

Table continues on the next page...

PORT memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4004_D064	Pin Control Register n (PORTE_PCR25)	32	R/W	See section	13.5.1/252
4004_D068	Pin Control Register n (PORTE_PCR26)	32	R/W	See section	13.5.1/252
4004_D06C	Pin Control Register n (PORTE_PCR27)	32	R/W	See section	13.5.1/252
4004_D070	Pin Control Register n (PORTE_PCR28)	32	R/W	See section	13.5.1/252
4004_D074	Pin Control Register n (PORTE_PCR29)	32	R/W	See section	13.5.1/252
4004_D078	Pin Control Register n (PORTE_PCR30)	32	R/W	See section	13.5.1/252
4004_D07C	Pin Control Register n (PORTE_PCR31)	32	R/W	See section	13.5.1/252
4004_D080	Global Pin Control Low Register (PORTE_GPCLR)	32	W (always reads 0)	0000_0000h	13.5.2/255
4004_D084	Global Pin Control High Register (PORTE_GPCHR)	32	W (always reads 0)	0000_0000h	13.5.3/255
4004_D0A0	Interrupt Status Flag Register (PORTE_ISFR)	32	w1c	0000_0000h	13.5.4/256
4004_D0C0	Digital Filter Enable Register (PORTE_DFER)	32	R/W	0000_0000h	13.5.5/256
4004_D0C4	Digital Filter Clock Register (PORTE_DFCR)	32	R/W	0000_0000h	13.5.6/257
4004_D0C8	Digital Filter Width Register (PORTE_DFWR)	32	R/W	0000_0000h	13.5.7/257

13.5.1 Pin Control Register n (PORTx_PCR*n*)

NOTE

See the Signal Multiplexing and Pin Assignment chapter for the reset value of this device.

See the GPIO Configuration section for details on the available functions for each pin.

Do not modify pin configuration registers associated with pins not available in your selected package. All unbonded pins not available in your package will default to DISABLE state for lowest power consumption.

Address: Base address + 0h offset + (4d × i), where i=0d to 31d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0							ISF	0				IRQC			
W								w1c								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	LK	0				MUX			0	DSE	ODE	PFE	0	SRE	PE	PS
W																
Reset	0	0	0	0	0	*	*	*	0	*	0	*	0	*	*	*

* Notes:
- MUX field: Varies by port. See Signal Multiplexing and Signal Descriptions chapter for reset values per port.
- DSE field: Varies by port. See the Signal Multiplexing and Signal Descriptions chapter for reset values per port.
- PFE field: Varies by port. See Signal Multiplexing and Signal Descriptions chapter for reset values per port.
- SRE field: Varies by port. See Signal Multiplexing and Signal Descriptions chapter for reset values per port.
- PE field: Varies by port. See Signal Multiplexing and Signal Descriptions chapter for reset values per port.
- PS field: Varies by port. See Signal Multiplexing and Signal Descriptions chapter for reset values per port.

PORTx_PCR*n* field descriptions

Field	Description
31–25 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
24 ISF	Interrupt Status Flag The pin interrupt configuration is valid in all digital pin muxing modes.

Table continues on the next page...

PORTx_PCR*n* field descriptions (continued)

Field	Description
	0 Configured interrupt is not detected. 1 Configured interrupt is detected. If the pin is configured to generate a DMA request, then the corresponding flag will be cleared automatically at the completion of the requested DMA transfer. Otherwise, the flag remains set until a logic 1 is written to the flag. If the pin is configured for a level sensitive interrupt and the pin remains asserted, then the flag is set again immediately after it is cleared.
23–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–16 IRQC	Interrupt Configuration The pin interrupt configuration is valid in all digital pin muxing modes. The corresponding pin is configured to generate interrupt/DMA request as follows: 0000 Interrupt Status Flag (ISF) is disabled. 0001 ISF flag and DMA request on rising edge. 0010 ISF flag and DMA request on falling edge. 0011 ISF flag and DMA request on either edge. 0100 Reserved. 0101 Reserved. 0110 Reserved. 0111 Reserved. 1000 ISF flag and Interrupt when logic 0. 1001 ISF flag and Interrupt on rising-edge. 1010 ISF flag and Interrupt on falling-edge. 1011 ISF flag and Interrupt on either edge. 1100 ISF flag and Interrupt when logic 1. 1101 Reserved. 1110 Reserved. 1111 Reserved.
15 LK	Lock Register 0 Pin Control Register fields [15:0] are not locked. 1 Pin Control Register fields [15:0] are locked and cannot be updated until the next system reset.
14–11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10–8 MUX	Pin Mux Control Not all pins support all pin muxing slots. Unimplemented pin muxing slots are reserved and may result in configuring the pin for a different pin muxing slot. The corresponding pin is configured in the following pin muxing slot as follows: 000 Pin disabled (Alternative 0) (analog). 001 Alternative 1 (GPIO). 010 Alternative 2 (chip-specific). 011 Alternative 3 (chip-specific). 100 Alternative 4 (chip-specific). 101 Alternative 5 (chip-specific). 110 Alternative 6 (chip-specific). 111 Alternative 7 (chip-specific).

Table continues on the next page...

PORTx_PCR*n* field descriptions (continued)

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 DSE	Drive Strength Enable Drive strength configuration is valid in all digital pin muxing modes. 0 Low drive strength is configured on the corresponding pin, if pin is configured as a digital output. 1 High drive strength is configured on the corresponding pin, if pin is configured as a digital output.
5 ODE	Open Drain Enable Open drain configuration is valid in all digital pin muxing modes. 0 Open drain output is disabled on the corresponding pin. 1 Open drain output is enabled on the corresponding pin, if the pin is configured as a digital output.
4 PFE	Passive Filter Enable Passive filter configuration is valid in all digital pin muxing modes. 0 Passive input filter is disabled on the corresponding pin. 1 Passive input filter is enabled on the corresponding pin, if the pin is configured as a digital input. Refer to the device data sheet for filter characteristics.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 SRE	Slew Rate Enable Slew rate configuration is valid in all digital pin muxing modes. 0 Fast slew rate is configured on the corresponding pin, if the pin is configured as a digital output. 1 Slow slew rate is configured on the corresponding pin, if the pin is configured as a digital output.
1 PE	Pull Enable Pull configuration is valid in all digital pin muxing modes. 0 Internal pullup or pulldown resistor is not enabled on the corresponding pin. 1 Internal pullup or pulldown resistor is enabled on the corresponding pin, if the pin is configured as a digital input.
0 PS	Pull Select Pull configuration is valid in all digital pin muxing modes. 0 Internal pulldown resistor is enabled on the corresponding pin, if the corresponding PE field is set. 1 Internal pullup resistor is enabled on the corresponding pin, if the corresponding PE field is set.

13.5.2 Global Pin Control Low Register (PORTx_GPCLR)

Only 32-bit writes are supported to this register.

Address: Base address + 80h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W	GPWE																GPWD															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PORTx_GPCLR field descriptions

Field	Description
31–16 GPWE	Global Pin Write Enable Selects which Pin Control Registers (15 through 0) bits [15:0] update with the value in GPWD. If a selected Pin Control Register is locked then the write to that register is ignored. 0 Corresponding Pin Control Register is not updated with the value in GPWD. 1 Corresponding Pin Control Register is updated with the value in GPWD.
GPWD	Global Pin Write Data Write value that is written to all Pin Control Registers bits [15:0] that are selected by GPWE.

13.5.3 Global Pin Control High Register (PORTx_GPCHR)

Only 32-bit writes are supported to this register.

Address: Base address + 84h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W	GPWE																GPWD															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PORTx_GPCHR field descriptions

Field	Description
31–16 GPWE	Global Pin Write Enable Selects which Pin Control Registers (31 through 16) bits [15:0] update with the value in GPWD. If a selected Pin Control Register is locked then the write to that register is ignored. 0 Corresponding Pin Control Register is not updated with the value in GPWD. 1 Corresponding Pin Control Register is updated with the value in GPWD.
GPWD	Global Pin Write Data Write value that is written to all Pin Control Registers bits [15:0] that are selected by GPWE.

13.5.4 Interrupt Status Flag Register (PORTx_ISFR)

The pin interrupt configuration is valid in all digital pin muxing modes. The Interrupt Status Flag for each pin is also visible in the corresponding Pin Control Register, and each flag can be cleared in either location.

Address: Base address + A0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ISF																															
W	w1c																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PORTx_ISFR field descriptions

Field	Description
ISF	Interrupt Status Flag Each bit in the field indicates the detection of the configured interrupt of the same number as the field. 0 Configured interrupt is not detected. 1 Configured interrupt is detected. If the pin is configured to generate a DMA request, then the corresponding flag will be cleared automatically at the completion of the requested DMA transfer. Otherwise, the flag remains set until a logic 1 is written to the flag. If the pin is configured for a level sensitive interrupt and the pin remains asserted, then the flag is set again immediately after it is cleared.

13.5.5 Digital Filter Enable Register (PORTx_DFER)

The corresponding bit is read only for pins that do not support a digital filter. Refer to the Chapter of Signal Multiplexing and Signal Descriptions for the pins that support digital filter.

The digital filter configuration is valid in all digital pin muxing modes.

Address: Base address + C0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	DFE																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PORTx_DFER field descriptions

Field	Description
DFE	Digital Filter Enable

PORTx_DFER field descriptions (continued)

Field	Description
	The digital filter configuration is valid in all digital pin muxing modes. The output of each digital filter is reset to zero at system reset and whenever the digital filter is disabled. Each bit in the field enables the digital filter of the same number as the field. 0 Digital filter is disabled on the corresponding pin and output of the digital filter is reset to zero. 1 Digital filter is enabled on the corresponding pin, if the pin is configured as a digital input.

13.5.6 Digital Filter Clock Register (PORTx_DFCR)

This register is read only for ports that do not support a digital filter.

The digital filter configuration is valid in all digital pin muxing modes.

Address: Base address + C4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															CS
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PORTx_DFCR field descriptions

Field	Description
31–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 CS	Clock Source The digital filter configuration is valid in all digital pin muxing modes. Configures the clock source for the digital input filters. Changing the filter clock source must be done only when all digital filters are disabled. 0 Digital filters are clocked by the bus clock. 1 Digital filters are clocked by the LPO clock.

13.5.7 Digital Filter Width Register (PORTx_DFWR)

This register is read only for ports that do not support a digital filter.

The digital filter configuration is valid in all digital pin muxing modes.

Address: Base address + C8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																											FILT				
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PORTx_DFWR field descriptions

Field	Description
31–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
FILT	Filter Length The digital filter configuration is valid in all digital pin muxing modes. Configures the maximum size of the glitches, in clock cycles, that the digital filter absorbs for the enabled digital filters. Glitches that are longer than this register setting will pass through the digital filter, and glitches that are equal to or less than this register setting are filtered. Changing the filter length must be done only after all filters are disabled.

13.6 Functional description

13.6.1 Pin control

Each port pin has a corresponding Pin Control register, PORT_PCRn, associated with it.

The upper half of the Pin Control register configures the pin's capability to either interrupt the CPU or request a DMA transfer, on a rising/falling edge or both edges as well as a logic level occurring on the port pin. It also includes a flag to indicate that an interrupt has occurred. The LK bit (bit 15 of Pin Control Register PCR*n*) locks the lower 16 bits of each Pin Control register and blocks any writes to that register until the next system reset.

The lower half of the Pin Control register configures the following functions for each pin within the 32-bit port.

- Pullup or pulldown enable
- Drive strength and slew rate configuration
- Open drain enable
- Passive input filter enable
- Pin Muxing mode

The functions apply across all digital pin muxing modes and individual peripherals do not override the configuration in the Pin Control register. For example, if an I^2C function is enabled on a pin, that does not override the pullup or open drain configuration for that pin.

When the Pin Muxing mode is configured for analog or is disabled, all the digital functions on that pin are disabled. This includes the pullup and pulldown enables, output buffer enable, input buffer enable, and passive filter enable.

A lock field also exists that allows the configuration for each pin to be locked until the next system reset. When locked, writes to the lower half of that pin control register are ignored, although a bus error is not generated on an attempted write to a locked register.

The configuration of each Pin Control register is retained when the PORT module is disabled.

Whenever a pin is configured in any digital pin muxing mode, the input buffer for that pin is enabled allowing the pin state to be read via the corresponding GPIO Port Data Input Register (GPIO_PDIR) or allowing a pin interrupt or DMA request to be generated. If a pin is ever floating when its input buffer is enabled, then this can cause an increase in power consumption and must be avoided. A pin can be floating due to an input pin that is not connected or an output pin that has tri-stated (output buffer is disabled).

Enabling the internal pull resistor (or implementing an external pull resistor) will ensure a pin does not float when its input buffer is enabled; note that the internal pull resistor is automatically disabled whenever the output buffer is enabled allowing the Pull Enable bit to remain set. Configuring the Pin Muxing mode to disabled or analog will disable the pin's input buffer and results in the lowest power consumption.

13.6.2 Global pin control

The two global pin control registers allow a single register write to update the lower half of the pin control register on up to 16 pins, all with the same value. Registers that are locked cannot be written using the global pin control registers.

The global pin control registers are designed to enable software to quickly configure multiple pins within the one port for the same peripheral function. However, the interrupt functions cannot be configured using the global pin control registers.

The global pin control registers are write-only registers, that always read as 0.

13.6.3 External interrupts

The external interrupt capability of the PORT module is available in all digital pin muxing modes provided the PORT module is enabled.

Each pin can be individually configured for any of the following external interrupt modes:

- Interrupt disabled, default out of reset
- Active high level sensitive interrupt
- Active low level sensitive interrupt
- Rising edge sensitive interrupt
- Falling edge sensitive interrupt
- Rising and falling edge sensitive interrupt
- Rising edge sensitive DMA request
- Falling edge sensitive DMA request
- Rising and falling edge sensitive DMA request

The interrupt status flag is set when the configured edge or level is detected on the pin or at the output of the digital input filter, if the digital input digital filter is enabled. When not in Stop mode, the input is first synchronized to the bus clock to detect the configured level or edge transition.

The PORT module generates a single interrupt that asserts when the interrupt status flag is set for any enabled interrupt for that port. The interrupt negates after the interrupt status flags for all enabled interrupts have been cleared by writing a logic 1 to the ISF flag in either the PORT_ISFR or PORT_PCRn registers.

The PORT module generates a single DMA request that asserts when the interrupt status flag is set for any enabled DMA request in that port. The DMA request negates after the DMA transfer is completed, because that clears the interrupt status flags for all enabled DMA requests.

During Stop mode, the interrupt status flag for any enabled interrupt is asynchronously set if the required level or edge is detected. This also generates an asynchronous wake-up signal to exit the Low-Power mode.

13.6.4 Digital filter

The digital filter capabilities of the PORT module are available in all digital Pin Muxing modes if the PORT module is enabled.

The clock used for all digital filters within one port can be configured between the bus clock or the LPO clock. This selection must be changed only when all digital filters for that port are disabled. If the digital filters for a port are configured to use the bus clock, then the digital filters are bypassed for the duration of Stop mode. While the digital filters are bypassed, the output of each digital filter always equals the input pin, but the internal state of the digital filters remains static and does not update due to any change on the input pin.

The filter width in clock size is the same for all enabled digital filters within one port and must be changed only when all digital filters for that port are disabled.

The output of each digital filter is logic zero after system reset and whenever a digital filter is disabled. After a digital filter is enabled, the input is synchronized to the filter clock, either the bus clock or the LPO clock. If the synchronized input and the output of the digital filter remain different for a number of filter clock cycles equal to the filter width register configuration, then the output of the digital filter updates to equal the synchronized filter input.

The minimum latency through a digital filter equals two or three filter clock cycles plus the filter width configuration register.

Chapter 14
System Integration Module (SIM)

14.1 Introduction

The System Integration Module (SIM) provides system control and chip configuration registers.

14.1.1 Features

Features of the SIM include:

- System clocking configuration
  - System clock divide values
  - Architectural clock gating control
  - USB clock selection and divide values
  - SDHC clock source selection
- Flash and system RAM size configuration
- USB regulator configuration
- FlexTimer external clock, hardware trigger, and fault source selection
- UART0 and UART1 receive/transmit source selection/configuration

14.2 Memory map and register definition

The SIM module contains many fields for selecting the clock source and dividers for various module clocks. See the Clock Distribution chapter for more information, including block diagrams and clock definitions.

NOTE

The SIM_SOPT1 and SIM_SOPT1CFG registers are located at a different base address than the other SIM registers.

SIM memory map

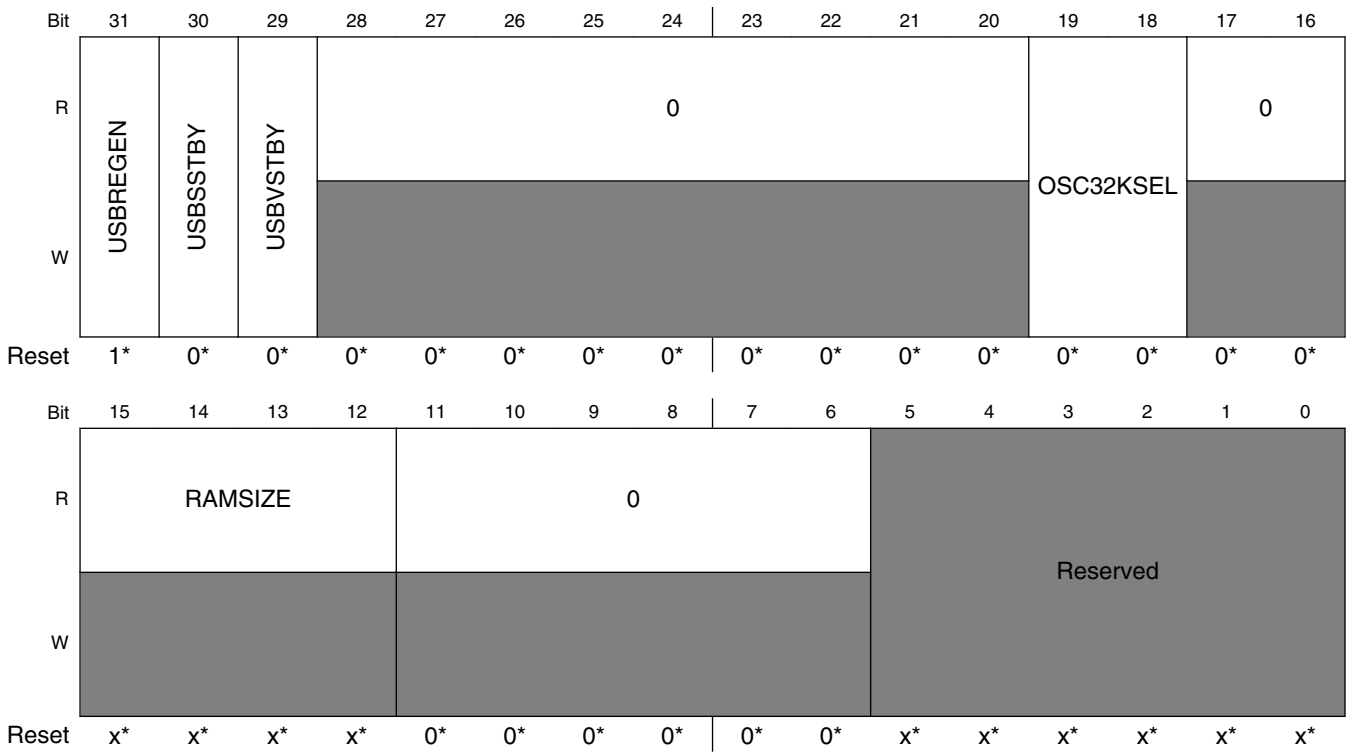
Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4004_7000	System Options Register 1 (SIM_SOPT1)	32	R/W	See section	14.2.1/265
4004_7004	SOPT1 Configuration Register (SIM_SOPT1CFG)	32	R/W	0000_0000h	14.2.2/267
4004_8004	System Options Register 2 (SIM_SOPT2)	32	R/W	0000_1000h	14.2.3/268
4004_800C	System Options Register 4 (SIM_SOPT4)	32	R/W	0000_0000h	14.2.4/271
4004_8010	System Options Register 5 (SIM_SOPT5)	32	R/W	0000_0000h	14.2.5/274
4004_8018	System Options Register 7 (SIM_SOPT7)	32	R/W	0000_0000h	14.2.6/275
4004_801C	System Options Register 8 (SIM_SOPT8)	32	R/W	0000_0000h	14.2.7/277
4004_8020	System Options Register 9 (SIM_SOPT9)	32	R/W	0000_0000h	14.2.8/279
4004_8024	System Device Identification Register (SIM_SDID)	32	R	See section	14.2.9/280
4004_8028	System Clock Gating Control Register 1 (SIM_SCGC1)	32	R/W	0000_0000h	14.2.10/282
4004_802C	System Clock Gating Control Register 2 (SIM_SCGC2)	32	R/W	0000_0000h	14.2.11/283
4004_8030	System Clock Gating Control Register 3 (SIM_SCGC3)	32	R/W	0000_0000h	14.2.12/286
4004_8034	System Clock Gating Control Register 4 (SIM_SCGC4)	32	R/W	F010_0030h	14.2.13/287
4004_8038	System Clock Gating Control Register 5 (SIM_SCGC5)	32	R/W	0004_0182h	14.2.14/289
4004_803C	System Clock Gating Control Register 6 (SIM_SCGC6)	32	R/W	4000_0001h	14.2.15/291
4004_8040	System Clock Gating Control Register 7 (SIM_SCGC7)	32	R/W	0000_0006h	14.2.16/294
4004_8044	System Clock Divider Register 1 (SIM_CLKDIV1)	32	R/W	See section	14.2.17/295
4004_8048	System Clock Divider Register 2 (SIM_CLKDIV2)	32	R/W	0000_0000h	14.2.18/297
4004_804C	Flash Configuration Register 1 (SIM_FCFG1)	32	R	See section	14.2.19/298
4004_8050	Flash Configuration Register 2 (SIM_FCFG2)	32	R	See section	14.2.20/299
4004_8054	Unique Identification Register High (SIM_UIDH)	32	R	See section	14.2.21/300
4004_8058	Unique Identification Register Mid-High (SIM_UIDMH)	32	R	See section	14.2.22/300
4004_805C	Unique Identification Register Mid Low (SIM_UIDML)	32	R	See section	14.2.23/301
4004_8060	Unique Identification Register Low (SIM_UIDL)	32	R	See section	14.2.24/301
4004_8064	System Clock Divider Register 3 (SIM_CLKDIV3)	32	R/W	0000_0000h	14.2.25/302
4004_8068	System Clock Divider Register 4 (SIM_CLKDIV4)	32	R/W	0000_0000h	14.2.26/303

14.2.1 System Options Register 1 (SIM_SOPT1)

NOTE

The SOPT1 register is only reset on POR or LVD.

Address: 4004_7000h base + 0h offset = 4004_7000h



* Notes:

- x = Undefined at reset.

SIM_SOPT1 field descriptions

Field	Description
31 USBREGEN	USB voltage regulator enable Controls whether the USB voltage regulator is enabled. 0 USB voltage regulator is disabled. 1 USB voltage regulator is enabled.
30 USBSSTBY	USB voltage regulator in standby mode during Stop, VLPS, LLS and VLLS modes. Controls whether the USB voltage regulator is placed in standby mode during Stop, VLPS, LLS and VLLS modes. 0 USB voltage regulator not in standby during Stop, VLPS, LLS and VLLS modes. 1 USB voltage regulator in standby during Stop, VLPS, LLS and VLLS modes.

Table continues on the next page...

SIM_SOPT1 field descriptions (continued)

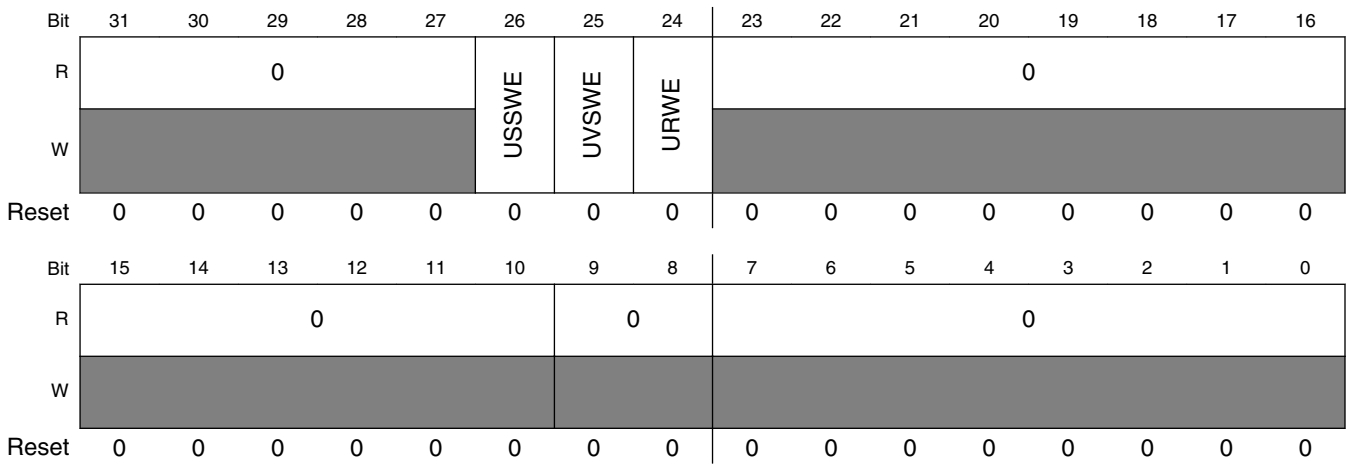
Field	Description
29 USBVSTBY	USB voltage regulator in standby mode during VLPR and VLPW modes Controls whether the USB voltage regulator is placed in standby mode during VLPR and VLPW modes. 0 USB voltage regulator not in standby during VLPR and VLPW modes. 1 USB voltage regulator in standby during VLPR and VLPW modes.
28–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–18 OSC32KSEL	32K oscillator clock select Selects the 32 kHz clock source (ERCLK32K) for TSI,and LPTMR. This field is reset only on POR/LVD. 00 System oscillator (OSC32KCLK) 01 Reserved 10 RTC 32.768kHz oscillator 11 LPO 1 kHz
17–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–12 RAMSIZE	RAM size This field specifies the amount of system RAM available on the device. 0001 8 KB 0011 16 KB 0100 24 KB 0101 32 KB 0110 48 KB 0111 64 KB 1000 96 KB 1001 128 KB 1011 256 KB
11–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
Reserved	This field is reserved.

14.2.2 SOPT1 Configuration Register (SIM_SOPT1CFG)

NOTE

The SOPT1CFG register is reset on System Reset not VLLS.

Address: 4004_7000h base + 4h offset = 4004_7004h



SIM_SOPT1CFG field descriptions

Field	Description
31–27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 USSWE	USB voltage regulator stop standby write enable Writing one to the USSWE bit allows the SOPT1 USBSSTBY bit to be written. This register bit clears after a write to USBSSTBY. 0 SOPT1 USBSSTBY cannot be written. 1 SOPT1 USBSSTBY can be written.
25 UVSWE	USB voltage regulator VLP standby write enable Writing one to the UVSWE bit allows the SOPT1 USBVSTBY bit to be written. This register bit clears after a write to USBVSTBY. 0 SOPT1 USBVSTBY cannot be written. 1 SOPT1 USBVSTBY can be written.
24 URWE	USB voltage regulator enable write enable Writing one to the URWE bit allows the SOPT1 USBREGEN bit to be written. This register bit clears after a write to USBREGEN. 0 SOPT1 USBREGEN cannot be written. 1 SOPT1 USBREGEN can be written.

Table continues on the next page...

SIM_SOPT1CFG field descriptions (continued)

Field	Description
23–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

14.2.3 System Options Register 2 (SIM_SOPT2)

SOPT2 contains the controls for selecting many of the module clock source options on this device. See the Clock Distribution chapter for more information including clocking diagrams and definitions of device clocks.

Address: 4004_7000h base + 1004h offset = 4004_8004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	EMVSIMSRC		SDHCSRC		LPUARTSRC		TPMSRC		FLEXIOSRC		0			USBSRC	PLLFLLSEL	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0			TRACECLKSEL	0	0	FBSL		CLKOUTSEL			RTCCLKOUTSEL	0			
W																
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

SIM_SOPT2 field descriptions

Field	Description
31–30 EMVSIMSRC	EMVSIM Module Clock Source Select Selects the clock source for the EMVSIM transmit and receive clock. 00 Clock disabled 01 MCGFLLCLK , or MCGPLLCLK, or IRC48M clock as selected by SOPT2[PLLFLLSEL], and then divided by the PLLFLLCLK fractional divider as configured by SIM_CLKDIV3[PLLFLLFRAC, PLLFLLDIV]. 10 OSCERCLK clock 11 MCGIRCLK clock

Table continues on the next page...

SIM_SOPT2 field descriptions (continued)

Field	Description
29–28 SDHCSRC	SDHC clock source select Selects the clock source for the SDHC clock . 00 Core/system clock. 01 MCGFLLCLK, or MCGPLLCLK, or IRC48M clock as selected by SOPT2[PLLFLLSEL]. 10 OSCERCLK clock 11 External bypass clock (SDHC0_CLKIN)
27–26 LPUARTSRC	LPUART clock source select Selects the clock source for the LPUART transmit and receive clock. 00 Clock disabled 01 MCGFLLCLK , or MCGPLLCLK, or IRC48M clock as selected by SOPT2[PLLFLLSEL], and then divided by the PLLFLLCLK fractional divider as configured by SIM_CLKDIV3[PLLFLLFRAC, PLLFLLDIV]. 10 OSCERCLK clock 11 MCGIRCLK clock
25–24 TPMSRC	TPM clock source select Selects the clock source for the TPM counter clock 00 Clock disabled 01 MCGFLLCLK , or MCGPLLCLK, or IRC48M clock as selected by SOPT2[PLLFLLSEL], and then divided by the PLLFLLCLK fractional divider as configured by SIM_CLKDIV3[PLLFLLFRAC, PLLFLLDIV]. 10 OSCERCLK clock 11 MCGIRCLK clock
23–22 FLEXIOSRC	FlexIO Module Clock Source Select Selects the clock source for the FlexIO transmit and receive clock. 00 System clock 01 MCGFLLCLK , or MCGPLLCLK, or IRC48M clock as selected by SOPT2[PLLFLLSEL], and then divided by the PLLFLLCLK fractional divider as configured by SIM_CLKDIV3[PLLFLLFRAC, PLLFLLDIV]. 10 OSCERCLK clock 11 MCGIRCLK clock
21–19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18 USBSRC	USB clock source select Selects the clock source for the USB 48 MHz clock. 0 External bypass clock (USB_CLKIN). 1 MCGFLLCLK, or MCGPLLCLK, or IRC48M clock as selected by SOPT2[PLLFLLSEL], and then divided by the USB fractional divider as configured by SIM_CLKDIV2[USBFRAC, USBDIV].
17–16 PLLFLLSEL	PLL/FLL clock select Selects the high frequency clock for various peripheral clocking options. 00 MCGFLLCLK clock

Table continues on the next page...

SIM_SOPT2 field descriptions (continued)

Field	Description
	01 MCGPLLCLK clock 10 Reserved 11 IRC48 MHz clock
15–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12 TRACECLKSEL	Debug trace clock select Selects the core/system clock, or MCG output clock (MCGOUTCLK) divided by the TRACECLK fractional divider as configured by SIM_CLKDIV4[TRACEFRAC, TRACEDIV] as the trace clock source. 0 MCGOUTCLK, divided by the TRACECLK fractional divider as configured by SIM_CLKDIV4[TRACEFRAC, TRACEDIV] 1 Core/system clock
11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9–8 FBSL	FlexBus security level If flash security is enabled, then this field affects what CPU operations can access off-chip via the FlexBus or SDRAMinterface. This field has no effect if flash security is not enabled. 00 All off-chip accesses (instruction and data) via the FlexBus or SDRAM are disallowed. 01 All off-chip accesses (instruction and data) via the FlexBus or SDRAM are disallowed. 10 Off-chip instruction accesses are disallowed. Data accesses are allowed. 11 Off-chip instruction accesses and data accesses are allowed.
7–5 CLKOUTSEL	CLKOUT select Selects the clock to output on the CLKOUT pin. 000 FlexBus CLKOUT 001 Reserved 010 Flash clock 011 LPO clock (1 kHz) 100 MCGIRCLK 101 RTC 32.768kHz clock 110 OSCERCLK0 111 IRC 48 MHz clock
4 RTCCLKOUTSEL	RTC clock out select Selects either the RTC 1 Hz clock or the 32.768kHz clock to be output on the RTC_CLKOUT pin. 0 RTC 1 Hz clock is output on the RTC_CLKOUT pin. 1 RTC 32.768kHz clock is output on the RTC_CLKOUT pin.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

14.2.4 System Options Register 4 (SIM_SOPT4)

Address: 4004_7000h base + 100Ch offset = 4004_800Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	FTM3TRG1SRC	FTM3TRG0SRC	FTM0TRG1SRC	FTM0TRG0SRC	FTM3CLKSEL	FTM2CLKSEL	FTM1CLKSEL	FTM0CLKSEL	0	FTM2CH1SRC	FTM2CH0SRC		FTM1CH0SRC		0	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0			FTM3FLT0	0			FTM2FLT0	0			FTM1FLT0	0	0	FTM0FLT1	FTM0FLT0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SIM_SOPT4 field descriptions

Field	Description
31 FTM3TRG1SRC	FlexTimer 3 Hardware Trigger 1 Source Select Selects the source of FTM3 hardware trigger 1. 0 Reserved 1 FTM2 channel match drives FTM3 hardware trigger 1
30 FTM3TRG0SRC	FlexTimer 3 Hardware Trigger 0 Source Select Selects the source of FTM3 hardware trigger 0. 0 Reserved 1 FTM1 channel match drives FTM3 hardware trigger 0
29 FTM0TRG1SRC	FlexTimer 0 Hardware Trigger 1 Source Select Selects the source of FTM0 hardware trigger 1. 0 PDB output trigger 1 drives FTM0 hardware trigger 1 1 FTM2 channel match drives FTM0 hardware trigger 1
28 FTM0TRG0SRC	FlexTimer 0 Hardware Trigger 0 Source Select Selects the source of FTM0 hardware trigger 0. 0 HSCMP0 output drives FTM0 hardware trigger 0 1 FTM1 channel match drives FTM0 hardware trigger 0
27 FTM3CLKSEL	FlexTimer 3 External Clock Pin Select Selects the external pin used to drive the clock to the FTM3 module.

Table continues on the next page...

SIM_SOPT4 field descriptions (continued)

Field	Description
	NOTE: The selected pin must also be configured for the FTM3 module external clock function through the appropriate pin control register in the port control module. 0 FTM3 external clock driven by FTM_CLK0 pin. 1 FTM3 external clock driven by FTM_CLK1 pin.
26 FTM2CLKSEL	FlexTimer 2 External Clock Pin Select Selects the external pin used to drive the clock to the FTM2 module. **NOTE:** The selected pin must also be configured for the FTM2 module external clock function through the appropriate pin control register in the port control module. 0 FTM2 external clock driven by FTM_CLK0 pin. 1 FTM2 external clock driven by FTM_CLK1 pin.
25 FTM1CLKSEL	FTM1 External Clock Pin Select Selects the external pin used to drive the clock to the FTM1 module. **NOTE:** The selected pin must also be configured for the FTM external clock function through the appropriate pin control register in the port control module. 0 FTM_CLK0 pin 1 FTM_CLK1 pin
24 FTM0CLKSEL	FlexTimer 0 External Clock Pin Select Selects the external pin used to drive the clock to the FTM0 module. **NOTE:** The selected pin must also be configured for the FTM external clock function through the appropriate pin control register in the port control module. 0 FTM_CLK0 pin 1 FTM_CLK1 pin
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 FTM2CH1SRC	FTM2 channel 1 input capture source select 0 FTM2_CH1 signal 1 Exclusive OR of FTM2_CH1, FTM2_CH0 and FTM1_CH1.
21–20 FTM2CH0SRC	FTM2 channel 0 input capture source select Selects the source for FTM2 channel 0 input capture. **NOTE:** When the FTM is not in input capture mode, clear this field. 00 FTM2_CH0 signal 01 CMP0 output 10 CMP1 output 11 Reserved
19–18 FTM1CH0SRC	FTM1 channel 0 input capture source select Selects the source for FTM1 channel 0 input capture. **NOTE:** When the FTM is not in input capture mode, clear this field.

Table continues on the next page...

SIM_SOPT4 field descriptions (continued)

Field	Description
	00 FTM1_CH0 signal 01 CMP0 output 10 CMP1 output 11 USB start of frame pulse
17–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12 FTM3FLT0	FTM3 Fault 0 Select Selects the source of FTM3 fault 0. **NOTE:** The pin source for fault 0 must be configured for the FTM module fault function through the appropriate PORTx pin control register. 0 FTM3_FLT0 pin 1 CMP0 out
11–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 FTM2FLT0	FTM2 Fault 0 Select Selects the source of FTM2 fault 0. **NOTE:** The pin source for fault 0 must be configured for the FTM module fault function through the appropriate PORTx pin control register. 0 FTM2_FLT0 pin 1 CMP0 out
7–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 FTM1FLT0	FTM1 Fault 0 Select Selects the source of FTM1 fault 0. **NOTE:** The pin source for fault 0 must be configured for the FTM module fault function through the appropriate pin control register in the port control module. 0 FTM1_FLT0 pin 1 CMP0 out
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 FTM0FLT1	FTM0 Fault 1 Select Selects the source of FTM0 fault 1. **NOTE:** The pin source for fault 1 must be configured for the FTM module fault function through the appropriate pin control register in the port control module. 0 FTM0_FLT1 pin 1 CMP1 out
0 FTM0FLT0	FTM0 Fault 0 Select

Table continues on the next page...

SIM_SOPT4 field descriptions (continued)

Field	Description
	Selects the source of FTM0 fault 0. **NOTE:** The pin source for fault 0 must be configured for the FTM module fault function through the appropriate pin control register in the port control module. 0 FTM0_FLT0 pin 1 CMP0 out

14.2.5 System Options Register 5 (SIM_SOPT5)

Address: 4004_7000h base + 1010h offset = 4004_8010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								LPUART1RXSRC		LPUART1TXSRC		LPUART0RXSRC		LPUART0TXSRC		0															
W									RC		RC		RC		RC																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SIM_SOPT5 field descriptions

Field	Description
31–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23–22 LPUART1RXSRC	LPUART1 receive data source select Selects the source for the LPUART1 receive data. 00 LPUART1_RX pin 01 CMP0 output 10 CMP1 output 11 Reserved
21–20 LPUART1TXSRC	LPUART1 transmit data source select Selects the source for the LPUART0 transmit data. 00 LPUART1_TX pin 01 LPUART1_TX pin modulated with TPM1 channel 0 output 10 LPUART0_TX pin modulated with TPM2 channel 0 output 11 Reserved
19–18 LPUART0RXSRC	LPUART0 receive data source select Selects the source for the LPUART0 receive data. 00 LPUART0_RX pin 01 CMP0 output

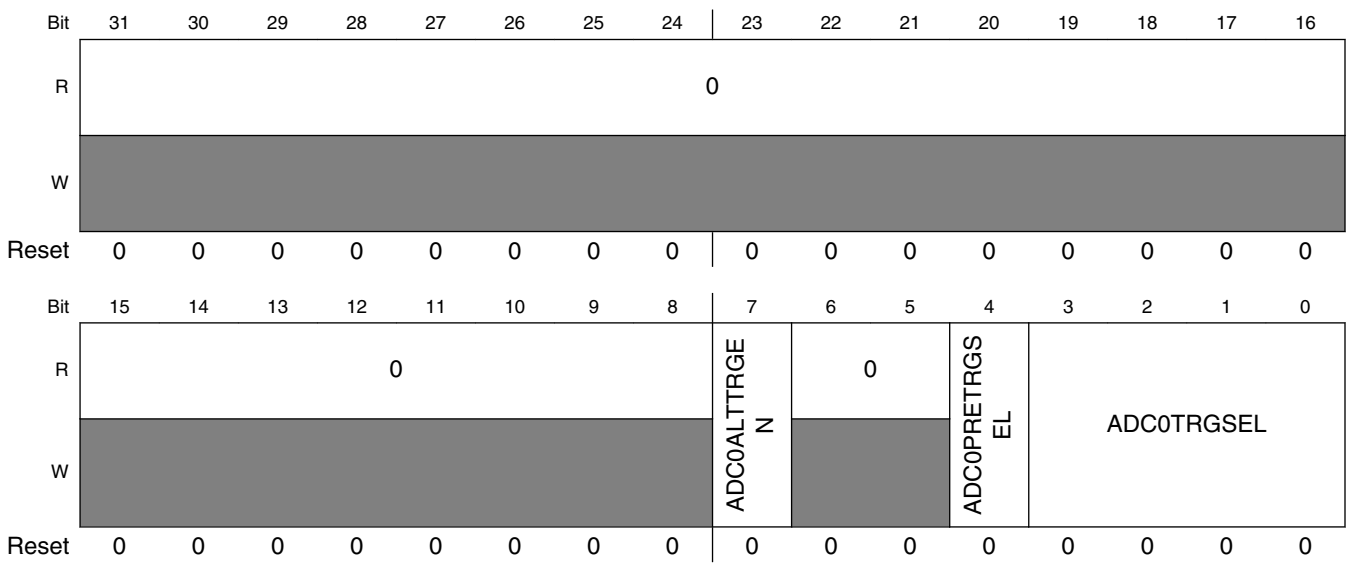
Table continues on the next page...

SIM_SOPT5 field descriptions (continued)

Field	Description
	10 CMP1 output 11 Reserved
17–16 LPUART0TXSRC	LPUART0 transmit data source select Selects the source for the LPUART0 transmit data. 00 LPUART0_TX pin 01 LPUART0_TX pin modulated with TPM1 channel 0 output 10 LPUART0_TX pin modulated with TPM2 channel 0 output 11 Reserved
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

14.2.6 System Options Register 7 (SIM_SOPT7)

Address: 4004_7000h base + 1018h offset = 4004_8018h



SIM_SOPT7 field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 ADC0ALTTRGEN	ADC0 alternate trigger enable Enable alternative conversion triggers for ADC0.

Table continues on the next page...

SIM_SOPT7 field descriptions (continued)

Field	Description
	0 PDB trigger selected for ADC0. 1 Alternate trigger selected for ADC0.
6–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 ADC0PRETRGSEL	ADC0 pretrigger select Selects the ADC0 pre-trigger source when alternative triggers are enabled through ADC0ALTTRGEN. This field is not used when the TPM trigger source is selected. 0 Pre-trigger A 1 Pre-trigger B
ADC0TRGSEL	ADC0 trigger select Selects the ADC0 trigger source when alternative triggers are functional in stop and VLPS modes. . 0000 PDB external trigger pin input (PDB0_EXTRG) 0001 High speed comparator 0 output 0010 High speed comparator 1 output 0011 Reserved 0100 PIT trigger 0 0101 PIT trigger 1 0110 PIT trigger 2 0111 PIT trigger 3 1000 FTM0 trigger 1001 FTM1 trigger 1010 FTM2 trigger 1011 FTM3 trigger 1100 RTC alarm 1101 RTC seconds 1110 Low-power timer (LPTMR) trigger 1111 TPM1 channel 0 (A pretrigger) and channel 1 (B pretrigger)

14.2.7 System Options Register 8 (SIM_SOPT8)

Address: 4004_7000h base + 101Ch offset = 4004_801Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	FTM3OCH7SRC	FTM3OCH6SRC	FTM3OCH5SRC	FTM3OCH4SRC	FTM3OCH3SRC	FTM3OCH2SRC	FTM3OCH1SRC	FTM3OCH0SRC	FTM0OCH7SRC	FTM0OCH6SRC	FTM0OCH5SRC	FTM0OCH4SRC	FTM0OCH3SRC	FTM0OCH2SRC	FTM0OCH1SRC	FTM0OCH0SRC
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												FTM3SYNCBIT	FTM2SYNCBIT	FTM1SYNCBIT	FTM0SYNCBIT
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SIM_SOPT8 field descriptions

Field	Description
31 FTM3OCH7SRC	FTM3 channel 7 output source 0 FTM3_CH7 pin is output of FTM3 channel 7 output 1 FTM3_CH7 pin is output of FTM3 channel 7 output modulated by FTM2 channel 1 output.
30 FTM3OCH6SRC	FTM3 channel 6 output source 0 FTM3_CH6 pin is output of FTM3 channel 6 output 1 FTM3_CH6 pin is output of FTM3 channel 6 output modulated by FTM2 channel 1 output.
29 FTM3OCH5SRC	FTM3 channel 5 output source 0 FTM3_CH5 pin is output of FTM3 channel 5 output 1 FTM3_CH5 pin is output of FTM3 channel 5 output modulated by FTM2 channel 1 output.
28 FTM3OCH4SRC	FTM3 channel 4 output source 0 FTM3_CH4 pin is output of FTM3 channel 4 output 1 FTM3_CH4 pin is output of FTM3 channel 4 output modulated by FTM2 channel 1 output.
27 FTM3OCH3SRC	FTM3 channel 3 output source 0 FTM3_CH3 pin is output of FTM3 channel 3 output 1 FTM3_CH3 pin is output of FTM3 channel 3 output modulated by FTM2 channel 1 output.
26 FTM3OCH2SRC	FTM3 channel 2 output source 0 FTM3_CH2 pin is output of FTM3 channel 2 output 1 FTM3_CH2 pin is output of FTM3 channel 2 output modulated by FTM2 channel 1 output.
25 FTM3OCH1SRC	FTM3 channel 1 output source

Table continues on the next page...

SIM_SOPT8 field descriptions (continued)

Field	Description
	0 FTM3_CH1 pin is output of FTM3 channel 1 output 1 FTM3_CH1 pin is output of FTM3 channel 1 output modulated by FTM2 channel 1 output.
24 FTM3OCH0SRC	FTM3 channel 0 output source 0 FTM3_CH0 pin is output of FTM3 channel 0 output 1 FTM3_CH0 pin is output of FTM3 channel 0 output modulated by FTM2 channel 1 output.
23 FTM0OCH7SRC	FTM0 channel 7 output source 0 FTM0_CH7 pin is output of FTM0 channel 7 output 1 FTM0_CH7 pin is output of FTM0 channel 7 output, modulated by FTM1 channel 1 output
22 FTM0OCH6SRC	FTM0 channel 6 output source 0 FTM0_CH6 pin is output of FTM0 channel 6 output 1 FTM0_CH6 pin is output of FTM0 channel 6 output, modulated by FTM1 channel 1 output
21 FTM0OCH5SRC	FTM0 channel 5 output source 0 FTM0_CH5 pin is output of FTM0 channel 5 output 1 FTM0_CH5 pin is output of FTM0 channel 5 output, modulated by FTM1 channel 1 output
20 FTM0OCH4SRC	FTM0 channel 4 output source 0 FTM0_CH4 pin is output of FTM0 channel 4 output 1 FTM0_CH4 pin is output of FTM0 channel 4 output, modulated by FTM1 channel 1 output
19 FTM0OCH3SRC	FTM0 channel 3 output source 0 FTM0_CH3 pin is output of FTM0 channel 3 output 1 FTM0_CH3 pin is output of FTM0 channel 3 output, modulated by FTM1 channel 1 output
18 FTM0OCH2SRC	FTM0 channel 2 output source 0 FTM0_CH2 pin is output of FTM0 channel 2 output 1 FTM0_CH2 pin is output of FTM0 channel 2 output, modulated by FTM1 channel 1 output
17 FTM0OCH1SRC	FTM0 channel 1 output source 0 FTM0_CH1 pin is output of FTM0 channel 1 output 1 FTM0_CH1 pin is output of FTM0 channel 1 output, modulated by FTM1 channel 1 output
16 FTM0OCH0SRC	FTM0 channel 0 output source 0 FTM0_CH0 pin is output of FTM0 channel 0 output 1 FTM0_CH0 pin is output of FTM0 channel 0 output, modulated by FTM1 channel 1 output
15–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 FTM3SYNCBIT	FTM3 Hardware Trigger 0 Software Synchronization 0 No effect. 1 Write 1 to assert the TRIG0 input to FTM3, software must clear this bit to allow other trigger sources to assert.
2 FTM2SYNCBIT	FTM2 Hardware Trigger 0 Software Synchronization

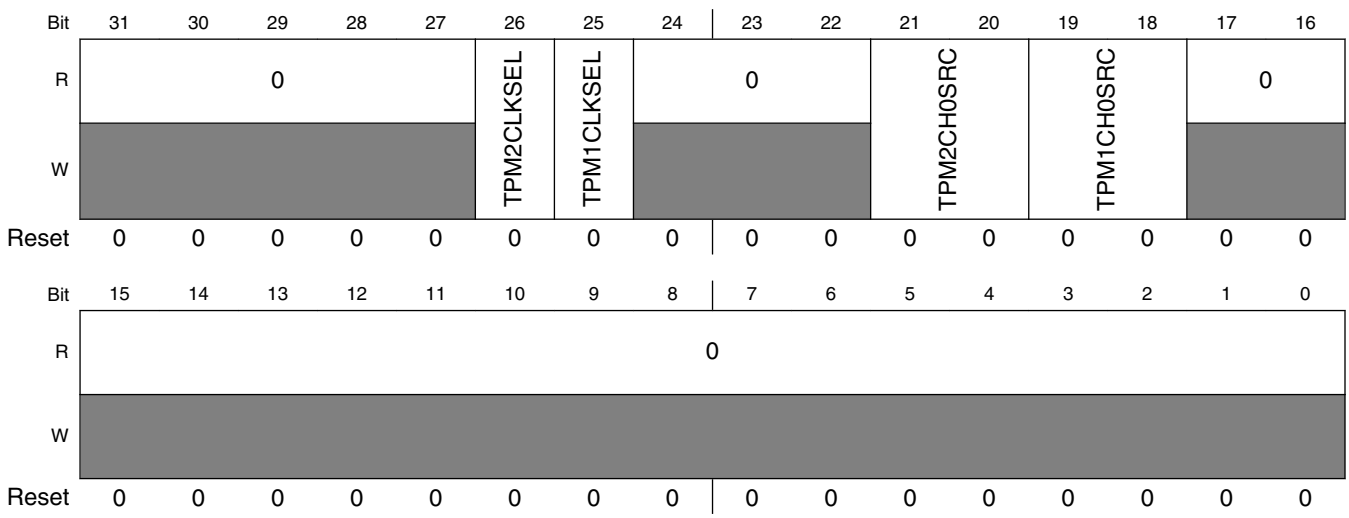
Table continues on the next page...

SIM_SOPT8 field descriptions (continued)

Field	Description
	0 No effect. 1 Write 1 to assert the TRIG0 input to FTM2, software must clear this bit to allow other trigger sources to assert.
1 FTM1SYNCBIT	FTM1 Hardware Trigger 0 Software Synchronization 0 No effect. 1 Write 1 to assert the TRIG0 input to FTM1, software must clear this bit to allow other trigger sources to assert.
0 FTM0SYNCBIT	FTM0 Hardware Trigger 0 Software Synchronization 0 No effect 1 Write 1 to assert the TRIG0 input to FTM0, software must clear this bit to allow other trigger sources to assert.

14.2.8 System Options Register 9 (SIM_SOPT9)

Address: 4004_7000h base + 1020h offset = 4004_8020h



SIM_SOPT9 field descriptions

Field	Description
31–27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 TPM2CLKSEL	TPM2 External Clock Pin Select Selects the external pin used to drive the clock to the TPM2 module. **NOTE:** The selected pin must also be configured for the TPM external clock function through the appropriate pin control register in the port control module. 0 TPM_CLKIN0 pin 1 TPM_CLKIN1 pin

Table continues on the next page...

SIM_SOPT9 field descriptions (continued)

Field	Description
25 TPM1CLKSEL	TPM1 External Clock Pin Select Selects the external pin used to drive the clock to the TPM1 module. **NOTE:** The selected pin must also be configured for the TPM external clock function through the appropriate pin control register in the port control module. 0 TPM_CLKIN0 pin 1 TPM_CLKIN1 pin
24–22 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
21–20 TPM2CH0SRC	TPM2 channel 0 input capture source select Selects the source for TPM2 channel 0 input capture. **NOTE:** When the TPM is not in input capture mode, clear this field. 00 TPM2_CH0 signal 01 CMP0 output 10 CMP1 output 11 Reserved
19–18 TPM1CH0SRC	TPM1 channel 0 input capture source select Selects the source for TPM1 channel 0 input capture. **NOTE:** When the TPM is not in input capture mode, clear this field. 00 TPM1_CH0 signal 01 CMP0 output 10 CMP1 output 11 Reserved
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

14.2.9 System Device Identification Register (SIM_SDID)

Address: 4004_7000h base + 1024h offset = 4004_8024h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	FAMILYID				SUBFAMID				SERIESID				0				REVID				DIEID					FAMID			PINID			
W																																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	0	0	0	0	x*	x*	x*	x*	1	0	1	1	1	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SIM_SDID field descriptions

Field	Description
31–28 FAMILYID	Kinetis Family ID Specifies the Kinetis family of the device. 0000 K0x Family 0001 K1x Family 0010 K2x Family 0011 K3x Family 0100 K4x Family 0110 K6x Family 0111 K7x Family 1000 K8x Family
27–24 SUBFAMID	Kinetis Sub-Family ID Specifies the Kinetis sub-family of the device. 0000 Kx0 Subfamily 0001 Kx1 Subfamily (tamper detect) 0010 Kx2 Subfamily 0011 Kx3 Subfamily (tamper detect) 0100 Kx4 Subfamily 0101 Kx5 Subfamily (tamper detect) 0110 Kx6 Subfamily
23–20 SERIESID	Kinetis Series ID Specifies the Kinetis series of the device. 0000 Kinetis K series 0001 Kinetis L series 0101 Kinetis W series 0110 Kinetis V series
19–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–12 REVID	Device revision number Specifies the silicon implementation number for the device.
11–7 DIEID	Device Die ID Specifies the silicon feature set identication number for the device.
6–4 FAMID	Kinetis family identification This field is maintained for compatibility only, but has been superceded by the SERIESID, FAMILYID and SUBFAMID fields in this register. 000 K1x Family (without tamper) 001 K2x Family (without tamper) 010 K3x Family or K1x/K6x Family (with tamper) 011 K4x Family or K2x Family (with tamper) 100 K6x Family (without tamper) 101 K7x Family

Table continues on the next page...

SIM_SDID field descriptions (continued)

Field	Description
	110 Reserved 111 Reserved
PINID	Pincount identification Specifies the pincount of the device. 0000 Reserved 0001 Reserved 0010 32-pin 0011 Reserved 0100 48-pin 0101 64-pin 0110 80-pin 0111 81-pin or 121-pin 1000 100-pin 1001 121-pin 1010 144-pin 1011 Custom pinout (WLCSP) 1100 169-pin 1101 Reserved 1110 256-pin 1111 Reserved

14.2.10 System Clock Gating Control Register 1 (SIM_SCGC1)

Address: 4004_7000h base + 1028h offset = 4004_8028h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0							0	0		0	0				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				0	0	0		I2C3	I2C2	0					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SIM_SCGC1 field descriptions

Field	Description
31–25 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23–22 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

SIM_SCGC1 field descriptions (continued)

Field	Description
21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 I2C3	I2C3 Clock Gate Control This bit controls the clock gate to the I2C3 module. 0 Clock disabled 1 Clock enabled
6 I2C2	I2C2 Clock Gate Control This bit controls the clock gate to the I2C2 module. 0 Clock disabled 1 Clock enabled
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

14.2.11 System Clock Gating Control Register 2 (SIM_SCGC2)

Address: 4004_7000h base + 102Ch offset = 4004_802Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	FLEXIO	0				QSPI	0		LPUART4	EMVSIM1	EMVSIM0	0			LTC	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		0	DAC0	0	TPM2	TPM1	0	LPUART3	LPUART2	LPUART1	LPUART0	0			0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SIM_SCGC2 field descriptions

Field	Description
31 FLEXIO	FlexIO Clock Gate Control This bit controls the clock gate to the FlexIO module. 0 Clock disabled 1 Clock enabled
30–27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 QSPI	QSPI Clock Gate Control This bit controls the clock gate to the QuadSPI module. 0 Clock disabled 1 Clock enabled
25–23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 LPUART4	LPUART4 Clock Gate Control This bit controls the clock gate to the LPUART4 module. 0 Clock disabled 1 Clock enabled
21 EMVSIM1	EMVSIM1 Clock Gate Control This bit controls the clock gate to the EMVSIM1 module. 0 Clock disabled 1 Clock enabled
20 EMVSIM0	EMVSIM0 Clock Gate Control This bit controls the clock gate to the EMVSIM0 module. 0 Clock disabled 1 Clock enabled
19–18 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
17 LTC	LTC Clock Gate Control This bit controls the clock gate to the LTC module. 0 Clock disabled 1 Clock enabled
16–14 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12 DAC0	DAC0 Clock Gate Control This bit controls the clock gate to the DAC0 module.

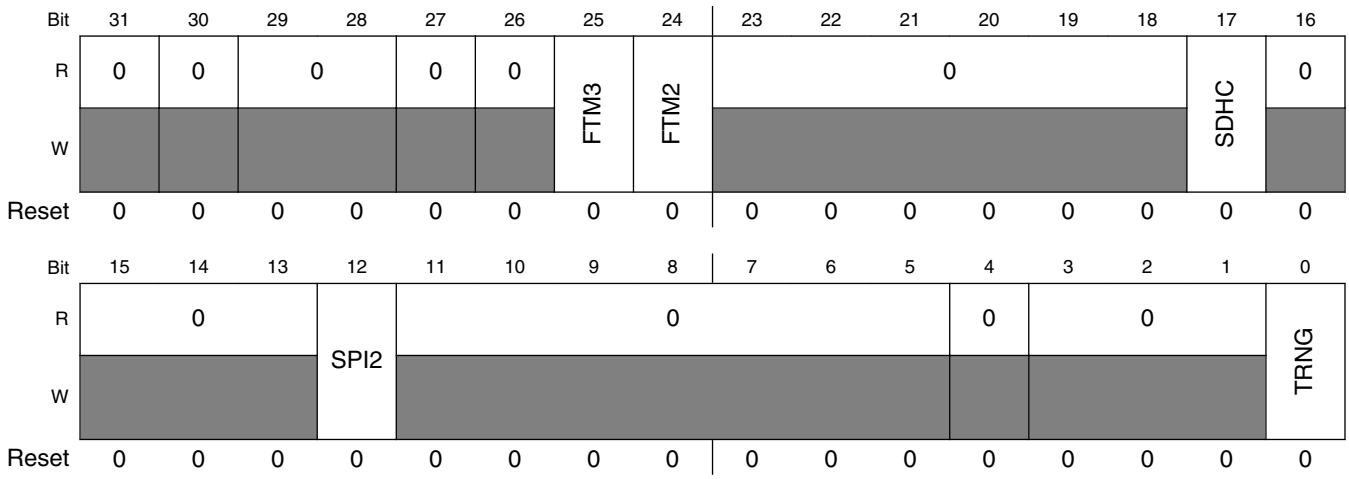
Table continues on the next page...

SIM_SCGC2 field descriptions (continued)

Field	Description
	0 Clock disabled 1 Clock enabled
11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10 TPM2	TPM2 Clock Gate Control This bit controls the clock gate to the TPM2 module. 0 Clock disabled 1 Clock enabled
9 TPM1	TPM1 Clock Gate Control This bit controls the clock gate to the TPM1 module. 0 Clock disabled 1 Clock enabled
8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 LPUART3	LPUART3 Clock Gate Control This bit controls the clock gate to the LPUART3 module. 0 Clock disabled 1 Clock enabled
6 LPUART2	LPUART2 Clock Gate Control This bit controls the clock gate to the LPUART2 module. 0 Clock disabled 1 Clock enabled
5 LPUART1	LPUART1 Clock Gate Control This bit controls the clock gate to the LPUART1 module. 0 Clock disabled 1 Clock enabled
4 LPUART0	LPUART0 Clock Gate Control This bit controls the clock gate to the LPUART0 module. 0 Clock disabled 1 Clock enabled
3–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

14.2.12 System Clock Gating Control Register 3 (SIM_SCGC3)

Address: 4004_7000h base + 1030h offset = 4004_8030h



SIM_SCGC3 field descriptions

Field	Description
31 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
30 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
29–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25 FTM3	FTM3 Clock Gate Control This bit controls the clock gate to the FTM3 module. 0 Clock disabled 1 Clock enabled
24 FTM2	FTM2 Clock Gate Control This bit controls the clock gate to the FTM2 module. 0 Clock disabled 1 Clock enabled
23–18 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
17 SDHC	SDHC Clock Gate Control This bit controls the clock gate to the SDHC module.

Table continues on the next page...

SIM_SCGC3 field descriptions (continued)

Field	Description
	0 Clock disabled 1 Clock enabled
16–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12 SPI2	SPI2 Clock Gate Control This bit controls the clock gate to the SPI2 module. 0 Clock disabled 1 Clock enabled
11–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 TRNG	TRNG Clock Gate Control This bit controls the clock gate to the TRNG module. 0 Clock disabled 1 Clock enabled

14.2.13 System Clock Gating Control Register 4 (SIM_SCGC4)

Address: 4004_7000h base + 1034h offset = 4004_8034h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	1				0							VREF	CMP	USBOTG	0	
W																
Reset	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		0	0	0	0	0		I2C1	I2C0	1		0	CMT	EWM	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

SIM_SCGC4 field descriptions

Field	Description
31–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.

Table continues on the next page...

SIM_SCGC4 field descriptions (continued)

Field	Description
27–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20 VREF	VREF Clock Gate Control This bit controls the clock gate to the VREF module. 0 Clock disabled 1 Clock enabled
19 CMP	Comparator Clock Gate Control This bit controls the clock gate to the comparator module. 0 Clock disabled 1 Clock enabled
18 USBOTG	USB Clock Gate Control This bit controls the clock gate to the USB module. 0 Clock disabled 1 Clock enabled
17–14 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 I2C1	I2C1 Clock Gate Control This bit controls the clock gate to the I^2C1 module. 0 Clock disabled 1 Clock enabled
6 I2C0	I2C0 Clock Gate Control This bit controls the clock gate to the I^2C0 module. 0 Clock disabled 1 Clock enabled
5–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

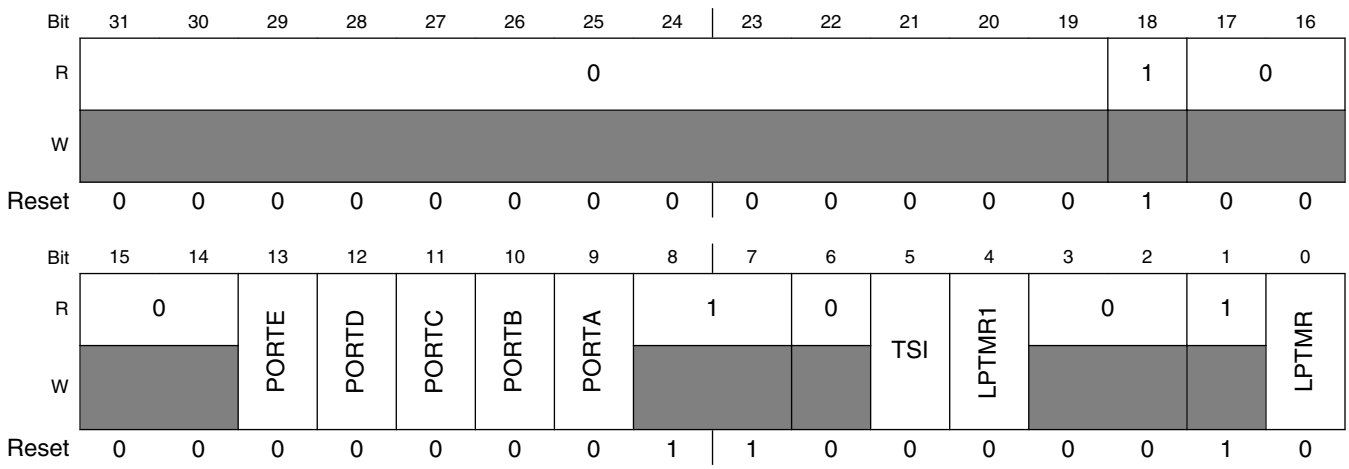
Table continues on the next page...

SIM_SCGC4 field descriptions (continued)

Field	Description
2 CMT	CMT Clock Gate Control This bit controls the clock gate to the CMT module. 0 Clock disabled 1 Clock enabled
1 EWM	EWM Clock Gate Control This bit controls the clock gate to the EWM module. 0 Clock disabled 1 Clock enabled
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

14.2.14 System Clock Gating Control Register 5 (SIM_SCGC5)

Address: 4004_7000h base + 1038h offset = 4004_8038h



SIM_SCGC5 field descriptions

Field	Description
31–19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
17–14 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
13 PORTE	Port E Clock Gate Control This bit controls the clock gate to the Port E module.

Table continues on the next page...

SIM_SCGC5 field descriptions (continued)

Field	Description
	0 Clock disabled 1 Clock enabled
12 PORTD	Port D Clock Gate Control This bit controls the clock gate to the Port D module. 0 Clock disabled 1 Clock enabled
11 PORTC	Port C Clock Gate Control This bit controls the clock gate to the Port C module. 0 Clock disabled 1 Clock enabled
10 PORTB	Port B Clock Gate Control This bit controls the clock gate to the Port B module. 0 Clock disabled 1 Clock enabled
9 PORTA	Port A Clock Gate Control This bit controls the clock gate to the Port A module. 0 Clock disabled 1 Clock enabled
8–7 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 TSI	TSI Clock Gate Control This bit controls the clock gate to the TSI module. 0 Clock disabled 1 Clock enabled
4 LPTMR1	LPTMR1 Clock Gate Control This bit controls software access to the LPTMR1 module. 0 Access disabled 1 Access enabled
3–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
0 LPTMR	Low Power Timer Access Control This bit controls software access to the Low Power Timer module.

Table continues on the next page...

SIM_SCGC5 field descriptions (continued)

Field	Description
	0 Access disabled 1 Access enabled

14.2.15 System Clock Gating Control Register 6 (SIM_SCGC6)

DAC0, FTM2 can be accessed through both AIPS0 and AIPS1. When accessing through AIPS1, define the clock gate control bits in the SCGC2 and SCGC3. When accessing through AIPS0, define the clock gate control bits in SCGC6. See the Chip Configuration chapter for the base addresses of FTM2, and DAC0 accessed via AIPS0 and AIPS1.

Address: 4004_7000h base + 103Ch offset = 4004_803Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DAC0	1	RTC	0	ADC0	FTM2	FTM1	FTM0	PIT	PDB	USBDCD	0		CRC	0	
W																
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	I2S	0	SPI1	SPI0	0		0		0			0	0		DMAMUX	FTF
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

SIM_SCGC6 field descriptions

Field	Description
31 DAC0	DAC0 Clock Gate Control This bit controls the clock gate to the DAC0 module. 0 Clock disabled 1 Clock enabled
30 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
29 RTC	RTC Access Control This bit controls software access and interrupts to the RTC module. 0 Access and interrupts disabled 1 Access and interrupts enabled

Table continues on the next page...

SIM_SCGC6 field descriptions (continued)

Field	Description
28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27 ADC0	ADC0 Clock Gate Control This bit controls the clock gate to the ADC0 module. 0 Clock disabled 1 Clock enabled
26 FTM2	FTM2 Clock Gate Control This bit controls the clock gate to the FTM2 module. 0 Clock disabled 1 Clock enabled
25 FTM1	FTM1 Clock Gate Control This bit controls the clock gate to the FTM1 module. 0 Clock disabled 1 Clock enabled
24 FTM0	FTM0 Clock Gate Control This bit controls the clock gate to the FTM0 module. 0 Clock disabled 1 Clock enabled
23 PIT	PIT Clock Gate Control This bit controls the clock gate to the PIT module. 0 Clock disabled 1 Clock enabled
22 PDB	PDB Clock Gate Control This bit controls the clock gate to the PDB module. 0 Clock disabled 1 Clock enabled
21 USBDCD	USB DCD Clock Gate Control This bit controls the clock gate to the USB DCD module. 0 Clock disabled 1 Clock enabled
20–19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18 CRC	CRC Clock Gate Control This bit controls the clock gate to the CRC module.

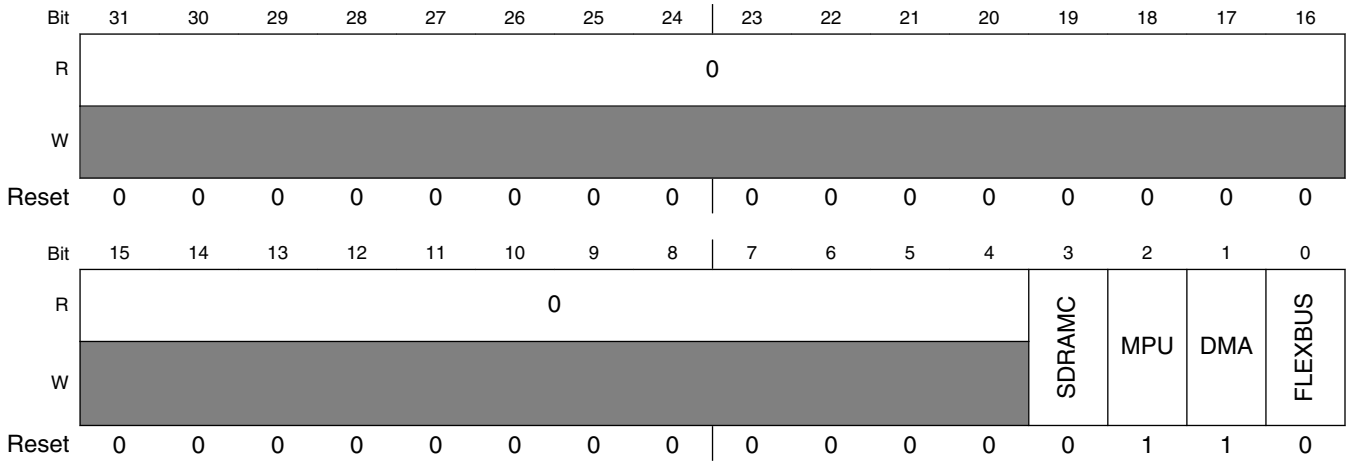
Table continues on the next page...

SIM_SCGC6 field descriptions (continued)

Field	Description
	0 Clock disabled 1 Clock enabled
17–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15 I2S	I2S Clock Gate Control This bit controls the clock gate to the I ^{2} S module. 0 Clock disabled 1 Clock enabled
14 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
13 SPI1	SPI1 Clock Gate Control This bit controls the clock gate to the SPI1 module. 0 Clock disabled 1 Clock enabled
12 SPI0	SPI0 Clock Gate Control This bit controls the clock gate to the SPI0 module. 0 Clock disabled 1 Clock enabled
11–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 DMAMUX	DMA Mux Clock Gate Control This bit controls the clock gate to the DMA Mux module. 0 Clock disabled 1 Clock enabled
0 FTF	Flash Memory Clock Gate Control This bit controls the clock gate to the flash memory. Flash reads are still supported while the flash memory is clock gated, but entry into low power modes is blocked. 0 Clock disabled 1 Clock enabled

14.2.16 System Clock Gating Control Register 7 (SIM_SCGC7)

Address: 4004_7000h base + 1040h offset = 4004_8040h



SIM_SCGC7 field descriptions

Field	Description
31–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 SDRAMC	SDRAMC Clock Gate Control This bit controls the clock gate to the SDRAMC module. 0 Clock disabled 1 Clock enabled
2 MPU	MPU Clock Gate Control This bit controls the clock gate to the MPU module. 0 Clock disabled 1 Clock enabled
1 DMA	DMA Clock Gate Control This bit controls the clock gate to the DMA module. 0 Clock disabled 1 Clock enabled
0 FLEXBUS	FlexBus Clock Gate Control This bit controls the clock gate to the FlexBus module. 0 Clock disabled 1 Clock enabled

14.2.17 System Clock Divider Register 1 (SIM_CLKDIV1)

When updating CLKDIV1, update all fields using the one write command. Attempting to write an invalid clock ratio to the CLKDIV1 register will cause the write to be ignored. The maximum divide ratio that can be programmed between core/system clock and the other divided clocks is divide by 8. When OUTDIV1 equals 0000 (divide by 1), the other dividers cannot be set higher than 0111 (divide by 8).

NOTE

The CLKDIV1 register cannot be written to when the device is in VLPR mode.

Address: 4004_7000h base + 1044h offset = 4004_8044h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	OUTDIV1				OUTDIV2				OUTDIV3				OUTDIV4				0															
W																																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	1*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

SIM_CLKDIV1 field descriptions

Field	Description
31–28 OUTDIV1	Clock 1 output divider value This field sets the divide value for the core/system clock from MCGOUTCLK. At the end of reset, it is loaded with either 0000 or 0111 depending on FTF_FOPT[LPBOOT]. 0000 Divide-by-1. 0001 Divide-by-2. 0010 Divide-by-3. 0011 Divide-by-4. 0100 Divide-by-5. 0101 Divide-by-6. 0110 Divide-by-7. 0111 Divide-by-8. 1000 Divide-by-9. 1001 Divide-by-10. 1010 Divide-by-11. 1011 Divide-by-12. 1100 Divide-by-13. 1101 Divide-by-14. 1110 Divide-by-15. 1111 Divide-by-16.
27–24 OUTDIV2	Clock 2 output divider value This field sets the divide value for the bus clock from MCGOUTCLK. At the end of reset, it is loaded with either 0000 or 0111 depending on FTF_FOPT[LPBOOT]. The bus clock frequency must be an integer divide of the core/system clock frequency.

Table continues on the next page...

SIM_CLKDIV1 field descriptions (continued)

Field	Description
	0000 Divide-by-1. 0001 Divide-by-2. 0010 Divide-by-3. 0011 Divide-by-4. 0100 Divide-by-5. 0101 Divide-by-6. 0110 Divide-by-7. 0111 Divide-by-8. 1000 Divide-by-9. 1001 Divide-by-10. 1010 Divide-by-11. 1011 Divide-by-12. 1100 Divide-by-13. 1101 Divide-by-14. 1110 Divide-by-15. 1111 Divide-by-16.
23–20 OUTDIV3	Clock 3 output divider value This field sets the divide value for the FlexBus clock (external pin FB_CLK) from MCGOUTCLK. At the end of reset, it is loaded with either 0001 or 1111 depending on FTF_FOPT[LPBOOT]. The FlexBus clock frequency must be an integer divide of the system clock frequency. 0000 Divide-by-1. 0001 Divide-by-2. 0010 Divide-by-3. 0011 Divide-by-4. 0100 Divide-by-5. 0101 Divide-by-6. 0110 Divide-by-7. 0111 Divide-by-8. 1000 Divide-by-9. 1001 Divide-by-10. 1010 Divide-by-11. 1011 Divide-by-12. 1100 Divide-by-13. 1101 Divide-by-14. 1110 Divide-by-15. 1111 Divide-by-16.
19–16 OUTDIV4	Clock 4 output divider value This field sets the divide value for the flash clock from MCGOUTCLK. At the end of reset, it is loaded with either 0001 or 1111 depending on FTF_FOPT[LPBOOT]. The flash clock frequency must be an integer divide of the system clock frequency. 0000 Divide-by-1. 0001 Divide-by-2. 0010 Divide-by-3. 0011 Divide-by-4. 0100 Divide-by-5.

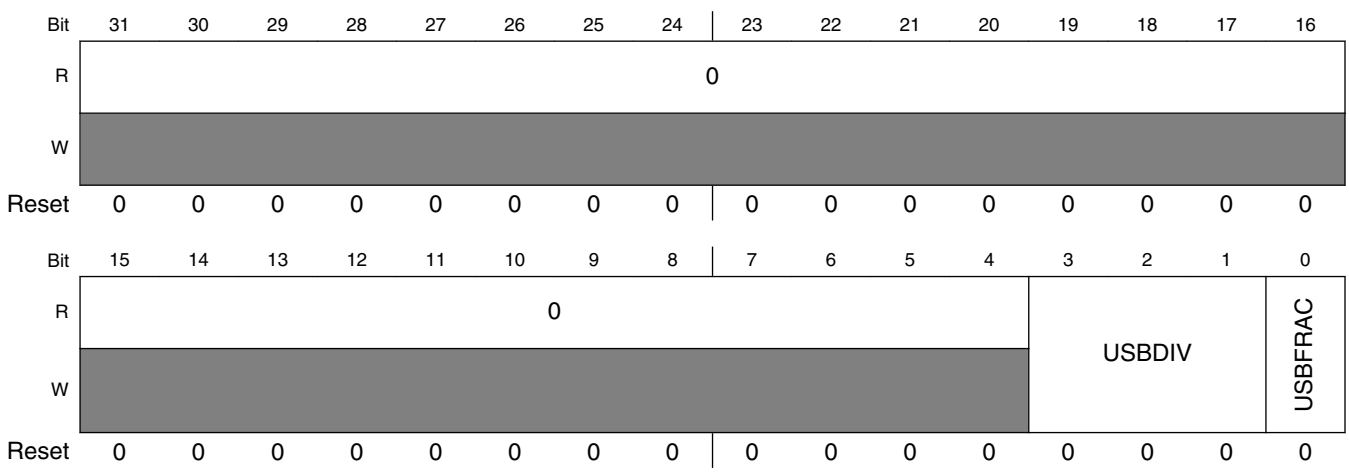
Table continues on the next page...

SIM_CLKDIV1 field descriptions (continued)

Field	Description
	0101 Divide-by-6. 0110 Divide-by-7. 0111 Divide-by-8. 1000 Divide-by-9. 1001 Divide-by-10. 1010 Divide-by-11. 1011 Divide-by-12. 1100 Divide-by-13. 1101 Divide-by-14. 1110 Divide-by-15. 1111 Divide-by-16.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

14.2.18 System Clock Divider Register 2 (SIM_CLKDIV2)

Address: 4004_7000h base + 1048h offset = 4004_8048h

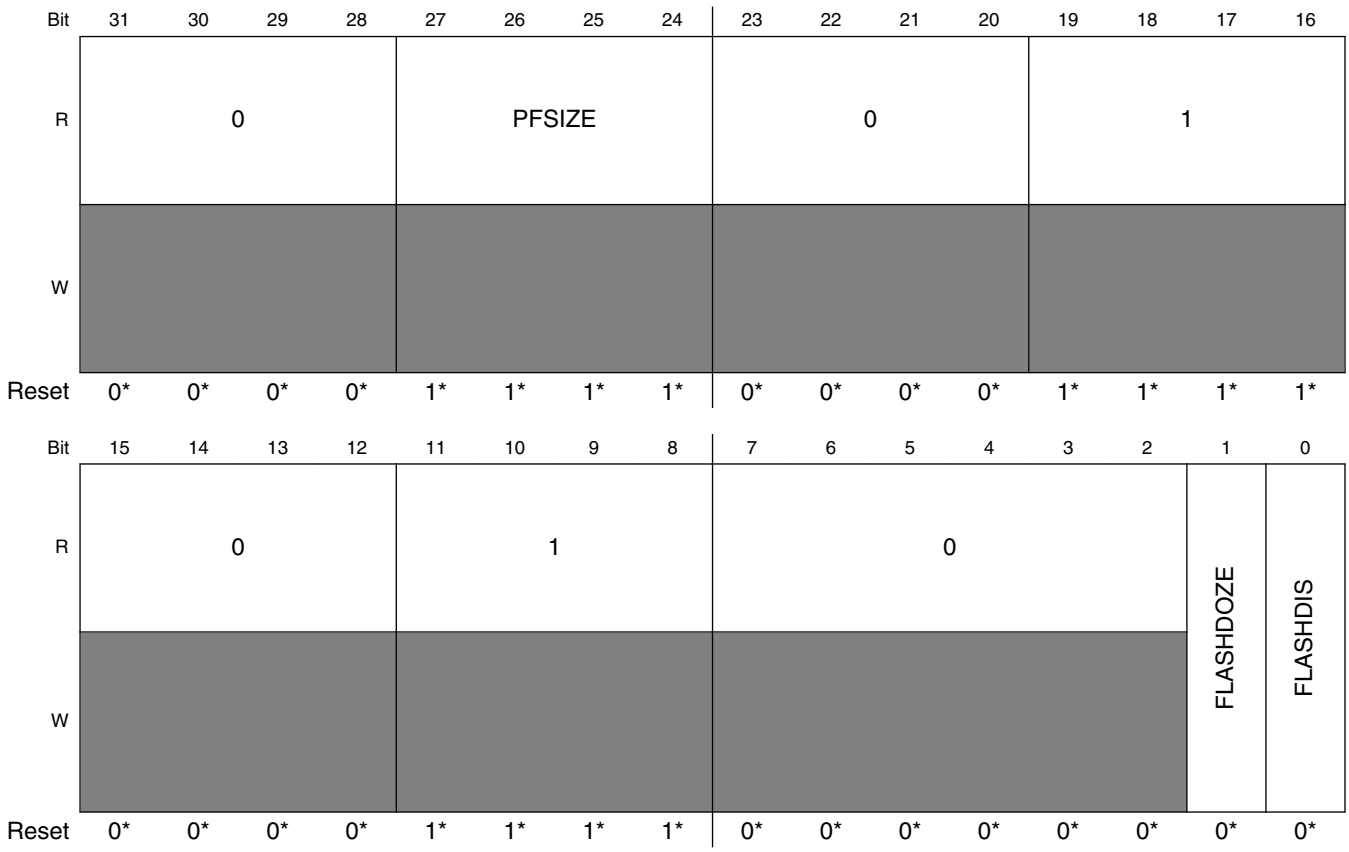


SIM_CLKDIV2 field descriptions

Field	Description
31–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3–1 USBDIV	USB clock divider divisor This field sets the divide value for the fractional clock divider when the MCGFLLCLK, or MCGPLLCLK, or IRC48M clock is the USB clock source (SOPT2[USBSRC] = 1). Divider output clock = Divider input clock × [(USBFRAC+1) / (USBDIV+1)]
0 USBFRAC	USB clock divider fraction This field sets the fraction multiply value for the fractional clock divider when the MCGFLLCLK, or MCGPLLCLK, or IRC48M clock is the USB clock source (SOPT2[USBSRC] = 1). Divider output clock = Divider input clock × [(USBFRAC+1) / (USBDIV+1)]

14.2.19 Flash Configuration Register 1 (SIM_FCFG1)

Address: 4004_7000h base + 104Ch offset = 4004_804Ch



SIM_FCFG1 field descriptions

Field	Description
31–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27–24 PFSIZE	Program flash size This field specifies the amount of program flash memory available on the device . Undefined values are reserved. 0011 32 KB of program flash memory 0101 64 KB of program flash memory 0111 128 KB of program flash memory 1001 256 KB of program flash memory 1011 512 KB of program flash memory 1101 1024 KB of program flash memory 1111 256 KB of program flash memory

Table continues on the next page...

SIM_FCFG1 field descriptions (continued)

Field	Description
23–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
15–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
7–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 FLASHDOZE	Flash Doze When set, Flash memory is disabled for the duration of Wait mode. An attempt by the DMA or other bus master to access the Flash when the Flash is disabled will result in a bus error. This bit should be clear during VLP modes. The Flash will be automatically enabled again at the end of Wait mode so interrupt vectors do not need to be relocated out of Flash memory. The wakeup time from Wait mode is extended when this bit is set. 0 Flash remains enabled during Wait mode 1 Flash is disabled for the duration of Wait mode
0 FLASHDIS	Flash Disable Flash accesses are disabled (and generate a bus error) and the Flash memory is placed in a low power state. This bit should not be changed during VLP modes. Relocate the interrupt vectors out of Flash memory before disabling the Flash. 0 Flash is enabled 1 Flash is disabled

14.2.20 Flash Configuration Register 2 (SIM_FCFG2)

Address: 4004_7000h base + 1050h offset = 4004_8050h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	MAXADDR0							1	MAXADDR1						
W																
Reset	0*	1*	1*	1*	1*	1*	1*	1*	1*	1*	1*	1*	1*	1*	1*	1*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

SIM_FCFG2 field descriptions

Field	Description
31 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
30–24 MAXADDR0	Max address block 0 This field concatenated with 13 trailing zeros indicates the first invalid address of each program flash block. For example, if MAXADDR0 = 0x20 the first invalid address of flash block 0 is 0x0004_0000. This would be the MAXADDR0 value for a device with 256 KB program flash in flash block 0.
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
22–16 MAXADDR1	Max address block 1 This field equals zero if there is only one program flash block, otherwise it equals the value of the MAXADDR0 field. For example, with MAXADDR0 = MAXADDR1 = 0x20 the first invalid address of flash block 1 is 0x4_0000 + 0x4_0000. This would be the MAXADDR1 value for a device with 512 KB program flash memory across two flash blocks and no FlexNVM.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

14.2.21 Unique Identification Register High (SIM_UIDH)

Address: 4004_7000h base + 1054h offset = 4004_8054h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	UID																															
W																																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

SIM_UIDH field descriptions

Field	Description
UID	Unique Identification Unique identification for the device.

14.2.22 Unique Identification Register Mid-High (SIM_UIDMH)

Address: 4004_7000h base + 1058h offset = 4004_8058h

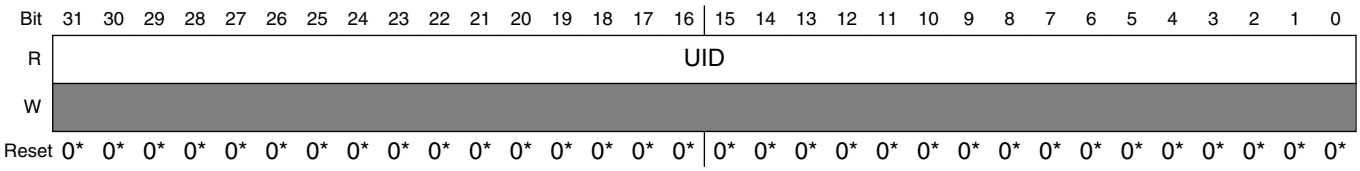
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	UID																															
W																																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

SIM_UIDMH field descriptions

Field	Description
UID	Unique Identification Unique identification for the device.

14.2.23 Unique Identification Register Mid Low (SIM_UIDML)

Address: 4004_7000h base + 105Ch offset = 4004_805Ch

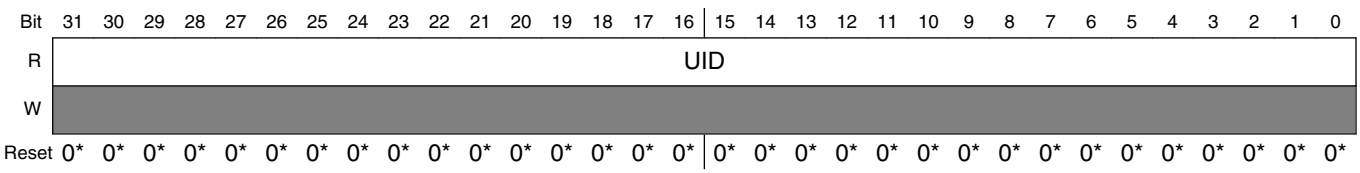


SIM_UIDML field descriptions

Field	Description
UID	Unique Identification Unique identification for the device.

14.2.24 Unique Identification Register Low (SIM_UIDL)

Address: 4004_7000h base + 1060h offset = 4004_8060h



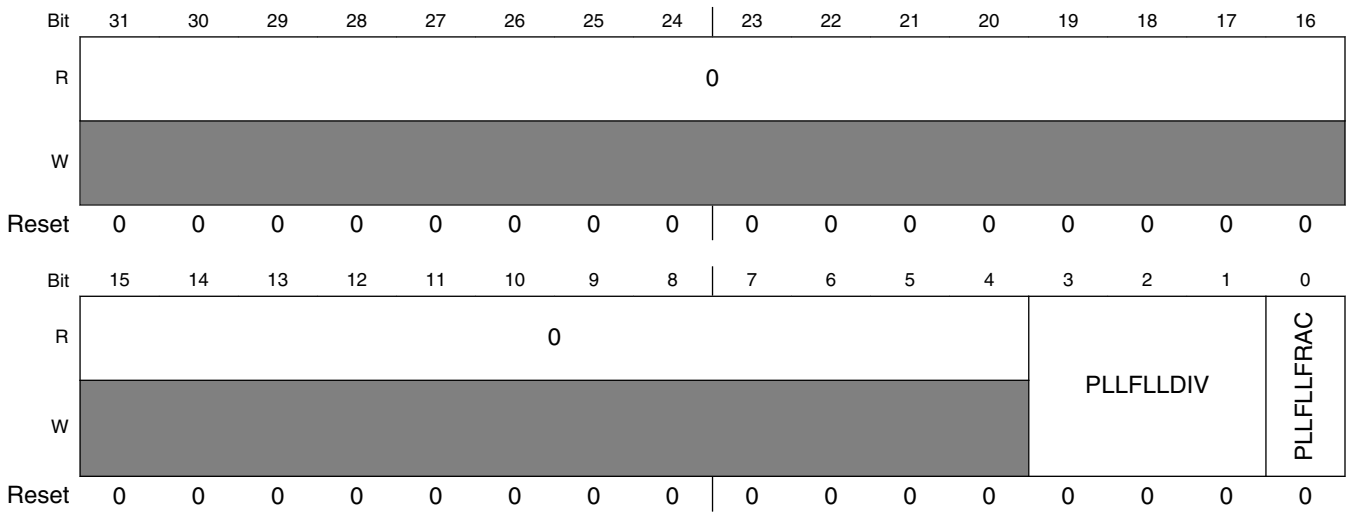
SIM_UIDL field descriptions

Field	Description
UID	Unique Identification Unique identification for the device.

14.2.25 System Clock Divider Register 3 (SIM_CLKDIV3)

This register should only be written when the LPUART, EMVSIM,FlexIO and TPM modules are disabled.

Address: 4004_7000h base + 1064h offset = 4004_8064h



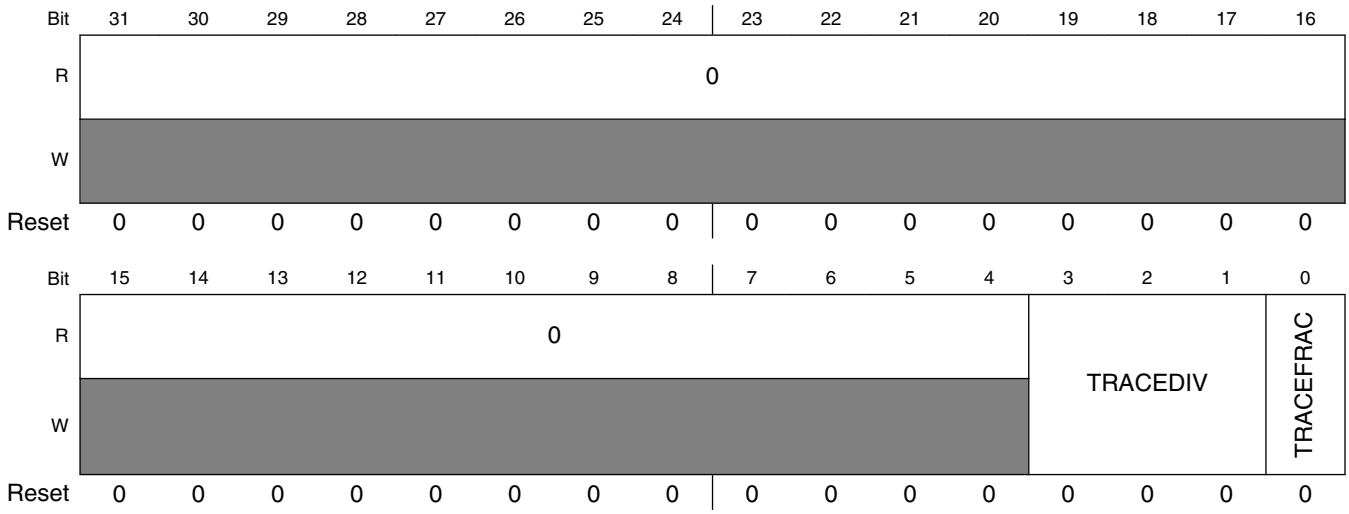
SIM_CLKDIV3 field descriptions

Field	Description
31–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3–1 PLLFLLDIV	PLLFLL clock divider divisor This field sets the divide value for the fractional clock divider used as a source for various peripheral clocks. The source clock for the fractional clock divider is set by the SOPT2 PLLFLLSEL register bit. Divider output clock = Divider input clock * ((PLLFLLFRAC+1)/(PLLFLLDIV+1))
0 PLLFLLFRAC	PLLFLL clock divider fraction This field sets the divide value for the fractional clock divider used as a source for various peripherals. The source clock for the fractional clock divider is set by the SOPT2 PLLFLLSEL register bit. Divider output clock = Divider input clock*((PLLFLLFRAC+1)/(PLLFLLDIV+1))

14.2.26 System Clock Divider Register 4 (SIM_CLKDIV4)

This register should only be written when the SOPT2 TRACECLKSEL register bit is set.

Address: 4004_7000h base + 1068h offset = 4004_8068h



SIM_CLKDIV4 field descriptions

Field	Description
31–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3–1 TRACEDIV	Trace clock divider divisor This field sets the divide value for the MCGCLKOUT fractional clock divider used as a source for trace clock. The source clock for the trace clock is set by the SOPT2 TRACECLKSEL register bit. Divider output clock = Divider input clock * ((TRACEFRAC+1)/(TRACEDIV+1))
0 TRACEFRAC	Trace clock divider fraction This field sets the divide value for the MCGCLKOUT fractional clock divider used as a source for trace clock. The source clock for the trace clock is set by the SOPT2 TRACECLKSEL register bit. Divider output clock = Divider input clock*((TRACEFRAC+1)/(TRACEDIV+1))

14.3 Functional description

For more information about the functions of SIM, see the Introduction section.

Chapter 15
EMV SIM

15.1 Chip-specific EMVSIM information

15.1.1 Overview

The EMV_SIM (Euro/Mastercard/Visa/SIM Serial Interface Module) is a module that supports ISO-7816 protocol. For more information, please see Introduction

15.1.2 EMV_SIM Instantiations

This device contains 2 EMV_SIM modules. This section describes how each module is configured on this device.

15.2 Introduction

The Euro, MasterCard, Visa Subscriber Identification Module (EMV SIM) is designed to facilitate communication to Smart Cards compatible to the EMV ver4.3 standard (Book 1) and Smart Cards compatible with ISO/IEC 7816-3 Standard.

15.2.1 Features

The EMV SIM module supports the following features:

- Supports Smart Cards based on the EMV Standard v4.3 and ISO 7816-3 standard

- Independent clock for SIM logic (transmitter + receiver) and independent clock for register read-write interface
- 16 byte deep FIFO for transmitter and receiver
- Automatic NACK generation on parity error and receiver FIFO overflow error
- Support for both Inverse and Direct conventions
- Re-transmission of byte upon Smart Card NACK request with programmable threshold of re-transmissions
- Auto detection of Initial Character in receiver and setting of data format (inverse or direct)
- NACK detection in receiver
- Independent timers to measure character wait time, block wait time and block guard time
- Two general purpose counters available for use by software application with programmable clock selection for the counters
- DMA support available to transfer data to/from FIFOs. Programmable option available to select interrupt or DMA feature
- Programmable Prescaler to generate the desired frequency for Card Clock and Baud Rate Divisor to generate the internal ETU clocks for transmitter and receiver for any F/D ratio
- Deep sleep wake-up via Smart Card presence detect interrupt
- Manual control of all Smart Card interface signals
- Automatic power down of port logic on Smart Card presence detect
- Support for 8-bit LRC and 16-bit CRC generation for bytes sent out from transmitter and checking incoming message checksum for receiver

15.3 Block Diagram

Figure below shows the block diagram for the EMV SIM module.

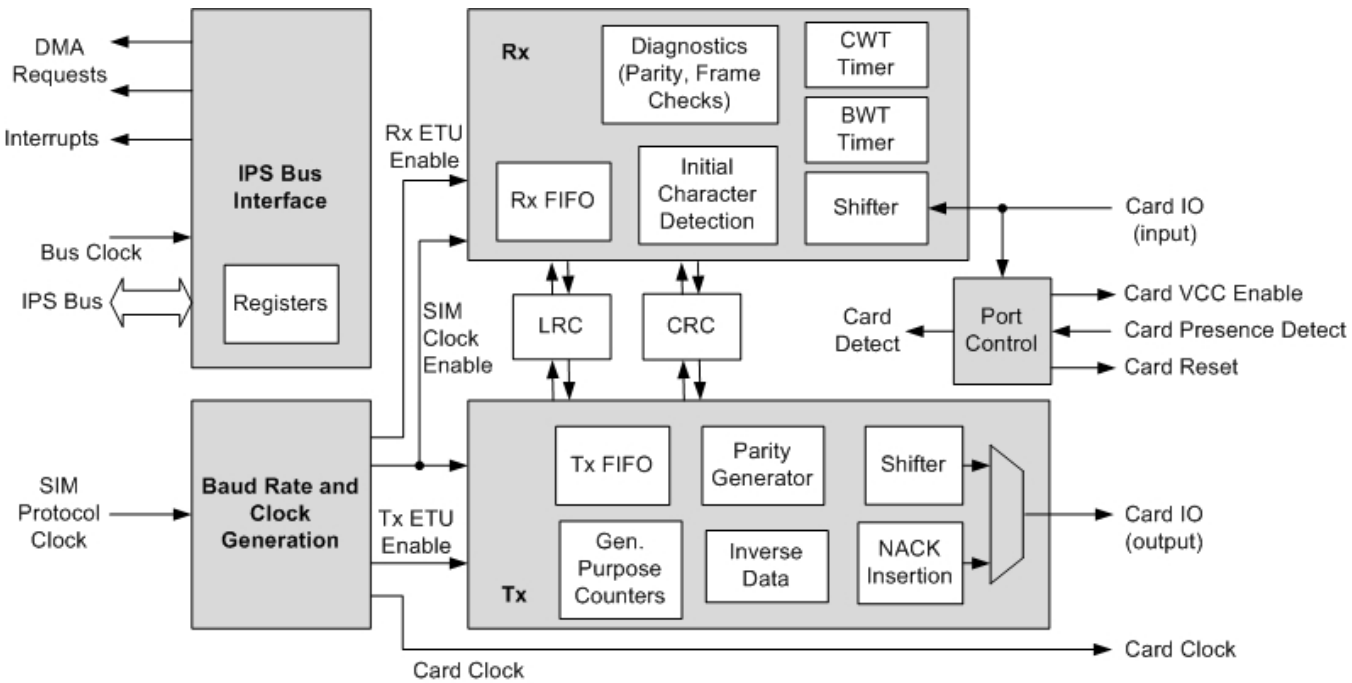


Figure 15-1. EMV SIM Block Diagram

15.4 Design Overview

The EMV SIM is designed to be compliant to the EMV ICC Specifications ver. 4.3 (dated Nov 2011) and the ISO-7816-3 standard.

The EMV SIM module is a block that is configured via the device's peripheral bus interface. The module has 32-bit aligned memory mapped registers that are used to configure and control the operations of the module. The software can write the transmit bytes or read the received bytes using either interrupt operation or DMA operation. The module can generate necessary DMA requests for the operation.

The module interfaces to the external card (Smart Card) via card clock, card reset, card V_{CC} enable and IO pins. The transmitter output from the module and the receiver input to the module are connected to the same IO pin and used in the open drain configuration. A pull-up resistor must be connected to the IO pin on board to allow proper functioning.

The key functional blocks in the module are clocking, transmitter and receiver which control the interactions with the Smart Card. These blocks function on a clock that is different and asynchronous to the register read/write clock. In order for the transmitter and receiver to function properly, the respective configuration must be done before enabling the transmitter or receiver.

The clocking module generates the card clock (output to Smart Card), and the internal clocks for the transmitter and receiver. The internal clocks control the ETU period and the sampling and driving of data on the IO line. The receive operation uses an internal over-sampled clock that oversamples the received input at 16x times the ETU rate. The prescaler generates the card clock in the range of 1 to 5 MHz with near 50% duty cycle and the baud divider generates the internal ETU clocks for transmitter and receiver.

The transmitter comprises of a 16-byte deep FIFO to store the bytes to be sent to the Smart Card. These bytes are sent to the Smart Card serially by the transmitter. The data format (i.e. inverse or direct conversion) is supported and the byte is converted into the right data format before being shifted out serially. The transmitter also supports retransmission of the current byte on the reception of a NACK. The transmitter automatically inserts NACK when the receiver indicates a parity or FIFO overflow error, if configured to do so by software. The transmitter is not required to be enabled for this. The transmitter also includes timer to insert the programmable guard time between the transmitter bytes and general purpose timers to allow software performs certain measurements. The status of the transmitter operation is intimated to software via maskable interrupts.

The receiver comprises of a 16-byte deep FIFO to store the correctly received bytes from the Smart Card. Software must ensure that it reads out the data from FIFO to prevent any overflow when more bytes are sent from the card. The receiver can be configured to detect the initial character. When configured to do so, the data format (direct or inverse convention) is also determined by the receiver and appropriate bit is set in the register map. Internal timers in the receiver measure the various wait times (Character, Block and Guard). On reception of a byte, the receiver checks the byte for Parity Error (in T=0 mode) and Framing Error. It can then direct the transmitter to insert NACK on parity error detection. For a block of bytes received, the receiver checks for LRC or CRC errors (in T=1 mode). Other errors are stored as status for software to be aware of their occurrence. The status of the receiver operation is intimated to software via maskable interrupts.

In addition to the above blocks, the module also contains the 8-bit LRC and the 16-bit CRC blocks that are common to the transmitter and receiver. Both transmitter and receiver can use the LRC and CRC blocks and can insert the LRC or CRC into the byte stream or check the validity of the input stream using the LRC and CRC values received. Since transmit and receive operations are mutually exclusive, common LRC and CRC blocks for the transmitter and receiver can be used.

The Smart Card interface signals, except IO, which is controlled by the transmitter and receiver; are generated by the port control block which controls the assertion and de-assertion of the clock, reset and VCC signals to Smart Card. It can do so manually (software needs to explicitly write the necessary bits) or using auto power down wherein

the module can itself power down the Smart Card when configured to do so by software. The port control block can also detect the Smart Card presence and generate necessary interrupts to indicate the same.

15.5 Signal Description

The following table shows the user-accessible signals available on EMV SIM. See the chip-level specification to find out which signals are actually connected to the external pins.

Table 15-1. EMV SIM Signal Description

Signal	Description	I/O
EMVSIM_SCLK	Card Clock. Clock to Smart Card.	O
EMVSIM_SRST	Card Reset. Reset signal to Smart Card	O
EMVSIM_VCC_EN	Card Power Enable. This signal controls the power to Smart Card	O
EMVSIM_IO	Card Data Line. Bi-directional data line.	I/O
EMVSIM_PD	Card Presence Detect. Signal indicating presence or removal of card	I
EMVSIM_PF	External PMIC power fail indication.	I

15.6 Memory Map and Registers

The memory map comprises of 32-bit aligned registers which can be accessed via 8-bit, 16-bit, or 32-bit accesses. Write access to reserved locations will generate transfer error. Read access to reserved locations will also generate transfer error and the read data bus will show all 0s.

The module will not check for correctness of programmed values in the registers and software must ensure that correct values are being written.

EMVSIM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_4000	Version ID Register (EMVSIM0_VER_ID)	32	R	0000_0000h	15.6.1/311
400D_4004	Parameter Register (EMVSIM0_PARAM)	32	R	0000_1010h	15.6.2/311
400D_4008	Clock Configuration Register (EMVSIM0_CLKCFG)	32	R/W	0000_0000h	15.6.3/312
400D_400C	Baud Rate Divisor Register (EMVSIM0_DIVISOR)	32	R/W	0000_0174h	15.6.4/313

Table continues on the next page...

EMVSIM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_4010	Control Register (EMVSIM0_CTRL)	32	R/W	0100_0006h	15.6.5/314
400D_4014	Interrupt Mask Register (EMVSIM0_INT_MASK)	32	R/W	0000_FFFFh	15.6.6/318
400D_4018	Receiver Threshold Register (EMVSIM0_RX_THD)	32	R/W	0000_0001h	15.6.7/320
400D_401C	Transmitter Threshold Register (EMVSIM0_TX_THD)	32	R/W	0000_000Fh	15.6.8/321
400D_4020	Receive Status Register (EMVSIM0_RX_STATUS)	32	w1c	0000_0000h	15.6.9/322
400D_4024	Transmitter Status Register (EMVSIM0_TX_STATUS)	32	w1c	0000_00B8h	15.6.10/326
400D_4028	Port Control and Status Register (EMVSIM0_PCSR)	32	R/W	0100_0000h	15.6.11/329
400D_402C	Receive Data Read Buffer (EMVSIM0_RX_BUF)	32	R	0000_0000h	15.6.12/331
400D_4030	Transmit Data Buffer (EMVSIM0_TX_BUF)	32	W (always reads 0)	0000_0000h	15.6.13/332
400D_4034	Transmitter Guard ETU Value Register (EMVSIM0_TX_GETU)	32	R/W	0000_0000h	15.6.14/332
400D_4038	Character Wait Time Value Register (EMVSIM0_CWT_VAL)	32	R/W	0000_FFFFh	15.6.15/333
400D_403C	Block Wait Time Value Register (EMVSIM0_BWT_VAL)	32	R/W	FFFF_FFFFh	15.6.16/333
400D_4040	Block Guard Time Value Register (EMVSIM0_BGT_VAL)	32	R/W	0000_0000h	15.6.17/333
400D_4044	General Purpose Counter 0 Timeout Value Register (EMVSIM0_GPCNT0_VAL)	32	R/W	0000_FFFFh	15.6.18/334
400D_4048	General Purpose Counter 1 Timeout Value (EMVSIM0_GPCNT1_VAL)	32	R/W	0000_FFFFh	15.6.19/334
400D_5000	Version ID Register (EMVSIM1_VER_ID)	32	R	0000_0000h	15.6.1/311
400D_5004	Parameter Register (EMVSIM1_PARAM)	32	R	0000_1010h	15.6.2/311
400D_5008	Clock Configuration Register (EMVSIM1_CLKCFG)	32	R/W	0000_0000h	15.6.3/312
400D_500C	Baud Rate Divisor Register (EMVSIM1_DIVISOR)	32	R/W	0000_0174h	15.6.4/313
400D_5010	Control Register (EMVSIM1_CTRL)	32	R/W	0100_0006h	15.6.5/314
400D_5014	Interrupt Mask Register (EMVSIM1_INT_MASK)	32	R/W	0000_FFFFh	15.6.6/318
400D_5018	Receiver Threshold Register (EMVSIM1_RX_THD)	32	R/W	0000_0001h	15.6.7/320
400D_501C	Transmitter Threshold Register (EMVSIM1_TX_THD)	32	R/W	0000_000Fh	15.6.8/321
400D_5020	Receive Status Register (EMVSIM1_RX_STATUS)	32	w1c	0000_0000h	15.6.9/322
400D_5024	Transmitter Status Register (EMVSIM1_TX_STATUS)	32	w1c	0000_00B8h	15.6.10/326
400D_5028	Port Control and Status Register (EMVSIM1_PCSR)	32	R/W	0100_0000h	15.6.11/329
400D_502C	Receive Data Read Buffer (EMVSIM1_RX_BUF)	32	R	0000_0000h	15.6.12/331
400D_5030	Transmit Data Buffer (EMVSIM1_TX_BUF)	32	W (always reads 0)	0000_0000h	15.6.13/332
400D_5034	Transmitter Guard ETU Value Register (EMVSIM1_TX_GETU)	32	R/W	0000_0000h	15.6.14/332
400D_5038	Character Wait Time Value Register (EMVSIM1_CWT_VAL)	32	R/W	0000_FFFFh	15.6.15/333
400D_503C	Block Wait Time Value Register (EMVSIM1_BWT_VAL)	32	R/W	FFFF_FFFFh	15.6.16/333
400D_5040	Block Guard Time Value Register (EMVSIM1_BGT_VAL)	32	R/W	0000_0000h	15.6.17/333

Table continues on the next page...

EMVSIM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_5044	General Purpose Counter 0 Timeout Value Register (EMVSIM1_GPCNT0_VAL)	32	R/W	0000_FFFFh	15.6.18/334
400D_5048	General Purpose Counter 1 Timeout Value (EMVSIM1_GPCNT1_VAL)	32	R/W	0000_FFFFh	15.6.19/334

15.6.1 Version ID Register (EMVSIMx_VER_ID)

Version ID for the IP. It corresponds to the version of IP being used.

Address: Base address + 0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	VER																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EMVSIMx_VER_ID field descriptions

Field	Description
VER	Version ID of the module EMV SIM Version Number used on the chip 31:16 - Major Version (example: 01.00) 15:0 - Minor Version (example: 01.00)

15.6.2 Parameter Register (EMVSIMx_PARAM)

This register provides details on the parameter settings that were used while including this module in the chip.

Address: Base address + 4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																TX_FIFO_DEPTH								RX_FIFO_DEPTH							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

EMVSIMx_PARAM field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–8 TX_FIFO_ DEPTH	Transmit FIFO Depth Value of parameter for Transmit FIFO Depth (in Bytes)
RX_FIFO_ DEPTH	Receive FIFO Depth Value of parameter for Receive FIFO Depth (in Bytes)

15.6.3 Clock Configuration Register (EMVSIMx_CLKCFG)

This register provides configuration details to enable the right clock frequency of clocks used by EMV SIM module.

Address: Base address + 8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				GPCNT0_ CLK_SEL		GPCNT1_ CLK_SEL		CLK_PRSC							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EMVSIMx_CLKCFG field descriptions

Field	Description
31–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11–10 GPCNT0_CLK_ SEL	General Purpose Counter 0 Clock Select Selects which clock source is used by EMV SIM Module general purpose counter 0. The only way to reset the counter is to set these bits to zero. The counter will begin counting as soon as the clock input is selected and the clocks are active. These input clocks are enabled through other register bits of the EMV SIM module (KILL_CLOCK, RCV_EN, and XMT_EN). Counter is active while RCV_EN or XMT_EN are set. 00 Disabled / Reset (default) 01 Card Clock 10 Receive Clock 11 ETU Clock (transmit clock)
9–8 GPCNT1_CLK_ SEL	General Purpose Counter 1 Clock Select Selects which clock source is used by EMV SIM Module general purpose counter 1. The only way to reset the counter is to set these bits to zero. The counter will begin counting as soon as the clock input is selected and the clocks are active. These input clocks are enabled through other register bits of the EMV

Table continues on the next page...

EMVSIMx_CLKCFG field descriptions (continued)

Field	Description
	SIM module (KILL_CLOCK, RCV_EN, and XMT_EN). Counter is active while RCV_EN or XMT_EN are set. 00 Disabled / Reset (default) 01 Card Clock 10 Receive Clock 11 ETU Clock (transmit clock)
CLK_PRSC	Clock Prescaler Value The value written to this register will determine the desired card clock frequency. The Card Clock frequency is the EMV SIM Protocol (or logic) clock divided by this prescaler value. The prescaler value should be updated only when card clock is disabled and transmitter and receiver are not operational. 0, 1 Max Divide value used (default 0 is used) 2 Divide by 2 >2 Non-zero value will divide clock accordingly

15.6.4 Baud Rate Divisor Register (EMVSIMx_DIVISOR)

This regiter configures the divisor value to generate the baud clock which will drive the card clock and also generate the transmit and receive clocks and respective ETUs.

Address: Base address + Ch offset

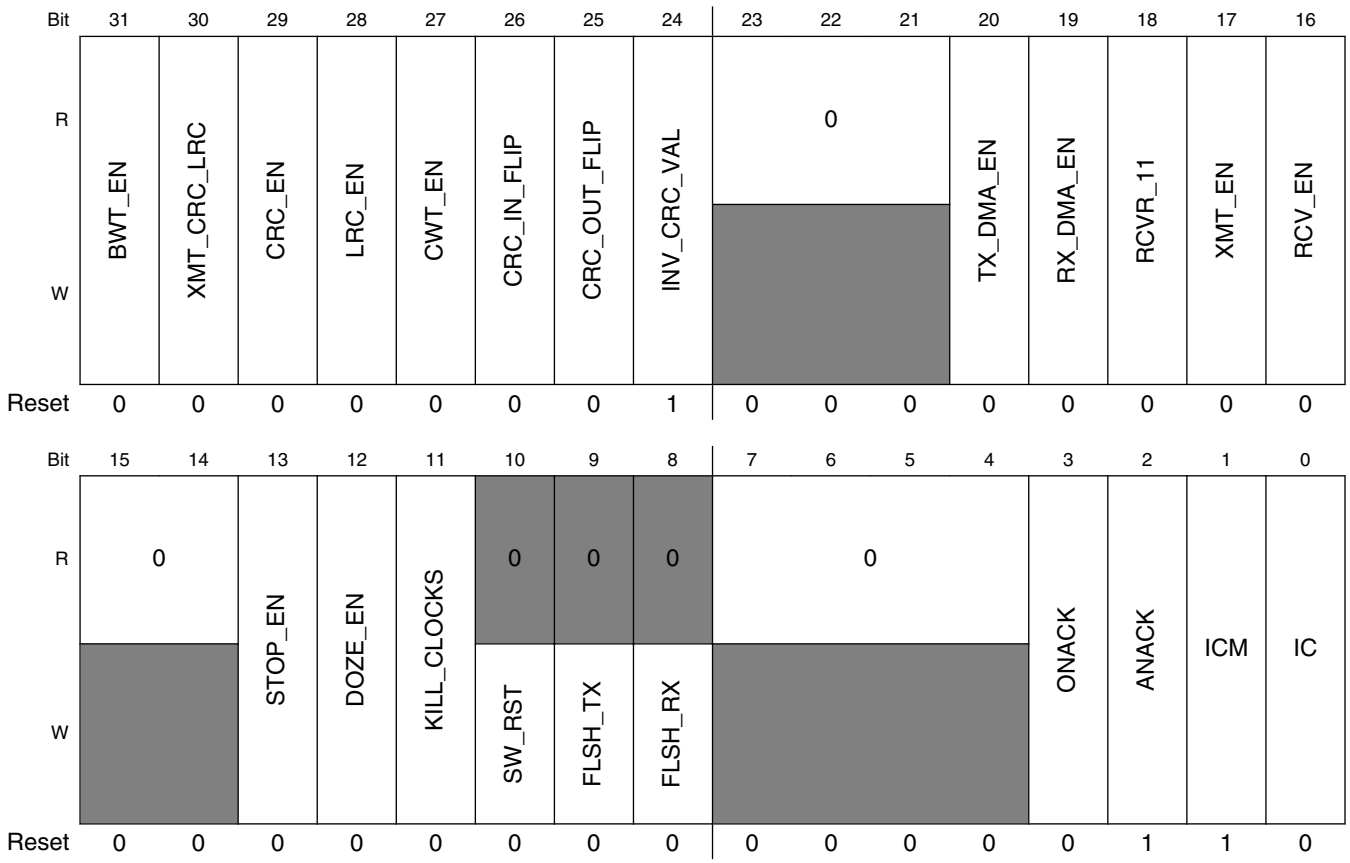
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																DIVISOR_VALUE																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	0	0

EMVSIMx_DIVISOR field descriptions

Field	Description
31–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
DIVISOR_ VALUE	Divisor (F/D) Value The value written to this register will be used to generate the ETU bit period that will be used by the transmitter and receiver. The divisor value is the integer result of F/D value; where F and D are the clock rate conversion integer and baud rate adjustment integer, respectively, that required for the desired operation. The value in this register can be changed when no transaction is active with the smart card. When programming this field, the fractional part of F/D should be rounded off the nearest integer. 0 - 4 Invalid. As per ISO 7816 specification, minimum value of F/D is 5 372 Divisor value for F = 372 and D = 1 (default) others Integer value of result of F/D

15.6.5 Control Register (EMVSIMx_CTRL)

Address: Base address + 10h offset



EMVSIMx_CTRL field descriptions

Field	Description
31 BWT_EN	Block Wait Time Counter Enable Writing a '1' to this bit will enable the BWT and BGT functions. The BWT and BGT functions can then be individually selected using the interrupt mask. 0 Disable BWT, BGT Counters (default) 1 Enable BWT, BGT Counters
30 XMT_CRC_LRC	Transmit CRC or LRC Enable This bit specifies whether or not to transmit the redundancy checking data (LRC or CRC) at the end of a transmission (that is, when the FIFO becomes empty). 0 No CRC or LRC value is transmitted (default) 1 Transmit LRC or CRC info when FIFO empties (whichever is enabled)
29 CRC_EN	CRC Enable This bit enables the calculation of the 16-bit CRC value for both receiver and transmitter. The result of the calculation is continuously compared to the expected remainder and reflected in the CRC_OK bit in the RX_STATUS register. Clearing this bit resets the current CRC residual value in the EMV SIM hardware.

Table continues on the next page...

EMVSIMx_CTRL field descriptions (continued)

Field	Description
	0 16-bit Cyclic Redundancy Checking disabled (default) 1 16-bit Cyclic Redundancy Checking enabled
28 LRC_EN	LRC Enable This bit enables the calculation of the 8-bit LRC value for both receiver and transmitter. The result of the calculation is continuously compared to zero and reflected in the LRC_OK bit in the RX_STATUS register. Clearing this bit resets the current LRC value in the EMV SIM hardware. 0 8-bit Linear Redundancy Checking disabled (default) 1 8-bit Linear Redundancy Checking enabled
27 CWT_EN	Character Wait Time Counter Enable Enables the character wait time counter. Clearing this bit resets the counter to zero. 0 Character Wait time Counter is disabled (default) 1 Character Wait time counter is enabled
26 CRC_IN_FLIP	CRC Input Byte's Bit Reversal or Flip Control This bit control whether the bits in the CRC input byte will be reversed before CRC calculation or not. When set to '1', the bits within the input byte for CRC will change from 7:0 to 0:7. For CCITT CRC calculation, this bit should be set to '1'. For any other CRC using same polynomial, this bit can be set accordingly. 0 Bits in the input byte will not be reversed (i.e. 7:0 will remain 7:0) before the CRC calculation (default) 1 Bits in the input byte will be reversed (i.e. 7:0 will become 0:7) before CRC calculation
25 CRC_OUT_FLIP	CRC Output Value Bit Reversal or Flip This bit control whether the bits in the CRC output bytes will be reversed or not. When set to '1', the bits within the two bytes for CRC Output will change from 15:0 to {8:15,0:7}. For CCITT CRC calculation, this bit should be set to '1'. For any other CRC using same polynomial, this bit can be set accordingly. 0 Bits within the CRC output bytes will not be reversed i.e. 15:0 will remain 15:0 (default) 1 Bits within the CRC output bytes will be reversed i.e. 15:0 will become {8:15,0:7}
24 INV_CRC_VAL	Invert bits in the CRC Output Value This bit control whether the bits within the CRC Output value will be inverted (1's complement) or not. For CCITT CRC calculation, this bit should be set to '1'. For any other CRC using same polynomial, this bit can be set accordingly. 0 Bits in CRC Output value will not be inverted. 1 Bits in CRC Output value will be inverted. (default)
23–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20 TX_DMA_EN	Transmit DMA Enable Enables assertion of DMA write request when Transmit FIFO is empty. Request is held asserted till Transmit FIFO reaches the programmed data threshold value. Transmit Data Threshold Interrupt will not be generated when this bit is asserted. 0 No DMA Write Request asserted for Transmitter (default) 1 DMA Write Request asserted for Transmitter

Table continues on the next page...

EMVSIMx_CTRL field descriptions (continued)

Field	Description
19 RX_DMA_EN	Receive DMA Enable Enables assertion of DMA read request when Receive FIFO reaches the programmed data threshold value. Request is held asserted till all the programmed threshold bytes are read out. Receiver Data Interrupt will not be generated when this bit is asserted. 0 No DMA Read Request asserted for Receiver (default) 1 DMA Read Request asserted for Receiver
18 RCVR_11	Receiver 11 ETU Mode Enable Used to configure the EMV SIM module receiver for 11 ETU operation (that is, 1 Stop bit). This bit is provided for support of T=1 cards. 0 Receiver configured for 12 ETU operation mode (default) 1 Receiver configured for 11 ETU operation mode
17 XMT_EN	Transmitter Enable Used to enable/disable the EMV SIM transmitter block. It can be set to 0 during the auto power down sequence. **Note:** Setting this bit (transition from 0 to 1) will reset the CRC and LRC values. 0 EMV SIM Transmitter disabled (default) 1 EMV SIM Transmitter enabled
16 RCV_EN	Receiver Enable Used to enable/disable the EMV SIM receiver block. Once the transmitter has completed its operation, the software must enable the receiver using this bit. It can be set to 0 during the auto power down sequence. 0 EMV SIM Receiver disabled (default) 1 EMV SIM Receiver enabled
15–14 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
13 STOP_EN	STOP Enable Used to configure the operation of the EMV SIM module when a processor STOP instruction is executed. This bit is added to provide support for Smart Cards that do not allow the Smart Card clock to be stopped while power is applied. **Note:** To enable Card Clock in STOP mode, both STOP_EN and DOZE_EN should be set to 1. 0 STOP instruction shuts down all EMV SIM clocks (default) 1 STOP instruction shuts down all clocks except for the Smart Card Clock (SCK) (clock provided to Smart Card)
12 DOZE_EN	Doze Enable Used to configure the operation of the EMV SIM module when a processor DOZE instruction is executed. 0 DOZE instruction will gate all internal EMV SIM clocks as well as the Smart Card clock when the transmit FIFO is empty (default) 1 DOZE instruction has no effect on EMV SIM module
11 KILL_CLOCKS	Kill all internal clocks Used to enable/disable the clock input to the EMV SIM module. This bit will gate all clocks including the Smart Card clock regardless of the state of the STOP bit described above.

Table continues on the next page...

EMVSIMx_CTRL field descriptions (continued)

Field	Description
	Note: This bit will have no effect on the register read write clock. Only EMV SIM logic clock is gated. 0 EMV SIM input clock enabled (default) 1 EMV SIM input clock is disabled
10 SW_RST	Software Reset Bit Used to reset the entire EMV SIM module. This acts the same as a hardware reset for the EMV SIM module. This bit is self-clearing and always reads 0. **Note:** Software should allow a minimum of 4 Protocol clock cycles before attempting to access the EMV SIM module after a software reset. 0 EMV SIM Normal operation (default) 1 EMV SIM held in Reset
9 FLSH_TX	Flush Transmitter Bit This bit operates as an EMV SIM transmitter reset. The receive portion of the EMV SIM module is not affected. This bit clears automatically and always reads 0. 0 EMV SIM Transmitter normal operation (default) 1 EMV SIM Transmitter held in Reset
8 FLSH_RX	Flush Receiver Bit This bit operates as an EMV SIM receiver reset. The transmit portion of the EMV SIM module is not affected. This bits clears automatically and always reads 0. 0 EMV SIM Receiver normal operation (default) 1 EMV SIM Receiver held in Reset
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 ONACK	Overrun NACK Enable Enables NACK generation when Rx FIFO is full and another message is ready for writing into the FIFO. 0 NACK generation on overrun is disabled (default) 1 NACK generation on overrun is enabled
2 ANACK	Auto NACK Enable Enables NACK generation for parity errors in receieved messages or when invalid initial characters are received in ICM mode. 0 NACK generation on errors disabled 1 NACK generation on errors enabled (default)
1 ICM	Initial Character Mode Enables initial character mode. Will be automatically cleared by hardware once a valid initial character is received. 0 Initial Character Mode disabled 1 Initial Character Mode enabled (default)
0 IC	Inverse Convention

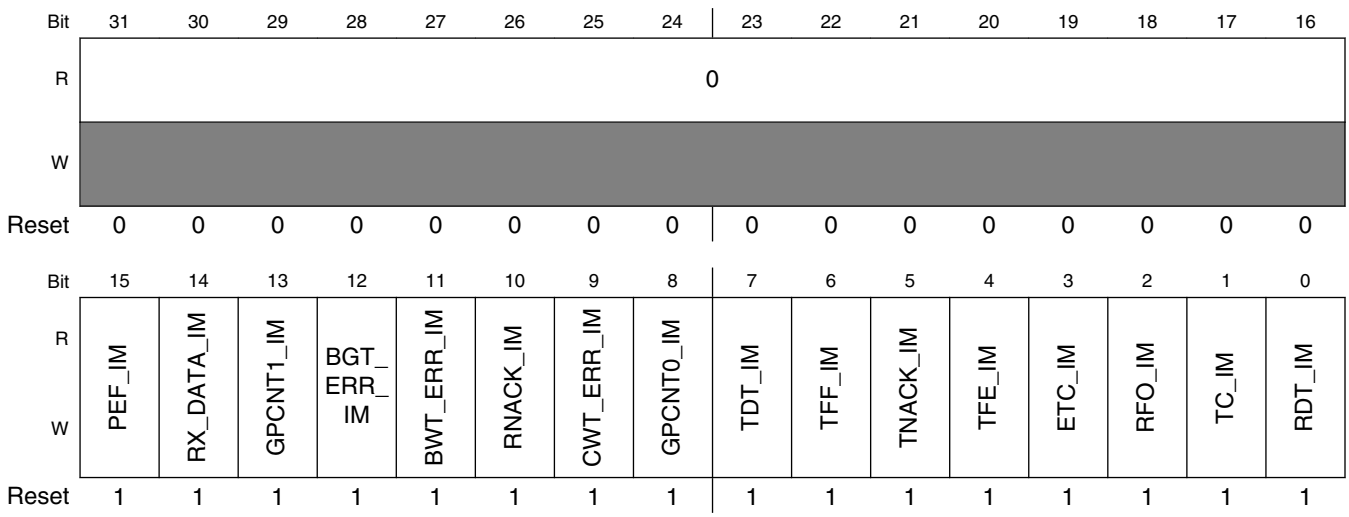
Table continues on the next page...

EMVSIMx_CTRL field descriptions (continued)

Field	Description
	Used to configure the EMV SIM to use either inverse convention or direct convention for its data format. The IC bit can be controlled by software, but it is normally set by hardware as a result of the interpretation of the initial character when in ICM mode. 0 Direction convention transfers enabled (default) 1 Inverse convention transfers enabled

15.6.6 Interrupt Mask Register (EMVSIMx_INT_MASK)

Address: Base address + 14h offset



EMVSIMx_INT_MASK field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15 PEF_IM	Parity Error Interrupt Mask Used to enable/disable the ability of the PEF flag in the RX_STATUS register to generate EMV SIM interrupts. 0 PEF interrupt enabled 1 PEF interrupt masked (default)
14 RX_DATA_IM	Receive Data Interrupt Mask Used to enable/disable the ability of the RX_DATA flag in the RX_STATUS register to generate EMV SIM interrupts. 0 RX_DATA interrupt enabled 1 RX_DATA interrupt masked (default)
13 GPCNT1_IM	General Purpose Counter 1 Timeout Interrupt Mask

Table continues on the next page...

EMVSIMx_INT_MASK field descriptions (continued)

Field	Description
	Used to enable/disable the ability of the GPCNT1_TO flag in the TX_STATUS register to generate EMV SIM interrupts. 0 GPCNT1_TO interrupt enabled 1 GPCNT1_TO interrupt masked (default)
12 BGT_ERR_IM	Block Guard Time Error Interrupt Used to enable/disable the ability of the BGT_ERR flag in the RX_STATUS register to generate EMV SIM interrupts. 0 BGT_ERR interrupt enabled 1 BGT_ERR interrupt masked (default)
11 BWT_ERR_IM	Block Wait Time Error Interrupt Mask Used to enable/disable the ability of the BWT_ERR flag in the RX_STATUS register to generate EMV SIM interrupts. 0 BWT_ERR interrupt enabled 1 BWT_ERR interrupt masked (default)
10 RNACK_IM	Receiver NACK Threshold Interrupt Mask Used to enable/disable the ability of the RTE flag in the RX_STATUS register to generate EMV SIM interrupts. 0 RTE interrupt enabled 1 RTE interrupt masked (default)
9 CWT_ERR_IM	Character Wait Time Error Interrupt Mask Used to enable/disable the ability of the CWT_ERR flag in the RX_STATUS register to generate EMV SIM interrupts. 0 CWT_ERR interrupt enabled 1 CWT_ERR interrupt masked (default)
8 GPCNT0_IM	General Purpose Timer 0 Timeout Interrupt Mask Used to enable/disable the ability of the GPCNT0_TO flag in the TX_STATUS register to generate EMV SIM interrupts. 0 GPCNT0_TO interrupt enabled 1 GPCNT0_TO interrupt masked (default)
7 TDT_IM	Transmit Data Threshold Interrupt Mask Used to enable/disable the ability of the TDTF flag in the TX_STATUS register to generate EMV SIM interrupts. 0 TDTF interrupt enabled 1 TDTF interrupt masked (default)
6 TFF_IM	Transmit FIFO Full Interrupt Mask Used to enable/disable the ability of the TFF flag in the TX_STATUS register to generate EMV SIM interrupts. 0 TFF interrupt enabled 1 TFF interrupt masked (default)

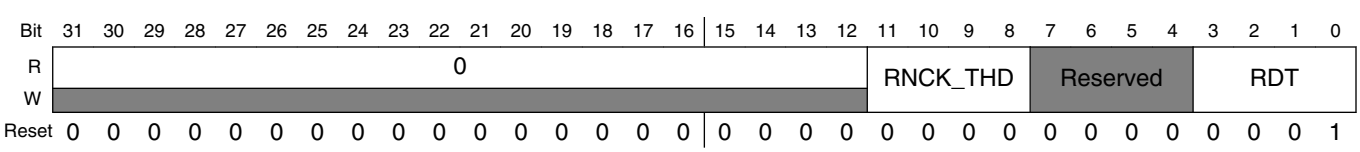
Table continues on the next page...

EMVSIMx_INT_MASK field descriptions (continued)

Field	Description
5 TNACK_IM	Transmit NACK Threshold Interrupt Mask Used to enable/disable the ability of the TNTE flag in the TX_STATUS register to generate EMV SIM interrupts. 0 TNTE interrupt enabled 1 TNTE interrupt masked (default)
4 TFE_IM	Transmit FIFO Empty Interrupt Mask Used to enable/disable the ability of the TFE flag in the TX_STATUS register to generate EMV SIM interrupts. 0 TFE interrupt enabled 1 TFE interrupt masked (default)
3 ETC_IM	Early Transmit Complete Interrupt Mask Used to enable/disable the ability of the ETC flag in the TX_STATUS register to generate EMV SIM interrupts. 0 ETC interrupt enabled 1 ETC interrupt masked (default)
2 RFO_IM	Receive FIFO Overflow Interrupt Mask Used to enable/disable the ability of the RFO flag in the RX_STATUS register to generate EMV SIM interrupts. 0 RFO interrupt enabled 1 RFO interrupt masked (default)
1 TC_IM	Transmit Complete Interrupt Mask Used to enable/disable the ability of the TCF flag in the TX_STATUS register to generate EMV SIM interrupts. 0 TCF interrupt enabled 1 TCF interrupt masked (default)
0 RDT_IM	Receive Data Threshold Interrupt Mask Used to enable/disable the ability of the RDTF flag in the RX_STATUS register to generate EMV SIM interrupts. 0 RDTF interrupt enabled 1 RDTF interrupt masked (default)

15.6.7 Receiver Threshold Register (EMVSIMx_RX_THD)

Address: Base address + 18h offset



EMVSIMx_RX_THD field descriptions

Field	Description
31–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11–8 RNCK_THD	Receiver NACK Threshold Value Used to specify the number of consecutive NACK's transmitted by the EMV SIM module, for a given character, before the receive threshold error (RTE) flag is triggered. A value of 0 indicates that RTE is never set. When a valid character is received by the EMV SIM, the internal counter keeping track of the NACK count resets to zero for the subsequent byte being received. If the ANACK bit is clear in the CNTL register, RNCK_THD has no effect. 0 Zero Threshold. RTE will not be set >0 RTE will set after programmed value of NACKs are received
7–4 Reserved	This field is reserved.
RDT	Receiver Data Threshold Value Determines the number of bytes that must exist in the Receive FIFO to trigger the receive data threshold interrupt flag (RDTF). Value must not exceed the total bytes that can be stored in the Receive FIFO.

15.6.8 Transmitter Threshold Register (EMVSIMx_TX_THD)

Address: Base address + 1Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																				TNCK_THD				0				TDT			
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

EMVSIMx_TX_THD field descriptions

Field	Description
31–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11–8 TNCK_THD	Transmitter NACK Threshold Value Used to set the NACK threshold for the transmitter. Once the threshold number set by TNCK_THD has been reached for the current byte being transmitted, the error flag TNTE in the TX_STATUS register will be set. Setting of TNTE causes the remaining transmissions queued in the transmit FIFO to be aborted and no more transmissions to occur until software clears TNTE. To trigger TNTE, a given byte being transmitted must reach the TNCK_THD threshold itself. Transmit NACKs accumulated on one byte are not carried over to the next. 0 TNTE will never be set; retransmission after NACK reception is disabled. 1 TNTE will be set after 1 nack is received; 0 retransmissions occurs. 2 TNTE will be set after 2 nacks are received; at most 1 retransmission occurs. 3 TNTE will be set after 3 nacks are received; at most 2 retransmissions occurs. . . . . . . N TNTE will be set after N nacks are received; at most (N - 1) retransmissions occurs.

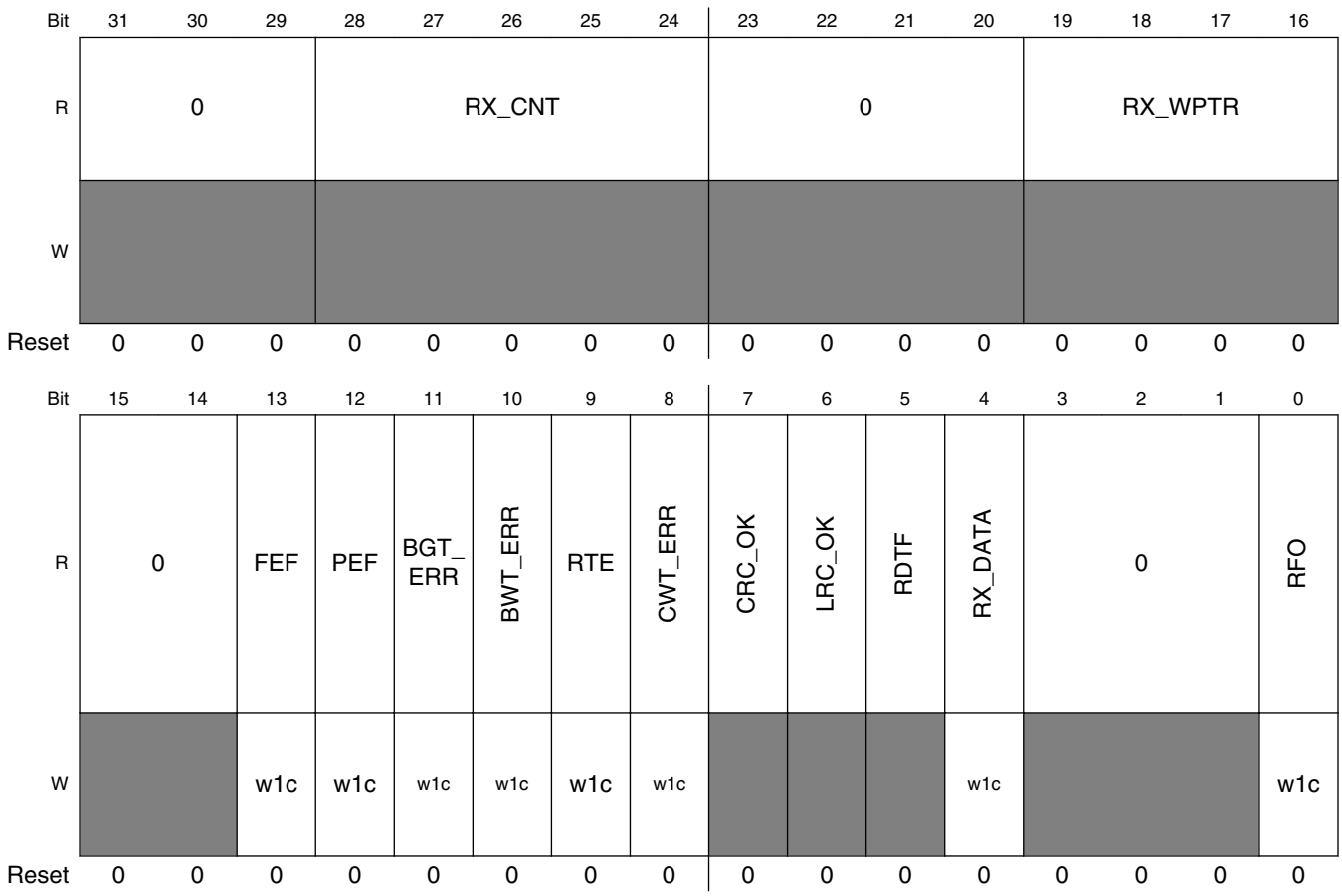
Table continues on the next page...

EMVSIMx_TX_THD field descriptions (continued)

Field	Description
	. . . . 15 TNTE will be set after 15 nacks are received; at most 14 retransmissions occurs.
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
TDT	Transmitter Data Threshold Value Used to set the threshold value for the Transmit FIFO at which the TDTF bit in the TX_STATUS register will be set. When the number of bytes in the Transmit FIFO is less than or equal to TDT[3:0], TDTF will be set.

15.6.9 Receive Status Register (EMVSIMx_RX_STATUS)

Address: Base address + 20h offset



EMVSIMx_RX_STATUS field descriptions

Field	Description
31–29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

EMVSIMx_RX_STATUS field descriptions (continued)

Field	Description
28–24 RX_CNT	Receive FIFO Byte Count These bits indicate the number of bytes stored in the receive FIFO. 0 FIFO is emtpy >0 Total bytes available in FIFO
23–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–16 RX_WPTR	Receive FIFO Write Pointer Value Value of write pointer of Receive FIFO
15–14 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
13 FEF	Frame Error Flag Used to indicate if the current received byte did not have proper STOP bits. This will not cause a NACK transmission. This bit will not cause an interrupt assertion. It is simply an indication that a framing error has occured. 0 No frame error detected 1 Frame error detected
12 PEF	Parity Error Flag Used to indicate if a received byte had a parity error or not. A parity error will cause transmission of NACK if ANACK bit is set in CTRL register and PEF bit will not be asserted. When ANACK is *not* set, PEF will be asserted. This bit will also not assert when ICM bit is set; however parity is checked in ICM = 1 mode. It is simply an indication that a parity error has occured. 0 No parity error detected 1 Parity error detected
11 BGT_ERR	Block Guard Time Error Flag Used to indicate if the block guard time was too small. The threshold is set by the block guard time register. 0 Block guard time was sufficient 1 Block guard time was too small
10 BWT_ERR	Block Wait Time Error Flag Used to indicate if the block wait time has been exceeded. The threshold is set by the block wait time registers. 0 Block wait time not exceeded 1 Block wait time was exceeded
9 RTE	Received NACK Threshold Error Flag Used to indicate whether the number of consecutive NACK's generated by the EMV SIM module in response to receive parity errors, for the byte being received, equals the value programmed in the RTH[3:0] in the RX_THRESHOLD register. This bit will never set unless the ANACK bit is set in the CNTL register. The SAPDx bit in the CNTL resister must be set to enable the threshold error to trigger the auto

Table continues on the next page...

EMVSIMx_RX_STATUS field descriptions (continued)

Field	Description
	power down sequence. RTE is a write once to clear bit. Clearing this bit also resets the internal counter for consecutive NACK's being transmitted for a given byte. 0 Number of NACKs generated by the receiver is less than the value programmed in RTH[3:0] 1 Number of NACKs generated by the receiver is equal to the value programmed in RTH[3:0]
8 CWT_ERR	Character Wait Time Error Flag Used to indicate when the time between received characters is equal to or greater than the value programmed in the CHAR_WAIT register. 0 No CWT violation has occurred (default). 1 Time between two consecutive characters has exceeded the value in CHAR_WAIT.
7 CRC_OK	CRC Check OK Flag Used to indicate when the calculated 16-bit CRC value matches the expected value for the current input data stream. The value is calculated across all received characters from the point the CRC_EN bit is set in the CTRL register. The current CRC residual can be reset by three mechanisms: • Clear CRC_EN bit in CTRL register • Set XMT_EN bit in ENABLE register • Automatically by hardware when ETC flag is set at the end of a transmission. 0 Current CRC value does not match remainder. 1 Current calculated CRC value matches the expected result.
6 LRC_OK	LRC Check OK Flag Used to indicate when the calculated 8-bit LRC value is correct for the current input data stream. The value is calculated across all received characters from the point the LRC_EN bit is set in the CTRL register. The current LRC residual can be reset by three mechanisms: • Clear LRC_EN bit in CTRL register • Set XMT_EN bit in ENABLE register • Automatically by hardware when ETC flag is set at the end of a transmission. 0 Current LRC value does not match remainder. 1 Current calculated LRC value matches the expected result (i.e. zero).
5 RDTF	Receive Data Threshold Interrupt Flag Interrupt flag asserted when total bytes in the Receive FIFO equal or is greater than the programmed receive threshold RDT[3:0]. The RDTF flag will be set any time the number of unread bytes in the receive FIFO is equal to or greater than the value set by RDT[3:0]. The flag can be cleared by reading enough bytes out of the receive FIFO so as to bring the number of bytes left in the FIFO below the RDT[3:0] level. Another way to clear the flag is to set the RDT[3:0] level higher than the number of unread bytes currently in the FIFO. The RDTF flag will create an interrupt if the RDT_IM bit in the INT_MASK register is cleared. 0 Number of unread bytes in receive FIFO less than the value set by RDT[3:0] (default). 1 Number of unread bytes in receive FIFO greater or than equal to value set by RDT[3:0].
4 RX_DATA	Receive Data Interrupt Flag Interrupt asserted when a new data byte is received and entered into the Receive FIFO. 0 No new byte is received 1 New byte is received ans stored in Receive FIFO

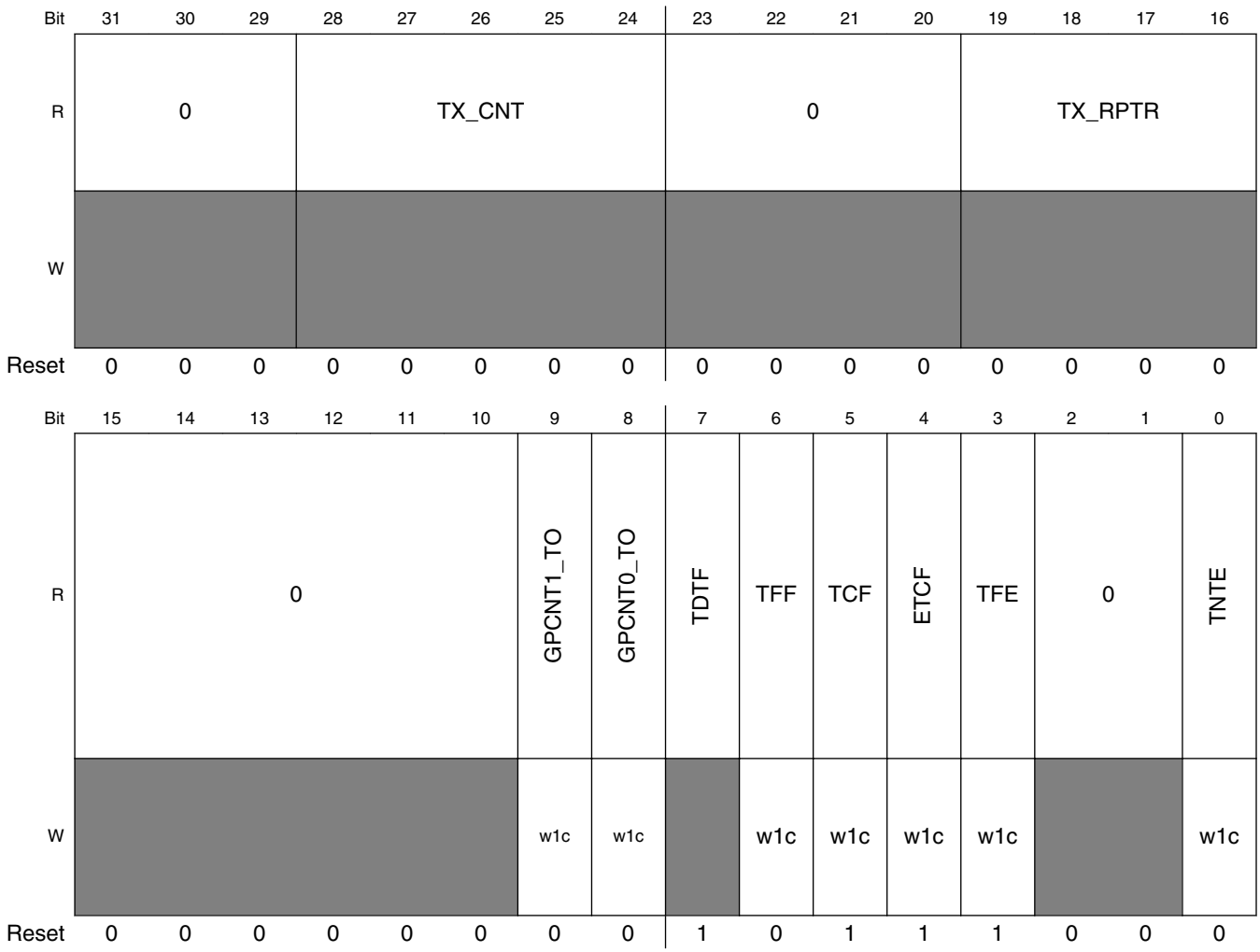
Table continues on the next page...

EMVSIMx_RX_STATUS field descriptions (continued)

Field	Description
3–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 RFO	Receive FIFO Overflow Flag Used to indicate that the EMV SIM was unable to store received data due to already unread bytes in the FIFO (FIFO full or almost full). It does not necessarily indicate that data has been lost. If the ONACK control bit in the CNTL register is set, there will be a NACK pulse generated on bytes that would otherwise cause a loss of data due to a full FIFO. These bytes should be retransmitted by the Smart Card which implies that no data has actually been lost. In this case, the RFO flag is just an indicator that this situation has occurred which may be helpful in system debug. For the case where ONACK is not set, a set RFO flag does indicate a loss of data since all bytes received with the OEF flag set will indeed be lost (including the byte that caused the bit to be set). The RFO flag will cause an interrupt if the RFO_IM bit in the INT_MASK register. The RFO flag is a write-one-to-clear bit. 0 No overrun error has occurred (default) 1 A byte was received when the received FIFO was already full

15.6.10 Transmitter Status Register (EMVSIMx_TX_STATUS)

Address: Base address + 24h offset



EMVSIMx_TX_STATUS field descriptions

Field	Description
31–29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28–24 TX_CNT	Transmit FIFO Byte Count These bits indicate the number of bytes stored in the transmit FIFO. 0 FIFO is emtpy >0 Total bytes in FIFO
23–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–16 TX_RPTR	Transmit FIFO Read Pointer

Table continues on the next page...

EMVSIMx_TX_STATUS field descriptions (continued)

Field	Description
	Value of the read pointer of transmit FIFO.
15–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9 GPCNT1_TO	General Purpose Counter 1 Timeout Flag Used to indicate when the General Purpose Counter 1 has reached the GPCNT1_VAL value in the GPCNT_VAL register. 0 GPCNT1_VAL time not reached, or bit has been cleared. (default) 1 General Purpose counter has reached the GPCNT1_VAL value
8 GPCNT0_TO	General Purpose Counter 0 Timeout Flag Used to indicate when the General Purpose Counter 0 has reached the GPCNT0_VAL value in the GPCNT_VAL register. 0 GPCNT0_VAL time not reached, or bit has been cleared. (default) 1 General Purpose counter has reached the GPCNT0_VAL value
7 TDTF	Transmit Data Threshold Flag Interrupt flag asserted when total bytes in the Transmit FIFO is less than or equal to the programmed transmit data threshold TDT[3:0]. The TDTF flag will be set any time the number of bytes in the transmit FIFO is less than or equal to the value set by TDT[3:0]. The flag can be cleared by writing enough bytes into the transmit FIFO so as to take the number of bytes in the FIFO above the TDT[3:0] level. Another way to clear the flag is to set the TDT[3:0] level lower than the number of bytes currently in the FIFO. The TDTF flag will create an interrupt if the TDT_IM bit in the INT_MASK register is cleared. 0 Number of bytes in FIFO is greater than TDT[3:0], or bit has been cleared 1 Number of bytes in FIFO is less than or equal to TDT[3:0] (default)
6 TFF	Transmit FIFO Full Flag Used to indicate when the Transmit FIFO has been written with maximum number of bytes that it can store. Subsequent writes may get ignored. The TFF bit can only be cleared by writing 1 to this bit or setting the FLUSH_XMT or SOFT_RESET bit in the RESET_CNTL register. 0 Transmit FIFO Full condition has *not* occurred (default) 1 A Transmit FIFO Full condition has occurred
5 TCF	Transmit Complete Flag Used to indicate whether the EMV SIM transmitter is ready for a new transmission. The TC flag becomes set when the guard time has expired after the last byte in the transmit FIFO (if XMT_CRC_LRC = 0) or the LRC or CRC byte (if XMT_CRC_LRC bit = 1) has been transmitted. The TC flag will create an interrupt if TC_IM in the INT_MASK register is low. The TC bit is a write-one-to-clear bit. 0 Transmit pending or in progress 1 Transmit complete (default)
4 ETCF	Early Transmit Complete Flag Used to indicate that the EMV SIM transmitter has finished sending the last byte in transmit FIFO (if XMT_CRC_LRC = 0) or finished sending the LRC or CRC byte (if XMT_CRC_LRC = 1). This bit differs from the TC bit in that it is set before the guard time of the last byte has elapsed. The ETC flag will create an interrupt if ETC_IM in the INT_MASK register is low. The ETC bit is a write-one-to-clear bit.

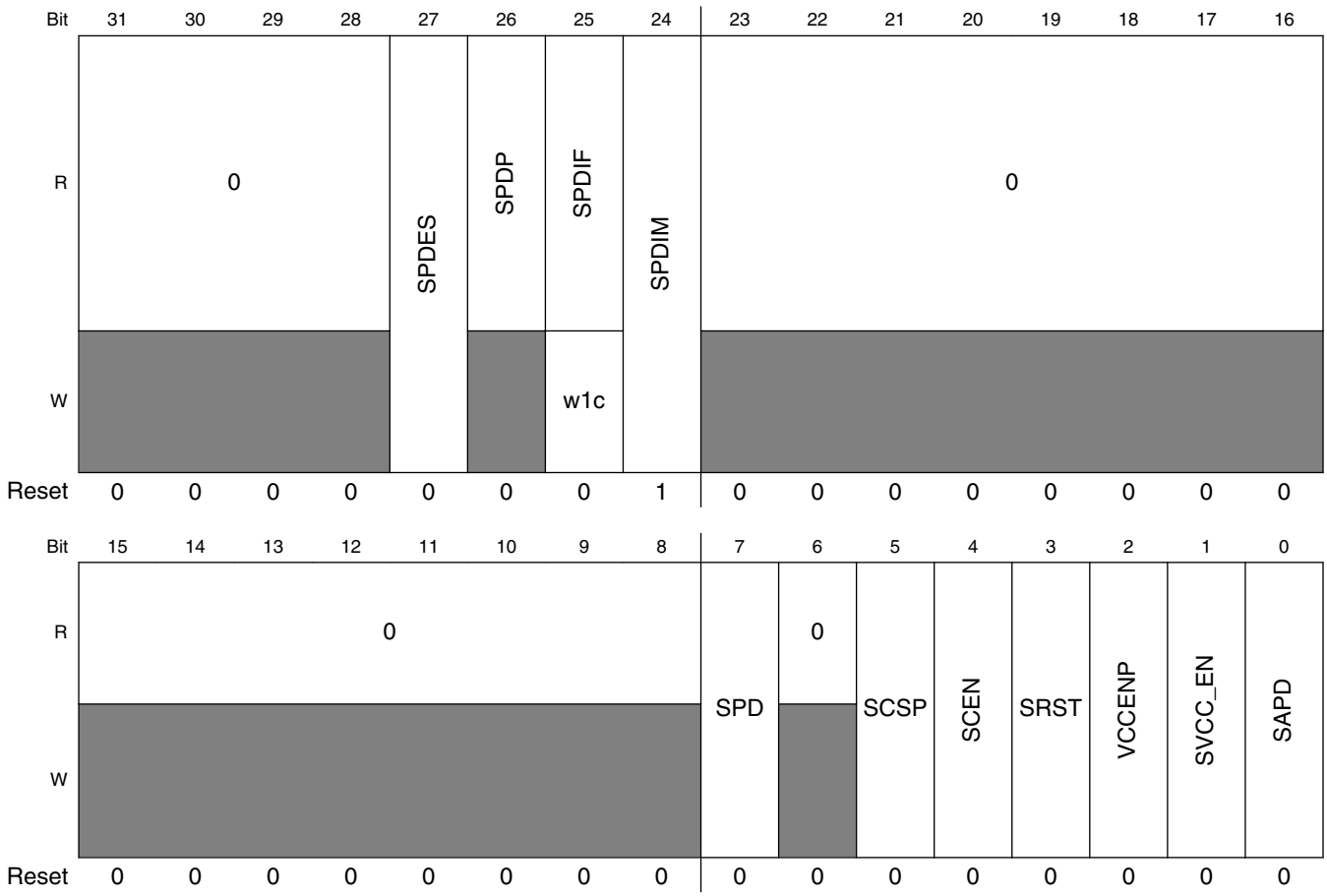
Table continues on the next page...

EMVSIMx_TX_STATUS field descriptions (continued)

Field	Description
	0 Transmit pending or in progress 1 Transmit complete (default)
3 TFE	Transmit FIFO Empty Flag Used to indicate that the EMV SIM transmit FIFO has been emptied. This bit will be set when the last byte in the transmit FIFO has been transferred out of the EMV SIM transmitter to the Smart Card successfully. TFE will also be set when the TNTE flag is set. The TFE flag will create an interrupt if TFE_IM in the INT_MASK register is low. The TFE bit is a write-one-to-clear bit. 0 Transmit FIFO is not empty 1 Transmit FIFO is empty (default)
2–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 TNTE	Transmit NACK Threshold Error Flag Used to indicate the transmit NACK threshold has been reached. When TNTE is high, no further transmissions will be done until the TNTE flag is cleared. Any data transmissions still pending in the transmit FIFO will be aborted, and the TC, ETC, and TFE flags will be set. The TNTE flag will create an interrupt if TNACK_IM in the INT_MASK register is low. The TNTE bit is a write-one-to-clear bit. 0 Transmit NACK threshold has not been reached (default) 1 Transmit NACK threshold reached; transmitter frozen

15.6.11 Port Control and Status Register (EMVSIMx_PCSR)

Address: Base address + 28h offset



EMVSIMx_PCSR field descriptions

Field	Description
31–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27 SPDES	SIM Presence Detect Edge Select Controls which edge of the Smart Card Presence Detect pin is used to detect the presence of the Smart Card. 0 Falling edge on the pin (default) 1 Rising edge on the pin
26 SPDP	Smart Card Presence Detect Pin Status This bit reflects the state of the Smart Card Presence Detect pin. It is not a latched register bit, but instead a synchronized version of the state of the pin itself. 0 SIM Presence Detect pin is logic low 1 SIM Presence Detectpin is logic high

Table continues on the next page...

EMVSIMx_PCSR field descriptions (continued)

Field	Description
25 SPDIF	Smart Card Presence Detect Interrupt Flag Status flag to indicate that an insertion or removal of a Smart Card has been detected on port. Can create an interrupt to the MCU if SPDIM is low and/or initiate the auto power down sequence if SAPD bit is '1'. Write a '1' to this bit to clear. 0 No insertion or removal of Smart Card detected on Port (default) 1 Insertion or removal of Smart Card detected on Port
24 SPDIM	Smart Card Presence Detect Interrupt Mask Interrupt mask for the presence detect interrupt flag (SPDIF). 0 SIM presence detect interrupt is enabled 1 SIM presence detect interrupt is masked (default)
23–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 SPD	Auto Power Down Control Writing a '1' to this location will start the autopower down sequence provided the auto power down feature is enabled by writing '1' to SAPD bit of this register. The SPD bit will autoclear when power down is complete. 0 No effect (default) 1 Start Auto Powerdown or Power Down is in progress
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 SCSP	Smart Card Clock Stop Polarity Used to control the polarity of the idle EMV SIM clock when the clock is disabled by SCEN. 0 Clock is logic 0 when stopped by SCEN 1 Clock is logic 1 when stopped by SCEN
4 SCEN	Clock Enable for Smart Card Used to enable/disable the clock to the Smart Card. It can be forced low by hardware during the auto power down sequence. 0 Smart Card Clock Disabled 1 Smart Card Clock Enabled
3 SRST	Reset to Smart Card Used to control state of reset line to the Smart Card. It can be forced low by hardware during the auto power down sequence. Smart Card reset signals are active low. 0 Smart Card Reset is asserted (default) 1 Smart Card Reset is de-asserted
2 VCCENP	VCC Enable Polarity Control Used to control the polarity of the SVEN output pad via the SVCC_EN bit. When set to '1', this bit will invert the value of SVCC_EN bit of this register and output to SVEN output pad of device.

Table continues on the next page...

EMVSIMx_PCSR field descriptions (continued)

Field	Description
	0 VCC_EN is active high. Polarity of SVCC_EN is unchanged. 1 VCC_EN is active low. Polarity of SVCC_EN is inverted.
1 SVCC_EN	Vcc Enable for Smart Card Used to control the state of the SVEN pin on Smart Card port. The SVEN pin controls the Smart Card Vcc enable in the power management chip. It can be forced low by hardware during the auto power down sequence. This bit is XORed with the VCCENP bit to control the polarity of the SVEN output pad. 0 Smart Card Voltage disabled (default) 1 Smart Card Voltage enabled
0 SAPD	Auto Power Down Enable Used to enable/disable the auto power down feature. This bit must be set prior to the auto power conditions are met. This bit will be return to 0 at the end of the auto power down sequence. This bit controls the auto power down function which can be initiated by: • Setting the SPD bit in this register by software • Assertion of the RTE bit in the RX_STATUS register • Assertion of the SPDIF bit when the interrupt is used for detecting card removal Manual Power Down via software by writing to the SCEN, SRST, and VCC_EN can still be carried out irrespective of the value of this bit. 0 Auto power down disabled (default) 1 Auto power down enabled

15.6.12 Receive Data Read Buffer (EMVSIMx_RX_BUF)

Address: Base address + 2Ch offset

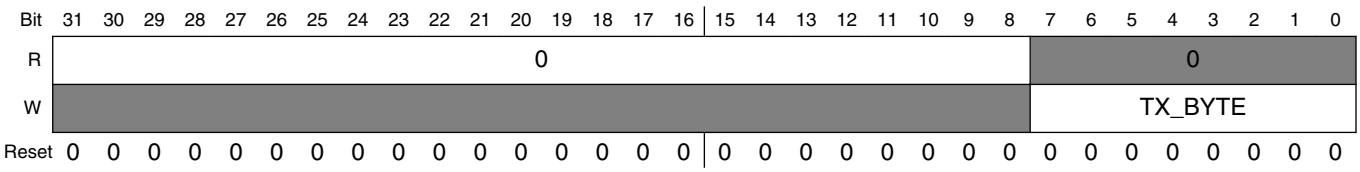
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																								RX_BYTE							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EMVSIMx_RX_BUF field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
RX_BYTE	Receive Data Byte Read Provides the byte value from the top of the receive FIFO. Each read access to this register will increment the read pointer of the Receive FIFO.

15.6.13 Transmit Data Buffer (EMVSIMx_TX_BUF)

Address: Base address + 30h offset

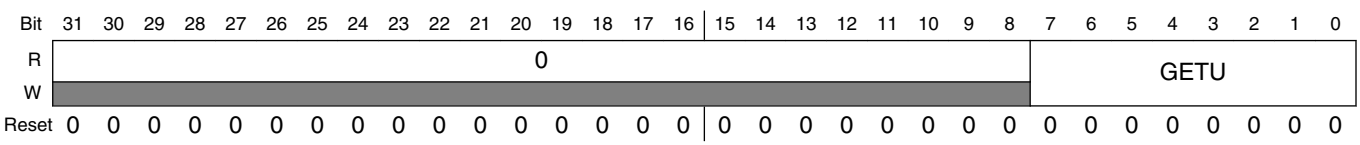


EMVSIMx_TX_BUF field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
TX_BYTE	Transmit Data Byte Write to this register to fill the transmit FIFO with the bytes to be transmitted. The Tx FIFO can be written to only when the transmitter is enabled. Writing to this register while transmitter is disabled will lead to ignoring of all write accesses to this register. Reads to this register will return zeros. **NOTE:** Writing more data to the transmit FIFO than it can hold, will cause a Transmit FIFO Full (TFF) error.

15.6.14 Transmitter Guard ETU Value Register (EMVSIMx_TX_GETU)

Address: Base address + 34h offset



EMVSIMx_TX_GETU field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
GETU	Transmitter Guard Time Value in ETU Used to control the number of additional Elementary Time Units (ETUs) inserted between bytes transmitted by the EMV SIM transmitter. An ETU is equivalent to one bit time at the given baud rate (for example, the length of a START bit). The guard time has no effect on the EMV SIM receiver. A value of 0x00 inserts no additional ETUs, while a value of 0xFE inserts 254 additional ETUs. A value of 0xFF subtracts one ETU by reducing the number of STOP bits from two to one. 0 no additional ETUs inserted (default) 1 1 additional ETU inserted ... 254 254 additional ETUs inserted 255 Subtracts one ETU by reducing the number of STOP bits from two to one

15.6.15 Character Wait Time Value Register (EMVSIMx_CWT_VAL)

Address: Base address + 38h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																CWT															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

EMVSIMx_CWT_VAL field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CWT	Character Wait Time Value The value written to this register will specify the number of ETU times allowed between characters. Default is 0xFFFF

15.6.16 Block Wait Time Value Register (EMVSIMx_BWT_VAL)

Address: Base address + 3Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BWT																															
W																																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

EMVSIMx_BWT_VAL field descriptions

Field	Description
BWT	Block Wait Time Value The time from START bit of last byte sent from the EMV SIM module to the START bit of the first byte sent from the Smart Card must be less than the value in this register. If it is not, then the BWT_TO flag is set.

15.6.17 Block Guard Time Value Register (EMVSIMx_BGT_VAL)

Address: Base address + 40h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																BGT															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EMVSIMx_BGT_VAL field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
BGT	Block Guard Time Value The value in this register is the block guard time. Time from START bit of last byte sent from the EMV SIM module to the START bit of the first byte sent from the SmartCard must be greater than this value. If it is not, then the BGT flag will be set.

15.6.18 General Purpose Counter 0 Timeout Value Register (EMVSIMx_GPCNT0_VAL)

Address: Base address + 44h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																GPCNT0																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

EMVSIMx_GPCNT0_VAL field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
GPCNT0	General Purpose Counter 0 Timeout Value The value written to this register will be used to compare to the general purpose counter 0 in the EMV SIM module. Once the General purpose counter reaches this value, the GPCNT0 flag in the TX_STATUS register will be set. This counter is intended to be used for any events that must be monitored for duration based on the card clock, receiver sample rate, or ETU rate (transmit clock). Example: ATR arrival time and ATR duration.

15.6.19 General Purpose Counter 1 Timeout Value (EMVSIMx_GPCNT1_VAL)

Address: Base address + 48h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																GPCNT1																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

EMVSIMx_GPCNT1_VAL field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
GPCNT1	General Purpose Counter 1 Timeout Value The value written to this register will be used to compare to the general purpose counter in the EMV SIM module. Once the General purpose counter reaches this value, the GPCNT1 flag in the XMT_STATUS register will be set. This counter is intended to be used for any events that must be monitored for duration based on the card clock, receiver sample rate, or ETU rate (transmit clock). Example: ATR arrival time and ATR duration.

15.7 Functional Description

15.7.1 Initialization

15.7.1.1 Configuring EMV SIM

The first operation that must be done is to configure the EMV SIM interface signals to allow the EMV SIM Transmit or Receive operation to commence. The following steps describe a typical way to enable the Smart Card:

- Configure prescaler by programming the desired value in PRSC register to generate the card clock. The card clock frequency is calculated as:
  - f_{SIM} / (PRSC[7:0]); where f_{SIM} is the EMV SIM Clock Frequency
  - Prescaler value must be set such that the maximum card clock frequency specification set by EMV & ISO-7816 specifications are not violated
- Configure the DIVISOR_VALUE in the Baud Rate Divisor Register. This value determines the ETU period to be used by the transmitter or receiver
- Enable power to the Smart Card by setting the VCC_EN bit in PCSR register
- Enable the Smart Card clock by setting the SCEN bit in PCSR register
- Release Smart Card reset using the SRST bit in PCSR register to bring the Smart Card out of reset
- Program the power down functionality i.e. if Auto Power Down of Smart Card is required or not
- Select the Data Format type for the EMV SIM
  - Either set the IC bit to the desired data format (inverse or direct) OR
  - Set the ICM bit to allow automatic detection of Initial Character. IC bit will be updated to desired data format upon valid Initial Character detection

- Configure if the EMV SIM module is enabled to run in STOP and DOZE modes by setting the STOP_EN and DOZE_EN bits as desired
- Enable DMA request generation for Transmitter or Receiver as desired

Once the above configuration is complete, the receiver or transmitter can be configured depending on the operation to be carried out on the Smart Card.

NOTE

XMT_EN and RCV_EN bits should not be changed in the same write cycle. Software should attempt separate write accesses to CTRL register for updating these bits, one by one. For example, if XMT_EN = 1 and RCV_EN = 0 and in order to enable the receiver, first write to CTRL register should make XMT_EN = 0 and second write to CTRL register should make RCV_EN = 1.

15.7.1.2 Configuring Receiver

The following is a list of configurations that need to be performed (after the "Configuring EMV SIM" step) in order to configure the EMV SIM receiver for operation:

- Enable NACK generation capability
  - To generate NACK on parity errors and invalid initial characters, set the ANACK bit in CTRL register
  - To generate NACK on receiver FIFO overflow error, set the ONACK bit in CTRL register
- Configure the desired threshold for NACK generation and data threshold in the RX_THD register. These are the thresholds at which the RTE and RDTF flags will be set, respectively.
  - If auto power down is desired on RTE flag assertion, then write to SAPD bit PCSR to initiate the Smart Card power down
- Configure the timeout values for Character Wait Time Counter, the Block Wait Timer Counter and the Block Guard Time Counter
- Enable necessary interrupts by clearing respective bits in the INT_MASK register
- Configure the General Purpose Counter as needed and select desired clock source (GPCNT0/1_CLKSEL in the CLKCFG register)
- Enable Receiver by setting RCV_EN bit to 1 in CTRL register
- Receiver will enter Initial Character Detection mode if ICM bit is set or enter normal receive mode if ICM bit is not set
- Enable LRC or CRC as desired

15.7.1.3 Configuring Transmitter

The following is a list of configurations that need to be performed (after the "Configuring EMV SIM" step) in order to configure the EMV SIM transmitter for operation:

- Select desired re-transmission threshold for NACKed characters in TX_THD register
  - This is the threshold at which the TNTE flag will be set by using the TNACK_THD[3:0] bits
- Configure the desired Guard Time between the characters transmitted by writing to the GETU[7:0] bits in TX_GETU register
- Configure the desired data threshold in TX_THD register.
- Enable necessary interrupts by clearing respective bits in the INT_MASK register
- Configure the General Purpose Counter as needed and select desired clock source (GPCNT0/1_CLKSEL in the CLKCFG register)
- Enable Transmitter by setting the XMT_EN in the CTRL register
- Enable LRC & CRC as desired
- Program bytes to be transmitted into the Tx FIFO. If DMA is enabled, DMA request will get asserted automatically.

NOTE

Tx FIFO can be written to after the transmitter is enabled (XMT_EN = 1). Writing to Tx FIFO while transmitter is disabled will not be successful and write access will be ignored.

NOTE

The Transmit and Receive operations are mutually exclusive and should not be enabled together.

15.7.2 Smart Card Interface and Control

The EMV SIM module controls the all the interface signals for the Smart Card. The Smart Card clock is generated using the prescaler (PRSC register) and the ETU periods are generated using the baud rate divisor (DIVISOR register). The Smart Card Reset and Voltage Enable are controlled by software through the PCSR register. The message bytes are transmitted and received on the Card IO device pin which is used in open drain configuration.

15.7.2.1 Smart Card Presence Detect

The Smart Card Presence Detect pin (SIMPD) allows for detection of the insertion or removal of a Smart Card. The SPDES bit in the PCSR register allows the software to configure which edge of the SIMPD pin will cause a presence detect interrupt flag to be asserted.

An internal pull-down is required on SIMPD pin to allow a high to low transition on this pin when the Smart Card is removed.

15.7.2.2 Powering Up

The first step to communicating with a Smart Card is to provide power and a clock signal to the card. Once the card is detected as present (using the presence detect features, or some other method), the Smart Card should be powered up according to the power up sequence specified in the ISO 7816-3 specification.

1. Apply voltage to the Smart Card by setting the VCC_EN bit in the PCSR register.
2. Select the appropriate clock frequency for the Smart Card by programming the CLKCFG and DIVISOR registers.
3. Enable the clock to the Smart Card by setting the SCEN bit in the PCSR register.
4. Remove the card from reset by setting the SRST bit in the PCSR register.

15.7.2.3 Automatic Power Down

Smart Cards require a proper sequence of operations to be followed to allow them to be powered down. The power down sequence as per ISO 7816 specifications is:

- Smart Card Reset (RST) pin transitions from high to low
- Smart Card Clock (CLK) is turned off to low
- Smart Card IO (IO) is transitioned from high impedance to low
- Smart Card Voltage Enable (VCC_EN) to turned off (pin driven low)

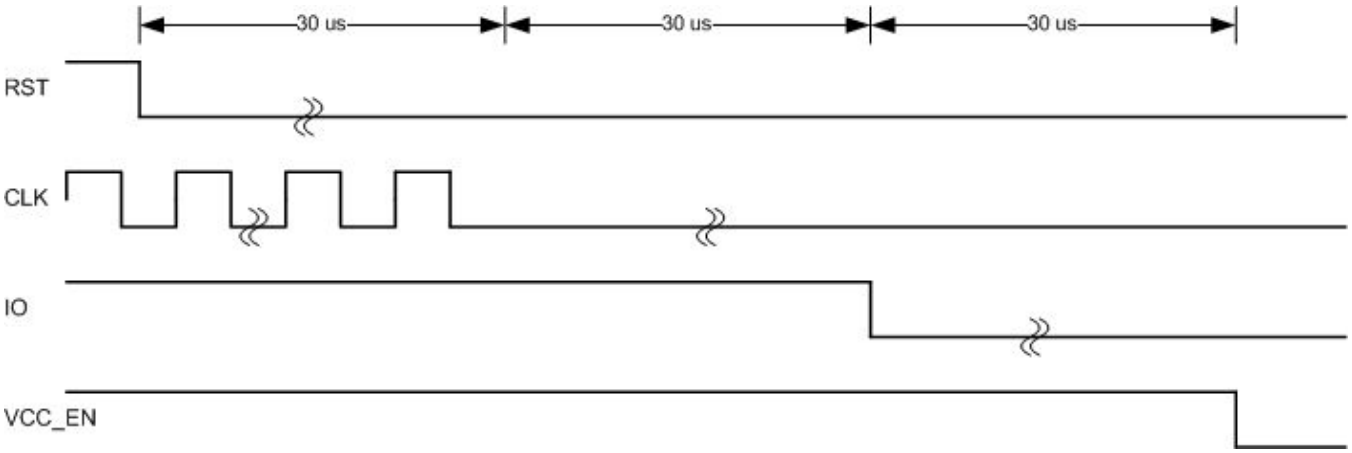


Figure 15-2. Auto Power Down Sequence

These operations can be done manually by software by writing to appropriate bits (SCEN, SRST and VCC_EN) in the PCSR register or automatically by hardware under the following conditions provided the auto power down feature is enabled in the PCSR register.

- Setting the SPD bit in PSCR register by software
- Assertion of RTE bit in RX_STATUS register
- Assertion of SPDIF bit in PCSR register when configured to detect card removal
- Power Fail indication from on-chip power management controller

NOTE

The SPDES bit in PCSR register determines which edge transition of the Smart Card Presence Detect pin is used for Smart Card presence detection. Presence detection can be used to determine if the card has been inserted or removed. The occurrence of the edge specified by SPDES bit will cause the following: SPDIF to be set; if the SPDIM mask is clear, an interrupt to the CPU; and if SAPD in the PCSR register is set, an auto power down sequence to begin. If Smart card insertion is expected, SAPD can be set low to avoid the auto power down sequence from falsely triggering. The bit SPDP can be used to determine the current state of the Smart Card Presence Detect pin.

NOTE

The auto power down operation requires a low frequency clock (usually 32 kHz clock source and selected by by SIM_SOPT1[OSC32KSEL]) to be active on the device.

The auto power down sequence will clear the following register bits upon power down sequence completion:

- SPD bit in PCSR register
- SCEN bit in PCSR register
- SRST bit in PCSR register
- VCC_EN bit in PCSR register
- XMT_EN and RCV_EN bits in CTRL register

15.7.3 EMV SIM Receiver

The EMV SIM Receiver is designed to receive all message bytes and store valid bytes into the receive FIFO. It performs checks on the incoming messages and indicates the transmitter to enable NACK insertion for each message. In addition, the receiver automatically detects NACKs received when the transmitter is sending out message bytes.

15.7.3.1 Data Sampling

The incoming data is internally synchronized and sampled using a 16x oversampled clock, called the EMV SIM logic clock. The frequency of this clock is 16 times the ETU Clock (1/ETU Period). The whole receiver works on this EMV SIM logic clock.

15.7.3.2 Initial Character Detection

The EMV SIM module supports the detection of the Initial Character and determine the data format when it is placed in the initial character mode by setting the ICM bit in CTRL register. When placed in this mode, the EMV SIM module samples in the input line and waits for one of the initial characters to be detected. Once detected, the ICM bit is cleared and the data format bit, IC bit, is set to appropriate value depending on the data format detected using the initial character.

The two possible data formats are inverse convention and direct convention. Figures below illustrate the differences between the two formats. Essentially, inverse convention differs from direct convention in that the order of the bits is flipped (i.e. MSB for LSB) and the data bits and parity bit are logically inverted. When receiving inverse convention data, the transformation of the data back to direct convention format is done in hardware, including the inversion of the data and parity bits.

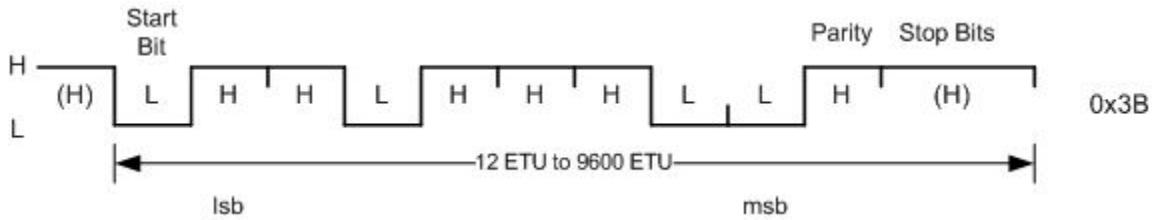


Figure 15-3. Initial Character in Direct Conversion

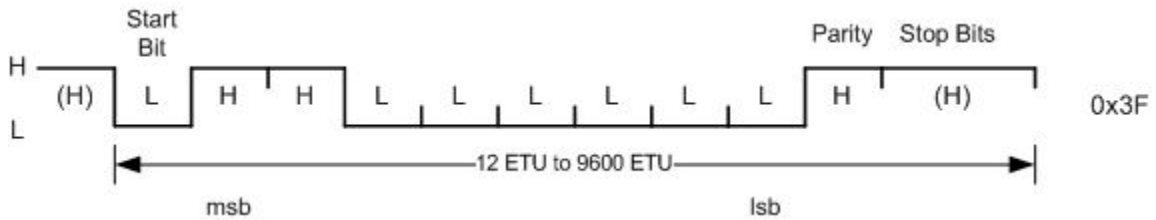


Figure 15-4. Initial Character in Inverse Conversion

To place the EMV SIM into initial character mode, set the ICM bit in the CTRL register. Once a valid initial character is received, the IC bit in the CTRL register will be set accordingly by the hardware, and the ICM bit will be cleared. Software can read the state of the IC bit to determine which mode the EMV SIM is currently using. The 0x3B (as decoded by direct convention) with parity bit high will cause direct convention to be used (IC set to logic 0), whereas a 0x3F (as decoded by inverse convention) with parity bit high will cause inverse convention to be used (IC set to logic 1).

The receiver remains in initial character mode until disabled by software or a valid initial character is detected. Upon detection of valid character, the receiver enters data receive mode. It is recommended to use one of the general purpose counter as a timeout during initial character mode.

When the receiver is in initial character mode, all received bytes will continue to be placed into the receive FIFO whether they be valid initial characters or not. If a valid initial character is received that causes the data format being used to change, all subsequent bytes will be decoded with that format before being placed into the FIFO, including the initial character byte itself. That is, if the IC bit is low, and the correct initial character for setting inverse convention is received, that character and all subsequently received characters will be stored in the FIFO after having been decoded using inverse convention (for example, the initial character will be stored as 0x3F).

NOTE

There is a condition where a parity error in the initial byte for direct convention (0x3B) could be decoded as what appears to be a valid initial character for inverse convention (that is, 0x3F). The EMV SIM module will not recognize this as a valid

initial character for inverse convention and will set the PEF flag.

15.7.3.3 Receiver Diagnostics

The EMV SIM module performs diagnostic checks on the incoming messages. These checks include parity check and message frame checks.

Parity Error Detection: The receiver is responsible for detecting parity errors in the received data. Data is always transmitted with even parity, except when in inverse convention mode. In inverse convention mode, all data bits and the parity bit are complemented making the data appear to be odd parity. The parity bit is defined as the 10th bit of the received data. The parity of the 2nd through 10th received bits is calculated by the receiver parity logic. This logic determines if the parity of the 9 received bits is correct.

When a parity error is detected on a given byte, the parity error flag (PEF bit) is asserted in the RX_STATUS register if NACK generation on errors is disabled (ANACK = 0 in CTRL register). The parity error flag does not generate an interrupt to the system, however, the module can cause the transmitter to transmit a NACK (if ANACK = 1 in CTRL register) without software needed to enable transmitter for this and request re-transmission of the current byte.

Framing Error Detection: The receiver is responsible for detecting framing errors in the received data. Data is always transmitted with 2 STOP bits, except when in 11 ETU mode, where there is one STOP bit. The STOP bits are defined as high state at the 11th and 12th bit positions in the received data. In either mode, the receiver expects to see a high at the 11th bit position in the received data. If a low is detected at the 11th bit position, the receiver indicates a framing error for that byte.

When a framing error is detected on a given byte, the FEF bit is set in the RX_STATUS register. A framing error cannot cause an interrupt, nor can it create a NACK pulse to the Smart Card asking for a retransmission of the corrupted data.

LRC & CRC: The receiver also checks the LRC or CRC on the incoming block of bytes (if LRC or CRC is enabled). The result of the CRC or LRC check is updated in the RX_STATUS register once the complete message block is received.

15.7.3.4 NACK Detection

During transmission of message bytes, the receiver automatically checks for NACKs sent by the Smart Card. The software does not need to enable receiver for this. The NACK is detected by sampling the IO line at 11 ETUs after the falling edge of the START bit. Once a NACK is detected, the transmitter is signaled and the transmitter will retransmit the current byte after two ETU time (as per ISO 7816 specification).

15.7.3.5 Using EMV SIM Receiver with "T=1" Smart Cards

The EMV SIM module provides hardware support for “T=1” type Smart Cards. These type of cards present several requirements above and beyond the standard “T=0” cards. The features provided to meet the requirements that pertain to the EMV SIM receiver are as follows:

- 11 ETU Characters
  - “T=1” cards can transmit with character lengths of 11 ETUs (that is, one STOP bit). The EMV SIM module provides the RCVR11 bit in the CTRL register in order to configure the receiver state machine to accept 11 ETU characters.
- Character Wait Time Counter
  - The character waiting time (CWT) is defined as the time between the start bits of two consecutive characters received from the Smart Card. The value of CWT can range from 12 ETU to 32779 ETU. The EMV SIM module provides a 16-bit counter with programmable comparator clocked at the ETU bit rate to identify when the CWT has been exceeded by the Smart Card.
- Block Wait Time
  - The block waiting time (BWT) is defined as the maximum time between the start bits of the last character of a transmitted block and the first character of the next received block. The block wait time must not exceed a value that is programmable. The EMV SIM module provides a 32-bit Block Wait Timer that can be used to identify when the BWT has been violated.
- Block Guard Time
  - The block guard time (BGT) is defined as the minimum delay between the start bits of the last character of a transmitted block and the first character of the next received block. The block guard must be greater than a value that is programmable. The EMV SIM module provides a 16-bit Block Guard Timer that can be used to identify when the BGT has been violated.
- Error Detection Code
  - “T=1” cards can specify LRC or CRC error detection codes to be used. The EMV SIM module provides hardware support for both the LRC and CRC operations.

15.7.4 EMV SIM Transmitter

The transmitter is responsible for reading the message bytes from the Tx FIFO, adding the LRC or CRC at the end of the message block and re-transmit any byte on reception of a NACK. It assists the receive operation by inserting NACKs when directed by the receiver.

15.7.4.1 Message Transmission

The transmitter operation does not start until the Tx FIFO is empty. Software can configure the EMV SIM module and enable the transmitter but unless a byte is written into the Tx FIFO, no transmission will start. Clearing the XMT_EN bit while the transmitter is in operation, will halt any transmission in progress, flush the transmit FIFO. Refer Message Handling section for more details on using the Tx FIFO.

The transmitter continuously transmits the messages from the Tx FIFO. Upon NACK detection, the transmitter resends the same byte until the Transmitter NACK Threshold limit is reached. When TNTE is set, the EMV SIM transmitter is halted, and all pending transfers are aborted, and the TC, ETC, AND TFE flags are set. All bytes remaining in the transmit FIFO are lost. There is no way to restart the transmission on the next byte in the FIFO. The transmitter remains frozen until TNTE is cleared by software. The only way to clear TNTE is to write a 1 to the TNTE bit in the TX_STATUS register. It is possible to disable the detection of NACKs from the Smart Card by setting TNCK_THD[3:0] to 0x0. By setting TNCK_THD[3:0] to 0x1, it is possible to disable all retransmissions while still setting TNTE on the first NACK received. In general, TNTE is set on the NACK that causes the threshold set by TNCK_THD[3:0] to be reached. This final NACK will not cause a retransmission, whereas all previous NACKs will cause a retransmission.

If all bytes are successfully transmitted and the Tx FIFO is empty, the transmitter send the check byte (i.e. LRC or CRC) if the XMT_CRC_LRC and LRC_EN or CRC_EN bits are set. The transmitter sends each byte to the LRC or CRC block to allow the check byte generation.

At the end of each byte, the transmitter inserts the programmed Guard ETUs. Refer to Protocol Timers section for more details on Guard Time Counter.

15.7.4.2 NACK Insertion

The transmitter is responsible for driving the output low during the STOP bit time to signify an error was detected in the received data from the Smart Card. This logic responds to a NACK request generated by the receiver block.

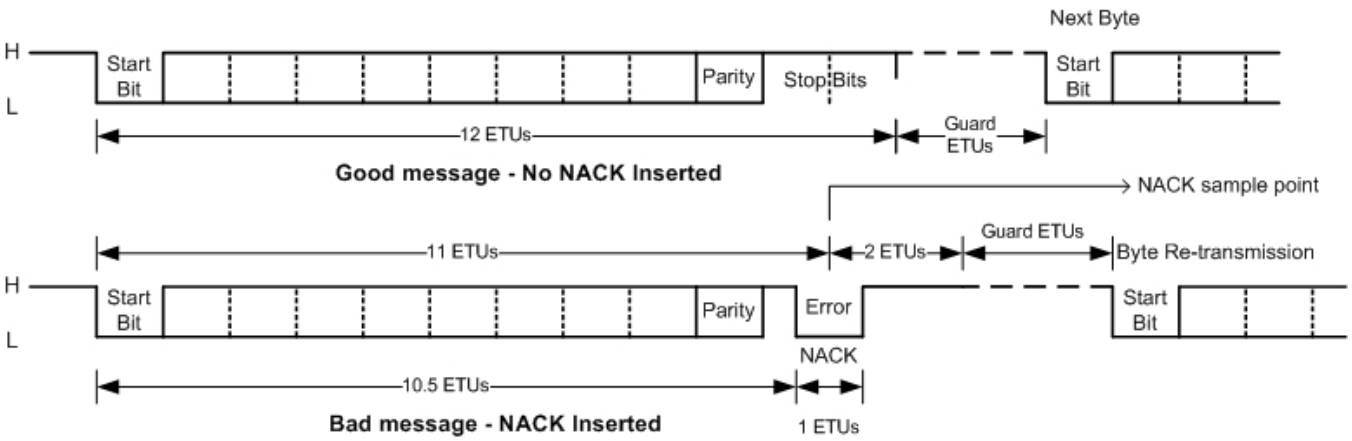


Figure 15-5. NACK Insertion

The NACK generation logic is also responsible for keeping track of the number of NACKs received during a transmit operation. The receiver detects NACKs generated by the Smart Card, and reports them to the transmit NACK logic. Once the number of detected NACKs has reached the programmed threshold (TNCK_THD[3:0]), an interrupt flag (TNTE) is generated, the transmit FIFO is flushed, and the transmitter is disabled.

15.7.4.3 Using EMV SIM Transmitter with "T=1" Smart Cards

The EMV SIM module provides hardware support for “T=1” type Smart Cards. These type of cards present several requirements above and beyond the standard “T=0” cards. The features provided to meet the requirements that pertain to the EMV SIM transmitter are as follows:

- 11 ETU Characters
  - The EMV SIM module transmitter has a programmable guard time register that allows the programmer to specify the number of ETUs between character transmissions. Programming a value of 255 (0xFF) in the GETU[7:0] bits in the GUARD_CNTL register will set the number of ETUs per character transmitted to 11.
- Character Waiting Time
  - The character waiting time (CWT) is defined as the time between the start bits of two consecutive characters. The value of CWT can range from 12 ETU to 32779 ETU. The time between transmitted characters is controlled by the

programmable guard time in the GETU register. However, the time between the last byte in the transmit FIFO, and the next transmitted byte can be largely affected by software response time to the transmit interrupts. The EMV SIM transmitter provides a Transmit FIFO threshold (TDTF) interrupt to signal the system when the expected number of characters have been transmitted from the transmit FIFO. The minimum CWT is achieved only if the software can respond to the TDTF interrupt and write new data to the transmit FIFO before the last character in the Transmit FIFO has been sent.

- Block Waiting Time
  - The block waiting time (BWT) is defined as the maximum time between the start bits of the last character of a transmitted block and the first character of the next received block. The value of BWT is always greater than 1800 ETU. The EMV SIM transmitter provides two General Purpose Counter(s) either of which can be used to track the BWT. The BWT is purely determined by software response time to the transmit interrupts.
- Block Guard Time
  - The block guard time (BGT) is defined as the minimum delay between the start bits of the last character of a transmitted block and the first character of the next received block. The value of BGT is 22 ETU. The EMV SIM module supports the BGT by providing the ability to generate an interrupt when the last byte is received, and transmitting within 2 ETU after the XMT_EN bit is set. The BGT will be determined by the speed at which the software can react to an interrupt and enable the transmitter.
- Error Detection Code
  - “T=1” cards can specify LRC or CRC error detection codes to be used. The EMV SIM module provides hardware support for both the LRC and CRC operation.

15.7.5 LRC and CRC

15.7.5.1 LRC Block

The EMV SIM module provides an 8-bit Linear Redundancy Check (LRC) generator / checker. The block is provided for use with T=1 Smart Cards that support LRC. This block can be enabled through the LRC_EN bit in the CNTL register. This block performs an 8-bit exclusive-OR on all received or transmitted characters. At the end of the reception of a block of characters, the result is expected to be 00. If so, the LRC_OK bit is set in the RX_STATUS register. During transmission, the LRC block Exclusive-ORs

each character that is transmitted with the current value of the LRC. If the XMT_CRC_LRC bit in the CTRL register is set, the LRC value will automatically be sent by the transmitter as the final character when the transmit FIFO empties.

The LRC value can be reset in multiple ways. Clearing the LCR_EN bit in the CTRL register will reset the LRC value. At the end of a transmission (either after the LRC byte is transmitted, or after the last character in the transmit FIFO is sent when XMT_CRC_LRC is clear), the LRC value is automatically reset by the EMV SIM hardware. Finally, when setting the XMT_EN bit, the EMV SIM hardware resets the LRC value.

Summary of configuration needed to use LRC block:

- Use the LRC_EN bit in CTRL register to enable the LRC block
- Use the XMT_CRC_LRC bit to enable the transmission of the LRC Character after the last character in the Transmit FIFO is sent.

15.7.5.2 CRC Block

The EMV SIM module provides an 16-bit Cyclic Redundancy Check (CRC) generator / checker. The block is provided for use with T=1 Smart Cards that support CRC. This block can be enabled through the CRC_EN bit in the CTRL register. This block performs a polynomial based check on all received or transmitted characters. The polynomial used for calculating the CRC is $G(x) = x^{16} + x^{12} + x^5 + 1$. The CRC register is initialized to all “1” before the data is shifted in. The CRC block can be configured to compute using the ISO 7816 CRC method or the 16-bit CCITT CRC method. The software can select the following bits: CRC_IN_FLIP, CRC_OUT_FLIP, and INV_CRC_VAL of the CTRL register.

- To select CCITT CRC method, set
  - CRC_IN_FLIP = 1
  - CRC_OUT_FLIP = 1
  - INV_CRC_VAL = 1
- To select normal CRC method (i.e. ISO 7816 CRC method), set
  - CRC_IN_VAL = 0
  - CRC_OUT_VAL = 0
  - INV_CRC_VAL = 1

During transmission, the CRC block updates the current value of the CRC using each character. If the XMT_CRC_LRC bit in the CTRL register is set, the CRC value will automatically be formatted as per the selected CRC method (CCITT or normal) and sent by the EMV SIM transmitter as the final two characters when the transmit FIFO empties. At the end of the reception of a block of characters, the residual from the CRC calculation is compared and the CRC_OK bit is set in the RX_STATUS register.

NOTE

Setting any other value for CRC_IN_FLIP, CRC_OUT_FLIP and INV_CRC_VAL will cause CRC value to be formatted accordingly; however the CRC will not be compliant to the standard CRC used in Smart Cards.

The CRC value can be reset/initialized in multiple ways. Clearing the CRC_EN bit in the CTRL register will reset the CRC value. At the end of a transmission (either after the CRC characters are transmitted, or after the last character in the transmit FIFO is sent when XMT_CRC_LRC is clear), the CRC value is automatically reset by the EMV SIM hardware. Finally, when setting the XMT_EN bit, the EMV SIM hardware resets the CRC value.

Summary of configuration needed to use CRC block:

- Use CRC_IN_FLIP, CRC_OUT_FLIP and INV_CRC_VAL bits in CTRL register to select the desired CRC method (CCITT or normal)
- Use the CRC_EN bit in CTRL register to enable the CRC block
- Use the XMT_CRC_LRC bit to enable the transmission of the CRC Characters after the last character in the Transmit FIFO is sent.

15.7.6 Message Handling

The EMV SIM module has FIFOs on both transmit and receive side for handling all message bytes.

15.7.6.1 Transmit FIFO

A 16-byte deep FIFO is implemented in the transmitter. The transmit FIFO can be written into by the software but reads to this FIFO will return zeros. To take care of clock synchronization, each write access will have wait states inserted by the module but this is transparent to the software. The Tx FIFO can be written to while the transmitter is enabled, however, the transmitter does not start transmitting while the FIFO is empty. A write to the Tx FIFO will initiate the transmit operation. Software can store more bytes into the Tx FIFO until the programmed threshold is reached. Software can enable DMA operation by setting TX_DMA_EN = 1 in the CTRL register. On setting this bit, a DMA request will be asserted and remain asserted till the number of bytes in FIFO reached the programmed threshold value (TDT[3:0] in the TX_THD register).

The transmit FIFO can be flushed by setting the FLSH_TX bit in the CTRL register. A transmit NACK threshold error (TNTE) will halt the transmitter, and flush the transmit FIFO. The flush operation resets the transmit read and write pointers to equal values. Everything in the transmitter block is reset by the transmit flush operation. This does not include the control registers associated with the transmitter. The Transmit data threshold flag (TDTF) does not get cleared by the FLSH_TX operation.

15.7.6.2 Receive FIFO

A 16-byte deep FIFO is implemented in the receiver. Since more than 16-bytes can be received in the FIFO, the software must ensure that the Rx FIFO is periodically read. The Rx FIFO can be read by software via normal CPU accesses on interrupt (RX_DATA interrupt flag) or via DMA by setting the DMA_RX_EN bit in CTRL register. The software cannot write to this register. A write access may terminate in a transfer error.

The Rx FIFO is loaded by the receiver when it receives an error free message byte with correct parity. The FIFO stores the message byte only. When the total bytes in the Rx FIFO equals the programmed threshold value (RDT[3:0] in RX_THD register), the RDTF bit is asserted in the RX_STATUS register. An interrupt will be asserted if the RDT_IM bit in the INT_MASK is cleared. If DMA access to RX_FIFO is enabled, the DMA request to read the Rx FIFO will be asserted when the threshold flag is set and will clear when all the bytes are read out from the Rx FIFO.

The receive FIFO can be flushed by setting the FLSH_RX bit in the CTRL register. The flush operation resets the receiver except for receiver control registers.

NOTE

Since the register bits and the receiver logic are in different clock domains, the software needs to make sure to allow clock synchronization time when sampling the RDTF bit. One proposed method could be to read one byte at a time (from Rx FIFO) when RDTF is asserted, allow a time of 3 bus clock cycles after Rx FIFO read and then check the status of the RDTF bit and repeat as necessary. Alternatively, one could set the receiver threshold one more than actually needed.

Rx FIFO Overflow Detection: When a byte is received by the receiver and the Rx FIFO is not read and already contains 16 bytes, a FIFO overflow error will be asserted (RFO bit set to 1 in RX_STATUS register). The received byte will be discarded leaving the FIFO with the first 16 bytes received. If the ONACK bit in the CTRL register is asserted, the

transmitter will generate a NACK for the overflow condition every time a new byte is received that cannot be stored in the Rx FIFO. The EMV SIM module will continually send NACKs till the Rx FIFO is read or NACK transmit threshold is reached.

15.7.7 Protocol Timers

The EMV SIM module has several 16-bit and 32-bit timers to allow the software perform protocol timing checks and measurements like:

- Guard Time
- Character Wait Time
- Block Wait Time
- Block Guard Time
- Work Wait Time

In addition to the above, the EMV SIM module also contains two 32-bit general purpose counters which can be used by software for any application specific time measurement.

15.7.7.1 Transmit Guard Time

The Transmit Guard time is the number of ETUs inserted by the transmitter between each character being transmitted. The number of ETUs is controlled by programming the TX_GETU register. The Guard Time is measured as the time (in ETUs) between the STOP bits of previous character and the START bit of next character.

For a Guard Time programmed as 0xFF in GETU[7:0] bits of TX_GETU register, the transmitter inserts one STOP bit instead of two.

15.7.7.2 Character Wait Time

The EMV SIM receiver block includes a 16-bit counter that counts the number of bit times (ETUs) between received characters (i.e. time between start bits in the consecutive characters received). When enabled, the Character Wait Time Counter (CWT) will not start counting until after the START bit(s) of a valid character has been received. The counter is synchronized to the receive character bit positions so that an accurate count of the number of ETUs between characters can be made. The Character Wait Time Counter has a 16-bit programmable comparator. Software can write the expected number of ETUs between characters to the comparator. If the time between characters exceeds this value, an interrupt flag will be set and an interrupt generated if the mask is clear. The CWT can be configured as follows:

- Program the CWT_VAL register to the value that needs to be enforced
- Activate CWT function by setting the CWT_EN bit in the CTRL register
- Enable the CWT_ERR interrupt by clearing the CWT_IM bit in the INT_MASK register
- If an interrupt occurs, then the software should read the RX_STATUS register to determine if the error was caused by a CWT_ERR violation. The software should clear the CWT_ERR interrupt by writing a “1” to the CWT_ERR bit in the RX_STATUS register
- Software can disable the CWT counter by clearing the CWT_EN bit in the CTRL register at any time

15.7.7.3 Block Wait Time and Block Guard Time

A 32-bit timer is used to measure both Block Wait Time (BWT) and Block Guard Time (BGT). The BWT and BGT timer are used to measure the delay between the leading edge of the last character of the block received by the card and the leading edge of the first character of the next block sent by the card. If this time measured is larger than the value in BWT_VAL register, then the BWT_ERR flag will be set and an interrupt generated. If the time is less than the value in the BGT_VAL register, then the BGT_ERR flag will be set and an interrupt generated. The block wait timer can be configured as follows:

- Program the BWT_VAL and BGT_VAL registers to the value that need to be enforced
- Activate the block wait timer by writing '1' to BWT_EN bit in the CTRL register
- Enable the BWT_ERR and BGT_ERR interrupts by clearing the BWT_IM and BGT_IM bits in the INT_MASK register
- If an interrupt occurs, then the software should read the RX_STATUS register to determine if the error was caused by a BWT_ERR or BGT_ERR violation. The software should clear the interrupt status bit by writing a “1” to the BWT_ERR bit or BGT_ERR, respectively, in the RX_STATUS register
- Software can disable the BWT counter by clearing the BWT_EN bit in the CTRL register at any time

NOTE

BWT should be enabled after all bytes are written to in Tx FIFO. This is necessary to avoid the condition where writes to Tx FIFO are very slow (more than 1 ETU time apart) and if BWT is enabled earlier, then BWT error can trigger falsely.

15.7.7.4 Work Wait Time

There is no separate counter to measure the work wait time (WWT). Work wait time is a combination of BWT and CWT. To measure WWT, software must configure both CWT_VAL and BWT_VAL to the value to enforced. When measuring WWT, the BGT timer will not be used so it should be masked (inactive) by the BGT_IM bit. Below is the sequence to program the EMV SIM to send and receive data while checking WWT:

- Program both the CWT_VAL and the BWT_VAL registers to the WWT (work wait time) value that needs to be enforced. Set BGT register to 0 (this is the default value).
- Activate both the CWT and BWT functions by setting the CWT_EN and BWT_EN bit in the CTRL register
- Enable the CWT_ERR and BWT_ERR interrupts by clearing the CWT_IM and BWT_IM bits in the INT_MASK register
- Program the EMV SIM module to enable Receiver or Transmitter as desired by application
- If an interrupt occurs, then the software should consider that a WWT violation if the CWT_ERR or BWT_ERR bits are asserted. The software should clear the CWT_ERR or BWT_ERR interrupt by writing a “1” to the BWT_ERR or CWT_ERR bit in the RX_STATUS register

15.7.7.5 General Purpose Timers

The EMV SIM module provides TWO 16-bit counters for use, when timing events during Smart Card communication. The clock source for the counter is selectable between three sources: Card Clock, Receiver Clock (16 times the ETU clock) or ETU Clock (for Transmitter). The GPCNT0/1_CLKSEL[1:0] bits in the CTRL register are used to select the clock input. The counter is enabled as soon as the input clock is selected. The starting of the counter is immediate once the input clock is running. Software can control the three input clock sources by using the SCEN, KILL_CLOCKS, RCV_EN and XMT_EN bits provided in the CTRL register.

To run the counters from the card clock source the following conditions must be met:

- ‘KILL_CLOCKS = 0’ in the CTRL register
- ‘RCV_EN = 1’ or XMT_EN = 1 in the CTRL register
- 'SCEN = 1' in the PCSR register
- ‘GPCNT_CLKSET[1:0] = 01’ in the CLKCFG register

The counter will begin to count at the card clock rate as soon as these conditions are met.

To run the counters from the receive clock source the following conditions must be met:

- ‘KILL_CLOCKS = 0’ in the CTRL register.

- ‘RCV_EN = 1’ or XMT_EN = 1 in the CTRL register
- ‘GPCNT0/1_CLKSET[1:0] = 10’ in the CLKCFG register

The counter will begin to count at the receive clock rate as soon as these conditions are met.

To run the counters from the ETU (transmit) clock source the following conditions must be met:

- ‘KILL_CLOCKS = 0’ in the CTRL register.
- ‘RCV_EN = 1’ or XMT_EN = 1 in the CTRL register
- ‘GPCNT0/1_CLKSET[1:0] = 11’ in the CLKCFG register

The counters will begin to count at the ETU clock rate as soon as these conditions are met.

The counters can be reset by setting GPCNT0/1_CLKSEL[1:0] to 00. A 16-bit comparator value (GPCNT0/1_VAL register) is provided that allows the software to select a count value at which the interrupt flags (GPCNT0/1_TO bit in TX_STATUS register) can be set and an interrupt generated if the mask (GPCNT0/1_IM bits in INT_MASK register) are clear.

The following sequence should be followed to configure both general purpose timers:

- Program counter comparator using the GPCNT0/1_VAL register
- Enable the conditions described above using the CTRL register
- Select desired clock source for the General Purpose Counter using the CLKCFG register
- Enable interrupts in the INT_MASK register

15.7.8 Answer To Reset (ATR) Detection

The first communication that occurs between the Smart Card and the EMV SIM module will be a block of data sent from the Smart Card to the EMV SIM module after the card is powered up and the card reset is removed (As described in Smart Card Interface and Control Section). This block is called the Answer To Reset (ATR). To receive the ATR, the EMV SIM module should be configured for 12 ETU character reception. According to the ISO 7816-3 spec, both “T=0” and “T=1” cards will communicate initially using 12 ETU character durations.

The following steps provide a suggested approach to configure the EMV SIM module to receive the ATR.

- Clear RCVR11 bit in the CTRL register

- Set ANACK bit in the CTRL register to enable NACK generation. The ISO 7816-3 spec allows the EMV SIM module to NACK any communication errors that occur during the initial communication at 12 ETU.

NOTE

The Europay MasterCard and VISA (EMV) cards are similar to “T=1”, but do not allow the EMV SIM module to NACK during the initial communication

- Enable RDTF and RFO interrupts by setting RDT_IM and RFO_IM bits in INT_MASK register. These interrupts are enabled to notify the software when characters are received. A threshold can be set for the number of characters to receive before generating an interrupt.
- Set desired threshold for received characters by writing RDT in RX_THD register

The EMV SIM should be setup to perform in initial character mode during ATR detection. This will cause the hardware to identify the first valid character sent during the ATR as an initial character. This character will automatically configure the hardware for the data convention used by the Smart Card.

- Set Initial Character Mode by setting the ICM bit in the CTRL register

The ISO 7816-3 spec requires that Smart Cards meet certain timing restrictions. One of these is the time from the de-assertion of the card reset to the beginning of the ATR sequence. The EMV SIM module's General Purpose Counter can be used to verify that the Smart Card begins its ATR within the 400 to 40,000 card clock cycle range.

- Set the General Purpose Counter 0 or 1 Timeout Value to 0x9C40 using GPCNT0/1_VAL register.
- Enable General Purpose Counter Interrupt by clearing GPCNT0/1_IM in INT_MASK register.
- Enable General Purpose Counter by programming the GPCNT0/1_CLKSEL[1:0] bits to 01, so that the card clock is used for counting.

The ISO7816-3 spec states that the maximum allowed time between two characters during the ATR is 9600 ETUs (Initial Waiting Time). The Character Wait Time Counter should be setup to detect any errors for this condition.

- Set Character Wait Time Counter Comparator to 9600 using the CWT_VAL register
- Enable the Character Wait Time Counter Interrupt by clearing CWT_ERR_IM in INT_MASK register
- Enable the Character Wait Time Counter by setting the CWT_EN bit in the CTRL register

The last step in preparing for ATR reception is to enable the receiver.

- Set RCV_EN bit in CTRL register

The EMV SIM module will generate interrupts once a threshold number of characters is received. The software should react to these interrupts and read the characters from the receive FIFO (RX_BUF) until the complete ATR has been received. If a General Purpose Counter interrupt occurs before the final ATR character is received, then the card should be deactivated according to the ISO 7816-3 spec (See Section Smart Card Interface and Control). Otherwise, once a valid ATR is received, the software will know from the ATR information the specific characteristics for this card (refer to the ISO 7816-3 spec for details).

15.7.8.1 Programming Considerations for T=0 Smart Cards

If the card is of type T=0, the software should adjust the following parameters according to the information in the ATR:

- Adjust the baud rate by changing the values of DIVISOR register based on the values of 'F' and 'D' received in the ATR.
- Adjust the guard time between characters by changing the value of GETU[7:0] in the TX_GETU register.
- Adjust NACK capability by modifying the values of the ONACK and ANACK bits in the CTRL register.
- Adjust the stop clock polarity by modifying the value of the SCSP bit in the PCSR register.
- Adjust the level of transmit NACK re-transmissions allowed by modifying the value of the TNCK_THD[3:0] bits in the TX_THD register.
- Adjust the level for the Receive NACK threshold by modifying the RNCK_THD[3:0] bits in the RX_THD register.

If a negotiation with the Smart Card is desired, the software sends a PPS response to the Smart Card. To send the response, the following steps should be performed:

- Set the desired transmit FIFO threshold level by writing the TDT[3:0] bits in the TX_THD register.
- Clear all transmit interrupt flags in the TX_STATUS register by writing a one to the bits of the register.
- Enable the transmit interrupts desired by clearing the mask bits in the INT_MASK register. If more than 16 characters are to be sent, it is suggested that the TDTF interrupt be used to signify when to write more characters to the transmit FIFO. This results in the most efficient transfer times to the Smart Card.
- Enable the transmitter by setting the XMT_EN bit in the CTRL register.
- Write the characters to be sent as response (max 16) to the transmit FIFO using the TX_BUF register.

At this point, the EMV SIM module will transmit the characters in the transmit FIFO. If more than 16 characters are to be sent, the transmit threshold interrupt will be set when the threshold number of characters are remaining in the FIFO. The software can then write an additional number of characters to be sent without interrupting transmission to the Smart Card.

Once the transmission is complete, the EMV SIM module should be completely configured for standard operation with the T=0 Smart Card. The software can continue to service RDTF interrupts for received characters, and TDTF interrupts for transmitted characters.

15.7.8.2 Programming Considerations for T=1 Smart Cards

If the card is of type T=1, the software should adjust the following parameters according to the information in the ATR:

- Adjust the baud rate by changing the values of DIVISOR register based on the values of 'F' and 'D' received in the ATR.
- Adjust the guard time between characters by changing the value of GETU[7:0] in the TX_GETU register. Setting GETU[7:0] to 0xFF configures the SIM transmitter for 11 ETU transmissions.
- Disable NACK capability by clearing the ONACK and ANACK bits in the CTRL register. T=1 cards do not allow NACKs.
- Adjust the stop clock polarity by modifying the value of the SCSP bit in the PCSR register.
- Set Character Wait Time Counter Timeout Value to value specified in the ATR by using the CWT_VAL register.
- Enable the Character Wait Time Counter Interrupt by clearing CWT_ERR_IM in INT_MASK register.
- Enable the Character Wait Time Counter by setting the CWT_EN bit in the CTRL register.
- Enable CRC or LRC error checking according to the ATR information by setting either the CRC_EN or LRC_EN bit in the CTRL register. These bits should never be set at the same time!

For T=1 cards, the ATR is sent using a T=0 type of structure (12 ETU, no LRC or CRC). If a negotiation with the Smart Card is desired, the software will send a PPS response to the Smart Card. Otherwise, the protocol is initiated with a block transfer from the EMV SIM module. In order to send the response or the first block, the following steps should be performed:

- Set the desired transmit FIFO threshold level by writing the TDT[3:0] bits in the TX_THD register.

- Clear all transmit interrupt flags in the TX_STATUS register by writing a one to the bits of the register.
- Enable the transmit interrupts desired by clearing the mask bits in the INT_MASK register. If more than 16 characters are to be sent, it is suggested that the TDTF interrupt be used to signify when to write more characters to the transmit FIFO. This results in the most efficient transfer times to the Smart Card.
- Enable the transmission of the error checking characters (LRC or CRC) by setting the XMT_CRC_LRC bit in the CTRL register.

NOTE

If the card supports PPS, the software may not be allowed to send the LRC/CRC information until the PPS exchange is completed. If so, do not set the XMT_CRC_LRC bit during the PPS exchange.

- Enable the transmitter by setting the XMT_EN bit in the CTRL register.
- Write the characters to be sent as response (max 16) to the transmit FIFO using the TX_BUF register.

At this point, the EMV SIM module will transmit the characters in the transmit FIFO. If more than 16 characters are to be sent, the transmit threshold interrupt will be set when the threshold number of characters are remaining in the FIFO. The software can then write an additional number of characters to be sent without interrupting transmission to the Smart Card.

Once the transmission is complete, the EMV SIM module should be completely configured for standard operation with the T=1 Smart Card. The software can continue to service RDTF interrupts for received characters, and TDTF interrupts for transmitted characters.

Chapter 16
Reset Control Module (RCM)

16.1 Introduction

Information found here describes the registers of the Reset Control Module (RCM). The RCM implements many of the reset functions for the chip. See the chip's reset chapter for more information.

See AN4503: Power Management for Kinetis MCUs for further details on using the RCM.

16.2 Reset memory map and register descriptions

The RCM Memory Map/Register Definition can be found here.

The Reset Control Module (RCM) registers provide reset status information and reset filter control.

NOTE

The RCM registers can be written only in supervisor mode. Write accesses in user mode are blocked and will result in a bus error.

RCM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4007_F000	System Reset Status Register 0 (RCM_SRS0)	8	R	82h	16.2.1/360
4007_F001	System Reset Status Register 1 (RCM_SRS1)	8	R	00h	16.2.2/361
4007_F004	Reset Pin Filter Control register (RCM_RPFC)	8	R/W	00h	16.2.3/363
4007_F005	Reset Pin Filter Width register (RCM_RPFW)	8	R/W	00h	16.2.4/364

Table continues on the next page...

RCM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4007_F006	Force Mode Register (RCM_FM)	8	R/W	00h	16.2.5/365
4007_F007	Mode Register (RCM_MR)	8	R/W	See section	16.2.6/366
4007_F008	Sticky System Reset Status Register 0 (RCM_SSRS0)	8	R/W	82h	16.2.7/367
4007_F009	Sticky System Reset Status Register 1 (RCM_SSRS1)	8	R/W	00h	16.2.8/368

16.2.1 System Reset Status Register 0 (RCM_SRS0)

This register includes read-only status flags to indicate the source of the most recent reset. The reset state of these bits depends on what caused the MCU to reset.

NOTE

The reset value of this register depends on the reset source:

- POR (including LVD) — 0x82
- LVD (without POR) — 0x02
- VLLS mode wakeup due to $\overline{\text{RESET}}$ pin assertion — 0x41
- VLLS mode wakeup due to other wakeup sources — 0x01
- Other reset — a bit is set if its corresponding reset source caused the reset

Address: 4007_F000h base + 0h offset = 4007_F000h

Bit	7	6	5	4	3	2	1	0
Read	POR	PIN	WDOG	0	LOL	LOC	LVD	WAKEUP
Write								
Reset	1	0	0	0	0	0	1	0

RCM_SRS0 field descriptions

Field	Description
7 POR	Power-On Reset Indicates a reset has been caused by the power-on detection logic. Because the internal supply voltage was ramping up at the time, the low-voltage reset (LVD) status bit is also set to indicate that the reset occurred while the internal supply was below the LVD threshold. 0 Reset not caused by POR 1 Reset caused by POR
6 PIN	External Reset Pin Indicates a reset has been caused by an active-low level on the external $\overline{\text{RESET}}$ pin. 0 Reset not caused by external reset pin 1 Reset caused by external reset pin

Table continues on the next page...

RCM_SRS0 field descriptions (continued)

Field	Description
5 WDOG	Watchdog Indicates a reset has been caused by the watchdog timer timing out. This reset source can be blocked by disabling the watchdog. 0 Reset not caused by watchdog timeout 1 Reset caused by watchdog timeout
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 LOL	Loss-of-Lock Reset Indicates a reset has been caused by a loss of lock in the MCG PLL. See the MCG description for information on the loss-of-clock event. 0 Reset not caused by a loss of lock in the PLL 1 Reset caused by a loss of lock in the PLL
2 LOC	Loss-of-Clock Reset Indicates a reset has been caused by a loss of external clock. The MCG clock monitor must be enabled for a loss of clock to be detected. Refer to the detailed MCG description for information on enabling the clock monitor. 0 Reset not caused by a loss of external clock. 1 Reset caused by a loss of external clock.
1 LVD	Low-Voltage Detect Reset If PMC_LVDSC1[LVDRE] is set and the supply drops below the LVD trip voltage, an LVD reset occurs. This field is also set by POR. 0 Reset not caused by LVD trip or POR 1 Reset caused by LVD trip or POR
0 WAKEUP	Low Leakage Wakeup Reset Indicates a reset has been caused by an enabled LLWU module wakeup source while the chip was in a low leakage mode. In LLS mode, the $\overline{\text{RESET}}$ pin is the only wakeup source that can cause this reset. Any enabled wakeup source in a VLLSx mode causes a reset. This bit is cleared by any reset except WAKEUP. 0 Reset not caused by LLWU module wakeup source 1 Reset caused by LLWU module wakeup source

16.2.2 System Reset Status Register 1 (RCM_SRS1)

This register includes read-only status flags to indicate the source of the most recent reset. The reset state of these bits depends on what caused the MCU to reset.

NOTE

The reset value of this register depends on the reset source:

- POR (including LVD) — 0x00

- LVD (without POR) — 0x00
- VLLS mode wakeup — 0x00
- Other reset — a bit is set if its corresponding reset source caused the reset

Address: 4007_F000h base + 1h offset = 4007_F001h

Bit	7	6	5	4	3	2	1	0
Read	0	0	SACKERR	0	MDM_AP	SW	LOCKUP	JTAG
Write								
Reset	0	0	0	0	0	0	0	0

RCM_SRS1 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 SACKERR	Stop Mode Acknowledge Error Reset Indicates that after an attempt to enter Stop mode, a reset has been caused by a failure of one or more peripherals to acknowledge within approximately one second to enter stop mode. 0 Reset not caused by peripheral failure to acknowledge attempt to enter stop mode 1 Reset caused by peripheral failure to acknowledge attempt to enter stop mode
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 MDM_AP	MDM-AP System Reset Request Indicates a reset has been caused by the host debugger system setting of the System Reset Request bit in the MDM-AP Control Register. 0 Reset not caused by host debugger system setting of the System Reset Request bit 1 Reset caused by host debugger system setting of the System Reset Request bit
2 SW	Software Indicates a reset has been caused by software setting of SYSRESETREQ bit in Application Interrupt and Reset Control Register in the ARM core. 0 Reset not caused by software setting of SYSRESETREQ bit 1 Reset caused by software setting of SYSRESETREQ bit
1 LOCKUP	Core Lockup Indicates a reset has been caused by the ARM core indication of a LOCKUP event. 0 Reset not caused by core LOCKUP event 1 Reset caused by core LOCKUP event
0 JTAG	JTAG Generated Reset Indicates a reset has been caused by JTAG selection of certain IR codes: EXTEST, HIGHZ, and CLAMP.

Table continues on the next page...

RCM_SRS1 field descriptions (continued)

Field	Description
	0 Reset not caused by JTAG 1 Reset caused by JTAG

16.2.3 Reset Pin Filter Control register (RCM_RPFC)

NOTE

The reset values of bits 2-0 are for Chip POR only. They are unaffected by other reset types.

NOTE

The bus clock filter is reset when disabled or when entering stop mode. The LPO filter is reset when disabled .

Address: 4007_F000h base + 4h offset = 4007_F004h

Bit	7	6	5	4	3	2	1	0
Read	0					RSTFLTSS	RSTFLTSRW	
Write								
Reset	0	0	0	0	0	0	0	0

RCM_RPFC field descriptions

Field	Description
7–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 RSTFLTSS	Reset Pin Filter Select in Stop Mode Selects how the reset pin filter is enabled in Stop and VLPS modes , and also during LLS and VLLS modes. On exit from VLLS mode, this bit should be reconfigured before clearing PMC_REGSC[ACKISO]. 0 All filtering disabled 1 LPO clock filter enabled
RSTFLTSRW	Reset Pin Filter Select in Run and Wait Modes Selects how the reset pin filter is enabled in run and wait modes. 00 All filtering disabled 01 Bus clock filter enabled for normal operation 10 LPO clock filter enabled for normal operation 11 Reserved

16.2.4 Reset Pin Filter Width register (RCM_RPFW)

NOTE

The reset values of the bits in the RSTFLTSEL field are for Chip POR only. They are unaffected by other reset types.

Address: 4007_F000h base + 5h offset = 4007_F005h

Bit	7	6	5	4	3	2	1	0
Read	0				RSTFLTSEL			
Write								
Reset	0	0	0	0	0	0	0	0

RCM_RPFW field descriptions

Field	Description
7–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
RSTFLTSEL	Reset Pin Filter Bus Clock Select Selects the reset pin bus clock filter width. 00000 Bus clock filter count is 1 00001 Bus clock filter count is 2 00010 Bus clock filter count is 3 00011 Bus clock filter count is 4 00100 Bus clock filter count is 5 00101 Bus clock filter count is 6 00110 Bus clock filter count is 7 00111 Bus clock filter count is 8 01000 Bus clock filter count is 9 01001 Bus clock filter count is 10 01010 Bus clock filter count is 11 01011 Bus clock filter count is 12 01100 Bus clock filter count is 13 01101 Bus clock filter count is 14 01110 Bus clock filter count is 15 01111 Bus clock filter count is 16 10000 Bus clock filter count is 17 10001 Bus clock filter count is 18 10010 Bus clock filter count is 19 10011 Bus clock filter count is 20 10100 Bus clock filter count is 21 10101 Bus clock filter count is 22 10110 Bus clock filter count is 23 10111 Bus clock filter count is 24 11000 Bus clock filter count is 25

Table continues on the next page...

RCM_RPFW field descriptions (continued)

Field	Description
	11001 Bus clock filter count is 26 11010 Bus clock filter count is 27 11011 Bus clock filter count is 28 11100 Bus clock filter count is 29 11101 Bus clock filter count is 30 11110 Bus clock filter count is 31 11111 Bus clock filter count is 32

16.2.5 Force Mode Register (RCM_FM)

NOTE

The reset values of the bits in the FORCEROM field are for Chip POR only. They are unaffected by other reset types.

Address: 4007_F000h base + 6h offset = 4007_F006h

Bit	7	6	5	4	3	2	1	0
Read	0					FORCEROM		0
Write								
Reset	0	0	0	0	0	0	0	0

RCM_FM field descriptions

Field	Description
7–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2–1 FORCEROM	Force ROM Boot When either bit is set, will force boot from ROM during all subsequent system resets. 00 No effect 01 Force boot from ROM with RCM_MR[1] set. 10 Force boot from ROM with RCM_MR[2] set. 11 Force boot from ROM with RCM_MR[2:1] set.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

16.2.6 Mode Register (RCM_MR)

This register includes status flags to indicate the state of the mode pins during the last Chip Reset.

Address: 4007_F000h base + 7h offset = 4007_F007h

Bit	7	6	5	4	3	2	1	0
Read	0					BOOTROM		0
Write						w1c		
Reset	0	0	0	0	0	*	*	0

* Notes:
- BOOTROM field: The reset state of this register depends on the boot mode.

RCM_MR field descriptions

Field	Description
7–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2–1 BOOTROM	Boot ROM Configuration Indicates the boot source, the boot source remains set until the next System Reset or software can write logic one to clear the corresponding mode bit. While either bit is set, the NMI input is disabled and the vector table is relocated to the ROM base address at 0x1C00_0000. These bits should be cleared by writing logic one before executing any code from either Flash or SRAM. 00 Boot from Flash 01 Boot from ROM due to BOOTCFG0 pin assertion 10 Boot form ROM due to FOPT[7] configuration 11 Boot from ROM due to both BOOTCFG0 pin assertion and FOPT[7] configuration
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

16.2.7 Sticky System Reset Status Register 0 (RCM_SSRS0)

This register includes status flags to indicate all reset sources since the last POR, LVD or VLLS Wakeup that have not been cleared by software. Software can clear the status flags by writing a logic one to a flag.

Address: 4007_F000h base + 8h offset = 4007_F008h

Bit	7	6	5	4	3	2	1	0
Read	SPOR	SPIN	SWDOG	0	SLOL	SLOC	SLVD	SWAKEUP
Write	w1c	w1c	w1c		w1c	w1c	w1c	w1c
Reset	1	0	0	0	0	0	1	0

RCM_SSRS0 field descriptions

Field	Description
7 SPOR	Sticky Power-On Reset Indicates a reset has been caused by the power-on detection logic. Because the internal supply voltage was ramping up at the time, the low-voltage reset (LVD) status bit is also set to indicate that the reset occurred while the internal supply was below the LVD threshold. 0 Reset not caused by POR 1 Reset caused by POR
6 SPIN	Sticky External Reset Pin Indicates a reset has been caused by an active-low level on the external $\overline{\text{RESET}}$ pin. 0 Reset not caused by external reset pin 1 Reset caused by external reset pin
5 SWDOG	Sticky Watchdog Indicates a reset has been caused by the watchdog timer timing out.This reset source can be blocked by disabling the watchdog. 0 Reset not caused by watchdog timeout 1 Reset caused by watchdog timeout
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 SLOL	Sticky Loss-of-Lock Reset Indicates a reset has been caused by a loss of lock in the MCG PLL. See the MCG description for information on the loss-of-clock event. 0 Reset not caused by a loss of lock in the PLL 1 Reset caused by a loss of lock in the PLL
2 SLOC	Sticky Loss-of-Clock Reset

Table continues on the next page...

RCM_SSRS0 field descriptions (continued)

Field	Description
	Indicates a reset has been caused by a loss of external clock. The MCG clock monitor must be enabled for a loss of clock to be detected. Refer to the detailed MCG description for information on enabling the clock monitor. 0 Reset not caused by a loss of external clock. 1 Reset caused by a loss of external clock.
1 SLVD	Sticky Low-Voltage Detect Reset If PMC_LVDSC1[LVDRE] is set and the supply drops below the LVD trip voltage, an LVD reset occurs. This field is also set by POR. 0 Reset not caused by LVD trip or POR 1 Reset caused by LVD trip or POR
0 SWAKEUP	Sticky Low Leakage Wakeup Reset Indicates a reset has been caused by an enabled LLWU modulewakeup source while the chip was in a low leakage mode. In LLS mode, the $\overline{\text{RESET}}$ pin is the only wakeup source that can cause this reset. Any enabled wakeup source in a VLLSx mode causes a reset. 0 Reset not caused by LLWU module wakeup source 1 Reset caused by LLWU module wakeup source

16.2.8 Sticky System Reset Status Register 1 (RCM_SSRS1)

This register includes status flags to indicate all reset sources since the last POR, LVD or VLLS Wakeup that have not been cleared by software. Software can clear the status flags by writing a logic one to a flag.

Address: 4007_F000h base + 9h offset = 4007_F009h

Bit	7	6	5	4	3	2	1	0
Read	0	0	SSACKERR	0	SMDM_AP	SSW	SLOCKUP	SJTAG
Write			w1c		w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

RCM_SSRS1 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 SSACKERR	Sticky Stop Mode Acknowledge Error Reset

Table continues on the next page...

RCM_SSRS1 field descriptions (continued)

Field	Description
	Indicates that after an attempt to enter Stop mode, a reset has been caused by a failure of one or more peripherals to acknowledge within approximately one second to enter stop mode. 0 Reset not caused by peripheral failure to acknowledge attempt to enter stop mode 1 Reset caused by peripheral failure to acknowledge attempt to enter stop mode
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 SMDM_AP	Sticky MDM-AP System Reset Request Indicates a reset has been caused by the host debugger system setting of the System Reset Request bit in the MDM-AP Control Register. 0 Reset not caused by host debugger system setting of the System Reset Request bit 1 Reset caused by host debugger system setting of the System Reset Request bit
2 SSW	Sticky Software Indicates a reset has been caused by software setting of SYSRESETREQ bit in Application Interrupt and Reset Control Register in the ARM core. 0 Reset not caused by software setting of SYSRESETREQ bit 1 Reset caused by software setting of SYSRESETREQ bit
1 SLOCKUP	Sticky Core Lockup Indicates a reset has been caused by the ARM core indication of a LOCKUP event. 0 Reset not caused by core LOCKUP event 1 Reset caused by core LOCKUP event
0 SJTAG	Sticky JTAG Generated Reset Indicates a reset has been caused by JTAG selection of certain IR codes: EXTEST, HIGHZ, and CLAMP. 0 Reset not caused by JTAG 1 Reset caused by JTAG

Chapter 17
System Mode Controller (SMC)

17.1 Introduction

The System Mode Controller (SMC) is responsible for sequencing the system into and out of all low-power Stop and Run modes.

Specifically, it monitors events to trigger transitions between power modes while controlling the power, clocks, and memories of the system to achieve the power consumption and functionality of that mode.

This chapter describes all the available low-power modes, the sequence followed to enter/exit each mode, and the functionality available while in each of the modes.

The SMC is able to function during even the deepest low power modes.

See AN4503: Power Management for Kinetis MCUs for further details on using the SMC.

17.2 Modes of operation

The ARM CPU has three primary modes of operation:

- Run
- Sleep
- Deep Sleep

The WFI or WFE instruction is used to invoke Sleep and Deep Sleep modes. Run, Wait, and Stop are the common terms used for the primary operating modes of Freescale microcontrollers.

The following table shows the translation between the ARM CPU modes and the Freescale MCU power modes.

ARM CPU mode	MCU mode
Sleep	Wait
Deep Sleep	Stop

Accordingly, the ARM CPU documentation refers to sleep and deep sleep, while the Freescale MCU documentation normally uses wait and stop.

In addition, Freescale MCUs also augment Stop, Wait, and Run modes in a number of ways. The power management controller (PMC) contains a run and a stop mode regulator. Run regulation is used in normal run, wait and stop modes. Stop mode regulation is used during all very low power and low leakage modes. During stop mode regulation, the bus frequencies are limited in the very low power modes.

The SMC provides the user with multiple power options. The Very Low Power Run (VLPR) mode can drastically reduce run time power when maximum bus frequency is not required to handle the application needs. From Normal Run mode, the Run Mode (RUNM) field can be modified to change the MCU into VLPR mode when limited frequency is sufficient for the application. From VLPR mode, a corresponding wait (VLPW) and stop (VLPS) mode can be entered.

Depending on the needs of the user application, a variety of stop modes are available that allow the state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. Several registers are used to configure the various modes of operation for the device.

The following table describes the power modes available for the device.

Table 17-1. Power modes

Mode	Description
RUN	The MCU can be run at full speed and the internal supply is fully regulated, that is, in run regulation. This mode is also referred to as Normal Run mode.
HSRUN	The MCU can be run at a faster frequency compared with RUN mode and the internal supply is fully regulated. See the Power Management chapter for details about the maximum allowable frequencies.
WAIT	The core clock is gated off. The system clock continues to operate. Bus clocks, if enabled, continue to operate. Run regulation is maintained.
STOP	The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid.
VLPR	The core, system, bus, and flash clock maximum frequencies are restricted in this mode. See the Power Management chapter for details about the maximum allowable frequencies.
VLPW	The core clock is gated off. The system, bus, and flash clocks continue to operate, although their maximum frequency is restricted. See the Power Management chapter for details on the maximum allowable frequencies.
VLPS	The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid.

Table continues on the next page...

Table 17-1. Power modes (continued)

Mode	Description
LLS3	The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid. The MCU is placed in a low leakage mode by reducing the voltage to internal logic. All system RAM contents, internal logic and I/O states are retained.
LLS2	The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid. The MCU is placed in a low leakage mode by reducing the voltage to internal logic and powering down the system RAM3 partition. The system RAM2 partition can be optionally retained using STOPCTRL[RAM2PO]. The system RAM1 partition, internal logic and I/O states are retained.[1]
VLLS3	The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid. The MCU is placed in a low leakage mode by powering down the internal logic. All system RAM contents are retained and I/O states are held. Internal logic states are not retained.
VLLS2	The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid. The MCU is placed in a low leakage mode by powering down the internal logic and the system RAM3 partition. The system RAM2 partition can be optionally retained using STOPCTRL[RAM2PO].The system RAM1 partition contents are retained in this mode. Internal logic states are not retained. [2]
VLLS1	The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid. The MCU is placed in a low leakage mode by powering down the internal logic and all system RAM. I/O states are held. Internal logic states are not retained.
VLLS0	The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid. The MCU is placed in a low leakage mode by powering down the internal logic and all system RAM. I/O states are held. Internal logic states are not retained. The 1kHz LPO clock is disabled and the power on reset (POR) circuit can be optionally enabled using STOPCTRL[PORPO].

1. See the devices' chip configuration details for the size and location of the system RAM partitions.
2. See the devices' chip configuration details for the size and location of the system RAM partitions.

17.3 Memory map and register descriptions

Information about the registers related to the system mode controller can be found here.

Different SMC registers reset on different reset types. Each register's description provides details. For more information about the types of reset on this chip, refer to the Reset section details.

NOTE

The SMC registers can be written only in supervisor mode. Write accesses in user mode are blocked and will result in a bus error.

NOTE

Before executing the WFI instruction, the last register written to must be read back. This ensures that all register writes

associated with setting up the low power mode being entered have completed before the MCU enters the low power mode. Failure to do this may result in the low power mode not being entered correctly.

SMC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4007_E000	Power Mode Protection register (SMC_PMPROT)	8	R/W	See section	17.3.1/374
4007_E001	Power Mode Control register (SMC_PMCTRL)	8	R/W	See section	17.3.2/375
4007_E002	Stop Control Register (SMC_STOPCTRL)	8	R/W	03h	17.3.3/377
4007_E003	Power Mode Status register (SMC_PMSTAT)	8	R	See section	17.3.4/378

17.3.1 Power Mode Protection register (SMC_PMPROT)

This register provides protection for entry into any low-power run or stop mode. The enabling of the low-power run or stop mode occurs by configuring the Power Mode Control register (PMCTRL).

The PMPROT register can be written only once after any system reset.

If the MCU is configured for a disallowed or reserved power mode, the MCU remains in its current power mode. For example, if the MCU is in normal RUN mode and AVLP is 0, an attempt to enter VLPR mode using PMCTRL[RUNM] is blocked and PMCTRL[RUNM] remains 00b, indicating the MCU is still in Normal Run mode.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Reset section details for more information.

Address: 4007_E000h base + 0h offset = 4007_E000h

Bit	7	6	5	4	3	2	1	0
Read	AHSRUN	0	AVLP	0	ALLS	0	AVLLS	0
Write								
Reset	0	0	*	0	0	0	0	0

* Notes:
- AVLP field: When booting in run mode, the reset value is 0. When booting in VLPR mode, the reset value is 1.

SMC_PMPROT field descriptions

Field	Description
7 AHSRUN	Allow High Speed Run mode Provided the appropriate control bits are set up in PMCTRL, this write-once field allows the MCU to enter High Speed Run mode (HSRUN). 0 HSRUN is not allowed 1 HSRUN is allowed
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 AVLP	Allow Very-Low-Power Modes Provided the appropriate control bits are set up in PMCTRL, this write-once field allows the MCU to enter any very-low-power mode (VLPR, VLPW, and VLPS). 0 VLPR, VLPW, and VLPS are not allowed. 1 VLPR, VLPW, and VLPS are allowed.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 ALLS	Allow Low-Leakage Stop Mode Provided the appropriate control bits are set up in PMCTRL, this write-once field allows the MCU to enter any low-leakage stop mode (LLS). 0 Any LLSx mode is not allowed 1 Any LLSx mode is allowed
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 AVLLS	Allow Very-Low-Leakage Stop Mode Provided the appropriate control bits are set up in PMCTRL, this write once bit allows the MCU to enter any very-low-leakage stop mode (VLLSx). 0 Any VLLSx mode is not allowed 1 Any VLLSx mode is allowed
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

17.3.2 Power Mode Control register (SMC_PMCTRL)

The PMCTRL register controls entry into low-power Run and Stop modes, provided that the selected power mode is allowed via an appropriate setting of the protection (PMPROT) register.

NOTE

This register is reset on Chip POR not VLLS and by reset types that trigger Chip POR not VLLS. It is unaffected by reset types that do not trigger Chip POR not VLLS. See the Reset section details for more information.

Address: 4007_E000h base + 1h offset = 4007_E001h

Bit	7	6	5	4	3	2	1	0
Read	Reserved	RUNM		0	STOPA	STOPM		
Write								
Reset	0	*	*	0	0	0	0	0

* Notes:
- RUNM field: When booting in run mode, the reset value is 00. When booting in VLPR mode, the reset value is 10.

SMC_PMCTRL field descriptions

Field	Description
7 Reserved	This field is reserved. This bit is reserved for future expansion and should always be written zero.
6–5 RUNM	Run Mode Control When written, causes entry into the selected run mode. Writes to this field are blocked if the protection level has not been enabled using the PMPROT register. **NOTE:** RUNM may be set to VLPR only when PMSTAT=RUN. After being written to VLPR, RUNM should not be written back to RUN until PMSTAT=VLPR. **NOTE:** RUNM may be set to HSRUN only when PMSTAT=RUN. After being programmed to HSRUN, RUNM should not be programmed back to RUN until PMSTAT=HSRUN. Also, stop mode entry should not be attempted while RUNM=HSRUN or PMSTAT=HSRUN. 00 Normal Run mode (RUN) 01 Reserved 10 Very-Low-Power Run mode (VLPR) 11 High Speed Run mode (HSRUN)
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 STOPA	Stop Aborted When set, this read-only status bit indicates an interrupt occured during the previous stop mode entry sequence, preventing the system from entering that mode. This field is cleared by reset or by hardware at the beginning of any stop mode entry sequence and is set if the sequence was aborted. 0 The previous stop mode entry was successsful. 1 The previous stop mode entry was aborted.
STOPM	Stop Mode Control When written, controls entry into the selected stop mode when Sleep-Now or Sleep-On-Exit mode is entered with SLEEPDEEP=1 . Writes to this field are blocked if the protection level has not been enabled using the PMPROT register. After any system reset, this field is cleared by hardware on any successful write to the PMPROT register. **NOTE:** When set to VLLSxor LLSx, the LLSM in the STOPCTRL register is used to further select the particular VLLSor LLS submode which will be entered. **NOTE:** When set to STOP, the PSTOPO bits in the STOPCTRL register can be used to select a Partial Stop mode if desired. 000 Normal Stop (STOP) 001 Reserved

Table continues on the next page...

SMC_PMCTRL field descriptions (continued)

Field	Description
	010 Very-Low-Power Stop (VLPS) 011 Low-Leakage Stop (LLSx) 100 Very-Low-Leakage Stop (VLLSx) 101 Reserved 110 Reseved 111 Reserved

17.3.3 Stop Control Register (SMC_STOPCTRL)

The STOPCTRL register provides various control bits allowing the user to fine tune power consumption during the stop mode selected by the STOPM field.

NOTE

This register is reset on Chip POR not VLLS and by reset types that trigger Chip POR not VLLS. It is unaffected by reset types that do not trigger Chip POR not VLLS. See the Reset section details for more information.

Address: 4007_E000h base + 2h offset = 4007_E002h

Bit	7	6	5	4	3	2	1	0
Read Write	PSTOPO		PORPO	RAM2PO	LPOPO	LLSM		
Reset	0	0	0	0	0	0	1	1

SMC_STOPCTRL field descriptions

Field	Description
7–6 PSTOPO	Partial Stop Option These bits control whether a Partial Stop mode is entered when STOPM=STOP. When entering a Partial Stop mode from RUN (or VLPR) mode, the PMC, MCG and flash remain fully powered, allowing the device to wakeup almost instantaneously at the expense of higher power consumption. In PSTOP2, only system clocks are gated allowing peripherals running on bus clock to remain fully functional. In PSTOP1, both system and bus clocks are gated. 00 STOP - Normal Stop mode 01 PSTOP1 - Partial Stop with both system and bus clocks disabled 10 PSTOP2 - Partial Stop with system clock disabled and bus clock enabled 11 Reserved
5 PORPO	POR Power Option This bit controls whether the POR detect circuit is enabled in VLLS0 mode. 0 POR detect circuit is enabled in VLLS0 1 POR detect circuit is disabled in VLLS0

Table continues on the next page...

SMC_STOPCTRL field descriptions (continued)

Field	Description
4 RAM2PO	RAM2 Power Option This bit controls powering of RAM partition 2 in LLS2 or VLLS2 mode. **NOTE:** See the device's Chip Configuration details for the size and location of RAM parition 2 0 RAM2 not powered in LLS2/VLLS2 1 RAM2 powered in LLS2/VLLS2
3 LPOPO	LPO Power Option Controls whether the 1 kHz LPO clock is enabled in LLS/VLLSx modes. **NOTE:** During VLLS0 mode, the LPO clock is disabled by hardware and this bit has no effect. 0 LPO clock is enabled in LLS/VLLSx 1 LPO clock is disabled in LLS/VLLSx
LLSM	LLS or VLLS Mode Control This field controls which LLS orVLLS sub-mode to enter if STOPM = LLSx orVLLSx. 000 VLLS0 if PMCTRL[STOPM]=VLLSx, reserved if PMCTRL[STOPM]=LLSx 001 VLLS1 if PMCTRL[STOPM]=VLLSx, reserved if PMCTRL[STOPM]=LLSx 010 VLLS2 if PMCTRL[STOPM]=VLLSx, LLS2 if PMCTRL[STOPM]=LLSx 011 VLLS3 if PMCTRL[STOPM]=VLLSx, LLS3 if PMCTRL[STOPM]=LLSx 100 Reserved 101 Reserved 110 Reserved 111 Reserved

17.3.4 Power Mode Status register (SMC_PMSTAT)

PMSTAT is a read-only, one-hot register which indicates the current power mode of the system.

NOTE

This register is reset on Chip POR not VLLS and by reset types that trigger Chip POR not VLLS. It is unaffected by reset types that do not trigger Chip POR not VLLS. See the Reset section details for more information.

Address: 4007_E000h base + 3h offset = 4007_E003h

Bit	7	6	5	4	3	2	1	0
Read	PMSTAT							
Write								
Reset	*	*	*	*	*	*	*	*

* Notes:
- PMSTAT field: When booting in run mode, the reset value is 0x01. When booting in VLPR mode, the reset value is 0x04.

SMC_PMSTAT field descriptions

Field	Description
PMSTAT	Power Mode Status **NOTE:** When debug is enabled, the PMSTAT will not update to STOP or VLPS **NOTE:** When a PSTOP mode is enabled, the PMSTAT will not update to STOP or VLPS **NOTE:** Since the RUNM bits in the PMCTRL register are reset to VLPR on any Chip Reset not VLLS, the PMSTAT will update to VLPR shortly after the reset sequence is complete. 0000_0001 Current power mode is RUN. 0000_0010 Current power mode is STOP. 0000_0100 Current power mode is VLPR. 0000_1000 Current power mode is VLPW. 0001_0000 Current power mode is VLPS. 0010_0000 Current power mode is LLS. 0100_0000 Current power mode is VLLS. 1000_0000 Current power mode is HSRUN

17.4 Functional description

17.4.1 Power mode transitions

The following figure shows the power mode state transitions available on the chip. Any reset will initially bring the MCU back to the normal RUN state. However, in order to minimize peak power consumption, the RUNM bits in the PMCTRL register can be reset to VLPR via Flash IFR settings, causing the SMC to begin transitioning the MCU into VLPR mode during the reset recovery sequence.

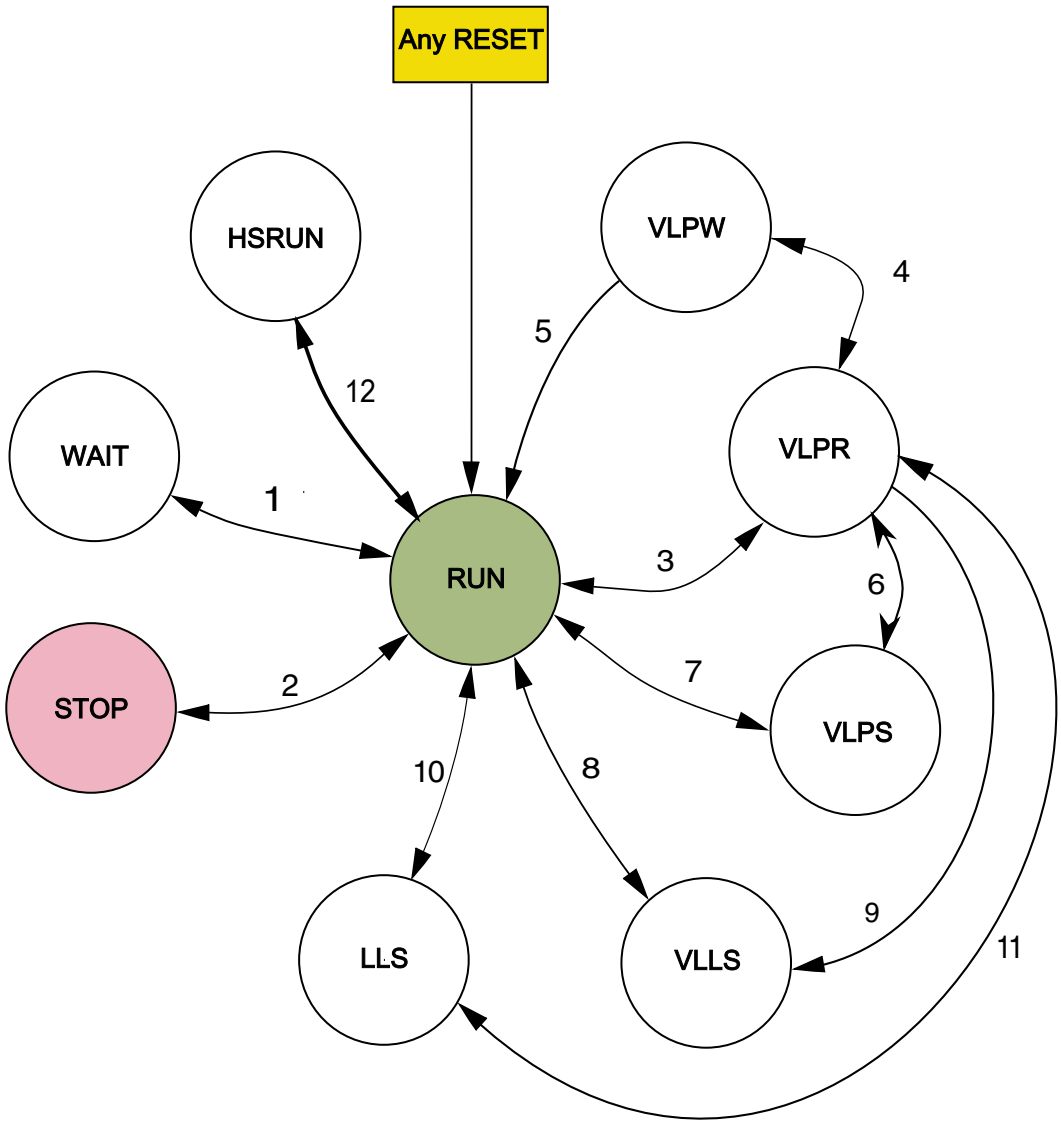


Figure 17-1. Power mode state diagram

The following table defines triggers for the various state transitions shown in the previous figure.

Table 17-2. Power mode transition triggers

Transition #	From	To	Trigger conditions
1	RUN	WAIT	Sleep-now or sleep-on-exit modes entered with SLEEPDEEP clear, controlled in System Control Register in ARM core. See note.[1]
	WAIT	RUN	Interrupt or Reset
2	RUN	STOP	PMCTRL[RUNM]=00, PMCTRL[STOPM]=000[2]

Table continues on the next page...

Table 17-2. Power mode transition triggers (continued)

Transition #	From	To	Trigger conditions
			Sleep-now or sleep-on-exit modes entered with SLEEPDEEP set, which is controlled in System Control Register in ARM core. See note.[1]
	STOP	RUN	Interrupt or Reset
3	RUN	VLPR	The core, system, bus and flash clock frequencies and MCG clocking mode are restricted in this mode. See the Power Management chapter for the maximum allowable frequencies and MCG modes supported. Set PMPROT[AVLP]=1, PMCTRL[RUNM]=10. **NOTE:** In order to limit peak current, PMPROT[AVLP] and PMCTRL[RUNM] bits can be set on any Reset via Flash IFR settings, causing the SMC to transition the MCU from RUN->VLPR during the reset recovery sequence.
	VLPR	RUN	Set PMCTRL[RUNM]=00 or Reset.
4	VLPR	VLPW	Sleep-now or sleep-on-exit modes entered with SLEEPDEEP clear, which is controlled in System Control Register in ARM core. See note.[1]
	VLPW	VLPR	Interrupt
5	VLPW	RUN	Reset
6	VLPR	VLPS	PMCTRL[STOPM]=000[3] or 010, Sleep-now or sleep-on-exit modes entered with SLEEPDEEP set, which is controlled in System Control Register in ARM core. See note.[1]
	VLPS	VLPR	Interrupt **NOTE:** If VLPS was entered directly from RUN (transition #7), hardware forces exit back to RUN and does not allow a transition to VLPR.
7	RUN	VLPS	PMPROT[AVLP]=1, PMCTRL[STOPM]=010, Sleep-now or sleep-on-exit modes entered with SLEEPDEEP set, which is controlled in System Control Register in ARM core. See note.[1]
	VLPS	RUN	Interrupt and VLPS mode was entered directly from RUN or Reset
8	RUN	VLLSx	PMPROT[AVLLS]=1, PMCTRL[STOPM]=100, STOPCTRL[LLSM]=x (VLLSx), Sleep-now or sleep-on-exit modes entered with SLEEPDEEP set, which is controlled in System Control Register in ARM core.
	VLLSx	RUN	Wakeup from enabled LPTMR input source or RESET pin

Table continues on the next page...

Table 17-2. Power mode transition triggers (continued)

Transition #	From	To	Trigger conditions
9	VLPR	VLLSx	PMPROT[AVLLS]=1, PMCTRL[STOPM]=100, STOPCTRL[LLSM]=x (VLLSx), Sleep-now or sleep-on-exit modes entered with SLEEPDEEP set, which is controlled in System Control Register in ARM core.
10	RUN	LLSx	PMPROT[ALLS]=1, PMCTRL[STOPM]=011, STOPCTRL[LLSM]=x (LLSx), Sleep-now or sleep-on-exit modes entered with SLEEPDEEP set, which is controlled in System Control Register in ARM core.
	LLSx	RUN	Wakeup from enabled LLWU input source and LLSx mode was entered directly from RUN or RESET pin.
11	VLPR	LLSx	PMPROT[ALLS]=1, PMCTRL[STOPM]=011, Sleep-now or sleep-on-exit modes entered with SLEEPDEEP set, which is controlled in System Control Register in ARM core.
	LLSx	VLPR	Wakeup from enabled LLWU input source and LLSx mode was entered directly from VLPR **NOTE:** If LLSx was entered directly from RUN, hardware will not allow this transition and will force exit back to RUN
12	RUN	HSRUN	Set PMPROT[AHSRUN]=1, PMCTRL[RUNM]=11.
	HSRUN	RUN	Set PMCTRL[RUNM]=00 or Reset

1. If debug is enabled, the core clock remains to support debug.
2. If PMCTRL[STOPM]=000 and STOPCTRL[PSTOPO]=01 or 10, then only a Partial Stop mode is entered instead of STOP
3. If PMCTRL[STOPM]=000 and STOPCTRL[PSTOPO]=00, then VLPS mode is entered instead of STOP. If PMCTRL[STOPM]=000 and STOPCTRL[PSTOPO]=01 or 10, then only a Partial Stop mode is entered instead of VLPS

17.4.2 Power mode entry/exit sequencing

When entering or exiting low-power modes, the system must conform to an orderly sequence to manage transitions safely.

The SMC manages the system's entry into and exit from all power modes. This diagram illustrates the connections of the SMC with other system components in the chip that are necessary to sequence the system through all power modes.

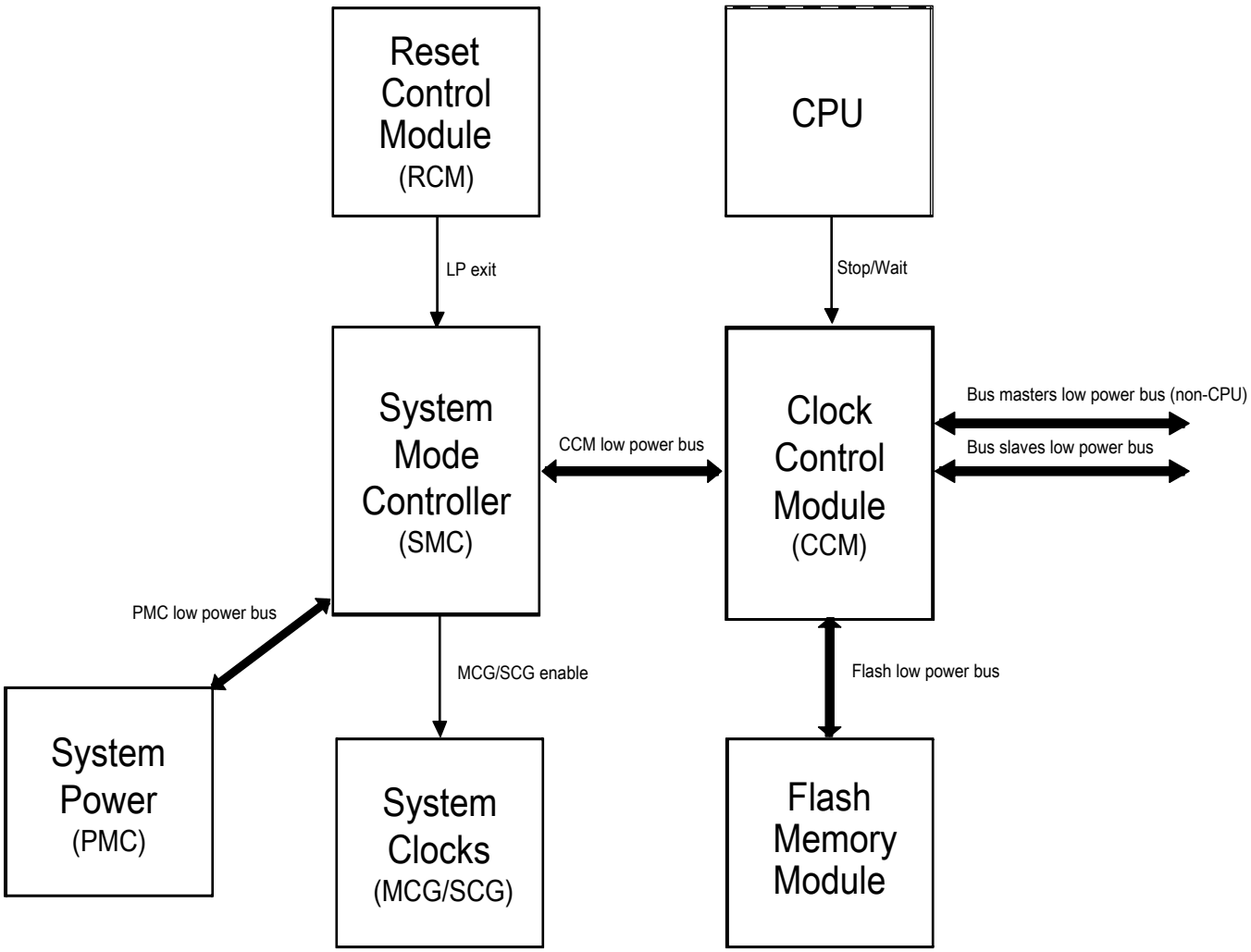


Figure 17-2. Low-power system components and connections

17.4.2.1 Stop mode entry sequence

Entry into a low-power stop mode (Stop, VLPS, LLS, VLLSx) is initiated by a CPU executing the WFI instruction. After the instruction is executed, the following sequence occurs:

1. The CPU clock is gated off immediately.
2. Requests are made to all non-CPU bus masters to enter Stop mode.
3. After all masters have acknowledged they are ready to enter Stop mode, requests are made to all bus slaves to enter Stop mode.
4. After all slaves have acknowledged they are ready to enter Stop mode, all system and bus clocks are gated off.
5. Clock generators are disabled in the MCG.
6. The on-chip regulator in the PMC and internal power switches are configured to meet the power consumption goals for the targeted low-power mode.

17.4.2.2 Stop mode exit sequence

Exit from a low-power stop mode is initiated either by a reset or an interrupt event. The following sequence then executes to restore the system to a run mode (RUN or VLPR):

1. The on-chip regulator in the PMC and internal power switches are restored.
2. Clock generators are enabled in the MCG.
3. System and bus clocks are enabled to all masters and slaves.
4. The CPU clock is enabled and the CPU begins servicing the reset or interrupt that initiated the exit from the low-power stop mode.

17.4.2.3 Aborted stop mode entry

If an interrupt occurs during a stop entry sequence, the SMC can abort the transition early and return to RUN mode without completely entering the stop mode. An aborted entry is possible only if the interrupt occurs before the PMC begins the transition to stop mode regulation. After this point, the interrupt is ignored until the PMC has completed its transition to stop mode regulation. When an aborted stop mode entry sequence occurs, SMC_PMCTRL[STOPA] is set to 1.

17.4.2.4 Transition to wait modes

For wait modes (WAIT and VLPW), the CPU clock is gated off while all other clocking continues, as in RUN and VLPR mode operation. Some modules that support stop-in-wait functionality have their clocks disabled in these configurations.

17.4.2.5 Transition from stop modes to Debug mode

The debugger module supports a transition from STOP, WAIT, VLPS, and VLPW back to a Halted state when the debugger has been enabled. As part of this transition, system clocking is re-established and is equivalent to the normal RUN and VLPR mode clocking configuration.

17.4.3 Run modes

The run modes supported by this device can be found here.

- Run (RUN)

- Very Low-Power Run (VLPR)
- High Speed Run (HSRUN)

17.4.3.1 RUN mode

This mode is selected after any reset. In order to reduce peak power consumption, however, the SMC will begin transitioning the MCU into VLPR mode during the reset recovery sequence. When the ARM processor exits reset, it sets up the stack, program counter (PC), and link register (LR):

- The processor reads the start SP (SP_main) from vector-table offset 0x000
- The processor reads the start PC from vector-table offset 0x004
- LR is set to 0xFFFF_FFFF.

To reduce power in this mode, disable the clocks to unused modules using their corresponding clock gating control bits in the SIM's (or PCC's) registers.

17.4.3.2 Very-Low Power Run (VLPR) mode

In VLPR mode, the on-chip voltage regulator is put into a stop mode regulation state. In this state, the regulator is designed to supply enough current to the MCU over a reduced frequency. To further reduce power in this mode, disable the clocks to unused modules using their corresponding clock gating control bits in the SIM's registers.

Before entering this mode, the following conditions must be met:

- The MCG must be configured in a mode which is supported during VLPR. See the Power Management details for information about these MCG modes.
- All clock monitors in the MCG must be disabled.
- The maximum frequencies of the system, bus, flash, and core are restricted. See the Power Management details about which frequencies are supported.
- Mode protection must be set to allow VLP modes, that is, PMPROT[AVLP] is 1.
- PMCTRL[RUNM] must be set to 10b to enter VLPR.
- Flash programming/erasing is not allowed.

NOTE

Do not increase the clock frequency while in VLPR mode, because the regulator is slow in responding and cannot manage fast load transitions. In addition, do not modify the clock source in the MCG module or any clock divider registers. Module clock enables in the SIM can be set, however should only be cleared one at a time to limit load transitions.

To reenter Normal Run mode, clear PMCTRL[RUNM]. PMSTAT is a read-only status register that can be used to determine when the system has completed an exit to RUN mode. When PMSTAT=RUN, the system is in run regulation and the MCU can run at full speed in any clock mode. If a higher execution frequency is desired, poll PMSTAT until it is set to RUN when returning from VLPR mode.

Any reset will initially cause the device to exit to RUN mode, however Flash IFR settings can be used to return the part to VLPR during the MCU reset flow.

17.4.3.3 High Speed Run (HSRUN) mode

In HSRUN mode, the on-chip voltage regulator remains in a run regulation state, but with a slightly elevated voltage output. In this state, the MCU is able to operate at a faster frequency compared to normal RUN mode. For the maximum allowable frequencies, see the Power Management chapter.

While in this mode, the following restrictions must be adhered to:

- The maximum allowable change in frequency of the system, bus, flash or core clocks is restricted to 2x (double the frequency).
- Before exiting HSRUN mode, clock frequencies should be reduced back down to those acceptable in RUN mode.
- Stop mode entry is not supported from HSRUN.
- Modifications to clock gating control bits are prohibited.
- Flash programming/erasing is not allowed.

To enter HSRUN mode, set PMPORT[AHSRUN]=HSRUN and set PMCTRL[RUNM]=HSRUN. Before increasing clock frequencies, the PMSTAT register should be polled to determine when the system has completed entry into HSRUN mode. To reenter normal RUN mode, clear RUNM. Any reset will also clear RUNM and cause the system to exit to normal RUN mode after the MCU exits its reset flow.

17.4.4 Wait modes

This device contains two different wait modes which are listed here.

- Wait
- Very-Low Power Wait (VLPW)

17.4.4.1 WAIT mode

WAIT mode is entered when the ARM core enters the Sleep-Now or Sleep-On-Exit modes while SLEEPDEEP is cleared. The ARM CPU enters a low-power state in which it is not clocked, but peripherals continue to be clocked provided they are enabled. Clock gating to the peripheral is enabled via the SIM module.

When an interrupt request occurs, the CPU exits WAIT mode and resumes processing in RUN mode, beginning with the stacking operations leading to the interrupt service routine.

A system reset will cause an exit from WAIT mode, temporarily returning the device to RUN mode before transitioning into VLPR during the MCU reset flow.

17.4.4.2 Very-Low-Power Wait (VLPW) mode

VLPW is entered by the entering the Sleep-Now or Sleep-On-Exit mode while SLEEPDEEP is cleared and the MCU is in VLPR mode.

In VLPW, the on-chip voltage regulator remains in its stop regulation state. In this state, the regulator is designed to supply enough current to the MCU over a reduced frequency. To further reduce power in this mode, disable the clocks to unused modules by clearing the peripherals' corresponding clock gating control bits in the SIM (or PCC).

VLPR mode restrictions also apply to VLPW.

When an interrupt from VLPW occurs, the device returns to VLPR mode to execute the interrupt service routine.

A system reset will cause an exit from VLPW mode, temporarily returning the device to RUN mode before transitioning into VLPR during the MCU reset flow.

17.4.5 Stop modes

This device contains a variety of stop modes to meet your application needs.

The stop modes range from:

- a stopped CPU, with all I/O, logic, and memory states retained, and certain asynchronous mode peripherals operating

to:

- a powered down CPU, with only I/O and a small register file retained, very few asynchronous mode peripherals operating, while the remainder of the MCU is powered down.

The choice of stop mode depends upon the user's application, and how power usage and state retention versus functional needs and recovery time may be traded off.

NOTE

All clock monitors must be disabled before entering these low-power modes: Stop, VLPS, VLPR, VLPW, LLSand VLLSx.

The various stop modes are selected by setting the appropriate fields in PMPROT and PMCTRL. The selected stop mode is entered during the sleep-now or sleep-on-exit entry with the SLEEPDEEP bit set in the System Control Register in the ARM core.

The available stop modes are:

- Normal Stop (STOP)
- Very-Low Power Stop (VLPS)
- Low-Leakage Stop (LLS)
- Very-Low-Leakage Stop (VLLSx)

17.4.5.1 STOP mode

STOP mode is entered via the sleep-now or sleep-on-exit with the SLEEPDEEP bit set in the System Control Register in the ARM core.

The MCG module can be configured to leave the reference clocks running.

A module capable of providing an asynchronous interrupt to the device takes the device out of STOP mode and returns the device to normal RUN mode. Refer to the device's Power Management chapter for peripheral, I/O, and memory operation in STOP mode. When an interrupt request occurs, the CPU exits STOP mode and resumes processing, beginning with the stacking operations leading to the interrupt service routine.

A system reset will cause an exit from STOP mode, temporarily returning the device to RUN mode before transitioning into VLPR during the MCU reset flow.

17.4.5.2 Very-Low-Power Stop (VLPS) mode

The two ways in which VLPS mode can be entered are listed here.

- Entry into stop via the sleep-now or sleep-on-exit with the SLEEPDEEP bit set in the System Control Register in the ARM core while the MCU is in VLPR mode and PMCTRL[STOPM] = 010 or 000.
- Entry into stop via the sleep-now or sleep-on-exit with the SLEEPDEEP bit set in the System Control Register in the ARM core while the MCU is in normal RUN mode and PMCTRL[STOPM] = 010. When VLPS is entered directly from RUN mode, exit to VLPR is disabled by hardware and the system will always exit back to RUN.

In VLPS, the on-chip voltage regulator remains in its stop regulation state as in VLPR.

A module capable of providing an asynchronous interrupt to the device takes the device out of VLPS and returns the device to VLPR mode.

A system reset will cause an exit from VLPS mode, temporarily returning the device to RUN mode before transitioning into VLPR during the MCU reset flow.

17.4.5.3 Low-Leakage Stop (LLSx) modes

This device contains two Low-Leakage Stop modes: LLS3 and LLS2. LLS or LLSx is often used in this document to refer to both modes. All LLS modes can be entered from normal RUN or VLPR modes.

The MCU enters LLS mode if:

- In Sleep-Now or Sleep-On-Exit mode, SLEEPDEEP is set in the System Control Register in the ARM core, and
- The device is configured as shown in Table 17-2.

In LLS, the on-chip voltage regulator is in stop regulation. Most of the peripherals are put in a state-retention mode that does not allow them to operate while in LLS.

Before entering LLS mode, the user should configure the Low-Leakage Wake-up (LLWU) module to enable the desired wake-up sources. The available wake-up sources in LLS are detailed in the chip configuration details for this device.

After wakeup from LLS, the device returns to the run mode from which LLS was entered (either normal RUN or VLPR) with a pending LLWU module interrupt. If LLS was entered from VLPR mode, then the MCU will begin VLPR entry shortly after wake-up. In the LLWU interrupt service routine (ISR), the user can poll the LLWU module wake-up flags to determine the source of the wakeup.

NOTE

The LLWU interrupt must not be masked by the interrupt controller to avoid a scenario where the system does not fully exit Stop mode on an LLS recovery.

An asserted RESET pin will cause an exit from LLS mode, temporarily returning the device to normal RUN mode before transitioning into VLPR during the MCU reset flow. When LLS is exiting via the RESET pin, RCM_SRS[PIN] and RCM_SRS[WAKEUP] are set.

17.4.5.4 Very-Low-Leakage Stop (VLLSx) modes

This device contains these very low leakage modes:

- VLLS3
- VLLS2
- VLLS1
- VLLS0

VLLSx is often used in this document to refer to all of these modes.

All VLLSx modes can be entered from normal RUN or VLPR modes.

The MCU enters the configured VLLS mode if:

- In Sleep-Now or Sleep-On-Exit mode, the SLEEPDEEP bit is set in the System Control Register in the ARM core, and
- The device is configured as shown in Table 17-2.

In VLLS, the on-chip voltage regulator is in its stop-regulation state while most digital logic is powered off.

Before entering VLLS mode, the user should configure the Low-Leakage Wake-up (LLWU) module to enable the desired wakeup sources. The available wake-up sources in VLLS are detailed in the chip configuration details for this device.

After wakeup from VLLS, the device returns to normal RUN mode with a pending LLWU interrupt. If VLLS was entered from VLPR mode, then the MCU will begin VLPR entry shortly after wakeup. In the LLWU interrupt service routine (ISR), the user can poll the LLWU module wake-up flags to determine the source of the wake-up.

When entering VLLS, each I/O pin is latched as configured before executing VLLS. Because all digital logic in the MCU is powered off, all port and peripheral data is lost during VLLS. This information must be restored before PMC_REGSC[ACKISO] is set.

An asserted RESET pin will cause an exit from any VLLS mode, temporarily returning the device to normal RUN mode before transitioning into VLPR during the MCU reset flow. When exiting VLLS via the RESET pin, RCM_SRS[PIN] and RCM_SRS[WAKEUP] are set.

17.4.6 Debug in low power modes

When the MCU is secure, the device disables/limits debugger operation. When the MCU is unsecure, the ARM debugger can assert two power-up request signals:

- System power up, via SYSPWR in the Debug Port Control/Stat register
- Debug power up, via CDBGPWRUPREQ in the Debug Port Control/Stat register

When asserted while in RUN, WAIT, VLPR, or VLPW, the mode controller drives a corresponding acknowledge for each signal, that is, both CDBGPWRUPACK and CSYSPWRUPACK. When both requests are asserted, the mode controller handles attempts to enter STOP and VLPS by entering an emulated stop state. In this emulated stop state:

- the regulator is in run regulation,
- the MCG-generated clock source is enabled,
- all system clocks, except the core clock, are disabled,
- the debug module has access to core registers, and
- access to the on-chip peripherals is blocked.

No debug is available while the MCU is in LLS or VLLS modes. LLS is a state-retention mode and all debug operation can continue after waking from LLS, even in cases where system wakeup is due to a system reset event.

Entering into a VLLS mode causes all of the debug controls and settings to be powered off. To give time to the debugger to sync with the MCU, the MDM AP Control Register includes a Very-Low-Leakage Debug Request (VLLDBGREQ) bit that is set to configure the Reset Controller logic to hold the system in reset after the next recovery from a VLLS mode. This bit allows the debugger time to reinitialize the debug module before the debug session continues.

The MDM AP Control Register also includes a Very Low Leakage Debug Acknowledge (VLLDBGACK) bit that is set to release the ARM core being held in reset following a VLLS recovery. The debugger reinitializes all debug IP, and then asserts the VLLDBGACK control bit to allow the RCM to release the ARM core from reset and allow CPU operation to begin.

The VLLDBGACK bit is cleared by the debugger (or can be left set as is) or clears automatically due to the reset generated as part of the next VLLS recovery.

Chapter 18
Power Management Controller (PMC)

18.1 Introduction

The power management controller (PMC) contains the internal voltage regulator, power on reset (POR), low voltage detect system (LVD), and high voltage detect system (HVD).

See AN4503: Power Management for Kinetis MCUs for further details on using the PMC.

18.2 Features

A list of included PMC features can be found here.

- Internal voltage regulator
- Active POR providing brown-out detect
- Low-voltage detect supporting two low-voltage trip points with four warning levels per trip point
- High-voltage detect supporting two high-voltage trip points

18.3 Low-voltage detect (LVD) system

This device includes a system to guard against low-voltage conditions. This protects memory contents and controls MCU system states during supply voltage variations.

The system is comprised of a power-on reset (POR) circuit and a LVD circuit with a user-selectable trip voltage: high (V_{LVDH}) or low (V_{LVDL}). The trip voltage is selected by LVDSC1[LVDV]. The LVD is disabled upon entering VLPx, LLS, and VLLSx modes.

Two flags are available to indicate the status of the low-voltage detect system:

- The Low Voltage Detect Flag in the Low Voltage Status and Control 1 Register (LVDSC1[LVDF]) operates in a level sensitive manner. LVDSC1[LVDF] is set when the supply voltage falls below the selected trip point (VLVD). LVDSC1[LVDF] is cleared by writing 1 to LVDSC1[LVDACK], but only if the internal supply has returned above the trip point; otherwise, LVDSC1[LVDF] remains set.
- The Low Voltage Warning Flag (LVWF) in the Low Voltage Status and Control 2 Register (LVDSC2[LVWF]) operates in a level sensitive manner. LVDSC2[LVWF] is set when the supply voltage falls below the selected monitor trip point (VLVW). LVDSC2[LVWF] is cleared by writing one to LVDSC2[LVWACK], but only if the internal supply has returned above the trip point; otherwise, LVDSC2[LVWF] remains set.

18.3.1 LVD reset operation

By setting LVDSC1[LVDRE], the LVD generates a reset upon detection of a low-voltage condition. The low-voltage detection threshold is determined by LVDSC1[LVDV]. After an LVD reset occurs, the LVD system holds the MCU in reset until the supply voltage rises above this threshold. The LVD field in the SRS register of the RCM module (RCM_SRS[LVD]) is set following an LVD or power-on reset.

18.3.2 LVD interrupt operation

By configuring the LVD circuit for interrupt operation (LVDSC1[LVDIE] set and LVDSC1[LVDRE] clear), LVDSC1[LVDF] is set and an LVD interrupt request occurs upon detection of a low voltage condition. LVDSC1[LVDF] is cleared by writing 1 to LVDSC1[LVDACK].

18.3.3 Low-voltage warning (LVW) interrupt operation

The LVD system contains a Low-Voltage Warning Flag (LVWF) in the Low Voltage Detect Status and Control 2 Register to indicate that the supply voltage is approaching, but is above, the LVD voltage. The LVW also has an interrupt, which is enabled by setting LVDSC2[LVWIE]. If enabled, an LVW interrupt request occurs when LVDSC2[LVWF] is set. LVDSC2[LVWF] is cleared by writing 1 to LVDSC2[LVWACK].

LVDSC2[LVWV] selects one of the four trip voltages:

- Highest: V_{LVW4}
- Two mid-levels: V_{LVW3} and V_{LVW2}
- Lowest: V_{LVW1}

18.4 High-voltage detect (HVD) system

This device includes a system to guard against high-voltage conditions.

The system is comprised of a HVD circuit with a user-selectable trip voltage: high (V_{HVDH}) or low (V_{HVDL}). The trip voltage is selected by HVDSC1[HVDV]. The HVD is disabled upon entering VLPx, LLS, and VLLSx modes.

A flag is available to indicate the status of the high-voltage detect system:

- The High Voltage Detect Flag in the High Voltage Status and Control 1 Register (HVDSC1[HVDF]) operates in a level sensitive manner. HVDSC1[HVDF] is set when the supply voltage rises above the selected trip point (VHVD). HVDSC1[HVDF] is cleared by writing 1 to HVDSC1[HVDACK], but only if the internal supply has returned below the trip point; otherwise, HVDSC1[LVDF] remains set.

18.4.1 HVD reset operation

By setting HVDSC1[HVDRE], the HVD generates a reset upon detection of a high-voltage condition. The high-voltage detection threshold is determined by HVDSC1[HVDV]. After an HVD reset occurs, the HVD system holds the MCU in reset until the supply voltage falls below this threshold. The LVD field in the SRS register of the RCM module (RCM_SRS[LVD]) is set following an HVD reset.

18.4.2 HVD interrupt operation

By configuring the HVD circuit for interrupt operation (HVDSC1[HVDIE] set and HVDSC1[HVDRE] clear), HVDSC1[HVDF] is set and an HVD interrupt request occurs upon detection of a high voltage condition. HVDSC1[HVDF] is cleared by writing 1 to HVDSC1[HVDACK].

18.5 I/O retention

When in LLS mode, the I/O pins are held in their input or output state.

Upon wakeup, the PMC is re-enabled, goes through a power up sequence to full regulation, and releases the logic from state retention mode. The I/O are released immediately after a wake-up or reset event. In the case of LLS exit via a RESET pin, the I/O default to their reset state.

When in VLLS modes, the I/O states are held on a wake-up event (with the exception of wake-up by reset event) until the wake-up has been acknowledged via a write to REGSC[ACKISO]. In the case of VLLS exit via a RESET pin, the I/O are released and default to their reset state. In this case, no write to REGSC[ACKISO] is needed.

18.6 Memory map and register descriptions

Details about the PMC registers can be found here.

NOTE

Different portions of PMC registers are reset only by particular reset types. Each register's description provides details. For more information about the types of reset on this chip, refer to the Reset section details.

The PMC registers can be written only in supervisor mode. Write accesses in user mode are blocked and will result in a bus error.

PMC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4007_D000	Low Voltage Detect Status And Control 1 register (PMC_LVDSC1)	8	R/W	10h	18.6.1/397
4007_D001	Low Voltage Detect Status And Control 2 register (PMC_LVDSC2)	8	R/W	00h	18.6.2/398
4007_D002	Regulator Status And Control register (PMC_REGSC)	8	R/W	04h	18.6.3/399
4007_D00B	High Voltage Detect Status And Control 1 register (PMC_HVDSC1)	8	R/W	01h	18.6.4/401

18.6.1 Low Voltage Detect Status And Control 1 register (PMC_LVDSC1)

This register contains status and control bits to support the low voltage detect function. This register should be written during the reset initialization program to set the desired controls even if the desired settings are the same as the reset settings.

While the device is in the very low power or low leakage modes, the LVD system is disabled regardless of LVDSC1 settings. To protect systems that must have LVD always on, configure the Power Mode Protection (PMPROT) register of the SMC module (SMC_PMPROT) to disallow any very low power or low leakage modes from being enabled.

See the device's data sheet for the exact LVD trip voltages.

NOTE

The LVDV bits are reset solely on a POR Only event. The register's other bits are reset on Chip Reset Not VLLS. For more information about these reset types, refer to the Reset section details.

Address: 4007_D000h base + 0h offset = 4007_D000h

Bit	7	6	5	4	3	2	1	0
Read	LVDF	0	LVDIE	LVDRE	0		LVDV	
Write		LVDACK						
Reset	0	0	0	1	0	0	0	0

PMC_LVDSC1 field descriptions

Field	Description
7 LVDF	Low-Voltage Detect Flag This read-only status field indicates a low-voltage detect event. 0 Low-voltage event not detected 1 Low-voltage event detected
6 LVDACK	Low-Voltage Detect Acknowledge This write-only field is used to acknowledge low voltage detection errors. Write 1 to clear LVDF. Reads always return 0.
5 LVDIE	Low-Voltage Detect Interrupt Enable Enables hardware interrupt requests for LVDF. 0 Hardware interrupt disabled (use polling) 1 Request a hardware interrupt when LVDF = 1

Table continues on the next page...

PMC_LVDSC1 field descriptions (continued)

Field	Description
4 LVDRE	Low-Voltage Detect Reset Enable This write-once bit enables LVDF events to generate a hardware reset. Additional writes are ignored. 0 LVDF does not generate hardware resets 1 Force an MCU reset when LVDF = 1
3–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
LVDV	Low-Voltage Detect Voltage Select Selects the LVD trip point voltage (V_{LVD}). 00 Low trip point selected ($V_{LVD} = V_{LVDL}$) 01 High trip point selected ($V_{LVD} = V_{LVDH}$) 10 Reserved 11 Reserved

18.6.2 Low Voltage Detect Status And Control 2 register (PMC_LVDSC2)

This register contains status and control bits to support the low voltage warning function.

While the device is in the very low power or low leakage modes, the LVD system is disabled regardless of LVDSC2 settings.

See the device's data sheet for the exact LVD trip voltages.

NOTE

The LVW trip voltages depend on LVWV and LVDV.

NOTE

LVWV is reset solely on a POR Only event. The other fields of the register are reset on Chip Reset Not VLLS. For more information about these reset types, refer to the Reset section details.

Address: 4007_D000h base + 1h offset = 4007_D001h

Bit	7	6	5	4	3	2	1	0
Read	LVWF	0	LVWIE	0			LVWV	
Write		LVWACK						
Reset	0	0	0	0	0	0	0	0

PMC_LVDSC2 field descriptions

Field	Description
7 LVWF	Low-Voltage Warning Flag This read-only status field indicates a low-voltage warning event. LVWF is set when V_{Supply} transitions below the trip point, or after reset and V_{Supply} is already below V_{LVW}. LVWF may be 1 after power-on reset, therefore, to use LVW interrupt function, before enabling LVWIE, LVWF must be cleared by writing LVWACK first. 0 Low-voltage warning event not detected 1 Low-voltage warning event detected
6 LVWACK	Low-Voltage Warning Acknowledge This write-only field is used to acknowledge low voltage warning errors. Write 1 to clear LVWF. Reads always return 0.
5 LVWIE	Low-Voltage Warning Interrupt Enable Enables hardware interrupt requests for LVWF. 0 Hardware interrupt disabled (use polling) 1 Request a hardware interrupt when LVWF = 1
4–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
LVWV	Low-Voltage Warning Voltage Select Selects the LVW trip point voltage (V_{LVW}). The actual voltage for the warning depends on LVDSC1[LVDV]. 00 Low trip point selected ($V_{LVW} = V_{LVW1}$) 01 Mid 1 trip point selected ($V_{LVW} = V_{LVW2}$) 10 Mid 2 trip point selected ($V_{LVW} = V_{LVW3}$) 11 High trip point selected ($V_{LVW} = V_{LVW4}$)

18.6.3 Regulator Status And Control register (PMC_REGSC)

The PMC contains an internal voltage regulator. The voltage regulator design uses a bandgap reference that is also available through a buffer as input to certain internal peripherals, such as the CMP and ADC. The internal regulator provides a status bit (REGONS) indicating the regulator is in run regulation.

NOTE

This register is reset on Chip Reset Not VLLS and by reset types that trigger Chip Reset not VLLS. See the Reset section details for more information.

Address: 4007_D000h base + 2h offset = 4007_D002h

Bit	7	6	5	4	3	2	1	0
Read	0	0	Reserved	BGEN	ACKISO	REGONS	Reserved	BGBE
Write					w1c			
Reset	0	0	0	0	0	1	0	0

PMC_REGSC field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 Reserved	This field is reserved.
4 BGEN	Bandgap Enable In VLPx Operation BGEN controls whether the bandgap is enabled in lower power modes of operation (VLPx, LLS, and VLLSx). When on-chip peripherals require the bandgap voltage reference in low power modes of operation, set BGEN to continue to enable the bandgap operation. **NOTE:** When the bandgap voltage reference is not needed in low power modes, clear BGEN to avoid excess power consumption. 0 Bandgap voltage reference is disabled in VLPx , LLS , and VLLSx modes. 1 Bandgap voltage reference is enabled in VLPx , LLS , and VLLSx modes.
3 ACKISO	Acknowledge Isolation Reading this field indicates whether certain peripherals and the I/O pads are in a latched state as a result of having been in a VLLS mode. Writing 1 to this field when it is set releases the I/O pads and certain peripherals to their normal run mode state. **NOTE:** After recovering from a VLLS mode, user should restore chip configuration before clearing ACKISO. In particular, pin configuration for enabled LLWU wakeup pins should be restored to avoid any LLWU flag from being falsely set when ACKISO is cleared. 0 Peripherals and I/O pads are in normal run state. 1 Certain peripherals and I/O pads are in an isolated and latched state.
2 REGONS	Regulator In Run Regulation Status This read-only field provides the current status of the internal voltage regulator. 0 Regulator is in stop regulation or in transition to/from it 1 Regulator is in run regulation
1 Reserved	This field is reserved. **NOTE:** This reserved bit must remain cleared (set to 0).
0 BGBE	Bandgap Buffer Enable Enables the bandgap buffer. 0 Bandgap buffer not enabled 1 Bandgap buffer enabled

18.6.4 High Voltage Detect Status And Control 1 register (PMC_HVDSC1)

This register contains status and control bits to support the high voltage detect function. This register should be written during the reset initialization program to set the desired controls even if the desired settings are the same as the reset settings.

While the device is in the very low power or low leakage modes, the HVD system is disabled regardless of HVDSC1 settings. To protect systems that must have HVD always on, configure the Power Mode Protection (PMPROT) register of the SMC module (SMC_PMPROT) to disallow any very low power or low leakage modes from being enabled.

See the device's data sheet for the exact HVD trip voltages.

NOTE

This register is reset solely on a POR Only event.For more information about these reset types, refer to the Reset section details.

Address: 4007_D000h base + Bh offset = 4007_D00Bh

Bit	7	6	5	4	3	2	1	0
Read	HVDF	0	HVDIE	HVDRE	0			HVDV
Write		HVDACK						
Reset	0	0	0	0	0	0	0	1

PMC_HVDSC1 field descriptions

Field	Description
7 HVDF	High-Voltage Detect Flag This read-only status field indicates a high-voltage detect event. 0 High-voltage event not detected 1 High-voltage event detected
6 HVDACK	High-Voltage Detect Acknowledge This write-only field is used to acknowledge high voltage detection errors. Write 1 to clear HVDF. Reads always return 0.
5 HVDIE	High-Voltage Detect Interrupt Enable Enables hardware interrupt requests for HVDF. 0 Hardware interrupt disabled (use polling) 1 Request a hardware interrupt when HVDF = 1

Table continues on the next page...

PMC_HVDSC1 field descriptions (continued)

Field	Description
4 HVDRE	High-Voltage Detect Reset Enable This write-once bit enables HVDF events to generate a hardware reset. Additional writes are ignored until the next chip reset. 0 HVDF does not generate hardware resets 1 Force an MCU reset when HVDF = 1
3–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 HVDV	High-Voltage Detect Voltage Select Selects the HVD trip point voltage (V_{HVD}). 0 Low trip point selected ($V_{HVD} = V_{HVDL}$) 1 High trip point selected ($V_{HVD} = V_{HVDH}$)

Chapter 19
Low-Leakage Wakeup Unit (LLWU)

19.1 Chip-specific LLWU information

19.1.1 Wake-up Sources

The device uses the following internal peripheral and external pin inputs as wakeup sources to the LLWU module. LLWU_Px are external pin inputs, and LLWU_M0IF-M7IF are connections to the internal peripheral interrupt flags.

NOTE

In addition to the LLWU wakeup sources, the device also wakes from low power modes when NMI or RESET pins are enabled and the respective pin is asserted.

Table 19-1. Wakeup Sources for LLWU inputs

LLWU pin	Module source or pin name
LLWU_P0	PTE1
LLWU_P1	PTE2
LLWU_P2	PTE4
LLWU_P3	PTA4
LLWU_P4	PTA13
LLWU_P5	PTB0
LLWU_P6	PTC1
LLWU_P7	PTC3
LLWU_P8	PTC4
LLWU_P9	PTC5
LLWU_P10	PTC6
LLWU_P11	PTC11
LLWU_P12	PTD0

Table continues on the next page...

Table 19-1. Wakeup Sources for LLWU inputs (continued)

LLWU pin	Module source or pin name
LLWU_P13	PTD2
LLWU_P14	PTD4
LLWU_P15	PTD6
LLWU_P16	PTE6
LLWU_P17	PTE9
LLWU_P18	PTE10
LLWU_P19	PTE17
LLWU_P20	PTE18
LLWU_P21	PTA21
LLWU_P22	PTA10
LLWU_P23	PTA11
LLWU_P24	PTD8
LLWU_P25	PTD11
LLWU_P26	VREGIN [1]
LLWU_P27	USB0_DP
LLWU_P28	USB0_DM[2]
LLWU_P29	RESERVED
LLWU_P30	RESERVED
LLWU_P31	RESERVED
LLWU_M0IF	LPTMR0 or LPTMR1(sharing M0IF)[3]
LLWU_M1IF	CMP0
LLWU_M2IF	CMP1
LLWU_M3IF	RESERVED
LLWU_M4IF	TSI0
LLWU_M5IF	RTC Alarm
LLWU_M6IF	Reserved
LLWU_M7IF	RTC Seconds

1. A LLWU wakeup source VREGIN is not available for VLLS1 or VLLS0 mode.
2. As a wakeup source of LLWU, USB0_DP and USB0_DM are only available when the chip is in USB host mode.
3. Requires the peripheral and the peripheral interrupt to be enabled. The LLWU's WUME bit enables the internal module flag as a wakeup input. After wakeup, the flags are cleared based on the peripheral clearing mechanism.

19.2 Introduction

The LLWU module allows the user to select up to 29 external pins and up to 8 internal modules as interrupt wake-up sources from low-leakage power modes.

The input sources are described in the device's chip configuration details. Each of the available wake-up sources can be individually enabled.

The $\overline{\text{RESET}}$ pin is an additional source for triggering an exit from low-leakage power modes, and causes the MCU to exit both LLS and VLLS through a reset flow.

The LLWU module also includes optional digital pin filters for the external wakeup pins.

See AN4503: Power Management for Kinetis MCUs for further details on using the LLWU.

19.2.1 Features

The LLWU module features include:

- Support for up to 29 external input pins and up to 8 internal modules with individual enable bits for MCU interrupt from low leakage modes
- Input sources may be external pins or from internal peripherals capable of running in LLS or VLLS. See the chip configuration information for wakeup input sources for this device.
- External pin wake-up inputs, each of which is programmable as falling-edge, rising-edge, or any change
- Wake-up inputs that are activated after MCU enters a low-leakage power mode
- Optional digital filters provided to qualify an external pin detect. Note that when the LPO clock is disabled, the filters are disabled and bypassed.

19.2.2 Modes of operation

The LLWU module becomes functional on entry into a low-leakage power mode. After recovery from LLS, the LLWU is immediately disabled. After recovery from VLLS, the LLWU continues to detect wake-up events until the user has acknowledged the wake-up via a write to PMC_REGSC[ACKISO].

19.2.2.1 LLS mode

Wake-up events due to external pin inputs (LLWU_Px) and internal module interrupt inputs (LLWU_MxIF) result in an interrupt flow when exiting LLS.

NOTE

The LLWU interrupt must not be masked by the interrupt controller to avoid a scenario where the system does not fully exit Stop mode on an LLS recovery.

19.2.2.2 VLLS modes

All wakeup and reset events result in VLLS exit via a reset flow.

19.2.2.3 Non-low leakage modes

The LLWU is not active in all non-low leakage modes where detection and control logic are in a static state. The LLWU registers are accessible in non-low leakage modes and are available for configuring and reading status when bus transactions are possible.

When the wake-up pin filters are enabled, filter operation begins immediately. If a low leakage mode is entered within five LPO clock cycles of an active edge, the edge event will be detected by the LLWU.

19.2.2.4 Debug mode

When the chip is in Debug mode and then enters LLS or a VLLSx mode, no debug logic works in the fully-functional low-leakage mode. Upon an exit from the LLS or VLLSx mode, the LLWU becomes inactive.

19.2.3 Block diagram

The following figure is the block diagram for the LLWU module.

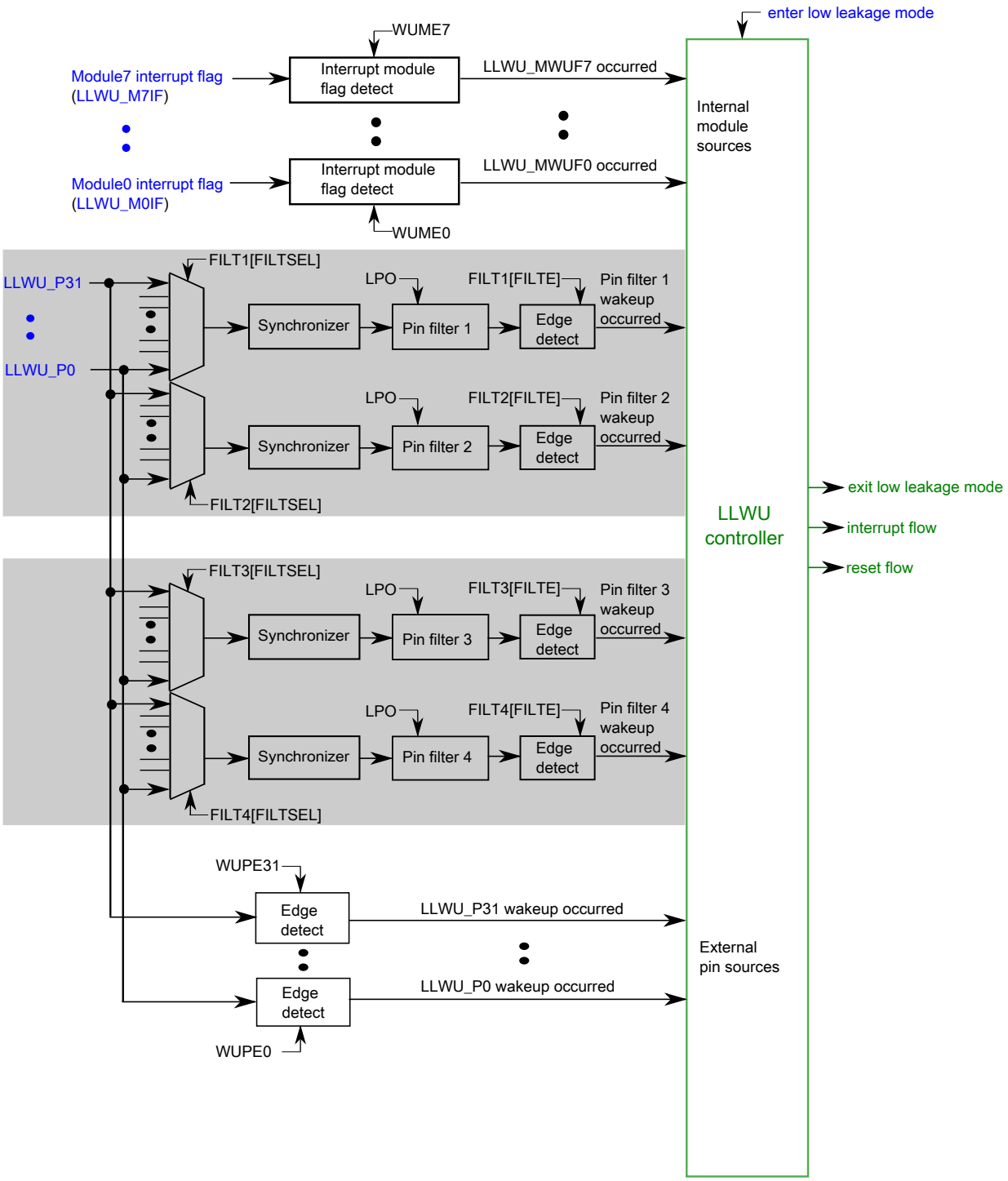


Figure 19-1. LLWU block diagram

19.3 LLWU signal descriptions

The signal properties of LLWU are shown in the table found here.

The external wakeup input pins can be enabled to detect either rising-edge, falling-edge, or on any change.

Table 19-2. LLWU signal descriptions

Signal	Description	I/O
LLWU_Pn	Wakeup inputs (n = 0- 28)	I

19.4 Memory map/register definition

The LLWU includes the following registers:

- Wake-up source enable registers
  - Enable external pin input sources
  - Enable internal peripheral interrupt sources
- Wake-up flag registers
  - Indication of wakeup source that caused exit from a low-leakage power mode includes external pin or internal module interrupt
- Wake-up pin filter enable registers

NOTE

The LLWU registers can be written only in supervisor mode. Write accesses in user mode are blocked and will result in a bus error.

All LLWU registers are reset by Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. Each register's displayed reset value represents this subset of reset types. LLWU registers are unaffected by reset types that do not trigger Chip Reset not VLLS. For more information about the types of reset on this chip, refer to the Introduction details.

LLWU memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4007_C000	LLWU Pin Enable 1 register (LLWU_PE1)	8	R/W	00h	19.4.1/409
4007_C001	LLWU Pin Enable 2 register (LLWU_PE2)	8	R/W	00h	19.4.2/410
4007_C002	LLWU Pin Enable 3 register (LLWU_PE3)	8	R/W	00h	19.4.3/411
4007_C003	LLWU Pin Enable 4 register (LLWU_PE4)	8	R/W	00h	19.4.4/412

Table continues on the next page...

LLWU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4007_C004	LLWU Pin Enable 5 register (LLWU_PE5)	8	R/W	00h	19.4.5/413
4007_C005	LLWU Pin Enable 6 register (LLWU_PE6)	8	R/W	00h	19.4.6/415
4007_C006	LLWU Pin Enable 7 register (LLWU_PE7)	8	R/W	00h	19.4.7/416
4007_C007	LLWU Pin Enable 8 register (LLWU_PE8)	8	R/W	00h	19.4.8/417
4007_C008	LLWU Module Enable register (LLWU_ME)	8	R/W	00h	19.4.9/418
4007_C009	LLWU Pin Flag 1 register (LLWU_PF1)	8	R/W	00h	19.4.10/419
4007_C00A	LLWU Pin Flag 2 register (LLWU_PF2)	8	R/W	00h	19.4.11/421
4007_C00B	LLWU Pin Flag 3 register (LLWU_PF3)	8	R/W	00h	19.4.12/423
4007_C00C	LLWU Pin Flag 4 register (LLWU_PF4)	8	R/W	00h	19.4.13/425
4007_C00D	LLWU Module Flag 5 register (LLWU_MF5)	8	R	00h	19.4.14/426
4007_C00E	LLWU Pin Filter 1 register (LLWU_FILT1)	8	R/W	00h	19.4.15/428
4007_C00F	LLWU Pin Filter 2 register (LLWU_FILT2)	8	R/W	00h	19.4.16/429
4007_C010	LLWU Pin Filter 3 register (LLWU_FILT3)	8	R/W	00h	19.4.17/430
4007_C011	LLWU Pin Filter 4 register (LLWU_FILT4)	8	R/W	00h	19.4.18/431

19.4.1 LLWU Pin Enable 1 register (LLWU_PE1)

LLWU_PE1 contains the field to enable and select the edge detect type for the external wakeup input pins LLWU_P3-LLWU_P0.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + 0h offset = 4007_C000h

Bit	7	6	5	4	3	2	1	0
Read Write	WUPE3		WUPE2		WUPE1		WUPE0	
Reset	0	0	0	0	0	0	0	0

LLWU_PE1 field descriptions

Field	Description
7–6 WUPE3	Wakeup Pin Enable For LLWU_P3 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection

Table continues on the next page...

LLWU_PE1 field descriptions (continued)

Field	Description
	10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
5–4 WUPE2	Wakeup Pin Enable For LLWU_P2 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
3–2 WUPE1	Wakeup Pin Enable For LLWU_P1 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
WUPE0	Wakeup Pin Enable For LLWU_P0 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection

19.4.2 LLWU Pin Enable 2 register (LLWU_PE2)

LLWU_PE2 contains the field to enable and select the edge detect type for the external wakeup input pins LLWU_P7-LLWU_P4.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + 1h offset = 4007_C001h

Bit	7	6	5	4	3	2	1	0
Read Write	WUPE7		WUPE6		WUPE5		WUPE4	
Reset	0	0	0	0	0	0	0	0

LLWU_PE2 field descriptions

Field	Description
7–6 WUPE7	Wakeup Pin Enable For LLWU_P7 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
5–4 WUPE6	Wakeup Pin Enable For LLWU_P6 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
3–2 WUPE5	Wakeup Pin Enable For LLWU_P5 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
WUPE4	Wakeup Pin Enable For LLWU_P4 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection

19.4.3 LLWU Pin Enable 3 register (LLWU_PE3)

LLWU_PE3 contains the field to enable and select the edge detect type for the external wakeup input pins LLWU_P11-LLWU_P8.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + 2h offset = 4007_C002h

Bit	7	6	5	4	3	2	1	0
Read Write	WUPE11		WUPE10		WUPE9		WUPE8	
Reset	0	0	0	0	0	0	0	0

LLWU_PE3 field descriptions

Field	Description
7–6 WUPE11	Wakeup Pin Enable For LLWU_P11 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
5–4 WUPE10	Wakeup Pin Enable For LLWU_P10 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
3–2 WUPE9	Wakeup Pin Enable For LLWU_P9 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
WUPE8	Wakeup Pin Enable For LLWU_P8 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection

19.4.4 LLWU Pin Enable 4 register (LLWU_PE4)

LLWU_PE4 contains the field to enable and select the edge detect type for the external wakeup input pins LLWU_P15-LLWU_P12.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset

types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + 3h offset = 4007_C003h

Bit	7	6	5	4	3	2	1	0
Read Write	WUPE15		WUPE14		WUPE13		WUPE12	
Reset	0	0	0	0	0	0	0	0

LLWU_PE4 field descriptions

Field	Description
7–6 WUPE15	Wakeup Pin Enable For LLWU_P15 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
5–4 WUPE14	Wakeup Pin Enable For LLWU_P14 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
3–2 WUPE13	Wakeup Pin Enable For LLWU_P13 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
WUPE12	Wakeup Pin Enable For LLWU_P12 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection

19.4.5 LLWU Pin Enable 5 register (LLWU_PE5)

LLWU_PE5 contains the field to enable and select the edge detect type for the external wakeup input pins LLWU_P19-LLWU_P16.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + 4h offset = 4007_C004h

Bit	7	6	5	4	3	2	1	0
Read Write	WUPE19		WUPE18		WUPE17		WUPE16	
Reset	0	0	0	0	0	0	0	0

LLWU_PE5 field descriptions

Field	Description
7–6 WUPE19	Wakeup Pin Enable For LLWU_P19 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
5–4 WUPE18	Wakeup Pin Enable For LLWU_P18 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
3–2 WUPE17	Wakeup Pin Enable For LLWU_P17 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
WUPE16	Wakeup Pin Enable For LLWU_P16 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection

19.4.6 LLWU Pin Enable 6 register (LLWU_PE6)

LLWU_PE6 contains the field to enable and select the edge detect type for the external wakeup input pins LLWU_P23-LLWU_P20.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + 5h offset = 4007_C005h

Bit	7	6	5	4	3	2	1	0
Read Write	WUPE23		WUPE22		WUPE21		WUPE20	
Reset	0	0	0	0	0	0	0	0

LLWU_PE6 field descriptions

Field	Description
7–6 WUPE23	Wakeup Pin Enable For LLWU_P23 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
5–4 WUPE22	Wakeup Pin Enable For LLWU_P22 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
3–2 WUPE21	Wakeup Pin Enable For LLWU_P21 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
WUPE20	Wakeup Pin Enable For LLWU_P20 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection

Table continues on the next page...

LLWU_PE6 field descriptions (continued)

Field	Description
	10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection

19.4.7 LLWU Pin Enable 7 register (LLWU_PE7)

LLWU_PE7 contains the field to enable and select the edge detect type for the external wakeup input pins LLWU_P27-LLWU_P24.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + 6h offset = 4007_C006h

Bit	7	6	5	4	3	2	1	0
Read Write	WUPE27		WUPE26		WUPE25		WUPE24	
Reset	0	0	0	0	0	0	0	0

LLWU_PE7 field descriptions

Field	Description
7–6 WUPE27	Wakeup Pin Enable For LLWU_P27 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
5–4 WUPE26	Wakeup Pin Enable For LLWU_P26 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
3–2 WUPE25	Wakeup Pin Enable For LLWU_P25 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection

Table continues on the next page...

LLWU_PE7 field descriptions (continued)

Field	Description
	10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
WUPE24	Wakeup Pin Enable For LLWU_P24 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection

19.4.8 LLWU Pin Enable 8 register (LLWU_PE8)

LLWU_PE8 contains the field to enable and select the edge detect type for the external wakeup input pins LLWU_P31-LLWU_P28.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + 7h offset = 4007_C007h

Bit	7	6	5	4	3	2	1	0
Read Write	WUPE31		WUPE30		WUPE29		WUPE28	
Reset	0	0	0	0	0	0	0	0

LLWU_PE8 field descriptions

Field	Description
7–6 WUPE31	Wakeup Pin Enable For LLWU_P31 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
5–4 WUPE30	Wakeup Pin Enable For LLWU_P30 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection

Table continues on the next page...

LLWU_PE8 field descriptions (continued)

Field	Description
	10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
3–2 WUPE29	Wakeup Pin Enable For LLWU_P29 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection
WUPE28	Wakeup Pin Enable For LLWU_P28 Enables and configures the edge detection for the wakeup pin. 00 External input pin disabled as wakeup input 01 External input pin enabled with rising edge detection 10 External input pin enabled with falling edge detection 11 External input pin enabled with any change detection

19.4.9 LLWU Module Enable register (LLWU_ME)

LLWU_ME contains the bits to enable the internal module flag as a wakeup input source for inputs MWUF7-MWUF0.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + 8h offset = 4007_C008h

Bit	7	6	5	4	3	2	1	0
Read Write	WUME7	WUME6	WUME5	WUME4	WUME3	WUME2	WUME1	WUME0
Reset	0	0	0	0	0	0	0	0

LLWU_ME field descriptions

Field	Description
7 WUME7	Wakeup Module Enable For Module 7 Enables an internal module as a wakeup source input. 0 Internal module flag not used as wakeup source 1 Internal module flag used as wakeup source

Table continues on the next page...

LLWU_ME field descriptions (continued)

Field	Description
6 WUME6	Wakeup Module Enable For Module 6 Enables an internal module as a wakeup source input. 0 Internal module flag not used as wakeup source 1 Internal module flag used as wakeup source
5 WUME5	Wakeup Module Enable For Module 5 Enables an internal module as a wakeup source input. 0 Internal module flag not used as wakeup source 1 Internal module flag used as wakeup source
4 WUME4	Wakeup Module Enable For Module 4 Enables an internal module as a wakeup source input. 0 Internal module flag not used as wakeup source 1 Internal module flag used as wakeup source
3 WUME3	Wakeup Module Enable For Module 3 Enables an internal module as a wakeup source input. 0 Internal module flag not used as wakeup source 1 Internal module flag used as wakeup source
2 WUME2	Wakeup Module Enable For Module 2 Enables an internal module as a wakeup source input. 0 Internal module flag not used as wakeup source 1 Internal module flag used as wakeup source
1 WUME1	Wakeup Module Enable for Module 1 Enables an internal module as a wakeup source input. 0 Internal module flag not used as wakeup source 1 Internal module flag used as wakeup source
0 WUME0	Wakeup Module Enable For Module 0 Enables an internal module as a wakeup source input. 0 Internal module flag not used as wakeup source 1 Internal module flag used as wakeup source

19.4.10 LLWU Pin Flag 1 register (LLWU_PF1)

LLWU_PF1 contains the wakeup flags indicating which wakeup source caused the MCU to exit LLS or VLLS mode. For LLS, this is the source causing the CPU interrupt flow. For VLLS, this is the source causing the MCU reset flow.

The external wakeup flags are read-only and clearing a flag is accomplished by a write of a 1 to the corresponding WUFx bit. The wakeup flag (WUFx), if set, will remain set if the associated WUPEx bit is cleared.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + 9h offset = 4007_C009h

Bit	7	6	5	4	3	2	1	0
Read	WUF7	WUF6	WUF5	WUF4	WUF3	WUF2	WUF1	WUF0
Write	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

LLWU_PF1 field descriptions

Field	Description
7 WUF7	Wakeup Flag For LLWU_P7 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF7. 0 LLWU_P7 input was not a wakeup source 1 LLWU_P7 input was a wakeup source
6 WUF6	Wakeup Flag For LLWU_P6 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF6. 0 LLWU_P6 input was not a wakeup source 1 LLWU_P6 input was a wakeup source
5 WUF5	Wakeup Flag For LLWU_P5 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF5. 0 LLWU_P5 input was not a wakeup source 1 LLWU_P5 input was a wakeup source
4 WUF4	Wakeup Flag For LLWU_P4 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF4. 0 LLWU_P4 input was not a wakeup source 1 LLWU_P4 input was a wakeup source
3 WUF3	Wakeup Flag For LLWU_P3 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF3.

Table continues on the next page...

LLWU_PF1 field descriptions (continued)

Field	Description
	0 LLWU_P3 input was not a wakeup source 1 LLWU_P3 input was a wakeup source
2 WUF2	Wakeup Flag For LLWU_P2 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF2. 0 LLWU_P2 input was not a wakeup source 1 LLWU_P2 input was a wakeup source
1 WUF1	Wakeup Flag For LLWU_P1 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF1. 0 LLWU_P1 input was not a wakeup source 1 LLWU_P1 input was a wakeup source
0 WUF0	Wakeup Flag For LLWU_P0 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF0. 0 LLWU_P0 input was not a wakeup source 1 LLWU_P0 input was a wakeup source

19.4.11 LLWU Pin Flag 2 register (LLWU_PF2)

LLWU_PF2 contains the wakeup flags indicating which wakeup source caused the MCU to exit LLS or VLLS mode. For LLS, this is the source causing the CPU interrupt flow. For VLLS, this is the source causing the MCU reset flow.

The external wakeup flags are read-only and clearing a flag is accomplished by a write of a 1 to the corresponding WUFx bit. The wakeup flag (WUFx), if set, will remain set if the associated WUPEx bit is cleared.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + Ah offset = 4007_C00Ah

Bit	7	6	5	4	3	2	1	0
Read	WUF15	WUF14	WUF13	WUF12	WUF11	WUF10	WUF9	WUF8
Write	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

LLWU_PF2 field descriptions

Field	Description
7 WUF15	Wakeup Flag For LLWU_P15 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF15. 0 LLWU_P15 input was not a wakeup source 1 LLWU_P15 input was a wakeup source
6 WUF14	Wakeup Flag For LLWU_P14 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF14. 0 LLWU_P14 input was not a wakeup source 1 LLWU_P14 input was a wakeup source
5 WUF13	Wakeup Flag For LLWU_P13 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF13. 0 LLWU_P13 input was not a wakeup source 1 LLWU_P13 input was a wakeup source
4 WUF12	Wakeup Flag For LLWU_P12 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF12. 0 LLWU_P12 input was not a wakeup source 1 LLWU_P12 input was a wakeup source
3 WUF11	Wakeup Flag For LLWU_P11 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF11. 0 LLWU_P11 input was not a wakeup source 1 LLWU_P11 input was a wakeup source
2 WUF10	Wakeup Flag For LLWU_P10 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF10. 0 LLWU_P10 input was not a wakeup source 1 LLWU_P10 input was a wakeup source
1 WUF9	Wakeup Flag For LLWU_P9 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF9. 0 LLWU_P9 input was not a wakeup source 1 LLWU_P9 input was a wakeup source
0 WUF8	Wakeup Flag For LLWU_P8

Table continues on the next page...

LLWU_PF2 field descriptions (continued)

Field	Description
	Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF8. 0 LLWU_P8 input was not a wakeup source 1 LLWU_P8 input was a wakeup source

19.4.12 LLWU Pin Flag 3 register (LLWU_PF3)

LLWU_PF3 contains the wakeup flags indicating which wakeup source caused the MCU to exit LLS or VLLS mode. For LLS, this is the source causing the CPU interrupt flow. For VLLS, this is the source causing the MCU reset flow.

The external wakeup flags are read-only and clearing a flag is accomplished by a write of a 1 to the corresponding WUFx bit. The wakeup flag (WUFx), if set, will remain set if the associated WUPEx bit is cleared.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + Bh offset = 4007_C00Bh

Bit	7	6	5	4	3	2	1	0
Read	WUF23	WUF22	WUF21	WUF20	WUF19	WUF18	WUF17	WUF16
Write	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

LLWU_PF3 field descriptions

Field	Description
7 WUF23	Wakeup Flag For LLWU_P23 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF23. 0 LLWU_P23 input was not a wakeup source 1 LLWU_P23 input was a wakeup source
6 WUF22	Wakeup Flag For LLWU_P22 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF22.

Table continues on the next page...

LLWU_PF3 field descriptions (continued)

Field	Description
	0 LLWU_P22 input was not a wakeup source 1 LLWU_P22 input was a wakeup source
5 WUF21	Wakeup Flag For LLWU_P21 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF21. 0 LLWU_P21 input was not a wakeup source 1 LLWU_P21 input was a wakeup source
4 WUF20	Wakeup Flag For LLWU_P20 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF20. 0 LLWU_P20 input was not a wakeup source 1 LLWU_P20 input was a wakeup source
3 WUF19	Wakeup Flag For LLWU_P19 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF19. 0 LLWU_P19 input was not a wakeup source 1 LLWU_P19 input was a wakeup source
2 WUF18	Wakeup Flag For LLWU_P18 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF18. 0 LLWU_P18 input was not a wakeup source 1 LLWU_P18 input was a wakeup source
1 WUF17	Wakeup Flag For LLWU_P17 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF17. 0 LLWU_P17 input was not a wakeup source 1 LLWU_P17 input was a wakeup source
0 WUF16	Wakeup Flag For LLWU_P16 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF16. 0 LLWU_P16 input was not a wakeup source 1 LLWU_P16 input was a wakeup source

19.4.13 LLWU Pin Flag 4 register (LLWU_PF4)

LLWU_PF4 contains the wakeup flags indicating which wakeup source caused the MCU to exit LLS or VLLS mode. For LLS, this is the source causing the CPU interrupt flow. For VLLS, this is the source causing the MCU reset flow.

The external wakeup flags are read-only and clearing a flag is accomplished by a write of a 1 to the corresponding WUFx bit. The wakeup flag (WUFx), if set, will remain set if the associated WUPEx bit is cleared.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + Ch offset = 4007_C00Ch

Bit	7	6	5	4	3	2	1	0
Read	WUF31	WUF30	WUF29	WUF28	WUF27	WUF26	WUF25	WUF24
Write	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

LLWU_PF4 field descriptions

Field	Description
7 WUF31	Wakeup Flag For LLWU_P31 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF31. 0 LLWU_P31 input was not a wakeup source 1 LLWU_P31 input was a wakeup source
6 WUF30	Wakeup Flag For LLWU_P30 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF30. 0 LLWU_P30 input was not a wakeup source 1 LLWU_P30 input was a wakeup source
5 WUF29	Wakeup Flag For LLWU_P29 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF29. 0 LLWU_P29 input was not a wakeup source 1 LLWU_P29 input was a wakeup source

Table continues on the next page...

LLWU_PF4 field descriptions (continued)

Field	Description
4 WUF28	Wakeup Flag For LLWU_P28 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF28. 0 LLWU_P28 input was not a wakeup source 1 LLWU_P28 input was a wakeup source
3 WUF27	Wakeup Flag For LLWU_P27 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF27. 0 LLWU_P27 input was not a wakeup source 1 LLWU_P27 input was a wakeup source
2 WUF26	Wakeup Flag For LLWU_P26 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF26. 0 LLWU_P26 input was not a wakeup source 1 LLWU_P26 input was a wakeup source
1 WUF25	Wakeup Flag For LLWU_P25 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF25. 0 LLWU_P25 input was not a wakeup source 1 LLWU_P25 input was a wakeup source
0 WUF24	Wakeup Flag For LLWU_P24 Indicates that an enabled external wakeup pin was a source of exiting a low-leakage power mode. To clear the flag write a one to WUF24. 0 LLWU_P24 input was not a wakeup source 1 LLWU_P24 input was a wakeup source

19.4.14 LLWU Module Flag 5 register (LLWU_MF5)

LLWU_MF5 contains the wakeup flags indicating which internal wakeup source caused the MCU to exit LLS or VLLS mode. For LLS, this is the source causing the CPU interrupt flow. For VLLS, this is the source causing the MCU reset flow.

For internal peripherals that are capable of running in a low-leakage power mode, such as a real time clock module or CMP module, the flag from the associated peripheral is accessible as the MWUFx bit. The flag will need to be cleared in the peripheral instead of writing a 1 to the MWUFx bit.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + Dh offset = 4007_C00Dh

Bit	7	6	5	4	3	2	1	0
Read	MWUF7	MWUF6	MWUF5	MWUF4	MWUF3	MWUF2	MWUF1	MWUF0
Write								
Reset	0	0	0	0	0	0	0	0

LLWU_MF5 field descriptions

Field	Description
7 MWUF7	Wakeup flag For module 7 Indicates that an enabled internal peripheral was a source of exiting a low-leakage power mode. To clear the flag, follow the internal peripheral flag clearing mechanism. 0 Module 7 input was not a wakeup source 1 Module 7 input was a wakeup source
6 MWUF6	Wakeup flag For module 6 Indicates that an enabled internal peripheral was a source of exiting a low-leakage power mode. To clear the flag, follow the internal peripheral flag clearing mechanism. 0 Module 6 input was not a wakeup source 1 Module 6 input was a wakeup source
5 MWUF5	Wakeup flag For module 5 Indicates that an enabled internal peripheral was a source of exiting a low-leakage power mode. To clear the flag, follow the internal peripheral flag clearing mechanism. 0 Module 5 input was not a wakeup source 1 Module 5 input was a wakeup source
4 MWUF4	Wakeup flag For module 4 Indicates that an enabled internal peripheral was a source of exiting a low-leakage power mode. To clear the flag, follow the internal peripheral flag clearing mechanism. 0 Module 4 input was not a wakeup source 1 Module 4 input was a wakeup source
3 MWUF3	Wakeup flag For module 3 Indicates that an enabled internal peripheral was a source of exiting a low-leakage power mode. To clear the flag, follow the internal peripheral flag clearing mechanism. 0 Module 3 input was not a wakeup source 1 Module 3 input was a wakeup source
2 MWUF2	Wakeup flag For module 2

Table continues on the next page...

LLWU_MF5 field descriptions (continued)

Field	Description
	Indicates that an enabled internal peripheral was a source of exiting a low-leakage power mode. To clear the flag, follow the internal peripheral flag clearing mechanism. 0 Module 2 input was not a wakeup source 1 Module 2 input was a wakeup source
1 MWUF1	Wakeup flag For module 1 Indicates that an enabled internal peripheral was a source of exiting a low-leakage power mode. To clear the flag, follow the internal peripheral flag clearing mechanism. 0 Module 1 input was not a wakeup source 1 Module 1 input was a wakeup source
0 MWUF0	Wakeup flag For module 0 Indicates that an enabled internal peripheral was a source of exiting a low-leakage power mode. To clear the flag, follow the internal peripheral flag clearing mechanism. 0 Module 0 input was not a wakeup source 1 Module 0 input was a wakeup source

19.4.15 LLWU Pin Filter 1 register (LLWU_FILT1)

LLWU_FILT1 is a control and status register that is used to enable/disable the digital filter 1 features for an external pin.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + Eh offset = 4007_C00Eh

Bit	7	6	5	4	3	2	1	0
Read	FILTF	FILTE			FILTSEL			
Write	w1c							
Reset	0	0	0	0	0	0	0	0

LLWU_FILT1 field descriptions

Field	Description
7 FILTF	Filter Detect Flag Indicates that the filtered external wakeup pin, selected by FILTSEL, was a source of exiting a low-leakage power mode. To clear the flag write a one to FILTF.

Table continues on the next page...

LLWU_FILT1 field descriptions (continued)

Field	Description
	0 Pin Filter 1 was not a wakeup source 1 Pin Filter 1 was a wakeup source
6–5 FILTE	Digital Filter On External Pin Controls the digital filter options for the external pin detect. 00 Filter disabled 01 Filter posedge detect enabled 10 Filter negedge detect enabled 11 Filter any edge detect enabled
FILTSEL	Filter Pin Select Selects 1 of the wakeup pins to be muxed into the filter. 00000 Select LLWU_P0 for filter ... ... 11111 Select LLWU_P31 for filter

19.4.16 LLWU Pin Filter 2 register (LLWU_FILT2)

LLWU_FILT2 is a control and status register that is used to enable/disable the digital filter 2 features for an external pin.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + Fh offset = 4007_C00Fh

Bit	7	6	5	4	3	2	1	0
Read	FILTF	FILTE			FILTSEL			
Write	w1c							
Reset	0	0	0	0	0	0	0	0

LLWU_FILT2 field descriptions

Field	Description
7 FILTF	Filter Detect Flag Indicates that the filtered external wakeup pin, selected by FILTSEL, was a source of exiting a low-leakage power mode. To clear the flag write a one to FILTF. 0 Pin Filter 2 was not a wakeup source 1 Pin Filter 2 was a wakeup source

Table continues on the next page...

LLWU_FILT2 field descriptions (continued)

Field	Description
6–5 FILTE	Digital Filter On External Pin Controls the digital filter options for the external pin detect. 00 Filter disabled 01 Filter posedge detect enabled 10 Filter negedge detect enabled 11 Filter any edge detect enabled
FILTSEL	Filter Pin Select Selects 1 of the wakeup pins to be muxed into the filter. 00000 Select LLWU_P0 for filter ... ... 11111 Select LLWU_P31 for filter

19.4.17 LLWU Pin Filter 3 register (LLWU_FILT3)

LLWU_FILT3 is a control and status register that is used to enable/disable the digital filter 3 features for an external pin.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + 10h offset = 4007_C010h

Bit	7	6	5	4	3	2	1	0
Read	FILTF	FILTE			FILTSEL			
Write	w1c							
Reset	0	0	0	0	0	0	0	0

LLWU_FILT3 field descriptions

Field	Description
7 FILTF	Filter Detect Flag Indicates that the filtered external wakeup pin, selected by FILTSEL, was a source of exiting a low-leakage power mode. To clear the flag write a one to FILTF. 0 Pin Filter 3 was not a wakeup source 1 Pin Filter 3 was a wakeup source
6–5 FILTE	Digital Filter On External Pin

Table continues on the next page...

LLWU_FILT3 field descriptions (continued)

Field	Description
	Controls the digital filter options for the external pin detect. 00 Filter disabled 01 Filter posedge detect enabled 10 Filter negedge detect enabled 11 Filter any edge detect enabled
FILTSEL	Filter Pin Select Selects 1 of the wakeup pins to be muxed into the filter. 00000 Select LLWU_P0 for filter ... ... 11111 Select LLWU_P31 for filter

19.4.18 LLWU Pin Filter 4 register (LLWU_FILT4)

LLWU_FILT4 is a control and status register that is used to enable/disable the digital filter 4 features for an external pin.

NOTE

This register is reset on Chip Reset not VLLS and by reset types that trigger Chip Reset not VLLS. It is unaffected by reset types that do not trigger Chip Reset not VLLS. See the Introduction details for more information.

Address: 4007_C000h base + 11h offset = 4007_C011h

Bit	7	6	5	4	3	2	1	0
Read	FILTF	FILTE			FILTSEL			
Write	w1c							
Reset	0	0	0	0	0	0	0	0

LLWU_FILT4 field descriptions

Field	Description
7 FILTF	Filter Detect Flag Indicates that the filtered external wakeup pin, selected by FILTSEL, was a source of exiting a low-leakage power mode. To clear the flag write a one to FILTF. 0 Pin Filter 4 was not a wakeup source 1 Pin Filter 4 was a wakeup source
6–5 FILTE	Digital Filter On External Pin Controls the digital filter options for the external pin detect.

Table continues on the next page...

LLWU_FILT4 field descriptions (continued)

Field	Description
	00 Filter disabled 01 Filter posedge detect enabled 10 Filter negedge detect enabled 11 Filter any edge detect enabled
FILTSEL	Filter Pin Select Selects 1 of the wakeup pins to be muxed into the filter. 00000 Select LLWU_P0 for filter ... ... 11111 Select LLWU_P31 for filter

19.5 Functional description

Thie low-leakage wakeup unit (LLWU) module allows internal peripherals and external input pins as a source of wakeup from low-leakage modes.

It is operational only in LLS and VLLSx modes.

The LLWU module contains pin enables for each external pin and internal module. For each external pin, the user can disable or select the edge type for the wakeup with the following options:

- Falling-edge
- Rising-edge
- Either-edge

When an external pin is enabled as a wakeup source, the pin must be configured as an input pin.

The LLWU implements optional 3-cycle glitch filters, based on the LPO clock. A detected external pin is required to remain asserted until the enabled glitch filter times out. Additional latency of up to 2 cycles is due to synchronization, which results in a total of up to 5 cycles of delay before the detect circuit alerts the system to the wakeup or reset event when the filter function is enabled. wakeup detect filters are available for selected external pins. Glitch filtering is not provided on the internal modules.

For internal module interrupts, the WUMEx bit enables the associated module interrupt as a wakeup source.

19.5.1 LLS mode

Wakeup events triggered from either an external pin input or an internal module interrupt, result in a CPU interrupt flow to begin user code execution.

19.5.2 VLLS modes

For any wakeup from VLLS, recovery is always via a reset flow and RCM_SRS[WAKEUP] is set indicating the low-leakage mode was active. State retention data is lost and I/O will be restored after PMC_REGSC[ACKISO] has been written.

A VLLS exit event due to $\overline{\text{RESET}}$ pin assertion causes an exit via a system reset. State retention data is lost and the I/O states immediately return to their reset state. The RCM_SRS[WAKEUP] and RCM_SRS[PIN] bits are set and the system executes a reset flow before CPU operation begins with a reset vector fetch.

19.5.3 Initialization

For an enabled peripheral wakeup input, the peripheral flag must be cleared by software before entering LLS or VLLSx mode to avoid an immediate exit from the mode.

Flags associated with external input pins, filtered and unfiltered, must also be cleared by software prior to entry to LLS or VLLSx mode.

After enabling an external pin filter or changing the source pin, wait at least five LPO clock cycles before entering LLS or VLLSx mode to allow the filter to initialize.

NOTE

After recovering from a VLLS mode, user must restore chip configuration before clearing PMC_REGSC[ACKISO]. In particular, pin configuration for enabled LLWU wake-up pins must be restored to avoid any LLWU flag from being falsely set when PMC_REGSC[ACKISO] is cleared.

The signal selected as a wake-up source pin must be a digital pin, as selected in the pin mux control.

Chapter 20
Miscellaneous Control Module (MCM)

20.1 Introduction

The Miscellaneous Control Module (MCM) provides a myriad of miscellaneous control functions.

20.1.1 Features

The MCM includes the following features:

- Program-visible information on the platform configuration and revision
- Floating Point Exception monitor and interrupt control
- AHBS WABORTS (imprecise write fault) monitor and interrupt control

20.2 Memory map/register descriptions

The memory map and register descriptions below describe the registers using byte addresses.

MCM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
E008_0008	Crossbar Switch (AXBS) Slave Configuration (MCM_PLASC)	16	R	003Fh	20.2.1/436
E008_000A	Crossbar Switch (AXBS) Master Configuration (MCM_PLAMC)	16	R	001Fh	20.2.2/437
E008_000C	Control Register (MCM_CR)	32	R/W	0000_0000h	20.2.3/438
E008_0010	Interrupt Status Register (MCM_ISCR)	32	R	0000_0000h	20.2.4/440
E008_0020	Fault address register (MCM_FADR)	32	R	Undefined	20.2.5/442

Table continues on the next page...

MCM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
E008_0024	Fault attributes register (MCM_FATR)	32	R	Undefined	20.2.6/443
E008_0028	Fault data register (MCM_FDR)	32	R	Undefined	20.2.7/445
E008_0030	Process ID register (MCM_PID)	32	R/W	0000_0000h	20.2.8/446
E008_0040	Compute Operation Control Register (MCM_CPO)	32	R/W	0000_0000h	20.2.9/447

20.2.1 Crossbar Switch (AXBS) Slave Configuration (MCM_PLASC)

PLASC is a 16-bit read-only register identifying the presence/absence of bus slave connections to the device's crossbar switch.

Address: E008_0000h base + 8h offset = E008_0008h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0								ASC							
Write																
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

MCM_PLASC field descriptions

Field	Description
15–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
ASC	Each bit in the ASC field indicates whether there is a corresponding connection to the crossbar switch's slave input port. 0 A bus slave connection to AXBS input port *n* is absent 1 A bus slave connection to AXBS input port *n* is present

20.2.2 Crossbar Switch (AXBS) Master Configuration (MCM_PLAMC)

PLAMC is a 16-bit read-only register identifying the presence/absence of bus master connections to the device's crossbar switch.

Address: E008_0000h base + Ah offset = E008_000Ah

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0								AMC							
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

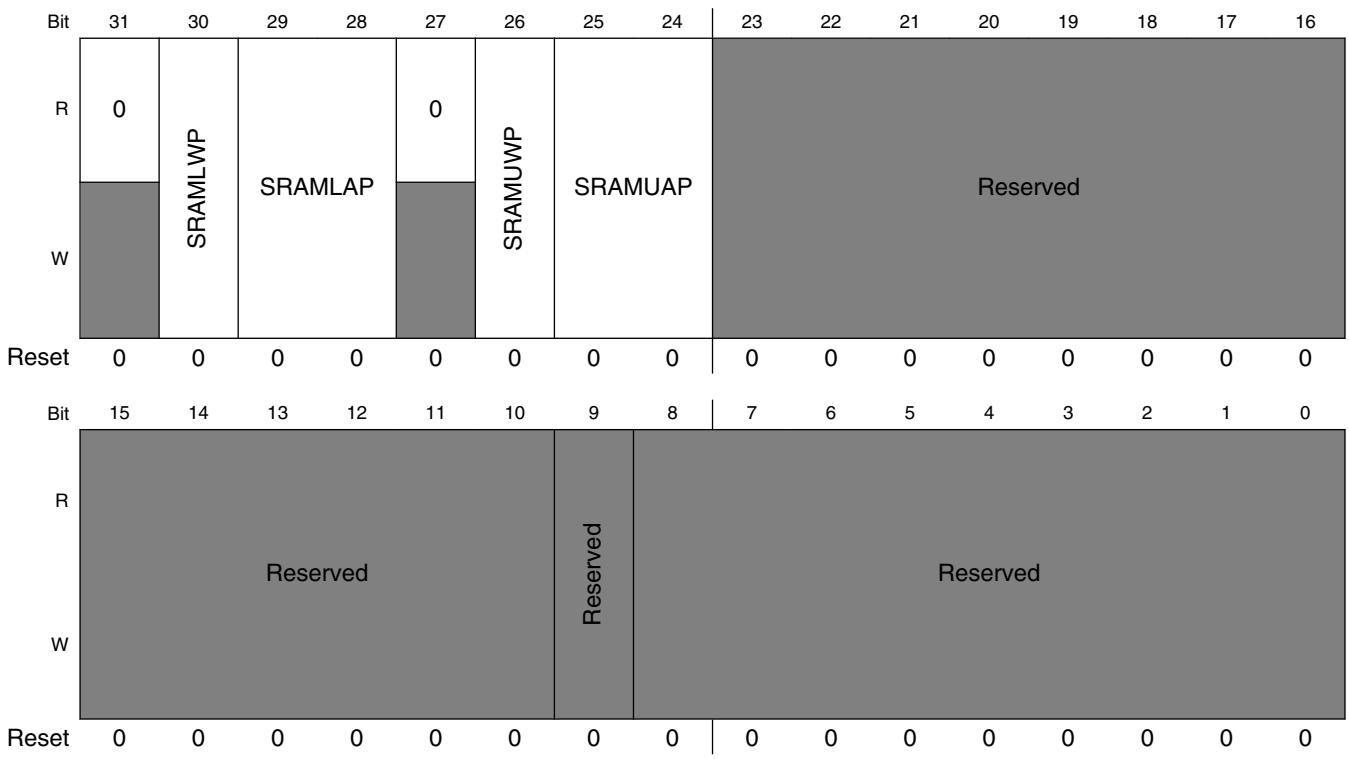
MCM_PLAMC field descriptions

Field	Description
15–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
AMC	Each bit in the AMC field indicates whether there is a corresponding connection to the AXBS master input port. 0 A bus master connection to AXBS input port *n* is absent 1 A bus master connection to AXBS input port *n* is present

20.2.3 Control Register (MCM_CR)

CR defines the arbitration and protection schemes for the two system RAM arrays.

Address: E008_0000h base + Ch offset = E008_000Ch



MCM_CR field descriptions

Field	Description
31 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
30 SRAMLWP	SRAM_L Write Protect When this bit is set, writes to SRAM_L array generates a bus error.
29–28 SRAMLAP	SRAM_L arbitration priority Defines the arbitration scheme and priority for the processor and SRAM backdoor accesses to the SRAM_L array. 00 Round robin 01 Special round robin (favors SRAM backoor accesses over the processor) 10 Fixed priority. Processor has highest, backdoor has lowest 11 Fixed priority. Backdoor has highest, processor has lowest
27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

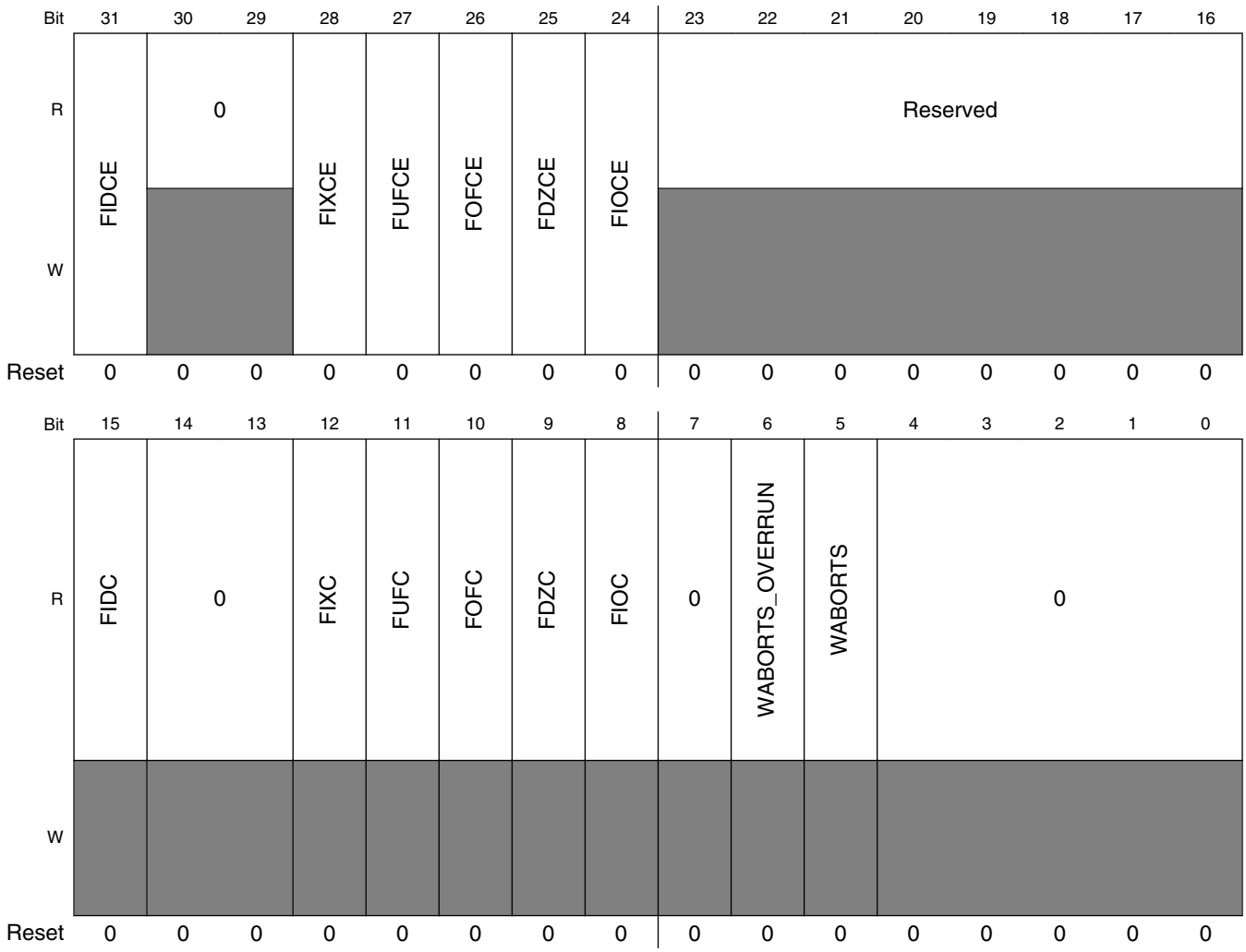
Table continues on the next page...

MCM_CR field descriptions (continued)

Field	Description
26 SRAMUWP	SRAM_U write protect When this bit is set, writes to SRAM_U array generates a bus error.
25–24 SRAMUAP	SRAM_U arbitration priority Defines the arbitration scheme and priority for the processor and SRAM backdoor accesses to the SRAM_U array. 00 Round robin 01 Special round robin (favors SRAM backoor accesses over the processor) 10 Fixed priority. Processor has highest, backdoor has lowest 11 Fixed priority. Backdoor has highest, processor has lowest
23–10 Reserved	This field is reserved.
9 Reserved	This field is reserved.
Reserved	This field is reserved.

20.2.4 Interrupt Status Register (MCM_ISCR)

Address: E008_0000h base + 10h offset = E008_0010h



MCM_ISCR field descriptions

Field	Description
31 FIDCE	FPU input denormal interrupt enable 0 Disable interrupt 1 Enable interrupt
30–29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28 FIXCE	FPU inexact interrupt enable 0 Disable interrupt 1 Enable interrupt

Table continues on the next page...

MCM_ISCR field descriptions (continued)

Field	Description
27 FUFCE	FPU underflow interrupt enable 0 Disable interrupt 1 Enable interrupt
26 FOFCE	FPU overflow interrupt enable 0 Disable interrupt 1 Enable interrupt
25 FDZCE	FPU divide-by-zero interrupt enable 0 Disable interrupt 1 Enable interrupt
24 FIOCE	FPU invalid operation interrupt enable 0 Disable interrupt 1 Enable interrupt
23–16 Reserved	This field is reserved.
15 FIDC	FPU input denormal interrupt status This read-only bit is a copy of the core's FPSCR[IDC] bit and signals input denormalized number has been detected in the processor's FPU. Once set, this bit remains set until software clears the FPSCR[IDC] bit. 0 No interrupt 1 Interrupt occurred
14–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12 FIXC	FPU inexact interrupt status This read-only bit is a copy of the core's FPSCR[IXC] bit and signals an inexact number has been detected in the processor's FPU. Once set, this bit remains set until software clears the FPSCR[IXC] bit. 0 No interrupt 1 Interrupt occurred
11 FUFC	FPU underflow interrupt status This read-only bit is a copy of the core's FPSCR[UFC] bit and signals an underflow has been detected in the processor's FPU. Once set, this bit remains set until software clears the FPSCR[UFC] bit. 0 No interrupt 1 Interrupt occurred
10 FOFC	FPU overflow interrupt status This read-only bit is a copy of the core's FPSCR[OFC] bit and signals an overflow has been detected in the processor's FPU. Once set, this bit remains set until software clears the FPSCR[OFC] bit. 0 No interrupt 1 Interrupt occurred
9 FDZC	FPU divide-by-zero interrupt status

Table continues on the next page...

MCM_ISCR field descriptions (continued)

Field	Description
	This read-only bit is a copy of the core's FPSCR[DZC] bit and signals a divide by zero has been detected in the processor's FPU. Once set, this bit remains set until software clears the FPSCR[DZC] bit. 0 No interrupt 1 Interrupt occurred
8 FIOC	FPU invalid operation interrupt status This read-only bit is a copy of the core's FPSCR[IOC] bit and signals an illegal operation has been detected in the processor's FPU. Once set, this bit remains set until software clears the FPSCR[IOC] bit. 0 No interrupt 1 Interrupt occurred
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 WABORTS_ OVERRUN	WABORTS is an imprecise write fault from the TCM backdoor (AHBS, that is, AHB Slave Interface). The assertion of this field means that more than one WABORTS assertion has occurred. Writing 1 to ISCR[WABORTS] also clears this field. For more information, see ISCR[WABORTS_EN] and ISCR[WABORTS]. 0 One or less than one WABORTS assertion has occurred 1 More than 1 WABORTS assertion has occurred before clearing ISCR[WABORTS]
5 WABORTS	WABORTS is an imprecise write fault from the TCM backdoor (AHBS, that is, AHB Slave Interface). Writing 1 to clear this field also clears ISCR[WABORTS_OVERRUN]. If ISCR[WABORTS_EN] is set to 1, a WABORTS occurrence will generate an MCM interrupt. For more information, see ISCR[WABORTS_EN] and ISCR[WABORTS_OVERRUN]. 0 A WABORTS assertion has not occurred 1 A WABORTS assertion has occurred
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

20.2.5 Fault address register (MCM_FADR)

When a properly-enabled cache write buffer error interrupt event is detected, the faulting address is captured in the MCM_FADR register. The MCM logic supports capturing a single cache write buffer bus error event; if a subsequent error is detected before the captured error information has been read from the corresponding registers and the MCM_ISCR[CWBER] indicator cleared, the MCM_FATR[BEOVR] flag is set. However, no additional information is captured.

The bits in this register are set by hardware and signaled by the assertion of MCM_ISCR[CWBER]. Attempted writes have no effect.

Address: E008_0000h base + 20h offset = E008_0020h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ADDRESS																															
W																																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

MCM_FADR field descriptions

Field	Description
ADDRESS	Fault address

20.2.6 Fault attributes register (MCM_FATR)

When a properly-enabled cache write buffer error interrupt event is detected, the faulting attributes are captured in the MCM_FATR register.

The bits in this register are set by hardware and signaled by the assertion of MCM_ISCR[CWBER]. Attempted writes have no effect.

Address: E008_0000h base + 24h offset = E008_0024h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	BEOVR	0														
W																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				BEMN				BEWT	0	BESZ		0		BEMD	BEDA
W																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

MCM_FATR field descriptions

Field	Description
31 BEOVR	Bus error overrun Indicates if another cache write buffer bus error is detected before system software has retrieved all the error information from the original event, this overrun flag is set. The window of time is defined from the detection of the original cache write buffer error termination until the MCM_ISCR[CWBER] is written with a 1 to clear it and rearm the capture logic. This bit is set by the hardware and cleared whenever software writes a 1 to the CWBER bit. 0 No bus error overrun 1 Bus error overrun occurred. The FADR and FDR registers and the other FATR bits are not updated to reflect this new bus error.
30–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11–8 BEMN	Bus error master number Crossbar switch bus master number of the captured cache write buffer bus error. For this device, this value is always 0x1.
7 BEWT	Bus error write Indicates the type of system bus access when the error was detected. Since this logic is monitoring data transfers from the cache write buffer, this bit is always a logical one, signaling a write operation. 0 Read access 1 Write access
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5–4 BESZ	Bus error size Indicates the size of the cache write buffer access when the error was detected. 00 8-bit access 01 16-bit access

Table continues on the next page...

MCM_FATR field descriptions (continued)

Field	Description
	10 32-bit access 11 Reserved
3–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 BEMD	Bus error privilege level Indicates the privilege level of the cache write buffer access when the error was detected. 0 User mode 1 Supervisor/privileged mode
0 BEDA	Bus error access type Indicates the type of cache write buffer access when the error was detected. This attribute is always a logical one signaling a data reference. 0 Instruction 1 Data

20.2.7 Fault data register (MCM_FDR)

When a properly-enabled cache write buffer error interrupt event is detected, the faulting data is captured in the MCM_FDR register.

The bits in this register are set by hardware and signaled by the assertion of MCM_ISCR[CWBER]. For byte and halfword writes, only the accessed byte lanes contain valid data; the contents of the other bytes are undefined. Attempted writes have no effect.

Address: E008_0000h base + 28h offset = E008_0028h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DATA																															
W																																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

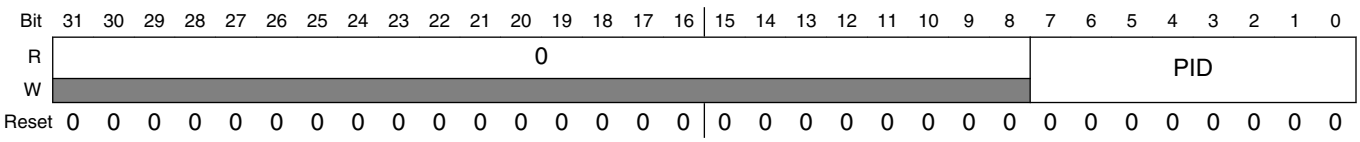
MCM_FDR field descriptions

Field	Description
DATA	Fault data

20.2.8 Process ID register (MCM_PID)

This register drives the M0_PID and M1_PID values in the Memory Protection Unit(MPU). System software loads this register before passing control to a given user mode process. If the PID of the process does not match the value in this register, a bus error occurs. See the MPU chapter for more details.

Address: E008_0000h base + 30h offset = E008_0030h



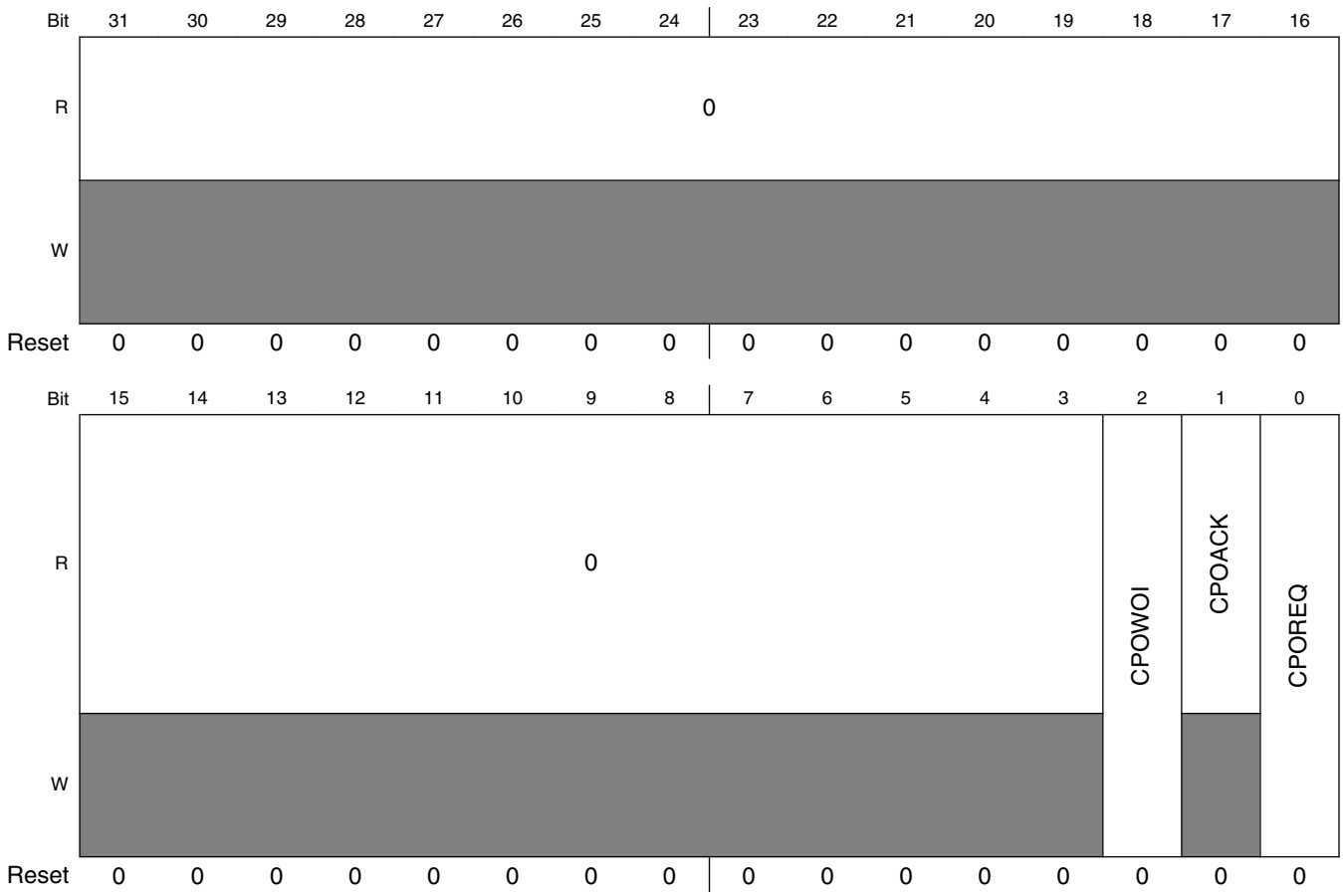
MCM_PID field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
PID	M0_PID And M1_PID For MPU Drives the M0_PID and M1_PID values in the MPU.

20.2.9 Compute Operation Control Register (MCM_CPO)

This register controls the Compute Operation.

Address: E008_0000h base + 40h offset = E008_0040h



MCM_CPO field descriptions

Field	Description
31–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 CPOWOI	Compute Operation wakeup on interrupt 0 No effect. 1 When set, the CPOREQ is cleared on any interrupt or exception vector fetch.
1 CPOACK	Compute Operation acknowledge 0 Compute operation entry has not completed or compute operation exit has completed. 1 Compute operation entry has completed or compute operation exit has not completed.
0 CPOREQ	Compute Operation request This bit is auto-cleared by vector fetching if CPOWOI = 1.

Table continues on the next page...

MCM_CPO field descriptions (continued)

Field	Description
	0 Request is cleared. 1 Request Compute Operation.

20.3 Functional description

This section describes the functional description of MCM module.

Chapter 21
Crossbar Switch (AXBS)

21.1 Chip-specific AXBS information

21.1.1 Crossbar Switch Master Assignments - with System MPU

The masters connected to the crossbar switch are assigned as follows:

Master port number	Master module	Default Priority
0	ARM core code bus	0
1	ARM core system bus	1
2	DMA	2
3	USB FS/LS OTG	3
4	SDHC	4
5	—	0
6	—	0
7	—	0

21.1.2 Crossbar Switch Slave Assignments - with System MPU

The slaves connected to the crossbar switch are assigned as follows:

Slave module	Slave port number	Protected by FSL MPU?
0	Flash memory controller / Boot ROM	Yes
1	SRAM backdoor	Yes
2	Peripheral bridge 0	No. Protection built into bridge.
3	Peripheral bridge 1 / GPIO1 / 2kB Secure SRAM	No. Protection built into bridge.

Table continues on the next page...

Slave module	Slave port number	Protected by FSL MPU?
4	FlexBus/SDRAM memory controller	Yes
5	QSPI	Yes
6	—	
7	—	

21.1.3 PRS register reset values

This device contains 5 bus AXBS masters.

The AXBS_PRS*n* registers reset to 0004_3210h

21.2 Introduction

The information found here provides information on the layout, configuration, and programming of the crossbar switch.

The crossbar switch connects bus masters and bus slaves using a crossbar switch structure. This structure allows all bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave. A variety of bus arbitration methods and attributes may be programmed on a slave-by-slave basis.

21.2.1 Features

The crossbar switch includes these features:

- Symmetric crossbar bus switch implementation
  - Allows concurrent accesses from different masters to different slaves
  - Slave arbitration attributes configured on a slave-by-slave basis
- Up to single-clock 32-bit transfer
- Support for burst transfers of up to 16 beats of data
- Low-Power Park mode support

21.3 Memory Map / Register Definition

Each slave port of the crossbar switch contains configuration registers. Read- and write-transfers require two bus clock cycles. The registers can be read from and written to only in supervisor mode. Additionally, these registers can be read from or written to only by 32-bit accesses.

A bus error response is returned if an unimplemented location is accessed within the crossbar switch.

The CRS*n* and PRS*n* registers can be programmed to be read-only to prevent changes to their configuration. After being read-only protected, future writes to them will terminate with an error.

NOTE

This section shows the registers for all eight master and slave ports. If a master or slave is not used on this particular device, then unexpected results occur when writing to its registers. See the chip configuration details for the exact master/slave assignments for your device.

All references to the crossbar switch registers are based on the physical port connections.

AXBS memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_4000	Priority Registers Slave (AXBS_PRS0)	32	R/W	See section	21.3.1/452
4000_4010	Control Register (AXBS_CRS0)	32	R/W	See section	21.3.2/454
4000_4100	Priority Registers Slave (AXBS_PRS1)	32	R/W	See section	21.3.1/452
4000_4110	Control Register (AXBS_CRS1)	32	R/W	See section	21.3.2/454
4000_4200	Priority Registers Slave (AXBS_PRS2)	32	R/W	See section	21.3.1/452
4000_4210	Control Register (AXBS_CRS2)	32	R/W	See section	21.3.2/454
4000_4300	Priority Registers Slave (AXBS_PRS3)	32	R/W	See section	21.3.1/452
4000_4310	Control Register (AXBS_CRS3)	32	R/W	See section	21.3.2/454
4000_4400	Priority Registers Slave (AXBS_PRS4)	32	R/W	See section	21.3.1/452
4000_4410	Control Register (AXBS_CRS4)	32	R/W	See section	21.3.2/454
4000_4500	Priority Registers Slave (AXBS_PRS5)	32	R/W	See section	21.3.1/452
4000_4510	Control Register (AXBS_CRS5)	32	R/W	See section	21.3.2/454
4000_4600	Priority Registers Slave (AXBS_PRS6)	32	R/W	See section	21.3.1/452

Table continues on the next page...

AXBS memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_4610	Control Register (AXBS_CRS6)	32	R/W	See section	21.3.2/454
4000_4700	Priority Registers Slave (AXBS_PRS7)	32	R/W	See section	21.3.1/452
4000_4710	Control Register (AXBS_CRS7)	32	R/W	See section	21.3.2/454
4000_4800	Master General Purpose Control Register (AXBS_MGPCR0)	32	R/W	0000_0000h	21.3.3/456
4000_4900	Master General Purpose Control Register (AXBS_MGPCR1)	32	R/W	0000_0000h	21.3.3/456
4000_4A00	Master General Purpose Control Register (AXBS_MGPCR2)	32	R/W	0000_0000h	21.3.3/456
4000_4B00	Master General Purpose Control Register (AXBS_MGPCR3)	32	R/W	0000_0000h	21.3.3/456
4000_4C00	Master General Purpose Control Register (AXBS_MGPCR4)	32	R/W	0000_0000h	21.3.3/456
4000_4D00	Master General Purpose Control Register (AXBS_MGPCR5)	32	R/W	0000_0000h	21.3.3/456
4000_4E00	Master General Purpose Control Register (AXBS_MGPCR6)	32	R/W	0000_0000h	21.3.3/456
4000_4F00	Master General Purpose Control Register (AXBS_MGPCR7)	32	R/W	0000_0000h	21.3.3/456

21.3.1 Priority Registers Slave (AXBS_PRS*n*)

The priority registers (PRSn) set the priority of each master port on a per slave port basis and reside in each slave port. The priority register can be accessed only with 32-bit accesses. After the CRSn[RO] bit is set, the PRSn register can only be read; attempts to write to it have no effect on PRSn and result in a bus-error response to the master initiating the write.

Two available masters must not be programmed with the same priority level. Attempts to program two or more masters with the same priority level result in a bus-error response and the PRSn is not updated.

NOTE

Valid values for the M*n* priority fields depend on which masters are available on the chip. This information can be found in the chip-specific information for the crossbar.

- If the chip contains less than five masters, values 0 to 3 are valid. Writing other values will result in an error.
- If the chip contains five or more masters, valid values are 0 to n-1, where n is the number of masters attached to the Crossbar Switch. Other values will result in an error.

NOTE

See the chip-specific crossbar information for the reset value of this register.

Address: 4000_4000h base + 0h offset + (256d × i), where i=0d to 7d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	Reserved			0	Reserved			0	Reserved			0	M4		
W		—				—				—						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0*	0*	0*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	M3			0	M2			0	M1			0	M0		
W																
Reset	0	0*	0*	0*	0	0*	0*	0*	0	0*	0*	0*	0	0*	0*	0*

* Notes:
- See the chip-specific crossbar information for the reset value of this register.

AXBS_PRS*n* field descriptions

Field	Description
31 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
30–28 Reserved	This field is reserved.
27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26–24 Reserved	This field is reserved.
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22–20 Reserved	This field is reserved.
19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18–16 M4	Master 4 Priority. Sets the arbitration priority for this port on the associated slave port. 000 This master has level 1, or highest, priority when accessing the slave port. 001 This master has level 2 priority when accessing the slave port. 010 This master has level 3 priority when accessing the slave port. 011 This master has level 4 priority when accessing the slave port. 100 This master has level 5 priority when accessing the slave port. 101 This master has level 6 priority when accessing the slave port. 110 This master has level 7 priority when accessing the slave port. 111 This master has level 8, or lowest, priority when accessing the slave port.
15 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
14–12 M3	Master 3 Priority. Sets the arbitration priority for this port on the associated slave port. 000 This master has level 1, or highest, priority when accessing the slave port. 001 This master has level 2 priority when accessing the slave port. 010 This master has level 3 priority when accessing the slave port. 011 This master has level 4 priority when accessing the slave port.

Table continues on the next page...

AXBS_PRS*n* field descriptions (continued)

Field	Description
	100 This master has level 5 priority when accessing the slave port. 101 This master has level 6 priority when accessing the slave port. 110 This master has level 7 priority when accessing the slave port. 111 This master has level 8, or lowest, priority when accessing the slave port.
11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10–8 M2	Master 2 Priority. Sets the arbitration priority for this port on the associated slave port. 000 This master has level 1, or highest, priority when accessing the slave port. 001 This master has level 2 priority when accessing the slave port. 010 This master has level 3 priority when accessing the slave port. 011 This master has level 4 priority when accessing the slave port. 100 This master has level 5 priority when accessing the slave port. 101 This master has level 6 priority when accessing the slave port. 110 This master has level 7 priority when accessing the slave port. 111 This master has level 8, or lowest, priority when accessing the slave port.
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6–4 M1	Master 1 Priority. Sets the arbitration priority for this port on the associated slave port. 000 This master has level 1, or highest, priority when accessing the slave port. 001 This master has level 2 priority when accessing the slave port. 010 This master has level 3 priority when accessing the slave port. 011 This master has level 4 priority when accessing the slave port. 100 This master has level 5 priority when accessing the slave port. 101 This master has level 6 priority when accessing the slave port. 110 This master has level 7 priority when accessing the slave port. 111 This master has level 8, or lowest, priority when accessing the slave port.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
M0	Master 0 Priority. Sets the arbitration priority for this port on the associated slave port. 000 This master has level 1, or highest, priority when accessing the slave port. 001 This master has level 2 priority when accessing the slave port. 010 This master has level 3 priority when accessing the slave port. 011 This master has level 4 priority when accessing the slave port. 100 This master has level 5 priority when accessing the slave port. 101 This master has level 6 priority when accessing the slave port. 110 This master has level 7 priority when accessing the slave port. 111 This master has level 8, or lowest, priority when accessing the slave port.

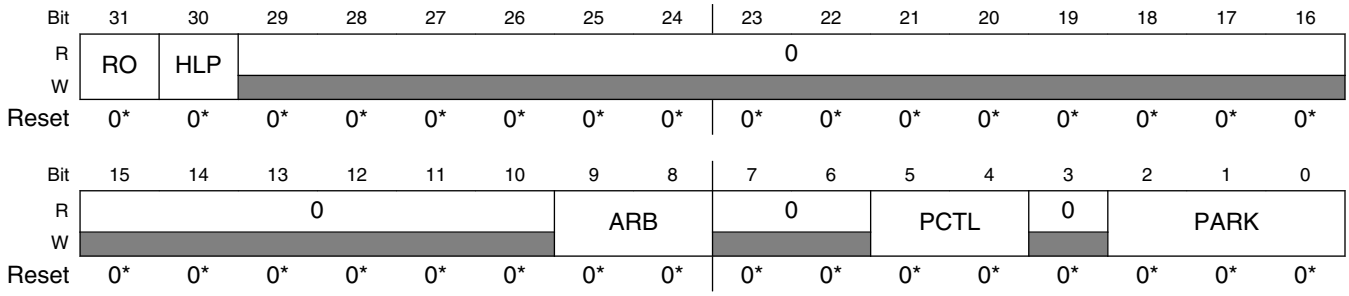
21.3.2 Control Register (AXBS_CRS*n*)

These registers control several features of each slave port and must be accessed using 32-bit accesses. After CRSn[RO] is set, the PRSn can only be read; attempts to write to it have no effect and result in an error response.

NOTE

See the chip-specific crossbar information for the reset value of this register.

Address: 4000_4000h base + 10h offset + (256d × i), where i=0d to 7d



* Notes:
- See the chip-specific crossbar information for the reset value of this register.

AXBS_CRS*n* field descriptions

Field	Description
31 RO	Read Only Forces the slave port's CSRn and PRSn registers to be read-only. After set, only a hardware reset clears it. 0 The slave port's registers are writeable 1 The slave port's registers are read-only and cannot be written. Attempted writes have no effect on the registers and result in a bus error response.
30 HLP	Halt Low Priority Sets the initial arbitration priority for low power mode requests . Setting this bit will not affect the request for low power mode from attaining highest priority once it has control of the slave ports. 0 The low power mode request has the highest priority for arbitration on this slave port 1 The low power mode request has the lowest initial priority for arbitration on this slave port
29–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9–8 ARB	Arbitration Mode Selects the arbitration policy for the slave port. 00 Fixed priority 01 Round-robin, or rotating, priority 10 Reserved 11 Reserved
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5–4 PCTL	Parking Control

Table continues on the next page...

AXBS_CRS*n* field descriptions (continued)

Field	Description
	Determines the slave port's parking control. The low-power park feature results in an overall power savings if the slave port is not saturated. However, this forces an extra latency clock when any master tries to access the slave port while not in use because it is not parked on any master. 00 When no master makes a request, the arbiter parks the slave port on the master port defined by the PARK field 01 When no master makes a request, the arbiter parks the slave port on the last master to be in control of the slave port 10 When no master makes a request, the slave port is not parked on a master and the arbiter drives all outputs to a constant safe state 11 Reserved
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
PARK	Park Determines which master port the current slave port parks on when no masters are actively making requests and the PCTL bits are cleared. **NOTE:** Select only master ports that are present on the chip. Otherwise, undefined behavior might occur. 000 Park on master port M0 001 Park on master port M1 010 Park on master port M2 011 Park on master port M3 100 Park on master port M4 101 Park on master port M5 110 Park on master port M6 111 Park on master port M7

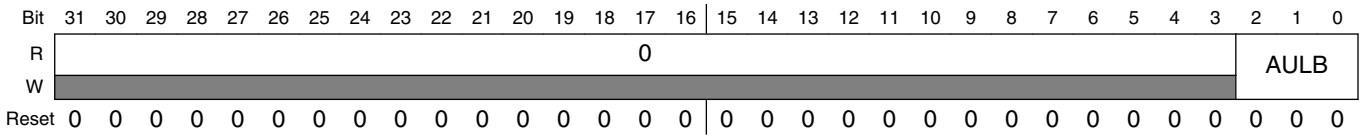
21.3.3 Master General Purpose Control Register (AXBS_MGPCR*n*)

The MGPCR controls only whether the master's undefined length burst accesses are allowed to complete uninterrupted or whether they can be broken by requests from higher priority masters. The MGPCR can be accessed only in Supervisor mode with 32-bit accesses.

NOTE

If there are fewer than eight master ports, only the registers associated with those masters are present. Register addresses associated with master ports that are not present are reserved. Please see this module's chip-specific information for which master ports are present on this module.

Address: 4000_4000h base + 800h offset + (256d × i), where i=0d to 7d



AXBS_MGPCR*n* field descriptions

Field	Description
31–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
AULB	Arbitrates On Undefined Length Bursts Determines whether, and when, the crossbar switch arbitrates away the slave port the master owns when the master is performing undefined length burst accesses. 000 No arbitration is allowed during an undefined length burst 001 Arbitration is allowed at any time during an undefined length burst 010 Arbitration is allowed after four beats of an undefined length burst 011 Arbitration is allowed after eight beats of an undefined length burst 100 Arbitration is allowed after 16 beats of an undefined length burst 101 Reserved 110 Reserved 111 Reserved

21.4 Functional Description

21.4.1 General operation

When a master accesses the crossbar switch, the access is immediately taken. If the targeted slave port of the access is available, then the access is immediately presented on the slave port. Single-clock or zero-wait-state accesses are possible through the crossbar. If the targeted slave port of the access is busy or parked on a different master port, the requesting master simply sees wait states inserted until the targeted slave port can service the master's request. The latency in servicing the request depends on each master's priority level and the responding slave's access time.

Because the crossbar switch appears to be just another slave to the master device, the master device has no knowledge of whether it actually owns the slave port it is targeting. While the master does not have control of the slave port it is targeting, it simply waits.

A master is given control of the targeted slave port only after a previous access to a different slave port completes, regardless of its priority on the newly targeted slave port. This prevents deadlock from occurring when:

- A higher priority master has:

- An outstanding request to one slave port that has a long response time and
- A pending access to a different slave port, and

- A lower priority master is also making a request to the same slave port as the pending access of the higher priority master.

After the master has control of the slave port it is targeting, the master remains in control of the slave port until it relinquishes the slave port by running an IDLE cycle or by targeting a different slave port for its next access.

The master can also lose control of the slave port if another higher-priority master makes a request to the slave port. However, if the master is running a fixed- or undefined-length burst transfer it retains control of the slave port until that transfer completes. Based on MGPCR[AULB], the master either retains control of the slave port when doing undefined-length, incrementing burst transfers or loses the bus to a higher-priority master.

The crossbar terminates all master IDLE transfers, as opposed to allowing the termination to come from one of the slave buses. Additionally, when no master is requesting access to a slave port, the crossbar drives IDLE transfers onto the slave bus, even though a default master may be granted access to the slave port.

When a slave bus is being idled by the crossbar, it can park the slave port on the master port indicated by CRS*n*[PARK] . This is done to save the initial clock of arbitration delay that otherwise would be seen if the same master had to arbitrate to gain control of the slave port. The slave port can also be put into Low Power Park mode to save power, by using CRS*n*[PCTL].

21.4.2 Register coherency

The operation of the crossbar is affected as soon as a register is written. The values of the registers do not track with slave-port-related master accesses, but instead track only with slave accesses.

The MGPCRx[AULB] bits are the exception to this rule. The update of these bits is only recognized when the master on that master port runs an IDLE cycle, even though the slave bus cycle to write them will have already terminated successfully. If the MGPCRx[AULB] bits are written between two burst accesses, the new AULB encodings do not take effect until an IDLE cycle is initiated by the master on that master port.

21.4.3 Arbitration

The crossbar switch supports two arbitration algorithms:

- Fixed priority
- Round-robin

The arbitration scheme is independently programmable for each slave port.

21.4.3.1 Arbitration during undefined length bursts

Arbitration points during an undefined length burst are defined by the current master's MGPCR[AULB] field setting. When a defined length is imposed on the burst via the AULB bits, the undefined length burst is treated as a single or series of single back-to-back fixed-length burst accesses.

The following figure illustrates an example:

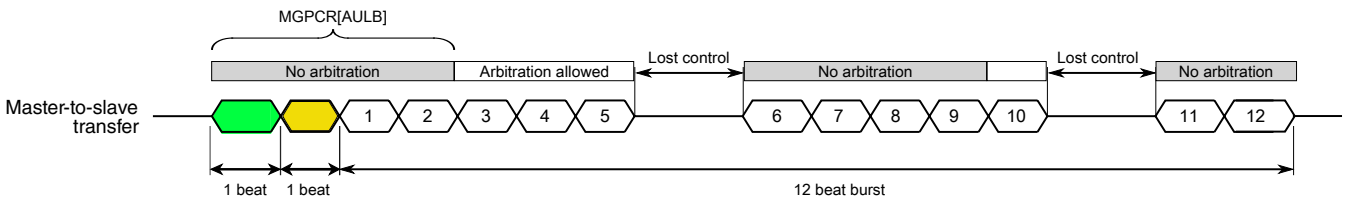


Figure 21-1. Undefined length burst example

In this example, a master runs an undefined length burst and the MGPCR[AULB] bits indicate arbitration occurs after the fourth beat of the burst. The master runs two sequential beats and then starts what will be a 12-beat undefined length burst access to a new address within the same slave port region as the previous access. The crossbar does not allow an arbitration point until the fourth overall access, or the second beat of the second burst. At that point, all remaining accesses are open for arbitration until the master loses control of the slave port.

Assume the master loses control of the slave port after the fifth beat of the second burst. After the master regains control of the slave port no arbitration point is available until after the master has run four more beats of its burst. After the fourth beat of the now continued burst, or the ninth beat of the second burst from the master's perspective, is taken, all beats of the burst are once again open for arbitration until the master loses control of the slave port.

Assume the master again loses control of the slave port on the fifth beat of the third now continued burst, or the 10th beat of the second burst from the master's perspective. After the master regains control of the slave port, it is allowed to complete its final two beats of its burst without facing arbitration.

Note

Fixed-length burst accesses are not affected by the AULB bits. All fixed-length burst accesses lock out arbitration until the last beat of the fixed-length burst.

21.4.3.2 Fixed-priority operation

When operating in fixed-priority mode, each master is assigned a unique priority level in the priority registers (PRS*n*). If two masters request access to the same slave port, the master with the highest priority in the selected priority register gains control over the slave port.

NOTE

In this arbitration mode, a higher-priority master can monopolize a slave port, preventing accesses from any lower-priority master to the port.

When a master makes a request to a slave port, the slave port checks whether the new requesting master's priority level is higher than that of the master that currently has control over the slave port, unless the slave port is in a parked state. The slave port performs an arbitration check at every clock edge to ensure that the proper master, if any, has control of the slave port.

The following table describes possible scenarios based on the requesting master port:

Table 21-1. How the Crossbar Switch grants control of a slave port to a master

When	Then the Crossbar Switch grants control to the requesting master
Both of the following are true: • The current master is not running a transfer. • The new requesting master's priority level is higher than that of the current master.	At the next clock edge
Both of the following are true: • The current master is running a fixed length burst transfer or a locked transfer. • The requesting master's priority level is higher than that of the current master.	At the end of the burst transfer or locked transfer
Both of the following are true: • The current master is running an undefined length burst transfer. • The requesting master's priority level is higher than that of the current master.	At the next arbitration point for the undefined length burst transfer **NOTE:** Arbitration points for an undefined length burst are defined in the MGPCR for each master.
The requesting master's priority level is lower than the current master.	At the conclusion of one of the following cycles: • An IDLE cycle • A non-IDLE cycle to a location other than the current slave port

21.4.3.3 Round-robin priority operation

When operating in round-robin mode, each master is assigned a relative priority based on the master port number. This relative priority is compared to the master port number (ID) of the last master to perform a transfer on the slave bus. The highest priority requesting master becomes owner of the slave bus at the next transfer boundary, accounting for locked and fixed-length burst transfers. Priority is based on how far ahead the ID of the requesting master is to the ID of the last master.

After granted access to a slave port, a master may perform as many transfers as desired to that port until another master makes a request to the same slave port. The next master in line is granted access to the slave port at the next transfer boundary, or possibly on the next clock cycle if the current master has no pending access request.

As an example of arbitration in round-robin mode, assume the crossbar is implemented with master ports 0, 1, 4, and 5. If the last master of the slave port was master 1, and master 0, 4, and 5 make simultaneous requests, they are serviced in the order: 4 then 5 then 0.

Parking may continue to be used in a round-robin mode, but does not affect the round-robin pointer unless the parked master actually performs a transfer. Handoff occurs to the next master in line after one cycle of arbitration. If the slave port is put into low-power park mode, the round-robin pointer is reset to point at master port 0, giving it the highest priority.

21.4.3.4 Priority assignment

Each master port must be assigned a unique 3-bit priority level. If an attempt is made to program multiple master ports with the same priority level within the priority registers (PRS*n*), the crossbar switch responds with a bus error and the registers are not updated.

21.5 Initialization/application information

No initialization is required for the crossbar switch.

Hardware reset ensures all the register bits used by the crossbar switch are properly initialized to a valid state. However, settings and priorities may be programmed to achieve maximum system performance.

Chapter 22
Peripheral Bridge (AIPS-Lite)

22.1 Chip-specific AIPS-Lite information

22.1.1 Number of peripheral bridges

This device contains two identical peripheral bridges.

22.1.2 Memory maps

The peripheral bridges are used to access the registers of most of the modules on this device. See AIPS0 Memory Map and AIPS1 Memory Map for the memory slot assignment for each module.

22.1.3 AIPS_Lite MPRA register reset value

- AIPS*x*_MPRA reset value is 0x7770_0000

Therefore, masters 0, 1, and 2 are trusted bus masters after reset.

22.1.4 AIPS_Lite PACRE-P register reset values

The AIPS*x*_PACRE-P reset values depend on if the module is available on your particular device. For each populated slot in slots 32-127 in Peripheral Bridge 0 (AIPS-Lite 0) Memory Map and Peripheral Bridge 1 (AIPS-Lite 1) Memory Map, the corresponding module's PACR[32:127] field resets to 0x4.

22.2 Introduction

The peripheral bridge converts the crossbar switch interface to an interface that can access most of the slave peripherals on this chip.

The peripheral bridge occupies 64 MB of the address space, which is divided into peripheral slots of 4 KB. (It might be possible that all the peripheral slots are not used. See the memory map chapter for details on slot assignments.) The bridge includes separate clock enable inputs for each of the slots to accommodate slower peripherals.

22.2.1 Features

Key features of the peripheral bridge are:

- Supports peripheral slots with 8-, 16-, and 32-bit datapath width
- Programming model provides memory protection functionality

22.2.2 General operation

The slave devices connected to the peripheral bridge are modules which contain a programming model of control and status registers. The system masters read and write these registers through the peripheral bridge.

The register maps of the peripherals are located on 4-KB boundaries. Each peripheral is allocated one or more 4-KB block(s) of the memory map.

22.3 Memory map/register definition

The 32-bit peripheral bridge registers can be accessed only in supervisor mode by trusted bus masters. Additionally, these registers must be read from or written to only by a 32-bit aligned access. The peripheral bridge registers are mapped into the Peripheral Access Control Register A PACRA[PACR0] address space.

AIPS memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_0000	Master Privilege Register A (AIPS0_MPRA)	32	R/W	See section	22.3.1/466
4000_0020	Peripheral Access Control Register (AIPS0_PACRA)	32	R/W	See section	22.3.2/469
4000_0024	Peripheral Access Control Register (AIPS0_PACRB)	32	R/W	See section	22.3.2/469
4000_0028	Peripheral Access Control Register (AIPS0_PACRC)	32	R/W	See section	22.3.2/469
4000_002C	Peripheral Access Control Register (AIPS0_PACRD)	32	R/W	See section	22.3.2/469
4000_0040	Peripheral Access Control Register (AIPS0_PACRE)	32	R/W	See section	22.3.3/474
4000_0044	Peripheral Access Control Register (AIPS0_PACRF)	32	R/W	See section	22.3.3/474
4000_0048	Peripheral Access Control Register (AIPS0_PACRG)	32	R/W	See section	22.3.3/474
4000_004C	Peripheral Access Control Register (AIPS0_PACRH)	32	R/W	See section	22.3.3/474
4000_0050	Peripheral Access Control Register (AIPS0_PACRI)	32	R/W	See section	22.3.3/474
4000_0054	Peripheral Access Control Register (AIPS0_PACRJ)	32	R/W	See section	22.3.3/474
4000_0058	Peripheral Access Control Register (AIPS0_PACRK)	32	R/W	See section	22.3.3/474
4000_005C	Peripheral Access Control Register (AIPS0_PACRL)	32	R/W	See section	22.3.3/474
4000_0060	Peripheral Access Control Register (AIPS0_PACRM)	32	R/W	See section	22.3.3/474
4000_0064	Peripheral Access Control Register (AIPS0_PACRN)	32	R/W	See section	22.3.3/474
4000_0068	Peripheral Access Control Register (AIPS0_PACRO)	32	R/W	See section	22.3.3/474
4000_006C	Peripheral Access Control Register (AIPS0_PACRP)	32	R/W	See section	22.3.3/474
4008_0000	Master Privilege Register A (AIPS1_MPRA)	32	R/W	See section	22.3.1/466
4008_0020	Peripheral Access Control Register (AIPS1_PACRA)	32	R/W	See section	22.3.2/469
4008_0024	Peripheral Access Control Register (AIPS1_PACRB)	32	R/W	See section	22.3.2/469
4008_0028	Peripheral Access Control Register (AIPS1_PACRC)	32	R/W	See section	22.3.2/469
4008_002C	Peripheral Access Control Register (AIPS1_PACRD)	32	R/W	See section	22.3.2/469
4008_0040	Peripheral Access Control Register (AIPS1_PACRE)	32	R/W	See section	22.3.3/474
4008_0044	Peripheral Access Control Register (AIPS1_PACRF)	32	R/W	See section	22.3.3/474
4008_0048	Peripheral Access Control Register (AIPS1_PACRG)	32	R/W	See section	22.3.3/474
4008_004C	Peripheral Access Control Register (AIPS1_PACRH)	32	R/W	See section	22.3.3/474
4008_0050	Peripheral Access Control Register (AIPS1_PACRI)	32	R/W	See section	22.3.3/474
4008_0054	Peripheral Access Control Register (AIPS1_PACRJ)	32	R/W	See section	22.3.3/474
4008_0058	Peripheral Access Control Register (AIPS1_PACRK)	32	R/W	See section	22.3.3/474
4008_005C	Peripheral Access Control Register (AIPS1_PACRL)	32	R/W	See section	22.3.3/474
4008_0060	Peripheral Access Control Register (AIPS1_PACRM)	32	R/W	See section	22.3.3/474
4008_0064	Peripheral Access Control Register (AIPS1_PACRN)	32	R/W	See section	22.3.3/474
4008_0068	Peripheral Access Control Register (AIPS1_PACRO)	32	R/W	See section	22.3.3/474
4008_006C	Peripheral Access Control Register (AIPS1_PACRP)	32	R/W	See section	22.3.3/474

22.3.1 Master Privilege Register A (AIPSx_MPRA)

The MPRA specifies identical 4-bit fields defining the access-privilege level associated with a bus master to various peripherals on the chip. The register provides one field per bus master.

NOTE

At reset, the default value loaded into the MPRA fields is chip-specific. See the chip configuration details for the value of a particular device.

A register field that maps to an unimplemented master or peripheral behaves as read-only-zero.

Each master is assigned a logical ID from 0 to 15. See the master logical ID assignment table in the chip-specific AIPS information.

Address: Base address + 0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	MTR0	MTW0	MPL0	0	MTR1	MTW1	MPL1	0	MTR2	MTW2	MPL2	0	MTR3	MTW3	MPL3
W																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	MTR4	MTW4	MPL4	Reserved				Reserved				Reserved			
W																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- The reset value is chip-dependent and can be found in the chip-specific AIPS information.

AIPSx_MPRA field descriptions

Field	Description
31 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
30 MTR0	Master 0 Trusted For Read Determines whether the master is trusted for read accesses. 0 This master is not trusted for read accesses. 1 This master is trusted for read accesses.

Table continues on the next page...

AIPSx_MPRA field descriptions (continued)

Field	Description
29 MTW0	Master 0 Trusted For Writes Determines whether the master is trusted for write accesses. 0 This master is not trusted for write accesses. 1 This master is trusted for write accesses.
28 MPL0	Master 0 Privilege Level Specifies how the privilege level of the master is determined. 0 Accesses from this master are forced to user-mode. 1 Accesses from this master are not forced to user-mode.
27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 MTR1	Master 1 Trusted for Read Determines whether the master is trusted for read accesses. 0 This master is not trusted for read accesses. 1 This master is trusted for read accesses.
25 MTW1	Master 1 Trusted for Writes Determines whether the master is trusted for write accesses. 0 This master is not trusted for write accesses. 1 This master is trusted for write accesses.
24 MPL1	Master 1 Privilege Level Specifies how the privilege level of the master is determined. 0 Accesses from this master are forced to user-mode. 1 Accesses from this master are not forced to user-mode.
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 MTR2	Master 2 Trusted For Read Determines whether the master is trusted for read accesses. 0 This master is not trusted for read accesses. 1 This master is trusted for read accesses.
21 MTW2	Master 2 Trusted For Writes Determines whether the master is trusted for write accesses. 0 This master is not trusted for write accesses. 1 This master is trusted for write accesses.
20 MPL2	Master 2 Privilege Level Specifies how the privilege level of the master is determined. 0 Accesses from this master are forced to user-mode. 1 Accesses from this master are not forced to user-mode.

Table continues on the next page...

AIPSx_MPRA field descriptions (continued)

Field	Description
19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18 MTR3	Master 3 Trusted For Read Determines whether the master is trusted for read accesses. 0 This master is not trusted for read accesses. 1 This master is trusted for read accesses.
17 MTW3	Master 3 Trusted For Writes Determines whether the master is trusted for write accesses. 0 This master is not trusted for write accesses. 1 This master is trusted for write accesses.
16 MPL3	Master 3 Privilege Level Specifies how the privilege level of the master is determined. 0 Accesses from this master are forced to user-mode. 1 Accesses from this master are not forced to user-mode.
15 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
14 MTR4	Master 4 Trusted For Read Determines whether the master is trusted for read accesses. 0 This master is not trusted for read accesses. 1 This master is trusted for read accesses.
13 MTW4	Master 4 Trusted For Writes Determines whether the master is trusted for write accesses. 0 This master is not trusted for write accesses. 1 This master is trusted for write accesses.
12 MPL4	Master 4 Privilege Level Specifies how the privilege level of the master is determined. 0 Accesses from this master are forced to user-mode. 1 Accesses from this master are not forced to user-mode.
11–8 Reserved	This field is reserved.
7–4 Reserved	This field is reserved.
Reserved	This field is reserved.

22.3.2 Peripheral Access Control Register (AIPSx_PACR*n*)

Each PACR register consists of eight 4-bit PACR fields. Each PACR field defines the access levels for a particular peripheral. The mapping between a peripheral and its PACR field is shown in the table below. The peripheral assignment to each PACR is defined by the memory map slot that the peripheral is assigned to. See this chip's memory map for the assignment of a particular peripheral.

The following table shows the location of each peripheral slot's PACR field in the PACR registers.

Offset	Register	[31:28]	[27:24]	[23:20]	[19:16]	[15:12]	[11:8]	[7:4]	[3:0]
0x20	PACRA	PACR0	PACR1	PACR2	PACR3	PACR4	PACR5	PACR6	PACR7
0x24	PACRB	PACR8	PACR9	PACR10	PACR11	PACR12	PACR13	PACR14	PACR15
0x28	PACRC	PACR16	PACR17	PACR18	PACR19	PACR20	PACR21	PACR22	PACR23
0x2C	PACRD	PACR24	PACR25	PACR26	PACR27	PACR28	PACR29	PACR30	PACR31
0x30	Reserved								
0x34	Reserved								
0x38	Reserved								
0x3C	Reserved								
0x40	PACRE	PACR32	PACR33	PACR34	PACR35	PACR36	PACR37	PACR38	PACR39
0x44	PACRF	PACR40	PACR41	PACR42	PACR43	PACR44	PACR45	PACR46	PACR47
0x48	PACRG	PACR48	PACR49	PACR50	PACR51	PACR52	PACR53	PACR54	PACR55
0x4C	PACRH	PACR56	PACR57	PACR58	PACR59	PACR60	PACR61	PACR62	PACR63
0x50	PACRI	PACR64	PACR65	PACR66	PACR67	PACR68	PACR69	PACR70	PACR71
0x54	PACRJ	PACR72	PACR73	PACR74	PACR75	PACR76	PACR77	PACR78	PACR79
0x58	PACRK	PACR80	PACR81	PACR82	PACR83	PACR84	PACR85	PACR86	PACR87
0x5C	PACRL	PACR88	PACR89	PACR90	PACR91	PACR92	PACR93	PACR94	PACR95
0x60	PACRM	PACR96	PACR97	PACR98	PACR99	PACR100	PACR101	PACR102	PACR103
0x64	PACRN	PACR104	PACR105	PACR106	PACR107	PACR108	PACR109	PACR110	PACR111
0x68	PACRO	PACR112	PACR113	PACR114	PACR115	PACR116	PACR117	PACR118	PACR119
0x6C	PACRP	PACR120	PACR121	PACR122	PACR123	PACR124	PACR125	PACR126	PACR127

NOTE

The register field descriptions for PACR A-D, which control peripheral slots 0-31, are shown below. The following section, Peripheral Access Control Register (AIPS_PACR*n*), shows the register field descriptions for PACR E-P. All PACR registers are identical. They are divided into two sections because they occupy two non-contiguous address spaces.

Address: Base address + 20h offset + (4d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	SP0	WP0	TP0	0	SP1	WP1	TP1	0	SP2	WP2	TP2	0	SP3	WP3	TP3
W																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	SP4	WP4	TP4	0	SP5	WP5	TP5	0	SP6	WP6	TP6	0	SP7	WP7	TP7
W																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- The reset value is chip-dependent and can be found in the AIPS chip-specific information.

AIPSx_PACRn field descriptions

Field	Description
31 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
30 SP0	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for accesses. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPRx[MPLn] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.
29 WP0	Write Protect Determines whether the peripheral allows write accesss. When this bit is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
28 TP0	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this field is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 SP1	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for accesses. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPRx[MPLn] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.

Table continues on the next page...

AIPSx_PACRn field descriptions (continued)

Field	Description
25 WP1	Write Protect Determines whether the peripheral allows write accesses. When this field is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
24 TP1	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this bit is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 SP2	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for accesses. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPRx[MPLn] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.
21 WP2	Write Protect Determines whether the peripheral allows write accesss. When this bit is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
20 TP2	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this field is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18 SP3	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for access. When this bit is set, the master privilege level must indicate the supervisor access attribute, and the MPRx[MPLn] control bit for the master must be set. If not, access terminates with an error response and no peripheral access initiates. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.

Table continues on the next page...

AIPSx_PACRn field descriptions (continued)

Field	Description
17 WP3	Write Protect Determines whether the peripheral allows write accesses. When this field is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
16 TP3	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this bit is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
15 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
14 SP4	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for accesses. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPR*x*[MPL*n*] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.
13 WP4	Write Protect Determines whether the peripheral allows write accesss. When this bit is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
12 TP4	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this field is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10 SP5	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for accesses. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPR*x*[MPL*n*] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.

Table continues on the next page...

AIPSx_PACR*n* field descriptions (continued)

Field	Description
9 WP5	Write Protect Determines whether the peripheral allows write accesses. When this field is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
8 TP5	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this field is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 SP6	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for accesses. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPR*x*[MPL*n*] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.
5 WP6	Write Protect Determines whether the peripheral allows write accesses. When this field is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
4 TP6	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this field is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 SP7	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for accesses. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPR*x*[MPL*n*] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.

Table continues on the next page...

AIPSx_PACRn field descriptions (continued)

Field	Description
1 WP7	Write Protect Determines whether the peripheral allows write accesses. When this field is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
0 TP7	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this field is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.

22.3.3 Peripheral Access Control Register (AIPSx_PACRn)

This section describes PACR registers E-P, which control peripheral slots 32-127. See Peripheral Access Control Register (AIPS_PACRn) for the description of these registers.

Address: Base address + 40h offset + (4d × i), where i=0d to 11d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	SP0	WP0	TP0	0	SP1	WP1	TP1	0	SP2	WP2	TP2	0	SP3	WP3	TP3
W																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	SP4	WP4	TP4	0	SP5	WP5	TP5	0	SP6	WP6	TP6	0	SP7	WP7	TP7
W																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- The reset value is chip-dependent and can be found in the AIPS chip-specific information.

AIPSx_PACRn field descriptions

Field	Description
31 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
30 SP0	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for accesses. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPRx[MPLn] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates.

Table continues on the next page...

AIPSx_PACRn field descriptions (continued)

Field	Description
	0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.
29 WP0	Write Protect Determines whether the peripheral allows write accesses. When this field is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
28 TP0	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this bit is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 SP1	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for access. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPR*x*[MPL*n*] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.
25 WP1	Write Protect Determines whether the peripheral allows write accesses. When this field is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
24 TP1	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this field is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 SP2	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for access. When this bit is set, the master privilege level must indicate the supervisor access attribute, and the MPR*x*[MPL*n*] control bit for the master must be set. If not, access terminates with an error response and no peripheral access initiates.

Table continues on the next page...

AIPSx_PACRn field descriptions (continued)

Field	Description
	0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.
21 WP2	Write Protect Determines whether the peripheral allows write accesses. When this field is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
20 TP2	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this bit is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18 SP3	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for accesses. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPR*x*[MPL*n*] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.
17 WP3	Write Protect Determines whether the peripheral allows write accesss. When this bit is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
16 TP3	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this field is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
15 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
14 SP4	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for access. When this bit is set, the master privilege level must indicate the supervisor access attribute, and the MPR*x*[MPL*n*] control bit for the master must be set. If not, access terminates with an error response and no peripheral access initiates.

Table continues on the next page...

AIPSx_PACR*n* field descriptions (continued)

Field	Description
	0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.
13 WP4	Write Protect Determines whether the peripheral allows write accesses. When this field is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
12 TP4	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this bit is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10 SP5	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for accesses. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPR*x*[MPL*n*] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.
9 WP5	Write Protect Determines whether the peripheral allows write accesses. When this field is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
8 TP5	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this field is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 SP6	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for accesses. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPR*x*[MPL*n*] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates.

Table continues on the next page...

AIPSx_PACR*n* field descriptions (continued)

Field	Description
	0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.
5 WP6	Write Protect Determines whether the peripheral allows write accesses. When this field is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
4 TP6	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this field is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 SP7	Supervisor Protect Determines whether the peripheral requires supervisor privilege level for accesses. When this field is set, the master privilege level must indicate the supervisor access attribute, and the MPR*x*[MPL*n*] control field for the master must be set. If not, access terminates with an error response and no peripheral access initiates. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses.
1 WP7	Write Protect Determines whether the peripheral allows write accesses. When this field is set and a write access is attempted, access terminates with an error response and no peripheral access initiates. 0 This peripheral allows write accesses. 1 This peripheral is write protected.
0 TP7	Trusted Protect Determines whether the peripheral allows accesses from an untrusted master. When this field is set and an access is attempted by an untrusted master, the access terminates with an error response and no peripheral access initiates. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed.

22.4 Functional description

The peripheral bridge functions as a bus protocol translator between the crossbar switch and the slave peripheral bus.

The peripheral bridge manages all transactions destined for the attached slave devices and generates select signals for modules on the peripheral bus by decoding accesses within the attached address space.

22.4.1 Access support

Aligned and misaligned 32-bit, 16-bit, and byte accesses are supported for 32-bit peripherals. Misaligned accesses are supported to allow memory to be placed on the slave peripheral bus. Peripheral registers must not be misaligned, although no explicit checking is performed by the peripheral bridge. All accesses are performed with a single transfer.

All accesses to the peripheral slots must be sized less than or equal to the designated peripheral slot size. If an access is attempted that is larger than the targeted port, an error response is generated.

Chapter 23
Memory Protection Unit (MPU)

23.1 Chip-specific MPU information

23.1.1 MPU Slave Port Assignments

The memory-mapped resources protected by the MPU are:

Table 23-1. MPU Slave Port Assignments

Source	MPU Slave Port Assignment	Destination
Crossbar slave port 0	MPU slave port 0	Flash Controller
Crossbar slave port 1	MPU slave port 1	SRAM backdoor
Code Bus	MPU slave port 2	SRAM_L frontdoor
System Bus	MPU slave port 3	SRAM_U frontdoor
Crossbar slave port 4	MPU slave port 4	FlexBus/SDRAM Controller
Crossbar slave port 5	MPU slave port 5	OTFAD/QSPI

23.1.2 MPU Logical Bus Master Assignments

The logical bus master assignments for the MPU are:

Table 23-2. MPU Logical Bus Master Assignments

MPU Logical Bus Master Number	Bus Master
0	Core
1	Debugger
2	eDMA
3	USB
4	eSDHC

23.1.3 Reset Values for RGD0 Registers

At reset, the MPU is enabled with a single region descriptor (RGD0) that maps the entire 4 GB address space with read, write and execute permissions given to the core, debugger and the DMA bus masters.

The following table shows the chip-specific reset values for RGD0 and RGDAAC0.

Table 23-3. Reset Values for RGD0 Registers

Register	Reset value
RGD0_WORD0	0000_0000h
RGD0_WORD1	FFFF_FFFFh
RGD0_WORD2	0061_F7DFh
RGD0_WORD3	0000_0001h
RGDAAC0	0061_F7DFh

23.1.4 Write Access Restrictions for RGD0 Registers

In addition to configuring the initial state of RGD0, the MPU implements further access control on writes to the RGD0 registers. Specifically, the MPU assigns a priority scheme where the debugger is treated as the highest priority master followed by the core and then all the remaining masters.

The MPU does not allow writes from the core to affect the RGD0 start or end addresses nor the permissions associated with the debugger; it can only write the permission fields associated with the other masters.

These protections (summarized below) guarantee that the debugger always has access to the entire address space and those rights cannot be changed by the core or any other bus master.

Table 23-4. Write Access to RGD0 Registers

Bus Master	Write Access?
Core	Partial. The Core cannot write to the following registers or register fields: • RGD0_WORD0, RGD0_WORD1, RGD0_WORD3 • RGD0_WORD2[M1SM, M1UM] • RGDAAC0[M1SM, M1UM] **NOTE:** Changes to the RGD0_WORD2 alterable fields should be done via a write to RGDAAC0.

Table continues on the next page...

Table 23-4. Write Access to RGD0 Registers (continued)

Bus Master	Write Access?
Debugger	Yes
All other masters	No

23.2 Introduction

The memory protection unit (MPU) provides hardware access control for all memory references generated in the device.

23.3 Overview

The MPU concurrently monitors all system bus transactions and evaluates their appropriateness using pre-programmed region descriptors that define memory spaces and their access rights. Memory references that have sufficient access control rights are allowed to complete, while references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

23.3.1 Block diagram

A simplified block diagram of the MPU module is shown in the following figure.

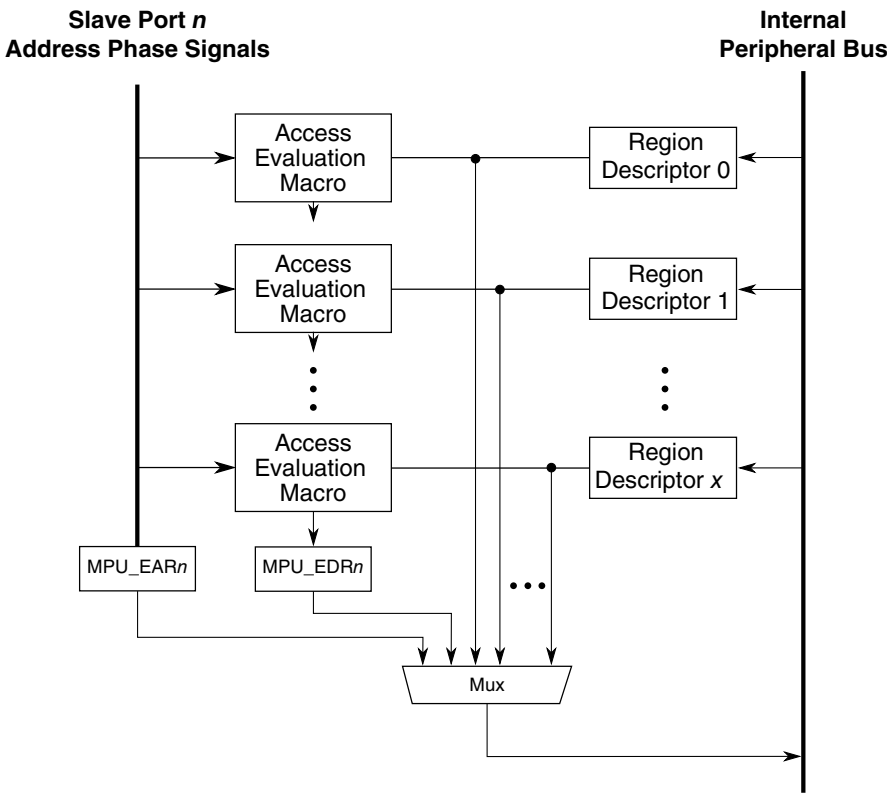


Figure 23-1. MPU block diagram

The hardware's two-dimensional connection matrix is clearly visible with the basic access evaluation macro shown as the replicated submodule block. The crossbar switch slave ports are shown on the left, the region descriptor registers in the middle, and the peripheral bus interface on the right side. The evaluation macro contains two magnitude comparators connected to the start and end address registers from each region descriptor as well as the combinational logic blocks to determine the region hit and the access protection error. For details of the access evaluation macro, see Access evaluation macro.

23.3.2 Features

The MPU implements a two-dimensional hardware array of memory region descriptors and the crossbar slave ports to continuously monitor the legality of every memory reference generated by each bus master in the system.

The feature set includes:

- 12 program-visible 128-bit region descriptors, accessible by four 32-bit words each
  - Each region descriptor defines a modulo-32 byte space, aligned anywhere in memory

        - Region sizes can vary from 32 bytes to 4 Gbytes
    - Two access control permissions defined in a single descriptor word
        - Masters 0–3: read, write, and execute attributes for supervisor and user accesses
        - Masters 4–7: read and write attributes
    - Hardware-assisted maintenance of the descriptor valid bit minimizes coherency issues
    - Alternate programming model view of the access control permissions word
    - Priority given to granting permission over denying access for overlapping region descriptors
- Detects access protection errors if a memory reference does not hit in any memory region, or if the reference is illegal in all hit memory regions. If an access error occurs, the reference is terminated with an error response, and the MPU inhibits the bus cycle being sent to the targeted slave device.
- Error registers, per slave port, capture the last faulting address, attributes, and other information
- Global MPU enable/disable control bit

23.4 Memory map/register definition

The programming model is partitioned into three groups:

- Control/status registers
- The data structure containing the region descriptors
- The alternate view of the region descriptor access control values

The programming model can only be referenced using 32-bit accesses. Attempted references using different access sizes, to undefined, that is, reserved, addresses, or with a non-supported access type, such as a write to a read-only register, or a read of a write-only register, generate an error termination.

The programming model can be accessed only in supervisor mode.

NOTE

See the chip configuration details for any chip-specific register information in this module.

MPU memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_D000	Control/Error Status Register (MPU_CESR)	32	R/W	0081_5101h	23.4.1/488
4000_D010	Error Address Register, slave port n (MPU_EAR0)	32	R	0000_0000h	23.4.2/489
4000_D014	Error Detail Register, slave port n (MPU_EDR0)	32	R	0000_0000h	23.4.3/490
4000_D018	Error Address Register, slave port n (MPU_EAR1)	32	R	0000_0000h	23.4.2/489
4000_D01C	Error Detail Register, slave port n (MPU_EDR1)	32	R	0000_0000h	23.4.3/490
4000_D020	Error Address Register, slave port n (MPU_EAR2)	32	R	0000_0000h	23.4.2/489
4000_D024	Error Detail Register, slave port n (MPU_EDR2)	32	R	0000_0000h	23.4.3/490
4000_D028	Error Address Register, slave port n (MPU_EAR3)	32	R	0000_0000h	23.4.2/489
4000_D02C	Error Detail Register, slave port n (MPU_EDR3)	32	R	0000_0000h	23.4.3/490
4000_D030	Error Address Register, slave port n (MPU_EAR4)	32	R	0000_0000h	23.4.2/489
4000_D034	Error Detail Register, slave port n (MPU_EDR4)	32	R	0000_0000h	23.4.3/490
4000_D400	Region Descriptor n, Word 0 (MPU_RGD0_WORD0)	32	R/W	0000_0000h	23.4.4/491
4000_D404	Region Descriptor n, Word 1 (MPU_RGD0_WORD1)	32	R/W	See section	23.4.5/492
4000_D408	Region Descriptor n, Word 2 (MPU_RGD0_WORD2)	32	R/W	See section	23.4.6/492
4000_D40C	Region Descriptor n, Word 3 (MPU_RGD0_WORD3)	32	R/W	See section	23.4.7/495
4000_D410	Region Descriptor n, Word 0 (MPU_RGD1_WORD0)	32	R/W	0000_0000h	23.4.4/491
4000_D414	Region Descriptor n, Word 1 (MPU_RGD1_WORD1)	32	R/W	See section	23.4.5/492
4000_D418	Region Descriptor n, Word 2 (MPU_RGD1_WORD2)	32	R/W	See section	23.4.6/492
4000_D41C	Region Descriptor n, Word 3 (MPU_RGD1_WORD3)	32	R/W	See section	23.4.7/495
4000_D420	Region Descriptor n, Word 0 (MPU_RGD2_WORD0)	32	R/W	0000_0000h	23.4.4/491
4000_D424	Region Descriptor n, Word 1 (MPU_RGD2_WORD1)	32	R/W	See section	23.4.5/492
4000_D428	Region Descriptor n, Word 2 (MPU_RGD2_WORD2)	32	R/W	See section	23.4.6/492
4000_D42C	Region Descriptor n, Word 3 (MPU_RGD2_WORD3)	32	R/W	See section	23.4.7/495
4000_D430	Region Descriptor n, Word 0 (MPU_RGD3_WORD0)	32	R/W	0000_0000h	23.4.4/491
4000_D434	Region Descriptor n, Word 1 (MPU_RGD3_WORD1)	32	R/W	See section	23.4.5/492
4000_D438	Region Descriptor n, Word 2 (MPU_RGD3_WORD2)	32	R/W	See section	23.4.6/492
4000_D43C	Region Descriptor n, Word 3 (MPU_RGD3_WORD3)	32	R/W	See section	23.4.7/495
4000_D440	Region Descriptor n, Word 0 (MPU_RGD4_WORD0)	32	R/W	0000_0000h	23.4.4/491
4000_D444	Region Descriptor n, Word 1 (MPU_RGD4_WORD1)	32	R/W	See section	23.4.5/492
4000_D448	Region Descriptor n, Word 2 (MPU_RGD4_WORD2)	32	R/W	See section	23.4.6/492
4000_D44C	Region Descriptor n, Word 3 (MPU_RGD4_WORD3)	32	R/W	See section	23.4.7/495
4000_D450	Region Descriptor n, Word 0 (MPU_RGD5_WORD0)	32	R/W	0000_0000h	23.4.4/491
4000_D454	Region Descriptor n, Word 1 (MPU_RGD5_WORD1)	32	R/W	See section	23.4.5/492
4000_D458	Region Descriptor n, Word 2 (MPU_RGD5_WORD2)	32	R/W	See section	23.4.6/492
4000_D45C	Region Descriptor n, Word 3 (MPU_RGD5_WORD3)	32	R/W	See section	23.4.7/495
4000_D460	Region Descriptor n, Word 0 (MPU_RGD6_WORD0)	32	R/W	0000_0000h	23.4.4/491
4000_D464	Region Descriptor n, Word 1 (MPU_RGD6_WORD1)	32	R/W	See section	23.4.5/492
4000_D468	Region Descriptor n, Word 2 (MPU_RGD6_WORD2)	32	R/W	See section	23.4.6/492

Table continues on the next page...

MPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_D46C	Region Descriptor n, Word 3 (MPU_RGD6_WORD3)	32	R/W	See section	23.4.7/495
4000_D470	Region Descriptor n, Word 0 (MPU_RGD7_WORD0)	32	R/W	0000_0000h	23.4.4/491
4000_D474	Region Descriptor n, Word 1 (MPU_RGD7_WORD1)	32	R/W	See section	23.4.5/492
4000_D478	Region Descriptor n, Word 2 (MPU_RGD7_WORD2)	32	R/W	See section	23.4.6/492
4000_D47C	Region Descriptor n, Word 3 (MPU_RGD7_WORD3)	32	R/W	See section	23.4.7/495
4000_D480	Region Descriptor n, Word 0 (MPU_RGD8_WORD0)	32	R/W	0000_0000h	23.4.4/491
4000_D484	Region Descriptor n, Word 1 (MPU_RGD8_WORD1)	32	R/W	See section	23.4.5/492
4000_D488	Region Descriptor n, Word 2 (MPU_RGD8_WORD2)	32	R/W	See section	23.4.6/492
4000_D48C	Region Descriptor n, Word 3 (MPU_RGD8_WORD3)	32	R/W	See section	23.4.7/495
4000_D490	Region Descriptor n, Word 0 (MPU_RGD9_WORD0)	32	R/W	0000_0000h	23.4.4/491
4000_D494	Region Descriptor n, Word 1 (MPU_RGD9_WORD1)	32	R/W	See section	23.4.5/492
4000_D498	Region Descriptor n, Word 2 (MPU_RGD9_WORD2)	32	R/W	See section	23.4.6/492
4000_D49C	Region Descriptor n, Word 3 (MPU_RGD9_WORD3)	32	R/W	See section	23.4.7/495
4000_D4A0	Region Descriptor n, Word 0 (MPU_RGD10_WORD0)	32	R/W	0000_0000h	23.4.4/491
4000_D4A4	Region Descriptor n, Word 1 (MPU_RGD10_WORD1)	32	R/W	See section	23.4.5/492
4000_D4A8	Region Descriptor n, Word 2 (MPU_RGD10_WORD2)	32	R/W	See section	23.4.6/492
4000_D4AC	Region Descriptor n, Word 3 (MPU_RGD10_WORD3)	32	R/W	See section	23.4.7/495
4000_D4B0	Region Descriptor n, Word 0 (MPU_RGD11_WORD0)	32	R/W	0000_0000h	23.4.4/491
4000_D4B4	Region Descriptor n, Word 1 (MPU_RGD11_WORD1)	32	R/W	See section	23.4.5/492
4000_D4B8	Region Descriptor n, Word 2 (MPU_RGD11_WORD2)	32	R/W	See section	23.4.6/492
4000_D4BC	Region Descriptor n, Word 3 (MPU_RGD11_WORD3)	32	R/W	See section	23.4.7/495
4000_D800	Region Descriptor Alternate Access Control n (MPU_RGDAAC0)	32	R/W	See section	23.4.8/496
4000_D804	Region Descriptor Alternate Access Control n (MPU_RGDAAC1)	32	R/W	See section	23.4.8/496
4000_D808	Region Descriptor Alternate Access Control n (MPU_RGDAAC2)	32	R/W	See section	23.4.8/496
4000_D80C	Region Descriptor Alternate Access Control n (MPU_RGDAAC3)	32	R/W	See section	23.4.8/496
4000_D810	Region Descriptor Alternate Access Control n (MPU_RGDAAC4)	32	R/W	See section	23.4.8/496
4000_D814	Region Descriptor Alternate Access Control n (MPU_RGDAAC5)	32	R/W	See section	23.4.8/496
4000_D818	Region Descriptor Alternate Access Control n (MPU_RGDAAC6)	32	R/W	See section	23.4.8/496
4000_D81C	Region Descriptor Alternate Access Control n (MPU_RGDAAC7)	32	R/W	See section	23.4.8/496
4000_D820	Region Descriptor Alternate Access Control n (MPU_RGDAAC8)	32	R/W	See section	23.4.8/496
4000_D824	Region Descriptor Alternate Access Control n (MPU_RGDAAC9)	32	R/W	See section	23.4.8/496

Table continues on the next page...

MPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_D828	Region Descriptor Alternate Access Control n (MPU_RGDAAC10)	32	R/W	See section	23.4.8/496
4000_D82C	Region Descriptor Alternate Access Control n (MPU_RGDAAC11)	32	R/W	See section	23.4.8/496

23.4.1 Control/Error Status Register (MPU_CESR)

Address: 4000_D000h base + 0h offset = 4000_D000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	SPERR					0			1	0			HRL			
W	w1c															
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	NSP				NRGD				0							VLD
W																
Reset	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	1

MPU_CESR field descriptions

Field	Description
31–27 SPERR	Slave Port n Error Indicates a captured error in EARn and EDRn. This bit is set when the hardware detects an error and records the faulting address and attributes. It is cleared by writing one to it. If another error is captured at the exact same cycle as the write, the flag remains set. A find-first-one instruction or equivalent can detect the presence of a captured error. The following shows the correspondence between the bit number and slave port number: • Bit 31 corresponds to slave port 0. • Bit 30 corresponds to slave port 1. • Bit 29 corresponds to slave port 2. • Bit 28 corresponds to slave port 3. • Bit 27 corresponds to slave port 4. 0 No error has occurred for slave port n. 1 An error has occurred for slave port n.
26–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
22–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

MPU_CESR field descriptions (continued)

Field	Description
19–16 HRL	Hardware Revision Level Specifies the MPU's hardware and definition revision level. It can be read by software to determine the functional definition of the module.
15–12 NSP	Number Of Slave Ports Specifies the number of slave ports connected to the MPU.
11–8 NRGD	Number Of Region Descriptors Indicates the number of region descriptors implemented in the MPU. 0000 8 region descriptors 0001 12 region descriptors 0010 16 region descriptors
7–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 VLD	Valid Global enable/disable for the MPU. 0 MPU is disabled. All accesses from all bus masters are allowed. 1 MPU is enabled

23.4.2 Error Address Register, slave port n (MPU_EAR*n*)

When the MPU detects an access error on slave port n, the 32-bit reference address is captured in this read-only register and the corresponding bit in CESR[SPERR] set. Additional information about the faulting access is captured in the corresponding EDRn at the same time. This register and the corresponding EDRn contain the most recent access error; there are no hardware interlocks with CESR[SPERR], as the error registers are always loaded upon the occurrence of each protection violation.

Address: 4000_D000h base + 10h offset + (8d × i), where i=0d to 4d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	EADDR																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

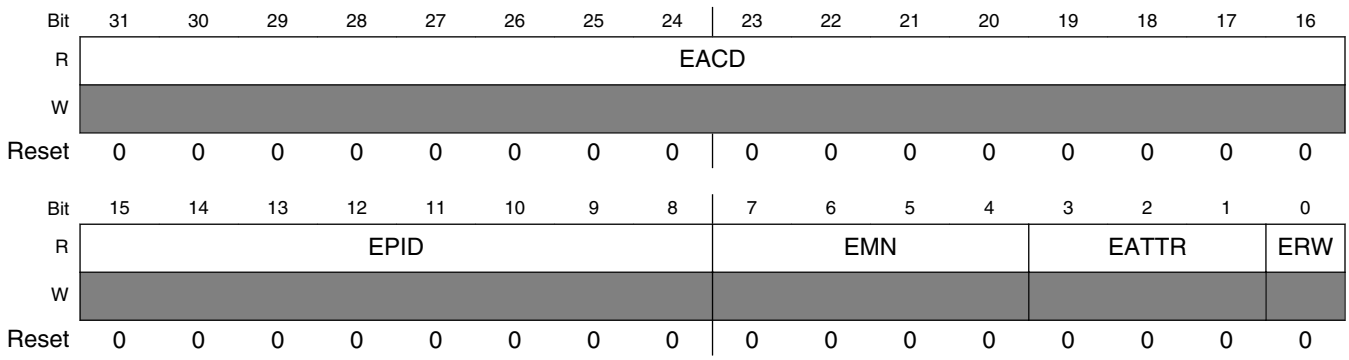
MPU_EAR*n* field descriptions

Field	Description
EADDR	Error Address Indicates the reference address from slave port n that generated the access error

23.4.3 Error Detail Register, slave port n (MPU_EDR*n*)

When the MPU detects an access error on slave port n, 32 bits of error detail are captured in this read-only register and the corresponding bit in CESR[SPERR] is set. Information on the faulting address is captured in the corresponding EARn register at the same time. This register and the corresponding EARn register contain the most recent access error; there are no hardware interlocks with CESR[SPERR] as the error registers are always loaded upon the occurrence of each protection violation.

Address: 4000_D000h base + 14h offset + (8d × i), where i=0d to 4d



MPU_EDR*n* field descriptions

Field	Description
31–16 EACD	Error Access Control Detail Indicates the region descriptor with the access error. • If EDRn contains a captured error and EACD is cleared, an access did not hit in any region descriptor. • If only a single EACD bit is set, the protection error was caused by a single non-overlapping region descriptor. • If two or more EACD bits are set, the protection error was caused by an overlapping set of region descriptors.
15–8 EPID	Error Process Identification Records the process identifier of the faulting reference. The process identifier is typically driven only by processor cores; for other bus masters, this field is cleared.
7–4 EMN	Error Master Number Indicates the bus master that generated the access error.
3–1 EATTR	Error Attributes Indicates attribute information about the faulting reference. **NOTE:** All other encodings are reserved. 000 User mode, instruction access 001 User mode, data access 010 Supervisor mode, instruction access 011 Supervisor mode, data access

Table continues on the next page...

MPU_EDR*n* field descriptions (continued)

Field	Description
0 ERW	Error Read/Write Indicates the access type of the faulting reference. 0 Read 1 Write

23.4.4 Region Descriptor n, Word 0 (MPU_RGD*n*_WORD0)

The first word of the region descriptor defines the 0-modulo-32 byte start address of the memory region. Writes to this register clear the region descriptor's valid bit (RGDn_WORD3[VLD]).

Address: 4000_D000h base + 400h offset + (16d × i), where i=0d to 11d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SRTADDR																											0				
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MPU_RGD*n*_WORD0 field descriptions

Field	Description
31–5 SRTADDR	Start Address Defines the most significant bits of the 0-modulo-32 byte start address of the memory region.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

23.4.5 Region Descriptor n, Word 1 (MPU_RGD*n*_WORD1)

The second word of the region descriptor defines the 31-modulo-32 byte end address of the memory region. Writes to this register clear the region descriptor's valid bit (RGDn_WORD3[VLD]).

Address: 4000_D000h base + 404h offset + (16d × i), where i=0d to 11d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ENDADDR																											Reserved				
W																																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	1*	1*	1*	1*	1*

* Notes:
- Reset value of RGD0_WORD1 is FFFF_FFFFh

  Reset value of RGD[1:11]_WORD1 is 0000_001Fh

MPU_RGD*n*_WORD1 field descriptions

Field	Description
31–5 ENDADDR	End Address Defines the most significant bits of the 31-modulo-32 byte end address of the memory region. **NOTE:** The MPU does not verify that ENDADDR ≥ SRTADDR.
Reserved	This field is reserved.

23.4.6 Region Descriptor n, Word 2 (MPU_RGD*n*_WORD2)

The third word of the region descriptor defines the access control rights of the memory region. The access control privileges depend on two broad classifications of bus masters:

- Bus masters 0–3 have a 5-bit field defining separate privilege rights for user and supervisor mode accesses, as well as the optional inclusion of a process identification field within the definition.
- Bus masters 4–7 are limited to separate read and write permissions.

For the privilege rights of bus masters 0–3, there are three flags associated with this function:

- Read (r) refers to accessing the referenced memory address using an operand (data) fetch

- Write (w) refers to updating the referenced memory address using a store (data) instruction
- Execute (x) refers to reading the referenced memory address using an instruction fetch

Writes to RGDn_WORD2 clear the region descriptor's valid bit (RGDn_WORD3[VLD]). If only updating the access controls, write to RGDAACn instead because stores to these locations do not affect the descriptor's valid bit.

Address: 4000_D000h base + 408h offset + (16d × i), where i=0d to 11d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	M7RE	M7WE	M6RE	M6WE	M5RE	M5WE	M4RE	M4WE	M3PE	M3SM		M3UM			M2PE	M2SM
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	M2SM	M2UM			M1PE	M1SM		M1UM			M0PE	M0SM		M0UM		
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- Reset value of RGD0_WORD2 is 0061_F7DFh

  Reset value of RGD[1:12]_WORD2 is 0000_0000h

MPU_RGD*n*_WORD2 field descriptions

Field	Description
31 M7RE	Bus Master 7 Read Enable 0 Bus master 7 reads terminate with an access error and the read is not performed 1 Bus master 7 reads allowed
30 M7WE	Bus Master 7 Write Enable 0 Bus master 7 writes terminate with an access error and the write is not performed 1 Bus master 7 writes allowed
29 M6RE	Bus Master 6 Read Enable 0 Bus master 6 reads terminate with an access error and the read is not performed 1 Bus master 6 reads allowed
28 M6WE	Bus Master 6 Write Enable 0 Bus master 6 writes terminate with an access error and the write is not performed 1 Bus master 6 writes allowed

Table continues on the next page...

MPU_RGD*n*_WORD2 field descriptions (continued)

Field	Description
27 M5RE	Bus Master 5 Read Enable 0 Bus master 5 reads terminate with an access error and the read is not performed 1 Bus master 5 reads allowed
26 M5WE	Bus Master 5 Write Enable 0 Bus master 5 writes terminate with an access error and the write is not performed 1 Bus master 5 writes allowed
25 M4RE	Bus Master 4 Read Enable 0 Bus master 4 reads terminate with an access error and the read is not performed 1 Bus master 4 reads allowed
24 M4WE	Bus Master 4 Write Enable 0 Bus master 4 writes terminate with an access error and the write is not performed 1 Bus master 4 writes allowed
23 M3PE	Bus Master 3 Process Identifier Enable 0 Do not include the process identifier in the evaluation 1 Include the process identifier and mask (RGDn_WORD3) in the region hit evaluation
22–21 M3SM	Bus Master 3 Supervisor Mode Access Control Defines the access controls for bus master 3 in Supervisor mode. 00 r/w/x; read, write and execute allowed 01 r/x; read and execute allowed, but no write 10 r/w; read and write allowed, but no execute 11 Same as User mode defined in M3UM
20–18 M3UM	Bus Master 3 User Mode Access Control Defines the access controls for bus master 3 in User mode. M3UM consists of three independent bits, enabling read (r), write (w), and execute (x) permissions. In M3UM[2:0]: M3UM[2] controls read permissions, M3UM[1] controls write permissions, and M3UM[0] controls execute permissions. 0 An attempted access of that mode may be terminated with an access error (if not allowed by another descriptor) and the access not performed. 1 Allows the given access type to occur
17 M2PE	Bus Master 2 Process Identifier Enable See M3PE description.
16–15 M2SM	Bus Master 2 Supervisor Mode Access Control See M3SM description.
14–12 M2UM	Bus Master 2 User Mode Access control See M3UM description.
11 M1PE	Bus Master 1 Process Identifier enable See M3PE description.

Table continues on the next page...

MPU_RGD*n*_WORD2 field descriptions (continued)

Field	Description
10–9 M1SM	Bus Master 1 Supervisor Mode Access Control See M3SM description.
8–6 M1UM	Bus Master 1 User Mode Access Control See M3UM description.
5 M0PE	Bus Master 0 Process Identifier enable See M0PE description.
4–3 M0SM	Bus Master 0 Supervisor Mode Access Control See M3SM description.
M0UM	Bus Master 0 User Mode Access Control See M3UM description.

23.4.7 Region Descriptor n, Word 3 (MPU_RGD*n*_WORD3)

The fourth word of the region descriptor contains the optional process identifier and mask, plus the region descriptor's valid bit.

Address: 4000_D000h base + 40Ch offset + (16d × i), where i=0d to 11d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PID								PIDMASK							
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															VLD
W																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- Reset value of RGD0_WORD3 is 0000_0001h

  Reset value of RGD[1:12]_WORD3 is 0000_0000h

MPU_RGD*n*_WORD3 field descriptions

Field	Description
31–24 PID	Process Identifier Specifies the process identifier that is included in the region hit determination if RGDn_WORD2[MxPE] is set. PIDMASK can mask individual bits in this field.
23–16 PIDMASK	Process Identifier Mask

Table continues on the next page...

MPU_RGD*n*_WORD3 field descriptions (continued)

Field	Description
	Provides a masking capability so that multiple process identifiers can be included as part of the region hit determination. If a bit in PIDMASK is set, then the corresponding PID bit is ignored in the comparison. This field and PID are included in the region hit determination if RGDn_WORD2[MxPE] is set. For more information on the handling of the PID and PIDMASK, see “Access Evaluation - Hit Determination.”
15–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 VLD	Valid Signals the region descriptor is valid. Any write to RGDn_WORD0–2 clears this bit. 0 Region descriptor is invalid 1 Region descriptor is valid

23.4.8 Region Descriptor Alternate Access Control n (MPU_RGDAAC*n*)

Because software may adjust only the access controls within a region descriptor (RGDn_WORD2) as different tasks execute, an alternate programming view of this 32-bit entity is available. Writing to this register does not affect the descriptor’s valid bit.

Address: 4000_D000h base + 800h offset + (4d × i), where i=0d to 11d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	M7RE	M7WE	M6RE	M6WE	M5RE	M5WE	M4RE	M4WE	M3PE	M3SM		M3UM			M2PE	M2SM
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	M2SM	M2UM			M1PE	M1SM			M1UM			M0PE	M0SM		M0UM	
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- Reset value of RGDAAC0 is 0061_F7DFh

  Reset value of RGDAAC[1:12] is 0000_0000h

MPU_RGDAAC*n* field descriptions

Field	Description
31 M7RE	Bus Master 7 Read Enable 0 Bus master 7 reads terminate with an access error and the read is not performed 1 Bus master 7 reads allowed
30 M7WE	Bus Master 7 Write Enable 0 Bus master 7 writes terminate with an access error and the write is not performed 1 Bus master 7 writes allowed
29 M6RE	Bus Master 6 Read Enable 0 Bus master 6 reads terminate with an access error and the read is not performed 1 Bus master 6 reads allowed
28 M6WE	Bus Master 6 Write Enable 0 Bus master 6 writes terminate with an access error and the write is not performed 1 Bus master 6 writes allowed
27 M5RE	Bus Master 5 Read Enable 0 Bus master 5 reads terminate with an access error and the read is not performed 1 Bus master 5 reads allowed
26 M5WE	Bus Master 5 Write Enable 0 Bus master 5 writes terminate with an access error and the write is not performed 1 Bus master 5 writes allowed
25 M4RE	Bus Master 4 Read Enable 0 Bus master 4 reads terminate with an access error and the read is not performed 1 Bus master 4 reads allowed
24 M4WE	Bus Master 4 Write Enable 0 Bus master 4 writes terminate with an access error and the write is not performed 1 Bus master 4 writes allowed
23 M3PE	Bus Master 3 Process Identifier Enable 0 Do not include the process identifier in the evaluation 1 Include the process identifier and mask (RGDn.RGDAAC) in the region hit evaluation
22–21 M3SM	Bus Master 3 Supervisor Mode Access Control Defines the access controls for bus master 3 in Supervisor mode. 00 r/w/x; read, write and execute allowed 01 r/x; read and execute allowed, but no write 10 r/w; read and write allowed, but no execute 11 Same as User mode defined in M3UM
20–18 M3UM	Bus Master 3 User Mode Access Control Defines the access controls for bus master 3 in user mode. M3UM consists of three independent bits, enabling read (r), write (w), and execute (x) permissions. In M3UM[2:0]: M3UM[2] controls read permissions, M3UM[1] controls write permissions, and M3UM[0] controls execute permissions.

Table continues on the next page...

MPU_RGDAAC*n* field descriptions (continued)

Field	Description
	0 An attempted access of that mode may be terminated with an access error (if not allowed by another descriptor) and the access not performed. 1 Allows the given access type to occur
17 M2PE	Bus Master 2 Process Identifier Enable See M3PE description.
16–15 M2SM	Bus Master 2 Supervisor Mode Access Control See M3SM description.
14–12 M2UM	Bus Master 2 User Mode Access Control See M3UM description.
11 M1PE	Bus Master 1 Process Identifier Enable See M3PE description.
10–9 M1SM	Bus Master 1 Supervisor Mode Access Control See M3SM description.
8–6 M1UM	Bus Master 1 User Mode Access Control See M3UM description.
5 M0PE	Bus Master 0 Process Identifier Enable See M3PE description.
4–3 M0SM	Bus Master 0 Supervisor Mode Access Control See M3SM description.
M0UM	Bus Master 0 User Mode Access Control See M3UM description.

23.5 Functional description

In this section, the functional operation of the MPU is detailed, including the operation of the access evaluation macro and the handling of error-terminated bus cycles.

23.5.1 Access evaluation macro

The basic operation of the MPU is performed in the access evaluation macro, a hardware structure replicated in the two-dimensional connection matrix. As shown in the following figure, the access evaluation macro inputs the crossbar bus address phase signals and the contents of a region descriptor (RGD*n*) and performs two major functions:

- Region hit determination
- Detection of an access protection violation

The following figure shows a functional block diagram.

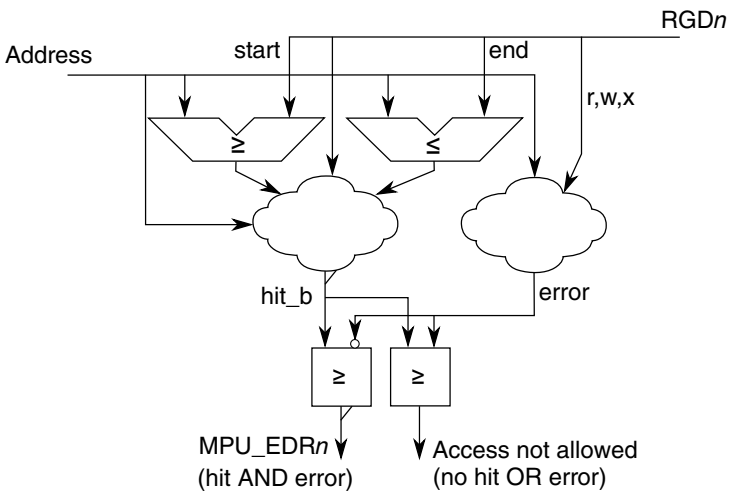


Figure 23-2. MPU access evaluation macro

23.5.1.1 Hit determination

To determine whether the current reference hits in the given region, two magnitude comparators are used with the region's start and end addresses. The boolean equation for this portion of the hit determination is:

```
region_hit = ((addr[31:5] >= RGDn_Word0[SRTADDR]) & (addr[31:5] <= RGDn_Word1[ENDADDR])) &
RGDn_Word3[VLD]
```

where addr is the current reference address, RGD*n*_Word0[SRTADDR] and RGD*n*_Word1[ENDADDR] are the start and end addresses, and RGD*n*_Word3[VLD] is the valid bit.

NOTE

The MPU does not verify that ENDADDR ≥ SRTADDR.

In addition to the comparison of the reference address versus the region descriptor's start and end addresses, the optional process identifier is examined against the region descriptor's PID and PIDMASK fields. A process identifier hit term is formed as follows:

```
pid_hit = ~RGDn_Word2[MxPE] |
          ((current_pid |
          RGDn_Word3[PIDMASK]) == (RGDn_Word3[PID] | RGDn_Word3[PIDMASK]))
```

where the current_pid is the selected process identifier from the current bus master, and RGD*n*_Word3[PID] and RGD*n*_Word3[PIDMASK] are the process identifier fields from region descriptor *n*. For bus masters that do not output a process identifier, the MPU forces the pid_hit term to assert.

23.5.1.2 Privilege violation determination

While the access evaluation macro is determining region hit, the logic is also evaluating if the current access is allowed by the permissions defined in the region descriptor. Using the master and supervisor/user mode signals, a set of effective permissions is generated from the appropriate fields in the region descriptor. The protection violation logic then evaluates the access against the effective permissions using the specification shown below.

Table 23-5. Protection violation definition

Description	MxUM			Protection violation?
	r	w	x	
Instruction fetch read	—	—	0	Yes, no execute permission
	—	—	1	No, access is allowed
Data read	0	—	—	Yes, no read permission
	1	—	—	No, access is allowed
Data write	—	0	—	Yes, no write permission
	—	1	—	No, access is allowed

23.5.2 Putting it all together and error terminations

For each slave port monitored, the MPU performs a reduction-AND of all the individual terms from each access evaluation macro. This expression then terminates the bus cycle with an error and reports a protection error for three conditions:

- If the access does not hit in any region descriptor, a protection error is reported.
- If the access hits in a single region descriptor and that region signals a protection violation, a protection error is reported.
- If the access hits in multiple (overlapping) regions and all regions signal protection violations, a protection error is reported.

As shown in the third condition, granting permission is a higher priority than denying access for overlapping regions. This approach is more flexible to system software in region descriptor assignments. For an example of the use of overlapping region descriptors, see Application information.

23.5.3 Power management

Disabling the MPU by clearing CESR[VLD] minimizes power dissipation. To minimize the power dissipation of an enabled MPU, invalidate unused region descriptors by clearing the associated RGDn_Word3[VLD] bits.

23.6 Initialization information

At system startup, load the appropriate number of region descriptors, including setting RGD*n*_Word3[VLD]. Setting CESR[VLD] enables the module.

If the system requires that all the loaded region descriptors be enabled simultaneously, first ensure that the entire MPU is disabled (CESR[VLD]=0).

Note

A region descriptor must be set to allow access to the MPU registers if further changes are needed.

23.7 Application information

In an operational system, interfacing with the MPU is generally classified into the following activities:

- Creating a new memory region—Load the appropriate region descriptor into an available RGD*n*, using four sequential 32-bit writes. The hardware assists in the maintenance of the valid bit, so if this approach is followed, there are no coherency issues with the multi-cycle descriptor writes. (Clearing RGD*n*_Word3[VLD] deletes/removes an existing memory region.)
- Altering only access privileges—To not affect the valid bit, write to the alternate version of the access control word (RGDAAC*n*), so there are no coherency issues involved with the update. When the write completes, the memory region's access rights switch instantaneously to the new value.

- Changing a region's start and end addresses—Write a minimum of three words to the region descriptor (RGD*n*_Word{0,1,3}). Word 0 and 1 redefine the start and end addresses, respectively. Word 3 re-enables the region descriptor valid bit. In most situations, all four words of the region descriptor are rewritten.
- Accessing the MPU—Allocate a region descriptor to restrict MPU access to supervisor mode from a specific master.
- Detecting an access error—The current bus cycle is terminated with an error response and EAR*n* and EDR*n* capture information on the faulting reference. The error-terminated bus cycle typically initiates an error response in the originating bus master. For example, a processor core may respond with a bus error exception, while a data movement bus master may respond with an error interrupt. The processor can retrieve the captured error address and detail information simply by reading E{A,D}R*n*. CESR[SPERR] signals which error registers contain captured fault data.
- Overlapping region descriptors—Applying overlapping regions often reduces the number of descriptors required for a given set of access controls. In the overlapping memory space, the protection rights of the corresponding region descriptors are logically summed together (the boolean OR operator).

  The following dual-core system example contains four bus masters:

  - The two processors: CP0, CP1
  - Two DMA engines: DMA1, a traditional data movement engine transferring data between RAM and peripherals and DMA2, a second engine transferring data to/from the RAM only

  Consider the following region descriptor assignments:

Table 23-6. Overlapping region descriptor example

Region description	RGDn		CP0	CP1	DMA1	DMA2	
CP0 code	0		rwx	r--	—	—	Flash
CP1 code	1		r--	rwx	—	—	
CP0 data & stack	2		rw-	—	—	—	RAM
CP0 → CP1 shared data	2	3	r--	r--	—	—	
CP1 → CP0 shared data	4						
CP1 data & stack	4		—	rw-	—	—	
Shared DMA data	5		rw-	rw-	rw	rw	
MPU	6		rw-	rw-	—	—	Peripheral space
Peripherals	7		rw-	rw-	rw	—	

In this example, there are eight descriptors used to span nine regions in the three main spaces of the system memory map: flash, RAM, and peripheral space. Each region indicates the specific permissions for each of the four bus masters and this definition provides an appropriate set of shared, private and executable memory spaces.

Of particular interest are the two overlapping spaces: region descriptors 2 & 3 and 3 & 4.

The space defined by RGD2 with no overlap is a private data and stack area that provides read/write access to CP0 only. The overlapping space between RGD2 and RGD3 defines a shared data space for passing data from CP0 to CP1 and the access controls are defined by the logical OR of the two region descriptors. Thus, CP0 has (rw- | r--) = (rw-) permissions, while CP1 has (--- | r--) = (r--) permission in this space. Both DMA engines are excluded from this shared processor data region. The overlapping spaces between RGD3 and RGD4 defines another shared data space, this one for passing data from CP1 to CP0. For this overlapping space, CP0 has (r-- | ---) = (r--) permission, while CP1 has (rw- | r--) = (rw-) permission. The non-overlapped space of RGD4 defines a private data and stack area for CP1 only.

The space defined by RGD5 is a shared data region, accessible by all four bus masters. Finally, the slave peripheral space mapped onto the IPS bus is partitioned into two regions:

- One containing the MPU's programming model accessible only to the two processor cores
- The remaining peripheral region accessible to both processors and the traditional DMA1 master

This example shows one possible application of the capabilities of the MPU in a typical system.

Chapter 24
Bit Manipulation Engine2 (BME2)

24.1 Introduction

The Bit Manipulation Engine with the BME2 definition (BME2) provides hardware support for atomic read-modify-write memory operations to the first 1 Mbyte of slave peripheral address space in Cortex-M based microcontrollers. The second generation BME2 provides similar atomic read-modify-write capabilities to a larger peripheral address space versus the original implementation. The BME terminology is meant to be equivalent to BME2 throughout this chapter.

This architectural capability is also known as "decorated storage" as it defines a mechanism for providing additional semantics for load and store operations to memory-mapped peripherals beyond just the reading and writing of data values to the addressed memory locations. In the BME definition, the "decoration", that is, the additional semantic information, is encoded into the peripheral address used to reference the memory. The BME2 definition supports up to two AIPS bus controllers, each capable of addressing 512 KB of peripheral address space. BME2 supports an 8-bit or less data field width for bit field inserts and extracts, regardless of reference size. All other BME2 operations are exactly the same as the original definition.

By combining the basic load and store instructions of the ARM Cortex-M instruction set architecture (v6M, v7M) with the concept of decorated storage provided by BME, the resulting implementation provides a robust and efficient read-modify-write capability. The resulting architectural capability defined by this core platform function is targeted at the manipulation of n-bit fields in peripheral registers and is consistent with I/O hardware addressing in the Embedded C standard. For most BME commands, a single core read or write bus cycle is converted into an atomic read-modify-write, that is, an indivisible "read followed by a write" bus sequence.

BME decorated references are only available on system bus transactions generated by the processor core, DMA and M2B, and targeted at the 1024 KB peripheral address space based at 0x4000_0000. The decoration semantic is embedded into address bits[28:20],

creating a 448 MB space at addresses 0x4400_0000–0x5FFF_FFFF; these bits are stripped out of the actual address sent to the peripheral bus controller and used by the BME to define and control its operation.

24.1.1 Overview

The following figure is a generic block diagram of the processor core and platform of the Cortex-M4 microcontroller.

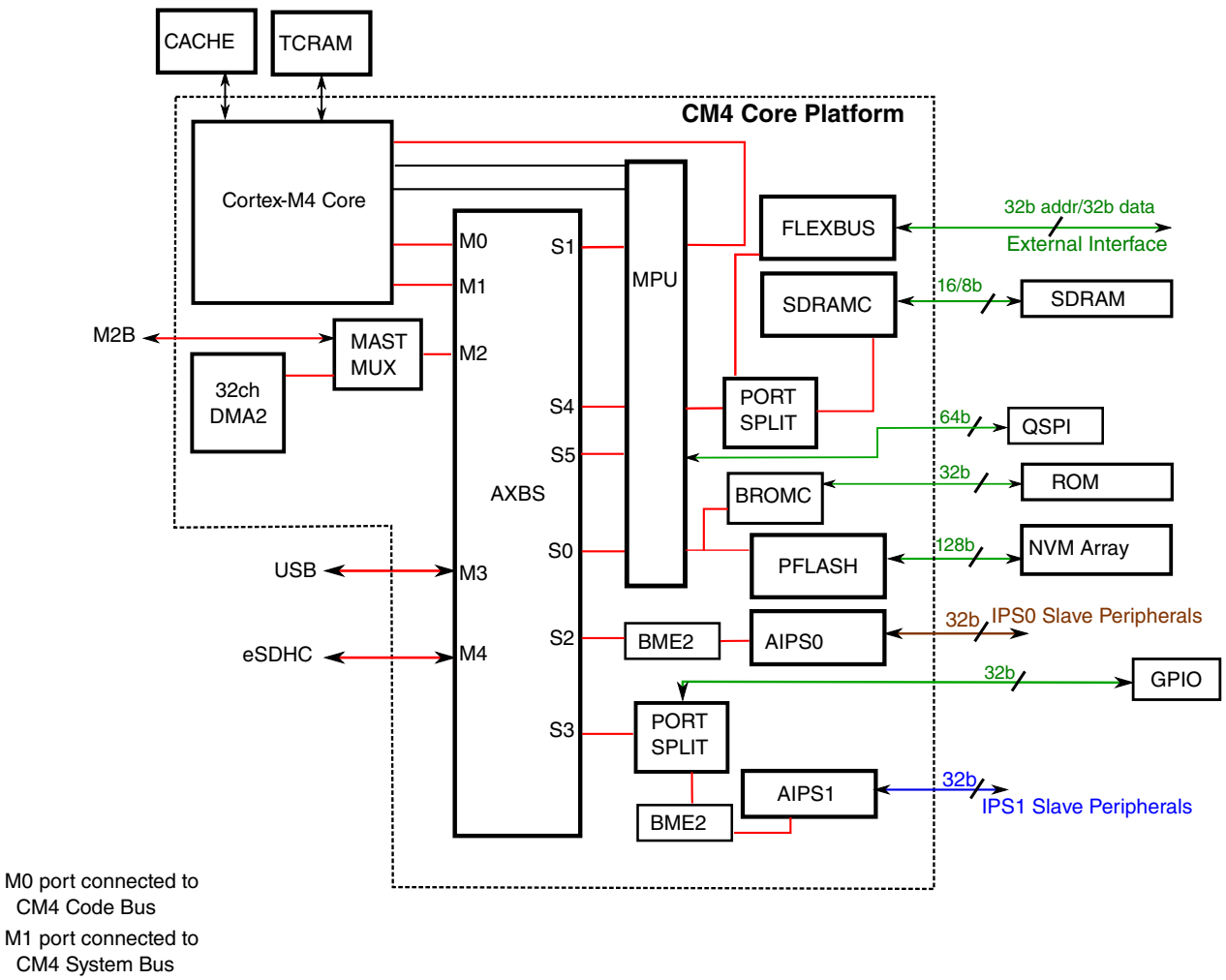


Figure 24-1. Cortex-M4 core platform block diagram

As shown in the block diagram, the BME modules interface to two AHB slave ports on the crossbar switch, thereby allowing them to support atomic read-modify-write operations to the two AIPS controllers. The BME hardware microarchitecture is a 2-stage

pipeline design matching the protocol of the AMBA-AHB system bus interfaces. The AIPS modules convert the AHB system bus protocol into the IPS/APB protocol used by the attached slave peripherals.

24.1.2 Features

The key features of the BME2 include:

- Lightweight implementation of decorated storage for selected address spaces
- Additional access semantics encoded into the reference address
- Resides between crossbar switch slave port(s) and their associated peripheral bridge bus controller(s)
- Two-stage pipeline design matching the AHB system bus protocol
- Combinationally passes non-decorated accesses to peripheral bridge bus controllers
- Conversion of decorated loads and stores from processor core into atomic read-modify-writes
- Decorated loads support unsigned bit field extracts, load-and-{set,clear} 1-bit operations
- Decorated stores support bit field inserts, logical AND, OR, and XOR operations
- Support for byte, halfword and word-sized decorated operations
- Supports minimum signal toggling on AHB output bus to reduce power dissipation

24.1.3 Modes of operation

The BME modules do not support any special modes of operation. As memory-mapped devices located on crossbar slave AHB system bus ports, BME responds strictly on the basis of memory addresses for accesses to the AIPS controllers.

All functionality associated with the BME modules reside in the core platform's clock domain; this includes their connections with the crossbar slave ports and the AIPS controllers.

24.2 Memory map and register definition

The BME module provides a memory-mapped capability and does not include any programming model registers.

The exact set of functions supported by the BME are detailed in the Functional description.

The generic BME2 definition supports a 1024 KB address space based at 0x4000_0000. For the K80_256 device, the upper 16 KB of this address space is not supported, so the BME2 functionality covers the (512 + 512 - 16 = 1008) KB space at 0x4000_0000 - 0x400F_BFFF. The decorated address space is mapped to the 448 MB region located at 0x4400_0000–0x5FFF_FFFF.

24.3 Functional description

Information found here details the specific functions supported by the BME.

Recall the combination of the basic load and store instructions of the Cortex-M instruction set architecture (v6M, v7M) plus the concept of decorated storage provided by the BME provides a robust and efficient read-modify-write capability. The resulting architectural capability defined by this core platform function is targeted at the manipulation of n-bit fields in peripheral registers and is consistent with I/O hardware addressing in the Embedded C standard. For most BME commands, a single core read or write bus cycle is converted into an atomic read-modify-write, that is, an indivisible "read followed by a write" bus sequence.

Consider decorated store operations first, then decorated loads.

24.3.1 BME decorated stores

The functions supported by the BME's decorated stores include three logical operators (AND, OR, XOR) plus a bit field insert.

For all these operations, BME converts a single decorated AHB store transaction into a 2-cycle atomic read-modify-write sequence, where the combined read-modify operation is performed in the first AHB data phase, and then the write is performed in the second AHB data phase.

A generic timing diagram of a decorated store showing a peripheral bit field insert operation is shown as follows:

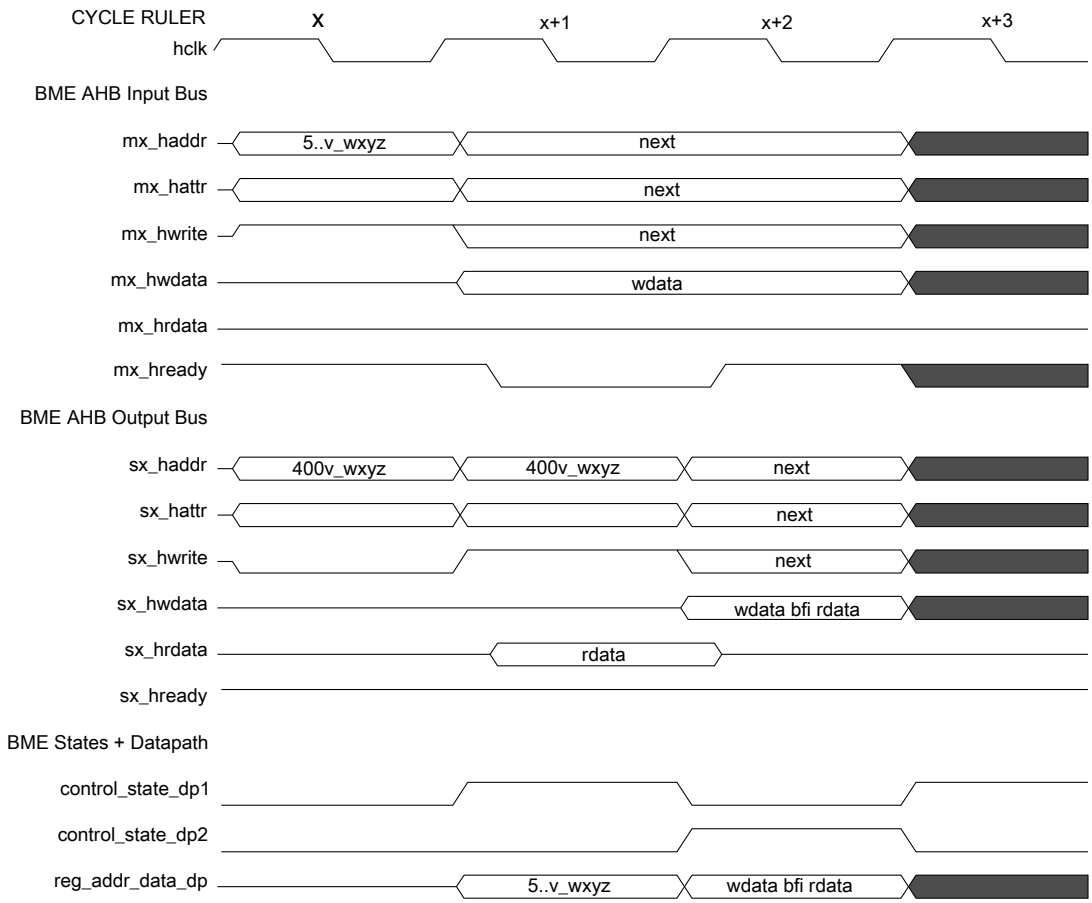


Figure 24-2. Decorated store: bit field insert timing diagram

All the decorated store operations follow the same execution template shown in Figure 24-2, a two-cycle read-modify-write operation:

1. Cycle x, 1st AHB address phase: Write from input bus is translated into a read operation on the output bus using the actual memory address (with the decoration removed) and then captured in a register.
2. Cycle x+1, 2nd AHB address phase: Write access with the registered (but actual) memory address is output
3. Cycle x+1, 1st AHB data phase: Memory read data is modified using the input bus write data and the function defined by the decoration and captured in a data register; the input bus cycle is stalled.
4. Cycle x+2, 2nd AHB data phase: Registered write data is sourced onto the output write data bus.

NOTE

Any wait states inserted by the slave device are simply passed through the BME back to the master input bus, stalling the AHB transaction cycle for cycle.

24.3.1.1 Decorated store logical AND (AND)

This command performs an atomic read-modify-write of the referenced memory location.

1. First, the location is read;
2. It is then modified by performing a logical AND operation using the write data operand sourced for the system bus cycle
3. Finally, the result of the AND operation is written back into the referenced memory location.

The data size is specified by the write operation and can be byte (8-bit), halfword (16-bit) or word (32-bit). The core performs the required write data lane replication on byte and halfword transfers.

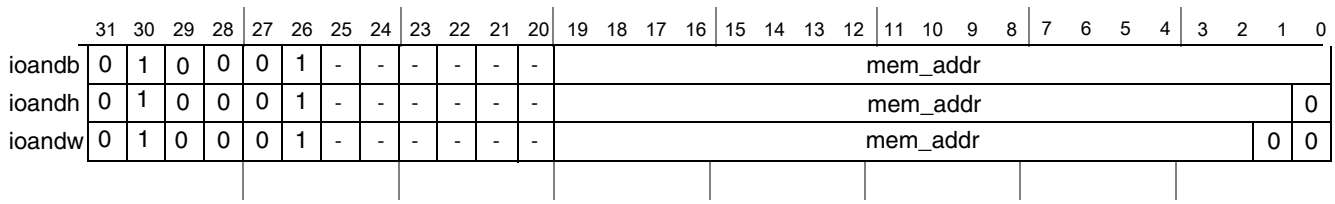


Figure 24-3. Decorated store address: logical AND

See Figure 24-3 where addr[30:29] = 10 for peripheral, addr[28:26] = 001 specifies the AND operation, and mem_addr[19:0] specifies the address offset into the space based at a 0x4000_0000 for peripherals. The "-" indicates an address bit "don't care".

The decorated AND write operation is defined in the following pseudo-code as:

```
ioand<sz>(accessAddress, wdata)                  // decorated store AND
tmp    =  mem[accessAddress & 0xE00FFFFF, size]  // memory read
tmp    =  tmp & wdata                            // modify
mem[accessAddress & 0xE00FFFFF, size] = tmp      // memory write
```

where the operand size <sz> is defined as b(yte, 8-bit), h(alfword, 16-bit) and w(ord, 32-bit). This notation is used throughout the document.

In the cycle definition tables, the notations AHB_ap and AHB_dp refer to the address and data phases of the BME AHB transaction. The cycle-by-cycle BME operations are detailed in the following table.

Table 24-1. Cycle definitions of decorated store: logical AND

Pipeline stage	Cycle		
	x	x+1	x+2
BME AHB_ap	Forward addr to memory; Decode decoration; Convert	Recirculate captured addr + attr to memory as slave_wt	<next>

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Table 24-1. Cycle definitions of decorated store: logical AND (continued)

Pipeline stage	Cycle		
	x	x+1	x+2
	master_wt to slave_rd; Capture address, attributes		
BME AHB_dp	<previous>	Perform memory read; Form (rdata & wdata) and capture destination data in register	Perform write sending registered data to memory

24.3.1.2 Decorated store logical OR (OR)

This command performs an atomic read-modify-write of the referenced memory location.

1. First, the location is read.
2. It is then modified by performing a logical OR operation using the write data operand sourced for the system bus cycle.
3. Finally, the result of the OR operation is written back into the referenced memory location.

The data size is specified by the write operation and can be byte (8-bit), halfword (16-bit) or word (32-bit). The core performs the required write data lane replication on byte and halfword transfers.

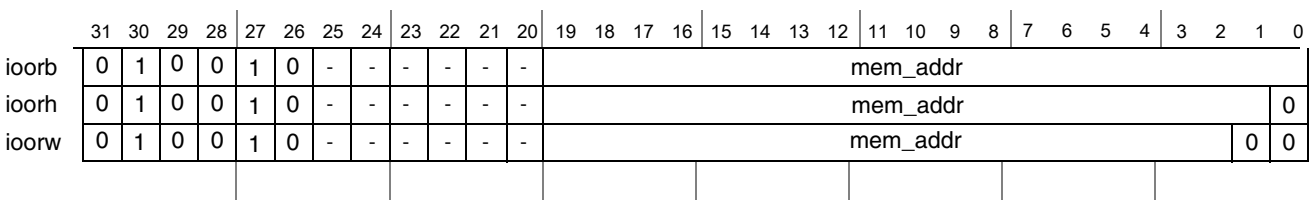


Figure 24-4. Decorated address store: logical OR

See Figure 24-4,where addr[30:29] =10 for peripheral, addr[28:26] = 010 specifies the OR operation, and mem_addr[19:0] specifies the address offset into the space based at a 0x4000_0000 for peripherals. The "-" indicates an address bit "don't care".

The decorated OR write operation is defined in the following pseudo-code as:

```
ioor<sz>(accessAddress, wdata)                  // decorated store OR

tmp    =  mem[accessAddress & 0xE00FFFFF, size]  // memory read
tmp    =  tmp | wdata                            // modify
mem[accessAddress & 0xE00FFFFF, size] = tmp      // memory write
```

The cycle-by-cycle BME operations are detailed in the following table.

Table 24-2. Cycle definitions of decorated store: logical OR

Pipeline stage	Cycle		
	x	x+1	x+2
BME AHB_ap	Forward addr to memory; Decode decoration; Convert master_wt to slave_rd; Capture address, attributes	Recirculate captured addr + attr to memory as slave_wt	<next>
BME AHB_dp	<previous>	Perform memory read; Form (rdata | wdata) and capture destination data in register	Perform write sending registered data to memory

24.3.1.3 Decorated store logical XOR (XOR)

This command performs an atomic read-modify-write of the referenced memory location.

1. First, the location is read.
2. It is then modified by performing a logical XOR (exclusive-OR) operation using the write data operand sourced for the system bus cycle.
3. Finally, the result of the XOR operation is written back into the referenced memory location.

The data size is specified by the write operation and can be byte (8-bit), halfword (16-bit) or word (32-bit). The core performs the required write data lane replication on byte and halfword transfers.

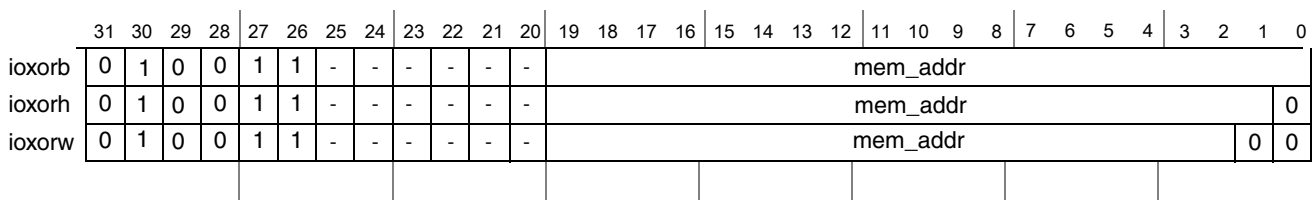


Figure 24-5. Decorated address store: logical XOR

See Figure 24-5, where addr[30:29] =10 for peripheral, addr[28:26] = 011 specifies the XOR operation, and mem_addr[19:0] specifies the address offset into the peripheral space based at a 0x4000_0000 for peripherals. The "-" indicates an address bit "don't care".

The decorated XOR write operation is defined in the following pseudo-code as:

```
ioxor<sz>(accessAddress, wdata)                  // decorated store XOR

tmp    =  mem[accessAddress & 0xE00FFFFF, size]  // memory read
tmp    =  tmp ^ wdata                            // modify
mem[accessAddress & 0xE00FFFFF, size] = tmp      // memory write
```

The cycle-by-cycle BME operations are detailed in the following table.

Table 24-3. Cycle definitions of decorated store: logical XOR

Pipeline Stage	Cycle		
	x	x+1	x+2
BME AHB_ap	Forward addr to memory; Decode decoration; Convert master_wt to slave_rd; Capture address, attributes	Recirculate captured addr + attr to memory as slave_wt	<next>
BME AHB_dp	<previous>	Perform memory read; Form (rdata ^ wdata) and capture destination data in register	Perform write sending registered data to memory

24.3.1.4 Decorated store bit field insert (BFI)

This command inserts a bit field contained in the write data operand, defined by LSB position (b) and the bit field width (w+1), into the memory "container" defined by the access size associated with the store instruction using an atomic read-modify-write sequence.

The data size is specified by the write operation and can be byte (8-bit), halfword (16-bit) or word (32-bit). For BME2, the data field width (addr[22:20]) for bit field inserts and extracts is limited to an 8-bit or less value, regardless of reference size.

NOTE

The maximum bit field width is 8 bits. The core performs the required write data lane replication on byte and halfword transfers.

The BFI operation can be used to insert a single bit into a peripheral. For this case, the w field is simply set to 0, indicating a bit field width of 1.

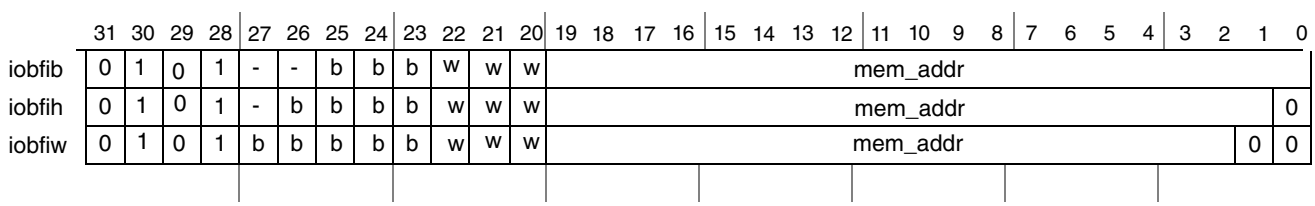


Figure 24-6. Decorated address store: bit field insert

where addr[30:29] =10 for peripheral, addr[28] = 1 signals a BFI operation, addr[27:23] is "b", the LSB identifier, addr[22:20] is "w", the bit field width minus 1 identifier, and addr[19:0] specifies the address offset into the peripheral space based at 0x4000_0000. The "-" indicates an address bit "don't care".

The decorated BFI write operation is defined in the following pseudo-code as:

```
iobfi<sz>(accessAddress, wdata)                  // decorated bit field insert

tmp    =  mem[accessAddress & 0xE00FFFFF, size]  // memory read
mask   = ((1 << (w+1)) - 1) << b                 // generate bit mask
tmp    =  tmp    & ~mask                         // modify
       |  wdata &  mask
mem[accessAddress & 0xE00FFFFF, size] = tmp      // memory write
```

The write data operand (wdata) associated with the store instruction contains the bit field to be inserted. It must be properly aligned within the right-aligned container, that is, within the lower 8 bits for a byte operation, the lower 16 bits for a halfword, or the entire 32 bits for a word operation.

To illustrate, consider the following example of the insertion of the 3-bit field "xyz" into an 8-bit memory container, initially set to "abcd_efgh". For all cases, w is 2, signaling a bit field width of 3.

```
if b = 0 and the decorated store (strb) Rt register[7:0] = ----_-xyz,
   then destination is "abcd_exyz"
if b = 1 and the decorated store (strb) Rt register[7:0] = ----_xyz-,
   then destination is "abcd_xyzh"
if b = 2 and the decorated store (strb) Rt register[7:0] = ---x_yz--,
   then destination is "abcx_yzgh"
if b = 3 and the decorated store (strb) Rt register[7:0] = --xy_z---,
   then destination is "abxy_zfgh"
if b = 4 and the decorated store (strb) Rt register[7:0] = -xyz_----,
   then destination is "axyz_efgh"
if b = 5 and the decorated store (strb) Rt register[7:0] = xyz-_----,
   then destination is "xyzd_efgh"
if b = 6 and the decorated store (strb) Rt register[7:0] = yz--_----,
   then destination is "yzcd_efgh"
if b = 7 and the decorated store (strb) Rt register[7:0] = z---_----,
   then destination is "zbcd_efgh"
```

Note from the example, when the starting bit position plus the field width exceeds the container size, only part of the source bit field is inserted into the destination memory location. Stated differently, if (b + w+1) > container_width, only the low-order "container_width - b" bits are actually inserted.

The cycle-by-cycle BME operations are detailed in the following table.

Table 24-4. Cycle definitions of decorated store: bit field insert

Pipeline stage	Cycle		
	x	x+1	x+2
BME AHB_ap	Forward addr to memory; Decode decoration; Convert master_wt to slave_rd; Capture address, attributes	Recirculate captured addr + attr to memory as slave_wt	<next>
BME AHB_dp	<previous>	Perform memory read; Form bit mask; Form bitwise ((mask) ? wdata : rdata)) and capture destination data in register	Perform write sending registered data to memory

24.3.2 BME decorated loads

The functions supported by the BME's decorated loads include two single-bit load-and-{set, clear} operators plus unsigned bit field extracts.

For the two load-and-{set, clear} operations, BME converts a single decorated AHB load transaction into a two-cycle atomic read-modify-write sequence, where the combined read-modify operations are performed in the first AHB data phase, and then the write is performed in the second AHB data phase as the original read data is returned to the processor core. For an unsigned bit field extract, the decorated load transaction is stalled for one cycle in the BME as the data field is extracted, then aligned and returned to the processor in the second AHB data phase. This is the only decorated transaction that is not an atomic read-modify-write, as it is a simple data read.

A generic timing diagram of a decorated load showing a peripheral load-and-set 1-bit operation is shown as follows.

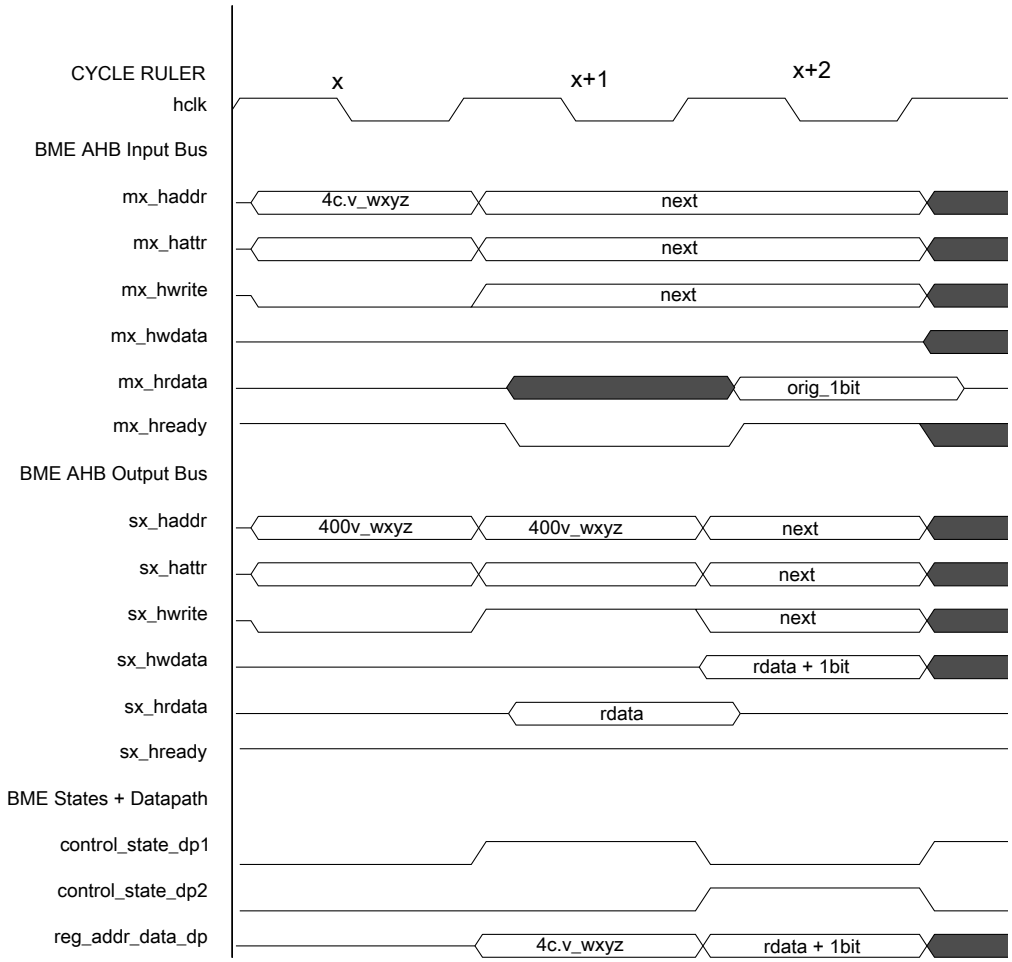


Figure 24-7. Decorated load: load-and-set 1-bit field insert timing diagram

Decorated load-and-{set, clear} 1-bit operations follow the execution template shown in the above figure: a 2-cycle read-modify-write operation:

1. Cycle x, first AHB address phase: Read from input bus is translated into a read operation on the output bus with the actual memory address (with the decoration removed) and then captured in a register
2. Cycle x+1, second AHB address phase: Write access with the registered (but actual) memory address is output
3. Cycle x+1, first AHB data phase: The "original" 1-bit memory read data is captured in a register, while the 1-bit field is set or clear based on the function defined by the decoration with the modified data captured in a register; the input bus cycle is stalled
4. Cycle x+2, second AHB data phase: The selected original 1-bit is right-justified, zero-filled and then driven onto the input read data bus, while the registered write data is sourced onto the output write data bus

NOTE

Any wait states inserted by the slave device are simply passed through the BME back to the master input bus, stalling the AHB transaction cycle for cycle.

A generic timing diagram of a decorated load showing an unsigned peripheral bit field operation is shown in the following figure.

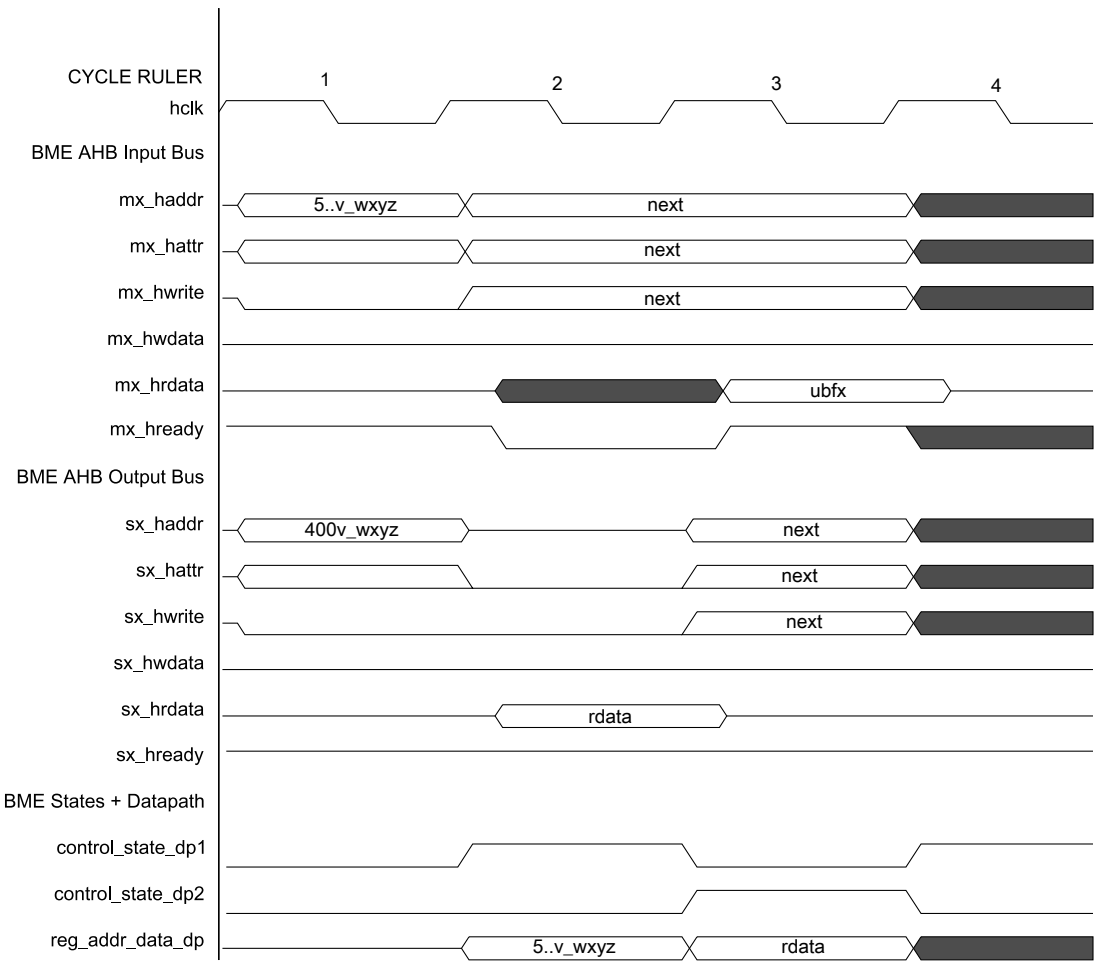


Figure 24-8. Decorated load: unsigned bit field insert timing diagram

The decorated unsigned bit field extract follows the same execution template shown in the above figure, a 2-cycle read operation:

- Cycle x, 1st AHB address phase: Read from input bus is translated into a read operation on the output bus with the actual memory address (with the decoration removed) and then captured in a register
- Cycle x+1, 2nd AHB address phase: Idle cycle

- Cycle x+1, 1st AHB data phase: A bit mask is generated based on the starting bit position and the field width; the mask is AND'ed with the memory read data to isolate the bit field; the resulting data is captured in a data register; the input bus cycle is stalled
- Cycle x+2, 2nd AHB data phase: Registered data is logically right-aligned for proper alignment and driven onto the input read data bus

NOTE

Any wait states inserted by the slave device are simply passed through the BME back to the master input bus, stalling the AHB transaction cycle for cycle.

24.3.2.1 Decorated load: load-and-clear 1 bit (LAC1)

This command loads a 1-bit field defined by the LSB position (b) into the core's general purpose destination register (Rt) and zeroes the bit in the memory space after performing an atomic read-modify-write sequence.

The extracted 1-bit data field from the memory address is right-justified and zero-filled in the operand returned to the core.

The data size is specified by the read operation and can be byte (8-bit), halfword (16-bit) or word (32-bit).

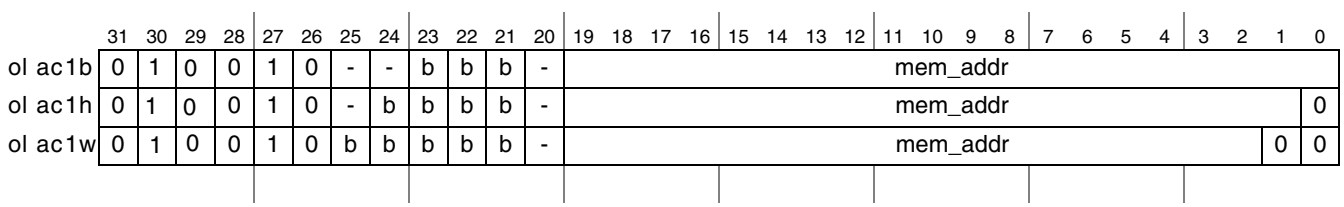


Figure 24-9. Decorated load address: load-and-clear 1 bit

See Figure 24-9 where addr[30:29] = 10 for peripherals, addr[28:26] = 010 specifies the load-and-clear 1 bit operation, addr[25:21] is "b", the bit identifier, and mem_addr[19:0] specifies the address offset into the space based at 0x4000_0000 for peripherals. The "-" indicates an address bit "don't care".

The decorated load-and-clear 1-bit read operation is defined in the following pseudo-code as:

```
rdata =  iolac1<sz>(accessAddress)              // decorated load-and-clear 1

tmp   =  mem[accessAddress & 0xE00FFFFF, size]  // memory read
mask  =  1 << b                                 // generate bit mask
rdata = (tmp &  mask) >> b                      // read data returned to core
tmp   =  tmp & ~mask                            // modify
mem[accessAddress & 0xE00FFFFF, size] = tmp     // memory write
```

The cycle-by-cycle BME operations are detailed in the following table.

Table 24-5. Cycle definitions of decorated load: load-and-clear 1 bit

Pipeline Stage	Cycle		
	x	x+1	x+2
BME AHB_ap	Forward addr to memory; Decode decoration; Capture address, attributes	Recirculate captured addr + attr to memory as slave_wt	<next>
BME AHB_dp	<previous>	Perform memory read; Form bit mask; Extract bit from rdata; Form (rdata & ~mask) and capture destination data in register	Return extracted bit to master; Perform write sending registered data to memory

24.3.2.2 Decorated Load: Load-and-Set 1 Bit (LAS1)

This command loads a 1-bit field defined by the LSB position (b) into the core's general purpose destination register (Rt) and sets the bit in the memory space after performing an atomic read-modify-write sequence.

The extracted one bit data field from the memory address is right justified and zero filled in the operand returned to the core.

The data size is specified by the read operation and can be byte (8-bit), halfword (16-bit) or word (32-bit).

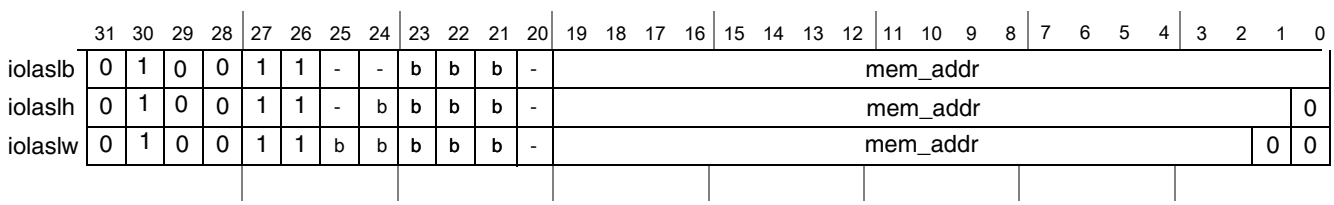


Figure 24-10. Decorated load address: load-and-set 1 bit

where addr[30:29] = 10 for peripherals, addr[28:26] = 011 specifies the load-and-set 1 bit operation, addr[25:21] is "b", the bit identifier, and mem_addr[19:0] specifies the address offset into the space based at 0x4000_0000 for peripherals. The "-" indicates an address bit "don't care".

The decorated Load-and-Set 1 Bit read operation is defined in the following pseudo-code as:

```
rdata =  iolas1<sz>(accessAddress)              // decorated load-and-set 1

tmp   =  mem[accessAddress & 0xE00FFFFF, size]  // memory read
mask  =  1 << b                                 // generate bit mask
rdata = (tmp &  mask) >> b                      // read data returned to core
```

```
tmp    =  tmp |  mask                              // modify
mem[accessAddress & 0xE00FFFFF, size] = tmp       // memory write
```

The cycle-by-cycle BME operations are detailed in the following table.

Table 24-6. Cycle definitions of decorated load: load-and-set 1-bit

Pipeline Stage	Cycle		
	x	x+1	x+2
BME AHB_ap	Forward addr to memory; Decode decoration; Capture address, attributes	Recirculate captured addr + attr to memory as slave_wt	<next>
BME AHB_dp	<previous>	Perform memory read; Form bit mask; Extract bit from rdata; Form (rdata | mask) and capture destination data in register	Return extracted bit to master; Perform write sending registered data to memory

24.3.2.3 Decorated load unsigned bit field extract (UBFX)

This command extracts a bit field defined by LSB position (b) and the bit field width (w +1) from the memory "container" defined by the access size associated with the load instruction using a two-cycle read sequence.

The extracted bit field from the memory address is right-justified and zero-filled in the operand returned to the core. Recall this is the only decorated operation that does not perform a memory write, that is, UBFX only performs a read.

The data size is specified by the read operation and can be byte (8-bit), halfword (16-bit) or word (32-bit). The maximum bit field width is 8 bits, regardless of reference size.

The use of a UBFX operation is recommended to extract a single bit. For this case, the w field is simply set to 0, indicating a bit field width of 1.

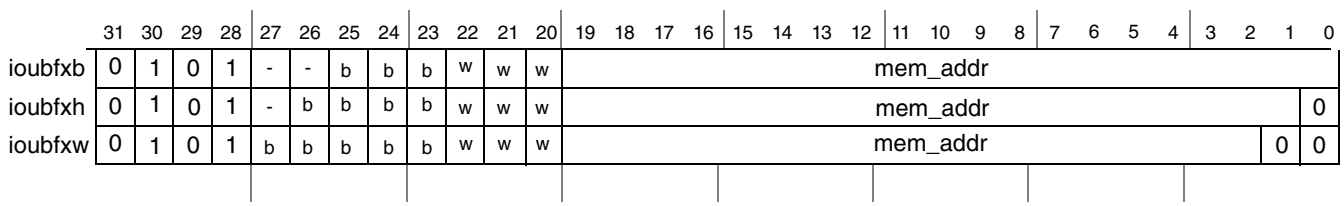


Figure 24-11. Decorated load address: unsigned bit field extract

See Figure 24-11, where addr[30:29] = 10 for peripherals, addr[28] = 1 specifies the unsigned bit field extract operation, addr[27:23] is "b", the LSB identifier, addr[22:20] is "w", the bit field width minus 1 identifier, and mem_addr[19:0] specifies the address offset into the space based at 0x4000_0000 for peripherals. The "-" indicates an address bit "don't care".

The decorated unsigned bit field extract read operation is defined in the following pseudo-code as:

```
rdata =  ioubfx<sz>(accessAddress)              // unsigned bit field extract

tmp   =  mem[accessAddress & 0xE00FFFFF, size]  // memory read
mask  = ((1 << (w+1)) - 1) << b                 // generate bit mask
rdata = (tmp &  mask) >> b                      // read data returned to core
```

Like the BFI operation, when the starting bit position plus the field width exceeds the container size, only part of the source bit field is extracted from the destination memory location. Stated differently, if (b + w+1) > container_width, only the low-order "container_width - b" bits are actually extracted. The cycle-by-cycle BME operations are detailed in the following table.

Table 24-7. Cycle definitions of decorated load: unsigned bit field extract

Pipeline Stage	Cycle		
	x	x+1	x+2
BME AHB_ap	Forward addr to memory; Decode decoration; Capture address, attributes	Idle AHB address phase	<next>
BME AHB_dp	<previous>	Perform memory read; Form bit mask; Form (rdata & mask) and capture destination data in register	Logically right shift registered data; Return justified rdata to master

24.4 Application information

In this section, GNU assembler macros with C expression operands are presented as examples of the required instructions to perform decorated operations.

This section specifically presents a partial bme.h file defining the assembly language expressions for decorated logical stores: AND, OR, and XOR. Comparable functions for BFI and the decorated loads are more complex and available in the complete BME header file.

These macros use the same function names presented in Functional description.

```
#define IOANDW(ADDR,WDATA)          \
    __asm("ldr    r3, =(1<<26);"    \
          "orr    r3, %[addr];"     \
          "mov    r2, %[wdata];"    \
          "str    r2, [r3];"        \
          :: [addr] "r" (ADDR), [wdata] "r" (WDATA) : "r2", "r3");

#define IOANDH(ADDR,WDATA)          \
    __asm("ldr    r3, =(1<<26);"    \
          "orr    r3, %[addr];"     \
          "mov    r2, %[wdata];"    \
          "strh   r2, [r3];"        \
```

```
          :: [addr] "r" (ADDR), [wdata] "r" (WDATA) : "r2", "r3");

#define IOANDB(ADDR,WDATA)           \
    __asm("ldr    r3, =(1<<26);"     \
          "orr    r3, %[addr];"      \
          "mov    r2, %[wdata];"     \
          "strb   r2, [r3];"         \
          :: [addr] "r" (ADDR), [wdata] "r" (WDATA) : "r2", "r3");

#define IOORW(ADDR,WDATA)            \
    __asm("ldr    r3, =(1<<27);"     \
          "orr    r3, %[addr];"      \
          "mov    r2, %[wdata];"     \
          "str    r2, [r3];"         \
          :: [addr] "r" (ADDR), [wdata] "r" (WDATA) : "r2", "r3");

#define IOORH(ADDR,WDATA)            \
    __asm("ldr    r3, =(1<<27);"     \
          "orr    r3, %[addr];"      \
          "mov    r2, %[wdata];"     \
          "strh   r2, [r3];"         \
          :: [addr] "r" (ADDR), [wdata] "r" (WDATA) : "r2", "r3");

#define IOORB(ADDR,WDATA)            \
    __asm("ldr    r3, =(1<<27);"     \
          "orr    r3, %[addr];"      \
          "mov    r2, %[wdata];"     \
          "strb   r2, [r3];"         \
          :: [addr] "r" (ADDR), [wdata] "r" (WDATA) : "r2", "r3");

#define IOXORW(ADDR,WDATA)           \
    __asm("ldr    r3, =(3<<26);"     \
          "orr    r3, %[addr];"      \
          "mov    r2, %[wdata];"     \
          "str    r2, [r3];"         \
          :: [addr] "r" (ADDR), [wdata] "r" (WDATA) : "r2", "r3");

#define IOXORH(ADDR,WDATA)           \
    __asm("ldr    r3, =(3<<26);"     \
          "orr    r3, %[addr];"      \
          "mov    r2, %[wdata];"     \
          "strh   r2, [r3];"         \
          :: [addr] "r" (ADDR), [wdata] "r" (WDATA) : "r2", "r3");

#define IOXORB(ADDR,WDATA)           \
    __asm("ldr    r3, =(3<<26);"     \
          "orr    r3, %[addr];"      \
          "mov    r2, %[wdata];"     \
          "strb   r2, [r3];"         \
          :: [addr] "r" (ADDR), [wdata] "r" (WDATA) : "r2", "r3");
```

Chapter 25
Direct Memory Access Multiplexer (DMAMUX)

25.1 Chip-specific DMAMUX information

25.1.1 DMA MUX request sources

This device includes a DMA request MUX that allows up to 126 DMA request signals to be mapped to any of the 32 DMA channels in two groups. Because of the mux there is not a hard correlation between any of the DMA request sources and a specific DMA channel. The first group is connected to channels 0-15 and the second group is connected to channels 16-31. To allow for flexibility and optimal usage of the available DMA channels some of the DMA request sources may be available on both groups.

Some of the modules support Asynchronous DMA operation as indicated by the last column in the following DMA source assignment table.

Table 25-1. DMA request sources - DMA Channels 0-15

Source number	Source module	Source description	Asynch DMA capable
0	—	Channel disabled[1]	
1	TSI0	—	Yes
2	LPUART0	Receive	Yes
3	LPUART0	Transmit	Yes
4	LPUART1	Receive	Yes
5	LPUART1	Transmit	Yes
6	LPUART2	Receive	Yes
7	LPUART2	Transmit	Yes
8	LPUART3	Receive	Yes
9	LPUART3	Transmit	Yes

Table continues on the next page...

Table 25-1. DMA request sources - DMA Channels 0-15 (continued)

Source number	Source module	Source description	Asynch DMA capable
10	LPUART4	Receive	Yes
11	LPUART4	Transmit	Yes
12	I2S0	Receive	Yes
13	I2S0	Transmit	Yes
14	SPI0	Receive	
15	SPI0	Transmit	
16	SPI1	Receive	
17	SPI1	Transmit	
18	I2C0 or I2C3	—	
19	I2C1 or I2C2	—	
20	FTM0	Channel 0	
21	FTM0	Channel 1	
22	FTM0	Channel 2	
23	FTM0	Channel 3	
24	FTM0	Channel 4	
25	FTM0	Channel 5	
26	FTM0	Channel 6	
27	FTM0	Channel 7	
28	FTM1	Channel 0	
29	FTM1	Channel 1	
30	FTM2	Channel 0	
31	FTM2	Channel 1	
32	FTM3	Channel 0	
33	FTM3	Channel 1	
34	FTM3	Channel 2	
35	FTM3	Channel 3	
36	FTM3	Channel 4	
37	FTM3	Channel 5	
38	FTM3	Channel 6	
39	FTM3	Channel 7	
40	ADC0	—	Yes
41	Reserved	—	
42	CMP0	—	Yes
43	CMP1	—	Yes
44	Reserved	—	
45	DAC0	—	
46	Reserved	—	

Table continues on the next page...

Table 25-1. DMA request sources - DMA Channels 0-15 (continued)

Source number	Source module	Source description	Asynch DMA capable
47	CMT	—	
48	PDB	—	
49	Port control module	Port A	Yes
50	Port control module	Port B	Yes
51	Port control module	Port C	Yes
52	Port control module	Port D	Yes
53	Port control module	Port E	Yes
54	Reserved		
55	Reserved		
56	Reserved		
57	Reserved		
58	SPI2	Receive	
59	SPI2	Transmit	
60	DMA MUX	Always enabled	
61	DMA MUX	Always enabled	
62	DMA MUX	Always enabled	
63	DMA MUX	Always enabled	

1. Configuring a DMA channel to select source 0 or any of the reserved sources disables that DMA channel.

Table 25-2. DMA request sources - DMA Channels 16-31

Source number	Source module	Source description	Asynch DMA capable
0	—	Channel disabled[1]	
1	FlexIO0	Shifter 0	Yes
2	FlexIO0	Shifter 1	Yes
3	DMA MUX	Shifter 2	Yes
4	FlexIO0	Shifter 3	Yes
5	FlexIO0	Shifter 4	Yes
6	FlexIO0	Shifter 5	Yes
7	FlexIO0	Shifter 6	Yes
8	FlexIO0	Shifter 7	Yes
9	Reserved	—	

Table continues on the next page...

Table 25-2. DMA request sources - DMA Channels 16-31 (continued)

Source number	Source module	Source description	Asynch DMA capable
10	Reserved	—	
11	Reserved	—	
12	Reserved	—	
13	Reserved	—	
14	Reserved	—	
15	Reserved	—	
16	Reserved	—	
17	LTC0	LP Trusted Cryptography - Input FIFO	
18	LTC0	LP Trusted Cryptography - Output FIFO	
19	LTC0	LP Trusted Cryptography - PKHA RAM read	
20	EMVSIM0	Receive	
21	EMVSIM0	Transmit	
22	EMVSIM1	Receive	
23	EMVSIM1	Transmit	
24	QSPI0	Receive	
25	QSPI0	Transmit	
26	Reserved		
27	Reserved		
28	SPI0	Receive	
29	SPI0	Transmit	
30	SPI1	Receive	
31	SPI1	Transmit	
32	Reserved		
33	Reserved		
34	Reserved		
35	Reserved		
36	Reserved		
37	Reserved		
38	Reserved		
39	Reserved		
40	Reserved		
41	Reserved		
42	TPM1	Channel 0	Yes
43	TPM1	Channel 1	Yes
44	TPM2	Channel 0	Yes
45	TPM2	Channel 1	Yes
46	Reserved	Reserved	Reserved

Table continues on the next page...

Table 25-2. DMA request sources - DMA Channels 16-31 (continued)

Source number	Source module	Source description	Asynch DMA capable
47	Reserved	Reserved	Reserved
48	Reserved	Reserved	Reserved
49	Reserved	Reserved	Reserved
50	Reserved	Reserved	Reserved
51	Reserved	Reserved	Reserved
52	Reserved	Reserved	Reserved
53	Reserved	Reserved	Reserved
54	Reserved		
55	TPM1	TPM1 Overflow	Yes
56	TPM2	TPM2 Overflow	Yes
57	Reserved	Reserved	Reserved
58	Reserved		
59	Reserved		
60	DMA MUX	Always enabled	
61	DMA MUX	Always enabled	
62	DMA MUX	Always enabled	
63	DMA MUX	Always enabled	

1. Configuring a DMA channel to select source 0 or any of the reserved sources disables that DMA channel.

25.1.2 DMA transfers via PIT trigger

The PIT module can trigger a DMA transfer on the first four DMA channels. The assignments are detailed at PIT/DMA Periodic Trigger Assignments .

25.2 Introduction

25.2.1 Overview

The Direct Memory Access Multiplexer (DMAMUX) routes DMA sources, called slots, to any of the 32 DMA channels. This process is illustrated in the following figure.

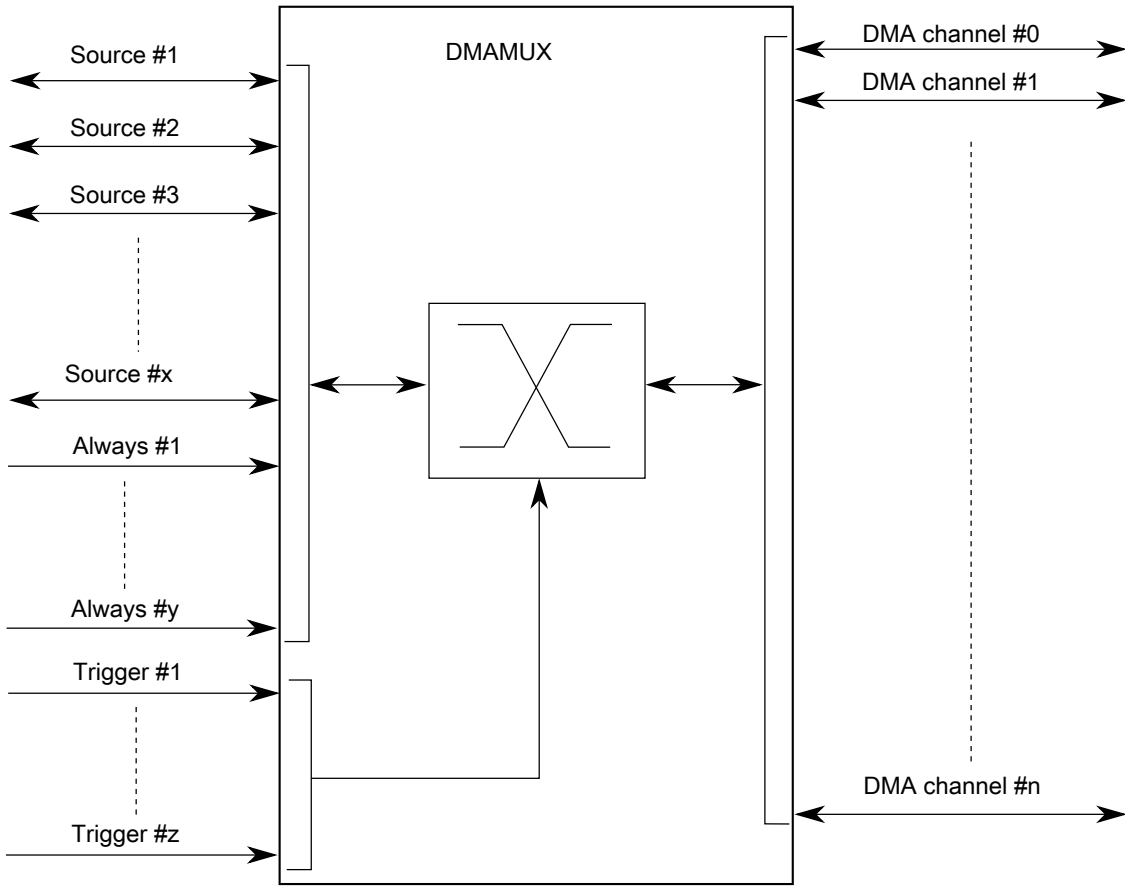


Figure 25-1. DMAMUX block diagram

25.2.2 Features

The DMAMUX module provides these features:

- Up to 59 peripheral slots and up to four always-on slots can be routed to 32 channels.
- 32 independently selectable DMA channel routers.
  - The first four channels additionally provide a trigger functionality.
- Each channel router can be assigned to one of the possible peripheral DMA slots or to one of the always-on slots.

25.2.3 Modes of operation

The following operating modes are available:

- Disabled mode

In this mode, the DMA channel is disabled. Because disabling and enabling of DMA channels is done primarily via the DMA configuration registers, this mode is used mainly as the reset state for a DMA channel in the DMA channel MUX. It may also be used to temporarily suspend a DMA channel while reconfiguration of the system takes place, for example, changing the period of a DMA trigger.

- Normal mode

  In this mode, a DMA source is routed directly to the specified DMA channel. The operation of the DMAMUX in this mode is completely transparent to the system.

- Periodic Trigger mode

  In this mode, a DMA source may only request a DMA transfer, such as when a transmit buffer becomes empty or a receive buffer becomes full, periodically.

  Configuration of the period is done in the registers of the periodic interrupt timer (PIT). This mode is available only for channels 0–3.

25.3 External signal description

The DMAMUX has no external pins.

25.4 Memory map/register definition

This section provides a detailed description of all memory-mapped registers in the DMAMUX.

DMAMUX memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4002_1000	Channel Configuration register (DMAMUX_CHCFG0)	8	R/W	00h	25.4.1/530
4002_1001	Channel Configuration register (DMAMUX_CHCFG1)	8	R/W	00h	25.4.1/530
4002_1002	Channel Configuration register (DMAMUX_CHCFG2)	8	R/W	00h	25.4.1/530
4002_1003	Channel Configuration register (DMAMUX_CHCFG3)	8	R/W	00h	25.4.1/530
4002_1004	Channel Configuration register (DMAMUX_CHCFG4)	8	R/W	00h	25.4.1/530
4002_1005	Channel Configuration register (DMAMUX_CHCFG5)	8	R/W	00h	25.4.1/530
4002_1006	Channel Configuration register (DMAMUX_CHCFG6)	8	R/W	00h	25.4.1/530
4002_1007	Channel Configuration register (DMAMUX_CHCFG7)	8	R/W	00h	25.4.1/530
4002_1008	Channel Configuration register (DMAMUX_CHCFG8)	8	R/W	00h	25.4.1/530

Table continues on the next page...

DMAMUX memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4002_1009	Channel Configuration register (DMAMUX_CHCFG9)	8	R/W	00h	25.4.1/530
4002_100A	Channel Configuration register (DMAMUX_CHCFG10)	8	R/W	00h	25.4.1/530
4002_100B	Channel Configuration register (DMAMUX_CHCFG11)	8	R/W	00h	25.4.1/530
4002_100C	Channel Configuration register (DMAMUX_CHCFG12)	8	R/W	00h	25.4.1/530
4002_100D	Channel Configuration register (DMAMUX_CHCFG13)	8	R/W	00h	25.4.1/530
4002_100E	Channel Configuration register (DMAMUX_CHCFG14)	8	R/W	00h	25.4.1/530
4002_100F	Channel Configuration register (DMAMUX_CHCFG15)	8	R/W	00h	25.4.1/530
4002_1010	Channel Configuration register (DMAMUX_CHCFG16)	8	R/W	00h	25.4.1/530
4002_1011	Channel Configuration register (DMAMUX_CHCFG17)	8	R/W	00h	25.4.1/530
4002_1012	Channel Configuration register (DMAMUX_CHCFG18)	8	R/W	00h	25.4.1/530
4002_1013	Channel Configuration register (DMAMUX_CHCFG19)	8	R/W	00h	25.4.1/530
4002_1014	Channel Configuration register (DMAMUX_CHCFG20)	8	R/W	00h	25.4.1/530
4002_1015	Channel Configuration register (DMAMUX_CHCFG21)	8	R/W	00h	25.4.1/530
4002_1016	Channel Configuration register (DMAMUX_CHCFG22)	8	R/W	00h	25.4.1/530
4002_1017	Channel Configuration register (DMAMUX_CHCFG23)	8	R/W	00h	25.4.1/530
4002_1018	Channel Configuration register (DMAMUX_CHCFG24)	8	R/W	00h	25.4.1/530
4002_1019	Channel Configuration register (DMAMUX_CHCFG25)	8	R/W	00h	25.4.1/530
4002_101A	Channel Configuration register (DMAMUX_CHCFG26)	8	R/W	00h	25.4.1/530
4002_101B	Channel Configuration register (DMAMUX_CHCFG27)	8	R/W	00h	25.4.1/530
4002_101C	Channel Configuration register (DMAMUX_CHCFG28)	8	R/W	00h	25.4.1/530
4002_101D	Channel Configuration register (DMAMUX_CHCFG29)	8	R/W	00h	25.4.1/530
4002_101E	Channel Configuration register (DMAMUX_CHCFG30)	8	R/W	00h	25.4.1/530
4002_101F	Channel Configuration register (DMAMUX_CHCFG31)	8	R/W	00h	25.4.1/530

25.4.1 Channel Configuration register (DMAMUX_CHCFG*n*)

Each of the DMA channels can be independently enabled/disabled and associated with one of the DMA slots (peripheral slots or always-on slots) in the system.

NOTE

Setting multiple CHCFG registers with the same source value will result in unpredictable behavior. This is true, even if a channel is disabled (ENBL==0).

Before changing the trigger or source settings, a DMA channel must be disabled via CHCFGn[ENBL].

Address: 4002_1000h base + 0h offset + (1d × i), where i=0d to 31d

Bit	7	6	5	4	3	2	1	0
Read Write	ENBL	TRIG	SOURCE					
Reset	0	0	0	0	0	0	0	0

DMAMUX_CHCFG*n* field descriptions

Field	Description
7 ENBL	DMA Channel Enable Enables the DMA channel. 0 DMA channel is disabled. This mode is primarily used during configuration of the DMAMux. The DMA has separate channel enables/disables, which should be used to disable or reconfigure a DMA channel. 1 DMA channel is enabled
6 TRIG	DMA Channel Trigger Enable Enables the periodic trigger capability for the triggered DMA channel. 0 Triggering is disabled. If triggering is disabled and ENBL is set, the DMA Channel will simply route the specified source to the DMA channel. (Normal mode) 1 Triggering is enabled. If triggering is enabled and ENBL is set, the DMAMUX is in Periodic Trigger mode.
SOURCE	DMA Channel Source (Slot) Specifies which DMA source, if any, is routed to a particular DMA channel. See the chip-specific DMAMUX information for details about the peripherals and their slot numbers.

25.5 Functional description

The primary purpose of the DMAMUX is to provide flexibility in the system's use of the available DMA channels.

As such, configuration of the DMAMUX is intended to be a static procedure done during execution of the system boot code. However, if the procedure outlined in Enabling and configuring sources is followed, the configuration of the DMAMUX may be changed during the normal operation of the system.

Functionally, the DMAMUX channels may be divided into two classes:

- Channels that implement the normal routing functionality plus periodic triggering capability
- Channels that implement only the normal routing functionality

25.5.1 DMA channels with periodic triggering capability

Besides the normal routing functionality, the first 4 channels of the DMAMUX provide a special periodic triggering capability that can be used to provide an automatic mechanism to transmit bytes, frames, or packets at fixed intervals without the need for processor intervention.

The trigger is generated by the periodic interrupt timer (PIT); as such, the configuration of the periodic triggering interval is done via configuration registers in the PIT. See the section on periodic interrupt timer for more information on this topic.

Note

Because of the dynamic nature of the system (due to DMA channel priorities, bus arbitration, interrupt service routine lengths, etc.), the number of clock cycles between a trigger and the actual DMA transfer cannot be guaranteed.

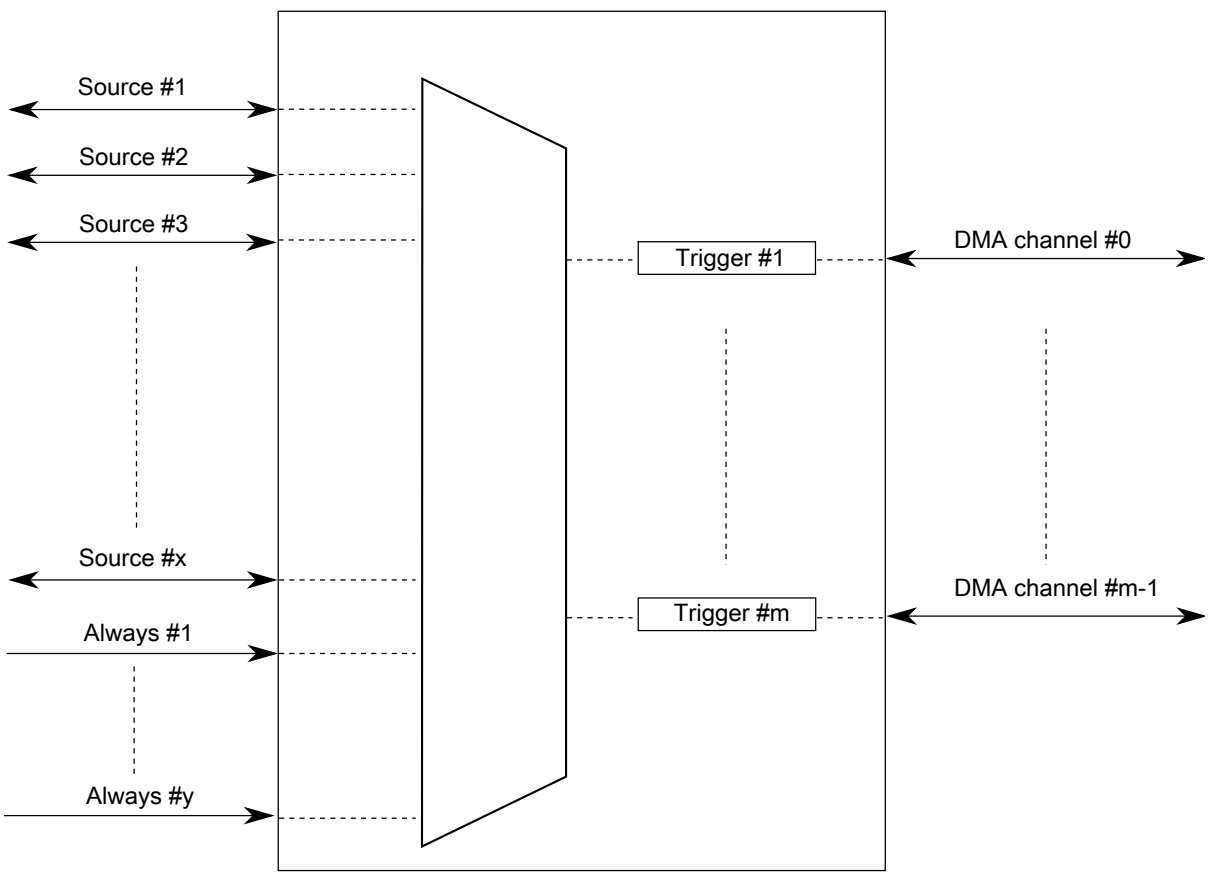


Figure 25-2. DMAMUX triggered channels

The DMA channel triggering capability allows the system to schedule regular DMA transfers, usually on the transmit side of certain peripherals, without the intervention of the processor. This trigger works by gating the request from the peripheral to the DMA until a trigger event has been seen. This is illustrated in the following figure.

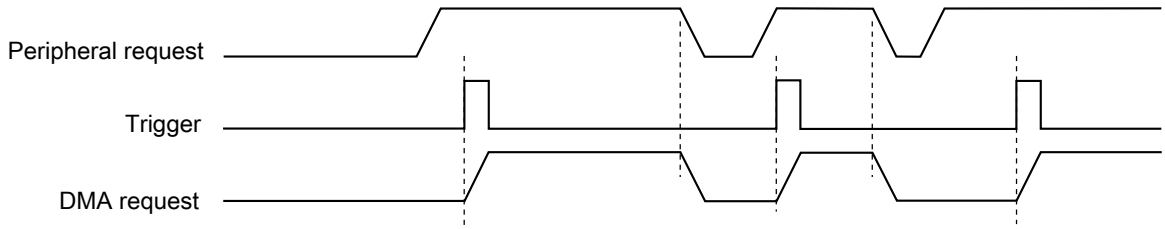


Figure 25-3. DMAMUX channel triggering: normal operation

After the DMA request has been serviced, the peripheral will negate its request, effectively resetting the gating mechanism until the peripheral reasserts its request and the next trigger event is seen. This means that if a trigger is seen, but the peripheral is not requesting a transfer, then that trigger will be ignored. This situation is illustrated in the following figure.

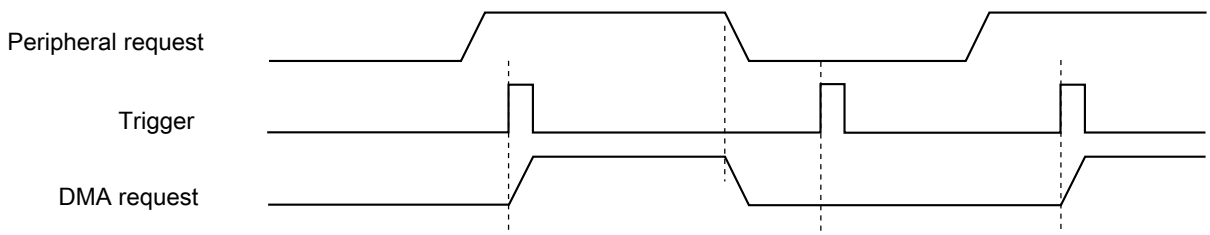


Figure 25-4. DMAMUX channel triggering: ignored trigger

This triggering capability may be used with any peripheral that supports DMA transfers, and is most useful for two types of situations:

- Periodically polling external devices on a particular bus

  As an example, the transmit side of an SPI is assigned to a DMA channel with a trigger, as described above. After it has been set up, the SPI will request DMA transfers, presumably from memory, as long as its transmit buffer is empty. By using a trigger on this channel, the SPI transfers can be automatically performed every 5 µs (as an example). On the receive side of the SPI, the SPI and DMA can be configured to transfer receive data into memory, effectively implementing a method to periodically read data from external devices and transfer the results into memory without processor intervention.

- Using the GPIO ports to drive or sample waveforms

By configuring the DMA to transfer data to one or more GPIO ports, it is possible to create complex waveforms using tabular data stored in on-chip memory. Conversely, using the DMA to periodically transfer data from one or more GPIO ports, it is possible to sample complex waveforms and store the results in tabular form in on-chip memory.

A more detailed description of the capability of each trigger, including resolution, range of values, and so on, may be found in the periodic interrupt timer section.

25.5.2 DMA channels with no triggering capability

The other channels of the DMAMUX provide the normal routing functionality as described in Modes of operation.

25.5.3 Always-enabled DMA sources

In addition to the peripherals that can be used as DMA sources, there are four additional DMA sources that are always enabled. Unlike the peripheral DMA sources, where the peripheral controls the flow of data during DMA transfers, the sources that are always enabled provide no such "throttling" of the data transfers. These sources are most useful in the following cases:

- Performing DMA transfers to/from GPIO—Moving data from/to one or more GPIO pins, either unthrottled (that is, as fast as possible), or periodically (using the DMA triggering capability).
- Performing DMA transfers from memory to memory—Moving data from memory to memory, typically as fast as possible, sometimes with software activation.
- Performing DMA transfers from memory to the external bus, or vice-versa—Similar to memory to memory transfers, this is typically done as quickly as possible.
- Any DMA transfer that requires software activation—Any DMA transfer that should be explicitly started by software.

In cases where software should initiate the start of a DMA transfer, an always-enabled DMA source can be used to provide maximum flexibility. When activating a DMA channel via software, subsequent executions of the minor loop require that a new start event be sent. This can either be a new software activation, or a transfer request from the DMA channel MUX. The options for doing this are:

- Transfer all data in a single minor loop.

By configuring the DMA to transfer all of the data in a single minor loop (that is, major loop counter = 1), no reactivation of the channel is necessary. The disadvantage to this option is the reduced granularity in determining the load that the DMA transfer will impose on the system. For this option, the DMA channel must be disabled in the DMA channel MUX.

- Use explicit software reactivation.

  In this option, the DMA is configured to transfer the data using both minor and major loops, but the processor is required to reactivate the channel by writing to the DMA registers *after every minor loop*. For this option, the DMA channel must be disabled in the DMA channel MUX.

- Use an always-enabled DMA source.

  In this option, the DMA is configured to transfer the data using both minor and major loops, and the DMA channel MUX does the channel reactivation. For this option, the DMA channel should be enabled and pointing to an "always enabled" source. Note that the reactivation of the channel can be continuous (DMA triggering is disabled) or can use the DMA triggering capability. In this manner, it is possible to execute periodic transfers of packets of data from one source to another, without processor intervention.

25.6 Initialization/application information

This section provides instructions for initializing the DMA channel MUX.

25.6.1 Reset

The reset state of each individual bit is shown in Memory map/register definition. In summary, after reset, all channels are disabled and must be explicitly enabled before use.

25.6.2 Enabling and configuring sources

To enable a source with periodic triggering:

1. Determine with which DMA channel the source will be associated. Note that only the first 4 DMA channels have periodic triggering capability.
2. Clear the CHCFG[ENBL] and CHCFG[TRIG] fields of the DMA channel.

3. Ensure that the DMA channel is properly configured in the DMA. The DMA channel may be enabled at this point.
4. Configure the corresponding timer.
5. Select the source to be routed to the DMA channel. Write to the corresponding CHCFG register, ensuring that the CHCFG[ENBL] and CHCFG[TRIG] fields are set.

NOTE

The following is an example. See the chip configuration details for the number of this device's DMA channels that have triggering capability.

To configure source #5 transmit for use with DMA channel 1, with periodic triggering capability:

1. Write 0x00 to CHCFG1.
2. Configure channel 1 in the DMA, including enabling the channel.
3. Configure a timer for the desired trigger interval.
4. Write 0xC5 to CHCFG1.

The following code example illustrates steps 1 and 4 above:

```
void DMAMUX_Init(uint8_t DMA_CH, uint8_t DMAMUX_SOURCE)
{
    DMAMUX_0.CHCFG[DMA_CH].B.SOURCE = DMAMUX_SOURCE;
    DMAMUX_0.CHCFG[DMA_CH].B.ENBL   = 1;
    DMAMUX_0.CHCFG[DMA_CH].B.TRIG   = 1;
}
```

To enable a source, without periodic triggering:

1. Determine with which DMA channel the source will be associated. Note that only the first 4 DMA channels have periodic triggering capability.
2. Clear the CHCFG[ENBL] and CHCFG[TRIG] fields of the DMA channel.
3. Ensure that the DMA channel is properly configured in the DMA. The DMA channel may be enabled at this point.
4. Select the source to be routed to the DMA channel. Write to the corresponding CHCFG register, ensuring that CHCFG[ENBL] is set while CHCFG[TRIG] is cleared.

NOTE

The following is an example. See the chip configuration details for the number of this device's DMA channels that have triggering capability.

To configure source #5 transmit for use with DMA channel 1, with no periodic triggering capability:

1. Write 0x00 to CHCFG1.

2. Configure channel 1 in the DMA, including enabling the channel.
3. Write 0x85 to CHCFG1.

The following code example illustrates steps 1 and 3 above:

```
In File registers.h:
#define DMAMUX_BASE_ADDR     0x40021000/* Example only ! */
/* Following example assumes char is 8-bits */
volatile unsigned char *CHCFG0 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0000);
volatile unsigned char *CHCFG1 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0001);
volatile unsigned char *CHCFG2 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0002);
volatile unsigned char *CHCFG3 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0003);
volatile unsigned char *CHCFG4 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0004);
volatile unsigned char *CHCFG5 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0005);
volatile unsigned char *CHCFG6 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0006);
volatile unsigned char *CHCFG7 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0007);
volatile unsigned char *CHCFG8 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0008);
volatile unsigned char *CHCFG9 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0009);
volatile unsigned char *CHCFG10= (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x000A);
volatile unsigned char *CHCFG11= (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x000B);
volatile unsigned char *CHCFG12= (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x000C);
volatile unsigned char *CHCFG13= (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x000D);
volatile unsigned char *CHCFG14= (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x000E);
volatile unsigned char *CHCFG15= (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x000F);

In File main.c:
#include "registers.h"
:
:
*CHCFG1 = 0x00;
*CHCFG1 = 0x85;
```

To disable a source:

A particular DMA source may be disabled by not writing the corresponding source value into any of the CHCFG registers. Additionally, some module-specific configuration may be necessary. See the appropriate section for more details.

To switch the source of a DMA channel:

1. Disable the DMA channel in the DMA and reconfigure the channel for the new source.
2. Clear the CHCFG[ENBL] and CHCFG[TRIG] bits of the DMA channel.
3. Select the source to be routed to the DMA channel. Write to the corresponding CHCFG register, ensuring that the CHCFG[ENBL] and CHCFG[TRIG] fields are set.

To switch DMA channel 8 from source #5 transmit to source #7 transmit:

1. In the DMA configuration registers, disable DMA channel 8 and reconfigure it to handle the transfers to peripheral slot 7. This example assumes channel 8 doesn't have triggering capability.
2. Write 0x00 to CHCFG8.
3. Write 0x87 to CHCFG8. (In this example, setting CHCFG[TRIG] would have no effect due to the assumption that channel 8 does not support the periodic triggering functionality.)

The following code example illustrates steps 2 and 3 above:

```
In File registers.h:
#define DMAMUX_BASE_ADDR     0x40021000/* Example only ! */
/* Following example assumes char is 8-bits */
volatile unsigned char *CHCFG0 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0000);
volatile unsigned char *CHCFG1 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0001);
volatile unsigned char *CHCFG2 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0002);
volatile unsigned char *CHCFG3 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0003);
volatile unsigned char *CHCFG4 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0004);
volatile unsigned char *CHCFG5 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0005);
volatile unsigned char *CHCFG6 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0006);
volatile unsigned char *CHCFG7 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0007);
volatile unsigned char *CHCFG8 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0008);
volatile unsigned char *CHCFG9 = (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x0009);
volatile unsigned char *CHCFG10= (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x000A);
volatile unsigned char *CHCFG11= (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x000B);
volatile unsigned char *CHCFG12= (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x000C);
volatile unsigned char *CHCFG13= (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x000D);
volatile unsigned char *CHCFG14= (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x000E);
volatile unsigned char *CHCFG15= (volatile unsigned char *) (DMAMUX_BASE_ADDR+0x000F);

In File main.c:
#include "registers.h"
:
:
*CHCFG8 = 0x00;
*CHCFG8 = 0x87;
```

Chapter 26
Enhanced Direct Memory Access (eDMA)

26.1 Introduction

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data transfers with minimal intervention from a host processor. The hardware microarchitecture includes:

- A DMA engine that performs:
  - Source address and destination address calculations
  - Data-movement operations
- Local memory containing transfer control descriptors for each of the 32 channels

26.1.1 eDMA system block diagram

Figure 26-1 illustrates the components of the eDMA system, including the eDMA module ("engine").

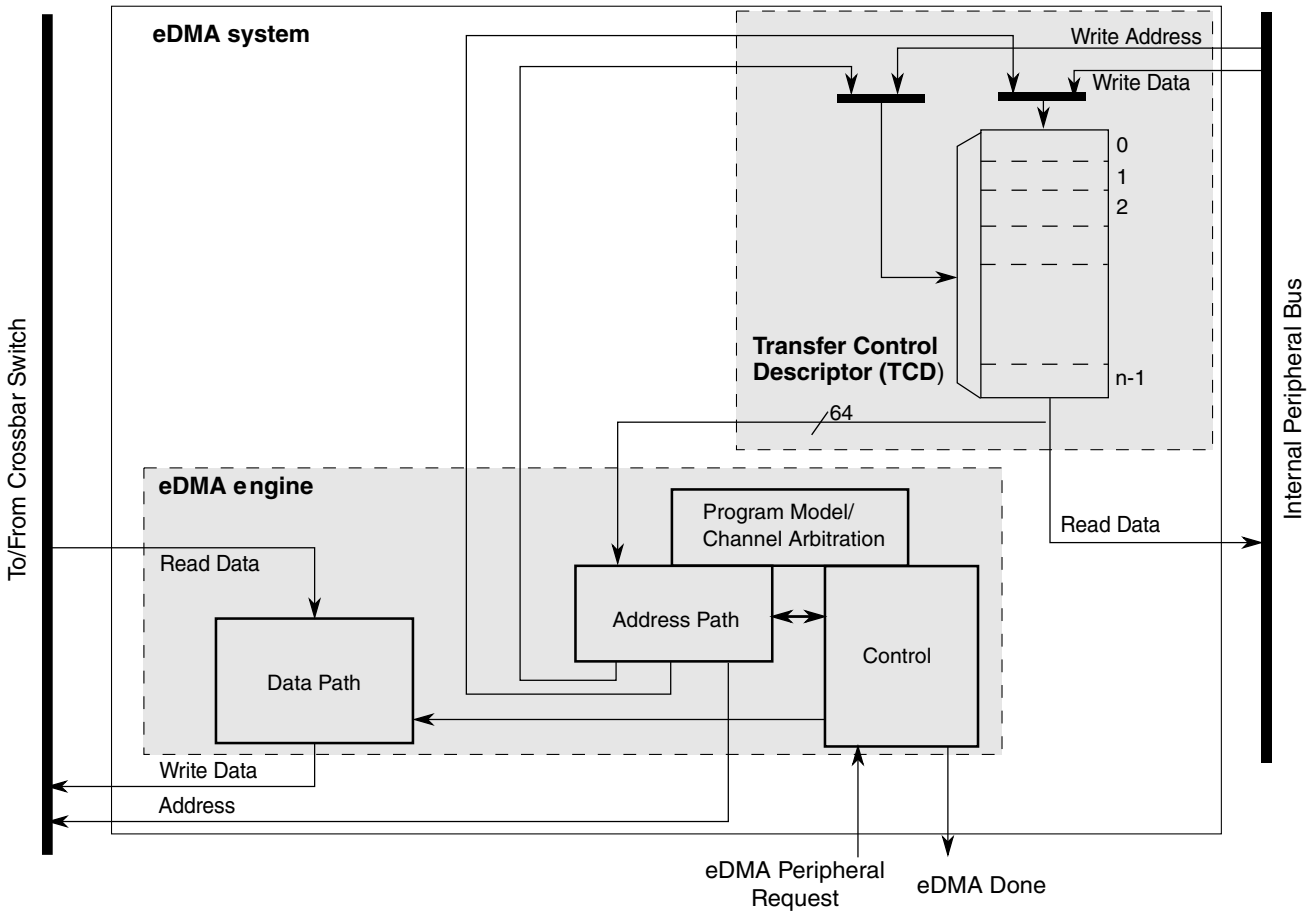


Figure 26-1. eDMA system block diagram

26.1.2 Block parts

The eDMA module is partitioned into two major modules: the eDMA engine and the transfer-control descriptor local memory.

The eDMA engine is further partitioned into four submodules:

Table 26-1. eDMA engine submodules

Submodule	Function
Address path	This block implements registered versions of two channel transfer control descriptors, channel x and channel y, and manages all master bus-address calculations. All the channels provide the same functionality. This structure allows data transfers associated with one channel to be preempted after the completion of a read/write sequence if a higher priority channel activation is asserted while the first channel is active. After a channel is activated, it runs until the minor loop is completed, unless preempted by a higher priority channel. This provides a mechanism (enabled by DCHPRI*n*[ECP]) where a large data move operation can be preempted to minimize the time another channel is blocked from execution. When any channel is selected to execute, the contents of its TCD are read from local memory and loaded into the address path channel x registers for a normal start and into channel y registers for a preemption start. After the minor loop completes execution, the address path hardware writes

Table continues on the next page...

Table 26-1. eDMA engine submodules (continued)

Submodule	Function
	the new values for the TCD*n*_{SADDR, DADDR, CITER} back to local memory. If the major iteration count is exhausted, additional processing is performed, including the final address pointer updates, reloading the TCD*n*_CITER field, and a possible fetch of the next TCD*n* from memory as part of a scatter/gather operation.
Data path	This block implements the bus master read/write datapath. It includes a data buffer and the necessary multiplex logic to support any required data alignment. The internal read data bus is the primary input, and the internal write data bus is the primary output. The address and data path modules directly support the 2-stage pipelined internal bus. The address path module represents the 1st stage of the bus pipeline (address phase), while the data path module implements the 2nd stage of the pipeline (data phase).
Program model/channel arbitration	This block implements the first section of the eDMA programming model as well as the channel arbitration logic. The programming model registers are connected to the internal peripheral bus. The eDMA peripheral request inputs and interrupt request outputs are also connected to this block (via control logic).
Control	This block provides all the control functions for the eDMA engine. For data transfers where the source and destination sizes are equal, the eDMA engine performs a series of source read/destination write operations until the number of bytes specified in the minor loop byte count has moved. For descriptors where the sizes are not equal, multiple accesses of the smaller size data are required for each reference of the larger size. As an example, if the source size references 16-bit data and the destination is 32-bit data, two reads are performed, then one 32-bit write.

The transfer-control descriptor local memory is further partitioned into:

Table 26-2. Transfer control descriptor memory

Submodule	Description
Memory controller	This logic implements the required dual-ported controller, managing accesses from the eDMA engine as well as references from the internal peripheral bus. As noted earlier, in the event of simultaneous accesses, the eDMA engine is given priority and the peripheral transaction is stalled.
Memory array	TCD storage for each channel's transfer profile.

26.1.3 Features

The eDMA is a highly programmable data-transfer engine optimized to minimize any required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known and not defined within the transferred data itself. The eDMA module features:

- All data movement via dual-address transfers: read from source, write to destination
  - Programmable source and destination addresses and transfer size
  - Support for enhanced addressing modes

- 32-channel implementation that performs complex data transfers with minimal intervention from a host processor
  - Internal data buffer, used as temporary storage to support 16- and 32-byte transfers
  - Connections to the crossbar switch for bus mastering the data movement
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
  - 32-byte TCD stored in local memory for each channel
  - An inner data transfer loop defined by a minor byte transfer count
  - An outer data transfer loop defined by a major iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests, one per channel
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via programmable interrupt requests
  - One interrupt per channel, which can be asserted at completion of major iteration count
  - Programmable error terminations per channel and logically summed together to form one error interrupt to the interrupt controller
- Programmable support for scatter/gather DMA processing
- Support for complex data structures

In the discussion of this module, *n* is used to reference the channel number.

26.2 Modes of operation

The eDMA operates in the following modes:

Table 26-3. Modes of operation

Mode	Description
Normal	In Normal mode, the eDMA transfers data between a source and a destination. The source and destination can be a memory block or an I/O block capable of operation with the eDMA. A service request initiates a transfer of a specific number of bytes (NBYTES) as specified in the transfer control descriptor (TCD). The minor loop is the sequence of read-write operations that transfers these NBYTES per service request. Each service request executes one iteration of the major loop, which transfers NBYTES of data.
Debug	DMA operation is configurable in Debug mode via the control register: • If CR[EDBG] is cleared, the DMA continues to operate. • If CR[EDBG] is set, the eDMA stops transferring data. If Debug mode is entered while a channel is active, the eDMA continues operation until the channel retires.
Wait	Before entering Wait mode, the DMA attempts to complete its current transfer. After the transfer completes, the device enters Wait mode.

26.3 Memory map/register definition

The eDMA's programming model is partitioned into two regions:

- The first region defines a number of registers providing control functions
- The second region corresponds to the local transfer control descriptor (TCD) memory

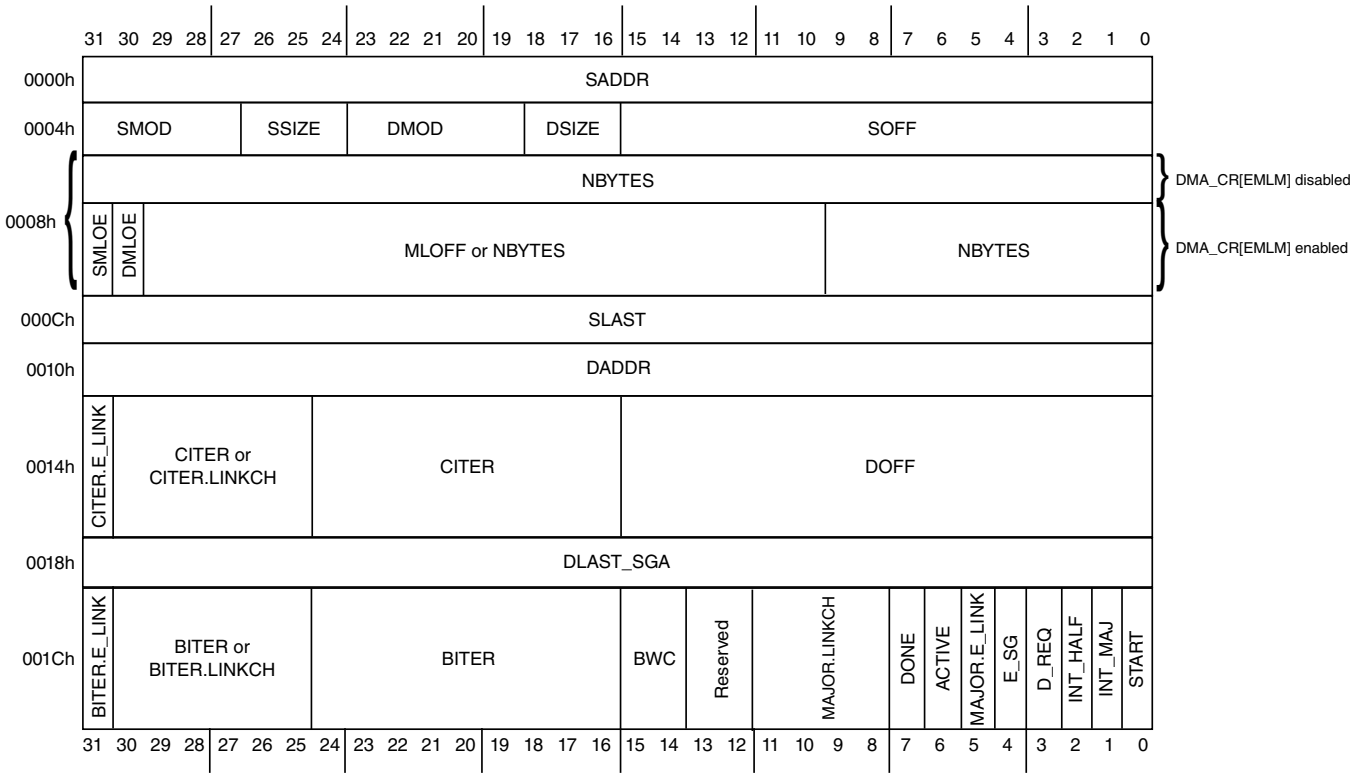
26.3.1 TCD memory

Each channel requires a 32-byte transfer control descriptor for defining the desired data movement operation. The channel descriptors are stored in the local memory in sequential order: channel 0, channel 1, ... channel 31. Each TCD*n* definition is presented as 11 registers of 16 or 32 bits.

26.3.2 TCD initialization

Prior to activating a channel, you must initialize its TCD with the appropriate transfer profile.

26.3.3 TCD structure



26.3.4 Reserved memory and bit fields

- Reading reserved bits in a register returns the value of zero.
- Writes to reserved bits in a register are ignored.
- Reading or writing a reserved memory location generates a bus error.

DMA memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_8000	Control Register (DMA_CR)	32	R/W	0000_0400h	26.3.1/570
4000_8004	Error Status Register (DMA_ES)	32	R	0000_0000h	26.3.2/573
4000_800C	Enable Request Register (DMA_ERQ)	32	R/W	0000_0000h	26.3.3/575
4000_8014	Enable Error Interrupt Register (DMA_EEI)	32	R/W	0000_0000h	26.3.4/579
4000_8018	Clear Enable Error Interrupt Register (DMA_CEEI)	8	W (always reads 0)	00h	26.3.5/582
4000_8019	Set Enable Error Interrupt Register (DMA_SEEI)	8	W (always reads 0)	00h	26.3.6/583

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_801A	Clear Enable Request Register (DMA_CERQ)	8	W (always reads 0)	00h	26.3.7/584
4000_801B	Set Enable Request Register (DMA_SERQ)	8	W (always reads 0)	00h	26.3.8/585
4000_801C	Clear DONE Status Bit Register (DMA_CDNE)	8	W (always reads 0)	00h	26.3.9/586
4000_801D	Set START Bit Register (DMA_SSRT)	8	W (always reads 0)	00h	26.3.10/ 587
4000_801E	Clear Error Register (DMA_CERR)	8	W (always reads 0)	00h	26.3.11/ 588
4000_801F	Clear Interrupt Request Register (DMA_CINT)	8	W (always reads 0)	00h	26.3.12/ 589
4000_8024	Interrupt Request Register (DMA_INT)	32	R/W	0000_0000h	26.3.13/ 590
4000_802C	Error Register (DMA_ERR)	32	R/W	0000_0000h	26.3.14/ 593
4000_8034	Hardware Request Status Register (DMA_HRS)	32	R	0000_0000h	26.3.15/ 597
4000_8044	Enable Asynchronous Request in Stop Register (DMA_EARS)	32	R/W	0000_0000h	26.3.16/ 603
4000_8100	Channel n Priority Register (DMA_DCHPRI3)	8	R/W	See section	26.3.17/ 606
4000_8101	Channel n Priority Register (DMA_DCHPRI2)	8	R/W	See section	26.3.17/ 606
4000_8102	Channel n Priority Register (DMA_DCHPRI1)	8	R/W	See section	26.3.17/ 606
4000_8103	Channel n Priority Register (DMA_DCHPRI0)	8	R/W	See section	26.3.17/ 606
4000_8104	Channel n Priority Register (DMA_DCHPRI7)	8	R/W	See section	26.3.17/ 606
4000_8105	Channel n Priority Register (DMA_DCHPRI6)	8	R/W	See section	26.3.17/ 606
4000_8106	Channel n Priority Register (DMA_DCHPRI5)	8	R/W	See section	26.3.17/ 606
4000_8107	Channel n Priority Register (DMA_DCHPRI4)	8	R/W	See section	26.3.17/ 606
4000_8108	Channel n Priority Register (DMA_DCHPRI11)	8	R/W	See section	26.3.17/ 606

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_8109	Channel n Priority Register (DMA_DCHPRI10)	8	R/W	See section	26.3.17/ 606
4000_810A	Channel n Priority Register (DMA_DCHPRI9)	8	R/W	See section	26.3.17/ 606
4000_810B	Channel n Priority Register (DMA_DCHPRI8)	8	R/W	See section	26.3.17/ 606
4000_810C	Channel n Priority Register (DMA_DCHPRI15)	8	R/W	See section	26.3.17/ 606
4000_810D	Channel n Priority Register (DMA_DCHPRI14)	8	R/W	See section	26.3.17/ 606
4000_810E	Channel n Priority Register (DMA_DCHPRI13)	8	R/W	See section	26.3.17/ 606
4000_810F	Channel n Priority Register (DMA_DCHPRI12)	8	R/W	See section	26.3.17/ 606
4000_8110	Channel n Priority Register (DMA_DCHPRI19)	8	R/W	See section	26.3.17/ 606
4000_8111	Channel n Priority Register (DMA_DCHPRI18)	8	R/W	See section	26.3.17/ 606
4000_8112	Channel n Priority Register (DMA_DCHPRI17)	8	R/W	See section	26.3.17/ 606
4000_8113	Channel n Priority Register (DMA_DCHPRI16)	8	R/W	See section	26.3.17/ 606
4000_8114	Channel n Priority Register (DMA_DCHPRI23)	8	R/W	See section	26.3.17/ 606
4000_8115	Channel n Priority Register (DMA_DCHPRI22)	8	R/W	See section	26.3.17/ 606
4000_8116	Channel n Priority Register (DMA_DCHPRI21)	8	R/W	See section	26.3.17/ 606
4000_8117	Channel n Priority Register (DMA_DCHPRI20)	8	R/W	See section	26.3.17/ 606
4000_8118	Channel n Priority Register (DMA_DCHPRI27)	8	R/W	See section	26.3.17/ 606
4000_8119	Channel n Priority Register (DMA_DCHPRI26)	8	R/W	See section	26.3.17/ 606
4000_811A	Channel n Priority Register (DMA_DCHPRI25)	8	R/W	See section	26.3.17/ 606
4000_811B	Channel n Priority Register (DMA_DCHPRI24)	8	R/W	See section	26.3.17/ 606
4000_811C	Channel n Priority Register (DMA_DCHPRI31)	8	R/W	See section	26.3.17/ 606
4000_811D	Channel n Priority Register (DMA_DCHPRI30)	8	R/W	See section	26.3.17/ 606
4000_811E	Channel n Priority Register (DMA_DCHPRI29)	8	R/W	See section	26.3.17/ 606

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_811F	Channel n Priority Register (DMA_DCHPRI28)	8	R/W	See section	26.3.17/ 606
4000_9000	TCD Source Address (DMA_TCD0_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9004	TCD Signed Source Address Offset (DMA_TCD0_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9006	TCD Transfer Attributes (DMA_TCD0_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9008	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD0_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9008	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD0_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9008	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD0_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_900C	TCD Last Source Address Adjustment (DMA_TCD0_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9010	TCD Destination Address (DMA_TCD0_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9014	TCD Signed Destination Address Offset (DMA_TCD0_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9016	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD0_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9016	DMA_TCD0_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9018	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD0_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_901C	TCD Control and Status (DMA_TCD0_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_901E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD0_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_901E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD0_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9020	TCD Source Address (DMA_TCD1_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9024	TCD Signed Source Address Offset (DMA_TCD1_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9026	TCD Transfer Attributes (DMA_TCD1_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9028	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD1_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9028	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD1_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_9028	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD1_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_902C	TCD Last Source Address Adjustment (DMA_TCD1_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9030	TCD Destination Address (DMA_TCD1_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9034	TCD Signed Destination Address Offset (DMA_TCD1_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9036	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD1_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9036	DMA_TCD1_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9038	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD1_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_903C	TCD Control and Status (DMA_TCD1_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_903E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD1_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_903E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD1_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9040	TCD Source Address (DMA_TCD2_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9044	TCD Signed Source Address Offset (DMA_TCD2_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9046	TCD Transfer Attributes (DMA_TCD2_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9048	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD2_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9048	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD2_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9048	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD2_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_904C	TCD Last Source Address Adjustment (DMA_TCD2_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9050	TCD Destination Address (DMA_TCD2_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9054	TCD Signed Destination Address Offset (DMA_TCD2_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9056	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD2_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9056	DMA_TCD2_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_9058	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD2_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_905C	TCD Control and Status (DMA_TCD2_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_905E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD2_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_905E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD2_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9060	TCD Source Address (DMA_TCD3_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9064	TCD Signed Source Address Offset (DMA_TCD3_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9066	TCD Transfer Attributes (DMA_TCD3_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9068	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD3_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9068	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD3_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9068	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD3_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_906C	TCD Last Source Address Adjustment (DMA_TCD3_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9070	TCD Destination Address (DMA_TCD3_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9074	TCD Signed Destination Address Offset (DMA_TCD3_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9076	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD3_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9076	DMA_TCD3_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9078	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD3_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_907C	TCD Control and Status (DMA_TCD3_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_907E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD3_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_907E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD3_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9080	TCD Source Address (DMA_TCD4_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9084	TCD Signed Source Address Offset (DMA_TCD4_SOFF)	16	R/W	Undefined	26.3.19/ 608

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_9086	TCD Transfer Attributes (DMA_TCD4_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9088	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD4_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9088	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD4_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9088	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD4_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_908C	TCD Last Source Address Adjustment (DMA_TCD4_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9090	TCD Destination Address (DMA_TCD4_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9094	TCD Signed Destination Address Offset (DMA_TCD4_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9096	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD4_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9096	DMA_TCD4_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9098	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD4_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_909C	TCD Control and Status (DMA_TCD4_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_909E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD4_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_909E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD4_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_90A0	TCD Source Address (DMA_TCD5_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_90A4	TCD Signed Source Address Offset (DMA_TCD5_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_90A6	TCD Transfer Attributes (DMA_TCD5_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_90A8	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD5_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_90A8	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD5_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_90A8	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD5_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_90AC	TCD Last Source Address Adjustment (DMA_TCD5_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_90B0	TCD Destination Address (DMA_TCD5_DADDR)	32	R/W	Undefined	26.3.25/ 613

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_90B4	TCD Signed Destination Address Offset (DMA_TCD5_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_90B6	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD5_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_90B6	DMA_TCD5_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_90B8	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD5_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_90BC	TCD Control and Status (DMA_TCD5_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_90BE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD5_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_90BE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD5_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_90C0	TCD Source Address (DMA_TCD6_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_90C4	TCD Signed Source Address Offset (DMA_TCD6_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_90C6	TCD Transfer Attributes (DMA_TCD6_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_90C8	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD6_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_90C8	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD6_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_90C8	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD6_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_90CC	TCD Last Source Address Adjustment (DMA_TCD6_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_90D0	TCD Destination Address (DMA_TCD6_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_90D4	TCD Signed Destination Address Offset (DMA_TCD6_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_90D6	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD6_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_90D6	DMA_TCD6_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_90D8	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD6_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_90DC	TCD Control and Status (DMA_TCD6_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_90DE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD6_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619

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DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_90DE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD6_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_90E0	TCD Source Address (DMA_TCD7_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_90E4	TCD Signed Source Address Offset (DMA_TCD7_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_90E6	TCD Transfer Attributes (DMA_TCD7_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_90E8	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD7_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_90E8	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD7_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_90E8	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD7_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_90EC	TCD Last Source Address Adjustment (DMA_TCD7_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_90F0	TCD Destination Address (DMA_TCD7_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_90F4	TCD Signed Destination Address Offset (DMA_TCD7_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_90F6	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD7_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_90F6	DMA_TCD7_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_90F8	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD7_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_90FC	TCD Control and Status (DMA_TCD7_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_90FE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD7_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_90FE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD7_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9100	TCD Source Address (DMA_TCD8_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9104	TCD Signed Source Address Offset (DMA_TCD8_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9106	TCD Transfer Attributes (DMA_TCD8_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9108	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD8_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9108	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD8_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610

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DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_9108	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD8_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_910C	TCD Last Source Address Adjustment (DMA_TCD8_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9110	TCD Destination Address (DMA_TCD8_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9114	TCD Signed Destination Address Offset (DMA_TCD8_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9116	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD8_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9116	DMA_TCD8_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9118	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD8_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_911C	TCD Control and Status (DMA_TCD8_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_911E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD8_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_911E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD8_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9120	TCD Source Address (DMA_TCD9_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9124	TCD Signed Source Address Offset (DMA_TCD9_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9126	TCD Transfer Attributes (DMA_TCD9_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9128	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD9_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9128	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD9_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9128	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD9_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_912C	TCD Last Source Address Adjustment (DMA_TCD9_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9130	TCD Destination Address (DMA_TCD9_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9134	TCD Signed Destination Address Offset (DMA_TCD9_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9136	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD9_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9136	DMA_TCD9_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615

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DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_9138	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD9_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_913C	TCD Control and Status (DMA_TCD9_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_913E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD9_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_913E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD9_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9140	TCD Source Address (DMA_TCD10_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9144	TCD Signed Source Address Offset (DMA_TCD10_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9146	TCD Transfer Attributes (DMA_TCD10_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9148	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD10_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9148	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD10_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9148	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD10_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_914C	TCD Last Source Address Adjustment (DMA_TCD10_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9150	TCD Destination Address (DMA_TCD10_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9154	TCD Signed Destination Address Offset (DMA_TCD10_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9156	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD10_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9156	DMA_TCD10_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9158	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD10_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_915C	TCD Control and Status (DMA_TCD10_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_915E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD10_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_915E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD10_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9160	TCD Source Address (DMA_TCD11_SADDR)	32	R/W	Undefined	26.3.18/ 607

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DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_9164	TCD Signed Source Address Offset (DMA_TCD11_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9166	TCD Transfer Attributes (DMA_TCD11_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9168	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD11_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9168	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD11_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9168	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD11_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_916C	TCD Last Source Address Adjustment (DMA_TCD11_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9170	TCD Destination Address (DMA_TCD11_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9174	TCD Signed Destination Address Offset (DMA_TCD11_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9176	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD11_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9176	DMA_TCD11_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9178	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD11_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_917C	TCD Control and Status (DMA_TCD11_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_917E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD11_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_917E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD11_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9180	TCD Source Address (DMA_TCD12_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9184	TCD Signed Source Address Offset (DMA_TCD12_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9186	TCD Transfer Attributes (DMA_TCD12_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9188	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD12_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9188	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD12_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9188	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD12_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611

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DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_918C	TCD Last Source Address Adjustment (DMA_TCD12_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9190	TCD Destination Address (DMA_TCD12_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9194	TCD Signed Destination Address Offset (DMA_TCD12_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9196	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD12_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9196	DMA_TCD12_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9198	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD12_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_919C	TCD Control and Status (DMA_TCD12_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_919E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD12_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_919E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD12_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_91A0	TCD Source Address (DMA_TCD13_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_91A4	TCD Signed Source Address Offset (DMA_TCD13_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_91A6	TCD Transfer Attributes (DMA_TCD13_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_91A8	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD13_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_91A8	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD13_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_91A8	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD13_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_91AC	TCD Last Source Address Adjustment (DMA_TCD13_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_91B0	TCD Destination Address (DMA_TCD13_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_91B4	TCD Signed Destination Address Offset (DMA_TCD13_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_91B6	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD13_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_91B6	DMA_TCD13_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_91B8	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD13_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616

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DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_91BC	TCD Control and Status (DMA_TCD13_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_91BE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD13_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_91BE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD13_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_91C0	TCD Source Address (DMA_TCD14_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_91C4	TCD Signed Source Address Offset (DMA_TCD14_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_91C6	TCD Transfer Attributes (DMA_TCD14_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_91C8	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD14_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_91C8	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD14_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_91C8	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD14_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_91CC	TCD Last Source Address Adjustment (DMA_TCD14_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_91D0	TCD Destination Address (DMA_TCD14_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_91D4	TCD Signed Destination Address Offset (DMA_TCD14_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_91D6	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD14_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_91D6	DMA_TCD14_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_91D8	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD14_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_91DC	TCD Control and Status (DMA_TCD14_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_91DE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD14_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_91DE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD14_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_91E0	TCD Source Address (DMA_TCD15_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_91E4	TCD Signed Source Address Offset (DMA_TCD15_SOFF)	16	R/W	Undefined	26.3.19/ 608

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_91E6	TCD Transfer Attributes (DMA_TCD15_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_91E8	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD15_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_91E8	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD15_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_91E8	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD15_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_91EC	TCD Last Source Address Adjustment (DMA_TCD15_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_91F0	TCD Destination Address (DMA_TCD15_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_91F4	TCD Signed Destination Address Offset (DMA_TCD15_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_91F6	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD15_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_91F6	DMA_TCD15_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_91F8	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD15_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_91FC	TCD Control and Status (DMA_TCD15_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_91FE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD15_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_91FE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD15_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9200	TCD Source Address (DMA_TCD16_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9204	TCD Signed Source Address Offset (DMA_TCD16_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9206	TCD Transfer Attributes (DMA_TCD16_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9208	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD16_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9208	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD16_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9208	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD16_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_920C	TCD Last Source Address Adjustment (DMA_TCD16_SLAST)	32	R/W	Undefined	26.3.24/ 613

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_9210	TCD Destination Address (DMA_TCD16_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9214	TCD Signed Destination Address Offset (DMA_TCD16_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9216	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD16_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9216	DMA_TCD16_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9218	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD16_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_921C	TCD Control and Status (DMA_TCD16_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_921E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD16_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_921E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD16_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9220	TCD Source Address (DMA_TCD17_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9224	TCD Signed Source Address Offset (DMA_TCD17_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9226	TCD Transfer Attributes (DMA_TCD17_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9228	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD17_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9228	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD17_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9228	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD17_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_922C	TCD Last Source Address Adjustment (DMA_TCD17_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9230	TCD Destination Address (DMA_TCD17_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9234	TCD Signed Destination Address Offset (DMA_TCD17_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9236	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD17_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9236	DMA_TCD17_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9238	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD17_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_923C	TCD Control and Status (DMA_TCD17_CSR)	16	R/W	Undefined	26.3.30/ 617

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_923E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD17_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_923E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD17_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9240	TCD Source Address (DMA_TCD18_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9244	TCD Signed Source Address Offset (DMA_TCD18_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9246	TCD Transfer Attributes (DMA_TCD18_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9248	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD18_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9248	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD18_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9248	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD18_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_924C	TCD Last Source Address Adjustment (DMA_TCD18_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9250	TCD Destination Address (DMA_TCD18_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9254	TCD Signed Destination Address Offset (DMA_TCD18_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9256	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD18_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9256	DMA_TCD18_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9258	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD18_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_925C	TCD Control and Status (DMA_TCD18_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_925E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD18_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_925E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD18_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9260	TCD Source Address (DMA_TCD19_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9264	TCD Signed Source Address Offset (DMA_TCD19_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9266	TCD Transfer Attributes (DMA_TCD19_ATTR)	16	R/W	Undefined	26.3.20/ 608

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DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_9268	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD19_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9268	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD19_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9268	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD19_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_926C	TCD Last Source Address Adjustment (DMA_TCD19_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9270	TCD Destination Address (DMA_TCD19_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9274	TCD Signed Destination Address Offset (DMA_TCD19_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9276	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD19_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9276	DMA_TCD19_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9278	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD19_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_927C	TCD Control and Status (DMA_TCD19_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_927E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD19_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_927E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD19_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9280	TCD Source Address (DMA_TCD20_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9284	TCD Signed Source Address Offset (DMA_TCD20_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9286	TCD Transfer Attributes (DMA_TCD20_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9288	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD20_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9288	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD20_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9288	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD20_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_928C	TCD Last Source Address Adjustment (DMA_TCD20_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9290	TCD Destination Address (DMA_TCD20_DADDR)	32	R/W	Undefined	26.3.25/ 613

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DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_9294	TCD Signed Destination Address Offset (DMA_TCD20_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9296	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD20_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9296	DMA_TCD20_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9298	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD20_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_929C	TCD Control and Status (DMA_TCD20_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_929E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD20_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_929E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD20_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_92A0	TCD Source Address (DMA_TCD21_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_92A4	TCD Signed Source Address Offset (DMA_TCD21_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_92A6	TCD Transfer Attributes (DMA_TCD21_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_92A8	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD21_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_92A8	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD21_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_92A8	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD21_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_92AC	TCD Last Source Address Adjustment (DMA_TCD21_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_92B0	TCD Destination Address (DMA_TCD21_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_92B4	TCD Signed Destination Address Offset (DMA_TCD21_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_92B6	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD21_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_92B6	DMA_TCD21_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_92B8	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD21_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_92BC	TCD Control and Status (DMA_TCD21_CSR)	16	R/W	Undefined	26.3.30/ 617

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DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_92BE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD21_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_92BE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD21_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_92C0	TCD Source Address (DMA_TCD22_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_92C4	TCD Signed Source Address Offset (DMA_TCD22_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_92C6	TCD Transfer Attributes (DMA_TCD22_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_92C8	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD22_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_92C8	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD22_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_92C8	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD22_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_92CC	TCD Last Source Address Adjustment (DMA_TCD22_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_92D0	TCD Destination Address (DMA_TCD22_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_92D4	TCD Signed Destination Address Offset (DMA_TCD22_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_92D6	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD22_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_92D6	DMA_TCD22_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_92D8	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD22_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_92DC	TCD Control and Status (DMA_TCD22_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_92DE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD22_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_92DE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD22_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_92E0	TCD Source Address (DMA_TCD23_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_92E4	TCD Signed Source Address Offset (DMA_TCD23_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_92E6	TCD Transfer Attributes (DMA_TCD23_ATTR)	16	R/W	Undefined	26.3.20/ 608

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DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_92E8	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD23_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_92E8	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD23_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_92E8	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD23_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_92EC	TCD Last Source Address Adjustment (DMA_TCD23_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_92F0	TCD Destination Address (DMA_TCD23_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_92F4	TCD Signed Destination Address Offset (DMA_TCD23_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_92F6	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD23_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_92F6	DMA_TCD23_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_92F8	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD23_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_92FC	TCD Control and Status (DMA_TCD23_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_92FE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD23_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_92FE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD23_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9300	TCD Source Address (DMA_TCD24_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9304	TCD Signed Source Address Offset (DMA_TCD24_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9306	TCD Transfer Attributes (DMA_TCD24_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9308	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD24_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9308	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD24_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9308	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD24_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_930C	TCD Last Source Address Adjustment (DMA_TCD24_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9310	TCD Destination Address (DMA_TCD24_DADDR)	32	R/W	Undefined	26.3.25/ 613

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DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_9314	TCD Signed Destination Address Offset (DMA_TCD24_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9316	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD24_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9316	DMA_TCD24_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9318	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD24_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_931C	TCD Control and Status (DMA_TCD24_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_931E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD24_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_931E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD24_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9320	TCD Source Address (DMA_TCD25_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9324	TCD Signed Source Address Offset (DMA_TCD25_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9326	TCD Transfer Attributes (DMA_TCD25_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9328	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD25_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9328	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD25_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9328	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD25_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_932C	TCD Last Source Address Adjustment (DMA_TCD25_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9330	TCD Destination Address (DMA_TCD25_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9334	TCD Signed Destination Address Offset (DMA_TCD25_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9336	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD25_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9336	DMA_TCD25_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9338	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD25_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_933C	TCD Control and Status (DMA_TCD25_CSR)	16	R/W	Undefined	26.3.30/ 617

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DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_933E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD25_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_933E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD25_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9340	TCD Source Address (DMA_TCD26_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9344	TCD Signed Source Address Offset (DMA_TCD26_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9346	TCD Transfer Attributes (DMA_TCD26_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9348	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD26_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9348	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD26_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9348	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD26_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_934C	TCD Last Source Address Adjustment (DMA_TCD26_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9350	TCD Destination Address (DMA_TCD26_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9354	TCD Signed Destination Address Offset (DMA_TCD26_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9356	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD26_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9356	DMA_TCD26_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9358	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD26_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_935C	TCD Control and Status (DMA_TCD26_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_935E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD26_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_935E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD26_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9360	TCD Source Address (DMA_TCD27_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9364	TCD Signed Source Address Offset (DMA_TCD27_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9366	TCD Transfer Attributes (DMA_TCD27_ATTR)	16	R/W	Undefined	26.3.20/ 608

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_9368	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD27_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9368	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD27_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9368	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD27_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_936C	TCD Last Source Address Adjustment (DMA_TCD27_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9370	TCD Destination Address (DMA_TCD27_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_9374	TCD Signed Destination Address Offset (DMA_TCD27_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9376	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD27_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9376	DMA_TCD27_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9378	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD27_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_937C	TCD Control and Status (DMA_TCD27_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_937E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD27_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_937E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD27_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_9380	TCD Source Address (DMA_TCD28_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_9384	TCD Signed Source Address Offset (DMA_TCD28_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_9386	TCD Transfer Attributes (DMA_TCD28_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_9388	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD28_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_9388	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD28_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_9388	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD28_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_938C	TCD Last Source Address Adjustment (DMA_TCD28_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_9390	TCD Destination Address (DMA_TCD28_DADDR)	32	R/W	Undefined	26.3.25/ 613

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_9394	TCD Signed Destination Address Offset (DMA_TCD28_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_9396	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD28_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_9396	DMA_TCD28_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_9398	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD28_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_939C	TCD Control and Status (DMA_TCD28_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_939E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD28_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_939E	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD28_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_93A0	TCD Source Address (DMA_TCD29_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_93A4	TCD Signed Source Address Offset (DMA_TCD29_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_93A6	TCD Transfer Attributes (DMA_TCD29_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_93A8	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD29_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_93A8	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD29_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_93A8	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD29_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_93AC	TCD Last Source Address Adjustment (DMA_TCD29_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_93B0	TCD Destination Address (DMA_TCD29_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_93B4	TCD Signed Destination Address Offset (DMA_TCD29_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_93B6	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD29_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_93B6	DMA_TCD29_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_93B8	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD29_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_93BC	TCD Control and Status (DMA_TCD29_CSR)	16	R/W	Undefined	26.3.30/ 617

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_93BE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD29_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_93BE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD29_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_93C0	TCD Source Address (DMA_TCD30_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_93C4	TCD Signed Source Address Offset (DMA_TCD30_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_93C6	TCD Transfer Attributes (DMA_TCD30_ATTR)	16	R/W	Undefined	26.3.20/ 608
4000_93C8	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD30_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_93C8	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD30_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_93C8	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD30_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_93CC	TCD Last Source Address Adjustment (DMA_TCD30_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_93D0	TCD Destination Address (DMA_TCD30_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_93D4	TCD Signed Destination Address Offset (DMA_TCD30_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_93D6	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD30_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_93D6	DMA_TCD30_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_93D8	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD30_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_93DC	TCD Control and Status (DMA_TCD30_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_93DE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD30_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_93DE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD30_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620
4000_93E0	TCD Source Address (DMA_TCD31_SADDR)	32	R/W	Undefined	26.3.18/ 607
4000_93E4	TCD Signed Source Address Offset (DMA_TCD31_SOFF)	16	R/W	Undefined	26.3.19/ 608
4000_93E6	TCD Transfer Attributes (DMA_TCD31_ATTR)	16	R/W	Undefined	26.3.20/ 608

Table continues on the next page...

DMA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_93E8	TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD31_NBYTES_MLNO)	32	R/W	Undefined	26.3.21/ 609
4000_93E8	TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD31_NBYTES_MLOFFNO)	32	R/W	Undefined	26.3.22/ 610
4000_93E8	TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD31_NBYTES_MLOFFYES)	32	R/W	Undefined	26.3.23/ 611
4000_93EC	TCD Last Source Address Adjustment (DMA_TCD31_SLAST)	32	R/W	Undefined	26.3.24/ 613
4000_93F0	TCD Destination Address (DMA_TCD31_DADDR)	32	R/W	Undefined	26.3.25/ 613
4000_93F4	TCD Signed Destination Address Offset (DMA_TCD31_DOFF)	16	R/W	Undefined	26.3.26/ 614
4000_93F6	TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD31_CITER_ELINKYES)	16	R/W	Undefined	26.3.27/ 614
4000_93F6	DMA_TCD31_CITER_ELINKNO	16	R/W	Undefined	26.3.28/ 615
4000_93F8	TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD31_DLASTSGA)	32	R/W	Undefined	26.3.29/ 616
4000_93FC	TCD Control and Status (DMA_TCD31_CSR)	16	R/W	Undefined	26.3.30/ 617
4000_93FE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD31_BITER_ELINKYES)	16	R/W	Undefined	26.3.31/ 619
4000_93FE	TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD31_BITER_ELINKNO)	16	R/W	Undefined	26.3.32/ 620

26.3.1 Control Register (DMA_CR)

The CR defines the basic operating configuration of the DMA. The DMA arbitrates channel service requests in two groups of 16 channels each:

- Group 1 contains channels 31-16
- Group 0 contains channels 15-0

Arbitration within a group can be configured to use either a fixed-priority or a round-robin scheme. For fixed-priority arbitration, the highest priority channel requesting service is selected to execute. The channel priority registers assign the priorities; see the DCHPRIn registers. For round-robin arbitration, the channel priorities are ignored and channels within each group are cycled through (from high to low channel number) without regard to priority.

NOTE

For correct operation, writes to the CR register must be performed only when the DMA channels are inactive; that is, when TCDn_CSR[ACTIVE] bits are cleared.

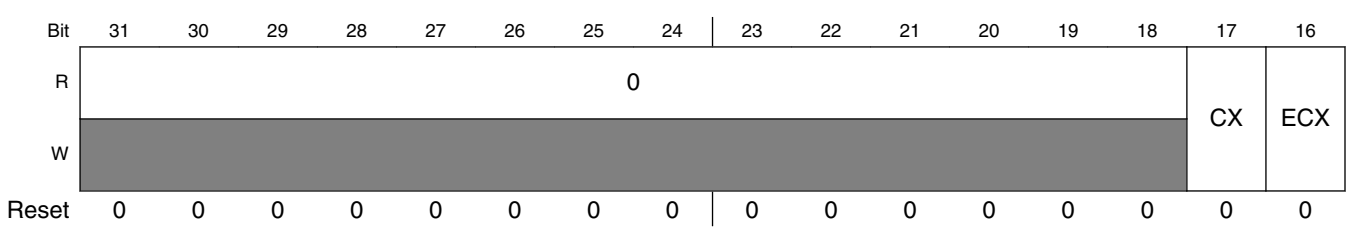
The group priorities operate in a similar fashion. In group fixed priority arbitration mode, channel service requests in the highest priority group are executed first, where priority level 1 is the highest and priority level 0 is the lowest. The group priorities are assigned in the GRPnPRI fields of the DMA Control Register (CR). All group priorities must have unique values prior to any channel service requests occurring; otherwise, a configuration error will be reported. For group round robin arbitration, the group priorities are ignored and the groups are cycled through (from high to low group number) without regard to priority.

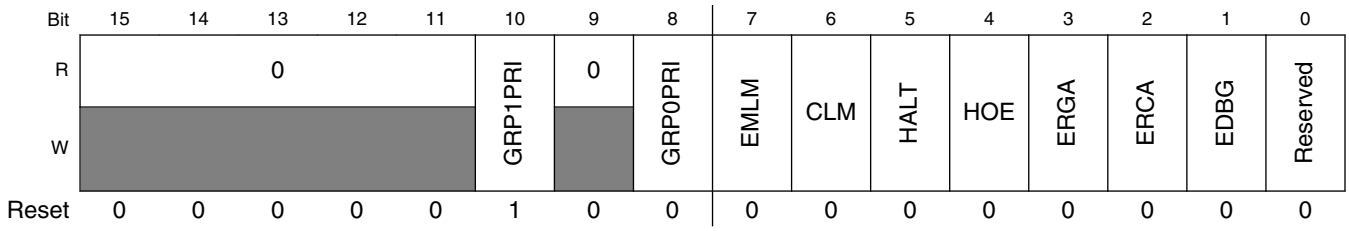
Minor loop offsets are address offset values added to the final source address (TCDn_SADDR) or destination address (TCDn_DADDR) upon minor loop completion. When minor loop offsets are enabled, the minor loop offset (MLOFF) is added to the final source address (TCDn_SADDR), to the final destination address (TCDn_DADDR), or to both prior to the addresses being written back into the TCD. If the major loop is complete, the minor loop offset is ignored and the major loop address offsets (TCDn_SLAST and TCDn_DLAST_SGA) are used to compute the next TCDn_SADDR and TCDn_DADDR values.

When minor loop mapping is enabled (EMLM is 1), TCDn word2 is redefined. A portion of TCDn word2 is used to specify multiple fields: a source enable bit (SMLOE) to specify the minor loop offset should be applied to the source address (TCDn_SADDR) upon minor loop completion, a destination enable bit (DMLOE) to specify the minor loop offset should be applied to the destination address (TCDn_DADDR) upon minor loop completion, and the sign extended minor loop offset value (MLOFF). The same offset value (MLOFF) is used for both source and destination minor loop offsets. When either minor loop offset is enabled (SMLOE set or DMLOE set), the NBYTES field is reduced to 10 bits. When both minor loop offsets are disabled (SMLOE cleared and DMLOE cleared), the NBYTES field is a 30-bit vector.

When minor loop mapping is disabled (EMLM is 0), all 32 bits of TCDn word2 are assigned to the NBYTES field.

Address: 4000_8000h base + 0h offset = 4000_8000h





DMA_CR field descriptions

Field	Description
31–18 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
17 CX	Cancel Transfer 0 Normal operation 1 Cancel the remaining data transfer. Stop the executing channel and force the minor loop to finish. The cancel takes effect after the last write of the current read/write sequence. The CX bit clears itself after the cancel has been honored. This cancel retires the channel normally as if the minor loop was completed.
16 ECX	Error Cancel Transfer 0 Normal operation 1 Cancel the remaining data transfer in the same fashion as the CX bit. Stop the executing channel and force the minor loop to finish. The cancel takes effect after the last write of the current read/write sequence. The ECX bit clears itself after the cancel is honored. In addition to cancelling the transfer, ECX treats the cancel as an error condition, thus updating the Error Status register (DMAx_ES) and generating an optional error interrupt.
15–11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10 GRP1PRI	Channel Group 1 Priority Group 1 priority level when fixed priority group arbitration is enabled.
9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 GRP0PRI	Channel Group 0 Priority Group 0 priority level when fixed priority group arbitration is enabled.
7 EMLM	Enable Minor Loop Mapping 0 Disabled. TCDn.word2 is defined as a 32-bit NBYTES field. 1 Enabled. TCDn.word2 is redefined to include individual enable fields, an offset field, and the NBYTES field. The individual enable fields allow the minor loop offset to be applied to the source address, the destination address, or both. The NBYTES field is reduced when either offset is enabled.
6 CLM	Continuous Link Mode **NOTE:** Do not use continuous link mode with a channel linking to itself if there is only one minor loop iteration per service request, e.g., if the channel's NBYTES value is the same as either the source or destination size. The same data transfer profile can be achieved by simply increasing the NBYTES value, which provides more efficient, faster processing.

Table continues on the next page...

DMA_CR field descriptions (continued)

Field	Description
	0 A minor loop channel link made to itself goes through channel arbitration before being activated again. 1 A minor loop channel link made to itself does not go through channel arbitration before being activated again. Upon minor loop completion, the channel activates again if that channel has a minor loop channel link enabled and the link channel is itself. This effectively applies the minor loop offsets and restarts the next minor loop.
5 HALT	Halt DMA Operations 0 Normal operation 1 Stall the start of any new channels. Executing channels are allowed to complete. Channel execution resumes when this bit is cleared.
4 HOE	Halt On Error 0 Normal operation 1 Any error causes the HALT bit to set. Subsequently, all service requests are ignored until the HALT bit is cleared.
3 ERGA	Enable Round Robin Group Arbitration 0 Fixed priority arbitration is used for selection among the groups. 1 Round robin arbitration is used for selection among the groups.
2 ERCA	Enable Round Robin Channel Arbitration 0 Fixed priority arbitration is used for channel selection within each group. 1 Round robin arbitration is used for channel selection within each group.
1 EDBG	Enable Debug 0 When in debug mode, the DMA continues to operate. 1 When in debug mode, the DMA stalls the start of a new channel. Executing channels are allowed to complete. Channel execution resumes when the system exits debug mode or the EDBG bit is cleared.
0 Reserved	This field is reserved. Reserved

26.3.2 Error Status Register (DMA_ES)

The ES provides information concerning the last recorded channel error. Channel errors can be caused by:

- A configuration error, that is:
  - An illegal setting in the transfer-control descriptor, or
  - An illegal priority register setting in fixed-arbitration
- An error termination to a bus master read or write cycle
- A bit in the ES shows an uncorrectable error occurred while the device has ECC protection on the TCD SRAM
- A cancel transfer with error bit that will be set when a transfer is canceled via the corresponding cancel transfer control bit

See the Error Reporting and Handling section for more details.

Address: 4000_8000h base + 4h offset = 4000_8004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	VLD	0														ECX
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	GPE	CPE	0	ERRCHN					SAE	SOE	DAE	DOE	NCE	SGE	SBE	DBE
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_ES field descriptions

Field	Description
31 VLD	Logical OR of all ERR status bits 0 No ERR bits are set. 1 At least one ERR bit is set indicating a valid error exists that has not been cleared.
30–17 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
16 ECX	Transfer Canceled 0 No canceled transfers 1 The last recorded entry was a canceled transfer by the error cancel transfer input
15 GPE	Group Priority Error 0 No group priority error 1 The last recorded error was a configuration error among the group priorities. All group priorities are not unique.
14 CPE	Channel Priority Error 0 No channel priority error 1 The last recorded error was a configuration error in the channel priorities within a group. Channel priorities within a group are not unique.
13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12–8 ERRCHN	Error Channel Number or Canceled Channel Number The channel number of the last recorded error, excluding GPE and CPE errors, or last recorded error canceled transfer.
7 SAE	Source Address Error 0 No source address configuration error. 1 The last recorded error was a configuration error detected in the TCDn_SADDR field. TCDn_SADDR is inconsistent with TCDn_ATTR[SSIZE].
6 SOE	Source Offset Error 0 No source offset configuration error 1 The last recorded error was a configuration error detected in the TCDn_SOFF field. TCDn_SOFF is inconsistent with TCDn_ATTR[SSIZE].

Table continues on the next page...

DMA_ES field descriptions (continued)

Field	Description
5 DAE	Destination Address Error 0 No destination address configuration error 1 The last recorded error was a configuration error detected in the TCDn_DADDR field. TCDn_DADDR is inconsistent with TCDn_ATTR[DSIZE].
4 DOE	Destination Offset Error 0 No destination offset configuration error 1 The last recorded error was a configuration error detected in the TCDn_DOFF field. TCDn_DOFF is inconsistent with TCDn_ATTR[DSIZE].
3 NCE	NBYTES/CITER Configuration Error 0 No NBYTES/CITER configuration error 1 The last recorded error was a configuration error detected in the TCDn_NBYTES or TCDn_CITER fields. • TCDn_NBYTES is not a multiple of TCDn_ATTR[SSIZE] and TCDn_ATTR[DSIZE], or • TCDn_CITER[CITER] is equal to zero, or • TCDn_CITER[ELINK] is not equal to TCDn_BITER[ELINK]
2 SGE	Scatter/Gather Configuration Error 0 No scatter/gather configuration error 1 The last recorded error was a configuration error detected in the TCDn_DLASTSGA field. This field is checked at the beginning of a scatter/gather operation after major loop completion if TCDn_CSR[ESG] is enabled. TCDn_DLASTSGA is not on a 32 byte boundary.
1 SBE	Source Bus Error 0 No source bus error 1 The last recorded error was a bus error on a source read
0 DBE	Destination Bus Error 0 No destination bus error 1 The last recorded error was a bus error on a destination write

26.3.3 Enable Request Register (DMA_ERQ)

The ERQ register provides a bit map for the 32 channels to enable the request signal for each channel. The state of any given channel enable is directly affected by writes to this register; it is also affected by writes to the SERQ and CERQ registers. These registers are provided so the request enable for a single channel can easily be modified without needing to perform a read-modify-write sequence to the ERQ.

DMA request input signals and this enable request flag must be asserted before a channel's hardware service request is accepted. The state of the DMA enable request flag does not affect a channel service request made explicitly through software or a linked channel request.

Address: 4000_8000h base + Ch offset = 4000_800Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	ERQ31	ERQ30	ERQ29	ERQ28	ERQ27	ERQ26	ERQ25	ERQ24	ERQ23	ERQ22	ERQ21	ERQ20	ERQ19	ERQ18	ERQ17	ERQ16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	ERQ15	ERQ14	ERQ13	ERQ12	ERQ11	ERQ10	ERQ9	ERQ8	ERQ7	ERQ6	ERQ5	ERQ4	ERQ3	ERQ2	ERQ1	ERQ0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_ERQ field descriptions

Field	Description
31 ERQ31	Enable DMA Request 31 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
30 ERQ30	Enable DMA Request 30 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
29 ERQ29	Enable DMA Request 29 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
28 ERQ28	Enable DMA Request 28 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
27 ERQ27	Enable DMA Request 27 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
26 ERQ26	Enable DMA Request 26 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
25 ERQ25	Enable DMA Request 25 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
24 ERQ24	Enable DMA Request 24 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled

Table continues on the next page...

DMA_ERQ field descriptions (continued)

Field	Description
23 ERQ23	Enable DMA Request 23 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
22 ERQ22	Enable DMA Request 22 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
21 ERQ21	Enable DMA Request 21 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
20 ERQ20	Enable DMA Request 20 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
19 ERQ19	Enable DMA Request 19 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
18 ERQ18	Enable DMA Request 18 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
17 ERQ17	Enable DMA Request 17 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
16 ERQ16	Enable DMA Request 16 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
15 ERQ15	Enable DMA Request 15 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
14 ERQ14	Enable DMA Request 14 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
13 ERQ13	Enable DMA Request 13 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
12 ERQ12	Enable DMA Request 12 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled

Table continues on the next page...

DMA_ERQ field descriptions (continued)

Field	Description
11 ERQ11	Enable DMA Request 11 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
10 ERQ10	Enable DMA Request 10 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
9 ERQ9	Enable DMA Request 9 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
8 ERQ8	Enable DMA Request 8 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
7 ERQ7	Enable DMA Request 7 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
6 ERQ6	Enable DMA Request 6 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
5 ERQ5	Enable DMA Request 5 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
4 ERQ4	Enable DMA Request 4 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
3 ERQ3	Enable DMA Request 3 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
2 ERQ2	Enable DMA Request 2 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
1 ERQ1	Enable DMA Request 1 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled
0 ERQ0	Enable DMA Request 0 0 The DMA request signal for the corresponding channel is disabled 1 The DMA request signal for the corresponding channel is enabled

26.3.4 Enable Error Interrupt Register (DMA_EEI)

The EEI register provides a bit map for the 32 channels to enable the error interrupt signal for each channel. The state of any given channel's error interrupt enable is directly affected by writes to this register; it is also affected by writes to the SEEI and CEEI. These registers are provided so that the error interrupt enable for a single channel can easily be modified without the need to perform a read-modify-write sequence to the EEI register.

The DMA error indicator and the error interrupt enable flag must be asserted before an error interrupt request for a given channel is asserted to the interrupt controller.

Address: 4000_8000h base + 14h offset = 4000_8014h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	EEI31	EEI30	EEI29	EEI28	EEI27	EEI26	EEI25	EEI24	EEI23	EEI22	EEI21	EEI20	EEI19	EEI18	EEI17	EEI16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	EEI15	EEI14	EEI13	EEI12	EEI11	EEI10	EEI9	EEI8	EEI7	EEI6	EEI5	EEI4	EEI3	EEI2	EEI1	EEI0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_EEI field descriptions

Field	Description
31 EEI31	Enable Error Interrupt 31 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
30 EEI30	Enable Error Interrupt 30 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
29 EEI29	Enable Error Interrupt 29 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
28 EEI28	Enable Error Interrupt 28 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request

Table continues on the next page...

DMA_EEI field descriptions (continued)

Field	Description
27 EEI27	Enable Error Interrupt 27 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
26 EEI26	Enable Error Interrupt 26 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
25 EEI25	Enable Error Interrupt 25 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
24 EEI24	Enable Error Interrupt 24 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
23 EEI23	Enable Error Interrupt 23 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
22 EEI22	Enable Error Interrupt 22 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
21 EEI21	Enable Error Interrupt 21 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
20 EEI20	Enable Error Interrupt 20 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
19 EEI19	Enable Error Interrupt 19 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
18 EEI18	Enable Error Interrupt 18 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
17 EEI17	Enable Error Interrupt 17 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
16 EEI16	Enable Error Interrupt 16 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request

Table continues on the next page...

DMA_EEI field descriptions (continued)

Field	Description
15 EEI15	Enable Error Interrupt 15 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
14 EEI14	Enable Error Interrupt 14 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
13 EEI13	Enable Error Interrupt 13 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
12 EEI12	Enable Error Interrupt 12 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
11 EEI11	Enable Error Interrupt 11 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
10 EEI10	Enable Error Interrupt 10 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
9 EEI9	Enable Error Interrupt 9 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
8 EEI8	Enable Error Interrupt 8 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
7 EEI7	Enable Error Interrupt 7 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
6 EEI6	Enable Error Interrupt 6 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
5 EEI5	Enable Error Interrupt 5 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
4 EEI4	Enable Error Interrupt 4 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request

Table continues on the next page...

DMA_EEI field descriptions (continued)

Field	Description
3 EEI3	Enable Error Interrupt 3 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
2 EEI2	Enable Error Interrupt 2 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
1 EEI1	Enable Error Interrupt 1 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request
0 EEI0	Enable Error Interrupt 0 0 The error signal for corresponding channel does not generate an error interrupt 1 The assertion of the error signal for corresponding channel generates an error interrupt request

26.3.5 Clear Enable Error Interrupt Register (DMA_CEEI)

The CEEI provides a simple memory-mapped mechanism to clear a given bit in the EEI to disable the error interrupt for a given channel. The data value on a register write causes the corresponding bit in the EEI to be cleared. Setting the CAEE bit provides a global clear function, forcing the EEI contents to be cleared, disabling all DMA request inputs. If the NOP bit is set, the command is ignored. This allows you to write multiple-byte registers as a 32-bit word. Reads of this register return all zeroes.

Address: 4000_8000h base + 18h offset = 4000_8018h

Bit	7	6	5	4	3	2	1	0
Read	0	0				0		
Write	NOP	CAEE	0			CEEI		
Reset	0	0	0	0	0	0	0	0

DMA_CEEI field descriptions

Field	Description
7 NOP	No Op enable 0 Normal operation 1 No operation, ignore the other bits in this register
6 CAEE	Clear All Enable Error Interrupts

Table continues on the next page...

DMA_CEEI field descriptions (continued)

Field	Description
	0 Clear only the EEI bit specified in the CEEI field 1 Clear all bits in EEI
5 Reserved	This field is reserved.
CEEI	Clear Enable Error Interrupt Clears the corresponding bit in EEI

26.3.6 Set Enable Error Interrupt Register (DMA_SEEI)

The SEEI provides a simple memory-mapped mechanism to set a given bit in the EEI to enable the error interrupt for a given channel. The data value on a register write causes the corresponding bit in the EEI to be set. Setting the SAEE bit provides a global set function, forcing the entire EEI contents to be set. If the NOP bit is set, the command is ignored. This allows you to write multiple-byte registers as a 32-bit word. Reads of this register return all zeroes.

Address: 4000_8000h base + 19h offset = 4000_8019h

Bit	7	6	5	4	3	2	1	0
Read	0	0		0				
Write	NOP	SAEE	0	SEEI				
Reset	0	0	0	0	0	0	0	0

DMA_SEEI field descriptions

Field	Description
7 NOP	No Op enable 0 Normal operation 1 No operation, ignore the other bits in this register
6 SAEE	Sets All Enable Error Interrupts 0 Set only the EEI bit specified in the SEEI field. 1 Sets all bits in EEI
5 Reserved	This field is reserved.
SEEI	Set Enable Error Interrupt Sets the corresponding bit in EEI

26.3.7 Clear Enable Request Register (DMA_CERQ)

The CERQ provides a simple memory-mapped mechanism to clear a given bit in the ERQ to disable the DMA request for a given channel. The data value on a register write causes the corresponding bit in the ERQ to be cleared. Setting the CAER bit provides a global clear function, forcing the entire contents of the ERQ to be cleared, disabling all DMA request inputs. If NOP is set, the command is ignored. This allows you to write multiple-byte registers as a 32-bit word. Reads of this register return all zeroes.

Address: 4000_8000h base + 1Ah offset = 4000_801Ah

Bit	7	6	5	4	3	2	1	0
Read	0	0		0				
Write	NOP	CAER	0	CERQ				
Reset	0	0	0	0	0	0	0	0

DMA_CERQ field descriptions

Field	Description
7 NOP	No Op enable 0 Normal operation 1 No operation, ignore the other bits in this register
6 CAER	Clear All Enable Requests 0 Clear only the ERQ bit specified in the CERQ field 1 Clear all bits in ERQ
5 Reserved	This field is reserved.
CERQ	Clear Enable Request Clears the corresponding bit in ERQ.

26.3.8 Set Enable Request Register (DMA_SERQ)

The SERQ provides a simple memory-mapped mechanism to set a given bit in the ERQ to enable the DMA request for a given channel. The data value on a register write causes the corresponding bit in the ERQ to be set. Setting the SAER bit provides a global set function, forcing the entire contents of ERQ to be set. If the NOP bit is set, the command is ignored. This allows you to write multiple-byte registers as a 32-bit word. Reads of this register return all zeroes.

Address: 4000_8000h base + 1Bh offset = 4000_801Bh

Bit	7	6	5	4	3	2	1	0
Read	0	0		0				
Write	NOP	SAER	0	SERQ				
Reset	0	0	0	0	0	0	0	0

DMA_SERQ field descriptions

Field	Description
7 NOP	No Op enable 0 Normal operation 1 No operation, ignore the other bits in this register
6 SAER	Set All Enable Requests 0 Set only the ERQ bit specified in the SERQ field 1 Set all bits in ERQ
5 Reserved	This field is reserved.
SERQ	Set Enable Request Sets the corresponding bit in ERQ.

26.3.9 Clear DONE Status Bit Register (DMA_CDNE)

The CDNE provides a simple memory-mapped mechanism to clear the DONE bit in the TCD of the given channel. The data value on a register write causes the DONE bit in the corresponding transfer control descriptor to be cleared. Setting the CADN bit provides a global clear function, forcing all DONE bits to be cleared. If the NOP bit is set, the command is ignored. This allows you to write multiple-byte registers as a 32-bit word. Reads of this register return all zeroes.

Address: 4000_8000h base + 1Ch offset = 4000_801Ch

Bit	7	6	5	4	3	2	1	0
Read	0	0		0				
Write	NOP	CADN	0	CDNE				
Reset	0	0	0	0	0	0	0	0

DMA_CDNE field descriptions

Field	Description
7 NOP	No Op enable 0 Normal operation 1 No operation, ignore the other bits in this register
6 CADN	Clears All DONE Bits 0 Clears only the TCDn_CSR[DONE] bit specified in the CDNE field 1 Clears all bits in TCDn_CSR[DONE]
5 Reserved	This field is reserved.
CDNE	Clear DONE Bit Clears the corresponding bit in TCDn_CSR[DONE]

26.3.10 Set START Bit Register (DMA_SSRT)

The SSRT provides a simple memory-mapped mechanism to set the START bit in the TCD of the given channel. The data value on a register write causes the START bit in the corresponding transfer control descriptor to be set. Setting the SAST bit provides a global set function, forcing all START bits to be set. If the NOP bit is set, the command is ignored. This allows you to write multiple-byte registers as a 32-bit word. Reads of this register return all zeroes.

Address: 4000_8000h base + 1Dh offset = 4000_801Dh

Bit	7	6	5	4	3	2	1	0
Read	0	0				0		
Write	NOP	SAST	0			SSRT		
Reset	0	0	0	0	0	0	0	0

DMA_SSRT field descriptions

Field	Description
7 NOP	No Op enable 0 Normal operation 1 No operation, ignore the other bits in this register
6 SAST	Set All START Bits (activates all channels) 0 Set only the TCDn_CSR[START] bit specified in the SSRT field 1 Set all bits in TCDn_CSR[START]
5 Reserved	This field is reserved.
SSRT	Set START Bit Sets the corresponding bit in TCDn_CSR[START]

26.3.11 Clear Error Register (DMA_CERR)

The CERR provides a simple memory-mapped mechanism to clear a given bit in the ERR to disable the error condition flag for a given channel. The given value on a register write causes the corresponding bit in the ERR to be cleared. Setting the CAEI bit provides a global clear function, forcing the ERR contents to be cleared, clearing all channel error indicators. If the NOP bit is set, the command is ignored. This allows you to write multiple-byte registers as a 32-bit word. Reads of this register return all zeroes.

Address: 4000_8000h base + 1Eh offset = 4000_801Eh

Bit	7	6	5	4	3	2	1	0
Read	0	0		0				
Write	NOP	CAEI	0	CERR				
Reset	0	0	0	0	0	0	0	0

DMA_CERR field descriptions

Field	Description
7 NOP	No Op enable 0 Normal operation 1 No operation, ignore the other bits in this register
6 CAEI	Clear All Error Indicators 0 Clear only the ERR bit specified in the CERR field 1 Clear all bits in ERR
5 Reserved	This field is reserved.
CERR	Clear Error Indicator Clears the corresponding bit in ERR

26.3.12 Clear Interrupt Request Register (DMA_CINT)

The CINT provides a simple, memory-mapped mechanism to clear a given bit in the INT to disable the interrupt request for a given channel. The given value on a register write causes the corresponding bit in the INT to be cleared. Setting the CAIR bit provides a global clear function, forcing the entire contents of the INT to be cleared, disabling all DMA interrupt requests. If the NOP bit is set, the command is ignored. This allows you to write multiple-byte registers as a 32-bit word. Reads of this register return all zeroes.

Address: 4000_8000h base + 1Fh offset = 4000_801Fh

Bit	7	6	5	4	3	2	1	0
Read	0	0		0				
Write	NOP	CAIR	0	CINT				
Reset	0	0	0	0	0	0	0	0

DMA_CINT field descriptions

Field	Description
7 NOP	No Op enable 0 Normal operation 1 No operation, ignore the other bits in this register
6 CAIR	Clear All Interrupt Requests 0 Clear only the INT bit specified in the CINT field 1 Clear all bits in INT
5 Reserved	This field is reserved.
CINT	Clear Interrupt Request Clears the corresponding bit in INT

26.3.13 Interrupt Request Register (DMA_INT)

The INT register provides a bit map for the 32 channels signaling the presence of an interrupt request for each channel. Depending on the appropriate bit setting in the transfer-control descriptors, the eDMA engine generates an interrupt on data transfer completion. The outputs of this register are directly routed to the interrupt controller. During the interrupt-service routine associated with any given channel, it is the software's responsibility to clear the appropriate bit, negating the interrupt request. Typically, a write to the CINT register in the interrupt service routine is used for this purpose.

The state of any given channel's interrupt request is directly affected by writes to this register; it is also affected by writes to the CINT register. On writes to INT, a 1 in any bit position clears the corresponding channel's interrupt request. A zero in any bit position has no affect on the corresponding channel's current interrupt status. The CINT register is provided so the interrupt request for a single channel can easily be cleared without the need to perform a read-modify-write sequence to the INT register.

Address: 4000_8000h base + 24h offset = 4000_8024h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	INT31	INT30	INT29	INT28	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT20	INT19	INT18	INT17	INT16
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	INT15	INT14	INT13	INT12	INT11	INT10	INT9	INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_INT field descriptions

Field	Description
31 INT31	Interrupt Request 31

Table continues on the next page...

DMA_INT field descriptions (continued)

Field	Description
	0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
30 INT30	Interrupt Request 30 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
29 INT29	Interrupt Request 29 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
28 INT28	Interrupt Request 28 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
27 INT27	Interrupt Request 27 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
26 INT26	Interrupt Request 26 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
25 INT25	Interrupt Request 25 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
24 INT24	Interrupt Request 24 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
23 INT23	Interrupt Request 23 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
22 INT22	Interrupt Request 22 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
21 INT21	Interrupt Request 21 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
20 INT20	Interrupt Request 20 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
19 INT19	Interrupt Request 19

Table continues on the next page...

DMA_INT field descriptions (continued)

Field	Description
	0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
18 INT18	Interrupt Request 18 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
17 INT17	Interrupt Request 17 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
16 INT16	Interrupt Request 16 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
15 INT15	Interrupt Request 15 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
14 INT14	Interrupt Request 14 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
13 INT13	Interrupt Request 13 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
12 INT12	Interrupt Request 12 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
11 INT11	Interrupt Request 11 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
10 INT10	Interrupt Request 10 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
9 INT9	Interrupt Request 9 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
8 INT8	Interrupt Request 8 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
7 INT7	Interrupt Request 7

Table continues on the next page...

DMA_INT field descriptions (continued)

Field	Description
	0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
6 INT6	Interrupt Request 6 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
5 INT5	Interrupt Request 5 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
4 INT4	Interrupt Request 4 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
3 INT3	Interrupt Request 3 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
2 INT2	Interrupt Request 2 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
1 INT1	Interrupt Request 1 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active
0 INT0	Interrupt Request 0 0 The interrupt request for corresponding channel is cleared 1 The interrupt request for corresponding channel is active

26.3.14 Error Register (DMA_ERR)

The ERR provides a bit map for the 32 channels, signaling the presence of an error for each channel. The eDMA engine signals the occurrence of an error condition by setting the appropriate bit in this register. The outputs of this register are enabled by the contents of the EEI, then logically summed across groups of 16 and 32 channels to form several group error interrupt requests, which are then routed to the interrupt controller. During the execution of the interrupt-service routine associated with any DMA errors, it is software's responsibility to clear the appropriate bit, negating the error-interrupt request. Typically, a write to the CERR in the interrupt-service routine is used for this purpose. The normal DMA channel completion indicators (setting the transfer control descriptor DONE flag and the possible assertion of an interrupt request) are not affected when an error is detected.

The contents of this register can also be polled because a non-zero value indicates the presence of a channel error regardless of the state of the EEI. The state of any given channel's error indicators is affected by writes to this register; it is also affected by writes to the CERR. On writes to the ERR, a one in any bit position clears the corresponding channel's error status. A zero in any bit position has no affect on the corresponding channel's current error status. The CERR is provided so the error indicator for a single channel can easily be cleared.

Address: 4000_8000h base + 2Ch offset = 4000_802Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	ERR31	ERR30	ERR29	ERR28	ERR27	ERR26	ERR25	ERR24	ERR23	ERR22	ERR21	ERR20	ERR19	ERR18	ERR17	ERR16
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ERR15	ERR14	ERR13	ERR12	ERR11	ERR10	ERR9	ERR8	ERR7	ERR6	ERR5	ERR4	ERR3	ERR2	ERR1	ERR0
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_ERR field descriptions

Field	Description
31 ERR31	Error In Channel 31 0 An error in this channel has not occurred 1 An error in this channel has occurred
30 ERR30	Error In Channel 30 0 An error in this channel has not occurred 1 An error in this channel has occurred
29 ERR29	Error In Channel 29 0 An error in this channel has not occurred 1 An error in this channel has occurred
28 ERR28	Error In Channel 28 0 An error in this channel has not occurred 1 An error in this channel has occurred

Table continues on the next page...

DMA_ERR field descriptions (continued)

Field	Description
27 ERR27	Error In Channel 27 0 An error in this channel has not occurred 1 An error in this channel has occurred
26 ERR26	Error In Channel 26 0 An error in this channel has not occurred 1 An error in this channel has occurred
25 ERR25	Error In Channel 25 0 An error in this channel has not occurred 1 An error in this channel has occurred
24 ERR24	Error In Channel 24 0 An error in this channel has not occurred 1 An error in this channel has occurred
23 ERR23	Error In Channel 23 0 An error in this channel has not occurred 1 An error in this channel has occurred
22 ERR22	Error In Channel 22 0 An error in this channel has not occurred 1 An error in this channel has occurred
21 ERR21	Error In Channel 21 0 An error in this channel has not occurred 1 An error in this channel has occurred
20 ERR20	Error In Channel 20 0 An error in this channel has not occurred 1 An error in this channel has occurred
19 ERR19	Error In Channel 19 0 An error in this channel has not occurred 1 An error in this channel has occurred
18 ERR18	Error In Channel 18 0 An error in this channel has not occurred 1 An error in this channel has occurred
17 ERR17	Error In Channel 17 0 An error in this channel has not occurred 1 An error in this channel has occurred
16 ERR16	Error In Channel 16 0 An error in this channel has not occurred 1 An error in this channel has occurred

Table continues on the next page...

DMA_ERR field descriptions (continued)

Field	Description
15 ERR15	Error In Channel 15 0 An error in this channel has not occurred 1 An error in this channel has occurred
14 ERR14	Error In Channel 14 0 An error in this channel has not occurred 1 An error in this channel has occurred
13 ERR13	Error In Channel 13 0 An error in this channel has not occurred 1 An error in this channel has occurred
12 ERR12	Error In Channel 12 0 An error in this channel has not occurred 1 An error in this channel has occurred
11 ERR11	Error In Channel 11 0 An error in this channel has not occurred 1 An error in this channel has occurred
10 ERR10	Error In Channel 10 0 An error in this channel has not occurred 1 An error in this channel has occurred
9 ERR9	Error In Channel 9 0 An error in this channel has not occurred 1 An error in this channel has occurred
8 ERR8	Error In Channel 8 0 An error in this channel has not occurred 1 An error in this channel has occurred
7 ERR7	Error In Channel 7 0 An error in this channel has not occurred 1 An error in this channel has occurred
6 ERR6	Error In Channel 6 0 An error in this channel has not occurred 1 An error in this channel has occurred
5 ERR5	Error In Channel 5 0 An error in this channel has not occurred 1 An error in this channel has occurred
4 ERR4	Error In Channel 4 0 An error in this channel has not occurred 1 An error in this channel has occurred

Table continues on the next page...

DMA_ERR field descriptions (continued)

Field	Description
3 ERR3	Error In Channel 3 0 An error in this channel has not occurred 1 An error in this channel has occurred
2 ERR2	Error In Channel 2 0 An error in this channel has not occurred 1 An error in this channel has occurred
1 ERR1	Error In Channel 1 0 An error in this channel has not occurred 1 An error in this channel has occurred
0 ERR0	Error In Channel 0 0 An error in this channel has not occurred 1 An error in this channel has occurred

26.3.15 Hardware Request Status Register (DMA_HRS)

The HRS register provides a bit map for the DMA channels, signaling the presence of a hardware request for each channel. The hardware request status bits reflect the current state of the register and qualified (via the ERQ fields) DMA request signals as seen by the DMA's arbitration logic. This view into the hardware request signals may be used for debug purposes.

NOTE

These bits reflect the state of the request as seen by the arbitration logic. Therefore, this status is affected by the ERQ bits.

Address: 4000_8000h base + 34h offset = 4000_8034h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	HRS31	HRS30	HRS29	HRS28	HRS27	HRS26	HRS25	HRS24	HRS23	HRS22	HRS21	HRS20	HRS19	HRS18	HRS17	HRS16
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	HRS15	HRS14	HRS13	HRS12	HRS11	HRS10	HRS9	HRS8	HRS7	HRS6	HRS5	HRS4	HRS3	HRS2	HRS1	HRS0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_HRS field descriptions

Field	Description
31 HRS31	Hardware Request Status Channel 31 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 31 is not present 1 A hardware service request for channel 31 is present
30 HRS30	Hardware Request Status Channel 30 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 30 is not present 1 A hardware service request for for channel 30 is present
29 HRS29	Hardware Request Status Channel 29 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 29 is not preset 1 A hardware service request for channel 29 is present
28 HRS28	Hardware Request Status Channel 28 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 28 is not present 1 A hardware service request for channel 28 is present
27 HRS27	Hardware Request Status Channel 27 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware.

Table continues on the next page...

DMA_HRS field descriptions (continued)

Field	Description
	0 A hardware service request for channel 27 is not present 1 A hardware service request for channel 27 is present
26 HRS26	Hardware Request Status Channel 26 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 26 is not present 1 A hardware service request for channel 26 is present
25 HRS25	Hardware Request Status Channel 25 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 25 is not present 1 A hardware service request for channel 25 is present
24 HRS24	Hardware Request Status Channel 24 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 24 is not present 1 A hardware service request for channel 24 is present
23 HRS23	Hardware Request Status Channel 23 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 23 is not present 1 A hardware service request for channel 23 is present
22 HRS22	Hardware Request Status Channel 22 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 22 is not present 1 A hardware service request for channel 22 is present
21 HRS21	Hardware Request Status Channel 21 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 21 is not present 1 A hardware service request for channel 21 is present
20 HRS20	Hardware Request Status Channel 20

Table continues on the next page...

DMA_HRS field descriptions (continued)

Field	Description
	The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 20 is not present 1 A hardware service request for channel 20 is present
19 HRS19	Hardware Request Status Channel 19 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 19 is not present 1 A hardware service request for channel 19 is present
18 HRS18	Hardware Request Status Channel 18 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 18 is not present 1 A hardware service request for channel 18 is present
17 HRS17	Hardware Request Status Channel 17 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 17 is not present 1 A hardware service request for channel 17 is present
16 HRS16	Hardware Request Status Channel 16 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 16 is not present 1 A hardware service request for channel 16 is present
15 HRS15	Hardware Request Status Channel 15 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 15 is not present 1 A hardware service request for channel 15 is present
14 HRS14	Hardware Request Status Channel 14 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware.

Table continues on the next page...

DMA_HRS field descriptions (continued)

Field	Description
	0 A hardware service request for channel 14 is not present 1 A hardware service request for channel 14 is present
13 HRS13	Hardware Request Status Channel 13 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 13 is not present 1 A hardware service request for channel 13 is present
12 HRS12	Hardware Request Status Channel 12 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 12 is not present 1 A hardware service request for channel 12 is present
11 HRS11	Hardware Request Status Channel 11 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 11 is not present 1 A hardware service request for channel 11 is present
10 HRS10	Hardware Request Status Channel 10 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 10 is not present 1 A hardware service request for channel 10 is present
9 HRS9	Hardware Request Status Channel 9 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 9 is not present 1 A hardware service request for channel 9 is present
8 HRS8	Hardware Request Status Channel 8 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 8 is not present 1 A hardware service request for channel 8 is present
7 HRS7	Hardware Request Status Channel 7

Table continues on the next page...

DMA_HRS field descriptions (continued)

Field	Description
	The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 7 is not present 1 A hardware service request for channel 7 is present
6 HRS6	Hardware Request Status Channel 6 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 6 is not present 1 A hardware service request for channel 6 is present
5 HRS5	Hardware Request Status Channel 5 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 5 is not present 1 A hardware service request for channel 5 is present
4 HRS4	Hardware Request Status Channel 4 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 4 is not present 1 A hardware service request for channel 4 is present
3 HRS3	Hardware Request Status Channel 3 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 3 is not present 1 A hardware service request for channel 3 is present
2 HRS2	Hardware Request Status Channel 2 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 2 is not present 1 A hardware service request for channel 2 is present
1 HRS1	Hardware Request Status Channel 1 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware.

Table continues on the next page...

DMA_HRS field descriptions (continued)

Field	Description
	0 A hardware service request for channel 1 is not present 1 A hardware service request for channel 1 is present
0 HRS0	Hardware Request Status Channel 0 The HRS bit for its respective channel remains asserted for the period when a Hardware Request is Present on the Channel. After the Request is completed and Channel is free, the HRS bit is automatically cleared by hardware. 0 A hardware service request for channel 0 is not present 1 A hardware service request for channel 0 is present

26.3.16 Enable Asynchronous Request in Stop Register (DMA_EARS)

Address: 4000_8000h base + 44h offset = 4000_8044h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	EDREQ_31	EDREQ_30	EDREQ_29	EDREQ_28	EDREQ_27	EDREQ_26	EDREQ_25	EDREQ_24	EDREQ_23	EDREQ_22	EDREQ_21	EDREQ_20	EDREQ_19	EDREQ_18	EDREQ_17	EDREQ_16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	EDREQ_15	EDREQ_14	EDREQ_13	EDREQ_12	EDREQ_11	EDREQ_10	EDREQ_9	EDREQ_8	EDREQ_7	EDREQ_6	EDREQ_5	EDREQ_4	EDREQ_3	EDREQ_2	EDREQ_1	EDREQ_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_EARS field descriptions

Field	Description
31 EDREQ_31	Enable asynchronous DMA request in stop mode for channel 31 0 Disable asynchronous DMA request for channel 31 1 Enable asynchronous DMA request for channel 31
30 EDREQ_30	Enable asynchronous DMA request in stop mode for channel 30 0 Disable asynchronous DMA request for channel 30 1 Enable asynchronous DMA request for channel 30
29 EDREQ_29	Enable asynchronous DMA request in stop mode for channel 29 0 Disable asynchronous DMA request for channel 29 1 Enable asynchronous DMA request for channel 29
28 EDREQ_28	Enable asynchronous DMA request in stop mode for channel 28

Table continues on the next page...

DMA_EARS field descriptions (continued)

Field	Description
	0 Disable asynchronous DMA request for channel 28 1 Enable asynchronous DMA request for channel 28
27 EDREQ_27	Enable asynchronous DMA request in stop mode for channel 27 0 Disable asynchronous DMA request for channel 27 1 Enable asynchronous DMA request for channel 27
26 EDREQ_26	Enable asynchronous DMA request in stop mode for channel 26 0 Disable asynchronous DMA request for channel 26 1 Enable asynchronous DMA request for channel 26
25 EDREQ_25	Enable asynchronous DMA request in stop mode for channel 25 0 Disable asynchronous DMA request for channel 25 1 Enable asynchronous DMA request for channel 25
24 EDREQ_24	Enable asynchronous DMA request in stop mode for channel 24 0 Disable asynchronous DMA request for channel 24 1 Enable asynchronous DMA request for channel 24
23 EDREQ_23	Enable asynchronous DMA request in stop mode for channel 23 0 Disable asynchronous DMA request for channel 23 1 Enable asynchronous DMA request for channel 23
22 EDREQ_22	Enable asynchronous DMA request in stop mode for channel 22 0 Disable asynchronous DMA request for channel 22 1 Enable asynchronous DMA request for channel 22
21 EDREQ_21	Enable asynchronous DMA request in stop mode for channel 21 0 Disable asynchronous DMA request for channel 21 1 Enable asynchronous DMA request for channel 21
20 EDREQ_20	Enable asynchronous DMA request in stop mode for channel 20 0 Disable asynchronous DMA request for channel 20 1 Enable asynchronous DMA request for channel 20
19 EDREQ_19	Enable asynchronous DMA request in stop mode for channel 19 0 Disable asynchronous DMA request for channel 19 1 Enable asynchronous DMA request for channel 19
18 EDREQ_18	Enable asynchronous DMA request in stop mode for channel 18 0 Disable asynchronous DMA request for channel 18 1 Enable asynchronous DMA request for channel 18
17 EDREQ_17	Enable asynchronous DMA request in stop mode for channel 17 0 Disable asynchronous DMA request for channel 17 1 Enable asynchronous DMA request for channel 17
16 EDREQ_16	Enable asynchronous DMA request in stop mode for channel 16

Table continues on the next page...

DMA_EARS field descriptions (continued)

Field	Description
	0 Disable asynchronous DMA request for channel 16 1 Enable asynchronous DMA request for channel 16
15 EDREQ_15	Enable asynchronous DMA request in stop mode for channel 15 0 Disable asynchronous DMA request for channel 15. 1 Enable asynchronous DMA request for channel 15.
14 EDREQ_14	Enable asynchronous DMA request in stop mode for channel 14 0 Disable asynchronous DMA request for channel 14. 1 Enable asynchronous DMA request for channel 14.
13 EDREQ_13	Enable asynchronous DMA request in stop mode for channel 13 0 Disable asynchronous DMA request for channel 13. 1 Enable asynchronous DMA request for channel 13.
12 EDREQ_12	Enable asynchronous DMA request in stop mode for channel 12 0 Disable asynchronous DMA request for channel 12. 1 Enable asynchronous DMA request for channel 12.
11 EDREQ_11	Enable asynchronous DMA request in stop mode for channel 11 0 Disable asynchronous DMA request for channel 11. 1 Enable asynchronous DMA request for channel 11.
10 EDREQ_10	Enable asynchronous DMA request in stop mode for channel 10 0 Disable asynchronous DMA request for channel 10. 1 Enable asynchronous DMA request for channel 10.
9 EDREQ_9	Enable asynchronous DMA request in stop mode for channel 9 0 Disable asynchronous DMA request for channel 9. 1 Enable asynchronous DMA request for channel 9.
8 EDREQ_8	Enable asynchronous DMA request in stop mode for channel 8 0 Disable asynchronous DMA request for channel 8. 1 Enable asynchronous DMA request for channel 8.
7 EDREQ_7	Enable asynchronous DMA request in stop mode for channel 7 0 Disable asynchronous DMA request for channel 7. 1 Enable asynchronous DMA request for channel 7.
6 EDREQ_6	Enable asynchronous DMA request in stop mode for channel 6 0 Disable asynchronous DMA request for channel 6. 1 Enable asynchronous DMA request for channel 6.
5 EDREQ_5	Enable asynchronous DMA request in stop mode for channel 5 0 Disable asynchronous DMA request for channel 5. 1 Enable asynchronous DMA request for channel 5.
4 EDREQ_4	Enable asynchronous DMA request in stop mode for channel 4

Table continues on the next page...

DMA_EARS field descriptions (continued)

Field	Description
	0 Disable asynchronous DMA request for channel 4. 1 Enable asynchronous DMA request for channel 4.
3 EDREQ_3	Enable asynchronous DMA request in stop mode for channel 3. 0 Disable asynchronous DMA request for channel 3. 1 Enable asynchronous DMA request for channel 3.
2 EDREQ_2	Enable asynchronous DMA request in stop mode for channel 2. 0 Disable asynchronous DMA request for channel 2. 1 Enable asynchronous DMA request for channel 2.
1 EDREQ_1	Enable asynchronous DMA request in stop mode for channel 1. 0 Disable asynchronous DMA request for channel 1 1 Enable asynchronous DMA request for channel 1.
0 EDREQ_0	Enable asynchronous DMA request in stop mode for channel 0. 0 Disable asynchronous DMA request for channel 0. 1 Enable asynchronous DMA request for channel 0.

26.3.17 Channel n Priority Register (DMA_DCHPRI*n*)

When fixed-priority channel arbitration is enabled (CR[ERCA] = 0), the contents of these registers define the unique priorities associated with each channel within a group. The channel priorities are evaluated by numeric value; for example, 0 is the lowest priority, 1 is the next higher priority, then 2, 3, etc. Software must program the channel priorities with unique values; otherwise, a configuration error is reported. The range of the priority value is limited to the values of 0 through 15. When read, the GRPPRI bits of the DCHPRIn register reflect the current priority level of the group of channels in which the corresponding channel resides. GRPPRI bits are not affected by writes to the DCHPRIn registers. The group priority is assigned in the DMA control register.

Address: 4000_8000h base + 100h offset + (1d × i), where i=0d to 31d

Bit	7	6	5	4	3	2	1	0
Read	ECP	DPA	GRPPRI		CHPRI			
Write								
Reset	0	0	*	*	*	*	*	*

* Notes:
- GRPPRI field: See bit field description.
- CHPRI field: See bit field description.

DMA_DCHPRI*n* field descriptions

Field	Description
7 ECP	Enable Channel Preemption. 0 Channel n cannot be suspended by a higher priority channel's service request. 1 Channel n can be temporarily suspended by the service request of a higher priority channel.
6 DPA	Disable Preempt Ability. 0 Channel n can suspend a lower priority channel. 1 Channel n cannot suspend any channel, regardless of channel priority.
5–4 GRPPRI	Channel n Current Group Priority Group priority assigned to this channel group when fixed-priority arbitration is enabled. This field is read-only; writes are ignored. **NOTE:** Reset value for the group and channel priority fields, GRPPRI and CHPRI, is equal to the corresponding channel number for each priority register, that is, DCHPRI31[GRPPRI] = 0b01 and DCHPRI31[CHPRI] equals 0b1111.
CHPRI	Channel n Arbitration Priority Channel priority when fixed-priority arbitration is enabled **NOTE:** Reset value for the group and channel priority fields, GRPPRI and CHPRI, is equal to the corresponding channel number for each priority register, that is, DCHPRI31[GRPPRI] = 0b01 and DCHPRI31[CHPRI] = 0b01111.

26.3.18 TCD Source Address (DMA_TCD*n*_SADDR)

Address: 4000_8000h base + 1000h offset + (32d × i), where i=0d to 31d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	SADDR																															
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_SADDR field descriptions

Field	Description
SADDR	Source Address Memory address pointing to the source data.

26.3.19 TCD Signed Source Address Offset (DMA_TCD*n*_SOFF)

Address: 4000_8000h base + 1004h offset + (32d × i), where i=0d to 31d

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	SOFF															
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_SOFF field descriptions

Field	Description
SOFF	Source address signed offset Sign-extended offset applied to the current source address to form the next-state value as each source read is completed.

26.3.20 TCD Transfer Attributes (DMA_TCD*n*_ATTR)

Address: 4000_8000h base + 1006h offset + (32d × i), where i=0d to 31d

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	SMOD					SSIZE			DMOD					DSIZE		
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_ATTR field descriptions

Field	Description
15–11 SMOD	Source Address Modulo 0 Source address modulo feature is disabled ≠0 This value defines a specific address range specified to be the value after SADDR + SOFF calculation is performed on the original register value. Setting this field provides the ability to implement a circular data queue easily. For data queues requiring power-of-2 size bytes, the queue should start at a 0-modulo-size address and the SMOD field should be set to the appropriate value for the queue, freezing the desired number of upper address bits. The value programmed into this field specifies the number of lower address bits allowed to change. For a circular queue application, the SOFF is typically set to the transfer size to implement post-increment addressing with the SMOD function constraining the addresses to a 0-modulo-size range.
10–8 SSIZE	Source data transfer size **NOTE:** Using a Reserved value causes a configuration error.

Table continues on the next page...

DMA_TCD*n*_ATTR field descriptions (continued)

Field	Description
	000 8-bit 001 16-bit 010 32-bit 011 Reserved 100 16-byte burst 101 32-byte burst 110 Reserved 111 Reserved
7–3 DMOD	Destination Address Modulo See the SMOD definition
DSIZE	Destination data transfer size See the SSIZE definition

26.3.21 TCD Minor Byte Count (Minor Loop Mapping Disabled) (DMA_TCD*n*_NBYTES_MLNO)

This register, or one of the next two registers (TCD_NBYTES_MLOFFNO, TCD_NBYTES_MLOFFYES), defines the number of bytes to transfer per request. Which register to use depends on whether minor loop mapping is disabled, enabled but not used for this channel, or enabled and used.

TCD word 2 is defined as follows if:

- Minor loop mapping is disabled (CR[EMLM] = 0)

If minor loop mapping is enabled, see the TCD_NBYTES_MLOFFNO and TCD_NBYTES_MLOFFYES register descriptions for the definition of TCD word 2.

Address: 4000_8000h base + 1008h offset + (32d × i), where i=0d to 31d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	NBYTES																															
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:

- x = Undefined at reset.

DMA_TCD*n*_NBYTES_MLNO field descriptions

Field	Description
NBYTES	Minor Byte Transfer Count Number of bytes to be transferred in each service request of the channel. As a channel activates, the appropriate TCD contents load into the eDMA engine, and the appropriate reads and writes perform until

DMA_TCD*n*_NBYTES_MLNO field descriptions (continued)

Field	Description
	the minor byte transfer count has transferred. This is an indivisible operation and cannot be halted. It can, however, be stalled by using the bandwidth control field, or via preemption. After the minor count is exhausted, the SADDR and DADDR values are written back into the TCD memory, the major iteration count is decremented and restored to the TCD memory. If the major iteration count is completed, additional processing is performed. **NOTE:** An NBYTES value of 0x0000_0000 is interpreted as a 4 GB transfer.

26.3.22 TCD Signed Minor Loop Offset (Minor Loop Mapping Enabled and Offset Disabled) (DMA_TCD*n*_NBYTES_MLOFFNO)

One of three registers (this register, TCD_NBYTES_MLNO, or TCD_NBYTES_MLOFFYES), defines the number of bytes to transfer per request. Which register to use depends on whether minor loop mapping is disabled, enabled but not used for this channel, or enabled and used.

TCD word 2 is defined as follows if:

- Minor loop mapping is enabled (CR[EMLM] = 1) and
- SMLOE = 0 and DMLOE = 0

If minor loop mapping is enabled and SMLOE or DMLOE is set, then refer to the TCD_NBYTES_MLOFFYES register description. If minor loop mapping is disabled, then refer to the TCD_NBYTES_MLNO register description.

Address: 4000_8000h base + 1008h offset + (32d × i), where i=0d to 31d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	SMLOE	DMLOE	NBYTES													
W																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	NBYTES															
W																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_NBYTES_MLOFFNO field descriptions

Field	Description
31 SMLOE	Source Minor Loop Offset Enable Selects whether the minor loop offset is applied to the source address upon minor loop completion. 0 The minor loop offset is not applied to the SADDR 1 The minor loop offset is applied to the SADDR
30 DMLOE	Destination Minor Loop Offset enable Selects whether the minor loop offset is applied to the destination address upon minor loop completion. 0 The minor loop offset is not applied to the DADDR 1 The minor loop offset is applied to the DADDR
NBYTES	Minor Byte Transfer Count Number of bytes to be transferred in each service request of the channel. As a channel activates, the appropriate TCD contents load into the eDMA engine, and the appropriate reads and writes perform until the minor byte transfer count has transferred. This is an indivisible operation and cannot be halted. It can, however, be stalled by using the bandwidth control field, or via preemption. After the minor count is exhausted, the SADDR and DADDR values are written back into the TCD memory, the major iteration count is decremented and restored to the TCD memory. If the major iteration count is completed, additional processing is performed.

26.3.23 TCD Signed Minor Loop Offset (Minor Loop Mapping and Offset Enabled) (DMA_TCD*n*_NBYTES_MLOFFYES)

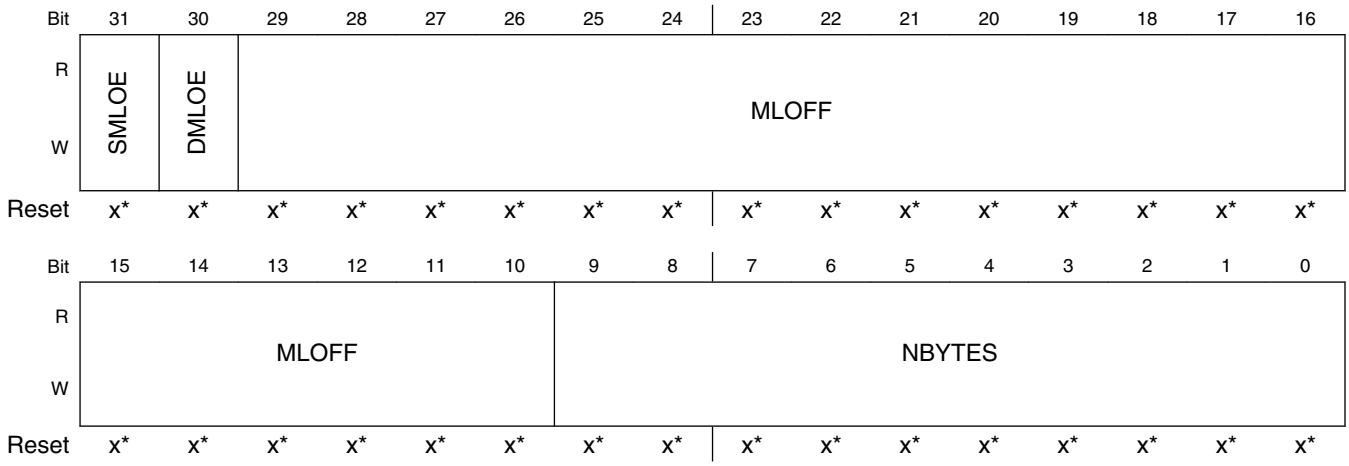
One of three registers (this register, TCD_NBYTES_MLNO, or TCD_NBYTES_MLOFFNO), defines the number of bytes to transfer per request. Which register to use depends on whether minor loop mapping is disabled, enabled but not used for this channel, or enabled and used.

TCD word 2 is defined as follows if:

- Minor loop mapping is enabled (CR[EMLM] = 1) and
- Minor loop offset is enabled (SMLOE or DMLOE = 1)

If minor loop mapping is enabled and SMLOE and DMLOE are cleared, then refer to the TCD_NBYTES_MLOFFNO register description. If minor loop mapping is disabled, then refer to the TCD_NBYTES_MLNO register description.

Address: 4000_8000h base + 1008h offset + (32d × i), where i=0d to 31d



* Notes:
- x = Undefined at reset.

DMA_TCD*n*_NBYTES_MLOFFYES field descriptions

Field	Description
31 SMLOE	Source Minor Loop Offset Enable Selects whether the minor loop offset is applied to the source address upon minor loop completion. 0 The minor loop offset is not applied to the SADDR 1 The minor loop offset is applied to the SADDR
30 DMLOE	Destination Minor Loop Offset enable Selects whether the minor loop offset is applied to the destination address upon minor loop completion. 0 The minor loop offset is not applied to the DADDR 1 The minor loop offset is applied to the DADDR
29–10 MLOFF	If SMLOE or DMLOE is set, this field represents a sign-extended offset applied to the source or destination address to form the next-state value after the minor loop completes.
NBYTES	Minor Byte Transfer Count Number of bytes to be transferred in each service request of the channel. As a channel activates, the appropriate TCD contents load into the eDMA engine, and the appropriate reads and writes perform until the minor byte transfer count has transferred. This is an indivisible operation and cannot be halted. It can, however, be stalled by using the bandwidth control field, or via preemption. After the minor count is exhausted, the SADDR and DADDR values are written back into the TCD memory, the major iteration count is decremented and restored to the TCD memory. If the major iteration count is completed, additional processing is performed.

26.3.24 TCD Last Source Address Adjustment (DMA_TCD*n*_SLAST)

Address: 4000_8000h base + 100Ch offset + (32d × i), where i=0d to 31d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	SLAST																															
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_SLAST field descriptions

Field	Description
SLAST	Last Source Address Adjustment Adjustment value added to the source address at the completion of the major iteration count. This value can be applied to restore the source address to the initial value, or adjust the address to reference the next data structure. This register uses two's complement notation; the overflow bit is discarded.

26.3.25 TCD Destination Address (DMA_TCD*n*_DADDR)

Address: 4000_8000h base + 1010h offset + (32d × i), where i=0d to 31d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	DADDR																															
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_DADDR field descriptions

Field	Description
DADDR	Destination Address Memory address pointing to the destination data.

26.3.26 TCD Signed Destination Address Offset (DMA_TCD*n*_DOFF)

Address: 4000_8000h base + 1014h offset + (32d × i), where i=0d to 31d

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	DOFF															
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_DOFF field descriptions

Field	Description
DOFF	Destination Address Signed Offset Sign-extended offset applied to the current destination address to form the next-state value as each destination write is completed.

26.3.27 TCD Current Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD*n*_CITER_ELINKYES)

If TCDn_CITER[ELINK] is set, the TCDn_CITER register is defined as follows.

Address: 4000_8000h base + 1016h offset + (32d × i), where i=0d to 31d

Bit	15	14	13	12	11	10	9	8
Read Write	ELINK	0	LINKCH					CITER
Reset	x*	x*	x*	x*	x*	x*	x*	x*

Bit	7	6	5	4	3	2	1	0
Read Write	CITER							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_CITER_ELINKYES field descriptions

Field	Description
15 ELINK	Enable channel-to-channel linking on minor-loop complete As the channel completes the minor loop, this flag enables linking to another channel, defined by the LINKCH field. The link target channel initiates a channel service request via an internal mechanism that sets the TCDn_CSR[START] bit of the specified channel.

Table continues on the next page...

DMA_TCD*n*_CITER_ELINKYES field descriptions (continued)

Field	Description
	If channel linking is disabled, the CITER value is extended to 15 bits in place of a link channel number. If the major loop is exhausted, this link mechanism is suppressed in favor of the MAJORELINK channel linking. **NOTE:** This bit must be equal to the BITER[ELINK] bit; otherwise, a configuration error is reported. 0 The channel-to-channel linking is disabled 1 The channel-to-channel linking is enabled
14 Reserved	This field is reserved.
13–9 LINKCH	Minor Loop Link Channel Number If channel-to-channel linking is enabled (ELINK = 1), then after the minor loop is exhausted, the eDMA engine initiates a channel service request to the channel defined by this field by setting that channel's TCDn_CSR[START] bit.
CITER	Current Major Iteration Count This 9-bit (ELINK = 1) or 15-bit (ELINK = 0) count represents the current major loop count for the channel. It is decremented each time the minor loop is completed and updated in the transfer control descriptor memory. After the major iteration count is exhausted, the channel performs a number of operations, for example, final source and destination address calculations, optionally generating an interrupt to signal channel completion before reloading the CITER field from the Beginning Iteration Count (BITER) field. **NOTE:** When the CITER field is initially loaded by software, it must be set to the same value as that contained in the BITER field. **NOTE:** If the channel is configured to execute a single service request, the initial values of BITER and CITER should be 0x0001.

26.3.28 TCD Current Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD*n*_CITER_ELINKNO)

If TCDn_CITER[ELINK] is cleared, the TCDn_CITER register is defined as follows.

Address: 4000_8000h base + 1016h offset + (32d × i), where i=0d to 31d

Bit	15	14	13	12	11	10	9	8
Read Write	ELINK	CITER						
Reset	x*	x*	x*	x*	x*	x*	x*	x*

Bit	7	6	5	4	3	2	1	0
Read Write	CITER							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_CITER_ELINKNO field descriptions

Field	Description
15 ELINK	Enable channel-to-channel linking on minor-loop complete As the channel completes the minor loop, this flag enables linking to another channel, defined by the LINKCH field. The link target channel initiates a channel service request via an internal mechanism that sets the TCDn_CSR[START] bit of the specified channel. If channel linking is disabled, the CITER value is extended to 15 bits in place of a link channel number. If the major loop is exhausted, this link mechanism is suppressed in favor of the MAJORELINK channel linking. **NOTE:** This bit must be equal to the BITER[ELINK] bit; otherwise, a configuration error is reported. 0 The channel-to-channel linking is disabled 1 The channel-to-channel linking is enabled
CITER	Current Major Iteration Count This 9-bit (ELINK = 1) or 15-bit (ELINK = 0) count represents the current major loop count for the channel. It is decremented each time the minor loop is completed and updated in the transfer control descriptor memory. After the major iteration count is exhausted, the channel performs a number of operations, for example, final source and destination address calculations, optionally generating an interrupt to signal channel completion before reloading the CITER field from the Beginning Iteration Count (BITER) field. **NOTE:** When the CITER field is initially loaded by software, it must be set to the same value as that contained in the BITER field. **NOTE:** If the channel is configured to execute a single service request, the initial values of BITER and CITER should be 0x0001.

26.3.29 TCD Last Destination Address Adjustment/Scatter Gather Address (DMA_TCD*n*_DLASTSGA)

Address: 4000_8000h base + 1018h offset + (32d × i), where i=0d to 31d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	DLASTSGA																															
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_DLASTSGA field descriptions

Field	Description
DLASTSGA	Destination last address adjustment or the memory address for the next transfer control descriptor to be loaded into this channel (scatter/gather). If (TCDn_CSR[ESG] = 0) then: • Adjustment value added to the destination address at the completion of the major iteration count. This value can apply to restore the destination address to the initial value or adjust the address to reference the next data structure. • This field uses two's complement notation for the final destination address adjustment.

DMA_TCD*n*_DLASTSGA field descriptions (continued)

Field	Description
	Otherwise: • This address points to the beginning of a 0-modulo-32-byte region containing the next transfer control descriptor to be loaded into this channel. This channel reload is performed as the major iteration count completes. The scatter/gather address must be 0-modulo-32-byte, otherwise a configuration error is reported.

26.3.30 TCD Control and Status (DMA_TCD*n*_CSR)

Address: 4000_8000h base + 101Ch offset + (32d × i), where i=0d to 31d

Bit	15	14	13	12	11	10	9	8
Read Write	BWC		0	MAJORLINKCH				
Reset	x*	x*	x*	x*	x*	x*	x*	x*

Bit	7	6	5	4	3	2	1	0
Read Write	DONE	ACTIVE	MAJORELINK	ESG	DREQ	INTHALF	INTMAJOR	START
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_CSR field descriptions

Field	Description
15–14 BWC	Bandwidth Control Throttles the amount of bus bandwidth consumed by the eDMA. Generally, as the eDMA processes the minor loop, it continuously generates read/write sequences until the minor count is exhausted. This field forces the eDMA to stall after the completion of each read/write access to control the bus request bandwidth seen by the crossbar switch. **NOTE:** If the source and destination sizes are equal, this field is ignored between the first and second transfers and after the last write of each minor loop. This behavior is a side effect of reducing start-up latency. 00 No eDMA engine stalls. 01 Reserved 10 eDMA engine stalls for 4 cycles after each R/W. 11 eDMA engine stalls for 8 cycles after each R/W.
13 Reserved	This field is reserved.
12–8 MAJORLINKCH	Major Loop Link Channel Number If (MAJORELINK = 0) then: • No channel-to-channel linking, or chaining, is performed after the major loop counter is exhausted. Otherwise:

Table continues on the next page...

DMA_TCD*n*_CSR field descriptions (continued)

Field	Description
	• After the major loop counter is exhausted, the eDMA engine initiates a channel service request at the channel defined by this field by setting that channel's TCDn_CSR[START] bit.
7 DONE	Channel Done This flag indicates the eDMA has completed the major loop. The eDMA engine sets it as the CITER count reaches zero. The software clears it, or the hardware when the channel is activated. **NOTE:** This bit must be cleared to write the MAJORELINK or ESG bits.
6 ACTIVE	Channel Active This flag signals the channel is currently in execution. It is set when channel service begins, and is cleared by the eDMA as the minor loop completes or when any error condition is detected.
5 MAJORELINK	Enable channel-to-channel linking on major loop complete As the channel completes the major loop, this flag enables the linking to another channel, defined by MAJORLINKCH. The link target channel initiates a channel service request via an internal mechanism that sets the TCDn_CSR[START] bit of the specified channel. **NOTE:** To support the dynamic linking coherency model, this field is forced to zero when written to while the TCDn_CSR[DONE] bit is set. 0 The channel-to-channel linking is disabled. 1 The channel-to-channel linking is enabled.
4 ESG	Enable Scatter/Gather Processing As the channel completes the major loop, this flag enables scatter/gather processing in the current channel. If enabled, the eDMA engine uses DLASTSGA as a memory pointer to a 0-modulo-32 address containing a 32-byte data structure loaded as the transfer control descriptor into the local memory. **NOTE:** To support the dynamic scatter/gather coherency model, this field is forced to zero when written to while the TCDn_CSR[DONE] bit is set. 0 The current channel's TCD is normal format. 1 The current channel's TCD specifies a scatter gather format. The DLASTSGA field provides a memory pointer to the next TCD to be loaded into this channel after the major loop completes its execution.
3 DREQ	Disable Request If this flag is set, the eDMA hardware automatically clears the corresponding ERQ bit when the current major iteration count reaches zero. 0 The channel's ERQ bit is not affected. 1 The channel's ERQ bit is cleared when the major loop is complete.
2 INTHALF	Enable an interrupt when major counter is half complete. If this flag is set, the channel generates an interrupt request by setting the appropriate bit in the INT register when the current major iteration count reaches the halfway point. Specifically, the comparison performed by the eDMA engine is (CITER == (BITER >> 1)). This halfway point interrupt request is provided to support double-buffered, also known as ping-pong, schemes or other types of data movement where the processor needs an early indication of the transfer's progress. **NOTE:** If BITER = 1, do not use INTHALF. Use INTMAJOR instead. 0 The half-point interrupt is disabled. 1 The half-point interrupt is enabled.

Table continues on the next page...

DMA_TCD*n*_CSR field descriptions (continued)

Field	Description
1 INTMAJOR	Enable an interrupt when major iteration count completes. If this flag is set, the channel generates an interrupt request by setting the appropriate bit in the INT when the current major iteration count reaches zero. 0 The end-of-major loop interrupt is disabled. 1 The end-of-major loop interrupt is enabled.
0 START	Channel Start If this flag is set, the channel is requesting service. The eDMA hardware automatically clears this flag after the channel begins execution. 0 The channel is not explicitly started. 1 The channel is explicitly started via a software initiated service request.

26.3.31 TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Enabled) (DMA_TCD*n*_BITER_ELINKYES)

If the TCDn_BITER[ELINK] bit is set, the TCDn_BITER register is defined as follows.

Address: 4000_8000h base + 101Eh offset + (32d × i), where i=0d to 31d

Bit	15	14	13	12	11	10	9	8
Read Write	ELINK	0	LINKCH					BITER
Reset	x*	x*	x*	x*	x*	x*	x*	x*

Bit	7	6	5	4	3	2	1	0
Read Write	BITER							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_BITER_ELINKYES field descriptions

Field	Description
15 ELINK	Enables channel-to-channel linking on minor loop complete As the channel completes the minor loop, this flag enables the linking to another channel, defined by BITER[LINKCH]. The link target channel initiates a channel service request via an internal mechanism that sets the TCDn_CSR[START] bit of the specified channel. If channel linking disables, the BITER value extends to 15 bits in place of a link channel number. If the major loop is exhausted, this link mechanism is suppressed in favor of the MAJORELINK channel linking. **NOTE:** When the software loads the TCD, this field must be set equal to the corresponding CITER field; otherwise, a configuration error is reported. As the major iteration count is exhausted, the contents of this field are reloaded into the CITER field.

Table continues on the next page...

DMA_TCD*n*_BITER_ELINKYES field descriptions (continued)

Field	Description
	0 The channel-to-channel linking is disabled 1 The channel-to-channel linking is enabled
14 Reserved	This field is reserved.
13–9 LINKCH	Link Channel Number If channel-to-channel linking is enabled (ELINK = 1), then after the minor loop is exhausted, the eDMA engine initiates a channel service request at the channel defined by this field by setting that channel's TCDn_CSR[START] bit. **NOTE:** When the software loads the TCD, this field must be set equal to the corresponding CITER field; otherwise, a configuration error is reported. As the major iteration count is exhausted, the contents of this field are reloaded into the CITER field.
BITER	Starting major iteration count As the transfer control descriptor is first loaded by software, this 9-bit (ELINK = 1) or 15-bit (ELINK = 0) field must be equal to the value in the CITER field. As the major iteration count is exhausted, the contents of this field are reloaded into the CITER field. **NOTE:** When the software loads the TCD, this field must be set equal to the corresponding CITER field; otherwise, a configuration error is reported. As the major iteration count is exhausted, the contents of this field are reloaded into the CITER field. If the channel is configured to execute a single service request, the initial values of BITER and CITER should be 0x0001.

26.3.32 TCD Beginning Minor Loop Link, Major Loop Count (Channel Linking Disabled) (DMA_TCD*n*_BITER_ELINKNO)

If the TCDn_BITER[ELINK] bit is cleared, the TCDn_BITER register is defined as follows.

Address: 4000_8000h base + 101Eh offset + (32d × i), where i=0d to 31d

Bit	15	14	13	12	11	10	9	8
Read Write	ELINK	BITER						
Reset	x*	x*	x*	x*	x*	x*	x*	x*

Bit	7	6	5	4	3	2	1	0
Read Write	BITER							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

DMA_TCD*n*_BITER_ELINKNO field descriptions

Field	Description
15 ELINK	Enables channel-to-channel linking on minor loop complete

Table continues on the next page...

DMA_TCD*n*_BITER_ELINKNO field descriptions (continued)

Field	Description
	As the channel completes the minor loop, this flag enables the linking to another channel, defined by BITER[LINKCH]. The link target channel initiates a channel service request via an internal mechanism that sets the TCDn_CSR[START] bit of the specified channel. If channel linking is disabled, the BITER value extends to 15 bits in place of a link channel number. If the major loop is exhausted, this link mechanism is suppressed in favor of the MAJORELINK channel linking. **NOTE:** When the software loads the TCD, this field must be set equal to the corresponding CITER field; otherwise, a configuration error is reported. As the major iteration count is exhausted, the contents of this field are reloaded into the CITER field. 0 The channel-to-channel linking is disabled 1 The channel-to-channel linking is enabled
BITER	Starting Major Iteration Count As the transfer control descriptor is first loaded by software, this 9-bit (ELINK = 1) or 15-bit (ELINK = 0) field must be equal to the value in the CITER field. As the major iteration count is exhausted, the contents of this field are reloaded into the CITER field. **NOTE:** When the software loads the TCD, this field must be set equal to the corresponding CITER field; otherwise, a configuration error is reported. As the major iteration count is exhausted, the contents of this field is reloaded into the CITER field. If the channel is configured to execute a single service request, the initial values of BITER and CITER should be 0x0001.

26.4 Functional description

The operation of the eDMA is described in the following subsections.

26.4.1 eDMA basic data flow

The basic flow of a data transfer can be partitioned into three segments.

As shown in the following diagram, the first segment involves the channel activation:

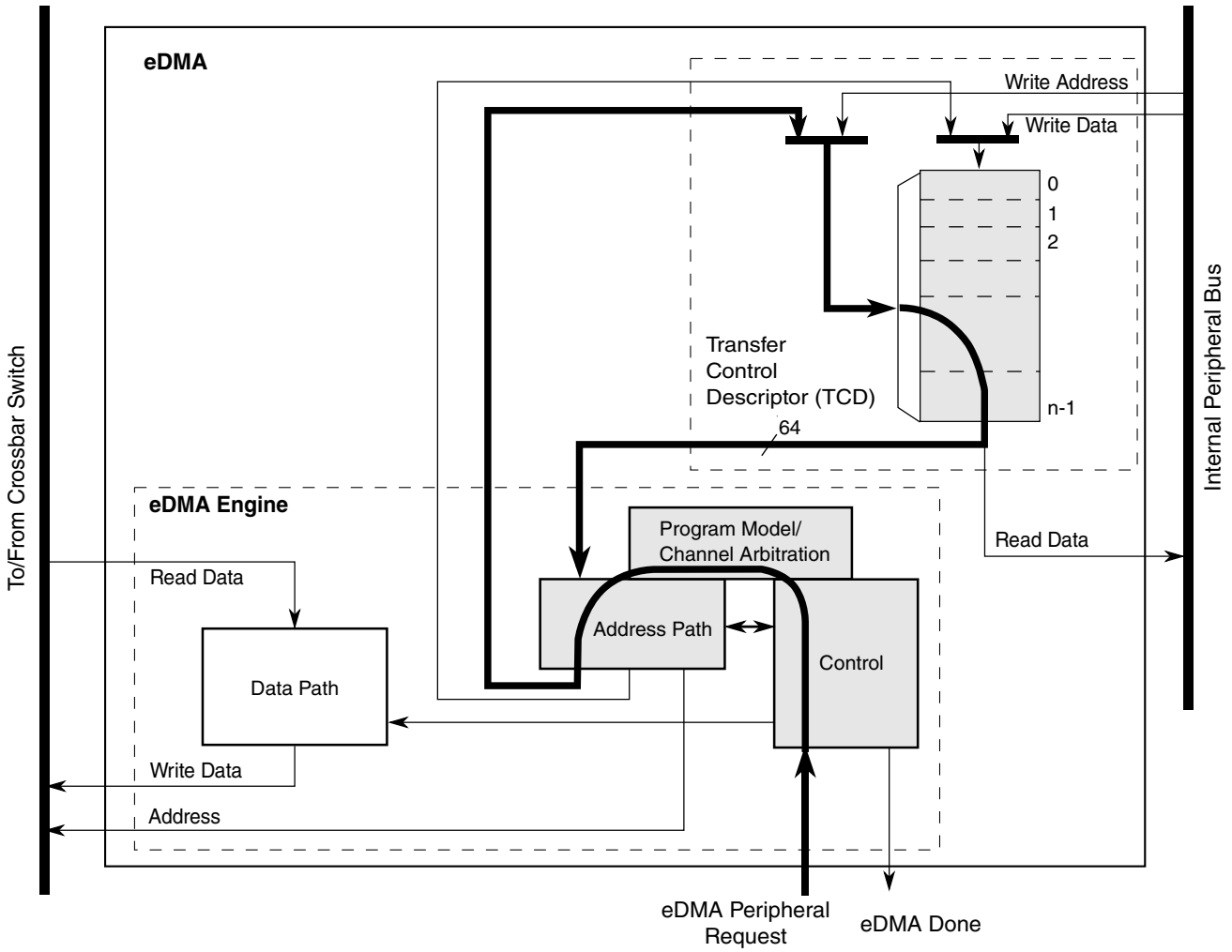


Figure 26-2. eDMA operation, part 1

This example uses the assertion of the eDMA peripheral request signal to request service for channel *n*. Channel activation via software and the TCD*n*_CSR[START] bit follows the same basic flow as peripheral requests. The eDMA request input signal is registered internally and then routed through the eDMA engine: first through the control module, then into the program model and channel arbitration. In the next cycle, the channel arbitration performs, using the fixed-priority or round-robin algorithm. After arbitration is complete, the activated channel number is sent through the address path and converted into the required address to access the local memory for TCD*n*. Next, the TCD memory is accessed and the required descriptor read from the local memory and loaded into the eDMA engine address path channel x or y registers. The TCD memory is 64 bits wide to minimize the time needed to fetch the activated channel descriptor and load it into the address path channel x or y registers.

The following diagram illustrates the second part of the basic data flow:

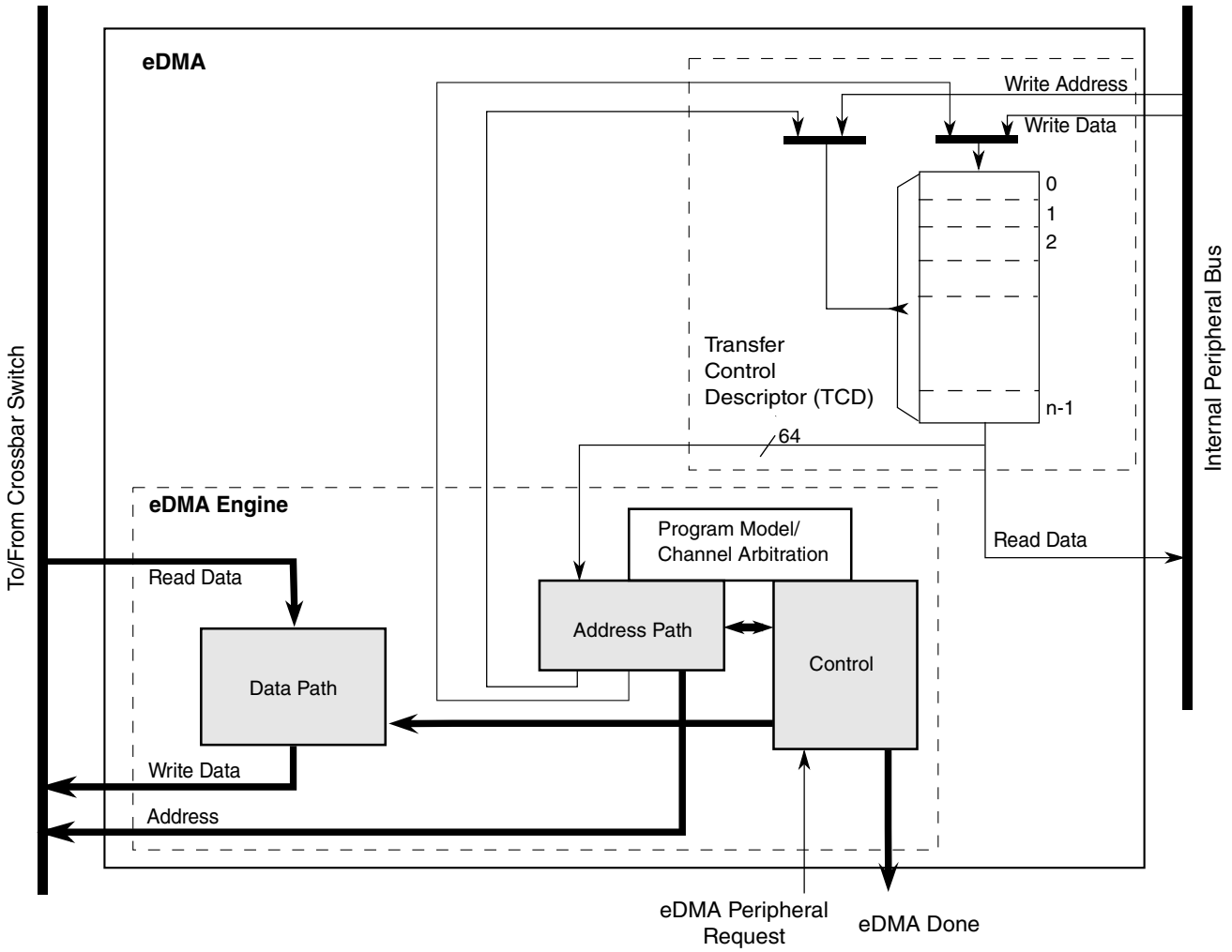


Figure 26-3. eDMA operation, part 2

The modules associated with the data transfer (address path, data path, and control) sequence through the required source reads and destination writes to perform the actual data movement. The source reads are initiated and the fetched data is temporarily stored in the data path block until it is gated onto the internal bus during the destination write. This source read/destination write processing continues until the minor byte count has transferred.

After the minor byte count has moved, the final phase of the basic data flow is performed. In this segment, the address path logic performs the required updates to certain fields in the appropriate TCD, for example, SADDR, DADDR, CITER. If the major iteration count is exhausted, additional operations are performed. These include the final address adjustments and reloading of the BITER field into the CITER. Assertion of an optional interrupt request also occurs at this time, as does a possible fetch of a new TCD from memory using the scatter/gather address pointer included in the descriptor (if scatter/gather is enabled). The updates to the TCD memory and the assertion of an interrupt request are shown in the following diagram.

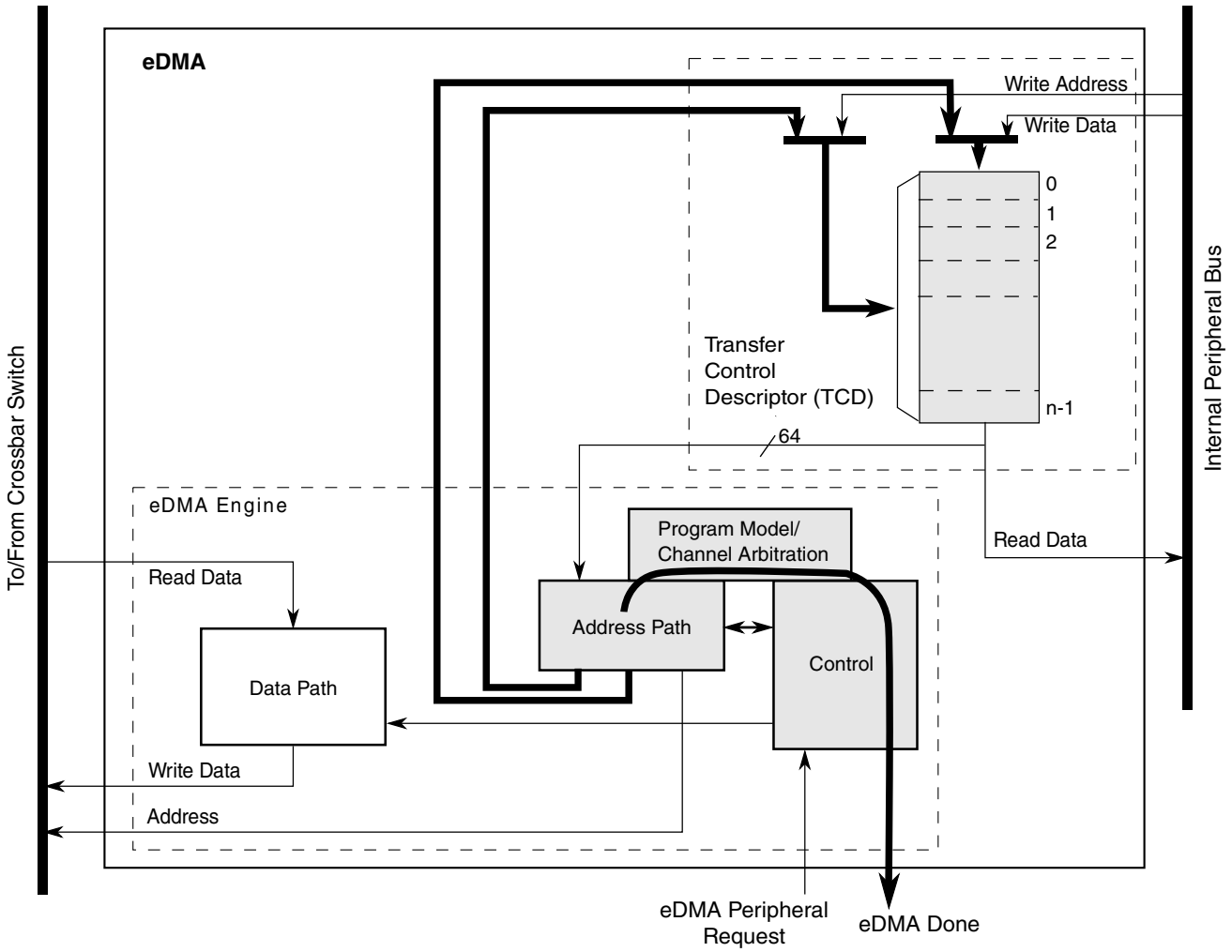


Figure 26-4. eDMA operation, part 3

26.4.2 Fault reporting and handling

Channel errors are reported in the Error Status register (DMAx_ES) and can be caused by:

- A configuration error, which is an illegal setting in the transfer-control descriptor or an illegal priority register setting in Fixed-Arbitration mode, or
- An error termination to a bus master read or write cycle

A configuration error is reported when the starting source or destination address, source or destination offsets, minor loop byte count, or the transfer size represent an inconsistent state. Each of these possible causes are detailed below:

- The addresses and offsets must be aligned on 0-modulo-transfer-size boundaries.
- The minor loop byte count must be a multiple of the source and destination transfer sizes.

- All source reads and destination writes must be configured to the natural boundary of the programmed transfer size respectively.
- In fixed arbitration mode, a configuration error is caused by any two channel priorities being equal. All channel priority levels must be unique when fixed arbitration mode is enabled.

NOTE

When two channels have the same priority, a channel priority error exists and will be reported in the Error Status register. However, the channel number will not be reported in the Error Status register. When all of the channel priorities within a group are not unique, the channel number selected by arbitration in undetermined.

To aid in Channel Priority Error (CPE) debug, set the Halt On Error bit in the DMA's Control Register. If all of the channel priorities within a group are not unique, the DMA will be halted after the CPE error is recorded. The DMA will remain halted and will not process any channel service requests. Once all of the channel priorities are set to unique numbers, the DMA may be enabled again by clearing the Halt bit.

- If a scatter/gather operation is enabled upon channel completion, a configuration error is reported if the scatter/gather address (DLAST_SGA) is not aligned on a 32-byte boundary.
- If minor loop channel linking is enabled upon channel completion, a configuration error is reported when the link is attempted if the TCDn_CITER[E_LINK] bit does not equal the TCDn_BITER[E_LINK] bit.

If enabled, all configuration error conditions, except the scatter/gather and minor-loop link errors, report as the channel activates and asserts an error interrupt request. A scatter/gather configuration error is reported when the scatter/gather operation begins at major loop completion when properly enabled. A minor loop channel link configuration error is reported when the link operation is serviced at minor loop completion.

If a system bus read or write is terminated with an error, the data transfer is stopped and the appropriate bus error flag set. In this case, the state of the channel's transfer control descriptor is updated by the eDMA engine with the current source address, destination address, and current iteration count at the point of the fault. When a system bus error occurs, the channel terminates after the next transfer. Due to pipeline effect, the next transfer is already in progress when the bus error is received by the eDMA. If a bus error

occurs on the last read prior to beginning the write sequence, the write executes using the data captured during the bus error. If a bus error occurs on the last write prior to switching to the next read sequence, the read sequence executes before the channel terminates due to the destination bus error.

A transfer may be cancelled by software with the CR[CX] bit. When a cancel transfer request is recognized, the DMA engine stops processing the channel. The current read-write sequence is allowed to finish. If the cancel occurs on the last read-write sequence of a major or minor loop, the cancel request is discarded and the channel retires normally.

The error cancel transfer is the same as a cancel transfer except the Error Status register (DMAx_ES) is updated with the cancelled channel number and ECX is set. The TCD of a cancelled channel contains the source and destination addresses of the last transfer saved in the TCD. If the channel needs to be restarted, you must re-initialize the TCD because the aforementioned fields no longer represent the original parameters. When a transfer is cancelled by the error cancel transfer mechanism, the channel number is loaded into DMA_ES[ERRCHN] and ECX and VLD are set. In addition, an error interrupt may be generated if enabled.

NOTE

The cancel transfer request allows the user to stop a large data transfer in the event the full data transfer is no longer needed. The cancel transfer bit does not abort the channel. It simply stops the transferring of data and then retires the channel through its normal shutdown sequence. The application software must handle the context of the cancel. If an interrupt is desired (or not), then the interrupt should be enabled (or disabled) before the cancel request. The application software must clean up the transfer control descriptor since the full transfer did not occur.

The occurrence of any error causes the eDMA engine to stop normal processing of the active channel immediately (it goes to its error processing states and the transaction to the system bus still has pipeline effect), and the appropriate channel bit in the eDMA error register is asserted. At the same time, the details of the error condition are loaded into the Error Status register (DMAx_ES). The major loop complete indicators, setting the transfer control descriptor DONE flag and the possible assertion of an interrupt request, are not affected when an error is detected. After the error status has been updated, the eDMA engine continues operating by servicing the next appropriate channel. A channel that experiences an error condition is not automatically disabled. If a channel is terminated by an error and then issues another service request before the error is fixed, that channel executes and terminates with the same error condition.

26.4.3 Channel preemption

Channel preemption is enabled on a per-channel basis by setting the DCHPRIn[ECP] bit. Channel preemption allows the executing channel's data transfers to temporarily suspend in favor of starting a higher priority channel. After the preempting channel has completed all its minor loop data transfers, the preempted channel is restored and resumes execution. After the restored channel completes one read/write sequence, it is again eligible for preemption. If any higher priority channel is requesting service, the restored channel is suspended and the higher priority channel is serviced. Nested preemption, that is, attempting to preempt a preempting channel, is not supported. After a preempting channel begins execution, it cannot be preempted. Preemption is available only when fixed arbitration is selected.

A channel's ability to preempt another channel can be disabled by setting DCHPRIn[DPA]. When a channel's preempt ability is disabled, that channel cannot suspend a lower priority channel's data transfer, regardless of the lower priority channel's ECP setting. This allows for a pool of low priority, large data-moving channels to be defined. These low priority channels can be configured to not preempt each other, thus preventing a low priority channel from consuming the preempt slot normally available to a true, high priority channel.

26.4.4 Performance

This section addresses the performance of the eDMA module, focusing on two separate metrics:

- In the traditional data movement context, performance is best expressed as the peak data transfer rates achieved using the eDMA. In most implementations, this transfer rate is limited by the speed of the source and destination address spaces.
- In a second context where device-paced movement of single data values to/from peripherals is dominant, a measure of the requests that can be serviced in a fixed time is a more relevant metric. In this environment, the speed of the source and destination address spaces remains important. However, the microarchitecture of the eDMA also factors significantly into the resulting metric.

26.4.4.1 Peak transfer rates

The peak transfer rates for several different source and destination transfers are shown in the following tables. These tables assume:

- Internal SRAM can be accessed with zero wait-states when viewed from the system bus data phase
- All internal peripheral bus reads require two wait-states, and internal peripheral bus writes three wait-states, when viewed from the system bus data phase
- All internal peripheral bus accesses are 32-bits in size

NOTE

All architectures will not meet the assumptions listed above. See the SRAM configuration section for more information.

This table compares peak transfer rates based on different possible system speeds. Specific chips/devices may not support all system speeds listed.

Table 26-4. eDMA peak transfer rates (Mbytes/sec)

System Speed, Width	Internal SRAM-to-Internal SRAM	32 bit internal peripheral bus-to-Internal SRAM	Internal SRAM-to-32 bit internal peripheral bus
66.7 MHz, 32 bit	133.3	66.7	53.3
83.3 MHz, 32 bit	166.7	83.3	66.7
100.0 MHz, 32 bit	200.0	100.0	80.0
133.3 MHz, 32 bit	266.7	133.3	106.7
150.0 MHz, 32 bit	300.0	150.0	120.0

Internal-SRAM-to-internal-SRAM transfers occur at the core's datapath width. For all transfers involving the internal peripheral bus, 32-bit transfer sizes are used. In all cases, the transfer rate includes the time to read the source plus the time to write the destination.

26.4.4.2 Peak request rates

The second performance metric is a measure of the number of DMA requests that can be serviced in a given amount of time. For this metric, assume that the peripheral request causes the channel to move a single internal peripheral bus-mapped operand to/from internal SRAM. The same timing assumptions used in the previous example apply to this calculation. In particular, this metric also reflects the time required to activate the channel.

The eDMA design supports the following hardware service request sequence. Note that the exact timing from Cycle 7 is a function of the response times for the channel's read and write accesses. In the case of an internal peripheral bus read and internal SRAM write, the combined data phase time is 4 cycles. For an SRAM read and internal peripheral bus write, it is 5 cycles.

Table 26-5. Hardware service request process

Cycle		Description
With internal peripheral bus read and internal SRAM write	With SRAM read and internal peripheral bus write	
1		eDMA peripheral request is asserted.
2		The eDMA peripheral request is registered locally in the eDMA module and qualified. TCD*n*_CSR[START] bit initiated requests start at this point with the registering of the user write to TCD*n* word 7.
3		Channel arbitration begins.
4		Channel arbitration completes. The transfer control descriptor local memory read is initiated.
5–6		The first two parts of the activated channel's TCD is read from the local memory. The memory width to the eDMA engine is 64 bits, so the entire descriptor can be accessed in four cycles
7		The first system bus read cycle is initiated, as the third part of the channel's TCD is read from the local memory. Depending on the state of the crossbar switch, arbitration at the system bus may insert an additional cycle of delay here.
8–11	8–12	The last part of the TCD is read in. This cycle represents the first data phase for the read, and the address phase for the destination write.
12	13	This cycle represents the data phase of the last destination write.
13	14	The eDMA engine completes the execution of the inner minor loop and prepares to write back the required TCD*n* fields into the local memory. The TCD*n* word 7 is read and checked for channel linking or scatter/gather requests.
14	15	The appropriate fields in the first part of the TCD*n* are written back into the local memory.
15	16	The fields in the second part of the TCD*n* are written back into the local memory. This cycle coincides with the next channel arbitration cycle start.
16	17	The next channel to be activated performs the read of the first part of its TCD from the local memory. This is equivalent to Cycle 4 for the first channel's service request.

Assuming zero wait states on the system bus, DMA requests can be processed every 9 cycles. Assuming an average of the access times associated with internal peripheral bus-to-SRAM (4 cycles) and SRAM-to-internal peripheral bus (5 cycles), DMA requests can be processed every 11.5 cycles (4 + (4+5)/2 + 3). This is the time from Cycle 4 to Cycle x +5. The resulting peak request rate, as a function of the system frequency, is shown in the following table.

Table 26-6. eDMA peak request rate (MReq/sec)

System frequency (MHz)	Request rate with zero wait states	Request rate with wait states
66.6	7.4	5.8
83.3	9.2	7.2
100.0	11.1	8.7
133.3	14.8	11.6
150.0	16.6	13.0

A general formula to compute the peak request rate with overlapping requests is:

PEAKreq = freq / [entry + (1 + read_ws) + (1 + write_ws) + exit]

where:

Table 26-7. Peak request formula operands

Operand	Description
PEAKreq	Peak request rate
freq	System frequency
entry	Channel startup (4 cycles)
read_ws	Wait states seen during the system bus read data phase
write_ws	Wait states seen during the system bus write data phase
exit	Channel shutdown (3 cycles)

26.4.4.3 eDMA performance example

Consider a system with the following characteristics:

- Internal SRAM can be accessed with one wait-state when viewed from the system bus data phase
- All internal peripheral bus reads require two wait-states, and internal peripheral bus writes three wait-states viewed from the system bus data phase
- System operates at 150 MHz

For an SRAM to internal peripheral bus transfer,

PEAKreq = 150 MHz / [4 + (1 + 1) + (1 + 3) + 3] cycles = 11.5 Mreq/sec

For an internal peripheral bus to SRAM transfer,

PEAKreq = 150 MHz / [4 + (1 + 2) + (1 + 1) + 3] cycles = 12.5 Mreq/sec

Assuming an even distribution of the two transfer types, the average peak request rate would be:

PEAKreq = (11.5 Mreq/sec + 12.5 Mreq/sec) / 2 = 12.0 Mreq/sec

The minimum number of cycles to perform a single read/write, zero wait states on the system bus, from a cold start where no channel is executing and eDMA is idle are:

- 11 cycles for a software, that is, a TCD*n*_CSR[START] bit, request
- 12 cycles for a hardware, that is, an eDMA peripheral request signal, request

Two cycles account for the arbitration pipeline and one extra cycle on the hardware request resulting from the internal registering of the eDMA peripheral request signals. For the peak request rate calculations above, the arbitration and request registering is absorbed in or overlaps the previous executing channel.

Note

When channel linking or scatter/gather is enabled, a two cycle delay is imposed on the next channel selection and startup. This allows the link channel or the scatter/gather channel to be eligible and considered in the arbitration pool for next channel selection.

26.5 Initialization/application information

The following sections discuss initialization of the eDMA and programming considerations.

26.5.1 eDMA initialization

To initialize the eDMA:

1. Write to the CR if a configuration other than the default is desired.
2. Write the channel priority levels to the DCHPRI*n* registers if a configuration other than the default is desired.
3. Enable error interrupts in the EEI register if so desired.
4. Write the 32-byte TCD for each channel that may request service.

5. Enable any hardware service requests via the ERQH and ERQL registers.
6. Request channel service via either:
   - Software: setting the TCD*n*_CSR[START]
   - Hardware: slave device asserting its eDMA peripheral request signal

After any channel requests service, a channel is selected for execution based on the arbitration and priority levels written into the programmer's model. The eDMA engine reads the entire TCD, including the TCD control and status fields, as shown in the following table, for the selected channel into its internal address path module.

As the TCD is read, the first transfer is initiated on the internal bus, unless a configuration error is detected. Transfers from the source, as defined by TCD*n*_SADDR, to the destination, as defined by TCD*n*_DADDR, continue until the number of bytes specified by TCD*n*_NBYTES are transferred.

When the transfer is complete, the eDMA engine's local TCD*n*_SADDR, TCD*n*_DADDR, and TCD*n*_CITER are written back to the main TCD memory and any minor loop channel linking is performed, if enabled. If the major loop is exhausted, further post processing executes, such as interrupts, major loop channel linking, and scatter/gather operations, if enabled.

Table 26-8. TCD Control and Status fields

TCD*n*_CSR field name	Description
START	Control bit to start channel explicitly when using a software initiated DMA service (Automatically cleared by hardware)
ACTIVE	Status bit indicating the channel is currently in execution
DONE	Status bit indicating major loop completion (cleared by software when using a software initiated DMA service)
D_REQ	Control bit to disable DMA request at end of major loop completion when using a hardware initiated DMA service
BWC	Control bits for throttling bandwidth control of a channel
E_SG	Control bit to enable scatter-gather feature
INT_HALF	Control bit to enable interrupt when major loop is half complete
INT_MAJ	Control bit to enable interrupt when major loop completes

The following figure shows how each DMA request initiates one minor-loop transfer, or iteration, without CPU intervention. DMA arbitration can occur after each minor loop, and one level of minor loop DMA preemption is allowed. The number of minor loops in a major loop is specified by the beginning iteration count (BITER).

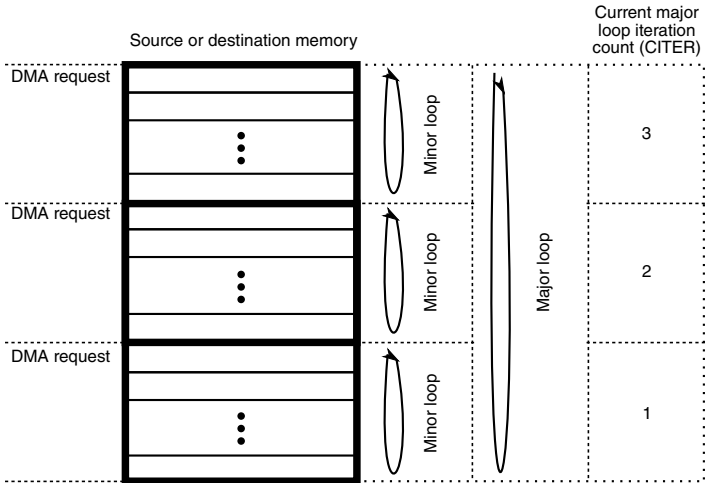


Figure 26-5. Example of multiple loop iterations

The following figure lists the memory array terms and how the TCD settings interrelate.

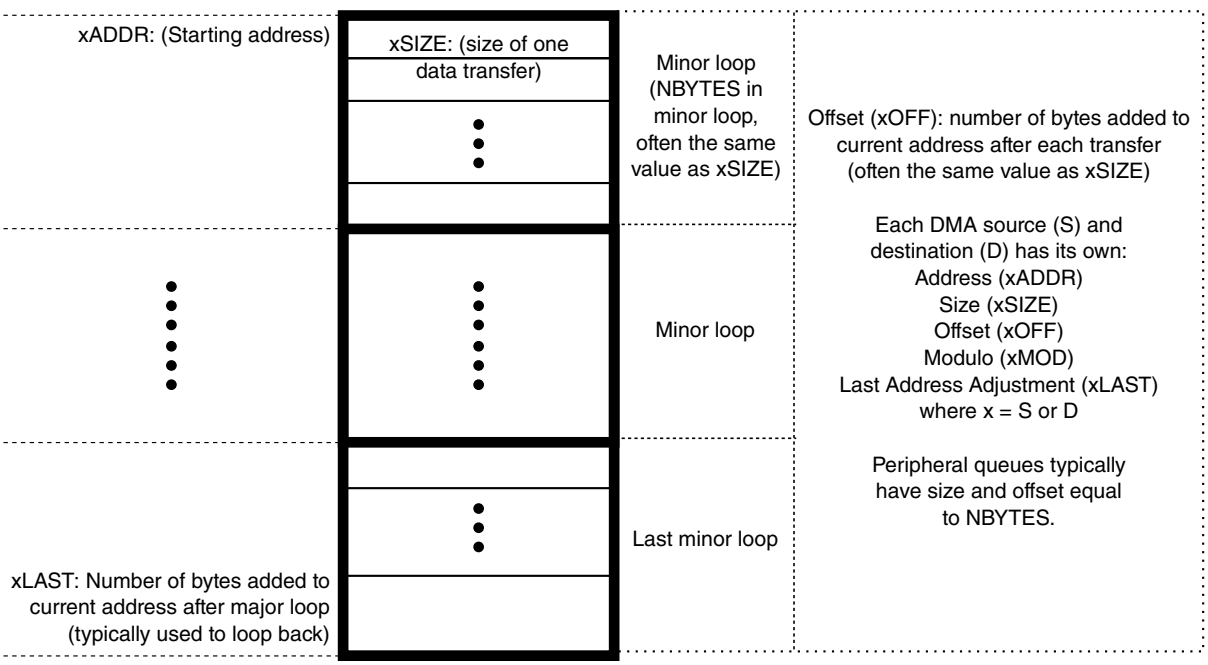


Figure 26-6. Memory array terms

26.5.2 Programming errors

The eDMA performs various tests on the transfer control descriptor to verify consistency in the descriptor data. Most programming errors are reported on a per channel basis with the exception of channel priority error (ES[CPE]).

For all error types other than group or channel priority errors, the channel number causing the error is recorded in the Error Status register (DMAx_ES). If the error source is not removed before the next activation of the problem channel, the error is detected and recorded again.

Channel priority errors are identified within a group once that group has been selected as the active group. For example:

1. The eDMA is configured for fixed group and fixed channel arbitration modes.
2. Group 1 is the highest priority and all channels are unique in that group.
3. Group 0 is the next highest priority and has two channels with the same priority level.
4. If Group 1 has any service requests, those requests will be executed.
5. After all of Group 1 requests have completed, Group 0 will be the next active group.
6. If Group 0 has a service request, then an undefined channel in Group 0 will be selected and a channel priority error will occur.
7. This repeats until the all of Group 0 requests have been removed or a higher priority Group 1 request comes in.

In this sequence, for item 2, the eDMA acknowledge lines will assert only if the selected channel is requesting service via the eDMA peripheral request signal. If interrupts are enabled for all channels, the user will get an error interrupt, but the channel number for the ERR register and the error interrupt request line may be wrong because they reflect the selected channel. A group priority error is global and any request in any group will cause a group priority error.

If priority levels are not unique, when any channel requests service, a channel priority error is reported. The highest channel/group priority with an active request is selected, but the lowest numbered channel with that priority is selected by arbitration and executed by the eDMA engine. The hardware service request handshake signals, error interrupts, and error reporting is associated with the selected channel.

26.5.3 Arbitration mode considerations

This section discusses arbitration considerations for the eDMA.

26.5.3.1 Fixed group arbitration, Fixed channel arbitration

In this mode, the channel service request from the highest priority channel in the highest priority group is selected to execute. If the eDMA is programmed so that the channels within one group use "fixed" priorities, and that group is assigned the highest "fixed" priority of all groups, that group can take all the bandwidth of the eDMA controller. That is, no other groups will be serviced if there is always at least one DMA request pending on a channel in the highest priority group when the controller arbitrates the next DMA request. The advantage of this scenario is that latency can be small for channels that need to be serviced quickly. Preemption is available in this scenario only.

26.5.3.2 Fixed group arbitration, Round-robin channel arbitration

The highest priority group with a request will be serviced. Lower priority groups will be serviced if no pending requests exist in the higher priority groups.

Within each group, channels are serviced starting with the highest channel number and rotating through to the lowest channel number without regard to the channel priority levels assigned within the group.

This scenario could cause the same bandwidth consumption problem as indicated in Fixed group arbitration, Fixed channel arbitration, but all the channels in the highest priority group will be serviced. Service latency will be short on the highest priority group, but could potentially be very much longer as the group priority decreases.

26.5.4 Performing DMA transfers

This section presents examples on how to perform DMA transfers with the eDMA.

26.5.4.1 Single request

To perform a simple transfer of n bytes of data with one activation, set the major loop to one (TCD*n*_CITER = TCD*n*_BITER = 1). The data transfer begins after the channel service request is acknowledged and the channel is selected to execute. After the transfer is complete, the TCD*n*_CSR[DONE] bit is set and an interrupt generates if properly enabled.

For example, the following TCD entry is configured to transfer 16 bytes of data. The eDMA is programmed for one iteration of the major loop transferring 16 bytes per iteration. The source memory has a byte wide memory port located at 0x1000. The destination memory has a 32-bit port located at 0x2000. The address offsets are

programmed in increments to match the transfer size: one byte for the source and four bytes for the destination. The final source and destination addresses are adjusted to return to their beginning values.

```
TCDn_CITER = TCDn_BITER = 1
TCDn_NBYTES = 16
TCDn_SADDR = 0x1000
TCDn_SOFF = 1
TCDn_ATTR[SSIZE] = 0
TCDn_SLAST = -16
TCDn_DADDR = 0x2000
TCDn_DOFF = 4
TCDn_ATTR[DSIZE] = 2
TCDn_DLAST_SGA= -16
TCDn_CSR[INT_MAJ] = 1
TCDn_CSR[START] = 1 (Should be written last after all other fields have been initialized)
All other TCDn fields = 0
```

This generates the following event sequence:

1. User write to the TCD*n*_CSR[START] bit requests channel service.
2. The channel is selected by arbitration for servicing.
3. eDMA engine writes: TCD*n*_CSR[DONE] = 0, TCD*n*_CSR[START] = 0, TCD*n*_CSR[ACTIVE] = 1.
4. eDMA engine reads: channel TCD data from local memory to internal register file.
5. The source-to-destination transfers are executed as follows:
   a. Read byte from location 0x1000, read byte from location 0x1001, read byte from 0x1002, read byte from 0x1003.
   b. Write 32-bits to location 0x2000 → first iteration of the minor loop.
   c. Read byte from location 0x1004, read byte from location 0x1005, read byte from 0x1006, read byte from 0x1007.
   d. Write 32-bits to location 0x2004 → second iteration of the minor loop.
   e. Read byte from location 0x1008, read byte from location 0x1009, read byte from 0x100A, read byte from 0x100B.
   f. Write 32-bits to location 0x2008 → third iteration of the minor loop.
   g. Read byte from location 0x100C, read byte from location 0x100D, read byte from 0x100E, read byte from 0x100F.
   h. Write 32-bits to location 0x200C → last iteration of the minor loop → major loop complete.

6. The eDMA engine writes: TCD*n*_SADDR = 0x1000, TCD*n*_DADDR = 0x2000, TCD*n*_CITER = 1 (TCD*n*_BITER).
7. The eDMA engine writes: TCD*n*_CSR[ACTIVE] = 0, TCD*n*_CSR[DONE] = 1, INT[*n*] = 1.
8. The channel retires and the eDMA goes idle or services the next channel.

26.5.4.2 Multiple requests

The following example transfers 32 bytes via two hardware requests, but is otherwise the same as the previous example. The only fields that change are the major loop iteration count and the final address offsets. The eDMA is programmed for two iterations of the major loop transferring 16 bytes per iteration. After the channel's hardware requests are enabled in the ERQ register, the slave device initiates channel service requests.

```
TCDn_CITER = TCDn_BITER = 2
TCDn_SLAST = -32
TCDn_DLAST_SGA = -32
```

This would generate the following sequence of events:

1. First hardware, that is, eDMA peripheral, request for channel service.
2. The channel is selected by arbitration for servicing.
3. eDMA engine writes: TCD*n*_CSR[DONE] = 0, TCD*n*_CSR[START] = 0, TCD*n*_CSR[ACTIVE] = 1.
4. eDMA engine reads: channel TCD*n* data from local memory to internal register file.
5. The source to destination transfers are executed as follows:
   a. Read byte from location 0x1000, read byte from location 0x1001, read byte from 0x1002, read byte from 0x1003.
   b. Write 32-bits to location 0x2000 → first iteration of the minor loop.
   c. Read byte from location 0x1004, read byte from location 0x1005, read byte from 0x1006, read byte from 0x1007.
   d. Write 32-bits to location 0x2004 → second iteration of the minor loop.
   e. Read byte from location 0x1008, read byte from location 0x1009, read byte from 0x100A, read byte from 0x100B.
   f. Write 32-bits to location 0x2008 → third iteration of the minor loop.

g. Read byte from location 0x100C, read byte from location 0x100D, read byte from 0x100E, read byte from 0x100F.

h. Write 32-bits to location 0x200C → last iteration of the minor loop.

6. eDMA engine writes: TCD*n*_SADDR = 0x1010, TCD*n*_DADDR = 0x2010, TCD*n*_CITER = 1.

7. eDMA engine writes: TCD*n*_CSR[ACTIVE] = 0.

8. The channel retires → one iteration of the major loop. The eDMA goes idle or services the next channel.

9. Second hardware, that is, eDMA peripheral, requests channel service.

10. The channel is selected by arbitration for servicing.

11. eDMA engine writes: TCD*n*_CSR[DONE] = 0, TCD*n*_CSR[START] = 0, TCD*n*_CSR[ACTIVE] = 1.

12. eDMA engine reads: channel TCD data from local memory to internal register file.

13. The source to destination transfers are executed as follows:

a. Read byte from location 0x1010, read byte from location 0x1011, read byte from 0x1012, read byte from 0x1013.

b. Write 32-bits to location 0x2010 → first iteration of the minor loop.

c. Read byte from location 0x1014, read byte from location 0x1015, read byte from 0x1016, read byte from 0x1017.

d. Write 32-bits to location 0x2014 → second iteration of the minor loop.

e. Read byte from location 0x1018, read byte from location 0x1019, read byte from 0x101A, read byte from 0x101B.

f. Write 32-bits to location 0x2018 → third iteration of the minor loop.

g. Read byte from location 0x101C, read byte from location 0x101D, read byte from 0x101E, read byte from 0x101F.

h. Write 32-bits to location 0x201C → last iteration of the minor loop → major loop complete.

14. eDMA engine writes: TCD*n*_SADDR = 0x1000, TCD*n*_DADDR = 0x2000, TCD*n*_CITER = 2 (TCD*n*_BITER).

15. eDMA engine writes: TCD*n*_CSR[ACTIVE] = 0, TCD*n*_CSR[DONE] = 1, INT[n] = 1.

16. The channel retires → major loop complete. The eDMA goes idle or services the next channel.

26.5.4.3 Using the modulo feature

The modulo feature of the eDMA provides the ability to implement a circular data queue in which the size of the queue is a power of 2. MOD is a 5-bit field for the source and destination in the TCD, and it specifies which lower address bits increment from their original value after the address+offset calculation. All upper address bits remain the same as in the original value. A setting of 0 for this field disables the modulo feature.

The following table shows how the transfer addresses are specified based on the setting of the MOD field. Here a circular buffer is created where the address wraps to the original value while the 28 upper address bits (0x1234567*x*) retain their original value. In this example the source address is set to 0x12345670, the offset is set to 4 bytes and the MOD field is set to 4, allowing for a 2^4 byte (16-byte) size queue.

Table 26-9. Modulo example

Transfer Number	Address
1	0x12345670
2	0x12345674
3	0x12345678
4	0x1234567C
5	0x12345670
6	0x12345674

26.5.5 Monitoring transfer descriptor status

This section discusses how to monitor eDMA status.

26.5.5.1 Testing for minor loop completion

There are two methods to test for minor loop completion when using software initiated service requests. The first is to read the TCD*n*_CITER field and test for a change. Another method may be extracted from the sequence shown below. The second method is to test the TCD*n*_CSR[START] bit and the TCD*n*_CSR[ACTIVE] bit. The minor-loop-

complete condition is indicated by both bits reading zero after the TCD*n*_CSR[START] was set. Polling the TCD*n*_CSR[ACTIVE] bit may be inconclusive, because the active status may be missed if the channel execution is short in duration.

The TCD status bits execute the following sequence for a software activated channel:

Stage	TCD*n*_CSR bits			State
	START	ACTIVE	DONE	
1	1	0	0	Channel service request via software
2	0	1	0	Channel is executing
3a	0	0	0	Channel has completed the minor loop and is idle
3b	0	0	1	Channel has completed the major loop and is idle

The best method to test for minor-loop completion when using hardware, that is, peripheral, initiated service requests is to read the TCD*n*_CITER field and test for a change. The hardware request and acknowledge handshake signals are not visible in the programmer's model.

The TCD status bits execute the following sequence for a hardware-activated channel:

Stage	TCD*n*_CSR bits			State
	START	ACTIVE	DONE	
1	0	0	0	Channel service request via hardware (peripheral request asserted)
2	0	1	0	Channel is executing
3a	0	0	0	Channel has completed the minor loop and is idle
3b	0	0	1	Channel has completed the major loop and is idle

For both activation types, the major-loop-complete status is explicitly indicated via the TCD*n*_CSR[DONE] bit.

The TCD*n*_CSR[START] bit is cleared automatically when the channel begins execution regardless of how the channel activates.

26.5.5.2 Reading the transfer descriptors of active channels

The eDMA reads back the true TCD*n*_SADDR, TCD*n*_DADDR, and TCD*n*_NBYTES values if read while a channel executes. The true values of the SADDR, DADDR, and NBYTES are the values the eDMA engine currently uses in its internal register file and not the values in the TCD local memory for that channel. The addresses, SADDR and

DADDR, and NBYTES, which decrement to zero as the transfer progresses, can give an indication of the progress of the transfer. All other values are read back from the TCD local memory.

26.5.5.3 Checking channel preemption status

Preemption is available only when fixed arbitration is selected for both group and channel arbitration modes. A preemptive situation is one in which a preempt-enabled channel runs and a higher priority request becomes active. When the eDMA engine is not operating in fixed group, fixed channel arbitration mode, the determination of the actively running relative priority outstanding requests become undefined. Channel and/or group priorities are treated as equal, that is, constantly rotating, when Round-Robin Arbitration mode is selected.

The TCD*n*_CSR[ACTIVE] bit for the preempted channel remains asserted throughout the preemption. The preempted channel is temporarily suspended while the preempting channel executes one major loop iteration. If two TCD*n*_CSR[ACTIVE] bits are set simultaneously in the global TCD map, a higher priority channel is actively preempting a lower priority channel.

26.5.6 Channel Linking

Channel linking (or chaining) is a mechanism where one channel sets the TCD*n*_CSR[START] bit of another channel (or itself), therefore initiating a service request for that channel. When properly enabled, the EDMA engine automatically performs this operation at the major or minor loop completion.

The minor loop channel linking occurs at the completion of the minor loop (or one iteration of the major loop). The TCD*n*_CITER[E_LINK] field determines whether a minor loop link is requested. When enabled, the channel link is made after each iteration of the major loop except for the last. When the major loop is exhausted, only the major loop channel link fields are used to determine if a channel link should be made. For example, the initial fields of:

```
TCDn_CITER[E_LINK] = 1
TCDn_CITER[LINKCH] = 0xC
TCDn_CITER[CITER] value = 0x4
TCDn_CSR[MAJOR_E_LINK] = 1
TCDn_CSR[MAJOR_LINKCH] = 0x7
```

executes as:

1. Minor loop done → set TCD12_CSR[START] bit

2. Minor loop done → set TCD12_CSR[START] bit
3. Minor loop done → set TCD12_CSR[START] bit
4. Minor loop done, major loop done→ set TCD7_CSR[START] bit

When minor loop linking is enabled (TCD*n*_CITER[E_LINK] = 1), the TCD*n*_CITER[CITER] field uses a nine bit vector to form the current iteration count. When minor loop linking is disabled (TCD*n*_CITER[E_LINK] = 0), the TCD*n*_CITER[CITER] field uses a 15-bit vector to form the current iteration count. The bits associated with the TCD*n*_CITER[LINKCH] field are concatenated onto the CITER value to increase the range of the CITER.

Note

The TCD*n*_CITER[E_LINK] bit and the TCD*n*_BITER[E_LINK] bit must equal or a configuration error is reported. The CITER and BITER vector widths must be equal to calculate the major loop, half-way done interrupt point.

The following table summarizes how a DMA channel can link to another DMA channel, i.e, use another channel's TCD, at the end of a loop.

Table 26-10. Channel Linking Parameters

Desired Link Behavior	TCD Control Field Name	Description
Link at end of Minor Loop	CITER[E_LINK]	Enable channel-to-channel linking on minor loop completion (current iteration)
	CITER[LINKCH]	Link channel number when linking at end of minor loop (current iteration)
Link at end of Major Loop	CSR[MAJOR_E_LINK]	Enable channel-to-channel linking on major loop completion
	CSR[MAJOR_LINKCH]	Link channel number when linking at end of major loop

26.5.7 Dynamic programming

This section provides recommended methods to change the programming model during channel execution.

26.5.7.1 Dynamically changing the channel priority

The following two options are recommended for dynamically changing channel priority levels:

1. Switch to Round-Robin Channel Arbitration mode, change the channel priorities, then switch back to Fixed Arbitration mode,
2. Disable all the channels, change the channel priorities, then enable the appropriate channels.

26.5.7.2 Dynamic channel linking

Dynamic channel linking is the process of setting the TCD.major.e_link bit during channel execution (see the diagram in TCD structure). This bit is read from the TCD local memory at the end of channel execution, thus allowing the user to enable the feature during channel execution.

Because the user is allowed to change the configuration during execution, a coherency model is needed. Consider the scenario where the user attempts to execute a dynamic channel link by enabling the TCD.major.e_link bit at the same time the eDMA engine is retiring the channel. The TCD.major.e_link would be set in the programmer's model, but it would be unclear whether the actual link was made before the channel retired.

The following coherency model is recommended when executing a dynamic channel link request.

1. Write 1 to the TCD.major.e_link bit.
2. Read back the TCD.major.e_link bit.
3. Test the TCD.major.e_link request status:
   - If TCD.major.e_link = 1, the dynamic link attempt was successful.
   - If TCD.major.e_link = 0, the attempted dynamic link did not succeed (the channel was already retiring).

For this request, the TCD local memory controller forces the TCD.major.e_link bit to zero on any writes to a channel's TCD.word7 after that channel's TCD.done bit is set, indicating the major loop is complete.

NOTE

The user must clear the TCD.done bit before writing the TCD.major.e_link bit. The TCD.done bit is cleared automatically by the eDMA engine after a channel begins execution.

26.5.7.3 Dynamic scatter/gather

Scatter/gather is the process of automatically loading a new TCD into a channel. It allows a DMA channel to use multiple TCDs; this enables a DMA channel to scatter the DMA data to multiple destinations or gather it from multiple sources.When scatter/gather is enabled and the channel has finished its major loop, a new TCD is fetched from system memory and loaded into that channel's descriptor location in eDMA programmer's model, thus replacing the current descriptor.

Because the user is allowed to change the configuration during execution, a coherency model is needed. Consider the scenario where the user attempts to execute a dynamic scatter/gather operation by enabling the TCD.e_sg bit at the same time the eDMA engine is retiring the channel. The TCD.e_sg would be set in the programmer's model, but it would be unclear whether the actual scatter/gather request was honored before the channel retired.

Two methods for this coherency model are shown in the following subsections. Method 1 has the advantage of reading the major.linkch field and the e_sg bit with a single read. For both dynamic channel linking and scatter/gather requests, the TCD local memory controller forces the TCD.major.e_link and TCD.e_sg bits to zero on any writes to a channel's TCD.word7 if that channel's TCD.done bit is set indicating the major loop is complete.

NOTE

The user must clear the TCD.done bit before writing the TCD.major.e_link or TCD.e_sg bits. The TCD.done bit is cleared automatically by the eDMA engine after a channel begins execution.

26.5.7.3.1 Method 1 (channel not using major loop channel linking)

For a channel not using major loop channel linking, the coherency model described here may be used for a dynamic scatter/gather request.

When the TCD.major.e_link bit is zero, the TCD.major.linkch field is not used by the eDMA. In this case, the TCD.major.linkch bits may be used for other purposes. This method uses the TCD.major.linkch field as a TCD indentification (ID).

1. When the descriptors are built, write a unique TCD ID in the TCD.major.linkch field for each TCD associated with a channel using dynamic scatter/gather.
2. Write 1b to the TCD.d_req bit.

Should a dynamic scatter/gather attempt fail, setting the TCD.d_req bit will prevent a future hardware activation of this channel. This stops the channel from executing with a destination address (daddr) that was calculated using a scatter/gather address (written in the next step) instead of a dlast final offest value.

3. Write the TCD.dlast_sga field with the scatter/gather address.
4. Write 1b to the TCD.e_sg bit.
5. Read back the 16 bit TCD control/status field.
6. Test the TCD.e_sg request status and TCD.major.linkch value:

   If e_sg = 1b, the dynamic link attempt was successful.

   If e_sg = 0b and the major.linkch (ID) did not change, the attempted dynamic link did not succeed (the channel was already retiring).

   If e_sg = 0b and the major.linkch (ID) changed, the dynamic link attempt was successful (the new TCD's e_sg value cleared the e_sg bit).

26.5.7.3.2 Method 2 (channel using major loop channel linking)

For a channel using major loop channel linking, the coherency model described here may be used for a dynamic scatter/gather request. This method uses the TCD.dlast_sga field as a TCD indentification (ID).

1. Write 1b to the TCD.d_req bit.

   Should a dynamic scatter/gather attempt fail, setting the d_req bit will prevent a future hardware activation of this channel. This stops the channel from executing with a destination address (daddr) that was calculated using a scatter/gather address (written in the next step) instead of a dlast final offest value.

2. Write theTCD.dlast_sga field with the scatter/gather address.
3. Write 1b to the TCD.e_sg bit.
4. Read back the TCD.e_sg bit.
5. Test the TCD.e_sg request status:

   If e_sg = 1b, the dynamic link attempt was successful.

   If e_sg = 0b, read the 32 bit TCD dlast_sga field.

   If e_sg = 0b and the dlast_sga did not change, the attempted dynamic link did not succeed (the channel was already retiring).

If e_sg = 0b and the dlast_sga changed, the dynamic link attempt was successful (the new TCD's e_sg value cleared the e_sg bit).

Chapter 27
External Watchdog Monitor (EWM)

27.1 Chip-specific EWM information

27.1.1 EWM clocks

This table shows the EWM clocks and the corresponding chip clocks.

Table 27-1. EWM clock connections

Module clock	Chip clock
Low Power Clock	1 kHz LPO Clock

NOTE

lpo_clk[0] is the only available low power clock source on this chip. lpo_clk[3:1] clocks are reserved.

27.1.2 EWM low-power modes

This table shows the EWM low-power modes and the corresponding chip low-power modes.

Table 27-2. EWM low-power modes

Module mode	Chip mode
Wait	Wait, VLPW
Stop	Stop, VLPS, LLS

27.1.3 $\overline{\text{EWM_OUT}}$ pin state in low power modes

During Wait, Stop and Power Down modes the $\overline{\text{EWM_OUT}}$ pin preserves its state before entering Wait or Stop mode. When the CPU enters a Run mode from Wait or Stop recovery, the pin resumes its previous state before entering Wait or Stop mode. When the CPU enters Run mode from Power Down, the pin returns to its reset state.

27.2 Introduction

The watchdog is generally used to monitor the flow and execution of embedded software within an MCU. The watchdog consists of a counter that if allowed to overflow, forces an internal reset (asynchronous) to all on-chip peripherals and optionally assert the $\overline{\text{RESET}}$ pin to reset external devices/circuits. The overflow of the watchdog counter must not occur if the software code works well and services the watchdog to re-start the actual counter.

For safety, a redundant watchdog system, External Watchdog Monitor (EWM), is designed to monitor external circuits, as well as the MCU software flow. This provides a back-up mechanism to the internal watchdog that resets the MCU's CPU and peripherals.

The EWM differs from the internal watchdog in that it does not reset the MCU's CPU and peripherals. The EWM if allowed to time-out, provides an independent $\overline{\text{EWM_out}}$ pin that when asserted resets or places an external circuit into a safe mode. The CPU resets the EWM counter that is logically ANDed with an external digital input pin. This pin allows an external circuit to influence the reset_out signal.

27.2.1 Features

Features of EWM module include:

- Independent LPO clock source
- Programmable time-out period specified in terms of number of EWM LPO clock cycles.
- Windowed refresh option
  - Provides robust check that program flow is faster than expected.
  - Programmable window.
  - Refresh outside window leads to assertion of $\overline{\text{EWM_out}}$.
- Robust refresh mechanism

- Write values of 0xB4 and 0x2C to EWM Refresh Register within 15 (*EWM_service_time*) peripheral bus clock cycles.

- One output port, $\overline{\text{EWM_out}}$, when asserted is used to reset or place the external circuit into safe mode.
- One Input port, EWM_in, allows an external circuit to control the $\overline{\text{EWM_out}}$ signal.

27.2.2 Modes of Operation

This section describes the module's operating modes.

27.2.2.1 Stop Mode

When the EWM is in stop mode, the CPU services to the EWM cannot occur. On entry to stop mode, the EWM's counter freezes.

There are two possible ways to exit from Stop mode:

- On exit from stop mode through a reset, the EWM remains disabled.
- On exit from stop mode by an interrupt, the EWM is re-enabled, and the counter continues to be clocked from the same value prior to entry to stop mode.

Note the following if the EWM enters the stop mode during CPU service mechanism: At the exit from stop mode by an interrupt, refresh mechanism state machine starts from the previous state which means, if first service command is written correctly and EWM enters the stop mode immediately, the next command has to be written within the next 15 (*EWM_service_time*) peripheral bus clocks after exiting from stop mode. User must mask all interrupts prior to executing EWM service instructions.

27.2.2.2 Debug Mode

Entry to debug mode has no effect on the EWM.

- If the EWM is enabled prior to entry of debug mode, it remains enabled.
- If the EWM is disabled prior to entry of debug mode, it remains disabled.

27.2.3 Block Diagram

This figure shows the EWM block diagram.

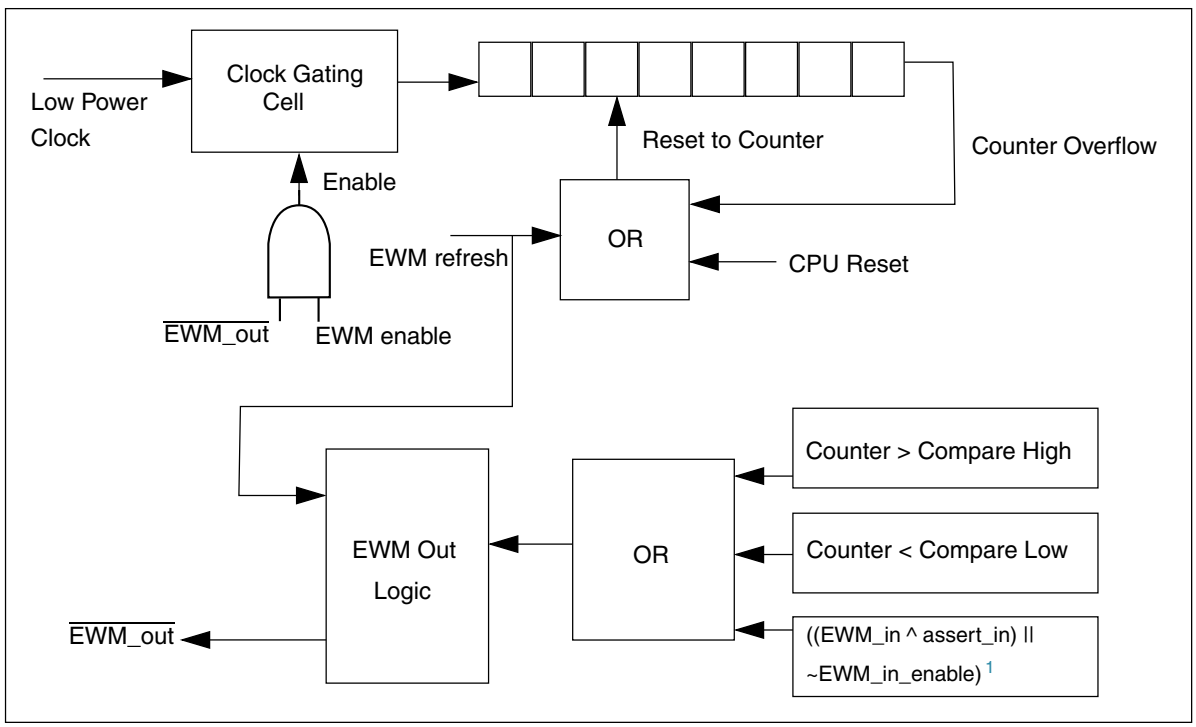


Figure 27-1. EWM Block Diagram

27.3 EWM Signal Descriptions

The EWM has two external signals and internal options for the counter clock sources, as shown in the following table.

Table 27-3. EWM Signal Descriptions

Signal	Description	I/O
EWM_in	EWM input for safety status of external safety circuits. The polarity of EWM_in is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low.	I
$\overline{\text{EWM_out}}$	EWM reset out signal	O
lpo_clk[3:0]	Low power clock sources for running counter	I

27.4 Memory Map/Register Definition

This section contains the module memory map and registers.

EWM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4006_1000	Control Register (EWM_CTRL)	8	R/W	00h	27.4.1/651
4006_1001	Service Register (EWM_SERV)	8	W (always reads 0)	00h	27.4.2/652
4006_1002	Compare Low Register (EWM_CMPL)	8	R/W	00h	27.4.3/652
4006_1003	Compare High Register (EWM_CMPH)	8	R/W	FFh	27.4.4/653
4006_1004	Clock Control Register (EWM_CLKCTRL)	8	R/W	00h	27.4.5/653
4006_1005	Clock Prescaler Register (EWM_CLKPRESCALER)	8	R/W	00h	27.4.6/654

27.4.1 Control Register (EWM_CTRL)

The CTRL register is cleared by any reset.

NOTE

INEN, ASSIN and EWMEN bits can be written once after a CPU reset. Modifying these bits more than once, generates a bus transfer error.

Address: 4006_1000h base + 0h offset = 4006_1000h

Bit	7	6	5	4	3	2	1	0
Read	0				INTEN	INEN	ASSIN	EWMEN
Write								
Reset	0	0	0	0	0	0	0	0

EWM_CTRL field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 INTEN	Interrupt Enable. This bit when set and $\overline{\text{EWM_out}}$ is asserted, an interrupt request is generated. To de-assert interrupt request, user should clear this bit by writing 0.
2 INEN	Input Enable. This bit when set, enables the EWM_in port.

Table continues on the next page...

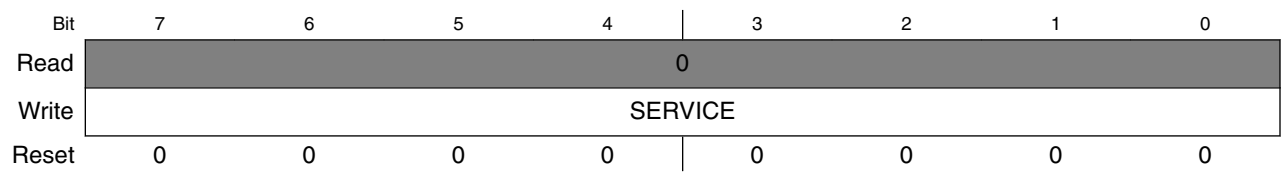
EWM_CTRL field descriptions (continued)

Field	Description
1 ASSIN	EWM_in's Assertion State Select. Default assert state of the EWM_in signal is logic zero. Setting ASSIN bit inverts the assert state to a logic one.
0 EWMEN	EWM enable. This bit when set, enables the EWM module. This resets the EWM counter to zero and deasserts the $\overline{\text{EWM_out}}$ signal. Clearing EWMEN bit disables the EWM, and therefore it cannot be enabled until a reset occurs, due to the write-once nature of this bit.

27.4.2 Service Register (EWM_SERV)

The SERV register provides the interface from the CPU to the EWM module. It is write-only and reads of this register return zero.

Address: 4006_1000h base + 1h offset = 4006_1001h



EWM_SERV field descriptions

Field	Description
SERVICE	The EWM service mechanism requires the CPU to write two values to the SERV register: a first data byte of 0xB4, followed by a second data byte of 0x2C. The EWM service is illegal if either of the following conditions is true. • The first or second data byte is not written correctly. • The second data byte is not written within a fixed number of peripheral bus cycles of the first data byte. This fixed number of cycles is called *EWM_service_time*.

27.4.3 Compare Low Register (EWM_CMPL)

The CMPL register is reset to zero after a CPU reset. This provides no minimum time for the CPU to service the EWM counter.

NOTE

This register can be written only once after a CPU reset. Writing this register more than once generates a bus transfer error.

Address: 4006_1000h base + 2h offset = 4006_1002h

Bit	7	6	5	4	3	2	1	0
Read Write	COMPAREL							
Reset	0	0	0	0	0	0	0	0

EWM_CMPL field descriptions

Field	Description
COMPAREL	To prevent runaway code from changing this field, software should write to this field after a CPU reset even if the (default) minimum service time is required.

27.4.4 Compare High Register (EWM_CMPH)

The CMPH register is reset to 0xFF after a CPU reset. This provides a maximum of 256 clocks time, for the CPU to service the EWM counter.

NOTE

This register can be written only once after a CPU reset. Writing this register more than once generates a bus transfer error.

NOTE

The valid values for CMPH are up to 0xFE because the EWM counter never expires when CMPH = 0xFF. The expiration happens only if EWM counter is greater than CMPH.

Address: 4006_1000h base + 3h offset = 4006_1003h

Bit	7	6	5	4	3	2	1	0
Read Write	COMPAREH							
Reset	1	1	1	1	1	1	1	1

EWM_CMPH field descriptions

Field	Description
COMPAREH	To prevent runaway code from changing this field, software should write to this field after a CPU reset even if the (default) maximum service time is required.

27.4.5 Clock Control Register (EWM_CLKCTRL)

This CLKCTRL register is reset to 0x00 after a CPU reset.

NOTE

This register can be written only once after a CPU reset. Writing this register more than once generates a bus transfer error.

NOTE

User should select the required low power clock before enabling the EWM.

Address: 4006_1000h base + 4h offset = 4006_1004h

Bit	7	6	5	4	3	2	1	0
Read	0						CLKSEL	
Write								
Reset	0	0	0	0	0	0	0	0

EWM_CLKCTRL field descriptions

Field	Description
7–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLKSEL	EWM has 4 possible low power clock sources for running EWM counter. One of the clock source can be selected by writing into this field. • 00 - lpo_clk[0] will be selected for running EWM counter. • 01 - lpo_clk[1] will be selected for running EWM counter. • 10 - lpo_clk[2] will be selected for running EWM counter. • 11 - lpo_clk[3] will be selected for running EWM counter.

27.4.6 Clock Prescaler Register (EWM_CLKPRESCALER)

This CLKPRESCALER register is reset to 0x00 after a CPU reset.

NOTE

This register can be written only once after a CPU reset. Writing this register more than once generates a bus transfer error.

NOTE

Write the required prescaler value before enabling the EWM.

NOTE

The implementation of this register is chip-specific. See the Chip Configuration details.

Address: 4006_1000h base + 5h offset = 4006_1005h

Bit	7	6	5	4	3	2	1	0
Read Write	CLK_DIV							
Reset	0	0	0	0	0	0	0	0

EWM_CLKPRESCALER field descriptions

Field	Description
CLK_DIV	Selected low power clock source for running the EWM counter can be prescaled as below. • Prescaled clock frequency = low power clock source frequency / (1 + CLK_DIV)

27.5 Functional Description

The following sections describe functional details of the EWM module.

27.5.1 The $\overline{\text{EWM_out}}$ Signal

The $\overline{\text{EWM_out}}$ is a digital output signal used to gate an external circuit (application specific) that controls critical safety functions. For example, the $\overline{\text{EWM_out}}$ could be connected to the high voltage transistors circuits that control an AC motor in a large appliance.

The $\overline{\text{EWM_out}}$ signal remains deasserted when the EWM is being regularly serviced by the CPU within the programmable service window, indicating that the application code is executed as expected.

The $\overline{\text{EWM_out}}$ signal is asserted in any of the following conditions:

- Servicing the EWM when the counter value is less than CMPL value.
- If the EWM counter value reaches the CMPH value, and no EWM service has occurred.
- Servicing the EWM when the counter value is more than CMPL and less than CMPH values and EWM_in signal is asserted.
- If functionality of EWM_in pin is enabled and EWM_in pin is asserted while servicing the EWM.
- After any reset (by the virtue of the external pull-down mechanism on the $\overline{\text{EWM_out}}$ pin)

On a normal reset, the $\overline{\text{EWM_out}}$ is asserted. To deassert the $\overline{\text{EWM_out}}$, set EWMEN bit in the CTRL register to enable the EWM.

If the $\overline{\text{EWM_out}}$ signal shares its pad with a digital I/O pin, on reset this actual pad defers to being an input signal. It takes the $\overline{\text{EWM_out}}$ output condition only after you enable the EWM by the EWMEN bit in the CTRL register.

When the EWM_out pin is asserted, it can only be deasserted by forcing a MCU reset.

Note

EWM_out pad must be in pull down state when EWM functionality is used and when EWM is under Reset.

27.5.2 The EWM_in Signal

The EWM_in is a digital input signal that allows an external circuit to control the EWM_out signal. For example, in the application, an external circuit monitors a critical safety function, and if there is fault with this circuit's behavior, it can then actively initiate the EWM_out signal that controls the gating circuit.

The EWM_in signal is ignored if the EWM is disabled, or if INEN bit of CTRL register is cleared, as after any reset.

On enabling the EWM (setting the CTRL[EWMEN] bit) and enabling EWM_in functionality (setting the CTRL[INEN] bit), the EWM_in signal must be in the deasserted state prior to the CPU servicing the EWM. This ensures that the EWM_out stays in the deasserted state; otherwise, the EWM_out pin is asserted.

Note

You must update the CMPH and CMPL registers prior to enabling the EWM. After enabling the EWM, the counter resets to zero, therefore providing a reasonable time after a power-on reset for the external monitoring circuit to stabilize and ensure that the EWM_in pin is deasserted.

27.5.3 EWM Counter

It is an 8-bit ripple counter fed from a clock source that is independent of the peripheral bus clock source. As the preferred time-out is between 1 ms and 100 ms the actual clock source should be in the kHz range.

The counter is reset to zero, after a CPU reset, or a EWM refresh cycle. The counter value is not accessible to the CPU.

27.5.4 EWM Compare Registers

The compare registers CMPL and CMPH are write-once after a CPU reset and cannot be modified until another CPU reset occurs.

The EWM compare registers are used to create a service window, which is used by the CPU to service/refresh the EWM module.

- If the CPU services the EWM when the counter value lies between CMPL value and CMPH value, the counter is reset to zero. This is a legal service operation.
- If the CPU executes a EWM service/refresh action outside the legal service window, $\overline{\text{EWM_out}}$ is asserted.

It is illegal to program CMPL and CMPH with same value. In this case, as soon as counter reaches (CMPL + 1), $\overline{\text{EWM_out}}$ is asserted.

27.5.5 EWM Refresh Mechanism

Other than the initial configuration of the EWM, the CPU can only access the EWM by the EWM Service Register. The CPU must access the EWM service register with correct write of unique data within the windowed time frame as determined by the CMPL and CMPH registers. Therefore, three possible conditions can occur:

Table 27-4. EWM Refresh Mechanisms

Condition	Mechanism
A unique EWM service occurs when CMPL < Counter < CMPH.	The software behaves as expected and the counter of the EWM is reset to zero, and $\overline{\text{EWM_out}}$ pin remains in the deasserted state. **Note:** EWM_in pin is also assumed to be in the deasserted state.
A unique EWM service occurs when Counter < CMPL	The software services the EWM and therefore resets the counter to zero and asserts the $\overline{\text{EWM_out}}$ pin (irrespective of the EWM_in pin). The $\overline{\text{EWM_out}}$ pin is expected to gate critical safety circuits.
Counter value reaches CMPH prior to a unique EWM service	The counter value reaches the CMPH value and no service of the EWM resets the counter to zero and assert the $\overline{\text{EWM_out}}$ pin (irrespective of the EWM_in pin). The $\overline{\text{EWM_out}}$ pin is expected to gate critical safety circuits.

Any illegal service on EWM has no effect on $\overline{\text{EWM_out}}$.

27.5.6 EWM Interrupt

When $\overline{\text{EWM_out}}$ is asserted, an interrupt request is generated to indicate the assertion of the EWM reset out signal. This interrupt is enabled when CTRL[INTEN] is set. Clearing this bit clears the interrupt request but does not affect $\overline{\text{EWM_out}}$. The $\overline{\text{EWM_out}}$ signal can be deasserted only by forcing a system reset.

27.5.7 Selecting the EWM counter clock

There are four possible low power clock sources for the EWM counter. Select one of the available clock sources by programming CLKCTRL[CLKSEL].

27.5.8 Counter clock prescaler

The EWM counter clock source can be prescaled by a clock divider, by programming CLKPRESCALER[CLK_DIV]. This divided clock is used to run the EWM counter.

NOTE

The divided clock used to run the EWM counter must be no more than half the frequency of the bus clock.

Chapter 28
Watchdog Timer (WDOG)

28.1 Chip-specific WDOG information

28.1.1 WDOG clocks

This table shows the WDOG module clocks and the corresponding chip clocks.

Table 28-1. WDOG clock connections

Module clock	Chip clock
LPO Oscillator	1 kHz LPO Clock
Alt Clock	Bus Clock
Fast Test Clock	Bus Clock
System Bus Clock	Bus Clock

28.1.2 WDOG low-power modes

This table shows the WDOG low-power modes and the corresponding chip low-power modes.

Table 28-2. WDOG low-power modes

Module mode	Chip mode
Wait	Wait, VLPW
Stop	Stop, VLPS
Power Down	LLS, VLLSx

28.2 Introduction

The Watchdog Timer (WDOG) keeps a watch on the system functioning and resets it in case of its failure. Reasons for failure include run-away software code and the stoppage of the system clock that in a safety critical system can lead to serious consequences. In such cases, the watchdog brings the system into a safe state of operation. The watchdog monitors the operation of the system by expecting periodic communication from the software, generally known as servicing or refreshing the watchdog. If this periodic refreshing does not occur, the watchdog resets the system.

28.3 Features

The features of the Watchdog Timer (WDOG) include:

- Clock source input independent from CPU/bus clock. Choice between two clock sources:
  - Low-power oscillator (LPO)
  - External system clock
- Unlock sequence for allowing updates to write-once WDOG control/configuration bits.
- All WDOG control/configuration bits are writable once only within 256 bus clock cycles of being unlocked.
  - You need to always update these bits after unlocking within 256 bus clock cycles. Failure to update these bits resets the system.
- Programmable time-out period specified in terms of number of WDOG clock cycles.
- Ability to test WDOG timer and reset with a flag indicating watchdog test.
  - Quick test—Small time-out value programmed for quick test.
  - Byte test—Individual bytes of timer tested one at a time.
  - Read-only access to the WDOG timer—Allows dynamic check that WDOG timer is operational.

NOTE

Reading the watchdog timer counter while running the watchdog on the bus clock might not give the accurate counter value.

- Windowed refresh option
  - Provides robust check that program flow is faster than expected.
  - Programmable window.
  - Refresh outside window leads to reset.
- Robust refresh mechanism
  - Write values of 0xA602 and 0xB480 to WDOG Refresh Register within 20 bus clock cycles.
- Count of WDOG resets as they occur.
- Configurable interrupt on time-out to provide debug breadcrumbs. This is followed by a reset after 256 bus clock cycles.

28.4 Functional overview

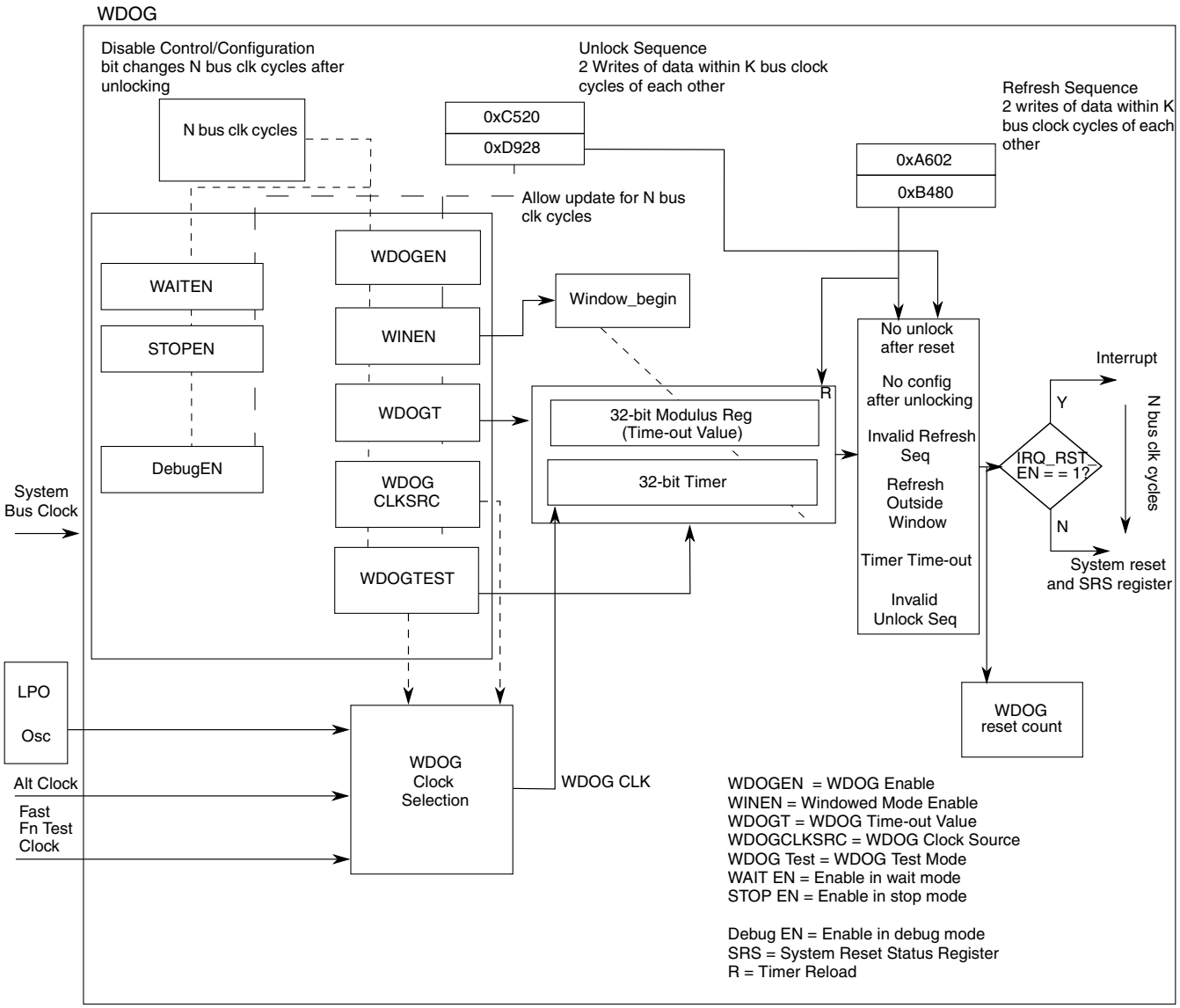


Figure 28-1. WDOG operation

The preceding figure shows the operation of the watchdog. The values for N and K are:

- N = 256
- K = 20

The watchdog is a fail safe mechanism that brings the system into a known initial state in case of its failure due to CPU clock stopping or a run-away condition in code execution. In its simplest form, the watchdog timer runs continuously off a clock source and expects to be serviced periodically, failing which it resets the system. This ensures that the software is executing correctly and has not run away in an unintended direction. Software can adjust the period of servicing or the time-out value for the watchdog timer to meet the needs of the application.

You can select a windowed mode of operation that expects the servicing to be done only in a particular window of the time-out period. An attempted servicing of the watchdog outside this window results in a reset. By operating in this mode, you can get an indication of whether the code is running faster than expected. The window length is also user programmable.

If a system fails to update/refresh the watchdog due to an unknown and persistent cause, it will be caught in an endless cycle of resets from the watchdog. To analyze the cause of such conditions, you can program the watchdog to first issue an interrupt, followed by a reset. In the interrupt service routine, the software can analyze the system stack to aid debugging.

To enhance the independence of watchdog from the system, it runs off an independent LPO oscillator clock. You can also switch over to an alternate clock source if required, through a control register bit.

28.4.1 Unlocking and updating the watchdog

As long as ALLOW_UPDATE in the watchdog control register is set, you can unlock and modify the write-once-only control and configuration registers:

1. Write 0xC520 followed by 0xD928 within 20 bus clock cycles to a specific unlock register (WDOG_UNLOCK).
2. Wait one bus clock cycle. You cannot update registers on the bus clock cycle immediately following the write of the unlock sequence.
3. An update window equal in length to the watchdog configuration time (WCT) opens. Within this window, you can update the configuration and control register bits.

These register bits can be modified only once after unlocking.

If none of the configuration and control registers is updated within the update window, the watchdog issues a reset, that is, interrupt-then-reset, to the system. Trying to unlock the watchdog within the WCT after an initial unlock has no effect. During the update operation, the watchdog timer is not paused and continues running in the background. After the update window closes, the watchdog timer restarts and the watchdog functions according to the new configuration.

The update feature is useful for applications that have an initial, non-safety critical part, where the watchdog is kept disabled or with a conveniently long time-out period. This means the application coder does not have to frequently service the watchdog. After the critical part of the application begins, the watchdog can be reconfigured as needed.

The watchdog issues a reset, that is, interrupt-then-reset if enabled, to the system for any of these invalid unlock sequences:

- Write any value other than 0xC520 or 0xD928 to the unlock register.
- ALLOW_UPDATE is set and a gap of more than 20 bus clock cycles is inserted between the writing of the unlock sequence values.

An attempted refresh operation between the two writes of the unlock sequence and in the WCT time following a successful unlock, goes undetected. Also, see Watchdog Operation with 8-bit access for guidelines related to 8-bit accesses to the unlock register.

Note

A context switch during unlocking and refreshing may lead to a watchdog reset.

28.4.2 Watchdog configuration time (WCT)

To prevent unintended modification of the watchdog's control and configuration register bits, you are allowed to update them only within a period of 256 bus clock cycles after unlocking. This period is known as the watchdog configuration time (WCT). In addition, these register bits can be modified only once after unlocking them for editing, even after reset.

You must unlock the registers within WCT after system reset, failing which the WDOG issues a reset to the system. In other words, you must write at least the first word of the unlocking sequence within the WCT after reset. After this is done, you have a further 20 bus clock cycles, the maximum allowed gap between the words of the unlock sequence, to complete the unlocking operation. Thereafter, to make sure that you do not forget to configure the watchdog, the watchdog issues a reset if none of the WDOG control and configuration registers is updated in the WCT after unlock. After the close of this window or after the first write, these register bits are locked out from any further changes.

The watchdog timer keeps running according to its default configuration through unlocking and update operations that can extend up to a maximum total of 2xWCT + 20 bus clock cycles. Therefore, it must be ensured that the time-out value for the watchdog is always greater than 2xWCT time + 20 bus clock cycles.

Updates in the write-once registers take effect only after the WCT window closes with the following exceptions for which changes take effect immediately:

- Stop, Wait, and Debug mode enable
- IRQ_RST_EN

The operations of refreshing the watchdog goes undetected during the WCT.

28.4.3 Refreshing the watchdog

A robust refreshing mechanism has been chosen for the watchdog. A valid refresh is a write of 0xA602 followed by 0xB480 within 20 bus clock cycles to watchdog refresh register. If these two values are written more than 20 bus cycles apart or if something other than these two values is written to the register, a watchdog reset, or interrupt-then-reset if enabled, is issued to the system. A valid refresh makes the watchdog timer restart on the next bus clock. Also, an attempted unlock operation in between the two writes of the refresh sequence goes undetected. See Watchdog Operation with 8-bit access for guidelines related to 8-bit accesses to the refresh register.

28.4.4 Windowed mode of operation

In this mode of operation, a restriction is placed on the point in time within the time-out period at which the watchdog can be refreshed. The refresh is considered valid only when the watchdog timer increments beyond a certain count as specified by the watchdog window register. This is known as refreshing the watchdog within a window of the total time-out period. If a refresh is attempted before the timer reaches the window value, the watchdog generates a reset, or interrupt-then-reset if enabled. If there is no refresh at all, the watchdog times out and generates a reset or interrupt-then-reset if enabled.

28.4.5 Watchdog disabled mode of operation

When the watchdog is disabled through the WDOG_EN bit in the watchdog status and control register, the watchdog timer is reset to zero and is disabled from counting until you enable it or it is enabled again by the system reset. In this mode, the watchdog timer cannot be refreshed–there is no requirement to do so while the timer is disabled. However, the watchdog still generates a reset, or interrupt-then-reset if enabled, on a non-time-out exception. See Generated Resets and Interrupts. You need to unlock the watchdog before enabling it. A system reset brings the watchdog out of the disabled mode.

28.4.6 Low-power modes of operation

The low-power modes of operation of the watchdog are described in the following table:

Table 28-3. Low-power modes of operation

Mode	Behavior
Wait	If the WDOG is enabled (WAIT_EN = 1), it can run on bus clock or low-power oscillator clock (CLK_SRC = x) to generate interrupt (IRQ_RST_EN=1) followed by a reset on time-out. After reset the WDOG reset counter increments by one.
Stop	Where the bus clock is gated, the WDOG can run only on low-power oscillator clock (CLK_SRC=0) if it is enabled in stop (STOP_EN=1). In this case, the WDOG runs to time-out twice, and then generates a reset from its backup circuitry. Therefore, if you program the watchdog to time-out after 100 ms and then enter such a stop mode, the reset will occur after 200 ms. Also, in this case, no interrupt will be generated irrespective of the value of IRQ_RST_EN bit. After WDOG reset, the WDOG reset counter will also not increment.
Power-Down	The watchdog is • static in LLS mode • powered off in VLLSx mode

28.4.7 Debug modes of operation

You can program the watchdog to disable in debug modes through DBG_EN in the watchdog control register. This results in the watchdog timer pausing for the duration of the mode. Register read/writes are still allowed, which means that operations like refresh, unlock, and so on are allowed. Upon exit from the mode, the timer resumes its operation from the point of pausing.

The entry of the system into the debug mode does not excuse it from compulsorily configuring the watchdog in the WCT time after unlock, unless the system bus clock is gated off, in which case the internal state machine pauses too. Failing to do so still results in a reset, or interrupt-then-reset, if enabled, to the system. Also, all of the exception conditions that result in a reset to the system, as described in Generated Resets and Interrupts, are still valid in this mode. So, if an exception condition occurs and the system bus clock is on, a reset occurs, or interrupt-then-reset, if enabled.

The entry into Debug mode within WCT after reset is treated differently. The WDOG timer is kept reset to zero and there is no need to unlock and configure it within WCT. You must not try to refresh or unlock the WDOG in this state or unknown behavior may result. Upon exit from this mode, the WDOG timer restarts and the WDOG has to be unlocked and configured within WCT.

28.5 Testing the watchdog

For IEC 60730 and other safety standards, the expectation is that anything that monitors a safety function must be tested, and this test is required to be fault tolerant. To test the watchdog, its main timer and its associated compare and reset logic must be tested. To

this end, two tests are implemented for the watchdog, as described in Quick Test and Byte Test. A control bit is provided to put the watchdog into functional test mode. There is also an overriding test-disable control bit which allows the functional test mode to be disabled permanently. After it is set, this test-disable bit can only be cleared by a reset.

These two tests achieve the overall aim of testing the counter functioning and the compare and reset logic.

Note

Do not enable the watchdog interrupt during these tests. If required, you must ensure that the effective time-out value is greater than WCT time. See Generated Resets and Interrupts for more details.

To run a particular test:

1. Select either quick test or byte test..
2. Set a certain test mode bit to put the watchdog in the functional test mode. Setting this bit automatically switches the watchdog timer to a fast clock source. The switching of the clock source is done to achieve a faster time-out and hence a faster test.

In a successful test, the timer times out after reaching the programmed time-out value and generates a system reset.

Note

After emerging from a reset due to a watchdog test, unlock and configure the watchdog. The refresh and unlock operations and interrupt are not automatically disabled in the test mode.

28.5.1 Quick test

In this test, the time-out value of watchdog timer is programmed to a very low value to achieve quick time-out. The only difference between the quick test and the normal mode of the watchdog is that TESTWDOG is set for the quick test. This allows for a faster test of the watchdog reset mechanism.

28.5.2 Byte test

The byte test is a more thorough a test of the watchdog timer. In this test, the timer is split up into its constituent byte-wide stages that are run independently and tested for time-out against the corresponding byte of the time-out value register. The following figure explains the splitting concept:

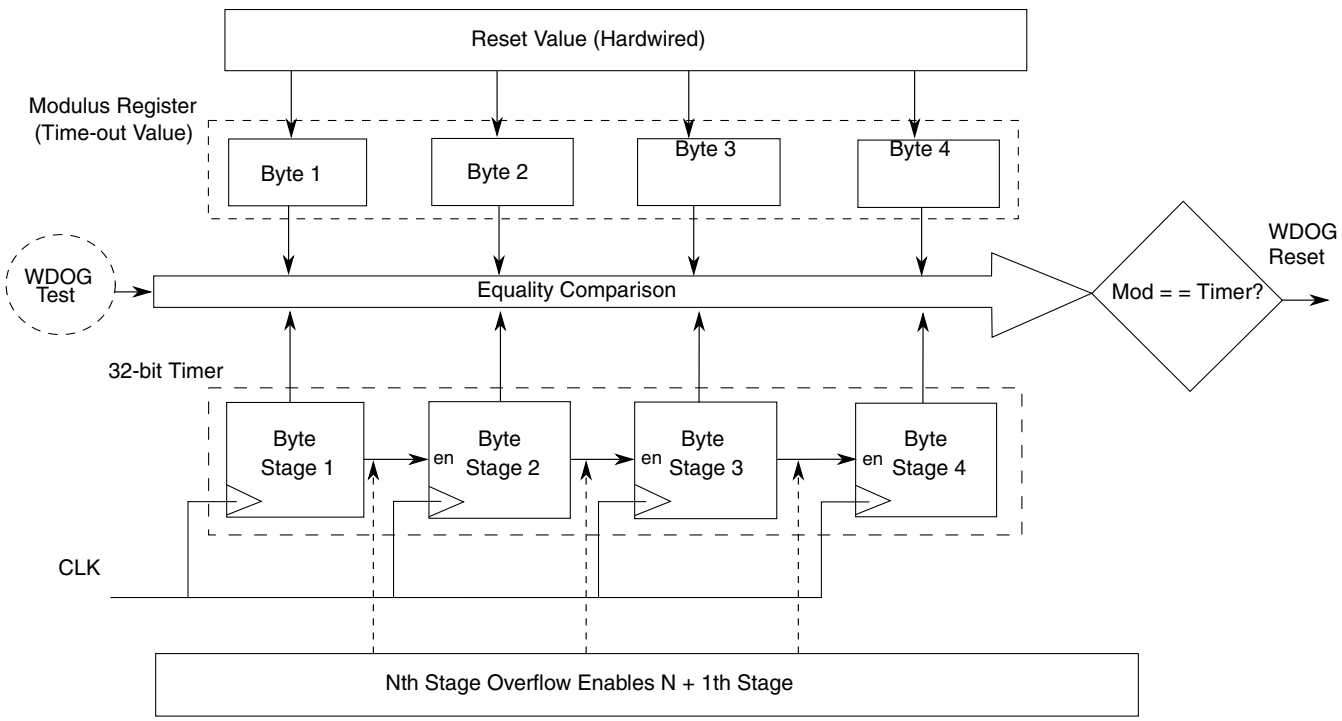


Figure 28-2. Watchdog timer byte splitting

Each stage is an 8-bit synchronous counter followed by combinational logic that generates an overflow signal. The overflow signal acts as an enable to the N + 1th stage.

In the test mode, when an individual byte, N, is tested, byte N – 1 is loaded forcefully with 0xFF, and both these bytes are allowed to run off the clock source. By doing so, the overflow signal from stage N – 1 is generated immediately, enabling counter stage N. The Nth stage runs and compares with the Nth byte of the time-out value register. In this way, the byte N is also tested along with the link between it and the preceding stage. No other stages, N – 2, N – 3... and N + 1, N + 2... are enabled for the test on byte N. These disabled stages, except the most significant stage of the counter, are loaded with a value of 0xFF.

28.6 Backup reset generator

The backup reset generator generates the final reset which goes out to the system. It has a backup mechanism which ensures that in case the bus clock stops and prevents the main state machine from generating a reset exception/interrupt, the watchdog timer's time-out is separately routed out as a reset to the system. Two successive timer time-outs without an intervening system reset result in the backup reset generator routing out the time-out signal as a reset to the system.

28.7 Generated resets and interrupts

The watchdog generates a reset in the following events, also referred to as exceptions:

- A watchdog time-out
- Failure to unlock the watchdog within WCT time after system reset deassertion
- No update of the control and configuration registers within the WCT window after unlocking. At least one of the following registers must be written to within the WCT window to avoid reset:
  - WDOG_ST_CTRL_H, WDOG_ST_CTRL_L
  - WDOG_TO_VAL_H, WDOG_TO_VAL_L
  - WDOG_WIN_H, WDOG_WIN_L
  - WDOG_PRESCALER
- A value other than the unlock sequence or the refresh sequence is written to the unlock and/or refresh registers, respectively.
- A gap of more than 20 bus cycles exists between the writes of two values of the unlock sequence.
- A gap of more than 20 bus cycles exists between the writes of two values of the refresh sequence.

The watchdog can also generate an interrupt. If IRQ_RST_EN is set, then on the above mentioned events WDOG_ST_CTRL_L[INT_FLG] is set, generating an interrupt. A watchdog reset is also generated WCT time later to ensure the watchdog is fault tolerant. The interrupt can be cleared by writing 1 to INT_FLG.

The gap of WCT between interrupt and reset means that the WDOG time-out value must be greater than WCT. Otherwise, if the interrupt was generated due to a time-out, a second consecutive time-out will occur in that WCT gap. This will trigger the backup reset generator to generate a reset to the system, prematurely ending the interrupt service routine execution. Also, jobs such as counting the number of watchdog resets would not be done.

28.8 Memory map and register definition

This section consists of the memory map and register descriptions.

WDOG memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4005_2000	Watchdog Status and Control Register High (WDOG_STCTRLH)	16	R/W	01D3h	28.8.1/671
4005_2002	Watchdog Status and Control Register Low (WDOG_STCTRLL)	16	R/W	0001h	28.8.2/672
4005_2004	Watchdog Time-out Value Register High (WDOG_TOVALH)	16	R/W	004Ch	28.8.3/673
4005_2006	Watchdog Time-out Value Register Low (WDOG_TOVALL)	16	R/W	4B4Ch	28.8.4/673
4005_2008	Watchdog Window Register High (WDOG_WINH)	16	R/W	0000h	28.8.5/674
4005_200A	Watchdog Window Register Low (WDOG_WINL)	16	R/W	0010h	28.8.6/674
4005_200C	Watchdog Refresh register (WDOG_REFRESH)	16	R/W	B480h	28.8.7/675
4005_200E	Watchdog Unlock register (WDOG_UNLOCK)	16	R/W	D928h	28.8.8/675
4005_2010	Watchdog Timer Output Register High (WDOG_TMROUTH)	16	R/W	0000h	28.8.9/675
4005_2012	Watchdog Timer Output Register Low (WDOG_TMROUTL)	16	R/W	0000h	28.8.10/ 676
4005_2014	Watchdog Reset Count register (WDOG_RSTCNT)	16	R/W	0000h	28.8.11/ 676
4005_2016	Watchdog Prescaler register (WDOG_PRESC)	16	R/W	0400h	28.8.12/ 676

28.8.1 Watchdog Status and Control Register High (WDOG_STCTRLH)

Address: 4005_2000h base + 0h offset = 4005_2000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	DISTESTWDOG	BYTESEL[1:0]		TESTSEL	TESTWDOG	0	Reserved	WAITEN	STOPEN	DBGEN	ALLOWUPDATE	WINEN	IRQRSTEN	CLKSRC	WDOGEN
Write																
Reset	0	0	0	0	0	0	0	1	1	1	0	1	0	0	1	1

WDOG_STCTRLH field descriptions

Field	Description
15 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
14 DISTESTWDOG	Allows the WDOG's functional test mode to be disabled permanently. After it is set, it can only be cleared by a reset. It cannot be unlocked for editing after it is set. 0 WDOG functional test mode is not disabled. 1 WDOG functional test mode is disabled permanently until reset.
13–12 BYTESEL[1:0]	This 2-bit field selects the byte to be tested when the watchdog is in the byte test mode. 00 Byte 0 selected 01 Byte 1 selected 10 Byte 2 selected 11 Byte 3 selected
11 TESTSEL	Effective only if TESTWDOG is set. Selects the test to be run on the watchdog timer. 0 Quick test. The timer runs in normal operation. You can load a small time-out value to do a quick test. 1 Byte test. Puts the timer in the byte test mode where individual bytes of the timer are enabled for operation and are compared for time-out against the corresponding byte of the programmed time-out value. Select the byte through BYTESEL[1:0] for testing.
10 TESTWDOG	Puts the watchdog in the functional test mode. In this mode, the watchdog timer and the associated compare and reset generation logic is tested for correct operation. The clock for the timer is switched from the main watchdog clock to the fast clock input for watchdog functional test. The TESTSEL bit selects the test to be run.
9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 Reserved	This field is reserved.
7 WAITEN	Enables or disables WDOG in Wait mode. 0 WDOG is disabled in CPU Wait mode. 1 WDOG is enabled in CPU Wait mode.
6 STOPEN	Enables or disables WDOG in Stop mode.

Table continues on the next page...

WDOG_STCTRLH field descriptions (continued)

Field	Description
	0 WDOG is disabled in CPU Stop mode. 1 WDOG is enabled in CPU Stop mode.
5 DBGEN	Enables or disables WDOG in Debug mode. 0 WDOG is disabled in CPU Debug mode. 1 WDOG is enabled in CPU Debug mode.
4 ALLOWUPDATE	Enables updates to watchdog write-once registers, after the reset-triggered initial configuration window (WCT) closes, through unlock sequence. 0 No further updates allowed to WDOG write-once registers. 1 WDOG write-once registers can be unlocked for updating.
3 WINEN	Enables Windowing mode. 0 Windowing mode is disabled. 1 Windowing mode is enabled.
2 IRQRSTEN	Used to enable the debug breadcrumbs feature. A change in this bit is updated immediately, as opposed to updating after WCT. 0 WDOG time-out generates reset only. 1 WDOG time-out initially generates an interrupt. After WCT, it generates a reset.
1 CLKSRC	Selects clock source for the WDOG timer and other internal timing operations. 0 WDOG clock sourced from LPO . 1 WDOG clock sourced from alternate clock source.
0 WDOGEN	Enables or disables the WDOG's operation. In the disabled state, the watchdog timer is kept in the reset state, but the other exception conditions can still trigger a reset/interrupt. A change in the value of this bit must be held for more than one WDOG_CLK cycle for the WDOG to be enabled or disabled. 0 WDOG is disabled. 1 WDOG is enabled.

28.8.2 Watchdog Status and Control Register Low (WDOG_STCTRLL)

Address: 4005_2000h base + 2h offset = 4005_2002h

Bit	15	14	13	12	11	10	9	8
Read Write	INTFLG	Reserved						
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	1

WDOG_STCTRLL field descriptions

Field	Description
15 INTFLG	Interrupt flag. It is set when an exception occurs. IRQRSTEN = 1 is a precondition to set this flag. INTFLG = 1 results in an interrupt being issued followed by a reset, WCT later. The interrupt can be cleared by writing 1 to this bit. It also gets cleared on a system reset.
Reserved	This field is reserved. **NOTE:** Do not modify this field value.

28.8.3 Watchdog Time-out Value Register High (WDOG_TOVALH)

Address: 4005_2000h base + 4h offset = 4005_2004h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	TOVALHIGH															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0

WDOG_TOVALH field descriptions

Field	Description
TOVALHIGH	Defines the upper 16 bits of the 32-bit time-out value for the watchdog timer. It is defined in terms of cycles of the watchdog clock.

28.8.4 Watchdog Time-out Value Register Low (WDOG_TOVALL)

The time-out value of the watchdog must be set to a minimum of four watchdog clock cycles. This is to take into account the delay in new settings taking effect in the watchdog clock domain.

Address: 4005_2000h base + 6h offset = 4005_2006h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	TOVALLOW															
Reset	0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	0

WDOG_TOVALL field descriptions

Field	Description
TOVALLOW	Defines the lower 16 bits of the 32-bit time-out value for the watchdog timer. It is defined in terms of cycles of the watchdog clock.

28.8.5 Watchdog Window Register High (WDOG_WINH)

NOTE

You must set the Window Register value lower than the Time-out Value Register.

Address: 4005_2000h base + 8h offset = 4005_2008h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	WINHIGH															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WDOG_WINH field descriptions

Field	Description
WINHIGH	Defines the upper 16 bits of the 32-bit window for the windowed mode of operation of the watchdog. It is defined in terms of cycles of the watchdog clock. In this mode, the watchdog can be refreshed only when the timer has reached a value greater than or equal to this window length. A refresh outside this window resets the system or if IRQRSTEN is set, it interrupts and then resets the system.

28.8.6 Watchdog Window Register Low (WDOG_WINL)

NOTE

You must set the Window Register value lower than the Time-out Value Register.

Address: 4005_2000h base + Ah offset = 4005_200Ah

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	WINLOW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

WDOG_WINL field descriptions

Field	Description
WINLOW	Defines the lower 16 bits of the 32-bit window for the windowed mode of operation of the watchdog. It is defined in terms of cycles of the pre-scaled watchdog clock. In this mode, the watchdog can be refreshed only when the timer reaches a value greater than or equal to this window length value. A refresh outside of this window resets the system or if IRQRSTEN is set, it interrupts and then resets the system.

28.8.7 Watchdog Refresh register (WDOG_REFRESH)

Address: 4005_2000h base + Ch offset = 4005_200Ch

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	WDOGREFRESH															
Reset	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0

WDOG_REFRESH field descriptions

Field	Description
WDOGREFRESH	Watchdog refresh register. A sequence of 0xA602 followed by 0xB480 within 20 bus clock cycles written to this register refreshes the WDOG and prevents it from resetting the system. Writing a value other than the above mentioned sequence or if the sequence is longer than 20 bus cycles, resets the system, or if IRQRSTEN is set, it interrupts and then resets the system.

28.8.8 Watchdog Unlock register (WDOG_UNLOCK)

Address: 4005_2000h base + Eh offset = 4005_200Eh

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	WDOGUNLOCK															
Reset	1	1	0	1	1	0	0	1	0	0	1	0	1	0	0	0

WDOG_UNLOCK field descriptions

Field	Description
WDOGUNLOCK	Writing the unlock sequence values to this register to makes the watchdog write-once registers writable again. The required unlock sequence is 0xC520 followed by 0xD928 within 20 bus clock cycles. A valid unlock sequence opens a window equal in length to the WCT within which you can update the registers. Writing a value other than the above mentioned sequence or if the sequence is longer than 20 bus cycles, resets the system or if IRQRSTEN is set, it interrupts and then resets the system. The unlock sequence is effective only if ALLOWUPDATE is set.

28.8.9 Watchdog Timer Output Register High (WDOG_TMROUTH)

Address: 4005_2000h base + 10h offset = 4005_2010h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	TIMEROUTHIGH															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WDOG_TMROUTH field descriptions

Field	Description
TIMEROUTHIGH	Shows the value of the upper 16 bits of the watchdog timer.

28.8.10 Watchdog Timer Output Register Low (WDOG_TMROUTL)

During Stop mode, the WDOG_TIMER_OUT will be caught at the pre-stop value of the watchdog timer. After exiting Stop mode, a maximum delay of 1 WDOG_CLK cycle + 3 bus clock cycles will occur before the WDOG_TIMER_OUT starts following the watchdog timer.

Address: 4005_2000h base + 12h offset = 4005_2012h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	TIMEROUTLOW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WDOG_TMROUTL field descriptions

Field	Description
TIMEROUTLOW	Shows the value of the lower 16 bits of the watchdog timer.

28.8.11 Watchdog Reset Count register (WDOG_RSTCNT)

Address: 4005_2000h base + 14h offset = 4005_2014h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	RSTCNT															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WDOG_RSTCNT field descriptions

Field	Description
RSTCNT	Counts the number of times the watchdog resets the system. This register is reset only on a POR. Writing 1 to the bit to be cleared enables you to clear the contents of this register.

28.8.12 Watchdog Prescaler register (WDOG_PRESC)

Address: 4005_2000h base + 16h offset = 4005_2016h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0					PRESCVAL			0							
Write																
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

WDOG_PRESC field descriptions

Field	Description
15–11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10–8 PRESCVAL	3-bit prescaler for the watchdog clock source. A value of zero indicates no division of the input WDOG clock. The watchdog clock is divided by (PRESCVAL + 1) to provide the prescaled WDOG_CLK.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

28.9 Watchdog operation with 8-bit access

28.9.1 General guideline

When performing 8-bit accesses to the watchdog's 16-bit registers where the intention is to access both the bytes of a register, place the two 8-bit accesses one after the other in your code.

28.9.2 Refresh and unlock operations with 8-bit access

One exception condition that generates a reset to the system is the write of any value other than those required for a legal refresh/update sequence to the respective refresh and unlock registers.

For an 8-bit access to these registers, writing a correct value requires at least two bus clock cycles, resulting in an invalid value in the registers for one cycle. Therefore, the system is reset even if the intention is to write a correct value to the refresh/unlock register. Keeping this in mind, the exception condition for 8-bit accesses is slightly modified.

Whereas the match for a correct value for a refresh/unlock sequence is as according to the original definition, the match for an incorrect value is done byte-wise on the refresh/unlock rather than for the whole 16-bit value. This means that if the high byte of the refresh/unlock register contains any value other than high bytes of the two values that make up the sequence, it is treated as an exception condition, leading to a reset or interrupt-then-reset. The same holds true for the lower byte of the refresh or unlock register. Take the refresh operation that expects a write of 0xA602 followed by 0xB480 to the refresh register, as an example.

Table 28-4. Refresh for 8-bit access

	WDOG_REFRESH[15:8]	WDOG_REFRESH[7:0]	Sequence value1 or value2 match	Mismatch exception
Current Value	0xB4	0x80	Value2 match	No
Write 1	0xB4	0x02	No match	No
Write 2	0xA6	0x02	Value1 match	No
Write 3	0xB4	0x02	No match	No
Write 4	0xB4	0x80	Value2 match. Sequence complete.	No
Write 5	0x02	0x80	No match	Yes

As shown in the preceding table, the refresh register holds its reset value initially. Thereafter, two 8-bit accesses are performed on the register to write the first value of the refresh sequence. No mismatch exception is registered on the intermediate write, Write1. The sequence is completed by performing two more 8-bit accesses, writing in the second value of the sequence for a successful refresh. It must be noted that the match of value2 takes place only when the complete 16-bit value is correctly written, write4. Hence, the requirement of writing value2 of the sequence within 20 bus clock cycles of value1 is checked by measuring the gap between write2 and write4.

It is reiterated that the condition for matching values 1 and 2 of the refresh or unlock sequence remains unchanged. The difference for 8-bit accesses is that the criterion for detecting a mismatch is less strict. Any 16-bit access still needs to adhere to the original guidelines, mentioned in the sections Refreshing the Watchdog.

28.10 Restrictions on watchdog operation

This section mentions some exceptions to the watchdog operation that may not be apparent to you.

- Restriction on unlock/refresh operations—In the period between the closure of the WCT window after unlock and the actual reload of the watchdog timer, unlock and refresh operations need not be attempted.
- The update and reload of the watchdog timer happens two to three watchdog clocks after WCT window closes, following a successful configuration on unlock.
- Clock Switching Delay—The watchdog uses glitch-free multiplexers at two places – one to choose between the LPO oscillator input and alternate clock input, and the other to choose between the watchdog functional clock and fast clock input for

watchdog functional test. A maximum time period of ~2 clock A cycles plus ~2 clock B cycles elapses from the time a switch is requested to the occurrence of the actual clock switch, where clock A and B are the two input clocks to the clock mux.

- For the windowed mode, there is a two to three bus clock latency between the watchdog counter going past the window value and the same registering in the bus clock domain.
- For proper operation of the watchdog, the watchdog clock must be at least five times slower than the system bus clock at all times. An exception is when the watchdog clock is synchronous to the bus clock wherein the watchdog clock can be as fast as the bus clock.
- WCT must be equivalent to at least three watchdog clock cycles. If not ensured, this means that even after the close of the WCT window, you have to wait for the synchronized system reset to deassert in the watchdog clock domain, before expecting the configuration updates to take effect.
- The time-out value of the watchdog should be set to a minimum of four watchdog clock cycles. This is to take into account the delay in new settings taking effect in the watchdog clock domain.
- You must take care not only to refresh the watchdog within the watchdog timer's actual time-out period, but also provide enough allowance for the time it takes for the refresh sequence to be detected by the watchdog timer, on the watchdog clock.
- Updates cannot be made in the bus clock cycle immediately following the write of the unlock sequence, but one bus clock cycle later.
- It should be ensured that the time-out value for the watchdog is always greater than 2xWCT time + 20 bus clock cycles.
- An attempted refresh operation, in between the two writes of the unlock sequence and in the WCT time following a successful unlock, will go undetected.
- Trying to unlock the watchdog within the WCT time after an initial unlock has no effect.
- The refresh and unlock operations and interrupt are not automatically disabled in the watchdog functional test mode.
- After emerging from a reset due to a watchdog functional test, you are still expected to go through the mandatory steps of unlocking and configuring the watchdog. The watchdog continues to be in its functional test mode and therefore you should pull the watchdog out of the functional test mode within WCT time of reset.

- After emerging from a reset due to a watchdog functional test, you still need to go through the mandatory steps of unlocking and configuring the watchdog.
- You must ensure that both the clock inputs to the glitchless clock multiplexers are alive during the switching of clocks. Failure to do so results in a loss of clock at their outputs.
- There is a gap of two to three watchdog clock cycles from the point that stop mode is entered to the watchdog timer actually pausing, due to synchronization. The same holds true for an exit from the stop mode, this time resulting in a two to three watchdog clock cycle delay in the timer restarting. In case the duration of the stop mode is less than one watchdog clock cycle, the watchdog timer is not guaranteed to pause.
- Consider the case when the first refresh value is written, following which the system enters stop mode with system bus clk still on. If the second refresh value is not written within 20 bus cycles of the first value, the system is reset, or interrupt-then-reset if enabled.

Chapter 29
Multipurpose Clock Generator (MCG)

29.1 Chip-specific MCG information

29.1.1 MCG oscillator clock input options

The MCG has multiple oscillator input clock sources. Within the context of the MCG these are all referred to as the external reference clock and selection is determined by MCG_C7[OSCSEL] bitfield. The following table shows the chip-specific clock assignments for this bitfield.

Table 29-1. MCG Oscillator Reference Options

MCG_C7[OSCSEL]	MCG defined selection	Chip clock
00	OSCCLK0 - System Oscillator	OSCCLK - System oscillator output. Derived from external crystal circuit or directly from EXTAL.
01	OSC2/RTC Oscillator	RTC 32kHz oscillator output. RTC clock is derived from external crystal circuit associated with RTC.
10	OSCCLK1 - Oscillator	IRC48MCLK. Derived from internal 48 MHz oscillator.
11	Reserved	—

See Clock Distribution for more details on these clocks.

29.2 Introduction

The multipurpose clock generator (MCG) module provides several clock source choices for the MCU.

The module contains a frequency-locked loop (FLL) and a phase-locked loop (PLL). The FLL is controllable by either an internal or an external reference clock. The PLL is controllable by the external reference clock. The module can select either an FLL or PLL output clock, or a reference clock (internal or external) as a source for the MCU system clock. The MCG operates in conjuction with a crystal oscillator, which allows an external crystal, ceramic resonator, or another external clock source to produce the external reference clock.

29.2.1 Features

Key features of the MCG module are:

- Frequency-locked loop (FLL):
  - Digitally-controlled oscillator (DCO)
  - DCO frequency range is programmable for up to four different frequency ranges.
  - Option to program and maximize DCO output frequency for a low frequency external reference clock source.
  - Option to prevent FLL from resetting its current locked frequency when switching clock modes if FLL reference frequency is not changed.
  - Internal or external reference clock can be used as the FLL source.
  - Can be used as a clock source for other on-chip peripherals.
- Phase-locked loop (PLL):
  - Voltage-controlled oscillator (VCO)
  - External reference clock is used as the PLL source.
  - Modulo VCO frequency divider
  - Phase/Frequency detector
  - Integrated loop filter
  - Can be used as a clock source for other on-chip peripherals.
- Internal reference clock generator:
  - Slow clock with nine trim bits for accuracy
  - Fast clock with four trim bits

    - Can be used as source clock for the FLL. In FEI mode, only the slow Internal Reference Clock (IRC) can be used as the FLL source.
    - Either the slow or the fast clock can be selected as the clock source for the MCU.
    - Can be used as a clock source for other on-chip peripherals.
- Control signals for the MCG external reference low power oscillator clock generators are provided:
    - HGO, RANGE, EREFS
- External clock from the Crystal Oscillator :
    - Can be used as a source for the FLL and/or the PLL.
    - Can be selected as the clock source for the MCU.
- External clock from the Real Time Counter (RTC):
    - Can only be used as a source for the FLL.
    - Can be selected as the clock source for the MCU.
- External clock monitor with reset and interrupt request capability to check for external clock failure when running in FBE, PEE, BLPE, or FEE modes
- Lock detector with interrupt request capability for use with the PLL
- Internal Reference Clocks Auto Trim Machine (ATM) capability using an external clock as a reference
- Reference dividers for both the FLL and the PLL are provided
- Reference dividers for the Fast Internal Reference Clock are provided
- MCG PLL Clock (MCGPLLCLK) is provided as a clock source for other on-chip peripherals
- MCG FLL Clock (MCGFLLCLK) is provided as a clock source for other on-chip peripherals
- MCG Fixed Frequency Clock (MCGFFCLK) is provided as a clock source for other on-chip peripherals
- MCG Internal Reference Clock (MCGIRCLK) is provided as a clock source for other on-chip peripherals

This figure presents the block diagram of the MCG module.

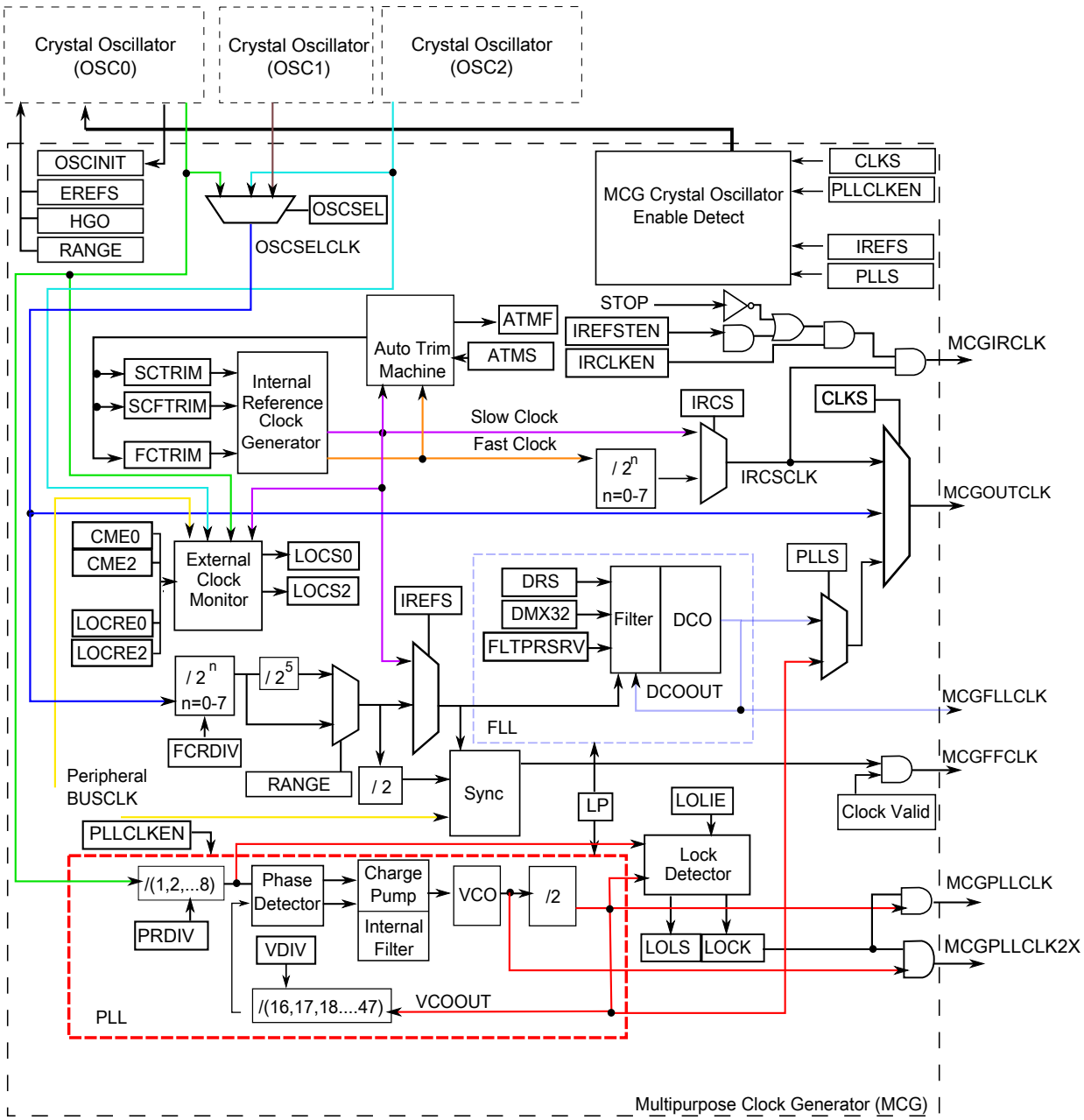


Figure 29-1. Multipurpose Clock Generator (MCG) block diagram

29.2.2 Modes of Operation

The MCG has the following modes of operation: FEI, FEE, FBI, FBE, PBE, PEE, BLPI, BLPE, and Stop. For details, see MCG modes of operation.

29.3 External Signal Description

There are no MCG signals that connect off chip.

29.4 Memory Map/Register Definition

This section includes the memory map and register definition.

The MCG registers can only be written when in supervisor mode. Write accesses when in user mode will result in a bus error. Read accesses may be performed in both supervisor and user mode.

MCG memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4006_4000	MCG Control 1 Register (MCG_C1)	8	R/W	04h	29.4.1/686
4006_4001	MCG Control 2 Register (MCG_C2)	8	R/W	80h	29.4.2/687
4006_4002	MCG Control 3 Register (MCG_C3)	8	R/W	Undefined	29.4.3/688
4006_4003	MCG Control 4 Register (MCG_C4)	8	R/W	Undefined	29.4.4/689
4006_4004	MCG Control 5 Register (MCG_C5)	8	R/W	00h	29.4.5/690
4006_4005	MCG Control 6 Register (MCG_C6)	8	R/W	00h	29.4.6/691
4006_4006	MCG Status Register (MCG_S)	8	R	10h	29.4.7/693
4006_4008	MCG Status and Control Register (MCG_SC)	8	R/W	02h	29.4.8/694
4006_400A	MCG Auto Trim Compare Value High Register (MCG_ATCVH)	8	R/W	00h	29.4.9/696
4006_400B	MCG Auto Trim Compare Value Low Register (MCG_ATCVL)	8	R/W	00h	29.4.10/ 696
4006_400C	MCG Control 7 Register (MCG_C7)	8	R/W	00h	29.4.11/ 696
4006_400D	MCG Control 8 Register (MCG_C8)	8	R/W	80h	29.4.12/ 697
4006_4011	MCG Control 12 Register (MCG_C12)	8	R/W	00h	29.4.13/ 698
4006_4012	MCG Status 2 Register (MCG_S2)	8	R/W	00h	29.4.13/ 698
4006_4013	MCG Test 3 Register (MCG_T3)	8	R/W	00h	29.4.13/ 699

29.4.1 MCG Control 1 Register (MCG_C1)

Address: 4006_4000h base + 0h offset = 4006_4000h

Bit	7	6	5	4	3	2	1	0
Read Write	CLKS		FRDIV			IREFS	IRCLKEN	IREFSTEN
Reset	0	0	0	0	0	1	0	0

MCG_C1 field descriptions

Field	Description
7–6 CLKS	Clock Source Select Selects the clock source for MCGOUTCLK . 00 Encoding 0 — Output of FLL or PLL is selected (depends on PLLS control bit). 01 Encoding 1 — Internal reference clock is selected. 10 Encoding 2 — External reference clock is selected. 11 Encoding 3 — Reserved.
5–3 FRDIV	FLL External Reference Divider Selects the amount to divide down the external reference clock for the FLL. The resulting frequency must be in the range 31.25 kHz to 39.0625 kHz (This is required when FLL/DCO is the clock source for MCGOUTCLK . In FBE mode, it is not required to meet this range, but it is recommended in the cases when trying to enter a FLL mode from FBE). 000 If RANGE = 0 or OSCSEL=1 , Divide Factor is 1; for all other RANGE values, Divide Factor is 32. 001 If RANGE = 0 or OSCSEL=1 , Divide Factor is 2; for all other RANGE values, Divide Factor is 64. 010 If RANGE = 0 or OSCSEL=1 , Divide Factor is 4; for all other RANGE values, Divide Factor is 128. 011 If RANGE = 0 or OSCSEL=1 , Divide Factor is 8; for all other RANGE values, Divide Factor is 256. 100 If RANGE = 0 or OSCSEL=1 , Divide Factor is 16; for all other RANGE values, Divide Factor is 512. 101 If RANGE = 0 or OSCSEL=1 , Divide Factor is 32; for all other RANGE values, Divide Factor is 1024. 110 If RANGE = 0 or OSCSEL=1 , Divide Factor is 64; for all other RANGE values, Divide Factor is 1280 . 111 If RANGE = 0 or OSCSEL=1 , Divide Factor is 128; for all other RANGE values, Divide Factor is 1536 .
2 IREFS	Internal Reference Select Selects the reference clock source for the FLL. 0 External reference clock is selected. 1 The slow internal reference clock is selected.
1 IRCLKEN	Internal Reference Clock Enable Enables the internal reference clock for use as MCGIRCLK. 0 MCGIRCLK inactive. 1 MCGIRCLK active.
0 IREFSTEN	Internal Reference Stop Enable Controls whether or not the internal reference clock remains enabled when the MCG enters Stop mode.

Table continues on the next page...

MCG_C1 field descriptions (continued)

Field	Description
	0 Internal reference clock is disabled in Stop mode. 1 Internal reference clock is enabled in Stop mode if IRCLKEN is set or if MCG is in FEI, FBI, or BLPI modes before entering Stop mode.

29.4.2 MCG Control 2 Register (MCG_C2)

Address: 4006_4000h base + 1h offset = 4006_4001h

Bit	7	6	5	4	3	2	1	0
Read Write	LOCRE0	FCFTRIM	RANGE		HGO	EREFS	LP	IRCS
Reset	1	0	0	0	0	0	0	0

MCG_C2 field descriptions

Field	Description
7 LOCRE0	Loss of Clock Reset Enable Determines whether an interrupt or a reset request is made following a loss of OSC0 external reference clock. The LOCRE0 only has an affect when CME0 is set. 0 Interrupt request is generated on a loss of OSC0 external reference clock. 1 Generate a reset request on a loss of OSC0 external reference clock.
6 FCFTRIM	Fast Internal Reference Clock Fine Trim FCFTRIM controls the smallest adjustment of the fast internal reference clock frequency. Setting FCFTRIM increases the period and clearing FCFTRIM decreases the period by the smallest amount possible. If an FCFTRIM value stored in nonvolatile memory is to be used, it is your responsibility to copy that value from the nonvolatile memory location to this bit.
5–4 RANGE	Frequency Range Select Selects the frequency range for the crystal oscillator or external clock source. See the Oscillator (OSC) chapter for more details and the device data sheet for the frequency ranges used. 00 Encoding 0 — Low frequency range selected for the crystal oscillator . 01 Encoding 1 — High frequency range selected for the crystal oscillator . 1X Encoding 2 — Very high frequency range selected for the crystal oscillator .
3 HGO	High Gain Oscillator Select Controls the crystal oscillator mode of operation. See the Oscillator (OSC) chapter for more details. 0 Configure crystal oscillator for low-power operation. 1 Configure crystal oscillator for high-gain operation.
2 EREFS	External Reference Select Selects the source for the external reference clock. See the Oscillator (OSC) chapter for more details. 0 External reference clock requested. 1 Oscillator requested.

Table continues on the next page...

MCG_C2 field descriptions (continued)

Field	Description
1 LP	Low Power Select Controls whether the FLL or PLL is disabled in BLPI and BLPE modes. In FBE or PBE modes, setting this bit to 1 will transition the MCG into BLPE mode; in FBI mode, setting this bit to 1 will transition the MCG into BLPI mode. In any other MCG mode, LP bit has no affect. 0 FLL or PLL is not disabled in bypass modes. 1 FLL or PLL is disabled in bypass modes (lower power)
0 IRCS	Internal Reference Clock Select Selects between the fast or slow internal reference clock source. 0 Slow internal reference clock selected. 1 Fast internal reference clock selected.

29.4.3 MCG Control 3 Register (MCG_C3)

Address: 4006_4000h base + 2h offset = 4006_4002h

Bit	7	6	5	4	3	2	1	0
Read Write	SCTRIM							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

MCG_C3 field descriptions

Field	Description
SCTRIM	Slow Internal Reference Clock Trim Setting SCTRIM [1] controls the slow internal reference clock frequency by controlling the slow internal reference clock period. The SCTRIM bits are binary weighted, that is, bit 1 adjusts twice as much as bit 0. Increasing the binary value increases the period, and decreasing the value decreases the period. An additional fine trim bit is available in C4 register as the SCFTRIM bit. Upon reset, this value is loaded with a factory trim value. If an SCTRIM value stored in nonvolatile memory is to be used, it is your responsibility to copy that value from the nonvolatile memory location to this register.

1. A value for SCTRIM is loaded during reset from a factory programmed location.

29.4.4 MCG Control 4 Register (MCG_C4)

NOTE

Reset values for DRST and DMX32 bits are 0.

Address: 4006_4000h base + 3h offset = 4006_4003h

Bit	7	6	5	4	3	2	1	0
Read Write	DMX32	DRST_DRS			FCTRIM			SCFTRIM
Reset	0	0	0	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.
- x = Undefined at reset.

MCG_C4 field descriptions

Field	Description
7 DMX32	DCO Maximum Frequency with 32.768 kHz Reference The DMX32 bit controls whether the DCO frequency range is narrowed to its maximum frequency with a 32.768 kHz reference. The following table identifies settings for the DCO frequency range. **NOTE:** The system clocks derived from this source should not exceed their specified maximums.

DRST_DRS	DMX32	Reference Range	FLL Factor	DCO Range
00	0	31.25–39.0625 kHz	640	20–25 MHz
	1	32.768 kHz	732	24 MHz
01	0	31.25–39.0625 kHz	1280	40–50 MHz
	1	32.768 kHz	1464	48 MHz
10	0	31.25–39.0625 kHz	1920	60–75 MHz
	1	32.768 kHz	2197	72 MHz
11	0	31.25–39.0625 kHz	2560	80–100 MHz
	1	32.768 kHz	2929	96 MHz

0 DCO has a default range of 25%.
1 DCO is fine-tuned for maximum frequency with 32.768 kHz reference.

6–5 DRST_DRS	DCO Range Select The DRS bits select the frequency range for the FLL output, DCOOUT. When the LP bit is set, writes to the DRS bits are ignored. The DRST read field indicates the current frequency range for DCOOUT. The DRST field does not update immediately after a write to the DRS field due to internal synchronization between clock domains. See the DCO Frequency Range table for more details. 00 Encoding 0 — Low range (reset default).

Table continues on the next page...

MCG_C4 field descriptions (continued)

Field	Description
	01 Encoding 1 — Mid range. 10 Encoding 2 — Mid-high range. 11 Encoding 3 — High range.
4–1 FCTRIM	Fast Internal Reference Clock Trim Setting FCTRIM [1] controls the fast internal reference clock frequency by controlling the fast internal reference clock period. The FCTRIM bits are binary weighted, that is, bit 1 adjusts twice as much as bit 0. Increasing the binary value increases the period, and decreasing the value decreases the period. If an FCTRIM[3:0] value stored in nonvolatile memory is to be used, it is your responsibility to copy that value from the nonvolatile memory location to this register.
0 SCFTRIM	Slow Internal Reference Clock Fine Trim SCFTRIM [2] controls the smallest adjustment of the slow internal reference clock frequency. Setting SCFTRIM increases the period and clearing SCFTRIM decreases the period by the smallest amount possible. If an SCFTRIM value stored in nonvolatile memory is to be used, it is your responsibility to copy that value from the nonvolatile memory location to this bit.

1. A value for FCTRIM is loaded during reset from a factory programmed location.
2. A value for SCFTRIM is loaded during reset from a factory programmed location .

29.4.5 MCG Control 5 Register (MCG_C5)

Address: 4006_4000h base + 4h offset = 4006_4004h

Bit	7	6	5	4	3	2	1	0
Read	0	PLLCLKEN	PLLSTEN	0		PRDIV		
Write								
Reset	0	0	0	0	0	0	0	0

MCG_C5 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 PLLCLKEN	PLL Clock Enable Enables PLL independent of PLLS and enables the PLL clock for use as MCGPLLCLK. (PRDIV needs to be programmed to the correct divider to generate a PLL reference clock in a valid reference range prior to setting the PLLCLKEN bit). Setting PLLCLKEN will enable the external oscillator if not already enabled. Whenever the PLL is being enabled by means of the PLLCLKEN bit, and the external oscillator is being used as the reference clock, the OSCINIT 0 bit should be checked to make sure it is set. 0 MCGPLLCLK is inactive. 1 MCGPLLCLK is active.
5 PLLSTEN	PLL Stop Enable

Table continues on the next page...

MCG_C5 field descriptions (continued)

Field	Description
	Enables the PLL Clock during Normal Stop (In Low Power Stop mode, the PLL clock gets disabled even if PLLSTEN=1). All other power modes, PLLSTEN bit has no affect and does not enable the PLL Clock to run if it is written to 1. 0 MCGPLLCLK and MCGPLLCLK2X are disabled in any of the Stop modes. 1 MCGPLLCLK and MCGPLLCLK2X are enabled if system is in Normal Stop mode.
4–3 Reserved	Reserved This field is reserved. This read-only field is reserved and always has the value 0.
PRDIV	PLL External Reference Divider Selects the amount to divide down the external reference clock for the PLL0. The resulting frequency must be in the range of 8 MHz to 16 MHz. After the PLL0 is enabled (by setting either PLLCLKEN0 or PLLS), the PRDIV0 value must not be changed when LOCK0 is zero.

Table 29-2. PLL External Reference Divide Factor

PRDIV	Divide Factor
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

29.4.6 MCG Control 6 Register (MCG_C6)

Address: 4006_4000h base + 5h offset = 4006_4005h

Bit	7	6	5	4	3	2	1	0
Read Write	LOLIE0	PLLS	CME0	VDIV				
Reset	0	0	0	0	0	0	0	0

MCG_C6 field descriptions

Field	Description
7 LOLIE0	Loss of Lock Interrrupt Enable Determines if an interrupt request is made following a loss of lock indication. This bit only has an effect when LOLS 0 is set.

Table continues on the next page...

MCG_C6 field descriptions (continued)

Field	Description
	0 No interrupt request is generated on loss of lock. 1 Generate an interrupt request on loss of lock.
6 PLLS	PLL Select Controls whether the PLL or FLL output is selected as the MCG source when CLKS[1:0]=00. If the PLLS bit is cleared and PLLCLKEN 0 is not set, the PLL is disabled in all modes. If the PLLS is set, the FLL is disabled in all modes. 0 FLL is selected. 1 PLL is selected (PRDIV 0 need to be programmed to the correct divider to generate a PLL reference clock in the range of 8–16 MHz prior to setting the PLLS bit).
5 CME0	Clock Monitor Enable Enables the loss of clock monitoring circuit for the OSC0 external reference mux select. The LOCRE0 bit will determine if a interrupt or a reset request is generated following a loss of OSC0 indication. The CME0 bit must only be set to a logic 1 when the MCG is in an operational mode that uses the external clock (FEE, FBE, PEE, PBE, or BLPE) . Whenever the CME0 bit is set to a logic 1, the value of the RANGE0 bits in the C2 register should not be changed. CME0 bit should be set to a logic 0 before the MCG enters any Stop mode. Otherwise, a reset request may occur while in Stop mode. CME0 should also be set to a logic 0 before entering VLPR or VLPW power modes if the MCG is in BLPE mode. 0 External clock monitor is disabled for OSC0. 1 External clock monitor is enabled for OSC0.
VDIV	VCO Divider Selects the amount to divide the VCO output of the PLL. The VDIV bits establish the multiplication factor (M) applied to the reference clock frequency. After the PLL is enabled (by setting either PLLCLKEN or PLLS), the VDIV value must not be changed when LOCK is zero.

Table 29-3. PLL VCO Divide Factor

VDIV	Multiply Factor		VDIV	Multiply Factor		VDIV	Multiply Factor		VDIV	Multiply Factor
00000	16		01000	24		10000	32		11000	40
00001	17		01001	25		10001	33		11001	41
00010	18		01010	26		10010	34		11010	42
00011	19		01011	27		10011	35		11011	43
00100	20		01100	28		10100	36		11100	44
00101	21		01101	29		10101	37		11101	45
00110	22		01110	30		10110	38		11110	46
00111	23		01111	31		10111	39		11111	47

29.4.7 MCG Status Register (MCG_S)

Address: 4006_4000h base + 6h offset = 4006_4006h

Bit	7	6	5	4	3	2	1	0
Read	LOLS0	LOCK0	PLLST	IREFST	CLKST		OSCINIT0	IRCST
Write								
Reset	0	0	0	1	0	0	0	0

MCG_S field descriptions

Field	Description
7 LOLS0	Loss of Lock Status This bit is a sticky bit indicating the lock status for the PLL. LOLS is set if after acquiring lock, the PLL output frequency has fallen outside the lock exit frequency tolerance, D_{unl} . LOLIE determines whether an interrupt request is made when LOLS is set. LOLRE determines whether a reset request is made when LOLS is set. This bit is cleared by reset or by writing a logic 1 to it when set. Writing a logic 0 to this bit has no effect. 0 PLL has not lost lock since LOLS 0 was last cleared. 1 PLL has lost lock since LOLS 0 was last cleared.
6 LOCK0	Lock Status This bit indicates whether the PLL has acquired lock. Lock detection is disabled when not operating in either PBE or PEE mode unless PLLCLKEN=1 and the MCG is not configured in BLPI or BLPE mode. While the PLL clock is locking to the desired frequency, MCGPLLCLK and MCGPLLCLK2X will be gated off until the LOCK bit gets asserted. If the lock status bit is set, changing the value of the PRDIV[2:0] bits in the C5 register or the VDIV[4:0] bits in the C6 register causes the lock status bit to clear and stay cleared until the PLL has reacquired lock. Loss of PLL reference clock will also cause the LOCK bit to clear until PLL has reacquired lock Entry into LLS, VLPS, or regular Stop with PLLSTEN=0 also causes the lock status bit to clear and stay cleared until the Stop mode is exited and the PLL has reacquired lock. Any time the PLL is enabled and the LOCK bit is cleared, the MCGPLLCLK and MCGPLLCLK2X will be gated off until the LOCK bit is asserted again. 0 PLL is currently unlocked. 1 PLL is currently locked.
5 PLLST	PLL Select Status This bit indicates the clock source selected by PLLS . The PLLST bit does not update immediately after a write to the PLLS bit due to internal synchronization between clock domains. 0 Source of PLLS clock is FLL clock. 1 Source of PLLS clock is PLL output clock.
4 IREFST	Internal Reference Status This bit indicates the current source for the FLL reference clock. The IREFST bit does not update immediately after a write to the IREFS bit due to internal synchronization between clock domains. 0 Source of FLL reference clock is the external reference clock. 1 Source of FLL reference clock is the internal reference clock.

Table continues on the next page...

MCG_S field descriptions (continued)

Field	Description
3–2 CLKST	Clock Mode Status These bits indicate the current clock mode. The CLKST bits do not update immediately after a write to the CLKS bits due to internal synchronization between clock domains. 00 Encoding 0 — Output of the FLL is selected (reset default). 01 Encoding 1 — Internal reference clock is selected. 10 Encoding 2 — External reference clock is selected. 11 Encoding 3 — Output of the PLL is selected.
1 OSCINIT0	OSC Initialization This bit, which resets to 0, is set to 1 after the initialization cycles of the crystal oscillator clock have completed. After being set, the bit is cleared to 0 if the OSC is subsequently disabled. See the OSC module's detailed description for more information.
0 IRCST	Internal Reference Clock Status The IRCST bit indicates the current source for the internal reference clock select clock (IRCSCLK). The IRCST bit does not update immediately after a write to the IRCS bit due to internal synchronization between clock domains. The IRCST bit will only be updated if the internal reference clock is enabled, either by the MCG being in a mode that uses the IRC or by setting the C1[IRCLKEN] bit . 0 Source of internal reference clock is the slow clock (32 kHz IRC). 1 Source of internal reference clock is the fast clock (4 MHz IRC).

29.4.8 MCG Status and Control Register (MCG_SC)

Address: 4006_4000h base + 8h offset = 4006_4008h

Bit	7	6	5	4	3	2	1	0
Read	ATME	ATMS	ATMF	FLTPRSRV	FCRDIV			LOCS0
Write			w1c					w1c
Reset	0	0	0	0	0	0	1	0

MCG_SC field descriptions

Field	Description
7 ATME	Automatic Trim Machine Enable Enables the Auto Trim Machine to start automatically trimming the selected Internal Reference Clock. **NOTE:** ATME deasserts after the Auto Trim Machine has completed trimming all trim bits of the IRCS clock selected by the ATMS bit. Writing to C1, C3, C4, and SC registers or entering Stop mode aborts the auto trim operation and clears this bit. 0 Auto Trim Machine disabled. 1 Auto Trim Machine enabled.

Table continues on the next page...

MCG_SC field descriptions (continued)

Field	Description
6 ATMS	Automatic Trim Machine Select Selects the IRCS clock for Auto Trim Test. 0 32 kHz Internal Reference Clock selected. 1 4 MHz Internal Reference Clock selected.
5 ATMF	Automatic Trim Machine Fail Flag Fail flag for the Automatic Trim Machine (ATM). This bit asserts when the Automatic Trim Machine is enabled, ATME=1, and a write to the C1, C3, C4, and SC registers is detected or the MCG enters into any Stop mode. A write to ATMF clears the flag. 0 Automatic Trim Machine completed normally. 1 Automatic Trim Machine failed.
4 FLTPRSRV	FLL Filter Preserve Enable This bit will prevent the FLL filter values from resetting allowing the FLL output frequency to remain the same during clock mode changes where the FLL/DCO output is still valid. (Note: This requires that the FLL reference frequency to remain the same as what it was prior to the new clock mode switch. Otherwise FLL filter and frequency values will change.) 0 FLL filter and FLL frequency will reset on changes to currect clock mode. 1 Fll filter and FLL frequency retain their previous values during new clock mode change.
3–1 FCRDIV	Fast Clock Internal Reference Divider Selects the amount to divide down the fast internal reference clock. The resulting frequency will be in the range 31.25 kHz to 4 MHz (Note: Changing the divider when the Fast IRC is enabled is not supported). 000 Divide Factor is 1 001 Divide Factor is 2. 010 Divide Factor is 4. 011 Divide Factor is 8. 100 Divide Factor is 16 101 Divide Factor is 32 110 Divide Factor is 64 111 Divide Factor is 128.
0 LOCS0	OSC0 Loss of Clock Status The LOCS0 indicates when a loss of OSC0 reference clock has occurred. The LOCS0 bit only has an effect when CME0 is set. This bit is cleared by writing a logic 1 to it when set. 0 Loss of OSC0 has not occurred. 1 Loss of OSC0 has occurred.

29.4.9 MCG Auto Trim Compare Value High Register (MCG_ATCVH)

Address: 4006_4000h base + Ah offset = 4006_400Ah

Bit	7	6	5	4	3	2	1	0
Read Write	ATCVH							
Reset	0	0	0	0	0	0	0	0

MCG_ATCVH field descriptions

Field	Description
ATCVH	ATM Compare Value High Values are used by Auto Trim Machine to compare and adjust Internal Reference trim values during ATM SAR conversion.

29.4.10 MCG Auto Trim Compare Value Low Register (MCG_ATCVL)

Address: 4006_4000h base + Bh offset = 4006_400Bh

Bit	7	6	5	4	3	2	1	0
Read Write	ATCVL							
Reset	0	0	0	0	0	0	0	0

MCG_ATCVL field descriptions

Field	Description
ATCVL	ATM Compare Value Low Values are used by Auto Trim Machine to compare and adjust Internal Reference trim values during ATM SAR conversion.

29.4.11 MCG Control 7 Register (MCG_C7)

Address: 4006_4000h base + Ch offset = 4006_400Ch

Bit	7	6	5	4	3	2	1	0
Read	0		0				OSCSEL	
Write								
Reset	0	0	0	0	0	0	0	0

MCG_C7 field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5–2 Reserved	Reserved This field is reserved. This read-only field is reserved and always has the value 0.
OSCSEL	MCG OSC Clock Select Selects the MCG FLL external reference clock **NOTE:** The OSCSEL field can't be changed during MCG modes (like PBE), when external clock is serving as the clock source for MCG. 00 Selects Oscillator (OSCCLK0). 01 Selects 32 kHz RTC Oscillator. 10 Selects Oscillator (OSCCLK1). 11 RESERVED

29.4.12 MCG Control 8 Register (MCG_C8)

Address: 4006_4000h base + Dh offset = 4006_400Dh

Bit	7	6	5	4	3	2	1	0
Read	LOCRE1	LOLRE	CME1	0				LOCS1
Write								w1c
Reset	1	0	0	0	0	0	0	0

MCG_C8 field descriptions

Field	Description
7 LOCRE1	Loss of Clock Reset Enable Determines if a interrupt or a reset request is made following a loss of RTC external reference clock. The LOCRE1 only has an affect when CME1 is set. 0 Interrupt request is generated on a loss of RTC external reference clock. 1 Generate a reset request on a loss of RTC external reference clock
6 LOLRE	PLL Loss of Lock Reset Enable Determines if an interrupt or a reset request is made following a PLL loss of lock. 0 Interrupt request is generated on a PLL loss of lock indication. The PLL loss of lock interrupt enable bit must also be set to generate the interrupt request. 1 Generate a reset request on a PLL loss of lock indication.
5 CME1	Clock Monitor Enable1 Enables the loss of clock monitoring circuit for the output of the RTC external reference clock. The LOCRE1 bit will determine whether an interrupt or a reset request is generated following a loss of RTC

Table continues on the next page...

MCG_C8 field descriptions (continued)

Field	Description
	clock indication. The CME1 bit should be set to a logic 1 when the MCG is in an operational mode that uses the RTC as its external reference clock or if the RTC is operational. CME1 bit must be set to a logic 0 before the MCG enters any Stop mode. Otherwise, a reset request may occur when in Stop mode. CME1 should also be set to a logic 0 before entering VLPR or VLPW power modes. 0 External clock monitor is disabled for RTC clock. 1 External clock monitor is enabled for RTC clock.
4–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 LOCS1	RTC Loss of Clock Status This bit indicates when a loss of clock has occurred. This bit is cleared by writing a logic 1 to it when set. 0 Loss of RTC has not occur. 1 Loss of RTC has occur

29.4.13 MCG Control 12 Register (MCG_C12)

Address: 4006_4000h base + 11h offset = 4006_4011h

Bit	7	6	5	4	3	2	1	0
Read	0							
Write								
Reset	0	0	0	0	0	0	0	0

MCG_C12 field descriptions

Field	Description
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

29.4.13 MCG Status 2 Register (MCG_S2)

Address: 4006_4000h base + 12h offset = 4006_4012h

Bit	7	6	5	4	3	2	1	0
Read	0							
Write								
Reset	0	0	0	0	0	0	0	0

MCG_S2 field descriptions

Field	Description
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

29.4.13 MCG Test 3 Register (MCG_T3)

Address: 4006_4000h base + 13h offset = 4006_4013h

Bit	7	6	5	4	3	2	1	0
Read	0							
Write								
Reset	0	0	0	0	0	0	0	0

MCG_T3 field descriptions

Field	Description
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

29.5 Functional description

29.5.1 MCG mode state diagram

The nine states of the MCG are shown in the following figure and are described in Table 29-4. The arrows indicate the permitted MCG mode transitions.

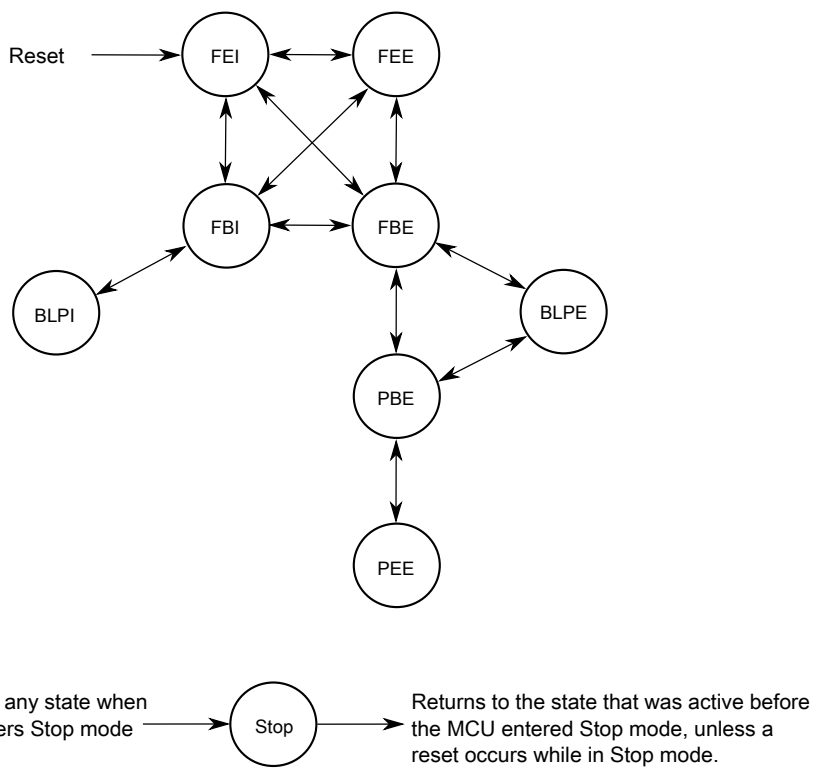


Figure 29-2. MCG mode state diagram

NOTE

- During exits from LLS or VLPS when the MCG is in PEE mode, the MCG will reset to PBE clock mode and the C1[CLKS] and S[CLKST] will automatically be set to 2'b10.
- If entering Normal Stop mode when the MCG is in PEE mode with PLLSTEN=0, the MCG will reset to PBE clock mode and C1[CLKS] and S[CLKST] will automatically be set to 2'b10.

29.5.1.1 MCG modes of operation

The MCG operates in one of the following modes.

Note

The MCG restricts transitions between modes. For the permitted transitions, see Figure 29-2.

Table 29-4. MCG modes of operation

Mode	Description
FLL Engaged Internal (FEI)	FLL engaged internal (FEI) is the default mode of operation and is entered when all the following condtions occur: • 00 is written to C1[CLKS]. • 1 is written to C1[IREFS]. • 0 is written to C6[PLLS]. In FEI mode, MCGOUTCLK is derived from the FLL clock (DCOCLK) that is controlled by the 32 kHz Internal Reference Clock (IRC). The FLL loop will lock the DCO frequency to the FLL factor, as selected by C4[DRST_DRS] and C4[DMX32] bits, times the internal reference frequency. See the C4[DMX32] bit description for more details. In FEI mode, the PLL is disabled in a low-power state unless C5[PLLCLKEN] is set .
FLL Engaged External (FEE)	FLL engaged external (FEE) mode is entered when all the following conditions occur: • 00 is written to C1[CLKS]. • 0 is written to C1[IREFS]. • C1[FRDIV] must be written to divide external reference clock to be within the range of 31.25 kHz to 39.0625 kHz • 0 is written to C6[PLLS].

Table continues on the next page...

Table 29-4. MCG modes of operation (continued)

Mode	Description
	In FEE mode, MCGOUTCLK is derived from the FLL clock (DCOCLK) that is controlled by the external reference clock. The FLL loop will lock the DCO frequency to the FLL factor, as selected by C4[DRST_DRS] and C4[DMX32] bits, times the external reference frequency, as specified by C1[FRDIV] and C2[RANGE]. See the C4[DMX32] bit description for more details. In FEE mode, the PLL is disabled in a low-power state unless C5[PLLCLKEN] is set .
FLL Bypassed Internal (FBI)	FLL bypassed internal (FBI) mode is entered when all the following conditions occur: • 01 is written to C1[CLKS]. • 1 is written to C1[IREFS]. • 0 is written to C6[PLLS] • 0 is written to C2[LP]. In FBI mode, the MCGOUTCLK is derived either from the slow (32 kHz IRC) or fast (4 MHz IRC) internal reference clock, as selected by the C2[IRCS] bit. The FLL is operational but its output is not used. This mode is useful to allow the FLL to acquire its target frequency while the MCGOUTCLK is driven from the C2[IRCS] selected internal reference clock. The FLL clock (DCOCLK) is controlled by the slow internal reference clock, and the DCO clock frequency locks to a multiplication factor, as selected by C4[DRST_DRS] and C4[DMX32] bits, times the internal reference frequency. See the C4[DMX32] bit description for more details. In FBI mode, the PLL is disabled in a low-power state unless C5[PLLCLKEN] is set .
FLL Bypassed External (FBE)	FLL bypassed external (FBE) mode is entered when all the following conditions occur: • 10 is written to C1[CLKS]. • 0 is written to C1[IREFS]. • C1[FRDIV] must be written to divide external reference clock to be within the range of 31.25 kHz to 39.0625 kHz. • 0 is written to C6[PLLS]. • 0 is written to C2[LP]. In FBE mode, the MCGOUTCLK is derived from the OSCSEL external reference clock. The FLL is operational but its output is not used. This mode is useful to allow the FLL to acquire its target frequency while the MCGOUTCLK is driven from the external reference clock. The FLL clock (DCOCLK) is controlled by the external reference clock, and the DCO clock frequency locks to a multiplication factor, as selected by C4[DRST_DRS] and C4[DMX32] bits, times the divided external reference frequency. See the C4[DMX32] bit description for more details. In FBE mode, the PLL is disabled in a low-power state unless C5[PLLCLKEN] is set .
PLL Engaged External (PEE)	PLL Engaged External (PEE) mode is entered when all the following conditions occur: • 00 is written to C1[CLKS]. • 0 is written to C1[IREFS]. • 1 is written to C6[PLLS]. In PEE mode, the MCGOUTCLK is derived from the output of PLL which is controlled by a external reference clock. The PLL clock frequency locks to a multiplication factor, as specified by its corresponding VDIV, times the selected PLL reference frequency, as specified by its corresponding PRDIV. The PLL's programmable reference divider must be configured to produce a valid PLL reference clock. The FLL is disabled in a low-power state.
PLL Bypassed External (PBE)	PLL Bypassed External (PBE) mode is entered when all the following conditions occur: • 10 is written to C1[CLKS].

Table continues on the next page...

Table 29-4. MCG modes of operation (continued)

Mode	Description
	• 0 is written to C1[IREFS]. • 1 is written to C6[PLLS]. • 0 is written to C2[LP]. In PBE mode, MCGOUTCLK is derived from the OSCSEL external reference clock; the PLL is operational, but its output clock is not used. This mode is useful to allow the PLL to acquire its target frequency while MCGOUTCLK is driven from the external reference clock. The PLL clock frequency locks to a multiplication factor, as specified by its [VDIV], times the PLL reference frequency, as specified by its [PRDIV]. In preparation for transition to PEE, the PLL's programmable reference divider must be configured to produce a valid PLL reference clock. The FLL is disabled in a low-power state.
Bypassed Low Power Internal (BLPI) [1]	Bypassed Low Power Internal (BLPI) mode is entered when all the following conditions occur: • 01 is written to C1[CLKS]. • 1 is written to C1[IREFS]. • 0 is written to C6[PLLS]. • 1 is written to C2[LP]. In BLPI mode, MCGOUTCLK is derived from the internal reference clock. The FLL is disabled and PLL is disabled even if C5[PLLCLKEN] is set to 1.
Bypassed Low Power External (BLPE) [1]	Bypassed Low Power External (BLPE) mode is entered when all the following conditions occur: • 10 is written to C1[CLKS]. • 0 is written to C1[IREFS]. • 1 is written to C2[LP]. In BLPE mode, MCGOUTCLK is derived from the OSCSEL external reference clock. The FLL is disabled and PLL is disabled even if the C5[PLLCLKEN] is set to 1.
Stop	Entered whenever the MCU enters a Stop state. The power modes are chip specific. For power mode assignments, see the chapter that describes how modules are configured and MCG behavior during Stop recovery. Entering Stop mode, the FLL is disabled, and all MCG clock signals are static except in the following case: MCGPLLCLK is active in Normal Stop mode when PLLSTEN=1 MCGIRCLK is active in Normal Stop mode when all the following conditions become true: • C1[IRCLKEN] = 1 • C1[IREFSTEN] = 1 **NOTE:** • In VLPS Stop Mode, the MCGIRCLK can be programmed to stay enabled and continue running if C1[IRCLKEN] = 1, C1[IREFSTEN]=1, and Fast IRC clock is selected (C2[IRCS] = 1)

Table 29-4. MCG modes of operation

Mode	Description
	NOTE: • When entering Low Power Stop modes (LLS or VLPS) from PEE mode, on exit the MCG clock mode is forced to PBE clock mode. C1[CLKS] and S[CLKST] will be configured to 2'b10if entering from PEE mode or to 2'b01 if entering from PEI mode, C5[PLLSTEN0] will be force to 1'b0 and S[LOCK] bit will be cleared without setting S[LOLS]. • When entering Normal Stop mode from PEE mode and if C5[PLLSTEN]=0, on exit the MCG clock mode is forced to PBE mode, the C1[CLKS] and S[CLKST] will be configured to 2'b10 and S[LOCK] bit will clear without setting S[LOLS]. If C5[PLLSTEN]=1, the S[LOCK] bit will not get cleared and on exit the MCG will continue to run in PEE mode.

1. **Caution:** If entering VLPR mode, MCG has to be configured and enter BLPE mode or BLPI mode with the Fast IRC clock selected (C2[IRCS]=1). After it enters VLPR mode, writes to any of the MCG control registers that can cause an MCG clock mode switch to a non low power clock mode must be avoided.

NOTE

For the chip-specific modes of operation, see the power management chapter of this MCU.

29.5.1.2 MCG mode switching

C1[IREFS] can be changed at any time, but the actual switch to the newly selected reference clocks is shown by S[IREFST]. When switching between engaged internal and engaged external modes, the FLL will begin locking again after the switch is completed.

C1[CLKS] can also be changed at any time, but the actual switch to the newly selected clock is shown by S[CLKST]. If the newly selected clock is not available, the previous clock will remain selected.

The C4[DRST_DRS] write bits can be changed at any time except when C2[LP] bit is 1. If C4[DRST_DRS] write bits are changed while in FLL engaged internal (FEI) or FLL engaged external (FEE) mode, the MCGOUTCLK switches to the new selected DCO range within three clocks of the selected DCO clock. After switching to the new DCO (indicated by the updated C4[DRST_DRS] read bits), the FLL remains unlocked for several reference cycles. The FLL lock time is provided in the device data sheet as $t_{fll_acquire}$.

29.5.2 Low-power bit usage

C2[LP] is provided to allow the FLL or PLL to be disabled and thus conserve power when these systems are not being used. C4[DRST_DRS] can not be written while C2[LP] is 1. However, in some applications, it may be desirable to enable the FLL or PLL and allow it to lock for maximum accuracy before switching to an engaged mode. Do this by writing 0 to C2[LP].

29.5.3 MCG Internal Reference Clocks

This module supports two internal reference clocks with nominal frequencies of 32 kHz (slow IRC) and 4 MHz (fast IRC). The fast IRC frequency can be divided down by programming of the FCRDIV to produce a frequency range of 32 kHz to 4 MHz.

29.5.3.1 MCG Internal Reference Clock

The MCG Internal Reference Clock (MCGIRCLK) provides a clock source for other on-chip peripherals and is enabled when C1[IRCLKEN]=1. When enabled, MCGIRCLK is driven by either the fast internal reference clock (4 MHz IRC which can be divided down by the FRDIV factors) or the slow internal reference clock (32 kHz IRC). The IRCS clock frequency can be re-targeted by trimming the period of its IRCS selected internal reference clock. This can be done by writing a new trim value to the C3[SCTRIM]:C4[SCFTRIM] bits when the slow IRC clock is selected or by writing a new trim value to C4[FCTRIM]:C2[FCFTRIM] when the fast IRC clock is selected. The internal reference clock period is proportional to the trim value written. C3[SCTRIM]:C4[SCFTRIM] (if C2[IRCS]=0) and C4[FCTRIM]:C2[FCFTRIM] (if C2[IRCS]=1) bits affect the MCGOUTCLK frequency if the MCG is in FBI or BLPI modes. C3[SCTRIM]:C4[SCFTRIM] (if C2[IRCS]=0) bits also affect the MCGOUTCLK frequency if the MCG is in FEI mode.

Additionally, this clock can be enabled in Stop mode by setting C1[IRCLKEN] and C1[IREFSTEN], otherwise this clock is disabled in Stop mode.

29.5.4 External Reference Clock

The MCG module can support an external reference clock in all modes. See the device datasheet for external reference frequency range. When C1[IREFS] is set, the external reference clock will not be used by the FLL or PLL. In these modes, the frequency can be equal to the maximum frequency the chip-level timing specifications will support.

If any of the CME bits are asserted the slow internal reference clock is enabled along with the enabled external clock monitor. For the case when C6[CME0]=1, a loss of clock is detected if the OSC0 external reference falls below a minimum frequency (f_{loc_high} or f_{loc_low} depending on C2[RANGE0]). For the case when C8[CME1]=1, a loss of clock is detected if the RTC external reference falls below a minimum frequency (f_{loc_low}).

NOTE

All clock monitors must be disabled before entering these low-power modes: Stop, VLPS, VLPR, VLPW, LLS, and VLLSx.

On detecting a loss-of-clock event, the MCU generates a system reset if the respective LOCRE bit is set. Otherwise the MCG sets the respective LOCS bit and the MCG generates a LOCS interrupt request. In the case where a OSC loss of clock is detected, the PLL LOCK status bit is cleared.

29.5.5 MCG Fixed Frequency Clock

The MCG Fixed Frequency Clock (MCGFFCLK) provides a fixed frequency clock source for other on-chip peripherals; see the block diagram. This clock is driven by either the slow clock from the internal reference clock generator or the external reference clock from the Crystal Oscillator, divided by the FLL reference clock divider. The source of MCGFFCLK is selected by C1[IREFS].

This clock is synchronized to the peripheral bus clock and is valid only when its frequency is not more than 1/8 of the MCGOUTCLK frequency. When it is not valid, it is disabled and held high. The MCGFFCLK is not available when the MCG is in BLPI mode. This clock is also disabled in Stop mode. The FLL reference clock must be set within the valid frequency range for the MCGFFCLK.

29.5.6 MCG PLL clock

The MCG PLL Clock (MCGPLLCLK) is available depending on the device's configuration of the MCG module. For more details, see the clock distribution chapter of this MCU. The MCGPLLCLK is prevented from coming out of the MCG until it is enabled and S[LOCK0] is set.

29.5.7 MCG Auto TRIM (ATM)

The MCG Auto Trim (ATM) is a MCG feature that when enabled, it configures the MCG hardware to automatically trim the MCG Internal Reference Clocks using an external clock as a reference. The selection between which MCG IRC clock gets tested and enabled is controlled by the ATC[ATMS] control bit (ATC[ATMS]=0 selects the 32 kHz IRC and ATC[ATMS]=1 selects the 4 MHz IRC). If 4 MHz IRC is selected for the ATM, a divide by 128 is enabled to divide down the 4 MHz IRC to a range of 31.250 kHz.

When MCG ATM is enabled by writing ATC[ATME] bit to 1, The ATM machine will start auto trimming the selected IRC clock. During the autotrim process, ATC[ATME] will remain asserted and will deassert after ATM is completed or an abort occurs. The MCG ATM is aborted if a write to any of the following control registers is detected : C1, C3, C4, or ATC or if Stop mode is entered. If an abort occurs, ATC[ATMF] fail flag is asserted.

The ATM machine uses the bus clock as the external reference clock to perform the IRC auto-trim. Therefore, it is required that the MCG is configured in a clock mode where the reference clock used to generate the system clock is the external reference clock such as FBE clock mode. The MCG must not be configured in a clock mode where selected IRC ATM clock is used to generate the system clock. The bus clock is also required to be running with in the range of 8–16 MHz.

To perform the ATM on the selected IRC, the ATM machine uses the successive approximation technique to adjust the IRC trim bits to generate the desired IRC trimmed frequency. The ATM SARs each of the ATM IRC trim bits starting with the MSB. For each trim bit test, the ATM uses a pulse that is generated by the ATM selected IRC clock to enable a counter that counts number of ATM external clocks. At end of each trim bit, the ATM external counter value is compared to the ATCV[15:0] register value. Based on the comparison result, the ATM trim bit under test will get cleared or stay asserted. This is done until all trim bits have been tested by ATM SAR machine.

Before the ATM can be enabled, the ATM expected count needs to be derived and stored into the ATCV register. The ATCV expected count is derived based on the required target Internal Reference Clock (IRC) frequency, and the frequency of the external reference clock using the following formula:

$$\text{ATCV Expected Count Value} = 21 * (Fe / Fr)$$

- Fr = Target Internal Reference Clock (IRC) Trimmed Frequency
- Fe = External Clock Frequency

If the auto trim is being performed on the 4 MHz IRC, the calculated expected count value must be multiplied by 128 before storing it in the ATCV register. Therefore, the ATCV Expected Count Value for trimming the 4 MHz IRC is calculated using the following formula.

$$\text{Expected Count Value} = (\text{Fe}/\text{Fr}) * 21 * (128)$$

29.6 Initialization / Application information

This section describes how to initialize and configure the MCG module in an application.

The following sections include examples on how to initialize the MCG and properly switch between the various available modes.

29.6.1 MCG module initialization sequence

The MCG comes out of reset configured for FEI mode.

The internal reference will stabilize in $t_{irefsts}$ microseconds before the FLL can acquire lock. As soon as the internal reference is stable, the FLL will acquire lock in $t_{fll_acquire}$ milliseconds.

29.6.1.1 Initializing the MCG

Because the MCG comes out of reset in FEI mode, the only MCG modes that can be directly switched to upon reset are FEE, FBE, and FBI modes (see Figure 29-2). Reaching any of the other modes requires first configuring the MCG for one of these three intermediate modes. Care must be taken to check relevant status bits in the MCG status register reflecting all configuration changes within each mode.

To change from FEI mode to FEE or FBE modes, follow this procedure:

1. Enable the external clock source by setting the appropriate bits in C2 register.
2. Write to C1 register to select the clock mode.
   - If entering FEE mode, set C1[FRDIV] appropriately, clear C1[IREFS] bit to switch to the external reference, and leave C1[CLKS] at 2'b00 so that the output of the FLL is selected as the system clock source.

- If entering FBE, clear C1[IREFS] to switch to the external reference and change C1[CLKS] to 2'b10 so that the external reference clock is selected as the system clock source. The C1[FRDIV] bits should also be set appropriately here according to the external reference frequency to keep the FLL reference clock in the range of 31.25 kHz to 39.0625 kHz. Although the FLL is bypassed, it is still on in FBE mode.
- The internal reference can optionally be kept running by setting C1[IRCLKEN]. This is useful if the application will switch back and forth between internal and external modes. For minimum power consumption, leave the internal reference disabled while in an external clock mode.

3. Once the proper configuration bits have been set, wait for the affected bits in the MCG status register to be changed appropriately, reflecting that the MCG has moved into the proper mode.
   - If the MCG is in FEE, FBE, PEE, PBE, or BLPE mode, and C2[EREFS] was also set in step 1, wait here for S[OSCINIT0] bit to become set indicating that the external clock source has finished its initialization cycles and stabilized.
   - If in FEE mode, check to make sure S[IREFST] is cleared before moving on.
   - If in FBE mode, check to make sure S[IREFST] is cleared and S[CLKST] bits have changed to 2'b10 indicating the external reference clock has been appropriately selected. Although the FLL is bypassed, it is still on in FBE mode.
4. Write to the C4 register to determine the DCO output (MCGFLLCLK) frequency range.
   - By default, with C4[DMX32] cleared to 0, the FLL multiplier for the DCO output is 640. For greater flexibility, if a mid-low-range FLL multiplier of 1280 is desired instead, set C4[DRST_DRS] bits to 2'b01 for a DCO output frequency of 40 MHz. If a mid high-range FLL multiplier of 1920 is desired instead, set the C4[DRST_DRS] bits to 2'b10 for a DCO output frequency of 60 MHz. If a high-range FLL multiplier of 2560 is desired instead, set the C4[DRST_DRS] bits to 2'b11 for a DCO output frequency of 80 MHz.
   - When using a 32.768 kHz external reference, if the maximum low-range DCO frequency that can be achieved with a 32.768 kHz reference is desired, set C4[DRST_DRS] bits to 2'b00 and set C4[DMX32] bit to 1. The resulting DCO output (MCGOUTCLK) frequency with the new multiplier of 732 will be 24 MHz.

- When using a 32.768 kHz external reference, if the maximum mid-range DCO frequency that can be achieved with a 32.768 kHz reference is desired, set C4[DRST_DRS] bits to 2'b01 and set C4[DMX32] bit to 1. The resulting DCO output (MCGOUTCLK) frequency with the new multiplier of 1464 will be 48 MHz.
- When using a 32.768 kHz external reference, if the maximum mid high-range DCO frequency that can be achieved with a 32.768 kHz reference is desired, set C4[DRST_DRS] bits to 2'b10 and set C4[DMX32] bit to 1. The resulting DCO output (MCGOUTCLK) frequency with the new multiplier of 2197 will be 72 MHz.
- When using a 32.768 kHz external reference, if the maximum high-range DCO frequency that can be achieved with a 32.768 kHz reference is desired, set C4[DRST_DRS] bits to 2'b11 and set C4[DMX32] bit to 1. The resulting DCO output (MCGOUTCLK) frequency with the new multiplier of 2929 will be 96 MHz.

5. Wait for the FLL lock time to guarantee FLL is running at new C4[DRST_DRS] and C4[DMX32] programmed frequency.

To change from FEI clock mode to FBI clock mode, follow this procedure:

1. Change C1[CLKS] bits in C1 register to 2'b01 so that the internal reference clock is selected as the system clock source.
2. Wait for S[CLKST] bits in the MCG status register to change to 2'b01, indicating that the internal reference clock has been appropriately selected.
3. Write to the C2 register to determine the IRCS output (IRCSCLK) frequency range.
   - By default, with C2[IRCS] cleared to 0, the IRCS selected output clock is the slow internal reference clock (32 kHz IRC). If the faster IRC is desired, set C2[IRCS] to 1 for a IRCS clock derived from the 4 MHz IRC source.

29.6.2 Using a 32.768 kHz reference

In FEE and FBE modes, if using a 32.768 kHz external reference, at the default FLL multiplication factor of 640, the DCO output (MCGFLLCLK) frequency is 20.97 MHz at low-range.

If C4[DRST_DRS] bits are set to 2'b01, the multiplication factor is doubled to 1280, and the resulting DCO output frequency is 41.94 MHz at mid-low-range. If C4[DRST_DRS] bits are set to 2'b10, the multiplication factor is set to 1920, and the resulting DCO output frequency is 62.91 MHz at mid high-range. If C4[DRST_DRS] bits are set to 2'b11, the multiplication factor is set to 2560, and the resulting DCO output frequency is 83.89 MHz at high-range.

In FBI and FEI modes, setting C4[DMX32] bit is not recommended. If the internal reference is trimmed to a frequency above 32.768 kHz, the greater FLL multiplication factor could potentially push the microcontroller system clock out of specification and damage the part.

29.6.3 MCG mode switching

When switching between operational modes of the MCG, certain configuration bits must be changed in order to properly move from one mode to another.

Each time any of these bits are changed (C6[PLLS], C1[IREFS], C1[CLKS], C2[IRCS], or C2[EREFS], the corresponding bits in the MCG status register (PLLST, IREFST, CLKST, IRCST, or OSCINIT) must be checked before moving on in the application software.

Additionally, care must be taken to ensure that the reference clock divider (C1[FRDIV] and C5[PRDIV0]) is set properly for the mode being switched to. For instance, in PEE mode, if using a 16 MHz crystal, C5[PRDIV0] must be set to 3'b000 (divide-by-1) or 3'b001 (divide-by-2) to divide the external reference down to the required frequency between 8 and 16 MHz

In FBE, FEE, FBI, and FEI modes, at any time, the application can switch the FLL multiplication factor between 640, 1280, 1920, and 2560 with C4[DRST_DRS] bits. Writes to C4[DRST_DRS] bits will be ignored if C2[LP]=1.

The table below shows MCGOUTCLK frequency calculations using C1[FRDIV], C5[PRDIV0], and C6[VDIV0] settings for each clock mode.

Table 29-5. MCGOUTCLK Frequency Calculation Options

Clock Mode	$f_{MCGOUTCLK}$[1]	Note
FEI (FLL engaged internal)	$f_{int} \times F$	Typical $f_{MCGOUTCLK}$ = 21 MHz immediately after reset.
FEE (FLL engaged external)	$(f_{ext} / FLL_R) \times F$	f_{ext} / FLL_R must be in the range of 31.25 kHz to 39.0625 kHz
FBE (FLL bypassed external)	OSCCLK	OSCCLK / FLL_R must be in the range of 31.25 kHz to 39.0625 kHz

Table continues on the next page...

Table 29-5. MCGOUTCLK Frequency Calculation Options (continued)

Clock Mode	$f_{MCGOUTCLK}$[1]	Note
FBI (FLL bypassed internal)	MCGIRCLK	Selectable between slow and fast IRC
PEE (PLL engaged external)	(OSCCLK / PLL_R) × M	OSCCLK / PLL_R must be in the range of 8 – 16 MHz
PBE (PLL bypassed external)	OSCCLK	OSCCLK / PLL_R must be in the range of 8 – 16 MHz
BLPI (Bypassed low power internal)	MCGIRCLK	Selectable between slow and fast IRC
BLPE (Bypassed low power external)	OSCCLK	

1. FLL_R is the reference divider selected by the C1[FRDIV] bits, F is the FLL factor selected by C4[DRST_DRS] and C4[DMX32] bits , PLL_R is the reference divider selected by C5[PRDIV0] bits, and M is the multiplier selected by C6[VDIV0] bits.

This section will include several mode switching examples, using an 16 MHz external crystal. If using an external clock source less than 8 MHz, the MCG must not be configured for any of the PLL modes (PEE and PBE).

29.6.3.1 Example 1: Moving from FEI to PEE Mode with OSC0 as the source for the external crystal clock: External Crystal = 16 MHz, MCGOUTCLK frequency = 120 MHz

In this example, the MCG will move through the proper operational modes from FEI to PEE to achieve 120 MHz MCGOUTCLK frequency from 16 MHz external crystal reference. First, the code sequence will be described. Then there is a flowchart that illustrates the sequence.

1. First, FEI must transition to FBE mode:
   a. C2 = 0x2C
      - C2[RANGE] set to 2'b10 because the frequency of 16 MHz is within the high frequency range.
      - C2[HGO] set to 1 to configure the crystal oscillator for high gain operation.
      - C2[EREFS] set to 1, because a crystal is being used.
   b. C1 = 0xA0
      - C1[CLKS] set to 2'b10 to select external reference clock as system clock source

- C1[FRDIV] set to 3'b100, or divide-by-512 because 8 MHz / 512 = 31.25 kHz which is in the 31.25 kHz to 39.0625 kHz range required by the FLL
- C1[IREFS] cleared to 0, selecting the external reference clock and enabling the external oscillator.

c. Loop until S[OSCINIT0] is 1, indicating the crystal selected by C2[EREFS0] has been initialized.

d. Loop until S[IREFST] is 0, indicating the external reference is the current source for the reference clock.

e. Loop until S[CLKST] is 2'b10, indicating that the external reference clock is selected to feed MCGOUTCLK.

2. Then configure C5[PRDIV0] to generate correct PLL reference frequency.

a. C5 = 0x01

- C5[PRDIV] set to 3'b001, or divide-by-2 resulting in a pll reference frequency of 16MHz/2 = 8 MHz.

3. Then, FBE must transition either directly to PBE mode or first through BLPE mode and then to PBE mode:

a. BLPE: If a transition through BLPE mode is desired, first set C2[LP] to 1.

b. BLPE/PBE: C6 = 0x4E

- C6[PLLS] set to 1, selects the PLL. At this time, with a C1[PRDIV] value of 2'b001, the PLL reference divider is 2 (see PLL External Reference Divide Factor table), resulting in a reference frequency of 16 MHz/ 2 = 8 MHz. In BLPE mode, changing the C6[PLLS] bit only prepares the MCG for PLL usage in PBE mode.
- C6[VDIV] set to 5'b01110, or multiply-by-30 because 8 MHz reference * 30 = 240 MHz. This is the MCGPLL0CLK2X frequency, which is the frequency of the VCO. This is divided by 2 to achieve the MCGPLL0CLK frequency of 120 MHz which is later used as the MCGOUTCLK frequency. In BLPE mode, the configuration of the VDIV bits does not matter because the PLL is disabled. Changing them only sets up the multiply value for PLL usage in PBE mode.

c. BLPE: If transitioning through BLPE mode, clear C2[LP] to 0 here to switch to PBE mode.

d. PBE: Loop until S[PLLST] is set, indicating that the current source for the PLLS clock is the PLL.

e. PBE: Then loop until S[LOCK0] is set, indicating that the PLL has acquired lock.

4. Lastly, PBE mode transitions into PEE mode:

   a. C1 = 0x20

      - C1[CLKS] set to 2'b00 to select the output of the PLL as the system clock source.

   b. Loop until S[CLKST] are 2'b11, indicating that the PLL output is selected to feed MCGOUTCLK in the current clock mode.

      - Now, with PRDIV of divide-by-2, and C6[VDIV] of multiply-by-30, MCGOUTCLK = [(16 MHz / 2) * 30] / 2 = 120 MHz.

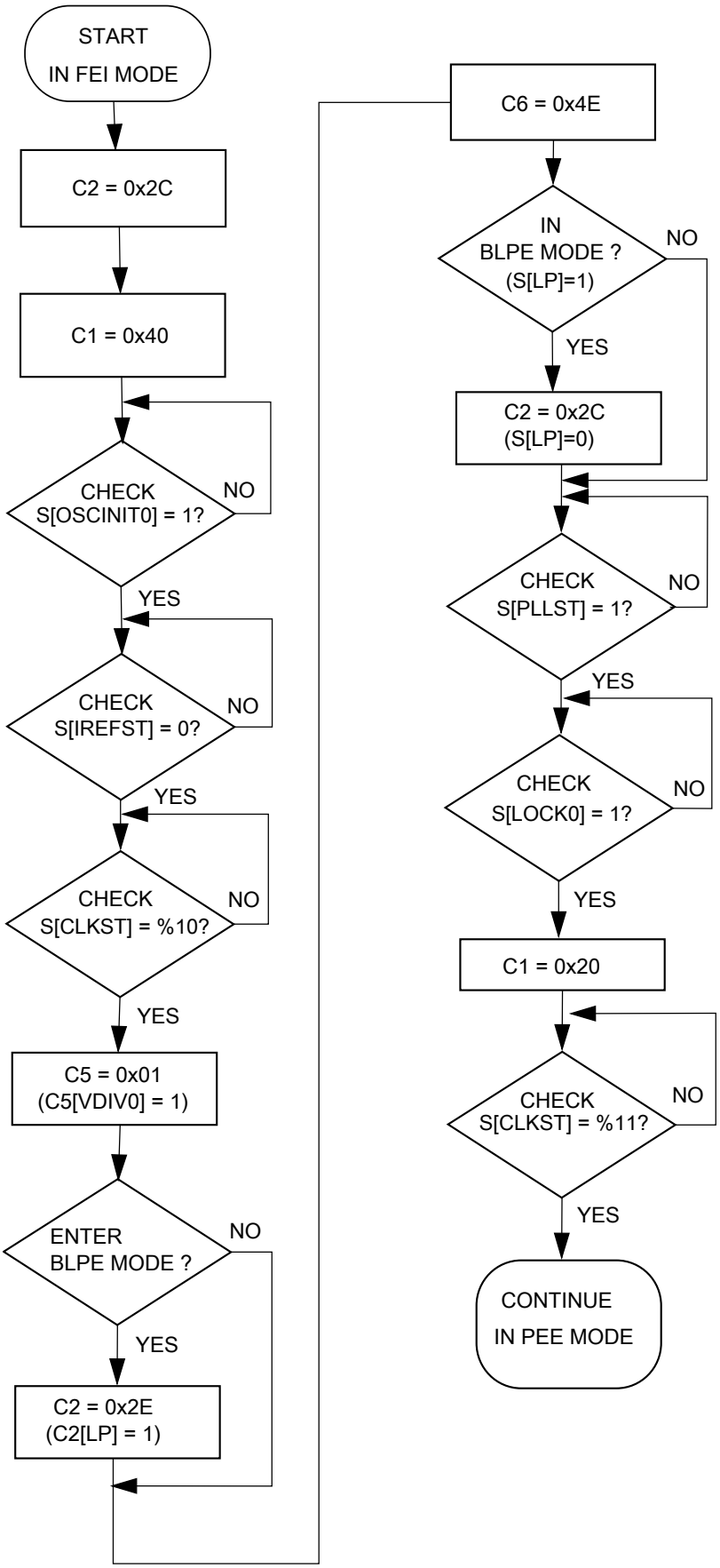


Figure 29-3. Flowchart of FEI to PEE mode transition using an 16 MHz crystal

29.6.3.2 Example 2: Moving from PEE to BLPI mode: MCGOUTCLK frequency =32 kHz

In this example, the MCG will move through the proper operational modes from PEE mode with a 16 MHz crystal configured for a 120 MHz MCGOUTCLK frequency (see previous example) to BLPI mode with a 32 kHz MCGOUTCLK frequency. First, the code sequence will be described. Then there is a flowchart that illustrates the sequence.

1. First, PEE must transition to PBE mode:
   a. C1 = 0x40
      - C1[CLKS] set to 2'b10 to switch the system clock source to the external reference clock.
   b. Loop until S[CLKST] are 2'b10, indicating that the external reference clock is selected to feed MCGOUTCLK.
2. Then, PBE must transition either directly to FBE mode or first through BLPE mode and then to FBE mode:
   a. BLPE: If a transition through BLPE mode is desired, first set C2[LP] to 1.
   b. BLPE/FBE: C6 = 0x00
      - C6[PLLS] clear to 0 to select the FLL. At this time, with C1[FRDIV] value of 3'b100, the FLL divider is set to 512, resulting in a reference frequency of 16 MHz / 512 = 31.25 kHz. If C1[FRDIV] was not previously set to 3'b100 (necessary to achieve required 31.25–39.06 kHz FLL reference frequency with an 16 MHz external source frequency), it must be changed prior to clearing C6[PLLS] bit. In BLPE mode,changing this bit only prepares the MCG for FLL usage in FBE mode. With C6[PLLS] = 0, the C6[VDIV] value does not matter.
   c. BLPE: If transitioning through BLPE mode, clear C2[LP] to 0 here to switch to FBE mode.
   d. FBE: Loop until S[PLLST] is cleared, indicating that the current source for the PLLS clock is the FLL.
3. Next, FBE mode transitions into FBI mode:
   a. C1 = 0x64
      - C1[CLKS] set to 2'b01 to switch the system clock to the internal reference clock.

- C1[IREFS] set to 1 to select the internal reference clock as the reference clock source.
- C1[FRDIV] remain unchanged because the reference divider does not affect the internal reference.

b. Loop until S[IREFST] is 1, indicating the internal reference clock has been selected as the reference clock source.

c. Loop until S[CLKST] are 2'b01, indicating that the internal reference clock is selected to feed MCGOUTCLK.

4. Lastly, FBI transitions into BLPI mode.

a. C2 = 0x22

- C2[LP] is 1
- C2[RANGE], C2[HGO], C2[EREFS], C1[IRCLKEN], and C1[IREFSTEN] bits are ignored when the C1[IREFS] bit is set. They can remain set, or be cleared at this point.

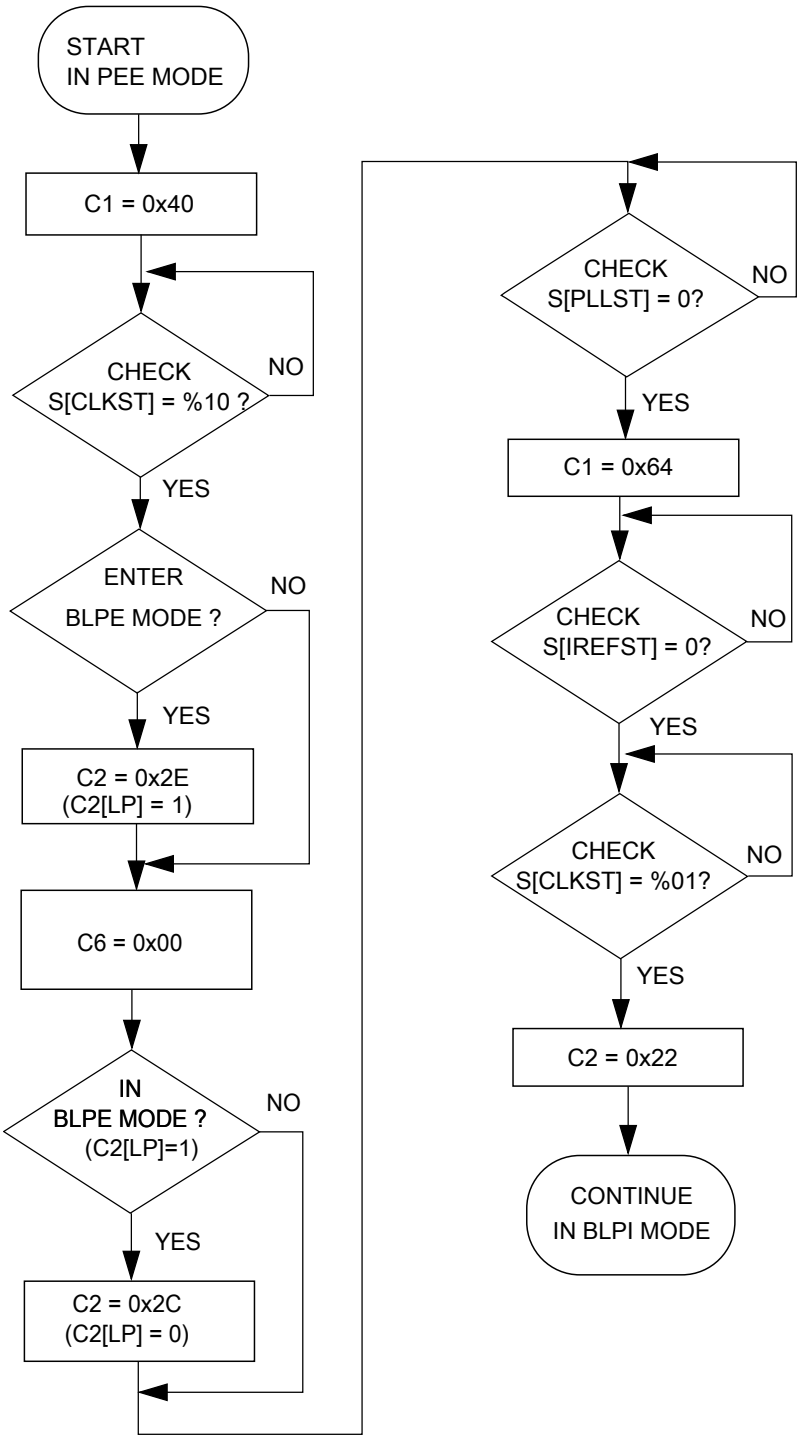


Figure 29-4. Flowchart of PEE to BLPI mode transition using an 16 MHz crystal

Chapter 30
Oscillator (OSC)

30.1 Chip-specific OSC information

30.1.1 OSC modes of operation with MCG

The MCG's C2 register bits configure the oscillator frequency range. See the OSC and MCG chapters for more details.

30.2 Introduction

The OSC module is a crystal oscillator. The module, in conjunction with an external crystal or resonator, generates a reference clock for the MCU.

30.3 Features and Modes

Key features of the module are listed here.

- Supports 32 kHz crystals (Low Range mode)
- Supports 3–8 MHz, 8–32 MHz crystals and resonators (High Range mode)
- Automatic Gain Control (AGC) to optimize power consumption in high frequency ranges 3–8 MHz, 8–32 MHz using low-power mode
- High gain option in frequency ranges: 32 kHz, 3–8 MHz, and 8–32 MHz
- Voltage and frequency filtering to guarantee clock frequency and stability
- Optionally external input bypass clock from EXTAL signal directly

- One clock for MCU clock system
- Two clocks for on-chip peripherals that can work in Stop modes

Functional Description describes the module's operation in more detail.

30.4 Block Diagram

The OSC module uses a crystal or resonator to generate three filtered oscillator clock signals.Three clocks are output from OSC module: OSCCLK for MCU system, OSCERCLK for on-chip peripherals, and OSC32KCLK. The OSCCLK can only work in run mode. OSCERCLK and OSC32KCLK can work in low power modes. For the clock source assignments, refer to the clock distribution information of this MCU.

Refer to the chip configuration details for the external reference clock source in this MCU.

The figure found here shows the block diagram of the OSC module.

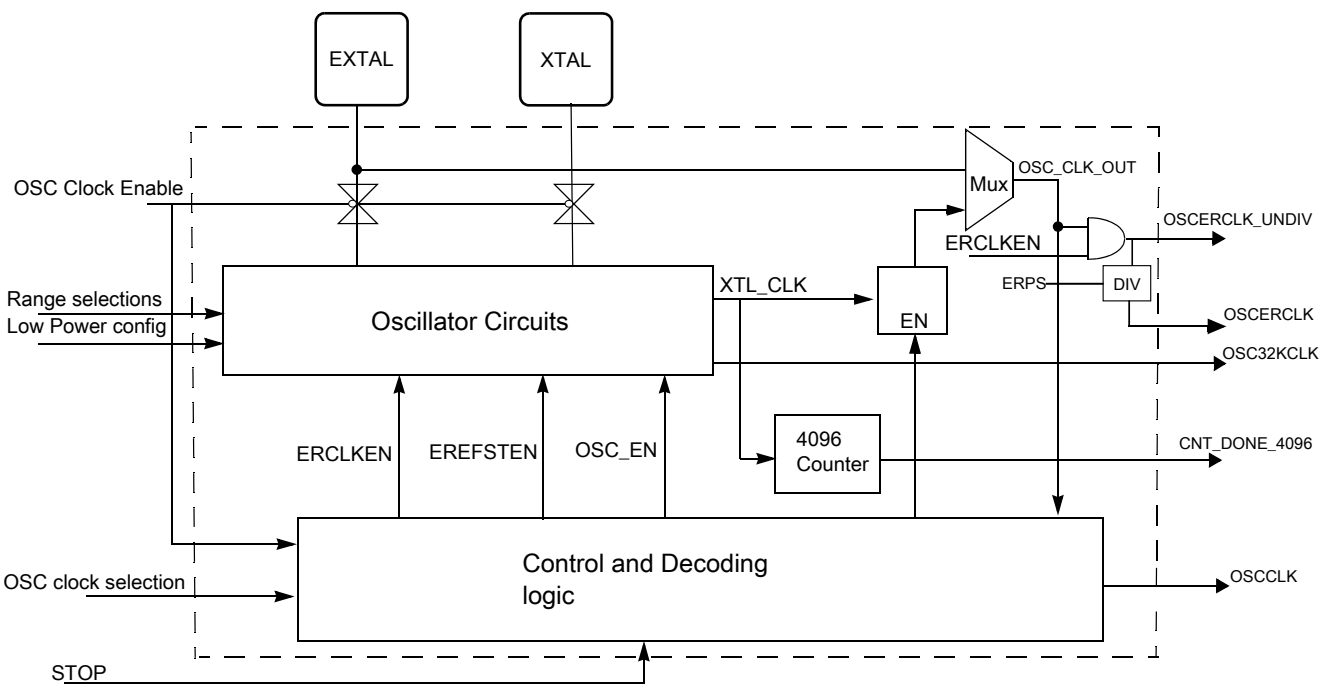


Figure 30-1. OSC Module Block Diagram

30.5 OSC Signal Descriptions

The table found here shows the user-accessible signals available for the OSC module.

Refer to signal multiplexing information for this MCU for more details.

Table 30-1. OSC Signal Descriptions

Signal	Description	I/O
EXTAL	External clock/Oscillator input	I
XTAL	Oscillator output	O

30.6 External Crystal / Resonator Connections

The connections for a crystal/resonator frequency reference are shown in the figures found here.

When using low-frequency, low-power mode, the only external component is the crystal or ceramic resonator itself. In the other oscillator modes, load capacitors (C_x, C_y) and feedback resistor (R_F) are required. The following table shows all possible connections.

Table 30-2. External Caystal/Resonator Connections

Oscillator Mode	Connections
Low-frequency (32 kHz), low-power	Connection 1[1]
Low-frequency (32 kHz), high-gain	Connection 2/Connection 3[2]
High-frequency (3~32 MHz), low-power	Connection 3[1]
High-frequency (3~32 MHz), high-gain	Connection 3

1. With the low-power mode, the oscillator has the internal feedback resistor R_F. Therefore, the feedback resistor must not be externally with the Connection 3.
2. When the load capacitors (Cx, Cy) are greater than 30 pF, use Connection 3.

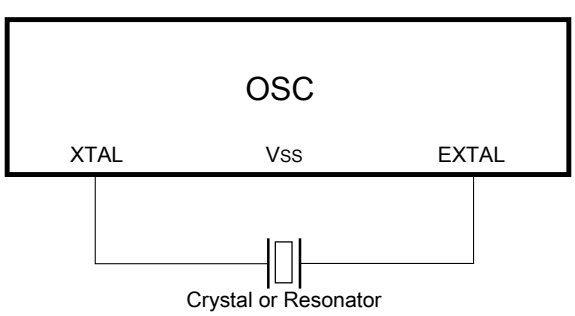


Figure 30-2. Crystal/Ceramic Resonator Connections - Connection 1

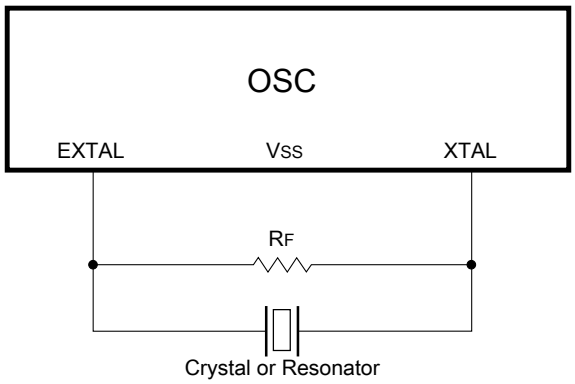


Figure 30-3. Crystal/Ceramic Resonator Connections - Connection 2

NOTE

Connection 1 and Connection 2 should use internal capacitors as the load of the oscillator by configuring the CR[SCxP] bits.

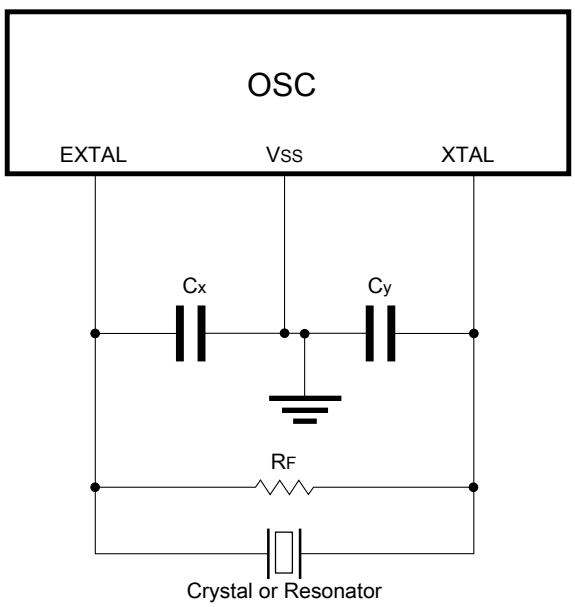


Figure 30-4. Crystal/Ceramic Resonator Connections - Connection 3

30.7 External Clock Connections

In external clock mode, the pins can be connected as shown in the figure found here.

NOTE

XTAL can be used as a GPIO when the GPIO alternate function is configured for it.

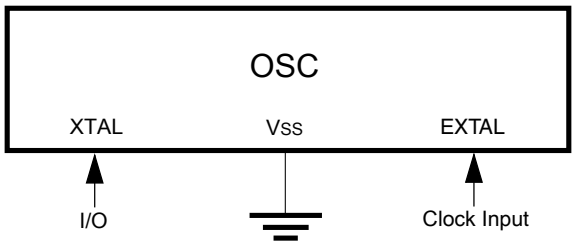


Figure 30-5. External Clock Connections

30.8 Memory Map/Register Definitions

Some oscillator module register bits are typically incorporated into other peripherals such as MCG or SIM.

30.8.1 OSC Memory Map/Register Definition

OSC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4006_5000	OSC Control Register (OSC_CR)	8	R/W	00h	30.8.1.1/ 723
4006_5002	OSC_DIV (OSC_OSC_DIV)	8	R/W	00h	30.8.1.2/ 725

30.8.1.1 OSC Control Register (OSC_CR)

NOTE

After OSC is enabled and starts generating the clocks, the configurations such as low power and frequency range, must not be changed.

Address: 4006_5000h base + 0h offset = 4006_5000h

Bit	7	6	5	4	3	2	1	0
Read	ERCLKEN	0	EREFSTEN	0	SC2P	SC4P	SC8P	SC16P
Write								
Reset	0	0	0	0	0	0	0	0

OSC_CR field descriptions

Field	Description
7 ERCLKEN	External Reference Enable Enables external reference clock (OSCERCLK) . 0 External reference clock is inactive. 1 External reference clock is enabled.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 EREFSTEN	External Reference Stop Enable Controls whether or not the external reference clock (OSCERCLK) remains enabled when MCU enters Stop mode. 0 External reference clock is disabled in Stop mode. 1 External reference clock stays enabled in Stop mode if ERCLKEN is set before entering Stop mode.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 SC2P	Oscillator 2 pF Capacitor Load Configure Configures the oscillator load. 0 Disable the selection. 1 Add 2 pF capacitor to the oscillator load.
2 SC4P	Oscillator 4 pF Capacitor Load Configure Configures the oscillator load. 0 Disable the selection. 1 Add 4 pF capacitor to the oscillator load.
1 SC8P	Oscillator 8 pF Capacitor Load Configure Configures the oscillator load. 0 Disable the selection. 1 Add 8 pF capacitor to the oscillator load.
0 SC16P	Oscillator 16 pF Capacitor Load Configure Configures the oscillator load. 0 Disable the selection. 1 Add 16 pF capacitor to the oscillator load.

30.8.1.2 OSC_DIV (OSC_OSC_DIV)

OSC Clock divider register.

Address: 4006_5000h base + 2h offset = 4006_5002h

Bit	7	6	5	4	3	2	1	0
Read	ERPS		0	0	0	0	0	0
Write								
Reset	0	0	0	0	0	0	0	0

OSC_OSC_DIV field descriptions

Field	Description
7–6 ERPS	ERCLK prescaler. These two bits are used to divide the ERCLK output. The un-divided ERCLK output is not affected by these two bits. 00 The divisor ratio is 1. 01 The divisor ratio is 2. 10 The divisor ratio is 4. 11 The divisor ratio is 8.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

30.9 Functional Description

Functional details of the module can be found here.

30.9.1 OSC module states

The states of the OSC module are shown in the following figure. The states and their transitions between each other are described in this section.

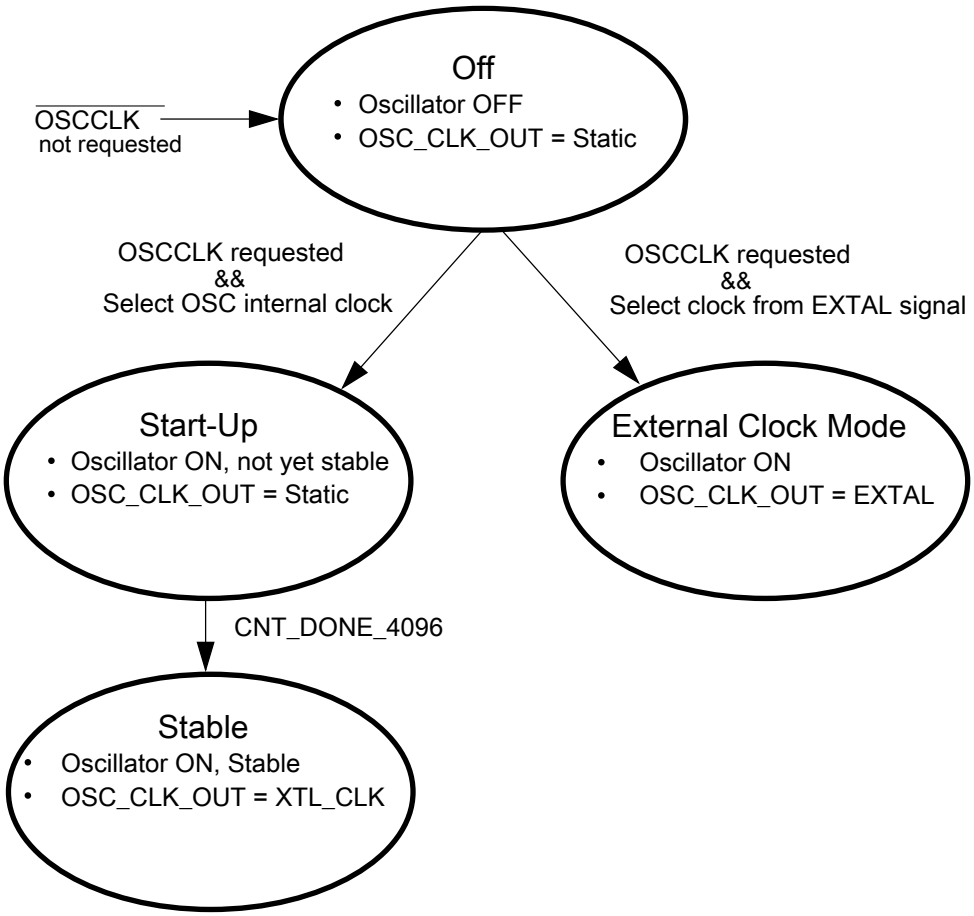


Figure 30-6. OSC Module state diagram

NOTE

XTL_CLK is the clock generated internally from OSC circuits.

30.9.1.1 Off

The OSC enters the Off state when the system does not require OSC clocks. Upon entering this state, XTL_CLK is static unless OSC is configured to select the clock from the EXTAL pad by clearing the external reference clock selection bit. For details regarding the external reference clock source in this MCU, refer to the chip configuration details. The EXTAL and XTAL pins are also decoupled from all other oscillator circuitry in this state. The OSC module circuitry is configured to draw minimal current.

30.9.1.2 Oscillator startup

The OSC enters startup state when it is configured to generate clocks (internally the OSC_EN transitions high) using the internal oscillator circuits by setting the external reference clock selection bit. In this state, the OSC module is enabled and oscillations are starting up, but have not yet stabilized. When the oscillation amplitude becomes large enough to pass through the input buffer, XTL_CLK begins clocking the counter. When the counter reaches 4096 cycles of XTL_CLK, the oscillator is considered stable and XTL_CLK is passed to the output clock OSC_CLK_OUT.

30.9.1.3 Oscillator Stable

The OSC enters stable state when it is configured to generate clocks (internally the OSC_EN transitions high) using the internal oscillator circuits by setting the external reference clock selection bit and the counter reaches 4096 cycles of XTL_CLK (when CNT_DONE_4096 is high). In this state, the OSC module is producing a stable output clock on OSC_CLK_OUT. Its frequency is determined by the external components being used.

30.9.1.4 External Clock mode

The OSC enters external clock state when it is enabled and external reference clock selection bit is cleared. For details regarding external reference clock source in this MCU, see the chip configuration details. In this state, the OSC module is set to buffer (with hysteresis) a clock from EXTAL onto the OSC_CLK_OUT. Its frequency is determined by the external clock being supplied.

30.9.2 OSC module modes

The OSC is a pierce-type oscillator that supports external crystals or resonators operating over the frequency ranges shown in Table 30-3. These modes assume the following conditions: OSC is enabled to generate clocks (OSC_EN=1), configured to generate clocks internally (MCG_C2[EREFS] = 1), and some or one of the other peripherals (MCG, Timer, and so on) is configured to use the oscillator output clock (OSC_CLK_OUT).

Table 30-3. Oscillator modes

Mode	Frequency Range
Low-frequency, high-gain	f_{osc_lo} (32.768 kHz) up to f_{osc_lo} (39.0625 kHz)

Table continues on the next page...

Table 30-3. Oscillator modes (continued)

Mode	Frequency Range
High-frequency mode1, high-gain	$f_{osc_hi_1}$ (3 MHz) up to $f_{osc_hi_1}$ (8 MHz)
High-frequency mode1, low-power	
High-frequency mode2, high-gain	$f_{osc_hi_2}$ (8 MHz) up to $f_{osc_hi_2}$ (32 MHz)
High-frequency mode2, low-power	

NOTE

For information about low power modes of operation used in this chip and their alignment with some OSC modes, see the chip's Power Management details.

30.9.2.1 Low-Frequency, High-Gain Mode

In Low-frequency, high-gain mode, the oscillator uses a simple inverter-style amplifier. The gain is set to achieve rail-to-rail oscillation amplitudes.

The oscillator input buffer in this mode is single-ended. It provides low pass frequency filtering as well as hysteresis for voltage filtering and converts the output to logic levels. In this mode, the internal capacitors could be used.

30.9.2.2 Low-Frequency, Low-Power Mode

In low-frequency, low-power mode, the oscillator uses a gain control loop to minimize power consumption. As the oscillation amplitude increases, the amplifier current is reduced. This continues until a desired amplitude is achieved at steady-state. This mode provides low pass frequency filtering as well as hysteresis for voltage filtering and converts the output to logic levels. In this mode, the internal capacitors could be used, the internal feedback resistor is connected, and no external resistor should be used.

In this mode, the amplifier inputs, gain-control input, and input buffer input are all capacitively coupled for leakage tolerance (not sensitive to the DC level of EXTAL).

Also in this mode, all external components except for the resonator itself are integrated, which includes the load capacitors and feeback resistor that biases EXTAL.

30.9.2.3 High-Frequency, High-Gain Mode

In high-frequency, high-gain mode, the oscillator uses a simple inverter-style amplifier. The gain is set to achieve rail-to-rail oscillation amplitudes. This mode provides low pass frequency filtering as well as hysteresis for voltage filtering and converts the output to logic levels.

30.9.2.4 High-Frequency, Low-Power Mode

In high-frequency, low-power mode, the oscillator uses a gain control loop to minimize power consumption. As the oscillation amplitude increases, the amplifier current is reduced. This continues until a desired amplitude is achieved at steady-state. In this mode, no external resistor should be used.

The oscillator input buffer in this mode is differential. It provides low pass frequency filtering as well as hysteresis for voltage filtering and converts the output to logic levels.

30.9.3 Counter

The oscillator output clock (OSC_CLK_OUT) is gated off until the counter has detected 4096 cycles of its input clock (XTL_CLK). After 4096 cycles are completed, the counter passes XTL_CLK onto OSC_CLK_OUT. This counting timeout is used to guarantee output clock stability.

30.9.4 Reference clock pin requirements

The OSC module requires use of both the EXTAL and XTAL pins to generate an output clock in Oscillator mode, but requires only the EXTAL pin in External clock mode. The EXTAL and XTAL pins are available for I/O. For the implementation of these pins on this device, refer to the Signal Multiplexing chapter.

30.10 Reset

There is no reset state associated with the OSC module. The counter logic is reset when the OSC is not configured to generate clocks.

There are no sources of reset requests for the OSC module.

30.11 Low power modes operation

When the MCU enters Stop modes, the OSC is functional depending on CR[ERCLKEN] and CR[EREFSETN] bit settings. If both these bits are set, the OSC is in operation.

In Low Leakage Stop (LLS) modes, the OSC holds all register settings. If CR[ERCLKEN] and CR[EREFSTEN] are set before entry to Low Leakage Stop modes, the OSC is still functional in these modes. After waking up from Very Low Leakage Stop (VLLSx) modes, all OSC register bits are reset and initialization is required through software.

30.12 Interrupts

The OSC module does not generate any interrupts.

Chapter 31
RTC Oscillator (OSC32K)

31.1 Introduction

The RTC oscillator module provides the clock source for the RTC. The RTC oscillator module, in conjunction with an external crystal, generates a reference clock for the RTC.

31.1.1 Features and Modes

The key features of the RTC oscillator are as follows:

- Supports 32 kHz crystals with very low power
- Consists of internal feed back resistor
- Consists of internal programmable capacitors as the C_{load} of the oscillator
- Automatic Gain Control (AGC) to optimize power consumption

The RTC oscillator operations are described in detail in Functional Description .

31.1.2 Block Diagram

The following is the block diagram of the RTC oscillator.

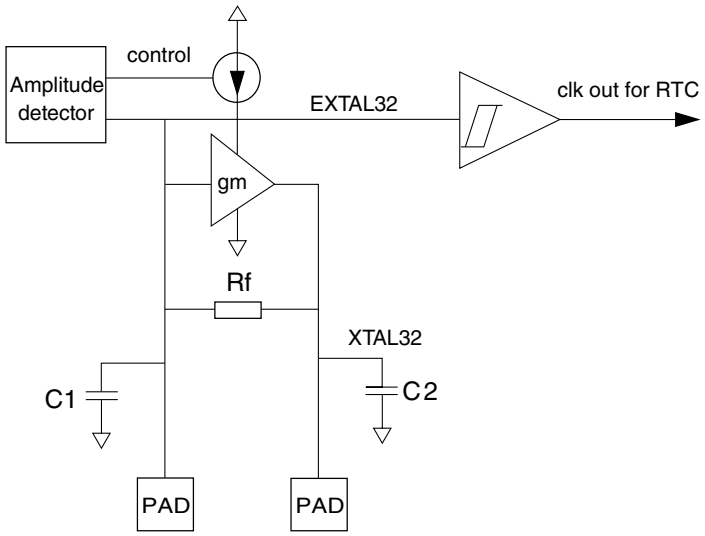


Figure 31-1. RTC Oscillator Block Diagram

31.2 RTC Signal Descriptions

The following table shows the user-accessible signals available for the RTC oscillator. See the chip-level specification to find out which signals are actually connected to the external pins.

Table 31-1. RTC Signal Descriptions

Signal	Description	I/O
EXTAL32	Oscillator Input	I
XTAL32	Oscillator Output	O

31.2.1 EXTAL32 — Oscillator Input

This signal is the analog input of the RTC oscillator.

31.2.2 XTAL32 — Oscillator Output

This signal is the analog output of the RTC oscillator module.

31.3 External Crystal Connections

The connections with a crystal is shown in the following figure. External load capacitors and feedback resistor are not required.

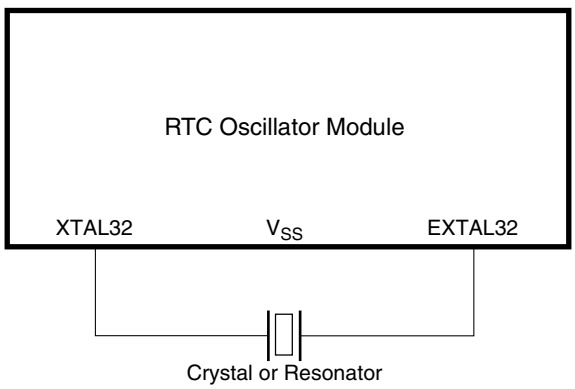


Figure 31-2. Crystal Connections

31.4 Memory Map/Register Descriptions

RTC oscillator control bits are part of the RTC registers. Refer to RTC Control Register (RTC_CR) , or RTC_GP_DATA_REG in the chip-specific information section, for more details.

31.5 Functional Description

As shown in Figure 31-1, the module includes an amplifier which supplies the negative resistor for the RTC oscillator. The gain of the amplifier is controlled by the amplitude detector, which optimizes the power consumption. A schmitt trigger is used to translate the sine-wave generated by this oscillator to a pulse clock out, which is a reference clock for the RTC digital core.

The oscillator includes an internal feedback resistor of approximately 100 MΩ between EXTAL32 and XTAL32.

In addition, there are two programmable capacitors with this oscillator, which can be used as the Cload of the oscillator. The programmable range is from 0pF to 30pF.

31.6 Reset Overview

There is no reset state associated with the RTC oscillator.

31.7 Interrupts

The RTC oscillator does not generate any interrupts.

Chapter 32
Local Memory Controller

32.1 Chip-specific LMEM information

32.1.1 Local memory controller region assignment

The following table shows the LMEM's region mode register assignment for each region field. It also shows the available cache modes for each region.

Table 32-1. Cache regions for devices with QSPI

Address range	Destination slave	Region number	Available cache modes
0x0000_0000–0x03FF_FFFF	Program flash and read-only data	R0	Write-through and non-cacheable [1]
0x0400_0000–0x07FF_FFFF	QSPI0 Alias	R0	Write-through and non-cacheable
0x0800_0000–0x0FFF_FFFF	DRAM Controller (Aliased Area)	R1	Write-through and non-cacheable
0x1000_0000–0x17FF_FFFF	Reserved	R2	Reserved
0x1800_0000–0x1BFF_FFFF	FlexBus (Aliased Area)	R3	Write-through and non-cacheable
0x1C00_0000–0x1DFF_FFFF	32kB BOOT ROM	-	Write-through (always)
0x1E00_0000–0x1FFF_FFFF	SRAM_L: Lower SRAM (ICODE/DCODE)	R4	Non-cacheable
0x2000_0000–0x200F_FFFF	SRAM_U: Upper SRAM	R5	Non-cacheable
0x6000_0000–0x66FF_FFFF	FlexBus (External Memory, Write-back)	R6	Write-back, write-through, and non-cacheable
0x6700_0000–0x677F_FFFF	QSPI0 Rx buffer	R6	Write-back, write-through, and non-cacheable
0x6780_0000–0x67FF_FFFF	Reserved	-	-

Table continues on the next page...

Table 32-1. Cache regions for devices with QSPI (continued)

Address range	Destination slave	Region number	Available cache modes
0x6800_0000–0x6FFF_FFFF	QSPI0	R6	Write-back, write-through, and non-cacheable
0x7000_0000–0x7FFF_FFFF	DRAM Controller	R7	Write-back, write-through, and non-cacheable
0x8000_0000–0x8FFF_FFFF	DRAM Controller - Write-through	R8	Write-through and non-cacheable
0x9000_0000–0x97FF_FFFF	Reserved	-	-
0x9800_0000–0x9FFF_FFFF	FlexBus (External memory - Write-through)	R9	Write-through and non-cacheable

1. Cache write hits do not write-through to program flash or FlexNVM regions because flash writes require flash programming.

32.2 Introduction

The Local Memory Controller provides the ARM®Cortex®-M4 processor with tightly-coupled processor-local memories and bus paths to all slave memory spaces.

32.2.1 Block Diagram

The Cortex-M4 processor has a modified 32-bit Harvard bus architecture. Using a 32-bit address space, low-order addresses (0x0000_0000 through 0x1FFF_FFFF) use the Processor Code (PC) bus, and high-order addresses (0x2000_0000 through 0xFFFF_FFFF) use the Processor System (PS) bus. As the bus names imply, normal operation has code accesses on the PC bus and data accesses on the PS bus.

This device has been augmented with tightly-coupled memories for the PC and PS buses. The memories include RAMs and caches. These local memories provide zero wait state access to RAM and cacheable address spaces.

The local memory controller includes four memory controllers and their attached memories:

- SRAM lower (SRAM_L) controller via the PC bus
- SRAM upper (SRAM_U) controller via the PS bus
- Cache memory controller via the PC bus
- Cache memory controller via the PS bus

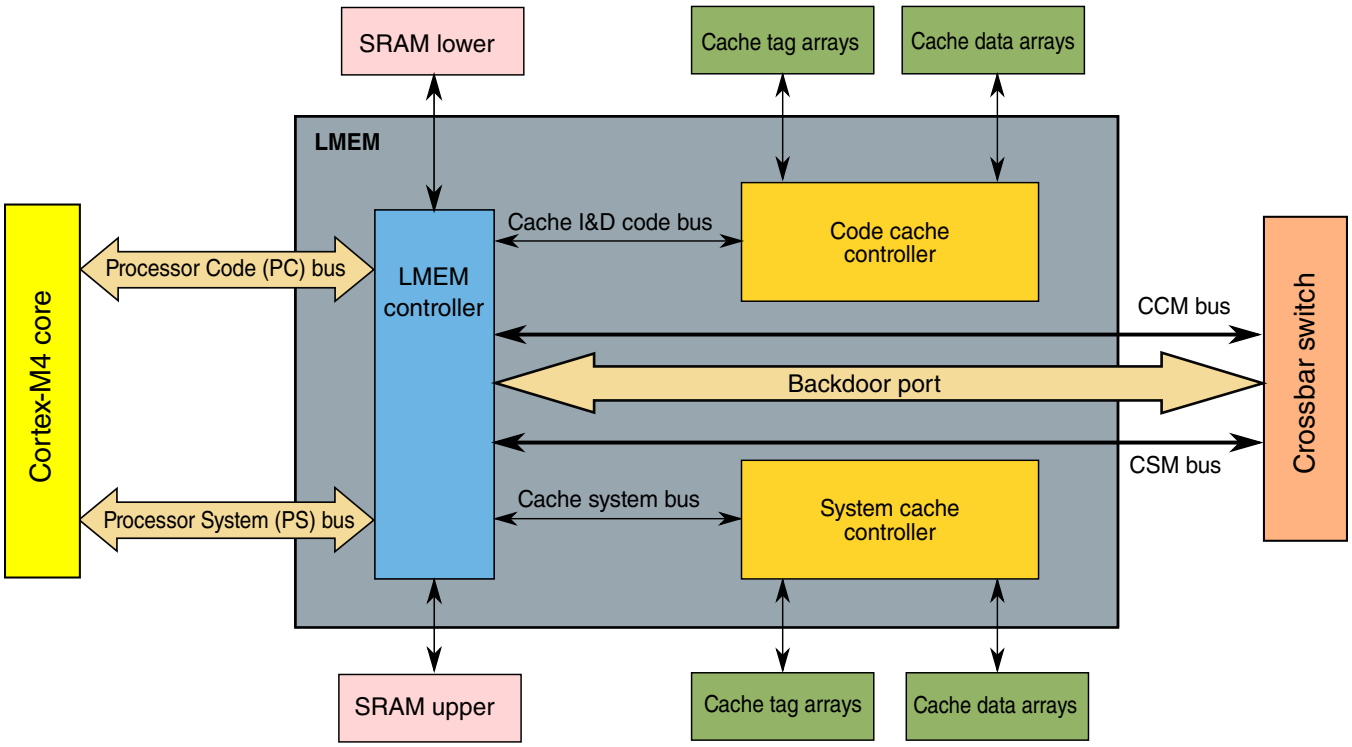


Figure 32-1. Local memory controller block diagram

NOTE

The SRAM and cache controllers reside within the LMEM, but the single-port synchronous RAM arrays used by these controllers are external.

The LMEM contains address decode logic for the PC and PS buses. This logic routes the core's accesses to the various system resources. The address spaces are device-specific and are specified in the device's Chip Configuration chapter.

32.2.2 Cache features

A cache is a block of high-speed memory locations containing address information (commonly known as a tag) and the associated data. The purpose is to decrease the average time of a memory access. Caches operate on two principles of locality:

- Spatial locality — An access to one location is likely to be followed by accesses from adjacent locations (for example, sequential instruction execution or usage of a data structure).
- Temporal locality — An access to an area of memory is likely to be repeated within a short time period (for example, execution of a code loop).

To minimize the quantity of control information stored, the spatial locality property is used to group several locations together under the same tag. This logical block is commonly known as a cache line.

When data is loaded into a cache, access times for subsequent loads and stores are reduced, resulting in overall performance benefits. An access to information already in a cache is known as a cache hit, and other accesses are called cache misses.

Normally, caches are self-managing, with the updates occurring automatically. Whenever the processor wants to access a cacheable location, the cache is checked. If the access is a cache hit, the access occurs immediately. Otherwise, a location is allocated and the cache line is loaded from memory. Different cache topologies and access policies are possible. However, they must comply with the memory coherency model of the underlying architecture.

Caches introduce a number of potential problems, mainly because of:

- memory accesses occurring at times other than when the programmer would normally expect them,
- the existence of multiple physical locations where a data item can be held.

The local memory controller supports three modes of operation:

1. Write-through — access to address spaces with this cache mode are cacheable.
   - A write-through read miss on the input bus causes a line read on the output bus of a 16-byte-aligned memory address containing the desired address. This miss data is loaded into the cache and is marked as valid and not modified.
   - A write-through read hit to a valid cache location returns data from the cache with no output bus access.
   - A write-through write miss bypasses the cache and writes to the output bus (no allocate on write miss policy for write-through mode spaces).
   - A write-through write hit updates the cache hit data and writes to the output bus.
2. Write-back — access to address spaces with this cache mode are cacheable.
   - A write-back read miss on the input bus will cause a line read on the output bus of a 16-byte-aligned memory address containing the desired address. This miss data is loaded into the cache and marked as valid and not modified.
   - A write-back read hit to a valid cache location will return data from the cache with no output bus access.
   - A write-back write miss will do a "read-to-write" (allocate on write miss policy for write-back mode spaces). A line read on the output bus of a 16 byte aligned memory address containing the desired write address is performed. This miss data is loaded into the cache and marked as valid and modified; and the write data will then update the appropriate cache data locations.

3. Non-cacheable — access to address spaces with this cache mode are not cacheable. These accesses bypass the cache and access the output bus.

32.3 Memory Map/Register Definition

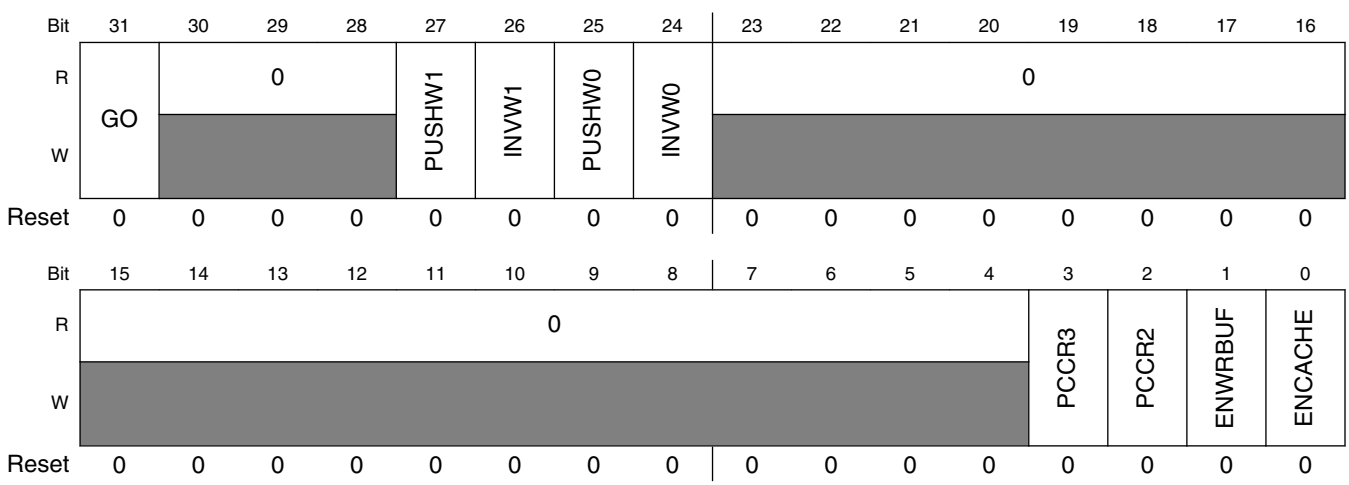
The cache programmer's model provides a variety of registers for configuring and controlling the cache, as well as indirect access paths to all cache tag and data storage.

LMEM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
E008_2000	Cache control register (LMEM_PCCCR)	32	R/W	0000_0000h	32.3.1/739
E008_2004	Cache line control register (LMEM_PCCLCR)	32	R/W	0000_0000h	32.3.2/741
E008_2008	Cache search address register (LMEM_PCCSAR)	32	R/W	0000_0000h	32.3.3/743
E008_200C	Cache read/write value register (LMEM_PCCCVR)	32	R/W	0000_0000h	32.3.4/744
E008_2020	Cache regions mode register (LMEM_PCCRMR)	32	R/W	AA0F_A000h	32.3.5/744
E008_2800	Cache control register (LMEM_PSCCR)	32	R/W	0000_0000h	32.3.6/748
E008_2804	Cache line control register (LMEM_PSCLCR)	32	R/W	0000_0000h	32.3.7/749
E008_2808	Cache search address register (LMEM_PSCSAR)	32	R/W	0000_0000h	32.3.8/752
E008_280C	Cache read/write value register (LMEM_PSCCVR)	32	R/W	0000_0000h	32.3.9/753
E008_2820	Cache regions mode register (LMEM_PSCRMR)	32	R/W	AA0F_A000h	32.3.10/ 753

32.3.1 Cache control register (LMEM_PCCCR)

Address: E008_2000h base + 0h offset = E008_2000h



LMEM_PCCCR field descriptions

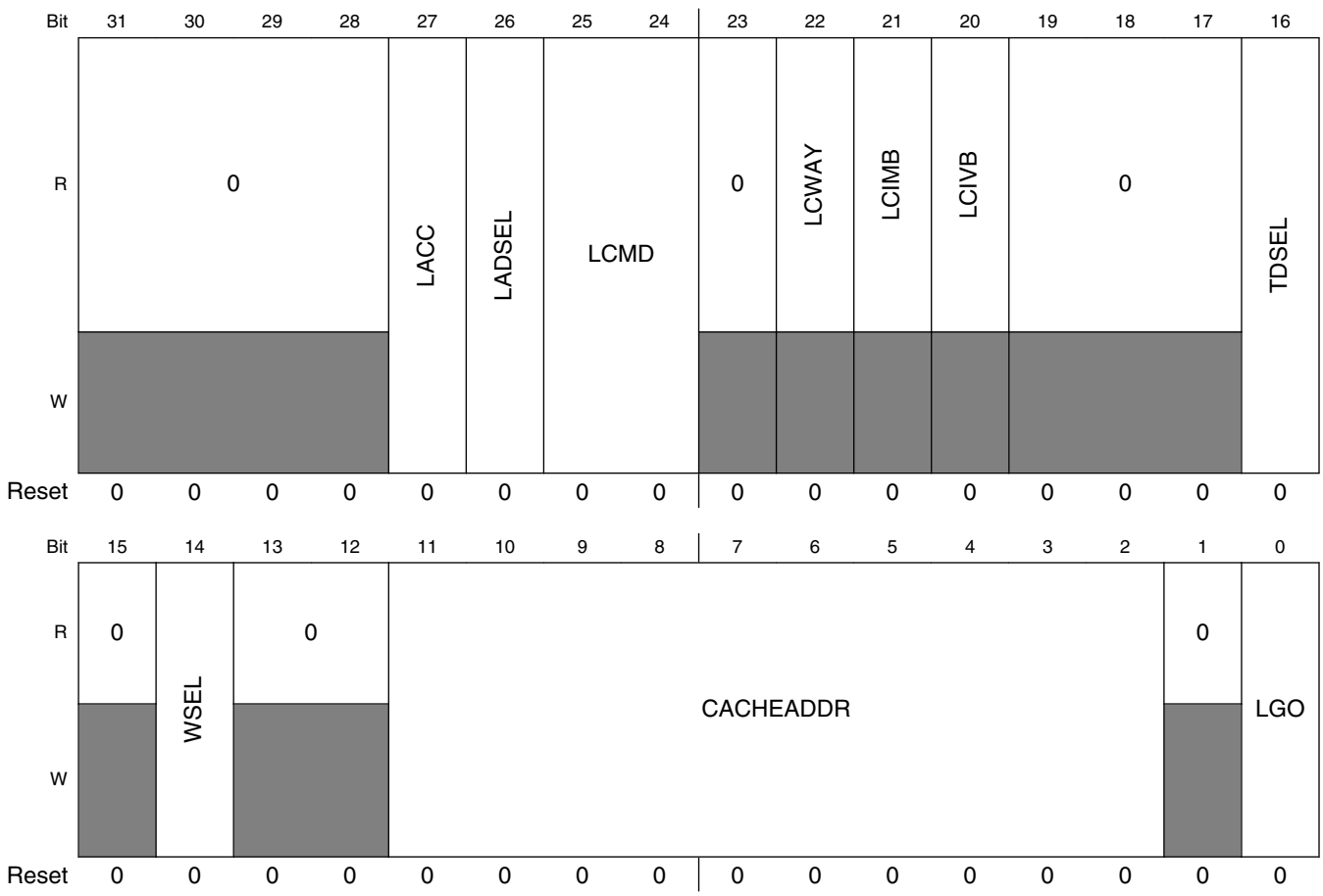
Field	Description
31 GO	Initiate Cache Command Setting this bit initiates the cache command indicated by bits 27-24. Reading this bit indicates if a command is active **NOTE:** This bit stays set until the command completes. Writing zero has no effect. 0 Write: no effect. Read: no cache command active. 1 Write: initiate command indicated by bits 27-24. Read: cache command active.
30–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27 PUSHW1	Push Way 1 0 No operation 1 When setting the GO bit, push all modified lines in way 1
26 INVW1	Invalidate Way 1 **NOTE:** If the PUSHW1 and INVW1 bits are set, then after setting the GO bit, push all modified lines in way 1 and invalidate all lines in way 1 (clear way 1). 0 No operation 1 When setting the GO bit, invalidate all lines in way 1
25 PUSHW0	Push Way 0 0 No operation 1 When setting the GO bit, push all modified lines in way 0
24 INVW0	Invalidate Way 0 **NOTE:** If the PUSHW0 and INVW0 bits are set, then after setting the GO bit, push all modified lines in way 0 and invalidate all lines in way 0 (clear way 0). 0 No operation 1 When setting the GO bit, invalidate all lines in way 0.
23–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 PCCR3	Forces no allocation on cache misses (must also have PCCR2 asserted)
2 PCCR2	Forces all cacheable spaces to write through
1 ENWRBUF	Enable Write Buffer 0 Write buffer disabled 1 Write buffer enabled
0 ENCACHE	Cache enable 0 Cache disabled 1 Cache enabled

32.3.2 Cache line control register (LMEM_PCCLCR)

This register defines specific line-sized cache operations to be performed using a specific cache line address or a physical address.

If a physical address is specified, both ways of the cache are searched, and the command is only performed on the way which hits.

Address: E008_2000h base + 4h offset = E008_2004h



LMEM_PCCLCR field descriptions

Field	Description
31–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27 LACC	Line access type 0 Read 1 Write
26 LADSEL	Line Address Select When using the cache address, the way must also be specified in CLCR[WSEL].

Table continues on the next page...

LMEM_PCCLCR field descriptions (continued)

Field	Description
	When using the physical address, both ways are searched and the command is performed only if a hit. 0 Cache address 1 Physical address
25–24 LCMD	Line Command 00 Search and read or write 01 Invalidate 10 Push 11 Clear
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 LCWAY	Line Command Way Indicates the way used by the line command.
21 LCIMB	Line Command Initial Modified Bit If command used cache address and way, then this bit shows the initial state of the modified bit If command used physical address and a hit, then this bit shows the initial state of the modified bit. If a miss, this bit reads zero.
20 LCIVB	Line Command Initial Valid Bit If command used cache address and way, then this bit shows the initial state of the valid bit If command used physical address and a hit, then this bit shows the initial state of the valid bit. If a miss, this bit reads zero.
19–17 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
16 TDSEL	Tag/Data Select Selects tag or data for search and read or write commands. 0 Data 1 Tag
15 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
14 WSEL	Way select Selects the way for line commands. 0 Way 0 1 Way 1
13–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11–2 CACHEADDR	Cache address CLCR[11:4] bits are used to access the tag arrays CLCR[11:2] bits are used to access the data arrays
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

LMEM_PCCLCR field descriptions (continued)

Field	Description
0 LGO	Initiate Cache Line Command Setting this bit initiates the cache line command indicated by bits 27-24. Reading this bit indicates if a line command is active **NOTE:** This bit stays set until the command completes. Writing zero has no effect. **NOTE:** This bit is shared with CSAR[LGO] 0 Write: no effect. Read: no line command active. 1 Write: initiate line command indicated by bits 27-24. Read: line command active.

32.3.3 Cache search address register (LMEM_PCCSAR)

The CSAR register is used to define the explicit cache address or the physical address for line-sized commands specified in the CLCR[LADSEL] bit.

Address: E008_2000h base + 8h offset = E008_2008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PHYADDR															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PHYADDR														0	LGO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LMEM_PCCSAR field descriptions

Field	Description
31–2 PHYADDR	Physical Address PHYADDR represents bits [31:2] of the system address. CSAR[31:12] bits are used for tag compare CSAR[11:4] bits are used to access the tag arrays CSAR[11:2] bits are used to access the data arrays
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 LGO	Initiate Cache Line Command Setting this bit initiates the cache line command indicated by bits 27-24. Reading this bit indicates if a line command is active **NOTE:** This bit stays set until the command completes. Writing zero has no effect. **NOTE:** This bit is shared with CLCR[LGO]

Table continues on the next page...

LMEM_PCCSAR field descriptions (continued)

Field	Description
	0 Write: no effect. Read: no line command active. 1 Write: initiate line command indicated by bits CLCR[27:24]. Read: line command active.

32.3.4 Cache read/write value register (LMEM_PCCCVR)

The CCVR register is used to source write data or return read data for the commands specified in the CLCR register.

Address: E008_2000h base + Ch offset = E008_200Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	DATA																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LMEM_PCCCVR field descriptions

Field	Description
DATA	Cache read/write Data For tag search, read or write: • CCVR[31:12] bits are used for tag array R/W value • CCVR[11:4] bits are used for tag set address on reads; unused on writes • CCVR[3:2] bits are reserved For data search, read or write: • CCVR[31:0] bits are used for data array R/W value

32.3.5 Cache regions mode register (LMEM_PCCRMR)

The CRMR register allows you to demote the cache mode of various subregions within the device's memory map. Demoting the cache mode reduces the cache function applied to a memory region from write-back to write-through to non-cacheable. After a region is demoted, its cache mode can only be raised by a reset, which returns it to its default state.

To maintain cache coherency, changes to the cache mode should be completed while the address space being changed is not being accessed or the cache is disabled. Before a cache mode change, complete a cache clear all command to push and invalidate any cache entries that may have changed.

NOTE

The address/module assignment of the 16 subregions is device-specific and are detailed in the Chip Configuration section. Some of the regions may not be used (non-cacheable), and some regions may not be capable of write-back.

Address: E008_2000h base + 20h offset = E008_2020h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	R0		R1		R2		R3		R4		R5		R6		R7		R8		R9		R10		R11		R12		R13		R14		R15	
Reset	1	0	1	0	1	0	1	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

LMEM_PCCRMR field descriptions

Field	Description
31–30 R0	Region 0 mode Controls the cache mode for region 0 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
29–28 R1	Region 1 mode Controls the cache mode for region 1 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
27–26 R2	Region 2 mode Controls the cache mode for region 2 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
25–24 R3	Region 3 mode Controls the cache mode for region 3 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
23–22 R4	Region 4 mode Controls the cache mode for region 4 00 Non-cacheable 01 Non-cacheable

Table continues on the next page...

LMEM_PCCRMR field descriptions (continued)

Field	Description
	10 Write-through 11 Write-back
21–20 R5	Region 5 mode Controls the cache mode for region 5 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
19–18 R6	Region 6 mode Controls the cache mode for region 6 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
17–16 R7	Region 7 mode Controls the cache mode for region 7 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
15–14 R8	Region 8 mode Controls the cache mode for region 8 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
13–12 R9	Region 9 mode Controls the cache mode for region 9 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
11–10 R10	Region 10 mode Controls the cache mode for region 10 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back

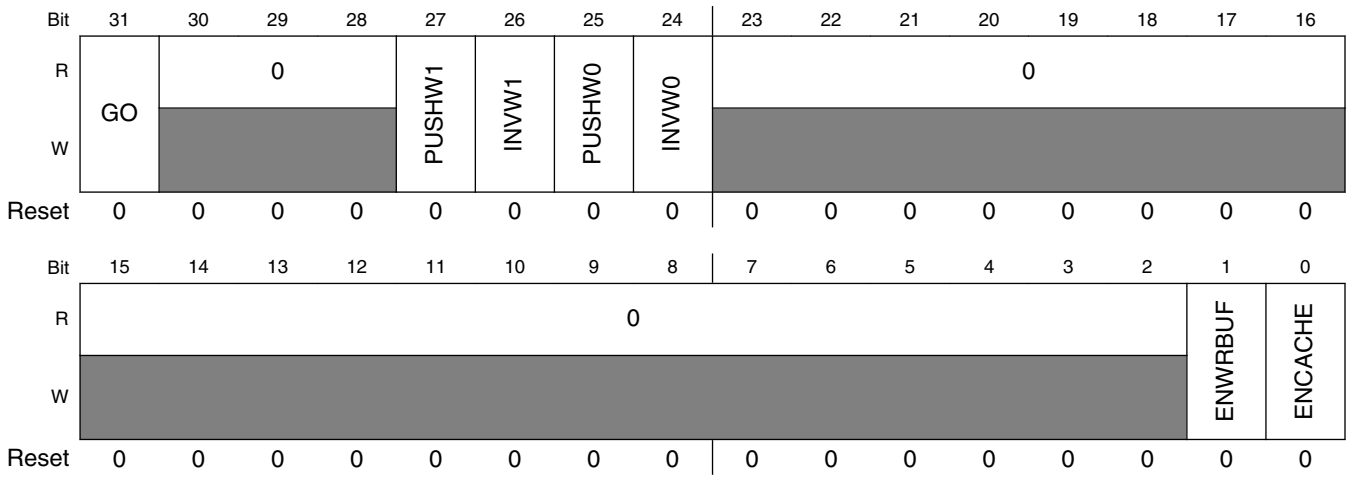
Table continues on the next page...

LMEM_PCCRMR field descriptions (continued)

Field	Description
9–8 R11	Region 11 mode Controls the cache mode for region 11 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
7–6 R12	Region 12 mode Controls the cache mode for region 12 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
5–4 R13	Region 13 mode Controls the cache mode for region 13 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
3–2 R14	Region 14 mode Controls the cache mode for region 14 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
R15	Region 15 mode Controls the cache mode for region 15 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back

32.3.6 Cache control register (LMEM_PSCCR)

Address: E008_2000h base + 800h offset = E008_2800h



LMEM_PSCCR field descriptions

Field	Description
31 GO	Initiate Cache Command Setting this bit initiates the cache command indicated by bits 27-24. Reading this bit indicates if a command is active **NOTE:** This bit stays set until the command completes. Writing zero has no effect. 0 Write: no effect. Read: no cache command active. 1 Write: initiate command indicated by bits 27-24. Read: cache command active.
30–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27 PUSHW1	Push Way 1 0 No operation 1 When setting the GO bit, push all modified lines in way 1
26 INVW1	Invalidate Way 1 **NOTE:** If the PUSHW1 and INVW1 bits are set, then after setting the GO bit, push all modified lines in way 1 and invalidate all lines in way 1 (clear way 1). 0 No operation 1 When setting the GO bit, invalidate all lines in way 1
25 PUSHW0	Push Way 0 0 No operation 1 When setting the GO bit, push all modified lines in way 0
24 INVW0	Invalidate Way 0

Table continues on the next page...

LMEM_PSCCR field descriptions (continued)

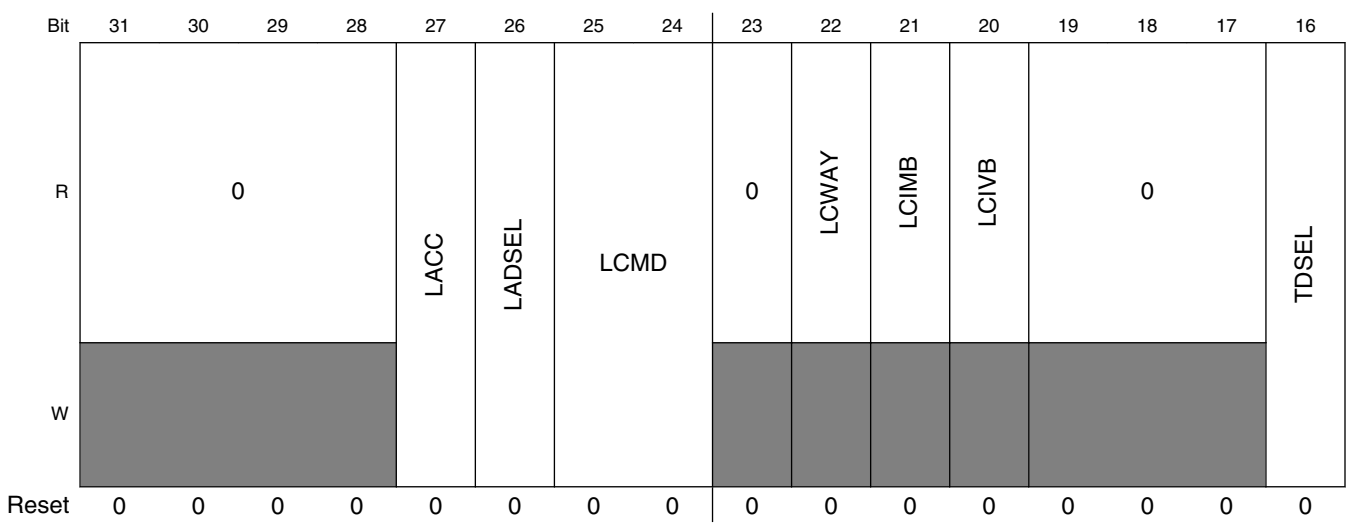
Field	Description
	NOTE: If the PUSHW0 and INVW0 bits are set, then after setting the GO bit, push all modified lines in way 0 and invalidate all lines in way 0 (clear way 0). 0 No operation 1 When setting the GO bit, invalidate all lines in way 0.
23–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 ENWRBUF	Enable Write Buffer 0 Write buffer disabled 1 Write buffer enabled
0 ENCACHE	Cache enable 0 Cache disabled 1 Cache enabled

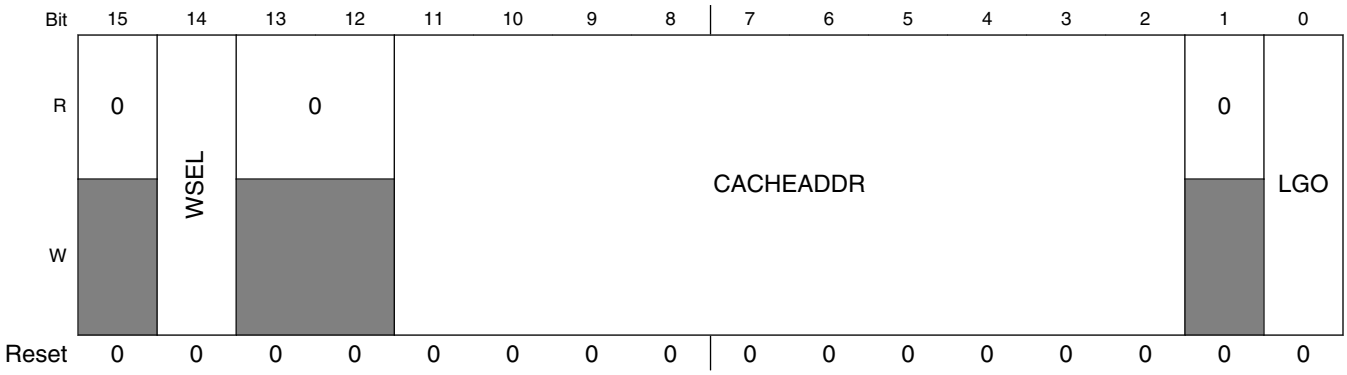
32.3.7 Cache line control register (LMEM_PSCLCR)

This register defines specific line-sized cache operations to be performed using a specific cache line address or a physical address.

If a physical address is specified, both ways of the cache are searched, and the command is only performed on the way which hits.

Address: E008_2000h base + 804h offset = E008_2804h





LMEM_PSCLCR field descriptions

Field	Description
31–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27 LACC	Line access type 0 Read 1 Write
26 LADSEL	Line Address Select When using the cache address, the way must also be specified in CLCR[WSEL]. When using the physical address, both ways are searched and the command is performed only if a hit. 0 Cache address 1 Physical address
25–24 LCMD	Line Command 00 Search and read or write 01 Invalidate 10 Push 11 Clear
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 LCWAY	Line Command Way Indicates the way used by the line command.
21 LCIMB	Line Command Initial Modified Bit If command used cache address and way, then this bit shows the initial state of the modified bit If command used physical address and a hit, then this bit shows the initial state of the modified bit. If a miss, this bit reads zero.
20 LCIVB	Line Command Initial Valid Bit If command used cache address and way, then this bit shows the initial state of the valid bit If command used physical address and a hit, then this bit shows the initial state of the valid bit. If a miss, this bit reads zero.
19–17 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

LMEM_PSCLCR field descriptions (continued)

Field	Description
16 TDSEL	Tag/Data Select Selects tag or data for search and read or write commands. 0 Data 1 Tag
15 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
14 WSEL	Way select Selects the way for line commands. 0 Way 0 1 Way 1
13–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11–2 CACHEADDR	Cache address CLCR[11:4] bits are used to access the tag arrays CLCR[11:2] bits are used to access the data arrays
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 LGO	Initiate Cache Line Command Setting this bit initiates the cache line command indicated by bits 27-24. Reading this bit indicates if a line command is active **NOTE:** This bit stays set until the command completes. Writing zero has no effect. **NOTE:** This bit is shared with CSAR[LGO] 0 Write: no effect. Read: no line command active. 1 Write: initiate line command indicated by bits 27-24. Read: line command active.

32.3.8 Cache search address register (LMEM_PSCSAR)

The CSAR register is used to define the explicit cache address or the physical address for line-sized commands specified in the CLCR[LADSEL] bit.

Address: E008_2000h base + 808h offset = E008_2808h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PHYADDR															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PHYADDR														0	LGO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LMEM_PSCSAR field descriptions

Field	Description
31–2 PHYADDR	Physical Address PHYADDR represents bits [31:2] of the system address. CSAR[31:12] bits are used for tag compare CSAR[11:4] bits are used to access the tag arrays CSAR[11:2] bits are used to access the data arrays
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 LGO	Initiate Cache Line Command Setting this bit initiates the cache line command indicated by bits 27-24. Reading this bit indicates if a line command is active **NOTE:** This bit stays set until the command completes. Writing zero has no effect. **NOTE:** This bit is shared with CLCR[LGO] 0 Write: no effect. Read: no line command active. 1 Write: initiate line command indicated by bits CLCR[27:24]. Read: line command active.

32.3.9 Cache read/write value register (LMEM_PSCCVR)

The CCVR register is used to source write data or return read data for the commands specified in the CLCR register.

Address: E008_2000h base + 80Ch offset = E008_280Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	DATA																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LMEM_PSCCVR field descriptions

Field	Description
DATA	Cache read/write Data For tag search, read or write: • CCVR[31:12] bits are used for tag array R/W value • CCVR[11:4] bits are used for tag set address on reads; unused on writes • CCVR[3:2] bits are reserved For data search, read or write: • CCVR[31:0] bits are used for data array R/W value

32.3.10 Cache regions mode register (LMEM_PSCRMR)

The CRMR register allows you to demote the cache mode of various subregions within the device's memory map. Demoting the cache mode reduces the cache function applied to a memory region from write-back to write-through to non-cacheable. After a region is demoted, its cache mode can only be raised by a reset, which returns it to its default state.

To maintain cache coherency, changes to the cache mode should be completed while the address space being changed is not being accessed or the cache is disabled. Before a cache mode change, complete a cache clear all command to push and invalidate any cache entries that may have changed.

NOTE

The address/module assignment of the 16 subregions is device-specific and are detailed in the Chip Configuration section. Some of the regions may not be used (non-cacheable), and some regions may not be capable of write-back.

Address: E008_2000h base + 820h offset = E008_2820h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	R0		R1		R2		R3		R4		R5		R6		R7		R8		R9		R10		R11		R12		R13		R14		R15	
Reset	1	0	1	0	1	0	1	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

LMEM_PSCRMR field descriptions

Field	Description
31–30 R0	Region 0 mode Controls the cache mode for region 0 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
29–28 R1	Region 1 mode Controls the cache mode for region 1 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
27–26 R2	Region 2 mode Controls the cache mode for region 2 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
25–24 R3	Region 3 mode Controls the cache mode for region 3 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
23–22 R4	Region 4 mode Controls the cache mode for region 4 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
21–20 R5	Region 5 mode Controls the cache mode for region 5 00 Non-cacheable 01 Non-cacheable

Table continues on the next page...

LMEM_PSCRMR field descriptions (continued)

Field	Description
	10 Write-through 11 Write-back
19–18 R6	Region 6 mode Controls the cache mode for region 6 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
17–16 R7	Region 7 mode Controls the cache mode for region 7 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
15–14 R8	Region 8 mode Controls the cache mode for region 8 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
13–12 R9	Region 9 mode Controls the cache mode for region 9 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
11–10 R10	Region 10 mode Controls the cache mode for region 10 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
9–8 R11	Region 11 mode Controls the cache mode for region 11 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back

Table continues on the next page...

LMEM_PSCRMR field descriptions (continued)

Field	Description
7–6 R12	Region 12 mode Controls the cache mode for region 12 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
5–4 R13	Region 13 mode Controls the cache mode for region 13 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
3–2 R14	Region 14 mode Controls the cache mode for region 14 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back
R15	Region 15 mode Controls the cache mode for region 15 00 Non-cacheable 01 Non-cacheable 10 Write-through 11 Write-back

32.4 Functional Description

32.4.1 LMEM Function

The Local Memory Controller receives the following requests:

- Core master bus requests on the Processor Code (PC) bus,
- Core master bus requests on the Processor Space (PS) bus, and
- SRAM controller requests from all other bus masters on the backdoor port.

The Local Memory Controller address decode logic routes these accesses and also provides any crossbar switch slave target logic. Finally, the Local Memory controller provides the needed MPU connections for checking all SRAM controller and cacheable accesses.

The programming model for the Code and System Caches is accessed via the core's Private Peripheral Bus (PPB).

32.4.1.1 Processor Code accesses

Processor Code accesses are routed to the SRAM_L if they are mapped to that space. All other PC accesses are routed to the Code Cache Memory Controller. This controller then processes the cacheable accesses as needed, while bypassing the non-cacheable, cache write-through, cache miss, and cache maintenance accesses to the CCM bus and the crossbar switch using the Master0 port.

32.4.1.2 Processor System accesses

Processor Space accesses are routed to the SRAM_U if they are mapped to that space. All other PS accesses are routed to the PS Cache Memory Controller. This controller then processes the cacheable accesses as needed, while bypassing the non-cacheable, cache write-through, cache miss, and cache maintenance accesses to the CCM bus and the crossbar switch using the Master1 port.

32.4.1.3 Backdoor port accesses

All LMEM backdoor port accesses are for the SRAM controller. These accesses go to the SRAM_L or the SRAM_U depending on their specific address.

32.4.2 SRAM Function

32.4.2.1 SRAM Configuration

SRAM Configuration shows how the SRAM controller is configured.

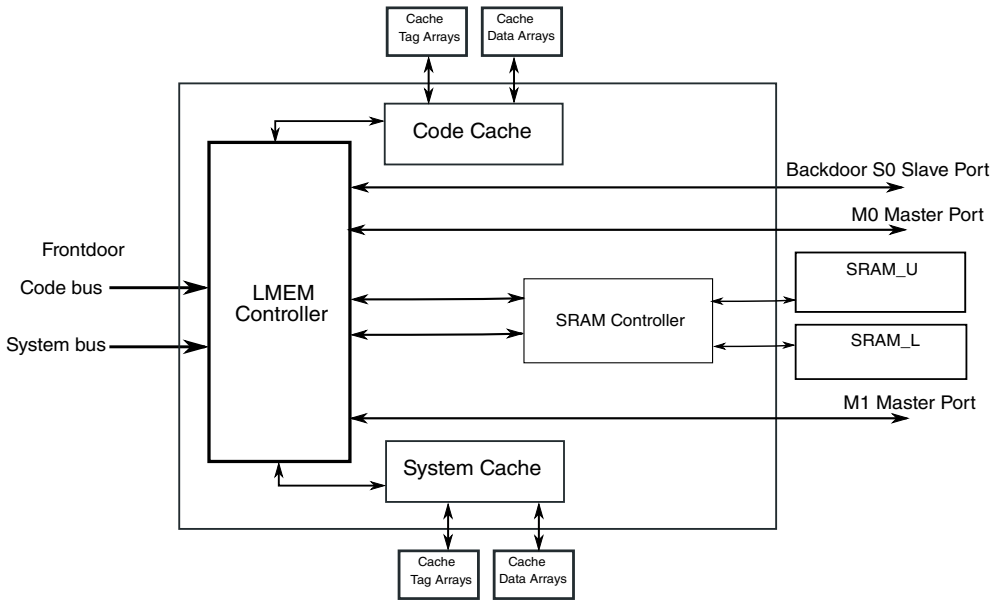


Figure 32-2. SRAM configuration

32.4.2.2 SRAM Arrays

The on-chip SRAM is split into two logical arrays, SRAM_L and SRAM_U.

The on-chip SRAM is implemented so the SRAM_L and SRAM_U ranges form a contiguous block in the memory map. As such:

- SRAM_L is anchored at address 0x2000_0000 and occupies the space below this address, that is, addresses < 0x2000_0000
- SRAM_U is anchored at address 0x2000_0000 and occupies the space at and above this beginning address, that is, addresses ≥ 0x2000_0000.

From equal-sized memories, valid address ranges for SRAM_L and SRAM_U are then defined as:

- SRAM_L = [0x2000_0000–(SRAM_size/4)] to 0x1FFF_FFFF
- SRAM_U = 0x2000_0000 to [0x2000_0000 + (3 x SRAM_size/4) - 1]

This is illustrated in Figure 32-3.

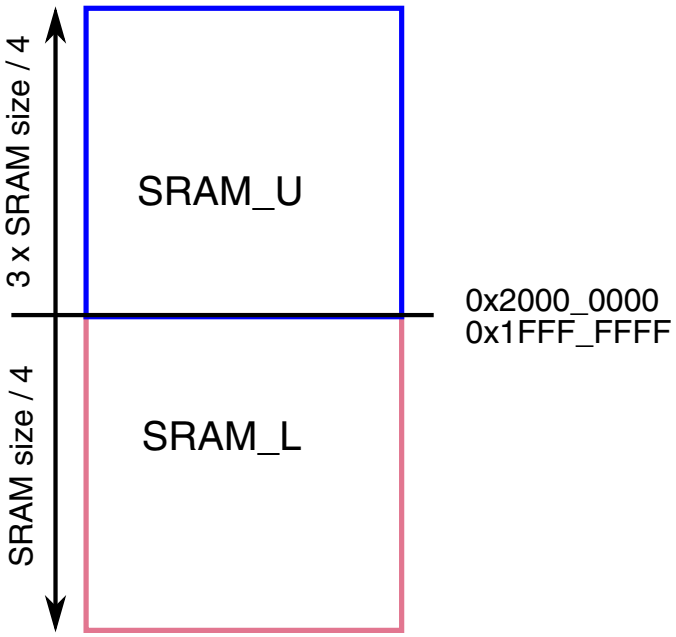


Figure 32-3. SRAM Arrays

For example, for a device containing 64 KB of SRAM the ranges are:

- SRAM_L: 0x1FFF_8000 – 0x1FFF_FFFF
- SRAM_U: 0x2000_0000 – 0x2000_7FFF

32.4.2.3 SRAM accesses

The SRAM is split into two logical arrays that are 32-bits wide:

- SRAM_L — Accessible by the code bus of the Cortex-M4 core and by the backdoor port.
- SRAM_U — Accessible by the system bus of the Cortex-M4 core and by the backdoor port.

The backdoor port makes the SRAM accessible to the non-core bus masters (such as DMA).

Figure 32-4 illustrates the SRAM accesses within the device.

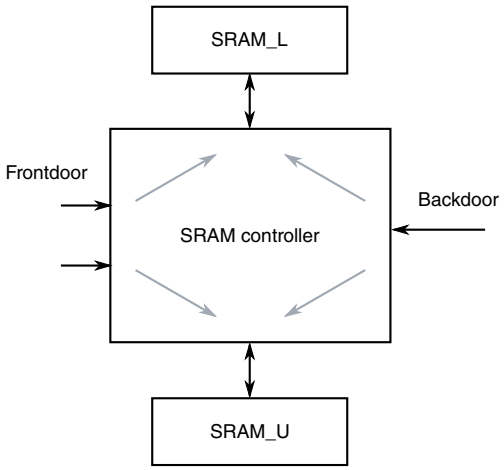


Figure 32-4. SRAM access diagram

The following simultaneous accesses can be made to different logical halves of the SRAM:

- Core code and core system
- Core code and non-core master
- Core system and non-core master

NOTE

Two non-core masters cannot access SRAM simultaneously. The required arbitration and serialization is provided by the crossbar switch. The SRAM_{L,U} arbitration is controlled by the SRAM controller based on the configuration bits in the MCM module.

NOTE

Burst-access cannot occur across the 0x2000_0000 boundary that separates the two SRAM arrays. The two arrays should be treated as separate memory ranges for burst accesses.

32.4.3 Cache Function

The caches on this device are structured as follows. Both caches have a 2-way set-associative cache structure with a total size of 8 KB. The caches have 32-bit address and data paths and a 16-byte line size. The cache tags and data storage use single-port, synchronous RAMs.

For these 8 KB caches, each cache TAG function uses two 256 x 22-bit RAM arrays and the cache DATA function uses two 1024 x 32-bit RAM arrays. The cache TAG entries store 20 bits of upper address as well as a modified and valid bit per cache line. The cache DATA entries store four bytes of code or data.

All normal cache accesses use physical addresses. This leads to the following cache address use:

CACHE - 8 KB size = (256 sets) x (16-byte lines) x (2-way set-associative)

TAG:

- address[31:12] used in tag for compare (hit) logic
- address[11:4] used to select 1 of 256 sets
- address[3:0] not used

DATA

- address[31:12] not used
- address[11:4] used to select one of 256 sets
- address[3:2] used to select one of four 32-bit words within a set
- address[1:0] used to select the byte within the 32-bit word

32.4.4 Cache Control

The Code and System Caches are disabled at reset. Cache tag and data arrays are not cleared at reset. Therefore, to enable the caches, cache commands must be done to clear and initialize the required tag array bits and to configure and enable the caches.

32.4.4.1 Cache set commands

The cache set commands may operate on:

- all of way 0,
- all of way 1, or
- all of both ways (complete cache).

Cache set commands are initiated using the upper bits in the CCR register. Cache set commands perform their operation on the cache independent of the cache enable bit, CCR[ENCACHE].

A cache set command is initiated by setting the CCR[GO] bit. This bit also acts as a busy bit for set commands. It stays set while the command is active and is cleared by the hardware when the set command completes.

Supported cache set commands are given in Table 32-2. Set commands work as follows:

- Invalidate – Unconditionally clear valid and modify bits of a cache entry.
- Push – Push a cache entry if it is valid and modified, then clear the modify bit. If entry not valid or not modified, leave as is.
- Clear – Push a cache entry if it is valid and modified, then clear the valid and modify bits. If entry not valid or not modified, clear the valid bit.

Table 32-2. Cache Set Commands

CCR[27:24]				Command
PUSHW1	INVW1	PUSHW0	INVW0	
0	0	0	0	NOP
0	0	0	1	Invalidate all way 0
0	0	1	0	Push all way 0
0	0	1	1	Clear all way 0
0	1	0	0	Invalidate all way 1
0	1	0	1	Invalidate all way 1; invalidate all way 0 (invalidate cache)
0	1	1	0	Invalidate all way 1; push all way 0
0	1	1	1	Invalidate all way 1; clear all way 0
1	0	0	0	Push all way 1
1	0	0	1	Push all way 1; invalidate all way 0
1	0	1	0	Push all way 1; push all way 0 (push cache)
1	0	1	1	Push all way 1; clear all way 0
1	1	0	0	Clear all way 1
1	1	0	1	Clear all way 1; invalidate all way 0
1	1	1	0	Clear all way 1; push all way 0
1	1	1	1	Clear all way 1; clear all way 0 (clear cache)

After a reset, complete an invalidate cache command before using the cache. It is possible to combine the cache invalidate command with the cache enable. That is, setting CCR to 0x8500_0003 will invalidate the cache and enable the cache and write buffer.

32.4.4.2 Cache line commands

Cache line commands operate on a single line in the cache at a time. Cache line commands can be performed using a physical or cache address.

- A cache address consists of a set address and a way select. The line command acts on the specified cache line.
- Cache line commands with physical addresses first search both ways of the cache set specified by bits [11:4] of the physical address. If they hit, the commands perform their action on the hit way.

Cache line commands are specified using the upper bits in the CLCR register. Cache line commands perform their operation on the cache independent of the cache enable bit (CCR[ENCACHE]). Using a cache address, the command can be completely specified using the CLCR register. Using a physical address, the command must also use the CSAR register to specify the physical address.

A line cache command is initiated by setting the line command go bit (CLCR[LGO] or CSAR[LGO]). This bit also acts a a busy bit for line commands. It stays set while the command is active and is cleared by the hardware when the command completes.

The CLCR[27:24] bits select the line command as follows:

Table 32-3. Cache Line Commands

CLCR[27:24]			Command
LACC	LADSEL	LCMD	
0	0	00	Search by cache address and way
0	0	01	Invalidate by cache address and way
0	0	10	Push by cache address and way
0	0	11	Clear by cache address and way
0	1	00	Search by physical address
0	1	01	Invalidate by physical address
0	1	10	Push by physical address
0	1	11	Clear by physical address
1	0	00	Write by cache address and way
1	0	01	Reserved, NOP
1	0	10	Reserved, NOP
1	0	11	Reserved, NOP
1	1	*xx*	Reserved, NOP

32.4.4.2.1 Executing a series of line commands using cache addresses

A series of line commands with incremental cache addresses can be performed by just writing to the CLCR.

- Place the command in CLCR[27:24],
- Set the way (CLCR[WSEL]) and tag/data (CLCR[TDSEL]) controls as needed,

- Place the cache address in CLCR[CACHEADDR], and
- Set the line command go bit (CLCR[LGO]).

When one line command completes, initiate the next command by following these steps:

- Increment the cache address (at bit 2 to step through data or at bit 4 to step through lines), and
- Set the line command go bit (CLCR[LGO]).

32.4.4.2.2 Executing a series of line commands using physical addresses

Perform a series of line commands with incremental physical addresses using the following steps:

- Write to the CLCR.
  - Place the command in CLCR[27:24]
  - Set the tag/data (CLCR[TDSEL]) control
- Place the physical address in CSAR[PHYADDR] and set the line command go bit (CSAR[LGO]).

When one line command completes, initiate the next command by following these steps:

- Increment the physical address (at bit 2 to step through data or at bit 4 to step through lines), and
- Set the line command go bit (CSAR[LGO]).

The line command go bit is shared between the CLCR and CSAR registers, so that the above steps can be completed in a single write to the CSAR register.

32.4.4.2.3 Line command results

At completion of a line command, the CLCR register contains information on the initial state of the line targeted by the command. For line commands with cache addresses, this information is read before the line command action is performed from the targeted cache line. For line commands with physical addresses, this information is read on a hit before the line command action is performed from the hit cache line or has initial valid bit cleared if the command misses. In general, if the valid indicator (CLCR[LCIVB] is cleared, the targeted line was invalid at the start of the line command and no line operation was performed.

Table 32-4. Line command results

CLCR[22:20]			For cache address commands	For physical address commands
LCWAY	LCIMB	LCIVB		
0	0	0	Way 0 line was invalid	No hit
0	0	1	Way 0 valid, not modified	Way 0 valid, not modified
0	1	0	Way 0 line was invalid	No hit
0	1	1	Way 0 valid and modified	Way 0 valid and modified
1	0	0	Way 1 line was invalid	No hit
1	0	1	Way 1 valid, not modified	Way 1 valid, not modified
1	1	0	Way 1 line was invalid	No hit
1	1	1	Way 1 valid and modified	Way 1 valid and modified

At completion of a line command other than a write, the CCVR (Cache R/W Value Register) contains information on the initial state of the line tag or data targeted by the command. For line commands, CLCR[TDSEL] selects between tag and data. If the line command used a physical address and missed, the data is don't care. For write commands, the CCVR holds the write data.

Chapter 33
Flash Memory Controller (FMC)

33.1 Chip-specific FMC information

33.1.1 Number of masters

The Flash Memory Controller supports up to eight crossbar switch masters. However, this device has a different number of crossbar switch masters. See Crossbar Switch Configuration for details on the master port assignments.

33.2 Introduction

The Flash Memory Controller (FMC) is a memory acceleration unit that provides:

- an interface between the device and the nonvolatile memory.
- buffers that can accelerate flash memory transfers.

33.2.1 Overview

The Flash Memory Controller manages the interface between the device and the flash memory. The FMC receives status information detailing the configuration of the memory and uses this information to ensure a proper interface. The following table shows the supported read/write operations.

Flash memory type	Read	Write
Program flash memory	8-bit, 16-bit, and 32-bit reads	—[1]

1. A write operation to program flash memory results in a bus error.

In addition, for bank 0, the FMC provides three separate mechanisms for accelerating the interface between the device and the flash memory. A 128-bit speculation buffer can prefetch the next 128-bit flash memory location, and both a 4-way, 4-set cache and a single-entry 128-bit buffer can store previously accessed flash memory data for quick access times.

33.2.2 Features

The FMC's features include:

- Interface between the device and the flash memory:
  - 8-bit, 16-bit, and 32-bit read operations to program flash memory.
  - For bank 0: Read accesses to consecutive 32-bit spaces in memory return the second, third, and fourth read data with no wait states. The memory returns 128 bits via the 32-bit bus access.
  - Crossbar master access protection for setting no access, read-only access, write-only access, or read/write access for each crossbar master.
- For bank 0: Acceleration of data transfer from program flash memory to the device:
  - 128-bit prefetch speculation buffer with controls for instruction/data access per master
  - 4-way, 4-set, 128-bit line size cache for a total of sixteen 128-bit entries with controls for replacement algorithm and lock per way
  - Single-entry buffer
  - Invalidation control for the speculation buffer and the single-entry buffer

33.3 Modes of operation

The FMC only operates when a bus master accesses the flash memory.

In terms of device power modes, the FMC only operates in run and wait modes, including VLPR and VLPW modes.

For any device power mode where the flash memory cannot be accessed, the FMC is disabled.

33.4 External signal description

The FMC has no external signals.

33.5 Memory map and register descriptions

The programming model consists of the FMC control registers and the program visible cache (data and tag/valid entries).

NOTE

Program the registers only while the flash controller is idle (for example, execute from RAM). Changing configuration settings while a flash access is in progress can lead to non-deterministic behavior.

Table 33-1. FMC register access

Registers	Read access		Write access	
	Mode	Length	Mode	Length
Control registers: PFAPR, PFB0CR, PFB1CR	Supervisor (privileged) mode or user mode	32 bits	Supervisor (privileged) mode only	32 bits
Cache registers	Supervisor (privileged) mode or user mode	32 bits	Supervisor (privileged) mode only	32 bits

NOTE

Accesses to unimplemented registers within the FMC's 4 KB address space return a bus error.

The cache entries, both data and tag/valid, can be read at any time.

NOTE

System software is required to maintain memory coherence when any segment of the flash cache is programmed. For example, all buffer data associated with the reprogrammed flash should be invalidated. Accordingly, cache program visible writes must occur after a programming or erase event is completed and before the new memory image is accessed.

The cache is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. The following table elaborates on the tag/valid and data entries.

Table 33-2. Program visible cache registers

Cache storage	Based at offset	Contents of 32-bit read	Nomenclature	Nomenclature example
Tag	100h	12'h0, tag[19:6], 5'h0, valid	In TAGVDWxSy, x denotes the way and y denotes the set.	TAGVDW2S0 is the 14-bit tag and 1-bit valid for cache entry way 2, set 0.
Data	200h	One of the four longwords in a 128-bit cache entry	In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost).	For data entry way 1, set 3, DATAW1S3UM represents bits [127:96], DATAW1S3MU represents bits [95:64], DATAW1S3ML represents bits [63:32], and DATAW1S3LM represents bits [31:0].

FMC memory map

Address offset (hex)	Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	4001_F000	Flash Access Protection Register (FMC_PFAPR)	32	R/W	0000_003Fh	33.5.1/774
4	4001_F004	Flash Bank 0 Control Register (FMC_PFB0CR)	32	R/W	3004_001Fh	33.5.2/776
8	4001_F008	Reserved (FMC_Reserved)	32	R/W	3000_0000h	33.5.3/778
100	4001_F100	Cache Tag Storage (FMC_TAGVDW0S0)	32	R/W	0000_0000h	33.5.4/779
104	4001_F104	Cache Tag Storage (FMC_TAGVDW0S1)	32	R/W	0000_0000h	33.5.4/779
108	4001_F108	Cache Tag Storage (FMC_TAGVDW0S2)	32	R/W	0000_0000h	33.5.4/779
10C	4001_F10C	Cache Tag Storage (FMC_TAGVDW0S3)	32	R/W	0000_0000h	33.5.4/779
110	4001_F110	Cache Tag Storage (FMC_TAGVDW1S0)	32	R/W	0000_0000h	33.5.5/780
114	4001_F114	Cache Tag Storage (FMC_TAGVDW1S1)	32	R/W	0000_0000h	33.5.5/780
118	4001_F118	Cache Tag Storage (FMC_TAGVDW1S2)	32	R/W	0000_0000h	33.5.5/780
11C	4001_F11C	Cache Tag Storage (FMC_TAGVDW1S3)	32	R/W	0000_0000h	33.5.5/780
120	4001_F120	Cache Tag Storage (FMC_TAGVDW2S0)	32	R/W	0000_0000h	33.5.6/781
124	4001_F124	Cache Tag Storage (FMC_TAGVDW2S1)	32	R/W	0000_0000h	33.5.6/781
128	4001_F128	Cache Tag Storage (FMC_TAGVDW2S2)	32	R/W	0000_0000h	33.5.6/781
12C	4001_F12C	Cache Tag Storage (FMC_TAGVDW2S3)	32	R/W	0000_0000h	33.5.6/781
130	4001_F130	Cache Tag Storage (FMC_TAGVDW3S0)	32	R/W	0000_0000h	33.5.7/782
134	4001_F134	Cache Tag Storage (FMC_TAGVDW3S1)	32	R/W	0000_0000h	33.5.7/782
138	4001_F138	Cache Tag Storage (FMC_TAGVDW3S2)	32	R/W	0000_0000h	33.5.7/782
13C	4001_F13C	Cache Tag Storage (FMC_TAGVDW3S3)	32	R/W	0000_0000h	33.5.7/782
200	4001_F200	Cache Data Storage (uppermost word) (FMC_DATAW0S0UM)	32	R/W	0000_0000h	33.5.8/783
204	4001_F204	Cache Data Storage (mid-upper word) (FMC_DATAW0S0MU)	32	R/W	0000_0000h	33.5.9/783
208	4001_F208	Cache Data Storage (mid-lower word) (FMC_DATAW0S0ML)	32	R/W	0000_0000h	33.5.10/ 784

Table continues on the next page...

FMC memory map (continued)

Address offset (hex)	Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
20C	4001_F20C	Cache Data Storage (lowermost word) (FMC_DATAW0S0LM)	32	R/W	0000_0000h	33.5.11/ 784
210	4001_F210	Cache Data Storage (uppermost word) (FMC_DATAW0S1UM)	32	R/W	0000_0000h	33.5.8/783
214	4001_F214	Cache Data Storage (mid-upper word) (FMC_DATAW0S1MU)	32	R/W	0000_0000h	33.5.9/783
218	4001_F218	Cache Data Storage (mid-lower word) (FMC_DATAW0S1ML)	32	R/W	0000_0000h	33.5.10/ 784
21C	4001_F21C	Cache Data Storage (lowermost word) (FMC_DATAW0S1LM)	32	R/W	0000_0000h	33.5.11/ 784
220	4001_F220	Cache Data Storage (uppermost word) (FMC_DATAW0S2UM)	32	R/W	0000_0000h	33.5.8/783
224	4001_F224	Cache Data Storage (mid-upper word) (FMC_DATAW0S2MU)	32	R/W	0000_0000h	33.5.9/783
228	4001_F228	Cache Data Storage (mid-lower word) (FMC_DATAW0S2ML)	32	R/W	0000_0000h	33.5.10/ 784
22C	4001_F22C	Cache Data Storage (lowermost word) (FMC_DATAW0S2LM)	32	R/W	0000_0000h	33.5.11/ 784
230	4001_F230	Cache Data Storage (uppermost word) (FMC_DATAW0S3UM)	32	R/W	0000_0000h	33.5.8/783
234	4001_F234	Cache Data Storage (mid-upper word) (FMC_DATAW0S3MU)	32	R/W	0000_0000h	33.5.9/783
238	4001_F238	Cache Data Storage (mid-lower word) (FMC_DATAW0S3ML)	32	R/W	0000_0000h	33.5.10/ 784
23C	4001_F23C	Cache Data Storage (lowermost word) (FMC_DATAW0S3LM)	32	R/W	0000_0000h	33.5.11/ 784
240	4001_F240	Cache Data Storage (uppermost word) (FMC_DATAW1S0UM)	32	R/W	0000_0000h	33.5.12/ 785
244	4001_F244	Cache Data Storage (mid-upper word) (FMC_DATAW1S0MU)	32	R/W	0000_0000h	33.5.13/ 785
248	4001_F248	Cache Data Storage (mid-lower word) (FMC_DATAW1S0ML)	32	R/W	0000_0000h	33.5.14/ 786
24C	4001_F24C	Cache Data Storage (lowermost word) (FMC_DATAW1S0LM)	32	R/W	0000_0000h	33.5.15/ 786
250	4001_F250	Cache Data Storage (uppermost word) (FMC_DATAW1S1UM)	32	R/W	0000_0000h	33.5.12/ 785
254	4001_F254	Cache Data Storage (mid-upper word) (FMC_DATAW1S1MU)	32	R/W	0000_0000h	33.5.13/ 785
258	4001_F258	Cache Data Storage (mid-lower word) (FMC_DATAW1S1ML)	32	R/W	0000_0000h	33.5.14/ 786
25C	4001_F25C	Cache Data Storage (lowermost word) (FMC_DATAW1S1LM)	32	R/W	0000_0000h	33.5.15/ 786
260	4001_F260	Cache Data Storage (uppermost word) (FMC_DATAW1S2UM)	32	R/W	0000_0000h	33.5.12/ 785

Table continues on the next page...

FMC memory map (continued)

Address offset (hex)	Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
264	4001_F264	Cache Data Storage (mid-upper word) (FMC_DATAW1S2MU)	32	R/W	0000_0000h	33.5.13/ 785
268	4001_F268	Cache Data Storage (mid-lower word) (FMC_DATAW1S2ML)	32	R/W	0000_0000h	33.5.14/ 786
26C	4001_F26C	Cache Data Storage (lowermost word) (FMC_DATAW1S2LM)	32	R/W	0000_0000h	33.5.15/ 786
270	4001_F270	Cache Data Storage (uppermost word) (FMC_DATAW1S3UM)	32	R/W	0000_0000h	33.5.12/ 785
274	4001_F274	Cache Data Storage (mid-upper word) (FMC_DATAW1S3MU)	32	R/W	0000_0000h	33.5.13/ 785
278	4001_F278	Cache Data Storage (mid-lower word) (FMC_DATAW1S3ML)	32	R/W	0000_0000h	33.5.14/ 786
27C	4001_F27C	Cache Data Storage (lowermost word) (FMC_DATAW1S3LM)	32	R/W	0000_0000h	33.5.15/ 786
280	4001_F280	Cache Data Storage (uppermost word) (FMC_DATAW2S0UM)	32	R/W	0000_0000h	33.5.16/ 787
284	4001_F284	Cache Data Storage (mid-upper word) (FMC_DATAW2S0MU)	32	R/W	0000_0000h	33.5.17/ 787
288	4001_F288	Cache Data Storage (mid-lower word) (FMC_DATAW2S0ML)	32	R/W	0000_0000h	33.5.18/ 788
28C	4001_F28C	Cache Data Storage (lowermost word) (FMC_DATAW2S0LM)	32	R/W	0000_0000h	33.5.19/ 788
290	4001_F290	Cache Data Storage (uppermost word) (FMC_DATAW2S1UM)	32	R/W	0000_0000h	33.5.16/ 787
294	4001_F294	Cache Data Storage (mid-upper word) (FMC_DATAW2S1MU)	32	R/W	0000_0000h	33.5.17/ 787
298	4001_F298	Cache Data Storage (mid-lower word) (FMC_DATAW2S1ML)	32	R/W	0000_0000h	33.5.18/ 788
29C	4001_F29C	Cache Data Storage (lowermost word) (FMC_DATAW2S1LM)	32	R/W	0000_0000h	33.5.19/ 788
2A0	4001_F2A0	Cache Data Storage (uppermost word) (FMC_DATAW2S2UM)	32	R/W	0000_0000h	33.5.16/ 787
2A4	4001_F2A4	Cache Data Storage (mid-upper word) (FMC_DATAW2S2MU)	32	R/W	0000_0000h	33.5.17/ 787
2A8	4001_F2A8	Cache Data Storage (mid-lower word) (FMC_DATAW2S2ML)	32	R/W	0000_0000h	33.5.18/ 788
2AC	4001_F2AC	Cache Data Storage (lowermost word) (FMC_DATAW2S2LM)	32	R/W	0000_0000h	33.5.19/ 788
2B0	4001_F2B0	Cache Data Storage (uppermost word) (FMC_DATAW2S3UM)	32	R/W	0000_0000h	33.5.16/ 787
2B4	4001_F2B4	Cache Data Storage (mid-upper word) (FMC_DATAW2S3MU)	32	R/W	0000_0000h	33.5.17/ 787
2B8	4001_F2B8	Cache Data Storage (mid-lower word) (FMC_DATAW2S3ML)	32	R/W	0000_0000h	33.5.18/ 788

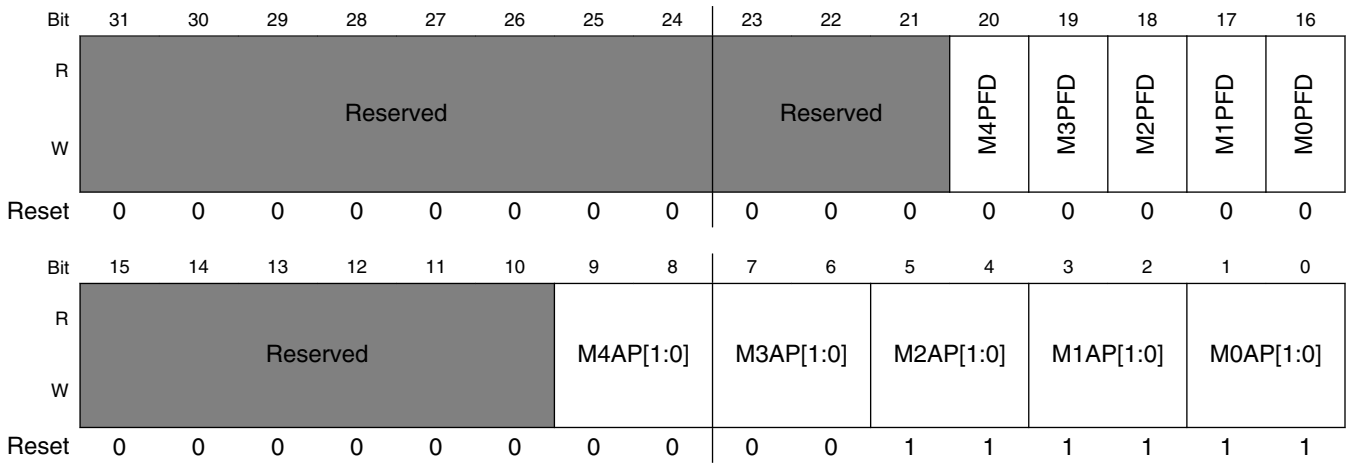
Table continues on the next page...

FMC memory map (continued)

Address offset (hex)	Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
2BC	4001_F2BC	Cache Data Storage (lowermost word) (FMC_DATAW2S3LM)	32	R/W	0000_0000h	33.5.19/ 788
2C0	4001_F2C0	Cache Data Storage (uppermost word) (FMC_DATAW3S0UM)	32	R/W	0000_0000h	33.5.20/ 789
2C4	4001_F2C4	Cache Data Storage (mid-upper word) (FMC_DATAW3S0MU)	32	R/W	0000_0000h	33.5.21/ 789
2C8	4001_F2C8	Cache Data Storage (mid-lower word) (FMC_DATAW3S0ML)	32	R/W	0000_0000h	33.5.22/ 790
2CC	4001_F2CC	Cache Data Storage (lowermost word) (FMC_DATAW3S0LM)	32	R/W	0000_0000h	33.5.23/ 790
2D0	4001_F2D0	Cache Data Storage (uppermost word) (FMC_DATAW3S1UM)	32	R/W	0000_0000h	33.5.20/ 789
2D4	4001_F2D4	Cache Data Storage (mid-upper word) (FMC_DATAW3S1MU)	32	R/W	0000_0000h	33.5.21/ 789
2D8	4001_F2D8	Cache Data Storage (mid-lower word) (FMC_DATAW3S1ML)	32	R/W	0000_0000h	33.5.22/ 790
2DC	4001_F2DC	Cache Data Storage (lowermost word) (FMC_DATAW3S1LM)	32	R/W	0000_0000h	33.5.23/ 790
2E0	4001_F2E0	Cache Data Storage (uppermost word) (FMC_DATAW3S2UM)	32	R/W	0000_0000h	33.5.20/ 789
2E4	4001_F2E4	Cache Data Storage (mid-upper word) (FMC_DATAW3S2MU)	32	R/W	0000_0000h	33.5.21/ 789
2E8	4001_F2E8	Cache Data Storage (mid-lower word) (FMC_DATAW3S2ML)	32	R/W	0000_0000h	33.5.22/ 790
2EC	4001_F2EC	Cache Data Storage (lowermost word) (FMC_DATAW3S2LM)	32	R/W	0000_0000h	33.5.23/ 790
2F0	4001_F2F0	Cache Data Storage (uppermost word) (FMC_DATAW3S3UM)	32	R/W	0000_0000h	33.5.20/ 789
2F4	4001_F2F4	Cache Data Storage (mid-upper word) (FMC_DATAW3S3MU)	32	R/W	0000_0000h	33.5.21/ 789
2F8	4001_F2F8	Cache Data Storage (mid-lower word) (FMC_DATAW3S3ML)	32	R/W	0000_0000h	33.5.22/ 790
2FC	4001_F2FC	Cache Data Storage (lowermost word) (FMC_DATAW3S3LM)	32	R/W	0000_0000h	33.5.23/ 790

33.5.1 Flash Access Protection Register (FMC_PFAPR)

Address: 4001_F000h base + 0h offset = 4001_F000h



FMC_PFAPR field descriptions

Field	Description
31–24 Reserved	This field is reserved.
23–21 Reserved	This field is reserved. This read-only bitfield is reserved. Do not write to this bitfield or indeterminate results will occur.
20 M4PFD	Master 4 Prefetch Disable These bits control whether prefetching is enabled, based on the logical number of the requesting crossbar switch master. This field is further qualified by the PFBnCR[BxDPE,BxIPE] bits. 0 Prefetching for this master is enabled. 1 Prefetching for this master is disabled.
19 M3PFD	Master 3 Prefetch Disable These bits control whether prefetching is enabled, based on the logical number of the requesting crossbar switch master. This field is further qualified by the PFBnCR[BxDPE,BxIPE] bits. 0 Prefetching for this master is enabled. 1 Prefetching for this master is disabled.
18 M2PFD	Master 2 Prefetch Disable These bits control whether prefetching is enabled, based on the logical number of the requesting crossbar switch master. This field is further qualified by the PFBnCR[BxDPE,BxIPE] bits. 0 Prefetching for this master is enabled. 1 Prefetching for this master is disabled.
17 M1PFD	Master 1 Prefetch Disable These bits control whether prefetching is enabled, based on the logical number of the requesting crossbar switch master. This field is further qualified by the PFBnCR[BxDPE,BxIPE] bits.

Table continues on the next page...

FMC_PFAPR field descriptions (continued)

Field	Description
	0 Prefetching for this master is enabled. 1 Prefetching for this master is disabled.
16 M0PFD	Master 0 Prefetch Disable These bits control whether prefetching is enabled, based on the logical number of the requesting crossbar switch master. This field is further qualified by the PFBnCR[BxDPE,BxIPE] bits. 0 Prefetching for this master is enabled. 1 Prefetching for this master is disabled.
15–10 Reserved	This field is reserved. This read-only bitfield is reserved and is reset to zero. Do not write to this bitfield or indeterminate results will occur.
9–8 M4AP[1:0]	Master 4 Access Protection This field controls whether read and write access to the flash is allowed, based on the logical master number of the requesting crossbar switch master. 00 No access may be performed by this master 01 Only read accesses may be performed by this master 10 Only write accesses may be performed by this master 11 Both read and write accesses may be performed by this master
7–6 M3AP[1:0]	Master 3 Access Protection This field controls whether read and write access to the flash is allowed, based on the logical master number of the requesting crossbar switch master. 00 No access may be performed by this master 01 Only read accesses may be performed by this master 10 Only write accesses may be performed by this master 11 Both read and write accesses may be performed by this master
5–4 M2AP[1:0]	Master 2 Access Protection This field controls whether read and write access to the flash is allowed, based on the logical master number of the requesting crossbar switch master. 00 No access may be performed by this master 01 Only read accesses may be performed by this master 10 Only write accesses may be performed by this master 11 Both read and write accesses may be performed by this master
3–2 M1AP[1:0]	Master 1 Access Protection This field controls whether read and write access to the flash is allowed, based on the logical master number of the requesting crossbar switch master. 00 No access may be performed by this master 01 Only read accesses may be performed by this master 10 Only write accesses may be performed by this master 11 Both read and write accesses may be performed by this master
M0AP[1:0]	Master 0 Access Protection

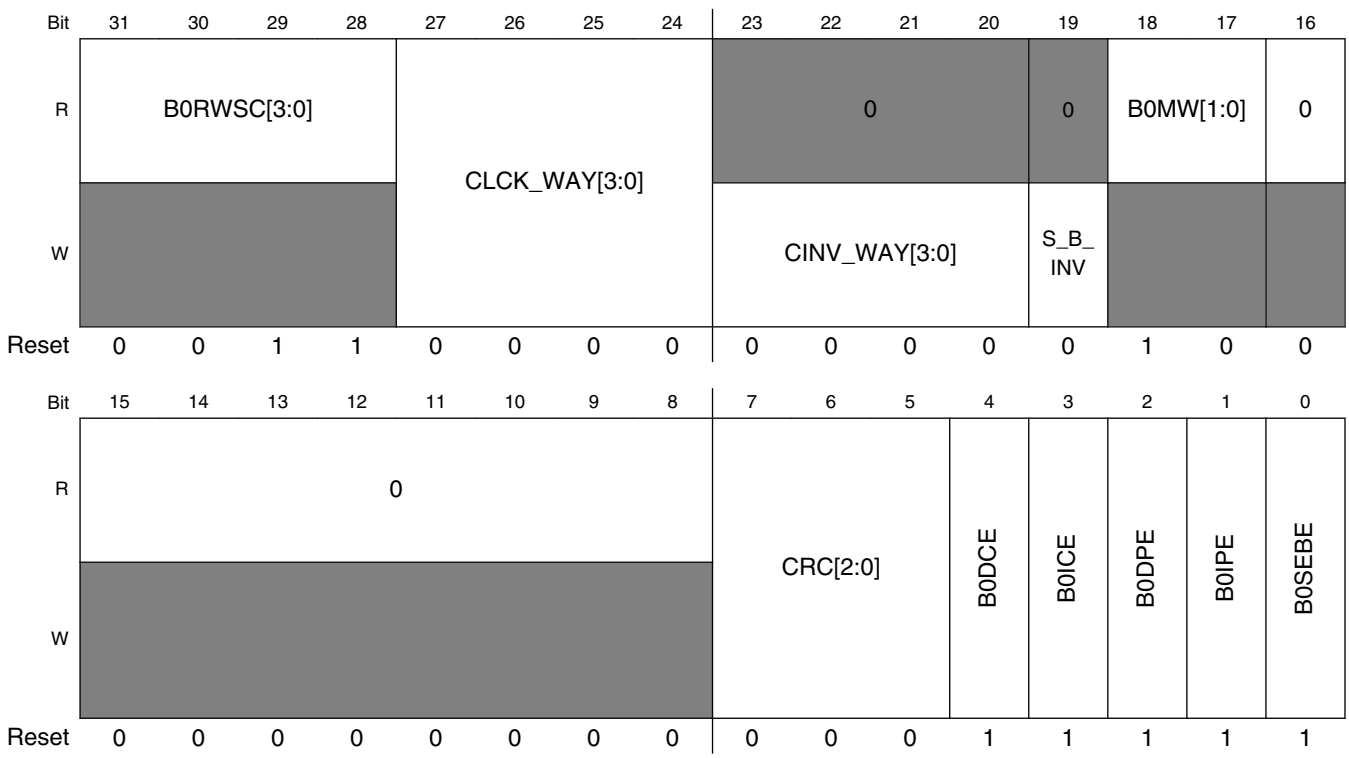
Table continues on the next page...

FMC_PFAPR field descriptions (continued)

Field	Description
	This field controls whether read and write access to the flash is allowed, based on the logical master number of the requesting crossbar switch master. 00 No access may be performed by this master 01 Only read accesses may be performed by this master 10 Only write accesses may be performed by this master 11 Both read and write accesses may be performed by this master

33.5.2 Flash Bank 0 Control Register (FMC_PFB0CR)

Address: 4001_F000h base + 4h offset = 4001_F004h



FMC_PFB0CR field descriptions

Field	Description
31–28 B0RWSC[3:0]	Bank 0 Read Wait State Control This read-only field defines the number of wait states required to access the bank 0 flash memory. The relationship between the read access time of the flash array (expressed in system clock cycles) and RWSC is defined as: Access time of flash array [system clocks] = RWSC + 1 The FMC automatically calculates this value based on the ratio of the system clock speed to the flash clock speed. For example, when this ratio is 4:1, the field's value is 3h.

Table continues on the next page...

FMC_PFB0CR field descriptions (continued)

Field	Description
27–24 CLCK_WAY[3:0]	Cache Lock Way x These bits determine if the given cache way is locked such that its contents will not be displaced by future misses. The bit setting definitions are for each bit in the field. 0 Cache way is unlocked and may be displaced 1 Cache way is locked and its contents are not displaced
23–20 CINV_WAY[3:0]	Cache Invalidate Way x These bits determine if the given cache way is to be invalidated (cleared). When a bit within this field is written, the corresponding cache way is immediately invalidated: the way's tag, data, and valid contents are cleared. This field always reads as zero. Cache invalidation takes precedence over locking. The cache is invalidated by system reset. System software is required to maintain memory coherency when any segment of the flash memory is programmed or erased. Accordingly, cache invalidations must occur after a programming or erase event is completed and before the new memory image is accessed. The bit setting definitions are for each bit in the field. 0 No cache way invalidation for the corresponding cache 1 Invalidate cache way for the corresponding cache: clear the tag, data, and vld bits of ways selected
19 S_B_INV	Invalidate Prefetch Speculation Buffer This bit determines if the FMC's prefetch speculation buffer and the single entry page buffer are to be invalidated (cleared). When this bit is written, the speculation buffer and single entry buffer are immediately cleared. This bit always reads as zero. 0 Speculation buffer and single entry buffer are not affected. 1 Invalidate (clear) speculation buffer and single entry buffer.
18–17 B0MW[1:0]	Bank 0 Memory Width This read-only field defines the width of the bank 0 memory. 00 32 bits 01 64 bits 10 128 bits 11 Reserved
16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7–5 CRC[2:0]	Cache Replacement Control This 3-bit field defines the replacement algorithm for accesses that are cached. 000 LRU replacement algorithm per set across all four ways 001 Reserved 010 Independent LRU with ways [0-1] for ifetches, [2-3] for data 011 Independent LRU with ways [0-2] for ifetches, [3] for data 1xx Reserved

Table continues on the next page...

FMC_PFB0CR field descriptions (continued)

Field	Description
4 B0DCE	Bank 0 Data Cache Enable This bit controls whether data references are loaded into the cache. 0 Do not cache data references. 1 Cache data references.
3 B0ICE	Bank 0 Instruction Cache Enable This bit controls whether instruction fetches are loaded into the cache. 0 Do not cache instruction fetches. 1 Cache instruction fetches.
2 B0DPE	Bank 0 Data Prefetch Enable This bit controls whether prefetches (or speculative accesses) are initiated in response to data references. 0 Do not prefetch in response to data references. 1 Enable prefetches in response to data references.
1 B0IPE	Bank 0 Instruction Prefetch Enable This bit controls whether prefetches (or speculative accesses) are initiated in response to instruction fetches. 0 Do not prefetch in response to instruction fetches. 1 Enable prefetches in response to instruction fetches.
0 B0SEBE	Bank 0 Single Entry Buffer Enable This bit controls whether the single entry page buffer is enabled in response to flash read accesses. A high-to-low transition of this enable forces the page buffer to be invalidated. 0 Single entry buffer is disabled. 1 Single entry buffer is enabled.

33.5.3 Reserved (FMC_Reserved)

This register address is reserved.

Address: 4001_F000h base + 8h offset = 4001_F008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved				0									Reserved		0
W																
Reset	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								0			0				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_Reserved field descriptions

Field	Description
31–28 Reserved	This field is reserved.
27–19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18–17 Reserved	This field is reserved.
16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

33.5.4 Cache Tag Storage (FMC_TAGVDW0S*n*)

The 128-entry cache is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In TAGVDWxSy, x denotes the way, and y denotes the set. This section represents tag/vld information for all sets (n=0-3) in way 0.

Address: 4001_F000h base + 100h offset + (4d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0												cache_tag			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	cache_tag										0					valid
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_TAGVDW0S*n* field descriptions

Field	Description
31–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–6 cache_tag	14-bit tag for cache entry
5–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 valid	1-bit valid for cache entry

33.5.5 Cache Tag Storage (FMC_TAGVDW1S*n*)

The 128-entry cache is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In TAGVDWxSy, x denotes the way, and y denotes the set. This section represents tag/vld information for all sets (n=0-3) in way 1.

Address: 4001_F000h base + 110h offset + (4d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0												cache_tag			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	cache_tag										0					valid
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_TAGVDW1S*n* field descriptions

Field	Description
31–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–6 cache_tag	14-bit tag for cache entry
5–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 valid	1-bit valid for cache entry

33.5.6 Cache Tag Storage (FMC_TAGVDW2S*n*)

The 128-entry cache is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In TAGVDWxSy, x denotes the way, and y denotes the set. This section represents tag/vld information for all sets (n=0-3) in way 2.

Address: 4001_F000h base + 120h offset + (4d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0												cache_tag			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	cache_tag										0					valid
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_TAGVDW2S*n* field descriptions

Field	Description
31–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–6 cache_tag	14-bit tag for cache entry
5–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 valid	1-bit valid for cache entry

33.5.7 Cache Tag Storage (FMC_TAGVDW3S*n*)

The 128-entry cache is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In TAGVDWxSy, x denotes the way, and y denotes the set. This section represents tag/vld information for all sets (n=0-3) in way 3.

Address: 4001_F000h base + 130h offset + (4d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0												cache_tag			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	cache_tag										0					valid
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_TAGVDW3S*n* field descriptions

Field	Description
31–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–6 cache_tag	14-bit tag for cache entry
5–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 valid	1-bit valid for cache entry

33.5.8 Cache Data Storage (uppermost word) (FMC_DATAW0S*n*UM)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the uppermost word (bits [127:96]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 200h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[127:96]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW0S*n*UM field descriptions

Field	Description
data[127:96]	Bits [127:96] of data entry

33.5.9 Cache Data Storage (mid-upper word) (FMC_DATAW0S*n*MU)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the mid-upper word (bits [95:64]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 204h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[95:64]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW0S*n*MU field descriptions

Field	Description
data[95:64]	Bits [95:64] of data entry

33.5.10 Cache Data Storage (mid-lower word) (FMC_DATAW0S*n*ML)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the mid-lower word (bits [63:32]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 208h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[63:32]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW0S*n*ML field descriptions

Field	Description
data[63:32]	Bits [63:32] of data entry

33.5.11 Cache Data Storage (lowermost word) (FMC_DATAW0S*n*LM)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the lowermost word (bits [31:0]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 20Ch offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[31:0]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW0S*n*LM field descriptions

Field	Description
data[31:0]	Bits [31:0] of data entry

33.5.12 Cache Data Storage (uppermost word) (FMC_DATAW1S*n*UM)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the uppermost word (bits [127:96]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 240h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[127:96]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW1S*n*UM field descriptions

Field	Description
data[127:96]	Bits [127:96] of data entry

33.5.13 Cache Data Storage (mid-upper word) (FMC_DATAW1S*n*MU)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the mid-upper word (bits [95:64]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 244h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[95:64]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW1S*n*MU field descriptions

Field	Description
data[95:64]	Bits [95:64] of data entry

33.5.14 Cache Data Storage (mid-lower word) (FMC_DATAW1S*n*ML)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the mid-lower word (bits [63:32]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 248h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[63:32]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW1S*n*ML field descriptions

Field	Description
data[63:32]	Bits [63:32] of data entry

33.5.15 Cache Data Storage (lowermost word) (FMC_DATAW1S*n*LM)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the lowermost word (bits [31:0]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 24Ch offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[31:0]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW1S*n*LM field descriptions

Field	Description
data[31:0]	Bits [31:0] of data entry

33.5.16 Cache Data Storage (uppermost word) (FMC_DATAW2S*n*UM)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the uppermost word (bits [127:96]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 280h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[127:96]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW2S*n*UM field descriptions

Field	Description
data[127:96]	Bits [127:96] of data entry

33.5.17 Cache Data Storage (mid-upper word) (FMC_DATAW2S*n*MU)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the mid-upper word (bits [95:64]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 284h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[95:64]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW2S*n*MU field descriptions

Field	Description
data[95:64]	Bits [95:64] of data entry

33.5.18 Cache Data Storage (mid-lower word) (FMC_DATAW2S*n*ML)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the mid-lower word (bits [63:32]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 288h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[63:32]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW2S*n*ML field descriptions

Field	Description
data[63:32]	Bits [63:32] of data entry

33.5.19 Cache Data Storage (lowermost word) (FMC_DATAW2S*n*LM)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the lowermost word (bits [31:0]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 28Ch offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[31:0]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW2S*n*LM field descriptions

Field	Description
data[31:0]	Bits [31:0] of data entry

33.5.20 Cache Data Storage (uppermost word) (FMC_DATAW3S*n*UM)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3. In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the uppermost word (bits [127:96]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 2C0h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[127:96]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW3S*n*UM field descriptions

Field	Description
data[127:96]	Bits [127:96] of data entry

33.5.21 Cache Data Storage (mid-upper word) (FMC_DATAW3S*n*MU)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3 . In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the mid-upper word (bits [95:64]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 2C4h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[95:64]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW3S*n*MU field descriptions

Field	Description
data[95:64]	Bits [95:64] of data entry

33.5.22 Cache Data Storage (mid-lower word) (FMC_DATAW3S*n*ML)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3 . In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the mid-lower word (bits [63:32]) of all 4 sets (n=0-3) in way 0.

Address: 4001_F000h base + 2C8h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[63:32]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW3S*n*ML field descriptions

Field	Description
data[63:32]	Bits [63:32] of data entry

33.5.23 Cache Data Storage (lowermost word) (FMC_DATAW3S*n*LM)

The cache of sixteen 128-bit entries is a 4-way, set-associative cache with 4 sets. The ways are numbered 0-3 and the sets are numbered 0-3 . In DATAWxSyUM, DATAWxSyMU, DATAWxSyML, and DATAWxSyLM, x denotes the way, y denotes the set, and the final two letters identify the word: UM (uppermost), MU (mid-upper), ML (mid-lower), and LM (lowermost). This section represents data for the lowermost word (bits [31:0]) of all 44 sets (n=0-3) in way 0.

Address: 4001_F000h base + 2CCh offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	data[31:0]																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMC_DATAW3S*n*LM field descriptions

Field	Description
data[31:0]	Bits [31:0] of data entry

33.6 Functional description

The FMC is a flash acceleration unit with flexible buffers for user configuration. Besides managing the interface between the device and the flash memory, the FMC can be used to restrict access from crossbar switch masters and customize the cache and buffers to provide single-cycle system-clock data-access times. Whenever a hit occurs for the prefetch speculation buffer, the cache, or the single-entry buffer, the requested data is transferred within a single system clock.

33.6.1 Default configuration

Upon system reset, the FMC is configured to provide a significant level of buffering for transfers from the flash memory:

- Crossbar masters 0, 1, 2 have read access to bank 0.
- For bank 0:
  - Prefetch support for data and instructions is enabled for crossbar masters 0, 1, 2.
  - The cache is configured for least recently used (LRU) replacement for all four ways.
  - The cache is configured for data or instruction replacement.
  - The single-entry buffer is enabled.

33.6.2 Configuration options

Though the default configuration provides a high degree of flash acceleration, advanced users may desire to customize the FMC buffer configurations to maximize throughput for their use cases. When reconfiguring the FMC for custom use cases, do not program the FMC's control registers while the flash memory is being accessed. Instead, change the control registers with a routine executing from RAM in supervisor mode.

The FMC's cache and buffering controls within PFB0CR allow the tuning of resources to suit particular applications' needs. The cache and buffer are each controlled individually. The register controls enable buffering and prefetching per access type (instruction fetch or data reference). The cache also supports 3 types of LRU replacement algorithms:

- LRU per set across all 4 ways,
- LRU with ways [0-1] for instruction fetches and ways [2-3] for data fetches, and
- LRU with ways [0-2] for instruction fetches and way [3] for data fetches.

As an application example: if both instruction fetches and data references are accessing flash memory, then control is available to send instruction fetches, data references, or both to the cache or the single-entry buffer. Likewise, speculation can be enabled or disabled for either type of access. If both instruction fetches and data references are cached, then the cache's way resources may be divided in several ways between the instruction fetches and data references.

33.6.3 Speculative reads

The FMC has a single buffer that reads ahead to the next word in the flash memory if there is an idle cycle. Speculative prefetching is programmable for each bank for instruction and/or data accesses using the B0DPE and B0IPE fields of PFB0CR. Because many code accesses are sequential, using the speculative prefetch buffer improves performance in most cases.

When speculative reads are enabled, the FMC immediately requests the next sequential address after a read completes. By requesting the next word immediately, speculative reads can help to reduce or even eliminate wait states when accessing sequential code and/or data.

For example, consider the following scenario:

- Assume a system with a 4:1 core-to-flash clock ratio and with speculative reads enabled.
- The core requests eight sequential longwords in back-to-back requests, meaning there are no core cycle delays except for stalls waiting for flash memory data to be returned.
- None of the data is already stored in the cache or speculation buffer.

In this scenario, the sequence of events for accessing the eight longwords is as follows:

1. The first longword read requires 4 to 7 core clocks. See Wait states for more information.
2. Due to the 128-bit data bus of the flash memory, the second longword read takes only 1 core clock because the data is already available inside the FMC. For the same reason, the third and fourth longword reads each take only 1 core clock.
3. Accessing the fifth longword requires 1 core clock cycle. The flash memory read itself takes 4 clocks, but the access starts immediately after the first read. As a result, 3 clocks for this access overlap with the second, third, and fourth longword reads from the core.
4. Reading the sixth, seventh, and eighth longwords takes only 1 clock each because the data is already available inside the FMC.

33.6.4 Flash Access Control (FAC) Function

The Flash Access Control (FAC) is a configurable memory protection scheme optimized to allow end users to use software libraries while offering programmable restrictions to these libraries. The flash memory is divided into *equal size segments* that provide protection to proprietary software libraries. The protection of these segments is controlled: the FAC provides a cycle-by-cycle evaluation of the access rights for each transaction routed to the on-chip flash memory. Two levels of vendors can add their proprietary software to a device; FAC protection of segments for each level are defined once, using the PGMONCE command.

Flash access control aligns to the 3 privilege levels supported by ARM Cortex-M family products:

- Most secure state is supervisor/privileged secure: allows execute-only and provides supervisor-only access control.
- Mid-level state is execute-only.
- Unsecure state is where no access control states are set.

Features:

- Lightweight access control logic for on-chip flash memory
- Flash address space divided into (32 or 64) equal-sized segments (segment size is defined as flash_size [bytes]/(32 or 64))
- Separate control bits for supervisor-only access and execute-only access per segment
- Access control evaluated on each bus cycle routed to the flash
- Access violation errors terminate the bus cycle and return zeroes for read data
- Programming model allows 2 levels of protected segments

33.6.4.1 Memory map and register definitions

The following table shows the mapping of FAC registers. Descriptions of each register and its bit assignments follow.

- The Flash Management Unit (FMU) supports access to its FAC programming model via a 32-bit slave peripheral bus connection.
- Unimplemented register bits read as zero.
- Some registers are implemented as two 32-bit registers, and include an H and L suffix, signaling the high and low portions of the control function.
- For implementations supporting only 32 segments, only the 32-bit "low" register is implemented.

- Writes to any read-only or reserved registers are ignored; attempts to access flash register space above offset '2B' will generate a transfer error.
- The terms *supervisor* and *user* modes are equivalent to *privileged* and *unprivileged* modes.
- In this FAC section, *n* refers to the segment number, and *x* is the acronym of the module that the registers are in (which sometimes varies from one device to another).

x memory map

Address offset (hex)	Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
18	18	Execute-only Access Register High (x_XACCH)	32	R	See section	33.6.4.1.1/ 794
1C	1C	Execute-only Access Register Low (x_XACCL)	32	R	See section	33.6.4.1.2/ 795
20	20	Supervisor-only Access Register High (x_SACCH)	32	R	See section	33.6.4.1.3/ 796
24	24	Supervisor-only Access Register Low (x_SACCL)	32	R	See section	33.6.4.1.4/ 796
28	28	Configuration Register (x_CR)	32	R	See section	33.6.4.1.5/ 797

33.6.4.1.1 Execute-only Access Register High (x_XACCH)

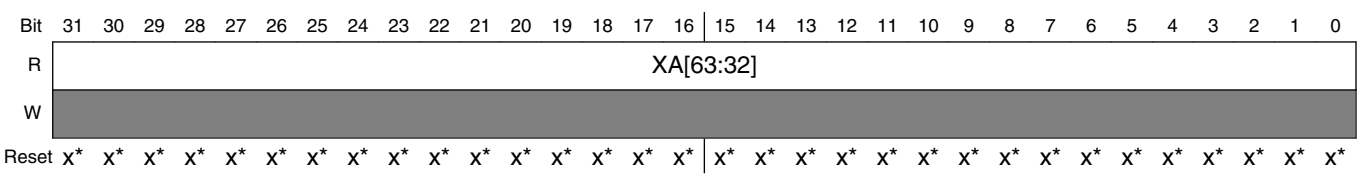
The execute-only access register is a 64-bit register that is implemented as two 32-bit registers.

- High execute-only access bits (segments 63-32) are contained in *x*_XACCH.
- Low execute-only access bits (segments 31-0) are contained in *x*_XACCL.

The *x*_XACC{H,L} registers provide a bit map for the flash segments, to allow *data read* or *execute only* or *both data and instruction fetches* for each associated segment. By definition, execute-only accesses include instruction fetches or PC-relative data loads from the processor.

During the reset sequence the XACC register is loaded with a pre-programmed value from non-volatile space in flash. For more about NVM characteristics, see the functional description. Any change made to an NVM location takes effect on the next system reset. The flash basis for the values is signified by * in the reset value.

Address: 0h base + 18h offset = 18h



* Notes:

- Pre-programmed flash valuex = Undefined at reset.

x_XACCH field descriptions

Field	Description
XA[63:32]	Execute-only Access Control for segments 63-32 0 Associated segment is accessible in execute mode only (as an instruction fetch) 1 Associated segment is accessible as data or in execute mode

33.6.4.1.2 Execute-only Access Register Low (x_XACCL)

The XACC{H,L} registers provide a bit map for the flash segments to allow execute only or both data and instruction fetches for each associated segment. XACCH covers segments 63-32 and XACCL covers segments 31-0. By definition, execute-only accesses include instruction fetches or PC-relative data loads from the processor.

During the reset sequence the XACC register is loaded with a pre-programmed value from non-volatile space in flash. For more about NVM characteristics, see the functional description. Any change made to an NVM location takes effect on the next system reset. The flash basis for the values is signified by * in the reset value.

Address: 0h base + 1Ch offset = 1Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	XA[31:0]																															
W																																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- Pre-programmed flash valuex = Undefined at reset.

x_XACCL field descriptions

Field	Description
XA[31:0]	Execute-only Access Control for segments 31-0 0 Associated segment is accessible in execute mode only (as an instruction fetch) 1 Associated segment is accessible as data or in execute mode

33.6.4.1.3 Supervisor-only Access Register High (x_SACCH)

The supervisor-only access register is a 64-bit register that is implemented as two 32-bit registers.

- High supervisor-only access bits (segments 63-32) are contained in *x*_SACCH.
- Low supervisor-only access bits (segments 31-0) are contained in *x*_SACCL.

The *x*_SACC{H,L} registers provide a bit map for the flash segments, to allow *supervisor only* or *user* and *supervisor* access to the associated segment.

During the reset sequence the SACC register is loaded with a pre-programmed value from non-volatile space in flash. See the functional description for more details on NVM characteristics. Any change made to an NVM location takes effect on the next system reset. The flash basis for the values is signified by * in the reset value.

Address: 0h base + 20h offset = 20h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SA[63:32]																															
W																																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- Pre-programmed flash valuex = Undefined at reset.

x_SACCH field descriptions

Field	Description
SA[63:32]	Supervisor Access Control for segments 63-32 0 Associated segment is accessible in supervisor mode only 1 Associated segment is accessible in user or supervisor mode

33.6.4.1.4 Supervisor-only Access Register Low (x_SACCL)

The SACC{H,L} registers provide a bit map for the flash segments to allow *supervisor only* or *user* and *supervisor* access to the associated segment. SACCH covers segments 63-32 and SACCL supports segments 31-0.

During the reset sequence the SACC register is loaded with a pre-programmed value from non-volatile space in flash. For more about NVM characteristics, see the functional description. Any change made to an NVM location takes effect on the next system reset. The flash basis for the values is signified by * in the reset value.

Address: 0h base + 24h offset = 24h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SA[31:0]																															
W																																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- Pre-programmed flash valuex = Undefined at reset.

x_SACCL field descriptions

Field	Description
SA[31:0]	Supervisor Access for segments 31-0 0 Associated segment is accessible in supervisor mode only 1 Associated segment is accessible in user or supervisor mode

33.6.4.1.5 Configuration Register (x_CR)

The FAC Configuration Register provides basic configuration information including the flash segment size and an indicator of segment divisions.

The NUMSG and SGSIZE values are fixed for a device. The chip-specific basis for the values is signified by * in the reset value.

Address: 0h base + 28h offset = 28h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	NUMSG								0																SGSIZE							
W																																
Reset	*	*	*	*	*	*	*	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*

* Notes:
- NUMSG field: Device specific value
- SGSIZE field: Device specific value

x_CR field descriptions

Field	Description
31–24 NUMSG	Number of Segments Indicator The NUMSG field indicates the number of equal-sized segments in the flash. 0x20 Flash is divided into 32 segments 0x40 Flash is divided into 64 segments
23–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
SGSIZE	Segment Size

Table continues on the next page...

x_CR field descriptions (continued)

Field	Description
	The segment size is a fixed value calculated from the available flash size (rounded up to nearest power of 2) divided by 32 or 64, depending on the amount of available program flash. This field determines which bits in the address are used to index into the *x*_SACC and *x*_XACC bitmaps to get the appropriate permission flags. The segment size is defined by the equation 2^(8 + SGSIZE[7:0]). The tables below show a sampling of possible settings.

Flash Size	Segment Size	Segment Size Encoding
32 Segment Encodings		
16 KBytes	16 KBytes/32 = 512 Bytes	0x1
32 KBytes	32 KBytes/32 = 1 KBytes	0x2
64 KBytes	64 KBytes/32 = 2 KBytes	0x3
128 KBytes	128 KBytes/32 = 4 KBytes	0x4
64 Segment Encodings		
256 KBytes	256 KBytes/64 = 4 KBytes	0x4
512 KBytes	512 KBytes/64 = 8 KBytes	0x5
1 MBytes	1 MBytes/64 = 16 KBytes	0x6

33.6.4.2 FAC functional description

The access control functionality is implemented in 2 separate blocks within the SoC. The Flash Management Unit (FMU) includes non-volatile configuration information that is retrieved during reset and and sent to the platform to control access to the flash array during normal operation.

There are (4) 64-bit NVM storage locations to support access control features. These NVM locations are summarized in the table below.

Table 33-3. NVM Locations

NVM location	Description	
NVSACC1, NVSACC2	Two locations are ANDed together and loaded during reset into the *x*_SACC register to provide access configuration.	Segment-wise control for supervisor-only access vs. supervisor and user access
NVXACC1, NVXACC2	Two locations are ANDed together and loaded during reset into the *x*_XACC register to provide access configuration.	Segment-wise control for execute-only vs. data and execute

Each of these NVM locations is programmable through a Program Once flash command and can be programmed one time. These NVM locations are unaffected by Erase All Blocks flash command and debug interface initiated mass erase operations. Since the 2 NVXACCx fields are ANDed, the access protection can only be increased. A segment's

access controls can be changed from data read and execute (XA*n* =1) to execute-only (XA*n* =0), or from supervisor and user mode (SAn = 1) to supervisor-only mode (SAn = 0).

The flash is released from reset early while the core continues to be held in reset. The FMU captures the NVM access control information in internal registers. The FMU ANDs the multiple execute-only fields to create a single execute-only field. This execute-only field driven to the platform is static prior to the core being released from reset. The supervisor-only field is handled in the same manner.

The FMU includes the FAC registers that provide control access to the flash address space. During the address phase of every attempted flash transfer, the supervisor access (SA*n*) and execute access (XA*n*) bits are examined to either allow or deny access. If access is denied, then the access is aborted and terminates with a bus error; the read data is also zeroed.

The next table shows segment assignments relative to the flash location.

Table 33-4. Flash Protection Ranges

SA*n* and XA*n* Bit	Protected Segment Address Range	Segment Size (Fraction of total Flash)
64 Segment Encodings		
0	0x0_0000_0000 – (Flash_size/64-1)	1/64
1	(Flash_size/64) – 2*(Flash_size/64-1)	1/64
.....		
63	63*(Flash_size/64) – 62*(Flash_size/64-1)	1/64
32 Segment Encodings		
0	0x0_0000_0000 – (Flash_size/32-1)	1/32
1	(Flash_size/32) – 2*(Flash_size/32-1)	1/32
.....		
31	31*(Flash_size/32) – 30*(Flash_size/32-1)	1/32

Individual segments within the flash memory can be independently protected from user access and data access. Protection is controlled by the individual bits within the *x*_SACC and *x*_XACC registers, as shown in the next figure.

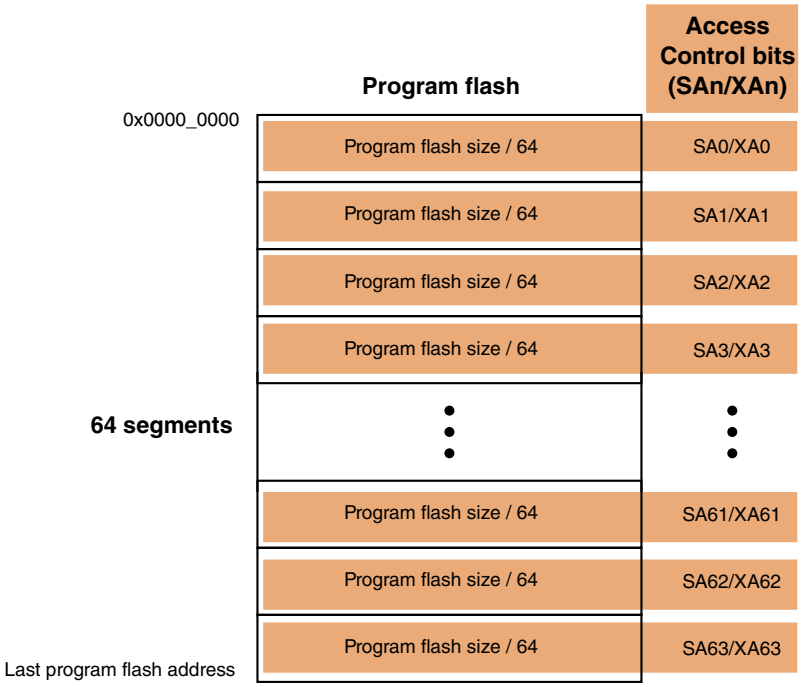


Figure 33-1. Program flash protection (64 segments)

33.6.4.2.1 Interface Signals

Table 33-5. Interface Signals

Signal	Width	From	To	Description
xacc	64 or 32	FMU	Platform	Direct xacc (execute-only access control) register
sacc	64 or 32	FMU	Platform	Direct sacc (supervisor access control) register
numsg	8	FMU	Platform	NUMSG bit field - Binary encoded number of segments 0x40 for 64 segments 0x20 for 32 segments
fac_enable	1	SIM	FMU	SIM Option bit - derived from an IFR bit and captured in SIM_SOPTx. A way to disable the flash access control for phantom devices without this feature. fac_enable==1 - Access Control feature is enabled fac_enable==0 - Access Control feature is disabled • During the reset sequence, XACC registers are written to all "1"s. • During the reset sequence, SACC registers are written to all 1"s. • Implied protection based on XACC registers is turned off.

33.6.4.2.2 Flash Command Impact

Program Longword/Phrase/ Section	If the targeted flash location is in an execute-only protected segment, then these program commands are not allowed unless a Read 1s All Blocks command is executed and returns with a pass code (which means the part has been fully erased). After the Read 1s All Blocks command is executed with a pass code returned, then the protected segment is open to program commands. To close off programmability to execute-only spaces once again, the device must be reset or a Read 1s All Blocks command is executed with a fail result. Attempts to program in a protected segment *when not open to program commands* causes a Protection Violation flag.
PGMCHK	The FMU will not execute the PGMCHK on a segment that has been configured as execute-only. The Flash Protection Violation flag is set if an attempt is made to execute PGMCHK command on an execute-only address.
Erase Flash Sector	If the targeted flash sector is in an execute-only protected segment, then the Erase Flash Sector command is not allowed, and sets the Protection Violation flag. The only means of erasing protected space is by an Erase All operation.
ERSALL	The Erase All Blocks command is not affected by Access Control. An Erase All Blocks command will erase any libraries that have been programmed in any execute-only segment. The programmed execute-only assignment is not erased as part of the Erase All Blocks command, and access control regions remain as previously programmed. **NOTE:** The ERSALL command may be used for field upgrades. Access control states remain programmed. Software must plan accordingly, possibly making extra space available for future use.
SWAP	A new control has been added to the SWAP command to disable the SWAP feature. The IFR SWAP Field and the SWAP indicator are erased during the Erase All Blocks command operation, resulting in the SWAP system being uninitialized. The SWAP command must be run with the initialization code to set the SWAP indicator address and initialize the SWAP system. After being disabled, SWAP cannot be enabled without doing an Erase All. An Erase All erases preloaded code and libraries in the flash array and resets the SWAP system back to uninitialized, but leaves the access controls as previously programmed. If SWAP is intended to be disabled as part of the access control protection, then the disabled setting must be restored after an Erase All Blocks operation.

33.6.4.2.3 Core Platform Impact

Platform core caches (Flash and LMEM caches)	If any segment is marked as *execute-only*, then the caches are hidden from the user. The tag is read-only and cannot be written, and the data caches cannot be read or written. Writes to the tag and data arrays are ignored, and reads of the data array return 0's. This will impact debug breakpoints. See the debug section for details.
Debug	The debugger is a non-processor bus master and cannot step, trace or break in execute-only regions. In supervisor-only mode, the debugger is restricted from changing modes. Debug accesses to any segment of flash space marked as execute-only also terminate with a bus error.
PC-relative addressing	The PC-relative addressing issue is still being understood and this section will be updated in the future. PC relative re-entry to execute-only segments will be allowed..... Restrictions will be placed on software for PC relative addressing, because hardware cannot determine if PC relative data references are crossing segment boundaries.

Table continues on the next page...

	• If ifetch is executing in a protected segment, then data references will be allowed. • Hardware cannot track speculative ifetches across boundaries.
Interrupts	If function calls are used to move into an execute-only segment, then this can be tracked by hardware when typical software controls are used (i.e., saving registers and states before executing new code).
Reset Vector	In the ARM core, the reset vector fetch is supervisor data, which poses issues if the reset vector is located in a segment marked execute-only. Additional logic has been implemented to allow supervisor data fetches to execute-only spaces, after reset until the first valid instruction fetch. After the first valid instruction fetch, the FAC logic follows normal checks.

33.6.4.2.4 Software Impact

As implementation, verification and validation continue, there will be more details on software impact that will need to be communicated to tool and library vendors. The hardware cannot see all states of the ARM core and cannot track the software flow requiring software restrictions to work with the hardware for a robust solution.

Any segment marked as execute-only can see all code in the system. This means one execute-only segment can read the execute-only code in another segment. Therefore, if Freescale is sending pre-loaded code to another vendor, then that vendor will have access to Freescale code. Possibly use NDAs and legal agreements to deal with this issue.

For single pre-loads (for example, if Freescale is pre-loading for a GP market or if a vendor with a blank part is pre-loading proprietary code), then both levels of access control must be programmed, to protect the pre-loaded code.

If any portion of a protected segment is not used by pre-loaded code, then it (the portion of a protected segment that is not used by pre-loaded code) should be programmed with NOPs, to prevent additional code from being programmed in that segment by hackers.

33.6.4.2.5 Access Check Evaluation

The flash controller FAC provides a cycle-by-cycle evaluation of the access rights for each data transaction routed to the on-chip flash memory.

The entire flash storage capacity is partitioned into equal sized segments. Two registers include a supervisor-only access control indicator and a execute-only access control indicator for each segment.

The FAC logic performs the required access control evaluation using the reference address and a 2-bit attribute (or "protection" field) as inputs from the bus cycle plus the contents of the programming model registers.

The following code example illustrates C code for FAC evaluation:

```
unsigned long long sacc;  // supervisor-only map
unsigned long long xacc;  // execute-only map
unsigned int seg_size;    // 8-bit segment size
unsigned int fac_error;

fac_evaluation (addr, prot)
  unsigned int addr;  // access address
  unsigned int hprot; // encoded 2-bit "protection" field {supv, data}
{
  unsigned int sacc_flag; // sacc flag for this segment
  unsigned int xacc_flag; // xacc flag for this segment
  unsigned int i;         // segment index

  i         = (addr >> (8 + seg_size & 0x0f)) & 0x3f; // form 6-bit segment index
  sacc_flag = (sacc >> i) & 1;              // extract sacc bit for this segment
  xacc_flag = (xacc >> i) & 1;              // extract xacc bit for this segment

  // create a 4-tuple concatenating the 2-bit protection field + {sacc, xacc} flags

  switch ((hprot & 3) << 2 | (sacc_flag << 1) | xacc_flag) {
  // all these combinations are allowed accesses
    case 0x2: // {user, ifetch} && {supv+user, ifetch-only}
    case 0x3: // {user, ifetch} && {supv+user, ifetch+data}
    case 0x7: // {user, data}   && {supv+user, ifetch+data}
    case 0x8: // {supv, ifetch} && {supv-only, ifetch-only}
    case 0x9: // {supv, ifetch} && {supv-only, ifetch+data}
    case 0xa: // {supv, ifetch} && {supv+user, ifetch-only}
    case 0xb: // {supv, ifetch} && {supv+user, ifetch+data}
    case 0xd: // {supv, data}   && {supv-only, ifetch+data}
    case 0xf: // {supv, data}   && {supv+user, ifetch+data}
      fac_error = 00;
      break;

  // all these combinations are unallowed, that is, errored accesses
    case 0x0: // {user, ifetch} && {supv-only, ifetch-only}
    case 0x1: // {user, ifetch} && {supv-only, ifetch+data}
    case 0x4: // {user, data}   && {supv-only, ifetch-only}
    case 0x5: // {user, data}   && {supv-only, ifetch+data}
    case 0x6: // {user, data}   && {supv+user, ifetch-only}
    case 0xc: // {supv, data}   && {supv-only, ifetch-only}
    case 0xe: // {supv, data}   && {supv+user, ifetch-only}
      fac_error = 1;
      break;

   } // switch()

} // fac_evaluation()
```

33.6.4.2.6 FAC application tips

In one use case, the NVSACC1 and NVXACC1 locations are programmed by Freescale and they protect Freescale libraries that have been programmed into associated flash segments in a device. Later, the NVSACC2 and NVXACC2 NVM locations can optionally be programmed by a third-party vendor who wants to program their proprietary software and to extend the protection of protected flash segments to include their software libraries before supplying it all to their customers.

Their customer would then develop their own code to use the available libraries, and program their code into the remaining available on-chip flash. The device continues to support the end user with standard security features that further limit external access to flash resources.

SWAP: If execute-only code is mirrored in both halves of the flash array, then SWAP can be enabled without any issues; otherwise SWAP should be disabled, because hardware does not track access control addressing during SWAP.

33.7 Initialization and application information

The FMC does not require user initialization. Flash acceleration features are enabled by default.

The FMC has no visibility into flash memory erase and program cycles because the Flash Memory module manages them directly. As a result, if an application is executing flash memory commands, the FMC's cache might need to be disabled and/or flushed to prevent the possibility of returning stale data. Use the PFB0CR[CINV_WAY] field to invalidate the cache in this manner.

Chapter 34
Flash Memory Module (FTFA)

34.1 Introduction

The flash memory module includes the following accessible memory regions:

- Program flash memory for vector space and code store

Flash memory is ideal for single-supply applications, permitting in-the-field erase and reprogramming operations without the need for any external high voltage power sources.

The flash memory module includes a memory controller that executes commands to modify flash memory contents. An erased bit reads '1' and a programmed bit reads '0'. The programming operation is unidirectional; it can only move bits from the '1' state (erased) to the '0' state (programmed). Only the erase operation restores bits from '0' to '1'; bits cannot be programmed from a '0' to a '1'.

CAUTION

A flash memory location must be in the erased state before being programmed. Cumulative programming of bits (back-to-back program operations without an intervening erase) within a flash memory location is not allowed. Re-programming of existing 0s to 0 is not allowed as this overstresses the device.

The standard shipping condition for flash memory is erased with security disabled. Data loss over time may occur due to degradation of the erased ('1') states and/or programmed ('0') states. Therefore, it is recommended that each flash block or sector be re-erased immediately prior to factory programming to ensure that the full data retention capability is achieved.

34.1.1 Features

The flash memory module includes the following features.

NOTE

See the device's Chip Configuration details for the exact amount of flash memory available on your device.

34.1.1.1 Program Flash Memory Features

- Sector size of 4 KB
- Program flash protection scheme prevents accidental program or erase of stored data
- Program flash access control scheme prevents unauthorized access to selected code segments
- Automated, built-in, program and erase algorithms with verify

34.1.1.2 Other Flash Memory Module Features

- Internal high-voltage supply generator for flash memory program and erase operations
- Optional interrupt generation upon flash command completion
- Supports MCU security mechanisms which prevent unauthorized access to the flash memory contents

34.1.2 Block Diagram

The block diagram of the flash memory module is shown in the following figure.

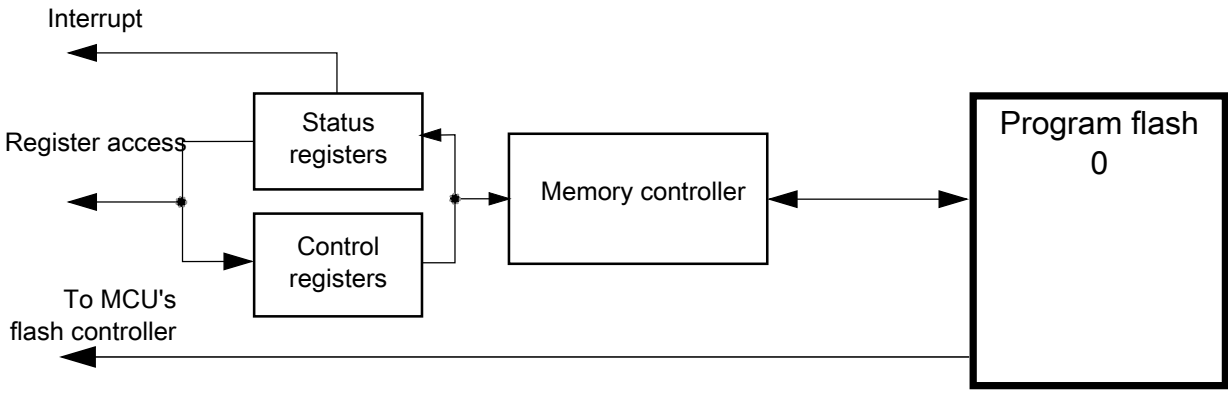


Figure 34-1. Flash Block Diagram

34.1.3 Glossary

Command write sequence — A series of MCU writes to the flash FCCOB register group that initiates and controls the execution of flash algorithms that are built into the flash memory module.

Double-Phrase — 128 bits of data with an aligned double-phrase having byte-address[3:0] = 0000.

Endurance — The number of times that a flash memory location can be erased and reprogrammed.

FCCOB (Flash Common Command Object) — A group of flash registers that are used to pass command, address, data, and any associated parameters to the memory controller in the flash memory module.

Flash block — A macro within the flash memory module which provides the nonvolatile memory storage.

Flash Memory Module — All flash blocks plus a flash management unit providing high-level control and an interface to MCU buses.

HSRUN — An MCU power mode enabling high-speed access to the memory resources in the flash module. The user has no access to the flash command set when the MCU is in HSRUN mode.

IFR — Nonvolatile information register found in each flash block, separate from the main memory array.

Longword — 32 bits of data with an aligned longword having byte-address[1:0] = 00.

NVM — Nonvolatile memory. A memory technology that maintains stored data during power-off. The flash array is an NVM using NOR-type flash memory technology.

NVM Normal Mode — An NVM mode that provides basic user access to flash memory module resources. The CPU or other bus masters initiate flash program and erase operations (or other flash commands) using writes to the FCCOB register group in the flash memory module.

NVM Special Mode — An NVM mode enabling external, off-chip access to the memory resources in the flash memory module. A reduced flash command set is available when the MCU is secured. See the Chip Configuration details for information on when this mode is used.

Phrase — 64 bits of data with an aligned phrase having byte-address[2:0] = 000.

Program flash — The program flash memory provides nonvolatile storage for vectors and code store.

Program flash Sector — The smallest portion of the program flash memory (consecutive addresses) that can be erased.

Retention — The length of time that data can be kept in the NVM without experiencing errors upon readout. Since erased (1) states are subject to degradation just like programmed (0) states, the data retention limit may be reached from the last erase operation (not from the programming time).

RWW— Read-While-Write. The ability to simultaneously read from one memory resource while commanded operations are active in another memory resource.

Secure — An MCU state conveyed to the flash memory module as described in the Chip Configuration details for this device. In the secure state, reading and changing NVM contents is restricted.

Word — 16 bits of data with an aligned word having byte-address[0] = 0.

34.2 External Signal Description

The flash memory module contains no signals that connect off-chip.

34.3 Memory Map and Registers

This section describes the memory map and registers for the flash memory module.

Data read from unimplemented memory space in the flash memory module is undefined. Writes to unimplemented or reserved memory space (registers) in the flash memory module are ignored.

34.3.1 Flash Configuration Field Description

The program flash memory contains a 16-byte flash configuration field that stores default protection settings (loaded on reset) and security information that allows the MCU to restrict access to the flash memory module.

Flash Configuration Field Byte Address	Size (Bytes)	Field Description
0x0_0400–0x0_0407	8	Backdoor Comparison Key. Refer to Verify Backdoor Access Key Command and Unsecuring the Chip Using Backdoor Key Access.
0x0_0408–0x0_040B	4	Program flash protection bytes. Refer to the description of the Program Flash Protection Registers (FPROT0-3).
0x0_040F	1	Reserved
0x0_040E	1	Reserved
0x0_040D	1	Flash nonvolatile option byte. Refer to the description of the Flash Option Register (FOPT).
0x0_040C	1	Flash security byte. Refer to the description of the Flash Security Register (FSEC).

34.3.2 Program Flash IFR Map

The program flash IFR is nonvolatile information memory that can be read freely, but the user has no erase and limited program capabilities (see the Read Once, Program Once, and Read Resource commands in Read Once Command, Program Once Command and Read Resource Command).

The contents of the program flash IFR are summarized in the table found here and further described in the subsequent paragraphs.

The program flash IFR is located within the program flash 0 memory block .

Address Range	Size (Bytes)	Field Description
0x00 – 0x9F	160	Reserved
0xA0 – 0xA3	4	Program Once XACCH-1 Field (index = 0x10)
0xA4 – 0xA7	4	Program Once XACCL-1 Field (index = 0x10)

Table continues on the next page...

Address Range	Size (Bytes)	Field Description
0xA8 – 0xAB	4	Program Once XACCH-2 Field (index = 0x11)
0xAC – 0xAF	4	Program Once XACCL-2 Field (index = 0x11)
0xB0 – 0xB3	4	Program Once SACCH-1 Field (index = 0x12)
0xB4 – 0xB7	4	Program Once SACCL-1 Field (index = 0x12)
0xB8 – 0xBB	4	Program Once SACCH-2 Field (index = 0x13)
0xBC – 0xBF	4	Program Once SACCL-2 Field (index = 0x13)
0xC0 – 0xFF	64	Program Once ID Field (index = 0x00 - 0x0F)

34.3.2.1 Program Once Field

The Program Once Field in the program flash IFR provides 96 bytes of user data storage separate from the program flash main array. The user can program the Program Once Field one time only as there is no program flash IFR erase mechanism available to the user. The Program Once Field can be read any number of times. This section of the program flash IFR is accessed in 4-byte or 8-Byte records using the Read Once and Program Once commands (see Read Once Command and Program Once Command).

34.3.3 Program Flash Erasable IFR Map

The program flash erasable IFR is nonvolatile information memory that can be erased but has limited program capabilities and limited read access. The contents of the program flash erasable IFR fields are summarized in the table found here.

Address Range	Size (Bytes)	Field Description
0x80 – 0x83	4	Erasable Program Once Field (index = 0x20)
0x84 – 0x87	4	Erasable Program Once Field (index = 0x21)
0x88 – 0x8B	4	Erasable Program Once Field (index = 0x22)
0x8C – 0x8F	4	Erasable Program Once Field (index = 0x23)
0xC0 – 0xC3	4	Erasable Program Once Field (index = 0x30)
0xC4 – 0xC7	4	Erasable Program Once Field (index = 0x31)
0xC8 – 0xCB	4	Erasable Program Once Field (index = 0x32)

Table continues on the next page...

Address Range	Size (Bytes)	Field Description
0xCC – 0xCF	4	Erasable Program Once Field (index = 0x33)

34.3.3.1 Erasable Program Once Field

The Program Once Field in the program flash erasable IFR with indexes 0x20 - 0x23 provides 16 bytes of user data storage that can be programmed using the Program Once command but cannot be read using the Read Once command. The Program Once Field in the program flash erasable IFR with indexes 0x30 - 0x33 provides 16 bytes of user data storage that can be programmed using the Program Once command and read using the Read Once command. The program flash erasable IFR is erased using the Erase All Blocks command, Erase All Blocks Unsecure command, and using the external erase all feature (mass erase).

34.3.4 Register Descriptions

The flash memory module contains a set of memory-mapped control and status registers.

NOTE

While a command is running (FSTAT[CCIF]=0), register writes are not accepted to any register except FCNFG and FSTAT. The no-write rule is relaxed during the start-up reset sequence, prior to the initial rise of CCIF. During this initialization period the user may write any register. All register writes are also disabled (except for registers FCNFG and FSTAT) whenever an erase suspend request is active (FCNFG[ERSSUSP]=1).

FTFA memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4002_0000	Flash Status Register (FTFA_FSTAT)	8	R/W	00h	34.3.4.1/ 813
4002_0001	Flash Configuration Register (FTFA_FCNFG)	8	R/W	00h	34.3.4.2/ 815
4002_0002	Flash Security Register (FTFA_FSEC)	8	R	Undefined	34.3.4.3/ 816
4002_0003	Flash Option Register (FTFA_FOPT)	8	R	Undefined	34.3.4.4/ 817

Table continues on the next page...

FTFA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4002_0004	Flash Common Command Object Registers (FTFA_FCCOB3)	8	R/W	00h	34.3.4.5/ 818
4002_0005	Flash Common Command Object Registers (FTFA_FCCOB2)	8	R/W	00h	34.3.4.5/ 818
4002_0006	Flash Common Command Object Registers (FTFA_FCCOB1)	8	R/W	00h	34.3.4.5/ 818
4002_0007	Flash Common Command Object Registers (FTFA_FCCOB0)	8	R/W	00h	34.3.4.5/ 818
4002_0008	Flash Common Command Object Registers (FTFA_FCCOB7)	8	R/W	00h	34.3.4.5/ 818
4002_0009	Flash Common Command Object Registers (FTFA_FCCOB6)	8	R/W	00h	34.3.4.5/ 818
4002_000A	Flash Common Command Object Registers (FTFA_FCCOB5)	8	R/W	00h	34.3.4.5/ 818
4002_000B	Flash Common Command Object Registers (FTFA_FCCOB4)	8	R/W	00h	34.3.4.5/ 818
4002_000C	Flash Common Command Object Registers (FTFA_FCCOBB)	8	R/W	00h	34.3.4.5/ 818
4002_000D	Flash Common Command Object Registers (FTFA_FCCOBA)	8	R/W	00h	34.3.4.5/ 818
4002_000E	Flash Common Command Object Registers (FTFA_FCCOB9)	8	R/W	00h	34.3.4.5/ 818
4002_000F	Flash Common Command Object Registers (FTFA_FCCOB8)	8	R/W	00h	34.3.4.5/ 818
4002_0010	Program Flash Protection Registers (FTFA_FPROT3)	8	R/W	Undefined	34.3.4.6/ 819
4002_0011	Program Flash Protection Registers (FTFA_FPROT2)	8	R/W	Undefined	34.3.4.6/ 819
4002_0012	Program Flash Protection Registers (FTFA_FPROT1)	8	R/W	Undefined	34.3.4.6/ 819
4002_0013	Program Flash Protection Registers (FTFA_FPROT0)	8	R/W	Undefined	34.3.4.6/ 819
4002_0018	Execute-only Access Registers (FTFA_XACCH3)	8	R	Undefined	34.3.4.7/ 821
4002_0019	Execute-only Access Registers (FTFA_XACCH2)	8	R	Undefined	34.3.4.7/ 821
4002_001A	Execute-only Access Registers (FTFA_XACCH1)	8	R	Undefined	34.3.4.7/ 821
4002_001B	Execute-only Access Registers (FTFA_XACCH0)	8	R	Undefined	34.3.4.7/ 821
4002_001C	Execute-only Access Registers (FTFA_XACCL3)	8	R	Undefined	34.3.4.7/ 821
4002_001D	Execute-only Access Registers (FTFA_XACCL2)	8	R	Undefined	34.3.4.7/ 821

Table continues on the next page...

FTFA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4002_001E	Execute-only Access Registers (FTFA_XACCL1)	8	R	Undefined	34.3.4.7/ 821
4002_001F	Execute-only Access Registers (FTFA_XACCL0)	8	R	Undefined	34.3.4.7/ 821
4002_0020	Supervisor-only Access Registers (FTFA_SACCH3)	8	R	Undefined	34.3.4.8/ 822
4002_0021	Supervisor-only Access Registers (FTFA_SACCH2)	8	R	Undefined	34.3.4.8/ 822
4002_0022	Supervisor-only Access Registers (FTFA_SACCH1)	8	R	Undefined	34.3.4.8/ 822
4002_0023	Supervisor-only Access Registers (FTFA_SACCH0)	8	R	Undefined	34.3.4.8/ 822
4002_0024	Supervisor-only Access Registers (FTFA_SACCL3)	8	R	Undefined	34.3.4.8/ 822
4002_0025	Supervisor-only Access Registers (FTFA_SACCL2)	8	R	Undefined	34.3.4.8/ 822
4002_0026	Supervisor-only Access Registers (FTFA_SACCL1)	8	R	Undefined	34.3.4.8/ 822
4002_0027	Supervisor-only Access Registers (FTFA_SACCL0)	8	R	Undefined	34.3.4.8/ 822
4002_0028	Flash Access Segment Size Register (FTFA_FACSS)	8	R	Undefined	34.3.4.9/ 823
4002_002B	Flash Access Segment Number Register (FTFA_FACSN)	8	R	Undefined	34.3.4.10/ 824

34.3.4.1 Flash Status Register (FTFA_FSTAT)

The FSTAT register reports the operational status of the flash memory module.

The CCIF, RDCOLERR, ACCERR, and FPVIOL bits are readable and writable. The MGSTAT0 bit is read only. The unassigned bits read 0 and are not writable.

NOTE

When set, the Access Error (ACCERR) and Flash Protection Violation (FPVIOL) bits in this register prevent the launch of any more commands until the flag is cleared (by writing a one to it).

Address: 4002_0000h base + 0h offset = 4002_0000h

Bit	7	6	5	4	3	2	1	0
Read	CCIF	RDCOLERR	ACCERR	FPVIOL	0			MGSTAT0
Write	w1c	w1c	w1c	w1c				
Reset	0	0	0	0	0	0	0	0

FTFA_FSTAT field descriptions

Field	Description
7 CCIF	Command Complete Interrupt Flag Indicates that a flash command has completed. The CCIF flag is cleared by writing a 1 to CCIF to launch a command, and CCIF stays low until command completion or command violation. CCIF is reset to 0 but is set to 1 by the memory controller at the end of the reset initialization sequence. Depending on how quickly the read occurs after reset release, the user may or may not see the 0 hardware reset value. 0 Flash command in progress 1 Flash command has completed
6 RDCOLERR	Flash Read Collision Error Flag Indicates that the MCU attempted a read from a flash memory resource that was being manipulated by a flash command (CCIF=0). Any simultaneous access is detected as a collision error by the block arbitration logic. The read data in this case cannot be guaranteed. The RDCOLERR bit is cleared by writing a 1 to it. Writing a 0 to RDCOLERR has no effect. 0 No collision error detected 1 Collision error detected
5 ACCERR	Flash Access Error Flag Indicates an illegal access has occurred to a flash memory resource caused by a violation of the command write sequence or issuing an illegal flash command. While ACCERR is set, the CCIF flag cannot be cleared to launch a command. The ACCERR bit is cleared by writing a 1 to ACCERR while CCIF is set. Writing a 0 to the ACCERR bit has no effect. 0 No access error detected 1 Access error detected
4 FPVIOL	Flash Protection Violation Flag Indicates an attempt was made to program or erase an address in a protected area of program flash memory during a command write sequence . While FPVIOL is set, the CCIF flag cannot be cleared to launch a command. The FPVIOL bit is cleared by writing a 1 to FPVIOL while CCIF is set. Writing a 0 to the FPVIOL bit has no effect. 0 No protection violation detected 1 Protection violation detected
3–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 MGSTAT0	Memory Controller Command Completion Status Flag The MGSTAT0 status flag is set if an error is detected during execution of a flash command or during the flash reset sequence. As a status flag, this field cannot (and need not) be cleared by the user like the other error flags in this register.

Table continues on the next page...

FTFA_FSTAT field descriptions (continued)

Field	Description
	The value of the MGSTAT0 bit for "command-N" is valid only at the end of the "command-N" execution when CCIF=1 and before the next command has been launched. At some point during the execution of "command-N+1," the previous result is discarded and any previous error is cleared.

34.3.4.2 Flash Configuration Register (FTFA_FCNFG)

This register provides information on the current functional state of the flash memory module.

The erase control bits (ERSAREQ and ERSSUSP) have write restrictions. The unassigned bits read as noted and are not writable.

Address: 4002_0000h base + 1h offset = 4002_0001h

Bit	7	6	5	4	3	2	1	0
Read	CCIE	RDCOLLIE	ERSAREQ	ERSSUSP	0	0	0	0
Write								
Reset	0	0	0	0	0	0	0	0

FTFA_FCNFG field descriptions

Field	Description
7 CCIE	Command Complete Interrupt Enable Controls interrupt generation when a flash command completes. 0 Command complete interrupt disabled 1 Command complete interrupt enabled. An interrupt request is generated whenever the FSTAT[CCIF] flag is set.
6 RDCOLLIE	Read Collision Error Interrupt Enable Controls interrupt generation when a flash memory read collision error occurs. 0 Read collision error interrupt disabled 1 Read collision error interrupt enabled. An interrupt request is generated whenever a flash memory read collision error is detected (see the description of FSTAT[RDCOLERR]).
5 ERSAREQ	Erase All Request Issues a request to the memory controller to execute the Erase All Blocks command and release security. ERSAREQ is not directly writable but is under indirect user control. Refer to the device's Chip Configuration details on how to request this command. ERSAREQ sets when an erase all request is triggered external to the flash memory module and CCIF is set (no command is currently being executed). ERSAREQ is cleared by the flash memory module when the operation completes. 0 No request or request complete 1 Request to: 1. run the Erase All Blocks command,

Table continues on the next page...

FTFA_FCNFG field descriptions (continued)

Field	Description
	2. verify the erased state, 3. program the security byte in the Flash Configuration Field to the unsecure state, and 4. release MCU security by setting the FSEC[SEC] field to the unsecure state.
4 ERSSUSP	Erase Suspend Allows the user to suspend (interrupt) the Erase Flash Sector command while it is executing. 0 No suspend requested 1 Suspend the current Erase Flash Sector command execution.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

34.3.4.3 Flash Security Register (FTFA_FSEC)

This read-only register holds all bits associated with the security of the MCU and flash memory module.

During the reset sequence, the register is loaded with the contents of the flash security byte in the Flash Configuration Field located in program flash memory. The flash basis for the values is signified by X in the reset value.

Address: 4002_0000h base + 2h offset = 4002_0002h

Bit	7	6	5	4	3	2	1	0
Read	KEYEN		MEEN		FSLACC		SEC	
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

FTFA_FSEC field descriptions

Field	Description
7–6 KEYEN	Backdoor Key Security Enable Enables or disables backdoor key access to the flash memory module. 00 Backdoor key access disabled 01 Backdoor key access disabled (preferred KEYEN state to disable backdoor key access)

Table continues on the next page...

FTFA_FSEC field descriptions (continued)

Field	Description
	10 Backdoor key access enabled 11 Backdoor key access disabled
5–4 MEEN	Mass Erase Enable Enables and disables mass erase capability of the flash memory module. The state of this field is relevant only when SEC is set to secure. When SEC is set to unsecure, the MEEN setting does not matter. 00 Mass erase is enabled 01 Mass erase is enabled 10 Mass erase is disabled 11 Mass erase is enabled
3–2 FSLACC	Freescale Failure Analysis Access Code Enables or disables access to the flash memory contents during returned part failure analysis at Freescale. When SEC is secure and FSLACC is denied, access to the program flash contents is denied and any failure analysis performed by Freescale factory test must begin with a full erase to unsecure the part. When access is granted (SEC is unsecure, or SEC is secure and FSLACC is granted), Freescale factory testing has visibility of the current flash contents. The state of the FSLACC bits is only relevant when SEC is set to secure. When SEC is set to unsecure, the FSLACC setting does not matter. 00 Freescale factory access granted 01 Freescale factory access denied 10 Freescale factory access denied 11 Freescale factory access granted
SEC	Flash Security Defines the security state of the MCU. In the secure state, the MCU limits access to flash memory module resources. The limitations are defined per device and are detailed in the Chip Configuration details. If the flash memory module is unsecured using backdoor key access, SEC is forced to 10b. 00 MCU security status is secure. 01 MCU security status is secure. 10 MCU security status is unsecure. (The standard shipping condition of the flash memory module is unsecure.) 11 MCU security status is secure.

34.3.4.4 Flash Option Register (FTFA_FOPT)

The flash option register allows the MCU to customize its operations by examining the state of these read-only bits, which are loaded from NVM at reset. The function of the bits is defined in the device's Chip Configuration details.

All bits in the register are read-only .

During the reset sequence, the register is loaded from the flash nonvolatile option byte in the Flash Configuration Field located in program flash memory. The flash basis for the values is signified by X in the reset value. However, the register is written to 0xFF if the contents of the flash nonvolatile option byte are 0x00.

Address: 4002_0000h base + 3h offset = 4002_0003h

Bit	7	6	5	4	3	2	1	0
Read	OPT							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

FTFA_FOPT field descriptions

Field	Description
OPT	Nonvolatile Option These bits are loaded from flash to this register at reset. Refer to the device's Chip Configuration details for the definition and use of these bits.

34.3.4.5 Flash Common Command Object Registers (FTFA_FCCOB*n*)

The FCCOB register group provides 12 bytes for command codes and parameters. The individual bytes within the set append a 0-B hex identifier to the FCCOB register name: FCCOB0, FCCOB1, ..., FCCOBB.

Address: 4002_0000h base + 4h offset + (1d × i), where i=0d to 11d

Bit	7	6	5	4	3	2	1	0
Read Write	CCOBn							
Reset	0	0	0	0	0	0	0	0

FTFA_FCCOB*n* field descriptions

Field	Description
CCOBn	The FCCOB register provides a command code and relevant parameters to the memory controller. The individual registers that compose the FCCOB data set can be written in any order, but you must provide all needed values, which vary from command to command. First, set up all required FCCOB fields and then initiate the command's execution by writing a 1 to the FSTAT[CCIF] bit. This clears the CCIF bit, which locks all FCCOB parameter fields and they cannot be changed by the user until the command completes (CCIF returns to 1). No command buffering or queueing is provided; the next command can be loaded only after the current command completes. Some commands return information to the FCCOB registers. Any values returned to FCCOB are available for reading after the FSTAT[CCIF] flag returns to 1 by the memory controller.

FTFA_FCCOB*n* field descriptions (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td></td><td>
The following table shows a generic flash command format. The first FCCOB register, FCCOB0, always contains the command code. This 8-bit value defines the command to be executed. The command code is followed by the parameters required for this specific flash command, typically an address and/or data values.

NOTE: The command parameter table is written in terms of FCCOB Number (which is equivalent to the byte number). This number is a reference to the FCCOB register name and is not the register address.
<table>
<tr><th>FCCOB Number</th><th>Typical Command Parameter Contents [7:0]</th></tr>
<tr><td>0</td><td>FCMD (a code that defines the flash command)</td></tr>
<tr><td>1</td><td>Flash address [23:16]</td></tr>
<tr><td>2</td><td>Flash address [15:8]</td></tr>
<tr><td>3</td><td>Flash address [7:0]</td></tr>
<tr><td>4</td><td>Data Byte 0</td></tr>
<tr><td>5</td><td>Data Byte 1</td></tr>
<tr><td>6</td><td>Data Byte 2</td></tr>
<tr><td>7</td><td>Data Byte 3</td></tr>
<tr><td>8</td><td>Data Byte 4</td></tr>
<tr><td>9</td><td>Data Byte 5</td></tr>
<tr><td>A</td><td>Data Byte 6</td></tr>
<tr><td>B</td><td>Data Byte 7</td></tr>
</table>
FCCOB Endianness and Multi-Byte Access :

The FCCOB register group uses a big endian addressing convention. For all command parameter fields larger than 1 byte, the most significant data resides in the lowest FCCOB register number. The FCCOB register group may be read and written as individual bytes, aligned words (2 bytes) or aligned longwords (4 bytes).
</td></tr>
</table>

34.3.4.6 Program Flash Protection Registers (FTFA_FPROT*n*)

The FPROT registers define which program flash regions are protected from program and erase operations. Protected flash regions cannot have their content changed; that is, these regions cannot be programmed and cannot be erased by any flash command. Unprotected regions can be changed by program and erase operations.

The four FPROT registers allow up to 32 protectable regions. Each bit protects a 1/32 region of the program flash memory except for memory configurations with less than 128 KB of program flash where each assigned bit protects 4 KB. For configurations with 96 KB of program flash memory or less, FPROT0 is not used. For configurations with 64

KB of program flash memory or less, FPROT1 is not used. For configurations with 32 KB of program flash memory, FPROT2 is not used. The bitfields are defined in each register as follows:

Program flash protection register	Program flash protection bits
FPROT0	PROT[31:24]
FPROT1	PROT[23:16]
FPROT2	PROT[15:8]
FPROT3	PROT[7:0]

During the reset sequence, the FPROT registers are loaded with the contents of the program flash protection bytes in the Flash Configuration Field as indicated in the following table.

Program flash protection register	Flash Configuration Field offset address
FPROT0	0x000B
FPROT1	0x000A
FPROT2	0x0009
FPROT3	0x0008

To change the program flash protection that is loaded during the reset sequence, unprotect the sector of program flash memory that contains the Flash Configuration Field. Then, reprogram the program flash protection byte.

Address: 4002_0000h base + 10h offset + (1d × i), where i=0d to 3d

Bit	7	6	5	4	3	2	1	0
Read Write	PROT							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

FTFA_FPROT*n* field descriptions

Field	Description
PROT	Program Flash Region Protect Each program flash region can be protected from program and erase operations by setting the associated PROT bit. **In NVM Normal mode:** The protection can only be increased, meaning that currently unprotected memory can be protected, but currently protected memory cannot be unprotected. Since unprotected regions are marked with a 1 and protected regions use a 0, only writes changing 1s to 0s are accepted. This 1-to-0 transition check is performed on a bit-by-bit basis. Those FPROT bits with 1-to-0 transitions are accepted while all bits with 0-to-1 transitions are ignored.

FTFA_FPROT*n* field descriptions (continued)

Field	Description
	In NVM Special mode: All bits of FPROT are writable without restriction. Unprotected areas can be protected and protected areas can be unprotected. **Restriction:** The user must never write to any FPROT register while a command is running (CCIF=0). Trying to alter data in any protected area in the program flash memory results in a protection violation error and sets the FSTAT[FPVIOL] bit. A full block erase of a program flash block is not possible if it contains any protected region. Each bit in the 32-bit protection register represents 1/32 of the total program flash except for memory configurations with less than 128 KB of program flash where each assigned bit protects 4 KB. 0 Program flash region is protected. 1 Program flash region is not protected

34.3.4.7 Execute-only Access Registers (FTFA_XACC*n*)

The XACC registers define which program flash segments are restricted to data read or execute only or both data and instruction fetches.

The eight XACC registers allow up to 64 restricted segments of equal memory size.

Execute-only access register	Program flash execute-only access bits
XACCH0	XA[63:56]
XACCH1	XA[55:48]
XACCH2	XA[47:40]
XACCH3	XA[39:32]
XACCL0	XA[31:24]
XACCL1	XA[23:16]
XACCL2	XA[15:8]
XACCL3	XA[7:0]

During the reset sequence, the XACC registers are loaded with the logical AND of Program Flash IFR addresses A and B as indicated in the following table.

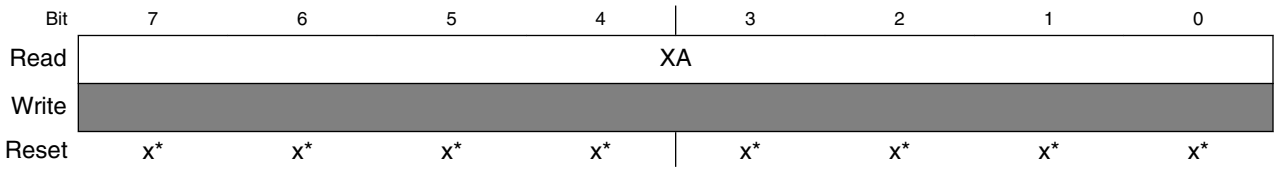
Execute-only access register	Program Flash IFR address A	Program Flash IFR address B
XACCH0	0xA3	0xAB
XACCH1	0xA2	0xAA
XACCH2	0xA1	0xA9
XACCH3	0xA0	0xA8
XACCL0	0xA7	0xAF
XACCL1	0xA6	0xAE
XACCL2	0xA5	0xAD

Table continues on the next page...

Execute-only access register	Program Flash IFR address A	Program Flash IFR address B
XACCL3	0xA4	0xAC

Use the Program Once command to program the execute-only access control fields that are loaded during the reset sequence.

Address: 4002_0000h base + 18h offset + (1d × i), where i=0d to 7d



* Notes:
- x = Undefined at reset.

FTFA_XACC*n* field descriptions

Field	Description
XA	Execute-only access control 0 Associated segment is accessible in execute mode only (as an instruction fetch) 1 Associated segment is accessible as data or in execute mode

34.3.4.8 Supervisor-only Access Registers (FTFA_SACC*n*)

The SACC registers define which program flash segments are restricted to supervisor only or user and supervisor access.

The eight SACC registers allow up to 64 restricted segments of equal memory size.

Supervisor-only access register	Program flash supervisor-only access bits
SACCH0	SA[63:56]
SACCH1	SA[55:48]
SACCH2	SA[47:40]
SACCH3	SA[39:32]
SACCL0	SA[31:24]
SACCL1	SA[23:16]
SACCL2	SA[15:8]
SACCL3	SA[7:0]

During the reset sequence, the SACC registers are loaded with the logical AND of Program Flash IFR addresses A and B as indicated in the following table.

Supervisor-only access register	Program Flash IFR address A	Program Flash IFR address B
SACCH0	0xB3	0xBB
SACCH1	0xB2	0xBA
SACCH2	0xB1	0xB9
SACCH3	0xB0	0xB8
SACCL0	0xB7	0xBF
SACCL1	0xB6	0xBE
SACCL2	0xB5	0xBD
SACCL3	0xB4	0xBC

Use the Program Once command to program the supervisor-only access control fields that are loaded during the reset sequence.

Address: 4002_0000h base + 20h offset + (1d × i), where i=0d to 7d

Bit	7	6	5	4	3	2	1	0
Read	SA							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

FTFA_SACC*n* field descriptions

Field	Description
SA	Supervisor-only access control 0 Associated segment is accessible in supervisor mode only 1 Associated segment is accessible in user or supervisor mode

34.3.4.9 Flash Access Segment Size Register (FTFA_FACSS)

The flash access segment size register determines which bits in the address are used to index into the SACC and XACC bitmaps to get the appropriate permission flags.

All bits in the register are read-only.

The contents of this register are loaded during the reset sequence.

Address: 4002_0000h base + 28h offset = 4002_0028h

Bit	7	6	5	4	3	2	1	0
Read	SGSIZE							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

FTFA_FACSS field descriptions

Field	Description
SGSIZE	Segment Size The segment size is a fixed value based on the available program flash size divided by NUMSG. Program Flash Size / Segment Size / Segment Size Encoding 64 KBytes / 2 KBytes / 0x3 128 KBytes / 4 KBytes / 0x4 160 KBytes / 4 KBytes / 0x4 256 KBytes / 4 KBytes / 0x4 512 KBytes / 8 KBytes / 0x5

34.3.4.10 Flash Access Segment Number Register (FTFA_FACSN)

The flash access segment number register provides the number of program flash segments that are available for XACC and SACC permissions.

All bits in the register are read-only.

The contents of this register are loaded during the reset sequence.

Address: 4002_0000h base + 2Bh offset = 4002_002Bh

Bit	7	6	5	4	3	2	1	0
Read	NUMSG							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

FTFA_FACSN field descriptions

Field	Description
NUMSG	Number of Segments Indicator The NUMSG field indicates the number of equal-sized segments in the program flash. 0x20 Program flash memory is divided into 32 segments (64 Kbytes, 128 Kbytes) 0x28 Program flash memory is divided into 40 segments (160 Kbytes) 0x40 Program flash memory is divided into 64 segments (256 Kbytes, 512 Kbytes)

FTFA_FACSN field descriptions (continued)

Field	Description

34.4 Functional Description

The information found here describes functional details of the flash memory module.

34.4.1 Flash Protection

Individual regions within the flash memory can be protected from program and erase operations.

Protection is controlled by the following registers:

- FPROT*n* —
  - For 2^n program flash sizes, four registers typically protect 32 regions of the program flash memory as shown in the following figure

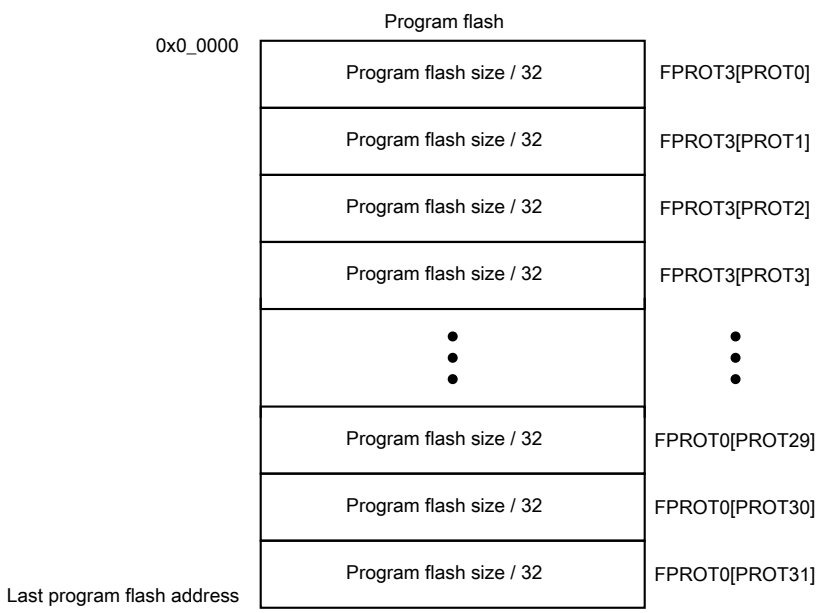


Figure 34-2. Program flash protection

NOTE

Flash protection features are discussed further in AN4507: Using the Kinetis Security and Flash Protection Features . Not all features described in the application note are available on this device.

34.4.2 Flash Access Protection

Individual segments within the program flash memory can be designated for restricted access. Specific flash commands (Program Check, Program Longword, Erase Flash Sector) monitor FXACC contents to protect flash memory but the FSACC contents do not impact flash command operation. Access is controlled by the following registers:

- FTFA_XACC —
  - For 2^n program flash sizes greater than 128KB, eight registers control 64 segments of the program flash memory as shown in the following figure

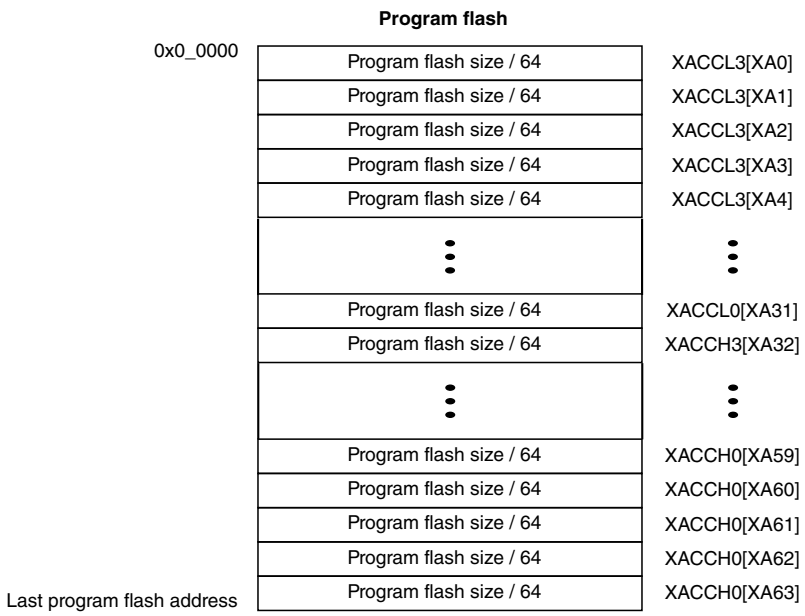


Figure 34-3. Program flash access control (256KB or 512KB of program flash)

- FTFA_SACC —
  - For 2^n program flash sizes greater than 128KB, eight registers control 64 segments of the program flash memory as shown in the following figure

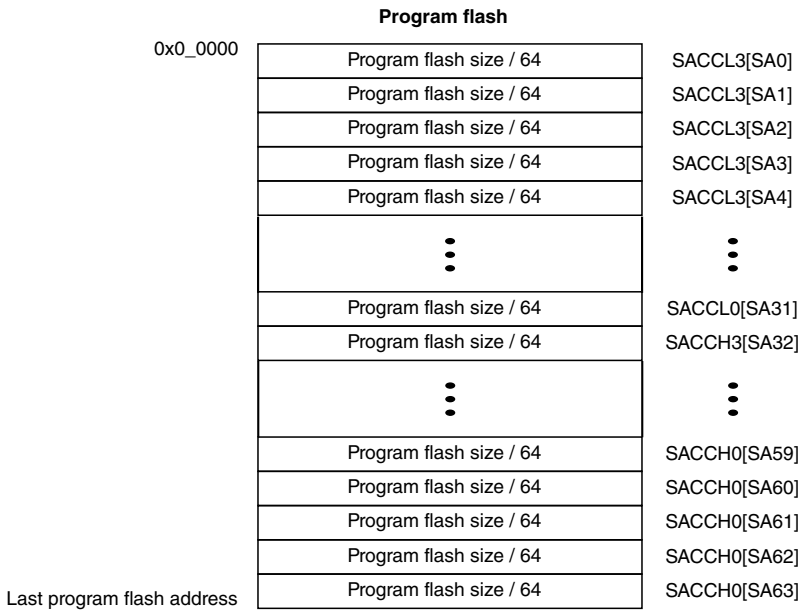


Figure 34-4. Program flash access control (256KB or 512KB of program flash)

34.4.3 Interrupts

The flash memory module can generate interrupt requests to the MCU upon the occurrence of various flash events.

These interrupt events and their associated status and control bits are shown in the following table.

Table 34-1. Flash Interrupt Sources

Flash Event	Readable Status Bit	Interrupt Enable Bit
Flash Command Complete	FSTAT[CCIF]	FCNFG[CCIE]
Flash Read Collision Error	FSTAT[RDCOLERR]	FCNFG[RDCOLLIE]

Note

Vector addresses and their relative interrupt priority are determined at the MCU level.

Some devices also generate a bus error response as a result of a Read Collision Error event. See the chip configuration information to determine if a bus error response is also supported.

34.4.4 Flash Operation in Low-Power Modes

34.4.4.1 Wait Mode

When the MCU enters wait mode, the flash memory module is not affected. The flash memory module can recover the MCU from wait via the command complete interrupt (see Interrupts).

34.4.4.2 Stop Mode

When the MCU requests stop mode, if a flash command is active (CCIF = 0) the command execution completes before the MCU is allowed to enter stop mode.

CAUTION

The MCU should never enter stop mode while any flash command is running (CCIF = 0).

NOTE

While the MCU is in very-low-power modes (VLPR, VLPW, VLPS), the flash memory module does not accept flash commands.

34.4.5 Functional Modes of Operation

The flash memory module has two operating modes: NVM Normal and NVM Special.

The operating mode affects the command set availability (see Table 34-2). Refer to the Chip Configuration details of this device for how to activate each mode.

34.4.6 Flash Reads and Ignored Writes

The flash memory module requires only the flash address to execute a flash memory read.

The MCU must not read from the flash memory while commands are running (as evidenced by CCIF=0) on that block. Read data cannot be guaranteed from a flash block while any command is processing within that block. The block arbitration logic detects any simultaneous access and reports this as a read collision error (see the FSTAT[RDCOLERR] bit).

34.4.7 Read While Write (RWW)

The following simultaneous accesses are not allowed:

- Reading from program flash memory space while a flash command is active (CCIF=0).

34.4.8 Flash Program and Erase

All flash functions except read require the user to setup and launch a flash command through a series of peripheral bus writes.

The user cannot initiate any further flash commands until notified that the current command has completed. The flash command structure and operation are detailed in Flash Command Operations.

34.4.9 Flash Command Operations

Flash command operations are typically used to modify flash memory contents.

The next sections describe:

- The command write sequence used to set flash command parameters and launch execution
- A description of all flash commands available

34.4.9.1 Command Write Sequence

Flash commands are specified using a command write sequence illustrated in Figure 34-5. The flash memory module performs various checks on the command (FCCOB) content and continues with command execution if all requirements are fulfilled.

Before launching a command, the ACCERR and FPVIOL bits in the FSTAT register must be zero and the CCIF flag must read 1 to verify that any previous command has completed. If CCIF is zero, the previous command execution is still active, a new command write sequence cannot be started, and all writes to the FCCOB registers are ignored.

Attempts to launch a flash command in VLP mode will be ignored. Attempts to launch a flash command in HSRUN mode will be trapped with the ACCERR flag being set.

34.4.9.1.1 Load the FCCOB Registers

The user must load the FCCOB registers with all parameters required by the desired flash command. The individual registers that make up the FCCOB data set can be written in any order.

34.4.9.1.2 Launch the Command by Clearing CCIF

Once all relevant command parameters have been loaded, the user launches the command by clearing FSTAT[CCIF] by writing a '1' to it. FSTAT[CCIF] remains 0 until the flash command completes.

The FSTAT register contains a blocking mechanism that prevents a new command from launching (can't clear FSTAT[CCIF]) if the previous command resulted in an access error (FSTAT[ACCERR]=1) or a protection violation (FSTAT[FPVIOL]=1). In error scenarios, two writes to FSTAT are required to initiate the next command: the first write clears the error flags, the second write clears CCIF.

34.4.9.1.3 Command Execution and Error Reporting

The command processing has several steps:

1. The flash memory module reads the command code and performs a series of parameter checks and protection checks, if applicable, which are unique to each command.

   If the parameter check fails, the FSTAT[ACCERR] (access error) flag is set. FSTAT[ACCERR] reports invalid instruction codes and out-of bounds addresses. Usually, access errors suggest that the command was not set-up with valid parameters in the FCCOB register group.

   Program and erase commands also check the address to determine if the operation is requested to execute on protected areas. If the protection check fails, FSTAT[FPVIOL] (protection error) flag is set.

Command processing never proceeds to execution when the parameter or protection step fails. Instead, command processing is terminated after setting FSTAT[CCIF].

2. If the parameter and protection checks pass, the command proceeds to execution. Run-time errors, such as failure to erase verify, may occur during the execution phase. Run-time errors are reported in FSTAT[MGSTAT0]. A command may have access errors, protection errors, and run-time errors, but the run-time errors are not seen until all access and protection errors have been corrected.
3. Command execution results, if applicable, are reported back to the user via the FCCOB and FSTAT registers.
4. The flash memory module sets FSTAT[CCIF] signifying that the command has completed.

The flow for a generic command write sequence is illustrated in the following figure.

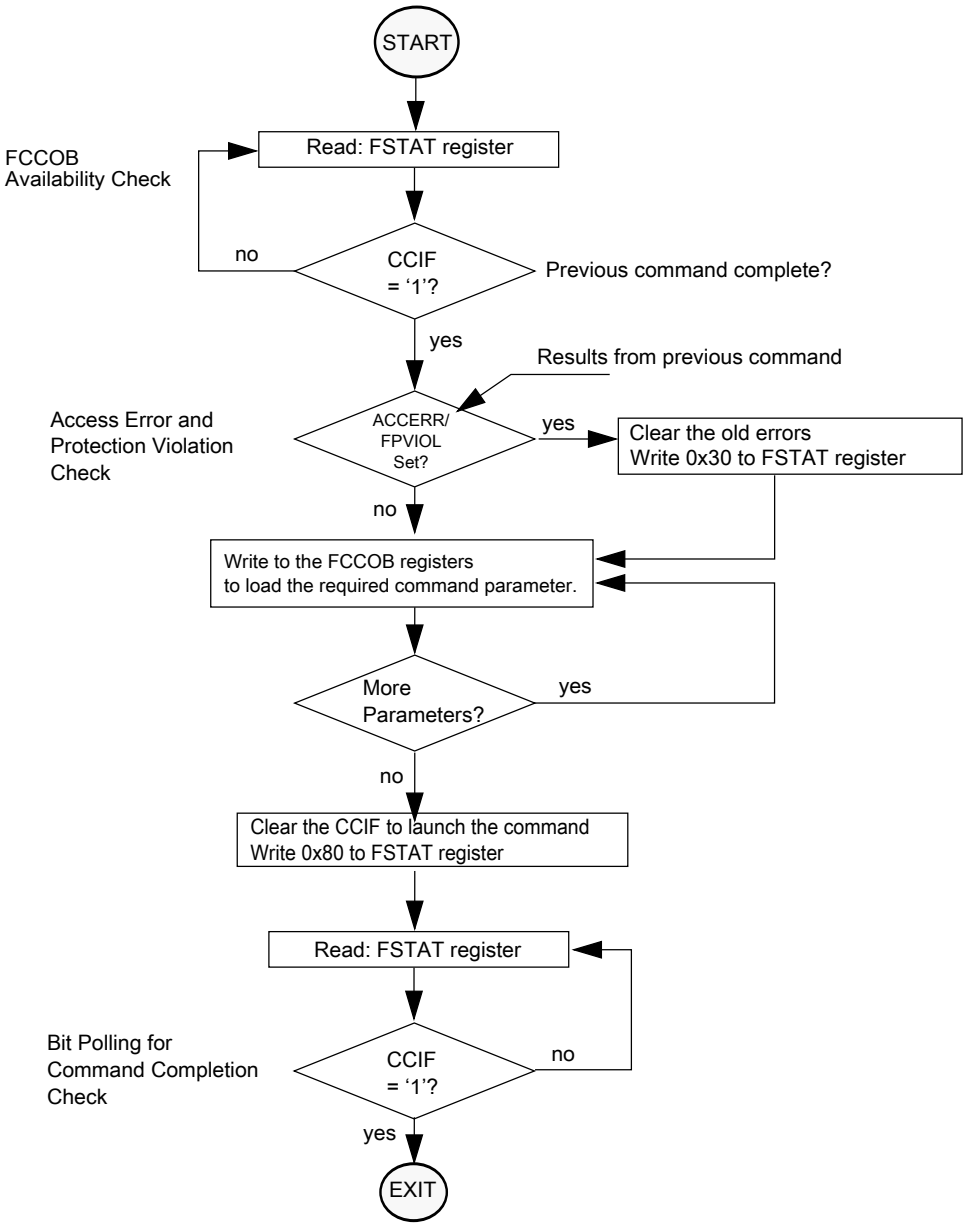


Figure 34-5. Generic flash command write sequence flowchart

34.4.9.2 Flash Commands

The following table summarizes the function of all flash commands.

FCMD	Command	Program flash	Function
0x01	Read 1s Section	×	Verify that a given number of program flash locations from a starting address are erased.

Table continues on the next page...

FCMD	Command	Program flash	Function
0x02	Program Check	×	Tests previously-programmed locations at margin read levels.
0x03	Read Resource	IFR, ID	Read 4 bytes from program flash IFR or version ID.
0x06	Program Longword	×	Program 4 bytes in a program flash block.
0x09	Erase Flash Sector	×	Erase all bytes in a program flash sector.
0x40	Read 1s All Blocks	×	Verify that the program flash block is erased then release MCU security.
0x41	Read Once	IFR	Read 4 bytes of a dedicated 64 byte field in the program flash 0 IFR.
0x43	Program Once	IFR	One-time program of 4 bytes of a dedicated 64-byte field in the program flash 0 IFR.
0x44	Erase All Blocks	×	Erase the program flash block, verify-erase and release MCU security. **NOTE:** An erase is only possible when all memory locations are unprotected.
0x45	Verify Backdoor Access Key	×	Release MCU security after comparing a set of user-supplied security keys to those stored in the program flash.
0x49	Erase All Blocks Unsecure	×	Erase the program flash block, verify-erase, program security byte to unsecure state, release MCU security.

34.4.9.3 Flash Commands by Mode

The following table shows the flash commands that can be executed in each flash operating mode.

Table 34-2. Flash Commands by Mode

FCMD	Command	NVM Normal			NVM Special		
		Unsecure	Secure	MEEN=10	Unsecure	Secure	MEEN=10
0x01	Read 1s Section	×	×	×	×	—	—
0x02	Program Check	×	×	×	×	—	—
0x03	Read Resource	×	×	×	×	—	—

Table continues on the next page...

Table 34-2. Flash Commands by Mode (continued)

FCMD	Command	NVM Normal			NVM Special		
		Unsecure	Secure	MEEN=10	Unsecure	Secure	MEEN=10
0x06	Program Longword	×	×	×	×	—	—
0x09	Erase Flash Sector	×	×	×	×	—	—
0x40	Read 1s All Blocks	×	×	×	×	×	—
0x41	Read Once	×	×	×	×	—	—
0x43	Program Once	×	×	×	×	—	—
0x44	Erase All Blocks	×	×	×	×	×	—
0x45	Verify Backdoor Access Key	×	×	×	×	—	—
0x49	Erase All Blocks Unsecure	×	×	—	×	×	—

34.4.10 Margin Read Commands

The Read-1s commands (Read 1s All Blocks, Read 1s Section) and the Program Check command have a margin choice parameter that allows the user to apply non-standard read reference levels to the program flash array reads performed by these commands. Using the preset 'user' and 'factory' margin levels, these commands perform their associated read operations at tighter tolerances than a 'normal' read. These non-standard read levels are applied only during the command execution. Basic flash array reads use the standard, un-margined, read reference level.

Only the 'normal' read level should be employed during normal flash usage. The non-standard, 'user' and 'factory' margin levels should be employed only in special cases. They can be used during special diagnostic routines to gain confidence that the device is not suffering from the end-of-life data loss customary of flash memory devices.

Erased ('1') and programmed ('0') bit states can degrade due to elapsed time and data cycling (number of times a bit is erased and re-programmed). The lifetime of the erased states is relative to the last erase operation. The lifetime of the programmed states is measured from the last program time.

The 'user' and 'factory' levels become, in effect, a minimum safety margin; i.e. if the reads pass at the tighter tolerances of the 'user' and 'factory' margins, then the 'normal' reads have at least this much safety margin before they experience data loss.

The 'user' margin is a small delta to the normal read reference level. 'User' margin levels can be employed to check that flash memory contents have adequate margin for normal level read operations. If unexpected read results are encountered when checking flash memory contents at the 'user' margin levels, loss of information might soon occur during 'normal' readout.

The 'factory' margin is a bigger deviation from the norm, a more stringent read criteria that should only be attempted immediately (or very soon) after completion of an erase or program command, early in the cycling life. 'Factory' margin levels can be used to check that flash memory contents have adequate margin for long-term data retention at the normal level setting. If unexpected results are encountered when checking flash memory contents at 'factory' margin levels, the flash memory contents should be erased and reprogrammed.

CAUTION

Factory margin levels must only be used during verify of the initial factory programming.

34.4.11 Flash Command Description

This section describes all flash commands that can be launched by a command write sequence.

The flash memory module sets the FSTAT[ACCERR] bit and aborts the command execution if any of the following illegal conditions occur:

- There is an unrecognized command code in the FCCOB FCMD field.
- There is an error in a FCCOB field for the specific commands. Refer to the error handling table provided for each command.

Ensure that FSTAT[ACCERR] and FSTAT[FPVIOL] are cleared prior to starting the command write sequence. As described in Launch the Command by Clearing CCIF, a new command cannot be launched while these error flags are set.

Do not attempt to read a flash block while the flash memory module is running a command (FSTAT[CCIF] = 0) on that same block. The flash memory module may return invalid data to the MCU with the collision error flag (FSTAT[RDCOLERR]) set.

CAUTION

Flash data must be in the erased state before being programmed. Cumulative programming of bits (adding more zeros) is not allowed.

34.4.11.1 Read 1s Section Command

The Read 1s Section command checks if a section of program flash memory is erased to the specified read margin level. The Read 1s Section command defines the starting address and the number of double-phrases to be verified.

Table 34-3. Read 1s Section Command FCCOB Requirements

FCCOB Number	FCCOB Contents [7:0]
0	0x01 (RD1SEC)
1	Flash address [23:16] of the first double-phrase to be verified
2	Flash address [15:8] of the first double-phrase to be verified
3	Flash address [7:0][1] of the first double-phrase to be verified
4	Number of double-phrases to be verified [15:8]
5	Number of double-phrases to be verified [7:0]
6	Read-1 Margin Choice

1. Must be double-phrase aligned (Flash address [3:0] = 0000).

Upon clearing CCIF to launch the Read 1s Section command, the flash memory module sets the read margin for 1s according to Table 34-4 and then reads all locations within the specified section of flash memory. If the flash memory module fails to read all 1s (that is, the flash section is not erased), FSTAT[MGSTAT0] is set. FSTAT[CCIF] sets after the Read 1s Section operation completes.

Table 34-4. Margin Level Choices for Read 1s Section

Read Margin Choice	Margin Level Description
0x00	Use the 'normal' read level for 1s
0x01	Apply the 'User' margin to the normal read-1 level
0x02	Apply the 'Factory' margin to the normal read-1 level

Table 34-5. Read 1s Section Command Error Handling

Error condition	Error bit
Command not available in current mode/security	FSTAT[ACCERR]
An invalid margin code is supplied.	FSTAT[ACCERR]
An invalid flash address is supplied.	FSTAT[ACCERR]
Flash address is not double-phrase aligned.	FSTAT[ACCERR]
The requested section crosses a Flash block boundary.	FSTAT[ACCERR]
The requested number of double-phrases is 0.	FSTAT[ACCERR]
Read-1s fails.	FSTAT[MGSTAT0]

34.4.11.2 Program Check Command

The Program Check command tests a previously programmed program flash longword to see if it reads correctly at the specified margin level.

Table 34-6. Program Check Command FCCOB Requirements

FCCOB Number	FCCOB Contents [7:0]
0	0x02 (PGMCHK)
1	Flash address [23:16]
2	Flash address [15:8]
3	Flash address [7:0][1]
4	Margin Choice
8	Byte 0 expected data
9	Byte 1 expected data
A	Byte 2 expected data
B	Byte 3 expected data

1. Must be longword aligned (Flash address [1:0] = 00).

Upon clearing CCIF to launch the Program Check command, the flash memory module sets the read margin for 1s according to Table 34-7, reads the specified longword, and compares the actual read data to the expected data provided by the FCCOB. If the comparison at margin-1 fails, FSTAT[MGSTAT0] is set.

The flash memory module then sets the read margin for 0s, re-reads, and compares again. If the comparison at margin-0 fails, FSTAT[MGSTAT0] is set. FSTAT[CCIF] is set after the Program Check operation completes.

The supplied address must be longword aligned (the lowest two bits of the byte address must be 00):

- Byte 3 data is written to the supplied byte address ('start'),
- Byte 2 data is programmed to byte address start+0b01,
- Byte 1 data is programmed to byte address start+0b10,
- Byte 0 data is programmed to byte address start+0b11.

NOTE

See the description of margin reads, Margin Read Commands

Table 34-7. Margin Level Choices for Program Check

Read Margin Choice	Margin Level Description
0x01	Read at 'User' margin-1 and 'User' margin-0
0x02	Read at 'Factory' margin-1 and 'Factory' margin-0

Table 34-8. Program Check Command Error Handling

Error Condition	Error Bit
Command not available in current mode/security	FSTAT[ACCERR]
An invalid flash address is supplied	FSTAT[ACCERR]
Flash address is not longword aligned	FSTAT[ACCERR]
An invalid margin choice is supplied	FSTAT[ACCERR]
Flash address is located in an XA controlled segment and the Erase All Blocks, Erase All Blocks Unsecure or the Read 1s All Blocks command has not successfully completed since the last reset	FSTAT[FPVIOL]
Either of the margin reads does not match the expected data	FSTAT[MGSTAT0]

34.4.11.3 Read Resource Command

The Read Resource command allows the user to read data from special-purpose memory resources located within the flash memory module. The special-purpose memory resources available include program flash IFR space and the Version ID field. Each resource is assigned a select code as shown in Table 34-10.

Table 34-9. Read Resource Command FCCOB Requirements

FCCOB Number	FCCOB Contents [7:0]
0	0x03 (RDRSRC)
1	Flash address [23:16]
2	Flash address [15:8]
3	Flash address [7:0][1]
Returned Values	
4	Read Data [31:24]
5	Read Data [23:16]
6	Read Data [15:8]
7	Read Data [7:0]
User-provided values	
8	Resource Select Code (see Table 34-10)

1. Must be longword aligned (Flash address [1:0] = 00).

Table 34-10. Read Resource Select Codes

Resource Select Code	Description	Resource Size	Local Address Range
0x00	Program Flash 0 IFR	256 Bytes	0x00_0000–0x00_00FF
0x01[1]	Version ID	8 Bytes	0x00_0000–0x00_0007

1. Located in program flash 0 reserved space.

After clearing CCIF to launch the Read Resource command, four consecutive bytes are read from the selected resource at the provided relative address and stored in the FCCOB register. The CCIF flag sets after the Read Resource operation completes. The Read Resource command exits with an access error if an invalid resource code is provided or if the address for the applicable area is out-of-range.

Table 34-11. Read Resource Command Error Handling

Error Condition	Error Bit
Command not available in current mode/security	FSTAT[ACCERR]
An invalid resource code is entered	FSTAT[ACCERR]
Flash address is out-of-range for the targeted resource.	FSTAT[ACCERR]
Flash address is not longword aligned	FSTAT[ACCERR]

34.4.11.4 Program Longword Command

The Program Longword command programs four previously-erased bytes in the program flash memory using an embedded algorithm.

CAUTION

A flash memory location must be in the erased state before being programmed. Cumulative programming of bits (back-to-back program operations without an intervening erase) within a flash memory location is not allowed. Re-programming of existing 0s to 0 is not allowed as this overstresses the device.

Table 34-12. Program Longword Command FCCOB Requirements

FCCOB Number	FCCOB Contents [7:0]
0	0x06 (PGM4)
1	Flash address [23:16]
2	Flash address [15:8]
3	Flash address [7:0][1]
4	Byte 0 program value
5	Byte 1 program value
6	Byte 2 program value
7	Byte 3 program value

1. Must be longword aligned (Flash address [1:0] = 00).

Upon clearing CCIF to launch the Program Longword command, the flash memory module programs the data bytes into the flash using the supplied address. The targeted flash locations must be currently unprotected (see the description of the FPROT registers) to permit execution of the Program Longword operation.

The programming operation is unidirectional. It can only move NVM bits from the erased state ('1') to the programmed state ('0'). Erased bits that fail to program to the '0' state are flagged as errors in FSTAT[MGSTAT0]. The CCIF flag is set after the Program Longword operation completes.

The supplied address must be longword aligned (flash address [1:0] = 00):

- Byte 3 data is written to the supplied byte address ('start'),
- Byte 2 data is programmed to byte address start+0b01,
- Byte 1 data is programmed to byte address start+0b10, and
- Byte 0 data is programmed to byte address start+0b11.

Table 34-13. Program Longword Command Error Handling

Error Condition	Error Bit
Command not available in current mode/security	FSTAT[ACCERR]
An invalid flash address is supplied	FSTAT[ACCERR]
Flash address is not longword aligned	FSTAT[ACCERR]
Flash address points to a protected area	FSTAT[FPVIOL]
Flash address is located in an XA controlled segment and the Erase All Blocks, Erase All Blocks Unsecure or the Read 1s All Blocks command has not successfully completed since the last reset	FSTAT[FPVIOL]
Any errors have been encountered during the verify operation	FSTAT[MGSTAT0]

34.4.11.5 Erase Flash Sector Command

The Erase Flash Sector operation erases all addresses in a flash sector.

Table 34-14. Erase Flash Sector Command FCCOB Requirements

FCCOB Number	FCCOB Contents [7:0]
0	0x09 (ERSSCR)
1	Flash address [23:16] in the flash sector to be erased
2	Flash address [15:8] in the flash sector to be erased
3	Flash address [7:0][1] in the flash sector to be erased

1. Must be double-phrase aligned (flash address [3:0] = 0000).

After clearing CCIF to launch the Erase Flash Sector command, the flash memory module erases the selected program flash sector and then verifies that it is erased. The Erase Flash Sector command aborts if the selected sector is protected (see the description of the FPROT registers). If the erase-verify fails the FSTAT[MGSTAT0] bit is set. The CCIF flag is set after the Erase Flash Sector operation completes. The Erase Flash Sector command is suspendable (see the FCNFG[ERSSUSP] bit and Figure 34-6).

Table 34-15. Erase Flash Sector Command Error Handling

Error Condition	Error Bit
Command not available in current mode/security	FSTAT[ACCERR]
An invalid Flash address is supplied	FSTAT[ACCERR]
Flash address is not double-phrase aligned	FSTAT[ACCERR]
The selected program flash sector is protected	FSTAT[FPVIOL]
The selected program flash sector is located in an XA controlled segment and the Erase All Blocks, Erase All Blocks Unsecure or the Read 1s All Blocks command has not successfully completed since the last reset	FSTAT[FPVIOL]
Any errors have been encountered during the verify operation[1]	FSTAT[MGSTAT0]

1. User margin read may be run using the Read 1s Section command to verify all bits are erased.

34.4.11.5.1 Suspending an Erase Flash Sector Operation

To suspend an Erase Flash Sector operation set the FCNFG[ERSSUSP] bit when CCIF, ACCERR, and FPVIOL are clear and the CCOB command field holds the code for the Erase Flash Sector command. During the Erase Flash Sector operation (see Erase Flash Sector Command), the flash memory module samples the state of the ERSSUSP bit at convenient points. If the flash memory module detects that the ERSSUSP bit is set, the Erase Flash Sector operation is suspended and the flash memory module sets CCIF. While ERSSUSP is set, all writes to flash registers are ignored except for writes to the FSTAT and FCNFG registers.

If an Erase Flash Sector operation effectively completes before the flash memory module detects that a suspend request has been made, the flash memory module clears the ERSSUSP bit prior to setting CCIF. When an Erase Flash Sector operation has been successfully suspended, the flash memory module sets CCIF and leaves the ERSSUSP bit set. While CCIF is set, the ERSSUSP bit can only be cleared to prevent the withdrawal of a suspend request before the flash memory module has acknowledged it.

34.4.11.5.2 Resuming a Suspended Erase Flash Sector Operation

If the ERSSUSP bit is still set when CCIF is cleared to launch the next command, the previous Erase Flash Sector operation resumes. The flash memory module acknowledges the request to resume a suspended operation by clearing the ERSSUSP bit. A new suspend request can then be made by setting ERSSUSP. A single Erase Flash Sector operation can be suspended and resumed multiple times.

There is a minimum elapsed time limit of 4.3 msec between the request to resume the Erase Flash Sector operation (CCIF is cleared) and the request to suspend the operation again (ERSSUSP is set). This minimum time period is required to ensure that the Erase Flash Sector operation will eventually complete. If the minimum period is continually violated, i.e. the suspend requests come repeatedly and too quickly, no forward progress is made by the Erase Flash Sector algorithm. The resume/suspend sequence runs indefinitely without completing the erase.

34.4.11.5.3 Aborting a Suspended Erase Flash Sector Operation

The user may choose to abort a suspended Erase Flash Sector operation by clearing the ERSSUSP bit prior to clearing CCIF for the next command launch. When a suspended operation is aborted, the flash memory module starts the new command using the new FCCOB contents.

Note

Aborting the erase leaves the bitcells in an indeterminate, partially-erased state. Data in this sector is not reliable until a new erase command fully completes.

The following figure shows how to suspend and resume the Erase Flash Sector operation.

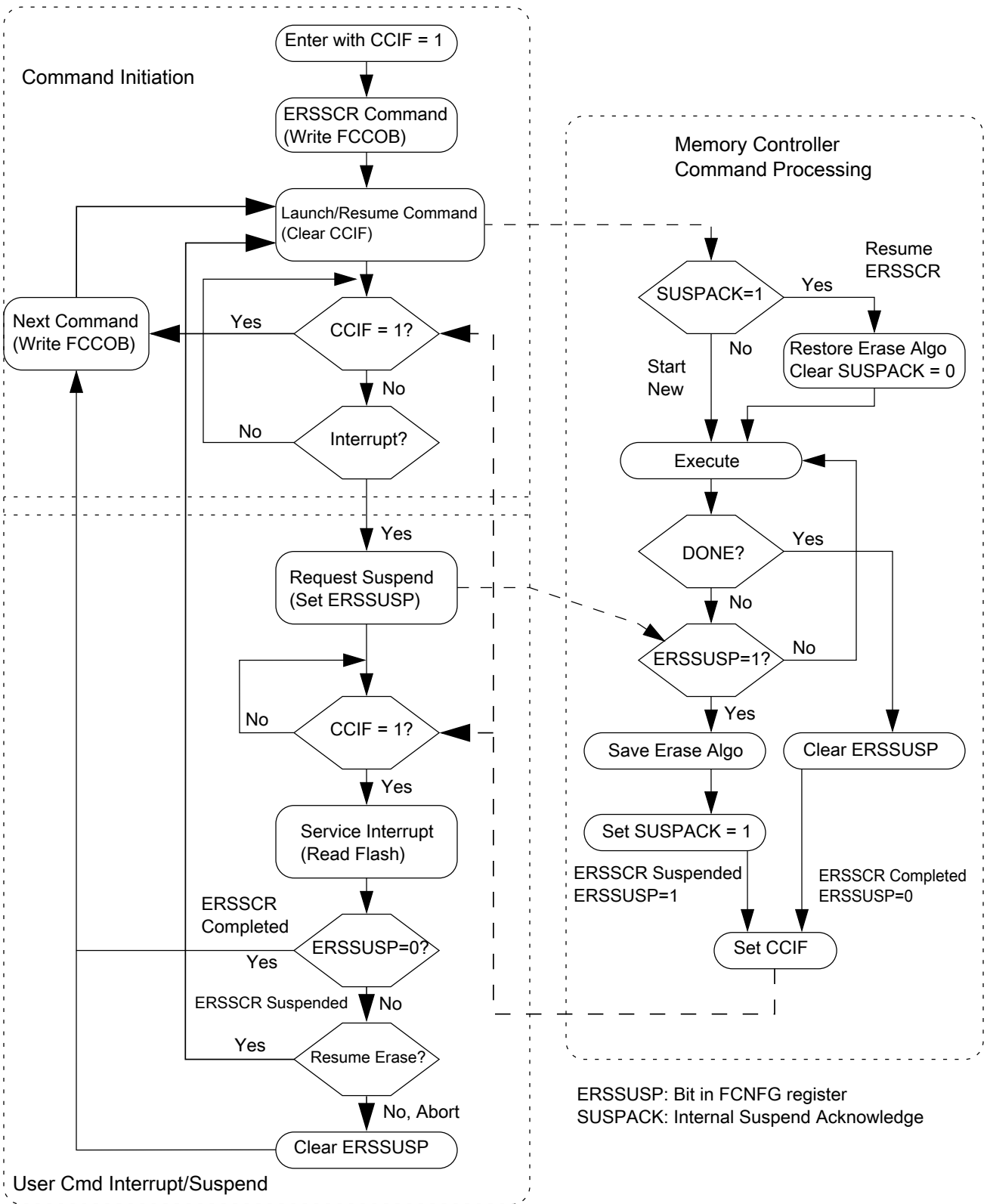


Figure 34-6. Suspend and Resume of Erase Flash Sector Operation

34.4.11.6 Read 1s All Blocks Command

The Read 1s All Blocks command checks if the program flash blocks and program flash erasable IFR have been erased to the specified read margin level, if applicable, and releases security if the readout passes, i.e. all data reads as '1'.

Table 34-16. Read 1s All Blocks Command FCCOB Requirements

FCCOB Number	FCCOB Contents [7:0]
0	0x40 (RD1ALL)
1	Read-1 Margin Choice

After clearing CCIF to launch the Read 1s All Blocks command, the flash memory module :

- sets the read margin for 1s according to Table 34-17,
- checks the contents of the program flash and program flash erasable IFR are in the erased state.

If the flash memory module confirms that these memory resources are erased, access control is disabled and security is released by setting the FSEC[SEC] field to the unsecure state. The security byte in the flash configuration field (see Flash Configuration Field Description) remains unaffected by the Read 1s All Blocks command. If the read fails, i.e. all memory resources are not in the fully erased state, the FSTAT[MGSTAT0] bit is set.

The CCIF flag sets after the Read 1s All Blocks operation has completed.

Table 34-17. Margin Level Choices for Read 1s All Blocks

Read Margin Choice	Margin Level Description
0x00	Use the 'normal' read level for 1s
0x01	Apply the 'User' margin to the normal read-1 level
0x02	Apply the 'Factory' margin to the normal read-1 level

Table 34-18. Read 1s All Blocks Command Error Handling

Error Condition	Error Bit
An invalid margin choice is specified	FSTAT[ACCERR]
Read-1s fails	FSTAT[MGSTAT0]

34.4.11.7 Read Once Command

The Read Once command provides read access to special 96-byte fields located in the program flash 0 IFR (see Program Flash IFR Map and Program Once Field). Access to the Program Once ID field is via 16 records (index values 0x00 - 0x0F), each 4 bytes long. Access to the Program Once XACC and SACC fields are via 4 records (index values 0x10 - 0x13), each of which is 8 bytes long. These fields are programmed using the Program Once command described in Program Once Command.

The Read Once command also provides read access to special 4-byte records (index values 0x30 - 0x33) located in the program flash erasable IFR (see Program Flash Erasable IFR Map and Erasable Program Once Field). These fields are programmed using the Program Once command.

Table 34-19. Read Once Command FCCOB Requirements

FCCOB Number	FCCOB Contents [7:0]
0	0x41 (RDONCE)
1	Program Once record index (0x00 - 0x13, 0x30 - 0x33)
2	Not used
3	Not used
Returned Values	
4	Program Once byte 0 value
5	Program Once byte 1 value
6	Program Once byte 2 value
7	Program Once byte 3 value
8	Program Once byte 4 value (index 0x10 - 0x13)
9	Program Once byte 5 value (index 0x10 - 0x13)
10	Program Once byte 6 value (index 0x10 - 0x13)
11	Program Once byte 7 value (index 0x10 - 0x13)

After clearing CCIF to launch the Read Once command, a 4-byte or 8-byte Program Once record is read and stored in the FCCOB register. The CCIF flag is set after the Read Once operation completes. Valid record index values for the Read Once command range from 0x00 - 0x13, 0x30 - 0x33. During execution of the Read Once command, any attempt to read addresses within the program flash block containing the selected record index returns invalid data. The Read Once command can be executed any number of times.

Table 34-20. Read Once Command Error Handling

Error Condition	Error Bit
Command not available in current mode/security	FSTAT[ACCERR]
An invalid record index is supplied	FSTAT[ACCERR]

34.4.11.8 Program Once Command

The Program Once command enables programming to special 96-byte fields in the program flash 0 IFR (see Program Flash IFR Map and Program Once Field). Access to the Program Once ID field is via 16 records (index values 0x00 - 0x0F), each 4 bytes long. Access to the Program Once XACC and SACC fields are via 4 records (index values 0x10 - 0x13), each of which is 8 bytes long. These records can be read using the Read Once command (see Read Once Command) or using the Read Resource command (see Read Resource Command). These records can be programmed only once since the program flash 0 IFR cannot be erased.

The Program Once command enables programming to special 4-byte records located in the program flash erasable IFR (see Program Flash Erasable IFR Map and Erasable Program Once Field). Record index values 0x20 - 0x23 cannot be read using the Read Once command. Record index values 0x30 - 0x33 can be read using the Read Once command. These records can be reprogrammed since the program flash erasable IFR can be erased using the Erase All Blocks command and Erase All Blocks Unsecure command.

Table 34-21. Program Once Command FCCOB Requirements

FCCOB Number	FCCOB Contents [7:0]
0	0x43 (PGMONCE)
1	Program Once record index (0x00 - 0x13, 0x20 - 0x23, 0x30 - 0x33)
2	Not Used
3	Not Used
4	Program Once byte 0 value
5	Program Once byte 1 value
6	Program Once byte 2 value
7	Program Once byte 3 value
8	Program Once byte 4 value (index 0x10 - 0x13)
9	Program Once byte 5 value (index 0x10 - 0x13)
10	Program Once byte 6 value (index 0x10 - 0x13)
11	Program Once byte 7 value (index 0x10 - 0x13)

After clearing CCIF to launch the Program Once command, the flash memory module first verifies that the selected record is erased. If erased, then the selected record is programmed using the values provided. The Program Once command also verifies that the programmed values read back correctly. The CCIF flag is set after the Program Once operation has completed.

Any attempt to program one of these records when the existing value is not Fs (erased) is not allowed. Valid record index values for the Program Once command range from 0x00 - 0x13, 0x20 - 0x23, 0x30 - 0x33. During execution of the Program Once command, any attempt to read addresses within the program flash block containing the selected record index returns invalid data.

Table 34-22. Program Once Command Error Handling

Error Condition	Error Bit
Command not available in current mode/security	FSTAT[ACCERR]
An invalid record index is supplied	FSTAT[ACCERR]
The requested record has already been programmed to a non-FFFF value[1]	FSTAT[ACCERR]
Any errors have been encountered during the verify operation	FSTAT[MGSTAT0]

1. If a Program Once record is initially programmed to 0xFFFF_FFFF (0xFFFF_FFFF_FFFF_FFFF for index 0x10 - 0x13), the Program Once command is allowed to execute again on that same record.

34.4.11.9 Erase All Blocks Command

The Erase All Blocks operation erases all flash memory, verifies all memory contents, and releases MCU security.

Table 34-23. Erase All Blocks Command FCCOB Requirements

FCCOB Number	FCCOB Contents [7:0]
0	0x44 (ERSALL)

After clearing CCIF to launch the Erase All Blocks command, the flash memory module erases all program flash memory and the program flash erasable IFR space, then verifies that all are erased.

If the flash memory module verifies that all flash memories were properly erased, access control is disabled and security is released by setting the FSEC[SEC] field to the unsecure state. The Erase All Blocks command aborts if any flash region is protected. The security byte and all other contents of the flash configuration field (see Flash Configuration Field Description) are erased by the Erase All Blocks command. If the erase-verify fails, the FSTAT[MGSTAT0] bit is set. The CCIF flag is set after the Erase All Blocks operation completes.

Access control determined by the contents of the FXACC registers will not block execution of the Erase All Blocks command. While most Flash memory will be erased, the program flash IFR space containing the Program Once XACC and SACC fields will not be erased and, therefore, the contents of the Program Once XACC and SACC fields will not change. The contents of the FXACC and FSACC registers will not be impacted

by the execution of the Erase All Blocks command. After completion of the Erase All Blocks command, access control is disabled until the next reset of the flash module or the Read 1s All Blocks command is executed and fails (FSTAT[MGSTAT0] is set).

Table 34-24. Erase All Blocks Command Error Handling

Error Condition	Error Bit
Command not available in current mode/security	FSTAT[ACCERR]
Any region of the program flash memory is protected	FSTAT[FPVIOL]
Any errors have been encountered during the verify operation[1]	FSTAT[MGSTAT0]

1. User margin read may be run using the Read 1s All Blocks command to verify all bits are erased.

34.4.11.9.1 Triggering an Erase All External to the Flash Memory Module

The functionality of the Erase All Blocks/Erase All Blocks Unsecure command is also available in an uncommanded fashion outside of the flash memory. Refer to the device's Chip Configuration details for information on this functionality.

Before invoking the external erase all function, the FSTAT[ACCERR and PVIOL] flags must be cleared and the FCCOB0 register must not contain 0x44. When invoked, the erase-all function erases all program flash memory and the program flash erasable IFR space regardless of the protection settings. If the post-erase verify passes, access control determined by the contents of the FXACC registers is disabled and the routine then releases security by setting the FSEC[SEC] field register to the unsecure state. The security byte in the Flash Configuration Field is also programmed to the unsecure state. The status of the erase-all request is reflected in the FCNFG[ERSAREQ] bit. The FCNFG[ERSAREQ] bit is cleared once the operation completes and the normal FSTAT error reporting is available, except FPVIOL, as described in Erase All Blocks Command/ Erase All Blocks Unsecure Command.

34.4.11.10 Verify Backdoor Access Key Command

The Verify Backdoor Access Key command only executes if the mode and security conditions are satisfied (see Flash Commands by Mode). Execution of the Verify Backdoor Access Key command is further qualified by the FSEC[KEYEN] bits. The Verify Backdoor Access Key command releases security if user-supplied keys in the FCCOB match those stored in the Backdoor Comparison Key bytes of the Flash Configuration Field (see Flash Configuration Field Description). The column labelled Flash Configuration Field offset address shows the location of the matching byte in the Flash Configuration Field.

Table 34-25. Verify Backdoor Access Key Command FCCOB Requirements

FCCOB Number	FCCOB Contents [7:0]	Flash Configuration Field Offset Address
0	0x45 (VFYKEY)	
1-3	Not Used	
4	Key Byte 0	0x0_0003
5	Key Byte 1	0x0_0002
6	Key Byte 2	0x0_0001
7	Key Byte 3	0x0_0000
8	Key Byte 4	0x0_0007
9	Key Byte 5	0x0_0006
A	Key Byte 6	0x0_0005
B	Key Byte 7	0x0_0004

After clearing CCIF to launch the Verify Backdoor Access Key command, the flash memory module checks the FSEC[KEYEN] bits to verify that this command is enabled. If not enabled, the flash memory module sets the FSTAT[ACCERR] bit and terminates. If the command is enabled, the flash memory module compares the key provided in FCCOB to the backdoor comparison key in the Flash Configuration Field. If the backdoor keys match, the FSEC[SEC] field is changed to the unsecure state and security is released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are immediately aborted and the FSTAT[ACCERR] bit is (again) set to 1 until a reset of the flash memory module module occurs. If the entire 8-byte key is all zeros or all ones, the Verify Backdoor Access Key command fails with an access error. The CCIF flag is set after the Verify Backdoor Access Key operation completes.

Table 34-26. Verify Backdoor Access Key Command Error Handling

Error Condition	Error Bit
The supplied key is all-0s or all-Fs	FSTAT[ACCERR]
An incorrect backdoor key is supplied	FSTAT[ACCERR]
Backdoor key access has not been enabled (see the description of the FSEC register)	FSTAT[ACCERR]
This command is launched and the backdoor key has mismatched since the last power down reset	FSTAT[ACCERR]

34.4.11.11 Erase All Blocks Unsecure Command

The Erase All Blocks Unsecure operation erases all flash memory, verifies all memory contents, programs the security byte in the Flash Configuration Field to the unsecure state, and releases MCU security.

Table 34-27. Erase All Blocks Unsecure Command FCCOB Requirements

FCCOB Number	FCCOB Contents [7:0]
0	0x49 (ERSALLU)

After clearing CCIF to launch the Erase All Blocks Unsecure command, the flash memory module erases all program flash memory and the program flash erasable IFR space, then verifies that all are erased.

If the flash memory module verifies that all program flash memory and the program flash erasable IFR space was properly erased, access control is disabled, security is released by setting the FSEC[SEC] field to the unsecure state, and the security byte (see Flash Configuration Field Description) is programmed to the unsecure state by the Erase All Blocks Unsecure command. If the erase or program verify fails, the FSTAT[MGSTAT0] bit is set. The CCIF flag is set after the Erase All Blocks Unsecure operation completes.

Access control determined by the contents of the FXACC registers will not block execution of the Erase All Blocks Unsecure command. While most Flash memory will be erased, the program flash IFR space containing the Program Once XACC and SACC fields will not be erased and, therefore, the contents of the Program Once XACC and SACC fields will not change. The contents of the FXACC and FSACC registers will not be impacted by the execution of the Erase All Blocks Unsecure command. After completion of the Erase All Blocks Unsecure command, access control is disabled until the next reset of the flash module or the Read 1s All Blocks command is executed and fails (FSTAT[MGSTAT0] is set).

Table 34-28. Erase All Blocks Unsecure Command Error Handling

Error Condition	Error Bit
Command not available in current mode/security	FSTAT[ACCERR]
Any errors have been encountered during erase or program verify operations	FSTAT[MGSTAT0]

34.4.12 Security

The flash memory module provides security information to the MCU based on contents of the FSEC security register.

The MCU then limits access to flash memory resources as defined in the device's Chip Configuration details. During reset, the flash memory module initializes the FSEC register using data read from the security byte of the Flash Configuration Field (see Flash Configuration Field Description).

The following fields are available in the FSEC register. The settings are described in the Flash Security Register (FTFA_FSEC) details.

Flash security features are discussed further in AN4507: Using the Kinetis Security and Flash Protection Features . Note that not all features described in the application note are available on this device.

Table 34-29. FSEC register fields

FSEC field	Description
KEYEN	Backdoor Key Access
MEEN	Mass Erase Capability
FSLACC	Freescale Factory Access
SEC	MCU security

34.4.12.1 Flash Memory Access by Mode and Security

The following table summarizes how access to the flash memory module is affected by security and operating mode.

Table 34-30. Flash Memory Access Summary

Operating Mode	Chip Security State	
	Unsecure	Secure
NVM Normal	Full command set	
NVM Special	Full command set	Only the Erase All Blocks, Erase All Blocks Unsecure and Read 1s All Blocks commands.

34.4.12.2 Changing the Security State

The security state out of reset can be permanently changed by programming the security byte of the flash configuration field. This assumes that you are starting from a mode where the necessary program flash erase and program commands are available and that the region of the program flash containing the flash configuration field is unprotected. If the flash security byte is successfully programmed, its new value takes affect after the next chip reset.

34.4.12.2.1 Unsecuring the Chip Using Backdoor Key Access

The chip can be unsecured by using the backdoor key access feature, which requires knowledge of the contents of the 8-byte backdoor key value stored in the Flash Configuration Field (see Flash Configuration Field Description). If the FSEC[KEYEN] bits are in the enabled state, the Verify Backdoor Access Key command (see Verify Backdoor Access Key Command) can be run; it allows the user to present prospective keys for comparison to the stored keys. If the keys match, the FSEC[SEC] bits are changed to unsecure the chip. The entire 8-byte key cannot be all 0s or all 1s; that is, 0000_0000_0000_0000h and FFFF_FFFF_FFFF_FFFFh are not accepted by the Verify Backdoor Access Key command as valid comparison values. While the Verify Backdoor Access Key command is active, program flash memory is not available for read access and returns invalid data.

The user code stored in the program flash memory must have a method of receiving the backdoor keys from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports.

If the KEYEN bits are in the enabled state, the chip can be unsecured by the following backdoor key access sequence:

1. Follow the command sequence for the Verify Backdoor Access Key command as explained in Verify Backdoor Access Key Command
2. If the Verify Backdoor Access Key command is successful, the chip is unsecured and the FSEC[SEC] bits are forced to the unsecure state

An illegal key provided to the Verify Backdoor Access Key command prohibits further use of the Verify Backdoor Access Key command. A reset of the chip is the only method to re-enable the Verify Backdoor Access Key command when a comparison fails.

After the backdoor keys have been correctly matched, the chip is unsecured by changing the FSEC[SEC] bits. A successful execution of the Verify Backdoor Access Key command changes the security in the FSEC register only. It does not alter the security byte or the keys stored in the Flash Configuration Field (Flash Configuration Field Description). After the next reset of the chip, the security state of the flash memory module reverts back to the flash security byte in the Flash Configuration Field. The Verify Backdoor Access Key command sequence has no effect on the program and erase protections defined in the program flash protection registers.

If the backdoor keys successfully match, the unsecured chip has full control of the contents of the Flash Configuration Field. The chip may erase the sector containing the Flash Configuration Field and reprogram the flash security byte to the unsecure state and change the backdoor keys to any desired value.

34.4.13 Reset Sequence

On each system reset the flash memory module executes a sequence which establishes initial values for the flash block configuration parameters, FPROT, FOPT, FSEC, FXACC, FSACC, and FACNFG registers.

FSTAT[CCIF] is cleared throughout the reset sequence. The flash memory module holds off CPU access during the reset sequence. Flash reads are possible when the hold is removed. Completion of the reset sequence is marked by setting CCIF which enables flash user commands.

If a reset occurs while any flash command is in progress, that command is immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed. Commands and operations do not automatically resume after exiting reset.

Chapter 35
Synchronous DRAM Controller Module (SDRAM)

35.1 Chip-specific SDRAM information

35.1.1 SDRAM clocking

The system provides a dedicated clock source (FlexBus clock to the SDRAM Controller module's CLKOUT input that is also used for FlexBus clocking. This clock source is divider controlled via SIM_CLKDIV1[OUTDIV3]. See Clock Distribution for more details.

35.1.2 SDRAM SDR signal multiplexing

The byte enable control signals of the SDRAM controller (SDRAM_DQMx) are multiplexed with the byte enable control signals of the FlexBus ($\overline{\text{FB_BE_xx_yy}}$). The port control module registers control whether the FlexBus or another module signals are available on the external pin, while the FlexBus's CSPMCR register configures which FlexBus signals are available from the FlexBus module.

NOTE

In order to use the SDRAM simultaneously with the FlexBus, the FlexBus CSPMCR register must be configured to select the FlexBus byte enable signals (value of 0xX222_2000). Once this is configured and SDRAM module enabled, the device will automatically select the correct signal based on the transaction which is activated (FlexBus or SDRAM).

The control signals are illustrated in the FlexBus signal multiplexing section.

Therefore, use the CSPMCR and port control registers to configure which control signal is available on the external pin.

35.1.3 SDRAMC Security

When security is enabled on the device, SDRAM accesses may be restricted by configuring the SIM_SOPT2[FBSL] register. This is a shared control register between SDRAM and FlexBus. See System Integration Module (SIM) for details.

35.2 Introduction

This chapter describes configuration and operation of the synchronous DRAM (SDRAM) controller. It begins with a general description and brief glossary, and includes a description of signals involved in DRAM operations. The remainder of the chapter describes the programming model and signal timing, as well as the command set required for synchronous operations. It also includes extensive examples that the designer can follow to better understand how to configure the DRAM controller for synchronous operations.

35.3 Overview

The synchronous DRAM controller module provides glueless integration of SDRAM. The key features of the DRAM controller include the following:

- Support for two independent blocks of SDRAM
- Interface to standard SDRAM components
- Programmable $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, and refresh timing
- Support for 8-, 16-, and 32-bit wide SDRAM blocks

35.3.1 Definitions

The following terminology is used in this chapter:

- SDRAM block: Any group of DRAM memories selected by one of the SDRAM_CS[1:0] signals. Thus, the controller can support two independent memory blocks. The base address of each block is programmed in the DRAM address and control registers (SDRAM_AC0 and SDRAM_AC1)

- SDRAM: RAMs that operate like asynchronous DRAMs but with a synchronous clock, a pipelined, multiple-bank architecture, and a faster speed
- SDRAM bank: An internal partition in an SDRAM device. For example, a 64-Mbit SDRAM component might be configured as four 512K x 32 banks. Banks are selected through the SDRAM component's bank select lines

35.3.2 Block Diagram and Major Components

The basic components of the SDRAM controller are shown in the figure below:

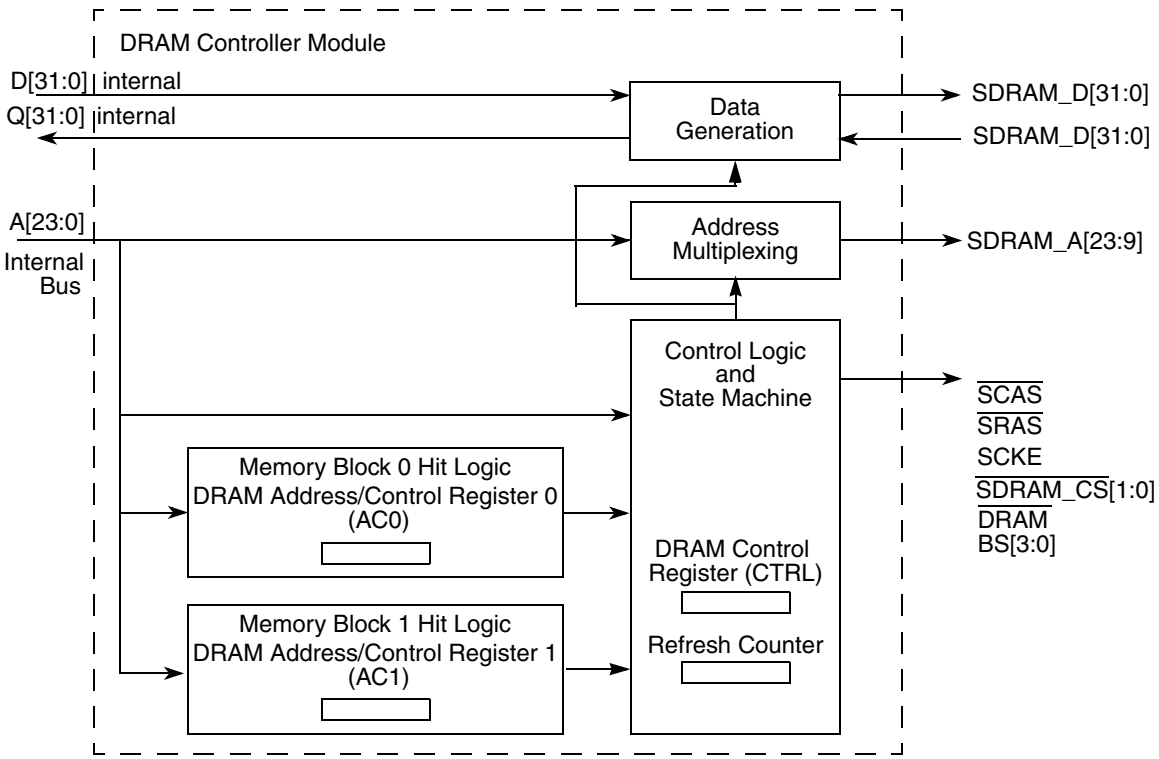


Figure 35-1. Block diagram

The DRAM controller's major components are as follows:

- DRAM address and control registers (SDRAM_AC0 and SDRAM_AC1)—The DRAM controller consists of two configuration register units, one for each supported memory block. SDRAM_AC0 is accessed at SDRAMC IPS Base Address + 0x048; SDRAM_AC1 is accessed at SDRAMC IPS Base Address + 0x050. The register information is passed on to the hit logic.
- Control logic and state machine—Generates all SDRAM signals, taking hit information and bus-cycle characteristic data from the block logic in order to generate SDRAM accesses. Handles refresh requests from the refresh counter

- DRAM control register (SDRAM_CTRL)—Contains data to control refresh operation of the DRAM controller. Both memory blocks are refreshed concurrently as controlled by SDRAM_CTRL[RC].
- Refresh counter—Determines when refresh should occur; controlled by the value of SDRAM_CTRL[RC]. It generates a refresh request to the control block.

- Hit logic—Compares address and attribute signals of a current SDRAM bus cycle to both SDRAM_ACn to determine if an SDRAM block is being accessed. Hits are passed to the control logic along with characteristics of the bus cycle to be generated
- Address multiplexing—Multiplexes addresses to allow column and row addresses to share pins. This allows glueless interface to SDRAMs
- Data Generation—Controls the data input and data output transmission between the on-platform and off-platform data buses.

35.4 SDRAM Controller Operation

By running synchronously with the system clock, SDRAM can (after an initial latency period) be accessed on every CLKOUT clock; 5-1-1-1 is a typical burst rate to the SDRAM. This controller does not have an independent SDRAM clock signal. The timing of the SDRAM controller is controlled by the CLKOUT signal. Note that because the controller cannot have more than one page open at a time, it does not support interleaving. SDRAM controllers send special commands for such functions as precharge, read, write, burst, auto-refresh, and various combinations of these functions. The following table lists common SDRAM commands.

Table 35-1. SDRAM Commands

Commands	Definitions
ACTV	Activate. Executed before read or write executes; SDRAM registers and decodes row address
MRS	Mode register set.
NOP	No-op. Does not affect SDRAM state machine; DRAM controller control signals negated; SDRAM_CS[1:0] asserted.
PALL	Precharge all. Precharges all internal banks of an SDRAM component; executed before new page is opened.
READ	Read access. SDRAM registers column address and decodes that a read access is occurring.
REF	Refresh. Refreshes internal bank rows of an SDRAM component.
SELF	Self refresh. Refreshes internal bank rows of an SDRAM component when it is in low-power mode.
SELFX	Exit self refresh. This command is sent to the DRAM controller when SDRAM_CTRL[IS] is cleared.
WRITE	Write access. SDRAM registers column address and decodes that a write access is occurring.

Commands are issued to memory using specific encodings on address and control pins. Soon after system reset, a command must be sent to the SDRAM mode register to configure SDRAM operating parameter

35.4.1 DRAM Controller Signals

The following table describes the behavior of DRAM signals in synchronous mode

Table 35-2. Synchronous DRAM Signal Connections

Signal	I/O	Description
$\overline{\text{SRAS}}$	O	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SRAS}}$.
$\overline{\text{SCAS}}$	O	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SCAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SCAS}}$.
$\overline{\text{DRAMW}}$	O	DRAM read/write. Asserted for write operations and negated for read operations.
$\overline{\text{SDRAM_CS}}$[1:0]	O	Row address strobe. Select each memory block of SDRAMs connected to the controller. One $\overline{\text{SDRAM_CS}}$ signal selects one SDRAM block and connects to the corresponding CS signals.
SCKE	O	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode in which operations are suspended or capable of entering self-refresh mode.
BS[3:0]	O	SDRAM byte selects BS[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or data qualifier masks) of the SDRAMs.
SDRAM_A [23:9]	O	SDRAM address bus output
SDRAM_D [31:0]	I/O	SDRAM data bus

35.4.2 Memory Map for SDRAMC Registers

The DRAM controller registers memory map is shown in the following table

SDRAM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_F042	Control Register (SDRAM_CTRL)	16	R/W	Undefined	35.4.2.1/ 860
4000_F048	Address and Control Register (SDRAM_AC0)	32	R/W	Undefined	35.4.2.2/ 862
4000_F04C	Control Mask (SDRAM_CM0)	32	R/W	Undefined	35.4.2.3/ 865
4000_F050	Address and Control Register (SDRAM_AC1)	32	R/W	Undefined	35.4.2.2/ 862
4000_F054	Control Mask (SDRAM_CM1)	32	R/W	Undefined	35.4.2.3/ 865

35.4.2.1 Control Register (SDRAM_CTRL)

SDRAM_CTRL register controls refresh logic

Address: 4000_F000h base + 42h offset = 4000_F042h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved		Reserved	Reserved	IS	RTIM		RC
Reset	x*	x*	x*	x*	x*	x*	x*	x*

Bit	7	6	5	4	3	2	1	0
Read Write	RC							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SDRAM_CTRL field descriptions

Field	Description
15–14 Reserved	Reserved This field is reserved. Should be cleared
13 Reserved	Reserved This field is reserved. Should be cleared

Table continues on the next page...

SDRAM_CTRL field descriptions (continued)

Field	Description
12 Reserved	Reserved This field is reserved. Should be cleared
11 IS	Initiate self-refresh command. 0 Take no action or issue a selfx command to exit self refresh. 1 SDRAM controller sends a self command to both SDRAM blocks to put them in low-power, self-refresh state where they remain until IS is cleared. When IS is cleared, the controller sends a selfx command for the SDRAMs to exit self-refresh. The refresh counter is suspended while the SDRAMs are in self-refresh; the SDRAM controls the refresh period.
10–9 RTIM	Refresh timing Determines the timing operation of auto-refresh in the SDRAM controller. Specifically, it determines the number of bus clocks inserted between a ref command and the next possible actv command. This same timing is used for both memory blocks controlled by the SDRAM controller. This corresponds to t_{RC} in the SDRAM specifications 00 3 clocks 01 6 clocks 10 9 clocks 11 9 clocks
RC	Refresh count Controls refresh frequency. The number of bus clocks between refresh cycles is (RC + 1) x 16. Refresh can range from 16–8192 bus clocks to accommodate both standard and low-power SDRAMs with bus clock operation from less than 2 MHz to greater than 50 MHz. The following example calculates RC for an auto-refresh period for 4096 rows to receive 64 ms of refresh every 15.625 µs for each row (1031 bus clocks at 66 MHz). # of bus clocks = 1031 = (RC field + 1) x 16; RC = (1031 bus clocks/16) -1 = 63.44, which rounds to 63; therefore, RC = 0x3F.

35.4.2.2 Address and Control Register (SDRAM_AC*n*)

The SDRAM_ACn registers, contain the base address compare value and the control bits for memory blocks 0 and 1 of the SDRAM controller. Address and timing are also controlled by bits in SDRAM_ACn.

Address: 4000_F000h base + 48h offset + (8d × i), where i=0d to 1d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	BA														Reserved	
W																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RE	Reserved	CASL		Reserved	CBM			Reserved	IMRS	PS		IP	Reserved		
W																
Reset	0	x*	x*	x*	x*	x*	x*	x*	x*	0	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SDRAM_AC*n* field descriptions

Field	Description
31–18 BA	Base address register. With SDRAM_CM[BAM], determines the address range in which the associated DRAM block is located. Each BA bit is compared with the corresponding address of the current bus cycle. If all unmasked bits match, the address hits in the associated DRAM block. BA functions the same as in asynchronous operation.
17–16 Reserved	Should be cleared This field is reserved.
15 RE	Refresh enable Determines when the DRAM controller generates a refresh cycle to the DRAM block.

Table continues on the next page...

SDRAM_AC*n* field descriptions (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td></td><td>0 Do not refresh associated DRAM block
1 Refresh associated DRAM block</td></tr>
<tr><td>14
Reserved</td><td>Should be cleared

This field is reserved.</td></tr>
<tr><td>13–12
CASL</td><td>$\overline{\text{CAS}}$ Latency

Affects the following SDRAM timing specifications. Timing nomenclature varies with manufacturers. Refer to the SDRAM specification for the appropriate timing nomenclature:

<table>
<tr><th rowspan="2">Parameter</th><th colspan="4">Number of Bus Clocks</th></tr>
<tr><th>CASL=00</th><th>CASL=01</th><th>CASL=10</th><th>CASL=11</th></tr>
<tr><td>trcd—$\overline{\text{SRAS}}$ assertion to $\overline{\text{SCAS}}$ assertion</td><td>1</td><td>2</td><td>3</td><td>3</td></tr>
<tr><td>tcasl—$\overline{\text{SCAS}}$ assertion to data out</td><td>1</td><td>2</td><td>3</td><td>3</td></tr>
<tr><td>tras—actv command to precharge command</td><td>2</td><td>4</td><td>6</td><td>6</td></tr>
<tr><td>trp—Precharge command to actv command</td><td>1</td><td>2</td><td>3</td><td>3</td></tr>
<tr><td>trwl,trdl—Last data input to precharge command</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>tep—Last data out to precharge command</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>11
Reserved</td><td>Reserved

This field is reserved.
Should be cleared</td></tr>
<tr><td>10–8
CBM</td><td>Command bit location

Because different SDRAM configurations cause the command lines on the memory to correspond to a different address, the location of command bit is programmable. CB determines the address onto which the command bit are multiplexed.

NOTE: It is important to set CB according to the location of the command bit.

<table>
<tr><th>Command</th><th>Command Bit</th><th>Notes</th></tr>
<tr><td>000</td><td>17</td><td>Not possible for 8-bit port</td></tr>
<tr><td>001</td><td>18</td><td></td></tr>
<tr><td>010</td><td>19</td><td></td></tr>
<tr><td>011</td><td>20</td><td></td></tr>
<tr><td>100</td><td>21</td><td></td></tr>
<tr><td>101</td><td>22</td><td></td></tr>
<tr><td>110</td><td>23</td><td></td></tr>
<tr><td>111</td><td>24</td><td>Not supported</td></tr>
</table>

This encoding and the address multiplexing scheme handle common SDRAM organizations.</td></tr>
<tr><td>7
Reserved</td><td>Reserved

This field is reserved.</td></tr>
</table>

Table continues on the next page...

SDRAM_AC*n* field descriptions (continued)

Field	Description
	Should be cleared
6 IMRS	Initiate mode register set (mrs) command. Setting IMRS generates a mrs command to the associated SDRAMs. In initialization, IMRS should be set only after all DRAM controller registers are initialized and pall and refresh commands have been issued. After IMRS is set, the next access to an SDRAM block programs the SDRAM's mode register. Thus, the address of the access should be programmed to place the correct mode information on the SDRAM address pins. Because the SDRAM does not register this information, it doesn't matter if the IMRS access is a read or a write or what, if any, data is put onto the data bus. The DRAM controller clears IMRS after the mrs command finishes. 0 Take no action 1 Initiate mrs command
5–4 PS	Port size. Indicates the port size of the associated block of SDRAM, which allows for dynamic sizing of associated SDRAM accesses. PS functions the same in asynchronous operation. 00 32-bit port 01 8-bit port 10 16-bit port 11 16-bit port
3 IP	Initiate precharge all (pall) command. The DRAM controller clears IP after the pall command is finished. Accesses via IP should be no wider than the port size programmed in PS. 0 Take no action. 1 A pall command is sent to the associated SDRAM block. During initialization, this command is executed after all DRAM controller registers are programmed. After IP is set, the next write to an appropriate SDRAM address generates the pall command to the SDRAM block.
Reserved	Reserved. This field is reserved. Should be cleared

35.4.2.3 Control Mask (SDRAM_CM*n*)

The SDRAM_CMn, includes mask bits for the base address and for address attributes

Address: 4000_F000h base + 4Ch offset + (8d × i), where i=0d to 1d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	BAM														Reserved	
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved							WP	Reserved							V
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	0

* Notes:
- x = Undefined at reset.

SDRAM_CM*n* field descriptions

Field	Description
31–18 BAM	Base address mask. Masks the associated SDRAM_ACn[BA]. Lets the DRAM controller connect to various DRAM sizes. Mask bits need not be contiguous 0 The associated address bit is used in decoding the DRAM hit to a memory block 1 The associated address bit is not used in the DRAM hit decode
17–9 Reserved	Reserved This field is reserved. Should be cleared
8 WP	Write protect. Determines whether the associated block of DRAM is write protected. 0 Allow write accesses 1 Ignore write accesses. The DRAM controller ignores write accesses to the memory block and an address exception occurs. Write accesses to a write-protected DRAM region are compared in the chip select module for a hit. If no hit occurs, an external bus cycle is generated. If this external bus cycle is not acknowledged, an access exception occurs.
7–1 Reserved	Reserved This field is reserved. Should be cleared
0 V	Valid. Cleared at reset to ensure that the DRAM block is not erroneously decoded 0 Do not decode DRAM accesses. 1 Registers controlling the DRAM block are initialized; DRAM accesses can be decoded

35.5 General Synchronous Operation Guidelines

To reduce system logic and to support a variety of SDRAM sizes, the DRAM controller provides SDRAM control signals as well as a multiplexed row address and column address to the SDRAM.

35.5.1 Address Multiplexing

The following table shows the generic address multiplexing scheme for SDRAM configurations. All possible address connection configurations can be derived from this table.

NOTE

The maximum SDRAM address size is 128 Mbits.

Table 35-3. Generic Address Multiplexing Scheme

Address Pins	Row Address	Column Address	Notes Relating to Port Sizes
17	17	0	8-bit port only
16	16	1	8- and 16-bit ports only
15	15	2	
14	14	3	
13	13	4	
12	12	5	
11	11	6	
10	10	7	
9	9	8	
17	17	16	32-bit port only
18	18	17	16-bit port only or 32-bit port with only 8 column address lines
19	19	18	16-bit port only when at least 9 column address lines are used
20	20	19	
21	21	20	
22	22	21	
23	23	22	

The following tables provide a more comprehensive, step-by-step way to determine the correct address line connections for interfacing the SDRAM. To use the tables, find the one that corresponds to the number of column address lines on the SDRAM and to the port size as seen by the controller, which is not necessarily the SDRAM port size. For example, if two 1M x 16-bit SDRAMs together form a 1M x 32-bit memory, the port size

is 32 bits. The tables below assume that the SDRAM's A10 signal is used for command. If using a memory where command is on a different address signal modifications to the connections shown might be needed. Most SDRAMs likely have fewer address lines than are shown in the tables, so follow only the connections shown until all SDRAM address lines are connected.

Table 35-4. SDRAM Controller to SDRAM Interface (8-Bit Port, 9-Column Address Lines)

SDRAM Controller Pins	A17	A16	A15	A14	A13	A12	A11	A10	A9	A18	A19	A20	A21	A22	A23
Row	17	16	15	14	13	12	11	10	9	18	19	20	21	22	23
Column	0	1	2	3	4	5	6	7	8		CMD				
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14

Table 35-5. SDRAM Controller to SDRAM Interface (8-Bit Port, 10-Column Address Lines)

SDRAM Controller Pins	A17	A16	A15	A14	A13	A12	A11	A10	A9	A19	A20	A21	A22	A23
Row	17	16	15	14	13	12	11	10	9	19	20	21	22	23
Column	0	1	2	3	4	5	6	7	8	18	CMD			
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13

Table 35-6. SDRAM Controller to SDRAM Interface (8-Bit Port, 11-Column Address Lines)

SDRAM Controller Pins	A17	A16	A15	A14	A13	A12	A11	A10	A9	A19	A21	A22	A23
Row	17	16	15	14	13	12	11	10	9	19	21	22	23
Column	0	1	2	3	4	5	6	7	8	18	20	CMD	
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12

Table 35-7. SDRAM Controller to SDRAM Interface (16-Bit Port, 8-Column Address Lines)

SDRAM Controller Pins	A16	A15	A14	A13	A12	A11	A10	A9	A17	A18	A19	A20	A21	A22	A23
Row	16	15	14	13	12	11	10	9	17	18	19	20	21	22	23
Column	1	2	3	4	5	6	7	8			CMD				
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14

Table 35-8. SDRAM Controller to SDRAM Interface (16-Bit Port, 9-Column Address Lines)

SDRAM Controller Pins	A16	A15	A14	A13	A12	A11	A10	A9	A18	A19	A20	A21	A22	A23
Row	16	15	14	13	12	11	10	9	18	19	20	21	22	23

Table continues on the next page...

Table 35-8. SDRAM Controller to SDRAM Interface (16-Bit Port, 9-Column Address Lines) (continued)

Column	1	2	3	4	5	6	7	8	17		CMD			
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13

Table 35-9. SDRAM Controller to SDRAM Interface (16-Bit Port, 10-Column Address Lines)

SDRAM Controller Pins	A16	A15	A14	A13	A12	A11	A10	A9	A18	A20	A21	A22	A23
Row	16	15	14	13	12	11	10	9	18	20	21	22	23
Column	1	2	3	4	5	6	7	8	17	19	CMD		
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12

Table 35-10. SDRAM Controller to SDRAM Interface (16-Bit Port, 11-Column Address Lines)

SDRAM Controller Pins	A16	A15	A14	A13	A12	A11	A10	A9	A18	A20	A22	A23
Row	16	15	14	13	12	11	10	9	18	20	22	23
Column	1	2	3	4	5	6	7	8	17	19	21	CMD
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11

Table 35-11. SDRAM Controller to SDRAM Interface (32-Bit Port, 8-Column Address Lines)

SDRAM Controller Pins	A15	A14	A13	A12	A11	A10	A9	A17	A18	A19	A20	A21	A22	A23
Row	15	14	13	12	11	10	9	17	18	19	20	21	22	23
Column	2	3	4	5	6	7	8	16			CMD			
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13

Table 35-12. SDRAM Controller to SDRAM Interface (32-Bit Port, 9-Column Address Lines)

SDRAM Controller Pins	A15	A14	A13	A12	A11	A10	A9	A17	A19	A20	A21	A22	A23
Row	15	14	13	12	11	10	9	17	19	20	21	22	23
Column	2	3	4	5	6	7	8	16	18		CMD		
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12

Table 35-13. SDRAM Controller to SDRAM Interface (32-Bit Port, 10-Column Address Lines)

SDRAM Controller Pins	A15	A14	A13	A12	A11	A10	A9	A17	A19	A21	A22	A23
Row	15	14	13	12	11	10	9	17	19	21	22	23

Table continues on the next page...

Table 35-13. SDRAM Controller to SDRAM Interface (32-Bit Port, 10-Column Address Lines) (continued)

Column	2	3	4	5	6	7	8	16	18	20	CMD	
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11

35.5.2 SDRAM Byte Strobe Connections

Following figure shows SDRAM connections for port sizes of 32, 16, or 8 bits.

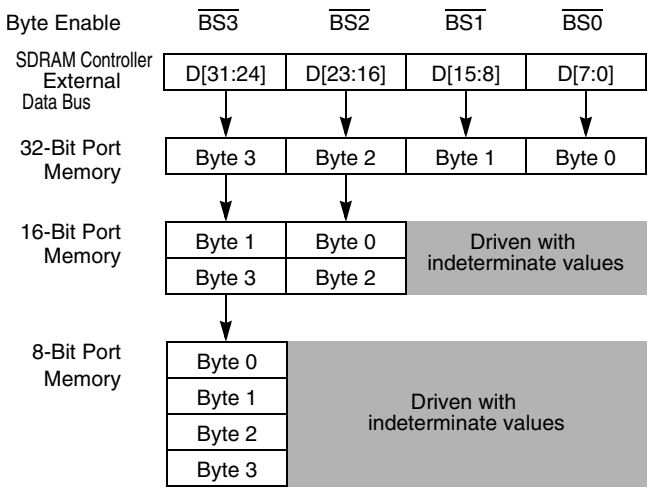


Figure 35-2. Connections for External Memory Port Sizes

35.5.3 Interfacing Example

The tables in the previous section can be used to configure the interface in the following example. To interface one 512KB x 32-bit x 4 bank SDRAM component (8 columns), use the connections shown in below table

Table 35-14. SDRAM Hardware Connections

SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10=CMD	BA0	BA1
SDRAM Controller Pins	A15	A14	A13	A12	A11	A10	A9	A17	A18	A19	A20	A21	A22

35.5.4 Burst Page Mode

SDRAM can efficiently provide data when an SDRAM page is opened. As soon as $\overline{SCAS}$ is issued, the SDRAM accepts a new address and asserts $\overline{SCAS}$ every CLKOUT for as long as accesses occur in that page. In burst page mode, there are multiple read or write operations for every ACTV command in the SDRAM if the requested transfer size exceeds the port size of the associated SDRAM. The primary cycle of the transfer generates the ACTV and READ or WRITE commands; secondary cycles generate only READ or WRITE commands. As soon as the transfer completes, the PALL command is generated to prepare for the next access.

Note that in synchronous operation, burst mode and address incrementing during burst cycles are controlled by the DRAM controller. Thus, instead of the SDRAM enabling its internal burst incrementing capability, the SDRAM Controller controls this function. This means that the burst function that is enabled in the mode register of SDRAMs must be disabled when interfacing to the SDRAM Controller.

Figure 35-3 figure shows a burst read operation. In this example, SDRAM_AC[CASL] = 01 for an $\overline{SRAS}$-to-$\overline{SCAS}$ delay (t_{RCD}) of 2 system clock cycles. Because t_{RCD} is equal to the read CAS latency ($\overline{SCAS}$ assertion to data out), this value is also 2 system clock cycles. Notice that NOPs are executed until the last data is read. A PALL command is executed one cycle after the last data transfer.

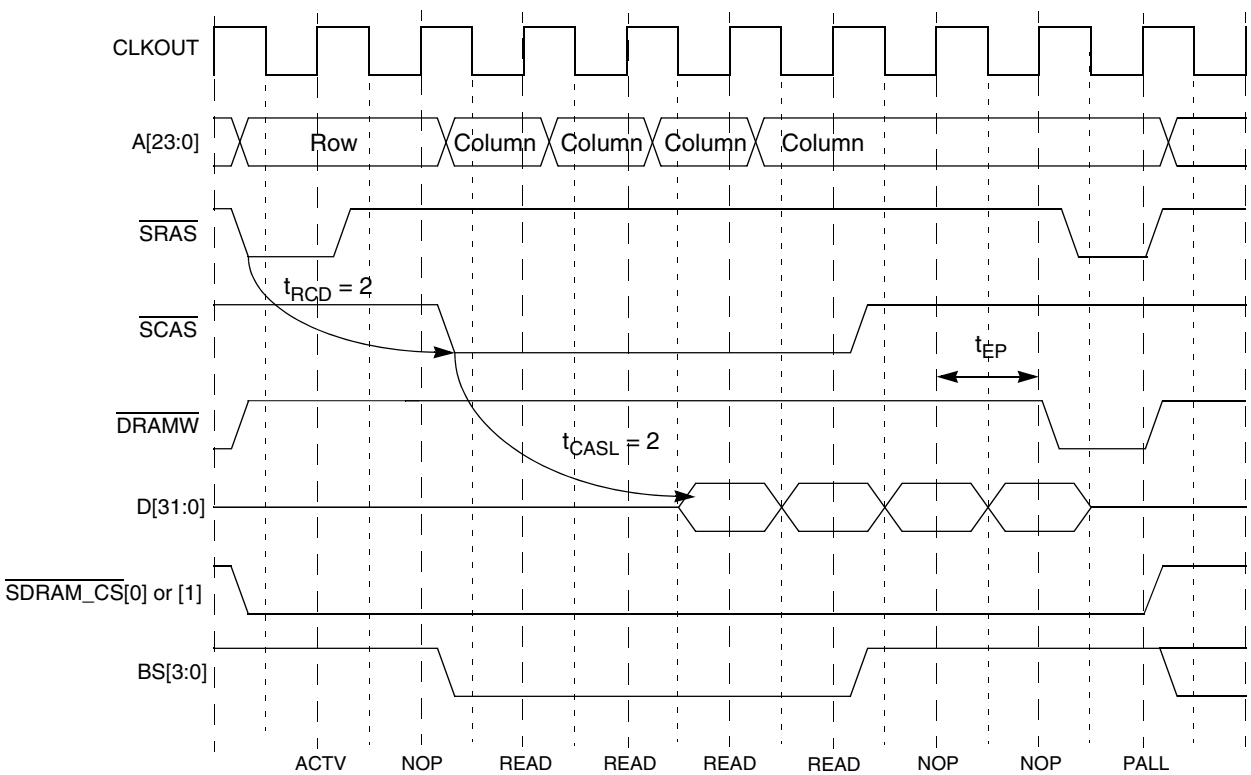


Figure 35-3. Burst Read SDRAM Access

Figure 35-4 figure shows the burst write operation. In this example, SDRAM_AC[CASL] = 01, which creates an $\overline{\text{SRAS}}$-to-$\overline{\text{SCAS}}$ delay (t_{RCD}) of 2 system clock cycles. Note that data is available upon $\overline{\text{SCAS}}$ assertion and a burst write cycle completes two cycles sooner than a burst read cycle with the same t_{RCD}. The next bus cycle is initiated sooner, but cannot begin an SDRAM cycle until the precharge-to-ACTV delay completes.

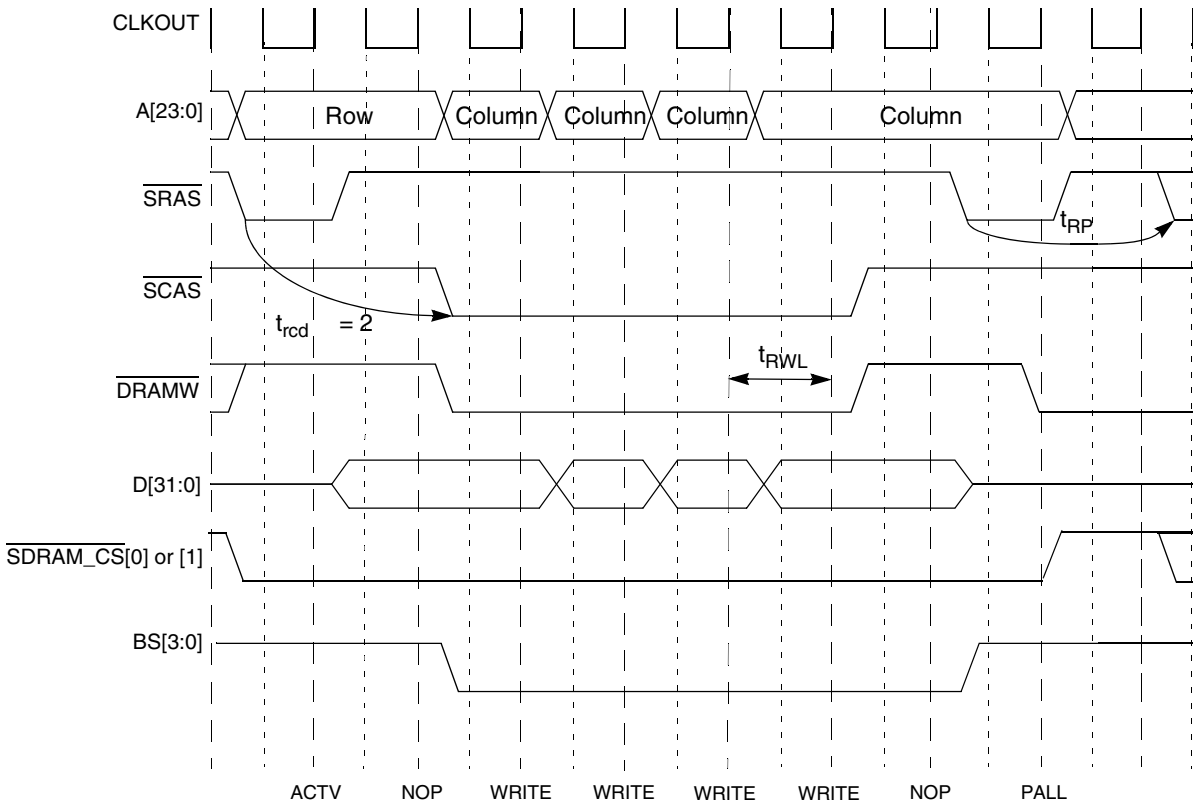


Figure 35-4. Burst Write SDRAM Access

Accesses in synchronous burst page mode always cause the following sequence

- ACTV command
- NOP commands to assure $\overline{\text{SRAS}}$-to-$\overline{\text{SCAS}}$ delay (if CAS latency is 1, there are no NOP commands).
- Required number of READ or WRITE commands to service the transfer size with the given port size.
- Some transfers need more NOP commands to assure the ACTV-to-precharge delay.
- PALL command
- Required number of idle clocks inserted to assure precharge-to-ACTV delay.

35.5.5 Auto-Refresh Operation

The DRAM controller is equipped with a refresh counter and control. This logic is responsible for providing timing and control to refresh the SDRAM without user interaction. Once the refresh counter is set, and refresh is enabled, the counter counts to zero. At this time, an internal refresh request flag is set and the counter begins counting down again. The DRAM controller completes any active burst operation and then performs a PALL operation. The DRAM controller then initiates a refresh cycle and clears the refresh request flag. This refresh cycle includes a delay from any precharge to the auto-refresh command, the auto-refresh command, and then a delay until any ACTV command is allowed. Any SDRAM access initiated during the auto-refresh cycle is delayed until the cycle is completed.

Figure 35-5 shows the auto-refresh timing. In this case, there is an SDRAM access when the refresh request becomes active. The request is delayed by the precharge to ACTV delay programmed into the active SDRAM bank by the CAS bits. The REF command is then generated and the delay required by SDRAM_CTRL[RTIM] is inserted before the next ACTV command is generated. In this example, the next bus cycle is initiated, but does not generate an SDRAM access until TRC is finished. Because both chip selects are active during the REF command, it is passed to both blocks of external SDRAM.

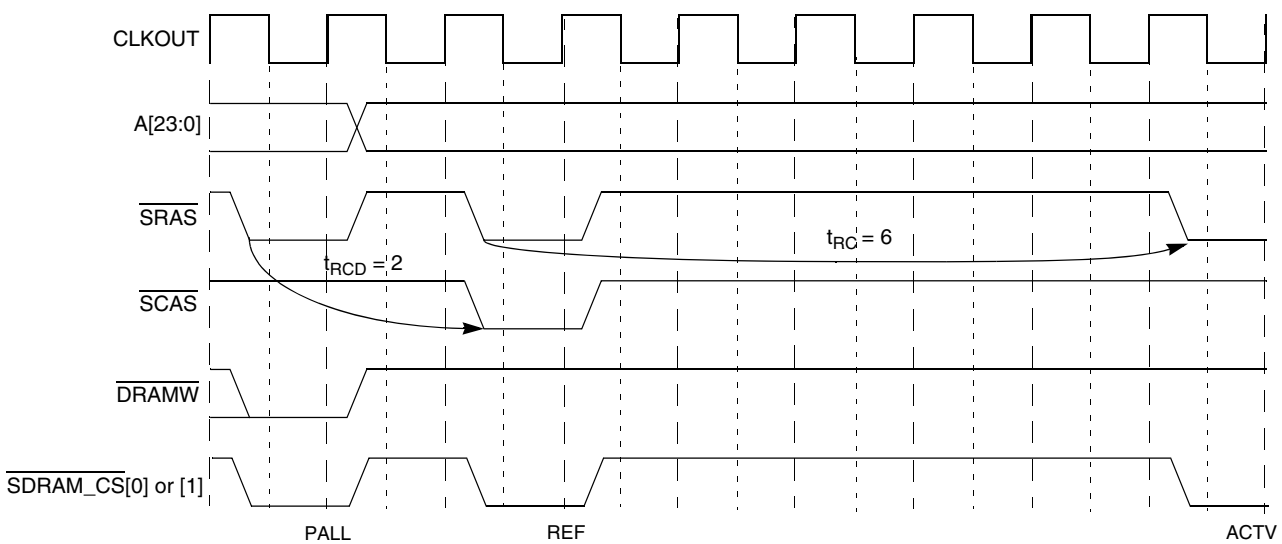


Figure 35-5. Auto-Refresh Operation

35.5.6 Self-Refresh Operation

Self-refresh is a method of allowing the SDRAM to enter into a low-power state, while at the same time to perform an internal refresh operation and to maintain the integrity of the data stored in the SDRAM. The DRAM controller supports self-refresh with

SDRAM_CTRL[IS]. When IS is set, the SELF command is sent to the SDRAM. When IS is cleared, the SELFX command is sent to the DRAM controller. Figure 35-6 diagram shows the self-refresh operation.

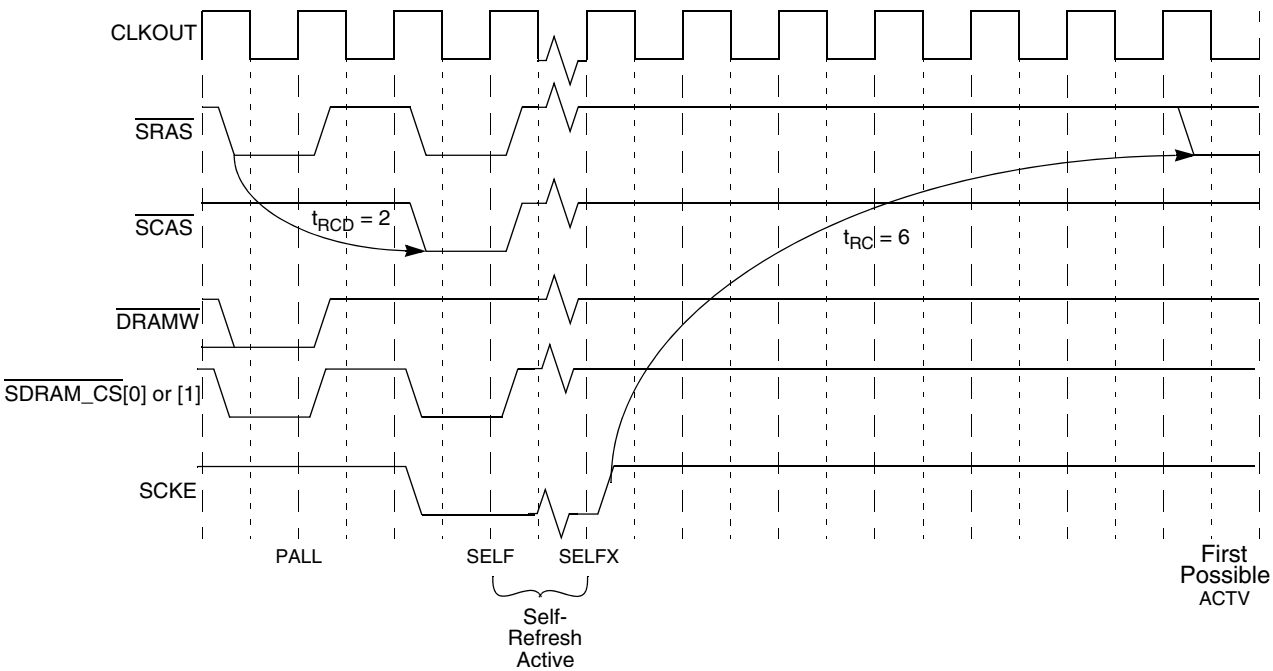


Figure 35-6. Self-Refresh Operation

35.6 Initialization Sequence

Synchronous DRAMs have a prescribed initialization sequence. The DRAM controller supports this sequence with the following procedure:

- SDRAM control signals are reset to idle state. Wait the prescribed period after reset before any action is taken on the SDRAMs. This is normally around 100 µs.
- Initialize the CTRL, AC, and CM registers in their operational configuration. Do not yet enable PALL or REF commands.
- Issue a PALL command to the SDRAMs by setting SDRAM_AC[IP] and accessing a SDRAM location with the size equal the SDRAM port size. Wait the time (determined by t_{RP}) before any other execution.
- Enable refresh (set SDRAM_AC[RE]) and wait for at least 8 refreshes to occur.
- Before issuing the MRS command, determine if the mask bits of CM register need to be modified to allow the MRS to execute properly
- Issue the MRS command by setting SDRAM_AC[IMRS] and accessing a location in the SDRAM with the size equal the SDRAM port size. Note that mode register settings are driven on the SDRAM address bus, so care must be taken to change

SDRAM_CM[BAM] if the mode register configuration does not fall in the address range determined by the address mask bits. After the mode register is set, mask bits of CM register can be restored to their desired configuration.

35.6.1 Mode Register Settings

It is possible to configure the operation of SDRAMs, namely their burst operation and CAS latency, through the SDRAM component's mode register. CAS latency is a function of the speed of the SDRAM and the bus clock of the DRAM controller. The DRAM controller operates at a CAS latency of 1, 2, or 3.

Although the DRAM controller supports bursting operations, it does not use the bursting features of the SDRAMs. Because the SDRAM Controller can burst operand sizes of 1, 2, 4, or 16 bytes long, the concept of a fixed burst length in the SDRAMs mode register becomes problematic. Therefore, the SDRAM controller generates the burst cycles rather than the SDRAM device. Because the SDRAM Controller generates a new address and a READ or WRITE command for each transfer within the burst, the SDRAM mode register should be set either not to burst or to a burst length of one. This allows bursting to be controlled by the SDRAM controller.

The SDRAM mode register is written by setting the associated block's SDRAM_AC[IMRS]. First, the base address and mask registers must be set to the appropriate configuration to allow the mode register to be set. Note that improperly set mask bits of CM register may prevent access to the mode register address. Thus, the user should determine the mapping of the mode register address to the processor address bits to find out if an access is blocked. If the CM register setting prohibits mode register access, then it should be reconfigured to enable the access and then set to its necessary configuration after the MRS command executes.

After SDRAM_AC[IMRS] is set, the next access to the SDRAM address space generates the MRS command to that SDRAM. The address of the access should be selected to place the correct mode information on the SDRAM address pins. The address is not multiplexed for the MRS command. The MRS access can be a read or write and should be equal the SDRAM port size. The important thing is that the address output of that access needs the correct mode programming information on the correct address bits.

Figure 35-7 shows the MRS command, which occurs in the first clock of the bus cycle.

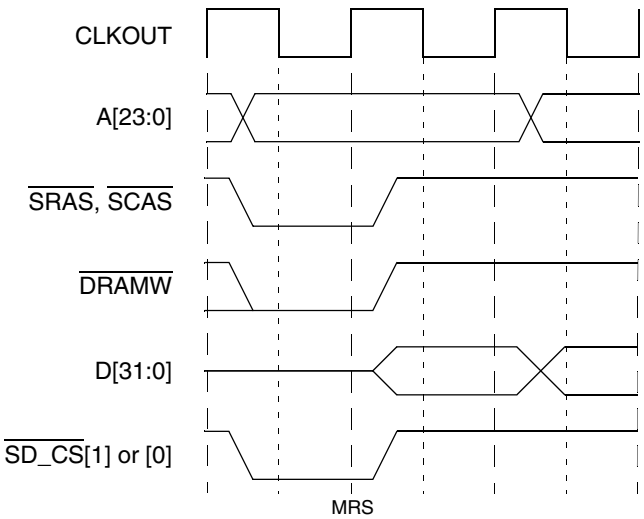


Figure 35-7. Mode Register Set (MRS) Command

35.7 SDRAM Example

This example interfaces a 512K x 32-bit x 4 bank SDRAM component operating at 40 MHz. Table 35-15 table lists design specifications for this example.

Table 35-15. SDRAM Example Specifications

Parameter	Specification
Speed grade (-8E)	40 MHz (25-ns period)
10 rows, 8 columns	
Two bank-select lines to access four internal banks	
ACTV-to-read/write delay (t_{RCD})	20ns(min)
Period between auto-refresh and ACTV command (t_{RC})	70 ns
ACTV command to precharge command (t_{RAS})	48 ns (min)
ACTV command to precharge command (t_{RAS}) 48 ns (min.) Precharge command to ACTV command (t_{RP})	20ns (min)
Last data input to PALL command (t_{RWL})	1 bus clock (25ns)
Auto-refresh period for 4096 rows (t_{REF})	64ms

35.7.1 SDRAM Interface Configuration

To interface this component to the DRAM controller, use the connection table that corresponds to a 32-bit port size with 8 columns. Two pins select one of four banks when the part is functional. The following table shows the proper hardware connections

Table 35-16. SDRAM Hardware Connections

SDRAM Controller Pins	A15	A14	A13	A12	A11	A10	A9	A17	A18	A19	A20	A21	A22
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10=CMD	BA0	BA1

35.7.2 SDRAM_CTRL Register Initialization

At power-up, the SDRAM_CTRL register has the following configuration if synchronous operation and SDRAM address multiplexing are desired.

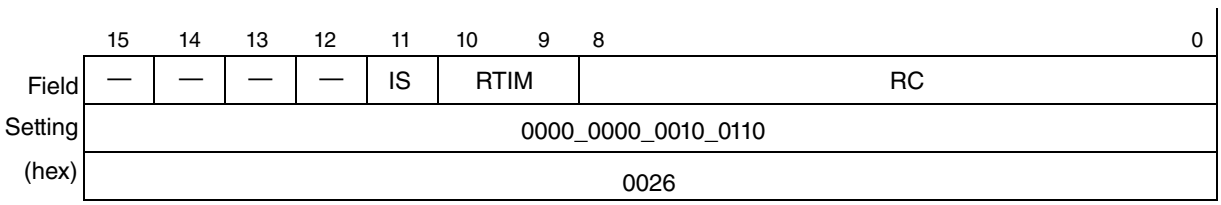


Figure 35-8. Initialization Values for SDRAM_CTRL Register

This configuration results in a value of 0x0026 for SDRAM_CTRL register, as shown in the following table

Table 35-17. DCR Initialization Values

Bits	Name	Setting	Description
15	–	0	Reserved
14	–	0	Reserved
13	-	0	Reserved
12	-	0	Reserved
11	IS	0	At power-up, allowing power self-refresh state is not appropriate because registers are being set up.
10-9	RTIM	00	Because t_{RC} value is 70 ns, indicating a 3-clock refresh-to-ACTV timing.
8-0	RC	0x26	Specification indicates auto-refresh period for 4096 rows to be 64 mS or refresh every 15.625 µs for each

Table 35-17. DCR Initialization Values

Bits	Name	Setting	Description
			row, or 625 bus clocks at 40 MHz. Because SDRAM_CTRL[RC] is incremented by 1 and multiplied by 16, RC = (625 bus clocks/16) -1 = 38.06 = 38

35.7.3 SDRAM_AC Register Initialization

The starting address of the SDRAM is 0x7000_0000. Continuous page mode feature is used.

The SDRAM_AC registers should be programmed as shown in Figure 35-9 figure.

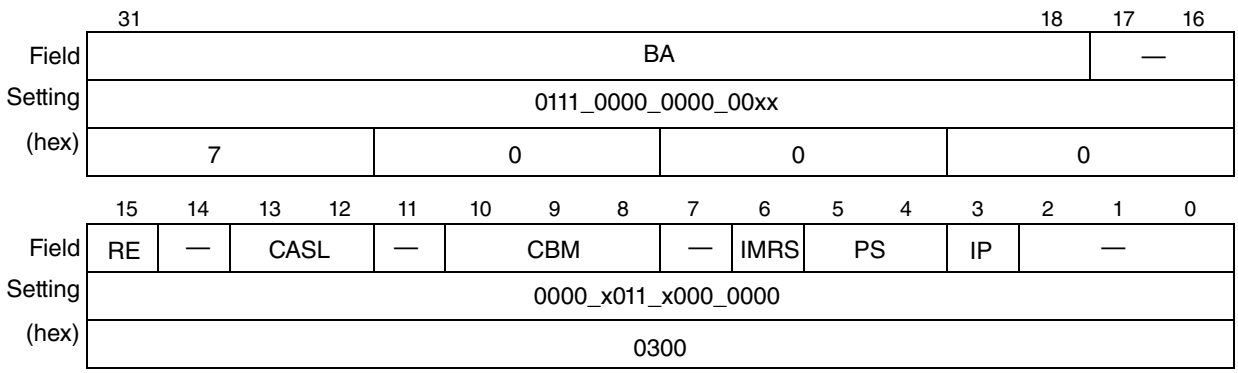


Figure 35-9. SDRAM_AC Register Configuration

This configuration results in a value of SDRAM_AC0 = 0x7000_0300, as described in the following table. SDRAM_AC1 initialization is not needed because there is only one block. Subsequently, SDRAM_AC1[RE,IMRS,IP] should be cleared; everything else is a don't care.

Table 35-18. DACR Initialization Values

Bits	Name	Setting	Description
31–18	BA	0111_0000_0000_00	Base address. So SDRAM_AC0[31–16] = 0x7000, placing the starting address of the SDRAM accessible

Table continues on the next page...

Table 35-18. DACR Initialization Values (continued)

Bits	Name	Setting	Description
			memory at 0x7000_0000.
17-16	–		Reserved. Don't Care.
15	RE	0	Keeps auto-refresh disabled because registers are being set up at this time.
14	–		Reserved. Don't Care.
13-12	CASL	00	Indicates a delay of data 1 cycle after $\overline{\text{SCAS}}$ is asserted
11	–		Reserved. Don't Care.
10-8	CBM	011	Command bit is pin 20 and bank selects are 21 and up.
7	–		Reserved. Don't Care.
6	IMRS	0	Indicates MRS command has not been initiated.
5-4	PS	00	32-bit port
3	IP	0	Indicates precharge has not been initiated.
2-0	–		Reserved. Don't Care.

35.7.4 SDRAM_CM Register Initialization

The SDRAM_CM registers have the following configuration.

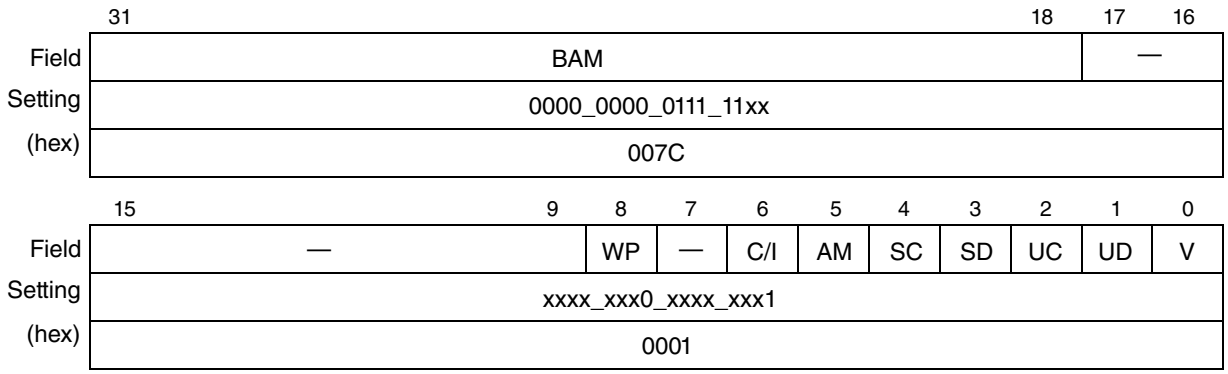


Figure 35-10. SDRAM_CM0 Register

With this configuration, the SDRAM_CM0 = 0x007C_0001, as described in the following table.

Table 35-19. SDRAM_CM0 Initialization Values

Bits	Name	Setting	Description
31–18	BAM		With bits 17 and 16 as don't cares, BAM = 0x007C, which creates 8 MByte block of memory.
17-16	–		Reserved. Don't Care.
15-1	–		Reserved. Don't Care.
0	V	1	Enable accesses.

35.7.5 Mode Register Initialization

When SDRAM_AC[IMRS] is set, a bus cycle initializes the mode register. If the mode register setting is read on A[10:0] of the SDRAM on the first bus cycle, the bit settings on the corresponding processor address pins must be determined while being aware of masking requirements

The following table lists the desired initialization setting:

Table 35-20. Mode Register Initialization

SDRAM Controller Pins	SDRAM Pins	Mode Register Initialization	
A20	A10	Reserved	X
A19	A9	WB	0
A18	A8	Opmode	0

Table continues on the next page...

Table 35-20. Mode Register Initialization (continued)

SDRAM Controller Pins	SDRAM Pins	Mode Register Initialization	
A17	A7	Opmode	0
A9	A6	CASL	0
A10	A5	CASL	0
A11	A4	CASL	1
A12	A3	BT	0
A13	A2	BL	0
A14	A1	BL	0
A15	A0	BL	0

Next, this information is mapped to an address to determine the hexadecimal value.

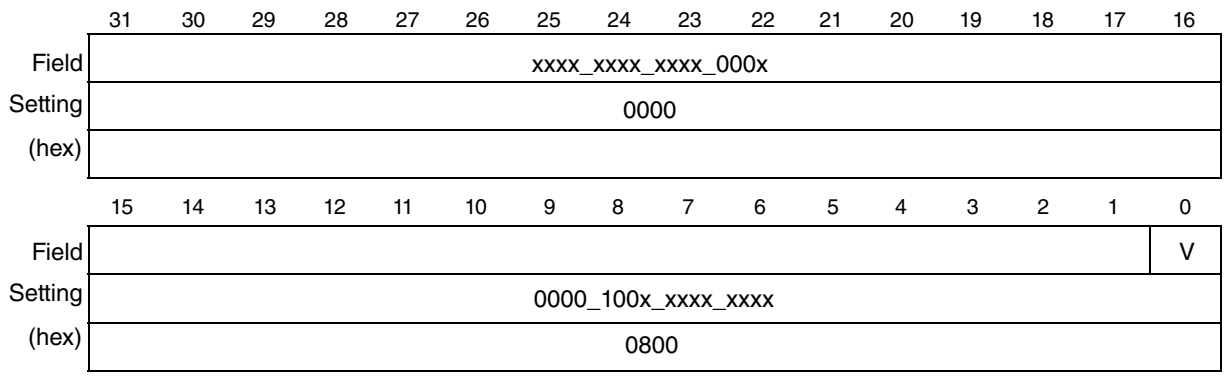


Figure 35-11. Mode Register Mapping to A[31:0]

Chapter 36
Quad Serial Peripheral Interface (QuadSPI)

36.1 Chip-specific QuadSPI information

36.1.1 QSPI Module Instantiations

This device contains one QSPI module . This device contains a single dual-QUADSPI module with upto 8 data lines for XiP functionality. The controller supports singles,dual, quad or octal data lines in single (SDR) or double (DDR) data rate configurations. SDR mode supports upto 100 MHz and DDR mode supports up to 75MHz. Several QuadSPI configurations are possible depending on QuadSPI memory selected. See QSPI Modes of Interfacing for more details.

36.1.2 QSPI Modes of Interfacing

Table 36-1. QSPI implementations supported

	2 separate QSPI/Dual Die flash	2 separate QSPI/Dual Die flash	Spansion HyperFlash™ NOR Memory	Octal flash	Octal flash	Single Die flash	Single Die flash (A)	Single Die flash (B)
	DDR(DQS)	SDR/DDR	DDR	DDR	SDR	DDR	SDR	SDR
Why use?	2 Ind. FLASH	2 Ind. FLASH	BW & Cap.	BW & Cap.	BW & Cap.	Cap.	min pins	min pins
Total pins	14 pins	12 pins	12 pins	11 pins	10 pins	7 pins	6 pins	6 pins
Flash die	2	2	1	1	1	1	1	1
Data pins per QSPI flash die	4	4	8	8	8	4	4	4
A_DQS	1	0	1	1	0	1	0	0
B_DQS	1	0	0	0	0	0	0	0

Table continues on the next page...

Table 36-1. QSPI implementations supported (continued)

	2 separate QSPI/Dual Die flash	2 separate QSPI/Dual Die flash	Spansion HyperFlash™ NOR Memory	Octal flash	Octal flash	Single Die flash	Single Die flash (A)	Single Die flash (B)
	DDR(DQS)	SDR/DDR	DDR	DDR	SDR	DDR	SDR	SDR
A_SS0	1	1	1	1	1	1	1	0
A_SS1	0	0	0	0	0	0	0	0
B_SS0	0	1	0	0	0	0	0	1
B_SS1	1	0	0	0	0	0	0	0
A_SCLK	1	1	1	1	1	1	1	0
B_SCLK	1	1	1	0	0	0	0	1
QSPI Mode Support by Package								
100 lqfp - K82	N	Y	Y	Y	Y	Y	Y	Y
121 xfbga -K82	N	Y	Y	Y	Y	Y	Y	Y
144 lqfp - K82	Y	Y	Y	Y	Y	Y	Y	Y

36.1.2.1 QSPI Pin Muxing

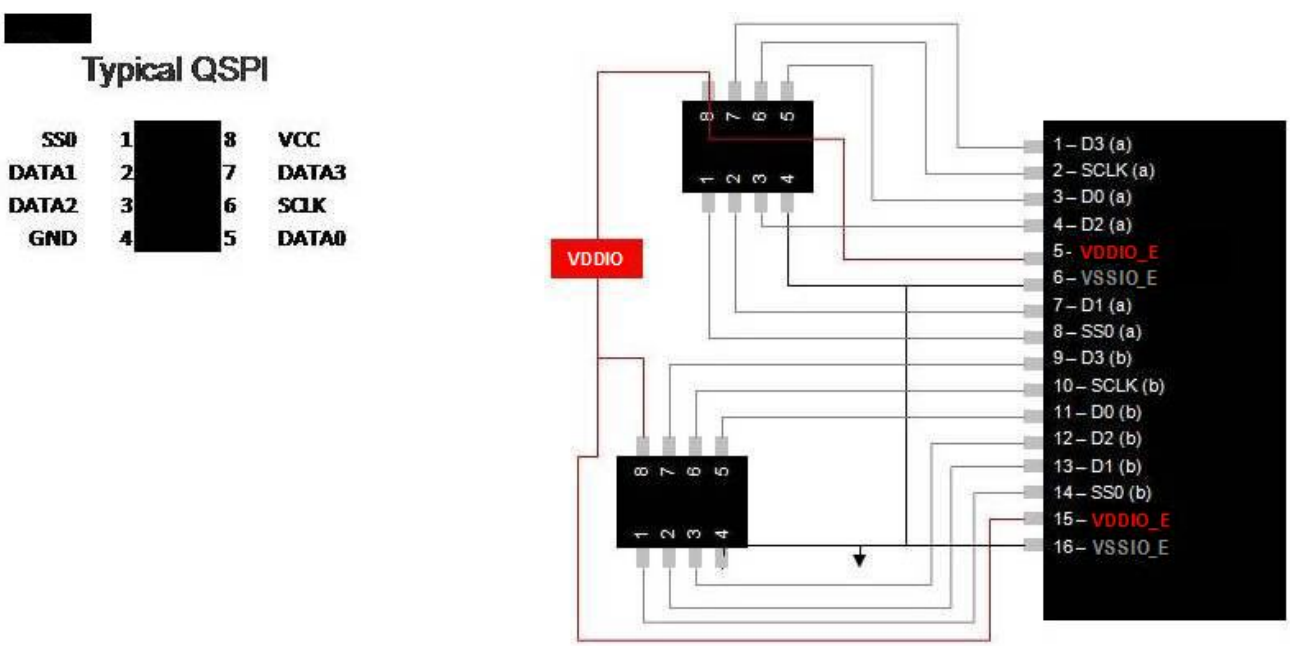


Figure 36-1. QSPI Interface to 2 Separate QSPI in SDR mode

36.1.3 QSPI clocking

Details on the QSPI module can be found in QuadSPI clocking.

36.1.4 QSPI Advanced Configuration

36.1.4.1 QSPI Clock Configuration

- Clock source selection for the clock divider is controlled by QuadSPIx_SOCCR[2:0]

Field	Description
2 – 0 QSPISRC	QSPI clock source select • 000 Core/system clock • 001 MCGFLL clock • 010 MCGPLL clock • 011 MCGPLL 2x clock • 100 IRC48M clock. • 101 OSCERCLK clock • 110 MCGIRCLK clock. • 111 Reserved

- Clock divider is configured by QuadSPIx_MCR[27:24]

Field	Description
27 – 24 SCLKCFG	Serial clock divider • 0000 Divide by 1 • 0001 Divide by 2 • 0010 Divide by 3 • 0011 Divide by 4 • .... • 1111 Divide by 16

36.1.4.2 QSPI Octal Flash Pinmux Configuration

- Octal flash pinmux is configured by QuadSPIx_SOCCR[15:13] in addition to the Port Control module.

Field	Description
15 OCTEN	Octal data pins enable When this bit is set QSPI0B_DATAx pins are switched to QSPI Port A to composite eight bit data bus 0 QSPI0B_DATAx pins are assigned to QSPI Port B

Table continues on the next page...

Field	Description
	1 QSPI0B_DATAx pins are assigned to QSPI Port A
14 DIFFCKEN	Differential flash clock pins enable When this bit is set QSPI0B_SCLK pin serves as an inverse QSPI0A_SCLK, QSPI0B_SS1_B pin serves as an inverse CK2 clock if CK2EN bit is set as well. 0 Differential flash clock is disabled. 1 Differential flash clock is enabled.
13 CK2EN	Flash CK2 clock pin enable When this bit is set QSPI0B_DQS pin serves as flash CK2 clock, QSPI0B_SS1_B pin serves as an inverse CK2 clock if DIFFCKEN bit is set as well. CK2 and inverse CK2 are only available in 144 pin packages 0 CK2 flash clock is disabled 1 CK2 flash clock is enabled

- After configure the Alt selection and QuadSPIx_SOCCR[15:13], QSPI Port A can operate in octal mode.

Pin Name	Alt Selection	Alt Function	QSPIx_SOCCR	Octal Flash Pin
PTE0	ALT5	QSPI0A_DATA3	–	DQ3
PTE1/LLWU_P0	ALT5	QSPI0A_SCLK	–	CK
PTE2/LLWU_P1	ALT5	QSPI0A_DATA0	–	DQ0
PTE3	ALT5	QSPI0A_DATA2	–	DQ2
PTE4/LLWU_P2	ALT5	QSPI0A_DATA1	–	DQ1
PTE5	ALT5	QSPI0A_SS0B	–	CS#
PTE6/LLWU_P16	ALT5	QSPI0B_DATA3	QSPIx_SOCCR[OCTEN]	DQ7
PTE7	ALT5	QSPI0B_SCLK	QSPIx_SOCCR[DIFFCKEN]	CK#
PTE8	ALT5	QSPI0B_DATA0	QSPIx_SOCCR[OCTEN]	DQ4
PTE9/LLWU_P17	ALT5	QSPI0B_DATA2	QSPIx_SOCCR[OCTEN]	DQ6
PTE10/LLWU_P18	ALT5	QSPI0B_DATA1	QSPIx_SOCCR[OCTEN]	DQ5
PTE11	ALT7	QSPI0A_DQS	–	DQS
PTE12	ALT5	QSPI0B_DQS	QSPIx_SOCCR[CK2EN]	CK2
PTE13	ALT5	QSPI0B_SS1_B	QSPIx_SOCCR[DIFFCKEN] QSPIx_SOCCR[CK2EN]	CK2#

36.1.4.3 QSPI DQS Configuration

- To support high flash clock frequency DQS function need be enabled. Besides the QuadSPIx_MCR[DQS_EN] and QuadSPIx_MCR[DQS_LAT_EN], there are other control bits in QuadSPIx_SOCCR register as below.

Field	Description
29 – 24 DLYTAPSELB	Delay chain tap number selection for QSPI Port B DQS 000000 Select 1 delay chain tap 000001 Select 2 delay chain taps 000010 Select 3 delay chain taps .... 111111 Select 64 delay chain tap
21 – 16 DLYTAPSELA	Delay chain tap number selection for QSPI Port A DQS 000000 Select 1 delay chain tap 000001 Select 2 delay chain taps 000010 Select 3 delay chain taps .... 111111 Select 64 delay chain tap
12 DQSINVSEL	Select clock source for internal DQS generation 0 Use 1x internal reference clock for the DQS generation 1 Use inverse 1x internal reference clock for the DQS generation
11 – 10 DQSPHASEL	Select phase shift for internal DQS generation. These bits are always zero in SDR mode. 00 No phase shift 01 Select 45 degree phase shift 10 Select 90 degree phase shift 11 Select 135 degree phase shift
9 DQSPADLPEN	When this bit is set the internal generated DQS will be sent to the DQS pad first and then looped back to QuadSPI. DQSLPEN should be cleared when this bit is set. 0 DQS loop back from DQS pad is disabled 1 DQS loop back from DQS pad is enabled
8 DQSLPEN	When this bit is set the internal generated DQS is selected and looped back to QuadSPI, without going to DQS pad. DQSPADLPEN should be cleared when this bit is set. 0 DQS loop back is disabled 1 DQS loop back is enabled

36.1.5 QuadSPI_MCR[SCLKCFG] implementation

The following table shows the serial clock configuration for this chip.

Table 36-2. QuadSPI_MCR[SCLKCFG] field description

Field	Description
31-24 SCLKCFG	Serial Clock Configuration. Used for dividing clocks. 0x00: Divide by 1 0x01: Divide by 2

Table 36-2. QuadSPI_MCR[SCLKCFG] field description

Field	Description
	0x02: Divide by 3 0x04: Divide by 4 ... 0x0F: Divide by 16 All others: reserved

36.1.6 QuadSPI register reset values

All reset values for the QuadSPI registers that are device specific are shown in the following tables. All other register reset values are shown in the module memory map.

Table 36-3. QuadSPI Module Configuration Register Reset Values

Register	Reset Value
Module Configuration Register (QuadSPI_MCR)	000F_400Ch

Table 36-4. QuadSPI Buffer Configuration Register Reset Values

Register	Reset Value
Buffer0 Configuration Register (QuadSPI_BUF0CR)	0000_0002h
Buffer1 Configuration Register (QuadSPI_BUF1CR)	0000_0003h
Buffer2 Configuration Register (QuadSPI_BUF2CR)	0000_0004h
Buffer3 Configuration Register (QuadSPI_BUF3CR)	8000_0000h

Table 36-5. Serial Flash A1 Top Address Reset Values

Register	Reset Value
QuadSPI0_SFA1AD	6fff_fc00h

Table 36-6. Serial Flash A2 Top Address Reset Values

Register	Reset Value
QuadSPI0_SFA2AD	6fff_fc00h

Table 36-7. Serial Flash B1 Top Address Reset Values

Register	Reset Value
QuadSPI0_SFB1AD	6fff_fc00h

Table 36-8. Serial Flash B2 Top Address Reset Values

Register	Reset Value
QuadSPI0_SFB2AD	6fff_fc00h

36.1.7 QuadSPI AHB flexible buffer size

For this chip, the size of the complete buffer mentioned in Flexible AHB buffers is 512 bytes.

36.2 Introduction

The Quad Serial Peripheral Interface (QuadSPI) block acts as an interface to one single or two external serial flash devices, each with up to eight bidirectional data lines.

36.2.1 Features

The QuadSPI supports the following features:

- Flexible sequence engine to support various flash vendor devices.
- Single, dual, quad and octal modes of operation.
- DDR/DTR mode wherein the data is generated on every edge of the serial flash clock.
- Support for flash data strobe signal for data sampling in DDR and SDR mode.
- Support for parallel writes via register mapped interface in single I/O mode.
- Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth.

- DMA support to read RX Buffer data via AMBA AHB bus (64-bit width interface) or IP registers space (32-bit access) and DMA support to fill TX Buffer via IPS register space (32-bit access).
  - Inner loop size of DMA access can be configured.
- Multimaster accesses with priority
  - Flexible and configurable buffer for each master
- Multiple interrupt conditions (see Table 36-18)
- Memory mapped read access to connected flash devices.
- Programmable sequence engine to cater to future command/protocol changes and able to support all existing vendor commands and operations.
  - Supports all types of addressing.
- Support for interfacing with On-The-Fly-Decryption-Engine (OTFAD).

36.2.2 Block Diagram

The following figure is a block diagram of the Quad Serial Peripheral Interface (QuadSPI) module.

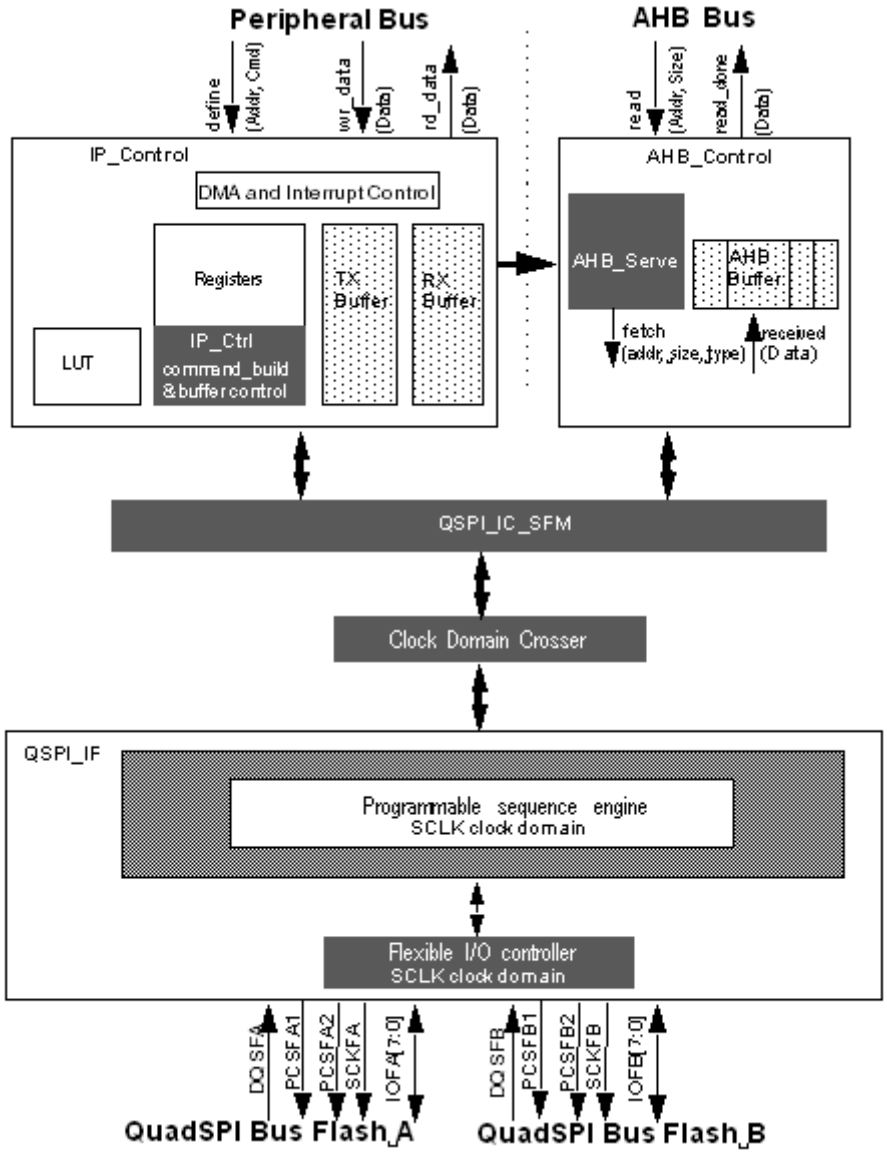


Figure 36-2. QuadSPI Block Diagram

36.2.3 QuadSPI Modes of Operation

This section provides information about the modes in which the QuadSPI module can be used.

36.2.3.1 Normal Mode

In this mode, one or two external serial flash memory devices can be accessed. Further details about this mode of operation can be found in Modes of Operation (Normal Mode).

36.2.3.2 Module Disable Mode

This mode is used for power management of the device containing the QuadSPI module. It is controlled by signals external to the QuadSPI. The clock to the non-memory mapped logic in the QuadSPI can be stopped while in Module Disable Mode.

36.2.3.3 Stop Mode

This mode is also used for power management. When a request is made to enter Stop Mode, the QuadSPI block completes the action currently being processed, before the request is acknowledged.

36.2.4 Acronyms and Abbreviations

The following table contains acronyms and abbreviations used in this document.

Table 36-9. Acronyms and Abbreviations

Terms	Description
AHB	Advanced High-performance Bus, version of AMBA
AMBA	Advanced Microcontroller Bus Architecture
BE	Big Endian Byte Ordering
CS	Chip Select
DMA	Direct Memory Access
MB	Megabyte. Each MB is 1024 * 1024 bytes
IFM	Individual Flash Mode
PFM	Parallel Flash Mode
LSB	Least Significant Bit
MSB	Most Significant Bit
PCS	Peripheral Chip Select
QSPI, QuadSPI	Quad Serial Peripheral Interface
SCK	Serial Communications Clock
w1c	Write 1 to clear, writing a 1 to this field resets the flag

36.2.5 Glossary for QuadSPI module

Table 36-10. Glossary

Term	Definition
AHB Command	An AHB Command is a SFM Command triggered by a read access to the address range belonging to the memory mapped access defined in Table 36-15. Refer to AHB Commands for details.
Asserted	A signal that is asserted is in its active state. An active low signal changes from logic level one to logic level zero when asserted, and an active high signal changes from logic level zero to logic level one.
Clear	To clear a bit or bits means to establish logic level zero on the bit or bits.
Clock Phase	Determines when the data should be sampled relative to the active edge of SCK
Clock Polarity	Determines the idle state of the SCK signal.
Drain	To remove entries from a FIFO by software or hardware.
Endianness	Byte Ordering scheme.
Field	Two or more register bits grouped together.
Fill	To add entries to a FIFO by software or hardware.
Host	Refers to another functional block in the device containing the QuadSPI module
Instruction Code	8 bits defining the type of command to be executed.
IP Command	An IP Command is a SFM Command triggered by writing into the QSPI_IPCR[SEQID] field.
Logic level one	The voltage that corresponds to Boolean true (1) state.
Logic level zero	The voltage that corresponds to Boolean false (0) state.
Negated	A signal that is negated is in its inactive state. An active low signal changes from logic level 0 to logic level 1 when negated, and an active high signal changes from logic level 1 to logic level 0.
QSPI_AMBA_BASE	First address of QuadSPI address space on system memory map.
QSPI_ARDB_BASE	First address of QuadSPI Rx Buffer on system memory map.
Set	To set a bit or bits means to establish logic level one on the bit or bits.
RX Buffer PUSH Event	Addition of valid entries into the RX Buffer. In the default case each Buffer PUSH Event adds 2 entries to the RX Buffer since the interface to the serial clock domain is 64 bits in width. Depending on the number of bytes read from the serial flash device it is possible for the very last Buffer PUSH Event that only one entry is added. The QSPI_RBSR[RDBFL] field is incremented by the number of entries added to the RX Buffer.
RX Buffer POP Event	Removal of valid entries from the RX Buffer. Each Buffer POP Event removes (QSPI_RBCT[WMRK] + 1) valid entries from the buffer. The QSPI_RBSR[RDBFL] field is decremented by the same number and the QSPI_RBSR[RDCTR] field is incremented accordingly.
Individual Flash Mode	Access to a single, individual serial flash device. Refer to Serial Flash Access Schemes for details.
Parallel Flash Mode	Read access to two serial flash devices attached to the QuadSPI module in parallel. Refer to Serial Flash Access Schemes for details.
SFM Command	Serial Flash Memory Command. A SFM command consists of an instruction code and all other parameters (for example, size or mode bytes) needed for that specific instruction code. Triggering a command either initiates a transaction on the external serial flash or results in an error. Refer to Table 36-29 for details on errors.
Single/Dual/Quad/Octal Instructions	Depending on the serial flash device connected to the QuadSPI module there will be instructions using a different number of data lines. • Single: Single line I/O with one data out and one data in line to/from the serial flash device. • Dual: Dual line I/O with two bidirectional I/O lines, driven alternatively by the serial flash device or the QuadSPI module

Table continues on the next page...

Table 36-10. Glossary (continued)

Term	Definition
	• Quad: Quad line I/O with 4 bidirectional I/O lines, driven alternatively by the serial flash device or the QuadSPI • Octal: Octal line I/O with 8 bidirectional I/O lines, driven alternatively by the serial flash device or the QuadSPI
Transaction	A transaction consists of all flags, data and signals in either direction to execute a command for an attached serial flash device. It is a combination of chip select, sclk, instruction code, address, mode- and/or dummy bytes, transmit and/or receive data.
LUT	Look-up table.

36.3 External Signal Description

This section provides the external signal information of the QuadSPI module.

The following table lists the external signals belonging to the module in conjunction with the different modes of operation.

Table 36-11. Signal Properties

Signal Name	Function	Direction	Description
PCSFA1	Peripheral Chip Select Flash A1	O	This signal is the chip select for the serial flash device A1. A1 represents the first device in a dual-die package flash A or the first of the two flash devices that share IOFA. Refer to Dual Die Flashes for more details.
PCSFA2	Peripheral Chip Select Flash A2	O	This signal is the chip select for the serial flash device A2. A2 represents the second device in a dual-die package flash A or the second of the two flash devices that share IOFA. Refer to Dual Die Flashes for more details.
PCSFB1	Peripheral Chip Select Flash B1	O	This signal is the chip select for the serial flash device B1. B1 represents the first device in a dual-die package flash B or the first of the two flash devices that share IOFB. Refer to Dual Die Flashes for more details.
PCSFB2	Peripheral Chip Select Flash B2	O	This signal is the chip select for the serial flash device B2. B2 represents the second device in a dual-die package flash B or the second of the two flash devices that share IOFB. Refer to Dual Die Flashes for more details.
SCKFA	Serial Clock Flash A	O	This signal is the serial clock output to the serial flash device A.
SCKFB	Serial Clock Flash B	O	This signal is the serial clock output to the serial flash device B.
IOFA[7:0]	Serial I/O Flash A	I/O	These signals are the data I/O lines to/from the serial flash device A. Refer to Driving External Signals for details about the signal drive and timing behavior. Note that the signal pins of the serial flash device may change their function according to the SFM Command executed, leaving them as control inputs when Single and Dual Instructions are executed. The module supports driving these inputs to dedicated values. In single I/O mode, QuadSPI drives data on IOFA[0] and expects data on IOFA[1].
IOFB[7:0]	Serial I/O Flash B	I/O	These signals are the data I/O lines to/from the serial flash device B. Refer to Driving External Signals for details about the signal drive and timing behavior. Note that the signal pins of the serial flash device may change their function according to the SFM Command executed, leaving them as

Table continues on the next page...

Table 36-11. Signal Properties (continued)

Signal Name	Function	Direction	Description
			control inputs when Single and Dual Instructions are executed. The module supports driving these inputs to dedicated values. In single I/O mode, QuadSPI drives data on IOFB[0] and expects data on IOFB[1].
DQSFA	Data Strobe signal Flash A	I	Data strobe signal for port A. Some flash vendors provide the DQS signal to which the read data is aligned in DDR mode.
DQSFB	Data Strobe signal Flash B	I	Data strobe signal for port B. Some flash vendors provide the DQS signal to which the read data is aligned in DDR mode.

36.3.1 Driving External Signals

The different phases of the serial flash access scheme are shown in the following figure.

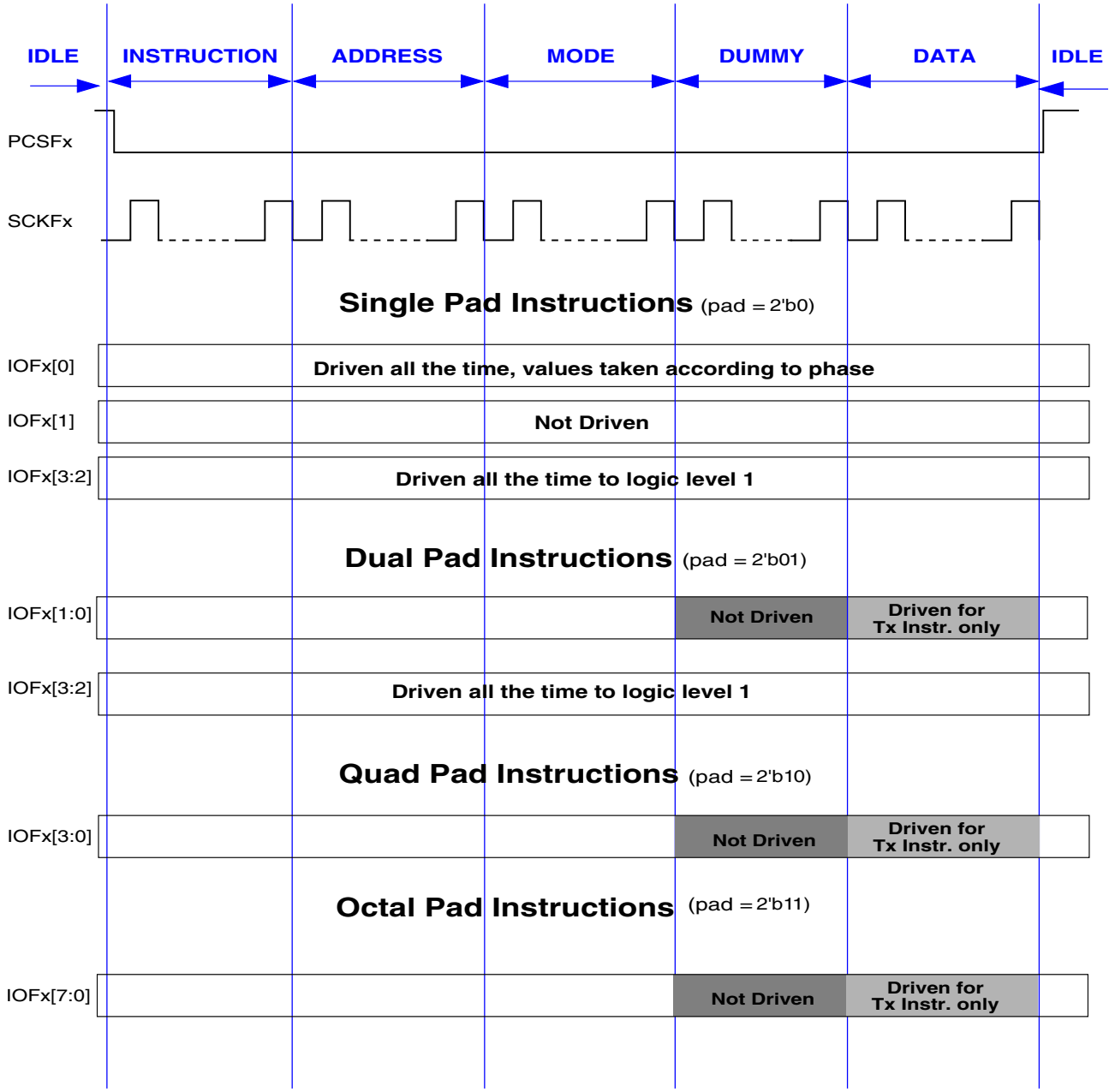


Figure 36-3. Serial Flash Access Scheme

The different phases and the I/O driving characteristics of the QuadSPI module are characterized in the following way:

- IDLE: Serial flash device not selected. No interaction with the serial flash device. All IOFx signals driven.
- INSTRUCTION: Serial flash device selected. The instruction is sent to the serial flash device. All IOFx signals are driven.

- ADDRESS: Serial Flash Address is sent to the device. All IOFx signals are driven. Note that this phase is not applicable for all SFM Commands.
- MODE: Mode bytes are sent to the serial flash device. All IOFx signals are driven. Note that this phase is not applicable for all SFM Commands.
- DUMMY: Dummy clocks are provided to the serial flash device. Refer to the Figure 36-3 for the IOFx signals driven. The actual data lines required for the SFM Command executed are not driven for data read commands. Note that this phase is not applicable for all SFM Commands.
- DATA: Serial flash data are sent to or received from the serial flash device. Refer to the preceding figure for the IOFx signals driven. The actual data lines required for the SFM Command executed are not driven for data read commands. Note that this phase is not applicable for all SFM Commands.

The PCSFx and SCKFx signals are driven permanently throughout all the phases.

In Individual Flash Mode this applies to the selected flash device. In Parallel Flash Mode this applies to both serial flash devices simultaneously.

36.4 Memory Map and Register Definition

This section provides the memory map and register definitions of the QuadSPI module.

36.4.1 Register Write Access

This section describes the write access restriction terms that apply to all registers, which can be one of the following:

- **Register Write Access Restriction**

  For each register bit and register field, the write access conditions are specified in the detailed register description. A description of the write access conditions is given in the following table. If, for a specific register bit or field, none of the given write access conditions is fulfilled, any write attempt to this register bit or field is ignored without any notification. The values of the bits or fields are not changed.

  The condition term [A or B] indicates that the register or field can be written to if at least one of the conditions is fulfilled.

Table 36-12. Register Write Access Restrictions

Condition	Description
Anytime	No write access restriction.
Disabled Mode	Write access only if *QSPI_MCR[MDIS] = 1*.
Normal Mode	Write access only if the module is in *Normal Mode*.

- **Register Write Access Requirements**

  All registers can be accessed with 8-bit, 16-bit, and 32-bit wide operations. For some of the registers, at least a 16/32-bit wide write access is required to ensure correct operation. This write access requirement is stated in the detailed register description for each register affected.

36.4.2 Peripheral Bus Register Descriptions

This section provides the memory map and register definitions of the QuadSPI module.

NOTE

Accesses to location 0x4 do not give transfer errors.

QuadSPI memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_A000	Module Configuration Register (QuadSPI0_MCR)	32	R/W	See section	36.4.2.1/ 901
400D_A008	IP Configuration Register (QuadSPI0_IPCR)	32	R/W	0000_0000h	36.4.2.2/ 904
400D_A00C	Flash Configuration Register (QuadSPI0_FLSHCR)	32	R/W	0000_0303h	36.4.2.3/ 905
400D_A010	Buffer0 Configuration Register (QuadSPI0_BUF0CR)	32	R/W	See section	36.4.2.4/ 906
400D_A014	Buffer1 Configuration Register (QuadSPI0_BUF1CR)	32	R/W	See section	36.4.2.5/ 907
400D_A018	Buffer2 Configuration Register (QuadSPI0_BUF2CR)	32	R/W	See section	36.4.2.6/ 909
400D_A01C	Buffer3 Configuration Register (QuadSPI0_BUF3CR)	32	R/W	See section	36.4.2.7/ 910

Table continues on the next page...

QuadSPI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_A020	Buffer Generic Configuration Register (QuadSPI0_BFGENCR)	32	R/W	0000_0000h	36.4.2.8/ 911
400D_A024	SOC Configuration Register (QuadSPI0_SOCCR)	32	R/W	0000_0000h	36.4.2.9/ 912
400D_A030	Buffer0 Top Index Register (QuadSPI0_BUF0IND)	32	R/W	0000_0000h	36.4.2.10/ 913
400D_A034	Buffer1 Top Index Register (QuadSPI0_BUF1IND)	32	R/W	0000_0000h	36.4.2.11/ 913
400D_A038	Buffer2 Top Index Register (QuadSPI0_BUF2IND)	32	R/W	0000_0000h	36.4.2.12/ 914
400D_A100	Serial Flash Address Register (QuadSPI0_SFAR)	32	R/W	0000_0000h	36.4.2.13/ 915
400D_A104	Serial Flash Address Configuration Register (QuadSPI0_SFACR)	32	R/W	0000_0000h	36.4.2.14/ 915
400D_A108	Sampling Register (QuadSPI0_SMPR)	32	R/W	0000_0000h	36.4.2.15/ 916
400D_A10C	RX Buffer Status Register (QuadSPI0_RBSR)	32	R	0000_0000h	36.4.2.16/ 918
400D_A110	RX Buffer Control Register (QuadSPI0_RBCT)	32	R/W	0000_0000h	36.4.2.17/ 919
400D_A150	TX Buffer Status Register (QuadSPI0_TBSR)	32	R	0000_0000h	36.4.2.18/ 920
400D_A154	TX Buffer Data Register (QuadSPI0_TBDR)	32	R/W	0000_0000h	36.4.2.19/ 921
400D_A158	Tx Buffer Control Register (QuadSPI0_TBCT)	32	R/W	0000_0000h	36.4.2.20/ 922
400D_A15C	Status Register (QuadSPI0_SR)	32	R	0200_3800h	36.4.2.21/ 923
400D_A160	Flag Register (QuadSPI0_FR)	32	w1c	0800_0000h	36.4.2.22/ 926
400D_A164	Interrupt and DMA Request Select and Enable Register (QuadSPI0_RSER)	32	R/W	0000_0000h	36.4.2.23/ 929
400D_A168	Sequence Suspend Status Register (QuadSPI0_SPNDST)	32	R	0000_0000h	36.4.2.24/ 933
400D_A16C	Sequence Pointer Clear Register (QuadSPI0_SPTRCLR)	32	R/W	0000_0000h	36.4.2.25/ 935
400D_A180	Serial Flash A1 Top Address (QuadSPI0_SFA1AD)	32	R/W	See section	36.4.2.26/ 936
400D_A184	Serial Flash A2 Top Address (QuadSPI0_SFA2AD)	32	R/W	See section	36.4.2.27/ 936
400D_A188	Serial Flash B1Top Address (QuadSPI0_SFB1AD)	32	R/W	See section	36.4.2.28/ 937
400D_A18C	Serial Flash B2Top Address (QuadSPI0_SFB2AD)	32	R/W	See section	36.4.2.29/ 937

Table continues on the next page...

QuadSPI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_A190	Data Learn Pattern Register (QuadSPI0_DLPR)	32	R/W	AA55_3443h	36.4.2.30/ 938
400D_A200	RX Buffer Data Register (QuadSPI0_RBDR0)	32	R	0000_0000h	36.4.2.31/ 938
400D_A204	RX Buffer Data Register (QuadSPI0_RBDR1)	32	R	0000_0000h	36.4.2.31/ 938
400D_A208	RX Buffer Data Register (QuadSPI0_RBDR2)	32	R	0000_0000h	36.4.2.31/ 938
400D_A20C	RX Buffer Data Register (QuadSPI0_RBDR3)	32	R	0000_0000h	36.4.2.31/ 938
400D_A210	RX Buffer Data Register (QuadSPI0_RBDR4)	32	R	0000_0000h	36.4.2.31/ 938
400D_A214	RX Buffer Data Register (QuadSPI0_RBDR5)	32	R	0000_0000h	36.4.2.31/ 938
400D_A218	RX Buffer Data Register (QuadSPI0_RBDR6)	32	R	0000_0000h	36.4.2.31/ 938
400D_A21C	RX Buffer Data Register (QuadSPI0_RBDR7)	32	R	0000_0000h	36.4.2.31/ 938
400D_A220	RX Buffer Data Register (QuadSPI0_RBDR8)	32	R	0000_0000h	36.4.2.31/ 938
400D_A224	RX Buffer Data Register (QuadSPI0_RBDR9)	32	R	0000_0000h	36.4.2.31/ 938
400D_A228	RX Buffer Data Register (QuadSPI0_RBDR10)	32	R	0000_0000h	36.4.2.31/ 938
400D_A22C	RX Buffer Data Register (QuadSPI0_RBDR11)	32	R	0000_0000h	36.4.2.31/ 938
400D_A230	RX Buffer Data Register (QuadSPI0_RBDR12)	32	R	0000_0000h	36.4.2.31/ 938
400D_A234	RX Buffer Data Register (QuadSPI0_RBDR13)	32	R	0000_0000h	36.4.2.31/ 938
400D_A238	RX Buffer Data Register (QuadSPI0_RBDR14)	32	R	0000_0000h	36.4.2.31/ 938
400D_A23C	RX Buffer Data Register (QuadSPI0_RBDR15)	32	R	0000_0000h	36.4.2.31/ 938
400D_A300	LUT Key Register (QuadSPI0_LUTKEY)	32	R/W	5AF0_5AF0h	36.4.2.32/ 939
400D_A304	LUT Lock Configuration Register (QuadSPI0_LCKCR)	32	R/W	0000_0002h	36.4.2.33/ 940
400D_A310	Look-up Table register (QuadSPI0_LUT0)	32	R/W	See section	36.4.2.34/ 941
400D_A314	Look-up Table register (QuadSPI0_LUT1)	32	R/W	See section	36.4.2.34/ 941
400D_A318	Look-up Table register (QuadSPI0_LUT2)	32	R/W	See section	36.4.2.34/ 941

Table continues on the next page...

QuadSPI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_A31C	Look-up Table register (QuadSPI0_LUT3)	32	R/W	See section	36.4.2.34/ 941
400D_A320	Look-up Table register (QuadSPI0_LUT4)	32	R/W	See section	36.4.2.34/ 941
400D_A324	Look-up Table register (QuadSPI0_LUT5)	32	R/W	See section	36.4.2.34/ 941
400D_A328	Look-up Table register (QuadSPI0_LUT6)	32	R/W	See section	36.4.2.34/ 941
400D_A32C	Look-up Table register (QuadSPI0_LUT7)	32	R/W	See section	36.4.2.34/ 941
400D_A330	Look-up Table register (QuadSPI0_LUT8)	32	R/W	See section	36.4.2.34/ 941
400D_A334	Look-up Table register (QuadSPI0_LUT9)	32	R/W	See section	36.4.2.34/ 941
400D_A338	Look-up Table register (QuadSPI0_LUT10)	32	R/W	See section	36.4.2.34/ 941
400D_A33C	Look-up Table register (QuadSPI0_LUT11)	32	R/W	See section	36.4.2.34/ 941
400D_A340	Look-up Table register (QuadSPI0_LUT12)	32	R/W	See section	36.4.2.34/ 941
400D_A344	Look-up Table register (QuadSPI0_LUT13)	32	R/W	See section	36.4.2.34/ 941
400D_A348	Look-up Table register (QuadSPI0_LUT14)	32	R/W	See section	36.4.2.34/ 941
400D_A34C	Look-up Table register (QuadSPI0_LUT15)	32	R/W	See section	36.4.2.34/ 941
400D_A350	Look-up Table register (QuadSPI0_LUT16)	32	R/W	See section	36.4.2.34/ 941
400D_A354	Look-up Table register (QuadSPI0_LUT17)	32	R/W	See section	36.4.2.34/ 941
400D_A358	Look-up Table register (QuadSPI0_LUT18)	32	R/W	See section	36.4.2.34/ 941
400D_A35C	Look-up Table register (QuadSPI0_LUT19)	32	R/W	See section	36.4.2.34/ 941
400D_A360	Look-up Table register (QuadSPI0_LUT20)	32	R/W	See section	36.4.2.34/ 941
400D_A364	Look-up Table register (QuadSPI0_LUT21)	32	R/W	See section	36.4.2.34/ 941
400D_A368	Look-up Table register (QuadSPI0_LUT22)	32	R/W	See section	36.4.2.34/ 941
400D_A36C	Look-up Table register (QuadSPI0_LUT23)	32	R/W	See section	36.4.2.34/ 941
400D_A370	Look-up Table register (QuadSPI0_LUT24)	32	R/W	See section	36.4.2.34/ 941

Table continues on the next page...

QuadSPI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_A374	Look-up Table register (QuadSPI0_LUT25)	32	R/W	See section	36.4.2.34/ 941
400D_A378	Look-up Table register (QuadSPI0_LUT26)	32	R/W	See section	36.4.2.34/ 941
400D_A37C	Look-up Table register (QuadSPI0_LUT27)	32	R/W	See section	36.4.2.34/ 941
400D_A380	Look-up Table register (QuadSPI0_LUT28)	32	R/W	See section	36.4.2.34/ 941
400D_A384	Look-up Table register (QuadSPI0_LUT29)	32	R/W	See section	36.4.2.34/ 941
400D_A388	Look-up Table register (QuadSPI0_LUT30)	32	R/W	See section	36.4.2.34/ 941
400D_A38C	Look-up Table register (QuadSPI0_LUT31)	32	R/W	See section	36.4.2.34/ 941
400D_A390	Look-up Table register (QuadSPI0_LUT32)	32	R/W	See section	36.4.2.34/ 941
400D_A394	Look-up Table register (QuadSPI0_LUT33)	32	R/W	See section	36.4.2.34/ 941
400D_A398	Look-up Table register (QuadSPI0_LUT34)	32	R/W	See section	36.4.2.34/ 941
400D_A39C	Look-up Table register (QuadSPI0_LUT35)	32	R/W	See section	36.4.2.34/ 941
400D_A3A0	Look-up Table register (QuadSPI0_LUT36)	32	R/W	See section	36.4.2.34/ 941
400D_A3A4	Look-up Table register (QuadSPI0_LUT37)	32	R/W	See section	36.4.2.34/ 941
400D_A3A8	Look-up Table register (QuadSPI0_LUT38)	32	R/W	See section	36.4.2.34/ 941
400D_A3AC	Look-up Table register (QuadSPI0_LUT39)	32	R/W	See section	36.4.2.34/ 941
400D_A3B0	Look-up Table register (QuadSPI0_LUT40)	32	R/W	See section	36.4.2.34/ 941
400D_A3B4	Look-up Table register (QuadSPI0_LUT41)	32	R/W	See section	36.4.2.34/ 941
400D_A3B8	Look-up Table register (QuadSPI0_LUT42)	32	R/W	See section	36.4.2.34/ 941
400D_A3BC	Look-up Table register (QuadSPI0_LUT43)	32	R/W	See section	36.4.2.34/ 941
400D_A3C0	Look-up Table register (QuadSPI0_LUT44)	32	R/W	See section	36.4.2.34/ 941
400D_A3C4	Look-up Table register (QuadSPI0_LUT45)	32	R/W	See section	36.4.2.34/ 941
400D_A3C8	Look-up Table register (QuadSPI0_LUT46)	32	R/W	See section	36.4.2.34/ 941

Table continues on the next page...

QuadSPI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_A3CC	Look-up Table register (QuadSPI0_LUT47)	32	R/W	See section	36.4.2.34/ 941
400D_A3D0	Look-up Table register (QuadSPI0_LUT48)	32	R/W	See section	36.4.2.34/ 941
400D_A3D4	Look-up Table register (QuadSPI0_LUT49)	32	R/W	See section	36.4.2.34/ 941
400D_A3D8	Look-up Table register (QuadSPI0_LUT50)	32	R/W	See section	36.4.2.34/ 941
400D_A3DC	Look-up Table register (QuadSPI0_LUT51)	32	R/W	See section	36.4.2.34/ 941
400D_A3E0	Look-up Table register (QuadSPI0_LUT52)	32	R/W	See section	36.4.2.34/ 941
400D_A3E4	Look-up Table register (QuadSPI0_LUT53)	32	R/W	See section	36.4.2.34/ 941
400D_A3E8	Look-up Table register (QuadSPI0_LUT54)	32	R/W	See section	36.4.2.34/ 941
400D_A3EC	Look-up Table register (QuadSPI0_LUT55)	32	R/W	See section	36.4.2.34/ 941
400D_A3F0	Look-up Table register (QuadSPI0_LUT56)	32	R/W	See section	36.4.2.34/ 941
400D_A3F4	Look-up Table register (QuadSPI0_LUT57)	32	R/W	See section	36.4.2.34/ 941
400D_A3F8	Look-up Table register (QuadSPI0_LUT58)	32	R/W	See section	36.4.2.34/ 941
400D_A3FC	Look-up Table register (QuadSPI0_LUT59)	32	R/W	See section	36.4.2.34/ 941
400D_A400	Look-up Table register (QuadSPI0_LUT60)	32	R/W	See section	36.4.2.34/ 941
400D_A404	Look-up Table register (QuadSPI0_LUT61)	32	R/W	See section	36.4.2.34/ 941
400D_A408	Look-up Table register (QuadSPI0_LUT62)	32	R/W	See section	36.4.2.34/ 941
400D_A40C	Look-up Table register (QuadSPI0_LUT63)	32	R/W	See section	36.4.2.34/ 941

36.4.2.1 Module Configuration Register (QuadSPIx_MCR)

The QuadSPI_MCR holds configuration data associated with QuadSPI operation.

Write:

- *All other fields: Anytime*

Address: 400D_A000h base + 0h offset = 400D_A000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	SCLKCFG								Reserved				Reserved			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved	MDIS	Reserved		0	0	Reserved		DDR_EN	DQS_EN	DQS_LAT_EN	Reserved	END_CFG		SWRSTHD	SWRSTSD
W					CLR_TXF	CLR_RXF										
Reset	0	1	0	0	0	0	0	0	0	0	0	0	*	*	0	0

* Notes:

- END_CFG field: See the module configuration for the device specific reset value.

QuadSPIx_MCR field descriptions

Field	Description
31–24 SCLKCFG	Serial Clock Configuration. This field configuration is chip specific. For details, refer to chip-specific QuadSPI information. It may be used for dividing clocks.

Table continues on the next page...

QuadSPIx_MCR field descriptions (continued)

Field	Description
23–20 Reserved	This field is reserved.
19–16 Reserved	This field is reserved. This field is reserved and should always be set to 0xF.
15 Reserved	This field is reserved. This field is reserved.
14 MDIS	Module Disable. The MDIS bit allows the clock to the non-memory mapped logic in the QuadSPI to be stopped, putting the QuadSPI in a software controlled power-saving state. 0 Enable QuadSPI clocks. 1 Allow external logic to disable QuadSPI clocks.
13–12 Reserved	This field is reserved.
11 CLR_TXF	Clear TX FIFO/Buffer. Invalidates the TX Buffer content. This is a self-clearing field. 0 No action. 1 Read and write pointers of the TX Buffer are reset to 0. QSPI_TBSR[TRCTR] is reset to 0.
10 CLR_RXF	Clear RX FIFO. Invalidates the RX Buffer. This is a self-clearing field. 0 No action. 1 Read and write pointers of the RX Buffer are reset to 0. QSPI_RBSR[RDBFL] is reset to 0.
9–8 Reserved	This field is reserved.
7 DDR_EN	DDR mode enable 0 2x and 4x clocks are disabled for SDR instructions only 1 2x and 4x clocks are enabled supports both SDR and DDR instruction.
6 DQS_EN	DQS enable. This field is valid for both SDR and DDR mode. For more details, refer to Data Strobe (DQS) sampling method. 0 DQS disabled. 1 DQS enabled. When enabled, the incoming data is sampled on both the edges of DQS input when QSPI_MCR[DDR_EN] is set, else, on only one edge when QSPI_MCR[DDR_EN] is 0. The QSPI_SMPR[DDR_SMP] values are ignored.
5 DQS_LAT_EN	DQS Latency Enable. This field is valid when latency is included in between read access from flash memory in cases when QSPI_MCR[DQS_EN] is 1. For more details, refer to Data Strobe (DQS) sampling method. 0 DQS Latency disabled 1 DQS feature with latency included enabled
4 Reserved	This field is reserved.
3–2 END_CFG	Defines the endianness of the QuadSPI module. For more details refer to Byte Ordering Endianess
1 SWRSTHD	Software reset for AHB domain

Table continues on the next page...

QuadSPIx_MCR field descriptions (continued)

Field	Description
	0 No action 1 AHB domain flops are reset. Does not reset configuration registers. It is advisable to reset both the serial flash domain and AHB domain at the same time. Resetting only one domain might lead to side effects. **NOTE:** The software resets need the clock to be running to propagate to the design. The MCR[MDIS] should therefore be set to 0 when the software reset bits are asserted. Also, before they can be deasserted again (by setting MCR[SWRSTHD] to 0), it is recommended to set the MCR[MDIS] bit to 1. Once the software resets have been deasserted, the normal operation can be started by setting the MCR[MDIS] bit to 0.
0 SWRSTSD	Software reset for serial flash domain 0 No action 1 Serial Flash domain flops are reset. Does not reset configuration registers. It is advisable to reset both the serial flash domain and AHB domain at the same time. Resetting only one domain might lead to side effects. **NOTE:** The software resets need the clock to be running to propagate to the design. The MCR[MDIS] should therefore be set to 0 when the software reset bits are asserted. Also, before they can be deasserted again (by setting MCR[SWRSTSD] to 0), it is recommended to set the MCR[MDIS] bit to 1. Once the software resets have been deasserted, the normal operation can be started by setting the MCR[MDIS] bit to 0.

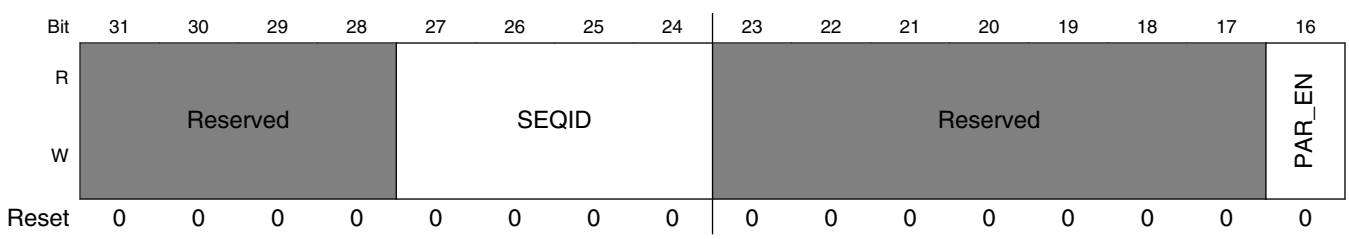
36.4.2.2 IP Configuration Register (QuadSPIx_IPCR)

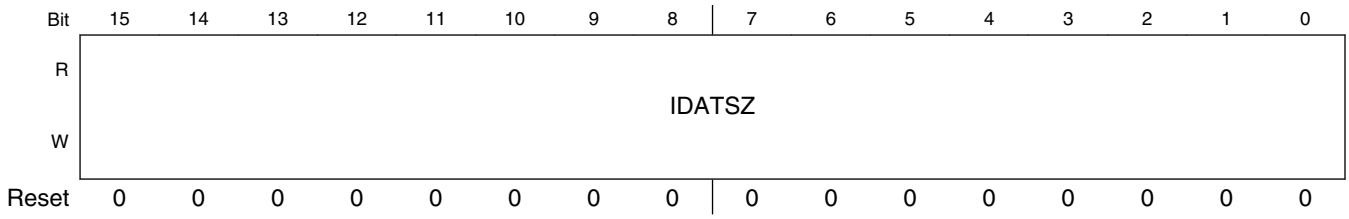
The IP configuration register provides all the configuration required for an IP initiated command. An IP command can be triggered by writing in the SEQID field of this register. If the SEQID field is written successfully, a new command to the external serial flash is started as per the sequence pointed to by the SEQID field. Refer to Normal Mode , for details about the command triggering and command execution.

Write:

- *QSPI_SR[IP_ACC]=0*

Address: 400D_A000h base + 8h offset = 400D_A008h





QuadSPIx_IPCR field descriptions

Field	Description
31–28 Reserved	This field is reserved.
27–24 SEQID	Points to a sequence in the Look-up table. This field defines bits [6:2] of the LUT index. The bits [1:0] are always assumed to be 0. Refer to Look-up Table for more details. A write to this field triggers a transaction on the serial flash interface.
23–17 Reserved	This field is reserved.
16 PAR_EN	When set, a transaction to two serial flash devices is triggered in parallel mode. Refer to Parallel Flash Mode for more details.
IDATSZ	IP data transfer size. Defines the data transfer size in bytes of the IP command.

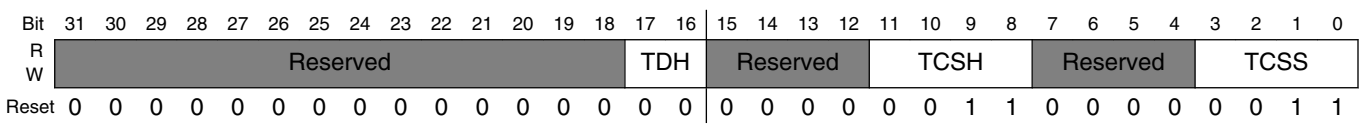
36.4.2.3 Flash Configuration Register (QuadSPIx_FLSHCR)

The Flash configuration register contains the flash device specific timings that must be met by the QuadSPI controller for the device to function correctly.

Write:

- *QSPI_SR[AHB_ACC] = 0*
- *QSPI_SR[IP_ACC] = 0*

Address: 400D_A000h base + Ch offset = 400D_A00Ch



QuadSPIx_FLSHCR field descriptions

Field	Description
31–18 Reserved	This field is reserved.
17–16 TDH	Serial flash data in hold time. This helps in meeting the Data In Hold time requirement of a flash. This is valid only in DDR mode. **NOTE:** This field should be set to 0x00 in SDR mode (QuadSPI_MCR[DDR_EN]=0). Refer to Data input hold requirement of Flash for details.

Table continues on the next page...

QuadSPIx_FLSHCR field descriptions (continued)

Field	Description
	00 Data aligned with the posedge of Internal reference clock of QuadSPI 01 Data aligned with 2x serial flash half clock 10 Data aligned with 4x serial flash half clock
15–12 Reserved	This field is reserved.
11–8 TCSH	Serial flash CS hold time in terms of serial flash clock cycles. **NOTE:** The actual delay between chip select and clock is defined as: • TCSH = 1 SCK clk if N= 0/1 else, N SCK clk if N>1, where N is the setting of TCSH
7–4 Reserved	This field is reserved. Reserved.
TCSS	Serial flash CS setup time in terms of serial flash clock cycles. **NOTE:** 1. The actual delay between chip select and clock is defined as: • TCSS = 0.5 SCK clk if N= 0/1 else, N+0.5 SCK clk if N>1, where N is the setting of TCSS. 2. Any update to the TCSS register bits is visible on the flash interface only from the second transaction following the update.

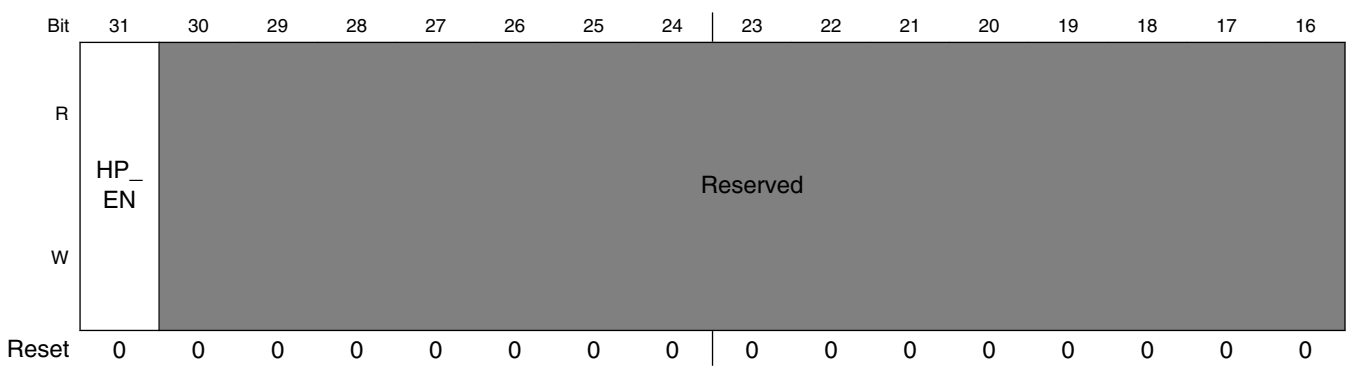
36.4.2.4 Buffer0 Configuration Register (QuadSPIx_BUF0CR)

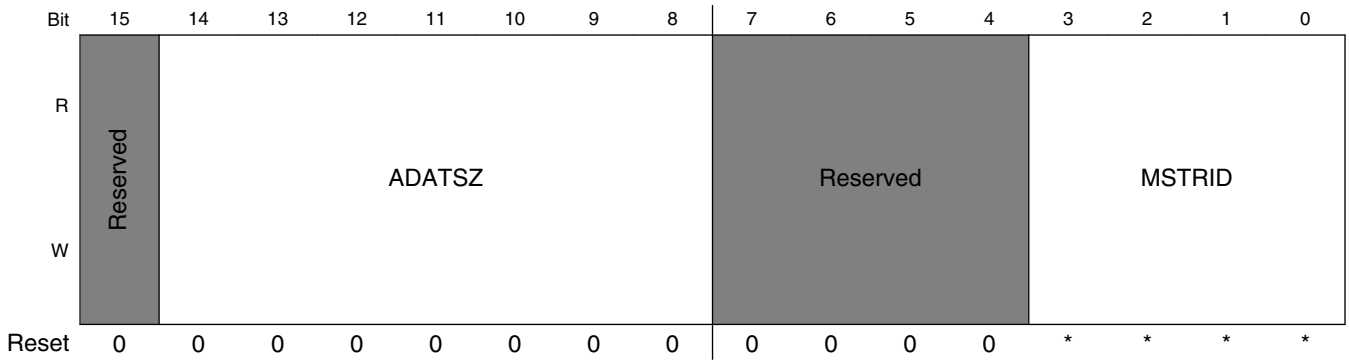
This register provides the configuration for any access to buffer0. An access is routed to buffer0 when the master port number of the incoming AHB request matches the MSTRID field of BUF0CR. Any buffer "miss" leads to a serial flash transaction being triggered as per the sequence pointed to the SEQID field. Buffer0 may also be configured as a high priority buffer by setting the HP_EN field of this register.

Write:

- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 10h offset = 400D_A010h





* Notes:
- MSTRID field: See the module configuration for reset value.

QuadSPIx_BUF0CR field descriptions

Field	Description
31 HP_EN	High Priority Enable. When set, the master associated with this buffer is assigned a priority higher than the rest of the masters. An access by a high priority master will suspend any ongoing prefetch by another AHB master and will be serviced on high priority. The high priority feature is disabled if OTFAD is enabled in the system. Refer to Flexible AHB Buffers for details.
30–16 Reserved	This field is reserved.
15 Reserved	This field is reserved.
14–8 ADATSZ	AHB data transfer size Defines the data transfer size in 8 bytes of an AHB triggered access to serial flash. For example, a value of 0x2 will set transfer size to 16 bytes. When ADATSZ = 0, the data size mentioned the sequence pointed to by the SEQID field overrides this value. Software should ensure that this transfer size is not greater than the size of this buffer. If OTFAD is enabled, the QuadSPI module prefetches only those many data's from flash memory such that the prefetch never crosses the 1 KB boundary.
7–4 Reserved	This field is reserved.
MSTRID	Master ID. The ID of the AHB master associated with BUFFER0. Any AHB access with this master port number is routed to this buffer. It must be ensured that the master IDs associated with all buffers must be different.

36.4.2.5 Buffer1 Configuration Register (QuadSPIx_BUF1CR)

This register provides the configuration for any access to buffer1. An access is routed to buffer1 when the master port number of the incoming AHB request matches the MSTRID field of BUF1CR. Any buffer "miss" leads to the buffer being flushed and a serial flash transaction being triggered as per the sequence pointed to by the SEQID field.

Write:
- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 14h offset = 400D_A014h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved	ADATSZ							Reserved				MSTRID			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*

* Notes:

- MSTRID field: See the module configuration for reset value.

QuadSPIx_BUF1CR field descriptions

Field	Description
31–16 Reserved	This field is reserved.
15 Reserved	This field is reserved.
14–8 ADATSZ	AHB data transfer size Defines the data transfer size in 8 bytes of an AHB triggered access to serial flash.For example, a value of 0x2 will set transfer size to 16bytes. When ADATSZ = 0, the data size mentioned the sequence pointed to by the SEQID field overrides this value. Software should ensure that this transfer size is not greater than the size of this buffer. If OTFAD is enabled, the QuadSPI module prefetches only those many data's from Flash such that the prefetch never crosses the 1 KB boundary.
7–4 Reserved	This field is reserved.
MSTRID	Master ID. The ID of the AHB master associated with BUFFER1. Any AHB access with this master port number is routed to this buffer. It must be ensured that the master IDs associated with all buffers must be different.

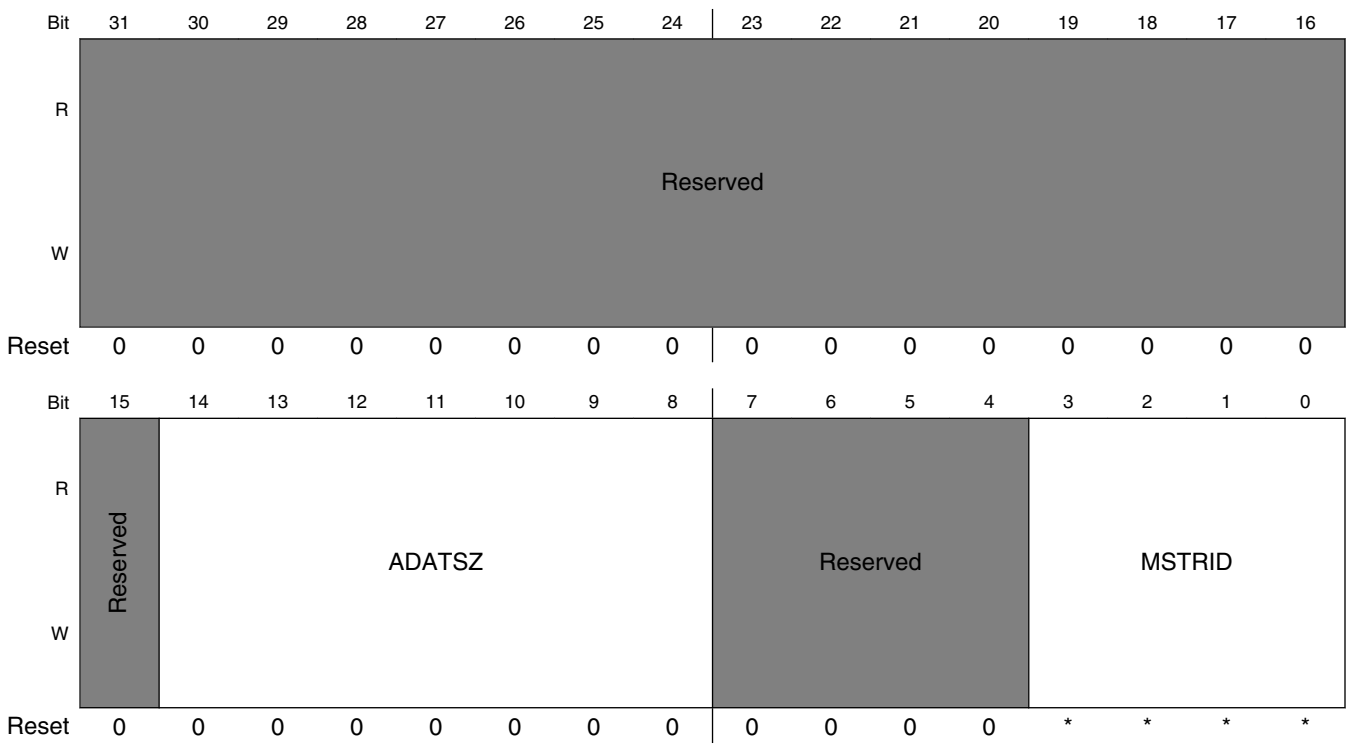
36.4.2.6 Buffer2 Configuration Register (QuadSPIx_BUF2CR)

This register provides the configuration for any access to buffer2. An access is routed to buffer2 when the master port number of the incoming AHB request matches the MSTRID field of BUF2CR. Any buffer "miss" leads to the buffer being flushed and a serial flash transaction being triggered as per the sequence pointed to by the SEQID field.

Write:

- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 18h offset = 400D_A018h



* Notes:

- MSTRID field: See the module configuration for the device specific reset value.

QuadSPIx_BUF2CR field descriptions

Field	Description
31–16 Reserved	This field is reserved. Reserved.
15 Reserved	This field is reserved.
14–8 ADATSZ	AHB data transfer size Defines the data transfer size in 8 bytes of an AHB triggered access to serial flash. For example, a value of 0x2 will set transfer size to 16 bytes. When ADATSZ = 0, the data size mentioned the sequence pointed

Table continues on the next page...

QuadSPIx_BUF2CR field descriptions (continued)

Field	Description
	to by the SEQID field overrides this value. Software should ensure that this transfer size is not greater than the size of this buffer. If OTFAD is enabled, the QuadSPI module prefetches only those many data's from flash memory such that the prefetch never crosses the 1KB boundary.
7–4 Reserved	This field is reserved. Reserved.
MSTRID	Master ID. The ID of the AHB master associated with BUFFER2. Any AHB access with this master port number is routed to this buffer. It must be ensured that the master IDs associated with all buffers must be different.

36.4.2.7 Buffer3 Configuration Register (QuadSPIx_BUF3CR)

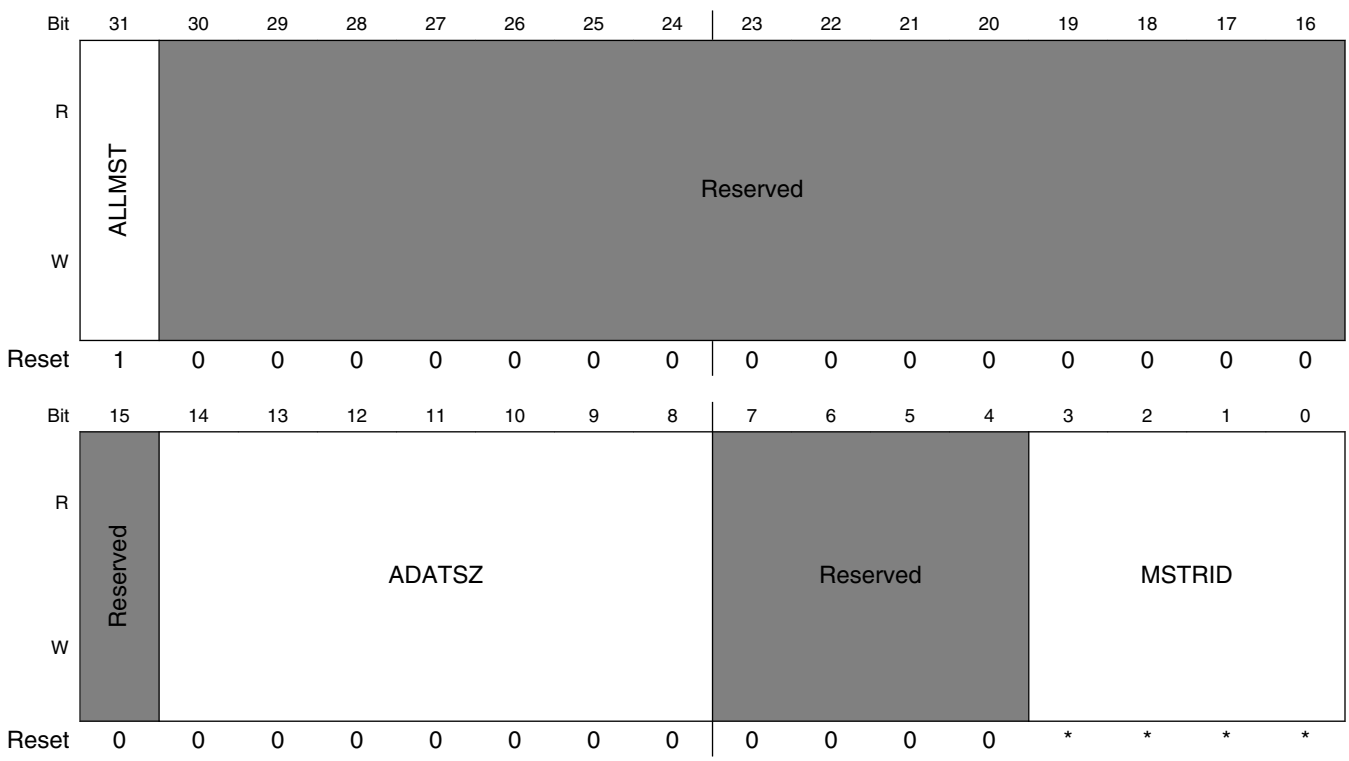
This register provides the configuration for any access to buffer3. An access is routed to buffer3 when the master port number of the incoming AHB request matches the MSTRID field of BUF3CR. Any buffer "miss" leads to the buffer being flushed a serial flash transaction being triggered as per the sequence pointed to by the SEQID field.

In the case that the ALLMST field is not set, any such transaction (where master port number does not match any of the MSTRID fields) will be returned an ERROR response.

Write:

- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 1Ch offset = 400D_A01Ch



* Notes:
- MSTRID field: See the module configuration for the device specific reset value.

QuadSPIx_BUF3CR field descriptions

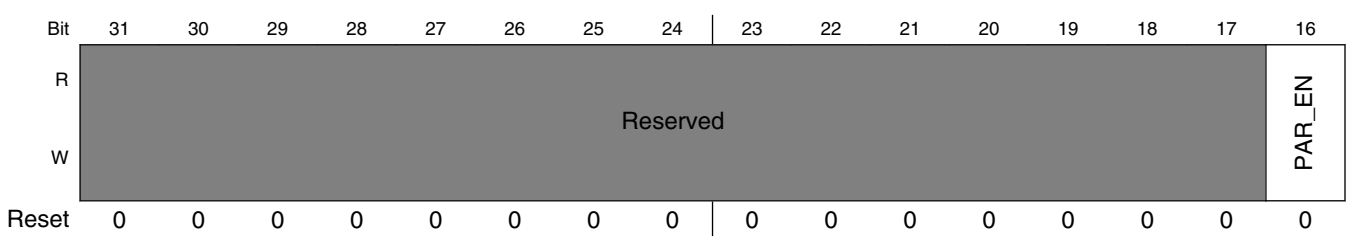
Field	Description
31 ALLMST	All master enable. When set, buffer3 acts as an all-master buffer. Any AHB access with a master port number not matching with the master ID of buffer0 or buffer1 or buffer2 is routed to buffer3. When set, the MSTRID field of this register is ignored.
30–16 Reserved	This field is reserved. Reserved.
15 Reserved	This field is reserved.
14–8 ADATSZ	AHB data transfer size Defines the data transfer size in 8 Bytes of an AHB triggered access to serial flash. When ADATSZ = 0, the data size mentioned the sequence pointed to by the SEQID field overrides this value. Software should ensure that this transfer size is not greater than the size of this buffer. If OTFAD is enabled, the QuadSPI module prefetches only those many data's from flash memory such that the prefetch never crosses the 1 KB boundary.
7–4 Reserved	This field is reserved.
MSTRID	Master ID. The ID of the AHB master associated with BUFFER3. Any AHB access with this master port number is routed to this buffer. It must be ensured that the master IDs associated with all buffers must be different.

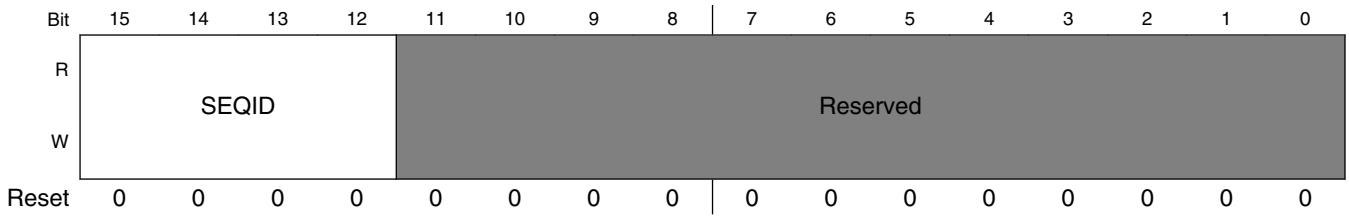
36.4.2.8 Buffer Generic Configuration Register (QuadSPIx_BFGENCR)

This register provides the generic configuration to any of the buffer accesses. Any buffer "miss" leads to the buffer being flushed and a serial flash transaction being triggered as per the sequence pointed to by the SEQID field. If the PAR_EN field is set, all the buffer accesses result in parallel accesses to the flashes.

Write:
- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 20h offset = 400D_A020h





QuadSPIx_BFGENCR field descriptions

Field	Description
31–17 Reserved	This field is reserved.
16 PAR_EN	When set, a transaction to two serial flash devices is triggered in parallel mode. Refer to Parallel Flash Mode for more details.
15–12 SEQID	Points to a sequence in the Look-up-table. The SEQID defines the bits [6:2] of the LUT index. The bits [1:0] are always assumed to be 0. Refer to Look-up Table. **NOTE:** If the sequence pointer differs between the new and previous sequence then the user should reset this. See QSPI_SPTRCLR for more information.
Reserved	This field is reserved.

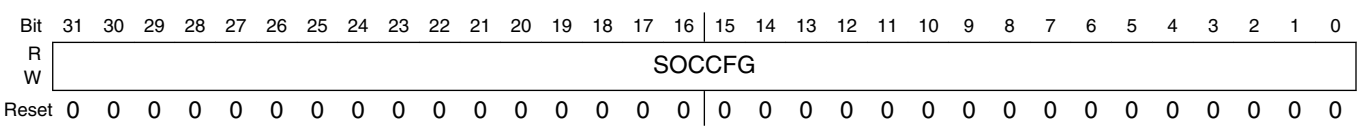
36.4.2.9 SOC Configuration Register (QuadSPIx_SOCCR)

This register is programmed at chip level for QuadSPI delay chain configuration. For details, refer to chip-specific QuadSPI information.

Write:

- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 24h offset = 400D_A024h



QuadSPIx_SOCCR field descriptions

Field	Description
SOCCFG	SOC Configuration For details, refer to chip-specific QuadSPI information.

36.4.2.10 Buffer0 Top Index Register (QuadSPIx_BUF0IND)

This register specifies the top index of buffer0, which defines its size. Note that that the 3 LSBs of this register are set to zero. This ensures that the buffer is 64-bit aligned, as each buffer entry is 64 bits long.

The register value should be set to the desired number of bytes less 8. For example, setting BUF0IND to 0 gives 8 bytes, 1 gives 16 bytes etc.

The size of buffer0 is the difference between BUF0IND+8 and 0.

It is the responsibility of the software to ensure that BUF0IND value is not greater than the overall size of the buffer. The hardware does not provide any protection against illegal programming.

Write:

- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 30h offset = 400D_A030h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	TPINDX0																													Reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

QuadSPIx_BUF0IND field descriptions

Field	Description
31–3 TPINDX0	Top index of buffer 0.
Reserved	This field is reserved. Reserved.

36.4.2.11 Buffer1 Top Index Register (QuadSPIx_BUF1IND)

This register specifies the top index of buffer1, which defines its size. Note that the 3 LSBs of this register are set to zero. This ensures that the buffer is 64-bit aligned as each buffer entry is 64 bits long.

The size of buffer1 is the difference between BUF1IND and BUF0IND. The register value should be entered in bytes. For example, If BUF0IND = 0x100 then setting BUF1IND = 0x130 will set buffer1 size to 0x30 bytes.

It is the responsibility of the software to ensure that BUF1IND value is not greater than the overall size of the buffer. The hardware does not provide any protection against illegal programming.

Write:

- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 34h offset = 400D_A034h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	TPINDX1																													Reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

QuadSPIx_BUF1IND field descriptions

Field	Description
31–3 TPINDX1	Top index of buffer 1.
Reserved	This field is reserved.

36.4.2.12 Buffer2 Top Index Register (QuadSPIx_BUF2IND)

This register specifies the top index of buffer2, which defines its size. Note that that the 3 LSBs of this register are set to zero. This ensures that the buffer is 64-bit aligned as each buffer entry is 64 bits long.

The size of buffer2 is the difference between the BUF2IND and BUF1IND. The register value should be entered in bytes. For example, if BUF1IND = 0x130 then setting BUF2IND = 0x180 will set buffer2 size to 0x50 bytes.

It is the responsibility of the software to ensure that BUF2IND value is not greater than the overall size of the buffer. The hardware does not provide any protection against illegal programming.

Write:

- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 38h offset = 400D_A038h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	TPINDX2																													Reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

QuadSPIx_BUF2IND field descriptions

Field	Description
31–3 TPINDX2	Top index of buffer 2.
Reserved	This field is reserved.

36.4.2.13 Serial Flash Address Register (QuadSPIx_SFAR)

The module automatically translates this address on the memory map to the address on the flash itself. When operating in 24-bit mode, only bits 23-0 are sent to the flash. In 32-bit mode, bits 27-0 are used with bits 31-28 driven to 0 when QSPI_SFACR[CAS] is set to 0. Say, if QSPI_SFACR[CAS] is 3 then bits 26-3 are sent to flash as it page address in case flash is operating in 24-bit mode. Total number of address bits request by flash as it page and column address must not be more than 32 bit. Refer to Table 36-13 for the mapping between the access mode and the QSPI_SFAR content and to Normal Mode for details about the command triggering and command execution. The software should ensure that the serial flash address provided in the QSPI_SFAR register lies in the valid flash address range as defined in Table 36-13.

Write:

- *QSPI_SR[IP_ACC] = 0*

Address: 400D_A000h base + 100h offset = 400D_A100h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	SFADR																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

QuadSPIx_SFAR field descriptions

Field	Description
SFADR	Serial Flash Address. The register content is used as byte address for all following IP Commands.

36.4.2.14 Serial Flash Address Configuration Register (QuadSPIx_SFACR)

This register contains the serial flash specific address requirements that must be configured according to the flash connected, for the controller to function properly. The module automatically translates the address QSPI_SFAR on the memory map or the incoming address on the AHB bus to the column address on the flash itself. Say, a flash needs 3 bits as its column address than only the lower 3 bits of QSPI_SFAR/AHB address are send to flash as its column address. The software should ensure that the serial flash address provided in the QSPI_SFAR register or the incoming AHB address lies in the valid flash address range.

Write:

- *QSPI_SR[IP_ACC] = 0*
- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 104h offset = 400D_A104h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved															WA
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved												CAS			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

QuadSPIx_SFACR field descriptions

Field	Description
31–17 Reserved	This field is reserved.
16 WA	Word Addressable Defines whether the serial flash is a byte addressable flash or a word addressable flash. According to this bit configuration the address is re-mapped to the flash interface. Refer to Address scheme for details. 0 Byte addressable serial flash mode. 1 Word (2 byte) addressable serial flash mode.
15–4 Reserved	This field is reserved.
CAS	Column Address Space Defines the width of the column address. If the coulmn address is say [2:0] of QSPI_SFAR/AHB address, then CAS must be 3. If there is no column address separation in any serial flash this bit must be programmed to 0.

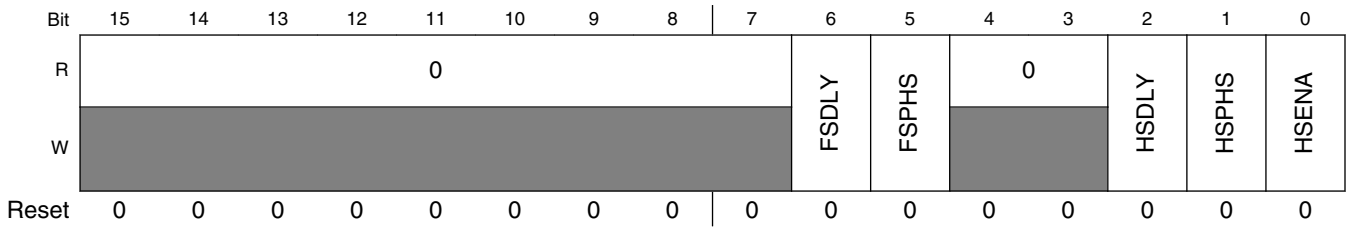
36.4.2.15 Sampling Register (QuadSPIx_SMPR)

The Sampling Register allows configuration of how the incoming data from the external serial flash devices are sampled in the QuadSPI module.

Write: Disabled Mode

Address: 400D_A000h base + 108h offset = 400D_A108h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0													DDRSMP		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



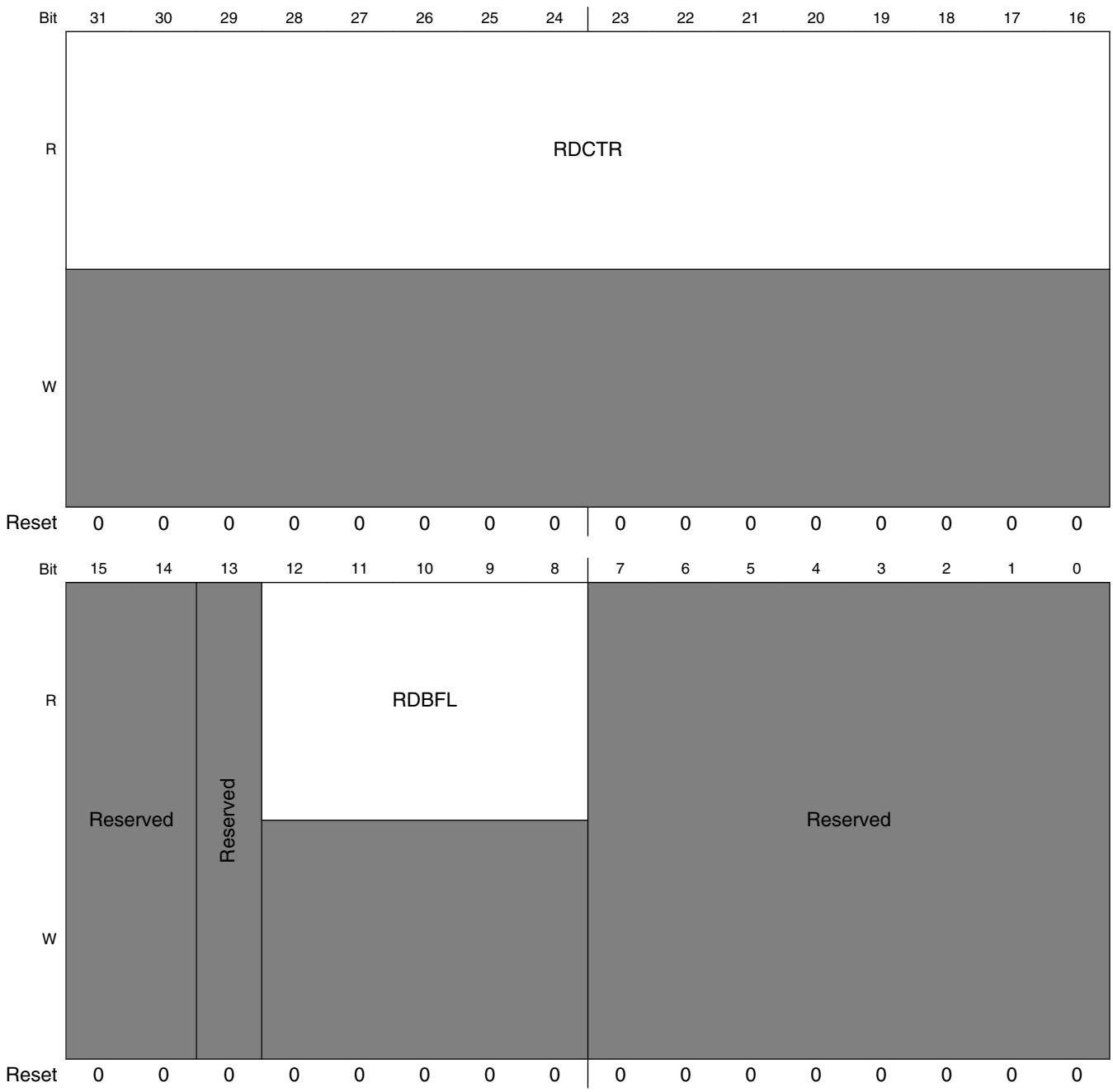
QuadSPIx_SMPR field descriptions

Field	Description
31–19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18–16 DDRSMP	DDR Sampling point Select the sampling point for incoming data when serial flash is executing a DDR instruction. Refer to Figure 36-13 for details on the sampling points.
15–7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 FSDLY	Full Speed Delay selection for SDR instructions. Select the delay with respect to the reference edge for the sample point valid for full speed commands. 0 One clock cycle delay 1 Two clock cycles delay. **NOTE:** This bit is also used in DQS mode and ignored when using non-DQS DDR instructions.
5 FSPHS	Full Speed Phase selection for SDR instructions. Select the edge of the sampling clock valid for full speed commands. 0 Select sampling at non-inverted clock 1 Select sampling at inverted clock. **NOTE:** This bit is also used in DQS mode and ignored when using non-DQS DDR instructions.
4–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 HSDLY	Half Speed Delay selection for SDR instructions. Only relevant when HSENA bit is set. Select the delay with respect to the reference edge for the sample point valid for half speed commands. 0 One clock cycle delay 1 Two clock cycle delay
1 HSPHS	Half Speed Phase selection for SDR instructions. Only relevant when HSENA bit is set. Select the delay with respect to the reference edge for the sample point valid for half speed commands. 0 Select sampling at non-inverted clock 1 Select sampling at inverted clock
0 HSENA	Half Speed serial flash clock Enable This bit enables the divide by 2 of the clock to the external serial flash device for all commands, only in SDR. Refer to Serial Flash Clock Frequency Limitations for details. 0 Disable divide by 2 of serial flash clock for half speed commands 1 Enable divide by 2 of serial flash clock for half speed commands

36.4.2.16 RX Buffer Status Register (QuadSPIx_RBSR)

This register contains information related to the receive data buffer.

Address: 400D_A000h base + 10Ch offset = 400D_A10Ch



QuadSPIx_RBSR field descriptions

Field	Description
31–16 RDCTR	Read Counter. Indicates how many entries of 4 bytes have been removed from the RX Buffer. For example, a value of 0x2 would indicate 8 bytes have been removed. It is incremented by the number (QSPI_RBCT[WMRK] + 1) on RX Buffer POP event. The RX Buffer can be popped using DMA or pop flag QSPI_FR[RBDF]. The QSPI_RSER[RBDDE] defines which pop has to be done. For further details, refer to AHB RX Data Buffer (QSPI_ARDB0 to QSPI_ARDB15) and "Data Transfer from the QuadSPI Module Internal Buffers" section in Flash Read.
15–14 Reserved	This field is reserved.
13 Reserved	This field is reserved.
12–8 RDBFL	RX Buffer Fill Level. Indicates how many entries of 4 bytes are still available in the RX Buffer.For example, a value of 0x2 would indicate 8bytes are available.
Reserved	This field is reserved.

36.4.2.17 RX Buffer Control Register (QuadSPIx_RBCT)

This register contains control data related to the receive data buffer.

Write:

- *QSPI_SR[IP_ACC] = 0*

Address: 400D_A000h base + 110h offset = 400D_A110h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved							RXBRD	Reserved			Reserved	WMRK			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

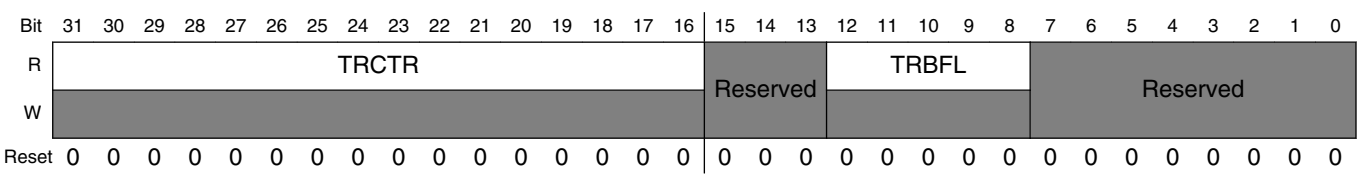
QuadSPIx_RBCT field descriptions

Field	Description
31–9 Reserved	This field is reserved.
8 RXBRD	RX Buffer Readout. This field specifies the access scheme for the RX Buffer readout. 0 RX Buffer content is read using the AHB Bus registers QSPI_ARDB0 to QSPI_ARDB15. For details, refer to Exclusive Access to Serial Flash for AHB Commands. 1 RX Buffer content is read using the IP Bus registers QSPI_RBDR0 to QSPI_RBDR15.
7–5 Reserved	This field is reserved.
4 Reserved	This field is reserved.
WMRK	RX Buffer Watermark. This field determines when the readout action of the RX Buffer is triggered. When the number of valid entries in the RX Buffer is equal to or greater than the number given by (WMRK+1) the QSPI_SR[RXWE] flag is asserted.The value should be entered as the number of 4-byte entries minus 1. For example, a value of 0x0 would set the watermark to 4 bytes, 1 to 8 bytes, 2 to 12 bytes, and so on. For details, refer to DMA Usage.

36.4.2.18 TX Buffer Status Register (QuadSPIx_TBSR)

This register contains information related to the transmit data buffer.

Address: 400D_A000h base + 150h offset = 400D_A150h



QuadSPIx_TBSR field descriptions

Field	Description
31–16 TRCTR	Transmit Counter. This field indicates how many entries of 4 bytes have been written into the TX Buffer by host accesses. It is reset to 0 when a 1 is written to QSPI_MCR[CLR_TXF]. It is incremented on each write access to the QSPI_TBDR register when another word has been pushed onto the TX Buffer. When it is not cleared the TRCTR field wraps around to 0. Refer to TX Buffer Data Register (QuadSPI_TBDR) for details.
15–13 Reserved	This field is reserved.
12–8 TRBFL	TX Buffer Fill Level. The TRBFL field contains the number of entries of 4 bytes each available in the TX Buffer for the QuadSPI module to transmit to the serial flash device.
Reserved	This field is reserved.

36.4.2.19 TX Buffer Data Register (QuadSPIx_TBDR)

The QSPI_TBDR register provides access to the circular TX Buffer of depth 64 bytes. This buffer provides the data written into it as write data for the page programming commands to the serial flash device. Refer to Table 36-22 for the byte ordering scheme. A write transaction on the flash with data size of less than 32 bits will lead to the removal of four data entry from the TX buffer. The valid bits will be used and the rest of the bits will be discarded.

Write:

- *QSPI_SR[TXFULL] = 0*

32-bit write access required

Address: 400D_A000h base + 154h offset = 400D_A154h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	TXDATA																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

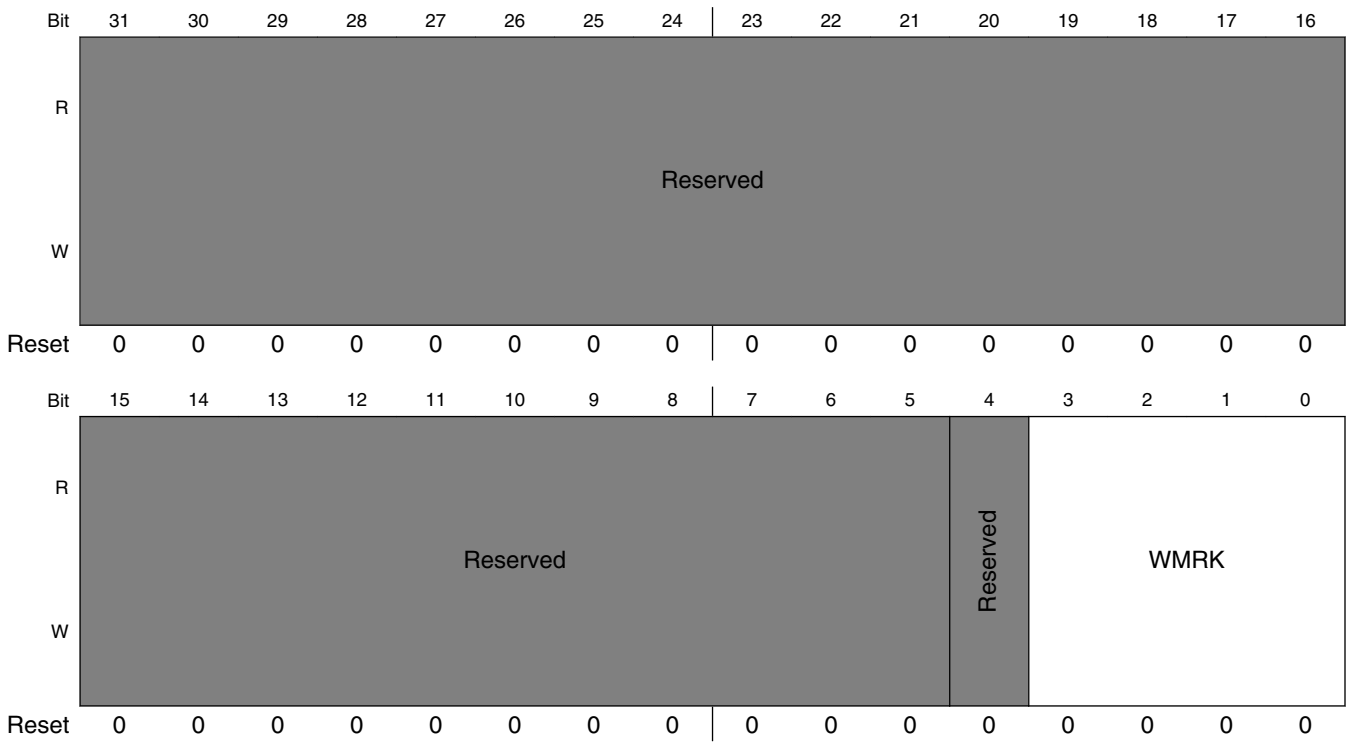
QuadSPIx_TBDR field descriptions

Field	Description
TXDATA	TX Data On write access the data is written into the next available entry of the TX Buffer and the QPSI_TBSR[TRBFL] field is updated accordingly. On a read access, the last data written to the register is returned.

36.4.2.20 Tx Buffer Control Register (QuadSPIx_TBCT)

This register contains control information for transmit data buffer.

Address: 400D_A000h base + 158h offset = 400D_A158h



QuadSPIx_TBCT field descriptions

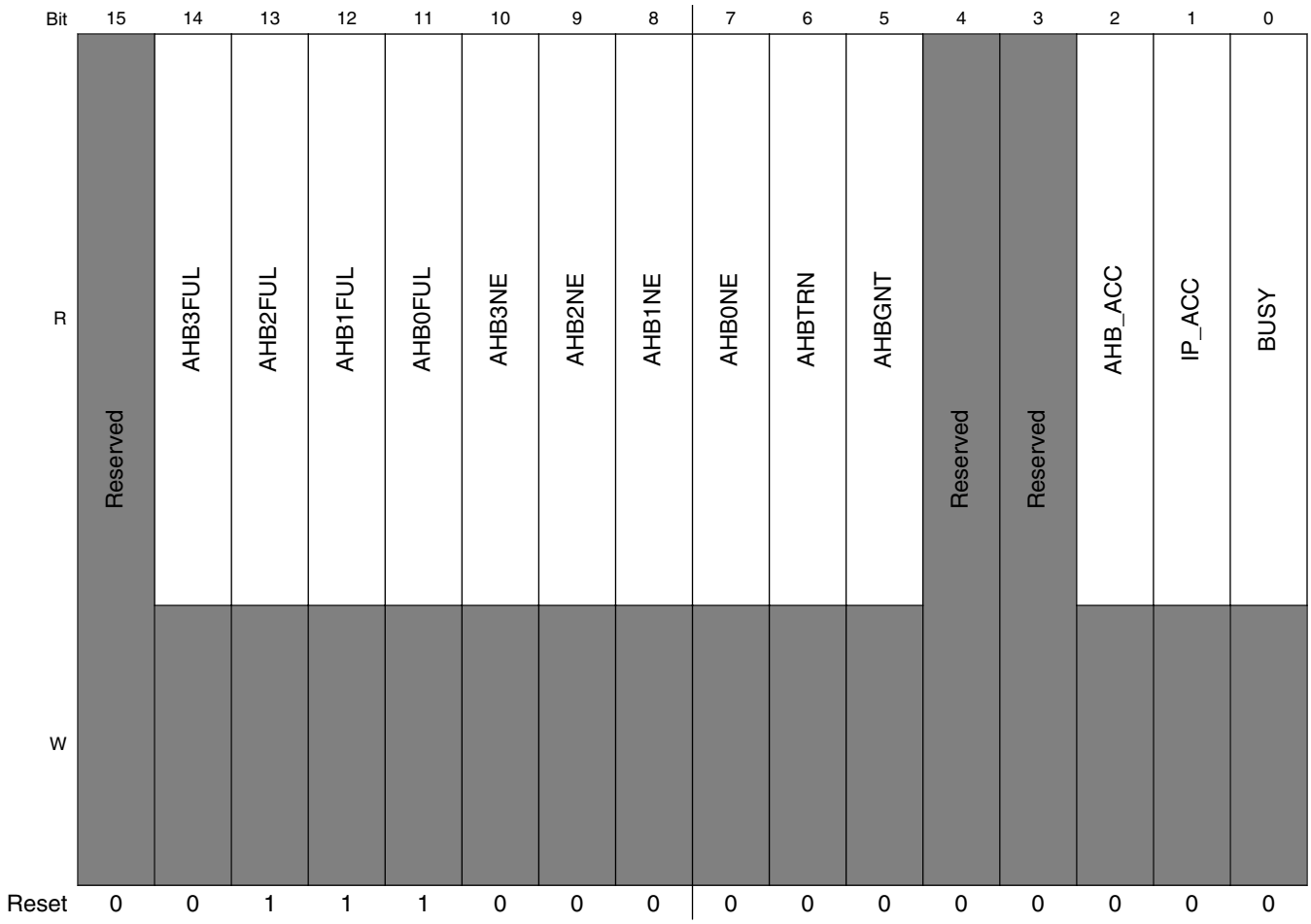
Field	Description
31–5 Reserved	This field is reserved.
4 Reserved	This field is reserved.
WMRK	Determines the watermark for the TX Buffer. When the number of available space in TX Buffer is greater than the number given by (WMRK+1), QSPI_SR[TXWA] is asserted. The values should be entered as the number of 4Bytes entries minus 1. For example, a value of 0x0 would set the watermark to 4 bytes, 1 to 8 bytes, 2 to 12 Bytes, and so on.For details, refer to DMA Usage.

36.4.2.21 Status Register (QuadSPIx_SR)

The QSPI_SR register provides all available status information about SFM command execution and arbitration, the RX Buffer, TX Buffer, and the AHB Buffer.

Address: 400D_A000h base + 15Ch offset = 400D_A15Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DLPSMP			Reserved	TXFULL	TXDMA	TXWA	TXEDA	RXDMA	Reserved			RXFULL	Reserved		RXWE
W																
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0



QuadSPIx_SR field descriptions

Field	Description
31–29 DLPSMP	Data learning pattern sampling point. The sampling point found by the controller with the data learning pattern. • This is used for DDR only. • If the learning fails, this field will return garbage and DLPFF bit will be set. • In case of Data learning with DQS this field will return the reset value as sampling point match is not found in case of DQS. For details, refer to Data Learning.
28 Reserved	This field is reserved.
27 TXFULL	TX Buffer Full. Asserted when no more data can be stored.
26 TXDMA	TXDMA Asserted when TXFIFO fill via DMA is active i.e. DMA is requested or running
25 TXWA	TX Buffer watermark Available Asserted when the number of available spaces in TX buffer is greater than or equal to the value give by QSPI_TBCT[WMRK].

Table continues on the next page...

QuadSPIx_SR field descriptions (continued)

Field	Description
24 TXEDA	Tx Buffer Enough Data Available Asserted when TX Buffer contains enough data for any pop operation to take place. There must be at least 128 bit data available in TX FIFO for any pop operation; otherwise, QSPI_FR[TBUF] will be set.
23 RXDMA	RX Buffer DMA. Asserted when RX Buffer read out via DMA is active i.e DMA is requested or running.
22–20 Reserved	This field is reserved.
19 RXFULL	RX Buffer Full. Asserted when the RX Buffer is full, i.e. that QSPI_RBSR[RDBFL] field is equal to 32.
18–17 Reserved	This field is reserved.
16 RXWE	RX Buffer Watermark Exceeded. Asserted when the number of valid entries in the RX Buffer exceeds the number given in the QSPI_RBCT[WMRK] field.
15 Reserved	This field is reserved.
14 AHB3FUL	AHB 3 Buffer Full. Asserted when AHB 3 buffer is full.
13 AHB2FUL	AHB 2 Buffer Full. Asserted when AHB 2 buffer is full.
12 AHB1FUL	AHB 1 Buffer Full. Asserted when AHB 1 buffer is full.
11 AHB0FUL	AHB 0 Buffer Full. Asserted when AHB 0 buffer is full.
10 AHB3NE	AHB 3 Buffer Not Empty. Asserted when AHB 3 buffer contains data.
9 AHB2NE	AHB 2 Buffer Not Empty. Asserted when AHB 2 buffer contains data.
8 AHB1NE	AHB 1 Buffer Not Empty. Asserted when AHB 1 buffer contains data.
7 AHB0NE	AHB 0 Buffer Not Empty. Asserted when AHB 0 buffer contains data.
6 AHBTRN	AHB Access Transaction pending. Asserted when there is a pending request on the AHB interface. Refer to the AMBA specification for details.
5 AHBGNT	AHB Command priority Granted: Asserted when another module has been granted priority of AHB Commands against IP Commands. For details refer to Command Arbitration.
4 Reserved	This field is reserved.
3 RESERVED	This field is reserved.
2 AHB_ACC	AHB Access. Asserted when the transaction currently executed was initiated by AHB bus.
1 IP_ACC	IP Access. Asserted when transaction currently executed was initiated by IP bus.
0 BUSY	Module Busy. Asserted when module is currently busy handling a transaction to an external flash device.

36.4.2.22 Flag Register (QuadSPIx_FR)

The QSPI_FR register provides all available flags about SFM command execution and arbitration which may serve as source for the generation of interrupt service requests. Note that the error flags in this register do not relate directly to the execution of the transaction in the serial flash device itself but only to the behavior and conditions visible in the QuadSPI module.

Write: Enabled Mode

Address: 400D_A000h base + 160h offset = 400D_A160h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DLPFF	Reserved		Reserved	TBFF	TBUF	Reserved		ILLINE	Reserved					RBOF	RBDF
W	w1c				w1c	w1c			w1c						w1c	w1c
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ABSEF	AITEF	AIBSEF	ABOF	IUEF	Reserved			IPAEF	IPIEF	Reserved	IPGEF	Reserved			TFF
W	w1c	w1c	w1c	w1c	w1c				w1c	w1c		w1c				w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

QuadSPIx_FR field descriptions

Field	Description
31 DLPFF	Data Learning Pattern Failure Flag. Set when DATA_LEARN instruction was encountered in a sequence but no sampling point was found for the data learning patternin case only 8 bit data learning is requested for non DQS mode. The controller automatically starts sampling using the value in QSPI_SMPR[DDRSMP].If more than 8 bits data learning are requested with QSPI_MCR[DQS_EN] set to 0, and the sampling point found after first 8 bit match doesn't remain the same for the whole instruction duration, this flag is set. In case of Data learn with DQS this flag is set whenever the incoming data from flash on DQS edges doesn't match the pattern in QSPI_DLPR. For details, refer to Data Learning.
30–29 RESERVED	This field is reserved.
28 Reserved	This field is reserved.
27 TBFF	TX Buffer Fill Flag. Before writing to the TX buffer, this bit should be cleared. Then this bit has to be read back. If the bit is set, the TX Buffer can take more data. If the bit remains cleared, the TX buffer is full. Refer to Tx Buffer Operation for details.
26 TBUF	TX Buffer Underrun Flag. Set when the module tried to pull data although TX Buffer was emptyor the buffer contains less than 128 bits of data. The application must ensure that the buffer never goes empty during a transaction except for the last data fetch. The IP Command leading to the TX Buffer underrun is continued (data sent to the serial flash device is all F in case of valid TX underrun. The application must clear the TX Buffer in response to this event by writing a 1 to the QSPI_MCR[CLR_TXF] bit.
25–24 Reserved	This field is reserved.
23 ILLINE	Illegal Instruction Error Flag. Set when an illegal instruction is encountered by the controller in any of the sequences. Refer to Table 36-20 for a list of legal instructions.
22–18 Reserved	This field is reserved.
17 RBOF	RX Buffer Overflow Flag. Set when not all the data read from the serial flash device could be pushed into the RX Buffer.

Table continues on the next page...

QuadSPIx_FR field descriptions (continued)

Field	Description
	The IP Command leading to this condition is continued until the number of bytes according to the QSPI_IPCR[IDATSZ] field has been read from the serial flash device. The content of the RX Buffer is not changed.
16 RBDF	RX Buffer Drain Flag. Will be set if the QuadSPI_SR[RXWE] status bit is asserted. Writing 1 into this bit triggers one of the following actions: • If the RX Buffer has up to QuadSPI_RBCT[WMRK] valid entries then the flag is cleared. • If the RX Buffer has more than QuadSPI_RBCT[WMRK] valid entries and the QuadSPI_RSER[RBDDE] bit is not set (flag driven mode) a RX Buffer POP event is triggered. The flag remains set if the RX Buffer contains more than QuadSPI_RBCT[WMRK] valid entries after the RX Buffer POP event is finished. The flag is cleared if the RX Buffer contains less than or equal to QuadSPI_RBCT[WMRK] valid entries after the RX Buffer POP event is finished. Refer to "Receive Buffer Drain Interrupt or DMA Request" section in Normal Mode Interrupt and DMA Requests, for details.
15 ABSEF	AHB Sequence Error Flag. Set when the execution of an AHB Command is started with a WRITE or WRITE_DDR Command in the sequence pointed to by the QSPI_BUFxCR register. (QSPI_BUFxCR implies any one of QSPI_BUF0CR/QSPI_BUF1CR/QSPI_BUF2CR/QSPI_BUF3CR.) Communication with the serial flash device is terminated before the execution of WRITE/WRITE_DDR command by the QuadSPI module. The AHB bus request which triggered this command is answered with an ERROR response.
14 AITEF	AHB Illegal transaction error flag. Set whenever there is no response generated from QSPI to AHB bus in case of illegal transaction and the watchdog timer expires.The timer value is taken as parameter.
13 AIBSEF	AHB Illegal Burst Size Error Flag. Set whenever the total burst size (size x beat) of an AHB transaction is greater than the prefetch data size. The prefecth data size is defined by QSPI_BUFxCR[ADATSZ] or data size mentioned in the sequence pointed to by the SEQID field in case ADATSZ = 0. Refer to HBURST Support for more details on HBURST feature.
12 ABOF	AHB Buffer Overflow Flag. Set when the size of the AHB access exceeds the size of the AHB buffer. This condition can occur only if the QSPI_BUFxCR[ADATSZ] field is programmed incorrectly. The AHB Command leading to this condition is continued until the number of entries according to the QSPI_BUFxCR[ADATSZ] field has been read from the serial flash device. The content of the AHB Buffer is not changed.
11 IUEF	IP Command Usage Error Flag. Set when in parallel flash mode the execution of an IP Command is started with more than one pad enabled and the sequence pointed to by the sequence ID contains a WRITE or a WRITE_DDR command. Refer to Table 36-20 table for the related commands. Communication with the serial flash device is terminated before the execution of WRITE/WRITE_DDR command by the QuadSPI module.
10–8 Reserved	This field is reserved.
7 IPAEF	IP Command Trigger during AHB Access Error Flag. Set when the following condition occurs: • A write access occurs to the QSPI_IPCR[SEQID] field and the QSPI_SR[AHB_ACC] bit is set. Any command leading to the assertion of the IPAEF flag is ignored.
6 IPIEF	IP Command Trigger could not be executed Error Flag. Set when the QSPI_SR[IP_ACC] bit is set (i.e. an IP triggered command is currently executing) and any of the following conditions occurs: • Write access to the QSPI_IPCR register. Any command leading to the assertion of the IPIEF flag is ignored

Table continues on the next page...

QuadSPIx_FR field descriptions (continued)

Field	Description
	• Write access to the QSPI_SFAR register. • Write access to the QSPI_RBCT register.
5 Reserved	This field is reserved.
4 IPGEF	IP Command Trigger during AHB Grant Error Flag. Set when the following condition occurs: • A write access occurs to the QSPI_IPCR[SEQID] field and the QSPI_SR[AHBGNT] bit is set. Any command leading to the assertion of the IPGEF flag is ignored.
3–1 Reserved	This field is reserved.
0 TFF	IP Command Transaction Finished Flag. Set when the QuadSPI module has finished a running IP Command. If an error occurred the related error flags are valid, at the latest, in the same clock cycle when the TFF flag is asserted.

36.4.2.23 Interrupt and DMA Request Select and Enable Register (QuadSPIx_RSER)

The QuadSPI_RSER register provides enables and selectors for the interrupts in the QuadSPI module.

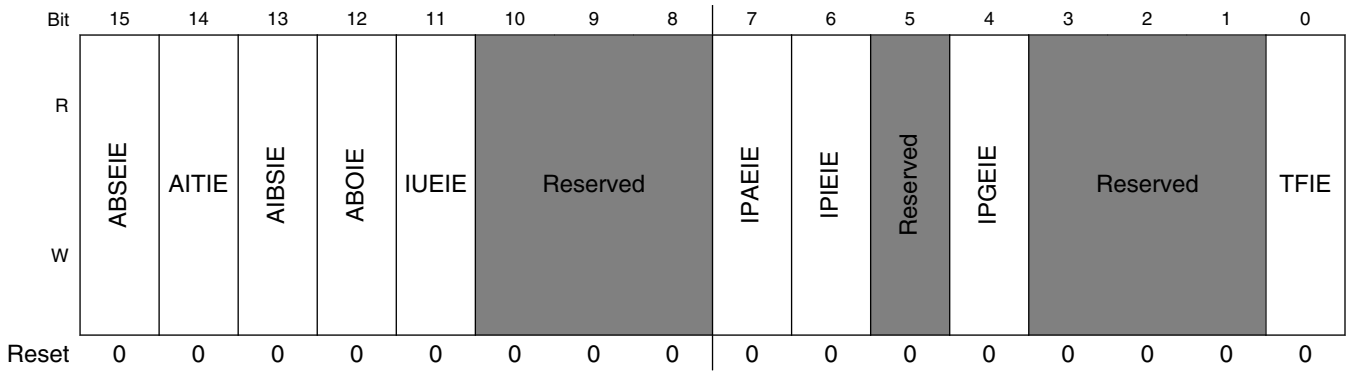
NOTE

Each flag of the QuadSPI_FR register enabled as source for an interrupt prevents the QuadSPI module from entering Stop Mode or Module Disable Mode when this flag is set.

Write: Anytime

Address: 400D_A000h base + 164h offset = 400D_A164h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	DLPFIE	Reserved		Reserved	TBFIE	TBUIE	TBFDE	Reserved	ILLINIE	Reserved	RBDDE	Reserved			RBOIE	RBDIE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



QuadSPIx_RSER field descriptions

Field	Description
31 DLPFIE	Data Learning Pattern Failure Interrupt enable . Triggered by DLPFF flag in QSPI_FR register 0 No DLPFF interrupt will be generated 1 DLPFF interrupt will be generated
30–29 Reserved	This field is reserved.
28 RESERVED	This field is reserved.
27 TBFIE	TX Buffer Fill Interrupt Enable 0 No TBFF interrupt will be generated 1 TBFF interrupt will be generated
26 TBUIE	TX Buffer Underrun Interrupt Enable 0 No TBUF interrupt will be generated 1 TBUF interrupt will be generated
25 TBFDE	TX Buffer Fill DMA Enable Enables generation of DMA requests for TX Buffer fill. When this is set DMA requests are generated as long as the QSPI_SR[TXWA] status bit is set. 0 No DMA request will be generated 1 DMA request will be generated
24 Reserved	This field is reserved.
23 ILLINIE	Illegal Instruction Error Interrupt Enable. Triggered by ILLINE flag in QSPI_FR 0 No ILLINE interrupt will be generated 1 ILLINE interrupt will be generated
22 Reserved	This field is reserved.
21 RBDDE	RX Buffer Drain DMA Enable: Enables generation of DMA requests for RX Buffer Drain. When this bit is set DMA requests are generated as long as the QSPI_SR[RXWE] status bit is set. 0 No DMA request will be generated 1 DMA request will be generated

Table continues on the next page...

QuadSPIx_RSER field descriptions (continued)

Field	Description
20–18 Reserved	This field is reserved.
17 RBOIE	RX Buffer Overflow Interrupt Enable 0 No RBOF interrupt will be generated 1 RBOF interrupt will be generated
16 RBDIE	RX Buffer Drain Interrupt Enable: Enables generation of IRQ requests for RX Buffer Drain. When this bit is set the interrupt is asserted as long as the QuadSPI_SR[RBDF] flag is set. 0 No RBDF interrupt will be generated 1 RBDF Interrupt will be generated
15 ABSEIE	AHB Sequence Error Interrupt Enable: Triggered by ABSEF flags of QSPI_FR 0 No ABSEF interrupt will be generated 1 ABSEF interrupt will be generated
14 AITIE	AHB Illegal transaction interrupt enable. 0 No AITEF interrupt will be generated 1 AITEF interrupt will be generated
13 AIBSIE	AHB Illegal Burst Size Interrupt Enable 0 No AIBSEF interrupt will be generated 1 AIBSEF interrupt will be generated
12 ABOIE	AHB Buffer Overflow Interrupt Enable 0 No ABOF interrupt will be generated 1 ABOF interrupt will be generated
11 IUEIE	IP Command Usage Error Interrupt Enable 0 No IUEF interrupt will be generated 1 IUEF interrupt will be generated
10–8 Reserved	This field is reserved.
7 IPAEIE	IP Command Trigger during AHB Access Error Interrupt Enable 0 No IPAEF interrupt will be generated 1 IPAEF interrupt will be generated
6 IPIEIE	IP Command Trigger during IP Access Error Interrupt Enable 0 No IPIEF interrupt will be generated 1 IPIEF interrupt will be generated
5 Reserved	This field is reserved.
4 IPGEIE	IP Command Trigger during AHB Grant Error Interrupt Enable 0 No IPGEF interrupt will be generated 1 IPGEF interrupt will be generated
3–1 Reserved	This field is reserved. Reserved.

Table continues on the next page...

QuadSPIx_RSER field descriptions (continued)

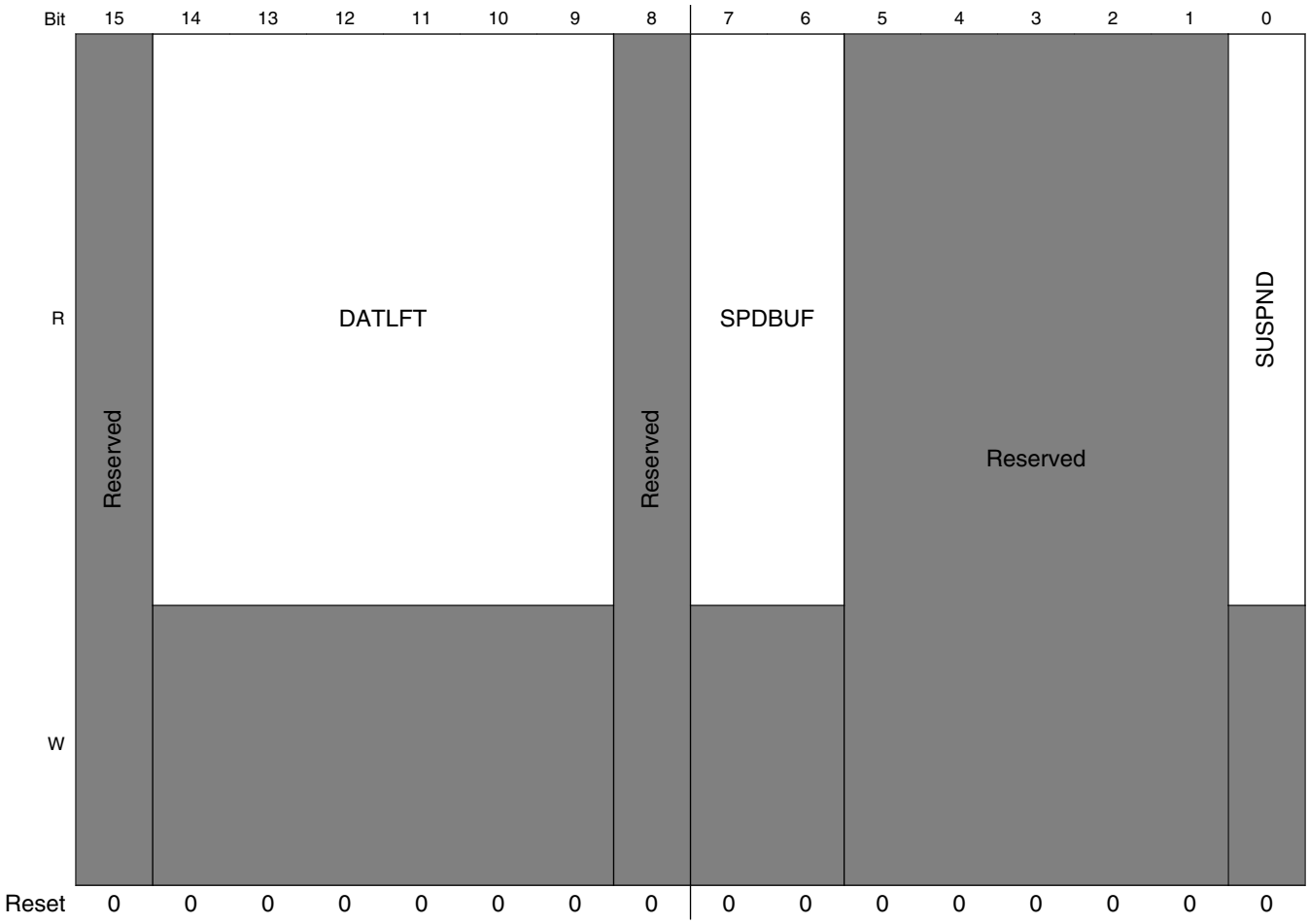
Field	Description
0 TFIE	Transaction Finished Interrupt Enable 0 No TFF interrupt will be generated 1 TFF interrupt will be generated

36.4.2.24 Sequence Suspend Status Register (QuadSPIx_SPNDST)

The sequence suspend status register provides information specific to any suspended sequence. An AHB sequence may be suspended when a high priority AHB master makes an access before the AHB sequence completes the data transfer requested.

Address: 400D_A000h base + 168h offset = 400D_A168h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



QuadSPIx_SPNDST field descriptions

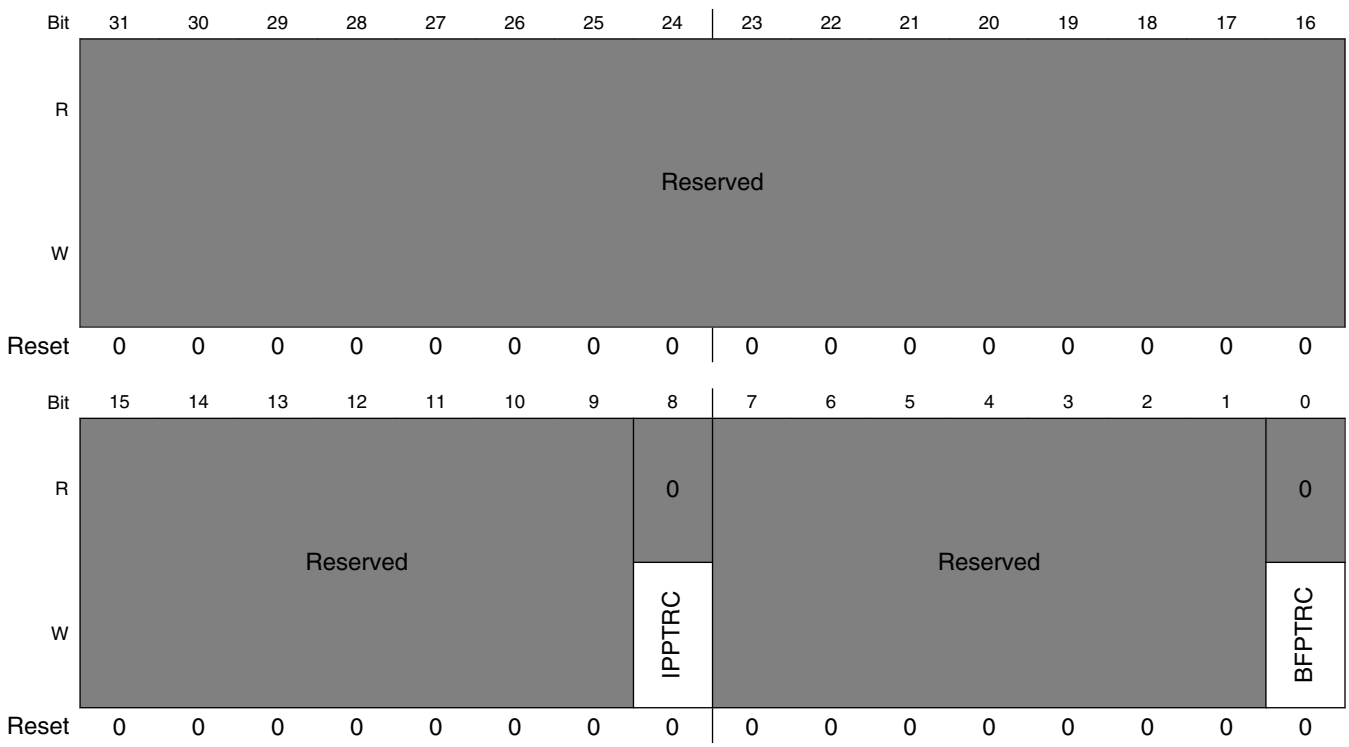
Field	Description
31–16 Reserved	This field is reserved.
15 Reserved	This field is reserved.
14–9 DATLFT	Data left: Provides information about the amount of data left to be read in the suspended sequence. Valid only when SUSPND is set to 1'b1. Value in terms of 64 bits or 8 bytes
8 Reserved	This field is reserved.
7–6 SPDBUF	Suspended Buffer: Provides the suspended buffer number. Valid only when SUSPND is set to 1'b1
5–1 Reserved	This field is reserved.
0 SUSPND	When set, it signifies that a sequence is in suspended state

36.4.2.25 Sequence Pointer Clear Register (QuadSPIx_SPTRCLR)

The sequence pointer clear register provides bits to reset the IP and Buffer sequence pointers. The sequence pointer contains the index of which instruction within the LUT entry is to be executed next. For example, if the LUT entry ends on a JMP_ON_CS value of 2, the index will be stored as 2.

The software should reset the sequence pointers whenever the sequence ID is changed by updating the SEQID field in QSPI_IPCR or QSPI_BFGENCR.

Address: 400D_A000h base + 16Ch offset = 400D_A16Ch



QuadSPIx_SPTRCLR field descriptions

Field	Description
31–9 Reserved	This field is reserved.
8 IPPTRC	IP Pointer Clear: 1: Clears the sequence pointer for IP accesses as defined in QuadSPI_IPCR This is a self-clearing field.
7–1 Reserved	This field is reserved. Reserved.
0 BFPTRC	Buffer Pointer Clear: 1: Clears the sequence pointer for AHB accesses as defined in QuadSPI_BFGENCR. This is a self-clearing field.

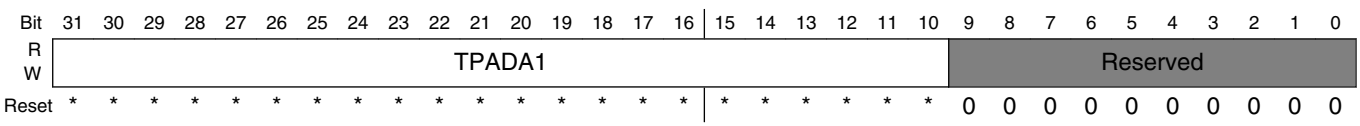
36.4.2.26 Serial Flash A1 Top Address (QuadSPIx_SFA1AD)

The QSPI_SFA1AD register provides the address mapping for the serial flash A1.The difference between QSPI_SFA1AD[TPADA1] and QSPI_AMBA_BASE defines the size of the memory map for serial flash A1.

Write:

- *QSPI_SR[IP_ACC] = 0*
- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 180h offset = 400D_A180h



* Notes:

- TPADA1 field: See the module configuration for the device specific reset values.

QuadSPIx_SFA1AD field descriptions

Field	Description
31–10 TPADA1	Top address for Serial Flash A1. In effect, TPADxx is the first location of the next memory.
Reserved	This field is reserved.

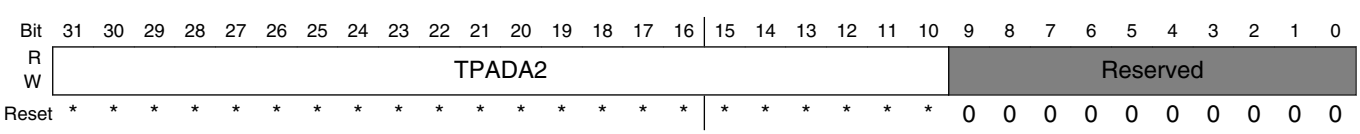
36.4.2.27 Serial Flash A2 Top Address (QuadSPIx_SFA2AD)

The QSPI_SFA2AD register provides the address mapping for the serial flash A2.The difference between QSPI_SFA2AD[TPADA2] and QSPI_SFA1AD[TPADA1] defines the size of the memory map for serial flash A2.

Write:

- *QSPI_SR[IP_ACC] = 0*
- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 184h offset = 400D_A184h



* Notes:

- TPADA2 field: See the module configuration for the device specific reset values.

QuadSPIx_SFA2AD field descriptions

Field	Description
31–10 TPADA2	Top address for Serial Flash A2. In effect, TPxxAD is the first location of the next memory.
Reserved	This field is reserved.

36.4.2.28 Serial Flash B1Top Address (QuadSPIx_SFB1AD)

The QSPI_SFB1AD register provides the address mapping for the serial flash B1.The difference between QSPI_SFB1AD[TPADB1] and QSPI_SFA2AD[TPADA2] defines the size of the memory map for serial flash B1.

Write:

- *QSPI_SR[IP_ACC] = 0*
- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 188h offset = 400D_A188h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	TPADB1																						Reserved									
Reset	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	0	0	0	0	0	0	0	0	0

* Notes:

- TPADB1 field: See the module configuration for the device specific reset values.

QuadSPIx_SFB1AD field descriptions

Field	Description
31–10 TPADB1	Top address for Serial Flash B1.In effect, TPxxAD is the first location of the next memory.
Reserved	This field is reserved.

36.4.2.29 Serial Flash B2Top Address (QuadSPIx_SFB2AD)

The QSPI_SFB2AD register provides the address mapping for the serial flash B2.The difference between QSPI_SFB2AD[TPADB2] and QSPI_SFB1AD[TPADB1] defines the size of the memory map for serial flash B2.

Write:

- *QSPI_SR[IP_ACC] = 0*
- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 18Ch offset = 400D_A18Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	TPADB2																						Reserved									
Reset	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	0	0	0	0	0	0	0	0	0

* Notes:
- TPADB2 field: See the module configuration for the device specific reset values.

QuadSPIx_SFB2AD field descriptions

Field	Description
31–10 TPADB2	Top address for Serial Flash B2. In effect, TPxxAD is the first location of the next memory.
Reserved	This field is reserved.

36.4.2.30 Data Learn Pattern Register (QuadSPIx_DLPR)

The QSPI_DLPR register contains the information of the data to be used for Data Learning.

Write:
- *QSPI_SR[IP_ACC] = 0*
- *QSPI_SR[AHB_ACC] = 0*

Address: 400D_A000h base + 190h offset = 400D_A190h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	DLPV																															
Reset	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	0	1	1	0	1	0	0	0	1	0	0	0	0	1	1

QuadSPIx_DLPR field descriptions

Field	Description
DLPV	Data Learning Pattern Value: This value is used for data learning in DDR and DQS mode. If programmer wants to do data learn for more than 32 bit than the same value in the register is repeated. Say if 64 bit data learning is requested by any flash and the value of DLPR is aa55_3443 then the 64 bit value will be aa55_3443_aa55_3443. If 8 bit data learning was enabled by programming in seq_operand fields of DATA_LEARN instruction to 1 , the bits [7:0] are used as data_learning pattern. For details, refer to Data Learning

36.4.2.31 RX Buffer Data Register (QuadSPIx_RBDR)

The QuadSPI_RBDR registers provide access to the individual entries in the RX Buffer. Refer to Table 36-22 for the byte ordering scheme.

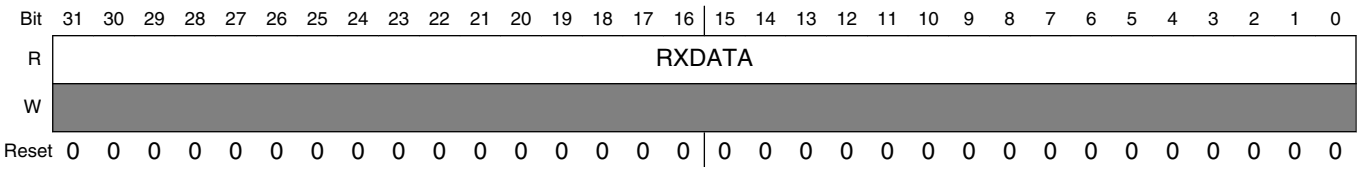
QuadSPI_RBDR0 corresponds to the actual position of the read pointer within the RX Buffer. The number of valid entries available depends from the number of RX Buffer entries implemented and from the number of valid buffer entries available in the RX Buffer.

Example 1, RX Buffer filled completely with 16 words: In this case the address range for valid read access extends from QuadSPI_RBDR0 to QuadSPI_RBDR15.

Example 2, RX Buffer filled with 5 valid words: RX Buffer fill level QuadSPI_RBSR[RDBFL] is 5. In this case an access to QuadSPI_RBDR4 provides the last valid entry.

Any access beyond the range of valid RX Buffer entries provides undefined results.

Address: 400D_A000h base + 200h offset + (4d × i), where i=0d to 15d



QuadSPIx_RBDR*n* field descriptions

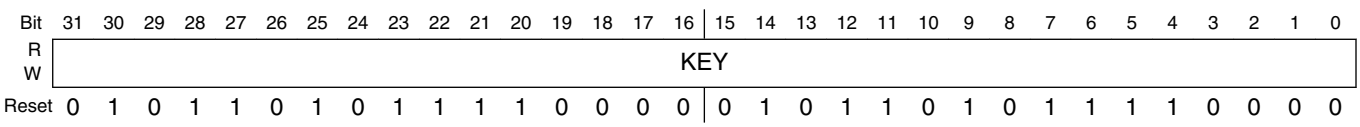
Field	Description
RXDATA	RX Data. The RXDATA field contains the data associated with the related RX Buffer entry. Data format and byte ordering is given in Byte Ordering of Serial Flash Read Data .

36.4.2.32 LUT Key Register (QuadSPIx_LUTKEY)

The LUT Key register contains the key to lock and unlock the Look-up-table. Refer to Look-up Table for details.

Write: Anytime

Address: 400D_A000h base + 300h offset = 400D_A300h



QuadSPIx_LUTKEY field descriptions

Field	Description
KEY	The key to lock or unlock the LUT. The KEY is 0x5AF05AF0. The read value is always 0x5AF05AF0

36.4.2.33 LUT Lock Configuration Register (QuadSPIx_LCKCR)

The LUT lock configuration register is used along with QSPI_LUTKEY register to lock or unlock the LUT. This register has to be written immediately after QSPI_LUTKEY register for the lock or unlock operation to be successful. Refer to Look-up Table for details. Setting both the LOCK and UNLOCK bits as "00" or "11" is not allowed.

Write: Just after writing the LUT Key Register

(QSPI_LUTKEY)

Address: 400D_A000h base + 304h offset = 400D_A304h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved														UNLOCK	LOCK
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

QuadSPIx_LCKCR field descriptions

Field	Description
31–2 Reserved	This field is reserved.
1 UNLOCK	Unlocks the LUT when the following two conditions are met: 1. This register is written just after the LUT Key Register (QuadSPI_LUTKEY) 2. The LUT key register was written with 0x5AF05AF0 key
0 LOCK	Locks the LUT when the following condition is met: 1. This register is written just after the LUT Key Register (QuadSPI_LUTKEY) 2. The LUT key register was written with 0x5AF05AF0 key

36.4.2.34 Look-up Table register (QuadSPIx_LUT*n*)

The LUT registers are a look-up-table for sequences of instructions. The programmable sequence engine executes the instructions in these sequences to generate a valid serial flash transaction. There are a total of 64 LUT registers. These 64 registers are divided into groups of 4 registers that make a valid sequence. Therefore, QSPI_LUT[0], QSPI_LUT[4], QSPI_LUT[8] ..... QSPI_LUT[60] are the starting registers of a valid sequence. Each of these sets of 4 registers can have a maximum of 8 instructions. Reset value of the register shown below is only applicable to LUT2 to LUT63. A maximum of 16 sequences can be defined at one time. Look-up Table describes the LUT registers in detail.

NOTE

The reset values for LUT0 and LUT1 are 0818_0403h and 2400_1C08h, respectively.

Write: Once the LUT is unlocked

Address: 400D_A000h base + 310h offset + (4d × i), where i=0d to 63d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	INSTR1						PAD1		OPRND1							
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	INSTR0						PAD0		OPRND0							
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- The reset values for LUT0 and LUT1 are 0818_0403h and 2400_1C08h respectively.

QuadSPIx_LUT*n* field descriptions

Field	Description
31–26 INSTR1	Instruction 1
25–24 PAD1	Pad information for INSTR1. 00 1 Pad 01 2 Pads 10 4 Pads 11 8 Pads
23–16 OPRND1	Operand for INSTR1.
15–10 INSTR0	Instruction 0

Table continues on the next page...

QuadSPIx_LUT*n* field descriptions (continued)

Field	Description
9–8 PAD0	Pad information for INSTR0. 00 1 Pad 01 2 Pads 10 4 Pads 11 8 Pads
OPRND0	Operand for INSTR0.

36.4.3 Serial Flash Address Assignment

The serial flash address assignment may be modified by writing into Serial Flash A1 Top Address (QuadSPI_SFA1AD) and Serial Flash A2 Top Address (QuadSPI_SFA2AD) for device A and into Serial Flash B1Top Address (QuadSPI_SFB1AD) and Serial Flash B2Top Address (QuadSPI_SFB2AD) for device B. The following table shows how different access modes are related to the address specified for the next SFM Command. Note that this address assignment is valid for both IP and AHB commands.

Table 36-13. Serial Flash Address Assignment

Parameter	Function	Access Mode
QSPI_AMBA_BASE ((31:10) - 22 bits)	QuadSPI AHB base address	
TOP_ADDR_MEMA1(TPADA1)	Top address for the external flash A1 (first device of the dual die flash A, or the first of the two independent flashes sharing the IOFA)	Any access to the address space between TOP_ADDR_MEMA1 and QSPI_AMBA_BASE will be routed to **Serial Flash A1**
TOP_ADDR_MEMA2(TPADA2)	Top address for the external flash A2 (second device of the dual die flash A, or the second of the two independent flashes sharing the IOFA).	Any access to the address space between TOP_ADDR_MEMA2 and TOP_ADDR_MEMA1 will be routed to **Serial Flash A2**
TOP_ADDR_MEMB1(TPADB1)	Top address for the external flash B1 (first device of the dual die flash B, or the first of the two independent flashes sharing the IOFB)	Any access to the address space between TOP_ADDR_MEMB1 and TOP_ADDR_MEMA2 will be routed to **Serial Flash B1**
TOP_ADDR_MEMB2(TPADB2)	Top address for the external flash B2 (second device of the dual die flash B or the second of the two independent flashes sharing the IOFB)	Any access to the address space between TOP_ADDR_MEMB2 and TOP_ADDR_MEMB1 will be routed to **Serial Flash A2**

36.4.4 AMBA Bus Register Memory Map

QSPI_AMBA_BASE defines the address to be used as start address of the serial flash device as defined by the system memory map..

Table 36-14. QuadSPI AMBA Bus Memory Map

Address	Register Name
Memory Mapped Serial Flash Data - Individual Flash Mode on Flash A	
QSPI_AMBA_BASE to (TOP_ADDR_MEMA2 - 0x01)	Memory Mapped Serial Flash Data - Individual Flash Mode on Flash A Refer to Memory Mapped Serial Flash Data - Individual Flash Mode on Flash A for details and to Table 36-22 and Table 36-27 for information about the byte ordering.
Memory Mapped Serial Flash Data - Individual Flash Mode on Flash B	
TOP_ADDR_MEMA2 to (TOP_ADDR_MEMB2 - 0x01)	Memory Mapped Serial Flash Data - Individual Flash Mode on Flash B Refer to Memory Mapped Serial Flash Data - Individual Flash Mode on Flash B for details and to Table 36-22 and Table 36-27 for information about the byte ordering.
Parallel Flash Mode	
QSPI_AMBA_BASE to (TOP_ADDR_MEMB2 - 0x01)	Parallel Flash Mode Refer to Parallel Flash Mode for details and to Table 36-26 and Table 36-27 for information about the byte ordering.
AHB RX Data Buffer (QSPI_ARDB0 to QSPI_ARDB15)	
QSPI_ARDB_BASE to… (32 * 4 Byte) QSPI_ARDB_BASE + 0x0000_01FF	AHB RX Data Buffer (QSPI_ARDB0 to QSPI_ARDB15) Refer to Table 36-22 and Table 36-24 for information about the byte ordering.

Note

Any read access to non-implemented addresses will provide undefined results.

In case single die flash devices, TOP_ADDR_MEMA2 and TOP_ADDR_MEMB2 should be initialized/programmed to TOP_ADDR_MEMA1 and TOP_ADDR_MEMB1 respectively- in effect, setting the size of these devices to 0. This would ensure that the complete memory map is assigned to only one flash device.

Parallel Flash Mode is valid only for commands related to data read and data write in single io mode from the serial flash. The first device of flash A has to be paired with the first device of flash B and the second device of flash A has to be paired with the second device of flash B in parallel mode. Parallel mode is selected via the QSPI_BFGENCR[PAR_EN] bit for all masters in AHB driven mode and via the QSPI_IPCR[PAR_EN] in IP driven mode. In parallel mode, the incoming address (SFAR

address in case of IP initiated transactions and the incoming AHB address in case of AHB initiated transactions) is divided by 2 and sent to the two flashes connected in parallel.

Any IP Command other than data read and write (through one pad) in Parallel Flash Mode will result in the assertion of the QSPI_FR[IUEF] flag and any AHB Command other than data read in Parallel Flash Mode will result in the assertion of the QSPI_FR[ABSEF] flag.

In the Individual Flash Modes, the 3/4 address bytes (as programmed in the instruction/operand in the sequence) available for the flash address is determined by SFADR [23:0] or SFADR [31:0]as given in the table above.

In Parallel Flash Mode, both flashes are read with the same starting address of 3/4 (as programmed in the instruction/operand in the sequence) bytes in size. This address is derived from SFADR [24:1] or SFADR [31:1] as given in the table above. The LSB of the SFADR field is used to select the appropriate bits of both flash devices to combine the byte corresponding to the selected address.

36.4.5 AHB Bus Register Memory Map Descriptions

This chapter contains definitions of registers in the AMBA address space.

36.4.5.1 AHB Bus Access Considerations

It has to be noted that all logic in the QuadSPI module implementing the AHB Bus access is designed to read the content of an external serial flash device. Therefore the following restrictions apply to the QuadSPI module with respect to accesses to the AHB bus:

- Any write access is answered with the ERROR condition according to the AMBA AHB Specification. No write occurs.
- Any AHB Command resulting in the assertion of the QSPI_FR[ABSEF] flag is answered with the ERROR condition according to the AMBA_AHB specification. The resulting AHB Command is ignored.

- AHB Bus access types fully supported are NONSEQ and BUSY.
- AHB access type SEQ is treated in the same way like NONSEQ. Refer to the AMBA AHB Specification for further details.

36.4.5.2 Memory Mapped Serial Flash Data - Individual Flash Mode on Flash A

Starting with address QSPI_AMBA_BASE the content of the first external serial flash devices is mapped into the address space of the device containing the QuadSPI module. Serial flash address byte address 0x0 corresponds to bus address QSPI_AMBA_BASE with increasing order. Assuming that a dual-die flash is connected on the first set of external pads, the address space is divided into two parts, one for each device of the dual die package. Refer to the following table for the address mapping. The byte ordering for 32 bit access is given in Table 36-22 and for 64 bit read access the byte ordering is given in Table 36-27.

Table 36-15. Memory Mapped Individual Flash Mode - Flash A Address Scheme

Memory Mapped Address 32 Bit Access	Memory Mapped Address 64 Bit Access	Serial Flash Byte Address	Flash Device
QSPI_AMBA_BASE + 0x00	QSPI_AMBA_BASE + 0x00	0x00_0000 to 0x00_0003	A1
QSPI_AMBA_BASE + 0x04		0x00_0004 to 0x00_0007	
…	…	…	
TOP_ADDR_MEMA1 - 0x08	TOP_ADDR_MEMA1 - 0x08	(TOP_ADDR_MEMA1- 0x08) to (TOP_ADDR_MEMA1 - 0x04 -0x01)	
TOP_ADDR_MEMA1 - 0x04		(TOP_ADDR_MEMA1 - 0x04) to (TOP_ADDR_MEMA1 - 0x01)	
TOP_ADDR_MEMA1 + 0x00	TOP_ADDR_MEMA1 + 0x00_0000	0x00_0000 to 0x00_0003	A2
TOP_ADDR_MEMA1 + 0x04		0x00_0004 to 0x00_0007	
…..	…	…	
TOP_ADDR_MEMA2 - 0x08	TOP_ADDR_MEMA2 - 0x08	(TOP_ADDR_MEMA2 - 0x08) to (TOP_ADDR_MEMA2 - 0x04 - 0x01)	
TOP_ADDR_MEMA2 - 0x04		(TOP_ADDR_MEMA2 - 0x04) to (TOP_ADDR_MEMA2 - 0x01)	

The available address range depends from the size of the external serial flash device. Any access beyond the size of the external serial flash provides undefined results.

For details concerning the read process refer to Flash Read.

36.4.5.3 Memory Mapped Serial Flash Data - Individual Flash Mode on Flash B

Starting with address TOP_ADDR_MEMA2 the content of the first external serial flash devices is mapped into the address space of the device containing the QuadSPI module. Serial flash address byte address 0x0 corresponds to bus address TOP_ADDR_MEMA2 with increasing order. Assuming that a dual-die flash is connected on the first set of external pads, the address space is divided into two parts, one for each device of the dual die package. Refer the following table for the address mapping. The byte ordering for 32 bit access is given in Table 36-22 and for 64 bit read access the byte ordering is given in Table 36-27.

Table 36-16. Memory Mapped Individual Flash Mode - Flash B Address Scheme

Memory Mapped Address 32 Bit Access	Memory Mapped Address 64 Bit Access	Serial Flash Byte Address	Flash Device
TOP_ADDR_MEMA2 + 0x00	TOP_ADDR_MEMA2 + 0x00	0x00_0000 to 0x00_0003	B1
TOP_ADDR_MEMA2 + 0x04		0x00_0004 to 0x00_0007	
…	…	…	
TOP_ADDR_MEMB1 - 0x08	TOP_ADDR_MEMB1 - 0x08	(TOP_ADDR_MEMB1- TOP_ADDR_MEMA2 - 0x08) to (TOP_ADDR_MEMB1 - TOP_ADDR_MEMA2 - 0x04 -0x01)	
TOP_ADDR_MEMB1 - 0x04		(TOP_ADDR_MEMB1- TOP_ADDR_MEMA2 - 0x04) to (TOP_ADDR_MEMB1- TOP_ADDR_MEMA2- 0x01)	
TOP_ADDR_MEMB1 + 0x00	TOP_ADDR_MEMB1 + 0x00_0000	0x00_0000 to 0x00_0003	B2
TOP_ADDR_MEMB1 + 0x04		0x00_0004 to 0x00_0007	
…..	…	…	
TOP_ADDR_MEMB2 - 0x08	TOP_ADDR_MEMA2 - 0x08	(TOP_ADDR_MEMB2 - TOP_ADDR_MEMB1- 0x08) to (TOP_ADDR_MEMB2 - TOP_ADDR_MEMB1 - 0x04 - 0x01)	
TOP_ADDR_MEMB2 - 0x04		(TOP_ADDR_MEMB2- TOP_ADDR_MEMB1 - 0x04) to (TOP_ADDR_MEMB2 - TOP_ADDR_MEMB1 - 0x01)	

The available address range depends from the size of the external serial flash device. Any access beyond the size of the external serial flash provides undefined results.

For details concerning the read process refer to Flash Read.

36.4.5.4 Parallel Flash Mode

Any of the AHB flexible-buffers can be configured to work in parallel flash mode by programming the QSPI_BFGENCR[PAR_EN] bit to '1'. When parallel mode is set, Flash A1 is paired with Flash B1 and Flash A2 is paired with Flash B2. In parallel mode, software should ensure that the size of Flash A1(A2) is equal to the size of Flash B1(B2).

Reads from any even AHB bus address provides bits [7:4] of both serial flash devices and reads from any odd AHB bus address provides bits [3:0] of both flash devices. Refer to the following table for the address mapping. The byte ordering for 32 bit access is given in Table 36-24 and for 64 bit read access the byte ordering is given in Table 36-27.

Table 36-17. Memory Mapped Parallel Flash Mode Address Scheme

Memory Mapped Address 32 Bit Access	Memory Mapped Address 64 Bit Access	Serial Flash A Byte Address	Serial Flash B Byte Address
QSPI_AMBA_BASE + 0x0000_0000	QSPI_AMBA_BASE + 0x00 For details, please refer to Parallel mode and Dual Die Flashes.	0x00_0000 - 0x00_0001	0x00_0000 - 0x00_0001
QSPI_AMBA_BASE + 0x0000_0004		0x00_002 - 0x00_0003	0x00_0002 - 0x00_0003
QSPI_AMBA_BASE + 0x0000_0008	QSPI_AMBA_BASE + 0x08	0x00_0004 - 0x00_0005	0x00_0004 - 0x00_0005
QSPI_AMBA_BASE + 0x0000_000C		0x00_0006 - 0x00_0007	0x00_0006 - 0x00_0007
…	…	…	…
TOP_ADDR_MEMB2 - 0x08	TOP_ADDR_MEMB2 - 0x08	(TOP_ADDR_MEMB2 - QSPI_AMBA_BASE - 0x08)/2	(TOP_ADDR_MEMB2 - QSPI_AMBA_BASE - 0x08)/2
TOP_ADDR_MEMB2 - 0x04		(TOP_ADDR_MEMB2 - QSPI_AMBA_BASE - 0x04)/2 +0x01	(TOP_ADDR_MEMB2 - QSPI_AMBA_BASE- 0x04)/2 + 0x01

The available address range covers 27 address bits, corresponding to 128 MB per flash device. The usable space depends from the size of the external serial flash devices. Any access beyond the size of the external serial flash provides undefined results.

For details concerning the read process refer to Flash Read.

36.4.5.5 AHB RX Data Buffer (QSPI_ARDB0 to QSPI_ARDB15)

NOTE

See the System Memory map in this document for the base address of the QSPI AHB RX Data Buffer.

memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	AHB RX Data Buffer register (ARDB0)	32	R/W	0000_0000h	36.4.5.5.1/ 948
4	AHB RX Data Buffer register (ARDB1)	32	R/W	0000_0000h	36.4.5.5.1/ 948
8	AHB RX Data Buffer register (ARDB2)	32	R/W	0000_0000h	36.4.5.5.1/ 948
C	AHB RX Data Buffer register (ARDB3)	32	R/W	0000_0000h	36.4.5.5.1/ 948
10	AHB RX Data Buffer register (ARDB4)	32	R/W	0000_0000h	36.4.5.5.1/ 948
14	AHB RX Data Buffer register (ARDB5)	32	R/W	0000_0000h	36.4.5.5.1/ 948
18	AHB RX Data Buffer register (ARDB6)	32	R/W	0000_0000h	36.4.5.5.1/ 948
1C	AHB RX Data Buffer register (ARDB7)	32	R/W	0000_0000h	36.4.5.5.1/ 948
20	AHB RX Data Buffer register (ARDB8)	32	R/W	0000_0000h	36.4.5.5.1/ 948
24	AHB RX Data Buffer register (ARDB9)	32	R/W	0000_0000h	36.4.5.5.1/ 948
28	AHB RX Data Buffer register (ARDB10)	32	R/W	0000_0000h	36.4.5.5.1/ 948
2C	AHB RX Data Buffer register (ARDB11)	32	R/W	0000_0000h	36.4.5.5.1/ 948
30	AHB RX Data Buffer register (ARDB12)	32	R/W	0000_0000h	36.4.5.5.1/ 948
34	AHB RX Data Buffer register (ARDB13)	32	R/W	0000_0000h	36.4.5.5.1/ 948
38	AHB RX Data Buffer register (ARDB14)	32	R/W	0000_0000h	36.4.5.5.1/ 948
3C	AHB RX Data Buffer register (ARDB15)	32	R/W	0000_0000h	36.4.5.5.1/ 948

36.4.5.5.1 AHB RX Data Buffer register (ARDB)

The AHB RX Data Buffer register 0 to 15 can be used to read the buffer content of the RX Buffer from successive addresses. QSPI_ARDB0 corresponds to the RX Buffer register entry corresponding to the current value of the read pointer with increasing order.

The increment of the read pointer depends from the access scheme (DMA or flag-driven). Refer to "Data Transfer from the QuadSPI Module Internal Buffers" section in Flash Read section, RX Buffer, data read via register interface and AHB read, for the description of successive accesses to the RX Buffer content. Refer also to Byte Ordering of Serial Flash Read Data for the byte ordering scheme.

Valid address range accessible in the QSPI_ARDBn range depends from the number of RX Buffer entries implemented and from the number of valid buffer entries available in the RX Buffer.

- Example 1, RX Buffer filled completely with 16 words: In this case the address range for valid read access extends from QSPI_ARDB0 to QSPI_ARDB15.
- Example 2, RX Buffer filled with 5 valid words, RX Buffer fill level QSPI_RBSR[RDBFL] is 5. In this case an access to QSPI_ARDB4 provides the last valid entry.

Address: 0h base + 0h offset + (4d × i), where i=0d to 15d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	ARXD																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ARDB*n* field descriptions

Field	Description
ARXD	ARDB provided RX Buffer Data. Byte order (endianness) is identical to the RX Buffer Data Registers.

36.5 Interrupt Signals

The interrupt request lines of the QuadSPI module are mapped to the internal flags according to the following table.

Table 36-18. Assignment of Interrupt Request Lines

IRQ/DMA line	QSPI_FR Flag	Interrupt Description
ipi_int_tfff	TBFF	TX Buffer Fill

Table continues on the next page...

Table 36-18. Assignment of Interrupt Request Lines (continued)

IRQ/DMA line	QSPI_FR Flag	Interrupt Description
ipi_int_tcf	TFF	Peripheral Command Transaction Finished
ipi_int_rfdf	RBDF	RX Buffer Drain
ipi_int_overrun		Buffer Overflow/Underrun Error Logical OR from:
	RBOF	RX Buffer Overrun
	TBUF	TX Buffer Underrun
	ABOF	AHB Buffer Overflow
ipi_int_cerr		Serial Flash Command Error Logical OR from:
	IPAEF	Peripheral access while AHB busy Error
	IPIEF	Peripheral Command could not be triggered Error
	IPGEF	Peripheral access while AHB Grant Error
	IUEF	Peripheral Command Usage Error
ipi_int_ored	DLPFF, TBFF, TFF, ILLINE, RBDF, RBOF, TBUF, ABSEF, ABOF, IPAEF, IPIEF, IPGEF, IUEF, AITEF,AIBSEF	Logical OR from all the QSPI_FR flags mentioned

36.6 Functional Description

This section provides the functional information of the QuadSPI module.

36.6.1 Serial Flash Access Schemes

The following access schemes are possible, depending on the serial flash devices attached to the QuadSPI module.

Table 36-19. Access Schemes for Serial Flash Data Access

Access Scheme	One Flash Device on Port A	One Flash Device on Port B	Two identical Flash Devices connected on Port A and Port B
Individual Flash Mode: Access to Flash A	**Yes**	**N/a**	**Yes**
Individual Flash Mode: Access to Flash B	**N/a**	**Yes**	**Yes**
Parallel Flash Mode: Read from Flash A and Flash B	**N/a**	**N/a**	**Yes**

Note

If two flash devices are accessed in Parallel Flash Mode, they are accessed with identical control signals. Special alignment on per-flash basis is **not** possible. It is within the responsibility of the application to ensure that the identical signals are applicable to both flash devices.

In Parallel Flash Mode, both external serial flash devices appear logically as one single memory doubled in size with respect to one individual flash device.

If two different flash devices are attached, they can be operated only in Individual Flash Mode.

In the Parallel Flash Mode, only data read commands and write command (in x1 mode) are supported. Any other IP Command will result in an error condition signaled by the assertion of the QSPI_FR[IUEF] flag and any other AHB Command will result in the assertion of the QSPI_FR[ABSEF] flag.

In the Individual Flash Mode, all supported commands are available.

Unless explicitly noted, all the following descriptions relate to the Individual Flash Mode.

36.6.2 Modes of Operation

Refer to QuadSPI Modes of Operation for an overview over the possible operational modes of the QuadSPI block.

- Normal Mode can be used for write or read accesses to an external serial flash device.
  - Serial Flash Write: Data can be programmed into the flash via the IP interface only. Refer to Flash Programming for further details.
  - Serial Flash Read: Read the contents of the serial flash device. Two separate read channels are available via RX Buffer and AHB Buffer, see Flash Read.

- Stop Mode: The mode is used for power management. When a request is made to enter Stop Mode, the QuadSPI block acknowledges the request and completes the SFM Command in progress, then the system clocks to the QuadSPI block may be shut off
- Module Disable Mode: The mode is used for power management. The clock to the non-memory mapped logic in the QuadSPI can be stopped while in Module Disable Mode. The module enters the mode by setting QSPI_MCR[MDIS].

36.6.3 Normal Mode

This mode is used to allow communication with an external serial flash device. Compared to the standard SPI protocol, this communication method uses up to 4 bidirectional data lines operating at high data rates. The communication to the external serial flash device consists of an instruction code and optional address, mode, dummy and data transfers. The flexible programmable core engine described below is immune to a wide variety of command/protocol differences in the serial flash devices provided by various flash vendors.

36.6.3.1 Programmable Sequence Engine

The core of the QuadSPI module is a programmable sequence engine that works on "instruction-operand" pairs. The core controller executes each programmed instruction sequentially. The complete list of instructions and the corresponding operands is given in the following table.

Table 36-20. Instruction set

Instruction	Instruction encoding	Pins	Operand	Action on Serial Flash(es)
CMD	6'd1	N=2'd{0,1,2,3} 2'd0 - One pad 2'd1 - Two pads 2'd2 - Four pads 2'd3- Eight pads	8 bit command value	Provide the serial flash with operand on the number of pads specified
ADDR	6'd2		Number of address bits to be sent (for example, 8'd24 => 24 address bits required)	Provide the serial flash with address cycles according to the operand on the number of pads specified. The actual address to be provided will be derived from the incoming address in case of AHB initiated transactions and the value of SFAR in case of IPS initiated transactions , if QSPI_SFACR[CAS] is set to 0, else the actual address will take CAS into consideration.

Table continues on the next page...

Table 36-20. Instruction set (continued)

Instruction	Instruction encoding	Pins	Operand	Action on Serial Flash(es)
DUMMY	6'd3		Number of dummy clock cycles (should be <= 64 cycles)	Provide the serial flash with dummy cycles as per the operand. The PAD information defines the number of pads in input mode. (for example, one pad implies that pad 1 is not driven, rest all are driven)
MODE	6'd4		8 bit mode value	Provide the serial flash with 8 bit operand on the number of pads specified
MODE2	6'd5	N=2'd{0,1}	2 bit mode value	Provide the serial flash with 2 bit operand on the number of pads[1] specified
MODE4	6'd6	N=2'd{0,1,2}	4 bit mode value	Provide the serial flash with 4 bit operand on the number of pads[2] specified
READ	6'd7	N=2'd{0,1,2,3} 2'd0 - One pad 2'd1 - Two pads 2'd2 - Four pads 2'd3- Eight pads	Read data size in bytes (the user's application should ensure that data size is a multiple of 8 bytes)	Read data from flash on the number of pads specified. The data size may be overwritten by writing to the ADATSZ field of the QSPI_BUFxCR registers for AHB initiated transactions and IDATSZ field of IP Configuration Register (QuadSPI_IPCR) for IP initiated transactions.
WRITE	6'd8		Write data size in bytes	Write data on number of pads sepcified. The data size may be overwritten by writing to the IDATSZ field of IP Configuration Register (QuadSPI_IPCR) register
JMP_ON_CS	6'd9	NA	Instruction number	Every time the CS is deasserted, jump to the instruction pointed to by the operand. This instruction allows the programmer to specify the behavior of the controller when a new read transaction is initiated following a CS deassertion.
ADDR_DDR	6'd10	N=2'd{0,1,2,3} 2'd0 - One pad 2'd1 - Two pads 2'd2 - Four pads 2'd3- Eight pads	Number of address bits to be sent (for example, 8'd24 => 24 address bits required)	Provide the serial flash with address cycles according to the operand on the number of pads specified at each clock edge of serial flash clock. The actual address to be provided will be derived from the incoming address in case of AHB initiated transactions and the value of QSPI_SFAR in case of IPS initiated transactions , if QSPI_SFACR[CAS] is set to 0, else the actual address will take CAS into consideration.
MODE_DDR	6'd11		8 bit mode value	Provide the serial flash with 8 bit operand on the number of pads specified at each clock edge of serial flash.
MODE2_DDR	6'd12	N=2'd{0}	2 bit mode value	Provide the serial flash with 2 bit operand on the number of pads specified at each clock edge of serial flash[3]
MODE4_DDR	6'd13	N=2'd{0,1}	4 bit mode value	Provide the serial flash with 4 bit operand on the number of pads specified at each clock edge of serial flash[4].
READ_DDR	6'd14	N=2'd{0,1,2,3} 2'd0 - One pad 2'd1 - Two pads 2'd2 - Four pads	Read data size in bytes (the user's application should ensure that data size is in multiple of 8 bytes)	Read data from flash on the number of pads specified at each clock edge of serial flash. The data size may be overwritten by writing to the ADATSZ field of the QSPI_BUFxCR registers for AHB initiated transactions and IDATSZ field of IP Configuration Register (QuadSPI_IPCR) for IP initiated transactions

Table continues on the next page...

Table 36-20. Instruction set (continued)

Instruction	Instruction encoding	Pins	Operand	Action on Serial Flash(es)
WRITE_DDR	6'd15	2'd3- Eight pads	Write data size in bytes	Write data on the number of pads specified at each clock edge of serial flash. The data size may be overwritten by writing to the IDATSZ field of IP Configuration Register (QuadSPI_IPCR) register
DATA_LEARN	6'd16		Number of data in bytes to be used for data learning. Say if operand is 1 than 8 bit data_learning is enabled.	Finds the correct sampling point in case of only DDR operations. When this instruction is encountered, the QSPI_SMPR[DDRSMP] values are ignored and the controller finds the correct sampling point on its own by data learning. But this feature of sampling point is valid for only DDR modes. If DQS mode is enabled, then data learn instruction just matches the incoming data from flash and if it does not matches the QSPI_DLPV then Flag in QSPI_FR[DLPFF] is set.
CMD_DDR	6'd17	N=2'd{0,1,2,3} 2'd0 - One pad 2'd1 - Two pads 2'd2 - Four pads 2'd3- Eight pads	8 bit command value	Provide the serial flash with the operand with number of pads specified at each clock edge of the serial flash
CADDR	6'd18		Number of Column address bits to be sent(8'd8 means 8 bits of column address is to be sent)	Provide the serial flash with column address cycles according to the operand on the number of pads specified. The actual address to be provided to flash will depend on value of QSPI_SFACR[CAS]. For example, if QSPI_SFACR[CAS] is 3, then the address to flash will be [2:0] of incoming address in case of AHB and the value of QSPI_SFAR in case of IP. This will be appended with zero if QSPI_SFACR[CAS] is less than number of pads for a Flash.
CADDR_DDR	6'd19		Number of Column address bits to be sent(8'd8 means 8 bits of column address is to be sent)	Provide the serial flash with column address cycles according to the operand on the number of pads specified at each clock edge of the serial flash. The actual address to be provided to flash will depend on value of QSPI_SFACR[CAS]. For example, if CAS is 3, then the address to flash will be [2:0] of incoming address in case of AHB and the value of QSPI_SFAR in case of IP. This will be appended with zero if CAS is less than number of pads for a Flash.
STOP	8'd0	NA	NA	Stop execution; deassert CS

1. For a one pad instruction, MODE2 will take 2 serial flash clock cycles on the flash interface.
2. For a one pad instruction, MODE4 will take 4 serial flash clock cycles on the flash interface. For a 4 pad instruction, MODE4 will take 1 serial flash clock cycle on the flash interface.
3. For a one pad instruction, MODE2_DDR will take 1 serial flash clock cycle on the flash interface.
4. For a one pad instruction, MODE4_DDR will take 2 serial flash clock cycles on the flash interface. For a 4 pad instruction MODE4_DDR will take half a cycle on the serial flash interface.

A sequence of such instruction-operand pairs may be pre-populated in the LUT according to the device connected on board. Each instruction-operand pair is of 16 bits (2 bytes) each. Every sequence pre-programmed in the LUT is referred to by its index.

The programmable sequence engine allows the user to configure the QuadSPI module according to the serial flash connected on board. The flexible structure is easily adaptable to new command/protocol changes from different vendors.

36.6.3.2 Flexible AHB buffers

In order to reduce the latency of the reads for AHB masters, the data read from the serial flash is buffered in flexible AHB buffers. There are four such flexible buffers. The size of each of these buffers is configurable with the minimum size being 0 Bytes and maximum size being the size of the complete buffer instantiated.The size of buffer 0 is defined as being from 0 to QSPI_BUF0IND. The Size of buffer 1 is from QSPI_BUF0IND to QSPI_BUF1IND, buffer2 is from QSPI_BUF1IND to QSPI_BUF2IND and buffer 3 is from QSPI_BUF2IND to the size of the complete buffer, which is given in the chip-specific QuadSPI information.

Each flexible AHB buffer is associated with the following

1. An AHB master. Optionally, buffer3 may be configured as an "all master" buffer by setting the QSPI_BUF3CR[ALLMST] bit. When buffer3 is configured in such a way, any access from a master not associated with any other buffer is routed to buffer3.
2. A datasize field representing the amount of data to be fetched from the flash on every "missed" access.

The master port number of every incoming request is checked and the data is returned/ fetched into the corresponding associated buffer. Every "missed" access to the buffer causes the controller to clear the buffer and fetch QSPI_BUFxCR[ADATSZ] amount of data from the serial flash.As such, there is no benefit in configuring a buffer size of greater than ADATSZ, as the locations greater than ADATSZ will never be used. For any AHB access, the sequence pointed to by the QSPI_BFGENCR[SEQID] field is used for the flash transaction initiated. The data is returned to the master as soon as the requested amount is read from the serial flash. The controller however, continues to prefetch the rest of the data in anticipation of a next consecutive request. Figure 36-4 shows the flexible AHB buffers.

The QSPI_BFGENCR[SEQID] field points to an index of the LUT. Refer to Look-up Table for details.

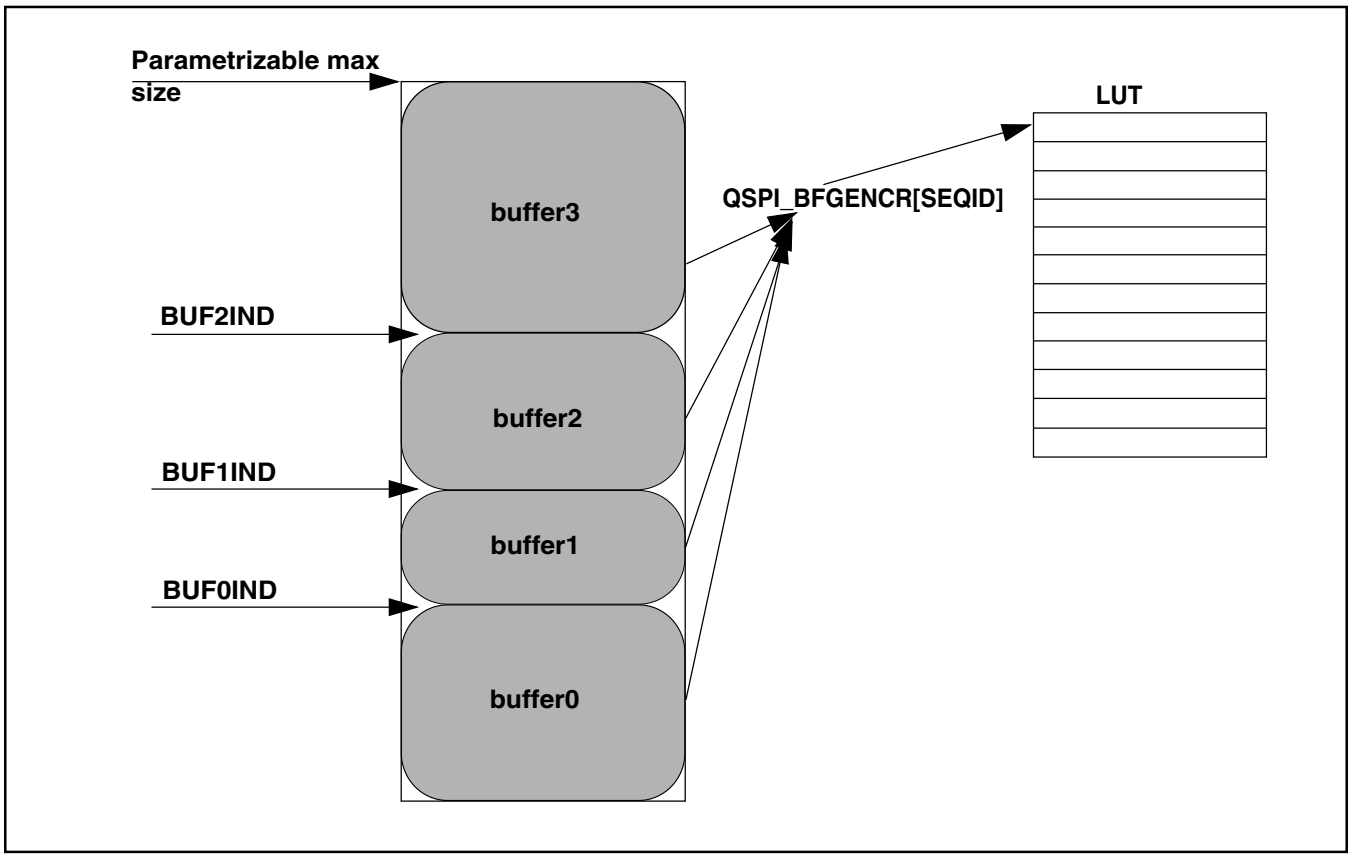


Figure 36-4. Flexible AHB Buffers

Buffer0 may optionally be configured to be associated with a high priority master by setting the QSPU_BUF0CR[HP_EN] bit.

NOTE

The high-priority feature is disabled if OTFAD is enabled in the system.

An access by a high priority master suspends any ongoing prefetch to any of the other buffers. The ongoing prefetch is suspended and the high priority master is serviced first. Once the high priority masters access completes, the suspended transaction is resumed (before any other AHB access is entertained). The status of the suspended buffer can be read from Sequence Suspend Status Register (QuadSPI_SPNDST).

36.6.3.3 Suspend-Abort Mechanism

Any low priority AHB access can be suspended by a high priority AHB master request. The ongoing transaction is suspended at 64 bit boundary. The suspended transaction is restarted after the high priority master is served and the high priority transaction

including data prefetch is completed. While a transaction is in suspended state, it may be aborted if a transaction by the same suspended master is made to a location which is different from the location of the suspended transaction.

Any ongoing transaction is aborted if a request from the same master arrives for a location other than the location at which the transaction is going on. The abort can happen at any point of time.

36.6.3.4 HBURST Support

QuadSPI controller supports HBURST and HSIZE on the AHB interface. HBURST indicates if the transfer forms part of a burst. Four, eight and sixteen beat bursts are supported and the burst may be either incrementing or wrapping. HSIZE indicates the size of the transfer. 8, 16, 32 and 64 bit data size are supported. In case of WRAP accesses, QuadSPI generates aligned accesses to Serial Flash if there is no buffer hit for any incoming non-sequential AHB access. In case there is a buffer hit, the incoming address in the haddr line is latched as it is. If the total burst size is more than the data prefetch size an error response is generated and QSPI_FR[AIBSEF] is set. The data perfetch size can be defined by QSPI_BUFxCR[ADATSZ] or data size mentioned in the sequence pointed to by the SEQID field when ADATSZ is programmed as zero. A few examples are shown in the figure below:

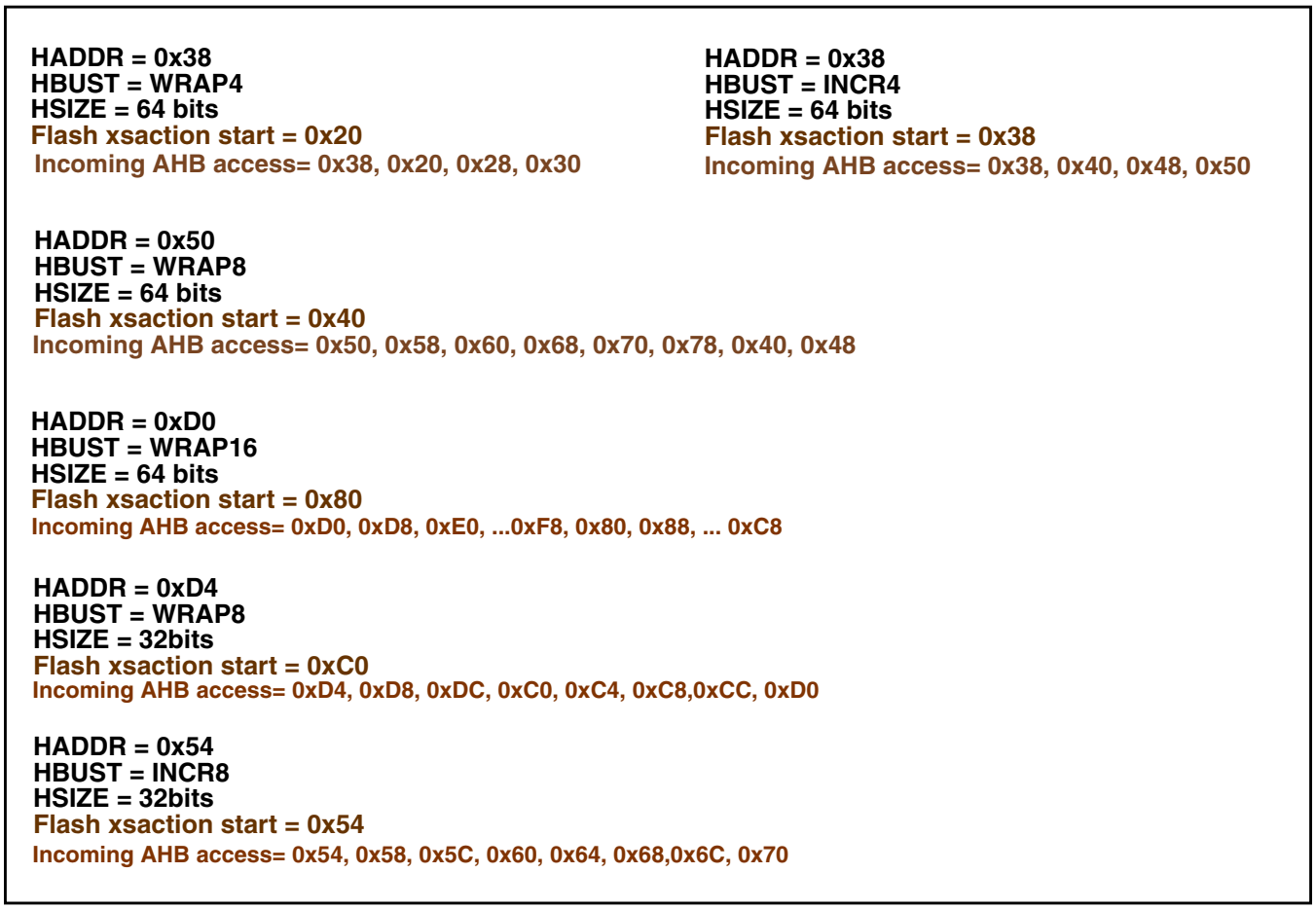


Figure 36-5. QuadSPI HBURST support

NOTE

The software must take care that the prefetch size should never be set less than the minimum data needed by any external interface to start processing.

36.6.3.5 Look-up Table

The Look-up-table or LUT consists of a number of pre-programmed sequences. Each sequence is basically a sequence of instruction-operand pairs which when executed sequentially generates a valid serial flash transaction. Each sequence can have a maximum of 8 instruction-operand pairs. The LUT can hold a maximum of 16 sequences. The figure below shows the basic structure of the sequence in the LUT.

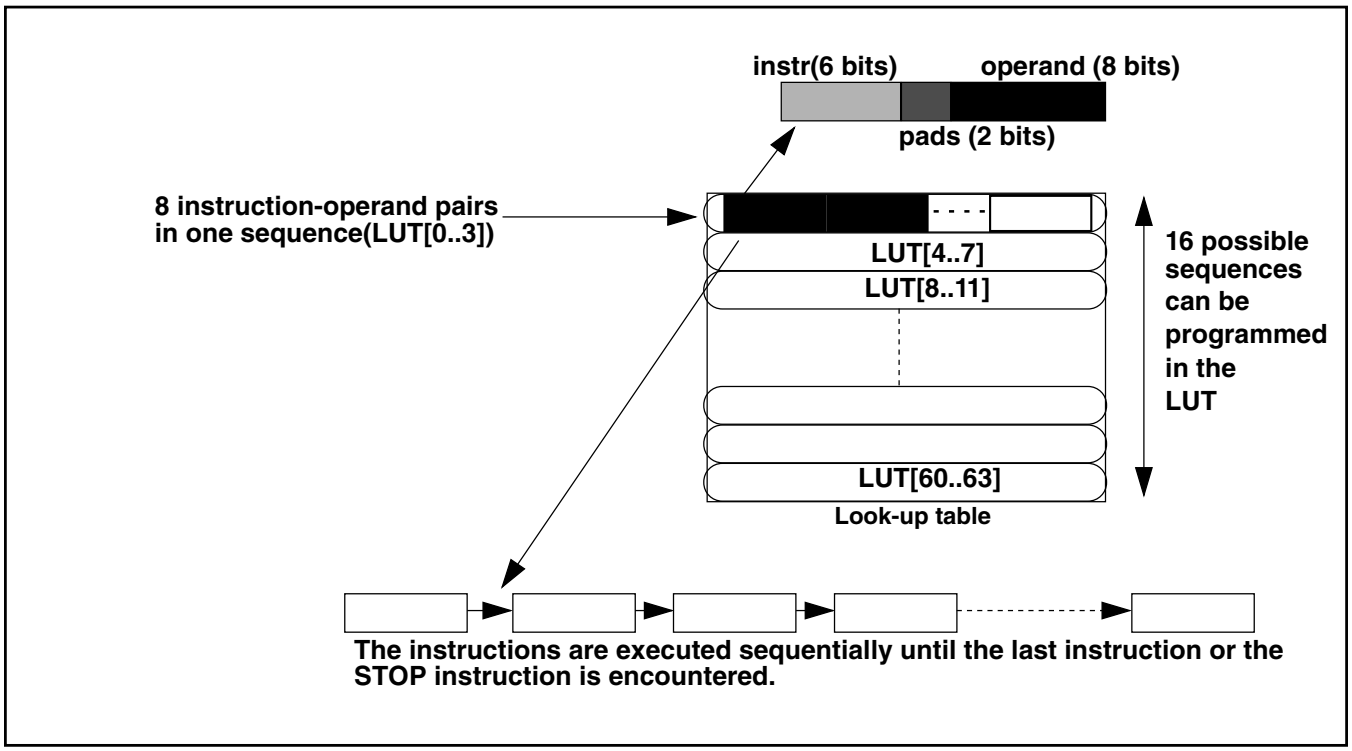


Figure 36-6. LUT and sequence structure

At reset, the index 0 of the look-up-table (LUT[0..3]) is programmed with a basic read sequence as given in Table 36-21. After reset the complete LUT may be reprogrammed according to the device connected on board.In order to protect its contents during a code runover the LUT may be locked, after which a write to the LUT will not be successful until it has been unlocked again.The key for locking or unlocking the LUT is **0x5AF05AF0**. The process for locking and un-locking the LUT is as follows:

Locking the LUT

1. Write the key **(0x5AF05AF0)** in to the LUT Key Register (QuadSPI_LUTKEY).
2. Write 0b01 to the LUT Lock Configuration Register (QuadSPI_LCKCR). Note that this IPS transaction should immediately follow the above IPS transaction (no other IPS transaction can be issued in between). A successful write into this register locks the LUT.

Unlocking the LUT

1. Write the key **(0x5AF05AF0)** into the LUT Key Register (QuadSPI_LUTKEY)
2. Write 0b10 to the LUT Lock Configuration Register (QuadSPI_LCKCR). Note that this IPS transaction should immediately follow the above IPS transaction (no other IPS transaction can be issued in between). A successful write into this register unlocks the LUT.

The lock status of the LUT can be read from QSPI_LCKCR[UNLOCK] and QSPI_LCKCR[LOCK] bit.

Some example sequences are defined in Example Sequences. The reset sequence at LUT index 0 is given in the following table.

Table 36-21. Reset sequence

Instruction	Pad	Operand	Comment
CMD	0x00	0x03	Read Data byte command on one pad
ADDR	0x00	0x18	24 Addr bits to be sent on one pad
READ	0x00	0x08	Read 64 bits
JMP_ON_CS	0x00	0x00	Jump to instruction 0 (CMD)

36.6.3.6 Issuing SFM Commands

Each access to the external device follows the same sequence:

1. The user must pre-populate the LUT with the serial flash command sequences that are required for the flash device being used.
2. The QuadSPI module starts executing the instructions in the sequence one by one. The transaction starts and the status bit QSPI_SR[BUSY] is set.
3. Communication with the external serial flash device is started and the transaction is executed.
4. When the transaction is finished (all transmit- and receive operations with the external serial flash device are finished) the status bit QSPI_SR[BUSY] is reset. In case of an IP Command the QSPI_FR[TFF] flag is asserted.

Further details are given in below in Flash Programming and Flash Read.

You can trigger the processing of SFM commands in the QuadSPI module in one of the following ways:

- **Using IP commands**

  For IP Commands the required components need to be written into the following registers:

  - Write the serial flash address to be used by the instruction into QSPI_SFAR, refer to Serial Flash Address Register (QSPI_SFAR). For IP Commands not related to specific addresses, the base address of the related flash need to be

programmed.For example, for an instruction which does not require an address (i.e. write enable instruction) the SFAR should be programmed with the base address of the memory the command is to be sent to.

- Write the sequence ID and data size details in the IP Configuration Register (QSPI_IPCR).
- Note that the write into the QSPI_IPCR[SEQID] field must be the last step of the sequence. It is possible to combine all fields of the QSPI_IPCR into one single write. Refer to IP Configuration Register (QSPI_IPCR) for details.

Note that there are some conditions where no IP Command is executed after writing the QSPI_IPCR[SEQID] field and the write operation itself is ignored. They are described in Command Arbitration.

- **Using AHB commands**

  Any AHB memory mapped access is routed to one of the buffers depending on the master port number of the request. If the access is a "miss", a new serial flash transaction is started. The transaction is based on the sequence pointed to by the BFGENCR[SEQID] field as described in Flexible AHB buffers.

  An AHB access is termed memory mapped when the access is to the memory mapped serial flashes, as described in Memory Mapped Serial Flash Data - Individual Flash Mode on Flash A and Memory Mapped Serial Flash Data - Individual Flash Mode on Flash B.

  Again the possible error conditions are described in Command Arbitration .

36.6.3.7 Flash Programming

In all cases the memory sector to be written needs to be erased first. The programming sequence itself is then initiated in the following way:

1. Check that the TX Buffer is empty. If the QSPI_SR[TXEDA] bit is set then the TX Buffer must be cleared by writing 1 into the QSPI_MCR[CLR_TXF] bit.
2. Program the address related to the command in the QSPI_SFAR register. Program the QSPI_SFACR[CAS] if required to desired value else to 0. Program the QSPI_SFACR[WA] to 1 if the serial flash is a word addressable flash else to 0 in case serial flash is byte addressable.

3. Provide initial data for the program command into the circular buffer via register TX Buffer Data Register (QSPI_TBDR) . At least four word of data must be written into the TX Buffer up to a maximum of 16.
4. Program the QSPI_IPCR register to trigger the command. The QSPI_IPCR[SEQID] should point to an index of the LUT which has the flash program sequence pre-programmed.The IDATSZ field should be set to denote the size of the write.
5. Depending on the amount of data required, step 3 must be repeated until all the required data have been written into the QSPI_TBDR register.The QSPI_SR[TXFULL] can be used to check if the buffer is ready to receive more data. At any time, the QSPI_TBSR[TRCTR] field can be read to check how many words have been written actually into the TX Buffer.

Upon writing the QSPI_IPCR[SEQID] field (refer to step 4) the QuadSPI module will start to execute the programmed sequence. It is the responsibility of the software to ensure that a correct sequence is programmed into the LUT in accordance with the flash memory connected to the module. The data is fetched from the TX Buffer. It consists of **16** entries of 32-bits and is organized as a circular FIFO, whose read pointer is incremented by four after each fetch. When all data are transmitted, the QuadSPI module will return from 'busy' to 'idle'. However, this is not true for the external device since the internal programming is still ongoing. It is up to the user to monitor the relevant status information available from the serial flash device and to ensure that the programming is finished properly.

36.6.3.8 Flash Read

Host access to the data stored in the external serial flash device is done in two steps. First, the data must be read into the internal buffers and in the second step these internal buffers can be read by the host.

1. **Reading Serial Flash Data into the QuadSPI Module Internal Buffers**

   A read access to the external serial flash device can be triggered in two different ways:

   - **IP Command Read**: For **reading flash data into the RX Buffer** the user must provide the correct sequence ID in the QuadSPI_IPCR[SEQID] register. The sequence ID points to a sequence in the LUT. It is the responsibility of the software to ensure that a correct read sequence is programmed in the LUT in accordance with the serial flash device connected on board. The user should

program the Serial Flash Address Register (QSPI_SFAR) , QSPI_SFACR[CAS] and the IP Configuration Register (QSPI_IPCR) registers. All available read commands supported by the external serial flash are possible.

Optionally it is possible to clear the RX Buffer pointer prior to triggering the IP Command by writing a 1 into the QuadSPI_MCR[CLR_RXF] field.

From these inputs, the complete transaction is built when the QSPI_IPCR[SEQID] field is written. The transaction related to the read access starts and the requested number of bytes is fetched from the external serial flash device into the RX Buffer. Since the read access is triggered by an IP command, the IP_ACC status bit and the BUSY bit are both set (both are located in the Status Register (QSPI_SR)). A count of the number of entries currently in the Rx Buffer can be obtained from QSPI_RBCT[RXBRD].

The communication with the external serial flash is stopped when the specified number of bytes has been read (successful completion of the transaction).

- **AHB Command Read**: For **reading flash data into the AHB Buffer** the user must set up a read access by a master to the address range in the system memory map which the external serial flash devices are mapped to. The user should program the QSPI_SFACR[CAS], if required, to desired value else to 0.The user should also program the buffer registers corresponding to the AHB master initiating the request, this is depends on the configuration of the QSPI_RBCT[RXBRD]. The user should provide the correct sequence ID into the buffer generic configuration register (QSPI_BFGENCR). It is the responsibility of the software to ensure that a correct read sequence in programmed in the LUT in accordance with the serial flash device connected on board. Flash device selection and access mode are determined by the address accessed in the AHB address space associated to the QuadSPI module (refer to Memory Mapped Serial Flash Data - Individual Flash Mode on Flash A, Memory Mapped Serial Flash Data - Individual Flash Mode on Flash B and Parallel Flash Mode.)

  On each AHB read access to the memory mapped area the valid data in the AHB Buffer is checked against the address requested in the actual read. When the AHB read request can't be served from the content of the AHB Buffer, the buffer is flushed and the sequence pointed to by the sequence ID is executed by the controller. The requested number of buffer entries defined in the QSPI_BUFxCR[ADATSZ] field is then fetched from the external serial flash device into the internal AHB Buffer. Since the read access is triggered via the AHB bus, the QSPI_SR[AHB_ACC] status bit is set driving in turn the

QSPI_SR[BUSY] bit until the transaction is finished. The communication with the external serial flash is stopped when the specified number of entries has been filled.

2. **Data Transfer from the QuadSPI Module Internal Buffers**

   The data read out from the external serial flash device by the QuadSPI module is stored in the internal buffers.The means of accessing the data from the buffer differs depending on which buffer the data has been loaded to. Refer to Block Diagram for details about the two available buffers, the RX Buffer and the AHB Buffer, in the QuadSPI module:

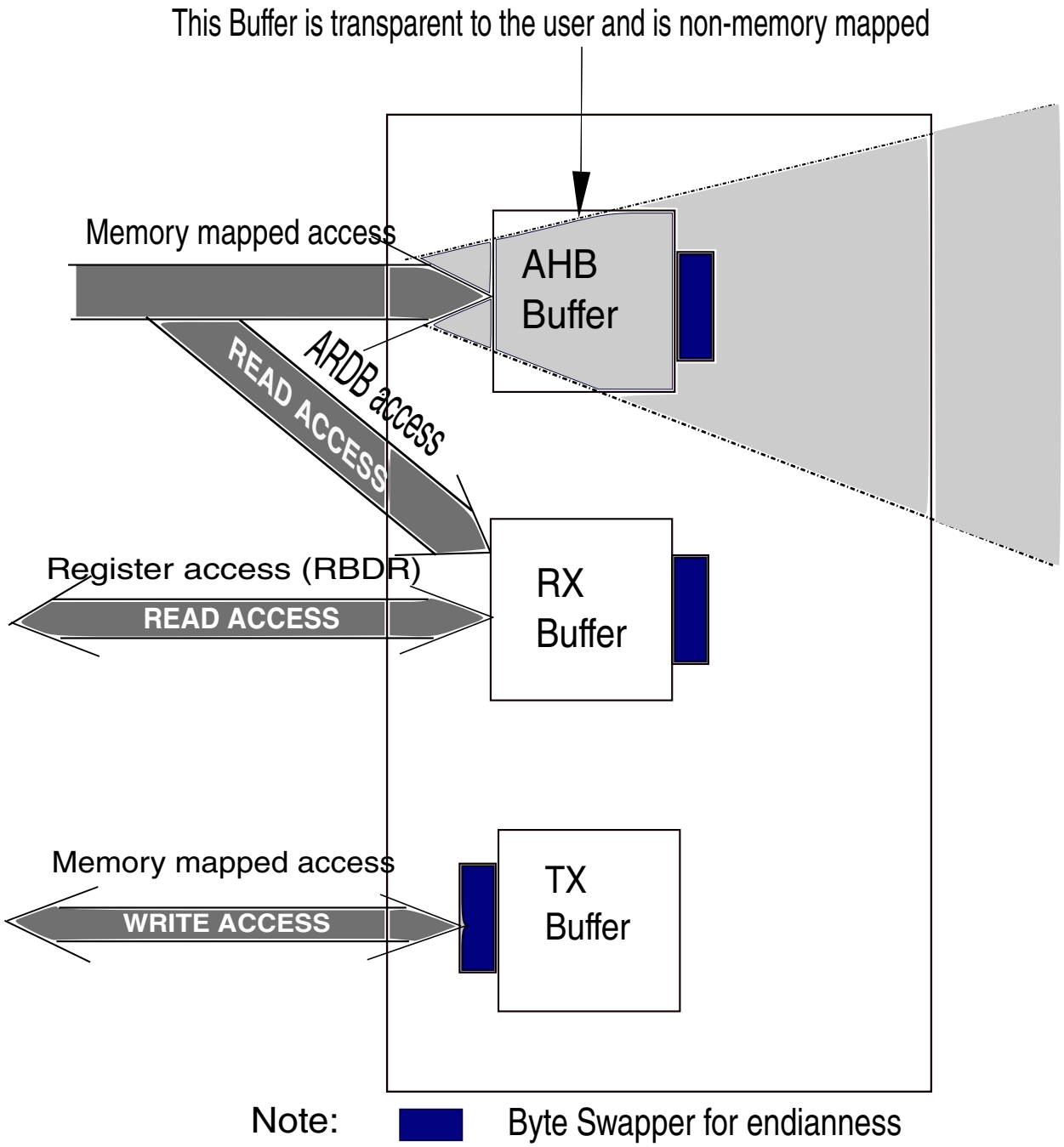


Figure 36-7. QuadSPI memory map

- The RX Buffer is implemented as FIFO of depth 16 entries of 4 bytes. Its content is accessible in two different address areas both referring to the identical data and the same physical memory.

  In the IPS address space in the area associated to QSPI_RBDR0 to QSPI_RBDR15

  In the AHB address space in the area associated to QSPI_ARDB0 to QSPI_ARDB15. Two successive entries are accessed with one single 64 bit AHB read operation.

RX Buffer operation can be summarized as follows: The QSPI_RBCT[WMRK] field determines at which fill level the RXWE bit is asserted and how many entries are removed from the RX Buffer on each Buffer POP operation. So the QSPI_SR[RXWE] bit indicates that the configured number of data entries is available in the RX Buffer and the QSPI_RBSR[RDBFL] field indicates how many valid entries are available in total. Note that the first entry (QSPI_RBDR0 or QSPI_ARDB0) always corresponds to the first valid entry in the RX Buffer. The software needs to manage the number of valid data bytes itself.

Further details can be found in RX Buffer Data Register (QuadSPI_RBDR) and in AHB RX Data Buffer (QSPI_ARDB0 to QSPI_ARDB15).

- **Flag-based Data Read of the RX Buffer** is done by polling the QSPI_SR[RXWE] bit. When it is asserted the valid entries can be read either via the IPS address space (QSPI_RBDRn) or the AHB address space (QSPI_ARDBn). A Buffer POP operation must be triggered by the application by writing a 1 into the QSPI_FR[RBDF] bit - this automatically updates the FIFO to point to the next entry as defined by RBCT[WMRK]. For example, if WMRK is set to 3, then the buffer will discard 16 bytes of data.
- **DMA controlled Data Read of the RX Buffer** is done by using the DMA module.The application must ensure that the DMA controller of the related device is programmed appropriately like it is described in DMA Usage.

  DMA controlled read out is triggered fully automatically by the assertion of the QSPI_SR[RXWE] bit. The related Buffer POP operation is also handled completely inside the QuadSPI module. Like in the case above, accessing the RX Buffer content either on QSPI_RBDRn or QSPI_ARDBn related addresses is equivalent.

- **AHB Buffer data read via memory mapped access:** This kind of access is done by reading one of the addresses assigned to the external serial flash device(s) within the range given in Table 36-14 table *under the condition that the data requested are already present in the AHB Buffer or it is currently being read from the serial flash device by the instruction in progress.* If this is not the case a memory mapped AHB command read is triggered as described above. If the requested data is already available in the AHB Buffer they are provided directly to the host.

  When AHB access are made to the flash memory mapped address, the data will be fetched and returned to the AHB interface. Till the data is being fetched the AHB interface would be stalled. As soon as the data from the requested address has been read by the QuadSPI module the AHB read access is served. So it is possible to run sequential reads from the AHB buffer at arbitrary speed without

the need to monitor any information about the availability of the data. Nevertheless this access scheme stalls the AHB bus for the time required to read the data from the serial flash device. A better way is (when it is known the access is sequential) to have a prefetch enabled (by programming the ADATSZ field) such that before the next sequential AHB access come, the data is already fetched into the buffer.

As long as the host restricts its accesses to the data already in the buffer and the data currently fetched from the serial flash, it is possible to run the host read from the AHB Buffer in parallel to the serial flash read into the AHB Buffer.

36.6.3.9 Byte Ordering of Serial Flash Read Data

In this paragraph the byte ordering of the serial flash data is given. The basic scheme is that the **first** byte read out of the serial flash device - which is addressed by the QSPI_SFAR[SFADR] field - corresponds to bit position QSPI_RBDR0[31:24] register for IP Command read. In contrast to that for AHB Command read the bytes are always positioned according to the byte ordering of the AHB bus.

- **Byte Ordering in Individual Flash Mode**

  The following table gives the byte ordering scheme of how the byte oriented data space of the serial flash device is mapped into one single 32 bit entry of the RX Buffer or the AHB Buffer. The table is valid within the following context:

  - Flash A or Flash B in Individual Flash Mode
  - All AHB data read commands with access size of 32 bit

Table 36-22. Byte Ordering in Individual Flash Mode

Serial Flash Byte Numbering	3	2	1	0
Buffer Entry Bit Position [31:0] (32 Bit data width)	[31:24]	[23:16]	[15:8]	[7:0]

Note

For IP Commands the read size can be given in number of bytes. If this number is not a multiple of 4, then the last buffer entry is not completely filled with the missing higher numbered bytes at undefined values.

For AHB Commands, reads, starting from an address not aligned to 32 bit boundaries, the requested bytes are given at the appropriate positions according to the AMBA AHB specification.

- **Byte Ordering in Parallel Flash Mode**

In Parallel Flash Mode each byte is combined out of 2 half bytes which are read or written in parallel from the two serial flash devices. The following tables shows how the flash content is separated into the half bytes and how the half bytes are assembled to the content of the QSPI_RBDR0 register.

Table 36-23. Serial Flash Device Half Byte Ordering

Serial Flash Device Byte #	Flash A Bit Position		Flash B Bit Position	
	[7:4]	[3:0]	[7:4]	[3:0]
0	fah0	fal0	fbh0	fbl0
1	fah1	fal1	fbh1	fbl1
2	fah2	fal2	fbh2	fbl2
3	fah3	fal3	fbh3	fbl3
4	fah4	fal4	fbh4	fbl4
5	fah5	fal5	fbh5	fbl5
6	fah6	fal6	fbh6	fbl6
7	fah7	fal7	fbh7	fbl7
8	fah8	fal8	fbh8	fbl8

The table entry naming reflects the half byte positioning in the serial flash devices:

- **<fa>**h0 means **Flash A**, <fb>h0 means Flash B.
- fa**<h>**0 means half byte in **high position**, fa<l>o means half byte in low position.
- fah**<0>** means **physical byte address 0** in the serial flash device, fal<1> means physical byte address 1 in the serial flash device.

Table 36-24. Byte Ordering in Parallel Flash Mode - RX Buffer

QSPI_SFAR[SFADR] set to 0x000_0000

Table continues on the next page...

Table 36-24. Byte Ordering in Parallel Flash Mode - RX Buffer (continued)

QSPI_RBDR0 **QSPI_ARDB0**	fal1	fbl1	fah1	fbh1	fal0	fbl0	fah0	fbh0
QSPI_RBDR1 **QSPI_ARDB1**	fal3	fbl3	fah3	fbh3	fal2	fbl2	fah2	fbh2
QSPI_SFAR[SFADR] set to 0x000_0001								
QSPI_RBDR0 **QSPI_ARDB0**	fal2	fbl2	fah2	fbh2	fal1	fbl1	fah1	fbh1
QSPI_RBDR1 **QSPI_ARDB1**	fal4	fbl4	fah4	fbh4	fal3	fbl3	fah3	fbh3

Note

For IP Commands the read size can be given in number of bytes. If this number is not a multiple of 4 the last buffer entry is not completely filled with the missing higher numbered bytes at undefined values.

Table 36-25. Byte Ordering in Parallel Flash Mode - TX Buffer*

QSPI_SFAR[SFADR] set to 0x000_0000								
QSPI_TBDR0	fal1	fbl1	fah1	fbh1	fal0	fbl0	fah0	fbh0
QSPI_TBDR1	fal3	fbl3	fah3	fbh3	fal2	fbl2	fah2	fbh2

* Applicable only for single I/O mode.

Table 36-26. Byte Ordering in Parallel Flash Mode - AHB Buffer

AHB Address **(32 Bit Access)**	fal1	fbl1	fah1	fbh1	fal0	fbl0	fah0	fbh0
AHB Address 0x800_0004 **(32 Bit Access)**	fal3	fbl3	fah3	fbh3	fal2	fbl2	fah2	fbh2

Note

For AHB Command read starting from an address not aligned to 32 bit boundaries or AHB access size smaller than 32 bit the requested bytes are given at the appropriate positions according to the AMBA AHB specification.

- **Buffer Entry Ordering for 64 Bit Read Access**

  For read access via the AHB interface 64 bit access is possible. Each 64 bit access reads 2 32 bit entries simultaneously. The ordering of these 32 bit entries within the 64 bit word is given in the following table.

Table 36-27. 64 Bit Read Access Buffer Entry Ordering

AHB Read Data Bit Position [63:0]	[63:32]	[31:0]
Buffer Entry #	Odd (1, 3, 5, ...)	Even (0, 2, 4, ...)

36.6.3.10 Normal Mode Interrupt and DMA Requests

The QuadSPI module has different flags that can only generate interrupt requests and one flag that can generate interrupt as well as DMA requests. The following table lists the eight conditions. Note that the flags mentioned in the table are related to the Flag Register (QSPI_FR).

Table 36-28. Interrupt and DMA Request Conditions

Condition	Flag(QSPI_FR)	DMA
Data Learn patttern Failure	DLPFF	-
TX Buffer Fill	TBFF	-
TX Buffer Underrun	TBUF	-
Illegal Instruction Error	ILLINE	-
RX Buffer Drain	RBDF	X
RX Buffer Overflow	RBOF	-
AHB Buffer Overflow	ABOF	-
AHB Sequence Error	ABSEF	-
AHB Illegal Transaction Error	AITEF	-
AHB Illegal Burst Size Error	AIBSEF	-
IP Command Usage Error	IUEF	-

Table continues on the next page...

Table 36-28. Interrupt and DMA Request Conditions (continued)

Condition	Flag(QSPI_FR)	DMA
IP Command Trigger during AHB Access Error	IPAEF	-
IP Command Trigger could not be executed Error	IPIEF	-
IP Access during AHB Grant Error	IPGEF	-
IP Command related Transaction Finished	TFF	-

Each condition has a flag bit in the Flag Register (QSPI_FR) and a Request Enable bit in the DMA Request Select and Enable Register (QSPI_RSER) . The RX Buffer Drain Flag (RBDF) has separate enable bits for generating IRQ and DMA requests. Note that not all flags have an individual IRQ line. Check the devices Interrupt Vector Table for more details.

- Transmit Buffer Fill Interrupt Request:

  The Transmit Buffer Fill IRQ indicates that the TX Buffer can accept new data. It is asserted if the QSPI_FR[TBFF] flag is asserted and if the corresponding enable bit (QSIP_RSER[TBFIE]) is set. Refer to TX Buffer Operation, for details about the assertion of the QSPI_FR[TBFF] flag.

  Aside from IRQ it is possible to handle TX Buffer fill by DMA. If the QSPI_RSER[TBFDE] bit is set, a DMA request will be triggered when the number of available space in the TX Buffer is more than the QSPI_TBCT[WMRK] valid entries and QSPI_SR[TXWA] is set. The application must set the environment appropriately (eg. the DMA controller) for the DMA transfer.

- Receive Buffer Drain Interrupt or DMA Request:

  The Receive Buffer Drain IRQ derived from the QSPI_FR[RBDF] flag indicates that the RX Buffer of the QuadSPI module has data available from the serial flash device to be read by the host. It remains set as long as the QSPI_RBSR[RXWE] bit is set. The QSPI_RSER[RBDIE] bit enables the related IRQ.

  Aside from the IRQ it is possible to handle RX Buffer drain by DMA. If the QSPI_RSER[RBDDE] bit is set, a DMA request will be triggered when the RX Buffer contains more than QSPI_RBCT[WMRK] valid entries.The application must set the environment appropriately (for example, the DMA controller) for the DMA transfers.

- Buffer Overflow/Underrun Interrupt Request:

The Buffer Overflow/Underrun IRQ is a combination of the following flags (all located in the QSPI_FR register with the related enable bits in the QSPI_RSER register):

- TBUF - TX Buffer Underrun, enabled by TBUIE
- RBOF - RX Buffer Overflow, enabled by RBOIE
- ABOF - AHB Buffer Overflow, enabled by ABOIE

  The Transmit Buffer Underrun indicates that an underrun condition in the TX Buffer has occurred. It is generated when a write instruction is triggered whilst the Tx Buffer is empty and the QSPI_RSER[TBUIE] bit is set.

  The Receive Buffer Overflow indicates that an overflow condition in the RX Buffer has occurred. It is generated when the RX Buffer is full, an additional read transfer attempts to write into the RX Buffer and the QSPI_RSER[RBOIE] bit is set.

  The AHB Buffer Overflow indicates that an overflow condition in the AHB Buffer has occurred. It is generated when the AHB Buffer is full, an additional read transfer attempts to write into the AHB Buffer and the QSPI_RSER[ABOIE] bit is set.

  The data from the transfers that generated the individual overflow conditions is ignored.

- Serial Flash Command Error Interrupt Request

  If the IPAEF, IPIEF, IPGEF or IUEF flags in the QSPI_FR are set, and the related interrupt enable bits in the QSPI_RSER are also set, then an interrupt is requested.

- Transaction Finished Interrupt Request

  The IP Command Transaction Finished IRQ indicates the completion of the current IP Command.It is triggered by the QSPI_FR[TFF] flag and is masked by the QSPI_RSER[TFIE] bit.

36.6.3.11 TX Buffer Operation

The TX Buffer provides the data used for page programming. For proper operation it is required to provide at least four entry in the TX Buffer prior to starting the execution of the page programming command. The application must ensure that the required number of data bytes is written into the TX Buffer fast enough as long as the command is executed without a TX Buffer overflow or underrun.

The QuadSPI module sets the QSPI_FR[TBFF] flag so long as the TX Buffer is not full and can accept more data.

When the QuadSPI module tries to pull data out of an empty TX Buffer the TX Buffer underrun is signaled by the QSPI_FR[TBUF] flag.The TX buffer underrun flag is also asserted when TX buffer contains less than 128 bits of data and QuadSPI module tries to pull out data from it. The current IP Command leading to the underrun condition is continued until the specified number of bytes has been sent to the serial flash device, in the underrun condition when QuadSPI module tries to pull out data of empty TX buffer, the data transferred is all F's i.e. once the underrun flag is set under this condition, it will return F's until the required number of bytes are not sent. This has been done to ensure that the software need not to erase whole sector after underrun, just reprogramming from failure point will serve the purpose. When this Sequence Command is finished, the QSPI_FR[TBFF] flag is asserted indicating that the Tx Buffer is ready to be written again.

The TX Buffer overflow isn't signaled explicitly, but the TX Buffer fill level can be monitored by the QSPI_TBSR[TRBFL] field.

Refer to TX Buffer Status Register (QuadSPI_TBSR) and Flag Register (QuadSPI_FR) for details about the TX Buffer related registers.

36.6.3.12 Address scheme

Earlier serial flash memories supported only 24-bit address space hence restricting the maximum memory size of the serial flash as 16 MB. The new memory specification supports two types of 32-bit addressing mode in addition to legacy 24-bit address mode. It also supports segregation of address programmed, into Row address and Column address of the Flash, as per requirement.

- **Extended Address Mode**

  In this mode, the legacy 24-bit commands are converted to accept 32-bit address commands. The flash memory needs to be configured for 32-bit address mode. Also, while programming the LUT sequence in QuadSPI for 32-bit mode, the ADDR and ADDR_DDR command should be programmed with 8’d32 as the operand value with QSPI_SFACR[CAS] programmed to 0. If a flash needs some bits of the address as its column address, then it must always considered that the total bits required by the Flash should not exceed 32, as maximum address supported by QuadSPI is 32 bits. Each of the memory vendors have a different way of enabling this mode (Refer to the memory specification from memory vendors). For example, the command B7h sent to Macronix flash will enable it for 32-bit address mode.

- **Extended Address register**

  In this mode, the upper 8-bit of the 32-bit address is provided by the Extended address register in the memory itself. The memory provides a specific register which is updated according to the address to be accessed. This effectively converts the legacy 24-bit address command into 32-bit address commands. The memories greater in size than 16 MB, consists of banks of 16 MB. The 8-bit written in the extended address register effectively enables a bank. For example in Spansion memory, when the extended address register is updated with a value of 0x01 with the help of the command 17h, it will open Bank1 of the memory. The consequent 24-bit address commands will lead to Bank1. The extended address register needs to be update with the respective value for access to other banks. This effectively converts the legacy 24-bit address command into 32-bit address commands.

- **Separation of address into row and column address**

  This mode has been introduced for flashes which needs addresses segregated into Row and Column. The value in QSPI_SFACR[CAS] defines the width of the column address required by a flash. The actual address to be provided will be derived from the incoming address in case of AHB initiated transactions and the value of SFAR in case of IPS initiated transactions , if QSPI_SFACR[CAS] is set to 0, else the actual address will take CAS into consideration. If QSPI_SFACR[CAS] is 3 then bits 26-3 of the address programmed are sent to flash as it page address in case flash is operating in 24bit mode and bits 2-0 are sent as its column address. If a flash requirement for column address is less than the number of pads in which address has to be sent than the remaining bits are appended with 0 by QuadSPI. The user must program the operand value in CADDR and CADDR_DDR command accordingly. It must be ensured that the total number of address bits request by flash as its page and column address must not be more than 32 bits.

- **Word addressable mode for Flash**

  This mode has been introduced for flashes which has word addressable memory i.e. each address of the flash contains one word (two bytes) of data. The QSPI_SFACR [WA] is set to 1 to enter this mode. QuadSPI internally divides the incoming address in the AHB bus or the address in the QSPI_SFAR to map it to a valid flash location. For example, if the incoming address is 0x2004, the controller re-maps this address to access the flash location 0x1002. If not in this mode, the incoming address 0x2004 will be mapped to flash location 0x2004.

36.6.3.13 OTFAD(On-the-fly AES Decryption) Support

If OTFAD is enabled in the system, any reads from the QuadSPI are first decrypted by the OTFAD engine and then returned on the AHB bus. In case OTFAD is enabled, the QuadSPI high priority feature as described in Flexible AHB buffers is disabled. If OTFAD is enabled, the prefetch never crosses the 1KB boundary.

36.7 Initialization/Application Information

This section provides the initialization and application information of the QuadSPI module.

36.7.1 Power Up and Reset

Note that the serial flash devices connected to the QuadSPI module may require special voltage characteristics of their inputs during power up or reset. It is the responsibility of the application to ensure this.

36.7.2 Available Status/Flag Information

This paragraph gives an overview of the different status and flag information available and their interdependencies for different use cases. Related registers are QSPI_SR and QSPI_FR. Refer to the related descriptions how to set up the QuadSPI module appropriately.

36.7.2.1 IP Commands

Refer to IP Configuration Register (QuadSPI_IPCR) for additional details not explicitly covered in this paragraph.

- **IP Commands - Normal Operation**

  Writing the QSPI_IPCR[SEQID] field triggers the execution of a new IP Command. Given that this is a legal command the QSPI_SR[IPACC] and the QSPI_SR[BUSY] bits are asserted simultaneously, immediately after the execution is started.

  When the instruction on the serial flash device has been finished these bits are de-asserted and the QSPI_FR[TFF] flag is set.

- **IP Commands - Error Situations**

Refer to Table 36-29 below.

36.7.2.2 AHB Commands

Refer to Section 1, Reading Serial Flash Data into the QuadSPI Module, in Flash Read for additional details not explicitly covered in this paragraph.

- **AHB Commands - Normal Operation**

  Memory mapped read access to a serial flash address not contained in the AHB Buffer, triggers the execution of an AHB Command. Given that this is a legal command the QSPI_SR[AHBACC] and the QSPI_SR[BUSY] bits are asserted simultaneously immediately after the execution is started. When the instruction on the serial flash device has been finished these bits are de-asserted.

- **IP Commands - Error Situations**

  Refer to Table 36-29 below.

36.7.2.3 Overview of Error Flags

The following table gives an overview of the different error flags in the QSPI_FR register and additional error-related details.

Table 36-29. Overview of QSPI_FR Error Flags

Error Category	Error Flag in QSPI_FR	Command Execution on Serial Flash Device TFF Behavior (in case of IP commands only)	Description
AHB Error Flag	ABSEF	Flash transaction is aborted	AHB sequence contains • WRITE instruction • WRITE_DDR instruction
AHB Error Flag	ABOF	Flash transaction continues until it finishes	Set when the module tried to push data into the AHB buffer that exceeded the size of the AHB buffer. Only occurs due to wrong programming of the QSPI_BUFxCR[ADATSZ].
AHB Error Flag	AIBSEF	Flash transaction is aborted	Total burst size of AHB transaction is greater than prefetch data size
AHB Error Flag	AITEF	Flash transaction is aborted	No response generated from QSPI to AHB bus in case of illegal transaction and the watchdog timer expires

Table continues on the next page...

Table 36-29. Overview of QSPI_FR Error Flags (continued)

Error Category	Error Flag in QSPI_FR	Command Execution on Serial Flash Device TFF Behavior (in case of IP commands only)	Description
Miscellaneous Error Flag	DLPFF	Flash transaction continues until it finishes	Set when DATA_LEARN instruction was encountered in a sequence but no sampling point was found for the data learning pattern.
Miscellaneous Error Flag	ILLINE	Flash transaction aborted	Illegal instruction Error Flag – Set when an illegal instruction is encountered by the controller in any of the sequences.
Command Arbitration Error	IPIEF	TFF not asserted in conjunction with that command	IP Command Error - caused when IP access is currently in progress (IP_ACC set) and • write attempt to QSPI_IPCR register. • write attempt to QSPI_SFAR register. • write attempt to QSPI_RBCT register.
Command Arbitration Error	IPAEF		• AHB Command already running, another IP Command could not be executed. • AHB Command already running, write attempt to QSPI_IPCR[SEQID] field.
Command Arbitration Error	IPGEF		• Exclusive access to the serial flash granted for AHB Commands, write attempt to QSPI_IPCR[SEQID] field.
IP Command Error	IUEF	—	• IP Command Usage Error
Buffer Related Error	RBOF	TFF is asserted on completion	• RX Buffer Overrun
Buffer Related Error	TBUF		• TX Buffer Underrun

Note that only the buffer related errors are related to a transaction on the external serial flash. All the other errors do not trigger an actual transaction.

36.7.2.4 IP Bus and AHB Access Command Collisions

There are two flags related to this topic, the QSPI_FR[IPAEF] and QSPI_FR[IPIEF]. Refer to sub-section "Reading Serial Flash Data into the QuadSPI Module" of Flash Read section, for a description of the flags and Command Arbitration , for details about possible command collisions.

36.7.3 Exclusive Access to Serial Flash for AHB Commands

It is possible that several masters need to access the serial flash device connected to the QuadSPI module separately, one master by triggering IP Commands and reading the RX Buffer (via RBDR*n* register) and the other masters by triggering AHB Commands (via ARDB*n* Registers). These two set of buffer (RBDR and ARDB Buffer) points to the same physical buffer.Refer to Figure 36-7 To avoid command collisions resulting in excessive latencies the QuadSPI module implements a request-handshake mechanism between the master triggering AHB Commands and the QuadSPI module allowing this specific master to request exclusive access to the serial flash device for AHB Commands. If this exclusive access is granted the execution of IP Commands is blocked. This resolves command collisions and excessive times where the AHB interface may be blocked.

If this capability is used in the device there is additional status and flag information available related to this mechanism. The QSPI_SR[AHBGNT] bit reflects the module-internal state that the exclusive access mentioned above is granted, any attempt to trigger an IP Command is rejected and results in the assertion of the QSPI_FR[IPGEF] flag. Refer to the descriptions of the related bit and flag for details.

It is within the responsibility of the application to set up the master using this mechanism appropriately, if used incorrectly no IP Commands at all can be triggered.

Two different cases can be distinguished:

36.7.3.1 RX Buffer Read via QSPI_ARDB Registers

In this case all masters share the AHB bus for RX Buffer as well as for AHB Buffer read. In this case the access to the AHB interface by the master triggering AHB Commands must be deferred until any pending IP Command has been finished **and** the RX Buffer readout has been finished as well. The QSPI ARDB Buffers access the Rx buffer i.e the data from the Rx Buffer is returned and no data from AHB Buffer is touched. This is the conservative use case, corresponding to the reset value 0 of the QSPI_RBCT[RXBRD] bit.

In this case the QSPI_SR[AHBGNT] bit is asserted not earlier than any running IP Command has been finished (QSPI_SR[IP_ACC] is 0), the RX Buffer has been read out completely (QSPI_RBSR[RDBFL] equal to 0) or no DMA read is pending (QSPI_SR[RXDMA] equal to 0 and Rx Buffer readout is via AHB(QSPI_RBCT[RXBRD]) equal to 1.

36.7.3.2 RX Buffer Read via QSPI_RBDR Registers

This is the preferred use case as an access to the AHB buffer (memory mapped flash) does not interfere with any IPS access to read the RBDR buffer. It is not possible that a pending AHB bus access triggered by an AHB Command stalls the AHB bus and blocks the RX Buffer readout since the RX Buffer is read via the IP bus based registers QSPI_RBDR0 to QSPI_RBDR15.

For this case it is recommended to program the QSPI_RBCT[RXBRD] bit to 1. The QSPI_SR[AHBGNT] bit is asserted immediately after any running IP Command has been finished (QSPI_SR[IP_ACC] is 0), the RX Buffer has been read out completely (QSPI_RBSR[RDBFL] equal to 0) or no DMA read is pending (QSPI_SR[RXDMA] equal to 0, allowing the master triggering AHB Commands to trigger AHB Commands as soon as possible without the need to wait for the RX Buffer readout to be finished.

36.7.4 Command Arbitration

In case of overlapping commands, the arbitration scheme is described in the following paragraphs under the assumption that the priority mechanism described in Exclusive Access to Serial Flash for AHB Commands is **not** used:

- During the execution of an IP Command, the running IP Command can't be terminated by issuing another IP Command or AHB Command. The QSPI_FR[IPIEF] flag is asserted when the host tries to write into the QSPI_IPCR register. When the host triggers an AHB Command (refer to sub-section "Reading Serial Flash Data into the QuadSPI Module" of Flash Read section, for details), this command is stalled until the currently running IP Command is finished.
- During the execution of an AHB Command, the running AHB Command can't be terminated by issuing an IP Command. The command is ignored and the QSPI_FR[IPAEF] flag is asserted. Refer to Flag Register (QuadSPI_FR) for the description of these flags.

  When another AHB Command is triggered the address of the memory mapped access is considered. If the requested address is currently read from the serial flash device, the running command is continued. If this is not the case the currently running

command is terminated and another AHB Command related to the requested address is executed. Refer to sub-section "Reading Serial Flash Data into the QuadSPI Module" of Flash Read section, for further details.

In case of coinciding commands the IP Command is triggered and the AHB Command is stalled until the IP Command has been finished (QSPI_SR[IP_ACC] has been deasserted).

The IP Commands ignored in case of command collision will not result in the assertion of the QSPI_FR[TFF] flag.

36.7.5 Flash Device Selection

Regardless of the SFM Command (IP or AHB) the access mode is selected by specifying the 32 bit address value for the following SFM Command.

For IP Commands the access mode is selected with the address programmed into the QSPI_SFAR register. Refer to Serial Flash Address Register (QuadSPI_SFAR) for details.

For AHB Commands the access mode is determined by the memory mapped address which is accessed Refer to AMBA Bus Register Memory Map for details.

36.7.6 DMA Usage

For the complete description of the DMA module refer to the related DMA Controller chapter. In this paragraph only the details specific to the DMA usage related to the QuadSPI module are given.

36.7.6.1 DMA Usage in Normal Mode

36.7.6.1.1 Bandwidth considerations

Careful consideration of the throughput rate of the entire chain (serial flash -> AHB bus / IP Bus -> DMA controller) involved in the read/write data process is essential for proper operation. Such analysis must take into account not only the data rate provided by the serial flash but also the data rate of the AHB bus and the performance of the DMA controller in reading/writing data from/to the RX/TX buffer.

Two figures must match for proper operation, that means that the data rate provided by the serial flash device must not exceed the average RX Buffer readout data rate. Otherwise, the longer this state persists, a RX Buffer overflow will result. Similarly, the data consumed by the serial flash device must not exceed the average TX buffer fill rate. If this persists, it would eventually lead to an underrun.

AHB Bus Side (data read):

The total number of bus cycles for each DMA Minor Loop completion is added from the following components:

- Overhead for each minor loop, given by DMA controller: Assume 10 cycles
- Overhead due to clock domain crossing: Assume 2 cycles
- Number of bus clock cycles required for 8 bytes (64 bit read size): Assume 2 cycles (read/write sequence of DMA controller)

Note that the size of the minor loop is determined by the size of the QSPI_RBCT[WMRK] field, therefore the overhead given above distributes among (QSPI_RBCT[WMRK]+1)/2 read accesses of 64 bit each.

The following table gives some examples for typical use cases:

Table 36-30. Access Duration Examples - Bus Clock Side

QSPI_RBCT[WMRK]	Number of Bytes per DMA Loop [1]	Number of Bus Clock cycles for DMA Minor Loop	Time Duration of DMA Minor Loop for 120Mhz Bus clock Frequency
0	4	12+2 = 14	~117ns
1	8	12+2 = 14	~117ns
3	16	12+4 = 16	~133ns
7	32	12+8 = 20	~167ns
11	48	12+12 = 24	~200ns

1. DMA Loop means one Minor Loop Completion which is equivalent to one.

NOTE

The table figure represents ideal scenario, actual performance will depend on how the system is integrated.

Serial Flash Device Side (data read):

The number of serial flash cycles can be determined in the following way:

- Number of serial flash clock cycles required to read 4 bytes, corresponding to one RX Buffer entry (setup of command and address not considered): 2 cycles for Quad DDR mode instructions in Parallel Flash Mode, 2 cycles for Octal DDR mode (Hyperflash) in individual flash mode, 4 cycles for Quad (SDR) mode instruction in

parallel flash mode or Dual IO DDR mode instruction in parallel flash mode, 8 cycles for Quad Mode (SDR) instructions in Individual Flash Mode etc.
- Overhead due to clock domain crossing : 1 cycle.

The following table lists the number of clock cycles required to read the data from the serial flash corresponding to the different settings of the QSPI_RBCT[WMRK] field:

Table 36-31. Access Duration Examples - Serial Flash side

QSPI_RBCT[WMRK] setting	Num Bytes per DMA Loop [1]	Num SCKFx for 80MHz SCKFx			Time duration of Flash data readout for 80MHz SCKFx (~12.5ns period)		
		IFM [2] Quad	IFM Quad DDR	PFM [3] Quad DDR/ IFM Octal DDR	IFM Quad	IFM Quad DDR	PFM Quad DDR
0	4	8	4	2	~100ns	~50ns	~25ns
1	8	16	8	4	~200ns	~100ns	~50ns
3	16	32	16	8	~400ns	~200ns	~100ns
7	32	64	32	16	~800ns	~400ns	~200ns
11	48	96	48	24	~1200ns	~600ns	~300ns

1. DMA Loop means one Minor loop completion which is equivalent to one Major Loop iteration.
2. Individual flash mode.
3. Parallel flash mode.

NOTE

The table figure represents ideal scenario, actual performance will depend on how the system is integrated.

From the examples given in the two tables above, it can be seen that depending on the relationship between the Bus clock and Serial flash clock frequencies, there are settings possible where the serial flash provides the read data faster than the AHB bus can read out the RX buffer. In the above tables, it is the case of PFM Quad DDR mode with Watermark up to 3 and other cases. In these cases, the RX buffer data keeps accumulating over time and will eventually overflow. To avoid RX Buffer overflow, the data transaction size should be small enough.

A complementary example would be when the watermark is set to be too high. In such a case, the time taken by the DMA to read out the RX buffer entries should be smaller than the time taken by the controller to push in the remaining entries in the buffer.

IPS Bus Side (data write):

The total number of bus cycles for each DMA Minor Loop completion is added from the following components:

- Overhead for each minor loop, given by DMA controller: Assume 10 cycles

- Overhead due to clock domain crossing: Assume 2 cycles
- Number of bus clock cycles required for 16 bytes (128 bit write size): Assume 4 cycles (read/write sequence of DMA controller)

Note that the size of the minor loop is determined by the size of the QSPI_TBCT[WMRK] field, therefore the overhead given above distributes among (QSPI_TBCT[WMRK]+1) write accesses of 32 bit each.

The following table gives some examples for typical use cases:

Table 36-32. Access Duration Examples - Bus Clock Side

QSPI_TBCT[WMRK]	Number of Bytes per DMA Loop [1]	Number of Bus Clock cycles for DMA Minor Loop	Time Duration of DMA Minor Loop for 80Mhz Bus clock Frequency
3	16	12+4 = 16	~200ns
7	32	12+8 = 20	~250ns
11	48	12+12 = 24	~300ns
15	64	12+16 = 28	~350ns

1. DMA Loop means one Minor Loop Completion which is equivalent to one.

NOTE

The table figure represents ideal scenario, actual performance will depend on how the system is integrated.

Serial Flash Device Side (data write):

The number of serial flash cycles can be determined in the following way:

- Number of serial flash clock cycles required to write 16 bytes, corresponding to four TX Buffer entry(setup of command and address not considered): 8 cycles for Octal DDR mode (Hyperflash) instructions in Individual Flash Mode, 32 cycles for Quad SDR writes in individual flash mode, 64 cycles in single io SDR writes in parallel flash mode.
- Overhead due to clock domain crossing : 1 cycle.

The following table lists the number of clock cycles required to read the data from the serial flash corresponding to the different settings of the QSPI_TBCT[WMRK] field:

Table 36-33. Access Duration Examples - Serial Flash side

QSPI_TBCT[WMRK] setting	Num Bytes per DMA Loop [1]	Num SCKFx			Time duration for consuming data at Flash interface 100MHz SCKFx (10ns period)[2]			Time for fifo to get empty[3]		
		IFM [4] Quad	IFM Octal DDR	[5] Single IO SDR Mode	IFM Quad	IFM Octal DDR	PFM Single IO SDR	IFM Quad	IFM Octal DDR	PFM Single IO SDR
3	16	32	8	64	320ns	80ns	640ns	2240ns	560ns	4480ns
7	32	64	16	128	640ns	160ns	1280ns	1920ns	480ns	3840ns
15	64	128	32	256	1280ns	320ns	2560ns	1280ns	320ns	2560ns

1. DMA Loop means one Minor loop completion which is equivalent to one Major Loop iteration.
2. Not all flash devices support writes at 100Mhz. Please refer to the flash datasheet for the actual page program frequency supported.
3. The assumption for these timings is that the TX Fifo was full when the transaction was initiated
4. Individual flash mode.
5. Parallel flash mode.

NOTE

The tables mentioned above are only examples which must be correlated with the DMA in the system.

From the examples given in the two tables above for TX fifo, it can be seen that depending on the relationship between the Bus clock and Serial flash clock frequencies, there are settings possible where the serial flash consumes data faster than the IPS bus can write data in TX buffer. In these cases, a TX buffer underrun situation will occur. To avoid TX Buffer underrun, the data transaction size should be large enough.

36.7.7 Parallel mode

QuadSPI can access two flashes in parallel. This increases the throughput of the QuadSPI by two times. Only read operations and x1 mode write are allowed in parallel mode. In case a write transaction is initiated in with mode than one pad in parallel mode, QSPI_FR[IUEF] is set. When dual die flashes are accessed in parallel mode, it is mandatory for flash A1 to be of the same size as B1 and A2 to be of the same size as B2. The following figure shows how QuadSPI maps the incoming addresses to the different flashes connected on board.

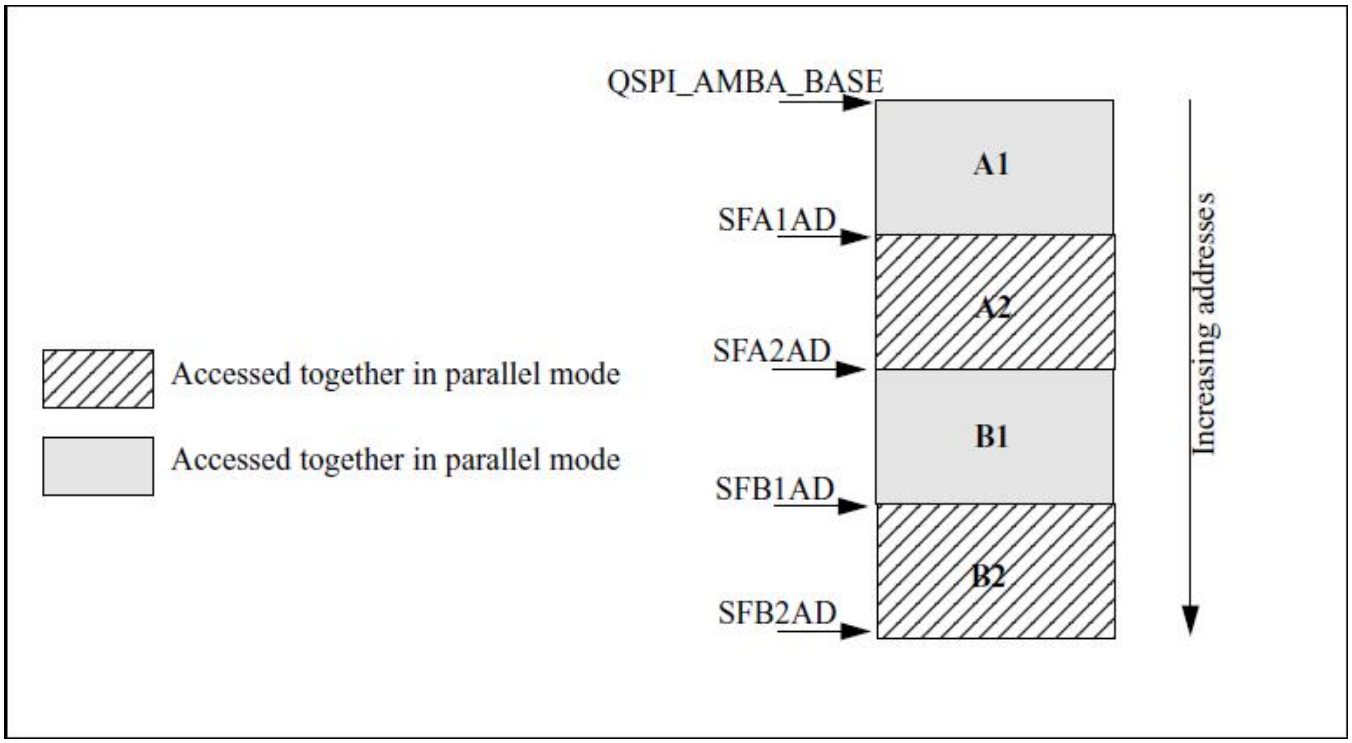


Figure 36-8. Flash addressing

An example programming for parallel mode access is given below (flash sizes are assumed to be 256MB):

- QSPI_AMBA_BASE - 0x10000000
- QSPI_SFA1AD[TPADA1] - 0x20000000
- QSPI_SFA2AD[TPADA2] - 0x30000000
- QSPI_SFB1AD[TPADB1] - 0x40000000
- QSPI_SFB2AD[TPADB2] - 0x50000000

In order to access the first location of A1/B1 pair, the incoming address should be 0x10000000. QSPI_AMBA_BASE is subtracted from this address and the result is divided by two. Therefore, address provided to flash A1 and B1

Flash Address = (Memory mapped address - QSPI_AMBA_BASE)/2

For Memory Mapped address:

- 0x10000000, flash address: 0x0 (Or, the first address of flash A1 and B1)
- 0x10000004, flash address: 0x2
- 0x10000008, flash address: 0x4 etc.

Similarly, in order to access the first location of A2/B2 pair, the incoming address should be 0x30000000.

Flash Address = (Memory mapped address - SFA2AD)/2

For Memory Mapped address:

- 0x30000000, flash address: 0x0 (Or, the first address of flash A2 and B2)
- 0x30000004, flash address: 0x2
- 0x30000008, flash address: 0x4 etc.

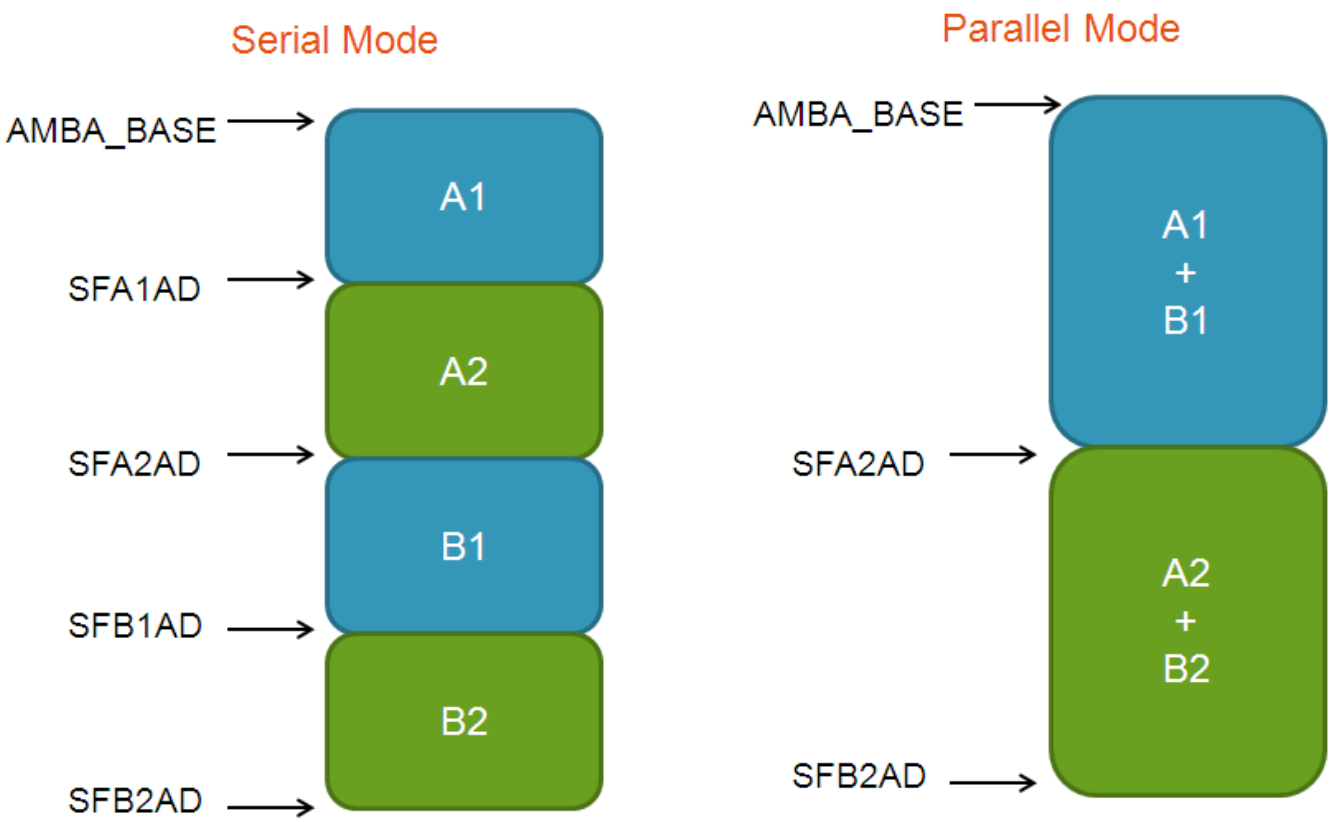


Figure 36-9. Memory map - Serial and Parallel

36.8 Byte Ordering - Endianness

QuadSPI provides support for swapping the flash read/write data based on the configuration of the QSPI_MCR[END_CFG]. By default the data is always returned in 64 bit LE format on the AHB bus and 32 bit LE format on the IPS interface when read via the RX buffer and written in 32 bit LE format when written via the TX buffer.

The table(QSPI_MCR[END_CFG]) below shows the complete bit ordering. BE signifies Big Endian which means the high order bits of the associated data vectors are associated with low order address positions. LE signifies Little Endian which means the lower order bits of the associated data vectors are associated with low order address positions.Refer to figure Figure 36-7

Table 36-34. QSPI_MCR[END_CFG]

00	64 bit BE
01	32 bit LE
10	32 bit BE
11	64 bit LE

The tables below (Byte ordering configuration in AHB) and (Byte ordering configuration in IPS) show how this configuration is implemented in QSPI AHB and IPS interfaces respectively. B in the table signifies Byte and the index 1-8 refers to the byte position i.e. 1 refer to bits[7:0], 8 refer to bits[63:56] and so on.

Table 36-35. Byte ordering configuration in AHB

64 bit BE	B1	B2	B3	B4	B5	B6	B7	B8
64 bit LE	B8	B7	B6	B5	B4	B3	B2	B1
32 bit BE	B5	B6	B7	B8	B1	B2	B3	B4
32 bit LE	B4	B3	B2	B1	B8	B7	B6	B5

Table 36-36. Byte ordering configuration in IPS

32BE	B1	B2	B3	B4
32LE	B4	B3	B2	B1

The examples below show the byte ordering in 64 bit BE configuration for AHB Buffer and 32 bit BE for TX/RX Buffer:

36.8.1 Programming Flash Data

CPU write instructions to the QSPI_TBDR register like

- Write QSPI_TBDR -> 0x01_02_03_04
- Write QSPI_TBDR -> 0x05_06_07_08

result in the following content of the TX Buffer:

Table 36-37. Example of QuadSPI TX Buffer

TX Buffer Entry	Content
0	32'h01_02_03_04
1	32'h05_06_07_08

Programming the TX Buffer into the external serial flash device results in the following byte order to be sent to the serial flash:

- 01…02…03…04…05…06…07…08

36.8.2 Reading Flash Data into the RX Buffer

Reading the content from the same address provides the following sequence of bytes, identical to the write case:

- 01…02…03…04…05…06…07…08

This results in the RX Buffer filled with:

Table 36-38. Resulting RX Buffer Content

RX Buffer Entry	Content
0	32'h01_02_03_04
1	32'h05_06_07_08

36.8.2.1 Readout of the RX Buffer via QSPI_RBDRn

The RX Buffer content appears at CPU read access via the Peripheral bus interface in the following order:

- Read QSPI_RBDR0 <- 0x01_02_03_04
- Read QSPI_RBDR1 <- 0x05_06_07_08

36.8.2.2 Readout of the RX Buffer via ARDBn

The RX Buffer content appears at read access on the AMBA AHB interface at the QuadSPI module boundary:

- (1a): 32 Bit Access: Read QSPI_ARDB0 <- 0x01_02_03_04
- (2a): 32 Bit Access: Read QSPI_ARDB1 <- 0x05_06_07_08
- (1b/2b): 64 Bit Access: Read QSPI_ARDB0 <- 0x01_02_03_04_05_06_07_08

36.8.3 Reading Flash Data into the AHB Buffer

Reading the content from the same address as it was written to provides the following sequence of bytes, identical to the write case:

- 01…02…03…04…05…06…07…08

This results in the AHB Buffer filled with:

Table 36-39. Resulting AHB Buffer Content

AHB Buffer Entry	Content
0	64'h01_02_03_04_05_06_07_08

36.8.3.1 Readout of the AHB Buffer via Memory Mapped Read

The AHB Buffer content appears at read access on the AMBA AHB interface at the QuadSPI module boundary:

- (1a): 32 Bit Read Access: <- 0x01_02_03_04
- (2a): 32 Bit Read Access: <- 0x05_06_07_08
- (1/2): 64 Bit Read Access: <- 0x01_02_03_04_05_06_07_08

36.9 Serial Flash Devices

Several different vendors make flash devices with a QuadSPI interface. At present there is no set standard for the QuadSPI instruction set. Most common commands currently have the same instruction code for all vendors, however some commands are unique to specific vendors. Some example sequences are provided below.

36.9.1 Example Sequences

This section provides the example sequences of the QuadSPI module.

Table 36-40. Exit 4 x I/O Read Enhance Performance Mode (XIP) (Macronix) and Read Status

INSTR	PAD	OPERAND	COMMENT
CMD	0x0	0xEB	4xIO Read Command
ADDR	0x2	0x18	24 Bit address to be send on 4 pads
MODE	0x2	0x00	2 mode cycles (exit XIP)
DUMMY	0x0	0x04	4 dummy cycles
READ	0x2	0x08	Read 64 bits
CMD	0x0	0x05	Read Status register
READ	0x0	0x01	Status register data
STOP	0x0	0x00	STOP, Instruction over

36.9.1.1 Read Command (Spansion Hyperflash)

This section provides the read command sequences (Spansion Hyperflash) of the QuadSPI module.

Table 36-41. Read Command (Spansion Hyperflash)

INSTR	PAD	OPERAND	COMMENT
CMD_DDR	0x3	0xA0	Read command with continuous burst type
ADDR_DDR	0x3	0x18	24 bit row address
CADDR_DDR	0x3	0x10	16 bit column address with lower 3 bits valid rest 0
DUMMY	0x3	0x0F	15 dummy cycles
READ_DDR	0x3	0x4	32 bit data read on 8 pads
STOP	0x3	0x00	STOP, Instruction over

Hyperflash is a word addressable flash i.e. each address accesses a word wide (2 bytes) data value, the software should ensure that when Hyperflash is connected to the controller, the QSPI_SFACR [WA] bit must be set. If this bit is set the controller remaps a byte addressable access to a word addressable access.

36.9.1.2 Read Status Register(Spansion Hyperflash)

This section provides the read status register of the QuadSPI module.

Table 36-42. Read Status register (Spansion Hyperflash)

INSTR	INSTR SEQUENCE	PAD	OPERAND	COMMENT
CMD_DDR	Read Pre Comman	0x3	0x00	Write command with wrapped burst type.
ADDR_DDR		0x3	0x18	24 bit row address(0000AAh)
CADDR_DDR		0x3	0x10	16 bit column address with lower 3 bits valid rest 0(0005h),treated as command
CMD_DDR		0x3	0x00	Write command with wrapped burst type
CMD_DDR		0x3	0x70	Write data to be sent to flash as pre-command
CMD_DDR	Command phase (fourth/final chip select phase)	0x3	0xA0	Read command with continuous burst type
ADDR_DDR		0x3	0x18	24 bit row address
CADDR_DDR		0x3	0x10	16 bit column address with lower 3 bits valid rest 0
DUMMY		0x3	0x0F	15 dummy cycles
READ_DDR		0x3	0x4	32 bit data read on 8 pads
STOP		0x3	0x00	STOP, Instruction over

36.9.1.3 Word Program (Spansion Hyperflash)

This section provides the Word Program (Spansion Hyperflash) of the QuadSPI module.

Table 36-43. Word Program (Spansion Hyperflash)

INSTR	INSTR SEQUENCE	PAD	OPERAND	COMMENT
CMD_DDR	Unlock Sequence 1 (first chip select phase)	0x3	0x00	Write command with wrapped burst type
CMD_DDR		0x3	0x00	8 bit address 00h treated as command
CMD_DDR		0x3	0x00	8 bit address 00h treated as command
CMD_DDR		0x3	0xAA	8 bit address AAh treated as command

Table continues on the next page...

Table 36-43. Word Program (Spansion Hyperflash) (continued)

CADDR_DDR		0x3	0x10	16 bit column address with lower 3 bits valid rest 0(0005h),treated as command
CMD_DDR		0x3	0x00	Write command with wrapped burst type.
CMD_DDR		0x3	0xAA	Write data to be sent to flash as pre-command.
CMD_DDR	Unlock Sequence 2 (second chip select phase)	0x3	0x00	Write command with wrapped burst type
CMD_DDR		0x3	0x00	8 bit address 00h treated as command
CMD_DDR		0x3	0x00	8 bit address 00h treated as command
CMD_DDR		0x3	0x55	8 bit address 55h treated as command
CADDR_DDR		0x3	0x10	16 bit column address with lower 3 bits valid rest 0(0002h),treated as command
CMD_DDR		0x3	0x00	Write command with wrapped burst type
CMD_DDR		0x3	0x55	Write data to be sent to flash as pre-command
CMD_DDR	Program setup phase (third chip select phase)	0x3	0x00	Write command with wrapped burst type
CMD_DDR		0x3	0x00	8 bit address 00h treated as command
CMD_DDR		0x3	0x00	8 bit address 00h treated as command
CMD_DDR		0x3	0xAA	8 bit address AAh treated as command
CADDR_DDR		0x3	0x10	16 bit column address with lower 3 bits valid rest 0(0005h),treated as command
CMD_DDR		0x3	0x00	Write command with wrapped burst type
CMD_DDR		0x3	0xA0	Write data to be sent to flash as pre-command
CMD_DDR	Command phase (fourth/final chip select phase)	0x3	0x00	Write command with wrapped burst type
ADDR_DDR		0x3	0x18	24 bit row address
CADDR_DDR		0x3	0x10	16 bit column address with lower 3 bits valid rest 0
WRITE_DDR		0x3	0x2	2 bytes data written on 8 pads (D1D2)

Table continues on the next page...

Table 36-43. Word Program (Spansion Hyperflash) (continued)

STOP		0x3	0x00	STOP, Instruction over

36.9.1.4 Fast Read Sequence (Macronix/Numonyx/Spansion/ Winbond)

The following table shows the fast read sequence for Macronix/Numonyx/Spansion/ Winbond flashes.

Table 36-44. Fast Read sequence

Instruction	Pad	Operand	Comment
CMD	0x0	0x0B	Fast Read command = 0x0B
ADDR	0x0	0x18	24 Addr bits to be sent on one pad
DUMMY	0x0	0x08	8 Dummy cycles
READ	0x0	0x04	Read 32 Bits on one pad
JMP_ON_CS	0x0	0x00	Jump to instruction 0 (CMD)

36.9.1.5 Fast Dual I/O DT Read Sequence (Macronix)

The following table shows the Fast Dual I/O DT read sequence for Macronix flashes.

Table 36-45. Fast Dual I/O DT Read sequence

Instruction	Pad	Operand	Comment
CMD	0x0	0xBD	Fast Dual I/O DT read command = 0xBD
ADDR_DDR	0x1	0x18	24 Addr bits to be sent on 2 pads in DDR mode
MODE4_DDR	0x1	0x00	P2=P0 or P3=P1 is necessary. Refer to Macronix datasheet for details. One clock cycle for mode.
DUMMY	0x0	0x06	6 Dummy cycles
READ_DDR	0x1	0x04	Read 32 Bits on 2 pads in DDR mode
JMP_ON_CS	0x0	0x00	Jump to instruction 0 (CMD)

36.9.1.6 Fast Read Quad Output (Winbond)

The following table shows the Fast read quad output sequence for Winbond memories

Table 36-46. Fast Read Quad output sequence

Instruction	Pad	Operand	Comment
CMD	0x0	0x6B	Fast read quad output command = 0x6B
ADDR	0x0	0x18	24 Addr bits to be sent on 1 pad
DUMMY	0x0	0x08	8 Dummy cycles
READ	0x2	0x04	Read 32 Bits on 4 pads
JMP_ON_CS	0x0	0x00	Jump to instruction 0 (CMD)

36.9.1.7 4 x I/O Read Enhance Performance Mode (XIP) (Macronix)

The following table shows the 4 x I/O Read Enhance Performance Mode for Macronix flashes. The enhanced performance mode is also known as XIP mode.

Table 36-47. Fast Read Quad output sequence

Instruction	Pad	Operand	Comment
CMD	0x0	0xEB	4xI/O Read command = 0xEB
ADDR	0x2	0x18	24 Addr bits to be sent on 4 pads
MODE	0x2	0xA5	2 mode cycles
DUMMY	0x0	0x04	4 Dummy cycles
READ	0x2	0x04	Read 32 Bits on 4 pads
JMP_ON_CS	0x0	0x01	Jump to instruction 1 (ADDR)

When in XIP mode the software should ensure that all the flashes connected to the controller are in XIP mode. As a part of initializing the controller, all the flashes may be enabled with XIP by carrying out dummy reads.

36.9.1.8 Dual Command Page Program (Numonyx)

The following table shows the Dual command page program sequence for Numonyx flashes.

Table 36-48. Dual Command Page Program sequence

Instruction	Pad	Operand	Comment
CMD	0x1	0x02	Dual command page program = 0x02 on 2 pads
ADDR	0x1	0x18	24 Addr bits to be sent on 2 pads
WRITE	0x1	0x20	Write 32 Bytes on 2 pads
STOP	0x0	0x00	STOP, Instruction over

36.9.1.9 Sector Erase (Macronix/Spansion/Numonyx)

The following table shows the Sector erase sequence for Macronix/Spansion/Numonyx flashes

Table 36-49. Sector Erase sequence

Instruction	Pad	Operand	Comment
CMD	0x0	0xD8	Sector erase command = 0xD8
ADDR	0x0	0x18	24 Addr bits to be sent on 1 pad
STOP	0x0	0x00	STOP, Instruction over

36.9.1.10 Read Status Register (Macronix/Spansion/Numonyx/ Winbond)

The following table shows the Read status register sequence for Macronix/Spansion/ Numonyx/Winbond flashes.

Table 36-50. Read Status Register Sequence

Instruction	Pad	Operand	Comment
CMD	0x0	0x05	Read status register command = 0x05
READ	0x0	0x01	Read status register data
STOP	0x0	0x00	STOP, Instruction over

36.9.1.11 Data Learn Instruction Sequence

The following table shows the data learn sequence for 4 I/O flash.

Table 36-51. Data learn Instruction sequence (4 I/O)

Instruction	Pad	Operand	Comment
CMD	0x0	0x6B	Fast Read Quad command = 0x6B
ADDR_DDR	0x2	0x18	24 address bits in DDR mode to be sent on four pads
DUMMY	0x2	0x08	8 Dummy cycle
DATA_LEARN	0x2	0x01	1 Byte data learn
READ_DDR	0x2	0x06	Read 6 bytes in 4 pads
JMP_ON_CS	0x0	0x00	Jump to Inst 0 (CMD)

The following table shows the data learn sequence for 8 I/O (Spansion Hyperflash) flash.

Table 36-52. Data learn Instruction sequence (8 I/O)

Instruction	Pad	Operand	Comment
CMD_DDR	0x3	0xAO	Read command for Hyperflash
ADDR_DDR	0x3	0x18	24 bit row address[1]
CADDR_DDR	0x3	0x10	16 bit column address
DUMMY	0x3	0x0F	15 cycle dummy
DATA_LEARN	0x3	0x01	1 byte data learn
READ_DDR	0x3	0x08	Read 8 bytes in 8 pads
STOP	0x3	0x00	STOP, instruction over

1. Address needs to be aligned i.e. No latency should be there between the RWDS edges.

36.9.2 Dual Die Flashes

Certain serial flash vendors provide dual-die packages which are essentially two devices (dies) stacked within the same package to increase the memory capacity of a single package. These two devices within a package share the same data and clock pins, but have individual Chip Selects. QuadSPI controller provides support for two dual-die packages to be connected simultaneously. The figure below shows the two dual-die packages and the naming conventions used in this document. For simplicity, the data pins are shown to be unidirectional.

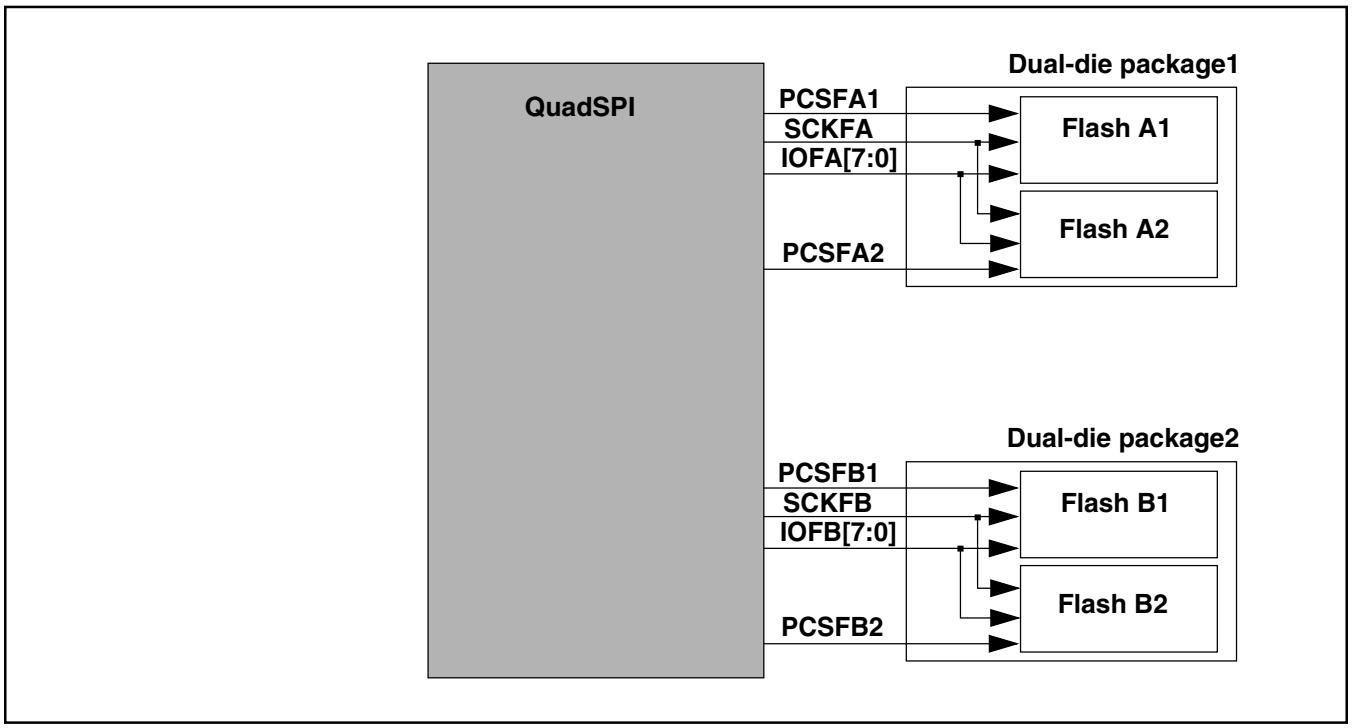


Figure 36-10. Dual-die support

Since the two devices within one package share the same i/o pads, they cannot function in parallel mode. Software should ensure that when QuadSPI is configured in parallel mode the two selected flash devices are from different dual-die packages.

36.9.3 Boot initialization sequence

The following are the recommended sequence of steps for booting from QuadSPI:

- System out of reset and flash available (300us)
- Clocks still at very low frequency. Clock tree configured, I/O pins configured. First request sent to QuadSPI for address 0x0 of flash.
- The reset command sequence in QuadSPI has 0x03 (basic read command) which is applicable to all flashes at < 50MHz serial flash clock
- The first few bytes of data is read from the flash which contains the following information:
  - The total sizes of all the flashes connected on board
  - Whether DDR mode supported
  - Frequency of DDR operation

- Continuous mode entry sequence
- 24bit or 32bit addressing (assuming 24bit for first accesses)

- All the serial flashes are configured
  - Quad Mode enabled
  - Dummy reads to enter into XIP
- QuadSPI is configured
  - Parallel enable set
  - LUT configured for highest performance reads
  - DDR mode enabled (if applicable)
  - Buffers configured
- Serial flash clock frequency increased.
- Boot reads happen in parallel, DDR enabled, quad output mode @66MHz.

36.9.4 Serial Flash Clock Frequency Limitations

Certain commands of some serial flash devices are limited in the frequency applied to the serial flash device on command execution. In order to support these commands without having to recalibrate the module clocks, the the serial flash device clock can be divided by 2 (half speed) by setting the QSPI_SMPR[HSENA] bit. The SCLK will return to full speed once the the QSPI_SMPR[HSENA] bit is cleared.

36.10 Sampling of Serial Flash Input Data

36.10.1 Basic Description

QuadSPI is used to read data from the serial flash device. Depending on the actual implementation, there is a delay between the internal clocking in the QuadSPI module and the external serial flash device. Refer to the following figure for an overview of this scheme.

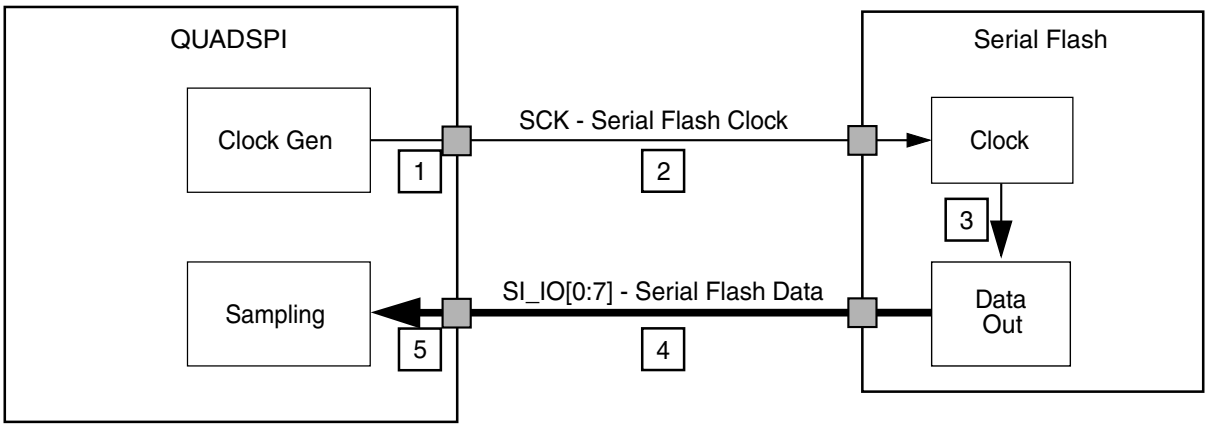


Figure 36-11. Serial Flash Sampling Clock Overview

The rising edge of the internal reference clock is taken as timing reference for the data output of the serial flash. After a time of $t_{Del,total}$ the data arrives at the internal sampling stage of the QuadSPI module. According to the Serial Flash Sampling Clock Overview figure, the following parts of the delay chain contribute to $t_{Del,total}$:

1. Output delay of the serial flash clock output of the device containing the QuadSPI module
2. Wire delay of application/PCB from the device containing the QuadSPI module to the external serial flash device
3. Clock to data out delay of the external serial flash device, including input and output delays
4. Wire delay of application/PCB from the external serial flash device to the device containing the QuadSPI module
5. Device delay corresponding to the input data

NOTE

The amount of total delay $t_{Del,total}$ is specific to the characteristics of the actual implementation. Also, the serial flash device clock (SCK) is inverted with respect to the QuadSPI internal reference clock.

36.10.2 Supported read modes

The table below provides an overview of QuadSPI read modes.

Table 36-53. QuadSPI read modes

Read modes			QuadSPI_MCR[DDR_EN]	QuadSPI_MCR[DQS_EN]	Data learning support	For more information
SDR mode	Internal sampling (N/1, I/1)		0	0	No	Internal sampling
	DQS sampling method	Internally generated DQS	0	1	No	Internally generated DQS
		External DQS	0	1	No	External DQS
DDR mode	Internal sampling (4x method)		1	0	Yes	Internal sampling (4x sampling method)
	DQS sampling method	Internally generated DQS	1	1	Yes	Internally generated DQS
		External DQS	1	1	Yes	External DQS

36.10.2.1 SDR mode

Most flash memories operate in single data rate (SDR) mode. In SDR mode, the data is transferred only on one edge of the clock signal. The SDR serial flash memories sample the incoming data on the rising edge of serial flash clock and drive the output data on the falling edge of the serial flash clock.

36.10.2.1.1 Internal sampling

QuadSPI uses different edges of the internal reference clock for sampling the input data in SDR mode.

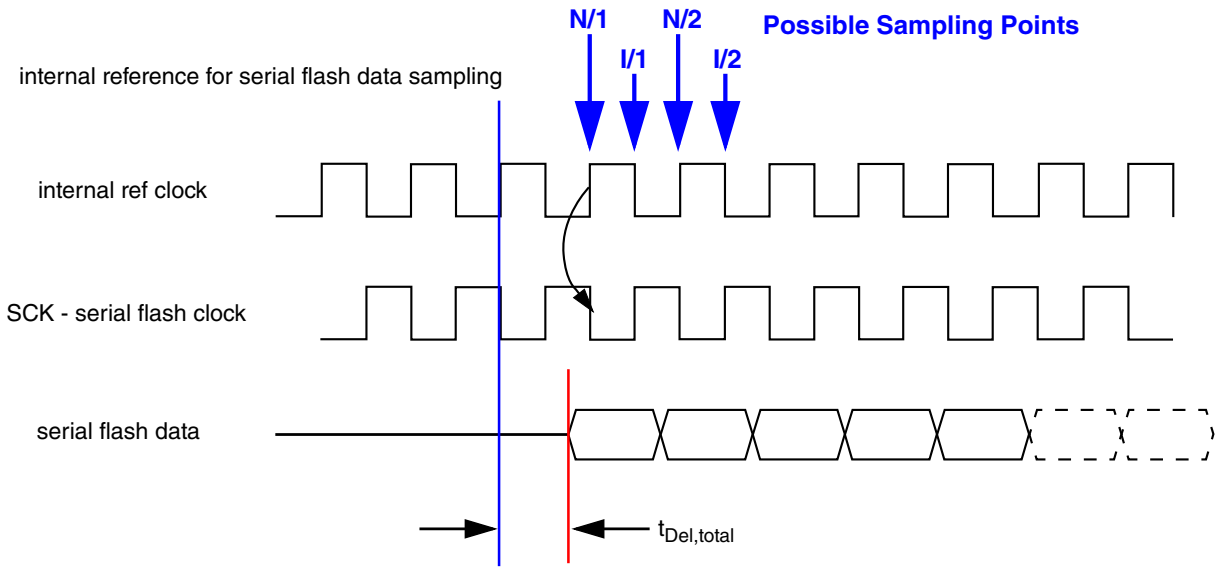


Figure 36-12. Internal sampling in SDR mode

The possible points in time for sampling incoming data are denoted as N/1, I/1, N/2 and I/2 above. The sampling point relevant for the internal sampling is configured in the QSPI_SMPR register. Refer to Sampling Register (QuadSPI_SMPR) for details. The following table gives an overview of the available configurations for the commands running at regular (full) speed:

Table 36-54. Sampling Configuration

Sampling Point	Description	Delay [FSDLY] [HSDLY]	Phase [FSPHS] [HSPHS]	QSPI_SMPR for Full Speed Setting[1]
N/1	sampling with non-inverted clock, 1 sample delay	0	0	0x0000000x
I/1	sampling with inverted clock, 1 sample delay	0	1	0x0000002x
N/2	sampling with non-inverted clock, 2 samples delay	1	0	0x0000004x
I/2	sampling with inverted clock, 2 samples delay	1	1	0x0000006x

1. 'x' is not considered here

Depending on the actual delay and the serial flash clock frequency, the appropriate sampling point can be chosen. The following remarks should be considered when selecting the appropriate setting:

- Theoretically there should be two settings possible to capture the correct data, since the serial flash output is valid for 1 clock cycle, disregarding rise and fall times and timing uncertainties.

- Depending on the timing uncertainties, it may turn out in actual applications that only one possible sample position remains. This is subject to careful consideration depending on the actual implementation.
- The delay $t_{Del,total}$ is an absolute size to shift the point in time when the serial flash data get valid at the QuadSPI input.
- For decreasing frequency of the serial flash clock the distance between the edges increases. So for large differences in the frequency the required setting may change.
- For commands running at half of the regular serial flash clock (QSPI_SMPR[HSENA] bit set) the sampling point must be figured separately to allow for the compensation of the absolute shift in time with respect to the sample-relative setting in the QSPI_SPMPR register.

36.10.2.1.2 DQS sampling method

Data sampling in SDR mode can be supported using the DQS sampling method. Refer to Data Strobe (DQS) sampling method for more details.

36.10.2.2 DDR Mode

The increasing requirement of improved throughput has introduced the double data rate (DDR) mode. In DDR mode, the data is transferred on both the rising and falling edges of the serial flash clock. The DDR serial flashes sample as well as drive the data on both rising and falling edges of serial flash clock.

36.10.2.2.1 Internal sampling (4x sampling method)

When the serial flash memories function in DDR mode, the data is valid for only half a clock cycle. This, along with the fact that the time for which the data is actually valid is smaller than half a clock cycle, requires that we provide closely spaced sampling points. The QuadSPI module provides a mechanism to sample the incoming data at multiple sampling points provided by a 4x serial flash clock in DDR mode. The figure below shows the different sampling points as configured by QuadSPI_SMPR[DDRSMP]. The FSDLY/FSPHS and HSDLY/HSPHS bits are ignored for DDR instructions.

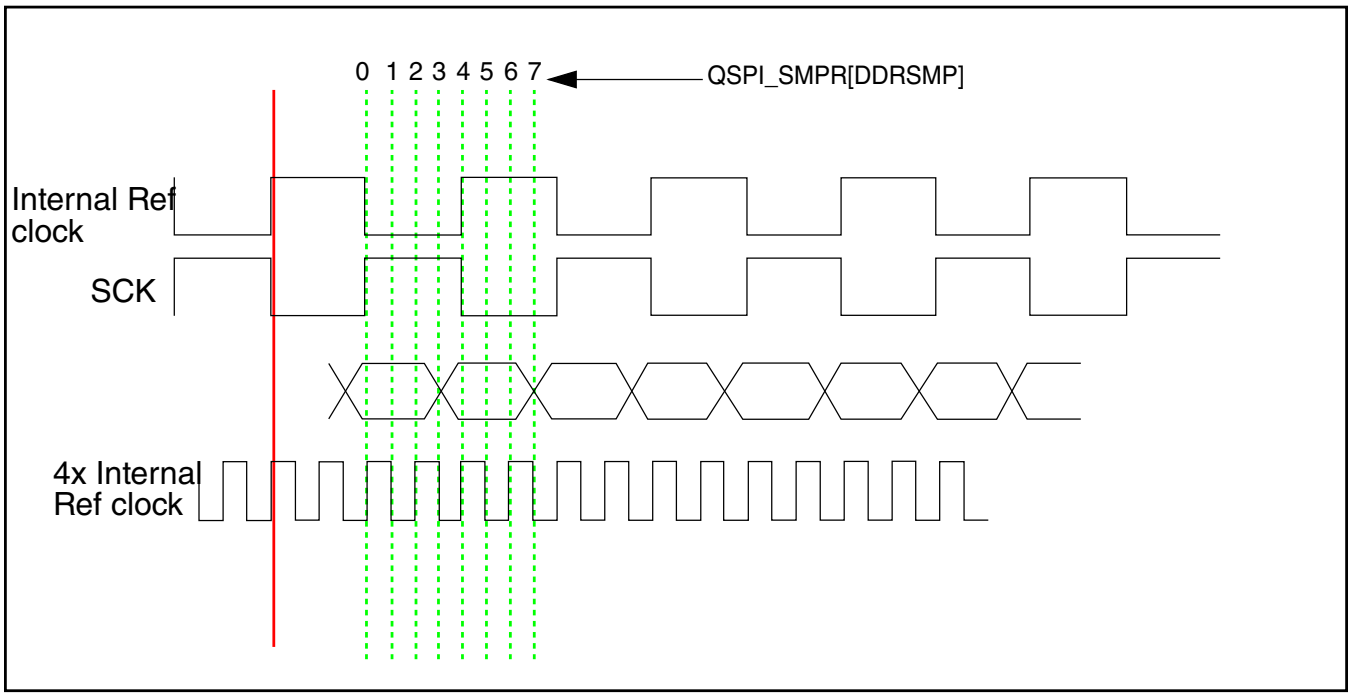


Figure 36-13. 4x sampling edges in DDR mode

Software should ensure that the correct sampling value is configured in the QuadSPI_SMPR[DDRSMP] register.

NOTE

Higher frequency can be achieved using data learning. For details, refer to Data Learning.

36.10.2.2.2 DQS sampling method

Data sampling in DDR mode can be supported using DQS method. Refer to Data Strobe (DQS) sampling method for more details.

A higher frequency can be achieved using Data learning. For details refer to Data Learning.

36.10.3 Data Strobe (DQS) sampling method

36.10.3.1 Basic Description

In DQS mode, the data strobe signal (DQS/RWDS) is used to sample the read data. Here, both DQS and the data sent by the flash move in the same direction, so it is relatively easier to achieve at higher frequencies.

When using DQS for SDR reads, QuadSPI internally samples the incoming data on only one of the edges (either rising edge or falling edge) of the strobe signal. The edge on which the data will be sampled depends on the setting of QuadSPI_SMPR[FSPHS].

QSPI_SMPR[FSPHS]	Sampling edge
0	rising
1	falling

The figure below shows sampling read data in SDR mode using DQS.

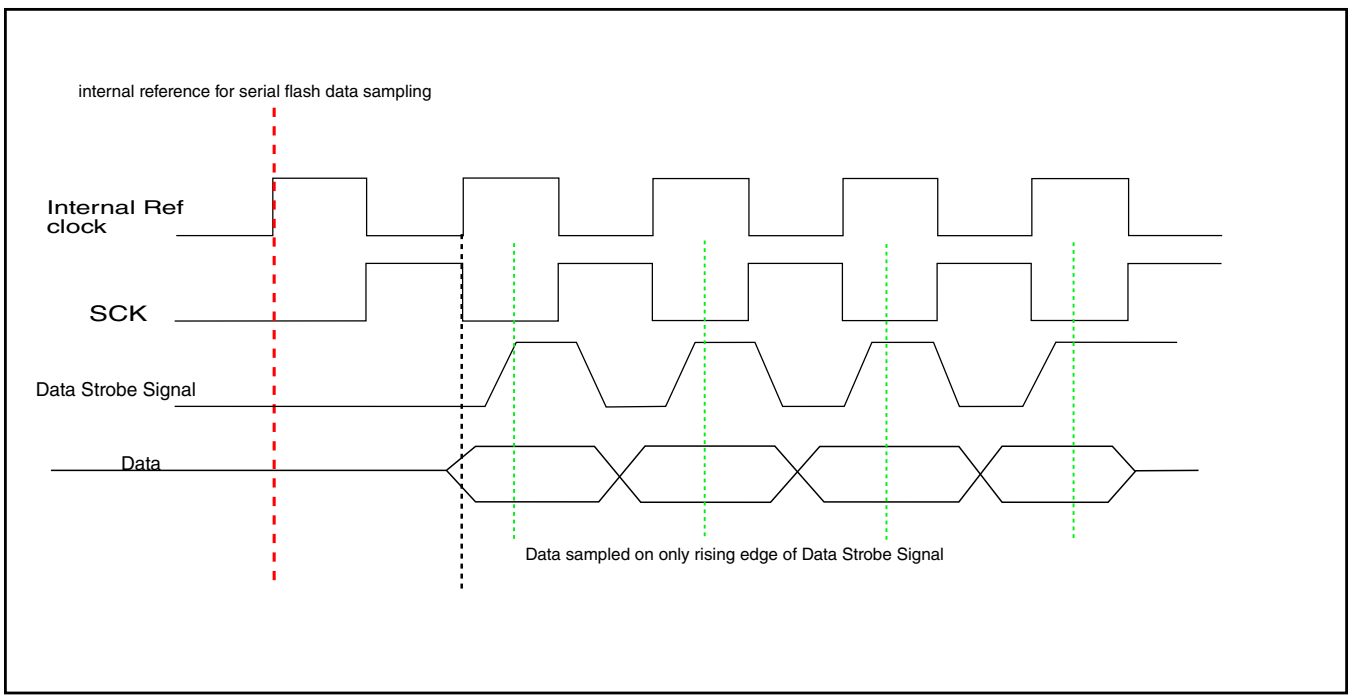


Figure 36-14. Data Strobe functionality in SDR mode

When using DQS for DDR reads, QuadSPI internally samples the incoming data on both the edges of the strobe signal. Refer to the figure below for more detail.

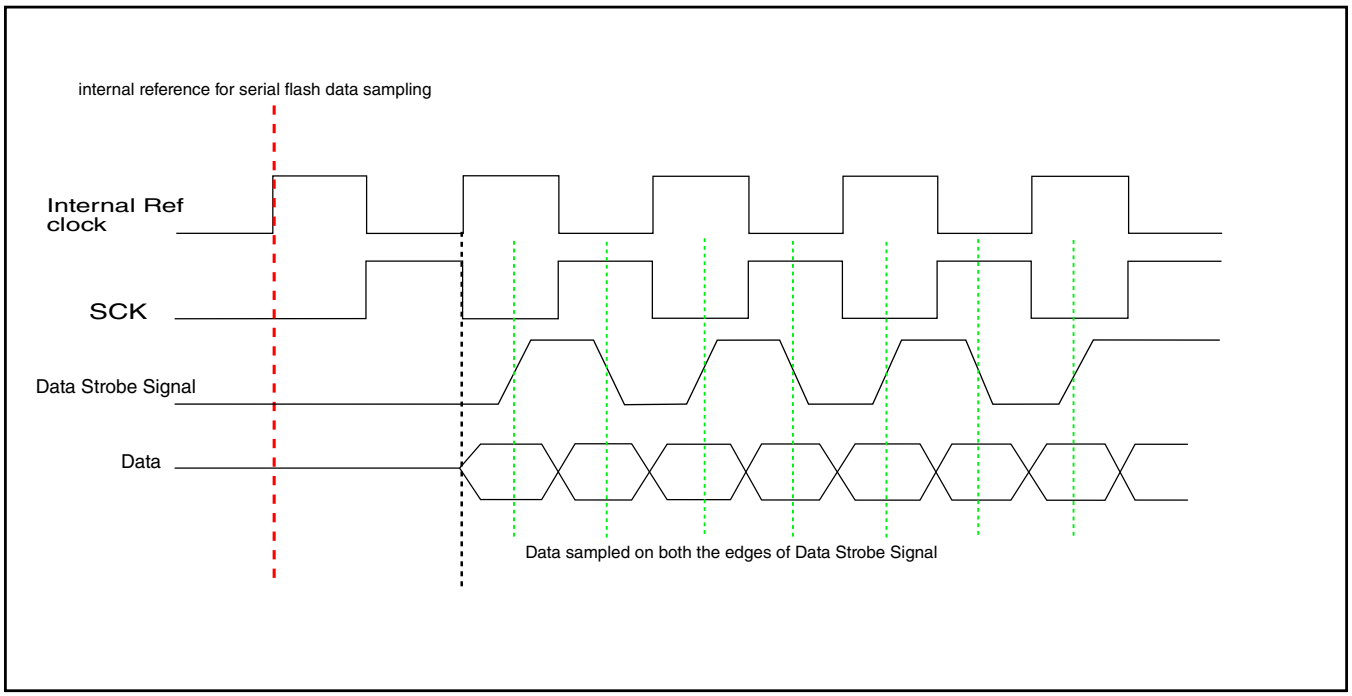


Figure 36-15. Data Strobe functionality in DDR mode

36.10.3.2 Internally generated DQS

In this mode, the internal reference clock is fed as a strobe to QuadSPI for read data sampling. The data strobe must be generated in a way such that the data is correctly sampled by the QuadSPI module. This internally generated data strobe signal can be used by QuadSPI to capture the data in:

- SDR mode
- DDR mode

Refer to QuadSPI chip-specific information for additional details about internally generated DQS.

36.10.3.3 External DQS

In serial flash memories supporting DQS, the data strobe signal is an output from the flash device that indicates when data is being transferred from the flash to the host controller. The data is then captured by the controller on:

- Only one edge (either rising or falling edge) of DQS signal in SDR mode
- Both rising/falling edge of the DQS signal in DDR mode

Some serial flash memories (for example, HyperFlash) provide the data strobe output (RWDS) with latency cycles included in between the ongoing read transaction. The data is sampled on both the edges of this signal taking into consideration that when no signal is provided by flash between ongoing transaction, data is not sampled then and at the end of transaction the required number of data to be fetched remains the same. Refer to the figure below for more detail.

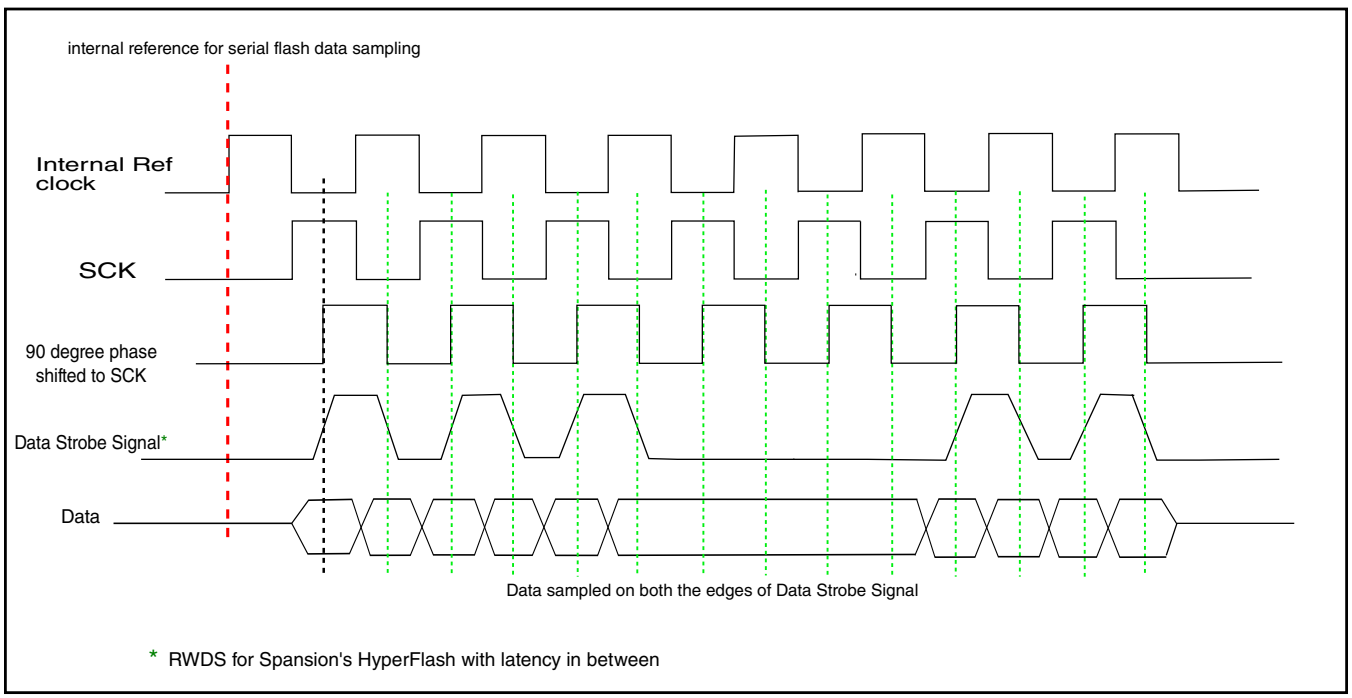


Figure 36-16. Data Strobe functionality with latency included

36.10.3.3.1 External Center Aligned Read Strobe

The QuadSPI supports serial flash memories using the Center Aligned Read Strobe (CRS) protocol. By virtue of this protocol, in addition to the SCK, the host controller provides a 90^{o} phase shifted SCK that allows the flash memory to generate valid data timed off SCK edges and a Data Read Strobe (DQS) signal output that is timed off the 90^{o} phase shifted SCK edges that is centered within the valid read data window. This allows the host controller to easily capture read data from the flash by using the data read strobe transitions and thereby allows for higher performance operation. Since the flash memory is the originator of the center aligned data read strobe as well as the read data, the temporal timing phase alignment between these signals is easier to guarantee across PVT (Process, Voltage and Temperature) corners.

The figure below shows data strobe functionality using CRS protocol.

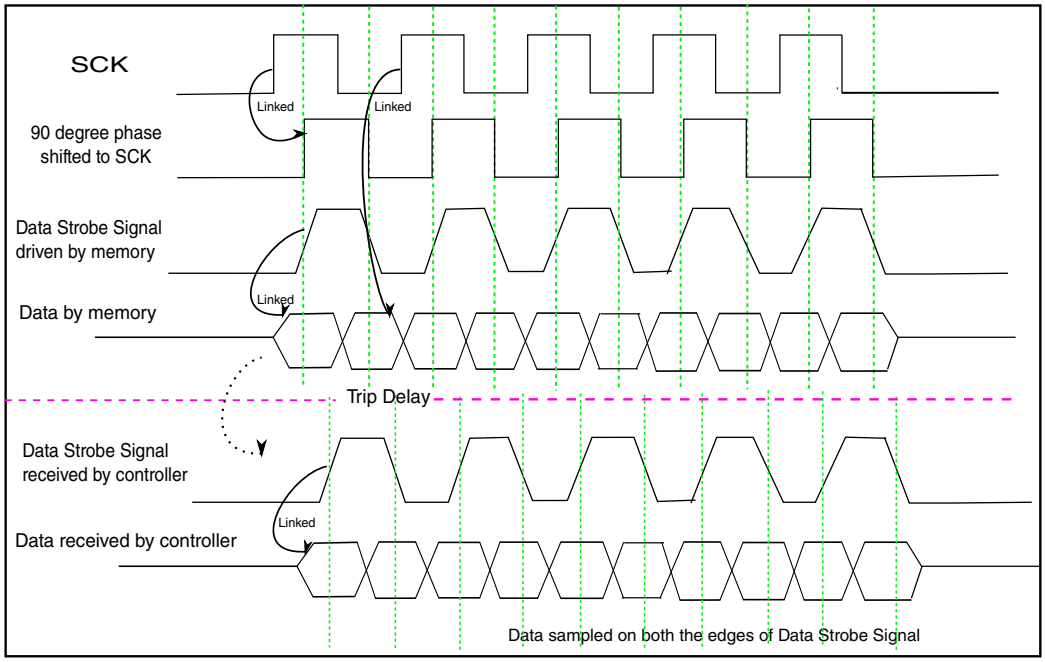


Figure 36-17. Data Strobe functionality using CRS protocol

36.10.4 Data Learning

36.10.4.1 Basic description

“Data learning” is used to manage varying data valid windows from flash memory as well as any variations in the chip based on PVT conditions in DDR mode. QuadSPI provides this feature via the DATA_LEARN instruction for all flash memories, irrespective of whether the flash supports it. The DATA_LEARN instruction accepts an operand that defines the number of bits of the known pattern for which the data learning has to be done. The known pattern is provided in the QSPI_DLPR register.

QuadSPI supports the data learning methods below:

- 4x sampling method
- Data Strobe (DQS) sampling method

The following sections explain data learning in greater detail.

36.10.4.2 4x sampling method

Automatic data learning is supported in 4x sampling mode. To start data learning:

1. Certain flash memories provide data learning as a feature for DDR data reads.

   For flash memories that support data learning, configure a known pattern in the Data Learn register inside flash. The pattern should be chosen to have multiple low and high transitions in the data bus. Set up a QuadSPI DDR data read sequence, inserting a DATA_LEARN instruction before the READ_DDR instruction. The flash will itself return the data learning pattern in between dummy cycles in every read command. Each I/O will output the same DLP value for every clock edge.

   For flash memories that *do not* support data learning, configure a known location in flash memory with a known pattern. The pattern should not have 0x00 or 0xFF in it. The pattern should be chosen to have multiple low and high transitions in the data bus. Set up a QuadSPI DDR data read sequence, inserting a DATA_LEARN instruction before the READ_DDR instruction. The address in the QuadSPI_SFAR register should point to the known location with the pattern. Configure the known pattern in the QuadSPI_DLPR [DLPV] field. Refer to Table 36-55 for details on how the data has to be ordered in memory for correct operation.

2. Select a sampling point using QuadSPI_SMPR[DDRSMP].
3. Initiate the read via a peripheral transaction.
4. QuadSPI reads the data from the flash. It then encounters the DATA_LEARN instruction and samples the incoming data on all 8 possible sampling points for all the data bus bits.
5. The sample point at which data matches the known pattern is reported in QuadSPI_SR[DLPSMP].
6. If data doesn't match at any sample point, QuadSPI_FR[DLPFF] is set.
7. If the correct sampling point is located, QuadSPI uses the new sampling point to sample the read data following the DATA_LEARN instruction.

This feature may be used to auto-calibrate the sampling point for DDR reads. This auto-calibration may be triggered at fixed intervals, or depending on a change in PVT conditions.

The following figure shows data learning with 4x DDR sampling:

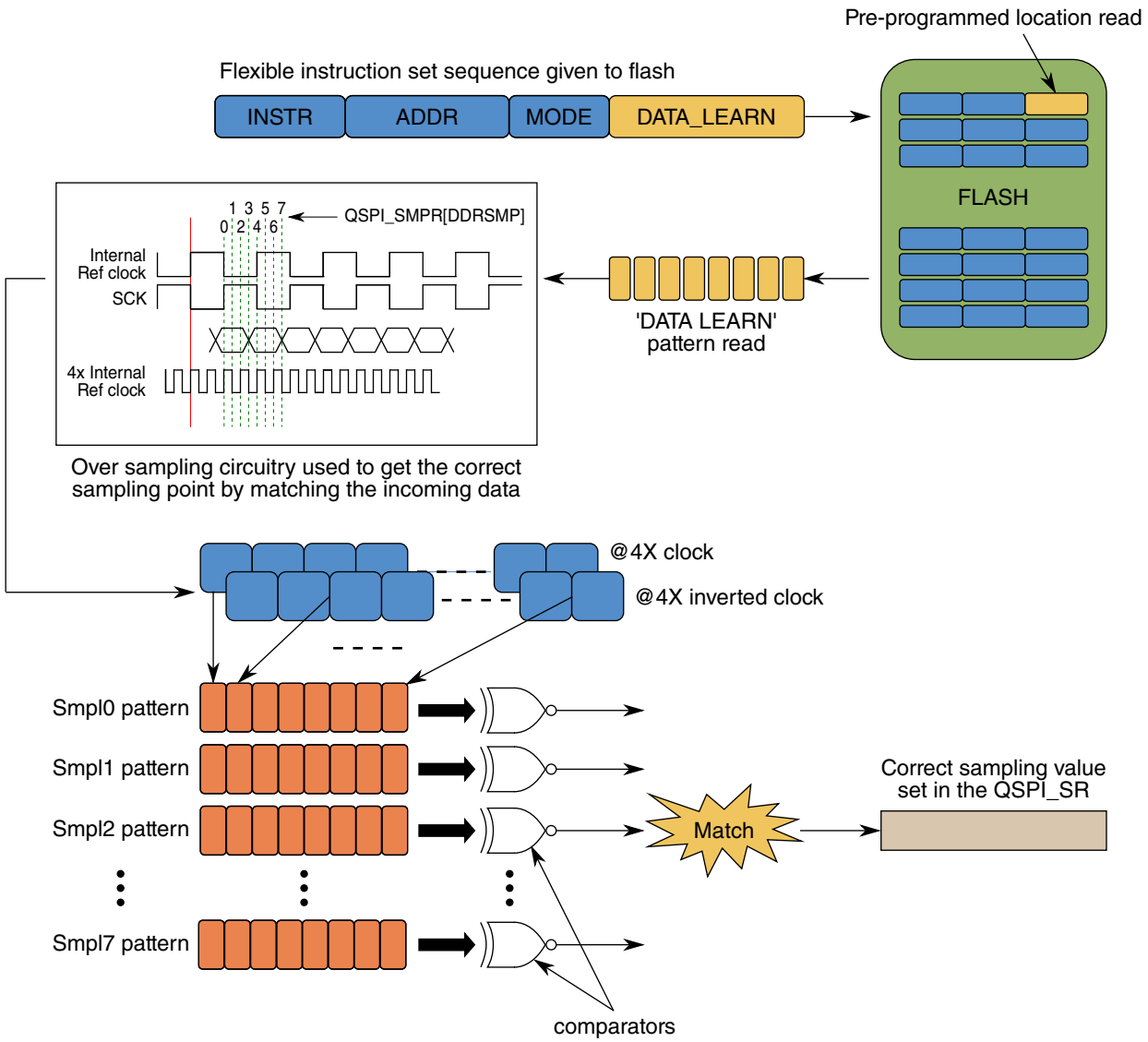


Figure 36-18. Data learning with 4x sampling method

36.10.4.3 Data Strobe (DQS) sampling method

Semi-automatic data learning is supported in DQS sampling method. To start data learning:

1. Certain flash memories provide data learning as a feature for DDR data reads.

   For flash memories that support data learning, configure a known pattern in the Data Learn register inside flash. The pattern should be chosen to have multiple low and high transitions in the data bus. Set up a QuadSPI DDR data read sequence, inserting a DATA_LEARN instruction before the READ_DDR instruction. The flash will itself return the data learning pattern in between dummy cycles in every read command. Each I/O will output the same DLP value for every clock edge.

For flash memories that *do not* support data learning, configure a known location in flash memory with a known pattern. The pattern should not have 0x00 or 0xFF in it. The pattern should be chosen to have multiple low and high transitions in the data bus. Set up a QuadSPI DDR data read sequence, inserting a DATA_LEARN instruction before the READ_DDR instruction. The address in the QSPI_SFAR register should point to the known location with the pattern. Configure the known pattern in the QSPI_DLPR[DLPV] field. Refer to Table 36-55 for details on how the data has to be ordered in memory for correct operation.

2. Select a sampling point. See chip-specific QuadSPI information for selection of the sampling point.
3. Initiate the read via a peripheral transaction.
4. QuadSPI reads the data from the flash. It then encounters the DATA_LEARN instruction and samples the incoming data on both edges (rising and falling) of the DQS.
5. If the data from the flash doesn't match the data learning pattern, the QuadSPI_FR[DLPFF] flag is set.
6. No sampling point is reported automatically by the QuadSPI module.
7. These steps (2-7) are repeated with varying VT conditions for a particular process until the QuadSPI_FR[DLPFF] is set. The sampling points where no QuadSPI_FR[DLPFF] is set signify valid setting.
8. In the case of multiple valid settings, software should choose the middle point.
9. The sampling point should be fixed with the above chosen point for the next READ transactions.

NOTE

It must be ensured that QuadSPI is not accessed during calibration.

NOTE

Ensure that there is no latency in between DQS edges while doing data learning using DQS sampling method.

This feature may be used to auto-calibrate the sampling point for DDR reads. This auto-calibration may be triggered at fixed intervals, or depending on a change in PVT conditions.

The following figure shows data learning in DQS mode:

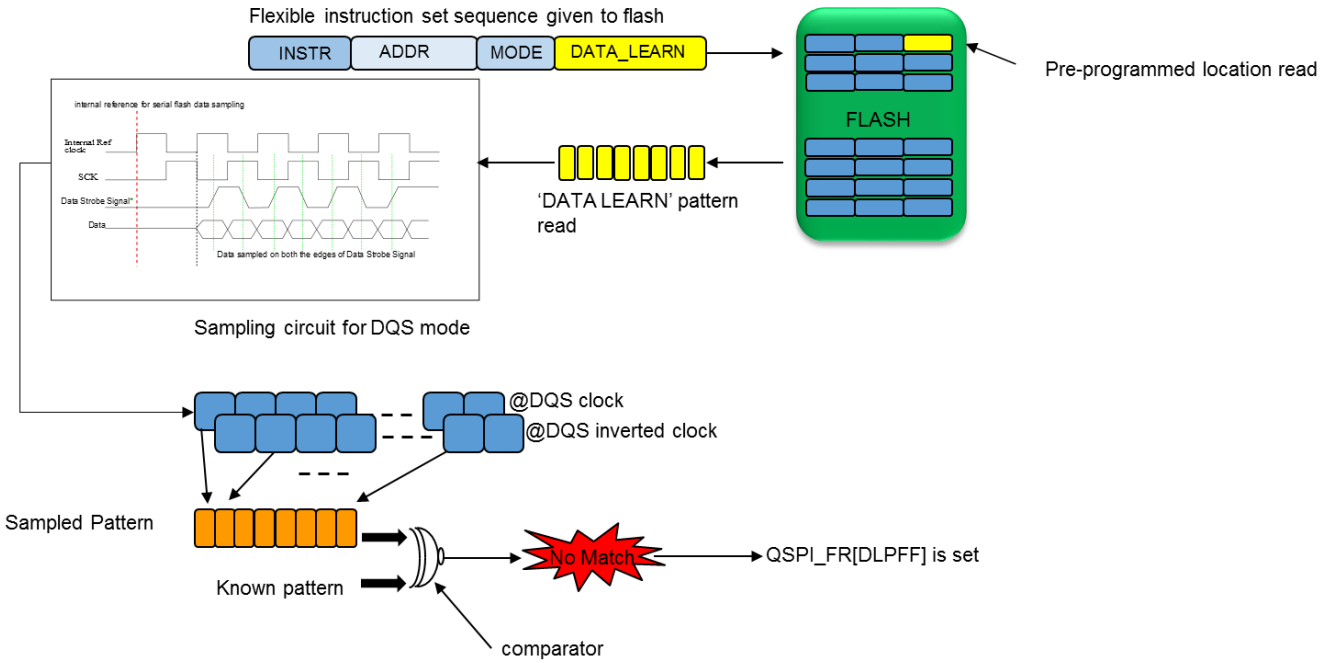


Figure 36-19. Data learning with DQS sampling method

36.10.4.4 Example: programming the data learning pattern in flash memory

If QSPI_DLPR[DLPV] is set to 0x43, QuadSPI tries to match this sample on every incoming data line for single, dual, quad, or octal configurations. The table below shows the data programmed in flash with endianness taken into consideration.

Table 36-55. Programming the Data Learning Pattern in flash memory

Endianness	Single IO	Dual IO	Quad IO	Octal IO
BE	0x43	0x300F	0x0F0000FF	0x00FF00000000FFFF
LE	0x43	0X0F30	0XFF00000F	0XFFFF0000000000FF

36.11 Data Input Hold Requirement of Flash

In DDR mode, the data is valid only for half clock cycle. It is difficult to meet the data input hold time requirement of flash. QuadSPI internally delays the data sent to flash so that it will be easy to meet the hold requirement. The QSPI_FLSHCR[TDH] is used for this purpose. If QSPI_FLSHCR[TDH] is configured to 0, the data sent to flash is aligned

with the internal reference clock of QuadSPI, if it is 1, then, the data is aligned to 2x internal reference half clock, if it is 2, then, the data is aligned to 4x internal reference half clock.

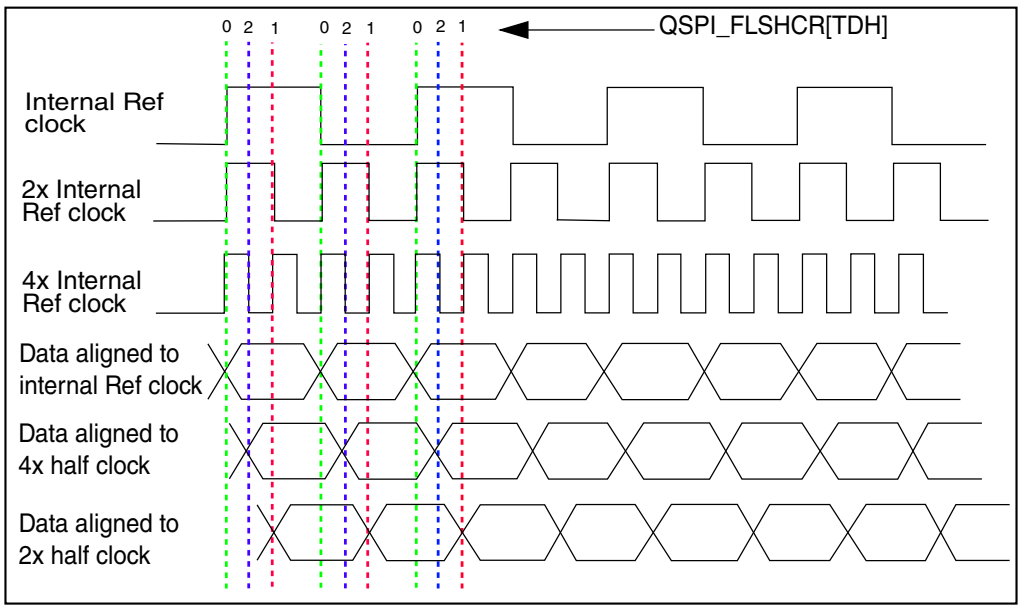


Figure 36-20. Data Hold

Chapter 37
On-the-Fly AES Decryption Module (OTFAD)

37.1 Introduction

One unmistakable trend in embedded processor design is the increasing need for hardware support of cryptographic calculations required for system security. In particular, there are emerging customer requirements to protect application code and data stored in external memories in an encrypted form and have the embedded processor provide hardware support for "on-the-fly" decryption. As the name suggests, the external memory image of the code and data is always in an encrypted format, and, in response to processor references of the memory space, the memory image is decrypted on the fly, returning the original values to the requesting bus master.

In these applications, the standard Advanced Encryption Standard (AES) [1] is the preferred cryptographic symmetric key block cipher algorithm. The AES function operates on 128-bit (16 byte) data blocks with either 128-, 192- or 256-bit secret keys. For this form of code and data encryption, the AES-128 mode, that is, the use of a 128-bit key is deemed sufficient.

The AES algorithm specifies a variable number of "rounds" be performed in the cryptographic calculation, based on the size of the key. For a 128-bit key, the data is processed through a series of calculations requiring 10 rounds to complete. Each round performs four different data transformations: 1) byte substitution using a substitution table (S-box), 2) shifting rows of the state array by different offsets, 3) mixing the data within each column of the state array, and 4) adding a round key to the state.

Many typical AES hardware implementations perform a single round operation in 1-2 machine cycles, but the performance requirements associated with on-the-fly decryption dictate a far more aggressive implementation.

The on-the-fly decryption engine is combined with the QuadSPI external flash memory controller. The QuadSPI memory controller supports glueless external connections to a wide variety of industry standard external "SPI" flashes. These memories were initially developed as very low pin count alternatives to traditional NOR flash memories with

their wide parallel data interfaces. Over time, the complexity of the SPI flash memories has increased (and this trend is continuing) and now, two bank, double data rate interfaces can supply 16 bits of flash data every cycle once the address and command have been sent and the basic access has been performed. For a 100 MHz DDR QuadSPI external interface, the access time for a 4-beat, 64-bit, 32-byte burst fetch might generate an 18-4-4-4 response at the microprocessor pins. Given these access times, the latest generation of QuadSPI external flash devices provides a cost effective non-volatile memory solution that supports eXecute-in-Place (XiP) capabilities. Stated differently, the combined access speed of these external flash memories, coupled with internal processor-local cache memories, allow the application code to be executed directly from the external memory without the need to copy the code into another (faster) memory, for example, an attached SDRAM or on-chip SRAM. This capability to execute directly from external flash without copying the code to another memory allows an easy migration from MCU to MPU configurations.

The resulting OTFAD engine adds ***zero cycles of additional latency*** to decrypt the code and data fetched from the external flash memory. The combination of the support for the CTR-AES128 mode plus an aggressive, pipelined implementation of the OTFAD performing up to 3 rounds in a single machine cycle allowing the engine to keep pace with the fastest data arrival rates. As a result, the OTFAD engine provides superior cryptographic decryption capabilities without compromising system performance for those embedded processor applications requiring this class of enhanced security.

37.1.1 References and terminology

These documents provide specific references to the cryptographic functions supported by the OTFAD:

1. FIPS Publication 197, "Advanced Encryption Standard (AES)", U.S. Department of Commerce, National Institute of Standards and Technology (NIST), November 26, 2001.
2. NIST Special Publication 800-38A, "Recommendation for Block Cipher Modes of Operation: Methods and Techniques", U.S. Department of Commerce, National Institute of Standards and Technology (NIST), December 2001.

There are numerous names and phrases that are commonly used in describing cryptographic functions. The following table provides a summary of the terms used in describing the OTFAD. It was mostly extracted from Section 4.1, "Definitions and Abbreviations" of [2].

Table 37-1. Cryptographic terms

Term	Definition
Block Cipher	A family of functions and their inverse functions that is parameterized by cryptographic keys; the functions map bit strings of a fixed length to bit strings of the same length.
Block Size	The number of bits in an input (or output) block of the block cipher. For OTFAD, this is 128 bits (16 bytes).
Ciphertext	Encrypted data.
CTR	Counter.
Cryptographic Key	A parameter used in the block cipher algorithm that determines the forward cipher operation and the inverse cipher operation.
Data Block (Block)	A sequence of bits whose length is the block size of the block cipher.
Decryption (Deciphering)	The process of a confidentiality mode that transforms encrypted data into the original usable data.
ECB	Electronic Codebook.
Encrypted Counter (ECTR)	An output in the CTR-AES decryption process, generated by encrypting the unique counter value. Exclusive-OR'ed with the ciphertext to produce plaintext.
Encryption (Enciphering)	The process of a confidentiality mode that transforms usable data into an unreadable form.
Forward Cipher Function (Forward Cipher Operation)	One of the two functions of the block cipher algorithm that is selected by the cryptographic key.
Initialization Vector (IV)	A data block that some modes of operation require as an additional initial input.
Input Block	A data block that is an input to either the forward cipher function or the inverse cipher function of the block cipher algorithm.
Inverse Cipher Function (Inverse Cipher Operation)	The function that reverses the transformation of the forward cipher function when the same cryptographic key is used.
Least Significant Bit(s)	The right-most bit(s) of a bit string.
Mode of Operation (Mode)	An algorithm for the cryptographic transformation of data that features a symmetric key block cipher algorithm.
Most Significant Bit(s)	The left-most bit(s) of a bit string.
Nonce	A value that is used only once.
Output Block	A data block that is an output of either the forward cipher function or the inverse cipher function of the block cipher algorithm.
Plaintext	Usable data that is formatted as input to a mode.

37.1.2 Features

The key features of the OTFAD include:

- AES-128 Counter Mode On-the-Fly Decryption

- 128-bit key and 128-bit data block sizes
  - 128-bit counter includes 64 bits of initialization vector + the 32-bit system address
- Adds zero cycles of incremental latency for decryption when used with QuadSPI
- Receives 64-bit encrypted data from QuadSPI, calculates decrypted data which is sent to AHB RAM buffer and bypassed back to system AHB read data bus

- Hardware support for 4 independent decryption segments, known as memory “contexts”
  - Each context has a unique 128-bit key, 64-bit counter and 64-bit memory region descriptor
- Functionally acts as a slave submodule to the QuadSPI
  - Logically connected "between" the QuadSPI and its AHB RAM buffer
  - Shares system AHB and IPS (slave peripheral) bus connections
  - Programming model mapped into the upper 1 KByte of the QuadSPI's IPS address space
  - Private 64-bit data buses for encrypted (ciphertext) and decrypted (plaintext) data
- Hardware microarchitecture
  - Heavily pipelined AES engine, optimized for encryption, performing 3 rounds per cycle
  - 64-bit AHB connections for easy integration to system bus fabric and QuadSPI
  - Data storage for two 128-byte encrypted counters and three 64-bit decrypted data buffers
  - Optimized for {32,64}-bit WRAP4 bursts (CPU cache miss fetch size, typical DMA fetch size)

37.1.3 Block diagrams

Figure 37-1 shows the connection topology of the OTFAD and its relationship to the QuadSPI and its AHB RAM buffer.

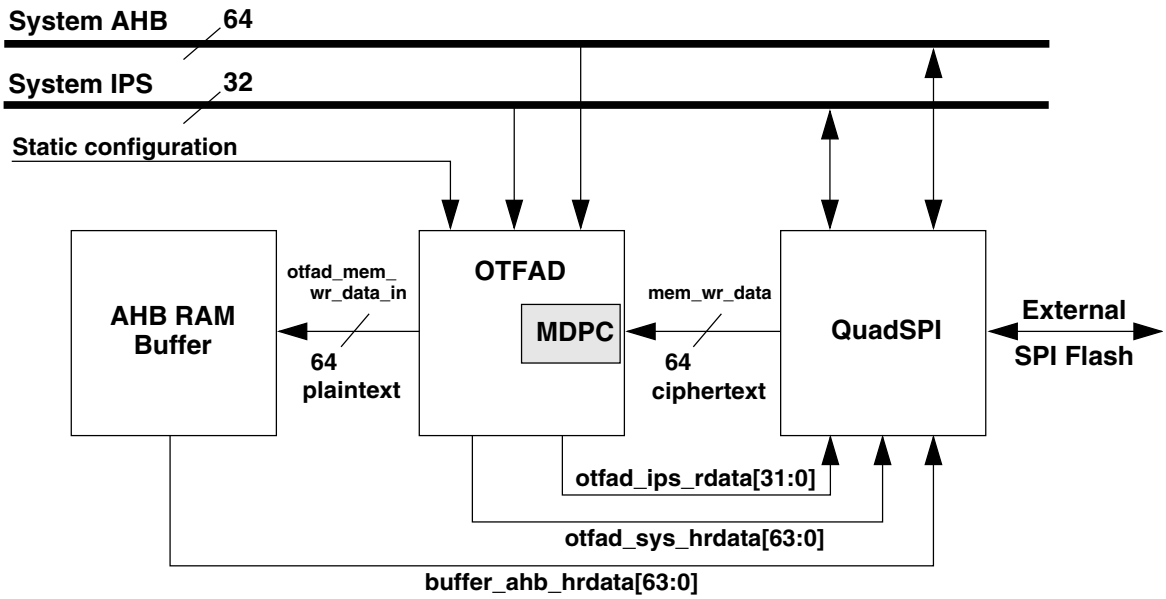


Figure 37-1. OTFAD and QuadSPI connection topology

See Figure 37-2 for the OTFAD block diagram.

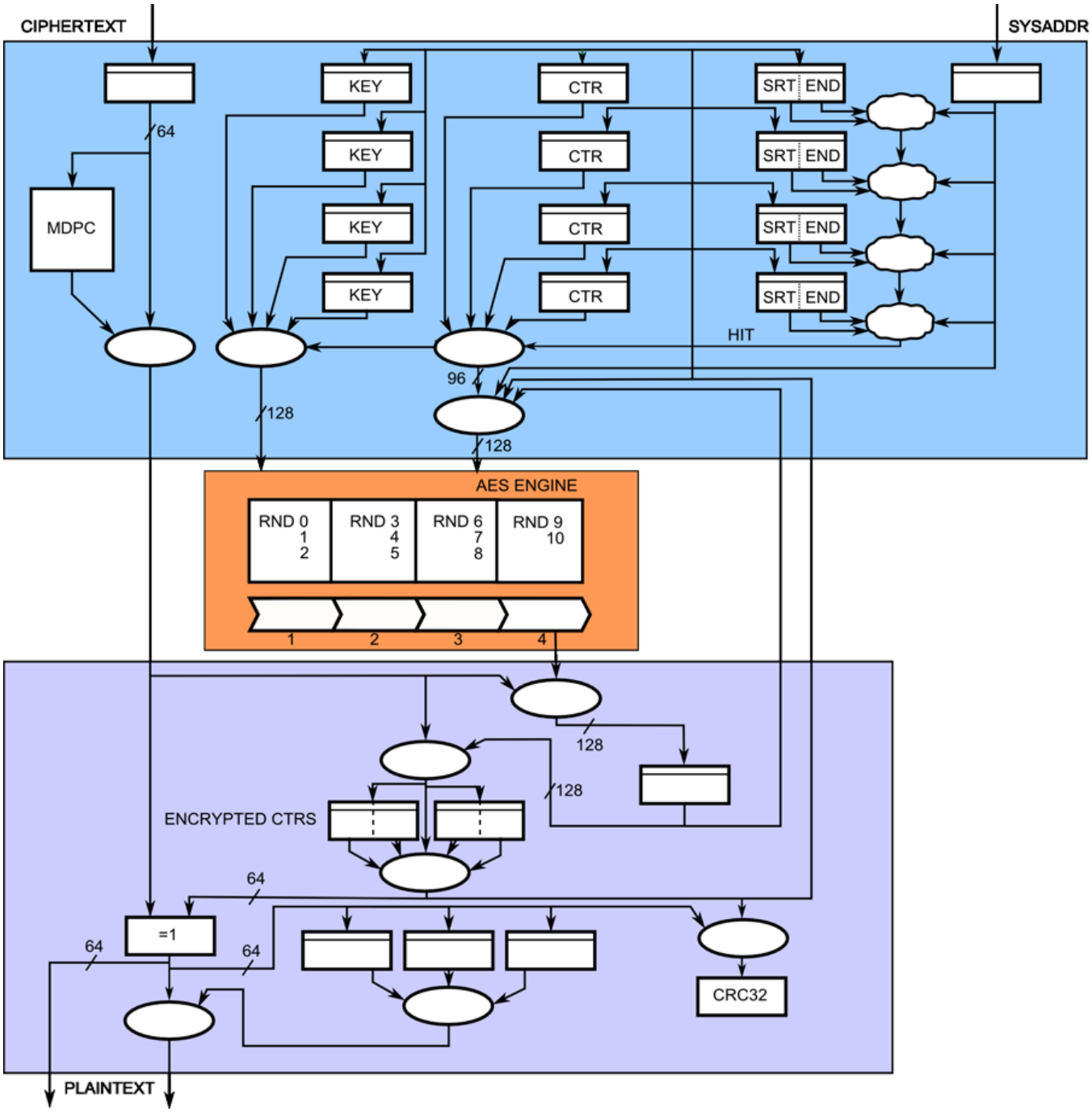


Figure 37-2. OTFAD module block diagram

37.1.4 Modes of operation

The OTFAD supports three modes of operation as defined by input configuration and control signals. The operating mode is signaled in the SR and includes:

1. Logically Disabled Mode (LDM)

This mode is entered immediately after reset by the assertion of a static configuration input signal, which is treated as the highest priority configuration signal. While in this mode, the OTFAD is logically disabled. Input data from the QuadSPI is simply passed through to the AHB RAM buffer and no data decryptions are performed. The OTFAD's programming model is inaccessible and all attempted accesses are error terminated. If the static configuration input signal is asserted, the OTFAD is always in this mode.

2. Security Violation Mode (SVM)

   This mode is entered by the assertion of an SoC security alarm input signal or the signaling of a non-volatile memory mass erase operation. The signaling of either event causes the OTFAD to immediately clear its entire programming model and enter this state, where it remains until the next reset. While in this mode, the CR[RRAE] flag is asserted to limit the accessibility of the OTFAD's programming model registers. Input data from the QuadSPI is simply passed through to the AHB RAM buffer and no data decryptions are performed.

3. Normal Mode (NM)

   This mode is defined when the OTFAD is not in the logically disabled or security violation modes. In this mode, the OTFAD functions normally and is capable of performing data decryptions and/or data bypasses as it responds strictly to the memory transactions on its connected system buses. It should be noted the OTFAD operates in this mode regardless of the state of CR[GE]. The assertion of the global enable is required when the OTFAD is to perform data decryptions; if CR[GE] = 0, then the OTFAD simply bypasses all data fetched by the QuadSPI.

   The OTFAD's operating mode is encoded and visible in the SR[MODE] field. For more information, see OTFAD operating modes.

   In normal mode, as a memory-mapped device located in the core platform’s clock domain, it responds based on the memory addresses of its connected system buses. The slave peripheral bus may be used to access the OTFAD’s programming model to configure the module’s operation.

37.2 External signal description

The OTFAD module does not directly support any external interfaces.

The internal interfaces include the address and attribute input signals from a standard 64-bit AMBA-AHB system bus and a 32-bit IPS slave peripheral bus for all programming model accesses, as shown in Figure 37-1.

The OTFAD receives the IPS input signals and generates a read data output which is sent to the QuadSPI where it is combined with local signals to form an IPS read data output as well as bus termination control signals. There are also three private 64-bit data buses: one input from the QuadSPI typically providing ciphertext and two outputs containing plaintext data after decryption - one sent to the AHB RAM buffer and another sent back to the QuadSPI for forwarding onto the system AHB read data bus. There is also a 64-bit read data bus from the AHB RAM buffer back to the QuadSPI for servicing system bus accesses which "hit" in the buffer. For more information on the OTFAD's interface signals, see Microarchitecture overview.

37.3 Memory map/register definition

The OTFAD module supports a number of program-visible registers located in the upper 1 KB region within the QuadSPI's 4 KB address space. The OTFAD receives the slave peripheral bus input signals and generates a read data output which is sent to the QuadSPI where it is combined with local signals to form the read data output as well as bus termination control signals.

The register resources of the OTFAD programming model can only be accessed while in secure privileged mode. Unless noted otherwise, the programming model registers can be accessed via 8-, 16- or 32-bit reads and 32-bit write references. Attempted accesses in a different operating mode, using unsupported write data sizes, writes to read-only resources, or to reserved spaces are terminated with an error unless noted otherwise.

The architectural definition of the OTFAD programming model is presented in this section.

It should be noted that a number of the programming model registers are organized as 2-dimensional data structures. These generic arrays contain "m" words representing the "columns" and "n" instances of the structure representing the "rows". These may be described as `structure[n][m]`. They appear in the address space of the programming model memory map in the standard C language row-major layout, that is, the "m" words representing the "column" appear sequentially with the entire row replicated "n" times. The OTFAD register structure uses the naming convention of *OTFAD_CTXn_<regname>_Wm*, where the column number "m" appears as a numeric suffix on the W (32-bit word) identifier, and the row identifier "n" appears as the context suffix.

The capabilities of the slave peripheral bus interface in this environment may be considerably reduced based on the state of the CR[RRAE] and static chip configuration inputs. For the affected registers, their access values are shown as "R/W, or RAZ/WI" in

this section. This is intended to denote that the affected registers have a "normal" access mode, or have attempted accesses treated as read-as-zero/write-ignore if operating in the restricted register access mode (CR[RRAE] = 1).

OTFAD memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_B800	Control Register (OTFAD_CR)	32	R/W	0000_0000h	37.3.1/1022
400D_B804	Status Register (OTFAD_SR)	32	R/W	See section	37.3.2/1025
400D_B808	Cyclic Redundancy Check Register (OTFAD_CRC)	32	R/W	0000_0000h	37.3.3/1026
400D_B900	AES Key Word0 (OTFAD_CTX0_KEY_W0)	32	R/W	0000_0000h	37.3.4/1027
400D_B904	AES Key Word1 (OTFAD_CTX0_KEY_W1)	32	R/W	0000_0000h	37.3.5/1028
400D_B908	AES Key Word2 (OTFAD_CTX0_KEY_W2)	32	R/W	0000_0000h	37.3.6/1029
400D_B90C	AES Key Word3 (OTFAD_CTX0_KEY_W3)	32	R/W	0000_0000h	37.3.7/1029
400D_B910	AES Counter Word0 (OTFAD_CTX0_CTR_W0)	32	R/W	0000_0000h	37.3.8/1030
400D_B914	AES Counter Word1 (OTFAD_CTX0_CTR_W1)	32	R/W	0000_0000h	37.3.9/1031
400D_B918	AES Region Descriptor Word0 (OTFAD_CTX0_RGD_W0)	32	R/W	0000_0000h	37.3.10/ 1031
400D_B91C	AES Region Descriptor Word1 (OTFAD_CTX0_RGD_W1)	32	R/W	See section	37.3.11/ 1032
400D_B940	AES Key Word0 (OTFAD_CTX1_KEY_W0)	32	R/W	0000_0000h	37.3.4/1027
400D_B944	AES Key Word1 (OTFAD_CTX1_KEY_W1)	32	R/W	0000_0000h	37.3.5/1028
400D_B948	AES Key Word2 (OTFAD_CTX1_KEY_W2)	32	R/W	0000_0000h	37.3.6/1029
400D_B94C	AES Key Word3 (OTFAD_CTX1_KEY_W3)	32	R/W	0000_0000h	37.3.7/1029
400D_B950	AES Counter Word0 (OTFAD_CTX1_CTR_W0)	32	R/W	0000_0000h	37.3.8/1030
400D_B954	AES Counter Word1 (OTFAD_CTX1_CTR_W1)	32	R/W	0000_0000h	37.3.9/1031
400D_B958	AES Region Descriptor Word0 (OTFAD_CTX1_RGD_W0)	32	R/W	0000_0000h	37.3.10/ 1031
400D_B95C	AES Region Descriptor Word1 (OTFAD_CTX1_RGD_W1)	32	R/W	See section	37.3.11/ 1032
400D_B980	AES Key Word0 (OTFAD_CTX2_KEY_W0)	32	R/W	0000_0000h	37.3.4/1027
400D_B984	AES Key Word1 (OTFAD_CTX2_KEY_W1)	32	R/W	0000_0000h	37.3.5/1028
400D_B988	AES Key Word2 (OTFAD_CTX2_KEY_W2)	32	R/W	0000_0000h	37.3.6/1029
400D_B98C	AES Key Word3 (OTFAD_CTX2_KEY_W3)	32	R/W	0000_0000h	37.3.7/1029
400D_B990	AES Counter Word0 (OTFAD_CTX2_CTR_W0)	32	R/W	0000_0000h	37.3.8/1030
400D_B994	AES Counter Word1 (OTFAD_CTX2_CTR_W1)	32	R/W	0000_0000h	37.3.9/1031
400D_B998	AES Region Descriptor Word0 (OTFAD_CTX2_RGD_W0)	32	R/W	0000_0000h	37.3.10/ 1031
400D_B99C	AES Region Descriptor Word1 (OTFAD_CTX2_RGD_W1)	32	R/W	See section	37.3.11/ 1032
400D_B9C0	AES Key Word0 (OTFAD_CTX3_KEY_W0)	32	R/W	0000_0000h	37.3.4/1027
400D_B9C4	AES Key Word1 (OTFAD_CTX3_KEY_W1)	32	R/W	0000_0000h	37.3.5/1028
400D_B9C8	AES Key Word2 (OTFAD_CTX3_KEY_W2)	32	R/W	0000_0000h	37.3.6/1029

Table continues on the next page...

OTFAD memory map (continued)

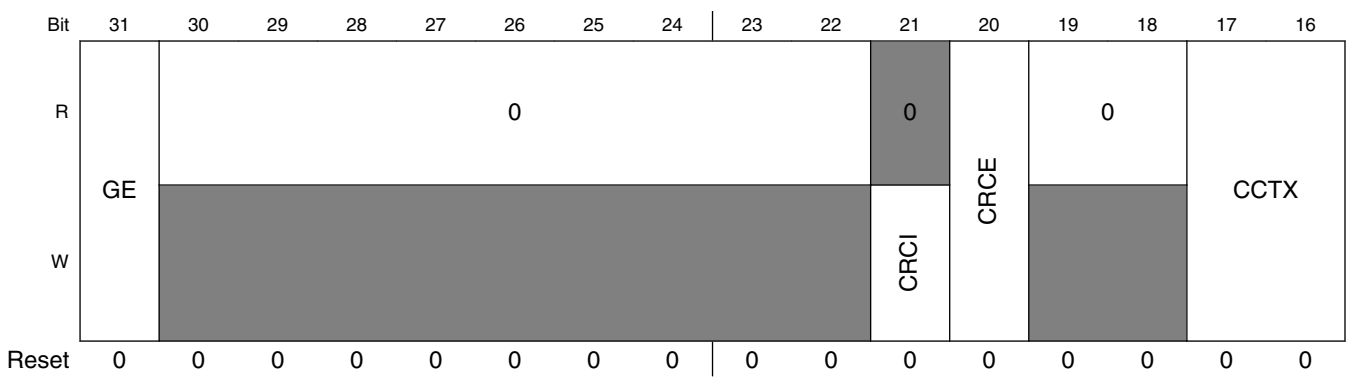
Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_B9CC	AES Key Word3 (OTFAD_CTX3_KEY_W3)	32	R/W	0000_0000h	37.3.7/1029
400D_B9D0	AES Counter Word0 (OTFAD_CTX3_CTR_W0)	32	R/W	0000_0000h	37.3.8/1030
400D_B9D4	AES Counter Word1 (OTFAD_CTX3_CTR_W1)	32	R/W	0000_0000h	37.3.9/1031
400D_B9D8	AES Region Descriptor Word0 (OTFAD_CTX3_RGD_W0)	32	R/W	0000_0000h	37.3.10/ 1031
400D_B9DC	AES Region Descriptor Word1 (OTFAD_CTX3_RGD_W1)	32	R/W	See section	37.3.11/ 1032

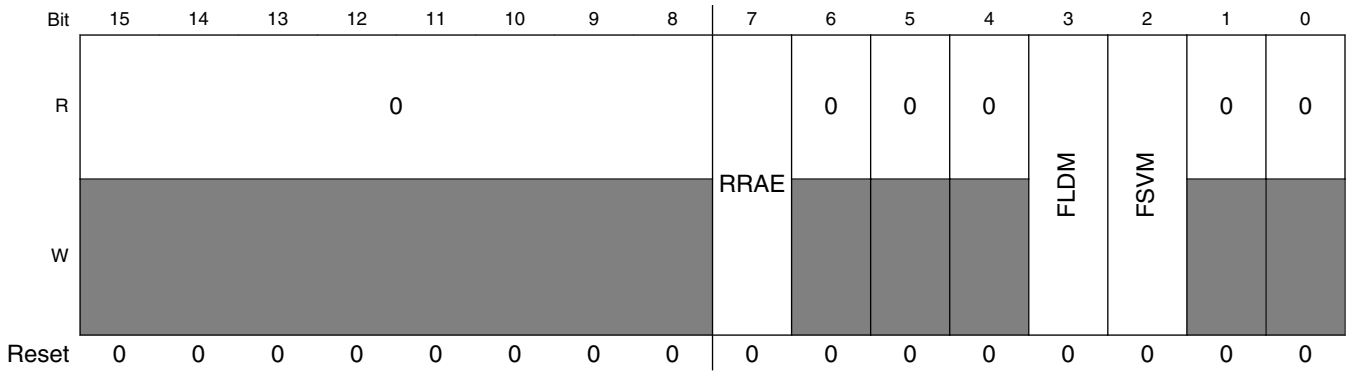
37.3.1 Control Register (OTFAD_CR)

This register defines the operating configuration of the OTFAD including a global enable indicator.

There are 2 register fields in the CR that control the OTFAD configuration. These fields (GE, RRAE) are generated based on both the contents of the CR plus static input configuration signals. For both bits, the contents of the CR flag is logically summed (OR'd) with the static input configuration signals to form the actual control used by the OTFAD. Reads of the CR return the logical summation of these configuration controls. Entry into the LDM or SVM modes clears both indicators. For more details, see OTFAD configuration details.

Address: 400D_AC00h base + C00h offset = 400D_B800h





OTFAD_CR field descriptions

Field	Description
31 GE	Global OTFAD Enable This field enables the OTFAD operation. It is cleared by entry into the LDM or SVM modes. 0 OTFAD has decryption disabled, and bypasses all data fetched by the QuadSPI. 1 OTFAD has decryption enabled, and processes fetched data as defined by the hardware configuration.
30–22 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
21 CRCI	CRC Initialization When set, this field forces an initialization of the CRC data register to all ones. This field always reads as zero. 0 CRC data register is unaffected. 1 CRC data register is immediately initialized after a write with this data bit set.
20 CRCE	CRC Enable This field controls if the standard 32-bit Ethernet cyclic redundancy check (CRC) for a given context is enabled. It is cleared by entry into the LDM or SVM modes. 0 CRC-32 is disabled. 1 CRC-32 for the context defined by CR[CCTRX] is enabled.
19–18 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
17–16 CCTX	CRC Context This field defines which context has its CRC check enabled when CR[CRCE] = 1. 00 Enable CTX0 CRC check. 01 Enable CTX1 CRC check. 10 Enable CTX2 CRC check. 11 Enable CTX3 CRC check.
15–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 RRAE	Restricted Register Access Enable

Table continues on the next page...

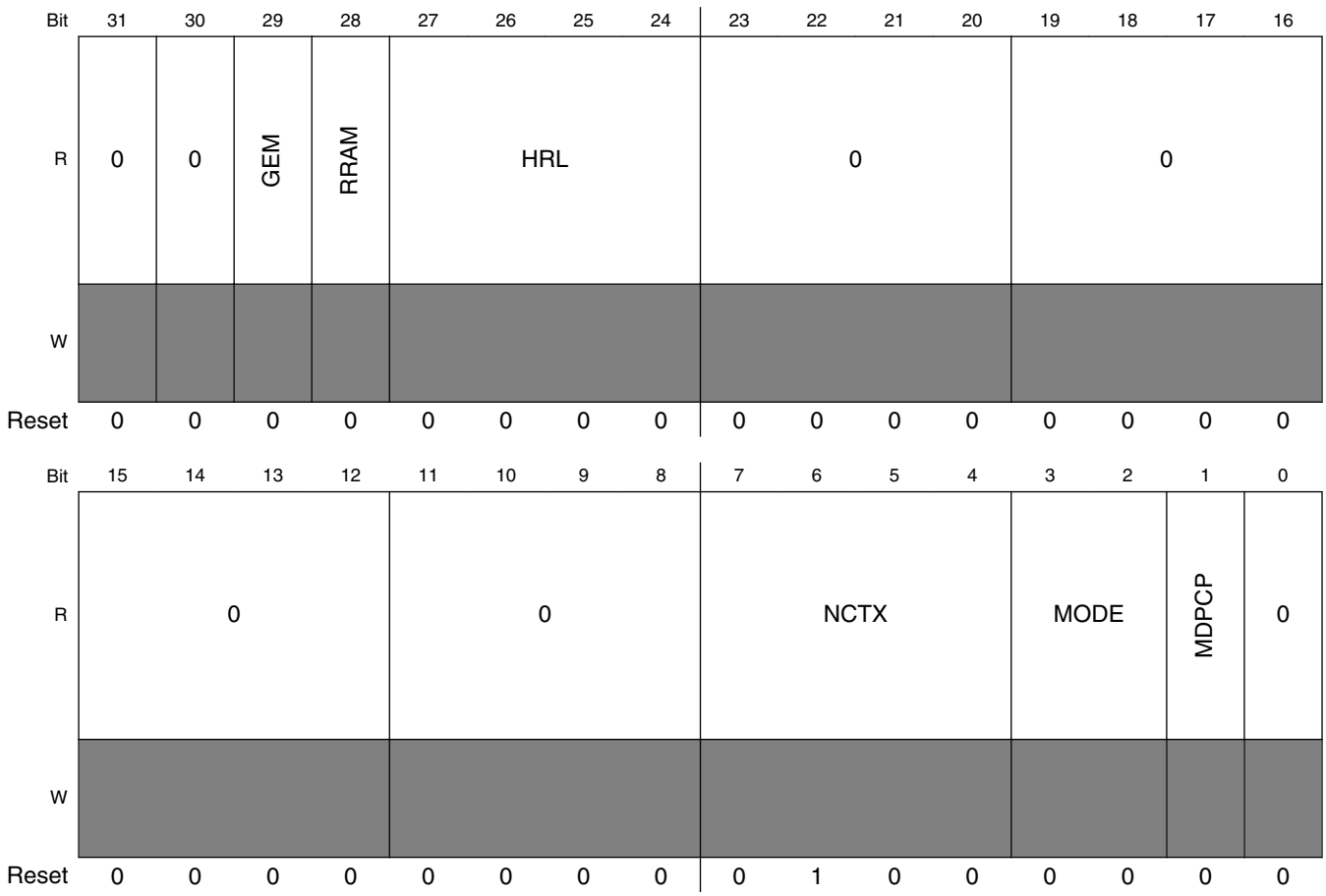
OTFAD_CR field descriptions (continued)

Field	Description
	If this bit is asserted, only the CR, SR and CRC registers can be accessed; attempted accesses of all other registers are treated as RAZ/WI (read-as-zero/write-ignore). This indicator is sticky; once set, it remains asserted until the next system reset, when it is cleared. It is also asserted by entry into the LDM or SVM modes. The value of this field is reflected in the SR[RRAM] flag. 0 Register access is fully enabled. The OTFAD programming model registers can be accessed “normally”. 1 Register access is restricted and only the CR, SR and CRC can be accessed; others are treated as RAZ/WI.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 FLDM	Force Logically Disabled Mode This field is intended to provide a mechanism for software testing of entry into the Logically Disabled Mode (LDM). This indicator is sticky; once set, it remains asserted until the next system reset, when it is cleared. 0 No effect on the operating mode. 1 Force entry into LDM after a write with this data bit set. SR[MODE] signals the operating mode.
2 FSVM	Force Security Violation Mode This field is intended to provide a mechanism for software testing of entry into the Security Violation Mode (SVM). This indicator is sticky; once set, it remains asserted until the next system reset, when it is cleared. 0 No effect on the operating mode. 1 Force entry into SVM after a write with this data bit set and the data bit associated with FLDM cleared. SR[MODE] signals the operating mode.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

37.3.2 Status Register (OTFAD_SR)

This register provides OTFAD status information.

Address: 400D_AC00h base + C04h offset = 400D_B804h



OTFAD_SR field descriptions

Field	Description
31 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
30 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
29 GEM	Global Enable Mode This indicator signals the global enabled/disabled state of the OTFAD. This flag is identical to the read value of CR[GE]. 0 OTFAD is disabled, and bypasses all data fetched by the QuadSPI. 1 OTFAD is enabled, and processes data fetched by the QuadSPI as defined by the hardware configuration.

Table continues on the next page...

OTFAD_SR field descriptions (continued)

Field	Description
28 RRAM	Restricted Register Access Mode This indicator signals that accesses to the slave peripheral bus are operating in a restricted mode, where only the CR, SR and CRC registers can be referenced. This access mode can be defined by the assertion of CR[RRAE] = 1. Attempted accesses to other registers are treated as RAZ/WI. This flag is identical to the read value of CR[RRAE]. 0 Register access is fully enabled. The OTFAD programming model registers can be accessed “normally”. 1 Register access is restricted and only the CR, SR and CRC can be accessed; others are treated as RAZ/WI.
27–24 HRL	Hardware Revision Level This field reads as zero.
23–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7–4 NCTX	Number of Contexts This field signals the number of implemented hardware contexts. It reads as 4.
3–2 MODE	Operating Mode This field specifies the OTFAD’s operating mode. Input configuration and control signals force entry from normal mode (NRM) into one of the two special operating modes (LDM, SVM). See Modes of operation for more details. 00 Operating in Normal mode (NRM) 01 Unused (reserved) 10 Operating in Security Violation Mode (SVM) 11 Operating in Logically Disabled Mode (LDM)
1 MDPCP	MDPC Present This field signals the presence of the Multi-Dimensional Parity Checker. For this device, it always has the value 0.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

37.3.3 Cyclic Redundancy Check Register (OTFAD_CRC)

The CRC register is the data register used during OTFAD cyclic redundancy check operations.

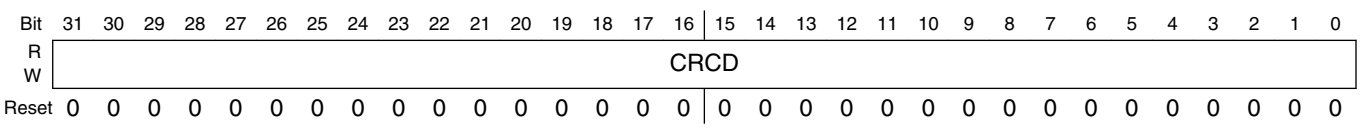
The CRC implements the standard 32-bit “Ethernet” polynomial, commonly expressed as 0x04C1_1DB7 or mathematically as $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$.

The OTFAD supports optional CRC calculations for a selected context. For all uses, the data being checked is the plaintext output, processed as a little endian array of 8-bit bytes. It must be accessed sequentially from the lowest address to the highest address.

For CRC checking on a selected context, the hardware must be configured by writing the CR[CRCI = 1, CRCE = 1, CCTX = n] bit fields. This initializes the CRC to 0xFFFF_FFFF, enables it and selects context n as the data source. See Context CRC for additional information.

It should also be noted that the CRC hardware implements a data pipeline and the CRC register is not updated with its final value until 2 clocks after the last input data is presented to the OTFAD. For typical system use cases, this exposed pipeline time is not visible to reads of this register on the slave peripheral bus.

Address: 400D_AC00h base + C08h offset = 400D_B808h



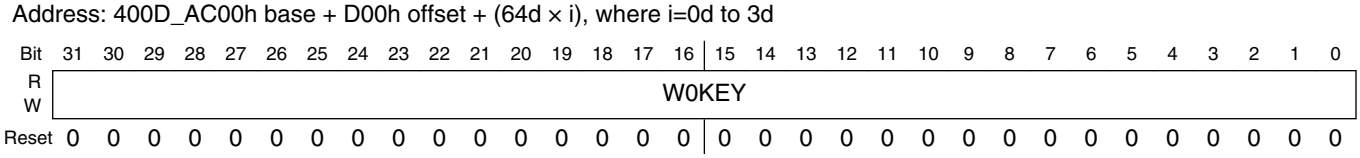
OTFAD_CRC field descriptions

Field	Description
CRCD	CRC Data.

37.3.4 AES Key Word0 (OTFAD_CTX*n*_KEY_W0)

The CTXn_KEY_Wm registers provide a 2-dimensional data structure for local OTFAD storage of the 128-bit key for context “n”. There are four consecutive memory-mapped register words containing the key used for the AES calculations associated with the given context. The programming model view of the CTXn_KEY_Wm registers is a little-endian 16-element byte data array, while the 128-bit key is defined as the concatenation of {A0, A1, A2,..., A14, A15}.

Address: 400D_AC00h base + D00h offset + (64d × i), where i=0d to 3d



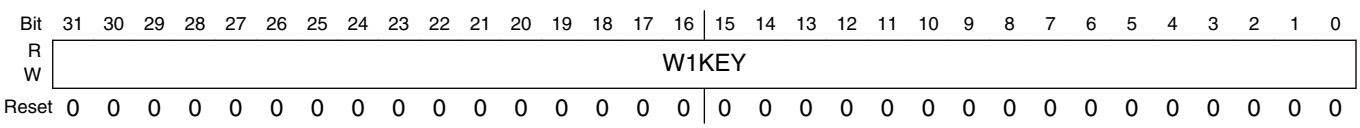
OTFAD_CTX*n*_KEY_W0 field descriptions

Field	Description
W0KEY	AES Key The key can be written using the slave peripheral bus. The four consecutive little-endian memory-mapped registers provide 128 bits of key storage. Word0: KEY[31:0][A03, A02, A01, A00] Word1: KEY[31:0][A07, A06, A05, A04] Word2: KEY[31:0][A11, A10, A09, A08] Word3: KEY[31:0][A15, A14, A13, A12]

37.3.5 AES Key Word1 (OTFAD_CTX*n*_KEY_W1)

The CTXn_KEY_Wm registers provide a 2-dimensional data structure for local OTFAD storage of the 128-bit key for context “n”. There are four consecutive memory-mapped register words containing the key used for the AES calculations associated with the given context. The programming model view of the CTXn_KEY_Wm registers is a little-endian 16-element byte data array, while the 128-bit key is defined as the concatenation of {A0, A1, A2,..., A14, A15}.

Address: 400D_AC00h base + D04h offset + (64d × i), where i=0d to 3d



OTFAD_CTX*n*_KEY_W1 field descriptions

Field	Description
W1KEY	AES Key The key can be written using the slave peripheral bus. The four consecutive little-endian memory-mapped registers provide 128 bits of key storage. Word0: KEY[31:0][A03, A02, A01, A00] Word1: KEY[31:0][A07, A06, A05, A04] Word2: KEY[31:0][A11, A10, A09, A08] Word3: KEY[31:0][A15, A14, A13, A12]

37.3.6 AES Key Word2 (OTFAD_CTX*n*_KEY_W2)

The CTXn_KEY_Wm registers provide a 2-dimensional data structure for local OTFAD storage of the 128-bit key for context “n”. There are four consecutive memory-mapped register words containing the key used for the AES calculations associated with the given context. The programming model view of the CTXn_KEY_Wm registers is a little-endian 16-element byte data array, while the 128-bit key is defined as the concatenation of {A0, A1, A2,..., A14, A15}.

Address: 400D_AC00h base + D08h offset + (64d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	W2KEY																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OTFAD_CTX*n*_KEY_W2 field descriptions

Field	Description
W2KEY	AES Key The key can be written using the slave peripheral bus. The four consecutive little-endian memory-mapped registers provide 128 bits of key storage. Word0: KEY[31:0][A03, A02, A01, A00] Word1: KEY[31:0][A07, A06, A05, A04] Word2: KEY[31:0][A11, A10, A09, A08] Word3: KEY[31:0][A15, A14, A13, A12]

37.3.7 AES Key Word3 (OTFAD_CTX*n*_KEY_W3)

The CTXn_KEY_Wm registers provide a 2-dimensional data structure for local OTFAD storage of the 128-bit key for context “n”. There are four consecutive memory-mapped register words containing the key used for the AES calculations associated with the given context. The programming model view of the CTXn_KEY_Wm registers is a little-endian 16-element byte data array, while the 128-bit key is defined as the concatenation of {A0, A1, A2,..., A14, A15}.

Address: 400D_AC00h base + D0Ch offset + (64d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	W3KEY																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OTFAD_CTX*n*_KEY_W3 field descriptions

Field	Description
W3KEY	AES Key The key can be written using the slave peripheral bus. The four consecutive little-endian memory-mapped registers provide 128 bits of key storage. Word0: KEY[31:0][A03, A02, A01, A00] Word1: KEY[31:0][A07, A06, A05, A04] Word2: KEY[31:0][A11, A10, A09, A08] Word3: KEY[31:0][A15, A14, A13, A12]

37.3.8 AES Counter Word0 (OTFAD_CTX*n*_CTR_W0)

The CTXn_CTR_Wm registers provide a 2-dimensional data structure for local OTFAD storage of 64 bits of the counter value for context “n”. There are two consecutive memory-mapped register words defining the upper 96 bits of the counter used for the AES calculations associated with the given context.

The programming model view of the CTXn_CTR_Wm registers is a little-endian 8-element byte data array.

The entire 128-bit counter value is defined as the concatenation of four 32-bit values:

CTR[127–0] = {CTR_W0[C0...C3], CTR_W1[C4...C7], CTR_W0[C0...C3] ^ CTR_W1[C4...C7], systemAddress[31–4], 0h}

Address: 400D_AC00h base + D10h offset + (64d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	W0CTR																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OTFAD_CTX*n*_CTR_W0 field descriptions

Field	Description
W0CTR	AES Counter The upper 64 bits of the counter can be written using the slave peripheral bus. The two consecutive memory-mapped registers directly provide the upper 64 bits of counter storage. Word0: CTR[31:0][C3, C2, C1, C0] Word1: CTR]31:0][C7, C6, C5, C4] The third 32-bit portion of the CTR is formed by exclusive-or’ing the upper 64 bits of the counter as two 32-bit values, while the least-significant portion of the counter is the 32-bit 0-modulo-16 byte system address of the external flash memory. CTR[C0...C15] = {CTR[C0...C7], CTR[C0...C3] ^ CTR[C4...C7], systemAddress[31–4], 0h}

37.3.9 AES Counter Word1 (OTFAD_CTX*n*_CTR_W1)

The CTXn_CTR_Wm registers provide a 2-dimensional data structure for local OTFAD storage of 64 bits of the counter value for context “n”. There are two consecutive memory-mapped register words defining the upper 96 bits of the counter used for the AES calculations associated with the given context.

The programming model view of the CTXn_CTR_Wm registers is a little-endian 8-element byte data array.

The entire 128-bit counter value is defined as the concatenation of four 32-bit values:

CTR[127–0] = {CTR_W0[C0...C3], CTR_W1[C4...C7], CTR_W0[C0...C3] ^ CTR_W1[C4...C7], systemAddress[31–4], 0h}

Address: 400D_AC00h base + D14h offset + (64d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	W1CTR																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OTFAD_CTX*n*_CTR_W1 field descriptions

Field	Description
W1CTR	AES Counter The upper 64 bits of the counter can be written using the slave peripheral bus. The two consecutive memory-mapped registers directly provide the upper 64 bits of counter storage. Word0: CTR[31:0][C3, C2, C1, C0] Word1: CTR]31:0][C7, C6, C5, C4] The third 32-bit portion of the CTR is formed by exclusive-or’ing the upper 64 bits of the counter as two 32-bit values, while the least-significant portion of the counter is the 32-bit 0-modulo-16 byte system address of the external flash memory. CTR[C0...C15] = {CTR[C0...C7], CTR[C0...C3] ^ CTR[C4...C7], systemAddress[31–4], 0h}

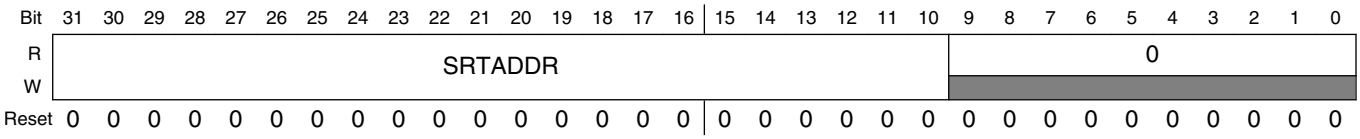
37.3.10 AES Region Descriptor Word0 (OTFAD_CTX*n*_RGD_W0)

The CTXn_RGD_Wm registers provide a 2-dimensional data structure for local OTFAD storage of 64 bits of memory region descriptor for context “n”. There are two consecutive memory-mapped register words defining the starting and ending addresses for the external flash memory region associated with the given context.

Each memory region context defines a specified section of external flash memory associated with the given context and its associated 128-bit key and 128-bit counter values.

The context memory regions are defined as modulo-1024 bytes to match the AMBA-AHB protocol requirement that no bursting transfer cross that boundary. As a result, no AHB command, either single transfer, or any type of wrapping or incrementing burst, can cross any 1 KB boundary. This means that any AHB transfer is limited to a single context for purposes of AES decryption.

Address: 400D_AC00h base + D18h offset + (64d × i), where i=0d to 3d



OTFAD_CTX*n*_RGD_W0 field descriptions

Field	Description
31–10 SRTADDR	Start Address This field defines the most significant bits of the 0-modulo-1024 byte start address of the memory region for context n.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

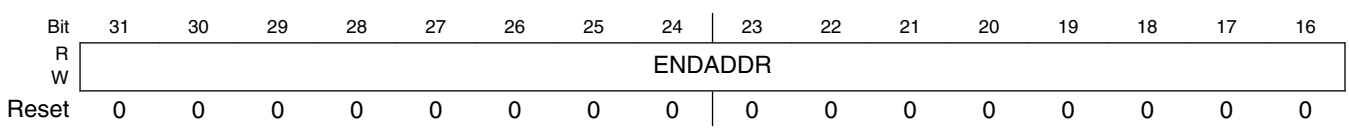
37.3.11 AES Region Descriptor Word1 (OTFAD_CTX*n*_RGD_W1)

The CTXn_RGD_Wm registers provide a 2-dimensional data structure for local OTFAD storage of 64 bits of memory region descriptor for context “n”. There are two consecutive memory-mapped register words defining the starting and ending addresses for the external flash memory region associated with the given context.

Each memory region context defines a specified section of external flash memory associated with the given context and its associated 128-bit key and 128-bit counter values.

The context memory regions are defined as modulo-1024 bytes to match the AMBA-AHB protocol requirement that no bursting transfer cross that boundary. As a result, no AHB command, either single transfer, or any type of wrapping or incrementing burst, can cross any 1 KB boundary. This means that any AHB transfer is limited to a single context for purposes of AES decryption.

Address: 400D_AC00h base + D1Ch offset + (64d × i), where i=0d to 3d



Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ENDADDR						1							RO	ADE	VLD
W																
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0

OTFAD_CTX*n*_RGD_W1 field descriptions

Field	Description
31–10 ENDADDR	End Address This field defines the most significant bits of the 1023-modulo-1024 byte end address of the memory region for context n.
9–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
2 RO	Read-Only This field signals that the entire set of context registers (CTXn_KEY_W[0-3], CTXn_CTR_W[0-1], CTXn_RGD_W[0-1] are read-only and cannot be modified. This field is sticky and remains asserted until the next system reset. SR[RRAM] provides another level of register access control and is independent of the RO indicator. 0 The context registers can be accessed normally (as defined by SR[RRAM]). 1 The context registers are read-only and accesses may be further restricted based on SR[RRAM].
1 ADE	Aes Decryption Enable. For accesses hitting in a valid context, this bit indicates if the fetched data is to be decrypted or simply bypassed. 0 Bypass the fetched data. 1 Perform the CTR-AES128 mode decryption on the fetched data.
0 VLD	Valid This field signals if the context is valid or not. 0 Context is invalid. 1 Context is valid.

37.3.12 Data organization and endianness considerations

OTFAD implements a little-endian memory organization. This affects the data organization of its programming model registers as well as how it handles memory data.

The OTFAD module follows the standard AES definition on data organization and mapping into the bit-oriented cryptographic algorithms. To review these definitions, recall the following:

"The basic unit for processing the AES algorithm is a byte, a sequence of eight bits treated as single entity. The input, output and Cipher Key bit sequences... are processed as arrays of bytes that are formed by dividing these sequences into groups of eight contiguous bits to form arrays of bytes" [1, pp. 8-9].

Further, if an input, output or key is denoted by the AES standard convention as "a", the bytes in the resulting array can be described as a[n], where $0 < n < 16$. The mapping of this byte array data into the required 128-bit sequence produces:

```
data[127:0] = {a[0], a[1], a[2],..., a[14], a[15]}
```

That is, the 128-bit data is formed as the concatenation of the 0th through the 15th byte array element. The OTFAD hardware performs all the required byte "swapping" to convert the programming model view of the keys and counters, etc. from the little endian 32-bit view into the organization required by the AES standard. As an example, consider the mapping of the 128-bit key from its 32-bit programming model registers for the OTFAD AES engine. Let the little-endian memory image of the 128-bit key be defined as a byte-sized, sixteen element array, a[16]. Note A[16] is intended to be an alternate, but equivalent, description:

```
AES Key Word 0[31:0] = {a[ 3], a[ 2], a[ 1], a[ 0]}
AES Key Word 1[31:0] = {a[ 7], a[ 6], a[ 5], a[ 4]}
AES Key Word 2[31:0] = {a[11], a[10], a[ 9], a[ 8]}
AES Key Word 3[31:0] = {a[15], a[14], a[13], a[12]}
```

This data is converted by the OTFAD into a 128-bit key of the form:

```
AES Key[127:0] = {a[0], a[1], a[2], a[3],..., a[12], a[13], a[14], a[15]}
```

Next, consider the 64-bit counter as an eight element byte array, c[8]:

```
AES Counter Word 0[31:0] = {c[ 3], c[ 2], c[ 1], c[ 0]}
AES Counter Word 1[31:0] = {c[ 7], c[ 6], c[ 5], c[ 4]}
```

Before being used, this data is reorganized into the required 128-bit counter value of the form:

```
AES Counter[127:0]  = {c[ 0], c[ 1], c[ 2], c[ 3],  // bits[127:96]
                       c[ 4], c[ 5], c[ 6], c[ 7],  // bits[ 95:64]
                      {c[ 0], c[ 1], c[ 2], c[ 3]}
                    ^ {c[ 4], c[ 5], c[ 6], c[ 7]}, // bits[ 63:32]
                       sysAddr[31:4], 4'b0000}      // bits[ 31: 0]
```

To summarize, the OTFAD programming model registers are organized as little-endian byte-size data arrays and the hardware automatically reorganizes the register data into the 128-bit formats required by AES.

Note that since OTFAD is a little-endian design, it processes each 64 bits of external memory data fetched by the QuadSPI using the following mapping for data byte array:

```
mem_wr_data[63:0]
= {data[i+7],data[i+6],data[i+5],data[i+4],data[i+3],data[i+2],data[i+1],data[i+0]}
```

37.4 Functional description

This section provides more details on the operation and implementation of the OTFAD.

37.4.1 CTR-AES128 mode basics

When processing data fetched from an external memory, the OTFAD implements the CTR-AES128 mode for on-the-fly decryption.

The OTFAD engine implements a block cipher mode of operation, specifically supporting counter mode (CTR). The CTR mode "provides a confidentiality mode that features the application of the forward cipher (encryption) to a set of input blocks, called counters, to produce a sequence of output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa." [2]

The block cipher was selected for two reasons: 1) it produces a cryptographically stronger solution than the simple Electronic Cookbook (ECB) mode since each block in the sequence is different than every other block, even for the same input data, and 2) the definition of CTR mode allows the 128-bit counter values to include the system memory address of the referenced flash block and to be computed in advance of their actual usage to convert the ciphertext back into plaintext for the requesting bus master device in the microprocessor - typically the CPU itself.

As a result, the OTFAD module adds zero cycles of additional latency to decrypt the code and data fetched from the external flash memory. The combined support for the CTR-AES128 mode plus an aggressive, pipelined implementation of the OTFAD performing up to 3 rounds in a single machine cycle allowing the engine to keep pace with the fastest data arrival rates.

Figure 37-3 presents an overview of both the CTR-AES128 encrypt and decrypt operations.

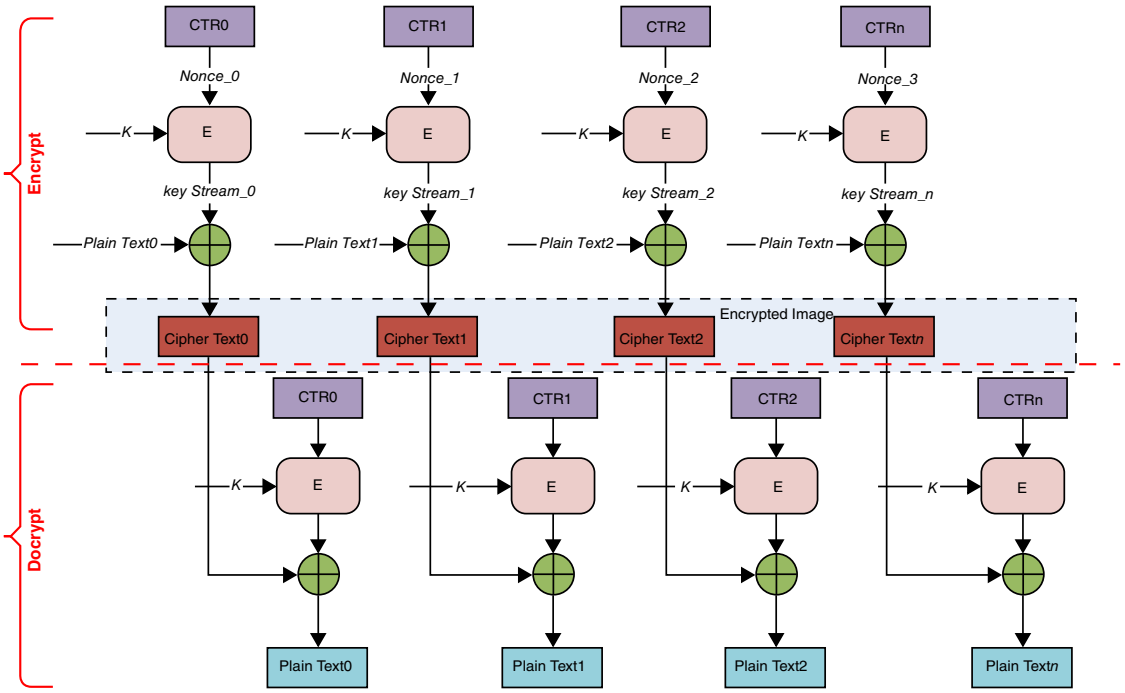


Figure 37-3. CTR-AES1288 encrypt and decrypt overview

As shown in Figure 37-3, CTR-AES128 scheme combines a unique 128-bit counter (CTR*n*) with a 128-bit key (K) to encrypt (Ciphertext*n*) or decrypt (Plaintext*n*) each 128 bit data block.

Authorized software executes the "encrypt" portion to create the ciphertext image stored in the external memory, while the OTFAD module, in conjunction with the QuadSPI external memory controller, executes the "decrypt" portion.

Consider these two basic operations in more detail.

For encryption, the 0-modulo-16 byte system address is combined with 96 bits of counter information defined in the memory context registers to produce a unique 128-bit CTRn value for each data block. Specifically, the OTFAD's implementation defines the 128-bit CTR*n* for memory context "x" as the concatenation of 4 values:

```
CTRn_x[127-0] = {CTR_W0_x[C0...C3],                    // 32 bits of pre-programmed CTR
                 CTR_W1_x[C4...C7],                    // another 32 bits of CTR
                 CTR_W0_x[C0...C3] ^ CTR_W1_x[C4...C7], // exclusive-OR of CTR values
                 systemAddress[31-4], 0000b}           // 0-modulo-16 system address
```

NOTE

The addresses used by both (software) encryption and OTFAD decryption are the physical system addresses associated with the QuadSPI, never the code alias addresses.

Software uses this CTR*n* value as the data input to the AES128 encryption process (E) to produce the Key_Stream_*n* output. The final step in encryption is to exclusive-OR the Key_Stream_n value with the data block's plaintext to create the 128-bit block of Ciphertextn which is stored in the external memory. This process is then repeated for each 16-bit data block of the code and data image needing encryption.

The OTFAD's decryption process begins by inputting the same CTRn value and same key K to the AES128 encryption process (E) to generate a 128-bit encrypted counter (ECTR*n*, not explicitly labeled in Figure 37-3). The ECTR*n* is exclusive-OR'ed with the Ciphertext*n* to produce the Plaintext*n*. The 128-bit key (K) is defined in the KEY_W[0-3]_x registers for context "x".

Since the encrypted counter value is *not* dependent on the ciphertext, it can be pre-calculated in response to a system bus access request such that the OTFAD only needs to perform the exclusive-OR once the ciphertext has been fetched from the external memory. This is the key concept in allowing the OTFAD to add zero incremental cycles of fetch latency.

For additional details on the OTFAD's processing during a 32-byte burst read, see Typical OTFAD CTR-AES128 decryption operation.

37.4.2 Microarchitecture overview

This section provides additional details on the hardware implementation. The following subsections provide details on the hardware decryption operations, and key blob processing. Refer to the block diagrams of Figure 37-1 and Figure 37-2.

37.4.2.1 Context determination

The first step in a CTR-AES128 decryption is the determination of the external memory context.

The OTFAD supports four memory contexts where each has its own 128-bit key, 64-bits of counter and a 64-bit memory region descriptor. The region descriptor includes start and end addresses plus three bits of control and configuration. See AES Region Descriptor Word0 (OTFAD_CTX*n*_RGD_W0) and AES Region Descriptor Word1 (OTFAD_CTX*n*_RGD_W1) for details.

NOTE

Always use an address range within the physical address space assigned to the QuadSPI module when defining an external

memory context in a region descriptor, even if the system application uses the aliased area of the QuadSPI module.

As shown in Figure 37-2 in the upper right portion of the block diagram, the system address (SYSADDR) is compared to the start and end addresses of each context to determine a region "hit". To determine if the current reference hits in a given context, two magnitude comparators are used in conjunction with the region's start and end addresses. The boolean equation for this portion of the hit determination is defined as:

```
context_hit_n
      = ((addr[31:10] >= rgd_w0_n[srtaddr]) & (addr[31:10] <= rgd_w1_n[endaddr]))
      & rgd_w1_n[vld]
```

where `addr[*]` is the current system reference address, `rgd_w0_n[srtaddr]` and `rgd_w1_n[endaddr]` are the start and end addresses, and `rgd_w1_n[vld]` is the valid bit, all from context region descriptor n.

There are no hardware checks to verify that `rgd_w1_n[endaddr] ≥ rgd_w0_n[srtaddr]`, and it is software's responsibility to load appropriate values into these fields of the context region descriptor.

Recall the context memory regions are defined as modulo-1024 byte values to match the AMBA-AHB protocol requirement that no bursting transfer cross that boundary. The result is that each AHB transfer, regardless of access size or length, is limited to a single context for purposes of AES decryption.

Since each context has unique key and counter values, the OTFAD does not support any form of memory region overlap. For system accesses that hit in multiple contexts or no contexts, the fetched data is simply bypassed.

For accesses that hit in a single context, there is a separate register bit (RGD_W1_n[ADE]) that enables AES decryption or a simple bypass of the fetched data. Based on the hit determination and the state of the ADE indicator, the appropriate 128-bit key and 64 bit counter are selected from the context registers.

37.4.2.2 AES engine and encrypted counter generation

Once the appropriate context has been determined and the corresponding key and counter values selected, the OTFAD proceeds with the generation of the encrypted counters. Since the dominant QuadSPI system bus reference is a 64-bit WRAP4 burst transfer in response to a cache miss, the OTFAD is optimized for this transaction type. The subsequent discussion is described in terms of the 64-bit WRAP4 transfer.

As the 64-bit WRAP4 accesses 32 bytes of data, the OTFAD calculates two 128-bit encrypted counters since there are two AES128 data blocks referenced by this transaction. Since external flash SPI memories typically do not support any type of address wrapping, the QuadSPI forces the external fetches to begin at the corresponding 0-modulo-size address. Accordingly, the OTFAD calculates the (first) encrypted counter associated with system address 0-modulo-32, and then the (second) address 16-modulo-32. The two encrypted counter calculations are performed in the AES Engine shown in the middle of Figure 37-2 as the QuadSPI is making the external flash fetches.

As each encrypted counter is generated, the 128-bit value is stored in one of the two data registers connected to the AES Engine output.

Recall the OTFAD's AES Engine is heavily pipelined, performing up to 3 rounds per cycle, so the encryption speed (4 cycles total) matches the fastest data arrival rate.

Each AES round performs 4 different data transformations:

- Byte substitution
- State array row shift
- State array column mix
- Round key addition

Recall the QuadSPI initiated the external fetch at a 0-modulo-32 address, so as the decrypted data is fetched and presented to the OTFAD, it uses the first encrypted counter to perform the required exclusive-OR operation to generate the corresponding plaintext. The generated plaintext is output to the QuadSPI's AHB RAM buffer to be written into that memory (which operates as a small cache for QuadSPI accesses). See Figure 37-1. This process continues as each of the four fetches of the 64-bit WRAP4 burst is presented to the OTFAD, decrypted and then sent to the AHB RAM buffer.

37.4.2.3 Decrypted data buffer operation

Although the QuadSPI initiated its external fetches from a 0-modulo-32 address, the system bus transaction does not have any restrictions about its starting address and can begin at any of the 64-bit addresses. So, as the sequential fetched data is decrypted by the OTFAD, the resulting plaintext is also loaded into three 64-bit decrypted data buffers as shown near the bottom of Figure 37-2.

Depending on the original address of the system bus reference, the OTFAD either decrypts and outputs data to *both* the AHB RAM buffer and the system bus, or registers the decrypted data so it can be sourced later after the system bus address "wraps". Consider the following two examples: first, examine the sequencing on a 64-bit WRAP4 with an original address of 0x00, and a second example with a starting address of 0x18.

In both examples, the QuadSPI's fetch addresses are {0x00, 0x08, 0x10, 0x18}. In the first example, the system bus addresses are {0x00, 0x08, 0x10, 0x18}, while in the second example, the sequence is {0x18, 0x00, 0x08, 0x10}. See Table 37-2 for a description of the operations for these two examples.

Table 37-2. OTFAD and decrypted data buffer operation

QuadSPI fetch	SystemBus fetch	Description
Example 1		**64-bit WRAP4, miss @ 0x00**
0x00	0x00	OTFAD decrypts data and simultaneously sends to AHB RAM Buffer and SystemBus
0x08	0x08	OTFAD decrypts data and simultaneously sends to AHB RAM Buffer and SystemBus
0x10	0x10	OTFAD decrypts data and simultaneously sends to AHB RAM Buffer and SystemBus
0x18	0x18	OTFAD decrypts data and simultaneously sends to AHB RAM Buffer and SystemBus
Example 2		**64-bit WRAP4, miss @ 0x18**
0x00	0x18	OTFAD decrypts data, sends to AHB RAM Buffer and loads into Decrypted Data Buffer 0, SystemBus read is stalled
0x08	0x18	OTFAD decrypts data, sends to AHB RAM Buffer and loads into Decrypted Data Buffer 1, SystemBus read is stalled
0x10	0x18	OTFAD decrypts data, sends to AHB RAM Buffer and loads into Decrypted Data Buffer 2, SystemBus read is stalled
0x18	0x18	OTFAD decrypts data and simultaneously sends to AHB RAM Buffer and SystemBus
	0x00	OTFAD sources data from decrypted data buffer 0
	0x08	OTFAD sources data from decrypted data buffer 1
	0x10	OTFAD sources data from decrypted data buffer 2

The resulting behavior from the combined QuadSPI + OTFAD provides the best system performance. For longer burst sizes, for example, 64-bit WRAP8 and 64-bit WRAP16, the implemented number of decrypted data buffers is not sufficient to temporary store the entire burst. In these cases, the three OTFAD buffers are used in conjunction with "hits" from the AHB RAM Buffer to source the decrypted data back to the system bus.

A simplified (partial) timing diagram for the 64-bit WRAP4 burst of Example 1 is shown in Figure 37-4.

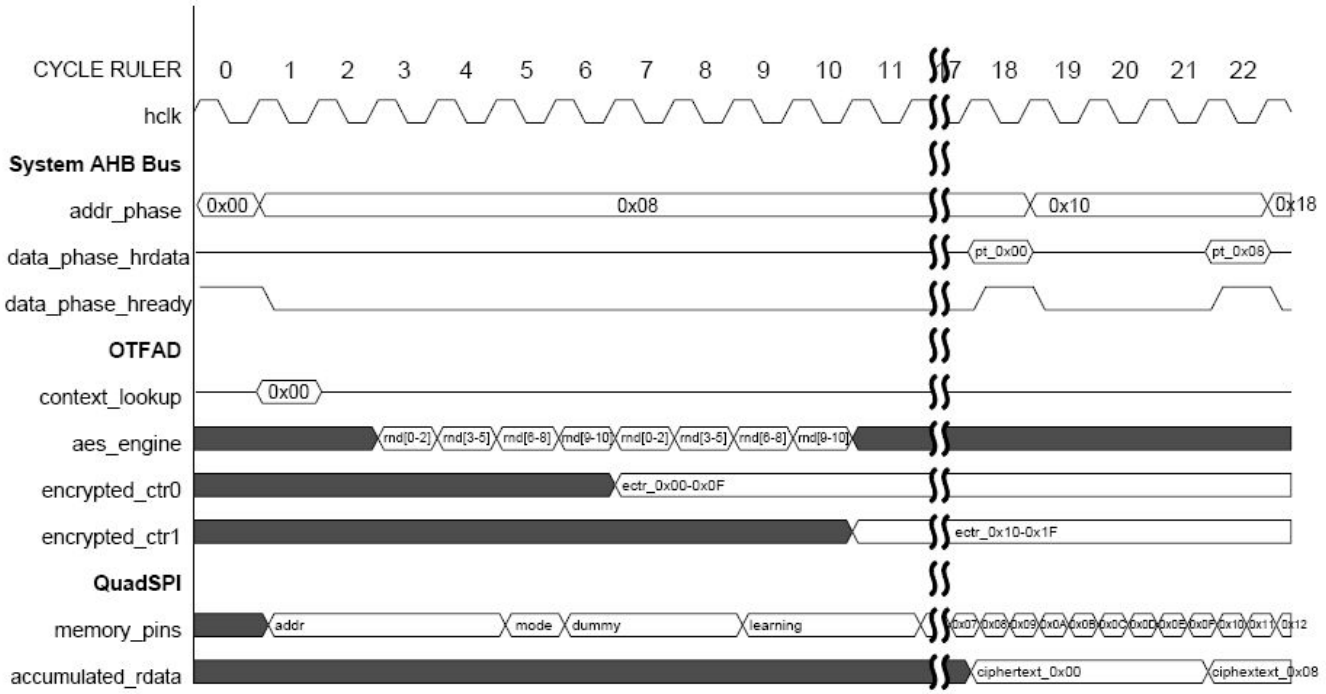


Figure 37-4. OTFAD 64-bit WRAP4 burst timing diagram

In Figure 37-4, the system AHB read data bus "pt_<burst_offset>" is meant to refer to decrypted plaintext data. The zero cycle incremental delay to perform the required CTR-AES128 decryption is visible in cycles 18 (the doubleword at burst offset 0×00) and 22 (doubleword at burst offset 0×08).

37.5 Initialization information

37.5.1 OTFAD configuration details

The operating configuration of the OTFAD is controlled by a number of static input signals plus programmable bits in the Control Register. The three basic modes are discussed in Modes of operation and OTFAD operating modes. This section focuses on the configuration capabilities associated with Normal mode (SR[MODE] = 00).

There is a static input signal and an associated CR bit that define various configuration features. In all cases, the static input signal and the associated CR bit are logically summed (OR'd) together to form an "effective" configuration bit. The combined control is visible via a slave peripheral bus CR read. For a hierarchical view of increasing normal mode capabilities, see Table 37-3.

Table 37-3. OTFAD normal mode configurations

otfad_enable | CR[GE]	Description
0	1) OTFAD operates with all data decryption disabled; QuadSPI fetched data is simply bypassed.
1	2) Basic OTFAD processing is enabled; decryptions are enabled based on context n “hit” and RGD_W1_n[ADE, VLD].

In addition to the static configuration inputs and associated CR bits shown in Table 37-3, there is one additional set: a static configuration input and CR[RRAE]. When either the configuration input signal or CR[RRAE] is asserted, only the CR, SR and CRC registers can be accessed; attempted accesses of all other registers are treated as read-as-zero, write-ignore.

For all configuration bits, the intended use case is to layer increasing OTFAD functionality into the system, first using the programmable CR indicators, and then, after the behavior has been fully debugged, to program the corresponding static input signals to define a “permanent” configuration.

37.6 Application information

37.6.1 OTFAD operating modes

As discussed in Modes of operation, the OTFAD supports three modes of operation as defined by input configuration and control signals. The mode states and their transitions are shown in Figure 37-5. The states include Normal Mode (00), Security Violation Mode (10), and Logically Disabled Mode (11). The operating mode state information is visible in the SR[MODE] field.

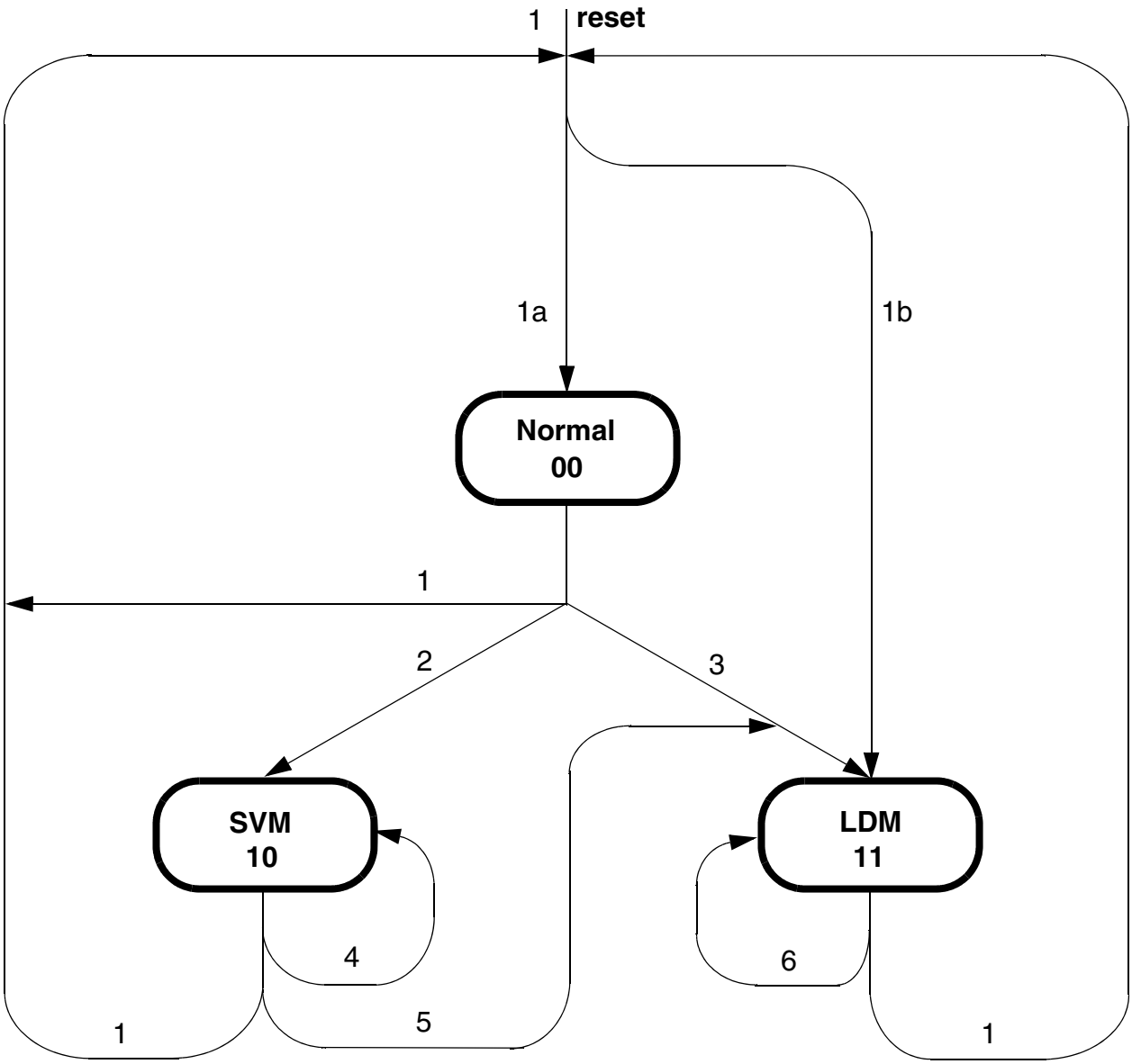


Figure 37-5. OTFAD Operating Mode States and Transitions

The state transitions are defined in Table 37-4.

Table 37-4. OTFAD mode state transitions

Current state	Next state	Transition	Description
–	Normal, LDM	1 -> 1a, 1b	Any reset event initializes the OTFAD mode state.
–	Normal	1a	Any reset, combined with a negated otfad_disable_override configuration input signal, unconditionally forces OTFAD into the Normal state.
–	LDM	1b	Any reset, combined with an asserted otfad_disable_override configuration input signal, unconditionally forces OTFAD into the LDM state.

Table continues on the next page...

Table 37-4. OTFAD mode state transitions (continued)

Current state	Next state	Transition	Description
Normal	SVM	2	A transition from Normal to SVM is made when the boolean expression ((soc_security_violation | nvm_mass_erase | cr[fsvm] & ~cr[fldm]) & ~reset) is true.
Normal	LDM	3	A transition from Normal to LDM is made when the boolean expression (cr[fldm] & ~reset) is true.
SVM	SVM	4	The SVM state is retained while the boolean expression (~cr[fldm] & ~reset) is true.
SVM	LDM	5	A transition from SVM to LDM occurs when the boolean expression (cr[fldm] & ~reset) is true.
LDM	LDM	6	The LDM is retained while reset is not asserted.

37.6.2 Typical OTFAD CTR-AES128 decryption operation

The dominant use case in normal mode is expected to be CTR-AES128 decryption operations performed in response to a 64-bit WRAP4 burst read in response to a processor cache miss. The following C code is a simplified representation of the OTFAD processing associated with this use case. The ciphertext fetched by the QuadSPI is the `quadspi_ciphertext[32]` byte array, and the resulting decrypted data is `otfad_plaintext[32]`. See Listing 37-1 on page 1044.

Listing 37-1. Basic OTFAD 32-byte decryption processing

```
void KeyExpansion (unsigned char ckey[], int nbits, unsigned int w[]);
void Cipher (unsigned char cin[], unsigned int w[], int nr, unsigned char cout[]);

unsigned char                          quadspi_ciphertext[32];
unsigned char                          otfad_plaintext[32];

union context_regs {
     volatile unsigned char      key[16];
     volatile unsigned char      ctr[8];
     volatile unsigned int      rgd[2];
     volatile unsigned int      unused_filler[8]
     } otfad_context[4];

void otfad_32byte_processing (unsigned int sys_addr,
                                        unsigned char quadspi_ciphertext[],
                                        unsigned char otfad_plaintext[])

{
     unsigned int      i;
     unsigned int      ctx_hit;
     unsigned int      combined_hits;
     unsigned int      enable_decryption;
     unsigned int      w[44];            // expanded key
     unsigned char      encrypted_ctr[2][16];
     unsigned char      temp_ctr[16];
     unsigned int      local_addr;
     unsigned int      hit_addr;

     local_addr &= 0xfffffff0;      // force byte addr to 0-mod-16 (aes size)
     hit_addr = local_addr & 0xfffffc00;      // force hit addr to 0-mod-1K
```

```
// context determination
combined_hits = 0;           // 4-bit hit indicator: ctx{3,2,1,0}
for (i = 0; i < 4; i++) {
     ctx_hit = ((hit_addr >= otfad_context[i].rgd[0])      // srtaddr
          & (hit_addr <= otfad_context[i].rgd[1]))      // endaddr
          & (otfad_context[i].rgd[i] & 1);           // vld
     combined_hits += (ctx_hit << i);
}
// check combined_hits to determine if decryption is enabled
enable_decryption = 0;
switch (combined_hits) {
     case 1:                      // ctx0 hit
          ctx_hit = 0;
          if ((otfad_context[0].rgd[1] & 2) != 0) {      // ade
               enable_decryption = 1;
          }
          break;
     case 2:                      // ctx1 hit
          ctx_hit = 1;
          if ((otfad_context[1].rgd[1] & 2) != 0) {      // ade
               enable_decryption = 1;
          }
          break;
     case 4:                      // ctx2 hit
          ctx_hit = 2;
          if ((otfad_context[2].rgd[1] & 2) != 0) {      // ade
               enable_decryption = 1;
          }
          break;
     case 8:                      // ctx3 hit
          ctx_hit = 3;
          if ((otfad_context[3].rgd[1] & 2) != 0) {      // ade
               enable_decryption = 1;
          }
          break;
     default:                      // none or multiple ctx hits
          ctx_hit = 0;
               enable_decryption = 0;           // no decryption, bypass data
     break;
     }

// clear encrypted counters
for (i = 0; i < 16; i++) {
     encrypted_ctr[0][i] = 0;
     encrypted_ctr[1][i] = 0;
}

// if decryption is enabled, calculate two encrypted counter values
if (enable_decryption == 1) {
     KeyExpansion (&otfad_context[ctx_hit].key[0], 128, w);
     // encrypt the counter for the 1st 16 bytes
          // step 1: generate the 128-bit counter
          // step 1a: first 8 bytes are taken directly from context.ctr[]
          for (i = 0; i < 8; i++) {
               temp_ctr[i] = otfad_context[ctx_hit].ctr[i];
          }
          // step 1b: next 4 bytes are xor of ctr[0-3] ^ ctr[4-7]
          temp_ctr[8] = temp_ctr[0] ^ temp_ctr[4];
          temp_ctr[9] = temp_ctr[1] ^ temp_ctr[5];
          temp_ctr[10] = temp_ctr[2] ^ temp_ctr[6];
          temp_ctr[11] = temp_ctr[3] ^ temp_ctr[7];
          // step 1c: final 4 bytes are local_addr
          temp_ctr[12] = (local_addr & 0xff000000) >> 24;
          temp_ctr[13] = (local_addr & 0x00ff0000) >> 16;
          temp_ctr[14] = (local_addr & 0x0000ff00) >> 8;
          temp_ctr[15] = (local_addr & 0x000000ff);

     // step 2: perform the 1st counter encryption
     Cipher (&temp_ctr[0], w, 10, &encrypted_ctr[0][0]);
```

```
            // encrypt the counter for the 2nd 16 bytes
                 // step 1a: increment the local_addr by 16
                 local_addr += 16;
                 // step 1b: final 4 bytes of counter are new local_addr
                 temp_ctr[12] = (local_addr & 0xff000000) >> 24;
                 temp_ctr[13] = (local_addr & 0x00ff0000) >> 16;
                 temp_ctr[14] = (local_addr & 0x0000ff00) >> 8;
                 temp_ctr[15] = (local_addr & 0x000000ff);

            // step 2: perform the 2nd counter encryption
            Cipher (&temp_ctr[0], w, 10, &encrypted_ctr[1][0]);
            }

            // generate plaintext data = f(encrypted_ctr[][], quadspi_ciphertext[])
            // for bypass operations, the encrypted_ctr[][] = 0, so plain = cipher
            // since quadspi_ciphertext arrives 8 bytes at a time, code does the same...
            for (i = 0; i < 8; i++)
                 otfad_plaintext[i]      = encrypted_ctr[0][i]      ^ quadspi_ciphertext[i];
            for (i = 8; i < 16; i++)
                 otfad_plaintext[i]      = encrypted_ctr[0][i]      ^ quadspi_ciphertext[i];
            for (i = 16; i < 24; i++)
                 otfad_plaintext[i]      = encrypted_ctr[1][i-16]      ^ quadspi_ciphertext[i];
            for (i = 24; i < 32; i++)
                 otfad_plaintext[i]      = encrypted_ctr[1][i-16]      ^ quadspi_ciphertext[i];
}
```

37.6.3 Context CRC

The OTFAD supports the capability to calculate a standard CRC32 across any arbitrary-sized external flash memory region. The image to be checked can be either decrypted ciphertext or bypassed plaintext. The following steps must be followed to enable this capability:

1. Configure a single context *n* to be checked.
2. The context CRC checking is enabled by setting CR[CRCI = 1, CRCE = 1, CCTX = *n*].
3. Typically, a DMA channel is used to fetch the external flash data to be checked. The fetches of the external flash data to be checked must be sequential fetches made with 64-bit single accesses or 0-modulo-size 64-bit WRAP{4,8,16} burst accesses. Alternatively, 0-modulo-size 32-bit WRAP{4,8,16} burst accesses may be used. The QuadSPI must be configured such that all fetches generate the external flash accesses and speculative prefetching is disabled. A processor core may be used to perform the required data fetches as long as the specified fetch sizes and types are used. Note that the recommended access types and sizes are typically supported by DMAs or processor cores for cache miss line fills. Use of any other access types or other configurations produces UNPREDICTABLE results.
4. As the external flash accesses are made and sent to the OTFAD, the resulting decrypted ciphertext or bypassed plaintext is routed to the check logic where it is accumulated in the CRC register.

5. When the fetch of the entire image to be checked is complete, the contents of the CRC register can be compared versus the expected CRC32 value under software control.

Chapter 38
External Bus Interface (FlexBus)

38.1 Chip-specific Flexbus information

38.1.1 FlexBus clocking

The system provides a dedicated clock source to the FlexBus module's external CLKOUT. Its clock frequency is derived from a divider of the MCGOUTCLK. See Clock Distribution for more details.

38.1.2 FlexBus signal multiplexing

The multiplexing of the FlexBus address and data signals is controlled by the port control module. However, the multiplexing of some of the FlexBus control signals are controlled by the port control and FlexBus modules. The port control module registers control whether the FlexBus or another module signals are available on the external pin, while the FlexBus's CSPMCR register configures which FlexBus signals and/or SDRAM_DQMx signals are available from the modules. The control signals are grouped as illustrated:

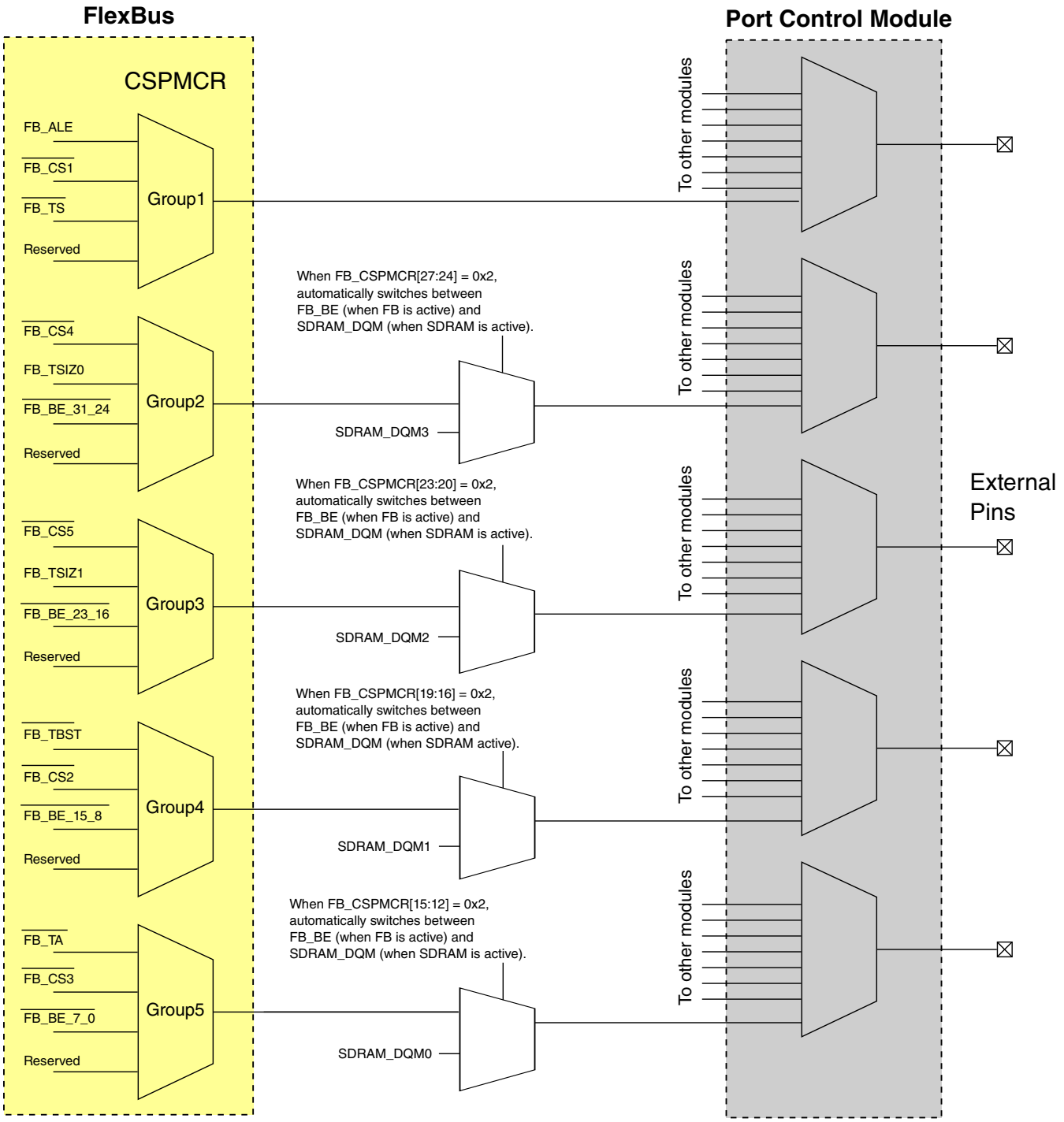


Figure 38-1. FlexBus control signal multiplexing

Therefore, use the CSPMCR and port control registers to configure which control signal is available on the external pin. All control signals, except for $\overline{\text{FB_TA}}$, are assigned to the ALT5 function in the port control module. Since, unlike the other control signals, $\overline{\text{FB_TA}}$ is an input signal, it is assigned to the ALT6 function.

38.1.3 FlexBus CSCR0 reset value

On this device the CSCR0 resets to 0x003F_FC00. Configure this register as needed before performing any FlexBus access.

38.1.4 FlexBus Security

When security is enabled on the device, FlexBus accesses may be restricted by configuring SIM_SOPT2[FBSL]. See System Integration Module (SIM) for details.

38.1.5 FlexBus line transfers

Line transfers are not possible from the ARM Cortex-M4 core. Ignore any references to line transfers in the FlexBus chapter.

38.2 Introduction

This chapter describes external bus data transfer operations and error conditions. It describes transfers initiated by the core processor (or any other bus master) and includes detailed timing diagrams showing the interaction of signals in supported bus operations.

38.2.1 Definition

The FlexBus multifunction external bus interface controller is a hardware module that:

- Provides memory expansion and provides connection to external peripherals with a parallel bus
- Can be directly connected to the following asynchronous or synchronous slave-only devices with little or no additional circuitry:
  - External ROMs
  - Flash memories

- Programmable logic devices
- Other simple target (slave) devices

38.2.2 Features

FlexBus offers the following features:

- Six independent, user-programmable chip-select signals ($\overline{\text{FB_CS5}}$ –$\overline{\text{FB_CS0}}$)
- 8-bit, 16-bit, and 32-bit transfers
- Programmable burst and burst-inhibited transfers selectable for each chip-select and transfer direction
- Programmable address-setup time with respect to the assertion of a chip-select
- Programmable address-hold time with respect to the deassertion of a chip-select and transfer direction
- Extended address latch enable option to assist with glueless connections to synchronous and asynchronous memory devices

38.3 Signal descriptions

This table describes the external signals involved in data-transfer operations.

NOTE

Not all of the following signals may be available on a particular device. See the Chip Configuration details for information on which signals are available.

Table 38-1. FlexBus signal descriptions

Signal	I/O	Function
FB_AD31 - FB_AD0	I/O	This is the address and data bus, FB_AD. The number of byte lanes carrying the data is determined by the port size associated with the matching chip-select. The full 32-bit address is driven on the first clock of a bus cycle (address phase). After the first clock, the data is driven on the bus (data phase). During the data phase, the address is driven on the pins not used for data. For example, in 16-bit mode, the lower address is driven on FB_AD15–FB_AD0, and in 8-bit mode, the lower address is driven on FB_AD23–FB_AD0.
$\overline{\text{FB_CS5}}$–$\overline{\text{FB_CS0}}$	O	General Purpose Chip-Selects—Indicate which external memory or peripheral is selected. A particular chip-select is asserted when the transfer address is within the external memory's or peripheral's address space, as defined in CSAR[BA] and CSMR[BAM].

Table continues on the next page...

Table 38-1. FlexBus signal descriptions (continued)

Signal	I/O	Function
FB_BE_31_24 FB_BE_23_16 FB_BE_15_8 FB_BE_7_0	O	Byte Enables—Indicate that data is to be latched or driven onto a specific byte lane of the data bus. CSCR[BEM] determines if these signals are asserted on reads and writes or on writes only. For external SRAM or flash devices, the FB_BE outputs should be connected to individual byte strobe signals.
FB_OE	O	Output Enable—Sent to the external memory or peripheral to enable a read transfer. This signal is asserted during read accesses only when a chip-select matches the current address decode.
FB_R/W	O	Read/Write—Indicates whether the current bus operation is a read operation (FB_R/W high) or a write operation (FB_R/W low).
FB_TS	O	Transfer Start—Indicates that the chip has begun a bus transaction and that the address and attributes are valid. An inverted FB_TS is available as an address latch enable (FB_ALE), which indicates when the address is being driven on the FB_AD bus. FB_TS/FB_ALE is asserted for one bus clock cycle. The chip can extend this signal until the first positive clock edge after FB_CS asserts. See CSCR[EXTS] and Extended Transfer Start/Address Latch Enable.
FB_ALE	O	Address Latch Enable—Indicates when the address is being driven on the FB_A bus (inverse of FB_TS).
FB_TSIZ1–FB_TSIZ0	O	Transfer Size—Indicates (along with FB_TBST) the data transfer size of the current bus operation. The interface supports 8-, 16-, and 32-bit operand transfers and allows accesses to 8-, 16-, and 32-bit data ports. • 00b = 4 bytes • 01b = 1 byte • 10b = 2 bytes • 11b = 16 bytes (line) For misaligned transfers, FB_TSIZ1–FB_TSIZ0 indicate the size of each transfer. For example, if a 32-bit access through a 32-bit port device occurs at a misaligned offset of 1h, 8 bits are transferred first (FB_TSIZ1–FB_TSIZ0 = 01b), 16 bits are transferred next at offset 2h (FB_TSIZ1–FB_TSIZ0 = 10b), and the final 8 bits are transferred at offset 4h (FB_TSIZ1–FB_TSIZ0 = 01b). For aligned transfers larger than the port size, FB_TSIZ1–FB_TSIZ0 behave as follows: • If bursting is used, FB_TSIZ1–FB_TSIZ0 are driven to the transfer size. • If bursting is inhibited, FB_TSIZ1–FB_TSIZ0 first show the entire transfer size and then show the port size. For burst-inhibited transfers, FB_TSIZ1–FB_TSIZ0 change with each FB_TS assertion to reflect the next transfer size. For transfers to port sizes smaller than the transfer size, FB_TSIZ1–FB_TSIZ0 indicate the size of the entire transfer on the first access and the size of the current port transfer on subsequent transfers. For example, for a 32-bit write to an 8-bit port, FB_TSIZ1–FB_TSIZ0 are 00b for the first transaction and 01b for the next three transactions. If bursting is used for a 32-bit write to an 8-bit port, FB_TSIZ1–FB_TSIZ0 are driven to 00b for the entire transfer.

Table continues on the next page...

Table 38-1. FlexBus signal descriptions (continued)

Signal	I/O	Function
FB_TBST	O	Transfer Burst—Indicates that a burst transfer is in progress as driven by the chip. A burst transfer can be 2 to 16 beats depending on FB_TSIZ1–FB_TSIZ0 and the port size. **Note:** When a burst transfer is in progress (FB_TBST = 0b), the transfer size is 16 bytes (FB_TSIZ1–FB_TSIZ0 = 11b), and the address is misaligned within the 16-byte boundary, the external memory or peripheral must be able to wrap around the address.
FB_TA	I	Transfer Acknowledge—Indicates that the external data transfer is complete. When FB_TA is asserted during a read transfer, FlexBus latches the data and then terminates the transfer. When FB_TA is asserted during a write transfer, the transfer is terminated. If auto-acknowledge is disabled (CSCR[AA] = 0), the external memory or peripheral drives FB_TA to terminate the transfer. If auto-acknowledge is enabled (CSCR[AA] = 1), FB_TA is generated internally after a specified number of wait states, or the external memory or peripheral may assert external FB_TA before the wait-state countdown to terminate the transfer early. The chip deasserts FB_CS one cycle after the last FB_TA is asserted. During read transfers, the external memory or peripheral must continue to drive data until FB_TA is recognized. For write transfers, the chip continues driving data one clock cycle after FB_CS is deasserted. The number of wait states is determined by CSCR or the external FB_TA input. If the external FB_TA is used, the external memory or peripheral has complete control of the number of wait states. **Note:** External memory or peripherals should assert FB_TA only while the FB_CS signal to the external memory or peripheral is asserted. The CSPMCR register controls muxing of FB_TA with other signals. When the CSPMCR register does not allow fb_ta control, auto-acknowledge must be used (CSCR[AA] =1'b1); otherwise the bus may hang.
FB_CLK	O	FlexBus Clock Output

38.4 Memory Map/Register Definition

The following tables describe the registers and bit meanings for configuring chip-select operation.

The actual number of chip selects available depends upon the device and its pin configuration. If the device does not support certain chip select signals or the pin is not configured for a chip-select function, then that corresponding set of chip-select registers has no effect on an external pin.

Note

You must set CSMR0[V] before the chip select registers take effect.

A bus error occurs when writing to reserved register locations.

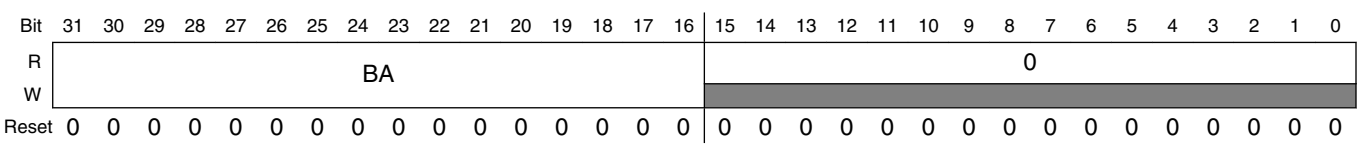
FB memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4000_C000	Chip Select Address Register (FB_CSAR0)	32	R/W	0000_0000h	38.4.1/1055
4000_C004	Chip Select Mask Register (FB_CSMR0)	32	R/W	0000_0000h	38.4.2/1056
4000_C008	Chip Select Control Register (FB_CSCR0)	32	R/W	Undefined	38.4.3/1057
4000_C00C	Chip Select Address Register (FB_CSAR1)	32	R/W	0000_0000h	38.4.1/1055
4000_C010	Chip Select Mask Register (FB_CSMR1)	32	R/W	0000_0000h	38.4.2/1056
4000_C014	Chip Select Control Register (FB_CSCR1)	32	R/W	Undefined	38.4.3/1057
4000_C018	Chip Select Address Register (FB_CSAR2)	32	R/W	0000_0000h	38.4.1/1055
4000_C01C	Chip Select Mask Register (FB_CSMR2)	32	R/W	0000_0000h	38.4.2/1056
4000_C020	Chip Select Control Register (FB_CSCR2)	32	R/W	Undefined	38.4.3/1057
4000_C024	Chip Select Address Register (FB_CSAR3)	32	R/W	0000_0000h	38.4.1/1055
4000_C028	Chip Select Mask Register (FB_CSMR3)	32	R/W	0000_0000h	38.4.2/1056
4000_C02C	Chip Select Control Register (FB_CSCR3)	32	R/W	Undefined	38.4.3/1057
4000_C030	Chip Select Address Register (FB_CSAR4)	32	R/W	0000_0000h	38.4.1/1055
4000_C034	Chip Select Mask Register (FB_CSMR4)	32	R/W	0000_0000h	38.4.2/1056
4000_C038	Chip Select Control Register (FB_CSCR4)	32	R/W	Undefined	38.4.3/1057
4000_C03C	Chip Select Address Register (FB_CSAR5)	32	R/W	0000_0000h	38.4.1/1055
4000_C040	Chip Select Mask Register (FB_CSMR5)	32	R/W	0000_0000h	38.4.2/1056
4000_C044	Chip Select Control Register (FB_CSCR5)	32	R/W	Undefined	38.4.3/1057
4000_C060	Chip Select port Multiplexing Control Register (FB_CSPMCR)	32	R/W	0000_0000h	38.4.4/1060

38.4.1 Chip Select Address Register (FB_CSAR*n*)

Specifies the associated chip-select's base address.

Address: 4000_C000h base + 0h offset + (12d × i), where i=0d to 5d



FB_CSAR*n* field descriptions

Field	Description
31–16 BA	Base Address Defines the base address for memory dedicated to the associated chip-select. BA is compared to bits 31–16 on the internal address bus to determine if the associated chip-select's memory is being accessed.

Table continues on the next page...

FB_CSAR*n* field descriptions (continued)

Field	Description
	NOTE: Because the FlexBus module is one of the slaves connected to the crossbar switch, it is only accessible within a certain memory range. See the chip memory map for the applicable FlexBus "expansion" address range for which the chip-selects can be active. Set the CSARn and CSMRn registers appropriately before accessing this region.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

38.4.2 Chip Select Mask Register (FB_CSMR*n*)

Specifies the address mask and allowable access types for the associated chip-select.

Address: 4000_C000h base + 4h offset + (12d × i), where i=0d to 5d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	BAM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0							WP	0							V
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FB_CSMR*n* field descriptions

Field	Description
31–16 BAM	Base Address Mask Defines the associated chip-select's block size by masking address bits. 0 The corresponding address bit in CSAR is used in the chip-select decode. 1 The corresponding address bit in CSAR is a don't care in the chip-select decode.
15–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 WP	Write Protect Controls write accesses to the address range in the corresponding CSAR. 0 Write accesses are allowed. 1 Write accesses are not allowed. Attempting to write to the range of addresses for which the WP bit is set results in a bus error termination of the internal cycle and no external cycle.
7–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 V	Valid Specifies whether the corresponding CSAR, CSMR, and CSCR contents are valid. Programmed chip-selects do not assert until the V bit is 1b (except for FB_CS0, which acts as the global chip-select).

Table continues on the next page...

FB_CSMR*n* field descriptions (continued)

Field	Description
	NOTE: At reset, FB_CS0 will fire for any access to the FlexBus memory region. CSMR0[V] must be set as part of the chip select initialization sequence to allow other chip selects to function as programmed. 0 Chip-select is invalid. 1 Chip-select is valid.

38.4.3 Chip Select Control Register (FB_CSCR*n*)

Controls the auto-acknowledge, address setup and hold times, port size, burst capability, and number of wait states for the associated chip select.

NOTE

To support the global chip-select (FB_CS0), the CSCR0 reset values differ from the other CSCRs. The reset value of CSCR0 is as follows:

- Bits 31–24 are 0b
- Bit 23–3 are chip-dependent
- Bits 3–0 are 0b

See the chip configuration details for your particular chip for information on the exact CSCR0 reset value.

Address: 4000_C000h base + 8h offset + (12d × i), where i=0d to 5d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	SWS						0		SWSEN	EXTS	ASET		RDAH		WRAH	
W																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	WS						BLS	AA	PS		BEM	BSTR	BSTW	0		
W																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

FB_CSCR*n* field descriptions

Field	Description
31–26 SWS	Secondary Wait States Used only when the SWSEN bit is 1b. Specifies the number of wait states inserted before an internal transfer acknowledge is generated for a burst transfer (except for the first termination, which is controlled by WS).
25–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23 SWSEN	Secondary Wait State Enable 0 Disabled. A number of wait states (specified by WS) are inserted before an internal transfer acknowledge is generated for all transfers. 1 Enabled. A number of wait states (specified by SWS) are inserted before an internal transfer acknowledge is generated for burst transfer secondary terminations.
22 EXTS	Extended Transfer Start/Extended Address Latch Enable Controls how long $\overline{\text{FB_TS}}$ /FB_ALE is asserted. 0 Disabled. $\overline{\text{FB_TS}}$ /FB_ALE asserts for one bus clock cycle. 1 Enabled. $\overline{\text{FB_TS}}$ /FB_ALE remains asserted until the first positive clock edge after $\overline{\text{FB_CSn}}$ asserts.
21–20 ASET	Address Setup Controls when the chip-select is asserted with respect to assertion of a valid address and attributes. 00 Assert $\overline{\text{FB_CSn}}$ on the first rising clock edge after the address is asserted (default for all but $\overline{\text{FB_CS0}}$). 01 Assert $\overline{\text{FB_CSn}}$ on the second rising clock edge after the address is asserted. 10 Assert $\overline{\text{FB_CSn}}$ on the third rising clock edge after the address is asserted. 11 Assert $\overline{\text{FB_CSn}}$ on the fourth rising clock edge after the address is asserted (default for $\overline{\text{FB_CS0}}$).
19–18 RDAH	Read Address Hold or Deselect Controls the address and attribute hold time after the termination during a read cycle that hits in the associated chip-select's address space. **NOTE:** • The hold time applies only at the end of a transfer. Therefore, during a burst transfer or a transfer to a port size smaller than the transfer size, the hold time is only added after the last bus cycle. • The number of cycles the address and attributes are held after $\overline{\text{FB_CSn}}$ deassertion depends on the value of the AA bit. 00 When AA is 1b, 1 cycle. When AA is 0b, 0 cycles. 01 When AA is 1b, 2 cycles. When AA is 0b, 1 cycle. 10 When AA is 1b, 3 cycles. When AA is 0b, 2 cycles. 11 When AA is 1b, 4 cycles. When AA is 0b, 3 cycles.
17–16 WRAH	Write Address Hold or Deselect Controls the address, data, and attribute hold time after the termination of a write cycle that hits in the associated chip-select's address space. **NOTE:** The hold time applies only at the end of a transfer. Therefore, during a burst transfer or a transfer to a port size smaller than the transfer size, the hold time is only added after the last bus cycle. 00 1 cycle (default for all but $\overline{\text{FB_CS0}}$) 01 2 cycles

Table continues on the next page...

FB_CSCR*n* field descriptions (continued)

Field	Description
	10 3 cycles 11 4 cycles (default for FB_CS0)
15–10 WS	Wait States Specifies the number of wait states inserted after FlexBus asserts the associated chip-select and before an internal transfer acknowledge is generated (WS = 00h inserts 0 wait states, ..., WS = 3Fh inserts 63 wait states).
9 BLS	Byte-Lane Shift Specifies if data on FB_AD appears left-aligned or right-aligned during the data phase of a FlexBus access. 0 Not shifted. Data is left-aligned on FB_AD. 1 Shifted. Data is right-aligned on FB_AD.
8 AA	Auto-Acknowledge Enable Asserts the internal transfer acknowledge for accesses specified by the chip-select address. **NOTE:** If AA is 1b for a corresponding FB_CSn and the external system asserts an external FB_TA before the wait-state countdown asserts the internal FB_TA, the cycle is terminated. Burst cycles increment the address bus between each internal termination. **NOTE:** This field must be 1b if CSPMCR disables FB_TA. 0 Disabled. No internal transfer acknowledge is asserted and the cycle is terminated externally. 1 Enabled. Internal transfer acknowledge is asserted as specified by WS.
7–6 PS	Port Size Specifies the data port width of the associated chip-select, and determines where data is driven during write cycles and where data is sampled during read cycles. 00 32-bit port size. Valid data is sampled and driven on FB_D[31:0]. 01 8-bit port size. Valid data is sampled and driven on FB_D[31:24] when BLS is 0b, or FB_D[7:0] when BLS is 1b. 1X 16-bit port size. Valid data is sampled and driven on FB_D[31:16] when BLS is 0b, or FB_D[15:0] when BLS is 1b.
5 BEM	Byte-Enable Mode Specifies whether the corresponding FB_BE is asserted for read accesses. Certain memories have byte enables that must be asserted during reads and writes. Write 1b to the BEM bit in the relevant CSCR to provide the appropriate mode of byte enable support for these SRAMs. 0 FB_BE is asserted for data write only. 1 FB_BE is asserted for data read and write accesses.
4 BSTR	Burst-Read Enable Specifies whether burst reads are enabled for memory associated with each chip select. 0 Disabled. Data exceeding the specified port size is broken into individual, port-sized, non-burst reads. For example, a 32-bit read from an 8-bit port is broken into four 8-bit reads. 1 Enabled. Enables data burst reads larger than the specified port size, including 32-bit reads from 8- and 16-bit ports, 16-bit reads from 8-bit ports, and line reads from 8-, 16-, and 32-bit ports.

Table continues on the next page...

FB_CSCR*n* field descriptions (continued)

Field	Description
3 BSTW	Burst-Write Enable Specifies whether burst writes are enabled for memory associated with each chip select. 0 Disabled. Data exceeding the specified port size is broken into individual, port-sized, non-burst writes. For example, a 32-bit write to an 8-bit port takes four byte writes. 1 Enabled. Enables burst write of data larger than the specified port size, including 32-bit writes to 8- and 16-bit ports, 16-bit writes to 8-bit ports, and line writes to 8-, 16-, and 32-bit ports.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

38.4.4 Chip Select port Multiplexing Control Register (FB_CSPMCR)

Controls the multiplexing of the FlexBus signals.

NOTE

A bus error occurs when you do any of the following:

- Write to a reserved address
- Write to a reserved field in this register, or
- Access this register using a size other than 32 bits.

Address: 4000_C000h base + 60h offset = 4000_C060h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	GROUP1				GROUP2				GROUP3				GROUP4				GROUP5				0											
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FB_CSPMCR field descriptions

Field	Description
31–28 GROUP1	FlexBus Signal Group 1 Multiplex control Controls the multiplexing of the FB_ALE, FB_CS1 , and FB_TS signals. 0000 FB_ALE 0001 FB_CS1 0010 FB_TS Any other value Reserved
27–24 GROUP2	FlexBus Signal Group 2 Multiplex control Controls the multiplexing of the FB_CS4, FB_TSIZ0, and FB_BE_31_24 signals. 0000 FB_CS4 0001 FB_TSIZ0 0010 FB_BE_31_24 Any other value Reserved

Table continues on the next page...

FB_CSPMCR field descriptions (continued)

Field	Description
23–20 GROUP3	FlexBus Signal Group 3 Multiplex control Controls the multiplexing of the FB_CS5 , FB_TSIZ1, and FB_BE_23_16 signals. 0000 FB_CS5 0001 FB_TSIZ1 0010 FB_BE_23_16 Any other value Reserved
19–16 GROUP4	FlexBus Signal Group 4 Multiplex control Controls the multiplexing of the FB_TBST , FB_CS2 , and FB_BE_15_8 signals. 0000 FB_TBST 0001 FB_CS2 0010 FB_BE_15_8 Any other value Reserved
15–12 GROUP5	FlexBus Signal Group 5 Multiplex control Controls the multiplexing of the FB_TA , FB_CS3 , and FB_BE_7_0 signals. **NOTE:** When GROUP5 is not 0000b, you must write 1b to the CSCR[AA] bit. Otherwise, the bus hangs during a transfer. 0000 FB_TA 0001 FB_CS3 . You must also write 1b to CSCR[AA]. 0010 FB_BE_7_0 . You must also write 1b to CSCR[AA]. Any other value Reserved
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

38.5 Functional description

38.5.1 Use cases

In general, FlexBus supports the following use cases, but note that your device may not support all of these use cases, because of limitations imposed by your specific package's pinouts:

- Multiplexed 32-bit address and 32-bit data
- Multiplexed 32-bit address and 16-bit data (non-multiplexed 16-bit address and 16-bit data)

- Multiplexed 32-bit address and 8-bit data (non-multiplexed 24-bit address and 8-bit data)
- Non-multiplexed 32-bit address and 32-bit data busses

NOTE

All use cases require signals to actually be available on the pins of your specific device package. Refer to your specific device's signal multiplexing table to verify the availability of specific signals for your device package.

38.5.2 Address comparison

When a bus cycle is routed to FlexBus, FlexBus compares the transfer address to the base address (see CSAR[BA]) and base address mask (see CSMR[BAM]). This table describes how FlexBus decides to assert a chip-select and complete the bus cycle based on the address comparison.

When the transfer address	Then FlexBus
Matches one address register configuration	Asserts the appropriate chip-select, generating a FlexBus bus cycle as defined in the appropriate CSCR. If CSMR[WP] is set and a write access is performed, FlexBus terminates the internal bus cycle with a bus error, does not assert a chip-select, and does not perform an external bus cycle.
Does not match an address register configuration	Terminates the transfer with a bus error response, does not assert a chip-select, and does not perform a FlexBus cycle.
Matches more than one address register configuration	Terminates the transfer with a bus error response, does not assert a chip-select, and does not perform a FlexBus cycle.

38.5.3 Address driven on address bus

FlexBus always drives a 32-bit address on the FB_AD bus regardless of the external memory's or peripheral's address size.

38.5.4 Connecting address/data lines

The external device must connect its address and data lines as follows:

- Address lines
  - FB_AD from FB_AD0 upward
- Data lines

- If CSCR[BLS] = 0, FB_AD from FB_AD31 downward
- If CSCR[BLS] = 1, FB_AD from FB_AD0 upward

38.5.5 Bit ordering

No bit ordering is required when connecting address and data lines to the FB_AD bus. For example, a full 16-bit address/16-bit data device connects its addr15–addr0 to FB_AD16–FB_AD1 and data15–data0 to FB_AD31–FB_AD16. See Data-byte alignment and physical connections for a graphical connection.

38.5.6 Data transfer signals

Data transfers between FlexBus and the external memory or peripheral involve these signals:

- Address/data bus (FB_AD31–FB_AD0)
- Control signals ($\overline{\text{FB_TS}}$/FB_ALE, $\overline{\text{FB_TA}}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, FB_R/$\overline{\text{W}}$, $\overline{\text{FB_BE}n}$)
- Attribute signals ($\overline{\text{FB_TBST}}$, FB_TSIZ1–FB_TSIZ0)

38.5.7 Signal transitions

These signals change on the rising edge of the FlexBus clock (FB_CLK):

- Address
- Write data
- $\overline{\text{FB_TS}}$/FB_ALE
- $\overline{\text{FB_CS}}$n
- All attribute signals

FlexBus latches the read data on the rising edge of the clock.

38.5.8 Data-byte alignment and physical connections

The device aligns data transfers in FlexBus byte lanes with the number of lanes depending on the data port width.

The following figure shows the byte lanes that external memory or peripheral connects to and the sequential transfers of a 32-bit transfer for the supported port sizes when byte lane shift is disabled. For example, an 8-bit memory connects to the single lane

FB_AD31–FB_AD24 ($\overline{\text{FB_BE_31_24}}$). A 32-bit transfer through this 8-bit port takes four transfers, starting with the LSB to the MSB. A 32-bit transfer through a 32-bit port requires one transfer on each four-byte lane.

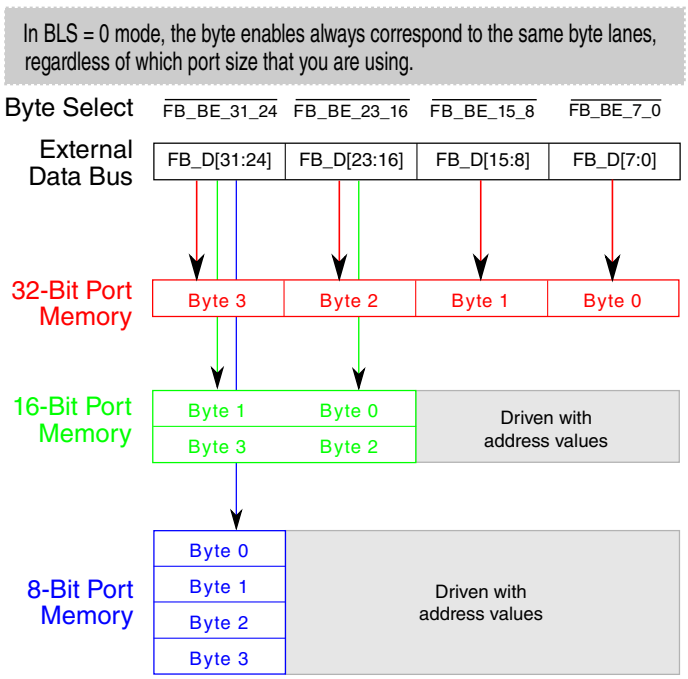


Figure 38-2. Connections for external memory port sizes (CSCRn[BLS] = 0)

The following figure shows the byte lanes that external memory or peripheral connects to and the sequential transfers of a 32-bit transfer for the supported port sizes when byte lane shift is enabled.

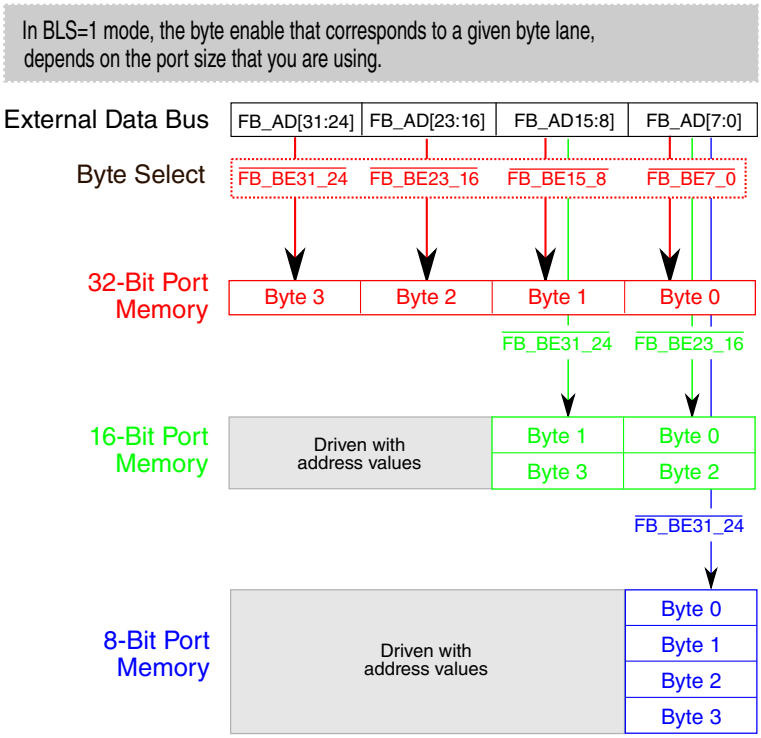


Figure 38-3. Connections for external memory port sizes (CSCRn[BLS] = 1)

38.5.9 Address/data bus multiplexing

FlexBus supports a single 32-bit wide multiplexed address and data bus (FB_AD31–FB_AD0). FlexBus always drives the full 32-bit address on the first clock of a bus cycle. During the data phase, the FB_AD31– FB_AD0 lines used for data are determined by the programmed port size and BLS setting for the corresponding chip-select. FlexBus continues to drive the address on any FB_AD31– FB_AD0 lines not used for data.

38.5.9.1 FlexBus multiplexed operating modes for CSCRn[BLS]=0

This table shows the supported combinations of address and data bus widths when CSCRn[BLS] is 0b.

Port size and phase		FB_AD			
		31–24	23–16	15–8	7–0
32-bit	Address phase	Address			
	Data phase	Data			
16-bit	Address phase	Address			
	Data phase	Data		Address	

Table continues on the next page...

Port size and phase		FB_AD			
		31–24	23–16	15–8	7–0
8-bit	Address phase	Address			
	Data phase	Data	Address		

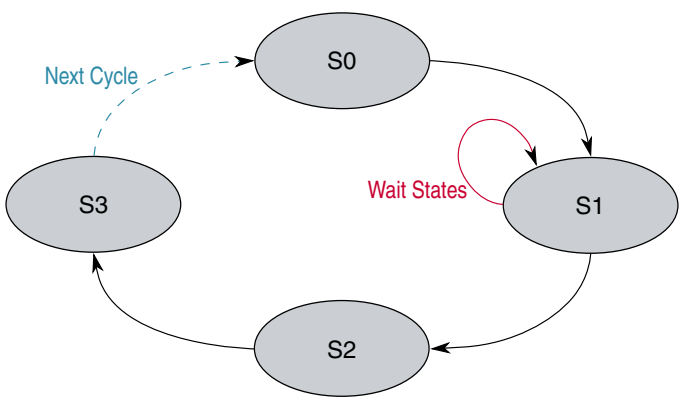
38.5.9.2 FlexBus multiplexed operating modes for CSCRn[BLS]=1

This table shows the supported combinations of address and data bus widths when CSCRn[BLS] is 1b.

Port size and phase		FB_AD			
		31–24	23–16	15–8	7–0
32-bit	Address phase	Address			
	Data phase	Data			
16-bit	Address phase	Address			
	Data phase	Address		Data	
8-bit	Address phase	Address			
	Data phase	Address			Data

38.5.10 Data transfer states

Basic data transfers occur in four clocks or states. (See Figure 38-5 and Figure 38-7 for examples of basic data transfers.) The FlexBus state machine controls the data-transfer operation. This figure shows the state-transition diagram for basic read and write cycles.



The states are described in this table.

State	Cycle	Description
S0	All	The read or write cycle is initiated. On the rising clock edge, FlexBus: • Places a valid address on FB_ADn • Asserts FB_TS/FB_ALE • Drives FB_R/W high for a read and low for a write
S1	All	FlexBus: • Negates FB_TS/FB_ALE on the rising edge of FB_CLK • Asserts FB_CSn • Drives the data on FB_AD31– FB_AD*X* for writes • Tristates FB_AD31– FB_AD*X* for reads • Continues to drive the address on FB_AD pins that are unused for data If the external memory or perihperal asserts FB_TA, then the process moves to S2. If FB_TA is not asserted internally or externally, then S1 repeats.
	Read	The external memory or peripheral drives the data before the next rising edge of FB_CLK (the rising edge that begins S2) with FB_TA asserted.
S2	All	For internal termination, FlexBus negates FB_CSn and the transfer is complete. For external termination, the external memory or peripheral negates FB_TA, and FlexBus negates FB_CSn after the rising edge of FB_CLK at the end of S2.
	Read	FlexBus latches the data on the rising clock edge entering S2. The external memory or peripheral can stop driving the data after this edge or continue to drive the data until the end of S3 or through any additional address hold cycles.
S3	All	FlexBus invalidates the address, data, and FB_R/W on the rising edge of FB_CLK at the beginning of S3, terminating the transfer.

38.5.11 FlexBus Timing Examples

Note

The timing diagrams throughout this section use signal names that may not be included on your particular device. Ignore these extraneous signals.

Note

Throughout this section:

- FB_D[*X*] indicates a 32-, 16-, or 8-bit wide data bus
- FB_A[*Y*] indicates an address bus that can be 32, 24, or 16 bits wide.

38.5.11.1 Basic Read Bus Cycle

During a read cycle, the MCU receives data from memory or a peripheral device. The following figure shows a read cycle flowchart.

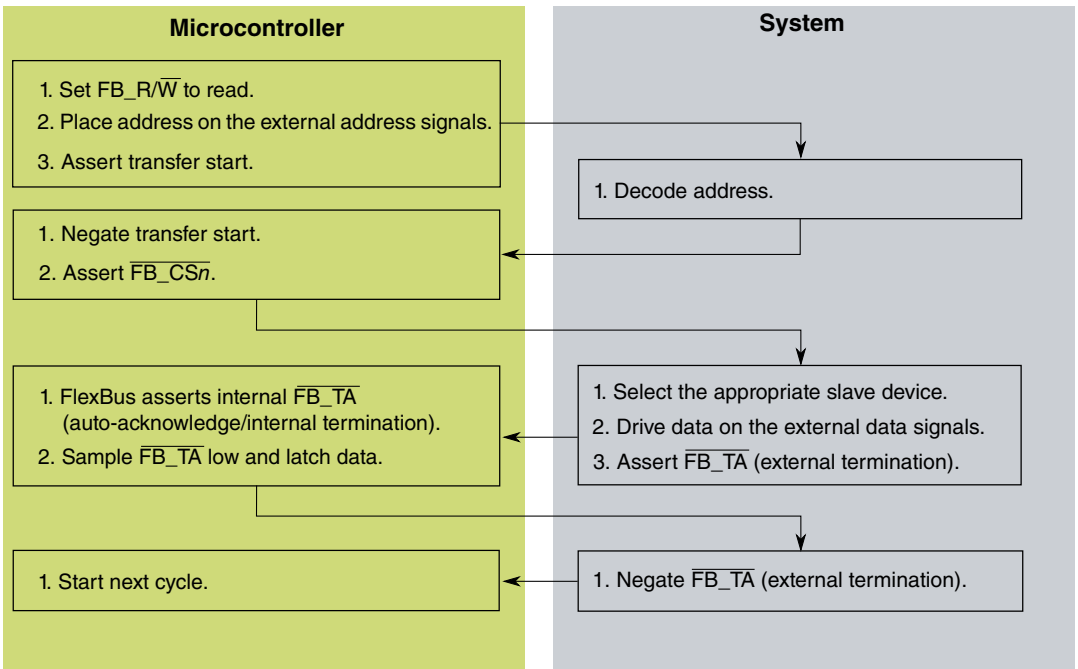


Figure 38-4. Read Cycle Flowchart

The read cycle timing diagram is shown in the following figure.

Note

FB_TA does not have to be driven by the external device for internally-terminated bus cycles.

Note

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and another module. At the end of the read bus cycles the address signals are indeterminate.

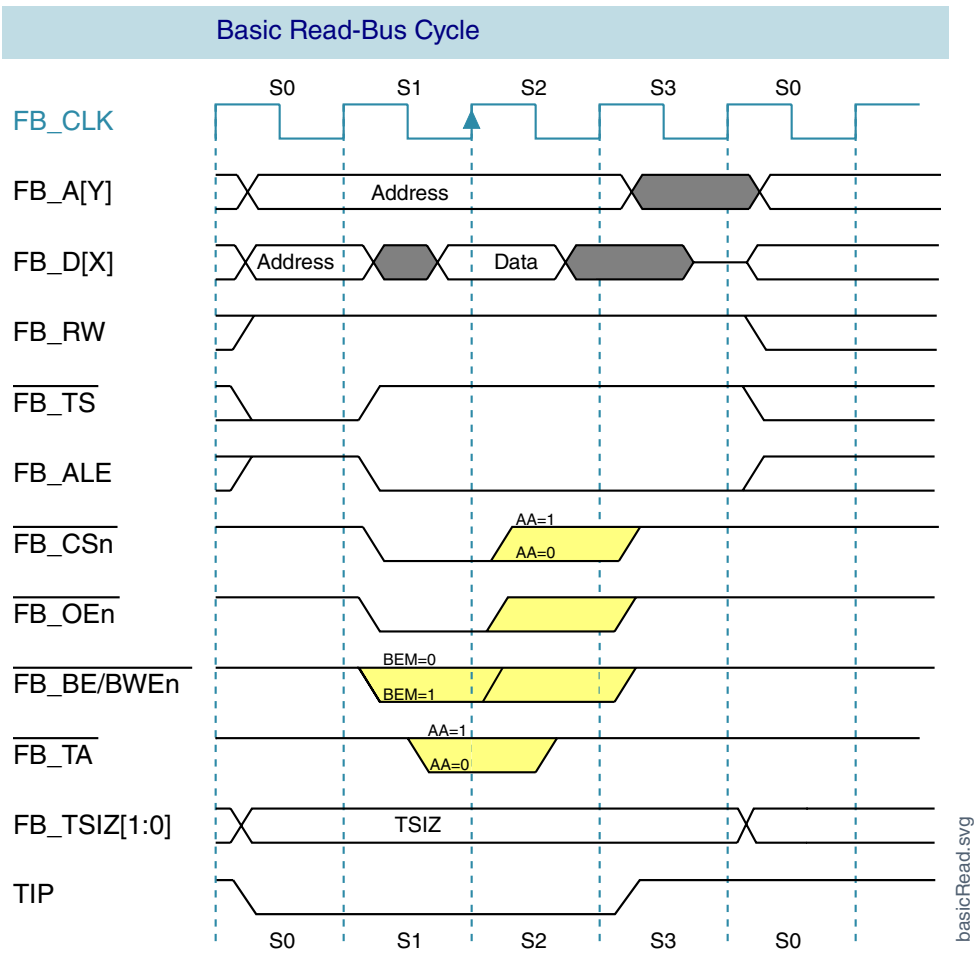


Figure 38-5. Basic Read-Bus Cycle

38.5.11.2 Basic Write Bus Cycle

During a write cycle, the device sends data to memory or to a peripheral device. The following figure shows the write cycle flowchart.

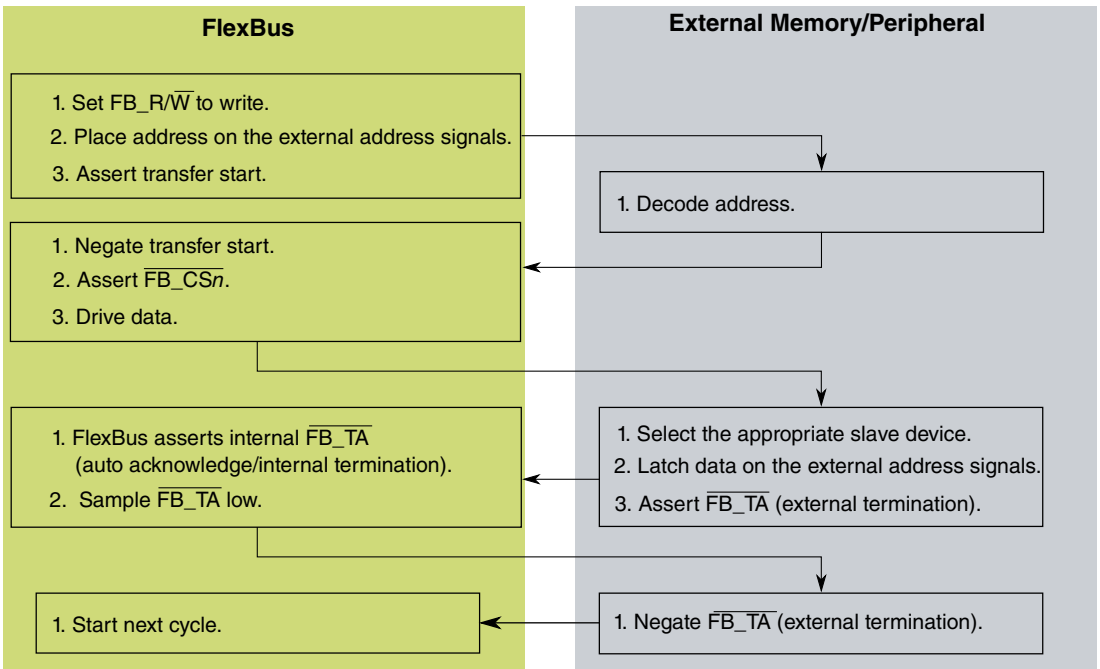


Figure 38-6. Write-Cycle Flowchart

The following figure shows the write cycle timing diagram.

Note

The address and data busses are muxed between the FlexBus and another module. At the end of the write bus cycles, the address signals are indeterminate.

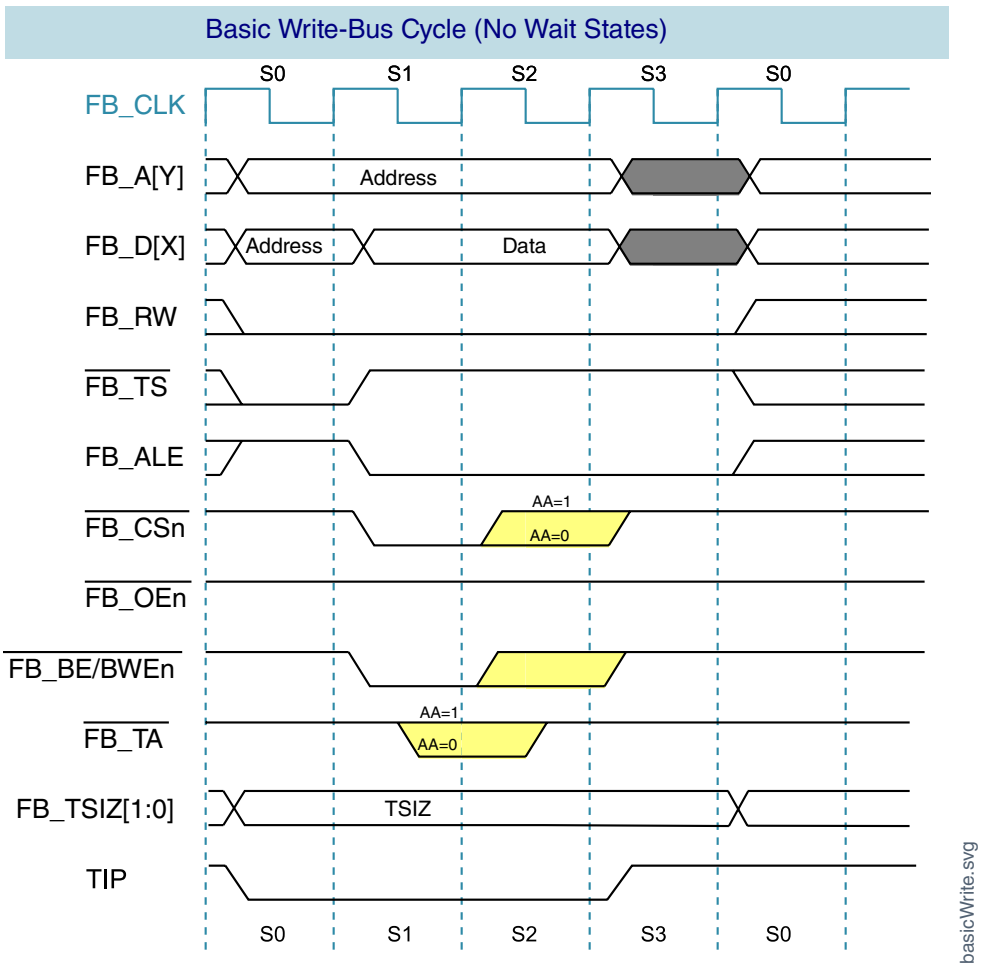


Figure 38-7. Basic Write-Bus Cycle

38.5.11.3 Bus Cycle Sizing

This section shows timing diagrams for various port size scenarios.

38.5.11.3.1 Bus Cycle Sizing—Byte Transfer, 8-bit Device, No Wait States

The following figure illustrates the basic byte read transfer to an 8-bit device with no wait states:

- The address is driven on the full FB_AD[31:0] bus in the first clock.

- The device tristates FB_AD[31:24] on the second clock and continues to drive address on FB_AD[23:0] throughout the bus cycle.
- The external device returns the read data on FB_AD[31:24] and may tristate the data line or continue driving the data one clock after $\overline{\text{FB_TA}}$ is sampled asserted.

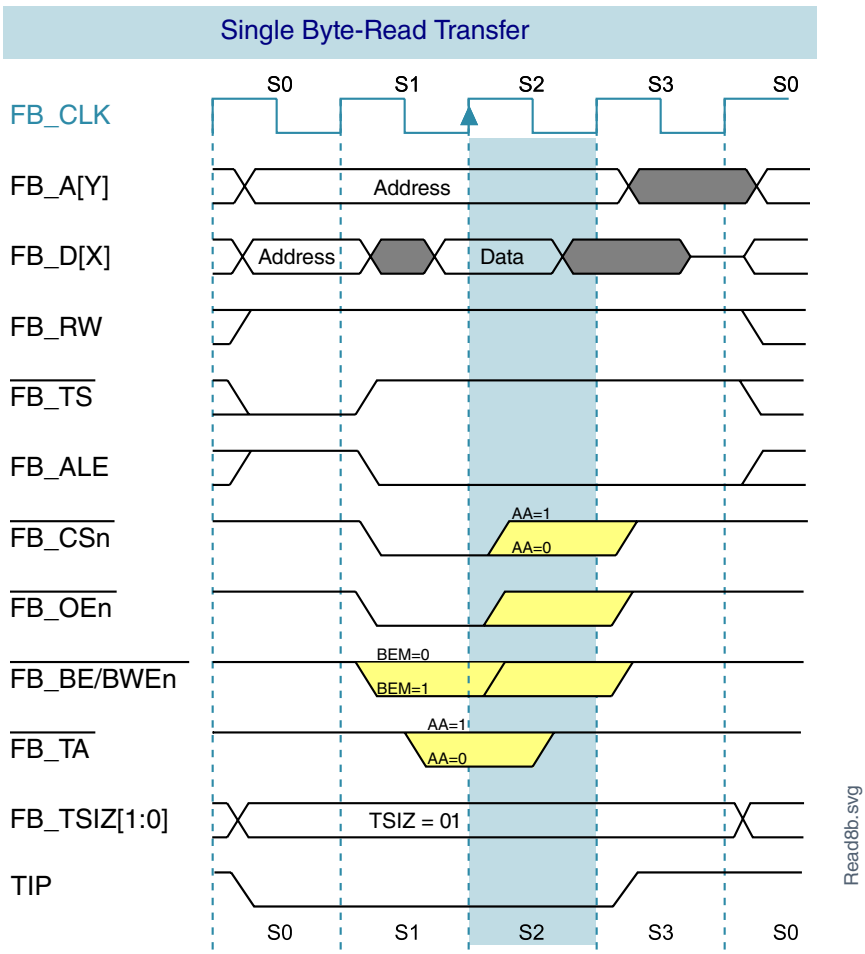


Figure 38-8. Single Byte-Read Transfer

The following figure shows the similar configuration for a write transfer. The data is driven from the second clock on FB_AD[31:24].

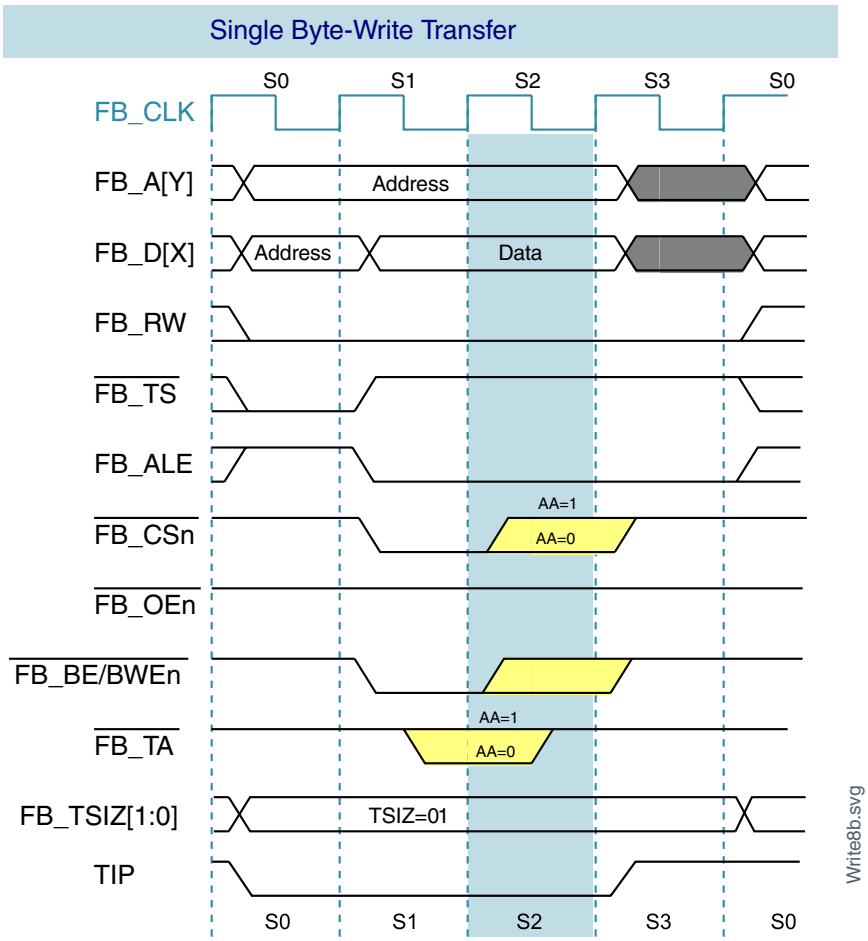


Figure 38-9. Single Byte-Write Transfer

38.5.11.3.2 Bus Cycle Sizing—Word Transfer, 16-bit Device, No Wait States

The following figure illustrates the basic word read transfer to a 16-bit device with no wait states.

- The address is driven on the full FB_AD[31:8] bus in the first clock.
- The device tristates FB_AD[31:16] on the second clock and continues to drive address on FB_AD[15:0] throughout the bus cycle.
- The external device returns the read data on FB_AD[31:16] and may tristate the data line or continue driving the data one clock after $\overline{\text{FB_TA}}$ is sampled asserted.

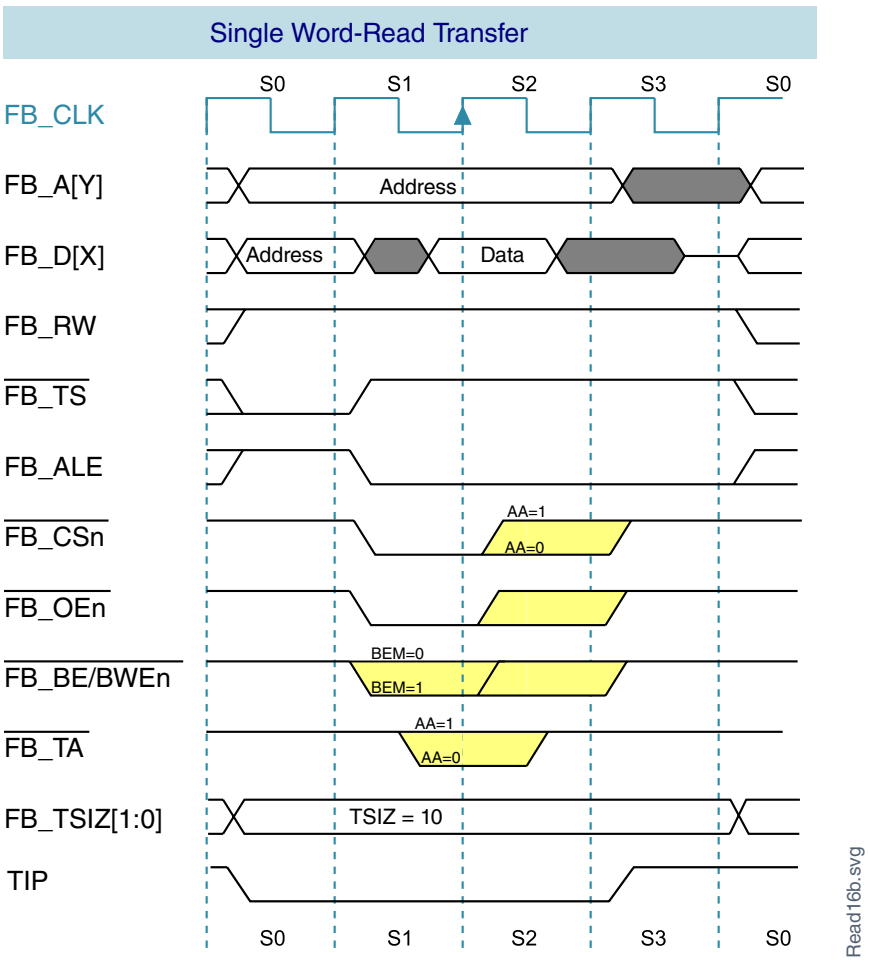


Figure 38-10. Single Word-Read Transfer

The following figure shows the similar configuration for a write transfer. The data is driven from the second clock on FB_AD[31:16].

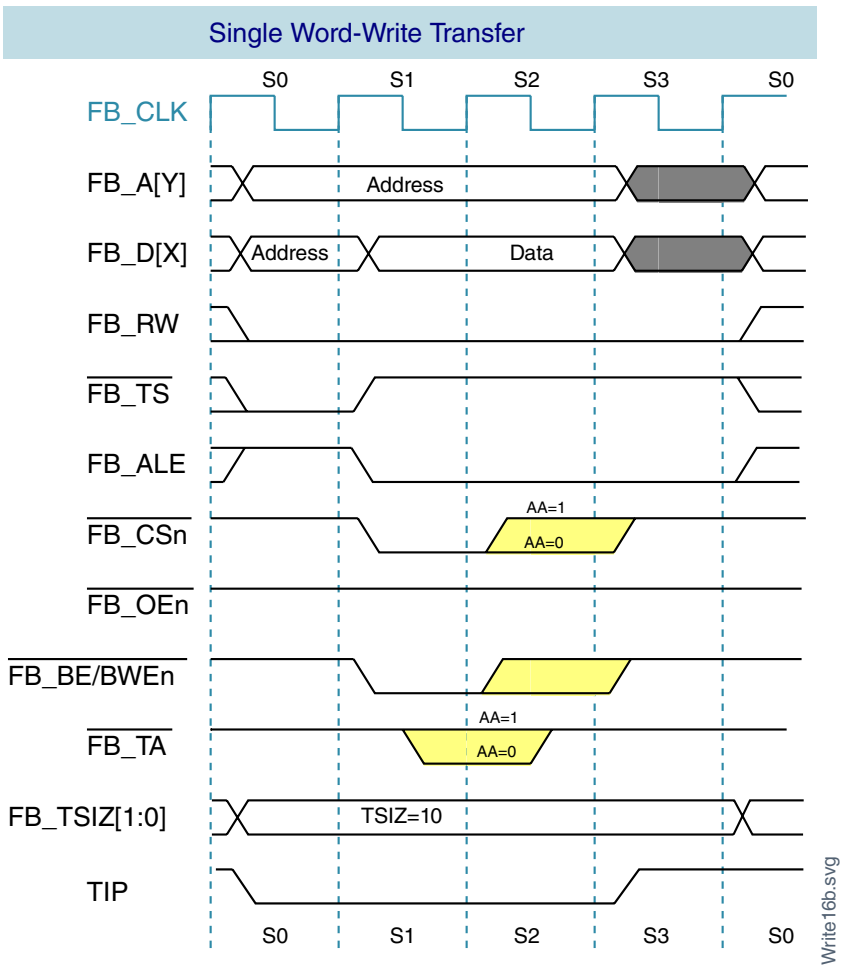


Figure 38-11. Single Word-Write Transfer

38.5.11.3.3 Bus Cycle Sizing—Longword Transfer, 32-bit Device, No Wait States

The following figure depicts a longword read from a 32-bit device.

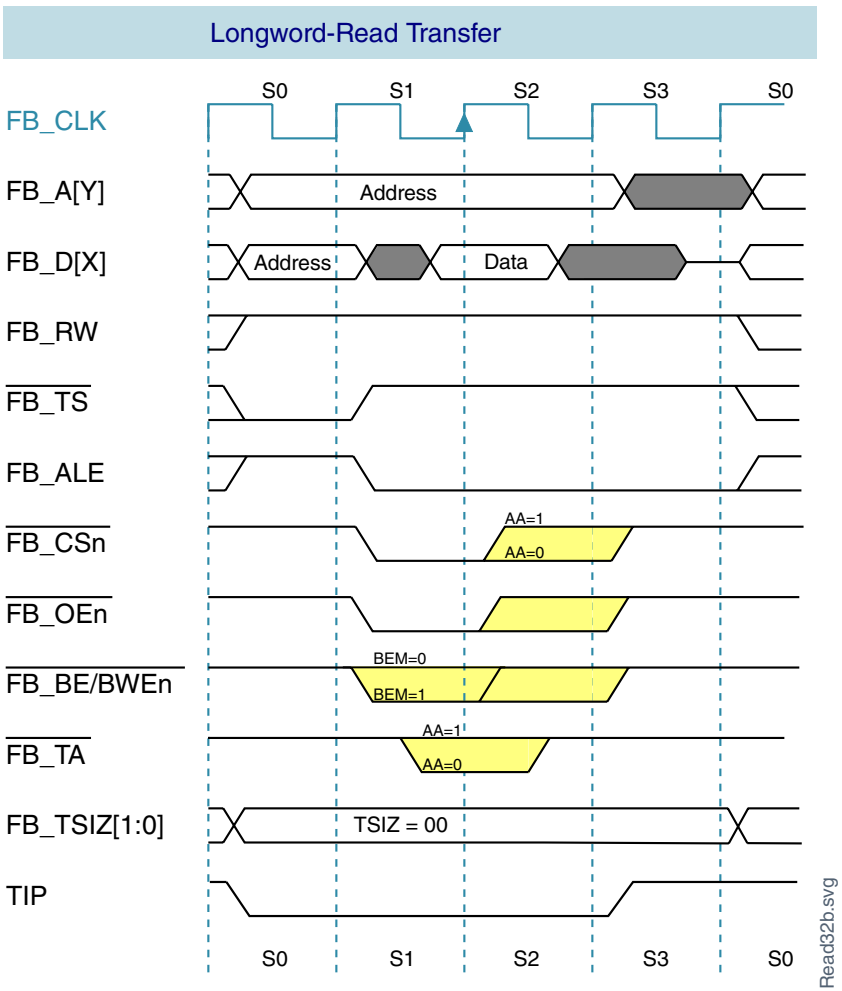


Figure 38-12. Longword-Read Transfer

The following figure illustrates the longword write to a 32-bit device.

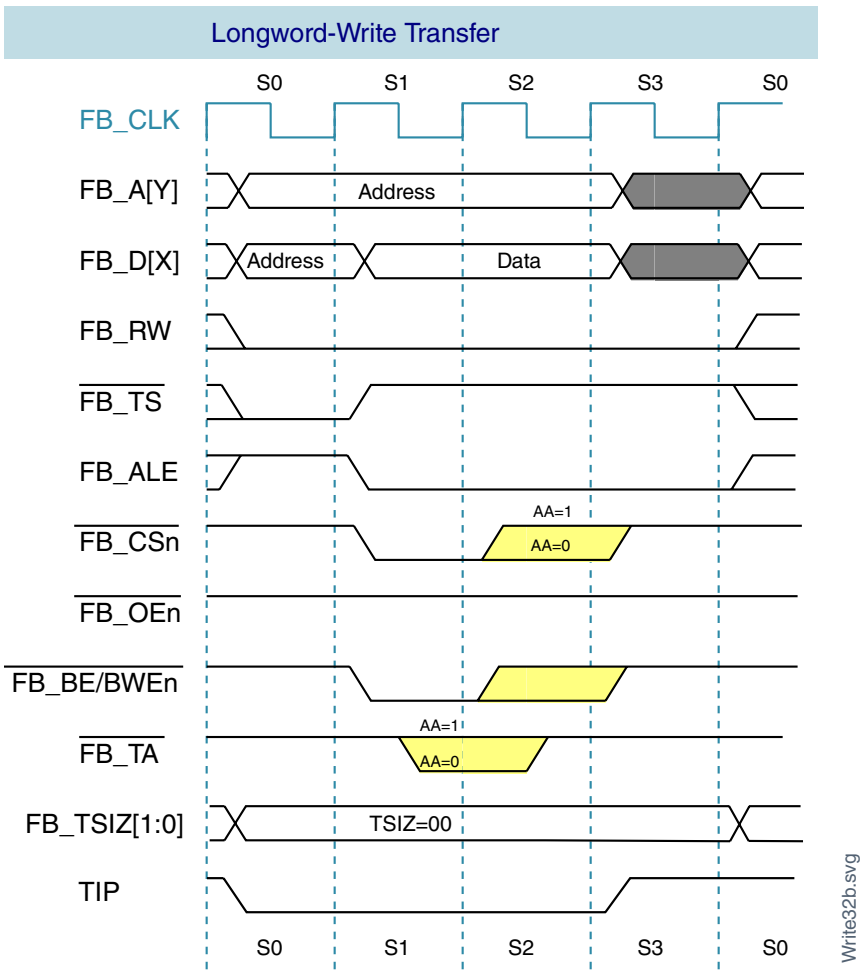


Figure 38-13. Longword-Write Transfer

38.5.11.4 Timing Variations

The FlexBus module has several features that can change the timing characteristics of a basic read- or write-bus cycle to provide additional address setup, address hold, and time for a device to provide or latch data.

38.5.11.4.1 Wait States

Wait states can be inserted before each beat of a transfer by programming the CSCR*n* registers. Wait states can give the peripheral or memory more time to return read data or sample write data.

The following figures show the basic read and write bus cycles (also shown in Figure 38-5 and Figure 38-10) with the default of no wait states respectively.

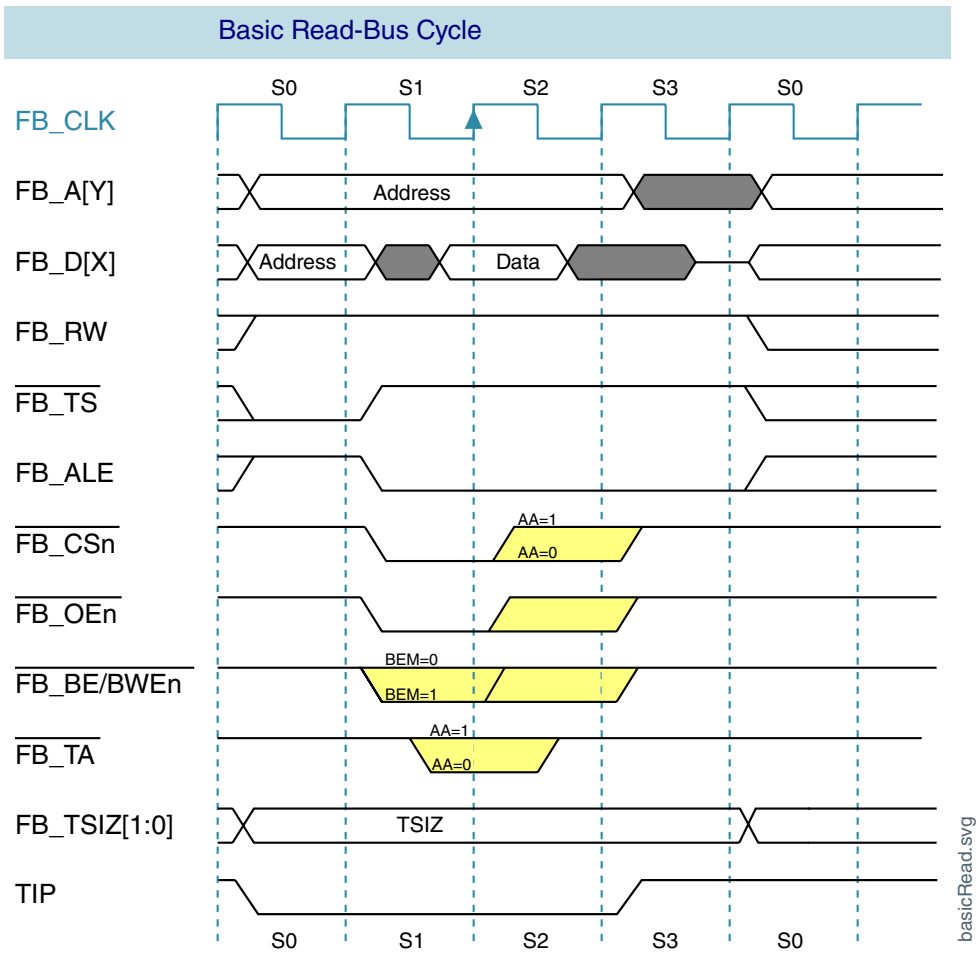


Figure 38-14. Basic Read-Bus Cycle (No Wait States)

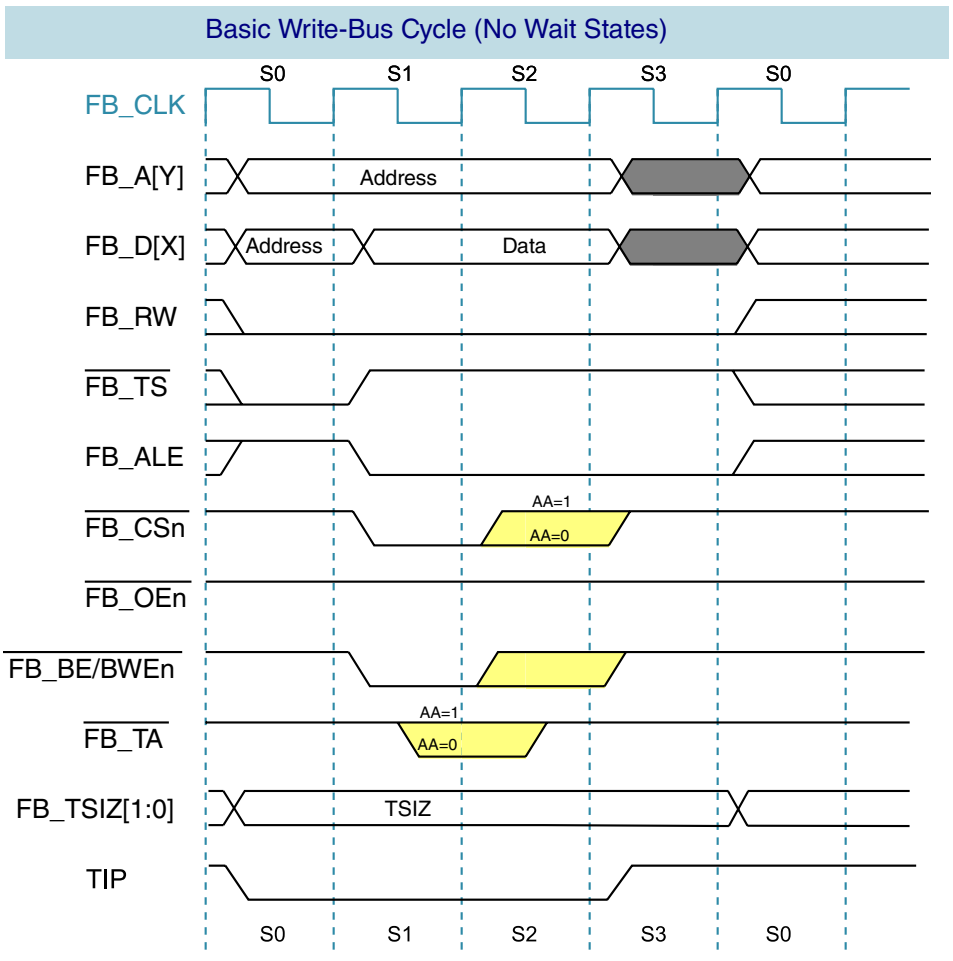


Figure 38-15. Basic Write-Bus Cycle (No Wait States)

If wait states are used, the S1 state repeats continuously until the chip-select auto-acknowledge unit asserts internal transfer acknowledge or the external $\overline{\text{FB_TA}}$ is recognized as asserted. The following figures show a read and write cycle with one wait state respectively.

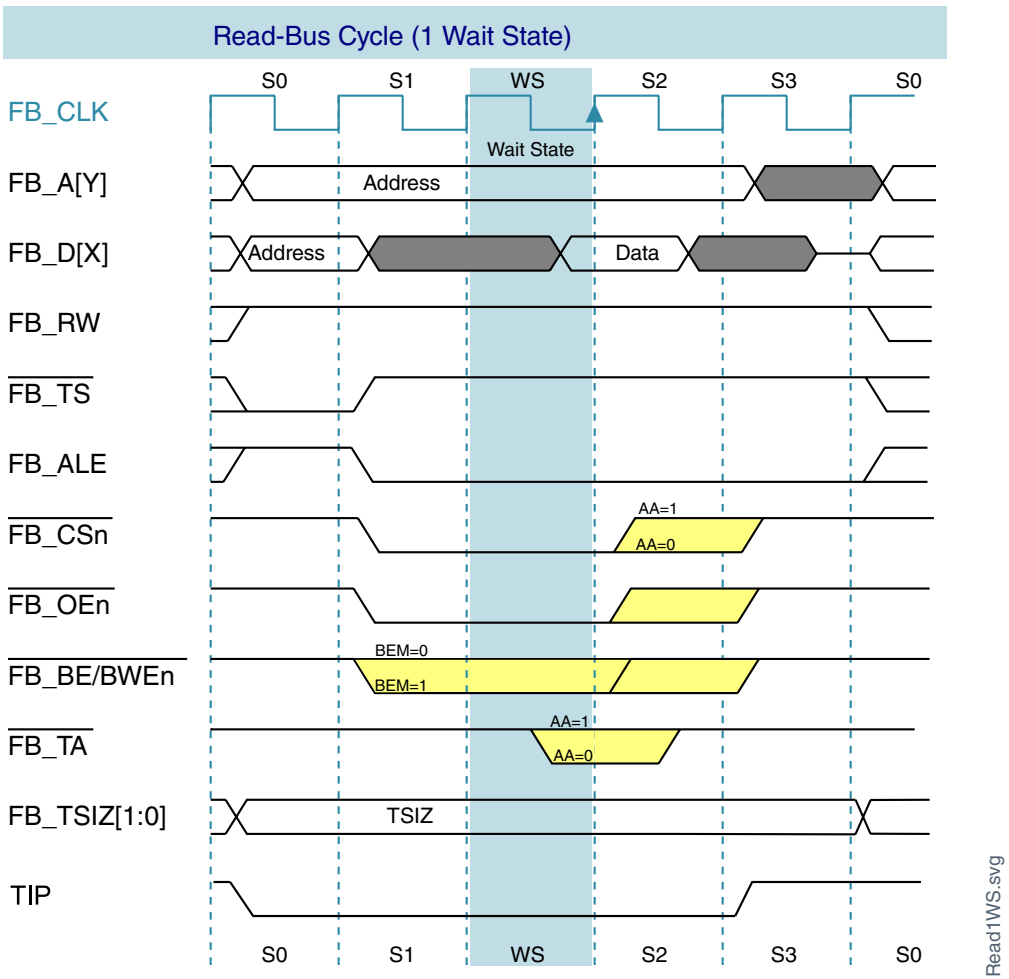


Figure 38-16. Read-Bus Cycle (One Wait State)

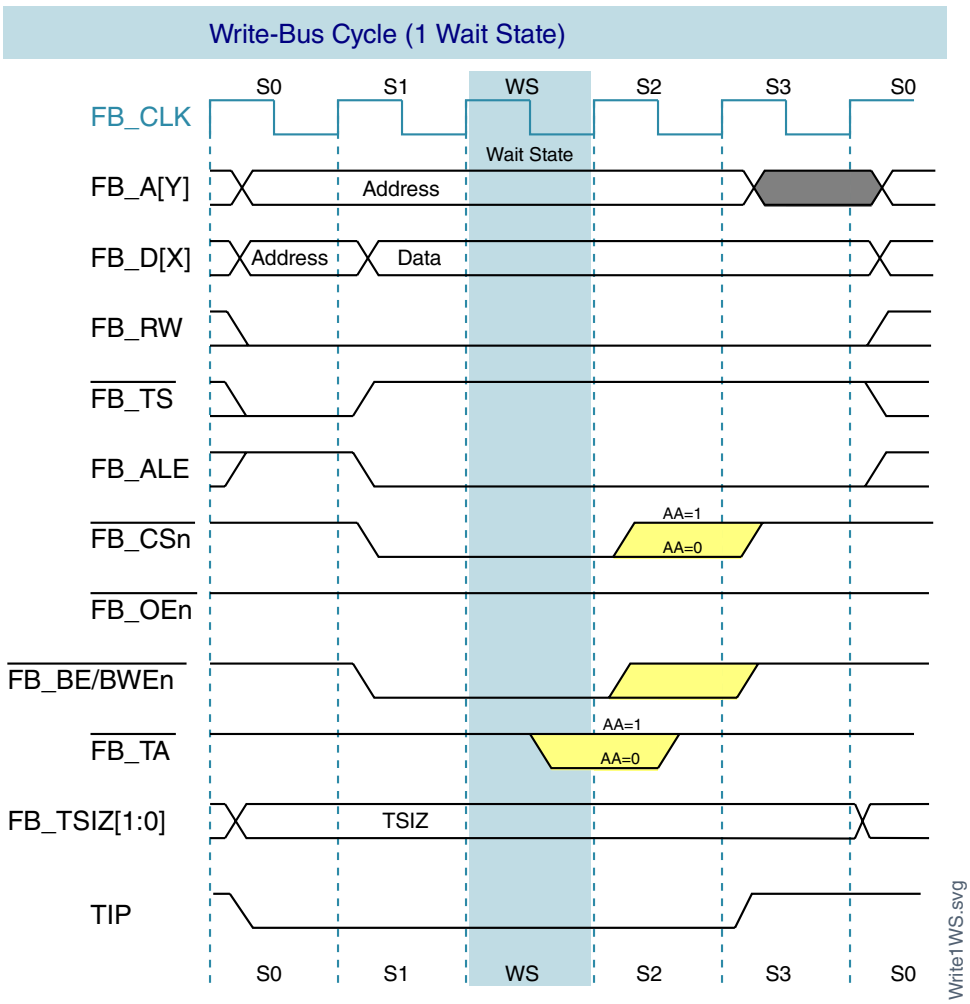


Figure 38-17. Write-Bus Cycle (One Wait State)

38.5.11.4.2 Address Setup and Hold

The timing of the assertion and negation of the chip selects, byte selects, and output enable can be programmed on a chip-select basis. Each chip-select can be programmed to assert one to four clocks after transfer start/address-latch enable ($\overline{\text{FB_TS}}$/FB_ALE) is asserted. The following figures show read- and write-bus cycles with two clocks of address setup respectively.

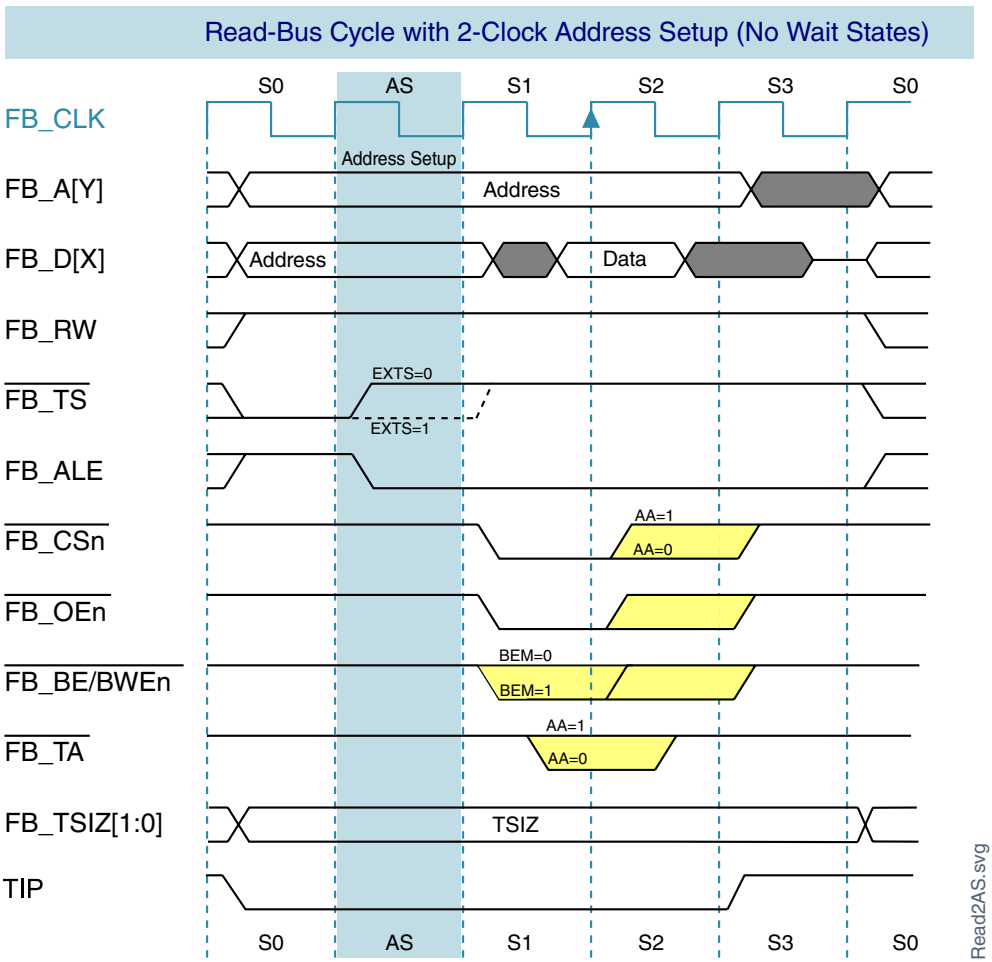


Figure 38-18. Read-Bus Cycle with Two-Clock Address Setup (No Wait States)

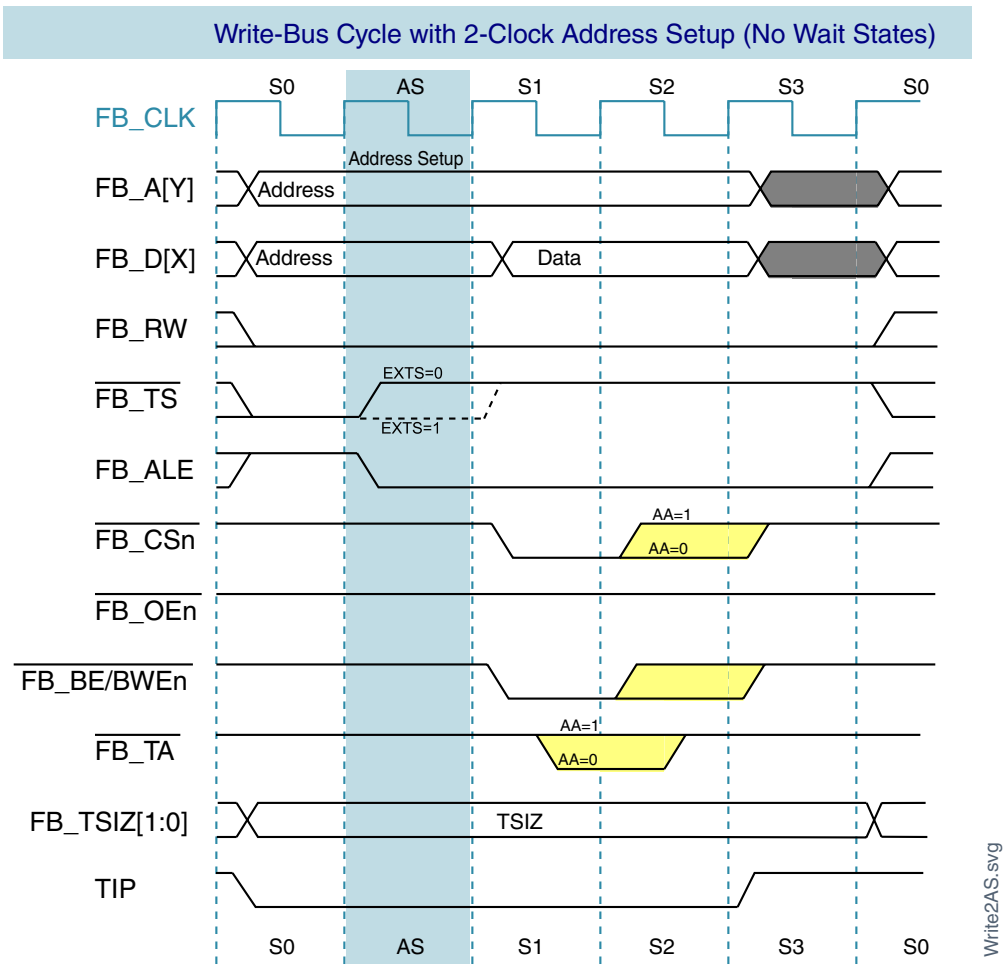


Figure 38-19. Write-Bus Cycle with Two Clock Address Setup (No Wait States)

In addition to address setup, a programmable address hold option for each chip select exists. Address and attributes can be held one to four clocks after chip-select, byte-selects, and output-enable negate. The following figures show read and write bus cycles with two clocks of address hold respectively.

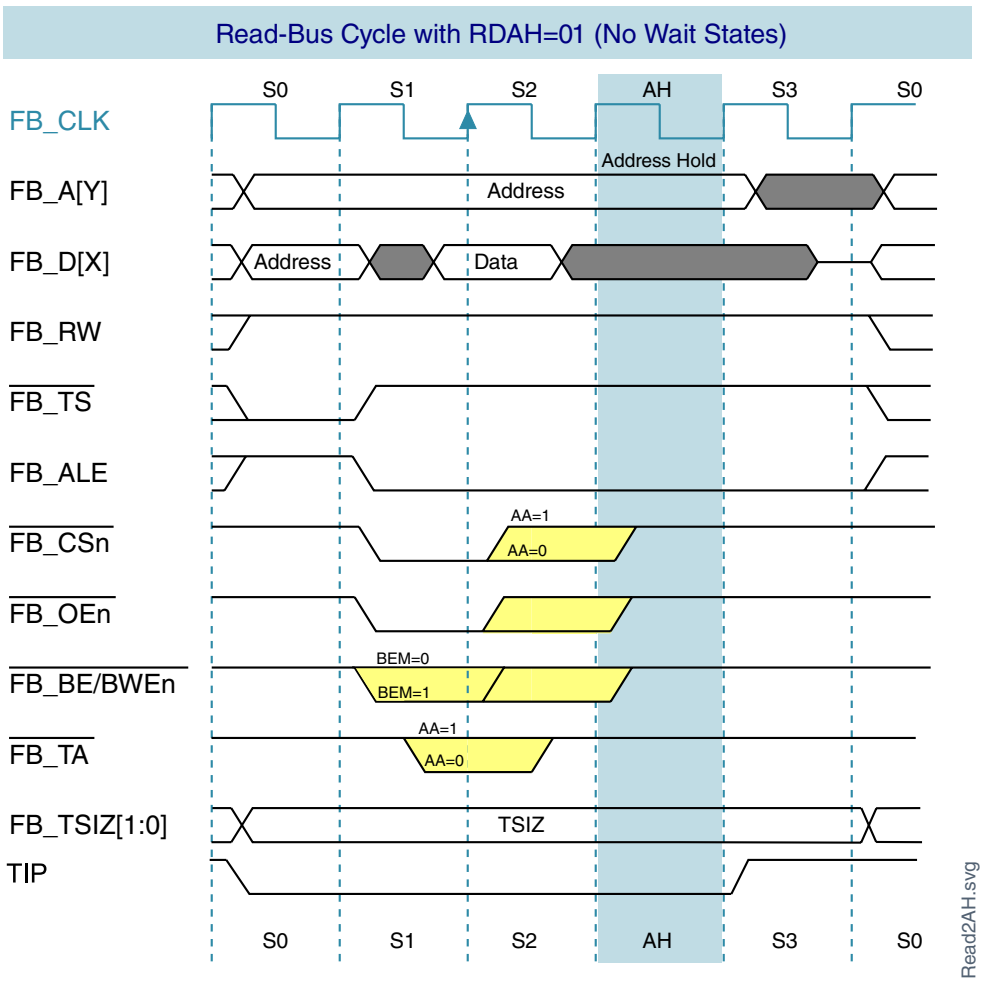


Figure 38-20. Read Cycle with Two-Clock Address Hold (No Wait States)

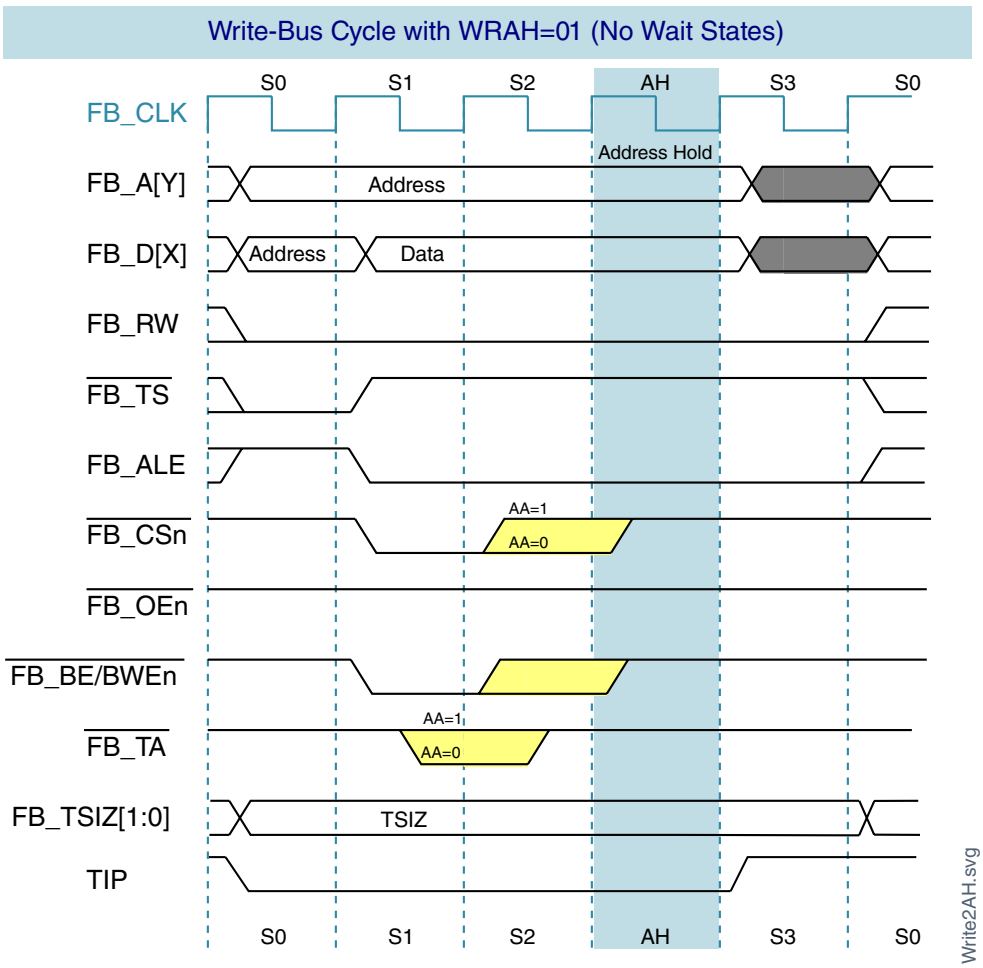


Figure 38-21. Write Cycle with Two-Clock Address Hold (No Wait States)

The following figure shows a bus cycle using address setup, wait states, and address hold.

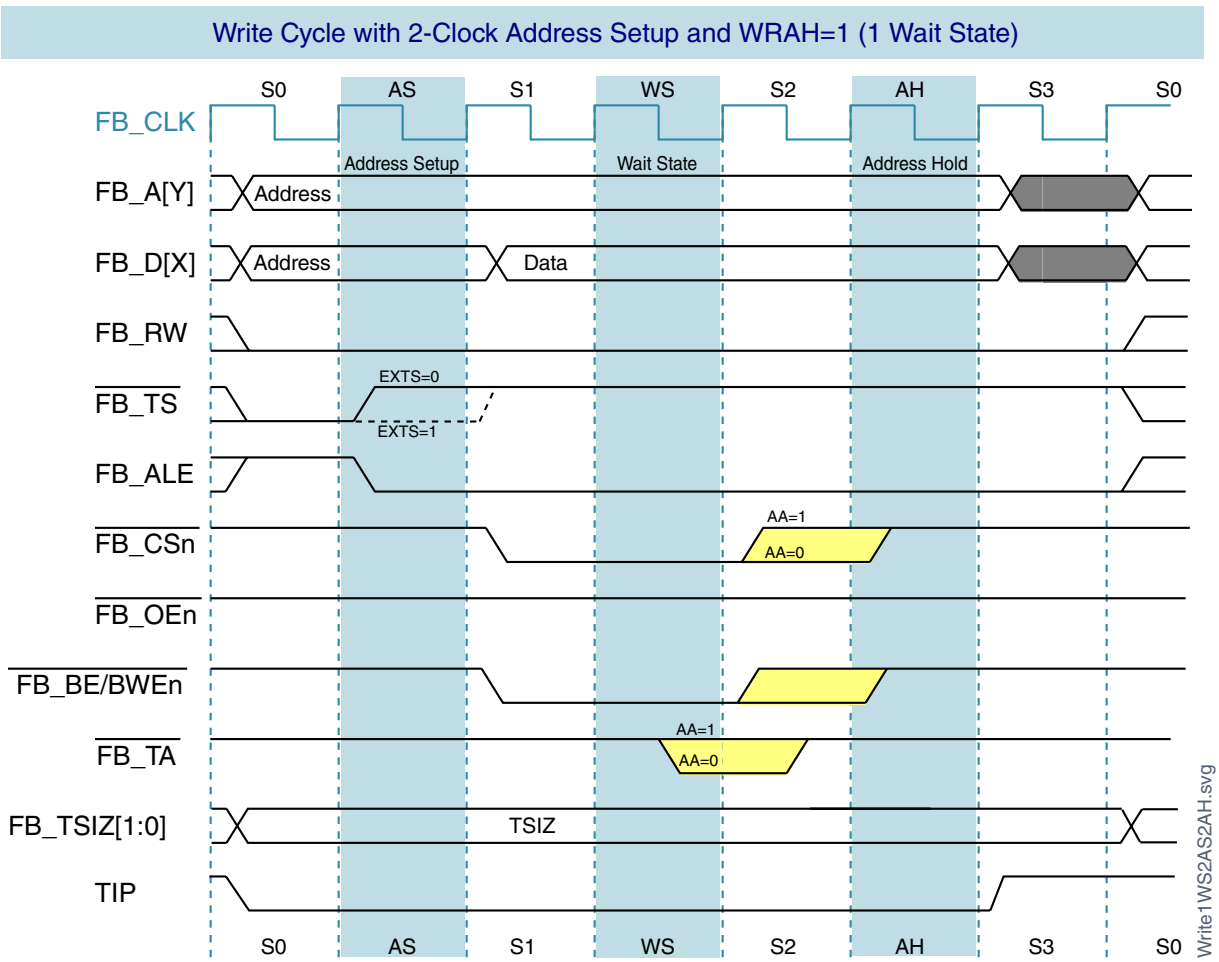


Figure 38-22. Write Cycle with Two-Clock Address Setup and Two-Clock Hold (One Wait State)

38.5.12 Burst cycles

The chip can be programmed to initiate burst cycles if its transfer size exceeds the port size of the selected destination. The initiation of a burst cycle is encoded on the transfer size pins (FB_TSIZ[1:0]). For burst transfers to smaller port sizes, FB_TSIZ[1:0] indicates the size of the entire transfer. For example, with bursting enabled, a 16-bit transfer to an 8-bit port takes two beats (two byte-sized transfers), for which FB_TSIZ[1:0] equals 10b throughout. A 32-bit transfer to an 8-bit port takes four beats (four byte-sized transfers), for which FB_TSIZ[1:0] equals 00b throughout.

38.5.12.1 Enabling and inhibiting burst

The CSCRn registers enable bursting for reads, writes, or both.

Memory spaces can be declared burst-inhibited for reads and writes by writing 0b to the appropriate CSCRn[BSTR] and CSCRn[BSTW] fields.

38.5.12.2 Transfer size and port size translation

With bursting disabled, any transfer larger than the port size breaks into multiple individual transfers (e.g. <Addr><Data><Addr+1><Data><Addr+2><Data>). With bursting enabled, any transfer larger than the port size results in a burst cycle of multiple beats (e.g. <Addr><Data><Data><Data>). The following table shows the result of such transfer translations.

Port size PS[1:0]	Transfer size FB_TSIZ[1:0]	Burst-inhibited: Number of transfers Burst enabled: Number of beats
01b (8 bit)	10b (16 bits)	2
	00b (32 bits)	4
	11b (16 bytes)	16
1Xb (16 bit)	00b (32 bits)	2
	11b (16 bytes)	8
00b (32 bit)	11b (line)	4

The FlexBus can support X-1-1-1 burst cycles to maximize system performance, where X is the primary number of wait states (max 63). Delaying termination of the cycle can add wait states. If internal termination is used, different wait state counters can be used for the first access and the following beats.

38.5.12.3 32-bit-Read burst from 8-Bit port 2-1-1-1 (no wait states)

The following figure shows a 32-bit read to an 8-bit external chip programmed for burst enable. The transfer results in a 4-beat burst and the data is driven on FB_AD[31:24]. The transfer size is driven at 32-bit (00b) throughout the bus cycle.

Note

- In **non-multiplexed address/data mode:** the address on FB_A increments only during internally-terminated burst cycles. The first address is driven throughout the entire burst for externally-terminated cycles.
- In **multiplexed address/data mode:** the address is driven on FB_AD only during the first cycle for all terminated cycles. In other words, the lower address lines only

increment during internally-terminated burst cycles (assuming that the lower address lines are being driven with the address during the data phase).

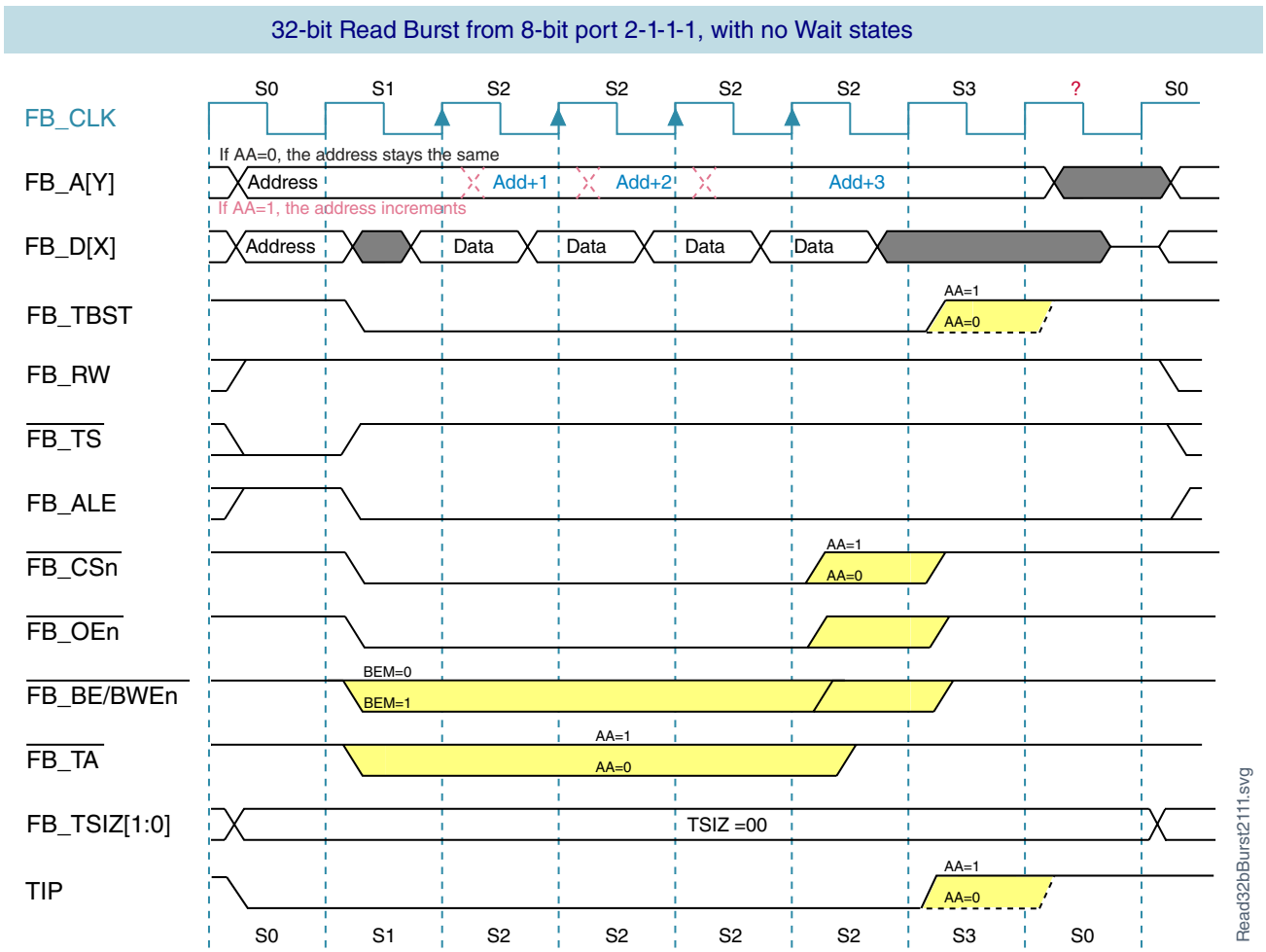


Figure 38-23. 32-bit-Read burst from 8-Bit port 2-1-1-1 (no wait states)

38.5.12.4 32-bit-Write burst to 8-Bit port 3-1-1-1 (no wait states)

The following figure shows a 32-bit write to an 8-bit external chip with burst enabled. The transfer results in a 4-beat burst and the data is driven on FB_AD[31:24]. The transfer size is driven at 32-bit (00b) throughout the bus cycle.

Note

The first beat of any write burst cycle has at least one wait state. If the bus cycle is programmed for zero wait states (CSCRn[WS] = 0b), one wait state is added. Otherwise, the programmed number of wait states are used.

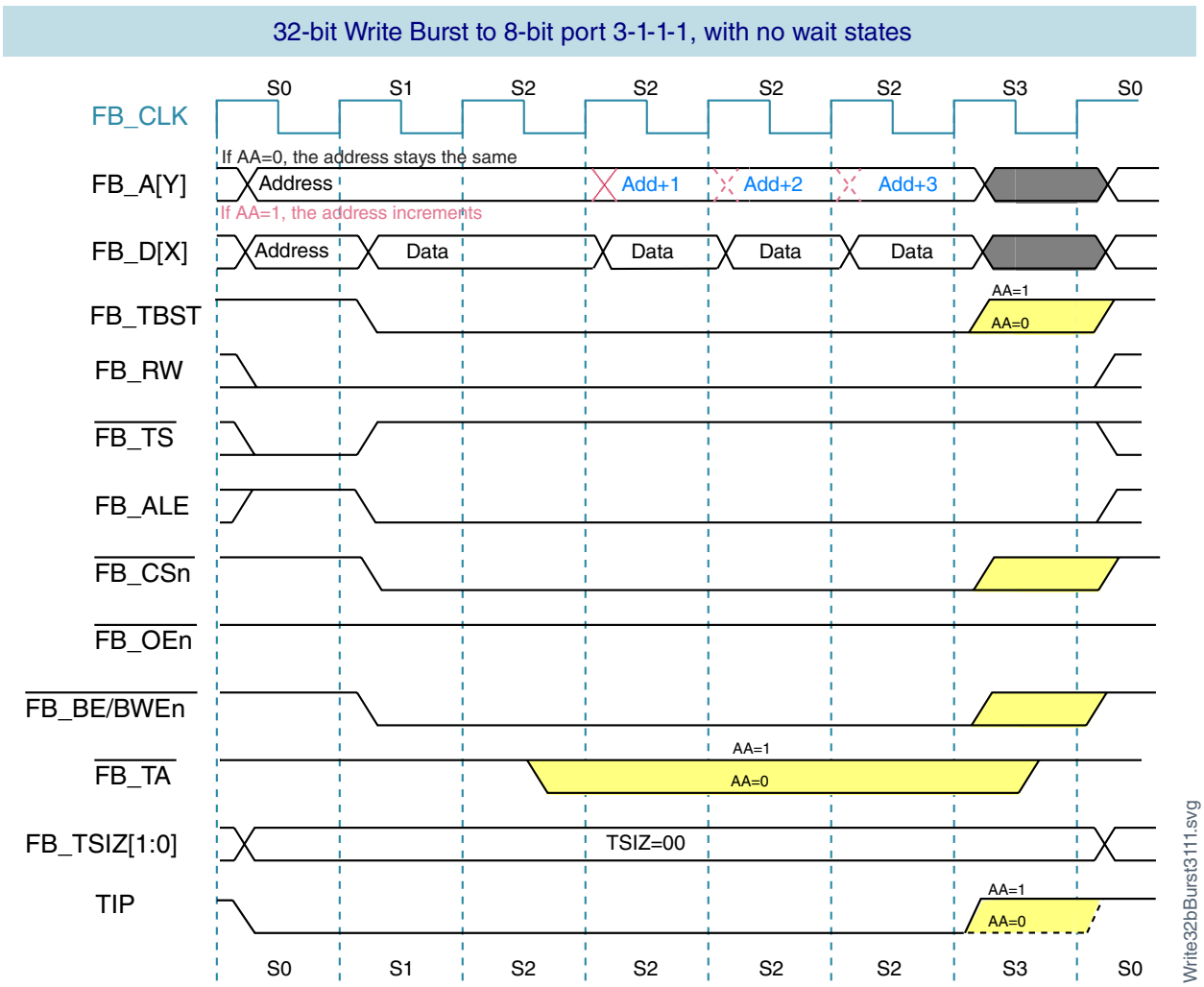


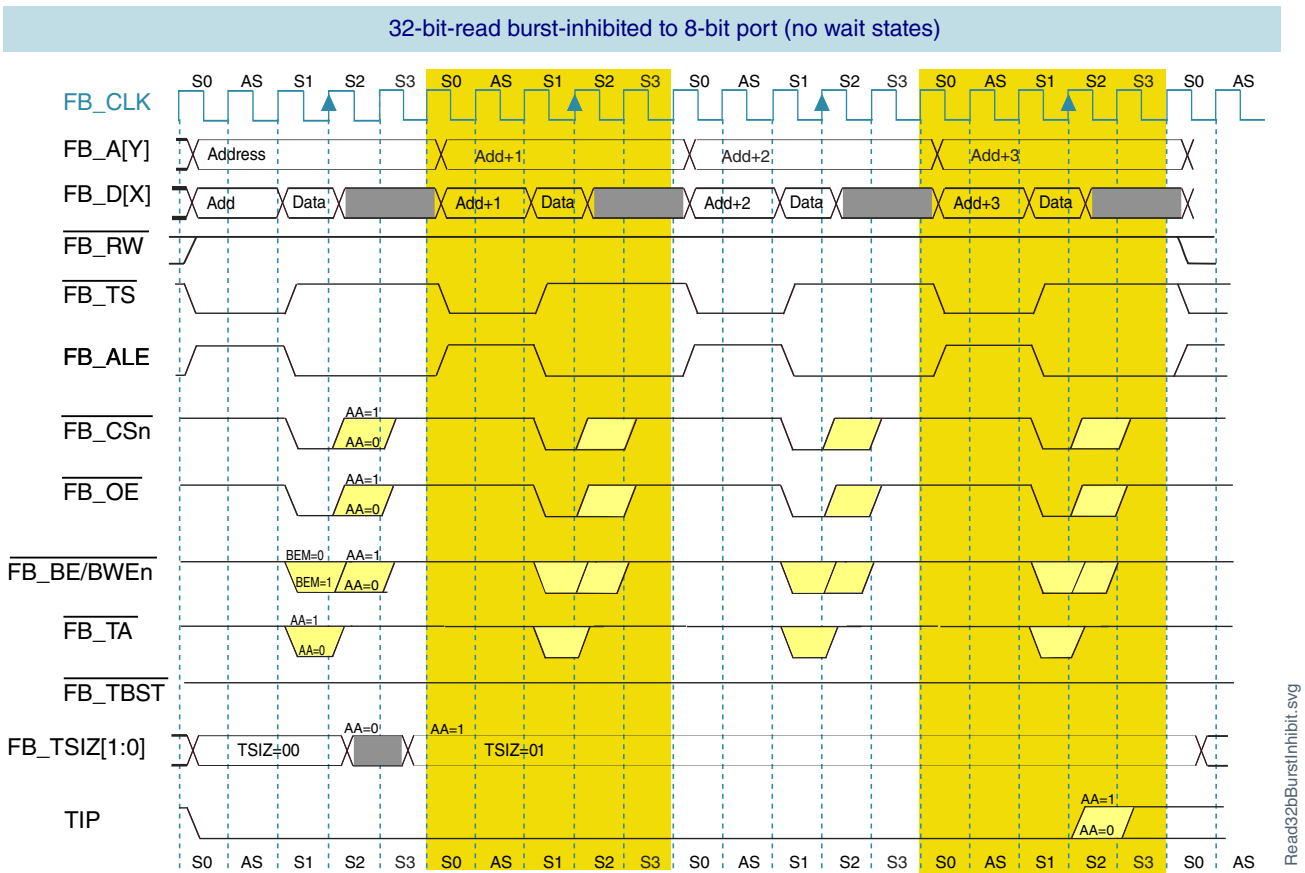
Figure 38-24. 32-bit-Write burst to 8-Bit port 3-1-1-1 (no wait states)

38.5.12.5 32-bit-read burst-inhibited from 8-bit port (no wait states)

The following figure shows a 32-bit read from an 8-bit device with burst inhibited. The transfer results in four individual transfers. The transfer size is driven at 32-bit (00b) during the first transfer and at byte (01b) during the next three transfers.

Note

There is an extra clock of address setup (AS) for each burst-inhibited transfer between states S0 and S1.



38.5.12.6 32-bit-write burst-inhibited to 8-bit port (no wait states)

The following figure shows a 32-bit write to an 8-bit device with burst inhibited. The transfer results in four individual transfers. The transfer size is driven at 32-bit (00b) during the first transfer and at byte (01b) during the next three transfers.

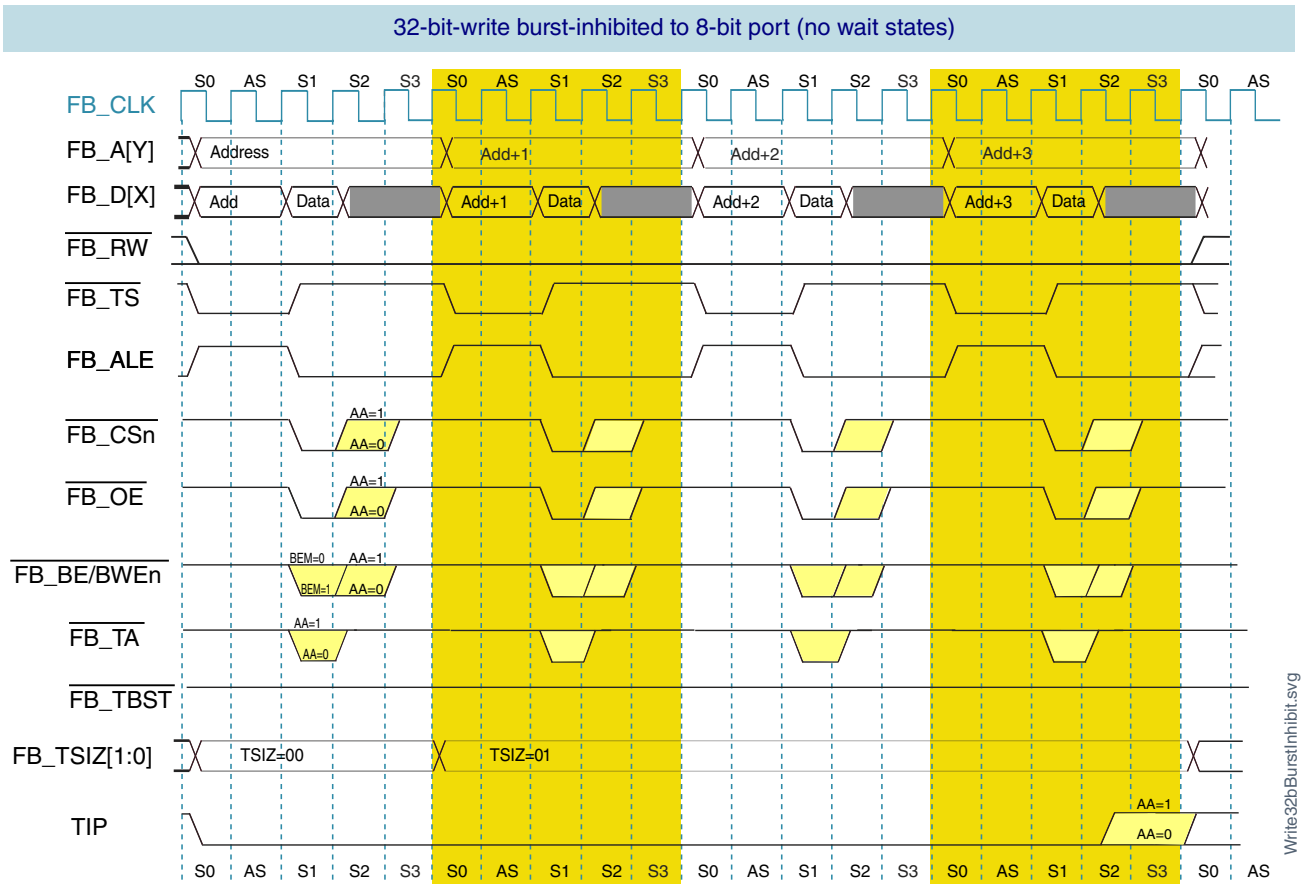


Figure 38-25. 32-bit-write burst-inhibited to 8-bit port (no wait states)

38.5.12.7 32-bit-read burst from 8-bit port 3-2-2-2 (one wait state)

The following figure illustrates another read burst transfer, but in this case a wait state is added between individual beats.

Note

CSCRn[WS] determines the number of wait states in the first beat. However, for subsequent beats, the CSCRn[WS] (or CSCRn[SWS] if CSCRn[SWSEN] = 1b) determines the number of wait states.

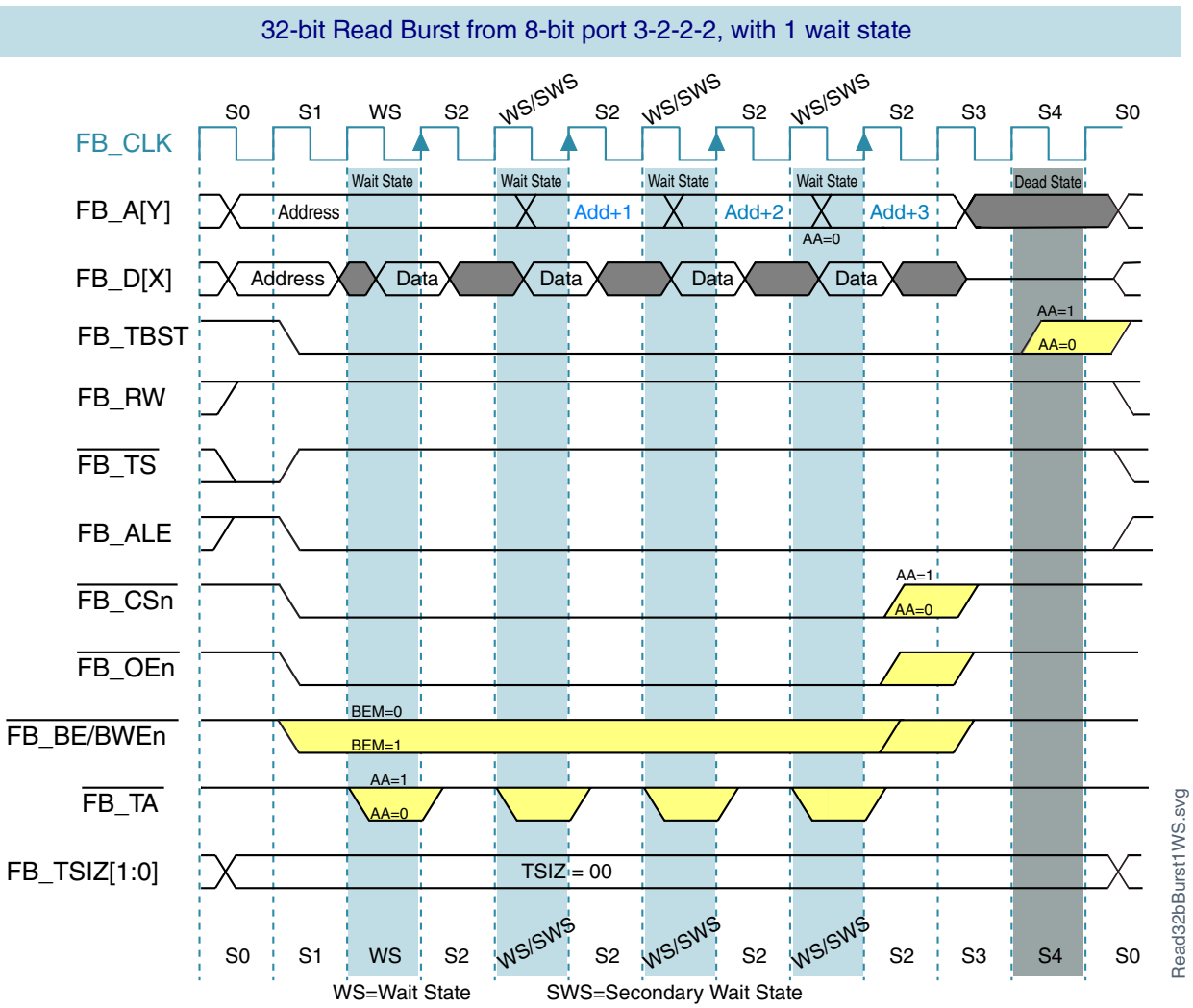


Figure 38-26. 32-bit-read burst from 8-bit port 3-2-2-2 (one wait state)

38.5.12.8 32-bit-write burst to 8-bit port 3-2-2-2 (one wait state)

The following figure illustrates a write burst transfer with one wait state.

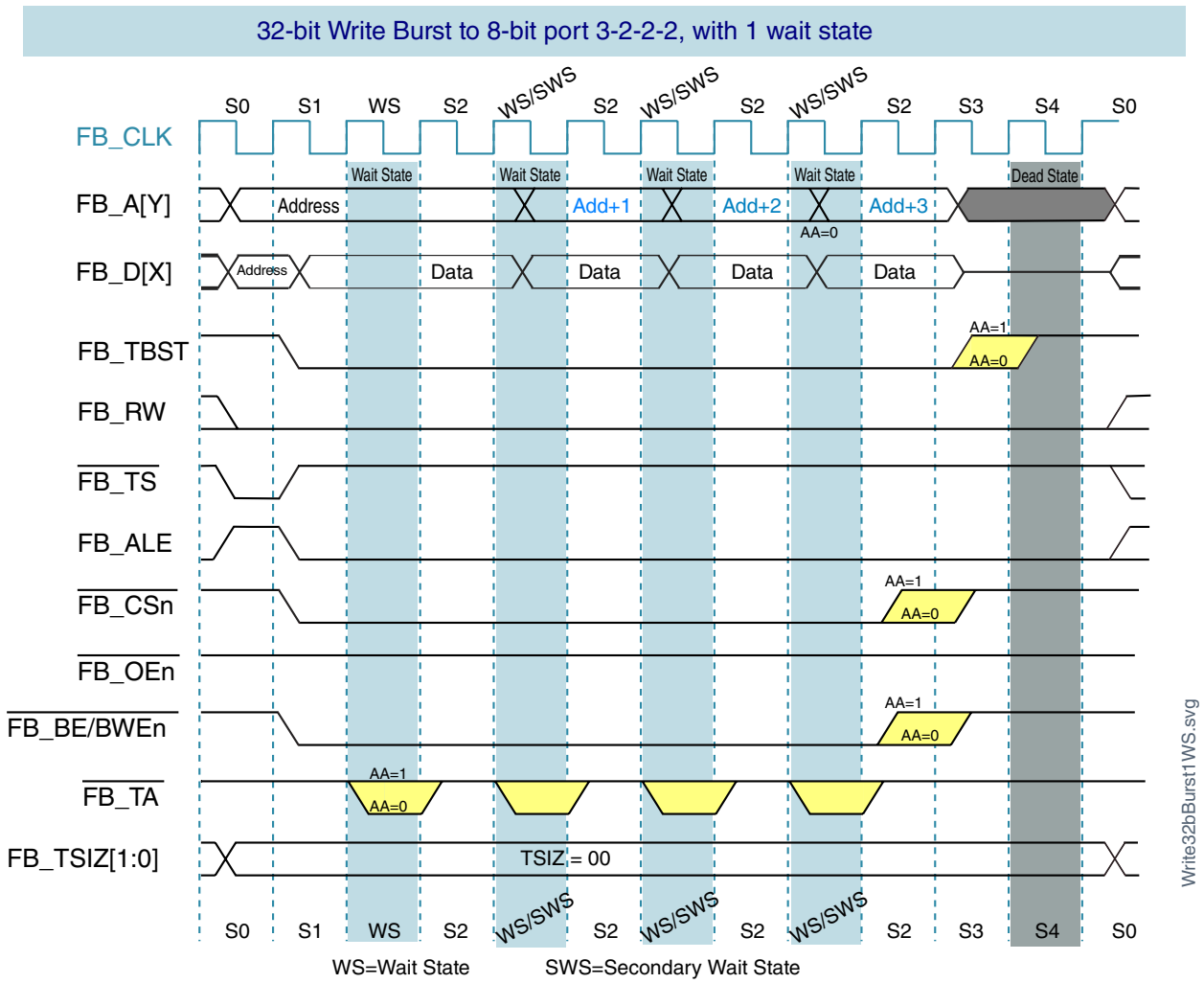


Figure 38-27. 32-bit-write burst to 8-bit port 3-2-2-2 (one wait state)

38.5.12.9 32-bit-read burst from 8-bit port 3-1-1-1 (address setup and hold)

If address setup and hold are used, only the first and last beat of the burst cycle are affected. The following figure shows a read cycle with one clock of address setup and address hold.

Note

In non-multiplexed address/data mode, the address on FB_A increments only during internally-terminated burst cycles (CSCRn[AA] = 1b). The attached device must be able to

account for this, or a wait state must be added. The first address is driven throughout the entire burst for externally-terminated cycles.

In multiplexed address/data mode, the address is driven on FB_AD only during the first cycle for internally- and externally-terminated cycles.

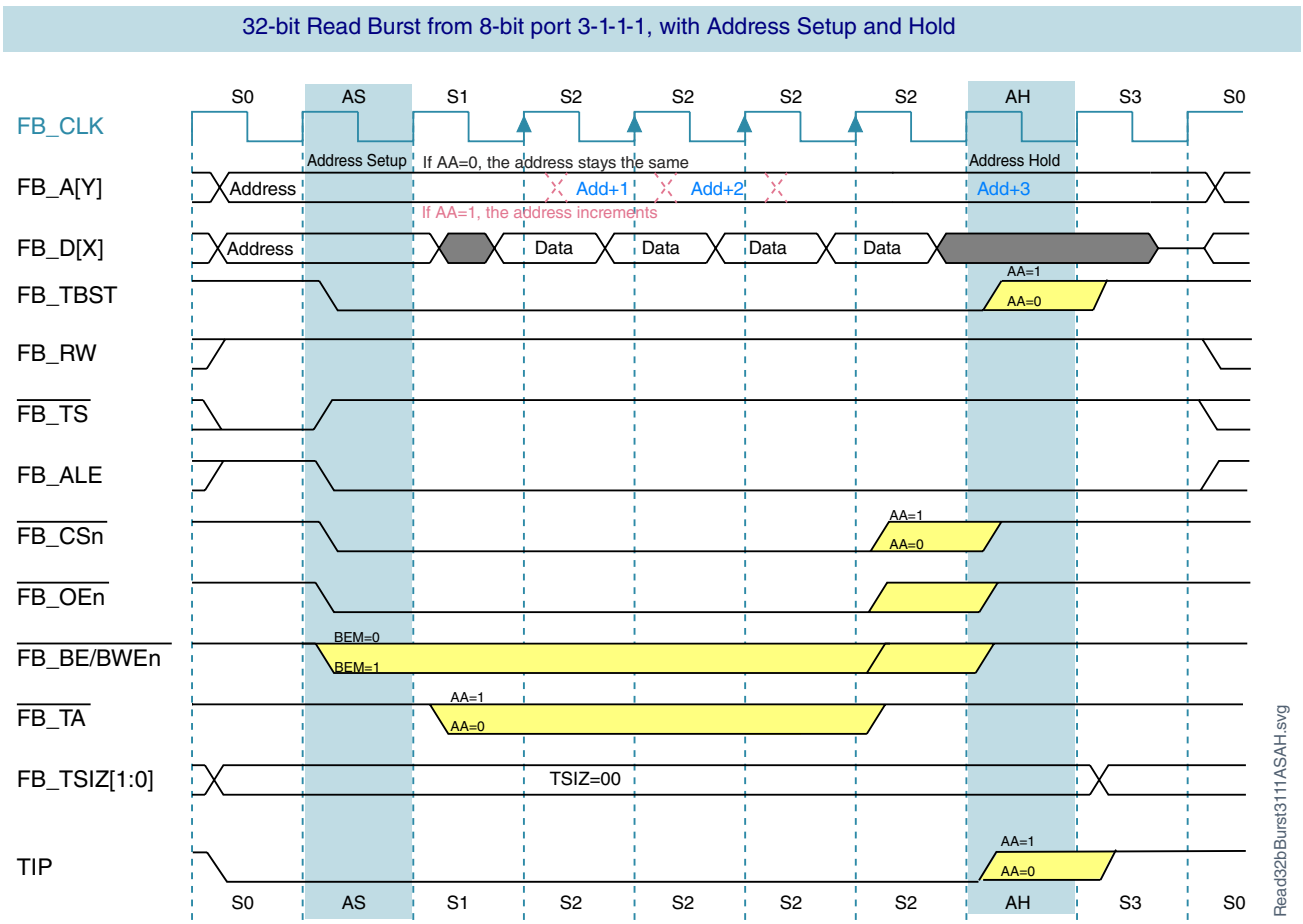


Figure 38-28. 32-bit-read burst from 8-bit port 3-1-1-1 (address setup and hold)

38.5.12.10 32-bit-write burst to 8-bit port 3-1-1-1 (address setup and hold)

The following figure shows a write cycle with one clock of address setup and address hold.

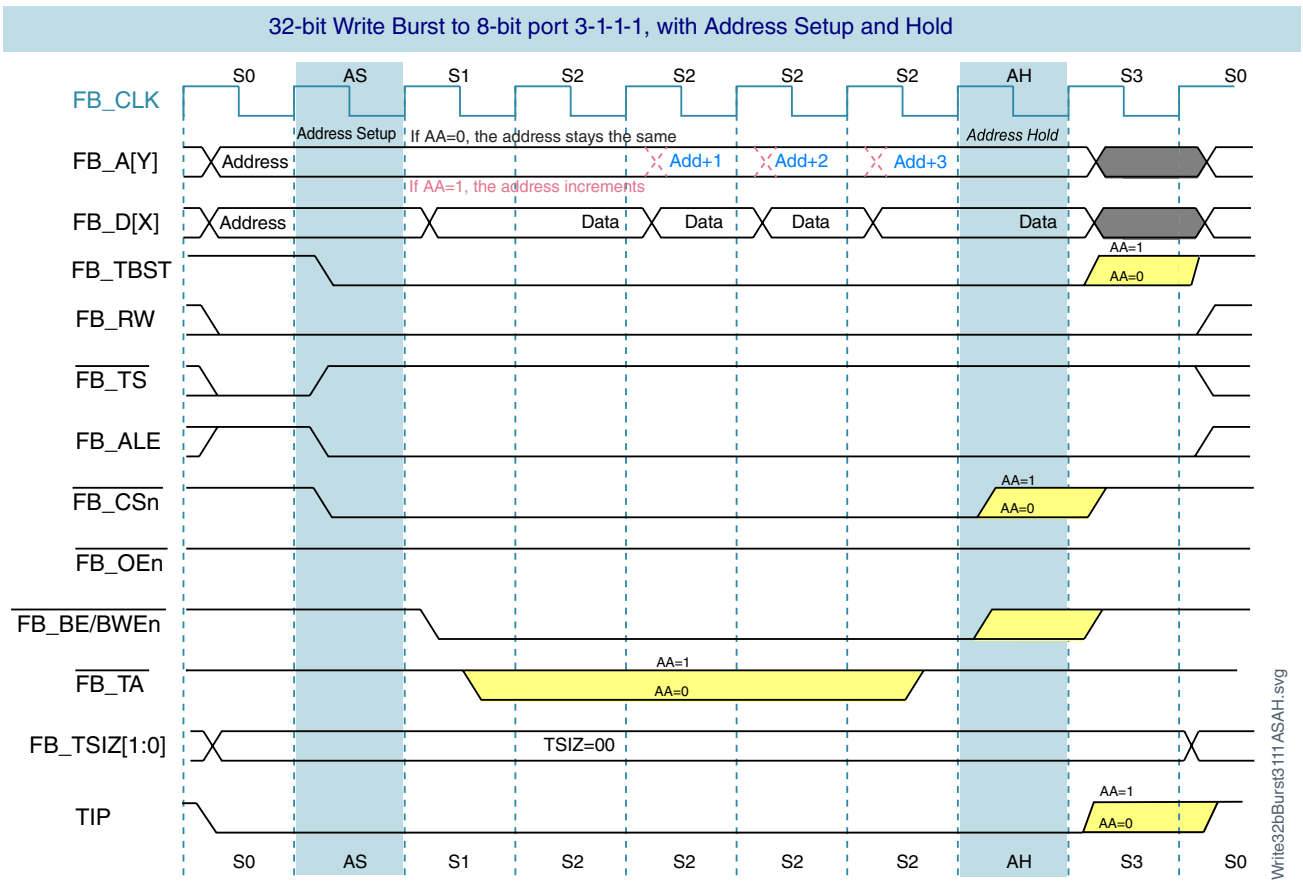


Figure 38-29. 32-bit-write burst to 8-bit port 3-1-1-1 (address setup and hold)

38.5.13 Extended Transfer Start/Address Latch Enable

The $\overline{\text{FB_TS}}$/FB_ALE signal indicates that a bus transaction has begun and the address and attributes are valid. By default, the $\overline{\text{FB_TS}}$/FB_ALE signal asserts for a single bus clock cycle. When CSCR*n*[EXTS] is set, the $\overline{\text{FB_TS}}$/FB_ALE signal asserts and remain asserted until the first positive clock edge after $\overline{\text{FB_CS}}$*n* asserts. See the following figure.

NOTE

When EXTS is set, CSCR*n*[WS] must be programmed to have at least one primary wait state.

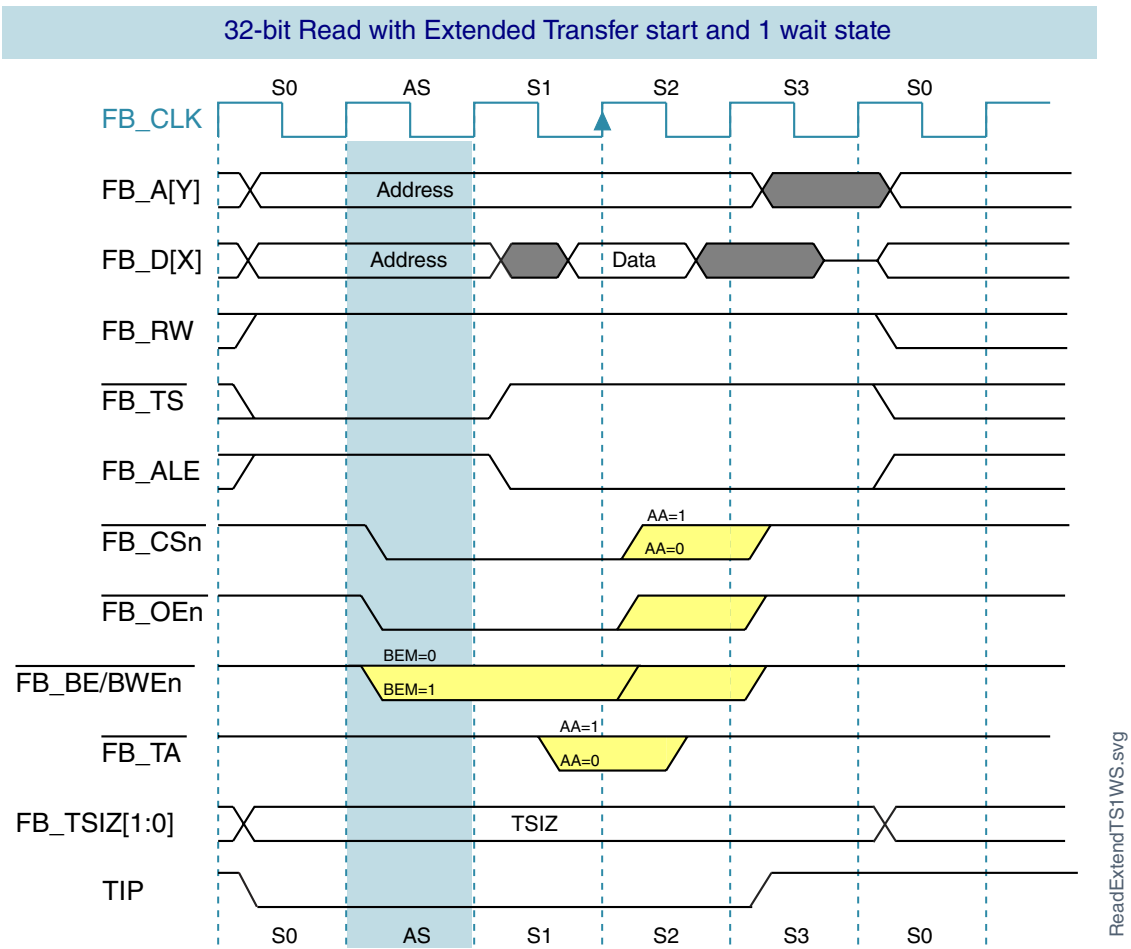


Figure 38-30. Read-Bus Cycle with CSCR*n*[EXTS] = 1 (One Wait State)

38.5.14 Bus errors

These types of accesses cause a transfer to terminate with a bus error:

- A write to a write-protected address range
- An access whose address is not in a range covered by a chip-select
- An access whose address is in a range covered by more than one chip-selects
- A write to a reserved address in the memory map
- A write to a reserved field in the CSPMCR
- Any FlexBus accesses when FlexBus is secure

If the auto-acknowledge feature is disabled (CSCR[AA] is 0) for an address that generates an error, then the transfer can be terminated by asserting $\overline{\text{FB_TA}}$. If the processor must manage a bus error differently, then asserting an interrupt to the core along with $\overline{\text{FB_TA}}$ when the bus error occurs can invoke an interrupt handler.

The device can hang if FlexBus is configured for external termination and the CSPMCR is not configured for FB_TA.

38.6 Initialization/Application Information

38.6.1 Initializing a chip-select

Before using any other chip select to take it out of global chip select mode, you must initialize CS0.

To initialize a chip-select:

1. Write to the associated CSAR.
2. Write to the associated CSCR.
3. Write to the associated CSMR, including writing 1b to the Valid field (CSMRn[V]).

38.6.2 Reconfiguring a chip-select

To reconfigure a previously-used chip-select:

1. Invalidate the chip-select by writing 0b to the associated CSMR's Valid field (CSMRn[V]).

2. Write to the associated CSAR.
3. Write to the associated CSCR.
4. Write to the associated CSMR, including writing 1b to the Valid field (CSMRn[V]).

Chapter 39
Cyclic Redundancy Check (CRC)

39.1 Introduction

The cyclic redundancy check (CRC) module generates 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial and other parameters required to implement a 16-bit or 32-bit CRC standard.

The 16/32-bit code is calculated for 32 bits of data at a time.

39.1.1 Features

Features of the CRC module include:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise. This option is required for certain CRC standards. A bytewise transpose operation is not possible when accessing the CRC data register via 8-bit accesses. In this case, the user's software must perform the bytewise transpose function.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

39.1.2 Block diagram

The following is a block diagram of the CRC.

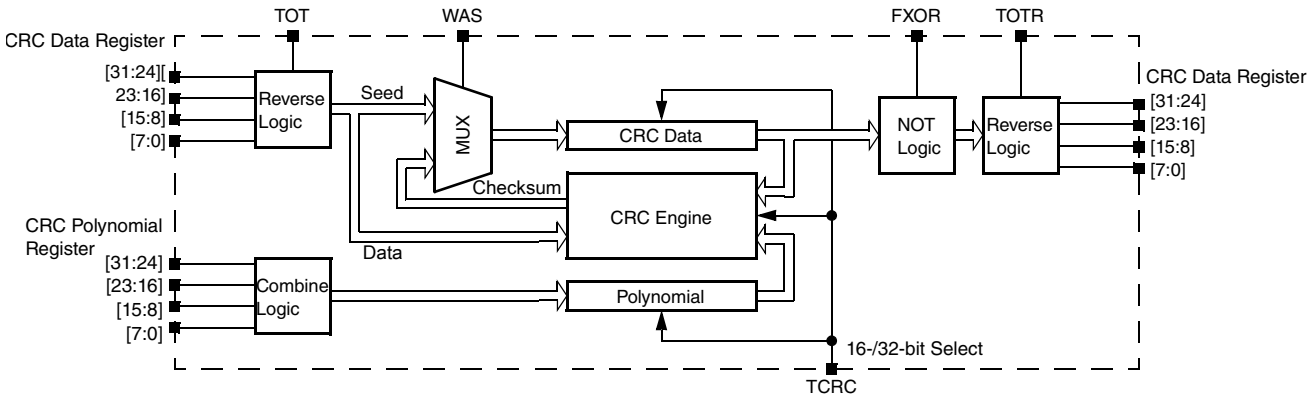


Figure 39-1. Programmable cyclic redundancy check (CRC) block diagram

39.1.3 Modes of operation

Various MCU modes affect the CRC module's functionality.

39.1.3.1 Run mode

This is the basic mode of operation.

39.1.3.2 Low-power modes (Wait or Stop)

Any CRC calculation in progress stops when the MCU enters a low-power mode that disables the module clock. It resumes after the clock is enabled or via the system reset for exiting the low-power mode. Clock gating for this module is dependent on the MCU.

39.2 Memory map and register descriptions

CRC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_2000	CRC Data register (CRC_DATA)	32	R/W	FFFF_FFFFh	39.2.1/1101
4003_2004	CRC Polynomial register (CRC_GPOLY)	32	R/W	0000_1021h	39.2.2/1102
4003_2008	CRC Control register (CRC_CTRL)	32	R/W	0000_0000h	39.2.3/1102

39.2.1 CRC Data register (CRC_DATA)

The CRC Data register contains the value of the seed, data, and checksum. When CTRL[WAS] is set, any write to the data register is regarded as the seed value. When CTRL[WAS] is cleared, any write to the data register is regarded as data for general CRC computation.

In 16-bit CRC mode, the HU and HL fields are not used for programming the seed value, and reads of these fields return an indeterminate value. In 32-bit CRC mode, all fields are used for programming the seed value.

When programming data values, the values can be written 8 bits, 16 bits, or 32 bits at a time, provided all bytes are contiguous; with MSB of data value written first.

After all data values are written, the CRC result can be read from this data register. In 16-bit CRC mode, the CRC result is available in the LU and LL fields. In 32-bit CRC mode, all fields contain the result. Reads of this register at any time return the intermediate CRC value, provided the CRC module is configured.

Address: 4003_2000h base + 0h offset = 4003_2000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	HU								HL								LU								LL							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

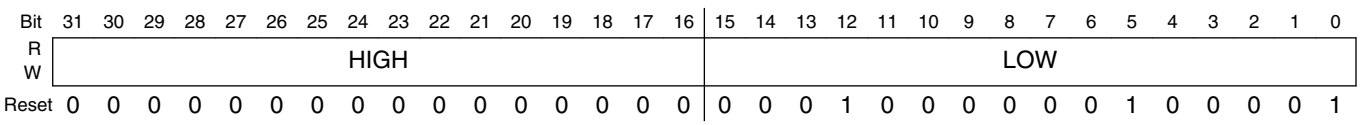
CRC_DATA field descriptions

Field	Description
31–24 HU	CRC High Upper Byte In 16-bit CRC mode (CTRL[TCRC] is 0), this field is not used for programming a seed value. In 32-bit CRC mode (CTRL[TCRC] is 1), values written to this field are part of the seed value when CTRL[WAS] is 1. When CTRL[WAS] is 0, data written to this field is used for CRC checksum generation in both 16-bit and 32-bit CRC modes.
23–16 HL	CRC High Lower Byte In 16-bit CRC mode (CTRL[TCRC] is 0), this field is not used for programming a seed value. In 32-bit CRC mode (CTRL[TCRC] is 1), values written to this field are part of the seed value when CTRL[WAS] is 1. When CTRL[WAS] is 0, data written to this field is used for CRC checksum generation in both 16-bit and 32-bit CRC modes.
15–8 LU	CRC Low Upper Byte When CTRL[WAS] is 1, values written to this field are part of the seed value. When CTRL[WAS] is 0, data written to this field is used for CRC checksum generation.
LL	CRC Low Lower Byte When CTRL[WAS] is 1, values written to this field are part of the seed value. When CTRL[WAS] is 0, data written to this field is used for CRC checksum generation.

39.2.2 CRC Polynomial register (CRC_GPOLY)

This register contains the value of the polynomial for the CRC calculation. The HIGH field contains the upper 16 bits of the CRC polynomial, which are used only in 32-bit CRC mode. Writes to the HIGH field are ignored in 16-bit CRC mode. The LOW field contains the lower 16 bits of the CRC polynomial, which are used in both 16- and 32-bit CRC modes.

Address: 4003_2000h base + 4h offset = 4003_2004h



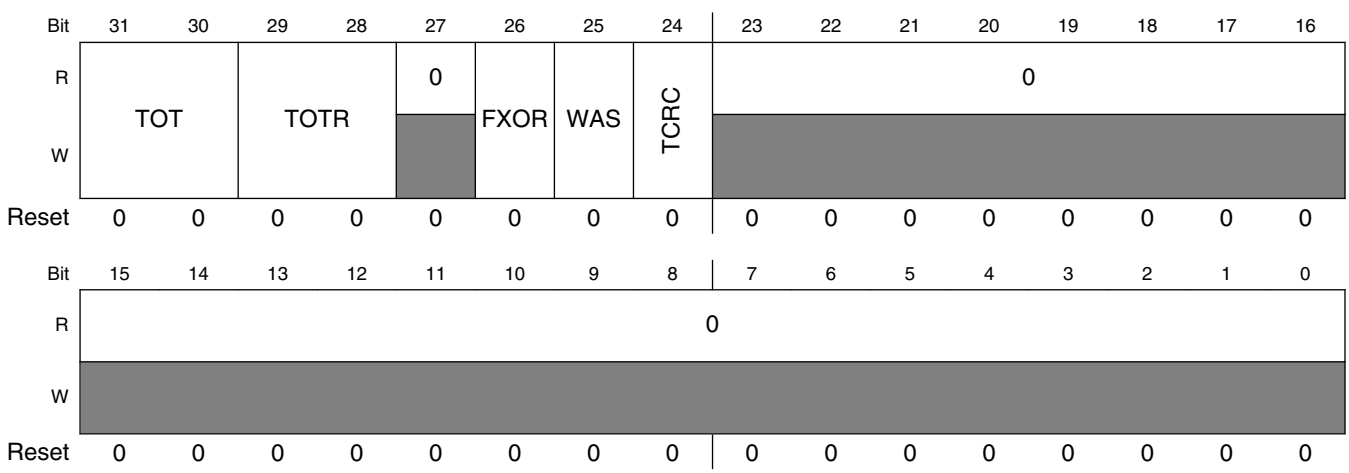
CRC_GPOLY field descriptions

Field	Description
31–16 HIGH	High Polynominal Half-word Writable and readable in 32-bit CRC mode (CTRL[TCRC] is 1). This field is not writable in 16-bit CRC mode (CTRL[TCRC] is 0).
LOW	Low Polynominal Half-word Writable and readable in both 32-bit and 16-bit CRC modes.

39.2.3 CRC Control register (CRC_CTRL)

This register controls the configuration and working of the CRC module. Appropriate bits must be set before starting a new CRC calculation. A new CRC calculation is initialized by asserting CTRL[WAS] and then writing the seed into the CRC data register.

Address: 4003_2000h base + 8h offset = 4003_2008h



CRC_CTRL field descriptions

Field	Description
31–30 TOT	Type Of Transpose For Writes Defines the transpose configuration of the data written to the CRC data register. See the description of the transpose feature for the available transpose options. 00 No transposition. 01 Bits in bytes are transposed; bytes are not transposed. 10 Both bits in bytes and bytes are transposed. 11 Only bytes are transposed; no bits in a byte are transposed.
29–28 TOTR	Type Of Transpose For Read Identifies the transpose configuration of the value read from the CRC Data register. See the description of the transpose feature for the available transpose options. 00 No transposition. 01 Bits in bytes are transposed; bytes are not transposed. 10 Both bits in bytes and bytes are transposed. 11 Only bytes are transposed; no bits in a byte are transposed.
27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 FXOR	Complement Read Of CRC Data Register Some CRC protocols require the final checksum to be XORed with 0xFFFFFFFF or 0xFFFF. Asserting this bit enables on the fly complementing of read data. 0 No XOR on reading. 1 Invert or complement the read value of the CRC Data register.
25 WAS	Write CRC Data Register As Seed When asserted, a value written to the CRC data register is considered a seed value. When deasserted, a value written to the CRC data register is taken as data for CRC computation. 0 Writes to the CRC data register are data values. 1 Writes to the CRC data register are seed values.
24 TCRC	Width of CRC protocol. 0 16-bit CRC protocol. 1 32-bit CRC protocol.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

39.3 Functional description

39.3.1 CRC initialization/reinitialization

To enable the CRC calculation, the user must program CRC_CTRL[WAS], CRC_GPOLY,necessary parameters for transposition and CRC result inversion in the applicable registers. Asserting CRC_CTRL[WAS] enables the programming of the seed value into the CRC_DATA register.

After a completed CRC calculation, the module can be reinitialized for a new CRC computation by reasserting CRC_CTRL[WAS] and programming a new, or previously used, seed value. All other parameters must be set before programming the seed value and subsequent data values.

39.3.2 CRC calculations

In 16-bit and 32-bit CRC modes, data values can be programmed 8 bits, 16 bits, or 32 bits at a time, provided all bytes are contiguous. Noncontiguous bytes can lead to an incorrect CRC computation.

39.3.2.1 16-bit CRC

To compute a 16-bit CRC:

1. Clear CRC_CTRL[TCRC] to enable 16-bit CRC mode.
2. Program the transpose and complement options in the CTRL register as required for the CRC calculation. See Transpose feature and CRC result complement for details.
3. Write a 16-bit polynomial to the CRC_GPOLY[LOW] field. The CRC_GPOLY[HIGH] field is not usable in 16-bit CRC mode.
4. Set CRC_CTRL[WAS] to program the seed value.
5. Write a 16-bit seed to CRC_DATA[LU:LL]. CRC_DATA[HU:HL] are not used.
6. Clear CRC_CTRL[WAS] to start writing data values.
7. Write data values into CRC_DATA[HU:HL:LU:LL]. A CRC is computed on every data value write, and the intermediate CRC result is stored back into CRC_DATA[LU:LL].
8. When all values have been written, read the final CRC result from CRC_DATA[LU:LL].

Transpose and complement operations are performed on the fly while reading or writing values. See Transpose feature and CRC result complement for details.

39.3.2.2 32-bit CRC

To compute a 32-bit CRC:

1. Set CRC_CTRL[TCRC] to enable 32-bit CRC mode.
2. Program the transpose and complement options in the CTRL register as required for the CRC calculation. See Transpose feature and CRC result complement for details.
3. Write a 32-bit polynomial to CRC_GPOLY[HIGH:LOW].
4. Set CRC_CTRL[WAS] to program the seed value.
5. Write a 32-bit seed to CRC_DATA[HU:HL:LU:LL].
6. Clear CRC_CTRL[WAS] to start writing data values.
7. Write data values into CRC_DATA[HU:HL:LU:LL]. A CRC is computed on every data value write, and the intermediate CRC result is stored back into CRC_DATA[HU:HL:LU:LL].
8. When all values have been written, read the final CRC result from CRC_DATA[HU:HL:LU:LL]. The CRC is calculated bytewise, and two clocks are required to complete one CRC calculation.

Transpose and complement operations are performed on the fly while reading or writing values. See Transpose feature and CRC result complement for details.

39.3.3 Transpose feature

By default, the transpose feature is not enabled. However, some CRC standards require the input data and/or the final checksum to be transposed. The user software has the option to configure each transpose operation separately, as desired by the CRC standard. The data is transposed on the fly while being read or written.

Some protocols use little endian format for the data stream to calculate a CRC. In this case, the transpose feature usefully flips the bits. This transpose option is one of the types supported by the CRC module.

39.3.3.1 Types of transpose

The CRC module provides several types of transpose functions to flip the bits and/or bytes, for both writing input data and reading the CRC result, separately using the CTRL[TOT] or CTRL[TOTR] fields, according to the CRC calculation being used.

The following types of transpose functions are available for writing to and reading from the CRC data register:

1. CTRL[TOT] or CTRL[TOTR] is 00.

No transposition occurs.

2. CTRL[TOT] or CTRL[TOTR] is 01

   Bits in a byte are transposed, while bytes are not transposed.

   reg[31:0] becomes {reg[24:31], reg[16:23], reg[8:15], reg[0:7]}

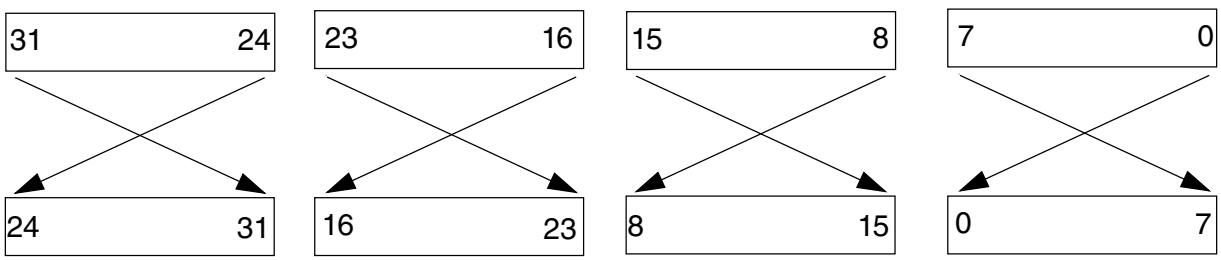


Figure 39-2. Transpose type 01

3. CTRL[TOT] or CTRL[TOTR] is 10.

   Both bits in bytes and bytes are transposed.

   reg[31:0] becomes = {reg[0:7], reg[8:15],reg[16:23], reg[24:31]}

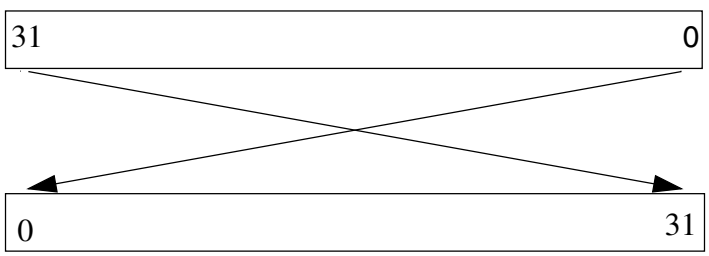


Figure 39-3. Transpose type 10

4. CTRL[TOT] or CTRL[TOTR] is 11.

   Bytes are transposed, but bits are not transposed.

   reg[31:0] becomes {reg[7:0], reg[15:8], reg[23:16], reg[31:24]}

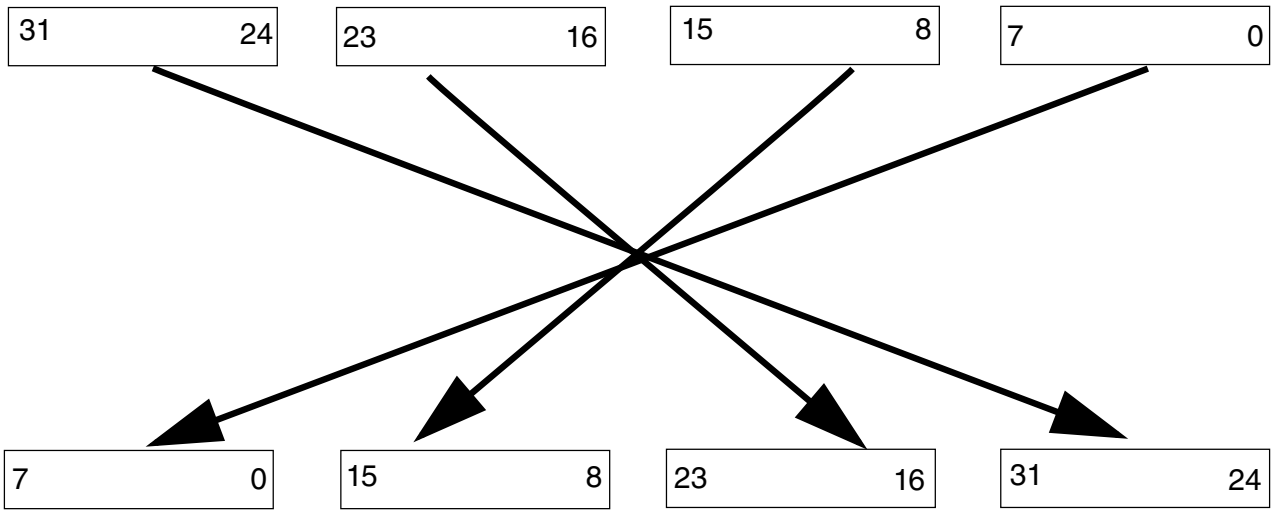


Figure 39-4. Transpose type 11

NOTE

For 8-bit and 16-bit write accesses to the CRC data register, the data is transposed with zeros on the unused byte or bytes (taking 32 bits as a whole), but the CRC is calculated on the valid byte(s) only. When reading the CRC data register for a 16-bit CRC result and using transpose options 10 and 11, the resulting value after transposition resides in the CRC[HU:HL] fields. The user software must account for this situation when reading the 16-bit CRC result, so reading 32 bits is preferred.

39.3.4 CRC result complement

When CTRL[FXOR] is set, the checksum is complemented. The CRC result complement function outputs the complement of the checksum value stored in the CRC data register every time the CRC data register is read. When CTRL[FXOR] is cleared, reading the CRC data register accesses the raw checksum value.

Chapter 40
Memory-Mapped Cryptographic Acceleration Unit (MMCAU)

40.1 Overview

The set of implemented algorithms provides excellent support for network security standards, such as SSL and IPsec. Additionally, using the CAU efficiently permits the implementation of any higher level functions or modes of operation, such as HMAC, CBC, and so on based on the supported algorithms.

The cryptographic algorithms are implemented partially in software with only functions critical to increasing performance implemented in hardware. The CAU allows for efficient, fine-grained partitioning of functions between hardware and software:

- Implement the innermost security kernel functions using the coprocessor instructions.
- Implement higher level functions in software by using the standard processor instructions.

This partitioning of functions is key to minimizing size of the CAU while maintaining a high level of throughput. Using software for some functions also simplifies the CAU design. The CAU implements a set of coprocessor commands that operate on a register file of 32-bit registers.

40.2 Features

The CAU includes the following distinctive features:

- Supports DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
- Simple, flexible programming model

40.3 Register definition

The CAU contains multiple registers used by each of the supported algorithms. The following table shows registers that are applicable to each supported algorithm and indicates the corresponding letter designations for each algorithm.

For more information on these letter designations, see the supported algorithm specifications.

Code	Register	DES	AES	MD5	SHA-1	SHA-256
0	CAU Status Register (CASR)	—	—	—	—	—
1	CAU Accumulator (CAA)	—	—	a	T	T
2	General-Purpose Register 0 (CA0)	C	W0	—	A	A
3	General-Purpose Register 1 (CA1)	D	W1	b	B	B
4	General-Purpose Register 2 (CA2)	L	W2	c	C	C
5	General-Purpose Register 3 (CA3)	R	W3	d	D	D
6	General-Purpose Register 4 (CA4)	—	—	—	E	E
7	General-Purpose Register 5 (CA5)	—	—	—	W	F
8	General-Purpose Register 6 (CA6)	—	—	—	—	G
9	General-Purpose Register 7 (CA7)	—	—	—	—	H

Table continues on the next page...

Code	Register	DES	AES	MD5	SHA-1	SHA-256
10	General-Purpose Register 8 (CA8)	—	—	—	—	W/T_1

The CAU supports only 32-bit operations and register accesses. All registers support read, write, and ALU operations. However, only bits 1–0 of the CASR are writeable. Bits 31–2 of the CASR must be written as 0 for compatibility with future versions of the CAU.

NOTE

In the following table, the "address" or "offset" refers to the command code value for the CAU registers.

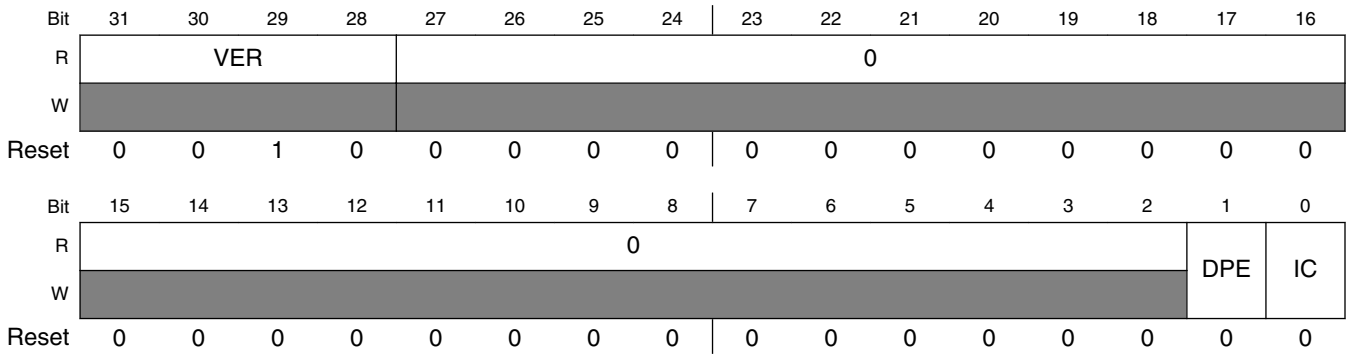
CAU memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
E008_1000	Status Register (CAU_CASR)	32	R/W	2000_0000h	40.3.1/1112
E008_1001	Accumulator (CAU_CAA)	32	R/W	0000_0000h	40.3.2/1113
E008_1002	General Purpose Register (CAU_CA0)	32	R/W	0000_0000h	40.3.3/1113
E008_1003	General Purpose Register (CAU_CA1)	32	R/W	0000_0000h	40.3.3/1113
E008_1004	General Purpose Register (CAU_CA2)	32	R/W	0000_0000h	40.3.3/1113
E008_1005	General Purpose Register (CAU_CA3)	32	R/W	0000_0000h	40.3.3/1113
E008_1006	General Purpose Register (CAU_CA4)	32	R/W	0000_0000h	40.3.3/1113
E008_1007	General Purpose Register (CAU_CA5)	32	R/W	0000_0000h	40.3.3/1113
E008_1008	General Purpose Register (CAU_CA6)	32	R/W	0000_0000h	40.3.3/1113
E008_1009	General Purpose Register (CAU_CA7)	32	R/W	0000_0000h	40.3.3/1113
E008_100A	General Purpose Register (CAU_CA8)	32	R/W	0000_0000h	40.3.3/1113

40.3.1 Status Register (CAU_CASR)

CASR contains the status and configuration for the CAU.

Address: E008_1000h base + 0h offset = E008_1000h



CAU_CASR field descriptions

Field	Description
31–28 VER	CAU Version Indicates CAU version. 0x1 Initial CAU version. 0x2 Second version, added support for SHA-256 algorithm (This is the value on this device).
27–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 DPE	DES Parity Error Indicates whether the DES parity error is detected. 0 No error detected. 1 DES key parity error detected.
0 IC	Illegal Command Indicates an illegal instruction has been executed. 0 No illegal commands issued. 1 Illegal command issued.

40.3.2 Accumulator (CAU_CAA)

Commands use the CAU accumulator for storage of results and as an operand for the cryptographic algorithms.

Address: E008_1000h base + 1h offset = E008_1001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	ACC																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CAU_CAA field descriptions

Field	Description
ACC	Accumulator Stores results of various CAU commands.

40.3.3 General Purpose Register (CAU_CA*n*)

The General Purpose Register is used in the CAU commands for storage of results and as operands for various cryptographic algorithms.

Address: E008_1000h base + 2h offset + (1d × i), where i=0d to 8d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	CAn																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CAU_CA*n* field descriptions

Field	Description
CAn	General Purpose Registers Used by the CAU commands. Some cryptographic operations work with specific registers.

40.4 Functional description

This section discusses the programming model and operation of the CAU.

40.4.1 CAU commands

The CAU supports the commands shown in the following table. All other encodings are reserved. The CASR[IC] bit is set if an undefined command is issued. A specific illegal command (ILL) is defined to allow software self-checking. Reserved commands must not be issued so as to ensure compatibility with future implementations.

The CMD field specifies the 9-bit CAU opcode for the operation command.

See Assembler equate values for a set of assembly constants used in the command descriptions here. If supported by the assembler, macros can also be created for each instruction. The value CA*x* should be interpreted as any CAU register (CASR, CAA, and CA*n*)

Table 40-1. CAU commands

Type	Command name	Description	CMD									Operation
			8	7	6	5	4	3	2	1	0	
	CNOP	No Operation	0x000									—
	LDR	Load Reg	0x01					CAx				Op1 → CAx
	STR	Store Reg	0x02					CAx				CAx → Result
	ADR	Add	0x03					CAx				CAx + Op1 → CAx
	RADR	Reverse and Add	0x04					CAx				CAx + ByteRev(Op1) → CAx
	ADRA	Add Reg to Acc	0x05					CAx				CAx + CAA → CAA
	XOR	Exclusive Or	0x06					CAx				CAx ^ Op1 → CAx
	ROTL	Rotate Left	0x07					CAx				(CAx <<< (Op1 % 32)) | (CAx >>> (32 - (Op1 % 32))) → CAx
	MVRA	Move Reg to Acc	0x08					CAx				CAx → CAA
	MVAR	Move Acc to Reg	0x09					CAx				CAA → CAx
	AESS	AES Sub Bytes	0x0A					CAx				SubBytes(CAx) → CAx
	AESIS	AES Inv Sub Bytes	0x0B					CAx				InvSubBytes(CAx) → CAx
	AESC	AES Column Op	0x0C					CAx				MixColumns(CAx)^Op1→ CAx
	AESIC	AES Inv Column Op	0x0D					CAx				InvMixColumns(CAx^Op1) → CAx
	AESR	AES Shift Rows	0x0E0									ShiftRows(CA0-CA3) → CA0-CA3
	AESIR	AES Inv Shift Rows	0x0F0									InvShiftRows(CA0-CA3)→ CA0-CA3
	DESR	DES Round	0x10					IP	FP	KS[1:0]		DES Round(CA0-CA3) →CA0-CA3
	DESK	DES Key Setup	0x11					0	0	CP	DC	DES Key Op(CA0-CA1)→ CA0-CA1 Key Parity Error & CP → CASR[1]

Table continues on the next page...

Table 40-1. CAU commands (continued)

Type	Command name	Description	CMD									Operation
			8	7	6	5	4	3	2	1	0	
	HASH	Hash Function	0x12					0	HF[2:0]			Hash Func(CA1-CA3)+CAA→ CAA
	SHS	Secure Hash Shift	0x130									CAA <<< 5→ CAA, CAA→CA0, CA0→CA1, CA1 <<< 30 → CA2, CA2→CA3, CA3→CA4
	MDS	Message Digest Shift	0x140									CA3→CAA, CAA→CA1, CA1→CA2, CA2→CA3,
	SHS2	Secure Hash Shift 2	0x150									CAA→CA0, CA0→CA1, CA1 → CA2, CA2→CA3, CA3 + CA8 →CA4, CA4 → CA5, CA5 → CA6, CA6 → CA7
	ILL	Illegal Command	0x1F0									0x1→CASR[IC]

40.4.1.1 Coprocessor No Operation (CNOP)

The CNOP command is the coprocessor no-op

40.4.1.2 Load Register (LDR)

The LDR command loads CAx with the source data specified by .

40.4.1.3 Store Register (STR)

The STR command returns the value of CAx to the destination specified .

40.4.1.4 Add to Register (ADR)

The ADR command adds the source operand specified by to CAx and stores the result in CAx.

40.4.1.5 Reverse and Add to Register (RADR)

The RADR command performs a byte reverse on the source operand specified by , adds that value to CAx, and stores the result in CAx. The table below shows an example.

Table 40-2. RADR command example

Operand	CAx before	CAx after
0x0102_0304	0xA0B0_C0D0	0xA4B3_C2D1

40.4.1.6 Add Register to Accumulator (ADRA)

The ADRA command adds CAx to CAA and stores the result in CAA.

40.4.1.7 Exclusive Or (XOR)

The XOR command performs an exclusive-or of the source operand specified by with CAx and stores the result in CAx.

40.4.1.8 Rotate Left (ROTL)

ROTL rotates the CAx bits to the left with the result stored back to CAx. The number of bits to rotate is the value specified by modulo 32.

40.4.1.9 Move Register to Accumulator (MVRA)

The MVRA command moves the value from the source register CAx to the destination register CAA.

40.4.1.10 Move Accumulator to Register (MVAR)

The MVAR command moves the value from source register CAA to the destination register CAx.

40.4.1.11 AES Substitution (AESS)

The AESS command performs the AES byte substitution operation on CAx and stores the result back to CAx.

40.4.1.12 AES Inverse Substitution (AESIS)

The AESIS command performs the AES inverse byte substitution operation on CAx and stores the result back to CAx.

40.4.1.13 AES Column Operation (AESC)

The AESC command performs the AES column operation on the contents of CAx. It then performs an exclusive-or of that result with the source operand specified by and stores the result in CAx.

40.4.1.14 AES Inverse Column Operation (AESIC)

The AESIC command performs an exclusive-or operation of the source operand specified by on the contents of CAx followed by the AES inverse mix column operation on that result and stores the result back in CAx.

40.4.1.15 AES Shift Rows (AESR)

The AESR command performs the AES shift rows operation on registers CA0, CA1, CA2, and CA3. The table below shows an example.

Table 40-3. AESR command example

Register	Before	After
CA0	0x0102_0304	0x0106_0B00
CA1	0x0506_0708	0x050A_0F04
CA2	0x090A_0B0C	0x090E_0308
CA3	0x0D0E_0F00	0x0D02_070C

Where:

- row 1 = CA0[31:24], CA1[31:24], CA2[31:24], CA3[31:24]
- row 2 = CA0[23:16], CA1[23:16], CA2[23:16], CA3[23:16]

- row 3 = CA0[15:8], CA1[15:8], CA2[15:8], CA3[15:8]
- row 4 = CA0[7:0], CA1[7:0], CA2[7:0], CA3[7:0]

40.4.1.16 AES Inverse Shift Rows (AESIR)

The AESIR command performs the AES inverse shift rows operation on registers CA0, CA1, CA2, and CA3. The table below shows an example.

Table 40-4. AESIR command example

Register	Before	After
CA0	0x0106_0B00	0x0102_0304
CA1	0x050A_0F04	0x0506_0708
CA2	0x090E_0308	0x090A_0B0C
CA3	0x0D02_070C	0x0D0E_0F00

Where:

- row 1 = CA0[31:24], CA1[31:24], CA2[31:24], CA3[31:24]
- row 2 = CA0[23:16], CA1[23:16], CA2[23:16], CA3[23:16]
- row 3 = CA0[15:8], CA1[15:8], CA2[15:8], CA3[15:8]
- row 4 = CA0[7:0], CA1[7:0], CA2[7:0], CA3[7:0]

40.4.1.17 DES Round (DESR)

The DESR command performs a round of the DES algorithm and a key schedule update with the following source and destination designations: CA0=C, CA1=D, CA2=L, CA3=R. If the IP bit is set, DES initial permutation performs on CA2 and CA3 before the round operation. If the FP bit is set, DES final permutation, that is, inverse initial permutation, performs on CA2 and CA3 after the round operation. The round operation uses the source values from registers CA0 and CA1 for the key addition operation. The KSx field specifies the shift for the key schedule operation to update the values in CA0 and CA1. The following table defines the specific shift function performed based on the KSx field.

Table 40-5. Key shift function codes

KSx code	KSx define	Shift function
0	KSL1	Left 1
1	KSL2	Left 2
2	KSR1	Right 1
3	KSR2	Right 2

40.4.1.18 DES Key setup (DESK)

The DESK command performs the initial key transformation, permuted choice 1, defined by the DES algorithm on CA0 and CA1 with CA0 containing bits 1–32 of the key and CA1 containing bits 33–64 of the key[1] . If the DC bit is set, no shift operation performs and the values C_0 and D_0 store back to CA0 and CA1, respectively. The DC bit must be set for decrypt operations. If the DC bit is not set, a left shift by one also occurs and the values C_1 and D_1 store back to CA0 and CA1, respectively. The DC bit should be cleared for encrypt operations. If the CP bit is set and a key parity error is detected, CASR[DPE] bit is set; otherwise, it is cleared.

40.4.1.19 Hash Function (HASH)

The HASH command performs a hashing operation on a set of registers and adds that result to the value in CAA and stores the result in CAA. The specific hash function performed is based on the HFx field as defined in the table below.

This table uses the following terms:

- ROTR^n(CAx): rotate CAx register right *n* times
- SHR^n(CAx): shift CAx register right *n* times

Table 40-6. Hash Function codes

HFx code	HFx define	Hash Function	Hash logic
0	HFF	MD5 F()	(CA1 & CA2) | ($\overline{CA1}$ & CA3)
1	HFG	MD5 G()	(CA1 & CA3) | (CA2 & $\overline{CA3}$)
2	HFH	MD5 H(), SHA Parity()	CA1 ^ CA2 ^ CA3
3	HFI	MD5 I()	CA2 ^ (CA1 | $\overline{CA3}$)
4	HFC	SHA Ch()	(CA1 & CA2) ^ ($\overline{CA1}$ & CA3)
5	HFM	SHA Maj()	(CA1 & CA2) ^ (CA1 & CA3) ^ (CA2 & CA3)
6	HF2C	SHA-256 Ch()	(CA4 & CA5) ^ ($\overline{CA1}$ & CA6)
7	HF2M	SHA-256 Maj()	(CA0 & CA1) ^ (CA0 & CA2) ^ (CA1 & CA2)
8	HF2S	SHA-256 Sigma 0	ROTR^2(CA0) ^ ROTR^{13}(CA0) ^ ROTR^{22}(CA0)
9	HF2T	SHA-256 Sigma 1	ROTR^6(CA4) ^ ROTR^{11}(CA4) ^ ROTR^{25}(CA4)
A	HF2U	SHA-256 Sigma 0	ROTR^7(CA8) ^ ROTR^{18}(CA8) ^ SHR^3(CA8)
B	HF2V	SHA-256 Sigma 1	ROTR^{17}(CA8) ^ ROTR^{19}(CA8) ^ SHR^{10}(CA8)

1. The DES algorithm numbers the most significant bit of a block as bit 1 and the least significant as bit 64.

40.4.1.20 Secure Hash Shift (SHS)

The SHS command does a set of parallel register-to-register move and shift operations for implementing SHA-1. The following source and destination assignments are made:

Register	Value prior to command	Value after command executes
CA4	CA4	CA3
CA3	CA3	CA2
CA2	CA2	CA1<<<30
CA1	CA1	CA0
CA0	CA0	CAA
CAA	CAA	CAA<<<5

40.4.1.21 Message Digest Shift (MDS)

The MDS command does a set of parallel register-to-register move operations for implementing MD5. The following source and destination assignments are made:

Register	Value prior to command	Value after command executes
CA3	CA3	CA2
CA2	CA2	CA1
CA1	CA1	CAA
CAA	CAA	CA3

40.4.1.22 Secure Hash Shift 2 (SHS2)

The SHS2 command does an addition and a set of register to register moves in parallel for implementing SHA-256. The following source and destination assignments are made:

Register	Value prior to command	Value after command executes
CA7	CA7	CA6
CA6	CA6	CA5
CA5	CA5	CA4
CA4	CA4	CA3+CA8
CA3	CA3	CA2
CA2	CA2	CA1
CA1	CA1	CA0
CA0	CA0	CAA

40.4.1.23 Illegal command (ILL)

The ILL command is a specific illegal command that sets CASR[IC]. All other illegal commands are reserved for use in future implementations.

40.5 Application/initialization information

This section discusses how to initialize and use the CAU.

40.5.1 Code example

A code fragment is shown below as an example of how the CAU is used. This example shows the round function of the AES algorithm.

40.5.2 Assembler equate values

The following equates ease programming of the CAU.

```
; CAU Registers (CAx)
      .set CASR,0x0
      .set CAA,0x1
      .set CA0,0x2
      .set CA1,0x3
      .set CA2,0x4
      .set CA3,0x5
      .set CA4,0x6
      .set CA5,0x7
      .set CA6,0x8
      .set CA7,0x9
      .set CA8,0xA
; CAU Commands
      .set CNOP,0x000
      .set LDR,0x010
      .set STR,0x020
      .set ADR,0x030
      .set RADR,0x040
      .set ADRA,0x050
      .set XOR,0x060
      .set ROTL,0x070
      .set MVRA,0x080
      .set MVAR,0x090
      .set AESS,0x0A0
      .set AESIS,0x0B0
      .set AESC,0x0C0
      .set AESIC,0x0D0
      .set AESR,0x0E0
      .set AESIR,0x0F0
      .set DESR,0x100
      .set DESK,0x110
      .set HASH,0x120
      .set SHS,0x130
      .set MDS,0x140
      .set SHS2,0x150
```

```
     .set ILL,0x1F0
; DESR  Fields
     .set IP,0x08          ; initial permutation
     .set FP,0x04          ; final permutation
     .set KSL1,0x00        ; key schedule left 1 bit
     .set KSL2,0x01        ; key schedule left 2 bits
     .set KSR1,0x02        ; key schedule right 1 bit
     .set KSR2,0x03        ; key schedule right 2 bits
; DESK Field
     .set DC,0x01          ; decrypt key schedule
     .set CP,0x02          ; check parity
; HASH Functions Codes
     .set HFF,0x0          ; MD5 F() CA1&CA2 | ~CA1&CA3
     .set HFG,0x1          ; MD5 G() CA1&CA3 | CA2&~CA3
     .set HFH,0x2          ; MD5 H(), SHA Parity() CA1^CA2^CA3
     .set HFI,0x3          ; MD5 I()  CA2^(CA1|~CA3)
     .set HFC,0x4          ; SHA Ch() CA1&CA2 ^ ~CA1&CA3
     .set HFM,0x5          ; SHA Maj() CA1&CA2 ^ CA1&CA3 ^ CA2&CA3
     .set HF2C,0x6         ; SHA-256 Ch() CA4&CA5 ^ ~CA4&CA6
     .set HF2M,0x7         ; SHA-256 Maj() CA0&CA1 ^ CA0&CA2 ^ CA1&CA2
     .set HF2S,0x8         ; SHA-256 Sigma 0 ROTR2(CA0)^ROTR13(CA0)^ROTR22(CA0)
     .set HF2T,0x9         ; SHA-256 Sigma 1 ROTR6(CA4)^ROTR11(CA4)^ROTR25(CA4)
     .set HF2U,0xA         ; SHA-256 sigma 0 ROTR7(CA8)^ROTR18(CA8)^SHR3(CA8)
     .set HF2V,0xB         ; SHA-256 sigma 1 ROTR17(CA8)^ROTR19(CA8)^SHR10(CA8)
```

Chapter 41
True Random Number Generator

41.1 Standalone True Random Number Generator (SA-TRNG).

The Standalone True Random Number Generator (SA-TRNG) is hardware accelerator module that generates a 512-bit entropy as needed by an entropy consuming module or by other post processing functions. A typical entropy consumer is a pseudo random-number generator (PRNG) which can be implemented to achieve both true randomness and cryptographic strength random numbers using the TRNG output as its entropy seed. The PRNG is not part of this module.

The entropy generated by an TRNG is intended for direct use by functions that generate secret keys, per-message secrets, random challenges, and other similar quantities used in cryptographic algorithms. In each of these cases, it is important that a random number be difficult to guess or predict. It is important that a random number is at least as difficult to predict as it is difficult to break the cryptographic algorithm with which it is being used. This stringent requirement is particularly difficult to fulfill if the entropy source from a TRNG contains bias and/or correlation. To increase the trustworthiness/quality of the generated random data, PRNGs are often used to post process the output of a TRNG.

This document describes only the TRNG design functionality and usage.

Note that before entropy can be obtained from the TRNG, it must be initialized and instantiated in a particular mode by setting the appropriate TRNG registers.

The TRNG contains the following sub modules: IP Slave bus (SkyBlue bus) interface, the TRNG Core and the free running oscillator (OSC).

41.1.1 Standalone True Random Number Generator Block Diagram

The following figure is a top-level diagram of the True Random Number Generator.

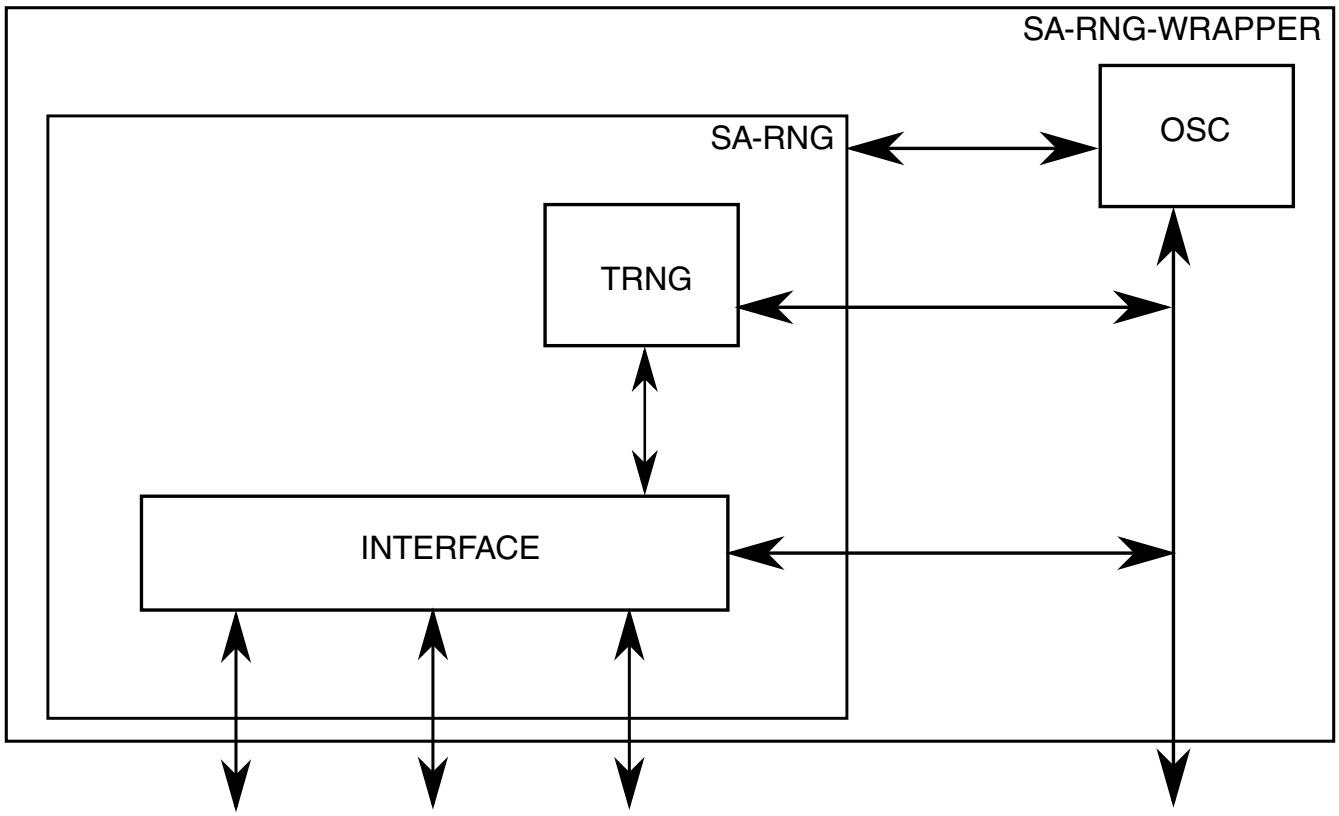


Figure 41-1. SA TRNG Block Diagram

41.1.2 TRNG Functional Description.

The TRNG consists of several functional sub-modules. Its overall functionality can be easily described from the top level in terms of generating entropy for seed generation. The functionality of each sub-module is briefly described in the following subsections.

TRNG is based on collecting bits from a random noise source. This random noise source is a ring oscillator that is sensitive to random noise (temperature variations, voltage variations, cross-talk and other random noise) within the device in which the TRNG is used. This noise causes various small changes in the period of the oscillator. Therefore, if the count of the ring oscillator clock cycles is sampled after a known period of time, this count will vary each time the sample is taken. By using the variance in this count over a large number of samples, random bits can be derived.

The TRNG comprises two entropy sources, each of which provides a single bit of output. Concatenated together, these 2 output bits are expected to provide 1 bit of entropy every 100 clock cycles. In addition to generating entropy, the TRNG also performs several statistical tests on its output.

41.1.3 SA-TRNG hardware functional description.

SA-TRNG functionality consists of several major subcomponents. This table describes these subcomponents.

Table 41-1. SA-TRNG subcomponents.

Description	Cross-reference(s)
Interfaces	
Register interface • Used for access to configuration, control, status and debugging registers	Register interface (IP Slave bus)
True Random Number Generator (TRNG)	Standalone True Random Number Generator (SA-TRNG).

41.1.3.1 Software Use Cases for the Stand Alone TRNG.

There are four things that a user (programmer/integrator) will want to do with a TRNG.

- Initialization.

  Set up the parameters to proper values, and start generation of the first block of entropy. This is done once.

- Read entropy from the TRNG, and start generation of the next block of entropy.

  This is done many times and is the normal flow of operation.

- Run a self-test on the TRNG, to assure proper continued operation.

  This involves taking TRNG off-line, setting some self-test parameters, running TRNG, and then reading the statistical test registers, to see that they are within proper operation values. This may not be needed, as TRNG has built-in self-test.

- Off-line determination and checking of TRNG parameter values.

  This is done in development in order to determine the proper initialization and self-test parameters. The TRNG is taken off-line. Test parameter values are written and entropy generation is started. If the statistical tests indicate poor operation (i.e., failing statistical tests), the entropy_delay value should be increased and entropy generation should be re-started. Every case is a variation of setting TRNG parameter values, starting or re-starting entropy generation and reading out the entropy. This process requires pausing or stopping and re-starting the TRNG.

The TRNG is designed to operate as a slave module on the standard IP Slave Bus. By understanding the TRNG register descriptions in "TRNG Register Descriptions" section below, the TRNG module can be controlled via the IP slave bus. In order to write to most TRNG registers, the MCTL register must be initialized in programming mode as described in the "TRNG Register Descriptions" section. At Power On Reset (POR), the TRNG resets to programming mode. And the it will not generate entropy until it is out of programming mode (in run mode) and access to Entropy Registers have been enabled.

Here is an example program flow of using the TRNG.

- After POR the TRNG will be reset into programming mode with the OK to stop bit set(MCTL[TSTOP_OK]=1). The TRNG must be put into Run Mode for Entropy Generation to begin (MCTL[PRGM]=0). Additionally, in order to have access to the Entropy registers and other critical TRNG registers, the TRNG access bit must be set (MCTL[TRNG_ACC]=1). Using the default self test limits that exist after bootup, the entropy valid bit can be polled until asserted (MCTL[ENT_VAL]=1). Alternatively, if using the interrupt, and the interrupts are enabled via the INT_MASK register and the ipi_rng_int_b is asserted when MCTL[ENT_VAL]=1.
- After the polling completes, the 512-bit entropy generated by the TRNG can be read. The values can be read in any order from entropy register 0 to register 15 (ENT0 to ENT 15). After reading ENT 15, the old entropy value is reset and a new entropy value is generated.

NOTE

Reading ENT 15always resets the entropy, so should always be read last.

- You can poll again for the new entropy value or you can use the Interrupt Status Register to handle reading the entropy values when the entropy valid interrupt is triggered.
- The interrupt can be masked or cleared as needed. See the Interrupt Status Register description.
- To change the self-test limits,the seed counters, how fast the entropy is generated, and how entropy is sampled, see the register description section. In particular, see the the TRNG Frequency Count Minimum Limit Register (FRQMIN), the seed control register(SCML), the statistical run length registers, and other parameter registers.
- Once in Run Mode, the entropy is re-generated automatically after ENT 15 is read. To stop the TRNG or access to TRNG registers at any point while in running mode, you can always set MCTL[TRNG_ACC]=0. Setting the TRNG back to programming mode (MCTL[PRGM]=1) also achieves the purpose of stopping entropy generation.

41.1.3.2 Register interface (IP Slave bus)

The TRNG's register interface (32-bit IP bus) is used to read and write registers within TRNG for the following purposes:

Table 41-2. Summary of register interface uses

Purpose	For more information, see
During chip initialization time	
To configure TRNG including initialization of the • Registers • TRNG Register Interface	
During hardware and software debugging	
Read status registers	• RNG TRNG Status Register • For all registers, see the TRNG Register Descriptions" appendix.

NOTE

Accesses to registers must use full-word (32-bit) reads or writes.

41.1.3.3 TRNG0 Register Descriptions

All accesses of undefined addresses always return zero and assert IPS transfer error. Writes to undefined and read-only addresses are ignored. Undefined addresses are those undocumented, protected or reserved addresses within and outside the range of the addresses defined in the memory map below. Although many of the TRNG0 registers hold more than 32 bits, the register addresses shown in the Memory Map below represent how these registers are accessed over the register bus as 32-bit words.

The format and fields in each TRNG0 register are defined below. Some of the register format figures apply to several different registers. In such cases a different register name will be associated with each of the register offset addresses that appear at the top of the register format figure. Although these registers share the same format, they are independent registers. In addition, many registers can be accessed at multiple addresses. In these cases there will be a single register name and the list of addresses at which that register is accessible will be indicated as aliases. Unless noted in the individual register descriptions, registers are reset only at Power-On Reset (POR).

41.1.3.3.1 TRNG0 Memory Map

Offset	Register	Width (In bits)	Access	Reset value
0h	TRNG0 Miscellaneous Control (TRNG0_MCTL)	32	RW	00012001h
4h	TRNG0 Statistical Check Miscellaneous (TRNG0_SCMISC)	32	RW	0001001Fh[1]
8h	TRNG0 Poker Range (TRNG0_PKRRNG)	32	RW	000009A3h
Ch	TRNG0 Poker Maximum Limit (TRNG0_PKRMAX)	32	RW	00006920h
Ch	TRNG0 Poker Square Calculation Result (TRNG0_PKRSQ)	32	RO	00000000h
10h	TRNG0 Seed Control (TRNG0_SDCTL)	32	RW	0C8009C4h
14h	TRNG0 Sparse Bit Limit (TRNG0_SBLIM)	32	RW	0000003Fh
14h	TRNG0 Total Samples (TRNG0_TOTSAM)	32	RO	00000000h
18h	TRNG0 Frequency Count Minimum Limit (TRNG0_FRQMIN)	32	RW	00000640h
1Ch	TRNG0 Frequency Count Maximum Limit (TRNG0_FRQMAX)	32	RW	00006400h
1Ch	TRNG0 Frequency Count (TRNG0_FRQCNT)	32	RO	00000000h
20h	TRNG0 Statistical Check Monobit Count (TRNG0_SCMC)	32	RO	00000000h
20h	TRNG0 Statistical Check Monobit Limit (TRNG0_SCML)	32	RW	010C0568h
24h	TRNG0 Statistical Check Run Length 1 Limit (TRNG0_SCR1L)	32	RW	00B20195h
24h	TRNG0 Statistical Check Run Length 1 Count (TRNG0_SCR1C)	32	RO	00000000h
28h	TRNG0 Statistical Check Run Length 2 Limit (TRNG0_SCR2L)	32	RW	007A00DCh
28h	TRNG0 Statistical Check Run Length 2 Count (TRNG0_SCR2C)	32	RO	00000000h
2Ch	TRNG0 Statistical Check Run Length 3 Count (TRNG0_SCR3C)	32	RO	00000000h
2Ch	TRNG0 Statistical Check Run Length 3 Limit (TRNG0_SCR3L)	32	RW	0058007Dh
30h	TRNG0 Statistical Check Run Length 4 Count (TRNG0_SCR4C)	32	RO	00000000h
30h	TRNG0 Statistical Check Run Length 4 Limit (TRNG0_SCR4L)	32	RW	0040004Bh
34h	TRNG0 Statistical Check Run Length 5 Limit (TRNG0_SCR5L)	32	RW	002E002Fh
34h	TRNG0 Statistical Check Run Length 5 Count (TRNG0_SCR5C)	32	RO	00000000h
38h	TRNG0 Statistical Check Run Length 6+ Limit (TRNG0_SCR6PL)	32	RW	002E002Fh
38h	TRNG0 Statistical Check Run Length 6+ Count (TRNG0_SCR6PC)	32	RO	00000000h
3Ch	TRNG0 Status (TRNG0_STATUS)	32	RO	00000000h
40h - 7Ch	TRNG0 Entropy Read (TRNG0_ENT0 - TRNG0_ENT15)	32	RO	00000000h
80h	TRNG0 Statistical Check Poker Count 1 and 0 (TRNG0_PKRCNT10)	32	RO	00000000h
84h	TRNG0 Statistical Check Poker Count 3 and 2 (TRNG0_PKRCNT32)	32	RO	00000000h
88h	TRNG0 Statistical Check Poker Count 5 and 4 (TRNG0_PKRCNT54)	32	RO	00000000h
8Ch	TRNG0 Statistical Check Poker Count 7 and 6 (TRNG0_PKRCNT76)	32	RO	00000000h
90h	TRNG0 Statistical Check Poker Count 9 and 8 (TRNG0_PKRCNT98)	32	RO	00000000h
94h	TRNG0 Statistical Check Poker Count B and A (TRNG0_PKRCNT BA)	32	RO	00000000h
98h	TRNG0 Statistical Check Poker Count D and C (TRNG0_PKRCNT DC)	32	RO	00000000h
9Ch	TRNG0 Statistical Check Poker Count F and E (TRNG0_PKRCNT FE)	32	RO	00000000h
B0h	TRNG0 Security Configuration (TRNG0_SEC_CFG)	32	RW	00000000h

Table continues on the next page...

Offset	Register	Width (In bits)	Access	Reset value
B4h	TRNG0 Interrupt Control (TRNG0_INT_CTRL)	32	RW	FFFFFFFFh
B8h	TRNG0 Mask (TRNG0_INT_MASK)	32	RW	00000000h
BCh	TRNG0 Interrupt Status (TRNG0_INT_STATUS)	32	RW	00000000h
F0h	TRNG0 Version ID (MS) (TRNG0_VID1)	32	RO	00300100h
F4h	TRNG0 Version ID (LS) (TRNG0_VID2)	32	RO	00000000h

1. Reset occurs at POR, and when TRNG0_MCTL[RST_DEF] is written to 1.

41.1.3.3.2 TRNG0 Miscellaneous Control (TRNG0_MCTL)

41.1.3.3.2.1 Address

Register	Offset
TRNG0_MCTL	0h

41.1.3.3.2.2 Function

This register is intended to be used for programming, configuring and testing the RNG. It is the main register to read/write, in order to enable Entropy generation, to stop entropy generation and to block access to entropy registers. This is done via the special TRNG_ACC and PRGM bits below.

The TRNG0 Miscellaneous Control Register is a read/write register used to control the RNG's True Random Number Generator (TRNG) access, operation and test.

NOTE

Note that in many cases two RNG registers share the same address, and a particular register at the shared address is selected based upon the value in the PRGM field of the TRNG0_MCTL register.

41.1.3.3.2.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved															PRGM
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved		TSTOP_OK	ERR	TST_OUT	ENT_VAL	FCT_VAL	FCT_FAIL	FOR_SCLK		TRNG_ACC	UNUSED	OSC_DIV		SAMP_MODE	
W				w1c						RST_DEF						
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1

41.1.3.3.2.4 Fields

Field	Function
31-17 —	Reserved.
16 PRGM	Programming Mode Select. When this bit is 1, the TRNG is in Program Mode, otherwise it is in Run Mode. No Entropy value will be generated while the TRNG is in Program Mode. Note that different RNG registers are accessible at the same address depending on whether PRGM is set to 1 or 0. This is noted in the RNG register descriptions.
15-14 —	Reserved.
13 TSTOP_OK	TRNG_OK_TO_STOP. Software should check that this bit is a 1 before transitioning TRNG0 to low power mode (TRNG0 clock stopped). TRNG0 turns on the TRNG free-running ring oscillator whenever new entropy is being generated and turns off the ring oscillator when entropy generation is complete. If the TRNG0 clock is stopped while the TRNG ring oscillator is running, the oscillator will continue running even though the TRNG0 clock is stopped. TSTOP_OK is asserted when the TRNG ring oscillator is not running. and therefore it is ok to stop the TRNG0 clock.
12 ERR	Read: Error status. 1 = error detected. 0 = no error. Write: Write 1 to clear errors. Writing 0 has no effect.
11 TST_OUT	Read only: Test point inside ring oscillator.
10 ENT_VAL	Read only: Entropy Valid. Will assert only if TRNG ACC bit is set, and then after an entropy value is generated. Will be cleared at most one (1) bus clock cycle after reading the TRNG0_ENT15 register. (TRNG0_ENT0 through TRNG0_ENT14 should be read before reading TRNG0_ENT15).
9 FCT_VAL	Read only: Frequency Count Valid. Indicates that a valid frequency count may be read from TRNG0_FRQCNT.
8 FCT_FAIL	Read only: Frequency Count Fail. The frequency counter has detected a failure. This may be due to improper programming of the TRNG0_FRQMAX and/or TRNG0_FRQMIN registers, or a hardware failure in the ring oscillator. This error may be cleared by writing a 1 to the ERR bit.

Table continues on the next page...

Field	Function
7 FOR_SCLK	Force System Clock. If set, the system clock is used to operate the TRNG, instead of the ring oscillator. This is for test use only, and indeterminate results may occur. This bit is writable only if PRGM bit is 1, or PRGM bit is being written to 1 simultaneously to writing this bit. This bit is cleared by writing the RST_DEF bit to 1.
6 RST_DEF	Reset Defaults. Writing a 1 to this bit clears various TRNG registers, and bits within registers, to their default state. This bit is writable only if PRGM bit is 1, or PRGM bit is being written to 1 simultaneously to writing this bit. Reading this bit always produces a 0.
5 TRNG_ACC	TRNG Access Mode. If this bit is set to 1, the TRNG will generate an Entropy value that can be read via the TRNG0_ENT0-TRNG0_ENT15 registers. The Entropy value may be read once the ENT VAL bit is asserted. Also see TRNG0_ENTa register descriptions (For a = 0 to 15).
4 UNUSED	This bit is unused but write-able. Must be left as zero.
3-2 OSC_DIV	Oscillator Divide. Determines the amount of dividing done to the ring oscillator before it is used by the TRNG. This field is writable only if PRGM bit is 1, or PRGM bit is being written to 1 simultaneously to writing this field. This field is cleared to the default POR value by writing the RST_DEF bit to 1. 00 - use ring oscillator with no divide 01 - use ring oscillator divided-by-2 10 - use ring oscillator divided-by-4 11 - use ring oscillator divided-by-8
1-0 SAMP_MODE	Sample Mode. Determines the method of sampling the ring oscillator while generating the Entropy value: This field is writable only if PRGM bit is 1, or PRGM bit is being written to 1 simultaneously with writing this field. This field is cleared to the POR default value by writing the RST_DEF bit to 1. 00 - use Von Neumann data into both Entropy shifter and Statistical Checker 01 - use raw data into both Entropy shifter and Statistical Checker 10 - use Von Neumann data into Entropy shifter. Use raw data into Statistical Checker 11 - undefined/reserved.

41.1.3.3.3 TRNG0 Statistical Check Miscellaneous (TRNG0_SCMISC)

41.1.3.3.3.1 Address

Register	Offset
TRNG0_SCMISC	4h

41.1.3.3.3.2 Function

The TRNG0 Statistical Check Miscellaneous Register contains the Long Run Maximum Limit value and the Retry Count value. This register is accessible only when the TRNG0_MCTL[PRGM] bit is 1, otherwise this register will read zeroes, and cannot be written.

41.1.3.3.3.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved												RTY_CT			
Reset	0[1]	0	0	0	0	0	0	0	0	0	0	0	0[1]	0	0	1

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved								LRUN_MAX							
Reset	0[1]	0	0	0	0	0	0	0	0[1]	0	0	1	1	1	1	1

1. Reset occurs at POR, and when TRNG0_MCTL[RST_DEF] is written to 1.

41.1.3.3.3.4 Fields

Field	Function
31-20 —	Reserved.
19-16 RTY_CT	RETRY COUNT. If a statistical check fails during the TRNG Entropy Generation, the RTY_CT value indicates the number of times a retry should occur before generating an error. This field is writable only if TRNG0_MCTL[PRGM] bit is 1. This field will read zeroes if TRNG0_MCTL[PRGM] = 0. This field is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.
15-8 —	Reserved.
7-0 LRUN_MAX	LONG RUN MAX LIMIT. This value is the largest allowable number of consecutive samples of all 1, or all 0, that is allowed during the Entropy generation. This field is writable only if TRNG0_MCTL[PRGM] bit is 1. This field will read zeroes if TRNG0_MCTL[PRGM] = 0. This field is cleared to the POR reset value by writing the TRNG0_MCTL[RST_DEF] bit to 1.

41.1.3.3.4 TRNG0 Poker Range (TRNG0_PKRRNG)

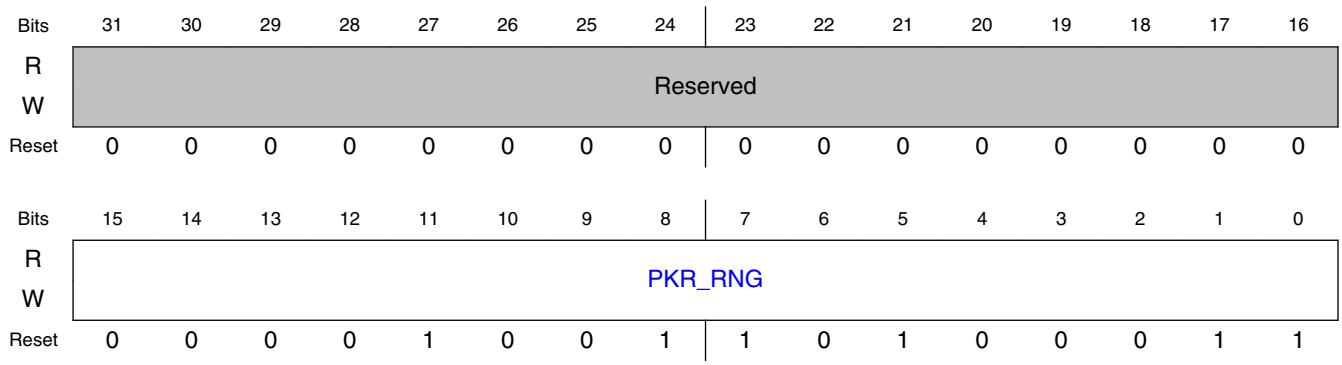
41.1.3.3.4.1 Address

Register	Offset
TRNG0_PKRRNG	8h

41.1.3.3.4.2 Function

The TRNG0 Poker Range Register defines the difference between the TRNG Poker Maximum Limit and the minimum limit. These limits are used during the TRNG Statistical Check Poker Test.

41.1.3.3.4.3 Diagram



41.1.3.3.4.4 Fields

Field	Function
31-16 —	Reserved. Always 0.
15-0 PKR_RNG	Poker Range. During the TRNG Statistical Checks, a "Poker Test" is run which requires a maximum and minimum limit. The maximum is programmed in the PKRMAX[PKR_MAX] register, and the minimum is derived by subtracting the PKR_RNG value from the programmed maximum value. This field is writable only if TRNG0_MCTL[PRGM] bit is 1. This field will read zeroes if TRNG0_MCTL[PRGM] = 0. This field is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1. Note that the minimum allowable Poker result is PKR_MAX - PKR_RNG + 1.

41.1.3.3.5 TRNG0 Poker Maximum Limit (TRNG0_PKRMAX)

41.1.3.3.5.1 Address

Register	Offset	Description
TRNG0_PKRMAX	Ch	Accessible at this address when TRNG0_MCTL[PRGM] = 1]

41.1.3.3.5.2 Function

The TRNG0 Poker Maximum Limit Register defines Maximum Limit allowable during the TRNG Statistical Check Poker Test. Note that this offset (0x0C) is used as TRNG0_PKRMAX only if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as the TRNG0_PKRSQ readback register.

41.1.3.3.5.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved								PKR_MAX							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKR_MAX															
Reset	0	1	1	0	1	0	0	1	0	0	1	0	0	0	0	0

41.1.3.3.5.4 Fields

Field	Function
31-24 —	Reserved. Always 0.
23-0 PKR_MAX	Poker Maximum Limit. During the TRNG Statistical Checks, a "Poker Test" is run which requires a maximum and minimum limit. The maximum allowable result is programmed in the TRNG0_PKRMAX[PKR_MAX] register. This field is writable only if TRNG0_MCTL[PRGM] bit is 1. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1. Note that the TRNG0_PKRMAX and TRNG0_PKRRNG registers combined are used to define the minimum allowable Poker result, which is PKR_MAX - PKR_RNG + 1. Note that if TRNG0_MCTL[PRGM] bit is 0, this register address is used to read the Poker Test Square Calculation result in register TRNG0_PKRSQ, as defined in the following section.

41.1.3.3.6 TRNG0 Poker Square Calculation Result (TRNG0_PKRSQ)

41.1.3.3.6.1 Address

Register	Offset	Description
TRNG0_PKRSQ	Ch	Accessible at this address when TRNG0_MCTL[PRGM] = 0]

41.1.3.3.6.2 Function

The TRNG0 Poker Square Calculation Result Register is a read-only register used to read the result of the TRNG Statistical Check Poker Test's Square Calculation. This test starts with the TRNG0_PKRMAX value and decreases towards a final result, which is read here. For the Poker Test to pass, this final result must be less than the programmed TRNG0_PKRRNG value. Note that this offset (0x0C) is used as TRNG0_PKRMAX if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as TRNG0_PKRSQ readback register, as described here.

41.1.3.3.6.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved								PKR_SQ							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PKR_SQ															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

41.1.3.3.6.4 Fields

Field	Function
31-24 —	Reserved. Always 0.
23-0 PKR_SQ	Poker Square Calculation Result. During the TRNG Statistical Checks, a "Poker Test" is run which starts with the value TRNG0_PKRMAX[PKR_MAX]. This value decreases according to a "sum of squares" algorithm, and must remain greater than zero, but less than the TRNG0_PKRRNG[PKR_RNG] limit. The resulting value may be read through this register, if TRNG0_MCTL[PRGM] bit is 0. Note that if TRNG0_MCTL[PRGM] bit is 1, this register address is used to access the Poker Test Maximum Limit in register TRNG0_PKRMAX, as defined in the previous section.

41.1.3.3.7 TRNG0 Seed Control (TRNG0_SDCTL)

41.1.3.3.7.1 Address

Register	Offset
TRNG0_SDCTL	10h

41.1.3.3.7.2 Function

The TRNG0 Seed Control Register contains two fields. One field defines the length (in system clocks) of each Entropy sample (ENT_DLY), and the other field indicates the number of samples that will taken during each TRNG Entropy generation (SAMP_SIZE).

41.1.3.3.7.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	ENT_DLY															
Reset	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	SAMP_SIZE															
Reset	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0

41.1.3.3.7.4 Fields

Field	Function
31-16 ENT_DLY	Entropy Delay. Defines the length (in system clocks) of each Entropy sample taken. This field is writable only if TRNG0_MCTL[PRGM] bit is 1. This field will read zeroes if TRNG0_MCTL[PRGM] = 0. This field is cleared to its reset value at POR.
15-0 SAMP_SIZE	Sample Size. Defines the total number of Entropy samples that will be taken during Entropy generation. This field is writable only if TRNG0_MCTL[PRGM] bit is 1. This field will read zeroes if TRNG0_MCTL[PRGM] = 0. This field is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.

41.1.3.3.8 TRNG0 Sparse Bit Limit (TRNG0_SBLIM)

41.1.3.3.8.1 Address

Register	Offset	Description
TRNG0_SBLIM	14h	Accessible at this address when TRNG0_MCTL[PRGM] = 1]

41.1.3.3.8.2 Function

The TRNG0 Sparse Bit Limit Register is used when Von Neumann sampling is selected during Entropy Generation. It defines the maximum number of consecutive Von Neumann samples which may be discarded before an error is generated. Note that this address (0x14) is used as TRNG0_SBLIM only if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this address is used as TRNG0_TOTSAM readback register.

41.1.3.3.8.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved						SB_LIM									
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

41.1.3.3.8.4 Fields

Field	Function
31-10 —	Reserved. Always 0.
9-0 SB_LIM	Sparse Bit Limit. During Von Neumann sampling (if enabled by TRNG0_MCTL[SAMP_MODE], samples are discarded if two consecutive raw samples are both 0 or both 1. If this discarding occurs for a long period of time, it indicates that there is insufficient Entropy. The Sparse Bit Limit defines the maximum number of consecutive samples that may be discarded before an error is generated. This field is writable only if TRNG0_MCTL[PRGM] bit is 1. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1. Note that if TRNG0_MCTL[PRGM] bit is 0, this register address is used to read the Total Samples count in register TRNG0_TOTSAM, as defined in the following section.

41.1.3.3.9 TRNG0 Total Samples (TRNG0_TOTSAM)

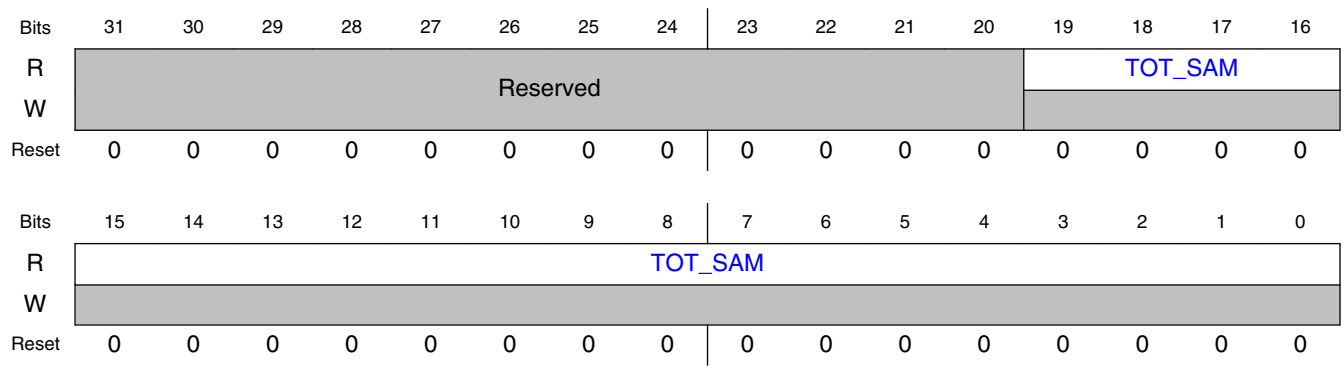
41.1.3.3.9.1 Address

Register	Offset	Description
TRNG0_TOTSAM	14h	Accessible at this address when TRNG0_MCTL[PRGM] = 0]

41.1.3.3.9.2 Function

The TRNG0 Total Samples Register is a read-only register used to read the total number of samples taken during Entropy generation. It is used to give an indication of how often a sample is actually used during Von Neumann sampling. Note that this offset (0x14) is used as TRNG0_SBLIM if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as TRNG0_TOTSAM readback register, as described here.

41.1.3.3.9.3 Diagram



41.1.3.3.9.4 Fields

Field	Function
31-20 —	Reserved. Always 0.
19-0 TOT_SAM	Total Samples. During Entropy generation, the total number of raw samples is counted. This count is useful in determining how often a sample is used during Von Neumann sampling. The count may be read through this register, if TRNG0_MCTL[PRGM] bit is 0. Note that if TRNG0_MCTL[PRGM] bit is 1, this register address is used to access the Sparse Bit Limit in register TRNG0_SBLIM, as defined in the previous section.

41.1.3.3.10 TRNG0 Frequency Count Minimum Limit (TRNG0_FRQMIN)

41.1.3.3.10.1 Address

Register	Offset
TRNG0_FRQMIN	18h

41.1.3.3.10.2 Function

The TRNG0 Frequency Count Minimum Limit Register defines the minimum allowable count taken by the Entropy sample counter during each Entropy sample. During any sample period, if the count is less than this programmed minimum, a Frequency Count Fail is flagged in TRNG0_MCTL[FCT_FAIL] and an error is generated.

41.1.3.3.10.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved										FRQ_MIN					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	FRQ_MIN															
Reset	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0

41.1.3.3.10.4 Fields

Field	Function
31-22 —	Reserved. Always 0.
21-0 FRQ_MIN	Frequency Count Minimum Limit. Defines the minimum allowable count taken during each entropy sample. This field is writable only if TRNG0_MCTL[PRGM] bit is 1. This field will read zeroes if TRNG0_MCTL[PRGM] = 0. This field is cleared to its reset value at POR.

41.1.3.3.11 TRNG0 Frequency Count (TRNG0_FRQCNT)

41.1.3.3.11.1 Address

Register	Offset	Description
TRNG0_FRQCNT	1Ch	Accessible at this address when TRNG0_MCTL[PRGM] = 0]

41.1.3.3.11.2 Function

The TRNG0 Frequency Count Register is a read-only register used to read the frequency counter within the TRNG entropy generator. It will read all zeroes unless TRNG0_MCTL[TRNG_ACC] = 1. Note that this offset (0x1C) is used as TRNG0_FRQMAX if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as TRNG0_FRQCNT readback register, as described here.

41.1.3.3.11.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved										FRQ_CT					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	FRQ_CT															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

41.1.3.3.11.4 Fields

Field	Function
31-22 —	Reserved. Always 0.
21-0 FRQ_CT	Frequency Count. If TRNG0_MCTL[TRNG_ACC] = 1, reads a sample frequency count taken during entropy generation. Requires TRNG0_MCTL[PRGM] = 0. Note that if TRNG0_MCTL[PRGM] bit is 1, this register address is used to access the Poker Test Maximum Limit in register TRNG0_PKRMAX, as defined in the previous section.

41.1.3.3.12 TRNG0 Frequency Count Maximum Limit (TRNG0_FRQMAX)

41.1.3.3.12.1 Address

Register	Offset	Description
TRNG0_FRQMAX	1Ch	Accessible at this address when TRNG0_MCTL[PRGM] = 1]

41.1.3.3.12.2 Function

The TRNG0 Frequency Count Maximum Limit Register defines the maximum allowable count taken by the Entropy sample counter during each Entropy sample. During any sample period, if the count is greater than this programmed maximum, a Frequency Count Fail is flagged in TRNG0_MCTL[FCT_FAIL] and an error is generated. Note that this address (001C) is used as TRNG0_FRQMAX only if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this address is used as TRNG0_FRQCNT readback register.

41.1.3.3.12.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved										FRQ_MAX					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	FRQ_MAX															
Reset	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0

41.1.3.3.12.4 Fields

Field	Function
31-22 —	Reserved. Always 0.
21-0 FRQ_MAX	Frequency Counter Maximum Limit. Defines the maximum allowable count taken during each entropy sample. This field is writable only if TRNG0_MCTL[PRGM] bit is 1. This field is cleared to its reset value at POR. Note that if TRNG0_MCTL[PRGM] bit is 0, this register address is used to read the Frequency Count result in register TRNG0_FRQCNT, as defined in the following section.

41.1.3.3.13 TRNG0 Statistical Check Monobit Count (TRNG0_SCMC)

41.1.3.3.13.1 Address

Register	Offset	Description
TRNG0_SCMC	20h	Accessible at this address when TRNG0_MCTL[PRGM] = 0]

41.1.3.3.13.2 Function

The TRNG0 Statistical Check Monobit Count Register is a read-only register used to read the final monobit count after entropy generation. This counter starts with the value in TRNG0_SCML[MONO_MAX], and is decremented each time a one is sampled. Note that this offset (0x20) is used as TRNG0_SCML if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as TRNG0_SCMC readback register, as described here.

41.1.3.3.13.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MONO_CT															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

41.1.3.3.13.4 Fields

Field	Function
31-16 —	Reserved. Always 0.
15-0 MONO_CT	Monobit Count. Reads the final Monobit count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0. Note that if TRNG0_MCTL[PRGM] bit is 1, this register address is used to access the Statistical Check Monobit Limit in register TRNG0_SCML, as defined in the previous section.

41.1.3.3.14 TRNG0 Statistical Check Monobit Limit (TRNG0_SCML)

41.1.3.3.14.1 Address

Register	Offset	Description
TRNG0_SCML	20h	Accessible at this address when TRNG0_MCTL[PRGM] = 1]

41.1.3.3.14.2 Function

The TRNG0 Statistical Check Monobit Limit Register defines the allowable maximum and minimum number of ones/zero detected during entropy generation. To pass the test, the number of ones/zeroes generated must be less than the programmed maximum value, and the number of ones/zeroes generated must be greater than (maximum - range). If this test fails, the Retry Counter in TRNG0_SCMISC will be decremented, and a retry will occur if the Retry Count has not reached zero. If the Retry Count has reached zero, an error will be generated. Note that this offset (0x20) is used as TRNG0_SCML only if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as TRNG0_SCMC readback register.

41.1.3.3.14.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	MONO_RNG															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	MONO_MAX															
Reset	0	0	0	0	0	1	0	1	0	1	1	0	1	0	0	0

41.1.3.3.14.4 Fields

Field	Function
31-16 MONO_RNG	Monobit Range. The number of ones/zeroes detected during entropy generation must be greater than MONO_MAX - MONO_RNG, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.
15-0 MONO_MAX	Monobit Maximum Limit. Defines the maximum allowable count taken during entropy generation. The number of ones/zeroes detected during entropy generation must be less than MONO_MAX, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.

41.1.3.3.15 TRNG0 Statistical Check Run Length 1 Count (TRNG0_SCR1C)

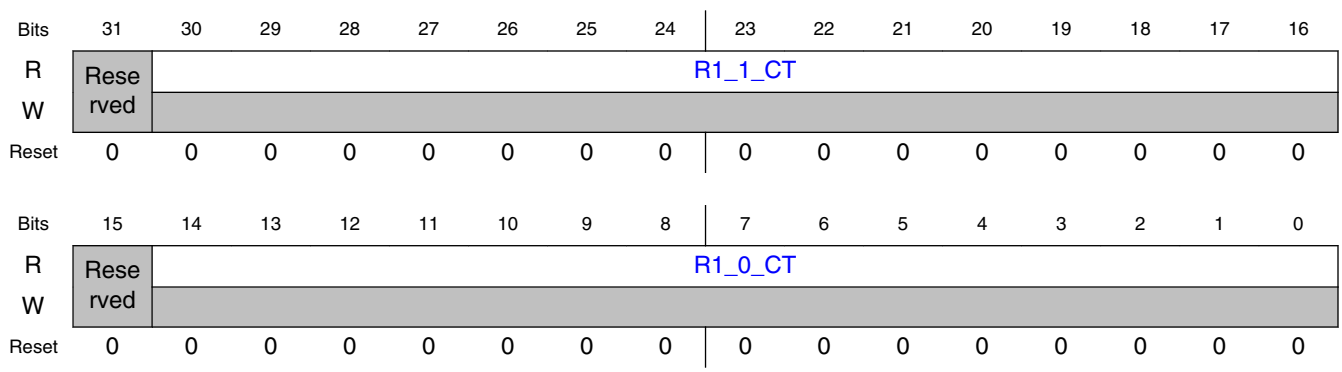
41.1.3.3.15.1 Address

Register	Offset	Description
TRNG0_SCR1C	24h	Accessible at this address when TRNG0_MCTL[PRGM] = 0]

41.1.3.3.15.2 Function

The TRNG0 Statistical Check Run Length 1 Counters Register is a read-only register used to read the final Run Length 1 counts after entropy generation. These counters start with the value in TRNG0_SCRxC1L[RUN1_MAX]. The R1_1_CT decrements each time a single one is sampled (preceded by a zero and followed by a zero). The R1_0_CT decrements each time a single zero is sampled (preceded by a one and followed by a one). Note that this offset (0x24) is used as TRNG0_SCRxC1L if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as TRNG0_SCRxC1C readback register, as described here.

41.1.3.3.15.3 Diagram



41.1.3.3.15.4 Fields

Field	Function
31 —	Reserved. Always 0.
30-16 R1_1_CT	Runs of One, Length 1 Count. Reads the final Runs of Ones, length 1 count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0.
15 —	Reserved. Always 0.
14-0 R1_0_CT	Runs of Zero, Length 1 Count. Reads the final Runs of Zeroes, length 1 count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.16 TRNG0 Statistical Check Run Length 1 Limit (TRNG0_SCR1L)

41.1.3.3.16.1 Address

Register	Offset	Description
TRNG0_SCR1L	24h	Accessible at this address when TRNG0_MCTL[PRGM] = 1]

41.1.3.3.16.2 Function

The TRNG0 Statistical Check Run Length 1 Limit Register defines the allowable maximum and minimum number of runs of length 1 detected during entropy generation. To pass the test, the number of runs of length 1 (for samples of both 0 and 1) must be less than the programmed maximum value, and the number of runs of length 1 must be greater than (maximum - range). If this test fails, the Retry Counter in TRNG0_SCMISC will be decremented, and a retry will occur if the Retry Count has not reached zero. If the Retry Count has reached zero, an error will be generated. Note that this address (0x24) is used as TRNG0_SCRxC1L only if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this address is used as TRNG0_SCRxC1C readback register.

41.1.3.3.16.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved	RUN1_RNG														
W																
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved	RUN1_MAX														
W																
Reset	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1

41.1.3.3.16.4 Fields

Field	Function
31	Reserved. Always 0.

Table continues on the next page...

Field	Function
—	
30-16 RUN1_RNG	Run Length 1 Range. The number of runs of length 1 (for both 0 and 1) detected during entropy generation must be greater than RUN1_MAX - RUN1_RNG, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.
15 —	Reserved. Always 0.
14-0 RUN1_MAX	Run Length 1 Maximum Limit. Defines the maximum allowable runs of length 1 (for both 0 and 1) detected during entropy generation. The number of runs of length 1 detected during entropy generation must be less than RUN1_MAX, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.

41.1.3.3.17 TRNG0 Statistical Check Run Length 2 Count (TRNG0_SCR2C)

41.1.3.3.17.1 Address

Register	Offset	Description
TRNG0_SCR2C	28h	Accessible at this address when TRNG0_MCTL[PRGM] = 0]

41.1.3.3.17.2 Function

The TRNG0 Statistical Check Run Length 2 Counters Register is a read-only register used to read the final Run Length 2 counts after entropy generation. These counters start with the value in TRNG0_SCRxC2L[RUN2_MAX]. The R2_1_CT decrements each time two consecutive ones are sampled (preceded by a zero and followed by a zero). The R2_0_CT decrements each time two consecutive zeroes are sampled (preceded by a one and followed by a one). Note that this offset (0x28) is used as TRNG0_SCRxC2L if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as TRNG0_SCRxC2C readback register, as described here.

41.1.3.3.17.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved		R2_1_CT													
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved		R2_0_CT													
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

41.1.3.3.17.4 Fields

Field	Function
31-30 —	Reserved. Always 0.
29-16 R2_1_CT	Runs of One, Length 2 Count. Reads the final Runs of Ones, length 2 count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0.
15-14 —	Reserved. Always 0.
13-0 R2_0_CT	Runs of Zero, Length 2 Count. Reads the final Runs of Zeroes, length 2 count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.18 TRNG0 Statistical Check Run Length 2 Limit (TRNG0_SCR2L)

41.1.3.3.18.1 Address

Register	Offset	Description
TRNG0_SCR2L	28h	Accessible at this address when TRNG0_MCTL[PRGM] = 1]

41.1.3.3.18.2 Function

The TRNG0 Statistical Check Run Length 2 Limit Register defines the allowable maximum and minimum number of runs of length 2 detected during entropy generation. To pass the test, the number of runs of length 2 (for samples of both 0 and 1) must be less than the programmed maximum value, and the number of runs of length 2 must be greater than (maximum - range). If this test fails, the Retry Counter in TRNG0_SCMISC

will be decremented, and a retry will occur if the Retry Count has not reached zero. If the Retry Count has reached zero, an error will be generated. Note that this address (0x28) is used as TRNG0_SCRxC2L only if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this address is used as TRNG0_SCRxC2C readback register.

41.1.3.3.18.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved								RUN2_RNG							
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved								RUN2_MAX							
Reset	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0

41.1.3.3.18.4 Fields

Field	Function
31-30 —	Reserved. Always 0.
29-16 RUN2_RNG	Run Length 2 Range. The number of runs of length 2 (for both 0 and 1) detected during entropy generation must be greater than RUN2_MAX - RUN2_RNG, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.
15-14 —	Reserved. Always 0.
13-0 RUN2_MAX	Run Length 2 Maximum Limit. Defines the maximum allowable runs of length 2 (for both 0 and 1) detected during entropy generation. The number of runs of length 2 detected during entropy generation must be less than RUN2_MAX, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.

41.1.3.3.19 TRNG0 Statistical Check Run Length 3 Count (TRNG0_SCR3C)

41.1.3.3.19.1 Address

Register	Offset	Description
TRNG0_SCR3C	2Ch	Accessible at this address when TRNG0_MCTL[PRGM] = 0]

41.1.3.3.19.2 Function

The TRNG0 Statistical Check Run Length 3 Counters Register is a read-only register used to read the final Run Length 3 counts after entropy generation. These counters start with the value in TRNG0_SCRxC3L[RUN3_MAX]. The R3_1_CT decrements each time three consecutive ones are sampled (preceded by a zero and followed by a zero). The R3_0_CT decrements each time three consecutive zeroes are sampled (preceded by a one and followed by a one). Note that this offset (0x2C) is used as TRNG0_SCRxC3L if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as TRNG0_SCRxC3C readback register, as described here.

41.1.3.3.19.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved			R3_1_CT												
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved			R3_0_CT												
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

41.1.3.3.19.4 Fields

Field	Function
31-29 —	Reserved. Always 0.
28-16 R3_1_CT	Runs of Ones, Length 3 Count. Reads the final Runs of Ones, length 3 count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0.
15-13 —	Reserved. Always 0.
12-0 R3_0_CT	Runs of Zeroes, Length 3 Count. Reads the final Runs of Zeroes, length 3 count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.20 TRNG0 Statistical Check Run Length 3 Limit (TRNG0_SCR3L)

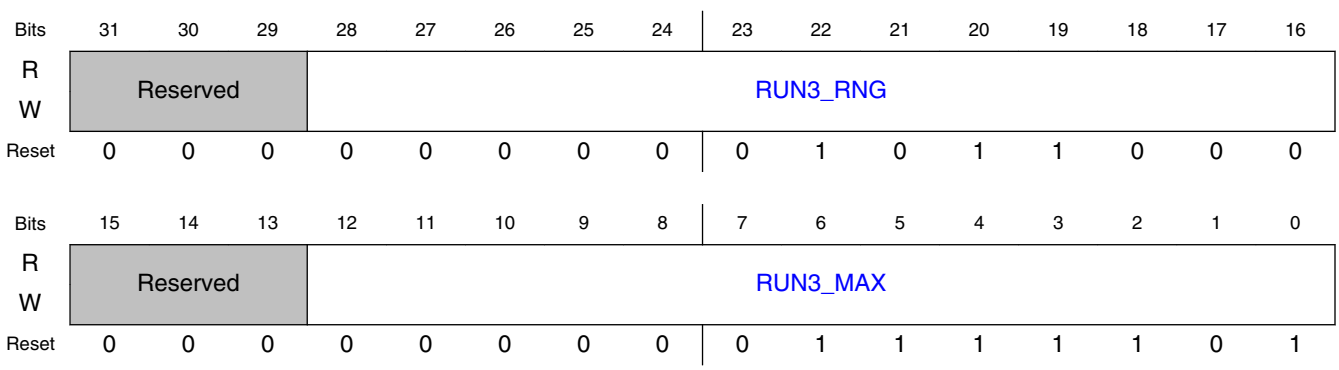
41.1.3.3.20.1 Address

Register	Offset	Description
TRNG0_SCR3L	2Ch	Accessible at this address when TRNG0_MCTL[PRGM] = 1]

41.1.3.3.20.2 Function

The TRNG0 Statistical Check Run Length 3 Limit Register defines the allowable maximum and minimum number of runs of length 3 detected during entropy generation. To pass the test, the number of runs of length 3 (for samples of both 0 and 1) must be less than the programmed maximum value, and the number of runs of length 3 must be greater than (maximum - range). If this test fails, the Retry Counter in TRNG0_SCMISC will be decremented, and a retry will occur if the Retry Count has not reached zero. If the Retry Count has reached zero, an error will be generated. Note that this address (0x2C) is used as TRNG0_SCRxC3L only if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this address is used as TRNG0_SCRxC3C readback register.

41.1.3.3.20.3 Diagram



41.1.3.3.20.4 Fields

Field	Function
31-29 —	Reserved. Always 0.
28-16 RUN3_RNG	Run Length 3 Range. The number of runs of length 3 (for both 0 and 1) detected during entropy generation must be greater than RUN3_MAX - RUN3_RNG, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.
15-13	Reserved. Always 0.

Table continues on the next page...

Field	Function
—	
12-0 RUN3_MAX	Run Length 3 Maximum Limit. Defines the maximum allowable runs of length 3 (for both 0 and 1) detected during entropy generation. The number of runs of length 3 detected during entropy generation must be less than RUN3_MAX, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.

41.1.3.3.21 TRNG0 Statistical Check Run Length 4 Count (TRNG0_SCR4C)

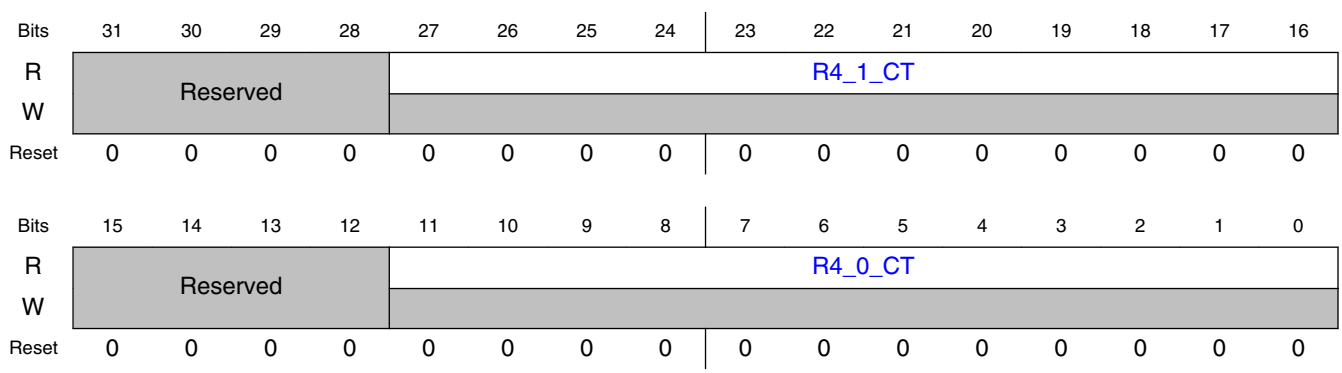
41.1.3.3.21.1 Address

Register	Offset	Description
TRNG0_SCR4C	30h	Accessible at this address when TRNG0_MCTL[PRGM] = 0]

41.1.3.3.21.2 Function

The TRNG0 Statistical Check Run Length 4 Counters Register is a read-only register used to read the final Run Length 4 counts after entropy generation. These counters start with the value in TRNG0_SCRxC4L[RUN4_MAX]. The R4_1_CT decrements each time four consecutive ones are sampled (preceded by a zero and followed by a zero). The R4_0_CT decrements each time four consecutive zeroes are sampled (preceded by a one and followed by a one). Note that this offset (0x30) is used as TRNG0_SCRxC4L if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as TRNG0_SCRxC4C readback register, as described here.

41.1.3.3.21.3 Diagram



41.1.3.3.21.4 Fields

Field	Function
31-28 —	Reserved. Always 0.
27-16 R4_1_CT	Runs of One, Length 4 Count. Reads the final Runs of Ones, length 4 count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0.
15-12 —	Reserved. Always 0.
11-0 R4_0_CT	Runs of Zero, Length 4 Count. Reads the final Runs of Ones, length 4 count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.22 TRNG0 Statistical Check Run Length 4 Limit (TRNG0_SCR4L)

41.1.3.3.22.1 Address

Register	Offset	Description
TRNG0_SCR4L	30h	Accessible at this address when TRNG0_MCTL[PRGM] = 1]

41.1.3.3.22.2 Function

The TRNG0 Statistical Check Run Length 4 Limit Register defines the allowable maximum and minimum number of runs of length 4 detected during entropy generation. To pass the test, the number of runs of length 4 (for samples of both 0 and 1) must be less than the programmed maximum value, and the number of runs of length 4 must be greater than (maximum - range). If this test fails, the Retry Counter in TRNG0_SCMISC will be decremented, and a retry will occur if the Retry Count has not reached zero. If the Retry Count has reached zero, an error will be generated. Note that this address (0x30) is used as TRNG0_SCRxC4L only if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this address is used as TRNG0_SCRxC4C readback register.

41.1.3.3.22.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved				RUN4_RNG											
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved				RUN4_MAX											
Reset	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1

41.1.3.3.22.4 Fields

Field	Function
31-28 —	Reserved. Always 0.
27-16 RUN4_RNG	Run Length 4 Range. The number of runs of length 4 (for both 0 and 1) detected during entropy generation must be greater than RUN4_MAX - RUN4_RNG, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.
15-12 —	Reserved. Always 0.
11-0 RUN4_MAX	Run Length 4 Maximum Limit. Defines the maximum allowable runs of length 4 (for both 0 and 1) detected during entropy generation. The number of runs of length 4 detected during entropy generation must be less than RUN4_MAX, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.

41.1.3.3.23 TRNG0 Statistical Check Run Length 5 Count (TRNG0_SCR5C)

41.1.3.3.23.1 Address

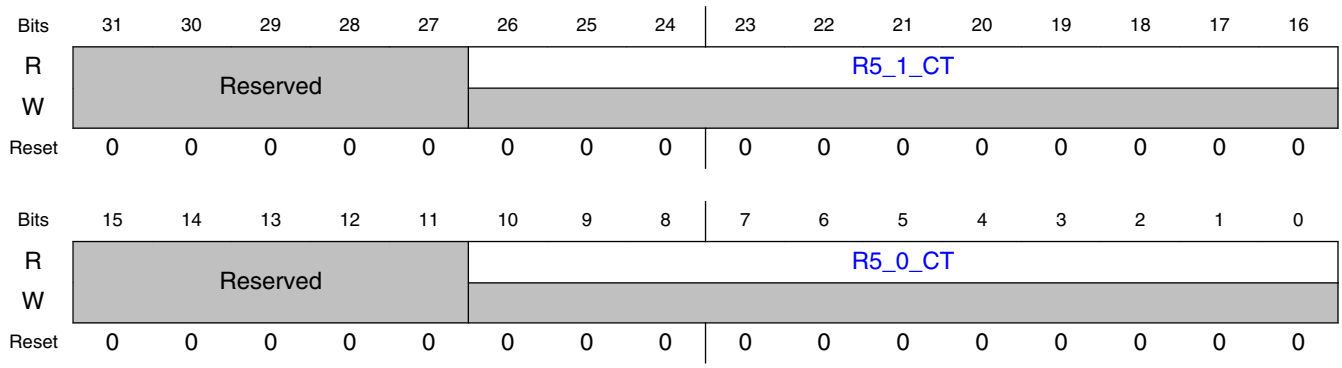
Register	Offset	Description
TRNG0_SCR5C	34h	Accessible at this address when TRNG0_MCTL[PRGM] = 0]

41.1.3.3.23.2 Function

The TRNG0 Statistical Check Run Length 5 Counters Register is a read-only register used to read the final Run Length 5 counts after entropy generation. These counters start with the value in TRNG0_SCRxC5L[RUN5_MAX]. The R5_1_CT decrements each time five consecutive ones are sampled (preceded by a zero and followed by a zero). The

R5_0_CT decrements each time five consecutive zeroes are sampled (preceded by a one and followed by a one). Note that this offset (0x34) is used as TRNG0_SCRxC5L if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as TRNG0_SCRxC5C readback register, as described here.

41.1.3.3.23.3 Diagram



41.1.3.3.23.4 Fields

Field	Function
31-27 —	Reserved. Always 0.
26-16 R5_1_CT	Runs of One, Length 5 Count. Reads the final Runs of Ones, length 5 count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0.
15-11 —	Reserved. Always 0.
10-0 R5_0_CT	Runs of Zero, Length 5 Count. Reads the final Runs of Ones, length 5 count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.24 TRNG0 Statistical Check Run Length 5 Limit (TRNG0_SCR5L)

41.1.3.3.24.1 Address

Register	Offset	Description
TRNG0_SCR5L	34h	Accessible at this address when TRNG0_MCTL[PRGM] = 1]

41.1.3.3.24.2 Function

The TRNG0 Statistical Check Run Length 5 Limit Register defines the allowable maximum and minimum number of runs of length 5 detected during entropy generation. To pass the test, the number of runs of length 5 (for samples of both 0 and 1) must be less than the programmed maximum value, and the number of runs of length 5 must be greater than (maximum - range). If this test fails, the Retry Counter in TRNG0_SCMISC will be decremented, and a retry will occur if the Retry Count has not reached zero. If the Retry Count has reached zero, an error will be generated. Note that this address (0x34) is used as TRNG0_SCRxC5L only if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this address is used as TRNG0_SCRxC5C readback register.

41.1.3.3.24.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved					RUN5_RNG										
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved					RUN5_MAX										
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1

41.1.3.3.24.4 Fields

Field	Function
31-27 —	Reserved. Always 0.
26-16 RUN5_RNG	Run Length 5 Range. The number of runs of length 5 (for both 0 and 1) detected during entropy generation must be greater than RUN5_MAX - RUN5_RNG, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.
15-11 —	Reserved. Always 0.
10-0 RUN5_MAX	Run Length 5 Maximum Limit. Defines the maximum allowable runs of length 5 (for both 0 and 1) detected during entropy generation. The number of runs of length 5 detected during entropy generation must be less than RUN5_MAX, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.

41.1.3.3.25 TRNG0 Statistical Check Run Length 6+ Count (TRNG0_SCR6PC)

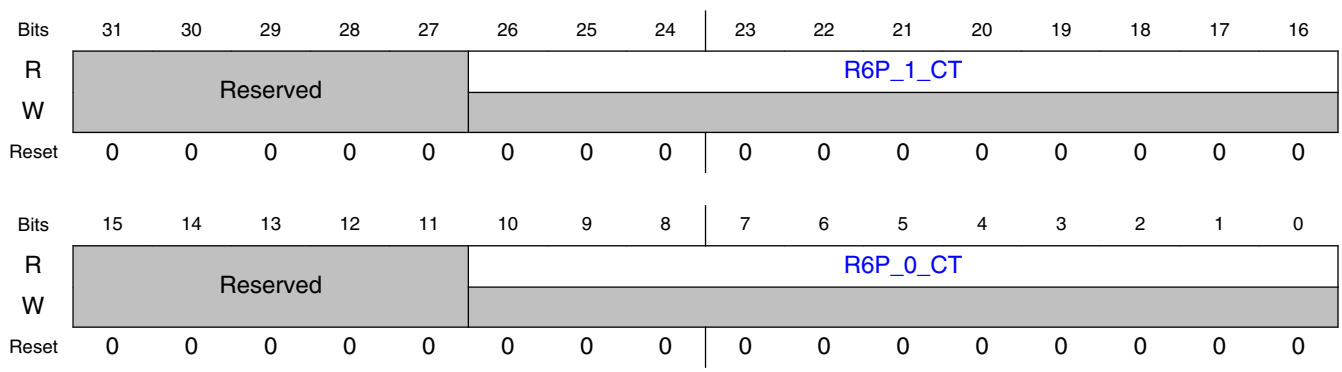
41.1.3.3.25.1 Address

Register	Offset	Description
TRNG0_SCR6PC	38h	Accessible at this address when TRNG0_MCTL[PRGM] = 0]

41.1.3.3.25.2 Function

The TRNG0 Statistical Check Run Length 6+ Counters Register is a read-only register used to read the final Run Length 6+ counts after entropy generation. These counters start with the value in TRNG0_SCRxC6PL[RUN6P_MAX]. The R6P_1_CT decrements each time six or more consecutive ones are sampled (preceded by a zero and followed by a zero). The R6P_0_CT decrements each time six or more consecutive zeroes are sampled (preceded by a one and followed by a one). Note that this offset (0x38) is used as TRNG0_SCRxC6PL if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as TRNG0_SCRxC6PC readback register, as described here.

41.1.3.3.25.3 Diagram



41.1.3.3.25.4 Fields

Field	Function
31-27 —	Reserved. Always 0.
26-16 R6P_1_CT	Runs of One, Length 6+ Count. Reads the final Runs of Ones, length 6+ count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0.

Table continues on the next page...

Field	Function
15-11 —	Reserved. Always 0.
10-0 R6P_0_CT	Runs of Zero, Length 6+ Count. Reads the final Runs of Ones, length 6+ count after entropy generation. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.26 TRNG0 Statistical Check Run Length 6+ Limit (TRNG0_SCR6PL)

41.1.3.3.26.1 Address

Register	Offset	Description
TRNG0_SCR6PL	38h	Accessible at this address when TRNG0_MCTL[PRGM] = 1]

41.1.3.3.26.2 Function

The TRNG0 Statistical Check Run Length 6+ Limit Register defines the allowable maximum and minimum number of runs of length 6 or more detected during entropy generation. To pass the test, the number of runs of length 6 or more (for samples of both 0 and 1) must be less than the programmed maximum value, and the number of runs of length 6 or more must be greater than (maximum - range). If this test fails, the Retry Counter in TRNG0_SCMISC will be decremented, and a retry will occur if the Retry Count has not reached zero. If the Retry Count has reached zero, an error will be generated. Note that this offset (0x38) is used as TRNG0_SCRxC6PL only if TRNG0_MCTL[PRGM] is 1. If TRNG0_MCTL[PRGM] is 0, this offset is used as TRNG0_SCRxC6PC readback register.

41.1.3.3.26.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved					RUN6P_RNG										
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved					RUN6P_MAX										
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1

41.1.3.3.26.4 Fields

Field	Function
31-27 —	Reserved. Always 0.
26-16 RUN6P_RNG	Run Length 6+ Range. The number of runs of length 6 or more (for both 0 and 1) detected during entropy generation must be greater than RUN6P_MAX - RUN6P_RNG, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.
15-11 —	Reserved. Always 0.
10-0 RUN6P_MAX	Run Length 6+ Maximum Limit. Defines the maximum allowable runs of length 6 or more (for both 0 and 1) detected during entropy generation. The number of runs of length 6 or more detected during entropy generation must be less than RUN6P_MAX, else a retry or error will occur. This register is cleared to the default POR value by writing the TRNG0_MCTL[RST_DEF] bit to 1.

41.1.3.3.27 TRNG0 Status (TRNG0_STATUS)

41.1.3.3.27.1 Address

Register	Offset
TRNG0_STATUS	3Ch

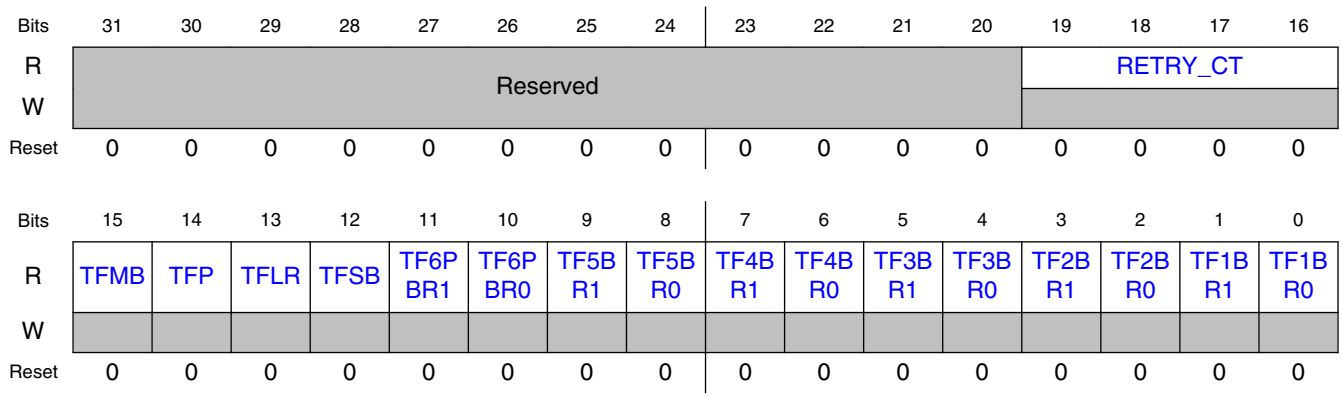
41.1.3.3.27.2 Function

Various statistical tests are run as a normal part of the TRNG's entropy generation process. The least-significant 16 bits of the TRNG0_STATUS register reflect the result of each of these tests. The status of these bits will be valid when the TRNG has finished its entropy generation process. Software can determine when this occurs by polling the ENT_VAL bit in the TRNG0 Miscellaneous Control Register.

Note that there is a very small probability that a statistical test will fail even though the TRNG is operating properly. If this happens the TRNG will automatically retry the entire entropy generation process, including running all the statistical tests. The value in RETRY_CT is decremented each time an entropy generation retry occurs. If a statistical check fails when the retry count is nonzero, a retry is initiated. But if a statistical check fails when the retry count is zero, an error is generated by the RNG. By default RETRY_CT is initialized to 1, but software can increase the retry count by writing to the RTY_CT field in the TRNG0_SCMISC register.

All 0s will be returned if this register address is read while the RNG is in Program Mode (see PRGM field in TRNG0_MCTL register. If this register is read while the RNG is in Run Mode the value returned will be formatted as follows.

41.1.3.3.27.3 Diagram



41.1.3.3.27.4 Fields

Field	Function
31-20 —	Reserved. Always 0.
19-16 RETRY_CT	RETRY COUNT. This represents the current number of entropy generation retries left before a statistical text failure will cause the RNG to generate an error condition.
15 TFMB	Test Fail, Mono Bit. If TFMB=1, the Mono Bit Test has failed.
14 TFP	Test Fail, Poker. If TFP=1, the Poker Test has failed.
13 TFLR	Test Fail, Long Run. If TFLR=1, the Long Run Test has failed.
12 TFSB	Test Fail, Sparse Bit. If TFSB=1, the Sparse Bit Test has failed.
11 TF6PBR1	Test Fail, 6 Plus Bit Run, Sampling 1s. If TF6PBR1=1, the 6 Plus Bit Run, Sampling 1s Test has failed.
10 TF6PBR0	Test Fail, 6 Plus Bit Run, Sampling 0s. If TF6PBR0=1, the 6 Plus Bit Run, Sampling 0s Test has failed.
9 TF5BR1	Test Fail, 5-Bit Run, Sampling 1s. If TF5BR1=1, the 5-Bit Run, Sampling 1s Test has failed.
8 TF5BR0	Test Fail, 5-Bit Run, Sampling 0s. If TF5BR0=1, the 5-Bit Run, Sampling 0s Test has failed.

Table continues on the next page...

Field	Function
7 TF4BR1	Test Fail, 4-Bit Run, Sampling 1s. If TF4BR1=1, the 4-Bit Run, Sampling 1s Test has failed.
6 TF4BR0	Test Fail, 4-Bit Run, Sampling 0s. If TF4BR0=1, the 4-Bit Run, Sampling 0s Test has failed.
5 TF3BR1	Test Fail, 3-Bit Run, Sampling 1s. If TF3BR1=1, the 3-Bit Run, Sampling 1s Test has failed.
4 TF3BR0	Test Fail, 3-Bit Run, Sampling 0s. If TF3BR0=1, the 3-Bit Run, Sampling 0s Test has failed.
3 TF2BR1	Test Fail, 2-Bit Run, Sampling 1s. If TF2BR1=1, the 2-Bit Run, Sampling 1s Test has failed.
2 TF2BR0	Test Fail, 2-Bit Run, Sampling 0s. If TF2BR0=1, the 2-Bit Run, Sampling 0s Test has failed.
1 TF1BR1	Test Fail, 1-Bit Run, Sampling 1s. If TF1BR1=1, the 1-Bit Run, Sampling 1s Test has failed.
0 TF1BR0	Test Fail, 1-Bit Run, Sampling 0s. If TF1BR0=1, the 1-Bit Run, Sampling 0s Test has failed.

41.1.3.3.28 TRNG0 Entropy Read (TRNG0_ENTa)

41.1.3.3.28.1 Address

For a = 0 to 15:

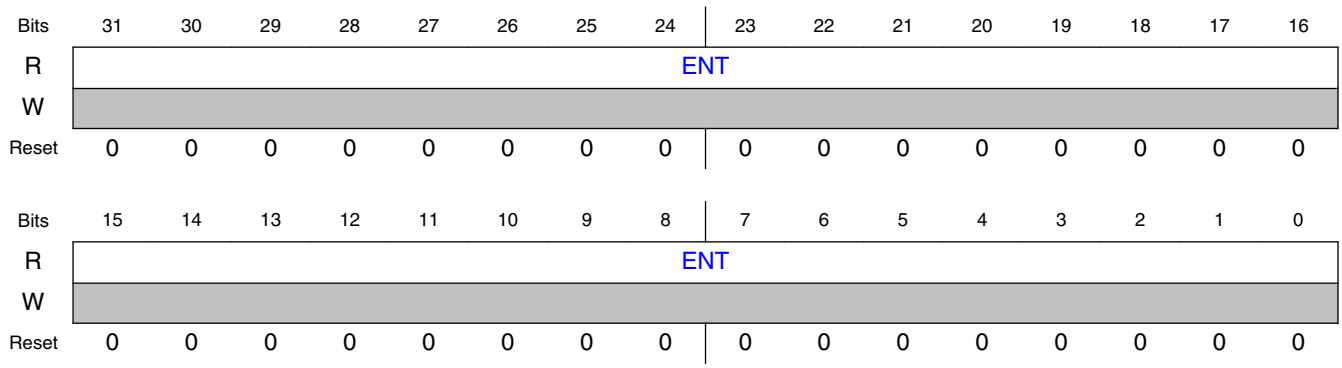
Register	Offset	Description
TRNG0_ENTa	40h + (a × 4h)	Word a

41.1.3.3.28.2 Function

The RNG TRNG can be programmed to generate an entropy value that is readable via the SkyBlue bus. To do this, set the TRNG0_MCTL[TRNG_ACC] bit to 1. Once the entropy value has been generated, the TRNG0_MCTL[ENT_VAL] bit will be set to 1. At this point, TRNG0_ENT0 through TRNG0_ENT15 may be read to retrieve the 512-bit entropy value. Note that once TRNG0_ENT15 is read, the entropy value will be cleared and a new value will begin generation, so it is important that TRNG0_ENT15 be read last. These registers are readable only when TRNG0_MCTL[PRGM] = 0 (Run Mode), TRNG0_MCTL[TRNG_ACC] = 1 (TRNG access mode) and

TRNG0_MCTL[ENT_VAL] = 1. After at most one (1) bus clock cycle of reading a valid TRNG0_ENT15 register value, reading any TRNG0_ENT0 through TRNG0_ENT15 register would return zeroes.

41.1.3.3.28.3 Diagram



41.1.3.3.28.4 Fields

Field	Function
31-0 ENT	Entropy Value. Will be non-zero only if TRNG0_MCTL[PRGM] = 0 Run Mode) and TRNG0_MCTL[ENT_VAL] = 1 (Entropy Valid). The most significant bits of the entropy are read from the lowest offset, and the least significant bits are read from the highest offset. Note that reading the highest offset also clears the entire entropy value, and starts a new entropy generation.

41.1.3.3.29 TRNG0 Statistical Check Poker Count 1 and 0 (TRNG0_PKRCNT10)

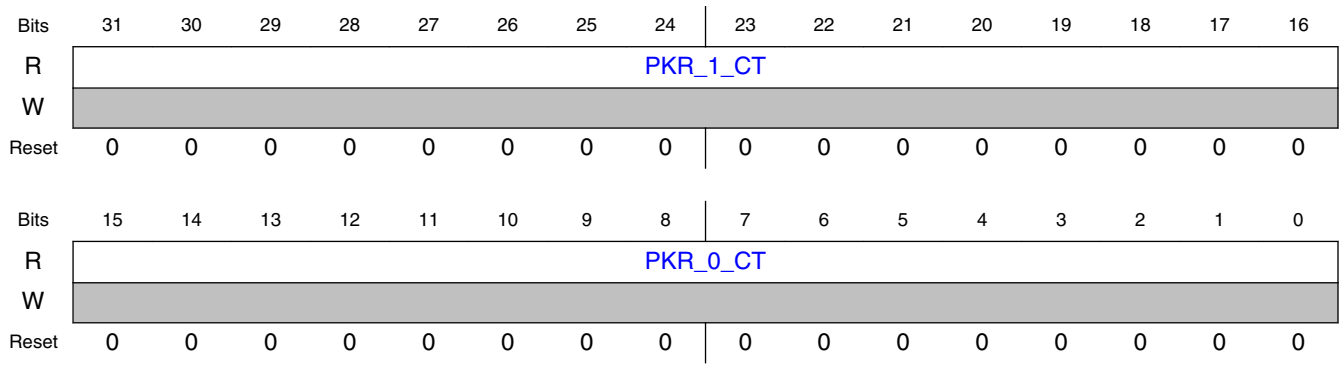
41.1.3.3.29.1 Address

Register	Offset
TRNG0_PKRCNT10	80h

41.1.3.3.29.2 Function

The TRNG0 Statistical Check Poker Count 1 and 0 Register is a read-only register used to read the final Poker test counts of 1h and 0h patterns. The Poker 0h Count increments each time a nibble of sample data is found to be 0h. The Poker 1h Count increments each time a nibble of sample data is found to be 1h. Note that this register is readable only if TRNG0_MCTL[PRGM] is 0, otherwise zeroes will be read.

41.1.3.3.29.3 Diagram



41.1.3.3.29.4 Fields

Field	Function
31-16 PKR_1_CT	Poker 1h Count. Total number of nibbles of sample data which were found to be 1h. Requires TRNG0_MCTL[PRGM] = 0.
15-0 PKR_0_CT	Poker 0h Count. Total number of nibbles of sample data which were found to be 0h. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.30 TRNG0 Statistical Check Poker Count 3 and 2 (TRNG0_PKRCNT32)

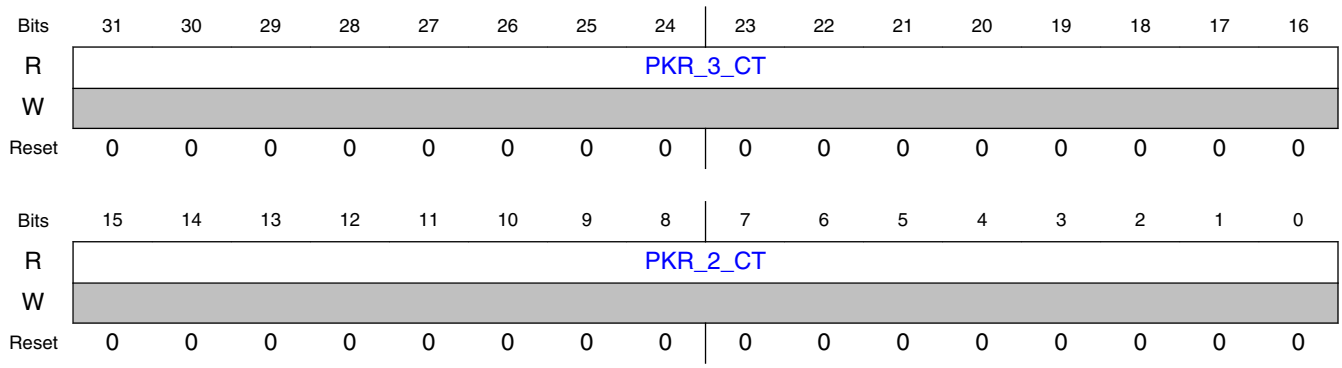
41.1.3.3.30.1 Address

Register	Offset
TRNG0_PKRCNT32	84h

41.1.3.3.30.2 Function

The TRNG0 Statistical Check Poker Count 3 and 2 Register is a read-only register used to read the final Poker test counts of 3h and 2h patterns. The Poker 2h Count increments each time a nibble of sample data is found to be 2h. The Poker 3h Count increments each time a nibble of sample data is found to be 3h. Note that this register is readable only if TRNG0_MCTL[PRGM] is 0, otherwise zeroes will be read.

41.1.3.3.30.3 Diagram



41.1.3.3.30.4 Fields

Field	Function
31-16 PKR_3_CT	Poker 3h Count. Total number of nibbles of sample data which were found to be 3h. Requires TRNG0_MCTL[PRGM] = 0.
15-0 PKR_2_CT	Poker 2h Count. Total number of nibbles of sample data which were found to be 2h. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.31 TRNG0 Statistical Check Poker Count 5 and 4 (TRNG0_PKRCNT54)

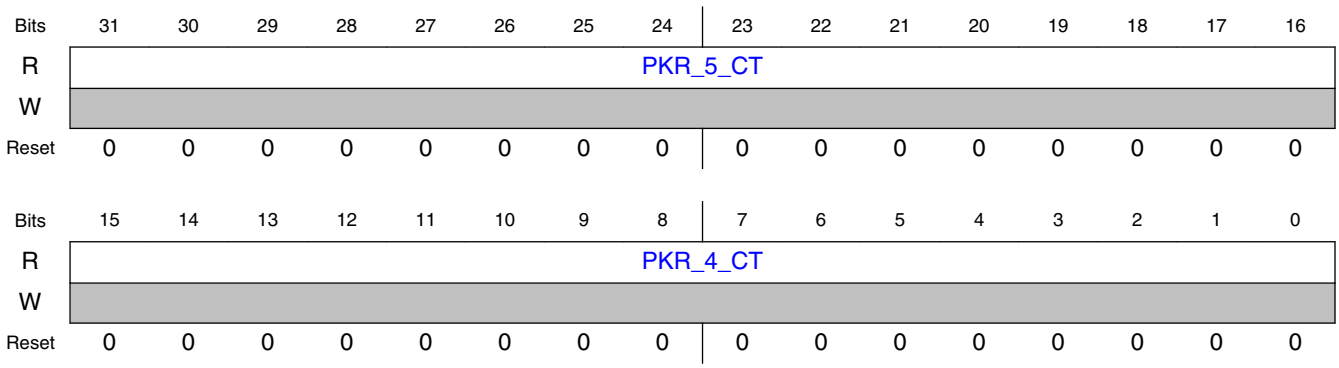
41.1.3.3.31.1 Address

Register	Offset
TRNG0_PKRCNT54	88h

41.1.3.3.31.2 Function

The TRNG0 Statistical Check Poker Count 5 and 4 Register is a read-only register used to read the final Poker test counts of 5h and 4h patterns. The Poker 4h Count increments each time a nibble of sample data is found to be 4h. The Poker 5h Count increments each time a nibble of sample data is found to be 5h. Note that this register is readable only if TRNG0_MCTL[PRGM] is 0, otherwise zeroes will be read.

41.1.3.3.31.3 Diagram



41.1.3.3.31.4 Fields

Field	Function
31-16 PKR_5_CT	Poker 5h Count. Total number of nibbles of sample data which were found to be 5h. Requires TRNG0_MCTL[PRGM] = 0.
15-0 PKR_4_CT	Poker 4h Count. Total number of nibbles of sample data which were found to be 4h. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.32 TRNG0 Statistical Check Poker Count 7 and 6 (TRNG0_PKRCNT76)

41.1.3.3.32.1 Address

Register	Offset
TRNG0_PKRCNT76	8Ch

41.1.3.3.32.2 Function

The TRNG0 Statistical Check Poker Count 7 and 6 Register is a read-only register used to read the final Poker test counts of 7h and 6h patterns. The Poker 6h Count increments each time a nibble of sample data is found to be 6h. The Poker 7h Count increments each time a nibble of sample data is found to be 7h. Note that this register is readable only if TRNG0_MCTL[PRGM] is 0, otherwise zeroes will be read.

41.1.3.3.32.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	PKR_7_CT															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PKR_6_CT															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

41.1.3.3.32.4 Fields

Field	Function
31-16 PKR_7_CT	Poker 7h Count. Total number of nibbles of sample data which were found to be 7h. Requires TRNG0_MCTL[PRGM] = 0.
15-0 PKR_6_CT	Poker 6h Count. Total number of nibbles of sample data which were found to be 6h. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.33 TRNG0 Statistical Check Poker Count 9 and 8 (TRNG0_PKRCNT98)

41.1.3.3.33.1 Address

Register	Offset
TRNG0_PKRCNT98	90h

41.1.3.3.33.2 Function

The TRNG0 Statistical Check Poker Count 9 and 8 Register is a read-only register used to read the final Poker test counts of 9h and 8h patterns. The Poker 8h Count increments each time a nibble of sample data is found to be 8h. The Poker 9h Count increments each time a nibble of sample data is found to be 9h. Note that this register is readable only if TRNG0_MCTL[PRGM] is 0, otherwise zeroes will be read.

41.1.3.3.33.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	PKR_9_CT															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PKR_8_CT															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

41.1.3.3.33.4 Fields

Field	Function
31-16 PKR_9_CT	Poker 9h Count. Total number of nibbles of sample data which were found to be 9h. Requires TRNG0_MCTL[PRGM] = 0.
15-0 PKR_8_CT	Poker 8h Count. Total number of nibbles of sample data which were found to be 8h. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.34 TRNG0 Statistical Check Poker Count B and A (TRNG0_PKRCNTBA)

41.1.3.3.34.1 Address

Register	Offset
TRNG0_PKRCNTBA	94h

41.1.3.3.34.2 Function

The TRNG0 Statistical Check Poker Count B and A Register is a read-only register used to read the final Poker test counts of Bh and Ah patterns. The Poker Ah Count increments each time a nibble of sample data is found to be Ah. The Poker Bh Count increments each time a nibble of sample data is found to be Bh. Note that this register is readable only if TRNG0_MCTL[PRGM] is 0, otherwise zeroes will be read.

41.1.3.3.34.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	PKR_B_CT															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PKR_A_CT															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

41.1.3.3.34.4 Fields

Field	Function
31-16 PKR_B_CT	Poker Bh Count. Total number of nibbles of sample data which were found to be Bh. Requires TRNG0_MCTL[PRGM] = 0.
15-0 PKR_A_CT	Poker Ah Count. Total number of nibbles of sample data which were found to be Ah. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.35 TRNG0 Statistical Check Poker Count D and C (TRNG0_PKRCNTDC)

41.1.3.3.35.1 Address

Register	Offset
TRNG0_PKRCNTDC	98h

41.1.3.3.35.2 Function

The TRNG0 Statistical Check Poker Count D and C Register is a read-only register used to read the final Poker test counts of Dh and Ch patterns. The Poker Ch Count increments each time a nibble of sample data is found to be Ch. The Poker Dh Count increments each time a nibble of sample data is found to be Dh. Note that this register is readable only if TRNG0_MCTL[PRGM] is 0, otherwise zeroes will be read.

41.1.3.3.35.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	PKR_D_CT															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PKR_C_CT															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

41.1.3.3.35.4 Fields

Field	Function
31-16 PKR_D_CT	Poker Dh Count. Total number of nibbles of sample data which were found to be Dh. Requires TRNG0_MCTL[PRGM] = 0.
15-0 PKR_C_CT	Poker Ch Count. Total number of nibbles of sample data which were found to be Ch. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.36 TRNG0 Statistical Check Poker Count F and E (TRNG0_PKRCNTFE)

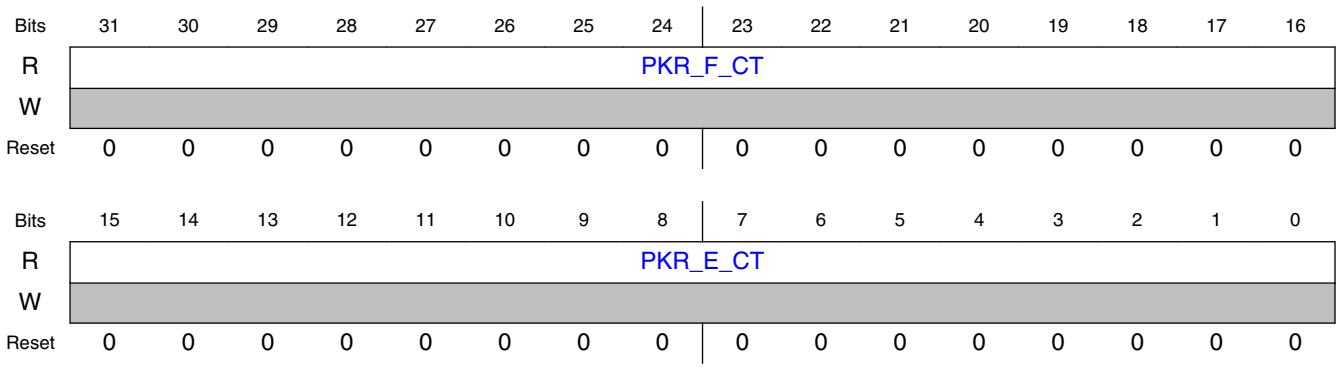
41.1.3.3.36.1 Address

Register	Offset
TRNG0_PKRCNTFE	9Ch

41.1.3.3.36.2 Function

The TRNG0 Statistical Check Poker Count F and E Register is a read-only register used to read the final Poker test counts of Fh and Eh patterns. The Poker Eh Count increments each time a nibble of sample data is found to be Eh. The Poker Fh Count increments each time a nibble of sample data is found to be Fh. Note that this register is readable only if TRNG0_MCTL[PRGM] is 0, otherwise zeroes will be read.

41.1.3.3.36.3 Diagram



41.1.3.3.36.4 Fields

Field	Function
31-16 PKR_F_CT	Poker Fh Count. Total number of nibbles of sample data which were found to be Fh. Requires TRNG0_MCTL[PRGM] = 0.
15-0 PKR_E_CT	Poker Eh Count. Total number of nibbles of sample data which were found to be Eh. Requires TRNG0_MCTL[PRGM] = 0.

41.1.3.3.37 TRNG0 Security Configuration (TRNG0_SEC_CFG)

41.1.3.3.37.1 Address

Register	Offset
TRNG0_SEC_CFG	B0h

41.1.3.3.37.2 Function

The TRNG0 Security Configuration Register is a read/write register used to control the test mode, programmability and state modes of the TRNG0. Many bits are place holders for this version. More configurability will be added here. Clears on asynchronous reset. For TRNG0 releases before 2014/July/01, offsets 0xA0 to 0xAC used to be 0xB0 to 0xBC respectively. So, update newer tests that use these registers, if hard coded.

41.1.3.3.37.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved													SK_VAL	NO_PRGM	SH0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

41.1.3.3.37.4 Fields

Field	Function
31-3 —	Reserved.
2 SK_VAL	Reserved. DRNG-specific, not applicable to this version. 0 - See DRNG version. 1 - See DRNG version.
1 NO_PRGM	If set, the TRNG registers cannot be programmed. That is, regardless of the TRNG access mode in the TRNG0 Miscellaneous Control Register. 0 - Programability of registers controlled only by the TRNG0 Miscellaneous Control Register's access mode bit. 1 - Overides TRNG0 Miscellaneous Control Register access mode and prevents TRNG register programming.
0 SH0	Reserved. DRNG specific, not applicable to this version. 0 - See DRNG version. 1 - See DRNG version.

41.1.3.3.38 TRNG0 Interrupt Control (TRNG0_INT_CTRL)

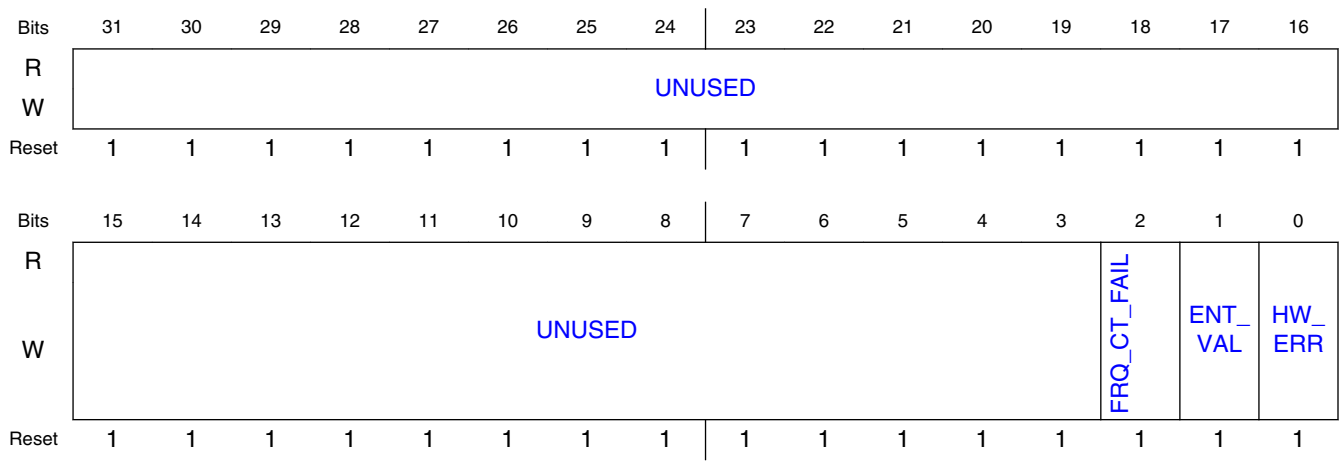
41.1.3.3.38.1 Address

Register	Offset
TRNG0_INT_CTRL	B4h

41.1.3.3.38.2 Function

The TRNG0 Interrupt Control Register is a read/write register used to control the status for the (currently) three important interrupts that are generated by the TRNG. See TRNG0_INT_STATUS register description above. Each interrupt can be cleared by de-asserting the corresponding bit in the TRNG0_INT_CTRL register. Only a new interrupt will reassert the corresponding bit in the status register. Even if the interrupt is cleared or masked, interrupt status information can be read from the TRNG0_MCTL register.

41.1.3.3.38.3 Diagram



41.1.3.3.38.4 Fields

Field	Function
31-3 UNUSED	Reserved but writeable.
2 FRQ_CT_FAIL	Same behavior as bit 0 above. 0 - Same behavior as bit 0 above. 1 - Same behavior as bit 0 above.
1 ENT_VAL	Same behavior as bit 0 above. 0 - Same behavior as bit 0 above. 1 - Same behavior as bit 0 above.
0 HW_ERR	Bit position that can be cleared if corresponding bit of TRNG0_INT_STATUS has been asserted. 0 - Corresponding bit of TRNG0_INT_STATUS cleared. 1 - Corresponding bit of TRNG0_INT_STATUS active.

41.1.3.3.39 TRNG0 Mask (TRNG0_INT_MASK)

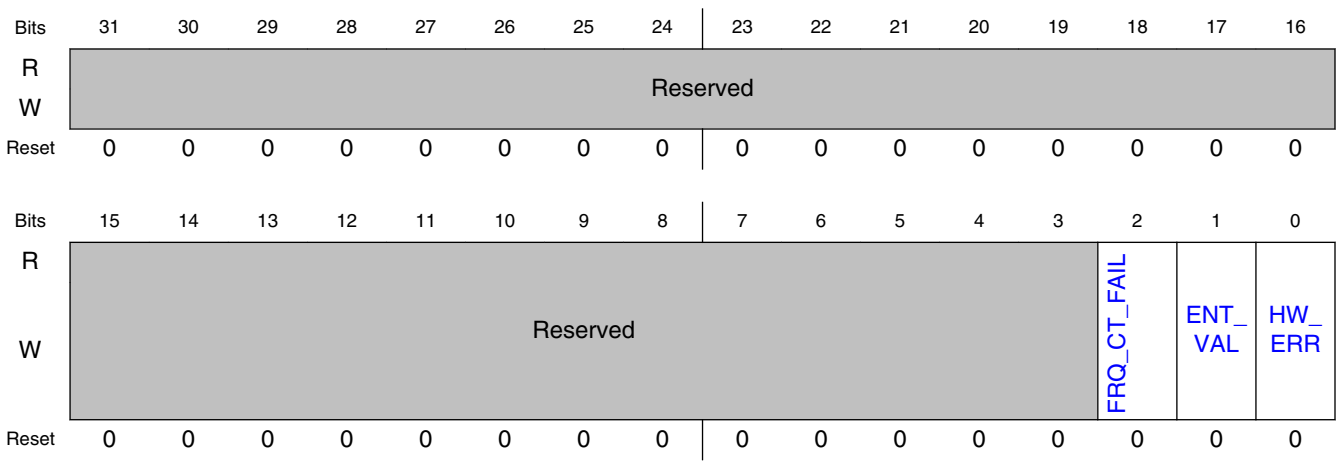
41.1.3.3.39.1 Address

Register	Offset
TRNG0_INT_MASK	B8h

41.1.3.3.39.2 Function

The TRNG0 Interrupt Mask Register is a read/write register used to disable/mask the status reporting of the (currently) three important interrupts that are generated by the TRNG. See TRNG0_INT_STATUS register description above. Each interrupt can be masked/disabled by de-asserting the corresponding bit in the TRNG0_INT_MASK register. Only setting this bit high will re-enable the interrupt in the status register. Even if the interrupt is cleared or masked, interrupt status information can be read from the TRNG0_MCTL register.

41.1.3.3.39.3 Diagram



41.1.3.3.39.4 Fields

Field	Function
31-3 —	Reserved.
2 FRQ_CT_FAIL	Same behavior as bit 0 above. 0 - Same behavior as bit 0 above. 1 - Same behavior as bit 0 above.
1 ENT_VAL	Same behavior as bit 0 above. 0 - Same behavior as bit 0 above. 1 - Same behavior as bit 0 above.

Table continues on the next page...

Field	Function
0 HW_ERR	Bit position that can be cleared if corresponding bit of TRNG0_INT_STATUS has been asserted. 0 - Corresponding interrupt of TRNG0_INT_STATUS is masked. 1 - Corresponding bit of TRNG0_INT_STATUS is active.

41.1.3.3.40 TRNG0 Interrupt Status (TRNG0_INT_STATUS)

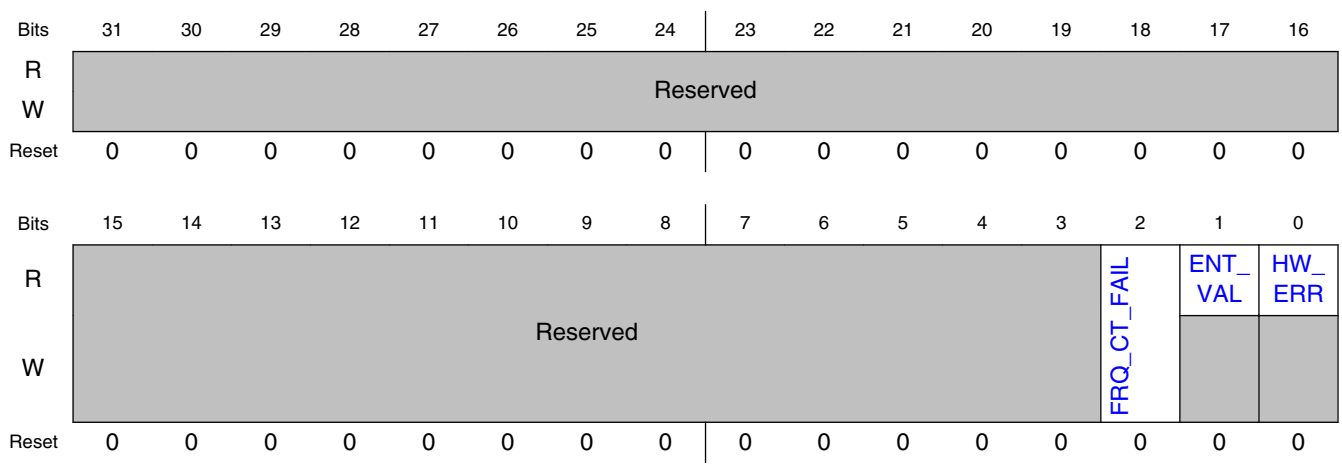
41.1.3.3.40.1 Address

Register	Offset
TRNG0_INT_STATUS	BCh

41.1.3.3.40.2 Function

The TRNG0 Interrupt Status Register is a read register used to control and provide status for the (currently) three important interrupts that are generated by the TRNG. The ipi_rng_int_b interrupt signals that TRNG0 has either generated a Frequency Count Fail, Entropy Valid or Error Interrupt. The cause of the interrupt can be decoded by checking the least significant bits of the TRNG0_INT_STATUS register. Each interrupt can be temporarily cleared by de-asserting the corresponding bit in the TRNG0_INT_CTRL register. To mask the interrupts, clear the corresponding bits in the TRNG0_INT_MASK register. The description of each of the 3 interrupts is defined in the Block Guide under the TRNG0_MCTL register description. Even if the interrupt is cleared or masked, interrupt status information can be read from the TRNG0_MCTL register.

41.1.3.3.40.3 Diagram



41.1.3.3.40.4 Fields

Field	Function
31-3 —	Reserved.
2 FRQ_CT_FAIL	Read only: Frequency Count Fail. The frequency counter has detected a failure. This may be due to improper programming of the TRNG0_FRQMAX and/or TRNG0_FRQMIN registers, or a hardware failure in the ring oscillator. 0 - No hardware nor self test frequency errors. 1 - The frequency counter has detected a failure.
1 ENT_VAL	Read only: Entropy Valid. Will assert only if TRNG ACC bit is set, and then after an entropy value is generated. Will be cleared when TRNG0_ENT15 is read. (TRNG0_ENT0 through TRNG0_ENT14 should be read before reading TRNG0_ENT15). 0 - Busy generation entropy. Any value read is invalid. 1 - TRNG can be stopped and entropy is valid if read.
0 HW_ERR	Read: Error status. 1 = error detected. 0 = no error. Any HW error in the TRNG will trigger this interrupt. 0 - no error 1 - error detected.

41.1.3.3.41 TRNG0 Version ID (MS) (TRNG0_VID1)

41.1.3.3.41.1 Address

Register	Offset
TRNG0_VID1	F0h

41.1.3.3.41.2 Function

The TRNG0 Version ID Register is a read only register used to identify the version of the TRNG in use. This register as well as TRNG0_VID2 should both be read to verify the expected version.

41.1.3.3.41.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	TRNG0_IP_ID															
W																
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	TRNG0_MAJ_REV								TRNG0_MIN_REV							
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

41.1.3.3.41.4 Fields

Field	Function
31-16 TRNG0_IP_ID	Shows the Freescale IP ID. 0000000000110000 - ID for TRNG.
15-8 TRNG0_MAJ_REV	Shows the Freescale IP's Major revision of the TRNG. 00000001 - Major revision number for TRNG.
7-0 TRNG0_MIN_REV	Shows the Freescale IP's Minor revision of the TRNG. 00000000 - Minor revision number for TRNG.

41.1.3.3.42 TRNG0 Version ID (LS) (TRNG0_VID2)

41.1.3.3.42.1 Address

Register	Offset
TRNG0_VID2	F4h

41.1.3.3.42.2 Function

The TRNG0 Version ID Register LSB is a read only register used to identify the architecture of the TRNG in use. This register as well as TRNG0_VID1 should both be read to verify the expected version.

41.1.3.3.42.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	TRNG0_ERA								TRNG0_INTG_OPT							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	TRNG0_ECO_REV								TRNG0_CONFIG_OPT							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

41.1.3.3.42.4 Fields

Field	Function
31-24 TRNG0_ERA	Shows the Freescale compile options for the TRNG. 00000000 - COMPILE_OPT for TRNG.
23-16 TRNG0_INTG_OPT	Shows the Freescale integration options for the TRNG. 00000000 - INTG_OPT for TRNG.
15-8 TRNG0_ECO_REV	Shows the Freescale IP's ECO revision of the TRNG. 00000000 - TRNG_ECO_REV for TRNG.
7-0 TRNG0_CONFIG_OPT	Shows the Freescale IP's Configuaration options for the TRNG. 00000000 - TRNG_CONFIG_OPT for TRNG.

41.1.4 Another TRNG usage example.

The TRNG can be used by a post processing pseudo-random number generator function. For example, TRNG can be used to seed a hardware or software based implementation of a DRBG defined by SP800-90.

Chapter 42
LP Trusted Cryptography (LTC)

42.1 LP Trusted Cryptography Block Diagram

LP Trusted Cryptography is an architecture that allows multiple cryptographic hardware accelerator engines to be instantiated and share common registers. This version of LTC only supports AES, DES, 3DES, RSA and ECC. The following figure presents a top-level diagram of the LP Trusted Cryptography module.

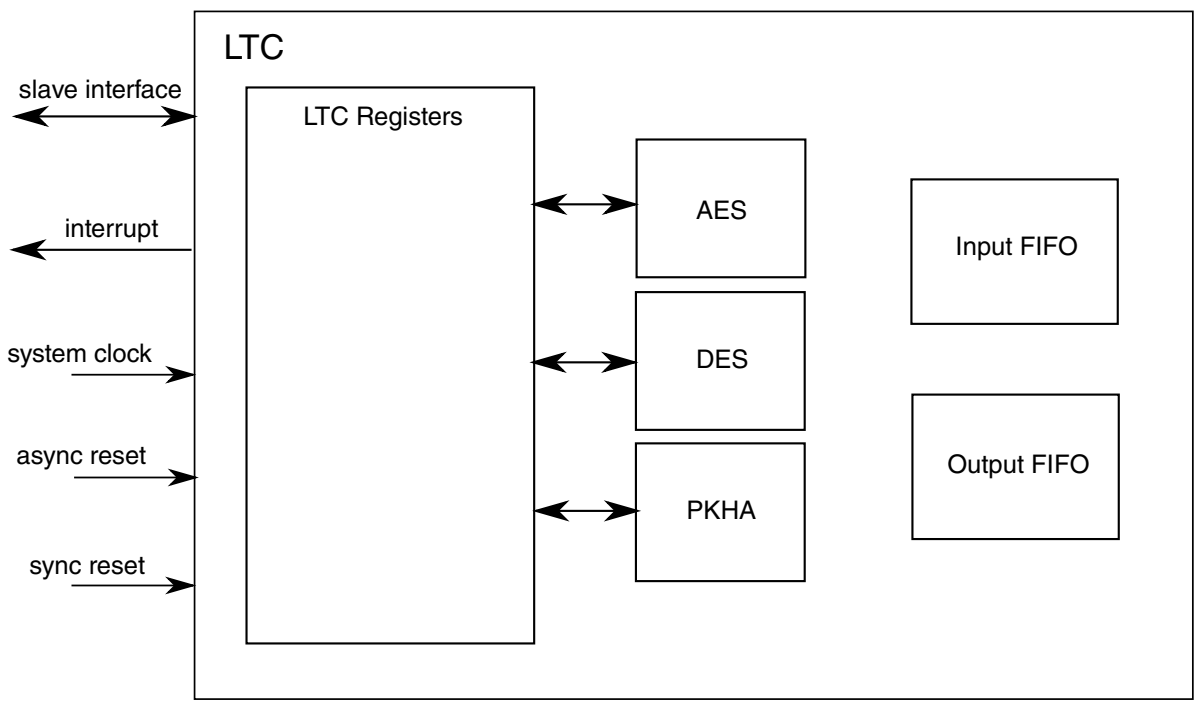


Figure 42-1. LTC Block Diagram

42.2 Feature summary

LTC includes the following features:

- Cryptographic authentication
  - Message authentication codes (MAC)
    - AES-CMAC
    - AES-XCBC-MAC
  - Auto padding
  - ICV checking
- Authenticated encryption algorithms
  - AES-CCM (counter with CBC-MAC)
  - AES-GCM (Galois counter mode)
- Symmetric key block ciphers
  - AES (128-bit, 192-bit or 256-bit keys)
  - DES (64-bit keys, including key parity)
  - 3DES (128-bit or 192-bit keys, including key parity)
  - Cipher modes
    - ECB, CBC, CTR for AES
    - ECB, CBC, CFB, OFB for DES
- Public key cryptography
  - Modular Arithmetic
    - Addition, subtraction, multiplication, exponentiation, reduction, inversion, greatest common denominator
    - Both integer and binary polynomial functions
    - Modulus size up to 2048 bits
    - Arithmetic operations performed with 16-bit-digit arithmetic unit
    - Timing-equalized and normal versions of modular exponentiation
  - DSA up to 2048 bits
  - Diffie-Hellman (DH) key agreement up to 2048 bits
  - RSA up to 2048 bits
  - Primality testing
    - Maximum size 2048 bits
  - Elliptic curve cryptography
    - Point add, point double, point multiply
    - Point validation (is point on curve)
    - Timing-equalized and normal versions of point multiplication
    - Both prime field and binary polynomial field functions
    - Elliptic curve Diffie-Hellman key agreement
    - Modulus size up to 512 bits
- Secure Scan

42.3 AES accelerator (AESA) functionality

The advanced encryption standard accelerator (AESA) module is a hardware co-processor capable of accelerating the advanced encryption standard (AES) cryptographic algorithm.

42.3.1 Differences between the AES encrypt and decrypt keys

The decrypt form of the key is different from the encrypt form of the key, because AES successively modifies the cryptographic key during the steps of the cryptographic operation. The decryption operation yields the correct result only if the modified form of the key (the decrypt key) is used at the beginning of the decryption operation. Unless told otherwise (via the DK bit in the Mode Register), AES assumes that a key loaded from memory is the encrypt key, that is, the form appropriate for encryption. If a decryption operation is specified and DK = 0, AES first goes through the steps required to derive the decrypt key from the encrypt key, and then performs the decryption operation. If a decryption operation is specified and DK = 1, the steps required to derive the decrypt key are skipped and the decryption operation is performed immediately, significantly improving performance for small data blocks.

Note that the difference between the encrypt key and the decrypt key must be taken into account when sharing keys between jobs. When an AES decryption job loads a key from memory, it is probably an encrypt key, so the DK bit in the Mode Register should be set to 0 so that AES derives the decrypt key from the encrypt key before beginning the decryption operation. But when a subsequent AES decryption job shares the key from a previous decryption job, the key that is shared is a decrypt key. In that case, the DK bit should be set to 1, which tells AES to skip the key derivation steps. If DK were set to 0 in this case, the decrypt key would be modified as if it were an encrypt key, and consequently, the wrong key value would be used in the decryption operation.

42.3.2 AESA modes of operation

The following modes are supported by AESA:

- Electronic codebook (ECB)
- Cipher block chaining (CBC)
- Counter (CTR)
- Extended cipher block chaining message authentication code (XCBC-MAC)
- Cipher-based MAC (CMAC)

- CTR and CBC-MAC (CCM)
- Galois/Counter mode (GCM)

AES modes can be classified into these categories:

- Confidentiality (ECB, CBC, CTR)
- Authenticated Confidentiality (CCM, GCM)
- Authentication (XCBC-MAC, CMAC)

CBC Mode can also be viewed as an authentication mode when used to encrypt data, because it provides CBC-MAC in the context registers.

42.3.3 AESA use of registers

Note the following regarding the AESA's use of registers:

- For all modes, if AES is selected and the mode code written to the Mode Register does not correspond to any of the implemented AES modes, the illegal-mode error is generated.
- KEY SIZE, MODE and DATA SIZE can be written in any order. The operation will begin after all of these have been written.
- When sharing context between consecutive AES jobs, software reset is not issued. To prepare AES for the next job, the Data Size Register and Mode Register must be cleared, as well as the Done Interrupt. The order of these should be such that the Done Interrupt is not cleared first.
- If ICV-only jobs are created (no data to be processed, only ICV to be checked) in modes that support ICV check, the AS mode field should be reset.

42.3.4 AES ECB mode

The electronic codebook (ECB) mode is a confidentiality mode that features, for a given key, the assignment of a fixed, ciphertext block to each plaintext block, analogous to the assignment of code words in a codebook. In ECB encryption, the forward cipher function is applied directly and independently to each block of the plaintext. The resulting sequence of output blocks is the ciphertext. In ECB decryption, the inverse cipher function is applied directly and independently to each block of the ciphertext. The resulting sequence of output blocks is the plaintext.

42.3.4.1 AES ECB mode use of the Mode Register

AES ECB mode uses the Mode Register as follows:

- The Encrypt (ENC) field should be 1 for ECB encryption and 0 for ECB decryption.
- The ICV/TEST bit is used in ECB mode to activate the fault detection test logic. This logic verifies that the fault detection logic is operational by injecting bit-level errors into input data and key bytes. Because ECB mode does not normally use the Context Registers, the first 128 bits of the context are used in the ECB TEST mode to define which byte of the input data and the key has a bit error injected.
- The Algorithm State (AS) field is not used in ECB mode.
- The Additional Algorithm Information (AAI) field must be set with value 20h that activates ECB mode. Setting the MSB in the AAI field (interpreted as the Decrypt Key or DK bit for AES operations) specifies that the key loaded to the Key Register is the decryption form of the key, rather than the encryption form of the key. If DK = 0, when a decryption operation is requested LTC processes the content of the Key Register to yield the decryption form of the key. If DK = 1, skips this processing. The illegal-mode error is generated if DK = 1 and ENC=1.
- The Algorithm (ALG) field is used to activate AESA by setting it to 10h.

42.3.4.2 AES ECB mode use of the Context Register

ECB does not use Context Registers.

42.3.4.3 AES ECB Mode use of the Data Size Register

The length of the message to be processed in bytes must be written to the Data Size register. If this value is not divisible by 16, the Data Size error is generated.

42.3.4.4 AES ECB Mode use of the Key Register

ECB keys must be written to the Key Register and can have 16, 24, or 32 bytes.

42.3.4.5 AES ECB Mode use of the Key Size Register

The number of bytes in the ECB key must be written to the Key Size register. The KEY SIZE, MODE and DATA SIZE can be written in any order. Processing starts after all of them have been written. Any value other than 16, 24, or 32 causes the key-size error to be generated.

42.3.5 AES CBC mode

The CBC mode is described in this table.

Table 42-1. AES CBC Mode

Name	Abbreviation	Function
Cipher-block chaining mode	CBC	Confidentiality mode whose encryption process features the combining ("chaining") of the plaintext blocks with the previous ciphertext blocks. The CBC mode requires an IV (Initialization Vector) to combine with the first plaintext block **NOTE:** CBC mode uses both forward and inverse AES cipher.

42.3.5.1 AES CBC mode use of the Mode Register

The AES CBC mode uses the Mode Register as follows:

- The Encrypt (ENC) field should be 1 for encryption and 0 for decryption.
- The ICV/TEST bit is not used in these modes.
- The Algorithm State (AS) field is used only in CBC mode to prevent IV update in the context for the last data block when set to "Finalize" (2h).
- The Additional Algorithm Information (AAI) field defines which mode is used for processing. For CBC this value is 10h. The Decrypt Key [DK] (AAI field MSB) bit affects CBC mode and specifies that the key loaded to the Key Register is the decrypt key. The illegal mode error is generated if DK=1 and ENC=1.
- The Algorithm (ALG) field is used to activate AESA by setting it to 10h.

42.3.5.2 AES CBC mode use of the Context Register

The AES CBC mode uses the Context Register as follows:

- AES CBC uses the Context Registers to provide IV, which is updated with every processed block of a message. When a message is split into chunks and processed in multiple sessions, the IV must be saved and later restored for the next chunk to be processed correctly. At the end of CBC processing, IV is also the MAC of the message.
- If the AS field of the Mode Register is set to "Finalize" (2h) in the CBC mode, the last IV update is not written to the context. This enables CBC encryption to effectively perform ECB encryption transformation of a single-block message

located in the context in place of IV, and with an all-zero block provided as input data through the FIFO without overwriting the context.

Table 42-2. Context usage in CBC mode

Context Word	Definition
0	IV [127:96]
1	IV [95:64]
2	IV [63:32]
3	IV [31:0]

42.3.5.3 AES CBC mode use of the Data Size Register

The AES CBC mode uses the Data Size Register as follows:

- The byte length of the message to be processed must be written to the Data Size Register.
- After the Data Size Register is written, its value must be divisible by 16 in CBC mode, otherwise the data-size error is generated.

42.3.5.4 AES CBC mode use of the Key Register

The AES CBC mode uses the Key Register as follows:

- A CBC key must be written to the Key Register.
- Keys can have 16, 24, or 32 bytes.

42.3.5.5 AES CBC mode use of the Key Size Register

The AES CBC mode uses the Key Size Register as follows:

- The number of bytes in a key must be written to the Key Size register.
- Any value other than 16, 24, or 32 causes a key-size error to be generated.

42.3.6 AES CTR mode

The counter (CTR) mode is a confidentiality mode that features the application of the forward cipher to a set of input blocks, called counters, to produce a sequence of output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice

versa. Note that the counter value must be unique for each data block that is encrypted with the same key. uses a 128-bit counter to ensure that the counter value will not overflow and wrap around.

NOTE

It is the user's responsibility to ensure that the same key value is not used again following a reset.

42.3.6.1 AES CTR mode use of the Mode Register

The AES CTR mode uses the Mode Register as follows:

- The Additional Algorithm Information (AAI) field should be set to 00h to activate CTR mode. If the Decrypt Key [DK] (AAI field MSB) bit is set, the illegal-mode error is generated, because CTR uses only forward AES cipher requiring encryption rather than decryption keys.
- The Algorithm State (AS) field when set to "Finalize" (2h) prevents counter update in the context for the last data block.
- The Algorithm (ALG) field is used to activate AESA by setting it to 10h.

42.3.6.2 AES CTR mode use of the Context Register

The AES CTR mode uses the Context Register as follows:

- CTR uses context words 4,5,6 and 7 to provide initial counter value (CTR0). This value is incremented with every processed block of a message. When a message is split into chunks and processed in multiple sessions, the CTRi field of context has to be saved and later restored for the next chunk to be processed correctly.
- If the AS field of the Mode Register is set to Finalize (2h) in the CTR mode, the last counter update is not written to the context. This enables CTR encryption to effectively perform ECB encryption transformation of a single-block message located in the context words 4,5,6 and 7 in place of CTR0 and with all-zero block provided as input data through the FIFO without overwriting the context.

Table 42-3. Context usage in CTR mode

Context Word	Initial-input definition	Context-switching definition
0	-	-
1	-	-
2	-	-
3	-	-

Table continues on the next page...

Table 42-3. Context usage in CTR mode (continued)

Context Word	Initial-input definition	Context-switching definition
4	CTR0 [127:96]	CTRi [127:96]
5	CTR0 [95:64]	CTRi [95:64]
6	CTR0 [63:32]	CTRi [63:32]
7	CTR0 [31:0]	CTRi [31:0]

42.3.6.3 AES CTR mode use of the Data Size Register

The byte-length of the message to be processed must be written to the Data Size register. After the Data Size register is written, the value of this register may not be divisible by 16. CTR decrements the value in this register with every processed block.

42.3.6.4 AES CTR mode use of the Key Register

- CTR key must be written to the Key Register.
- The Key Register can have 16, 24 or 32 bytes.

42.3.6.5 AES CTR mode use of the Key Size Register

The number of bytes in a key must be written to the Key Size register. Any value other than 16, 24, or 32 will cause Key Size error to be generated.

42.3.7 AES XCBC-MAC and CMAC modes

The AES XCBC-MAC and CMAC modes are described together because of their similarities. They are extensions of the AES CBC mode that produces a key-dependent, one--way hash (or message authentication code (MAC)) in a secure fashion across messages of varying lengths. They also provide data-integrity and data-origin authentication regarding the original message source.

42.3.7.1 AES XCBC-MAC and CMAC modes use of the Mode Register

The AES XCBC-MAC and CMAC modes use the Mode Register as follows:

- The Encrypt (ENC) bit is ignored.

- The ICV_TEST bit must be set for computed MAC to be compared with the received MAC. The received MAC must be written to the Input Data FIFO after message data. If this bit is not set, XCBC-MAC and CMAC do not expect received ICV to be supplied after message data.
- The Algorithm State (AS) field is defined for XCBC-MAC as shown in this table.

Table 42-4. Mode Register[AS] operation selections in AES XCBC-MAC

Operation	Description
INITIALIZE	Message is processed in multiple sessions and the current session is the first one. During initialization, derived keys K3 and K2 that are XOR-ed with the last message block are computed and stored in the context to be used in the last processing session. The derived key K1 used as an AES key is computed and written back to the Key Register over the original key
INITIALIZE/FINALIZE	Message is processed in a single XCBC session and the final MAC is computed
UPDATE	Message is processed in multiple sessions and the current session is neither the first nor the last. Derived keys K2 and K3 are provided in the context and the derived key K1 is provided in the Key Register. If decryption is requested, and data size is not written or is set to 0, and ICV_TEST bit is 1 - AS = UPDATE means that Check ICV (CICV) job is requested. The CICV-only job does not process any data, it just pops received ICV/MAC from the Input Data FIFO, and compares it to the computed MAC that is restored with the rest of the context from the previous session.
FINALIZE	Message is processed in multiple sessions and the current session is the last one. Derived keys K2 and K3 are provided in the context and the derived key K1 is provided in the Key Register. The final MAC is computed

- The Algorithm State (AS) field is defined for CMAC as shown in this table.

Table 42-5. Mode Register[AS] operation selections in CMAC

Operation	Function
INITIALIZE	Message is processed in multiple sessions and the current session is the first one. During initialization, the constant L = E(K, 0) is computed as encrypted block of zeros using key K and stored in the context to be used in the last processing session for derivation of keys K1 and K2. One of these keys will be XOR-ed with the last message block.
INITIALIZE/FINALIZE	Message is processed in a single session and the final MAC is computed
UPDATE	Message is processed in multiple sessions and the current session is neither the first nor the last. The constant L used for key derivation is provided in the context. If decryption is requested, and data size is not written or is set to 0, and ICV_TEST:w bit is 1 - AS = UPDATE means that Check ICV (CICV) job is requested. The CICV-only job does not process any data, it just pops received ICV/MAC from the Input Data FIFO, and compares it to the computed MAC that is restored with the rest of the context from the previous session
FINALIZE	Message is processed in multiple sessions and the current session is the last one. The constant L used for key derivation is provided in the context. The final MAC is computed

- If the AS field is not set to either "Initialize/Finalize" or "Finalize" and the ICV_TEST bit is set to 1, the illegal-mode error is generated, except for CICV-only jobs.

- The Additional Algorithm Information (AAI) field must be set to 70h for XCBC and 60h for CMAC to be activated. Setting the DK bit (AAI field MSB) will cause the Illegal Mode error.
- The Algorithm (ALG) field is used to activate AESA by setting it to 10h.

42.3.7.2 AES XCBC-MAC and CMAC Modes use of the Context Register

The AES XCBC-MAC and CMAC modes use the Context Register as follows:

- No data needs to be provided in the context when starting a new XCBC or CMAC session.
- The computed MAC and the derived keys K2 and K3 are written back to the context by XCBC.
- The computed MAC and the constant L = E(K,0), computed as encrypted block of zeros using key K, are written back to the context by CMAC.
- When a message is split into chunks and processed in multiple sessions, these values need to be saved before context switch and restored before the next chunk of a message is to be processed. At the end of message processing the first 2 dwords of the context contain the MAC value.

Table 42-6. Context usage in XCBC-MAC and CMAC modes

Mode	Context dword	Context-switching definition	Final-result definition
XCBC-MAC	0	MAC[127:64]	MAC[127:64]
	1	MAC[63:0]	MAC[63:0]
	2	K3[127:64]	-
	3	K3[63:0]	-
	4	K2[127:64]	-
	5	K2[63:0]	-
CMAC	0	MAC[127:64]	MAC[127:64]
	1	MAC[63:0]	MAC[63:0]
	2	L[127:64]	-
	3	L[63:0]	-

42.3.7.3 AES XCBC-MAC and CMAC modes use of the ICV Size Register

The AES XCBC-MAC and CMAC modes use the ICV Size Register as follows:

- This register is used to provide received ICV/MAC byte-size.

- The computed ICV/MAC written to the context in the XCBC mode is always 16 bytes.
- In CMAC mode, this register determines also the computed MAC size-the remaining bytes are cleared.
- Supported values for ICV size are 4 to 16 bytes. If this register is 0, the size of ICV is 16 bytes.

42.3.7.4 AES XCBC-MAC and CMAC modes use of the Data Size Register

The AES XCBC-MAC and CMAC modes use the Data Size Register as follows:

- The byte-length of the message to be processed must be written to the Data Size register.
- XCBC-MAC and CMAC decrement the value in this register with every processed block.

42.3.7.5 AES XCBC-MAC and CMAC modes use of the Key Register

The AES XCBC-MAC and CMAC modes use the Key Register as follows:

- The key must be written to this register.
- For XCBC-MAC, if the AS mode field is set to either "Initialize" or "Initialize/Finalize", it is the original XCBC key (K) that must be written here. Otherwise, the derived key (K1) must be restored to this register. CMAC only uses original key K as an AES key.

42.3.7.6 AES XCBC-MAC and CMAC modes use of the Key Size Register

The AES XCBC-MAC and CMAC modes use the Key Size Register as follows:

- The total number of key bytes must be written to the Key Size register.
- For XCBC-MAC, any value other than 16 causes a key-size error to be generated. For CMAC, this error is generated only if any value other than 16, 24, or 32 is written.

42.3.7.7 ICV checking in AES XCBC-MAC and CMAC modes

Automatic ICV checking is enabled by setting the ICV_TEST bit of the Mode Register to 1. When ICV is set to 1, the AS mode field must be set to either "Finalize" or "Initialize/Finalize"; otherwise the illegal-mode error is generated, except for CICV-only (Check-ICV-only) jobs.

The received ICV must be provided on the FIFO after the message data. The size of the received and computed ICV is provided in the ICV Size register.

If the ICV check detects a mismatch between the decrypted received ICV and the computed ICV, the ICV error is generated.

42.3.8 AESA CCM and CCM* mode

CCM and CCM* consists of two related processes: generation encryption and decryption verification, which combine two cryptographic primitives: counter mode encryption (CTR) and cipher-block chaining based authentication (CBC-MAC). Only the forward cipher function of the block cipher algorithm is used within these primitives. Note that the counter value must be unique for each data block that is encrypted with the same key. uses a 128-bit counter to ensure that the counter value does not overflow and wrap around.

NOTE

It is the user's responsibility to ensure that the same key value is not used again following a reset.

42.3.8.1 Generation encryption

A cipher-block chaining is applied to the payload, the associated data (AAD), and the nonce to generate a message authentication code (MAC); then counter mode encryption is applied to the MAC and the payload to transform them into an unreadable form, called the ciphertext. Thus, CCM generation encryption expands the size of the payload by the size of the MAC.

42.3.8.2 Decryption verification

Counter-mode decryption is applied to the purported ciphertext to recover the MAC and the corresponding payload; then cipher block chaining is applied to the payload, the received associated data, and the received nonce to verify the correctness of the MAC.

42.3.8.3 AES CCM and CCM* mode use of the Mode Register

The AES CCM and CCM* mode uses the Mode Register as follows:

- The Encrypt (ENC) bit must be set to 1 for encryption and 0 for decryption.
- The ICV_TEST bit must be set for CCM and CCM* to compare computed MAC with the received MAC when decryption is requested.
- The received MAC must be written to the input-data FIFO after message data.
- Setting the ICV_TEST bit causes the received MAC to be decrypted and compared with the computed MAC.
- The number of MSBs to be compared is defined by the MAC size in the CCM IV (B_0) as described in the CCM and CCM* specification.
- If the AS field is set to FINALIZE, but ICV = 0, AESA does not expect received ICV to be put on the input-data FIFO. In that case, MAC is computed and truncated to the specified size for decryption.
- For encryption, the computed MAC is encrypted and truncated to size. The illegal-mode error is generated if ICV = 1 and ENC = 1.
- If ICV = 1 and the decrypted received MAC do not match computed MAC, the ICV error is generated.
- The Algorithm State (AS) field is defined for CCM as follows:

Table 42-7. Mode Register[AS] operation selections in AES CCM

Operation	Description
INITIALIZE	Message is processed in multiple sessions and the current session is the first one. During initialization, the initial counter CTR0 is encrypted in the CTR mode and the B0 is processed with the CBC-MAC mode. The resulting values are stored in the context. Also, the size of MAC is decoded from B0 and written to the context. This AS setting must be used whenever the first part (or whole) AAD is being processed
INITIALIZE/FINALIZE	Message is processed in a single CCM session and the final MAC is computed and encrypted. The initial counter CTR0 and B0 must be provided in the context
UPDATE	Message is processed in multiple sessions and the current session is neither the first nor the last. All context data is restored from the previous session and the key is written to the Key Register. If decryption is requested, and data size is not written or is set to 0, and ICV_TEST bit is 1 - AS=UPDATE means that a CICV-only job is requested. The CICV-only job does not process any data, it just pops received ICV/MAC from the Input Data FIFO, decrypts it and compares it to the computed MAC that is restored with the rest of the context from the previous session
FINALIZE	Message is processed in multiple sessions and the current session is the last one. All context data is restored from the previous session and the key is written to the Key Register. The final MAC is computed and encrypted

- Whenever AS is set to Initialize or Initialize/Finalize, context registers must be zero.
- If the AS field is not set to either Initialize/Finalize or Finalize and the ICV_TEST bit is set to 1, the illegal-mode error is generated. This does not apply in case when only ICV check is requested as described for AS = UPDATE.

- The Additional Algorithm Information (AAI) field must be set to 80h for CCM or CCM* to be activated. Setting the DK bit causes the illegal-mode error.
- The Algorithm (ALG) field is used to activate AESA by setting it to 10h.

42.3.8.4 AES CCM and CCM* modes use of the Context Register

The AES CCM and CCM* mode uses the Context Register as follows:

- B0 and the initial counter CTR0 must be provided in the context before the first chunk of the message is to be processed. During initialization, the initial counter CTR0 is encrypted in the CTR mode and B0 (which functions like a CBC-MAC IV in CCM and CCM*) is processed with the CBC-MAC mode. The resulting values are stored in the context. Also, the size of MAC is decoded from B0 and written to context word 13.
- If there is AAD, the first block of it defines its size, and that value is decoded and written to context word 12. All of the context data must be restored before the next chunk of the message is to be processed in multi-session processing.
- For CCM and CCM* encryption, the ICV (encrypted final MAC) is written to context words 8-11. For CCM and CCM* decryption, the ICV (received MAC), which is always encrypted, is decrypted to words 8-11. The final computed MAC is written (in clear) to context words 0-3.

Table 42-8. Context usage in CCM and CCM* mode encryption

Context Word	Initial-input definition	Intermediate definition	Final-output definition
0	B0[127:96]	-	MAC[127:96]
1	B0[95:64]	-	MAC[95:64]
2	B0[63:32]	-	MAC[63:32]
3	B0[31:0]	-	MAC[31:0]
4	CTR0[127:96]	CTR[127:96]	-
5	CTR0[95:64]	CTR[95:64]	-
6	CTR0[63:32]	CTR[63:32]	-
7	CTR0[31:0]	CTR[31:0]	-
8	-	E(CTR0)[127:96][1]	E(MAC)[127:96]
9	-	E(CTR0)[95:64] [1]	E(MAC)[95:64]
10	-	E(CTR0)[63:32] [1]	E(MAC)[63:32]
11	-	E(CTR0)[31:0] [1]	E(MAC)[31:0]
12	-	AAD size; see Table 42-10	-
13	-	MAC size; see Table 42-11	-

1. E(x) means encrypted x

Table 42-9. Context usage in CCM and CCM* modes decryption

Context Word	Initial-input definition	Context-switching Definition	Final-result definition
0	B0[127:96]	-	MAC[127:96]
1	B0[95:64]	-	MAC[95:64]
2	B0[63:32]	-	MAC[63:32]
3	B0[31:0]	-	MAC[31:0]
4	CTR0[127:96]	CTR[127:96]	-
5	CTR0[95:64]	CTR[95:64]	-
6	CTR0[63:32]	CTR[63:32]	-
7	CTR0[31:0]	CTR[31:0]	-
8	-	E(CTR0)[127:96]	Decrypted Received MAC[127:96]
9	-	E(CTR0)[95:64]	Decrypted Received MAC[95:64]
10	-	E(CTR0)[63:32]	Decrypted Received MAC[63:32]
11	-	E(CTR0)[31:0] [1]	Decrypted Received MAC[31:0]
12	-	AAD size; see Table 42-10	-
13	-	MAC size; see Table 42-11	-

Table 42-10. Format of Context Word 12 for AES-CCM and AES-CCM* mode

Bit 31	Bits 30-16	Bits 15-0
AAD Presence Flag	0	AAD Size

Table 42-11. Format of Context Word 13 for AES-CCM and AES-CCM* mode

Bits 31-3	Bits 2-0
0	Encoded MAC Size

42.3.8.5 AES CCM and CCM* mode use of the Data Size Register

The AES CCM and CCM* mode uses the Data Size Register as follows:

- The byte-length of the message to be processed must be written to the Data Size register.

- CCM decrements the value in this register with every processed block.
- The content of the Data Size register must be divisible by 16 after the last write to it if the AS mode field is set to either "Update" or "Initialize". Otherwise, the data-size error is generated. In other words, message splitting can be done only on a 16-byte boundary.

42.3.8.6 AES CCM and CCM* mode use of the Key Register

CCM and CCM* key must be written to this register; it is always an encryption key.

42.3.8.7 AES CCM and CCM* mode use of the Key Size Register

The AES CCM and CCM* mode uses the Key Size Register as follows:

- The total number of key bytes must be written to the Key Size register.
- Any value other than 16, 24, or 32 causes a key-size error to be generated.

42.3.8.8 AES CCM and CCM* mode use of the ICV check

The AES CCM and CCM* mode uses ICV checking as follows:

- Automatic ICV checking is enabled by setting the ICV_TEST bit of the Mode Register to 1. When ICV is set to 1, the AS mode field must be set to either "Finalize" or "Initialize/Finalize"-otherwise the illegal-mode error is generated, unless data size is 0 indicating ICV check is only requested. Also, if ICV = 1, the ENC bit must be 0.
- The received ICV must be provided on the input data FIFO after the message data. In CCM, received ICV is always encrypted. The size of the received and computed ICV is for CCM encoded in the B0.
- If the ICV check detects mismatch between the decrypted received ICV and the computed ICV, the ICV error is generated.

42.3.9 AES GCM mode

The AES GCM provides the following:

- Data confidentiality using counter mode (CTR). Note that the counter value must be unique for each data block that is encrypted with the same key. uses a 128-bit counter to ensure that the counter value does not overflow and "wrap around", but it is the

user's responsibility to ensure that the same key value is not used again following a reset.

- Authentication (assurance of integrity) of the confidential data using a universal hash function (GHASH) that is defined over a binary Galois (that is, finite) field. GCM can also provide authentication assurance for additional data (AAD) that is not encrypted.
- Stronger authentication assurance than a (non-cryptographic) checksum or error detecting code; in particular, GCM can detect both of the following:
  - Accidental modifications of the data
  - Intentional, unauthorized modifications

42.3.9.1 GMAC

If the GCM input is restricted to data that is not encrypted, the resulting specialization of GCM, called GMAC, is simply an authentication mode on the input data.

42.3.9.2 GCM data types

These data types must always be provided in the following order:

1. IV
2. AAD
3. Message data

Any of these may be missing.

42.3.9.3 IV processing

IV is processed using GHASH function if the size of IV is not 12 bytes. The result of IV processing is the initial counter (Y0) value used for encryption/decryption. GHASH function is also performed on AAD and textdata before the MAC can be computed.

42.3.9.4 GCM initialization

GCM initialization is completed when all of the IV data is processed and the initial counter value (Y0) is computed as a result. For that to happen, IV data needs to be supplied through the Input Data FIFO and the FIFO data type must be set to IV.

42.3.9.5 AES GCM mode use of the Mode Register

The AES GCM mode uses the Mode Register as follows:

- The Encrypt (ENC) bit must be set to 1 for encryption and 0 for decryption. Even though operations performed in either case are identical, the authentication is done of the cipher text in parallel with decryption when ENC = 0, and after encryption of each block when ENC = 1.
- The ICV_TEST bit must be set for GCM to compare computed MAC with the received MAC. The received MAC must be written to the input-data FIFO after message data and the FIFO data type must be set to ICV. If this bit is not set, GCM does not expect received ICV to be supplied after textdata. The illegal-mode error is generated if ICV = 1 and ENC = 1.
- The Algorithm State (AS) field is defined for GCM as shown in this table:

Table 42-12. Mode Register[AS] operation selections in AES GCM

Operation	Value	Description
INITIALIZE	1h	Message is processed in multiple sessions and the current session processes final part of IV or textdata; do the final GHASH step, but do not compute MAC. **NOTE:** This AS state does not indicate initialization in GCM; instead, it means that the final step of the GHASH function is to be performed. In general, whenever the final GHASH iteration needs to be computed (either for GHASH(IV) or GHASH(AAD, ciphertext)), and the current message size provided in the Data Size Register is not equal to the total size for either IV, AAD, or textdata, AS should be set to INITIALIZE (1h). Consequently, an AS = 1h also indicates that the Context Registers 6-7 need to provide the total length of IV, AAD, or textdata for this to be accomplished.
INITIALIZE/ FINALIZE	3h	Message is processed in multiple sessions and the current session is the last. The final MAC is computed.
UPDATE	0h	Message is processed in multiple sessions (descriptors) and the current session is not the last. The descriptor contains a non-final part of IV, AAD, textdata (IV, AAD or textdata split between descriptors). If decryption is requested, and data size is not written or is set to 0, and ICV_TEST bit is 1 - AS = UPDATE means that Check ICV (CICV) job is requested. The CICV-only job does not process any data, it just pops received ICV/MAC from the Input Data FIFO, and compares it to the computed MAC that is restored with the rest of the context from the previous session
FINALIZE	2h	Message is processed in a single session. MAC is computed.

- If the AS field is not set to either "Initialize/Finalize" or "Finalize" and the ICV_TEST bit is set to 1, the Illegal Mode error will be generated except for CICV-only jobs.

Proper AS field settings

Assume that a message has IV, AAD, and textdata and each of these types is split into two sessions (descriptors). The first IV descriptor should have AS set to "Update", the second IV Descriptor should have AS set to "Initialize", both AAD Descriptors and the first textdata descriptor should have AS field set to "Update", and the final Descriptor sets AS to "Initialize/Finalize".

- The Additional Algorithm Information (AAI) field must be set to 90h for GCM to be activated. Setting the DK bit causes an illegal-mode error.
- The Algorithm (ALG) field is used to activate AESA by setting it to 10h.

42.3.9.6 AES GCM mode use of the Context Register

The AES GCM mode uses the Context Register as follows:

- New message processing does not need any data provided in the context. All of the context data is written back by the GCM mode and needs to be restored before the next data chunk is to be processed in the multi-session processing. The final MAC is written in the context dwords 0-1.
- The initial counter value required for encryption/decryption is derived from IV and written to dwords 4-5. It is also required for the MAC computation.
- The incremented counter is placed in dwords 2-3 and is updated with every encrypted/decrypted block.
- Bit sizes of IV, AAD and textdata are required for GHASH computation and are accumulated in dwords 6-7 when multi-session processing is used.

Table 42-13. Context usage in GCM mode

Context DWord	Context-switching definition	Final-result definition
0	MAC[0:63]	MAC[0:63]
1	MAC[64:127]	MAC[64:127]
2	Yi[0:63]	-
3	Yi[64:127]	-
4	Y0[0:63]	-
5	Y0[64:127]	-
6	IV bit size (during GHASH of IV), AAD bit size (during message processing)	-
7	textdata bit size	-

42.3.9.7 AES GCM Mode use of the Data Size Register

The AES GCM mode uses the Data Size Register as follows:

- The byte-length of the message to be processed (including IV, AAD and textdata) must be written to the Data Size register (IV and AAD sizes must include padding to the 16 byte boundary).
- he first write to this register initiates processing. It can also be written during processing in which case the value written will be accumulated to the current state of the register.
- GCM decrements the value in this register with every processed block.
- Message splitting must be done only on a 16-byte boundary.

42.3.9.8 AES GCM mode use of the IV Size Register

The IV Size register is written with the number of bytes in the last IV block. If the total IV size is written, only the low 4 bits are registered. GCM needs this information to determine correct byte size of the IV used in the GHASH computation.

42.3.9.9 AES GCM mode use of the AAD Size Register

The AAD Size register is written with the number of bytes in the last AAD block. If the total AAD size is written, only the low 4 bits are registered. GCM needs this information to determine correct byte size of the AAD used in the GHASH computation.

42.3.9.10 AES GCM mode use of the ICV Size Register

The AES GCM mode uses the ICV Size Register as follows:

- This register is used to provide ICV/MAC byte-size.
- If the ICV mode bit is set, the ICV Size register also determines the number of bytes in the received ICV. Supported values for ICV size are 4 to 16 bytes. If this register is 0, ICV size will be 16 bytes.

42.3.9.11 AES GCM mode use of the Key Register

GCM key must be written to this register; it is always an encryption key.

42.3.9.12 AES GCM mode use of the Key Size Register

The AES GCM mode uses the Key Size Register as follows:

- The total number of key bytes must be written to the Key Size register.
- Any value other than 16, 24, or 32 causes key-size error to be generated.

42.3.9.13 AES GCM mode use of the ICV check

The AES GCM mode uses ICV checking as follows:

- Automatic ICV checking is enabled by setting ICV_TEST bit of the Mode Register to 1. When ICV is set to 1, the AS mode field must be set to either "Finalize" or "Initialize/Finalize"; otherwise the Illegal Mode error is generated except for CICV-only jobs. Also, if ICV = 1, the ENC bit must be 0.
- The received ICV must be provided on the input-data FIFO after the message data. The size of the received and computed ICV is for GCM written to the ICV Size register.
- If the ICV check detects mismatch between the decrypted received ICV and the computed ICV, the ICV error is generated.

42.4 Data encryption standard accelerator (DES) functionality

DES performs encryption and decryption on 64-bit values using the algorithm found in FIPS46-3. The DES module in LTC supports both single- and triple-DES functionality and ECB, CBC, CFB, and OFB modes as well as key parity checking in compliance with the DES specification.

42.4.1 DESA use of the Mode Register

The DESA uses the Mode Register as follows:

- The encryption field (ENC) controls whether DESA is encrypting or decrypting data.
- The Algorithm State (AS) field is not used to affect DESA functionality and should be set to zero at all times.
- The Additional Algorithm Information field (AAI) specifies the mode DESA runs. The supported modes are electronic code book (ECB), cipher block chaining (CBC), cipher feedback (CFB-8), and output feedback (OFB), described as follows:
  - ECB (0x20h) mode is a confidentiality mode that features, for a given key, the assignment of a fixed ciphertext block to each plaintext block (analogous to the assignment of code words in a codebook).

  - CBC (0x10h) mode is a confidentiality mode whose encryption process features the combining ("chaining") of the plaintext blocks with the previous ciphertext blocks. CBC mode requires an IV to combine with the first plaintext block. The IV does not need to be secret, but it must be unpredictable.
  - CFB (0x30h) mode is a confidentiality mode that features the feedback of successive ciphertext segments into the input blocks of the forward cipher to generate output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. The CFB mode requires an IV as the initial input-block.
  - OFB (0x40h) mode is a confidentiality mode that features the iteration of the forward cipher on an IV to generate a sequence of output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. The OFB mode requires that the IV be unique for each execution of the mode under the given key.
- Key parity checking for DESA that checks for odd parity within each byte of the key is enabled with a value of (0x80h) in the AAI field.
- The algorithm field (ALG) must be programmed to DES (0x20h) or 3DES (0x21h).

42.4.2 DESA use of the Key Register

The DESA uses the Key Register as follows:

- The Key Register contains the 8-, 16-, or 24-byte key that is used during permutation in all DES modes.
- The DES specification defines the key as having odd parity in each byte.
- Key parity can be verified using the correct mode setting.

42.4.3 DESA use of the Key Size Register

DESA uses the Key Size Register as follows:

- Key size can be either 8, 16, or 24 bytes.
- A key size of 8 is valid only in single-DES mode.
- Values of 16 and 24 bytes can be used only in triple-DES mode.
- An illegal key size error is generated when in single-DES mode with a key size other than 8 or when in triple-DES mode with a key size other than 16 or 24.

42.4.4 DESA use of the Data Size Register

The DESA uses the Data Size Register as follows:

- The Data Size Register is written with the number of bytes of data to be processed.
- All DES modes except OFB expect to process data that is a multiple of 8 bytes and generates an error if the data size written is not an 8-byte multiple.
- This register must be written to start data processing.
- Because writing to the Data Size Register causes the written value to be added to the previous value in the register, the register may be written multiple times while data is being processed in order to increase the amount of input data that will be processed.

42.4.5 DESA Context Register

The DESA uses the Context Register as follows:

- For CBC, OFB, and CFB modes, the initialization vector is written to and read from the DESA Context Register.
- The value of this register changes as a result of the encryption process and reflects the context of DESA.
- DESA uses the first eight bytes of the Context Register to hold the beginning and final IV value for the CBC, OFB, and CFB modes.

42.4.6 Save and store operations in DESA context data

DESA is able to process data in chunks by saving the intermediate IV from the Context Register after each chunk of data and restoring the IV and key to the correct registers before processing any subsequent chunks of data.

42.5 Public-key hardware accelerator (PKHA) functionality

The PKHA module is capable of performing a number of different operations used in public-key cryptography, including modular arithmetic functions such as addition, subtraction, multiplication, exponentiation, reduction, and inversion, as well as elliptic-curve functions for point addition, point doubling, and point multiplication. All of these functions are provided in both integer and polynomial-binary field versions, except modular subtraction, which is the same as addition for binary polynomials. Most of these

functions can be performed timing-equalized to thwart timing-related side-channel attacks. PKHA also includes a Miller-Rabin primality test function for detecting prime numbers.

The PKHA internally performs modular multiply operations using "Montgomery multiplication". For efficiency, many of these functions have a variant which allows either inputs or outputs in Montgomery form. Some have variants to supply the Montgomery conversion factor. These save time over the variations without. Internally, the PKHA operates on digits of these values. Different versions of the PKHA may have a different digit size. This PKHA has a digit size of 16 bits. This has implications for the inputs and outputs of certain functions. See the discussion on Montgomery arithmetic.

Because the numbers used in public-key cryptography are typically quite large and often referenced many times during a funciton, the inputs to PKHA are loaded into registers. PKHA has four of these labeled A, B, E, and N. A and B are for operands and results. E is for "keys", and N holds the modulus. For ECC functions, A and B are divided up into equal-size quadrants to accommodate the greater number of inputs required.

PKHA also has two other types of functions for manipulating the data in the registers. These are the Clear Memory and Copy Memory functions. The Clear Memory function allows all or any combination of the registers to be overwritten with zeros. The Copy Memory functions can be used to copy data from any of the A, B or N registers or register quadrant to any register A, B, E or N.

PKHA requires that all data for a given function be loaded before the Mode Register is written to invoke a function. This convention indicates to PKHA that all needed data has been loaded, and the function can now be launched. The required data includes:

- PKHA A, B, E and N registers, as required per the function to be executed.
- PKHA A Size, PKHA B Size, PKHA E Size and PKHA N Size, as required.

Note that the PKHA A, B, E and N registers can be accessed only when the Mode Register is not programmed to any PKHA operation. Once the Mode Register contains any PKHA operation value, writes to the PKHA registers will be ignored, and reads will return zero data. After the PKHA operation is complete, the results can be read from the PKHA registers only after the Mode Register is cleared.

42.5.1 PKHA MODE: clear memory function

Table 42-14. PKHA Mode register format for clear memory function

19	18	17	16	11-10	9	8	7	6	5-0
Aram	Bram	Eram	Nram	Reserved	Q3	Q2	Q1	Q0	Function
PKHA_MODE_MS				*PKHA_MODE_LS*					

If the Function field in PKHA MODE specifies the clear memory function, PKHA expects to be in the format shown in Table 42-14. The PKHA RAMs to be cleared may be selected in any combination. Selecting one or more Quadrants for clearing will cause only the specified quadrants (of the specified RAMs) to be cleared. If no Quadrants are selected, then the whole RAM will be cleared.

Table 42-15. PKHA mode register field descriptions for clear memory function

Bits	Description
19	Aram This bit selects the A RAM for zeroization. 0 : A not selected 1 : A selected.
18	Bram This bit selects the B RAM for zeroization. 0 : B not selected 1 : B selected
17	Eram This bit selects the E RAM for zeroization. 0 : E not selected 1 : E selected
16	Nram This bit selects the N RAM for zeroization. 0 : N not selected 1 : N selected
11-10	Reserved
9	Quadrant 3 This bit selects the Quadrant 3 RAM for zeroization. 0 : not selected 1 : selected. Clearing will be only specified quadrant(s). Not valid if E RAM is selected.
8	Quadrant 2 This bit selects the Quadrant 2 RAM for zeroization. 0 : not selected 1 : selected. Clearing will be only specified quadrant(s). Not valid if E RAM is selected.
7	Quadrant 1 This bit selects the Quadrant 1 RAM for zeroization. 0 : not selected 1 : selected. Clearing will be only specified quadrant(s). Not valid is E RAM is selected.
6	Quadrant 0 This bit selects the Quadrant 0 RAM for zeroization.

Table continues on the next page...

Table 42-15. PKHA mode register field descriptions for clear memory function (continued)

Bits	Description
	0 : not selected 1 : selected. Clearing will be only specified quadrant(s). Not valid if E RAM is selected.
5-0	Function The Function value for clearmemory is 000001.

42.5.2 PKHA MODE: Arithmetic Functions

Table 42-16. PKHA Mode Register Format for Arithmetic Functions

19	18	17	16	11	10	9-8	7-6	5-0
inM	outM	F2m	R2	Reserved	Teq	OutSel	Reserved	Function
PKHA_MODE_MS				*PKHA_MODE_LS*				

Table 42-17. PKHA Mode register, format for arithmetic operation

Bits	Description
19 inM	Inputs in Montgomery Format. Indicates whether the inputs are in Montgomery format. If inM=0 : Normal value representation If inM=1 : Montgomery format. (Not valid for all functions.)
18 outM	Outputs in Montgomery format. Indicates whether the outputs are to be left in Montgomery format or converted to normal values. If outM=0 : Normal value representation If outM=1 : Montgomery format. (Not valid for all functions.)
17 F2m	F2m. Indicates whether to use integer or binary polynomial arithmetic in executing the function. If F2m=0 : Integer If F2m=1 : Binary polynomial. (Not valid for all functions.)
16 R2	(R2 mod N). Indicates whether the term (R2 mod N) must be supplied as an input or will be calculated by the routine. If R2=0 : (R^2 mod N) is calculated and applied, if needed If R2=1 : (R^2 mod N) is an input. (Not valid for all functions.)
11 Reserved	Reserved
10 Teq	Timing Equalized. Indicates that a timing equalized version of the function should be executed. If Teq=0 : No timing equalization If Teq=1 : Timing equalization. (Not valid for all functions.)
9-8 OutSel	Output destination select. Indicates which memory should contain the output of the selected function. If OutSel=00b : B

Table continues on the next page...

Table 42-17. PKHA Mode register, format for arithmetic operation (continued)

Bits	Description
	If OutSel=01b : A If OutSel=10b : Reserved If OutSel=11b : Reserved
7-6	Reserved
5-0 Function	Function. Indicates which arithmetic function to execute. If Function=000010b : Modular Addition (A + B) mod N If Function=000011b : Modular Subtraction 1 (A - B) mod N If Function=000100b : Modular Subtraction 2 (B - A) mod N If Function=000101b : Modular Multiplication (A x B) mod N If Function=000110b : Modular Exponentiation A^E mod N If Function=000111b : Modular Reduction A mod N If Function=001000b : Modular Inversion A^{-1} mod N If Function=001001b : ECC Point Add (P1 + P2) If Function=001010b : ECC Point Double (P2 + P2) If Function=001011b : ECC Point Multiply (E x P1) If Function=001110 : Greatest Common Divisor GCD(A,N)-see note below If Function=001111 : Miller-Rabin Primality Test -see note below All other values for this field are currently reserved. **NOTE:** When using the GCD function or any ECC function, a divide-by-zero error occurs if the value of the most significant digit of N is all zeros. **NOTE:** When using the Miller-Rabin primality test function, if the most-significant digit of N is all zeros, the result is composite regardless of the value of N.

NOTE

Note that the arithmetic functions with outputs going to the A RAM are identical to those with outputs going to the B RAM. The only difference is the output destination.

Table 42-18. List of mode values for PKHA Integer Arithmetic Functions

Function name	Brief description	Output reg	Teq	Bits 19-0, including PKHA_MODE and reserved bits[1] (Hex)	Detailed description
MOD_ADD	Integer Modular Addition	B	0	00002	Integer modular addition (MOD_ADD) function
		A	0	00102	

Table continues on the next page...

Table 42-18. List of mode values for PKHA Integer Arithmetic Functions (continued)

Function name	Brief description	Output reg	Teq	Bits 19-0, including PKHA_MODE and reserved bits[1] (Hex)	Detailed description
MOD_SUB_1	Integer modular subtraction (A - B)	B	0	00003	Integer Modular Subtraction (MOD_SUB_1) function
		A	0	00103	
MOD_SUB_2	Integer modular subtraction (B - A)	B	0	00004	Integer Modular Subtraction (MOD_SUB_2) function
		A	0	00104	
MOD_MUL MOD_MUL_TEQ	Integer modular multiplication	B	0	00005	Integer Modular Multiplication (MOD_MUL)
		A	0	00105	
	Timing equalized version	B	1	00405	
		A	1	00505	
MOD_MUL_IM MOD_MUL_IM_TEQ	Integer Modular Multiplication with Montgomery Inputs	B	0	80005	Integer Modular Multiplication with Montgomery Inputs (MOD_MUL_IM)
		A	0	80105	
	Timing equalized version	B	1	80405	
		A	1	80505	
MOD_MUL_IM_OM MOD_MUL_IM_OM_TEQ	Integer Modular Multiplication with Montgomery Inputs and Outputs	B	0	C0005	Integer Modular Multiplication with Montgomery Inputs and Outputs (MOD_MUL_IM_OM) Function
		A	0	C0105	
	Timinq equalized version	B	1	C0405	
		A	1	C0505	
MOD_EXP MOD_EXP_TEQ	Integer Modular Exponentiation	B	0	00006	Integer Modular Exponentiation (MOD_EXP)
		A	0	00106	
	Timing equalized version	B	1	00406	
		A	1	00506	
MOD_EXP_IM MOD_EXP_IM_TEQ	Integer Modular Exponentiation with Montgomery Inputs	B	0	80006	Integer Modular Exponentiation with Montgomery Input (MOD_EXP_IM) Function
		A	0	80106	
	Timing equalized version	B	1	80406	
		A	1	80506	
MOD_AMODN	Integer Modular Reduction	B	0	00007	Integer Modulo Reduction (MOD_AMODN)
		A	0	00107	
MOD_INV	Integer Modular Inversion	B	0	00008	Integer Modular Inversion (MOD_INV)
		A	0	00108	
MOD_R2	Integer R^2 mod N	B	0	0000C	Integer Montgomery factor computation (MOD_R2)
		A	0	0010C	
MOD_GCD	Integer Greatest Common Divisor	B	0	0000E	Integer Greatest Common Divisor (MOD_GCD)
		A	0	0010E	
PRIME_TEST	Miller_Rabin primality test	B	0	0000F	Miller_Rabin primality test (PRIME_TEST)
		A	0	0010F	

1. PKHA_MODE_MS concatenated with 0h concatenated with PKHA_MODE_LS

Arithmetic functions on a binary polynomials (characterestic two) (F2M). All operate in polynomial basis.

Table 42-19. List of mode values for PKHA Binary Polynomial Arithmetic Functions

Function name	Brief description	Output reg	Teq	Bits 19-0, including PKHA_MODE and reserved bits[1] (Hex)	Detailed description
F2M_ADD	Binary Polynomial Modular Addition	B	0	20002	Binary Polynomial (F_{2m}) addition (F2M_ADD) function
		A	0	20102	
F2M_MUL F2M_MUL_TEQ	Binary Polynomial Modular Multiplication	B	0	20005	Binary Polynomial (F2m) Modular Multiplication (F2M_MUL)
		A	0	20105	
	Timing equalized version	B	1	20405	
		A	1	20505	
F2M_MUL_IM F2M_MUL_IM_TEQ	Binary Polynomial Modular Multiplication with Montgomery Inputs	B	0	A0005	Binary Polynomial (F_{2m}) modular multiplication with Montgomery inputs (F2M_MUL_IM) Function
		A	0	A0105	
	Timing equalized version"	B	1	A0405	
		A	1	A0505	
F2M_MUL_IM_OM F2M_MUL_IM_OM_TEQ	Binary Polynomial Modular Multiplication with Montgomery Inputs and Output	B	0	E0005	Binary Polynomial (F_{2m}) Modular Multiplication with Montgomery Inputs And outputs (F2M_MUL_IM_OM) Function
		A	0	E0105	
	Timing equalized version	B	1	E0405	
		A	1	E0505	
F2M_EXP F2M_EXP_TEQ	Binary Polynomial Modular Exponentiation	B	0	20006	Binary Polynomial (F_{2m}) Modular Exponentiation (F2M_EXP)
		A	0	20106	
	Timing equalized version	B	1	20406	
		A	1	20506	
F2M_AMODN	Binary Polynomial Modular Reduction	B	0	20007	Binary Polynomial (F_{2m}) modulo reduction (F2M_AMODN)
		A	0	20107	
F2M_INV	Binary Polynomial Modular Inversion	B	0	20008	Binary Polynomial (F_{2m}) modular inversion (F2M_INV)
		A	0	20108	
F2M_R2	Binary Polynomial R^2 mod n	B	0	2000C	Binary Polynomial (F_2m) R^2 mod N (F2M_R2) Function
		A	0	2010C	
F2M_GCD	Binary Polynomial Greatest Common Divisor	B	0	2000E	Binary Polynomial (F_{2m}) Greatest Common Divisor (F2M_GCD) Function
		A	0	2010E	

1. PKHA_MODE_MS concatenated with 0h concatenated with PKHA_MODE_LS

Elliptic Curve Functions over a prime field (ECC_MOD), where prime p > 3.

Table 42-20. List of mode values for Prime Field (F_p) Elliptic Curve Arithmetic Functions

Function name	Brief description	Output reg	Teq	Bits 19-0, including PKHA_MODE and reserved bits[1] (Hex)	Detailed description
ECC_MOD_ADD	ECC prime field point add - affine coordinates	B	0	00009	ECC F_p Point Add - Affine Coordinates (ECC_MOD_ADD) Function
		A	0	00109	
ECC_MOD_ADD_R2	ECC prime field point add - affine coordinates, R2 input	B	0	10009	ECC F_p Point Add - Affine Coordinates, R2modN Input, (ECC_MOD_ADD_R2) Function
		A	0	10109	
ECC_MOD_DBL	ECC prime field point double - affine coordinates	B	0	0000A	ECC F_p Point Double - Affine Coordinates (ECC_MOD_DBL) Function
		A	0	0010A	
ECC_MOD_MUL ECC_MOD_MUL_TEQ	ECC prime field point multiply - affine coordinates	B	0	0000B	ECC F_p Point Multiply - Affine Coordinates (ECC_MOD_MUL) Function
		A	0	0010B	
	Timing equalized version	B	1	0040B	
		A	1	0050B	
ECC_MOD_MUL_R2 ECC_MOD_MUL_R2_TEQ	ECC prime field point multiply - affine coordinates, r2 mod n input	B	0	1000B	ECC F_p Point Multiply with R2modN Input - Affine Coordinates (ECC_MOD_MUL_R2) Function
		A	0	1010B	
	Timing equalized version	B	1	1040B	
		A	1	1050B	

1. PKHA_MODE_MS concatenated with 0h concatenated with PKHA_MODE_LS

Elliptic Curve Functions over a binary field (ECC_F2M). All operate in polynomial basis.

Table 42-21. List of mode values for Binary Field (F_{2^m}) Elliptic Curve Arithmetic Functions

Function name	Brief description	Output reg	Teq	Bits 19-0, including PKHA_MODE and reserved bits[1] (Hex)	Detailed description
ECC_F2M_ADD	ECC binary field point add - affine coordinates	B	0	20009	ECC F_{2^m} Point Add - Affine Coordinates (ECC_F2M_ADD) Function
		A	0	20109	
ECC_F2M_ADD_R2	ECC binary field point add - affine coordinates, R2 input	B	0	30009	ECC F_{2^m} Point Add - Affine Coordinates, R2modN Input (ECC_F2M_ADD_R2) Function
		A	0	30109	
ECC_F2M_DBL	ECC binary field point double - affine coordinates	B	0	2000A	ECC F_{2^m} Point Double - Affine Coordinates (ECC_F2M_DBL) Function
		A	0	2010A	
ECC_F2M_MUL ECC_F2M_MUL_TEQ	ECC binary field point multiply - affine coordinates	B	0	2000B	ECC F_{2^m} Point Multiply - Affine Coordinates (ECC_F2M_MUL) Function
		A	0	2010B	
	Timing equalized version	B	1	2040B	
		A	1	2050B	
ECC_F2M_MUL_R2 ECC_F2M_MUL_R2_TEQ	ECC binary field point multiply - affine coordinates, r2 mod n input	B	0	3000B	ECC F_{2^m} Point Multiply with R2modN Input- Affine Coordinates (ECC_F2M_MUL_R2) Function
		A	0	3010B	
	Timing equalized version	B	1	3040B	
		A	1	3050B	

1. PKHA_MODE_MS concatenated with 0h concatenated with PKHA_MODE_LS

These functions are grouped here because they do not fall into one of the previous categories of PKHA functions.

42.5.3 PKHA MODE: copy memory functions

Table 42-22. PKHA Mode register, format for copy memory functions

19-17	16	11-10	9-8	7-6	5-0
Source Register	Destination Register		Source Segment	Destination Segment	Function

Table continues on the next page...

Table 42-22. PKHA Mode register, format for copy memory functions (continued)

PKHA_MODE_MS	*PKHA_MODE_LS*

Table 42-23. PKHA Mode register, field descriptions for copy memory functions

Bits	Description
19-17 Source Register	Source Register. Specifies the register to be copied from. If Source Register=000 : A If Source Register=001 : B If Source Register=011 : N All other values are currently reserved.
16 Destination Register 11-10	Destination Register. Specifies the register to be copied to. If Destination Register=000 : A If Destination Register=001 : B If Destination Register=010 : E If Destination Register=011 : N All other values are currently reserved. **NOTE:** The source register and destination register fields must not be the same.
9-8 Source Segment	Source Segment. Used when copying a register segment to specify which segment in the source register to copy from. If Source Segment=00 : Segment 0 If Source Segment=01 : Segment 1 If Source Segment=10 : Segment 2 If Source Segment=11 : Segment 3 **NOTE:**
7-6 Destination Segment	Destination Segment. Used when copying a register segment to specify which segment in the Destination Register to copy to. If Destination Segment=00 : Segment 0 If Destination Segment=01 : Segment 1 If Destination Segment=10 : Segment 2 If Destination Segment=11 : Segment 3 **NOTE:** These bits must be zero when E is the destination register.
5-0 Function	Function. Indicates which copy function to execute. If Function=010000 : Copy Memory N-Size (copies the same number of words as are in the modulus.) If Function=010001 : Copy Memory SRC-Size (copies the number of words specified in the source's size register)

This table gives the encodings from memory-to-memory copy. The top encoding in each cell is for Copy memory, N-Size (COPY_NSZ), the second is for Copy memory, source-size (COPY_SSZ)

The encoding is bits 19-0, including PKHA_MODE (i.e. PKHA_MODE_MS concatenated with 0h concatenated with PKHA_MODE_LS) and reserved bits. (Hex)

Table 42-24. Mode values for PKHA copy memory functions

	Destination Memory			
Source Memory	**A**	**B**	**N**	**E**
A		00410 00411	00C10 00C11	00810 00811
B	20010 20011		20C10 20C11	20810 20811
N	60010 60011	60410 60411		60810 60811

This table gives the encodings from memory-to-memory copy when segments are involved. The top encoding in each cell is for Copy memory, N-Size (COPY_NSZ), the second is for Copy memory, source-size (COPY_SSZ)

The encoding is bits 19-0, including PKHA_MODE and reserved bits [1] (Hex)

Table 42-25. Mode values for PKHA copy memory by segment functions

	Destination Quadrant											
Source Quadrant	**A0**	**A1**	**A2**	**A3**	**B0**	**B1**	**B2**	**B3**	**N0**	**N1**	**N2**	**N3**
A0					00410 00411	00450 00451	00490 00491	004D0 004D1	00C10 00C11	00C50 00C51	00C90 00C91	00CD0 00CD1
A1					00510 00511	00550 00551	00590 00591	005D0 005D1	00D10 00D11	00D50 00D51	00D90 00D91	00DD0 00DD1
A2					00610 00611	00650 00651	00690 00691	006D0 006D1	00E10 00E11	00E50 00E51	00E90 00E91	00ED0 00ED1
A3					00710 00711	00750 00751	00790 00791	007D0 007D1	00F10 00F11	00F50 00F51	00F90 00F91	00FD0 00FD1
B0	20010 20011	20050 20051	20090 20091	200D0 200D1					20C10 20C11	20C50 20C51	20C90 20C91	20CD0 20CD1
B1	20110 20111	20150 20151	20190 20191	201D0 201D1					20D10 20D11	20D50 20D51	20D90 20D91	20DD0 20DD1
B2	20210 20211	20250 20251	20290 20291	202D0 202D1					20E10 20E11	20E50 20E51	20E90 20E91	20ED0 20ED1
B3	20310 20311	20350 20351	20390 20391	203D0 203D1					20F10 20F11	20F50 20F51	20F90 20F91	20FD0 20FD1
N0	60010 60011	60050 60051	60090 60091	600D0 600D1	60410 60411	60450 60451	60490 60491	604D0 604D1				
N1	60110 60111	60150 60151	60190 60191	601D0 601D1	60510 60511	60550 60551	60590 60591	605D0 605D1				
N2	60210 60211	60250 60251	60290 60291	602D0 602D1	60610 60611	60650 60651	60690 60691	606D0 606D1				

Table continues on the next page...

Table 42-25. Mode values for PKHA copy memory by segment functions (continued)

	Destination Quadrant											
Source Quadrant	A0	A1	A2	A3	B0	B1	B2	B3	N0	N1	N2	N3
N3	60310 60311	60350 60351	60390 60391	603D0 603D1	60710 60711	60750 60751	60790 60791	607D0 607D1				

1. PKHA_MODE_MS concatenated with 0h concatenated with PKHA_MODE_LS

42.5.4 Modular math

Almost all math operations require with a modulus value in the N Memory. Math operations involving multiplication (multiplication, exponentiation, prime test, and ECC functions) are performed internally using Montgomery values.

42.5.5 About Montgomery values

The PKHA contains a Modular Arithmetic Unit. Multiplication is always modular multiplication:

$A * B \bmod N$.

The PKHA performs this computation with a Montgomery multiplier. A Montgomery multiplier can be more efficient than a multiply-then-reduce calculation because the modular reduction is done as part of the multiplication and the working product never gets larger than the modulus. In a normal multiplication, the product, before reduction, would be the size of the sum of the factors, so usually twice the size of the modulus. The factors in a Montgomery multiplication each have an R factor, and, as part of the multiplication and modular reduction, one R is removed. Thus, the computation performed is:

$(AR * BR) / R \bmod N$.

The equivalent of "division by R" occurs even if one of the inputs does not have an R factor.

A number of PKHA functions accept inputs in Montgomery form instead of normal values. Some instead take $R^2 \bmod N$ as an input. These functions can be faster than their normal-value alternatives if several operations are performed in a row or if these values are known in advance. This is because, before being used, ($R^2 \bmod N$ needs to be computed and) normal values need to be converted internally to Montgomery form.

The Montgomery form of a value is *value*R* mod *N*, referred to here as *value*. The term $R = 2^{SD}$ is the Montgomery factor, where D is the digit size (of a digit in the PKHA arithmetic unit), in bits, and S is the minimum number of digits needed to hold the value in N. R is therefore dependent on N and D.

To use the PKHA to convert a normal value to a Montgomery value, one must first compute (or know) R^2 mod *N*, the Montgomery Conversion Factor. The following steps can be used to convert a value from a normal value into its Montgomery form (A and B inputs may be reversed):

R^2 = MOD_R2(*N*)

A = MOD_MUL_IM_OM(*A*, B=R^2, *N*)

The equivalent F2M function can be used for binary polynomial values.

Eventually, the value needs to be converted out of Montgomery form. This can be done by performing another multiply (R^2 is not needed for this).

A = MOD_MUL_IM_OM(A=A, B=1, N)

Another method is to cause the PKHA to perform a multiplication and conversion to normal form. Internally, there are two multiplications: first the two inputs, then the product by one.

AB mod N = MOD_MUL_IM(A=A, B=B, N)

A third method is to have just one factor (either one) in Montgomery form:

AB mod N = MOD_MUL_IM_OM(A=A, B=B, N)

The following operations can be used to convert a value from a normal value into its Montgomery form (A and B inputs may be reversed):

The equivalent F2M functions can be used for binary polynomial values.

It is possible to add and subtract Montgomery values, if *R* mod *N* is the same. Do not mix and match Montgomery and normal values for addition or subtraction. 5 + 3R => *5/R + 3R* or *5/R + 3*; neither is likely the desired result.

42.5.6 Non-modular Math

Although addition, subtraction, and multiplication functions require a modulus, it is possible to perform these calculations without any reduction: the modulus must be larger than the expected result.

For addition and subtraction, this is easily done. For multiplication, the MOD_MUL function may be used, but it is not the most efficient, as internally first R^2 mod N will be computed, then two multiplications will be performed (first to convert one factor into Montgomery, then to compute the product, not in Montgomery).

For non-modular multiplication, MUL_IM_OM is much more efficient, as only one multiplication will be performed. This can be used if the factors are not in Montgomery form, i.e., if the product to be calculated is *A*B* instead of *A*B mod N*. Since the multiplier always "divides by *R*', a special modulus value in Nram is required which will make *R* have the value 1. This is done by creating a modulus *N = R-1* so that *R mod N* will have the value one. This way, normal values are the same as Montgomery values; no conversion is necessary and the multiplier will quietly "divide by one" to no effect.

As an example, on a PKHA with a digit size of 32 bits and a product which will be no more than six bytes long, $R = 2^{SD} = 2^{2*32} = 2^{64}$. Therefore the modulus must be 0xFFFFFFFFFFFFFFFF.

For computation with binary polynomials, the equivalent F2M functions may be used.

42.5.7 Elliptic-Curve Math

The PKHA provides point math operations on elliptic curves. These include the ability to add two points (+ operator), double a point, and multiply a point by an integer (scalar) value (x operator).

The input points are assumed to be valid points on the curve. If non-point coordinates or invalid curve parameters are used an input, then a non-point set of coordinates are likely to be returned as output.

The same minimum-value restriction for the modulus exists for Elliptic Curve math as exist for Modular operations. The maximum modulus is 512 bits (64 bytes) in length, or one quadrant.

If xx is the Point at Infinity, *P*and *Q* are points on the curve, and *j* and *k* are integers, then the following identities, as well as others easily derived by taking advantage of associative and commutive properites, hold:

- $P + Q = Q + P$
- $P = xx + P$
- $xx = 0 \times P$
- $(j + k)P = (j \times P) + (k \times P)$

There may be times when the negative of a point is necessary:

- When subtracting points P_A - P_B
- When multiplying by a negative integer: -abs(k) x P_A

To subtract, one can negate the second term and perform an addition, i.e.

$P_C = P_A - P_B = P_A + (-P_{B)}$

When multiplying by a negative value, one can either negate the starting point or the ending point. The multiplication value is the absolute value of the scalar, i.e., when *k* is negative

$P_C = k \times P_A = -abs(k) \times P_A = abs(k) \times (-1P_{A)} = -(abs(k) \times P_A)$

42.5.7.1 Point math over a prime field (F_p)

The ECC_MOD family of functions perform Add, Double, and scalar Multiply operations on points on a curve defined by the equation:

$E: y^2 = x^3 + ax + b \bmod p$

where p is the a prime integer > 3. These operations are available in Affine Coordinates (*x*,*y*).

The modulus (value in N memory) for these operations is *p*, also referred to as *q*.

The equality for the negative of a point *P*, in affine coordinates, is $-P = -(x,y) = (x, -y)$

The operations will not provide useful outputs if the inputs are not valid points on the curve, i.e., if they are not solutions to the curve equation E.

42.5.7.2 Point math over a binary field (F_{2^m})

The ECC_F2M family of functions perform add, double, and scalar multiply operations on points on a curve defined by the equation:

E: $y^2 + xy = x^3 + ax^2 + b$

These operations are available in Affine Coordinates (*x*,*y*). All inputs and output values of polynomial values are in polynomial basis. For example, x^5+x+1 is represented as 23h

The modulus (value in N memory) for these functions is *q*, the field-defining irreducible polynomial for the curve. Other documents use other symbols, including *p(t)*, *f(t)*, and *f*.

The equality for the negative of a point, in affine coordinates, is $-P = -(x,y) = (x, x+y)$.

The operations will not provide useful outputs if the inputs are not valid points on the curve, i.e., if they are not solutions to the curve equation E.

Because of the way the point operations are performed over a binary field, these functions require as an input the value *c* rather than *b*. The relationship between these two values is:

$b = c^4 \bmod q$

and

$c = b^{2^{m-2}} \bmod q$, where *m* is the degree (the power of its highest-power term) of *q*.

This *c* value is referred to as *b'* in the ECC Public-Key protocols for ECDSA sign, and so on. The calculation of *c* is expensive, so it is obviously an advantage to calculate it only once or have it precomputed. See Special values for common ECC domains for these values for common ECC domains.

42.5.7.3 About the Point at Infinity

The point at infinity is a possible result for point math operations. Knowing its representation is important for programming, though the PIZ bit in Operation Status Register can be used to determine when the result of an operation is the point at infinity.

The representation of the point at infinity, in affine coordinates, depends upon the type of curve and the value of the *b* term of the curve's equation:

- For F_p curves, where *b* is equal to 0: (0, 1)
- For F_p and F_{2^m} curves, where *b* is not equal to 0: (0, 0)

42.5.8 PKHA Mode Register

The following tables list the valid PKHA_MODE values for all PKHA functions:

PKHA Clear Memory Functions: Table 42-27

PKHA Modular Arithmetic functions: Table 42-18

PKHA Copy Memory functions: Table 42-24

NOTE

Use of any PKHA_MODE value not listed in these tables results in an invalid mode error.

42.5.9 PKHA functions

The various PKHA functions are described in the following subsections. The following information applies to all PKHA functions.

- Mode Register bits that may be either 1's or 0's for the given function are represented with *x*.
- For convenience, in all the descriptions below the output is shown as the default B, although the actual output destination can be specified via the Class 1 Mode Register[OutSel] field to be either the B RAM or the A RAM.
- For each PKHA function, the specified mode bits are in the Class 1 Mode Register[PKHA_MODE_LS] field.
- For all of the PKHA functions, the Class 1 Mode Register[PKHA_MODE_MS] field is set to 8h.
- The descriptions specify the output register(s) and any other registers that might be modified. Note that the default output register is still modified but the output is placed into the specified destination register(s).
- Note that any parameter underlined is in Montgomery form (for example, $\underline{A}$ = AR mod N).
- Errors reported by PKHA are written to the Job Ring Output Status Register and termination status word (Job termination status/error codes). They are encoded in the ERRID field.
- Three flags in the CCB Status Register may be set by PKHA: PIZ, PIO, and PRM. These flags can be tested by the JUMP (HALT) command They are
  - PIZ is set to indicate that PKHA generated a result equal to zero, or, in the case of ECC functions, the point at infinity.
  - PIO is set whenever a GCD routine finds that the Greatest Common Denominator of two numbers is the number 1. For other general non-ECC functions, it means that the result is equal to one. This may also be referred to as the GCD flag.
  - PRM is set by the PRIME_TEST routine if it finds that a candidate integer is probably prime (that is, passes the Miller-Rabin primality test).
- It is important to note that the PKHA mathematical functions work in terms of "digits"; that is, the arithmetic unit is pipelined to work on a digit of data at a time. For PKHA-32 a digit = 32 bits (4 bytes) of data, for PKHA-64 a digit = 64 bits (8 bytes), and for PKHA-128 a digit = 128 bits (16 bytes). Therefore, the term 'digit' refers to 32, 64, or 128 bits of data in the input and/or output values used by the PKHA arithmetic unit.

42.5.9.1 Clear Memory (CLEAR_MEMORY) function

This function clears the specified registers or quadrants of registers in the PKHA. This includes the A, B, N and E. All registers or quadrants of registers are written with zeros.

A detailed description may be found in PKHA MODE: clear memory function.

Table 42-26. CLEAR_MEMORY function properties

Property	Notes
Mode value	*ABEN*_0000_00 *QQ_QQ* 00_0001, with the following restrictions on the combinations of ABEN and QQQQ: At least one of ABEN must be on. If E is on, all Q must be zero. Some example encodings are in the table below.
Input	None
Output	A = 0, B = 0, E = 0, N = 0, or some quadrant(s) thereof, as specified by ABEN and QQQQ. Each *Q* specifies a quadrant, in order from 3 through 0.
Requirements	The Mode Register specifies which registers or quadrants of registers to clear. If no quadrants are selected, then all quadrants of the specified register(s) are cleared.
Side effects	None
Errors reported	Invalid Mode, if no registers are selected, or E with one or more quadrants is selected
Flags set	None

Table 42-27. Example mode values for PKHA clear memory functions

Function name	Register selects				Quadrant selects				Brief description	Bits 19-0, including PKHA_MODE and reserved bits[1] (Hex)
	A	B	E	N	3	2	1	0		
CLEAR_MEMORY	1	1	1	1	0	0	0	0	Clear registers A, B, E, N	F0001
	1	1	1	0	0	0	0	0	Clear registers A, B, E	E0001
	1	1	0	1	0	0	0	0	Clear registers A, B, N	D0001
	1	0	1	0	0	0	0	0	Clear registers A, E	A0001
	1	0	0	1	0	0	0	0	Clear registers A, N	90001
	0	1	0	1	0	0	0	0	Clear registers B, N	50001
	0	1	0	0	0	0	0	0	Clear register B	40001
	0	0	1	0	0	0	0	0	Clear register E	20001
	0	0	0	1	0	0	0	0	Clear register N	10001
	1	0	0	0	1	1	0	0	Clear quadrants 2 and 3 of register A	80301
	0	1	0	1	0	0	0	1	Clear quadrant 0 of registers B, N	50041
	1	1	0	0	1	0	0	0	Clear quadrant 3 of registers A, B	C0201

1. PKHA_MODE_MS concatenated with 0h concatenated with PKHA_MODE_LS

42.5.9.2 Integer modular addition (MOD_ADD) function

Table 42-28. MOD_ADD function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_0010
Input	• N = modulus and data size, any integer • A = first addend, any integer less than N • B = second addend, any integer less than N
Output	B (or A, if selected) = (A + B) mod N
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • A and B are each < N.
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • A Size Error is set if the size of A is greater than size of N. • B Size Error is set if the size of B is greater than size of N. If (A + B) >= N, N will be subtracted just once from the sum. That is, if (A + B) >= 2N, then the result will not be mod N.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.3 Integer Modular Subtraction (MOD_SUB_1) function

Modular subtraction can be described as follows. If A ≥ B or A = B = 0, then B = A - B. Otherwise, if A < B, then B = A + N - B. The result is always positive and less than N.

Table 42-29. MOD_SUB_1 function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_0011
Input	• N = modulus, any integer • A = minuend, any integer less than N • B = subtrahend, any integer less than N
Output	B (or A, if selected) = (A - B) mod N
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • A and B are less than N.
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • A Size Error is set if the size of A is greater than size of N. • B Size Error is set if the size of B is greater than size of N.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.4 Integer Modular Subtraction (MOD_SUB_2) function

Table 42-30. MOD_SUB_2 function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_0100
Input	• N = modulus, any integer • B = minuend, any integer less than or equal to N • A = subtrahend, any integer less than or equal to N
Output	B (or A, if selected) = (B - A) mod N
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • A and B are < N
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • A Size Error is set if the size of A is greater than size of N. • B Size Error is set if the size of B is greater than size of N.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.5 Integer Modular Multiplication (MOD_MUL)

The (AB) mod N computation is provided to assist in algorithms and protocols where a single modular multiplication is required and not as a chaining of multiplications. In the latter case, Montgomery format multiplication routines (that is, MOD_MUL_IM or MOD_MUL_IM_OM) are more efficient. This function first computes R^2 mod N, then multiples one factor to produce AR, then multiplies AR*B to produce AB.

Table 42-31. MOD_MUL function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_0101
Input	• N = modulus, any odd integer • A = multiplicand, any integer less than N • B = multiplier, any integer less than N
Output	B (or A, if selected) = (AxB) mod N
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • A and B are < N.
Side effects	A and E are modified.
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even. • A Size Error is set if the size of A is greater than size of N.

Table continues on the next page...

Table 42-31. MOD_MUL function properties (continued)

Property	Notes
	• B Size Error is set if the size of B is greater than size of N. • Divide-By-Zero Error is set if the most significant digit of the modulus is all zeros.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.6 Integer Modular Multiplication with Montgomery Inputs (MOD_MUL_IM)

This function takes its inputs, integers, in Montgomery form, multiplies them modulo the value in the N register and returns the result as a field value. To do this, it performs two multiplications: AR*BR => ABR and ABR*1 => AB.

Table 42-32. MOD_MUL_IM function properties

Property	Notes
Mode value	1000_0000_000*x*_0000_0101
Input	• N = modulus, any odd integer • A = multiplicand, a value in Montgomery format • B = multiplier, a value in Montgomery format
Output	B (or A if selected) = A x B mod N, the non-Montgomery product of the inputs
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • A and B are less than modulus N
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even. • A Size Error is set if the size of A is greater than size of N. • B Size Error is set if the size of B is greater than size of N.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.7 Integer Modular Multiplication with Montgomery Inputs and Outputs (MOD_MUL_IM_OM) Function

This function performs the calculation A*B/R mod N, where R is the Montgomery factor for N. This can be used in several ways:

- If one value is a normal value, and the other is R2 mod N, then the result is the normal value converted to Montgomery.

- If A and B are both Montgomery values, then the result is the product of A and B as a Montgomery value.
- If only one of (A,B) is a Montgomery value, then the result is the product as a normal value.
- If one of (A,B) is a Montgomery value and the other is the value one, then the result is Montgomery value converted to a normal value.

Table 42-33. MOD_MUL_IM_OM function properties

Property	Notes
Mode value	1100_0000_000*x*_0000_0101
Input	• N = modulus, any odd integer • A = multiplicand, an integer 0 ≤ A < N • B = multiplier, an integer 0 ≤ B < N
Output	B (or A, if selected) = (AxB) mod N
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even. • A Size Error is set if the size of A is greater than size of N. • B Size Error is set if the size of B is greater than size of N.
Flags set	PIZ is set if the result is zero.

42.5.9.8 Integer Modular Exponentiation (MOD_EXP)

This function is commonly used to perform a single-step RSA operation. It computes R^2 mod N and converts A to Montgomery form before beginning the exponentiation.

Table 42-34. MOD_EXP function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_0110
Input	• N = modulus, any odd integer • A = an integer 0 ≤ A < N • E = exponent, any integer
Output	B (or A, if selected) = (A^E) mod N, a an integer 0 ≤ A < N
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • Maximum key (exponent) size = 256 bytes • A < N
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even. • Key Size Error is set if size of E = 0 or size of E > 256. • A Size Error is set if the size of A is greater than size of N.

Table continues on the next page...

Table 42-34. MOD_EXP function properties (continued)

Property	Notes
Flags set	PIZ is set if the result is zero.

42.5.9.9 Integer Modular Exponentiation, Timing Equalized (MOD_EXP_TEQ) Function

MOD_EXP_TEQ performs the same operation as Integer Modular Exponentiation (MOD_EXP) but with an added timing equalization security feature. Its exponentiation run-time, for a given modulus and size of exponent, is constant.

42.5.9.10 Integer Modular Exponentiation with Montgomery Input (MOD_EXP_IM) Function

The input data (base) to be exponentiated must be provided in the Montgomery format. That is $\underline{A}$ = AR (mod N), where R is the Montgomery constant). The result will be returned in the output in normal integer (non-Montgomery) representation.

Table 42-35. MOD_EXP_IM function properties

Property	Notes
Mode value	1000_0000_000*x*_0000_0110
Input	• N = modulus, any odd integer • A = a value 0 ≤ A < N, in Montgomery format • E = exponent, any integer (normal integer representation)
Output	B (or A, if selected) = (A^E) mod N
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • Maximum key (exponent) size = 256 bytes • A < N
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even. • Key Size Error is set if size of E = 0 or size of E > 256. • A Size Error is set if the size of A is greater than size of N.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.11 Integer Modular Exponentiation with Montgomery Input, Timing Equalized (MOD_EXP_IM_TEQ) Function

MOD_EXP_IM_TEQ performs the same operation as Integer Modular Exponentiation with Montgomery Input (MOD_EXP_IM) Function but with an added timing equalization security feature. Its computation run-time, for a given modulus and size of exponent, is constant.

42.5.9.12 Integer Modulo Reduction (MOD_AMODN)

A and N can be of any size and it is not required that A > N, but N must be non-zero. This function computes the remainder of A divided by N.

Table 42-36. MOD_AMODN function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_0111
Input	• N = modulus, any non-zero integer • A = any integer
Output	B (or A, if selected) = A mod N, A reduced modulo N
Requirements	• N = non-zero value • Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Divide By Zero Error is set if N = 0.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.13 Integer Modular Inversion (MOD_INV)

If the modulus, N, is prime, then all values of A, 1 ≤ A < N, are guaranteed to have an inverse mod N. If N is not prime, A may or may not have an inverse. It will have one only if GCD(A, N) == 1.

Table 42-37. MOD_INV function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_1000
Input	• N = modulus, any non-zero integer • A = any non-zero integer lass than N
Output	B (or A, if selected) = A^{-1} mod N, an integer, the multiplicative inverse of A

Table continues on the next page...

Table 42-37. MOD_INV function properties (continued)

Property	Notes
Requirements	• Neither A or N can be zero. • A must be less than N. • Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes
Side effects	A and E are modified.
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • A Size Error is set if the size of A is greater than size of N. • Divide-By-Zero Error is set if N or A = 0, or if the most significant digit of N = 0, or if there is no inverse.
Flags set	None

42.5.9.14 Integer Montgomery factor computation (MOD_R2)

This function is used to compute a constant to assist in converting operands into the Montgomery residue system representation. The constant $R^2 \pmod N$ is dependent upon the digit size of the PKHA and the value in N.

MUL, EXP, and ECC functions which do not have "IM" (Montgomery inputs) or an R2 input will internally invoke this routine to determine the constant and do the conversions before other operations.

If the modulus N is a protocol- or system-wide parameter that does not change frequently, such as in ECC operations for a specific curve, save this computed constant, because this routine takes a not-insignificant amount of time to complete.

Table 42-38. MOD_R2 function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_1100
Input	N = modulus, any odd integer
Output	B (or A, if selected) = R2 mod N, where R = 2^{SD} where S is size of a digit in bits and D is the number of digits of N; in other words, D = ceiling [sizeof(N) in bits / S]
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even.
Flags set	None

42.5.9.15 Integer Greatest Common Divisor (MOD_GCD)

Table 42-39. MOD_GCD function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_1110
Input	• N = any integer. The most-significant digit of N must be non-zero. • A = any integer less than or equal to N
Output	B (or A, if selected) = GCD(A,N), an integer less than or equal to A that divides both A and N
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • A and N may not both be zero
Side effects	A is modified
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • A Size Error is set if the size of A is greater than size of N. • Divide-By-Zero Error is set if N or A = 0, or if the most significant digit of N = 0.
Flags set	PIO is set if the result is 1.

42.5.9.16 Miller_Rabin primality test (PRIME_TEST)

Table 42-40. PRIME_TEST function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_1111
Input	• N[1] = Candidate prime integer • A = An initial random seed for the base value of exponentiation; can be any integer 2 < A < N - 2 • B = "t" parameter, which is the number of trial runs. By default, it is set at 1 or B[7:0], whichever is bigger. Only the lowest byte of the supplied value is used.
Output	B (or A, if selected) = 1 if candidate is believed to be prime, otherwise 0
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • A and N may not both be zero
Side effects	N and A are modified
Errors reported	• N Size Error is set if size of N = 0 or size of N > 256. • B Size Error is set if B[7:5] is nonzero and N size > 128 • Divide-By-Zero Error is set if no seed can be found that is in the legal range of 2 < A < N-2. This occurs if N = 1 or N = 3
Flags set	PRM is set if the candidate is believed to be prime

1. If the most significant digit of N is zero, the result is always composite, the output is the value zero, and the PRM flag is not set, regardless of the primality of the value of N.

42.5.9.17 Binary Polynomial (F_{2m}) addition (F2M_ADD) function

This function performs binary polynomial modular addition without any modulo reduction, as the value in the N register is ignored. Only its size is used, to determine the size of the result.

This type of addition is the equivalent of a bitwise XOR and this function may be used for that purpose.

This function could as easily be labeled F2M_SUB, as it is mathematically equivalent.

Table 42-41. F2M_ADD function properties

Property	Notes
Mode value	0010_0000_000*x*_0000_0010
Input	• Size of N (modulus size) • A = first addend, a binary polynomial • B = second addend, a binary polynomial
Output	B (or A, if selected) = A xor B, a binary polynomial
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • The N need not be written, because its contents are ignored, but the size of N must be written. This size is needed because inputs A and B are considered binary polynomials modulo some irreducible polynomial N.
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • A Size Error is set if the size of A is greater than size of N. • B Size Error is set if the size of B is greater than size of N.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.18 Binary Polynomial (F2m) Modular Multiplication (F2M_MUL)

The (AB) mod N computation is provided to assist in algorithms and protocols where a single modular multiplication is required and not as a chaining of multiplications. In the latter case, Montgomery format multiplication routines (that is, F2M_MUL_IM or F2M_MUL_IM_OM) are more efficient. This function first computes R^2 mod N, then multiples $A*R^2$ to produce AR, then multiplies AR*B to produce AB.

Table 42-42. F2M_MUL function properties

Property	Notes
Mode value	0010_0000_000*x*_0000_0101
Input	• N = modulus, an irreducible polynomial • A = multiplicand, a field element • B = multiplier, a field element

Table continues on the next page...

Table 42-42. F2M_MUL function properties (continued)

Property	Notes
Output	B (or A, if selected) = (AB) mod N, a field element
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • A and B are field elements modulo N.
Side effects	A and E are modified.
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even. • A Size Error is set if the size of A is greater than size of N. • B Size Error is set if the size of B is greater than size of N.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.19 Binary Polynomial (F_{2m}) modular multiplication with Montgomery inputs (F2M_MUL_IM) Function

This function takes its inputs, binary polynomials, in Montgomery form, multiplies them modulo the value in the N register, used as a reduction polynomial, and returns the result as a field value. To do this, it performs two multiplications: AR*BR => ABR and ABR*1 => AB.

Table 42-43. F2M_MUL_IM function properties

Property	Notes
Mode value	1010_0000_000*n*_0000_0101
Input	• N = modulus, an "odd" binary polynomial of order m • A = multiplicand, a binary polynomial < 2^m, in Montgomery format • B = multiplicand, a binary polynomial < 2^m, in Montgomery format
Output	B (or A, if selected) = (AxB) mod N, a a binary polynomial < 2^m, non-Montgomery format
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • A and B are field elements in Montgomery format and must be modulo reduced by irreducible polynomial N.
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even. • A Size Error is set if the size of A is greater than size of N. • B Size Error is set if the size of B is greater than size of N.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.20 Binary Polynomial (F_{2m}) Modular Multiplication with Montgomery Inputs And outputs (F2M_MUL_IM_OM) Function

This function performs the calculation A*B/R mod N, where R is the Montgomery factor for N. This can be used in several ways:

- If one value is a normal value, and the other is R2 mod N, then the result is the normal value converted to Montgomery.
- If A and B are both Montgomery values, then the result is the product of A and B as a Montgomery value.
- If only one of (A,B) is a Montgomery value, then the result is the product as a normal value.
- If one of (A,B) is a Montgomery value and the other is the value one, then the result is Montgomery value converted to a normal value.

Table 42-44. F2M_MUL_IM_OM function properties

Property	Notes
Mode value	1110_0000_000*x*_0000_0101
Input	• N = modulus, an "odd" binary polynomial of order m • A = a binary polynomial 0 < 2^m • B = a binary polynomial 0 < 2^m
Output	B (or A, if selected) = (AxB) mod N, in Montgomery format
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • A and B are field elements in Montgomery format.
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even. • A Size Error is set if the size of A is greater than size of N. • B Size Error is set if the size of B is greater than size of N.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.21 Binary Polynomial (F_{2m}) Modular Exponentiation (F2M_EXP)

This function is similar to MOD_EXP but works on binary polynomials. It is provided mainly to assist in the computation of elliptic curve parameter "c", where c = $b^{2^{m-2}} \bmod n$) given an elliptic curve parameter "b" and the field-defining polynomial in N. It computes R^2 mod N and converts A to Montgomery form before beginning the exponentiation.

Table 42-45. F2M_EXP function properties

Property	Notes
Mode value	0010_0000_000*x*_0000_0110
Input	• N = modulus, an "odd" binary polynomial of order m • A = a binary polynomial < 2^m • E = exponent, any integer
Output	B (or A, if selected) = (A^E) mod N, a binary polynomial
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • Maximum key (exponent) size = 256 bytes
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even. • Key Size Error is set if size of E = 0 or size of E > 256. • A Size Error is set if the size of A is greater than size of N.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.22 Binary Polynomial (F_{2m}) Modular Exponentiation, Timing Equalized (F2M_EXP_TEQ) Function

F2M_EXP_TEQ performs the same operation as Binary Polynomial (F_{2m}) Modular Exponentiation (F2M_EXP) but with an added timing equalization security feature. Its exponentiation run-time, for a given modulus and size of exponent, is constant.

Table 42-46. F2M_EXP_TEQ function properties

Property	Notes
Mode value	0010_0000_010*x*_0000_0110
Input	• N = modulus, an "odd" binary polynomial of order m • A = a binary polynomial 0 ≤ A < N • E = exponent, any integer
Output	B (or A, if selected) = (A^E) mod N, a binary polynomial field element
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • Maximum key (exponent) size = 256 bytes
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even. • Key Size Error is set if size of E = 0 or size of E > 256. • A Size Error is set if the size of A is greater than size of N.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.23 Binary Polynomial (F_{2m}) modulo reduction (F2M_AMODN)

A and N can be of any size, and it is not required that A > N, but N must be non-zero. This is the equivalent of the MOD_AMODN routine applied to binary polynomials.

Table 42-47. F2M_AMODN function properties

Property	Notes
Mode value	0010_0000_000*x*_0000_0111
Input	• N = modulus, any non-zero polynomial /> • A = any polynomial
Output	B (or A, if selected) = A mod N, a polynomial, binary element modulo N
Requirements	• N = non-zero value • Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Divide By Zero Error is set if N = 0.
Flags set	PIZ is set if the result is zero. PIO is set if the result is one.

42.5.9.24 Binary Polynomial (F_{2m}) modular inversion (F2M_INV)

Table 42-48. F2M_INV function properties

Property	Notes
Mode value	0010_0000_000*x*_0000_1000
Input	• N = modulus, an irreducible polynomial • A = a field element
Output	B (or A, if selected) = A^{-1} mod N, a field element, the multiplicative inverse of A
Requirements	• A is an element of the binary polynomial field. • Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes
Side effects	A and E are modified.
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even. • A Size Error is set if the size of A is greater than size of N. • Divide-By-Zero Error is set if N or A = 0, or if the most significant digit of N = 0.
Flags set	None

42.5.9.25 Binary Polynomial (F_2m) R^2 mod N (F2M_R2) Function

This function is used to compute the Montgomery Conversion Factor, which is used to convert operands into the Montgomery residue system representation. The constant R^2(mod N) is dependent upon the digit size of the PKHA and the value of N. If this value is not available, then this routine (function) is called to determine the constant before other operations. If N contains a protocol- or system-wide parameter that does not change frequently, such as in ECC operations for a specific curve, save this computed constant, because this routine takes a considerable amount of time to complete.

Table 42-49. F2M_R2 function properties

Property	Notes
Mode value	0010_0000_000*x*_0000_1100
Input	N = modulus, an irreducible polynomial
Output	B (or A, if selected) = R2 mod N, where R = 2^{SD} where S is size of a digit in bits and D is the number of digits of an irreducible polynomial, in other words D = ceiling [sizeof(N) in bits / S]
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes
Side effects	None
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • Modulus Even Error is set if N is even.
Flags set	None

42.5.9.26 Binary Polynomial (F_{2m}) Greatest Common Divisor (F2M_GCD) Function

Table 42-50. F2M_GCD function properties

Property	Notes
Mode value	0010_0000_000*x*_0000_1110
Input	• N = any polynomial. The most-significant digit of N must be non-zero. • A = any polynomial with degree less than or equal to N
Output	B (or A, if selected) = BINARY_GCD(A,N), a polynomial with degree less than or equal to polynomial A that divides both A and N
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 256 bytes • A and N may not both be zero
Side effects	A is modified
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 256. • A Size Error is set if the size of A is greater than size of N. • Divide-By-Zero Error is set if N or A = 0, or if the most significant digit of N = 0.
Flags set	PIO is set if the result is 1.

42.5.9.27 ECC F_p Point Add - Affine Coordinates (ECC_MOD_ADD) Function

Table 42-51. ECC_MOD_ADD function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_1001
Input	• N = modulus, a prime number. The most significant digit of N must be non-zero The most significant digit of N must be non-zero • [A0, A1] = first addend in affine coordinates • A2 = ignored • A3 = elliptic curve "a" parameter • B0 = elliptic curve "b" parameter • [B1, B2] = second addend in affine coordinates • B3 = ignored
Output	[B1, B2] (or [A0, A1], if A output selected) = [A0, A1] + [B1, B2], where "+" represents an elliptic curve point addition. Output is in affine coordinates.
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 64 bytes • Point coordinates A0, A1, B1 and B2, and elliptic curve parameters A3 and B0 are elements of the prime field and therefore are less than the modulus N.
Side effects	A0, A1, A2, A3 and B3 are modified.
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 64. • Modulus Even Error is set if N is even. • A Size Error is set if the size of A is greater than size of N. • B Size Error will be set if size of B is greater than size of N. • Divide-By-Zero Error is set if the most-significant digit of N = 0.
Flags set	None

42.5.9.28 ECC F_p Point Add - Affine Coordinates, R2modN Input, (ECC_MOD_ADD_R2) Function

This function is more efficient than (ECC F_p Point Add - Affine Coordinates (ECC_MOD_ADD) Function), which first must compute R^2 mod N

Table 42-52. ECC_MOD_ADD_R2 function properties

Property	Notes
Mode value	0001_0000_000*x*_0000_1001
Input	• N = modulus, a prime number. The most significant digit of N must be non-zero The most significant digit of N must be non-zero • [A0, A1] = first addend point in affine coordinates (x,y) • A2 = ignored • A3 = elliptic curve "a" parameter • B0 = elliptic curve "b" parameter • [B1, B2] = second addend point in affine coordinates (x,y) • B3 = R2 (R^2 mod N) input

Table continues on the next page...

Table 42-52. ECC_MOD_ADD_R2 function properties (continued)

Property	Notes
Output	[B1, B2] (or [A0, A1], if A output selected) = [A0, A1] + [B1, B2], where "+" represents an elliptic curve point addition. Output is in affine coordinates.
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 64 bytes • Point coordinates A0, A1, B1 and B2, and elliptic curve parameters A3 and B0 are elements of the prime field formed by N.
Side effects	A0, A1, A2, A3 and B3 are modified.
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 64. • Modulus Even Error is set if N is even. • A Size Error is set if the size of A is greater than size of N. • B Size Error will be set if size of B is greater than size of N. • Divide-By-Zero Error is set if the most-significant digit of N = 0.
Flags set	None

42.5.9.29 ECC F_p Point Double - Affine Coordinates (ECC_MOD_DBL) Function

Table 42-53. ECC_MOD_DBL function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_1010
Input	• N = modulus, a prime number. The most significant digit of N must be non-zero The most significant digit of N must be non-zero • [A0, A1, A2] = ignored • A3 = elliptic curve "a" parameter • B0 = elliptic curve "b" parameter • [B1, B2] = input point in affine coordinates • B3 = ignored
Output	[B1, B2] (or [A0, A1], if A output selected) = [B1, B2] + [B1, B2], where "+" represents an elliptic-curve point addition. Output is in affine coordinates (x, y).
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 64 bytes • Point coordinates B1 and B2, and elliptic curve parameters A3 and B0 are elements of the prime field formed by N.
Side effects	A0, A2, A3 and B3 are modified.
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 64. • Modulus Even Error is set if N is even. • A Size Error is set if size of A is greater than size of N. • B Size Error is set if size of B is greater than size of N. • Divide-by-Zero Error is set if the most significant digit of N = 0.
Flags set	PIZ is set if the result is the point at infinity.

42.5.9.30 ECC F_p Point Multiply - Affine Coordinates (ECC_MOD_MUL) Function

Table 42-54. ECC_MOD_MUL function properties

Property	Notes
Mode value	0000_0000_000*x*_0000_1011
Input	• N = modulus, a prime number. The most significant digit of N must be non-zero The most significant digit of N must be non-zero • E = scalar multiplier (k), any integer • [A0, A1] = multiplicand, an input point in affine coordinates (x,y) • A2 = ignored • A3 = elliptic curve "a" parameter • B0 = elliptic curve "b" parameter • B1 = ignored • B2 = ignored • B3 = ignored • A0-A3 and B0-B3 are four, equally size segments of A and B memory locations.
Output	• P[B1, B2] (or P[A0, A1], if A output selected) = E x P[A0, A1], where "x" denotes elliptic curve scalar point multiplication. Output is in affine coordinates (x,y). • B0 = undefined • B3 = undefined
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 64 bytes • The point (A0, A1) must be on the elliptic curve formed by (N, A3, B0).
Side effects	A0, A1, A2, A3 and B3 are modified.
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 64. • Key Size Error is set if size of E = 0 or size of E > 256. • Modulus Even Error is set if N is even. • A Size Error is set if size of A is greater than size of N. • B Size Error is set if size of B is greater than size of N. • Divide-by-Zero Error is set if the most significant digit of N = 0.
Flags set	PIZ is set if the result is the point at infinity.

The following special cases should be noted:

- For k = 0, this function returns a point at infinity; that is (0,0) if curve parameter "b" is nonzero and (0,1) otherwise.
- For k < 0, (that is, a negative scalar multiplication is required), its absolute value should be provided to the PKHA; that is, k = abs(-k). After the computation is complete, the formula -P= (x,-y) can be used to compute the "y" coordinate of the effective final result, and other coordinates are the same.

42.5.9.31 ECC F_p Point Multiply - Affine Coordinates, Timing Equalized (ECC_MOD_MUL_TEQ) Function

ECC_MOD_MUL_TEQ performs the same operation as ECC F_p Point Multiply - Affine Coordinates (ECC_MOD_MUL) Function but with an added timing equalization security feature. Its computation run-time is, for a given curve (N, A3, B0), constant for a given size of E.

42.5.9.32 ECC F_p Point Multiply with R2modN Input - Affine Coordinates (ECC_MOD_MUL_R2) Function

This function is more efficient than (ECC F_p Point Multiply - Affine Coordinates (ECC_MOD_MUL) Function), which first must compute R^2 mod N.

Table 42-55. ECC_MOD_MUL_R2 function properties

Property	Notes
Mode value	0001_0000_000*x*_0000_1011
Input	• N = modulus, a prime number. The most significant digit of N must be non-zero The most significant digit of N must be non-zero • E = key, scalar multiplier (k), any integer • [A0, A1] = multiplicand, an input point in affine coordinates (x,y) • A2 = ignored • A3 = elliptic curve "a" parameter • B0 = elliptic curve "b" parameter • B1 = R2 mod N, pre-computed as described in MOD_R2 • B2 = ignored • B3 = ignored • A0-A3 and B0-B3 are four, equally size segments of A and B memory locations.
Output	• P[B1, B2] (or P[A0, A1], if A output selected) = E x P[A0, A1], where "x" denotes elliptic curve scalar point multiplication. Output is in affine coordinates (x,y). • B0 = undefined • B3 = undefined
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 64 bytes • Point coordinates A0 and A1 and elliptic curve parameters A3 and B0 are elements of the prime field formed by the modulus N.
Side effects	A0, A1, A2, A3 and B3 are modified.
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 64. • Key Size Error is set if size of E = 0 or size of E > 256. • Modulus Even Error is set if N is even. • A Size Error is set if size of A is greater than size of N. • B Size Error is set if size of B is greater than size of N. • Divide-by-Zero Error is set if the most significant digit of N = 0.
Flags set	PIZ is set if the result is the point at infinity.

The following special cases should be noted:

- For k = 0, this function returns a point at infinity; that is, (0,0) if curve parameter "b" is nonzero and (0,1) otherwise.
- For k < 0, (that is, a negative scalar multiplication is required), its absolute value should be provided to the PKHA; that is, k = abs(- k). After the computation is complete, the formula -P = (x,-y) can be used to compute the "y" coordinate of the effective final result, and other coordinate is the same.

42.5.9.33 ECC F_p Point Multiply with R2modN Input - Affine Coordinates, Timing Equalized (ECC_MOD_MUL_R2_TEQ) Function

ECC_MOD_MUL_R2_TEQ performs the same operation as ECC F_p Point Multiply with R2modN Input - Affine Coordinates (ECC_MOD_MUL_R2) Function but with an added timing equalization security feature. Its computation run-time is, for a given curve (N, A3, B0), constant for a given size of E.

NOTE

The properties and special cases of ECC_MOD_MUL_R2_TEQ are identical to that of ECC F_p Point Multiply with R2modN Input - Affine Coordinates (ECC_MOD_MUL_R2) Function.

Table 42-56. ECC_MOD_MUL_R2_TEQ function

Property	Notes
Mode value	0001_0000_010*x*_0000_1011

42.5.9.34 ECC F_{2m} Point Add - Affine Coordinates (ECC_F2M_ADD) Function

Table 42-57. ECC_F2M_ADD function properties

Property	Notes
Mode value	0010_0000_000*x*_0000_1001
Input	• N = modulus, an irreducible polynomial. The most significant digit of N must be non-zero. • [A0, A1] = first addend in affine coordinates • A2 = ignored • A3 = elliptic curve "a" parameter • B0 = elliptic curve "c" parameter, where c = $b^{2^{m-2}}$ mod *n* • B1, B2] = second addend in affine coordinates • B3 = ignored
Output	P[B1, B2] (or P[A0, A1], if A output selected) = P[A0, A1] + P[B1, B2], where "+" represents an elliptic curve point addition. Output is in affine coordinates.

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Table 42-57. ECC_F2M_ADD function properties (continued)

Property	Notes
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 64 bytes • Point coordinates A0, A1, B1, and B2 and elliptic curve parameters A3 and B0 are elements of the binary polynomial field N.
Side effects	A0, A1, A2, A3 and B3 are modified.
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 64. • Modulus Even Error is set if N is even. • A Size Error is set if the size of A is greater than size of N. • B Size Error will be set if size of B is greater than size of N. • Divide By Zero Error is set if the most significant digit of N = 0. • C is Zero Error if B3 is zero.
Flags set	None

42.5.9.35 ECC F_{2^m} Point Add - Affine Coordinates, R2modN Input (ECC_F2M_ADD_R2) Function

This function is more efficient than (ECC F_{2^m} Point Add - Affine Coordinates (ECC_F2M_ADD) Function), which first must compute R^2 mod N

Table 42-58. ECC_F2M_ADD_R2 function properties

Property	Notes
Mode value	0011_0000_000*x*_0000_1001
Input	• N = modulus, an irreducible polynomial. The most significant digit of N must be non-zero. • [A0, A1] = first addend in affine coordinates • A2 = ignored • A3 = elliptic curve "a" parameter • B0 = elliptic curve "c" parameter, where c = $b^{2^{m-2}}$ mod *n*. Must not be zero. • [B1, B2] = second addend in affine coordinates • B3 = R2 input
Output	P[B1, B2] (or P[A0, A1], if A output selected) = P[A0, A1] + P[B1, B2], where "+" represents an elliptic curve point addition. Output is in affine coordinates.
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 64 bytes • Point coordinates A0, A1, B1 and B2, and elliptic curve parameters A3 and B0 are elements of the binary polynomial field.
Side effects	A0, A1, A2, A3 and B3 are modified.
Errors reported	• Data Size Error is set if size of N > 64. • Modulus Even Error is set if N is even. • A Size Error is set if the size of A is greater than size of N. • B Size Error will be set if size of B is greater than size of N. • Divide By Zero Error is set if the most significant digit of N = 0. • C is Zero Error if B3 is zero.
Flags set	None

42.5.9.36 ECC F_{2m} Point Double - Affine Coordinates (ECC_F2M_DBL) Function

Table 42-59. ECC_F2M_DBL function properties

Property	Notes
Mode value	0010_0000_000*x*_0000_1010
Input	• N = modulus, an irreducible polynomial. The most significant digit of N must be non-zero. • A0, A1, A2 = ignored • A3 = elliptic curve "a" parameter • B0 = elliptic curve "c" parameter where c = $b^{2^{m-2}}$ mod *n* • [B1, B2] = input point in affine coordinates • B3 = ignored
Output	P[B1, B2] (or P[A0, A1], if A output selected) = P[B1, B2] + P[B1, B2], where "+" represents an elliptic-curve point addition. Output is in affine coordinates.
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 64 bytes • Point coordinates B1 and B2, and elliptic curve parameters A3 and B0 are elements of the binary polynomial field formed by N.
Side effects	A0, A2, A3 and B3 are modified.
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 64. • Modulus Even Error is set if N is even. • A Size Error is set if size of A is greater than size of N. • B Size Error is set if size of B is greater than size of N. • Divide-by-Zero Error is set if the most significant digit of N = 0. • C is Zero Error if B3 is zero.
Flags set	PIZ is set if the result is the point at infinity.

42.5.9.37 ECC F_{2m} Point Multiply - Affine Coordinates (ECC_F2M_MUL) Function

Table 42-60. ECC_F2M_MUL function properties

Property	Notes
Mode value	0010_0000_000*x*_0000_1011
Input	• N = modulus, an irreducible polynomial. The most significant digit of N must be non-zero. • E = key, scalar multiplier (k), any integer • [A0, A1] = multiplicand, an input point in affine coordinates (x,y) • A2 = ignored • A3 = elliptic curve "a" parameter • B0 = elliptic curve "c" parameter where c = $b^{2^{m-2}}$ mod *n* • B1 = ignored • B2 = ignored • B3 = ignored
Output	• P[B1, B2] (or P[A0, A1], if A output selected) = E x P[A0, A1], where "x" denotes elliptic curve scalar point multiplication. Output is in affine coordinates (x,y).

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Table 42-60. ECC_F2M_MUL function properties (continued)

Property	Notes
	• B0 = undefined • B3 = undefined
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 64 bytes (irreducible polynomial of maximum degree 511) • Point coordinates A0 and A1 and elliptic curve parameters A3 and B0 must be elements of the binary polynomial field.
Side effects	A0, A1 and B3 are modified.
Errors reported	• Data Size Error is set if size of N = 0or size of N > 64. • Key Size Error is set if size of E = 0 or size of E > 256. • Modulus Even Error is set if N is even. • A Size Error is set if size of A is greater than size of N. • B Size Error is set if size of B is greater than size of N. • Divide-by-Zero Error is set if the most significant digit of N = 0. • C is Zero Error if B3 is zero.
Flags set	PIZ is set if the result is the point at infinity.

The following special cases should be noted:

- For E = 0, this function returns a point at infinity (0,0).
- For E < 0, (that is, a negative scalar multiplication is required), its absolute value should be provided to the PKHA; that is, `k = -E`). After the multiplication is complete, the formula `-P= (x, x+y)` can be used to compute the y coordinate of the effective final result; the x coordinate stays the same.

42.5.9.38 ECC F_{2m} Point Multiply - Affine Coordinates, Timing Equalized (ECC_F2M_MUL_TEQ) Function

ECC_F2M_MUL_TEQ performs the same operation as ECC F_{2m} Point Multiply - Affine Coordinates (ECC_F2M_MUL) Function but with an added timing equalization security feature. Its computation run-time is, for a given curve (N, A3, B0), constant for a given size of E.

NOTE

The properties of ECC_F2M_MUL_TEQ and its special cases are identical to that of ECC F_{2m} Point Multiply - Affine Coordinates (ECC_F2M_MUL) Function.

42.5.9.39 ECC F_{2^m} Point Multiply with R2modN Input- Affine Coordinates (ECC_F2M_MUL_R2) Function

This function is more efficient than (ECC F_{2^m} Point Multiply - Affine Coordinates (ECC_F2M_MUL) Function), which first must compute R^2 mod N.

Table 42-61. ECC_F2M_MUL_R2 function properties

Property	Notes
Mode value	0011_0000_000*x*_0000_1011
Input	• N = modulus, an irreducible polynomial. The most significant digit of N must be non-zero. • E = key, scalar multiplier (k), any integer • [A0, A1] = multiplicand, an input point in affine coordinates (x,y) • A2 = ignored • A3 = elliptic curve "a" parameter • B0 = elliptic curve "c" parameter where c = $b^{2^{m-2}}$ mod *n* and m = degree of polynomial M • B1 = (f2m) R2 mod N, pre-computed as described in F2M_R2MODN (0Eh) • B2 = ignored • B3 = ignored • A0-A3 and B0-B3 are four, equally size segments of A and B memory locations.
Output	• P[B1, B2] (or P[A0, A1], if A output selected) = E x P[A0, A1], where "x" denotes elliptic curve scalar point multiplication. Output is in affine coordinates (x,y). • B0 = undefined • B3 = undefined
Requirements	• Minimum modulus size = 1 byte • Maximum modulus size = 64 bytes (irreducible polynomial of maximum degree 511) • Point coordinates A0 and A1 and elliptic curve parameters A3 and B0 must be elements of the binary polynomial field.
Side effects	A0, A1, A2, and B3 are modified.
Errors reported	• Data Size Error is set if size of N = 0 or size of N > 64. • Key Size Error is set if size of E = 0 or size of E > 256. • Modulus Even Error is set if N is even. • A Size Error is set if size of A is greater than size of N. • B Size Error is set if size of B is greater than size of N. • Divide-by-Zero Error is set if the most significant digit of N = 0. • C is Zero Error if B3 is zero.
Flags set	PIZ is set if the result is the point at infinity.

The following special cases should be noted:

- For k = 0, this function returns a point at infinity (0,0).
- For k < 0, (that is, a negative scalar multiplication is required), its absolute value should be provided to the PKHA; that is, k = abs(- k). After the computation is complete, the formula -P = (x, x+y) can be used to compute the "y" coordinate of the effective final result, and other coordinate is the same.

42.5.9.40 ECC F_{2^m} Point Multiply with R2modN Input - Affine Coordinates, timing equalized (ECC_F2M_MUL_R2_TEQ) Function

ECC_F2M_MUL_R2_TEQ performs the same operation as ECC F_{2^m} Point Multiply with R2modN Input- Affine Coordinates (ECC_F2M_MUL_R2) Function but with an added timing equalization security feature. Its computation run-time is, for a given curve (N, A3, B0), constant for a given size of E.

Table 42-62. ECC_F2M_MUL_R2_TEQ function

Property	Notes
Mode value	0011_0000_010*x*_0000_1011

42.5.9.41 Copy memory, N-Size (COPY_NSZ)

This function copies the amount of data specified by the N Size register from the specified source register or register quadrant to the specified destination register or register quadrant. The source and destination are specified in the Mode Value. The source can be A, B or N. The destination can be A, B, E or N, but not the same as the source.

In a quadrant copy, when NSZ exceeds the length of a quadrant, the copy will carry on into the next (higher-numbered) quadrant(s).

When the copy operation has completed, the size register for the destination register will be updated to contain the size of the modulus.

Table 42-63. COPY_NSZ function properties

Property	Notes
Mode value	*xxxx*_0000_*xxxx*_*xx*01_0000
Input	None
Output	None
Requirements	N-size Register must contain a valid value
Side effects	Destination register size register is updated to contain N-size.
Errors reported	None
Flags set	None

42.5.9.42 Copy memory, source-size (COPY_SSZ)

This function copies the amount of data specified in the size register for the source register from the specified source register or register quadrant to the specified destination register or register quadrant. The source and destination are specified in the Mode Value. The source can be A, B or N. The destination can be A, B, E or N, but not the same as the source.

In a quadrant copy, when SSZ exceeds the length of a quadrant, the copy will carry on into the next (higher-numbered) quadrant(s).

When the copy operation has completed, the size for the destination register will be updated to contain the source register size.

Table 42-64. COPY_SSZ function properties

Property	Notes
Mode value	*xxxx*_0000_*xxxx*_*xx*01_0001
Input	None
Output	None
Requirements	The size register of the source register must contain a valid value.
Side effects	Destination register size register is updated to contain the source register size.
Errors reported	None
Flags set	None

42.5.10 Special values for common ECC domains

Software can sometimes use the PKHA more effectively if the Montgomery Conversion Factor (R^2 mod N) is either provided or previously used to convert other inputs into Montgomery form. For convenience, the conversion factors for common ECC domains have been computed and published here. Some of the other domain values are provided to aid in definite identification of the domain, in the case that the name is not found or is not an exact match.

The following tables give these values for the *q* and *r* modulus values found in ECC domains. These associated Montgomery values are dependent upon the PKHA digit size (16, 32, 64, 128). These tables are for a PKHA with a 16-bit digit.

ECC F_{2^m} requires a *c* (also called *b′*) parameter for the elliptic curve in place of the *b* value. Table 42-66 provides these values in addition to the Montgomery values. The *b′* values are universal and do not change with PKHA digit size.

The following variable definitions apply to both tables. Variable names (*q, r, b, c*) follow the conventions of IEEE Std 1363.

Name

The names in these tables are associated with, or named in, various published standards. Neither the names nor the domains are guaranteed to be complete. Two values of the domain parameters are provided for purposes of identification.

- Those beginning with "P-", "K-", and "B-" are in FIPS 186 from NIST, found at www.csrc.nist.gov
- Those beginning with "ansix9" are names from ANS X9.62-2005; those beginning with "prime" or "c2pnb" are from an earlier ANSI document
- Those beginning with "sec" are from SEC 2 from the Standards for Efficient Cryptography group, found at www.secg.org
- Those beginning with "wtls" are taken from Wireless Transport Layer Security / Wireless Access Protocol, Version 06-Apr-2001, WAP-261-WTLS-20010406-a. Not all software libraries agree with the mapping of these names to values; care has been taken to identify the values based upon the source documentation.
- Those beginning with "ECDSA", "ECP", "EC2N", "ecp_group", and "Oakley" are from various RFCs found at www.ietf.org
- Those beginning with "GOST" are from the Russian standard GOST R 3410-2001
- Those beginning with "brainpool" are from ECC Brainpool, found at www.ecc-brainpool.org and republished in RFC 5639

R

R is the Montgomery factor. Its value is 2^{SD}, where *D* is the PKHA digit size in bits, and *S* is the minimum number of digits needed to hold the modulus. As an example, for a modulus of nine bytes (72 bits), *R* would be

- 2^{80} for a PKHA with digit size of 16 bits
- 2^{96} for a PKHA with digit size of 32 bits
- 2^{128} for a PKHA with digit size of 64 or 128 bits

q

This is the *field-defining* value for the elliptic curve. For F_p curves, it is the prime number used as the modulus for all point arithmetic; it is named *p* in some other publications. For F_{2^m} curves, it is the irreducible binary polynomial used as the modulus for all point arithmetic. It is not, as usually defined, $q = 2^m$, i.e. the size of the field.

L

This is the number of bytes needed to hold *q* and each of its associated values: *R2modq*, *a*,*b*,*c*, the point coordinates *x* and *y*, the result of an ECDH key agreement, etc.

R2modq

This is $R^2 \bmod q$, the Montgomery Conversion Factor when *q* is the modulus.

r

This is the (usually prime) number which is the order of *G*, the generator point. It is also usually used as the modulus for the non-ECC-related arithmetic in an ECC primitive. This variable is named *n* in some other publications.

N

This is the number of bytes needed to hold *r* and each of its associated values: *R2modr*, private keys, each of the two components of an ECDSA signature, etc.

R2modr

This is R^2 *mod r*, the Montgomery Conversion Factor when *r* is the modulus.

b / c (b')

b is the coefficient for the x^0 (ones) term in an F_{2^m} elliptic curve equation. Its relationship with *c* is $b = c^4$. *c* is sometimes referred to as *b'* in Freescale documentation.

The domains in the table are ordered by size.

Table 42-65. Special Values for common ECC F_p domains when PKHA digit size is 16 bits

Name	L	N	
	var		Value (hex, decimal, sums of powers)
secp112r1	14	14	
wtls6	q		0xDB7C2ABF62E35E668076BEAD208B 4451685225093714772084598273548427
	R2modq		0x00030000000000000000000000
	r		0xDB7C2ABF62E35E7628DFAC6561C5 4451685225093714776491891542548933
	R2modr		0x6A1DD1858198B5BADC6CFD628D0A
secp112r2	14	14	
	q		0xDB7C2ABF62E35E668076BEAD208B 4451685225093714772084598273548427
	R2modq		0x00030000000000000000000000
	r		0x36DF0AAFD8B8D7597CA10520D04B 1112921306273428674967732714786891
	R2modr		0x2C19866CFA502191682A07EBB1DF
wtls8	14	15	
	q		0xFFFFFFFFFFFFFFFFFFFFFFFFDE7 5192296858534827628530496329219559 $2^{112} - 2^9 - 2^4 - 2^3 - 1$
	R2modq		0x00000000000000000000046671
	r		0x0100000000000001ECEA551AD837E9 5192296858534827767273836114360297
	R2modr		0x00E074FD104C86569DB6C204A52932
secp128r1	16	16	

Table continues on the next page...

Table 42-65. Special Values for common ECC F_p domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
	q		0xFFFFFFFDFFFFFFFFFFFFFFFFFFFFFFFF 340282366762482138434845932244680310783 $2^{128} - 2^{97} - 1$
	R2modq		0x00000024000000040000000800000011
	r		0xFFFFFFFE0000000075A30D1B9038A115 340282366762482138443322565580356624661
	R2modr		0x71875047CDD8151626BC6448FADE9BED
secp128r2	16	16	
	q		0xFFFFFFFDFFFFFFFFFFFFFFFFFFFFFFFF 340282366762482138434845932244680310783 $2^{128} - 2^{97} - 1$
	R2modq		0x00000024000000040000000800000011
	r		0x3FFFFFFF7FFFFFFFBE0024720613B5A3 85070591690620534603955721926813660579
	R2modr		0x0EFCA409C09D126A99CD2E9404A3B434
secp160k1 ansix9p160k1	20	21	
	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFEFFFFAC73 1461501637330902918203684832716283019651637554291 $2^{160} - 2^{32} - 2^{14} - 2^{12} - 2^{9} - 2^{8} - 2^{7} - 2^{3} - 2^{2} - 1$
	R2modq		0x0000000000000000000000010000A71A1B44BBA9
	r		0x0100000000000000000001B8FA16DFAB9ACA16B6B3 1461501637330902918203686915170869725397159163571
	R2modr		0x008CCA75EBCDCF2BABDFE44FB4D282030A56ECBB7D
secp160r1 ansix9p160r1 wtls7	20	21	
	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF7FFFFFFF 1461501637330902918203684832716283019653785059327 $2^{160} - 2^{31} - 1$
	R2modq		0x0000000000000000000000040000001000000001
	r		0x0100000000000000000001F4C8F927AED3CA752257 1461501637330902918203687197606826779884643492439
	R2modr		0x00436AB204A0E626837A98A22C8D8455E5563AADF1
secp160r2 ansix9p160r2	20	21	
	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFEFFFFAC73 1461501637330902918203684832716283019651637554291 $2^{160} - 2^{32} - 2^{14} - 2^{12} - 2^{9} - 2^{8} - 2^{7} - 2^{3} - 2^{2} - 1$
	R2modq		0x0000000000000000000000010000A71A1B44BBA9
	r		0x0100000000000000000000351EE786A818F3A1A16B

Table continues on the next page...

Table 42-65. Special Values for common ECC F_p domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
			1461501637330902918203685085371792140653176136043
	R2modr		0x00D68E04EB76E5A181476A1C23DB8912D0E66BA378
wtls9	20	21	
	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFC808F 1461501637330902918203684832716283019655932313743 $2^{160} - 2^{17} - 2^{16} - 2^{14} - 2^{13} - 2^{12} - 2^{11} - 2^{10} - 2^{9} - 2^{8} - 2^{6} - 2^{5} - 2^{4} - 1$
	R2modq		0x0000000000000000000000000000C3C174FE1
	r		0x0100000000000000000001CDC98AE0E2DE574ABF33 1461501637330902918203687013445034429194588307251
	R2modr		0x00519041ADCC3AB9A731EC45CB8499428E993A39C5
brainpoolP160r1	20	20	
	q		0xE95E4A5F737059DC60DFC7AD95B3D8139515620F 1332297598440044874827085558802491743757193798159
	R2modq		0x6CF12F81C0CA7EF8FED717E0B333F8D625BC14FF
	r		0xE95E4A5F737059DC60DF5991D45029409E60FC09 1332297598440044874827085038830181364212942568457
	R2modr		0x2BC73851FC9BE6F69E31FE16FC61D4351FDF90EA
brainpoolP160t1	20	20	
	q		0xE95E4A5F737059DC60DFC7AD95B3D8139515620F 1332297598440044874827085558802491743757193798159
	R2modq		0x6CF12F81C0CA7EF8FED717E0B333F8D625BC14FF
	r		0xE95E4A5F737059DC60DF5991D45029409E60FC09 1332297598440044874827085038830181364212942568457
	R2modr		0x2BC73851FC9BE6F69E31FE16FC61D4351FDF90EA
P-192 secp192r1 ansix9p192r1 prime192v1 ECPRGF192Random	24	24	
	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFEFFFFFFFFFFFFFFFF 6277101735386680763835789423207666416083908700390324961279 $2^{192} - 2^{64} - 1$
	R2modq		0x0000000000000001000000000000000200000000000000001
	r		0xFFFFFFFFFFFFFFFFFFFFFFFF99DEF836146BC9B1B4D22831 6277101735386680763835789423176059013767194773182842284081
	R2modr		0x28BE5677EA0581A24696EA5BBB3A6BEECE66BACCDEB35961
secp192k1 ansix9p192k1	24	24	
	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFEFFFFEE37 6277101735386680763835789423207666416102355444459739541047 $2^{192} - 2^{32} - 2^{12} - 2^{8} - 2^{7} - 2^{6} - 2^{3} - 1$
	R2modq		0x0000000000000000000000000000000100002392013C4FD1

Table continues on the next page...

Table 42-65. Special Values for common ECC F_p domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
	r		0xFFFFFFFFFFFFFFFFFFFFFFFE26F2FC170F69466A74DEFD8D 6277101735386680763835789423061264271957123915200845512077
	R2modr		0x6A21191C2EC4B2B1F0F4F172195E97E2461C1989250F0702
prime192v2	24	24	
	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFEFFFFFFFFFFFFFFFF 6277101735386680763835789423207666416083908700390324961279 $2^{192} - 2^{64} - 1$
	R2modq		0x0000000000000001000000000000000200000000000000001
	r		0xFFFFFFFFFFFFFFFFFFFFFFFE5FB1A724DC80418648D8DD31 6277101735386680763835789423078825936192100537584385056049
	R2modr		0xA4FEB8C277C030E139DA8CFB4E35E1F62814A261001BE8FF
prime192v3	24	24	
	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFEFFFFFFFFFFFFFFFF 6277101735386680763835789423207666416083908700390324961279 $2^{192} - 2^{64} - 1$
	R2modq		0x0000000000000001000000000000000200000000000000001
	r		0xFFFFFFFFFFFFFFFFFFFFFFFF7A62D031C83F4294F640EC13 6277101735386680763835789423166314882687165660350679936019
	R2modr		0x45BCB42FF1CC05D0194D076B366D09BF0305982367330969
brainpoolP192r1	24	24	
	q		0xC302F41D932A36CDA7A3463093D18DB78FCE476DE1A86297 4781668983906166242955001894344923773259119655253013193367
	R2modq		0xB6225126EED34F1033BF484602C3FE69E2474C6972C7B21A
	r		0xC302F41D932A36CDA7A3462F9E9E916B5BE8F1029AC4ACC1 4781668983906166242955001894269038308119863659119834868929
	R2modr		0x98769B9CE772102BBF4AFD5DBF53AFF0B4727C80E407E8F8
brainpoolP192t1	24	24	
	q		0xC302F41D932A36CDA7A3463093D18DB78FCE476DE1A86297 4781668983906166242955001894344923773259119655253013193367
	R2modq		0xB6225126EED34F1033BF484602C3FE69E2474C6972C7B21A
	r		0xC302F41D932A36CDA7A3462F9E9E916B5BE8F1029AC4ACC1 4781668983906166242955001894269038308119863659119834868929
	R2modr		0x98769B9CE772102BBF4AFD5DBF53AFF0B4727C80E407E8F8
P-224 secp224r1 ansix9p224r1 wtls12	28	28	
	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF000000000000000000000001 26959946667150639794667015087019630673557916260026308143510066298881
	R2modq		0x00000000FFFFFFFFFFFFFFFFFFFFFFFE0000000000000000000000001

Table continues on the next page...

Table 42-65. Special Values for common ECC F_p domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
ECPRGF224Random	r		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFF16A2E0B8F03E13DD29455C5C2A3D 26959946667150639794667015087019625940457807714424391721682722368061
	R2modr		0xD4BAA4CF1822BC47B1E979616AD09D9197A545526BDAAE6C3AD01289
secp224k1	28	29	
ansix9p224k1	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFEFFFFE56D 26959946667150639794667015087019630673637144422540572481099315275117 $2^{224} - 2^{32} - 2^{12} - 2^{11} - 2^{9} - 2^{7} - 2^{4} - 2^{1} - 1$
	R2modq		0x0000000000000000000000000000000000000010000352602C23069
	r		0x0100000000000000000000000001DCE8D2EC6184CAF0A971769FB1F7 26959946667150639794667015087019640346510327083120074548994958668279
	R2modr		0x0004DF3DA0993FF72BB882BD88BBFF3BF810C92B3D43C82C98C348E90E
brainpoolP224r1	28	28	
	q		0xD7C134AA264366862A18302575D1D787B09F075797DA89F57EC8C0FF 22721622932454352787552537995910928073340732145944992304435472941311
	R2modq		0x0578FD592E6A6CE43FE8A2AA96AF774C43C20E727867CA8064DCD04F
	r		0xD7C134AA264366862A18302575D0FB98D116BC4B6DDEBCA3A5A7939F 22721622932454352787552537995910923612567546342330757191396560966559
	R2modr		0x4A73A6563211A5611E9CAE249F24919B9399652CADDAF8AA486CA401
brainpoolP224t1	28	28	
	q		0xD7C134AA264366862A18302575D1D787B09F075797DA89F57EC8C0FF 22721622932454352787552537995910928073340732145944992304435472941311
	R2modq		0x0578FD592E6A6CE43FE8A2AA96AF774C43C20E727867CA8064DCD04F
	r		0xD7C134AA264366862A18302575D0FB98D116BC4B6DDEBCA3A5A7939F 22721622932454352787552537995910923612567546342330757191396560966559
	R2modr		0x4A73A6563211A5611E9CAE249F24919B9399652CADDAF8AA486CA401
prime239v1	30	30	
	q		0x7FFFFFFFFFFFFFFFFFFFFFFF7FFFFFFFFFFF8000000000007FFFFFFFFFF 883423532389192164791648750360308885314476597252960362792450860609699839
	R2modq		0x00000000000000000000000500000000005FFFFFFFFFFC000000000008
	r		0x7FFFFFFFFFFFFFFFFFFFFFFF7FFFF9E5E9A9F5D9071FBD1522688909D0B 883423532389192164791648750360308884807550341691627752275345424702807307
	R2modr		0x17789087ABE4B1BE15BDEB5DDB90D9E27D9E8C4D1C2BB940279628B08300
prime239v2	30	30	
	q		0x7FFFFFFFFFFFFFFFFFFFFFFF7FFFFFFFFFFF8000000000007FFFFFFFFFF 883423532389192164791648750360308885314476597252960362792450860609699839

Table continues on the next page...

Table 42-65. Special Values for common ECC F_p domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
	R2modq		0x0000000000000000000000050000000000005FFFFFFFFFFC000000000008
	r		0x7FFFFFFFFFFFFFFFFFFFFFFF800000CFA7E8594377D414C03821BC582063 88342353238919216479164875036030888639268765754699385514776573245129 5331
	R2modr		0x3CB60034F6CF025EBF73DDE8691B5F3A7A21FC865937164FCB06304ACE1E
prime239v3	30	30	
	q		0x7FFFFFFFFFFFFFFFFFFFFFFF7FFFFFFFFFFF8000000000007FFFFFFFFFF 88342353238919216479164875036030888531447659725296036279245086060969 9839
	R2modq		0x0000000000000000000000050000000000005FFFFFFFFFFC000000000008
	r		0x7FFFFFFFFFFFFFFFFFFFFFFF7FFFF975DEB41B3A6057C3C432146526551 88342353238919216479164875036030888477119036976592255051796717105803 4001
	R2modr		0x2441C5CD91500EB94E46F167137CF1B742FF58158145184FF0BE2809E6AD
P-256	32	32	
secp256r1 ansix9p256r1 prime256v1 ECDSA-256 ecp_group_19 ECPRGF256Random	q		0xFFFFFFFF00000001000000000000000000000000FFFFFFFFFFFFFFFFFFFFFFFF 11579208921035624876269744694940757353008614341529031419553363130886 7097853951
	R2modq		0x00000004FFFFFFFDFFFFFFFFFFFFFFFEFFFFFFFBFFFFFFFF0000000000000003
	r		0xFFFFFFFF00000000FFFFFFFFFFFFFFFFBCE6FAADA7179E84F3B9CAC2FC632551 11579208921035624876269744694940757352999695522413576034242225906106 8512044369
	R2modr		0x66E12D94F3D956202845B2392B6BEC594699799C49BD6FA683244C95BE79EEA2
secp256k1	32	32	
ansix9p256k1	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFEFFFFFC2F 11579208923731619542357098500868790785326998466564056403945758400790 8834671663 $2^{256} - 2^{32} - 2^9 - 2^8 - 2^7 - 2^6 - 2^4 - 1$
	R2modq		0x000000000000000000000000000000000000000000000001000007A2000E90A1
	r		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFEBAAEDCE6AF48A03BBFD25E8CD0364141 11579208923731619542357098500868790785283756427907490438260516314151 8161494337
	R2modr		0x9D671CD581C69BC5E697F5E45BCD07C6741496C20E7CF878896CF21467D7D140
brainpoolP256r1	32	32	

Table continues on the next page...

Table 42-65. Special Values for common ECC F_p domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
	q		0xA9FB57DBA1EEA9BC3E660A909D838D726E3BF623D52620282013481D1F6E5377 76884956397045344220809746629001649093037950200943055203735601445031516197751
	R2modq		0x4717AA21E5957FA8A1ECDACD6B1AC8075CCE4C26614D4F4D8CFEDF7BA6465B6C
	r		0xA9FB57DBA1EEA9BC3E660A909D838D718C397AA3B561A6F7901E0E82974856A7 76884956397045344220809746629001649092737531784414529538755519063063536359079
	R2modr		0x0B25F1B9C32367629B7F25E76C815CB0F35D176A1134E4A0E1D8D8DE3312FCA6
brainpoolP256t1	32	32	
	q		0xA9FB57DBA1EEA9BC3E660A909D838D726E3BF623D52620282013481D1F6E5377 76884956397045344220809746629001649093037950200943055203735601445031516197751
	R2modq		0x4717AA21E5957FA8A1ECDACD6B1AC8075CCE4C26614D4F4D8CFEDF7BA6465B6C
	r		0xA9FB57DBA1EEA9BC3E660A909D838D718C397AA3B561A6F7901E0E82974856A7 76884956397045344220809746629001649092737531784414529538755519063063536359079
	R2modr		0x0B25F1B9C32367629B7F25E76C815CB0F35D176A1134E4A0E1D8D8DE3312FCA6
GOSTR3410-CryptoPro-A	32	32	
	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFD97 115792089237316195423570985008687907853269984665640564039457584007913129639319 $2^{256} - 2^9 - 2^6 - 2^5 - 2^3 - 1$
	R2modq		0x000000000000000000000000000000000000000000000000000000005CF11
	r		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF6C611070995AD10045841B09B761B893 115792089237316195423570985008687907853073762908499243225378155805079068850323
	R2modr		0x551FE9CB451179DBF74885D08A3714C6FB07F8222E76DD529AC2D7858E79A469
GOSTR3410-CryptoPro-B	32	32	
	q		0x8000000000000000000000000000000000000000000000000000000000000C99 57896044618658097711785492504343953926634992332820282019728792003956564823193

Table continues on the next page...

Table 42-65. Special Values for common ECC F_p domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
	R2modq		0x0000000000000000000000000000000000000000000000000000000027ACDC4
	r		0x8000000000000000000000000000015F700CFFF1A624E5E497161BCC8A198F 57896044618658097711785492504343953927102133160255826820068844496087732066703
	R2modr		0x09D1D2C4E50824664A2E7E2F6882CF102A3104A7EA43E85529B721F4E6CD7823
GOSTR3410-CryptoPro-C	32	32	
	q		0x9B9F605F5A858107AB1EC85E6B41C8AACF846E86789051D37998F7B9022D759B 70390085352083305199547718019018437841079516630045180471284346843705633502619
	R2modq		0x807A394EDE097652186304212849C07B1017BB39C2D346C5409973B4C427FCEA
	r		0x9B9F605F5A858107AB1EC85E6B41C8AA582CA3511EDDFB74F02F3A6598980BB9 70390085352083305199547718019018437840920882647164081035322601458352298396601
	R2modr		0x7AA61B49A49D4759C67E5D0EE96E8ED304FDA8694AFDA24BE94FAAB66ABA180E
brainpoolP320r1	40	40	
	q		0xD35E472036BC4FB7E13C785ED201E065F98FCFA6F6F40DEF4F92B9EC7893EC28FCD412B1F1B32E27 1763593322239166354161909842446019520889512772719515192772960415288640868802149818095501499903527
	R2modq		0xA259BA4A6C2D92525455A964E614D6D21F4C881F30C5B676C2478A8D906978EF994EE88A743B52F9
	r		0xD35E472036BC4FB7E13C785ED201E065F98FCFA5B68F12A32D482EC7EE8658E98691555B44C59311 1763593322239166354161909842446019520889512772717686063760686124016784784845843468355685258203921
	R2modr		0x31EC87C73200B14FE30D35244E6390FE86B330BCAF86C40991C3001BE0E16805679D29DF2513E4CD
brainpoolP320t1	40	40	
	q		0xD35E472036BC4FB7E13C785ED201E065F98FCFA6F6F40DEF4F92B9EC7893EC28FCD412B1F1B32E27 1763593322239166354161909842446019520889512772719515192772960415288640868802149818095501499903527
	R2modq		0xA259BA4A6C2D92525455A964E614D6D21F4C881F30C5B676C2478A8D906978EF994EE88A743B52F9
	r		0xD35E472036BC4FB7E13C785ED201E065F98FCFA5B68F12A32D482EC7EE8658E98691555B44C59311 1763593322239166354161909842446019520889512772717686063760686124016784784845843468355685258203921

Table continues on the next page...

Table 42-65. Special Values for common ECC F_p domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
	R2modr		0x31EC87C73200B14FE30D35244E6390FE86B330BCAF86C40991C3001BE0E16805679D29DF2513E4CD
P-384 secp384r1 ansix9p384r1 ECDSA-384 ecp_group_20 ECPRGF384Random	48	48	
	q		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFEFFFFFFFF0000000000000000FFFFFFFF 39402006196394479212279040100143613805079739270465446667948293404245721771496870329047266088258938001861606973112319
	R2modq		0x00000000000000000000000000000001000000020000000FFFFFFFE0000000000000200000000FFFFFFFE00000001
	r		0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFC7634D81F4372DDF581A0DB248B0A77AECEC196ACCC52973 39402006196394479212279040100143613805079739270465446667946905279627659399113263569398956308152294913554433653942643
	R2modr		0x0C84EE012B39BF213FB05B7A28266895D40D49174AAB1CC5BC3E483AFCB82947FF3D81E5DF1AA4192D319B2419B409A9
brainpoolP384r1	48	48	
	q		0x8CB91E82A3386D280F5D6F7E50E641DF152F7109ED5456B412B1DA197FB71123ACD3A729901D1A71874700133107EC53 216592707701193161730692368423326049797961163870176486000816185038210899340259618222365619828445340884407084179733331
	R2modq		0x36BF6883178DF842D5C6EF3BA57E052C621401919918D5AF8E28F99CC9940899535283343D7FD965087CEFFF40B64BDE
	r		0x8CB91E82A3386D280F5D6F7E50E641DF152F7109ED5456B31F166E6CAC0425A7CF3AB6AF6B7FC3103B883202E9046565 216592707701193161730692368423326049797961163870176486000756452748216115013585155379626951173689032522296017187239 41
	R2modr		0x0CE8941A614E97C28F886DC965165FDB574A74CB52D748FF2A927E3B9802688A37264E202F2B6B6EAC4ED3A2DE771C8E
brainpoolP384t1	48	48	
	q		0x8CB91E82A3386D280F5D6F7E50E641DF152F7109ED5456B412B1DA197FB71123ACD3A729901D1A71874700133107EC53 216592707701193161730692368423326049797961163870176486000816185038210899340259618222365619828445340884407084179733331
	R2modq		0x36BF6883178DF842D5C6EF3BA57E052C621401919918D5AF8E28F99CC9940899535283343D7FD965087CEFFF40B64BDE
	r		0x8CB91E82A3386D280F5D6F7E50E641DF152F7109ED5456B31F166E6CAC0425A7CF3AB6AF6B7FC3103B883202E9046565 216592707701193161730692368423326049797961163870176486000756452748216115013585155379626951173689032522296017187239 41
	R2modr		0x0CE8941A614E97C28F886DC965165FDB574A74CB52D748FF2A927E3B9802688A37264E202F2B6B6EAC4ED3A2DE771C8E
brainpoolP512r1	64	64	

Table continues on the next page...

Table 42-65. Special Values for common ECC F_p domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
	q		0xAADD9DB8DBE9C48B3FD4E6AE33C9FC07CB308DB3B3C9D20ED6639CCA703308717D4D9B009BC66842AECDA12AE6A380E62881FF2F2D82C68528AA6056583A48F3 89489622076502325516566028151591534221626096440983545113445971872000570104135524399179343041919569427654465303864273459379638943099239285360705341607816947
	R2modq		0x3C4C9D05A9FF6450202E19402056EECCA16DAA5FD42BFF8319486FD8D5898057E0C19A7783514A2553B7F9BC905AFFD3793FB1302715790549AD144A6158F205
	r		0xAADD9DB8DBE9C48B3FD4E6AE33C9FC07CB308DB3B3C9D20ED6639CCA7033087053E5C414CA92619418661197FAC10471DB1D381085DDADDB58796829CA9069 89489622076502325516566028151591534221626096440983545113445971872000570104134185283789817306435249598574513983700292805830942156138820439733543921155441169
	R2modr		0xA794586A718407B095DF1B4C194B2E56723C37A22F16BBDFD7F9CC263B790DE3A6F230C72F0207E83EC64BD033B7627F0886B75895283DDDD2A3681ECDA81671
brainpoolP512t1	64	64	
	q		0xAADD9DB8DBE9C48B3FD4E6AE33C9FC07CB308DB3B3C9D20ED6639CCA703308717D4D9B009BC66842AECDA12AE6A380E62881FF2F2D82C68528AA6056583A48F3 89489622076502325516566028151591534221626096440983545113445971872000570104135524399179343041919569427654465303864273459379638943099239285360705341607816947
	R2modq		0x3C4C9D05A9FF6450202E19402056EECCA16DAA5FD42BFF8319486FD8D5898057E0C19A7783514A2553B7F9BC905AFFD3793FB1302715790549AD144A6158F205
	r		0xAADD9DB8DBE9C48B3FD4E6AE33C9FC07CB308DB3B3C9D20ED6639CCA703308705 53E5C414CA92619418661197FAC10471DB1D381085DDADDB58796829CA9069 89489622076502325516566028151591534221626096440983545113445971872000570104134185283789817306435249598574513983700292805830942156138820439733543921155441169
	R2modr		0xA794586A718407B095DF1B4C194B2E56723C37A22F16BBDFD7F9CC263B790DE3A6F230C72F0207E83EC64BD033B7627F0886B75895283DDDD2A3681ECDA81671

Table 42-66. Special Values for common ECC F_{2^m} domains when PKHA digit size is 16 bits

Name	L	N	
	var		Value (hex, decimal, sums of powers)
sect113r1	15	15	
wtls4	q		0x020000000000000000000000000201 $x^{113} + x^9 + 1$

Table continues on the next page...

Table 42-66. Special Values for common ECC F_{2^m} domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
	R2modq		0x00000000000000000001000040000000
	b		0xE8BEE4D3E2260744188BE0E9C723
	c		0x0173E834AF28EC76CB83BD8DFEB2D5
	r		0x0100000000000000D9CCEC8A39E56F
			5192296858534827689835882578830703
	R2modr		0x002D02609ABE76F866BDCE5B3F9BCC
sect113r2	15	15	
	q		0x02000000000000000000000000201
			$x^{113} + x^9 + 1$
	R2modq		0x00000000000000000001000040000000
	b		0x95E9A9EC9B297BD4BF36E059184F
	c		0x0054D9F03957174A32329167D7FE71
	r		0x01000000000000000108789B2496AF93
			5192296858534827702972497909952403
	R2modr		0x00471CB662E29CB41ABC888E16FF49
wtls1	15	14	
	q		0x02000000000000000000000000201
			$x^{113} + x^9 + 1$
	R2modq		0x00000000000000000001000040000000
	b		0x01
	c		0x00000000000000000000000000001
	r		0xFFFFFFFFFFFFFFFFDBF91AF6DEA73
			5192296858534827627896703833467507
	R2modr		0x000511F09A1AB7E0A600B6A46FA9
sect131r1	17	17	
	q		0x080000000000000000000000000010D
			$x^{131} + x^8 + x^3 + x^2 + 1$
	R2modq		0x00000000000000000000000040144000000
	b		0x0217C05610884B63B9C6C7291678F9D341
	c		0x03DB89B405E491160E3B2F07B0CE20B37E
	r		0x040000000000000000023123953A9464B54D
			136112946768375385389393275568536556065 3
	R2modr		0x03CE363344739BBCD370FB96ADB81025B9
sect131r2	17	17	
	q		0x080000000000000000000000000010D
			$x^{131} + x^8 + x^3 + x^2 + 1$
	R2modq		0x00000000000000000000000040144000000

Table continues on the next page...

Table 42-66. Special Values for common ECC F_{2^m} domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
	b		0x04B8266A46C55657AC734CE38F018F2192
	c		0x07CBB9920D71A48E099C38D71DA6490EB1
	r		0x040000000000000000016954A233049BA98F
			1361129467683753853879535043412812867983
	R2modr		0x02EBB3EA65BB896320D34767E38BE77465
Oakley 3	20	-	
	q		0x080000000000000000000000040000000000000001
			$x^{155} + x^{62} + 1$
	R2modq		0x000000400000000000000000000000000000000400
	b		0x07338F
	c		0x00311000000223A000C4474000088E8000111D1D
B-163	21	21	
ansix9t163r2	q		0x080000000000000000000000000000000000000000C9
sect163r2			$x^{163} + x^7 + x^6 + x^3 + 1$
EC2NGF163Random	R2modq		0x000000000000000000000000000000014104000000
	b		0x020A601907B8C953CA1481EB10512F78744A3205FD
	c		0x072C4E1EF7CB2F3A035D33104294159609138BB404
	r		0x040000000000000000000292FE77E70C12A4234C33
			5846006549323611672814742442876390689256843201587
	R2modr		0x011E0B46683488BE6C9C55E513CB679874C4E0E0B1
K-163	21	21	
ansix9t163k1	q		0x080000000000000000000000000000000000000000C9
sect163k1			$x^{163} + x^7 + x^6 + x^3 + 1$
EC2NGF163Koblitz	R2modq		0x000000000000000000000000000000014104000000
wtls3	b		0x01
	c		0x000000000000000000000000000000000000000001
	r		0x040000000000000000020108A2E0CC0D99F8A5EF
			5846006549323611672814741753598448348329118574063
	R2modr		0x013877C8B9719E20D16A359191E004B3D7105A3DB4
sect163r1	21	21	
ansix9t163r1	q		0x080000000000000000000000000000000000000000C9
			$x^{163} + x^7 + x^6 + x^3 + 1$
	R2modq		0x000000000000000000000000000000014104000000
	b		0x0713612DCDDCB40AAB946BDA29CA91F73AF958AFD9
	c		0x05ED403ED58EB45B1CCECA0F4F61655549861BE052
	r		0x03FFFFFFFFFFFFFFFFFFF48AAB689C29CA710279B
			5846006549323611672814738465098798981304420411291

Table continues on the next page...

Table 42-66. Special Values for common ECC F_{2^m} domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
	R2modr		0x030E95D72BF45AD7608E54BE73B44B4B1C327B65C1
wtls5	21	21	
	q		0x0800000000000000000000000000000000000107 $x^{163} + x^8 + x^2 + x^1 + 1$
	R2modq		0x0000000000000000000000000000040054000000
	b		0xC9517D06D5240D3CFF38C74B20B6CD4D6F9DD4D9
	c		0x0453E1E4B7291F5C2D53CE18483F007081E7EA26EC
	r		0x040000000000000000001E60FC8821CC74DAEAFC1 584600654932361167281474162622639205657383263840 1
	R2modr		0x007218FA96704CFBABEA28DE5A57F5A5C73FE73E87
Oakley 4	24	-	
	q		0x020000000000000000000000000020000000000000000001 $x^{185} + x^{69} + 1$
	R2modq		0x0000000010000000000000000000000000000004000
	b		0x1EE9
	c		0x000000000000300000018000C00C000000638030001C0009
sect193r1	25	25	
ansix9t193r1	q		0x020000000000000000000000000000000000000000008001 $x^{193} + x^{15} + 1$
	R2modq		0x0000000000000000000000000000000010000000040000000
	b		0xFDFB49BFE6C3A89FACADAA7A1E5BBC7CC1C2E5D831478814
	c		0x0167B35EB4313F263D0F7A3D5036F0A0A3C980D40E5A053ED2
	r		0x0100000000000000000000000C7F34A778F443ACC920EBA49 6277101735386680763835789423269548053691575186051040197193
	R2modr		0x00555F659B9F0A6812CD5A09619A2E7446C7F16EDAA6C25C24
sect193r2	25	25	
ansix9t193r2	q		0x020000000000000000000000000000000000000000008001 $x^{193} + x^{15} + 1$
	R2modq		0x0000000000000000000000000000000100000040000000
	b		0xC9BB9E8927D4D64C377E2AB2856A5B16E3EFB7F61D4316AE
	c		0x006989FE6BFE30EDDC3244269F3AAD18D66CF3DB3E3302FAA8
	r		0x0100000000000000000000015AAB561B005413CCD4EE99D5 6277101735386680763835789423314955362437298222279840143829
	R2modr		0x0021EBDCE9B24356750478EA3C9B8611E749E5446745FCDD4F
B-233	30	30	
sect233r1	q		0x020000000000000000000000000000000000000000400000000000000001
ansix9t233r1			$x^{233} + x^{74} + 1$

Table continues on the next page...

Table 42-66. Special Values for common ECC F_{2^m} domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
EC2NGF233Random	R2modq		0x0000000000000000000400000000000000000000000000000000000004000
wtls11	b		0x66647EDE6C332C7F8C0923BB58213B333B20E9CE4281FE115F7D8F90AD
	c		0x0007D5EF4389DFF11ECDBA39C30970D3CE35CEBBA58473F64B4DC0F2686C
	r		0x010000000000000000000000000013E974E72F8A6922031D2603CFE0D7 6901746346790563787434755862277025555839812737345013555379383634485463
	R2modr		0x00405345696AB044AA57CDD6D0CC913DB0DBA856F036B34D7EDB8C1383DC
K-233	30	29	
sect233k1	q		0x020000000000000000000000000000000000000004000000000000000001
ansix9t233k1			$x^{233} + x^{74} + 1$
EC2NGF233Koblitz	R2modq		0x0000000000000000000400000000000000000000000000000000000004000
wtls10	b		0x01
	c		0x000000000000000000000000000000000000000000000000000000000000001
	r		0x800000000000000000000000000069D5BB915BCD46EFB1AD5F173ABDF 3450873173395281893717377931138512760570940988862252126328087024741343
	R2modr		0x193B9A7B59BEBED80293C813EEB5B6D7DB65FF0B4A6545982B006BBF08
sect239k1	30	30	
ansix9t239k1	q		0x800000000000000000004000000000000000000000000000000000000001
			$x^{239} + x^{158} + 1$
	R2modq		0x200000000000000000000000000000000000000800000000000000000004
	b		0x01
	c		0x000000000000000000000000000000000000000000000000000000000000001
	r		0x2000000000000000000000000005A79FEC67CB6E91F1C1DA800E478A5 2208558830972980411979121875928648149482165613217098488874802192153622213
	R2modr		0x1E805199383E8C975E5EA68E20339652293F129E7CF3AB36516F788CE5A5
B-283	36	36	
sect283r1	q		0x0800000000000000000000000000000000000000000000000000000000000000000010A1
ansix9t283r1			$x^{283} + x^{12} + x^7 + x^5 + 1$
EC2NGF283Random	R2modq		0x0000000000000000000000000000000000000000000000000000000000000000401100400
	b		0x027B680AC8B8596DA5A4AF8A19A0303FCA97FD7645309FA2A581485AF6263E313B79A2F5
	c		0x03D8C93D3B0EA81D9294034D7EE3135D0AC5FC8D9CB0276F7211F880F0D81CA4C6E87B38
	r		0x03FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFEF90399660FC938A90165B042A7CEFADB307

Table continues on the next page...

Table 42-66. Special Values for common ECC F_{2^m} domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
			7770675568902916283677847627294075626569625924376904889109196526770044277787378692871
	R2modr		0x0299ADD3FE013DB2E23755FAA9545A49222D8461643773D41D288BCA1EBB695767D7CA78
K-283 sect283k1 ansix9t283k1 EC2NGF283Koblitz	36	36	
	q		0x0800000000000000000000000000000000000000000000000000000000000000000000000010A1 $x^{283} + x^{12} + x^7 + x^5 + 1$
	R2modq		0x0000000000000000000000000000000000000000000000000000000000000000000000401100400
	b		0x01
	c		0x0000000000000000000000000000000000000000000000000000000000000000000000000001
	r		0x01FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFE9AE2ED07577265DFF7F94451E061E163C61 3885337784451458141838923813647037813284811733793061324295874997529815829704422603873
	R2modr		0x00868DB4F6424B4B297831F5EBA11AE2B1AC177F33C6C133859892757E41B7CAE8927BDB
B-409 sect409r1 ansix9t409r1 EC2NGF409Random	52	52	
	q		0x020000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000800000000000000000001 $x^{409} + x^{87} + 1$
	R2modq		0x0000000000000000000000000000000000000000000000000000000000000000000000010000000000000000000000000000000000000000004000
	b		0x21A5C2C8EE9FEB5C4B9A753B7B476B7FD6422EF1F3DD674761FA99D6AC27C8A9A197B272822F6CD57A55AA4F50AE317B13545F
	c		0x0149B8B7BEBD9B63653EF1CD8C6A5DD105A2AAAC36FE2EAE43CF28CE1CB7C830C1ECDBFA413AB07FE35A57811AE4F88D30AC63FB
	r		0x010000000000000000000000000000000000000000000000000001E2AAD6A612F33307BE5FA47C3C9E052F838164CD37D9A21173 66105596879024859895191530803277103982840468296428121928464879830415777482737480520814372376217911096597986728836656752677 1
	R2modr		0x0007C24B27E70A941D4738F415F186A66A9FF8783C798E99D4A152BF0CE0C0CC273CDA3D70AA82C43A336EFBE1479034DB8EF936
K-409 sect409k1 ansix9t409k1 EC2NGF409Koblitz	52	51	
	q		0x020000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000800000000000000000001 $x^{409} + x^{87} + 1$
	R2modq		0x0000000000000000000000000000000000000000000000000000000000000000000000010000000000000000000000000000000000000000004000
	b		0x01

Table continues on the next page...

Table 42-66. Special Values for common ECC F_{2^m} domains when PKHA digit size is 16 bits (continued)

Name	L	N	
	var		Value (hex, decimal, sums of powers)
	c		0x0000000000000000000000000000000000000000000000000000000000000000 0000000000000000000000000000000000000001
	r		0x7FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFE5F83B2D4E A20400EC4557D5ED3E3E7CA5B4B5C83B8E01E5FCF 330527984395124299475957654016385519914202341482140609642324395022880 711289249191050673258457777458014096366590617731358671
	R2modr		0x50DC9B805D4BEBA0701EDA0D529DAD74A3ED9914801EFC3F5D0760180600F3 725B714A1C6E7B3C68A06DF3709E9354226F8D6C

42.6 LTC AES Examples

Example AES ECB Operation:

1. Write key to Primary Key Register.
2. Write key size to Primary Key Size Register.
   - Key Size is 16 bytes (00000010h)
   - Key Size is 24 bytes (00000018h)
   - Key Size is 32 bytes (00000020h)
3. Write Mode to Primary Mode Register. (0010020Dh)
4. Write Size of data to encrypt/decrypt to Data Size Register.
5. Write data into the Input FIFO.
6. Read data from the Output FIFO.
7. Interrupt is generated after final word is pushed to output FIFO.

Example AES CTR Operation:

1. Write key to Primary Key Register.
2. Write key size to Primary Key Size Register.
   - Key Size is 16 bytes (00000010h)
   - Key Size is 24 bytes (00000018h)
   - Key Size is 32 bytes (00000020h)
3. Write initial counter value to Context Words 4-7 in the Context Register.
4. Write Mode to Primary Mode Register. (0010000Dh)
5. Write Size of data to encrypt/decrypt to Data Size Register.
6. Write data into the Input FIFO.
7. Read data from the Output FIFO.
8. Interrupt is generated after final word is pushed to output FIFO.

Example AES CCM or CCM* Operation:

1. Write key to Primary Key Register.
2. Write key size to Primary Key Size Register.
   - Key Size is 16 bytes (00000010h)
   - Key Size is 24 bytes (00000018h)
   - Key Size is 32 bytes (00000020h)
3. Write B0 value to Context Words 0-3 in the Context Register.
4. Write initial counter value to Context Words 4-7 in the Context Register.
5. Write Mode to Primary Mode Register. (0010080Dh) CCM and CCM* both use the same mode value.
   - CCM and CCM* both use the same mode value.
6. Write Size of Authentication Only Data to the AAD Size Register.
7. Write Authentication Only data to the Input FIFO.
   - Authentication data needs to be padded to a 16 byte boundary with zeros.
   - For example if there is 8 bytes of AAD then (00000008h) should be written to AAD Size register and 8 bytes of AAD data followed by 8 bytes of Zero should be written into the Input FIFO.
8. Write Size of data to encrypt/decrypt and authenticate to Data Size Register.
9. Write data into the Input FIFO.
10. Read data from the Output FIFO.
11. Interrupt is generated after final word is pushed to output FIFO.
12. Read MAC from Context Registers
    - MAC is read from Context Registers 0-3.
    - Encrypted MAC is read from Context Registers 8-11.

Example AES CCM or CCM* Authentication Only Operation:

1. Write key to Primary Key Register.
2. Write key size to Primary Key Size Register.
   - Key Size is 16 bytes (00000010h)
   - Key Size is 24 bytes (00000018h)
   - Key Size is 32 bytes (00000020h)
3. Write B0 value to Context Words 0-3 in the Context Register.
4. Write initial counter value to Context Words 4-7 in the Context Register.
5. Write Mode to Primary Mode Register. (0010080Dh).
   - CCM and CCM* both use the same mode value.
6. Write Size of Authentication Only Data to the AAD Size Register.
   - The AL bit needs to be set in the AAD Size Register. This tells the AES core engine that it will recieve only Authentication Data. Note for encryption only the mechanism is handled automatically.
7. Write Authentication Only data to the Input FIFO.

- Authentication data needs to be padded to a 16 byte boundary with zeros.
- For example if there is 8 bytes of AAD then (00000008h) should be written to AAD Size register and 8 bytes of AAD data followed by 8 bytes of Zero should be written into the Input FIFO.

8. Write data into the Input FIFO.
9. Interrupt is generated after final word is processed from input FIFO.
10. Read MAC from Context Registers
    - MAC is read from Context Registers 0-3.
    - Encrypted MAC is read from Context Registers 8-11.

Example AES CCM or CCM* Encryption Only Operation:

1. Write key to Primary Key Register.
2. Write key size to Primary Key Size Register.
    - Key Size is 16 bytes (00000010h)
    - Key Size is 24 bytes (00000018h)
    - Key Size is 32 bytes (00000020h)
3. Write B0 value to Context Words 0-3 in the Context Register.
4. Write initial counter value to Context Words 4-7 in the Context Register.
5. Write Mode to Primary Mode Register. (0010080Dh).
    - CCM and CCM* both use the same mode value.
6. Write Size of data to encrypt/decrypt to Data Size Register.
7. Write data into the Input FIFO.
8. Read data from the Output FIFO.
9. Interrupt is generated after final word is pushed into the output FIFO.

42.7 LTC DES Examples

Example DES ECB Decrypt Operation:

1. Write key to Primary Key Register.
2. Write key size to Primary Key Size Register. (00000008h)
3. Write Mode to Primary Mode Register. (0020020Ch)
4. Write Size of data to encrypt/decrypt to Data Size Register.
5. Write data into the Input FIFO.
6. Read data from the Output FIFO.
7. Interrupt is generated after final word is pushed to output FIFO.

Example 3DES CBC Encrypt Operation:

1. Write key to Primary Key Register.
2. Write key size to Primary Key Size Register.

- Key Size is 16 bytes (00000010h)
- Key Size is 24 bytes (00000018h)

3. Write IV to Context Words 0-1 in the Context Register.
4. Write Mode to Primary Mode Register. (0021010Dh)
5. Write Size of data to encrypt/decrypt to Data Size Register.
6. Write data into the Input FIFO.
7. Read data from the Output FIFO.
8. Interrupt is generated after final word is pushed to output FIFO.

42.8 LTC PKHA Examples

Example PKHA MOD_ADD Operation:

1. Write N size to PKHA N Size Register.
2. Write A Size to PKHA A Size Register.
3. Write B Size to PKHA B Size Register.
4. Write Modulus to PKHA N0 Register.
5. Write first addend to PKHA A0 Register.
6. Write second addend to PKHA B0 Register.
7. Write Mode to Primary Mode Register. (00800002h)
8. Wait for interrupt to indicate 'done'.
9. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register.
10. Read the result of MOD_ADD from PKHA B0 Register.
11. If desired, read LTC Status Register, bits 30 and 29, to check PKZ, PKO flags.

Example PKHA F2M_MUL, result to PKHA A, Operation:

1. Write N size to PKHA N Size Register.
2. Write A Size to PKHA A Size Register.
3. Write B Size to PKHA B Size Register.
4. Write Modulus to PKHA N0 Register.
5. Write first multiplicand to PKHA A0 Register.
6. Write second multiplicand to PKHA B0 Register.
7. Write Mode to Primary Mode Register. (00820105h)
8. Wait for interrupt to indicate 'done'.
9. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register.
10. Read the result of F2M_MUL from PKHA A0 Register.
11. If desired, read LTC Status Register, bits 30 and 29, to check PKZ, PKO flags.

Example PKHA ECC_MOD_MUL Operation:

1. Write N size to PKHA N Size Register.
2. Write A Size to PKHA A Size Register.
3. Write B Size to PKHA B Size Register.
4. Write E Size to PKHA E Size Register.
5. Write Modulus to PKHA N0 Register.
6. Write multiplicand X coordinate to PKHA A0 Register.
7. Write multiplicand Y coordinate to PKHA A1 Register.
8. Write elliptic curve "a" parameter to PKHA A3 Register.
9. Write elliptic curve "b" parameter to PKHA B0 Register.
10. Write scalar multiplier "k" to PKHA E Register.
11. Write Mode to Primary Mode Register. (0080000Bh)
12. Wait for interrupt to indicate 'done'.
13. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register.
14. Read the resulting point X from PKHA B1 Register.
15. Read the resulting point Y from PKHA B2 Register.
16. Read LTC Status Register bit 30, to check PKZ flag. If set, this indicates the result is point at infinity.

Example PKHA MOD_R2 Operation:

1. Write N size to PKHA N Size Register.
2. Write Modulus to PKHA N0 Register.
3. Write Mode to Primary Mode Register. (0080000Ch)
4. Wait for interrupt to indicate 'done'.
5. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register.
6. Read the result of MOD_R2 from PKHA B0 Register. This is R^2modN.

Example PKHA ECC_F2M_MUL_R2_TEQ, result to PKHA A, Operation:

1. Write N size to PKHA N Size Register.
2. Write A Size to PKHA A Size Register.
3. Write B Size to PKHA B Size Register.
4. Write E Size to PKHA E Size Register.
5. Write Modulus to PKHA N0 Register.
6. Write multiplicand X coordinate to PKHA A0 Register.
7. Write multiplicand Y coordinate to PKHA A1 Register.
8. Write elliptic curve "a" parameter to PKHA A3 Register.
9. Write elliptic curve "c" parameter to PKHA B0 Register.
10. Write pre-computed R^2modN to PKHA B1 Register.
11. Write scalar multiplier "k" to PKHA E Register.
12. Write Mode to Primary Mode Register. (0083050Bh)

13. Wait for interrupt to indicate 'done'.
14. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register.
15. Read the resulting point X from PKHA A0 Register.
16. Read the resulting point Y from PKHA A1 Register.
17. Read LTC Status Register bit 30, to check PKZ flag. If set, this indicates the result is point at infinity.

Example PKHA Miller-Rabin Primality Test Operation:

1. Write N size to PKHA N Size Register.
2. Write A Size to PKHA A Size Register.
3. Write B Size to the value 1, to the PKHA B Size Register.
4. Write the prime candidate to PKHA N0 Register.
5. Write the random seed, range (1 < A < N-1) to PKHA A0 Register.
6. Write the number of trials PKHA B0[7:0] Register.
7. Write Mode to Primary Mode Register. (0080000Fh)
8. Wait for interrupt to indicate 'done'.
9. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register.
10. Read the result of the primality test from PKHA B0 Register. It will be "1" if the candidate is believed to be prime, else 0.
11. Alternatively, read LTC Status Register bit 28, to check the PKP flag, which will be set if the candidate is believed to be prime.

Example PKHA Performing ECDSA Sign Protocol.

In this example, a series of operations are run using PKHA to perform ECDSA Signature Generation (Sign). The sequence of operations in this example is:

1. Compute u = Nonce mod r (reduce Nonce random value).
2. Compute h = 1/u mod r.
3. Compute V = u*G, the public key for u.
4. Compute c = V_x mod r.
5. Compute s*c mod r.
6. Compute f + s*c mod r
7. Compute d = (h * (f + s*c)) mod r.

And the PKHA operations to be performed for ECDSA Sign Protocol are:

1. Write size of r to PKHA N Size Register.
2. Write size of Nonce to PKHA A Size Register.
3. Write value r to PKHA N Register.
4. Write the random Nonce value to PKHA A0 Register.

5. Write Mode command for AmodN, result to A, to Primary Mode Register (00800107h). This computes u = Nonce mod r.
6. Wait for interrupt to indicate 'done'.
7. Clear the interrupt by writing 10000h to LTC Status Register. PKHA A now contains u.
8. Write Mode command for COPY NSZ, Source A0, Destination N2, to Primary Mode Register (00800C90h). This saves u in PKHA N2.
9. Wait for interrupt to indicate 'done'.
10. Clear the interrupt by writing 10000h to LTC Status Register. PKHA N2 now contains u.
11. Write Mode command for MOD_INV to Primary Mode Register (00800008h). This computes h = 1/u mod r.
12. Wait for interrupt to indicate 'done'.
13. Clear the interrupt by writing 10000h to LTC Status Register. The also clears the Primary Mode Register. PKHA B now contains h.
14. Read the value h from PKHA B0 Register and save it for later use. The size of h is the r size, so this determines the number of bytes to read.
15. Write size of q to PKHA N Size Register.
16. Write value q to PKHA N Register.
17. Write size of q to PKHA A Size Register.
18. Write value a to PKHA A3 Register.
19. Write value G_x to PKHA A0 Register.
20. Write value G_y to PKHA A1 Register.
21. Write Mode command for COPY NSZ, Source N2, Destination B0, to Primary Mode Register (00800610h).
22. Wait for interrupt to indicate 'done'.
23. Clear the interrupt by writing 10000h to LTC Status Register. PKHA B0 now contains u.
24. Write Mode command for COPY NSZ, Source B, Destination E, to Primary Mode Register (00820810h).
25. Wait for interrupt to indicate 'done'.
26. Clear the interrupt by writing 10000h to LTC Status Register. PKHA E now contains u.
27. Write value b to PKHA B0 Register.
28. Write Mode command for ECC_MOD_MUL_TEQ to Primary Mode Register (0080040Bh), else if this is an F2m domain, the command is ECC_F2M_MUL_TEQ (0082040Bh).
29. Wait for interrupt to indicate 'done'.
30. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA B1/B2 now contain V_x/V_y.

31. Write Mode command for COPY SSZ, Source B1, Destination A0, to Primary Mode Register (00820111h).
32. Wait for interrupt to indicate 'done'.
33. Clear the interrupt by writing 10000h to LTC Status Register. PKHA A0 now contains V_x.
34. Write the size of r to PKHA N Size Register.
35. Write the value r to PKHA N Register.
36. Write Mode command for AmodN to Primary Mode Register (00800007h).
37. Wait for interrupt to indicate 'done'.
38. Clear the interrupt by writing 10000h to LTC Status Register. PKHA B now contains the Signature result c = V_x mod r.
39. Read the value c from PKHA B0 Register and save it as the c result. This size of this value is r size.
40. Write the size of r to PKHA A Size Register.
41. Write the value s (Private Key) to PKHA A0 Register.
42. Write Mode command for MOD_MUL to Primary Mode Register (00800005h).
43. Wait for interrupt to indicate "done".
44. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA B0 now contains (s*c) mod r.
45. Write the size of the message representative "f" to PKHA A Size Register.
46. Write the value f to PKHA A0 Register.
47. Write Mode command for MOD_ADD to Primary Mode Register (00800002h).
48. Wait for interrupt to indicate "done".
49. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA B0 now contains (f + (s*c)) mod r.
50. Write the size of r to PKHA A Size Register.
51. Write the value h (saved earlier) to PKHA A0 Register.
52. Write Mode command for MOD_MUL to Primary Mode Register (00800005h).
53. Wait for interrupt to indicate "done".
54. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA B0 now contains the Signature result d = (h * (f + (s*c))) mod r.
55. Read the value d from PKHA B0 Register and save it as the d result. This size of this value is r size.

Example PKHA Performing ECDSA Verify Protocol.

In this example, a series of operations are run using PKHA to perform ECDSA Verify. The sequence of operations in this example is:

1. Compute h = 1/d mod r.
2. Compute u1 = m*h mod r.
3. Compute u2 = c*h mod r.

4. Compute J = u2*W.
5. Compute K = u1*G.
6. Compute P = u1*G + u2*W.
7. Compute c' = P_x mod r.
8. Compare c' = c, if they match, verification is successful.

And the PKHA operations to be performed for ECDSA Verify Protocol are:

1. Write size of r to PKHA N Size Register.
2. Write size of r to PKHA A Size Register.
3. Write value r to PKHA N Register.
4. Write value d to PKHA A0 Register.
5. Write Mode command for MOD_INV to Primary Mode Register (00800008h).
6. Wait for interrupt to indicate 'done'.
7. Clear the interrupt by writing 10000h to LTC Status Register. PKHA B now contains h = 1/d mod r.
8. Read the value h from PKHA B0 Register and save it for later use. The size of h is the r size, so this determines the number of bytes to read.
9. Write Mode command for CLEAR_MEM A to Primary Mode Register (00880001h). This clears A in case r size > message representative size.
10. Wait for interrupt to indicate 'done'.
11. Clear the interrupt by writing 10000h to LTC Status Register.
12. Write size of m (message representative) to PKHA A Size Register.
13. Write value m to PKHA A0 Register.
14. Write Mode command for MOD_MUL to Primary Mode Register (00800005h).
15. Wait for interrupt to indicate 'done'.
16. Clear the interrupt by writing 10000h to LTC Status Register. PKHA B0 now contains u1 = m*h mod r.
17. Read the value u1 from PKHA B0 Register and save it for later use. The size of u1 is the r size, so this determines the number of bytes to read.
18. Write size of r to PKHA A Size Register.
19. Write value h (saved earlier) to PKHA B0 Register.
20. Write value c to PKHA A0 Register.
21. Write Mode command for MOD_MUL to Primary Mode Register (00800005h).
22. Wait for interrupt to indicate 'done'.
23. Clear the interrupt by writing 10000h to LTC Status Register. PKHA B now contains u2 = c*h mod r.
24. Write Mode command for COPY SSZ, Source B, Destination E, to Primary Mode Register (00820810h).
25. Wait for interrupt to indicate 'done'.
26. Clear the interrupt by writing 10000h to LTC Status Register. PKHA E now contains u2.

27. Write Mode command for CLEAR_MEM A, N to Primary Mode Register (00890001h). This clears A and N in case r size > q size.
28. Wait for interrupt to indicate 'done'.
29. Clear the interrupt by writing 10000h to LTC Status Register.
30. Write size of q to PKHA N Size Register.
31. Write value q to PKHA N Register.
32. Write size of q to PKHA A Size Register.
33. Write value a to PKHA A3 Register.
34. Write size of q to PKHA B Size Register.
35. Write value b to PKHA B0 Register.
36. Write public key x value to PKHA A0 Register.
37. Write public key y value to PKHA A1 Register.
38. Write Mode command for ECC_MOD_MUL, Destination A, to Primary Mode Register (0080010Bh), else if this is an F2m domain, the command is ECC_F2M_MUL, DST A (0082010Bh).
39. Wait for interrupt to indicate 'done'.
40. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA A0/A1 now contain J_x/J_y = u2*W.
41. Read the value J_x from PKHA A0 Register and save it for later use. This size of this value is q size.
42. Read the value J_y from PKHA A1 Register and save it for later use. This size of this value is q size.
43. Write size of r to PKHA E Size Register.
44. Write value u1 (saved earlier) to PKHA E Register.
45. Write value a to PKHA A3 Register.
46. Write value b to PKHA B0 Register.
47. Write G_x value to PKHA A0 Register.
48. Write G_y value to PKHA A1 Register.
49. Write Mode command for ECC_MOD_MUL, Destination A, to Primary Mode Register (0080010Bh), else if this is an F2m domain, the command is ECC_F2M_MUL, DST A (0082010Bh).
50. Wait for interrupt to indicate 'done'.
51. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA A0/A1 now contain K_x/K_y = u1*G.
52. Write size of q to PKHA B Size Register.
53. Write value J_x (saved earlier) to PKHA B1 Register.
54. Write value J_y (saved earlier) to PKHA B2 Register.
55. Write Mode command for ECC_MOD_ADD, Destination A, to Primary Mode Register (00800109h), else if this is an F2m domain, the command is ECC_F2M_ADD, DST A (00820109h).
56. Wait for interrupt to indicate 'done'.

57. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA A0/A1 now contain $P_x/P_y = J + K$.
58. Write size of r to PKHA N Size Register.
59. Write the value r to PKHA N Register.
60. Write Mode command for AmodN to Primary Mode Register (00800007h).
61. Wait for interrupt to indicate 'done'.
62. Clear the interrupt by writing 10000h to LTC Status Register. PKHA B now contains the Verify result $c' = P_x \bmod r$.
63. Write the size of r to PKHA B Size Register.
64. Write the value c to PKHA A0 Register.
65. Write Mode command for F2M_ADD to Primary Mode Register (00820002h).
66. Wait for interrupt to indicate "done".
67. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA B0 now contains zero if the verification is successful.
68. Read the result of the verification from PKHA B0 Register. It will be "0" if the verification is successful.
69. Alternatively, read LTC Status Register bit 30, to check the PKZ flag, which will be set if verification is successful.

Example PKHA Performing RSA Encryption Protocol.

In this example, a series of operations are run using PKHA to perform RSA Encryption from n, e. This is done by computing $g = f^e \bmod n$.

The PKHA operations to be performed for RSA Encryption Protocol are:

1. Write size of n to PKHA N Size Register.
2. Write size of e to PKHA E Size Register.
3. Write size of f (secret) to PKHA A Size Register.
4. Write value n to PKHA N Register.
5. Write value e to PKHA E Register.
6. Write value f to PKHA A0 Register.
7. Write Mode command for MOD_EXP, to Primary Mode Register (00800006h). This computes $g = f^e \bmod n$.
8. Wait for interrupt to indicate 'done'.
9. Clear the interrupt by writing 10000h to LTC Status Register. PKHA B now contains g.
10. Read the value g from PKHA B0 Register and save it as the RSA encrypt result. This size of this value is n size.

Example PKHA Performing RSA Decryption Format 1 (n, d) Protocol.

In this example, a series of operations are run using PKHA to perform RSA Decryption Format 1 (n, d). This is done by computing $f = g^d \bmod n$.

The PKHA operations to be performed for RSA Decryption (n, d) Protocol are:

1. Write size of n to PKHA N Size Register.
2. Write size of d to PKHA E Size Register.
3. Write size of g (encrypted secret) to PKHA A Size Register.
4. Write value n to PKHA N Register.
5. Write value d to PKHA E Register.
6. Write value g to PKHA A0 Register.
7. Write Mode command for MOD_EXP_TEQ, to Primary Mode Register (00800406h). This computes f = g^d mod n.
8. Wait for interrupt to indicate 'done'.
9. Clear the interrupt by writing 10000h to LTC Status Register. PKHA B now contains f.
10. Read the value f from PKHA B0 Register and save it as the RSA decrypt result. This size of this value is n size.

Example PKHA Performing RSA Decryption Format 2 (pqd) Protocol.

In this example, a series of operations are run using PKHA to perform RSA Decryption Format 2 (pqd). The sequence of operations in this example is:

1. Compute d2 = d mod (q - 1).
2. Compute j2 = g^{d2} mod q.
3. Compute d1 = d mod (p - 1).
4. Compute j1 = g^{d1} mod q.
5. Compute h = ((1 / q) * (j1 - j2)) mod p.
6. Compute j = j2 + (h * q)

And the PKHA operations to be performed for RSA Decryption Format 2 (pqd) Protocol are:

1. Write size of q to PKHA N Size Register.
2. Write value q to PKHA N Register.
3. Write Mode command for COPY NSZ, Source N0, Destination A0, to Primary Mode Register (00860010h). This saves q in PKHA A.
4. Wait for interrupt to indicate 'done'.
5. Clear the interrupt by writing 10000h to LTC Status Register. PKHA A now contains q.
6. Write the value 1 to PKHA B Size Register.
7. Write value 1 (one single byte) to PKHA B0 Register.
8. Write Mode command for MOD_SUB_1 to Primary Mode Register (00800003h). This computes q - 1.
9. Wait for interrupt to indicate 'done'.
10. Clear the interrupt by writing 10000h to LTC Status Register. The also clears the Primary Mode Register. PKHA B now contains q - 1.

11. Write Mode command for COPY NSZ, Source B0, Destination N0, to Primary Mode Register (00820C10h). This saves q - 1 in PKHA N.
12. Wait for interrupt to indicate 'done'.
13. Clear the interrupt by writing 10000h to LTC Status Register. PKHA N now contains q - 1.
14. Write size of d to PKHA A Size Register.
15. Write value d to PKHA A Register.
16. Write Mode command for AmodN to Primary Mode Register (00800007h).
17. Wait for interrupt to indicate 'done'.
18. Clear the interrupt by writing 10000h to LTC Status Register. PKHA B0 now contains d2 = d mod (q - 1).
19. Write Mode command for COPY NSZ, Source B, Destination E, to Primary Mode Register (00820810h).
20. Wait for interrupt to indicate 'done'.
21. Clear the interrupt by writing 10000h to LTC Status Register. PKHA E now contains d2.
22. Write value q to PKHA N Register.
23. Write Mode command for CLEAR_MEM A to Primary Mode Register (00880001h), in case size < q size.
24. Wait for interrupt to indicate 'done'.
25. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register.
26. Write the size of g to PKHA A Size Register.
27. Write the value g to PKHA A Register.
28. Write Mode command for AmodN, destination A, to Primary Mode Register (00800107h).
29. Wait for interrupt to indicate 'done'.
30. Clear the interrupt by writing 10000h to LTC Status Register. PKHA A now contains g mod q.
31. Write Mode command for MOD_EXP_TEQ to Primary Mode Register (00800406h).
32. Wait for interrupt to indicate "done".
33. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA B0 now contains j2 = g^{d2} mod q.
34. Read the value j2 from PKHA B0 Register and save it for later use. This size of this value is q size.
35. Write the size of p to PKHA N Size Register.
36. Write the value p to PKHA N Register.
37. Write Mode command for COPY NSZ, Source N0, Destination A0, to Primary Mode Register (00860010h). This saves p in PKHA A.
38. Wait for interrupt to indicate 'done'.

39. Clear the interrupt by writing 10000h to LTC Status Register. PKHA A now contains p.
40. Write Mode command for CLEAR_MEM B to Primary Mode Register (00840001h).
41. Wait for interrupt to indicate 'done'.
42. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register.
43. Write the value 1 to PKHA B Size Register.
44. Write value 1 (one single byte) to PKHA B0 Register.
45. Write Mode command for MOD_SUB_1 to Primary Mode Register (00800003h). This computes p - 1.
46. Wait for interrupt to indicate 'done'.
47. Clear the interrupt by writing 10000h to LTC Status Register. The also clears the Primary Mode Register. PKHA B now contains p - 1.
48. Write Mode command for COPY NSZ, Source B0, Destination N0, to Primary Mode Register (00820C10h). This saves p - 1 in PKHA N.
49. Wait for interrupt to indicate 'done'.
50. Clear the interrupt by writing 10000h to LTC Status Register. PKHA N now contains p - 1.
51. Write size of d to PKHA A Size Register.
52. Write value d to PKHA A Register.
53. Write Mode command for AmodN to Primary Mode Register (00800007h).
54. Wait for interrupt to indicate 'done'.
55. Clear the interrupt by writing 10000h to LTC Status Register. PKHA B0 now contains d1 = d mod (p - 1).
56. Write Mode command for COPY NSZ, Source B, Destination E, to Primary Mode Register (00820810h).
57. Wait for interrupt to indicate 'done'.
58. Clear the interrupt by writing 10000h to LTC Status Register. PKHA E now contains d1.
59. Write value p to PKHA N Register.
60. Write size of g to PKHA A Size Register.
61. Write value g to PKHA A Register.
62. Write Mode command for AmodN, Destination A, to Primary Mode Register (00800107h).
63. Wait for interrupt to indicate "done".
64. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA A now contains g mod p.
65. Write Mode command for MOD_EXP_TEQ to Primary Mode Register (00800406h).
66. Wait for interrupt to indicate "done".
67. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA B0 now contains j1 = g^{d1} mod p.

68. Read the value j1 from PKHA B0 Register and save it for later use. This size of this value is p size.
69. Write the size of q to PKHA A Size Register.
70. Write the value j2 (saved earlier) to PKHA A0 Register.
71. Write Mode command for AmodN to Primary Mode Register (00800007h).
72. Wait for interrupt to indicate "done".
73. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA B0 now contains j2 mod p.
74. If q size > p size, write Mode command for CLEAR_MEM A to Primary Mode Register (00880001h).
75. If q size > p size, wait for interrupt to indicate 'done'.
76. If q size > p size, clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register.
77. Write size of p to PKHA A Size Register.
78. Write value j1 (saved earlier) to PKHA A0 Register.
79. Write Mode command for MOD_SUB_1 to Primary Mode Register (00800003h).
80. Wait for interrupt to indicate "done".
81. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA B0 now contains (j1 - j2) mod p.
82. Read the value (j1 - j2) mod p from PKHA B0 Register and save it for later use. This size of this value is p size.
83. Write size of q to PKHA A Size Register.
84. Write value q to PKHA A0 Register.
85. Write Mode command for AmodN, Destination A, to Primary Mode Register (00800107h).
86. Wait for interrupt to indicate "done".
87. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA A0 now contains q mod p.
88. Write Mode command for MOD_INV to Primary Mode Register (00800008h).
89. Wait for interrupt to indicate "done".
90. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA A0 now contains c = 1/q mod p.
91. Write the value (j1 - j2) mod p (saved earlier) to PKHA A0 Register.
92. Write Mode command for MOD_MUL to Primary Mode Register (00800005h).
93. Wait for interrupt to indicate "done".
94. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register. PKHA B0 now contains h = (c * (j1 - j2)) mod p.
95. Write Mode command for CLEAR_MEM A to Primary Mode Register (00880001h).
96. Wait for interrupt to indicate 'done'.
97. Clear the interrupt by writing 10000h to LTC Status Register. This also clears the Primary Mode Register.

98. Write the value 1 to PKHA A Size Register. This is needed to avoid an error on the next operation which would occur if A size = 0.
99. Write Mode command for COPY NSZ, Source B, Destination A, to Primary Mode Register (00820010h).
10 Wait for interrupt to indicate 'done'.
0.
10 Clear the interrupt by writing 10000h to LTC Status Register. This also clears the
1. Primary Mode Register.
10 Write Mode command for CLEAR_MEM B to Primary Mode Register (00840001h).
2.
10 Wait for interrupt to indicate 'done'.
3.
10 Clear the interrupt by writing 10000h to LTC Status Register. This also clears the
4. Primary Mode Register.
10 Write PKHA N size with the n size, rounded up to the next 8-byte value
5.
10 Write all ones to PKHA N Register, up to the size written in the previous step.
6.
10 Write size of q to PKHA B Size Register.
7.
10 Write the value q to PKHA B Register.
8.
10 Write Mode command for MOD_MUL_IM_OM to Primary Mode Register
9. (008C0005h).
11 Wait for interrupt to indicate "done".
0.
11 Clear the interrupt by writing 10000h to LTC Status Register. This also clears the
1. Primary Mode Register. PKHA B0 now contains h * q.
11 Write Mode command for CLEAR_MEM A to Primary Mode Register (00880001h).
2. This clears leftover bytes in PKHA A Register.
11 Wait for interrupt to indicate 'done'.
3.
11 Clear the interrupt by writing 10000h to LTC Status Register. This also clears the
4. Primary Mode Register.
11 Write size of q to PKHA A Size Register.
5.
11 Write the value j2 (saved earlier) to PKHA A Register.
6.
11 Write Mode command for MOD_ADD to Primary Mode Register (00800002h).
7.

11 Wait for interrupt to indicate "done".
8.
11 Clear the interrupt by writing 10000h to LTC Status Register. This also clears the
9. Primary Mode Register. PKHA B0 now contains the final result j = j2 + (h * q).
12 Read the value j from PKHA B0 Register and save it as the j result. This size of this
0. value is n size.

42.9 LTC General Examples

Writing and Reading Data from the FIFOs:

1. Writing and reading by polling operations.
   - The FIFO Status Register(LTCFIFOSTA) shows the number of entries in both the input and output FIFOs. It also shows when the FIFOs are full.
   - The input and output FIFOs support 4x32bit entries each.
   - Whenever there is space in the input FIFO the user can write a word into the Input FIFO.
   - Whenever there is a word in the output FIFO then the user can read a word from the Output FIFO.
2. Writing and reading FIFOs by DMA operations.
   - The on chip DMA will handle all reads and writes of the FIFOs.
   - The IDE and ODE bits in the Control Register must be written to enable the DMA handshake.
     - IDE will enable dma transfers to the input FIFO when there is space available.
     - ODE will enable dma transfers from the output FIFO when there are words in the FIFO.
   - The on chip DMA should then be programmed to write data to the input FIFO and read data from the output FIFO.

42.10 LTC Register Descriptions

All reads of undefined and write-only addresses always return zero. Writes to undefined and read-only addresses are ignored. LTC will never generate a transfer error on the register bus. Although many of the LTC registers hold more than 32 bits, the register addresses shown in the Memory Map below represent how these registers are accessed over the register bus as 32-bit words.

NOTE

The reset value of some registers differs between different versions of LTC. To ensure driver compatibility across different versions of LTC, when updating fields within registers, the registers should first be read, the required fields updated, and then the register should be written. This will avoid inadvertently changing the settings of other fields in the same register.

42.10.1 LTC Memory Map

Offset	Register	Width (In bits)	Access	Reset value
0h	LTC Mode (non-PKHA/non-RNG use) (LTC0_MD)	32	RW	00000000h
0h	LTC Mode (PublicKey) (LTC0_MDPK)	32	RW	00000000h
8h	LTC Key Size (LTC0_KS)	32	RW	00000000h
10h	LTC Data Size (LTC0_DS)	32	RW	00000000h
18h	LTC ICV Size (LTC0_ICVS)	32	RW	00000000h
30h	LTC Command (LTC0_COM)	32	WO	00000000h
34h	LTC Control (LTC0_CTL)	32	RW	00000000h
40h	LTC Clear Written (LTC0_CW)	32	WO	00000000h
48h	LTC Status (LTC0_STA)	32	W1C	00000000h
4Ch	LTC Error Status (LTC0_ESTA)	32	RO	00000000h
58h	LTC AAD Size (LTC0_AADSZ)	32	RW	00000000h
60h	LTC IV Size (LTC0_IVSZ)	32	RW	00000000h
68h	LTC DPA Mask Seed (LTC0_DPAMS)	32	WO	00000000h
80h	LTC PKHA A Size (LTC0_PKASZ)	32	RW	00000000h
88h	LTC PKHA B Size (LTC0_PKBSZ)	32	RW	00000000h
90h	LTC PKHA N Size (LTC0_PKNSZ)	32	RW	00000000h
98h	LTC PKHA E Size (LTC0_PKESZ)	32	RW	00000000h
100h - 13Ch	LTC Context (LTC0_CTX_0 - LTC0_CTX_15)	32	RW	00000000h
200h - 21Ch	LTC Keys (LTC0_KEY_0 - LTC0_KEY_7)	32	RW	00000000h
4F0h	LTC Version ID (LTC0_VID1)	32	RO	00340100h
4F8h	LTC CHA Version ID (LTC0_CHAVID)	32	RO	00440151h
7C0h	LTC FIFO Status (LTC0_FIFOSTA)	32	RO	00000000h
7E0h	LTC Input Data FIFO (LTC0_IFIFO)	32	WO	00000000h
7F0h	LTC Output Data FIFO (LTC0_OFIFO)	32	RO	00000000h
800h - 83Ch	LTC PKHA A0 (LTC0_PKA0_0 - LTC0_PKA0_15)	32	RW	00000000h
800h - 8FCh	LTC PKHA A (LTC0_PKA_0 - LTC0_PKA_63)	32	RW	00000000h
840h - 87Ch	LTC PKHA A1 (LTC0_PKA1_0 - LTC0_PKA1_15)	32	RW	00000000h

Table continues on the next page...

Offset	Register	Width (In bits)	Access	Reset value
880h - 8BCh	LTC PKHA A2 (LTC0_PKA2_0 - LTC0_PKA2_15)	32	RW	00000000h
8C0h - 8FCh	LTC PKHA A3 (LTC0_PKA3_0 - LTC0_PKA3_15)	32	RW	00000000h
A00h - A3Ch	LTC PKHA B0 (LTC0_PKB0_0 - LTC0_PKB0_15)	32	RW	00000000h
A00h - AFCh	LTC PKHA B (LTC0_PKB_0 - LTC0_PKB_63)	32	RW	00000000h
A40h - A7Ch	LTC PKHA B1 (LTC0_PKB1_0 - LTC0_PKB1_15)	32	RW	00000000h
A80h - ABCh	LTC PKHA B2 (LTC0_PKB2_0 - LTC0_PKB2_15)	32	RW	00000000h
AC0h - AFCh	LTC PKHA B3 (LTC0_PKB3_0 - LTC0_PKB3_15)	32	RW	00000000h
C00h - C3Ch	LTC PKHA N0 (LTC0_PKN0_0 - LTC0_PKN0_15)	32	RW	00000000h
C00h - CFCh	LTC PKHA N (LTC0_PKN_0 - LTC0_PKN_63)	32	RW	00000000h
C40h - C7Ch	LTC PKHA N1 (LTC0_PKN1_0 - LTC0_PKN1_15)	32	RW	00000000h
C80h - CBCh	LTC PKHA N2 (LTC0_PKN2_0 - LTC0_PKN2_15)	32	RW	00000000h
CC0h - CFCh	LTC PKHA N3 (LTC0_PKN3_0 - LTC0_PKN3_15)	32	RW	00000000h
E00h - EFCh	LTC PKHA E (LTC0_PKE_0 - LTC0_PKE_63)	32	WO	00000000h

42.10.2 LTC Mode (PublicKey) (LTC0_MDPK)

42.10.2.1 Address

Register	Offset
LTC0_MDPK	0h

42.10.2.2 Function

The Mode Register is used to tell the CHAs which operation is being requested. The interpretation of this register is for public key operations (PKHA) only, and is described herein.

The bit assignments for the PKHA_MODE will be different depending on which of the three types of PKHA functions is being called. The three function types are: 1) Clear Memory, 2) Modular Arithmetic, and 3) Copy Memory. Detailed descriptions of their mode formats can be found in Table PKHA MODE: clear memory function, Table PKHA MODE: Arithmetic Functions and Table PKHA MODE: copy memory functions.

42.10.2.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved								ALG				PKHA_MODE_MS			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved				PKHA_MODE_LS											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.2.4 Fields

Field	Function
31-24 —	Options bits.
23-20 ALG	Algorithm. This field specifies which algorithm is being selected. 1000b - PKHA
19-16 PKHA_MODE_MS	PKHA_MODE most-significant 4 bits. The format of the PKHA_MODE field differs depending on which of the three types of PKHA functions is being executed. The three function types are: 1) Clear Memory, 2) Modular Arithmetic, and 3) Copy Memory. Detailed descriptions of their mode formats can be found in Table PKHA MODE: clear memory function, Table PKHA MODE: Arithmetic Functions and Table PKHA MODE: copy memory functions.
15-12 —	Reserved
11-0 PKHA_MODE_LS	PKHA_MODE least significant 12 bits. The format of the PKHA_MODE field differs depending on which of the three types of PKHA functions is being executed. The three function types are: 1) Clear Memory, 2) Modular Arithmetic, and 3) Copy Memory. Detailed descriptions of their mode formats can be found in Table PKHA MODE: clear memory function, Table PKHA MODE: Arithmetic Functions and Table PKHA MODE: copy memory functions.

42.10.3 LTC Mode (non-PKHA/non-RNG use) (LTC0_MD)

42.10.3.1 Address

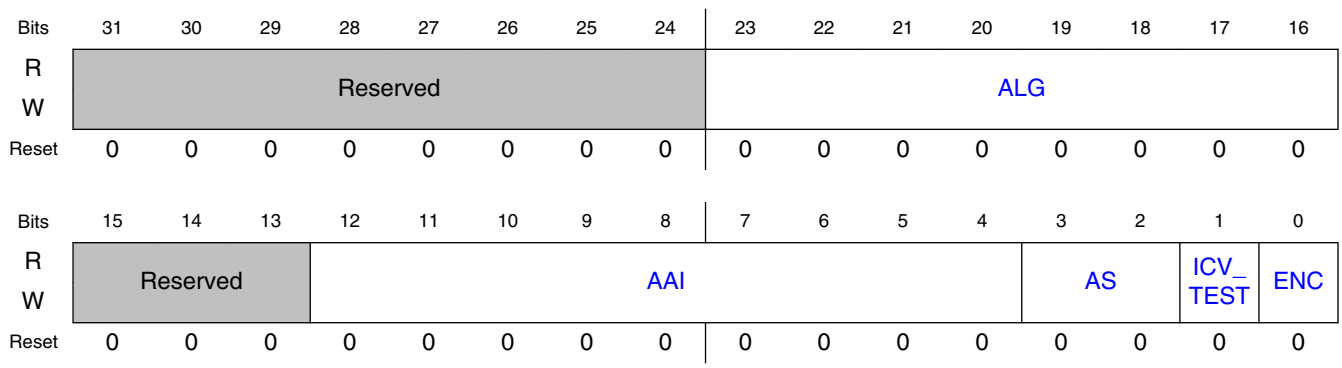
Register	Offset
LTC0_MD	0h

42.10.3.2 Function

The Mode Register is used to tell the cryptographic engines which operation is being requested. The interpretation of this register will be unique for each CHA.

This section defines the format of the Mode Register when used with non-public-key algorithms and non-RNG operations.

42.10.3.3 Diagram



42.10.3.4 Fields

Field	Function
31-24 —	Reserved. Must be 0.
23-16 ALG	Algorithm. This field specifies which algorithm is being selected. 00010000b - AES 00100000b - DES 00100001b - 3DES
15-13 —	Reserved. Must be 0.
12-4 AAI	Additional Algorithm information. This field contains additional mode information that is associated with the algorithm that is being executed. See also the section describing the appropriate CHA.

Table continues on the next page...

<table>
<tr><th>Field</th><th>Function</th></tr>
<tr><td></td><td>
NOTE: Some algorithms do not require additional algorithm information and in those cases this field should be all 0s.
<h3>Table 42-67. AAI Interpretation for AES Modes</h3>
<table>
<tr><th colspan="5">[For AES the MSB of AAI is the DK (Decrypt Key) bit.]</th></tr>
<tr><th>Code[1]</th><th>Interpretation</th><th></th><th>Code</th><th>Interpretation</th></tr>
<tr><td>00h</td><td>CTR (mod 2^{128})</td><td></td><td>80h</td><td>CCM, CCM*</td></tr>
<tr><td>10h</td><td>CBC</td><td></td><td>90h</td><td>GCM</td></tr>
<tr><td>20h</td><td>ECB</td><td></td><td>A0h</td><td>Reserved</td></tr>
<tr><td>30h</td><td>Reserved</td><td></td><td>B0h</td><td>Reserved</td></tr>
<tr><td>40h</td><td>Reserved</td><td></td><td>C0h</td><td>Reserved</td></tr>
<tr><td>50h</td><td>Reserved</td><td></td><td>D0h</td><td>Reserved</td></tr>
<tr><td>60h</td><td>CMAC</td><td></td><td>E0h</td><td>Reserved</td></tr>
<tr><td>70h</td><td>XCBC-MAC</td><td colspan="3"></td></tr>
<tr><td colspan="5">Setting the DK bit (i.e. ORing 100h with any AES code above) causes Key Register to be loaded with the AES Dcrypt key, rather than the AES Encrypt key.</td></tr>
</table>
1. The codes are mutually exclusive (i.e. they cannot be ORed with each other).
<h3>Table 42-68. AAI Interpretation for DES</h3>
<table>
<tr><th>Code[1]</th><th>Interpretation</th><th></th><th>Code[1]</th><th>Interpretation</th></tr>
<tr><td>10h</td><td>CBC</td><td></td><td>30h</td><td>CFB</td></tr>
<tr><td>20h</td><td>ECB</td><td></td><td>40h</td><td>OFB</td></tr>
<tr><td colspan="5">80h ORed with any DES code above: Check odd parity</td></tr>
</table>
1. The codes are mutually exclusive (i.e. they cannot be ORed with each other).
</td></tr>
<tr><td>3-2
AS</td><td>Algorithm State. This field defines the state of the algorithm that is being executed. This may not be used by every algorithm.
00b - Update
01b - Initialize
10b - Finalize
11b - Initialize/Finalize</td></tr>
<tr><td>1
ICV_TEST</td><td>ICV Checking / Test AES fault detection.
For algorithms other than AES ECB mode: ICV Checking
This bit selects whether the current algorithm should compare the known ICV versus the calculated ICV. This bit will be ignored by algorithms that do not support ICV checking.
0 - Don't compare
1 - Compare
For AES ECB mode: Test AES fault detection</td></tr>
</table>

Table continues on the next page...

Field	Function
	In AES ECB mode, this bit activates fault detection testing by injecting bit level errors into AES core logic as defined in the first 128 bits of the context. 0 - Don't inject bit errors 1 - Inject bit errors
0 ENC	Encrypt/Decrypt. This bit selects encryption or decryption. 0b - Decrypt. 1b - Encrypt.

1. The codes are mutually exclusive (i.e. they cannot be ORed with each other).

42.10.4 LTC Key Size (LTC0_KS)

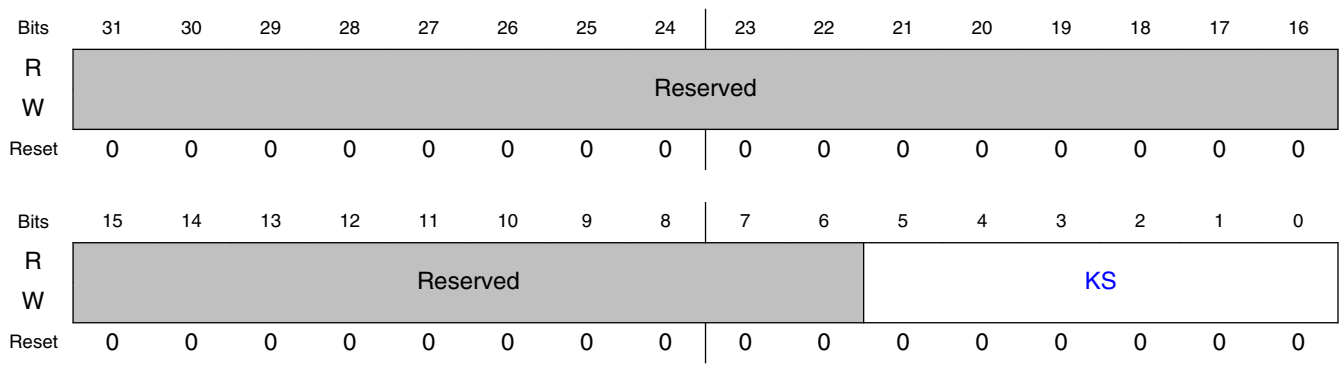
42.10.4.1 Address

Register	Offset
LTC0_KS	8h

42.10.4.2 Function

The Key Size Register is used to tell the crypto engine(AES) the size of the key that was loaded into the Key Register. The Key Size Register must be written after the key is written into the Key Register. Writing to the Key Size Register will prevent the user from modifying the Key Register. Only 16, 24, and 32 byte keys are supported.

42.10.4.3 Diagram



42.10.4.4 Fields

Field	Function
31-6 —	Reserved.
5-0 KS	Key Size. This is the size of a Key measured in bytes

42.10.5 LTC Data Size (LTC0_DS)

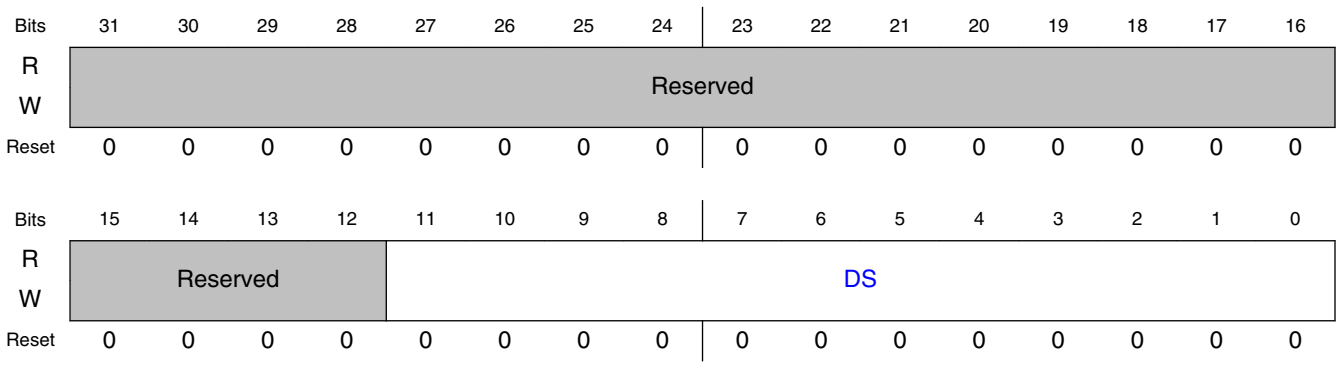
42.10.5.1 Address

Register	Offset
LTC0_DS	10h

42.10.5.2 Function

The Data Size Register is used to tell the AES the amount of data that will be loaded into the Input Data FIFO. This register should only be written to once during a single operation. Note that writing to the LTC AAD Size (LTC0_AADSZ) , or the LTC IV Size (LTC0_IVSZ), will cause this register to also update. When this register is then written directory to then the new value will be added to the previous value in the register. That is, if the DS field currently has the value 16, writing 2 to the least-significant half of the Data Size register (i.e. the DS field) will result in a value of 18 in the DS field. Note that AES decrements this register, so reading the register may return a value less than sum of the values that were written into it. This register is cleared whenever a key is decrypted or encrypted.

42.10.5.3 Diagram



42.10.5.4 Fields

Field	Function
31-12 —	Reserved.
11-0 DS	Data Size. This is the number of whole bytes of data that will be consumed by the CHA. Note that writing the AAD Size Register or IV Size Register will result in this register also being written to.

42.10.6 LTC ICV Size (LTC0_ICVS)

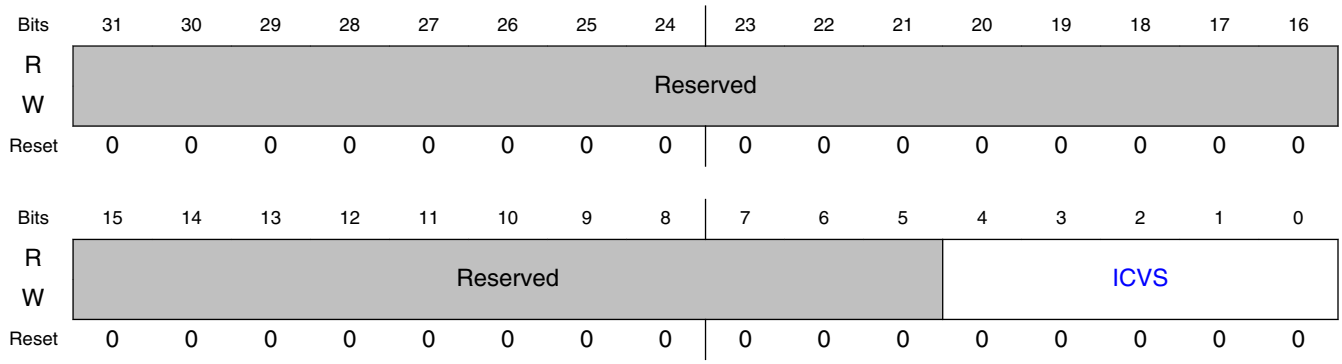
42.10.6.1 Address

Register	Offset
LTC0_ICVS	18h

42.10.6.2 Function

The ICV Size Register indicates how much of the last block of ICV is valid when performing AES integrity check modes (e.g. AES-CMAC, AES-XCBC-MAC). This register must be written prior to the corresponding word of data being consumed by AES. In practical terms, this means the register must be written prior to the corresponding data being written to the Input Data FIFO.

42.10.6.3 Diagram



42.10.6.4 Fields

Field	Function
31-5 —	Reserved.
4-0 ICVS	ICV Size, in Bytes.

42.10.7 LTC Command (LTC0_COM)

42.10.7.1 Address

Register	Offset
LTC0_COM	30h

42.10.7.2 Function

The LTC Command Register is used to send control signals to the Crypto Engines.

42.10.7.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved			Reserved	Reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved			Reserved		Reserved	Reserved	Reserved	Reserved	PK	Reserved	Reserved	Reserved	DES	AES	ALL
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.7.4 Fields

Field	Function
31-29 —	Reserved. To preserve software compatibility with other versions of LTC, 0 should be written to all reserved bits.
28 —	Reserved.
27-13 —	Reserved.
12-11 —	Reserved
10 —	Reserved
9 —	Reserved
8 —	Reserved
7 —	Reserved
6 PK	Reset PKHA. Writing a 1 to this bit resets the Public Key Hardware Accelerator. 0b - Do Not Reset 1b - Reset Public Key Hardware Accelerator
5 —	Reserved
4 —	Reserved
3	Reserved.

Table continues on the next page...

Field	Function
—	
2 DES	Reset DESA. Writing a 1 to this bit resets the DES Accelerator. 0b - Do Not Reset 1b - Reset DES Accelerator
1 AES	Reset AESA. Writing a 1 to this bit resets the AES Accelerator core engine. 0b - Do Not Reset 1b - Reset AES Accelerator
0 ALL	Reset All Internal Logic. Writing to this bit will reset all accelerator engines and as well as all the internal registers. 0b - Do Not Reset 1b - Reset all CHAs in use by this CCB.

42.10.8 LTC Control (LTC0_CTL)

42.10.8.1 Address

Register	Offset
LTC0_CTL	34h

42.10.8.2 Function

This register is used for some of the internal controls of the LTC block.

42.10.8.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	KAL	Reserved							COS	CIS	KOS	KIS	Reserved		OFS	IFS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved		OFR	OFE	Reserved		IFR	IFE	Reserved			PDE	Reserved			IM
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.8.4 Fields

Field	Function
31 KAL	Key Register Access Lock. Read access to the key register is blocked. Any reads of the key register will only return zero. Once this bit is set, it can only be cleared by hard reset. 0b - Key Register is readable. 1b - Key Register is not readable.
30-24 —	Reserved.
23 COS	Context Register Output Byte Swap. Byte swap all data that is read from the context register. Data is byte swapped only within a single word. 0b - Do Not Byte Swap Data. 1b - Byte Swap Data.
22 CIS	Context Register Input Byte Swap. Byte swap all data that is written to the context register. Data is byte swapped only within a single word. 0b - Do Not Byte Swap Data. 1b - Byte Swap Data.
21 KOS	Key Register Output Byte Swap. Byte swap all data that is read from the key register. Data is byte swapped only within a single word. 0b - Do Not Byte Swap Data. 1b - Byte Swap Data.
20 KIS	Key Register Input Byte Swap. Byte swap all data that is written to the key register. Data is byte swapped only within a single word. 0b - Do Not Byte Swap Data. 1b - Byte Swap Data.
19-18 —	Reserved.
17 OFS	Output FIFO Byte Swap. Byte swap all data that is read from the Onput FIFO. 0b - Do Not Byte Swap Data. 1b - Byte Swap Data.
16 IFS	Input FIFO Byte Swap. Byte swap all data that is written to the Input FIFO. 0b - Do Not Byte Swap Data. 1b - Byte Swap Data.
15-14 —	Reserved.
13 OFR	Output FIFO DMA Request Size. The DMA request logic will only request data if the OUTPUT FIFO has enough data to satisfy the request. 0b - DMA request size is 1 entry. 1b - DMA request size is 4 entries.
12 OFE	Output FIFO DMA Enable. 0b - DMA Request and Done signals disabled for the Output FIFO. 1b - DMA Request and Done signals enabled for the Output FIFO.
11-10 —	Reserved.

Table continues on the next page...

Field	Function
9 IFR	Input FIFO DMA Request Size. The DMA request logic will only request data if the INPUT FIFO has enough space for the request size. 0b - DMA request size is 1 entry. 1b - DMA request size is 4 entries.
8 IFE	Input FIFO DMA Enable. 0b - DMA Request and Done signals disabled for the Input FIFO. 1b - DMA Request and Done signals enabled for the Input FIFO.
7-5 —	Reserved.
4 PDE	PKHA Register DMA Enable. 0b - DMA Request and Done signals disabled for the PKHA Registers. 1b - DMA Request and Done signals enabled for the PKHA Registers.
3-1 —	Reserved.
0 IM	Interrupt Mask. Once this bit is set, it can only be cleared by hard reset. 0b - Interrupt not masked. 1b - Interrupt masked

42.10.9 LTC Clear Written (LTC0_CW)

42.10.9.1 Address

Register	Offset
LTC0_CW	40h

42.10.9.2 Function

The Clear Written Register is used to clear many of the internal registers. All fields of this register are self-clearing.

42.10.9.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			Reserved		Reserved											
W	CIF	COF														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R					Reserved							Reserved			Reserved	
W	CPKE	CPKN	CPKB	CPKA						CKR	CCR		CICV	CDS		CM
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.9.4 Fields

Field	Function
31 CIF	Clear Input FIFO. Writing a 1 to this bit causes the Input Data FIFO.
30 COF	Clear Output FIFO. Writing a 1 to this bit causes the Output FIFO to be cleared.
29-28 —	Reserved.
27-16 —	Reserved.
15 CPKE	Clear the PKHA E Size Register. Writing a one to this bit causes the PKHA E Size Register to be cleared.
14 CPKN	Clear the PKHA N Size Register. Writing a one to this bit causes the PKHA N Size Register to be cleared.
13 CPKB	Clear the PKHA B Size Register. Writing a one to this bit causes the PKHA B Size Register to be cleared.
12 CPKA	Clear the PKHA A Size Register. Writing a one to this bit causes the PKHA A Size Register to be cleared.
11-7 —	Reserved.
6 CKR	Clear the Key Register. Writing a one to this bit causes the Key and Key Size Registers to be cleared.
5 CCR	Clear the Context Register. Writing a one to this bit causes the Context Register to be cleared.
4 —	Reserved.

Table continues on the next page...

Field	Function
3 CICV	Clear the ICV Size Register. Writing a one to this bit causes the ICV Size Register to be cleared.
2 CDS	Clear the Data Size Register. Writing a one to this bit causes the Data Size Register to be cleared. This clears AAD Size as well.
1 —	Reserved.
0 CM	Clear the Mode Register. Writing a one to this bit causes the Mode Register to be cleared.

42.10.10 LTC Status (LTC0_STA)

42.10.10.1 Address

Register	Offset
LTC0_STA	48h

42.10.10.2 Function

The LTC Status Register shows the status of the internal Crypto engine and its internal registers.

42.10.10.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved	PKZ	PKO	PKP	Reserved				Reserved			EI	Reserved			DI
W																w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved			Reserved		Reserved	Reserved	Reserved	Reserved	PB	Reserved	Reserved	Reserved	DB	AB	Reserved
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.10.4 Fields

<table>
<tr><th>Field</th><th>Function</th></tr>
<tr><td>31
—</td><td>Reserved.</td></tr>
<tr><td>30
PKZ</td><td>Public Key Operation is Zero. For Finite Field operations the result of a Public Key operation is zero. For ECC operations, the result is Point at infinity.</td></tr>
<tr><td>29
PKO</td><td>Public Key Operation is One. The greatest common divisor of two numbers is one (that is, the two numbers are relatively prime) for GCD operation, or PKHA result = 1 for Finite Field operations.</td></tr>
<tr><td>28
PKP</td><td>Public Key is Prime. The given number is probably prime (that is, it passes the Miller-Rabin primality test).</td></tr>
<tr><td>27-25
—</td><td>Reserved.</td></tr>
<tr><td>24
—</td><td>Reserved.</td></tr>
<tr><td>23-21
—</td><td>Reserved.</td></tr>
<tr><td>20
EI</td><td>Error Interrupt. The Error Interrupt has been asserted. This error can only be cleared by resetting LTC.
0b - Not Error.
1b - Error Interrupt.</td></tr>
<tr><td>19-17
—</td><td>Reserved.</td></tr>
<tr><td>16
DI</td><td>Done Interrupt. The Done Interrupt has been asserted.
<table>
<tr><th>Value</th><th>Read</th><th>Write</th></tr>
<tr><td>0</td><td>No Done Interrupt</td><td>No change</td></tr>
<tr><td>1</td><td>Done Interrupt asserted</td><td>Clear the Done Interrupt</td></tr>
</table></td></tr>
<tr><td>15-13
—</td><td>Reserved.</td></tr>
<tr><td>12-11
—</td><td>Reserved</td></tr>
<tr><td>10
—</td><td>Reserved</td></tr>
<tr><td>9
—</td><td>Reserved</td></tr>
<tr><td>8
—</td><td>Reserved</td></tr>
<tr><td>7</td><td>Reserved</td></tr>
</table>

Table continues on the next page...

Field	Function
—	
6 PB	PKHA Busy. This bit indicates that the Public Key Hardware Accelerator is busy. The CHA can either be busy processing data or resetting. 0b - PKHA Idle 1b - PKHA Busy.
5 —	Reserved
4 —	Reserved
3 —	Reserved.
2 DB	DESA Busy. This bit indicates that the DES Accelerator is busy. The CHA can either be busy processing data or resetting. 0b - DESA Idle 1b - DESA Busy.
1 AB	AESA Busy. This bit indicates that the AES Accelertor is busy. The CHA can either be busy processing data or resetting. 0b - AESA Idle 1b - AESA Busy.
0 —	Reserved.

42.10.11 LTC Error Status (LTC0_ESTA)

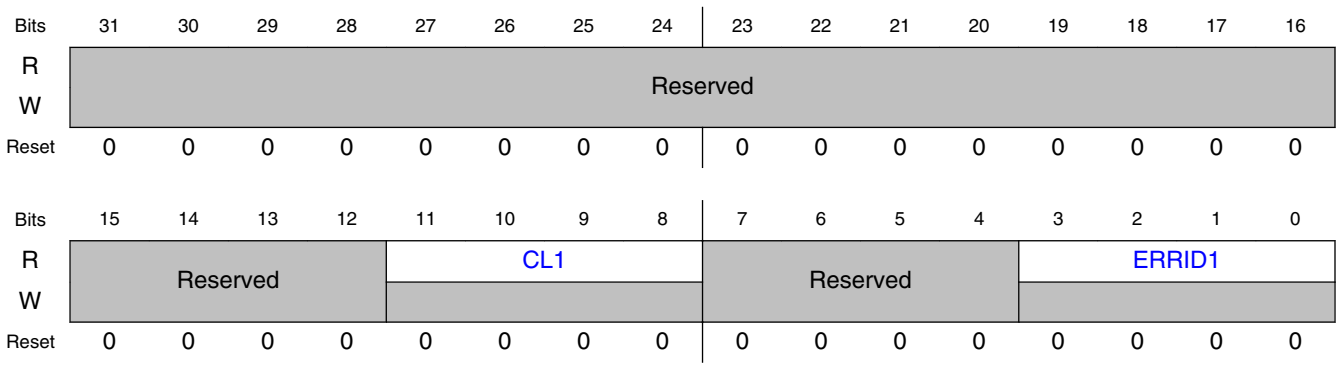
42.10.11.1 Address

Register	Offset
LTC0_ESTA	4Ch

42.10.11.2 Function

The LTC Error Register shows the status of the internal Crypto Engine and its internal registers.

42.10.11.3 Diagram



42.10.11.4 Fields

Field	Function
31-12 —	Reserved.
11-8 CL1	algorithms. The algorithms field indicates which algorithm is asserting an error. Others reserved 0000b - LTC General Error 0001b - AES 0010b - DES 1000b - Public Key
7-4 —	Reserved
3-0 ERRID1	Error ID 1. These bits indicate the type of error that was found while processing the Descriptor. The Algorithm that is associated with the error can be found in the CL1 field. Others reserved. 0001b - Mode Error 0010b - Data Size Error, including PKHA N Register Size Error 0011b - Key Size Error, including PKHA E Register Size Error 0100b - PKHA A Register Size Error 0101b - PKHA B Register Size Error 0110b - Data Arrived out of Sequence Error 0111b - PKHA Divide by Zero Error 1000b - PKHA Modulus Even Error 1001b - DES Key Parity Error 1010b - ICV Check Failed 1011b - Internal Hardware Failure 1100b - CCM AAD Size Error (either 1. AAD flag in B0 =1 and no AAD type provided, 2. AAD flag in B0 = 0 and AAD povided, or 3. AAD flag in B0 =1 and not enough AAD provided - expecting more based on AAD size.) 1111b - Invalid Crypto Engine Selected

42.10.12 LTC AAD Size (LTC0_AADSZ)

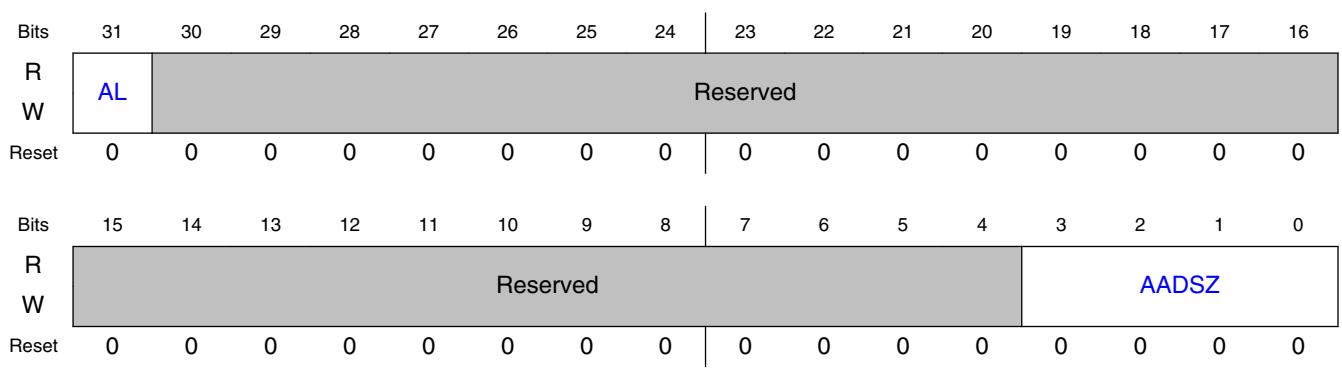
42.10.12.1 Address

Register	Offset
LTC0_AADSZ	58h

42.10.12.2 Function

The AAD Size Register is used by AESA to determine how much of the last block of AAD is valid. The write to this register should be the entire size of the AAD as it is also added directly to the Data Size Register. The size added to the Data Size Register is the AAD size rounded up to the next 16 byte boundary. For instance a size of 20 bytes written to the AAD size register will cause 32 bytes to be added to the Data Size Register. The size stored in the AADSZ field represents the number of bytes valid in the final block of AAD. However the entire size of AAD should be written to the LTC AAD Size (LTC0_AADSZ) Register address location. When authentication only is being done then the AL bit needs to be written to tell the AES engine that this is the last of the data.

42.10.12.3 Diagram



42.10.12.4 Fields

Field	Function
31 AL	AAD Last. Only AAD data will be written into the Input FIFO.
30-4 —	Reserved.
3-0 AADSZ	AAD size in Bytes, mod 16.

42.10.13 LTC IV Size (LTC0_IVSZ)

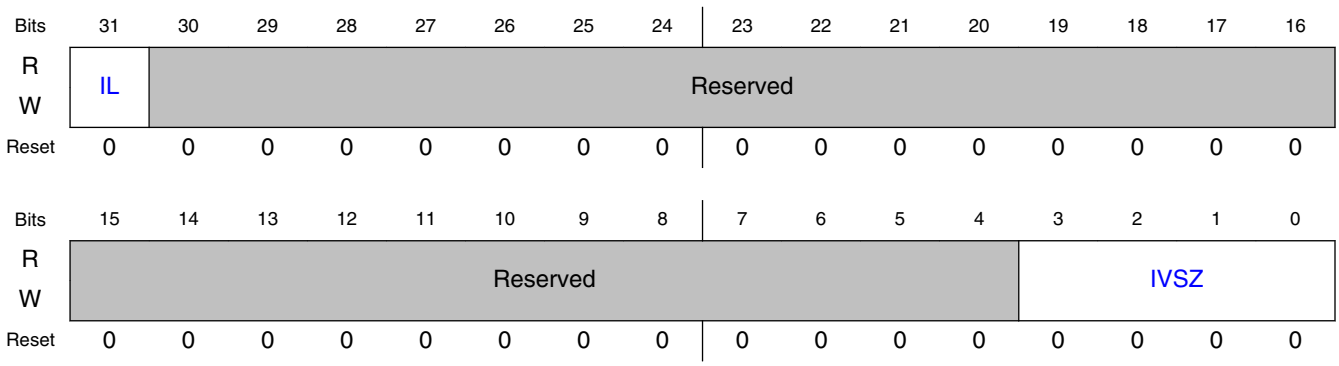
42.10.13.1 Address

Register	Offset
LTC0_IVSZ	60h

42.10.13.2 Function

The IV Size Register is used by AESA to determine how much of the last block of IV is valid. The write to this register should be the entire size of the IV as it is also added directly to the Data Size Register. The size added to the Data Size Register is the IV size rounded up to the next 16 byte boundary. For instance a size of 20 bytes written to the IV size register will cause 32 bytes to be added to the Data Size Register. The size stored in the IVSZ field represents the number of bytes valid in the final block of IV. However the entire size of IV should be written to the LTC IV Size (LTC0_IVSZ) Register address location. When IV only is being done then the IL bit needs to be written to tell the AES engine that this is the last of the data.

42.10.13.3 Diagram



42.10.13.4 Fields

Field	Function
31 IL	IV Last. Only IV data will be written into the Input FIFO.
30-4 —	Reserved.
3-0 IVSZ	IV size in Bytes, mod 16.

42.10.14 LTC DPA Mask Seed (LTC0_DPAMS)

42.10.14.1 Address

Register	Offset
LTC0_DPAMS	68h

42.10.14.2 Function

The DPA Mask Seed Register is used to reseed the mask that provides resistance against Differential Power Analysis attacks on AES keys.

42.10.14.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W	DPAMS															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W	DPAMS															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.14.4 Fields

Field	Function
31-0 DPAMS	Differential Power Analysis Mask Seed.This resistance uses a randomly changing mask that introduces "noise" into the power consumed by the AESA. This reduces the signal to noise ratio that differential power analysis attacks use to "guess" bits of the AES key. This randomly changing mask should be seeded at POR, and will continue to provide DPA resistance thereafter. However, to provide even more DPA protection it is recommended that the DPA Mask be reseeded after every 50,000 AESA blocks have been processed. At that time software can opt to write a new seed (preferably obtained from an RNG) into the DPA Mask Seed Register (DPAMS), or software can instead opt to provide new seed earlier or later, or not at all. DPA resistance continues even if the DPA Mask is never reseeded.

42.10.15 LTC PKHA A Size (LTC0_PKASZ)

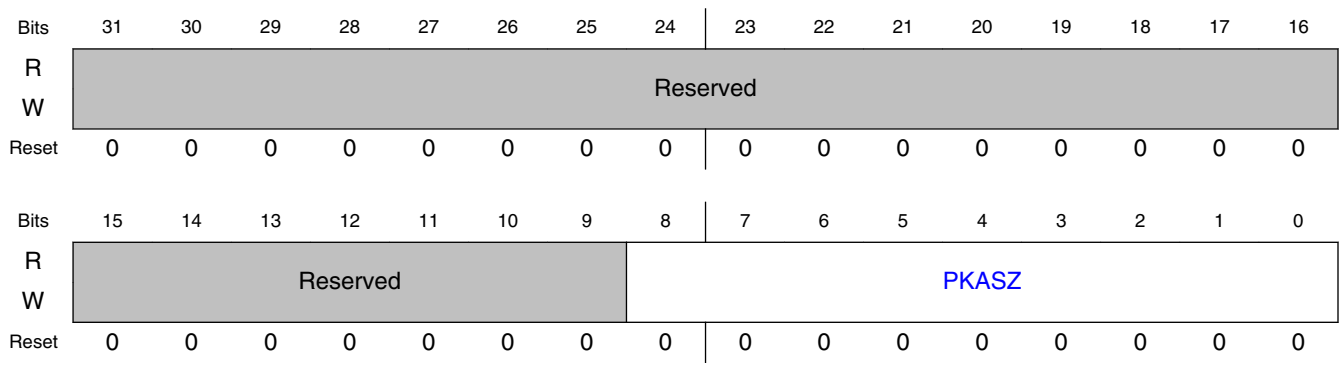
42.10.15.1 Address

Register	Offset
LTC0_PKASZ	80h

42.10.15.2 Function

The LTC PKHA A Size Register is used to indicate the number of bytes of valid data in the PKHA A Register. That is, it indicates the size, in bytes, of the numeric value contained in the PKHA A Register. Depending on the PKHA operation to be run, this register may need to be loaded prior to starting the PKHA operation. Note that some PKHA operations update this value at the completion of the operation.

42.10.15.3 Diagram



42.10.15.4 Fields

Field	Function
31-9 —	Reserved.
8-0 PKASZ	PKHA A Size. This is the size of the numeric value, in bytes, contained within the PKHA A Register.

42.10.16 LTC PKHA B Size (LTC0_PKBSZ)

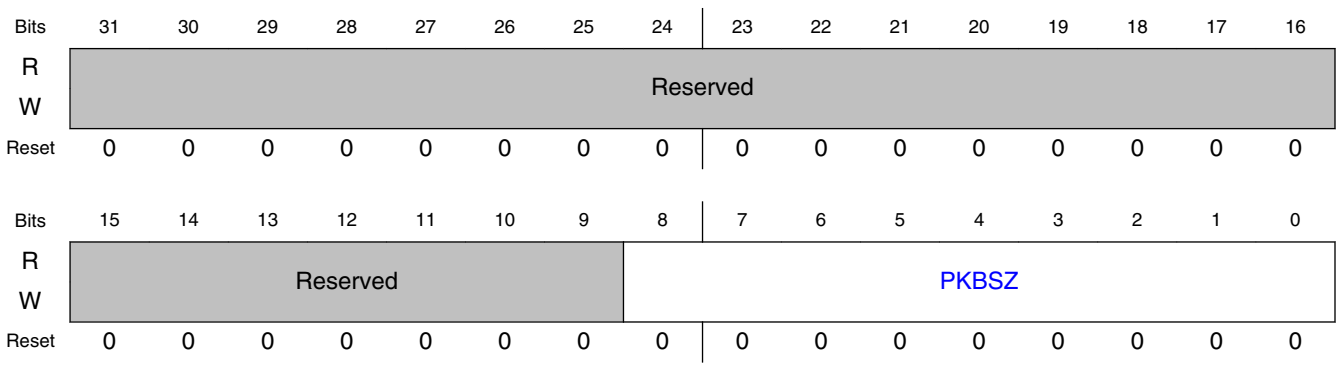
42.10.16.1 Address

Register	Offset
LTC0_PKBSZ	88h

42.10.16.2 Function

The LTC PKHA B Size Register is used to indicate the number of bytes of valid data in the PKHA B Register. That is, it indicates the size, in bytes, of the numeric value contained in the PKHA B Register. Depending on the PKHA operation to be run, this register may need to be loaded prior to starting the PKHA operation. Note that some PKHA operations update this value at the completion of the operation.

42.10.16.3 Diagram



42.10.16.4 Fields

Field	Function
31-9 —	Reserved.
8-0 PKBSZ	PKHA B Size. This is the size of the numeric value, in bytes, contained within the PKHA B Register.

42.10.17 LTC PKHA N Size (LTC0_PKNSZ)

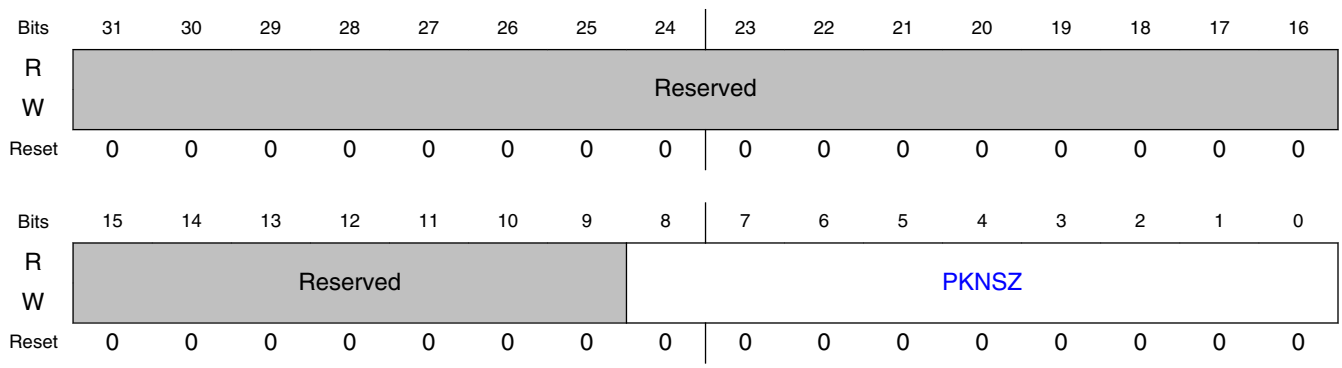
42.10.17.1 Address

Register	Offset
LTC0_PKNSZ	90h

42.10.17.2 Function

The LTC PKHA N Size Register is used to indicate the number of bytes of valid data in the PKHA N Register. That is, it indicates the size, in bytes, of the numeric value contained in the PKHA N Register. Depending on the PKHA operation to be run, this register may need to be loaded prior to starting the PKHA operation. Note that some PKHA operations update this value at the completion of the operation.

42.10.17.3 Diagram



42.10.17.4 Fields

Field	Function
31-9 —	Reserved.
8-0 PKNSZ	PKHA N Size. This is the size of the numeric value, in bytes, contained within the PKHA N Register.

42.10.18 LTC PKHA E Size (LTC0_PKESZ)

42.10.18.1 Address

Register	Offset
LTC0_PKESZ	98h

42.10.18.2 Function

The LTC PKHA E Size Register is used to indicate the number of bytes of valid data in the PKHA E Register. That is, it indicates the size, in bytes, of the numeric value contained in the PKHA E Register. Depending on the PKHA operation to be run, this register may need to be loaded prior to starting the PKHA operation. Note that some PKHA operations update this value at the completion of the operation.

42.10.18.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved								PKESZ							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.18.4 Fields

Field	Function
31-9 —	Reserved.
8-0 PKESZ	PKHA E Size. This is the size of the numeric value, in bytes, contained within the PKHA E Register.

42.10.19 LTC Context (LTC0_CTX_a)

42.10.19.1 Address

For a = 0 to 15:

Register	Offset
LTC0_CTX_a	100h + (a × 4h)

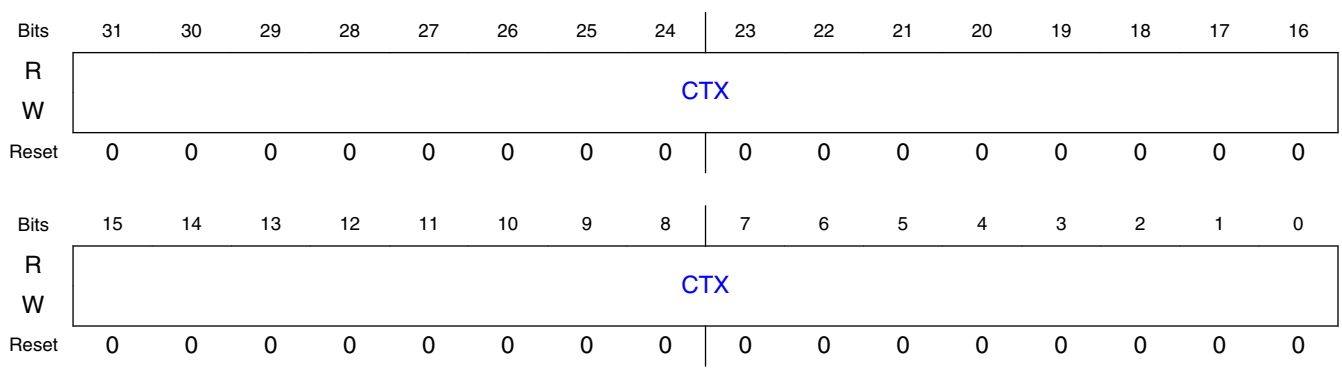
42.10.19.2 Function

The Context Register holds the context for the internal crypto engine. This register is 512 bits in length. The IP bus write to the Context Register is accessible only as full-word reads or writes to sixteen 32-bit registers. The MSB is located at offset 0100h with respect to the register page.

The bit assignments of this register are dependent on the algorithm, and in some cases the mode of that algorithm. See the appropriate section for the Context Register format used for that algorithm:

- AES ECB: Section AES ECB mode use of the Context Register
- AES CBC: Section AES CBC mode use of the Context Register
- AES CTR: Section AES CTR mode use of the Context Register
- AES CCM: Section AES CCM and CCM* mode use of the Context Register
- DES: Section DESA Context Register
- Triple DES: Section DESA Context Register

42.10.19.3 Diagram



42.10.19.4 Fields

Field	Function
31-0 CTX	CTX

42.10.20 LTC Keys (LTC0_KEY_a)

42.10.20.1 Address

Register	Offset
LTC0_KEY_0	200h
LTC0_KEY_1	204h
LTC0_KEY_2	208h
LTC0_KEY_3	20Ch
LTC0_KEY_4	210h
LTC0_KEY_5	214h
LTC0_KEY_6	218h
LTC0_KEY_7	21Ch

42.10.20.2 Function

The Key Register normally holds the left-aligned key for the internal crypto engine. The MSB is in offset 200h. The Key Register is 256 bits in length. The IP bus write to the Context Register is accessible only as full-word reads or writes to four 32-bit registers.

Before the value in the Key Register can be used in a cryptographic operation, the size of the key must be written into the Key Size Register. Once the Key Size Register has been written, the Key Register cannot be written again until the Key Size Register has been cleared.

42.10.20.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	KEY															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	KEY															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.20.4 Fields

Field	Function
31-0 KEY	KEY

42.10.21 LTC Version ID (LTC0_VID1)

42.10.21.1 Address

Register	Offset
LTC0_VID1	4F0h

42.10.21.2 Function

This register contains the ID for LTC and major and minor revision numbers.

42.10.21.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IP_ID															
W																
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MAJ_REV								MIN_REV							
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

42.10.21.4 Fields

Field	Function
31-16 IP_ID	ID(0x0038).
15-8 MAJ_REV	Major revision number.
7-0 MIN_REV	Minor revision number.

42.10.22 LTC CHA Version ID (LTC0_CHAVID)

42.10.22.1 Address

Register	Offset
LTC0_CHAVID	4F8h

42.10.22.2 Function

This register contains the Version ID and Revision Number for the CHAs contained within LTC.

42.10.22.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved								PKHAVID				PKHAREV			
W																
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DESVID				DESREV				AESVID				AESREV			
W																
Reset	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1

42.10.22.4 Fields

Field	Function
31-24 —	Reserved
23-20 PKHAVID	PK Version ID 0001 - 32-bit PKHA-SD 0010 - 64-bit PKHA-SD 0011 - 128-bit PKHA-SD 0100 - 16-bit PKHA-SD
19-16 PKHAREV	PK Revision Number
15-12 DESVID	DES Version ID(0x0). 0000 - High-performance DESA 0001 - Low-performance DESA
11-8 DESREV	DES Revision Number
7-4 AESVID	AES Version ID
3-0 AESREV	AES Revision Number

42.10.23 LTC FIFO Status (LTC0_FIFOSTA)

42.10.23.1 Address

Register	Offset
LTC0_FIFOSTA	7C0h

42.10.23.2 Function

The LTC FIFO Status shows the current levels of the Input and Output FIFO.

42.10.23.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	OFF	Reserved								OFL						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IFF	Reserved								IFL						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.23.4 Fields

Field	Function
31 OFF	Output FIFO Full. The Output FIFO is full and should not be written to.
30-23 —	Reserved
22-16 OFL	Output FIFO Level. These bits indicate the current number of entries in the Output FIFO.
15 IFF	Input FIFO Full. The Input FIFO is full and should not be written to.
14-7 —	Reserved
6-0 IFL	Input FIFO Level. These bits indicate the current number of entries in the Input FIFO.

42.10.24 LTC Input Data FIFO (LTC0_IFIFO)

42.10.24.1 Address

Register	Offset
LTC0_IFIFO	7E0h

42.10.24.2 Function

Data to be processed by the various crypto engines is first pushed into the Input Data FIFO. The Input Data FIFO supports byte enables, allowing one to four bytes to be written to the IFIFO from the IP bus. The IFIFO is four entries deep, and each entry is four bytes. Care must be used to not overflow the Input Data FIFO. Reads from this address will always return 0x0.

42.10.24.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W	IFIFO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W	IFIFO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.24.4 Fields

Field	Function
31-0 IFIFO	IFIFO

42.10.25 LTC Output Data FIFO (LTC0_OFIFO)

42.10.25.1 Address

Register	Offset
LTC0_OFIFO	7F0h

42.10.25.2 Function

Data that is output from the AES is pushed into the Output Data FIFO. The OFIFO is four entries deep, and each entry is four bytes. During normal operation, the AES will never overflow the Output Data FIFO. Writes to this register are ignored.

42.10.25.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	OFIFO															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	OFIFO															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.25.4 Fields

Field	Function
31-0 OFIFO	Output FIFO

42.10.26 LTC PKHA A0 (LTC0_PKA0_a)

42.10.26.1 Address

For a = 0 to 15:

Register	Offset
LTC0_PKA0_a	800h + (a × 4h)

42.10.26.2 Function

The LTC PKHA A0 Register contains a numeric value of up to 64 bytes, right-justified. The LSByte is in offset 800h, in the right-most byte. The LTC PKHA A0 register is 512 bits in length. Note that PKHA A3, A2, A1 and A0 Registers may be combined to contain a value of up to 2048 bits, with A0 containing the least-significant 64 bytes of this value. The value in the PKHA A0 Register (or {A3, A2, A1, A0}, if used as a single value) is limited by the LTC PKHA A Size (LTC0_PKASZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.26.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_A0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_A0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.26.4 Fields

Field	Function
31-0 PKHA_A0	A0 VALUE

42.10.27 LTC PKHA A (LTC0_PKA_a)

42.10.27.1 Address

For a = 0 to 63:

Register	Offset
LTC0_PKA_a	800h + (a × 4h)

42.10.27.2 Function

The LTC PKHA A Register contains a numeric value of up to 256 bytes, right-justified. The LSByte is in offset 800h, in the right-most byte. The LTC PKHA A register is 2048 bits in length. Note that PKHA A Register is a single register that combines A0, A1, A2 and A3. The value in the PKHA A Register is limited by the LTC PKHA A Size (LTC0_PKASZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.27.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_A															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_A															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.27.4 Fields

Field	Function
31-0 PKHA_A	A VALUE

42.10.28 LTC PKHA A1 (LTC0_PKA1_a)

42.10.28.1 Address

For a = 0 to 15:

Register	Offset
LTC0_PKA1_a	840h + (a × 4h)

42.10.28.2 Function

The LTC PKHA A1 Register contains a numeric value of up to 64 bytes, right-justified. The LSByte is in offset 840h, in the right-most byte. The LTC PKHA A1 register is 512 bits in length. Note that PKHA A3, A2, A1 and A0 Registers may be combined to contain a value of up to 2048 bits, with A0 containing the least-significant 64 bytes of this value. The value in the PKHA A1 Register, if used as a separate value, is limited by the LTC PKHA A Size (LTC0_PKASZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.28.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_A1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_A1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.28.4 Fields

Field	Function
31-0 PKHA_A1	A1 VALUE

42.10.29 LTC PKHA A2 (LTC0_PKA2_a)

42.10.29.1 Address

For a = 0 to 15:

Register	Offset
LTC0_PKA2_a	880h + (a × 4h)

42.10.29.2 Function

The LTC PKHA A2 Register contains a numeric value of up to 64 bytes, right-justified. The LSByte is in offset 880h, in the right-most byte. The LTC PKHA A2 register is 512 bits in length. Note that PKHA A3, A2, A1 and A0 Registers may be combined to contain a value of up to 2048 bits, with A0 containing the least-significant 64 bytes of this value. The value in the PKHA A2 Register, if used as a separate value, is limited by the LTC PKHA A Size (LTC0_PKASZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.29.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_A2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_A2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.29.4 Fields

Field	Function
31-0 PKHA_A2	A2 VALUE

42.10.30 LTC PKHA A3 (LTC0_PKA3_a)

42.10.30.1 Address

For a = 0 to 15:

Register	Offset
LTC0_PKA3_a	8C0h + (a × 4h)

42.10.30.2 Function

The LTC PKHA A3 Register contains a numeric value of up to 64 bytes, right-justified. The LSByte is in offset 8C0h, in the right-most byte. The LTC PKHA A3 register is 512 bits in length. Note that PKHA A3, A2, A1 and A0 Registers may be combined to contain a value of up to 2048 bits, with A0 containing the least-significant 64 bytes of this value. The value in the PKHA A3 Register, if used as a separate value, is limited by the LTC PKHA A Size (LTC0_PKASZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.30.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_A3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_A3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.30.4 Fields

Field	Function
31-0	A3 VALUE

Field	Function
PKHA_A3	

42.10.31 LTC PKHA B0 (LTC0_PKB0_a)

42.10.31.1 Address

For a = 0 to 15:

Register	Offset
LTC0_PKB0_a	A00h + (a × 4h)

42.10.31.2 Function

The LTC PKHA B0 Register contains a numeric value of up to 64 bytes, right-justified. The LSByte is in offset A00h, in the right-most byte. The LTC PKHA B0 register is 512 bits in length. Note that PKHA B3, B2, B1 and B0 Registers may be combined to contain a value of up to 2048 bits, with B0 containing the least-significant 64 bytes of this value. The value in the PKHA B0 Register (or in {B3, B2, B1, B0} if used as a single value) is limited by the LTC PKHA B Size (LTC0_PKBSZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTC Mode (PublicKey) (LTC0_MDPK) contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.31.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_B0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_B0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.31.4 Fields

Field	Function
31-0 PKHA_B0	B0 VALUE

42.10.32 LTC PKHA B (LTC0_PKB_a)

42.10.32.1 Address

For a = 0 to 63:

Register	Offset
LTC0_PKB_a	A00h + (a × 4h)

42.10.32.2 Function

The LTC PKHA B Register contains a numeric value of up to 256 bytes, right-justified. The LSByte is in offset A00h, in the right-most byte. The LTC PKHA B register is 2048 bits in length. Note that PKHA B Register is a single register that combines B0, B1, B2 and B3. The value in the PKHA B Register is limited by the LTC PKHA B Size (LTC0_PKBSZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.32.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_B															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_B															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.32.4 Fields

Field	Function
31-0 PKHA_B	B VALUE

42.10.33 LTC PKHA B1 (LTC0_PKB1_a)

42.10.33.1 Address

For a = 0 to 15:

Register	Offset
LTC0_PKB1_a	A40h + (a × 4h)

42.10.33.2 Function

The LTC PKHA B1 Register contains a numeric value of up to 64 bytes, right-justified. The LSByte is in offset A40h, in the right-most byte. The LTC PKHA B1 register is 512 bits in length. Note that PKHA B3, B2, B1 and B0 Registers may be combined to contain a value of up to 2048 bits, with B0 containing the least-significant 64 bytes of this value. The value in the PKHA B1 Register, if used as a separate value, is limited by the LTC PKHA B Size (LTC0_PKBSZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.33.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_B1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_B1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.33.4 Fields

Field	Function
31-0 PKHA_B1	B1 VALUE

42.10.34 LTC PKHA B2 (LTC0_PKB2_a)

42.10.34.1 Address

For a = 0 to 15:

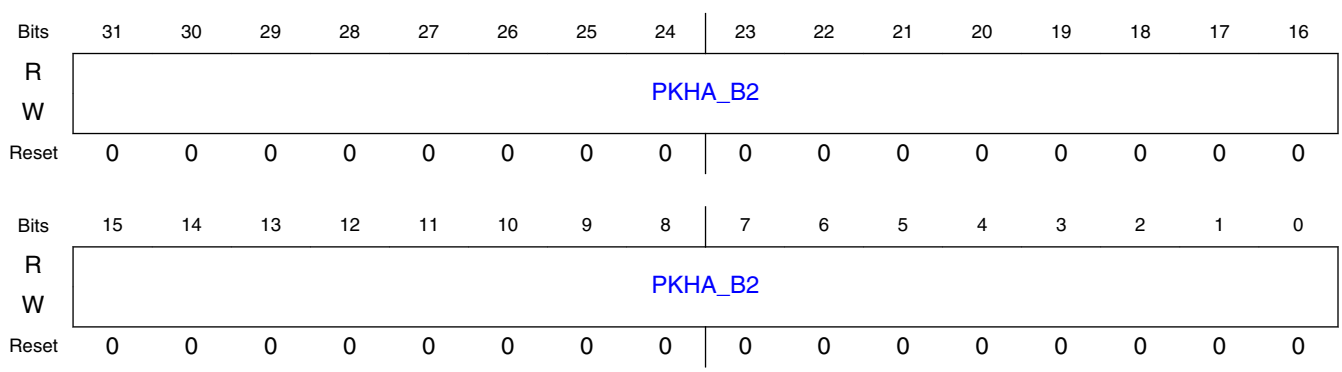
Register	Offset
LTC0_PKB2_a	A80h + (a × 4h)

42.10.34.2 Function

The LTC PKHA B2 Register contains a numeric value of up to 64 bytes, right-justified. The LSByte is in offset A80h, in the right-most byte. The LTC PKHA B2 register is 512 bits in length. Note that PKHA B3, B2, B1 and B0 Registers may be combined to contain a value of up to 2048 bits, with B0 containing the least-significant 64 bytes of this value. The value in the PKHA B2 Register, if used as a separate value, is limited by the LTC PKHA B Size (LTC0_PKBSZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.34.3 Diagram



42.10.34.4 Fields

Field	Function
31-0	B2 VALUE

Field	Function
PKHA_B2	

42.10.35 LTC PKHA B3 (LTC0_PKB3_a)

42.10.35.1 Address

For a = 0 to 15:

Register	Offset
LTC0_PKB3_a	AC0h + (a × 4h)

42.10.35.2 Function

The LTC PKHA B3 Register contains a numeric value of up to 64 bytes, right-justified. The LSByte is in offset AC0h, in the right-most byte. The LTC PKHA B3 register is 512 bits in length. Note that PKHA B3, B2, B1 and B0 Registers may be combined to contain a value of up to 2048 bits, with B0 containing the least-significant 64 bytes of this value. The value in the PKHA B3 Register, if used as a separate value, is limited by the LTC PKHA B Size (LTC0_PKBSZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.35.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_B3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_B3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.35.4 Fields

Field	Function
31-0 PKHA_B3	B3 VALUE

42.10.36 LTC PKHA N0 (LTC0_PKN0_a)

42.10.36.1 Address

For a = 0 to 15:

Register	Offset
LTC0_PKN0_a	C00h + (a × 4h)

42.10.36.2 Function

The LTC PKHA N0 Register contains a numeric value of up to 64 bytes, right-justified. The LSByte is in offset C00h, in the right-most byte. The LTC PKHA N0 register is 512 bits in length. Note that PKHA N3, N2, N1 and N0 Registers may be combined to contain a value of up to 2048 bits, with N0 containing the least-significant 64 bytes of this value. The value in the PKHA N0 Register (or {N3, N2, N1, N0}, if used as a single value) is limited by the LTC PKHA N Size (LTC0_PKNSZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.36.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_N0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_N0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.36.4 Fields

Field	Function
31-0 PKHA_N0	N0 VALUE

42.10.37 LTC PKHA N (LTC0_PKN_a)

42.10.37.1 Address

For a = 0 to 63:

Register	Offset
LTC0_PKN_a	C00h + (a × 4h)

42.10.37.2 Function

The LTC PKHA N Register contains a numeric value of up to 256 bytes, right-justified. The LSByte is in offset C00h, in the right-most byte. The LTC PKHA N register is 2048 bits in length. Note that PKHA N Register is a single register that combines N0, N1, N2 and N3. The value in the PKHA N Register is limited by the LTC PKHA N Size (LTC0_PKNSZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.37.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_N															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_N															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.37.4 Fields

Field	Function
31-0 PKHA_N	N VALUE

42.10.38 LTC PKHA N1 (LTC0_PKN1_a)

42.10.38.1 Address

For a = 0 to 15:

Register	Offset
LTC0_PKN1_a	C40h + (a × 4h)

42.10.38.2 Function

The LTC PKHA N1 Register contains a numeric value of up to 64 bytes, right-justified. The LSByte is in offset C40h, in the right-most byte. The LTC PKHA N1 register is 512 bits in length. Note that PKHA N3, N2, N1 and N0 Registers may be combined to contain a value of up to 2048 bits, with N0 containing the least-significant 64 bytes of this value. The value in the PKHA N1 Register, if used as a separate value, is limited by the LTC PKHA N Size (LTC0_PKNSZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.38.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_N1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_N1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.38.4 Fields

Field	Function
31-0 PKHA_N1	N1 VALUE

42.10.39 LTC PKHA N2 (LTC0_PKN2_a)

42.10.39.1 Address

For a = 0 to 15:

Register	Offset
LTC0_PKN2_a	C80h + (a × 4h)

42.10.39.2 Function

The LTC PKHA N2 Register contains a numeric value of up to 64 bytes, right-justified. The LSByte is in offset C80h, in the right-most byte. The LTC PKHA N2 register is 512 bits in length. Note that PKHA N3, N2, N1 and N0 Registers may be combined to contain a value of up to 2048 bits, with N0 containing the least-significant 64 bytes of this value. The value in the PKHA N2 Register, if used as a separate value, is limited by the LTC PKHA N Size (LTC0_PKNSZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.39.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	PKHA_N2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PKHA_N2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.39.4 Fields

Field	Function
31-0	N2 VALUE

Field	Function
PKHA_N2	

42.10.40 LTC PKHA N3 (LTC0_PKN3_a)

42.10.40.1 Address

For a = 0 to 15:

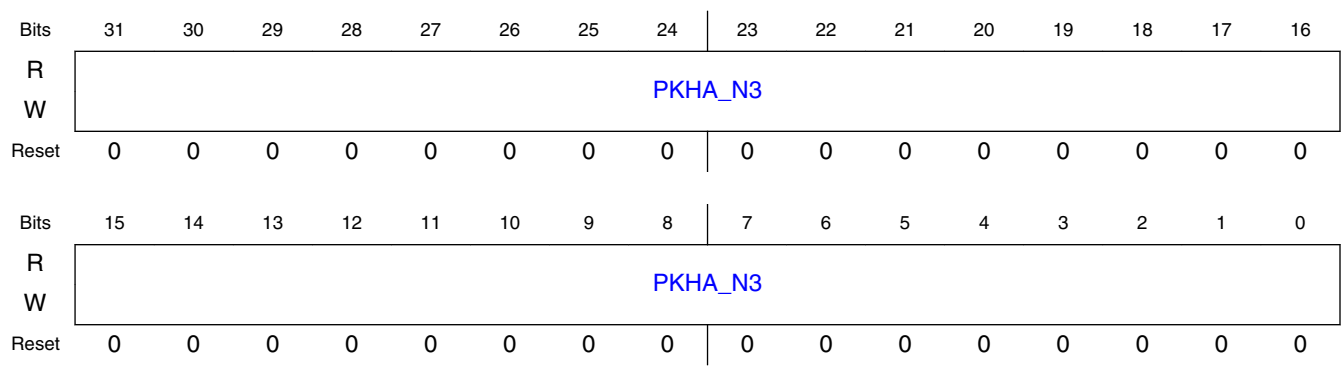
Register	Offset
LTC0_PKN3_a	CC0h + (a × 4h)

42.10.40.2 Function

The LTC PKHA N3 Register contains a numeric value of up to 64 bytes, right-justified. The LSByte is in offset CC0h, in the right-most byte. The LTC PKHA N3 register is 512 bits in length. Note that PKHA N3, N2, N1 and N0 Registers may be combined to contain a value of up to 2048 bits, with N0 containing the least-significant 64 bytes of this value. The value in the PKHA N3 Register, if used as a separate value, is limited by the LTC PKHA N Size (LTC0_PKNSZ).

Note that the PKHA Registers can be read/written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to PKHA Registers will be ignored, and reads of PKHA Registers will return a value of zero.

42.10.40.3 Diagram



42.10.40.4 Fields

Field	Function
31-0 PKHA_N3	N3 VALUE

42.10.41 LTC PKHA E (LTC0_PKE_a)

42.10.41.1 Address

For a = 0 to 63:

Register	Offset
LTC0_PKE_a	E00h + (a × 4h)

42.10.41.2 Function

The LTC PKHA E Register contains a numeric value of up to 256 bytes, right-justified. The LSByte is in offset E00h, in the right-most byte. The LTC PKHA E register is 2048 bits in length. The value in the PKHA E Register is limited by the LTC PKHA E Size (LTC0_PKESZ).

Note that the PKHA E Register can be written only when the LTC Mode (PublicKey) (LTC0_MDPK) does not contain a value enabling a PKHA operation. If the LTCMR_PK contains a PKHA operation mode value, then writes to the PKHA E Register will be ignored.

42.10.41.3 Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W	PKHA_E															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W	PKHA_E															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.10.41.4 Fields

Field	Function
31-0 PKHA_E	E VALUE

Chapter 43
Analog-to-Digital Converter (ADC)

43.1 Chip-specific ADC information

43.1.1 DMA Support on ADC

Applications may require continuous sampling of the ADC (4K samples/sec) that may have considerable load on the CPU. Though using PDB to trigger ADC may reduce some CPU load, the ADC supports DMA request functionality for higher performance when the ADC is sampled at a very high rate or cases where PDB is bypassed. The ADC can trigger the DMA (via DMA req) on conversion completion.

43.1.2 ADC0 Connections/Channel Assignment

NOTE

As indicated by the following sections, each ADCx_DPx input and certain ADCx_DMx inputs may operate as single-ended ADC channels in single-ended mode.

NOTE

Some ADC inputs may not appear on all packages. Please refer to Pinouts for more information.

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)	Direct connection
00000	DAD0	ADC0_DP0 and ADC0_DM0	ADC0_DP0	Yes
00001	DAD1	ADC0_DP1 and ADC0_DM1	ADC0_DP1	Yes
00010	DAD2	Reserved	Reserved	Yes

Table continues on the next page...

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)	Direct connection
00011	DAD3	ADC0_DP3 and ADC0_DM3	ADC0_DP3	Yes
00100	AD4a	Reserved	ADC0_SE4a	via ADC0MUX0
00101	AD5a	Reserved	ADC0_SE5a	via ADC0MUX0
00110	AD6a	Reserved	ADC0_SE6a	via ADC0MUX0
00111	AD7a	Reserved	ADC0_SE7a	via ADC0MUX0
00100	AD4b	Reserved	ADC0_SE4b	via ADC0MUX0
00101	AD5b	Reserved	ADC0_SE5b	via ADC0MUX0
00110	AD6b	Reserved	ADC0_SE6b	via ADC0MUX0
00111	AD7b	Reserved	ADC0_SE7b	via ADC0MUX0
01000	AD8	Reserved	ADC0_SE8	via ADC0MUX1
01001	AD9	Reserved	ADC0_SE9	via ADC0MUX1
01010	AD10	Reserved	ADC0_SE10	via ADC0MUX1
01011	AD11	Reserved	ADC0_SE11	via ADC0MUX1
01100	AD12	Reserved	ADC0_SE12	via ADC0MUX1
01101	AD13	Reserved	ADC0_SE13	via ADC0MUX1
01110	AD14	Reserved	ADC0_SE14	via ADC0MUX1
01111	AD15	Reserved	ADC0_SE15	via ADC0MUX1
10000	AD16	Reserved	Reserved	via ADC0MUX2
10001	AD17	Reserved	ADC0_DM0	via ADC0MUX2
10010	AD18	Reserved	ADC0_DM1	via ADC0MUX2
10011	AD19	Reserved	Reserved	via ADC0MUX2
10100	AD20	Reserved	ADC0_DM3	via ADC0MUX2
10101	AD21	Reserved	VBAT	via ADC0MUX2
10110	AD22	Reserved	VREF_OUT/ ADC0_SE22	via ADC0MUX2
10111	AD23	Reserved	12-bit DAC0 Output/ ADC0_SE23	via ADC0MUX2
11000	AD24	Sense bus (for test)	Reserved	Yes
11001	AD25	Reserved	Reserved	N/A (Fixed)
11010	AD26	Temperature Sensor (Diff)	Temperature Sensor (S.E)	N/A (Fixed)
11011	AD27	Bandgap (Diff)[1]	Bandgap (S.E)[21]	N/A (Fixed)
11100	AD28	Reserved	Reserved	N/A (Fixed)
11101	AD29	-VREFH (Diff)	VREFH (S.E)	N/A (Fixed)
11110	AD30	Reserved	VREFL	N/A (Fixed)
11111	AD31	Module Disabled	Module Disabled	N/A (Fixed)

1. This is the PMC bandgap 1V reference voltage. Prior to reading from this ADC channel, ensure that you enable the bandgap buffer by setting the PMC_REGSC[BGBE] bit. Refer to the device data sheet for the bandgap voltage (VBG) specification.

43.1.3 ADC Channels MUX Selection

The following figure shows the assignment of ADCx_SEn channels a and b through a MUX selection to ADC. To select between alternate set of channels, refer to ADCx_CFG2[MUXSEL] bit settings for more details.

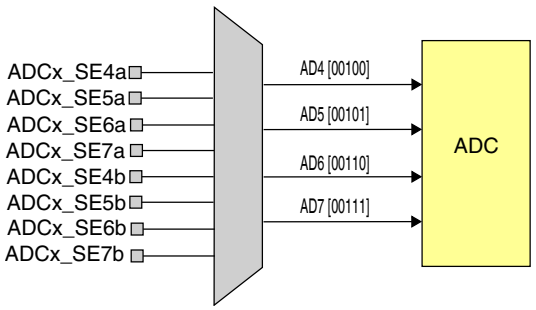


Figure 43-1. ADCx_SEn channels a and b selection

43.1.4 ADC Reference Options

The ADC supports the following references:

- VREFH/VREFL - connected as the primary reference option
- 1.2 V VREF_OUT - connected as the V_{ALT} reference option

ADCx_SC2[REFSEL] bit selects the voltage reference sources for ADC. Refer to REFSEL description in ADC chapter for more details.

43.1.5 VBAT connection to ADC input channel

The VBAT supply input can be converted as a single ended input to an ADC channel input. See ADC0 Connections/Channel Assignment for more details. When VBAT is greater than the selected voltage reference, the conversion result will show a saturated result (~0xFFFF in 16-bit operation). When measuring the VBAT voltage level the ADC should be configured for a long sample time (ADCx_CFG1[ADLSMP]=1, ADCx_CFG2[ADLSTS]=00).

43.1.6 ADC triggers

The ADC supports both software and hardware triggers. The primary hardware mechanism for triggering the ADC is the PDB. The PDB itself can be triggered by other peripherals. For example: RTC (Alarm, Seconds) signal is connected to the PDB. The PDB input trigger can receive the RTC (alarm/seconds) trigger forcing ADC conversions in run mode (where PDB is enabled). On the other hand, the ADC can conduct conversions in low power modes, not triggered by PDB. This allows the ADC to do conversions in low power mode and store the output in the result register. The ADC generates interrupt when the data is ready in the result register that wakes the system from low power mode. The PDB can also be bypassed by using the ADCxTRGSEL bits in the SIM_SOPT7 register.

Table 43-1. ADC Alternate trigger options

SIM_SOPT7[ADCxTRGSEL]	Selected source
00000	PDB external trigger pin input (PDB0_EXTRG)
00001	High speed comparator 0 output
00010	High speed comparator 1 output
00011	High speed comparator 2 output
00100	PIT trigger 0
00101	PIT trigger 1
00110	PIT trigger 2
00111	PIT trigger 3
01000	FTM0 trigger
01001	FTM1 trigger
01010	FTM2 trigger
01011	FTM3 trigger
01100	RTC alarm
01101	RTC Seconds
01110	Low-power timer (LPTMR) trigger
01111	TPM1 channel 0 (A pretrigger) and channel 1 (B pretrigger)

The TPM can also trigger the ADC. TPM1 can trigger ADC0.

For operation of triggers in different modes, refer to Power Management chapter.

43.1.7 ADC conversion clock options

The ADC has multiple input clock sources. Selection is determined by ADCx_CFG1[ADICLK] bitfield. The following table shows the chip-specific clock assignments for this bitfield.

NOTE

The ALTCLK option is only usable when OSCERCLK is in the MHz range. A system with OSCERCLK in the kHz range has the optional clock source below minimum ADC clock operating frequency.

Table 43-2. ADC Conversion Clock Options

ADCx_CFG1[ADICLK]	ADC defined selection	Chip clock	Note
00	Bus Clock	Bus Clock	
01	ALTCLK2	IRC48MCLK	Note [1]
10	ALTCLK	OSCERCLK	Note [1]
11	Asynchronous clock (ADACK)	N/A - sourced from within ADC block	Note[1]

1. For ADC operation in Compute only, PSTOP1, Stop and VLPS, ADACK and the alternate clock sources are allowed clock sources. Note however that ALTCLK2 is force disabled and therefore not available in VLPS.

43.1.8 ADC low-power modes

This table shows the ADC low-power modes and the corresponding chip low-power modes.

Table 43-3. ADC low-power modes

Module mode	Chip mode
Wait	Wait, VLPW
Normal Stop	Stop, VLPS
Low Power Stop	LLS, VLLS3, VLLS2, VLLS1, VLLS0

43.2 Introduction

The 16-bit analog-to-digital converter (ADC) is a successive approximation ADC designed for operation within an integrated microcontroller system-on-chip.

NOTE

For the chip specific modes of operation, see the power management information of the device.

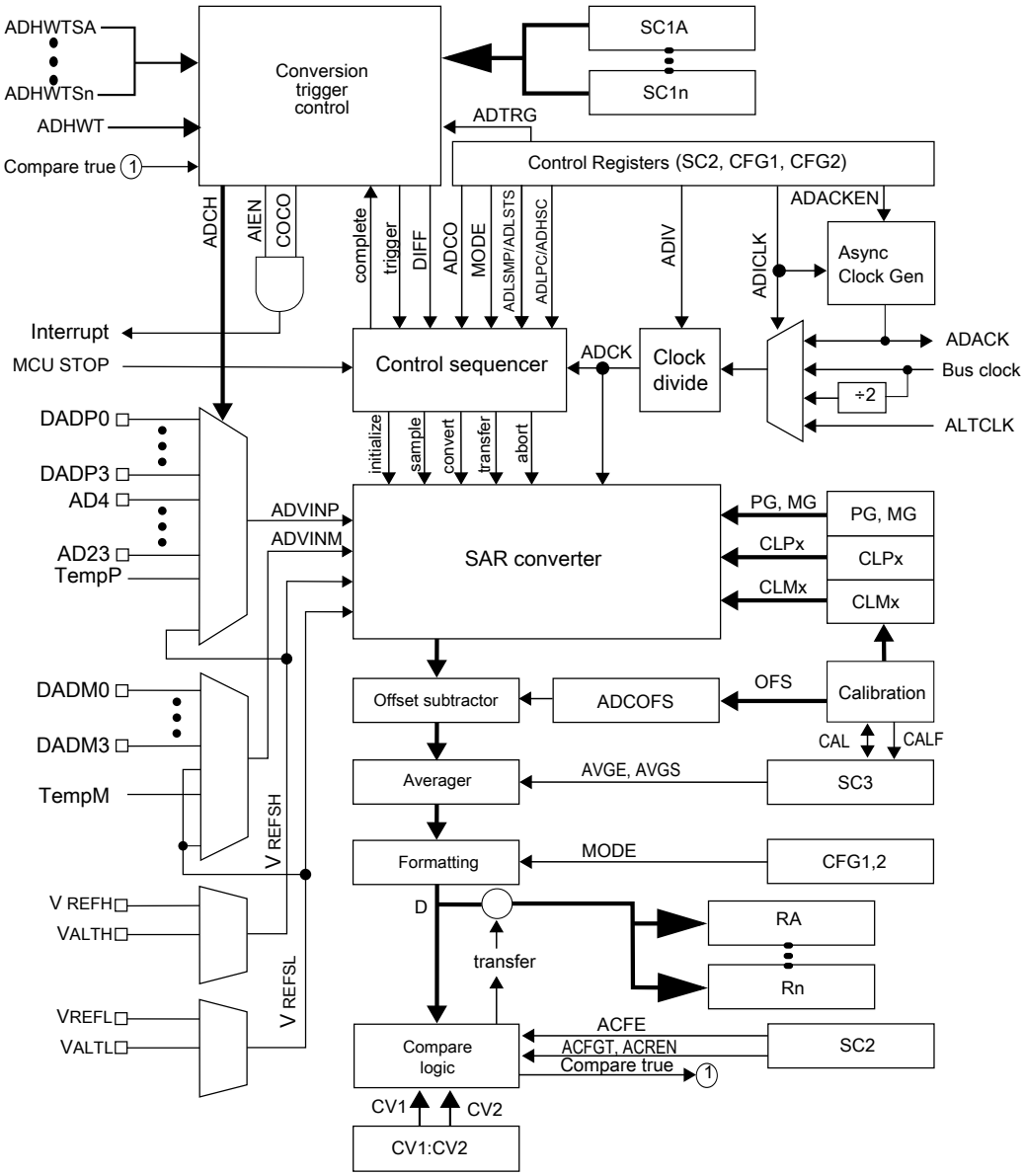
43.2.1 Features

Following are the features of the ADC module.

- Linear successive approximation algorithm with up to 16-bit resolution
- Up to four pairs of differential and 24 single-ended external analog inputs
- Output modes:
  - differential 16-bit, 13-bit, 11-bit, and 9-bit modes
  - single-ended 16-bit, 12-bit, 10-bit, and 8-bit modes
- Output format in 2's complement 16-bit sign extended for differential modes
- Output in right-justified unsigned format for single-ended
- Single or continuous conversion, that is, automatic return to idle after single conversion
- Configurable sample time and conversion speed/power
- Conversion complete/hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in low-power modes for lower noise
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable hardware conversion trigger with hardware channel select
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function
- Selectable voltage reference: external or alternate
- Self-Calibration mode

43.2.2 Block diagram

The following figure is the ADC module block diagram.


ADHWTSA
ADHWTSn
ADHWT
Compare true
Conversion trigger control
SC1A
SC1n
ADTRG
Control Registers (SC2, CFG1, CFG2)
ADACKEN
Async Clock Gen
ADICLK
ADIV
ADCH
AIEN
COCO
complete
trigger
DIFF
ADCO
MODE
ADLSMP/ADLSTS
ADLPC/ADHSC
Interrupt
MCU STOP
Control sequencer
ADCK
Clock divide
ADACK
Bus clock
÷2
ALTCLK
initialize
sample
convert
transfer
abort
DADP0
DADP3
AD4
AD23
TempP
ADVINP
ADVINM
SAR converter
PG, MG
CLPx
CLMx
DADM0
DADM3
TempM
Offset subtractor
ADCOFS
OFS
Calibration
CAL
CALF
Averager
AVGE, AVGS
SC3
Formatting
MODE
CFG1,2
V REFSH
V REFH
VALTH
V REFSL
VREFL
VALTL
D
transfer
RA
Rn
Compare logic
ACFE
ACFGT, ACREN
SC2
CV1
CV2
CV1:CV2

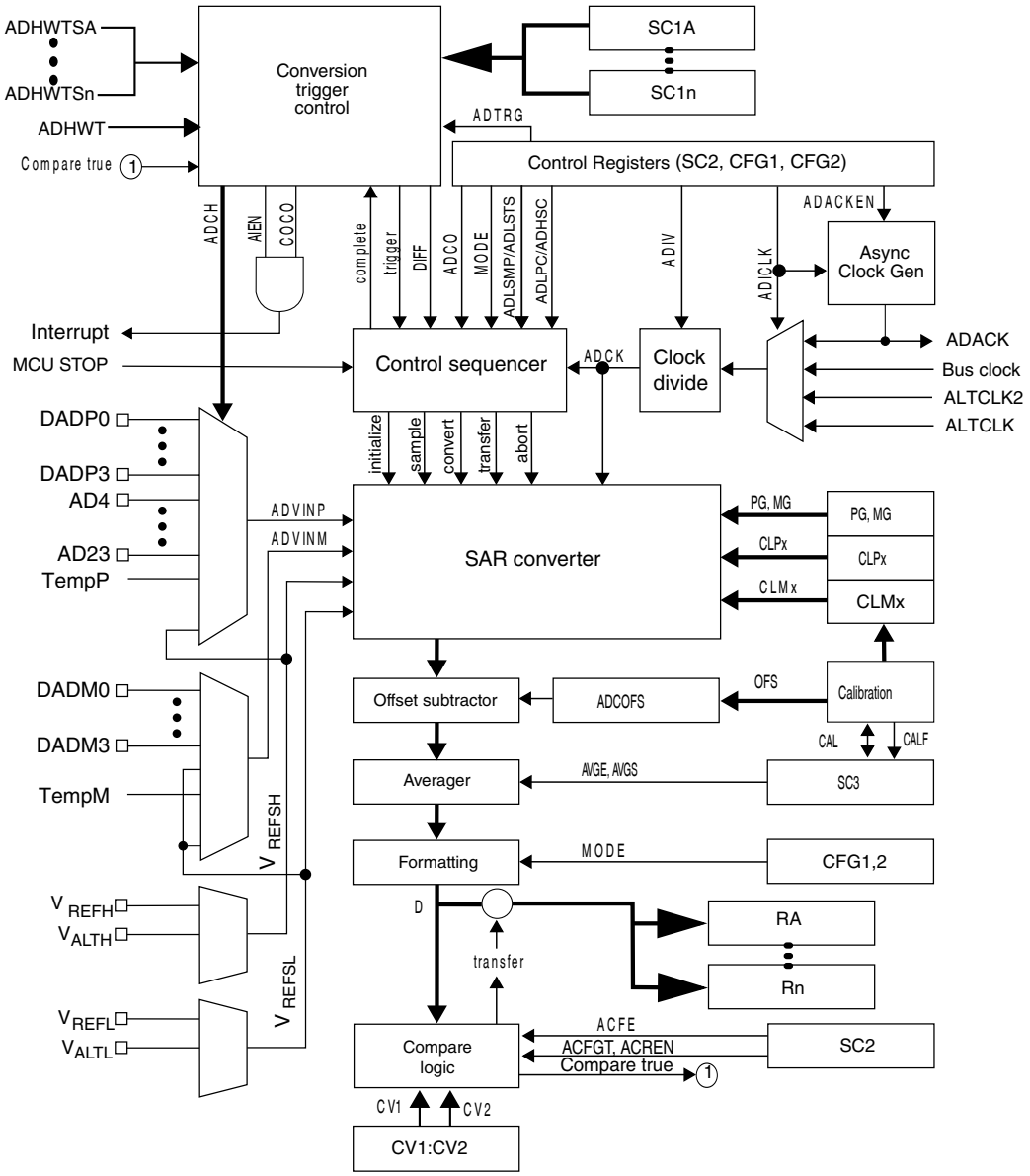


Figure 43-2. ADC block diagram

43.3 ADC signal descriptions

The ADC module supports up to 4 pairs of differential inputs and up to 24 single-ended inputs.

Each differential pair requires two inputs, DADPx and DADMx. The ADC also requires four supply/reference/ground connections.

NOTE

For the number of channels supported on this device as well as information regarding other chip-specific inputs into the ADC block, see the chip-specific ADC configuration information.

Table 43-4. ADC signal descriptions

Signal	Description	I/O
DADP3–DADP0	Differential Analog Channel Inputs	I
DADM3–DADM0	Differential Analog Channel Inputs	I
AD*n*	Single-Ended Analog Channel Inputs	I
V_{REFSH}	Voltage Reference Select High	I
V_{REFSL}	Voltage Reference Select Low	I
V_{DDA}	Analog Power Supply	I
V_{SSA}	Analog Ground	I

43.3.1 Analog Power (V_{DDA})

The ADC analog portion uses V_{DDA} as its power connection. In some packages, V_{DDA} is connected internally to V_{DD}. If externally available, connect the V_{DDA} pin to the same voltage potential as V_{DD}. External filtering may be necessary to ensure clean V_{DDA} for good results.

43.3.2 Analog Ground (V_{SSA})

The ADC analog portion uses V_{SSA} as its ground connection. In some packages, V_{SSA} is connected internally to V_{SS}. If externally available, connect the V_{SSA} pin to the same voltage potential as V_{SS}.

43.3.3 Voltage Reference Select

V_{REFSH} and V_{REFSL} are the high and low reference voltages for the ADC module.

The ADC can be configured to accept one of two voltage reference pairs for V_{REFSH} and V_{REFSL}. Each pair contains a positive reference that must be between the minimum Ref Voltage High and V_{DDA}, and a ground reference that must be at the same potential as V_{SSA}. The two pairs are external (V_{REFH} and V_{REFL}) and alternate (V_{ALTH} and V_{ALTL}). These voltage references are selected using SC2[REFSEL]. The alternate V_{ALTH} and

V_{ALTL} voltage reference pair may select additional external pins or internal sources depending on MCU configuration. See the chip configuration information on the Voltage References specific to this MCU.

In some packages, V_{REFH} is connected in the package to V_{DDA} and V_{REFL} to V_{SSA}. If externally available, the positive reference(s) may be connected to the same potential as V_{DDA} or may be driven by an external source to a level between the minimum Ref Voltage High and the V_{DDA} potential. V_{REFH} must never exceed V_{DDA}. Connect the ground references to the same voltage potential as V_{SSA}.

43.3.4 Analog Channel Inputs (ADx)

The ADC module supports up to 24 single-ended analog inputs. A single-ended input is selected for conversion through the SC1[ADCH] channel select bits when SC1n[DIFF] is low.

43.3.5 Differential Analog Channel Inputs (DADx)

The ADC module supports up to four differential analog channel inputs. Each differential analog input is a pair of external pins, DADPx and DADMx, referenced to each other to provide the most accurate analog to digital readings. A differential input is selected for conversion through SC1[ADCH] when SC1n[DIFF] is high. All DADPx inputs may be used as single-ended inputs if SC1n[DIFF] is low. In certain MCU configurations, some DADMx inputs may also be used as single-ended inputs if SC1n[DIFF] is low. For ADC connections specific to this device, see the chip-specific ADC information.

43.4 Memory map and register definitions

This section describes the ADC registers.

ADC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_B000	ADC Status and Control Registers 1 (ADC0_SC1A)	32	R/W	0000_001Fh	43.4.1/1341
4003_B004	ADC Status and Control Registers 1 (ADC0_SC1B)	32	R/W	0000_001Fh	43.4.1/1341
4003_B008	ADC Configuration Register 1 (ADC0_CFG1)	32	R/W	0000_0000h	43.4.2/1345
4003_B00C	ADC Configuration Register 2 (ADC0_CFG2)	32	R/W	0000_0000h	43.4.3/1346
4003_B010	ADC Data Result Register (ADC0_RA)	32	R	0000_0000h	43.4.4/1347

Table continues on the next page...

ADC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_B014	ADC Data Result Register (ADC0_RB)	32	R	0000_0000h	43.4.4/1347
4003_B018	Compare Value Registers (ADC0_CV1)	32	R/W	0000_0000h	43.4.5/1349
4003_B01C	Compare Value Registers (ADC0_CV2)	32	R/W	0000_0000h	43.4.5/1349
4003_B020	Status and Control Register 2 (ADC0_SC2)	32	R/W	0000_0000h	43.4.6/1350
4003_B024	Status and Control Register 3 (ADC0_SC3)	32	R/W	0000_0000h	43.4.7/1352
4003_B028	ADC Offset Correction Register (ADC0_OFS)	32	R/W	0000_0004h	43.4.8/1353
4003_B02C	ADC Plus-Side Gain Register (ADC0_PG)	32	R/W	0000_8200h	43.4.9/1354
4003_B030	ADC Minus-Side Gain Register (ADC0_MG)	32	R/W	0000_8200h	43.4.10/ 1354
4003_B034	ADC Plus-Side General Calibration Value Register (ADC0_CLPD)	32	R/W	0000_000Ah	43.4.11/ 1355
4003_B038	ADC Plus-Side General Calibration Value Register (ADC0_CLPS)	32	R/W	0000_0020h	43.4.12/ 1356
4003_B03C	ADC Plus-Side General Calibration Value Register (ADC0_CLP4)	32	R/W	0000_0200h	43.4.13/ 1356
4003_B040	ADC Plus-Side General Calibration Value Register (ADC0_CLP3)	32	R/W	0000_0100h	43.4.14/ 1357
4003_B044	ADC Plus-Side General Calibration Value Register (ADC0_CLP2)	32	R/W	0000_0080h	43.4.15/ 1357
4003_B048	ADC Plus-Side General Calibration Value Register (ADC0_CLP1)	32	R/W	0000_0040h	43.4.16/ 1358
4003_B04C	ADC Plus-Side General Calibration Value Register (ADC0_CLP0)	32	R/W	0000_0020h	43.4.17/ 1358
4003_B054	ADC Minus-Side General Calibration Value Register (ADC0_CLMD)	32	R/W	0000_000Ah	43.4.18/ 1359
4003_B058	ADC Minus-Side General Calibration Value Register (ADC0_CLMS)	32	R/W	0000_0020h	43.4.19/ 1359
4003_B05C	ADC Minus-Side General Calibration Value Register (ADC0_CLM4)	32	R/W	0000_0200h	43.4.20/ 1360
4003_B060	ADC Minus-Side General Calibration Value Register (ADC0_CLM3)	32	R/W	0000_0100h	43.4.21/ 1360
4003_B064	ADC Minus-Side General Calibration Value Register (ADC0_CLM2)	32	R/W	0000_0080h	43.4.22/ 1361
4003_B068	ADC Minus-Side General Calibration Value Register (ADC0_CLM1)	32	R/W	0000_0040h	43.4.23/ 1361
4003_B06C	ADC Minus-Side General Calibration Value Register (ADC0_CLM0)	32	R/W	0000_0020h	43.4.24/ 1362

43.4.1 ADC Status and Control Registers 1 (ADC*x*_SC1*n*)

SC1A is used for both software and hardware trigger modes of operation.

To allow sequential conversions of the ADC to be triggered by internal peripherals, the ADC can have more than one status and control register: one for each conversion. The SC1B–SC1n registers indicate potentially multiple SC1 registers for use only in hardware trigger mode. See the chip configuration information about the number of SC1n registers specific to this device. The SC1n registers have identical fields, and are used in a "ping-pong" approach to control ADC operation.

At any one point in time, only one of the SC1n registers is actively controlling ADC conversions. Updating SC1A while SC1n is actively controlling a conversion is allowed, and vice-versa for any of the SC1n registers specific to this MCU.

Writing SC1A while SC1A is actively controlling a conversion aborts the current conversion. In Software Trigger mode, when SC2[ADTRG]=0, writes to SC1A subsequently initiate a new conversion, if SC1[ADCH] contains a value other than all 1s (module disabled).

Writing any of the SC1n registers while that specific SC1n register is actively controlling a conversion aborts the current conversion. None of the SC1B-SC1n registers are used for software trigger operation and therefore writes to the SC1B–SC1n registers do not initiate a new conversion.

Address: 4003_B000h base + 0h offset + (4d × i), where i=0d to 1d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								COCO	AIEN	DIFF	ADCH				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

ADCx_SC1n field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 COCO	Conversion Complete Flag This is a read-only field that is set each time a conversion is completed when the compare function is disabled, or SC2[ACFE]=0 and the hardware average function is disabled, or SC3[AVGE]=0. When the compare function is enabled, or SC2[ACFE]=1, COCO is set upon completion of a conversion only if the compare result is true. When the hardware average function is enabled, or SC3[AVGE]=1, COCO is set upon completion of the selected number of conversions (determined by AVGS). COCO in SC1A is also set at the completion of a calibration sequence. COCO is cleared when the respective SC1n register is written or when the respective Rn register is read. 0 Conversion is not completed. 1 Conversion is completed.
6 AIEN	Interrupt Enable Enables conversion complete interrupts. When COCO becomes set while the respective AIEN is high, an interrupt is asserted. 0 Conversion complete interrupt is disabled. 1 Conversion complete interrupt is enabled.
5 DIFF	Differential Mode Enable Configures the ADC to operate in differential mode. When enabled, this mode automatically selects from the differential channels, and changes the conversion algorithm and the number of cycles to complete a conversion. 0 Single-ended conversions and input channels are selected. 1 Differential conversions and input channels are selected.
ADCH	Input channel select Selects one of the input channels. The input channel decode depends on the value of DIFF. DAD0-DAD3 are associated with the input pin pairs DADPx and DADMx. **NOTE:** Some of the input channel options in the bitfield-setting descriptions might not be available for your device. For the actual ADC channel assignments for your device, see the Chip Configuration details. The successive approximation converter subsystem is turned off when the channel select bits are all set, that is, ADCH = 11111. This feature allows explicit disabling of the ADC and isolation of the input channel from all sources. Terminating continuous conversions this way prevents an additional single conversion from being performed. It is not necessary to set ADCH to all 1s to place the ADC in a low-power state when continuous conversions are not enabled because the module automatically enters a low-power state when a conversion completes. 00000 When DIFF=0, DADP0 is selected as input; when DIFF=1, DAD0 is selected as input. 00001 When DIFF=0, DADP1 is selected as input; when DIFF=1, DAD1 is selected as input. 00010 When DIFF=0, DADP2 is selected as input; when DIFF=1, DAD2 is selected as input. 00011 When DIFF=0, DADP3 is selected as input; when DIFF=1, DAD3 is selected as input. 00100 When DIFF=0, AD4 is selected as input; when DIFF=1, it is reserved. 00101 When DIFF=0, AD5 is selected as input; when DIFF=1, it is reserved. 00110 When DIFF=0, AD6 is selected as input; when DIFF=1, it is reserved. 00111 When DIFF=0, AD7 is selected as input; when DIFF=1, it is reserved.

Table continues on the next page...

ADC*x*_SC1*n* field descriptions (continued)

Field	Description	
	01000	When DIFF=0, AD8 is selected as input; when DIFF=1, it is reserved.
	01001	When DIFF=0, AD9 is selected as input; when DIFF=1, it is reserved.
	01010	When DIFF=0, AD10 is selected as input; when DIFF=1, it is reserved.
	01011	When DIFF=0, AD11 is selected as input; when DIFF=1, it is reserved.
	01100	When DIFF=0, AD12 is selected as input; when DIFF=1, it is reserved.
	01101	When DIFF=0, AD13 is selected as input; when DIFF=1, it is reserved.
	01110	When DIFF=0, AD14 is selected as input; when DIFF=1, it is reserved.
	01111	When DIFF=0, AD15 is selected as input; when DIFF=1, it is reserved.
	10000	When DIFF=0, AD16 is selected as input; when DIFF=1, it is reserved.
	10001	When DIFF=0, AD17 is selected as input; when DIFF=1, it is reserved.
	10010	When DIFF=0, AD18 is selected as input; when DIFF=1, it is reserved.
	10011	When DIFF=0, AD19 is selected as input; when DIFF=1, it is reserved.
	10100	When DIFF=0, AD20 is selected as input; when DIFF=1, it is reserved.
	10101	When DIFF=0, AD21 is selected as input; when DIFF=1, it is reserved.
	10110	When DIFF=0, AD22 is selected as input; when DIFF=1, it is reserved.
	10111	When DIFF=0, AD23 is selected as input; when DIFF=1, it is reserved.
	11000	Reserved.
	11001	Reserved.
	11010	When DIFF=0, Temp Sensor (single-ended) is selected as input; when DIFF=1, Temp Sensor (differential) is selected as input.
	11011	When DIFF=0,Bandgap (single-ended) is selected as input; when DIFF=1, Bandgap (differential) is selected as input.
	11100	Reserved.
	11101	When DIFF=0,V_{REFSH} is selected as input; when DIFF=1, -V_{REFSH} (differential) is selected as input. Voltage reference selected is determined by SC2[REFSEL].
	11110	When DIFF=0,V_{REFSL} is selected as input; when DIFF=1, it is reserved. Voltage reference selected is determined by SC2[REFSEL].
	11111	Module is disabled.

43.4.2 ADC Configuration Register 1 (ADCx_CFG1)

The configuration Register 1 (CFG1) selects the mode of operation, clock source, clock divide, and configuration for low power or long sample time.

Address: 4003_B000h base + 8h offset = 4003_B008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								ADLPC	ADIV		ADLSMP	MODE		ADICLK	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADCx_CFG1 field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 ADLPC	Low-Power Configuration Controls the power configuration of the successive approximation converter. This optimizes power consumption when higher sample rates are not required. 0 Normal power configuration. 1 Low-power configuration. The power is reduced at the expense of maximum clock speed.
6–5 ADIV	Clock Divide Select Selects the divide ratio used by the ADC to generate the internal clock ADCK. 00 The divide ratio is 1 and the clock rate is input clock. 01 The divide ratio is 2 and the clock rate is (input clock)/2. 10 The divide ratio is 4 and the clock rate is (input clock)/4. 11 The divide ratio is 8 and the clock rate is (input clock)/8.
4 ADLSMP	Sample Time Configuration Selects between different sample times based on the conversion mode selected. This field adjusts the sample period to allow higher impedance inputs to be accurately sampled or to maximize conversion speed for lower impedance inputs. Longer sample times can also be used to lower overall power consumption if continuous conversions are enabled and high conversion rates are not required. When ADLSMP=1, the long sample time select bits, (ADLSTS[1:0]), can select the extent of the long sample time.

Table continues on the next page...

ADCx_CFG1 field descriptions (continued)

Field	Description
	0 Short sample time. 1 Long sample time.
3–2 MODE	Conversion mode selection Selects the ADC resolution mode. 00 When DIFF=0:It is single-ended 8-bit conversion; when DIFF=1, it is differential 9-bit conversion with 2's complement output. 01 When DIFF=0:It is single-ended 12-bit conversion ; when DIFF=1, it is differential 13-bit conversion with 2's complement output. 10 When DIFF=0:It is single-ended 10-bit conversion. ; when DIFF=1, it is differential 11-bit conversion with 2's complement output 11 When DIFF=0:It is single-ended 16-bit conversion..; when DIFF=1, it is differential 16-bit conversion with 2's complement output
ADICLK	Input Clock Select Selects the input clock source to generate the internal clock, ADCK. Note that when the ADACK clock source is selected, it is not required to be active prior to conversion start. When it is selected and it is not active prior to a conversion start, when CFG2[ADACKEN]=0, the asynchronous clock is activated at the start of a conversion and deactivated when conversions are terminated. In this case, there is an associated clock startup delay each time the clock source is re-activated. 00 Bus clock 01 Alternate clock 2 (ALTCLK2) 10 Alternate clock (ALTCLK) 11 Asynchronous clock (ADACK)

43.4.3 ADC Configuration Register 2 (ADCx_CFG2)

Configuration Register 2 (CFG2) selects the special high-speed configuration for very high speed conversions and selects the long sample time duration during long sample mode.

Address: 4003_B000h base + Ch offset = 4003_B00Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								0			MUXSEL	ADACKEN	ADHSC	ADLSTS	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADCx_CFG2 field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 MUXSEL	ADC Mux Select Changes the ADC mux setting to select between alternate sets of ADC channels. 0 ADxxa channels are selected. 1 ADxxb channels are selected.
3 ADACKEN	Asynchronous Clock Output Enable Enables the asynchronous clock source and the clock source output regardless of the conversion and status of CFG1[ADICLK]. Based on MCU configuration, the asynchronous clock may be used by other modules. See chip configuration information. Setting this field allows the clock to be used even while the ADC is idle or operating from a different clock source. Also, latency of initiating a single or first-continuous conversion with the asynchronous clock selected is reduced because the ADACK clock is already operational. 0 Asynchronous clock output disabled; Asynchronous clock is enabled only if selected by ADICLK and a conversion is active. 1 Asynchronous clock and clock output is enabled regardless of the state of the ADC.
2 ADHSC	High-Speed Configuration Configures the ADC for very high-speed operation. The conversion sequence is altered with 2 ADCK cycles added to the conversion time to allow higher speed conversion clocks. 0 Normal conversion sequence selected. 1 High-speed conversion sequence selected with 2 additional ADCK cycles to total conversion time.
ADLSTS	Long Sample Time Select Selects between the extended sample times when long sample time is selected, that is, when CFG1[ADLSMP]=1. This allows higher impedance inputs to be accurately sampled or to maximize conversion speed for lower impedance inputs. Longer sample times can also be used to lower overall power consumption when continuous conversions are enabled if high conversion rates are not required. 00 Default longest sample time; 20 extra ADCK cycles; 24 ADCK cycles total. 01 12 extra ADCK cycles; 16 ADCK cycles total sample time. 10 6 extra ADCK cycles; 10 ADCK cycles total sample time. 11 2 extra ADCK cycles; 6 ADCK cycles total sample time.

43.4.4 ADC Data Result Register (ADCx_R*n*)

The data result registers (Rn) contain the result of an ADC conversion of the channel selected by the corresponding status and channel control register (SC1A:SC1n). For every status and channel control register, there is a corresponding data result register.

Unused bits in R n are cleared in unsigned right-aligned modes and carry the sign bit (MSB) in sign-extended 2's complement modes. For example, when configured for 10-bit single-ended mode, D[15:10] are cleared. When configured for 11-bit differential mode, D[15:10] carry the sign bit, that is, bit 10 extended through bit 15.

The following table describes the behavior of the data result registers in the different modes of operation.

Table 43-5. Data result register description

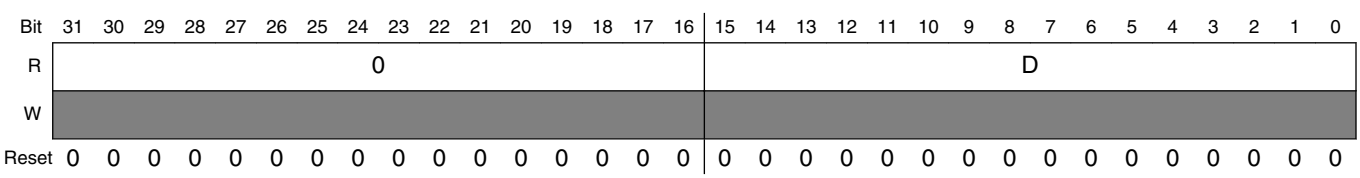
Conversion mode	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Format
16-bit differential	S	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	Signed 2's complement
16-bit single-ended	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	Unsigned right justified
13-bit differential	S	S	S	S	D	D	D	D	D	D	D	D	D	D	D	D	Sign-extended 2's complement
12-bit single-ended	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D	D	Unsigned right-justified
11-bit differential	S	S	S	S	S	S	D	D	D	D	D	D	D	D	D	D	Sign-extended 2's complement
10-bit single-ended	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D	D	Unsigned right-justified
9-bit differential	S	S	S	S	S	S	S	S	D	D	D	D	D	D	D	D	Sign-extended 2's complement
8-bit single-ended	0	0	0	0	0	0	0	0	D	D	D	D	D	D	D	D	Unsigned right-justified

NOTE

S: Sign bit or sign bit extension;

D: Data, which is 2's complement data if indicated

Address: 4003_B000h base + 10h offset + (4d × i), where i=0d to 1d



ADCx_R*n* field descriptions

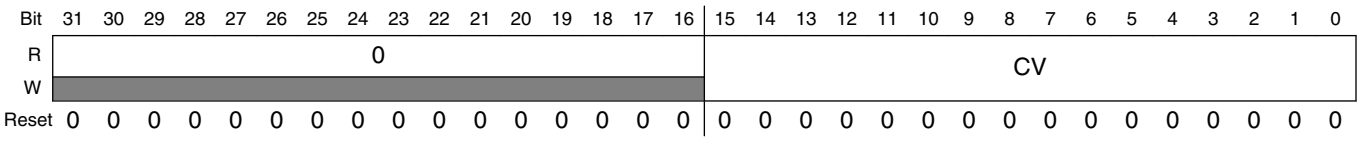
Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
D	Data result

43.4.5 Compare Value Registers (ADC*x*_CV*n*)

The Compare Value Registers (CV1 and CV2) contain a compare value used to compare the conversion result when the compare function is enabled, that is, SC2[ACFE]=1. This register is formatted in the same way as the Rn registers in different modes of operation for both bit position definition and value format using unsigned or sign-extended 2's complement. Therefore, the compare function uses only the CVn fields that are related to the ADC mode of operation.

The compare value 2 register (CV2) is used only when the compare range function is enabled, that is, SC2[ACREN]=1.

Address: 4003_B000h base + 18h offset + (4d × i), where i=0d to 1d



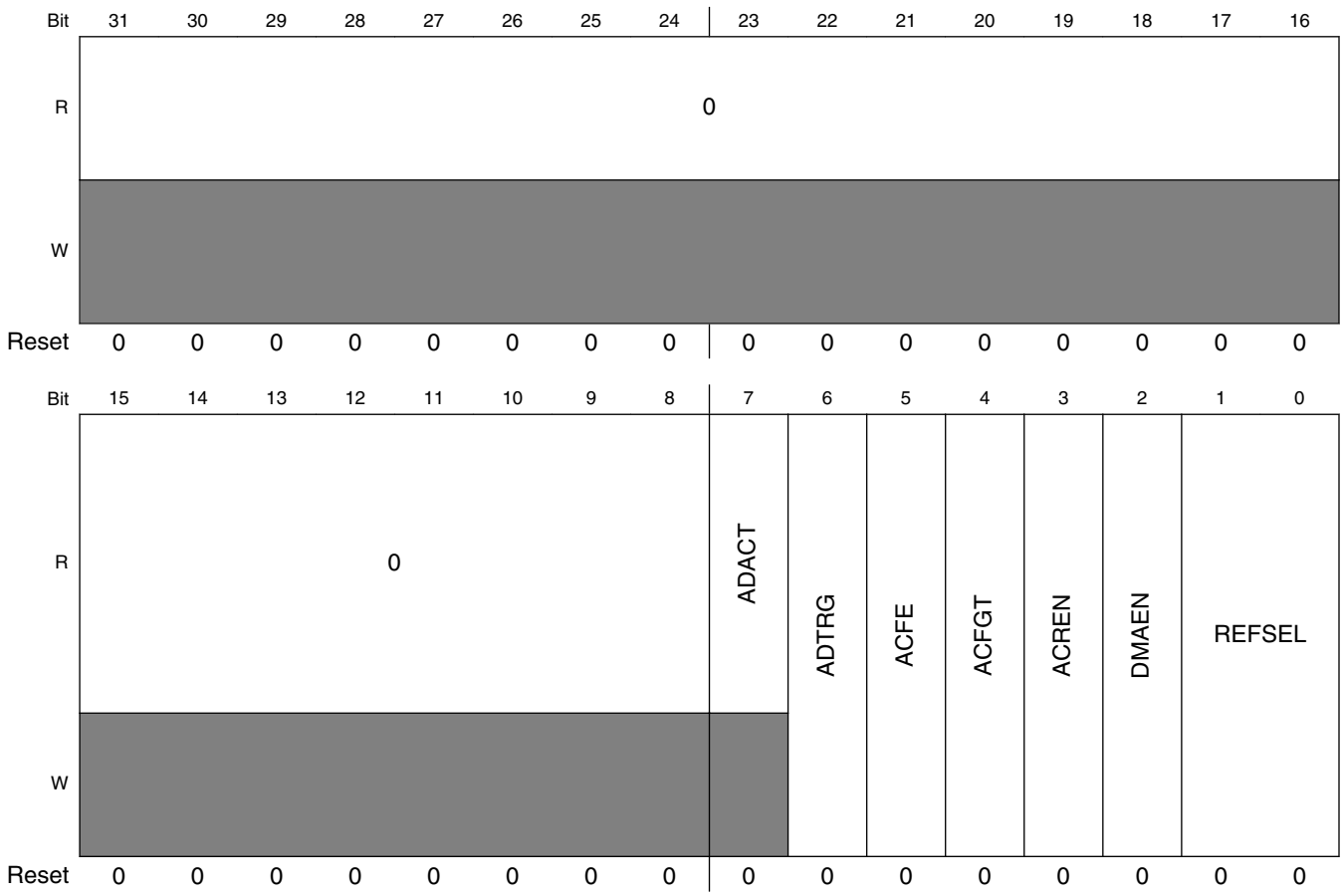
ADC*x*_CV*n* field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CV	Compare Value.

43.4.6 Status and Control Register 2 (ADCx_SC2)

The status and control register 2 (SC2) contains the conversion active, hardware/software trigger select, compare function, and voltage reference select of the ADC module.

Address: 4003_B000h base + 20h offset = 4003_B020h



ADCx_SC2 field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 ADACT	Conversion Active Indicates that a conversion or hardware averaging is in progress. ADACT is set when a conversion is initiated and cleared when a conversion is completed or aborted. 0 Conversion not in progress. 1 Conversion in progress.
6 ADTRG	Conversion Trigger Select Selects the type of trigger used for initiating a conversion. Two types of trigger are selectable:

Table continues on the next page...

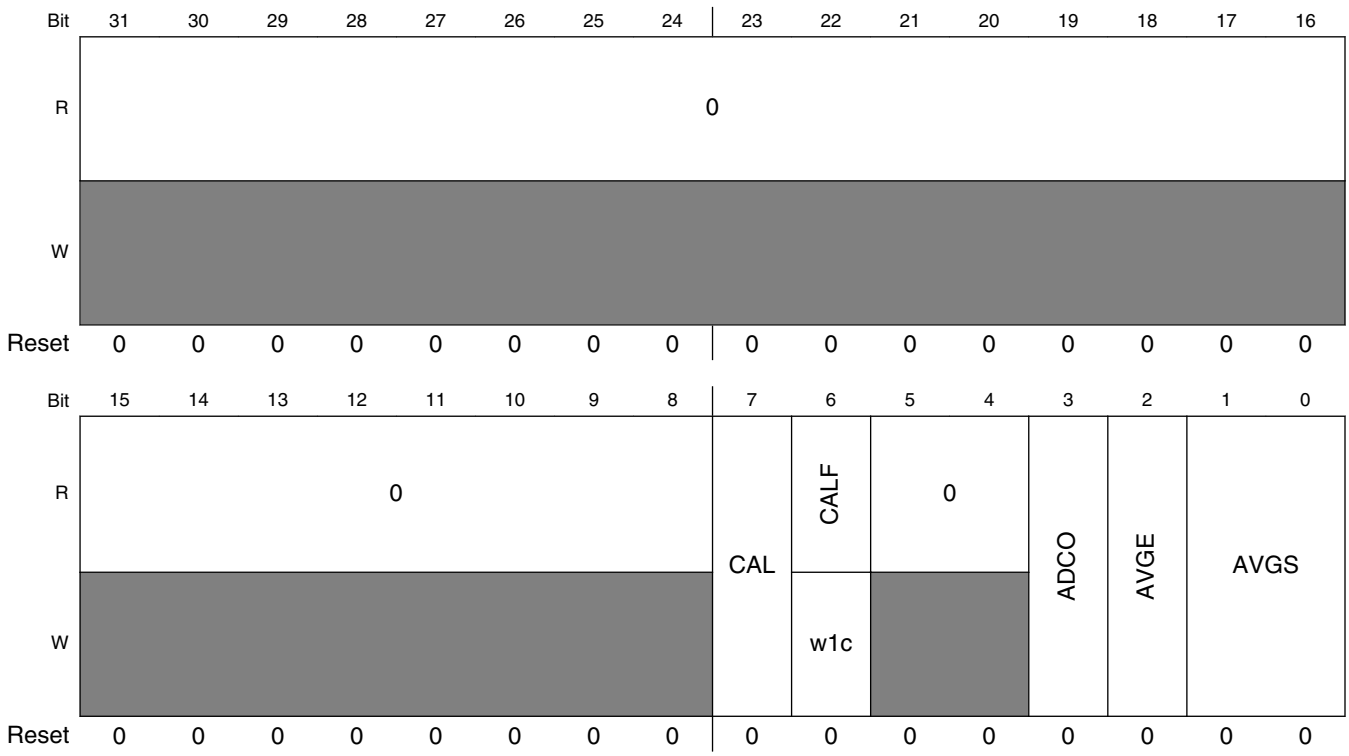
ADCx_SC2 field descriptions (continued)

Field	Description
	• Software trigger: When software trigger is selected, a conversion is initiated following a write to SC1A. • Hardware trigger: When hardware trigger is selected, a conversion is initiated following the assertion of the ADHWT input after a pulse of the ADHWTSn input. 0 Software trigger selected. 1 Hardware trigger selected.
5 ACFE	Compare Function Enable Enables the compare function. 0 Compare function disabled. 1 Compare function enabled.
4 ACFGT	Compare Function Greater Than Enable Configures the compare function to check the conversion result relative to the CV1 and CV2 based upon the value of ACREN. ACFE must be set for ACFGT to have any effect. 0 Configures less than threshold, outside range not inclusive and inside range not inclusive; functionality based on the values placed in CV1 and CV2. 1 Configures greater than or equal to threshold, outside and inside ranges inclusive; functionality based on the values placed in CV1 and CV2.
3 ACREN	Compare Function Range Enable Configures the compare function to check if the conversion result of the input being monitored is either between or outside the range formed by CV1 and CV2 determined by the value of ACFGT. ACFE must be set for ACFGT to have any effect. 0 Range function disabled. Only CV1 is compared. 1 Range function enabled. Both CV1 and CV2 are compared.
2 DMAEN	DMA Enable 0 DMA is disabled. 1 DMA is enabled and will assert the ADC DMA request during an ADC conversion complete event noted when any of the SC1n[COCO] flags is asserted.
REFSEL	Voltage Reference Selection Selects the voltage reference source used for conversions. 00 Default voltage reference pin pair, that is, external pins V_{REFH} and V_{REFL} 01 Alternate reference pair, that is, V_{ALTH} and V_{ALTL} . This pair may be additional external pins or internal sources depending on the MCU configuration. See the chip configuration information for details specific to this MCU 10 Reserved 11 Reserved

43.4.7 Status and Control Register 3 (ADCx_SC3)

The Status and Control Register 3 (SC3) controls the calibration, continuous convert, and hardware averaging functions of the ADC module.

Address: 4003_B000h base + 24h offset = 4003_B024h



ADCx_SC3 field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 CAL	Calibration Begins the calibration sequence when set. This field stays set while the calibration is in progress and is cleared when the calibration sequence is completed. CALF must be checked to determine the result of the calibration sequence. Once started, the calibration routine cannot be interrupted by writes to the ADC registers or the results will be invalid and CALF will set. Setting CAL will abort any current conversion.
6 CALF	Calibration Failed Flag Displays the result of the calibration sequence. The calibration sequence will fail if SC2[ADTRG] = 1, any ADC register is written, or any stop mode is entered before the calibration sequence completes. Writing 1 to CALF clears it. 0 Calibration completed normally. 1 Calibration failed. ADC accuracy specifications are not guaranteed.

Table continues on the next page...

ADCx_SC3 field descriptions (continued)

Field	Description
5–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 ADCO	Continuous Conversion Enable Enables continuous conversions. 0 One conversion or one set of conversions if the hardware average function is enabled, that is, AVGE=1, after initiating a conversion. 1 Continuous conversions or sets of conversions if the hardware average function is enabled, that is, AVGE=1, after initiating a conversion.
2 AVGE	Hardware Average Enable Enables the hardware average function of the ADC. 0 Hardware average function disabled. 1 Hardware average function enabled.
AVGS	Hardware Average Select Determines how many ADC conversions will be averaged to create the ADC average result. 00 4 samples averaged. 01 8 samples averaged. 10 16 samples averaged. 11 32 samples averaged.

43.4.8 ADC Offset Correction Register (ADCx_OFS)

The ADC Offset Correction Register (OFS) contains the user-selected or calibration-generated offset error correction value. This register is a 2's complement, left-justified, 16-bit value . The value in OFS is subtracted from the conversion and the result is transferred into the result registers, Rn. If the result is greater than the maximum or less than the minimum result value, it is forced to the appropriate limit for the current mode of operation.

For more information regarding the calibration procedure, please refer to the Calibration function section.

Address: 4003_B000h base + 28h offset = 4003_B028h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																OFS															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

ADCx_OFS field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
OFS	Offset Error Correction Value

43.4.9 ADC Plus-Side Gain Register (ADCx_PG)

The Plus-Side Gain Register (PG) contains the gain error correction for the plus-side input in differential mode or the overall conversion in single-ended mode. PG, a 16-bit real number in binary format, is the gain adjustment factor, with the radix point fixed between PG[15] and PG[14]. This register must be written by the user with the value described in the calibration procedure. Otherwise, the gain error specifications may not be met.

For more information regarding the calibration procedure, please refer to the Calibration function section.

Address: 4003_B000h base + 2Ch offset = 4003_B02Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																PG															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

ADCx_PG field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
PG	Plus-Side Gain

43.4.10 ADC Minus-Side Gain Register (ADCx_MG)

The Minus-Side Gain Register (MG) contains the gain error correction for the minus-side input in differential mode. This register is ignored in single-ended mode. MG, a 16-bit real number in binary format, is the gain adjustment factor, with the radix point fixed between MG[15] and MG[14]. This register must be written by the user with the value described in the calibration procedure. Otherwise, the gain error specifications may not be met.

For more information regarding the calibration procedure, please refer to the Calibration function section.

Address: 4003_B000h base + 30h offset = 4003_B030h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																MG															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

ADCx_MG field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
MG	Minus-Side Gain

43.4.11 ADC Plus-Side General Calibration Value Register (ADCx_CLPD)

The Plus-Side General Calibration Value Registers (CLPx) contain calibration information that is generated by the calibration function. These registers contain seven calibration values of varying widths: CLP0[5:0], CLP1[6:0], CLP2[7:0], CLP3[8:0], CLP4[9:0], CLPS[5:0], and CLPD[5:0]. CLPx are automatically set when the self-calibration sequence is done, that is, CAL is cleared. If these registers are written by the user after calibration, the linearity error specifications may not be met.

For more information regarding the calibration procedure, please refer to the Calibration function section.

Address: 4003_B000h base + 34h offset = 4003_B034h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																														CLPD	
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

ADCx_CLPD field descriptions

Field	Description
31–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLPD	Calibration Value Calibration Value

43.4.12 ADC Plus-Side General Calibration Value Register (ADCx_CLPS)

For more information, see CLPD register description.

Address: 4003_B000h base + 38h offset = 4003_B038h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																										CLPS					
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

ADCx_CLPS field descriptions

Field	Description
31–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLPS	Calibration Value Calibration Value

43.4.13 ADC Plus-Side General Calibration Value Register (ADCx_CLP4)

For more information, see CLPD register description.

Address: 4003_B000h base + 3Ch offset = 4003_B03Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																										CLP4					
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

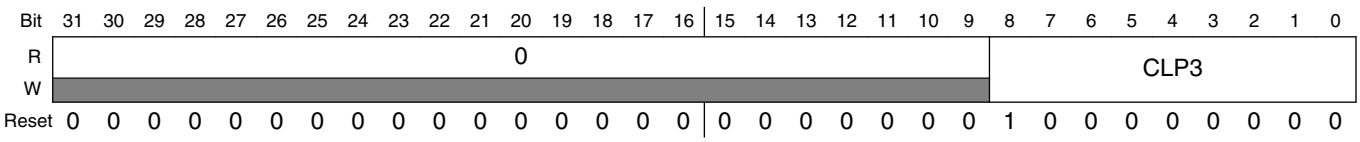
ADCx_CLP4 field descriptions

Field	Description
31–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLP4	Calibration Value Calibration Value

43.4.14 ADC Plus-Side General Calibration Value Register (ADCx_CLP3)

For more information, see CLPD register description.

Address: 4003_B000h base + 40h offset = 4003_B040h



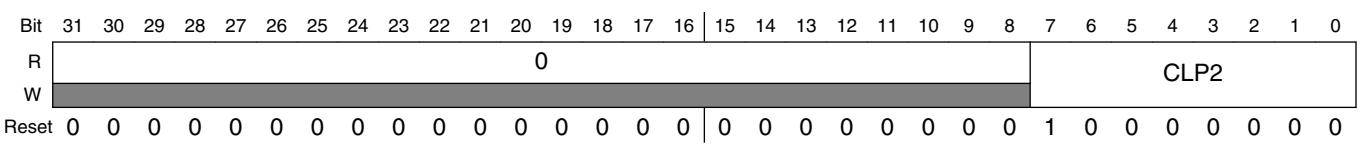
ADCx_CLP3 field descriptions

Field	Description
31–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLP3	Calibration Value Calibration Value

43.4.15 ADC Plus-Side General Calibration Value Register (ADCx_CLP2)

For more information, see CLPD register description.

Address: 4003_B000h base + 44h offset = 4003_B044h



ADCx_CLP2 field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLP2	Calibration Value Calibration Value

43.4.16 ADC Plus-Side General Calibration Value Register (ADCx_CLP1)

For more information, see CLPD register description.

Address: 4003_B000h base + 48h offset = 4003_B048h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																									CLP1						
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

ADCx_CLP1 field descriptions

Field	Description
31–7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLP1	Calibration Value Calibration Value

43.4.17 ADC Plus-Side General Calibration Value Register (ADCx_CLP0)

For more information, see CLPD register description.

Address: 4003_B000h base + 4Ch offset = 4003_B04Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																										CLP0					
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

ADCx_CLP0 field descriptions

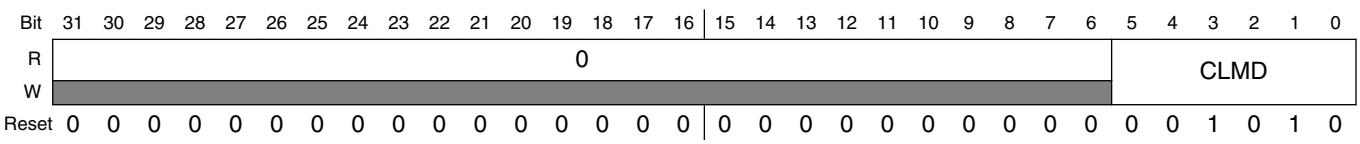
Field	Description
31–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLP0	Calibration Value Calibration Value

43.4.18 ADC Minus-Side General Calibration Value Register (ADCx_CLMD)

The Minus-Side General Calibration Value (CLMx) registers contain calibration information that is generated by the calibration function. These registers contain seven calibration values of varying widths: CLM0[5:0], CLM1[6:0], CLM2[7:0], CLM3[8:0], CLM4[9:0], CLMS[5:0], and CLMD[5:0]. CLMx are automatically set when the self-calibration sequence is done, that is, CAL is cleared. If these registers are written by the user after calibration, the linearity error specifications may not be met.

For more information regarding the calibration procedure, please refer to the Calibration function section.

Address: 4003_B000h base + 54h offset = 4003_B054h



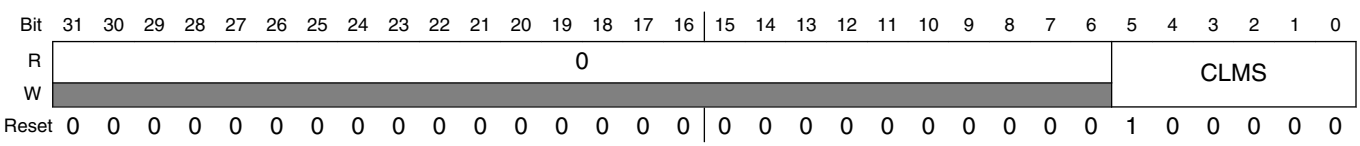
ADCx_CLMD field descriptions

Field	Description
31–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLMD	Calibration Value Calibration Value

43.4.19 ADC Minus-Side General Calibration Value Register (ADCx_CLMS)

For more information, see CLMD register description.

Address: 4003_B000h base + 58h offset = 4003_B058h



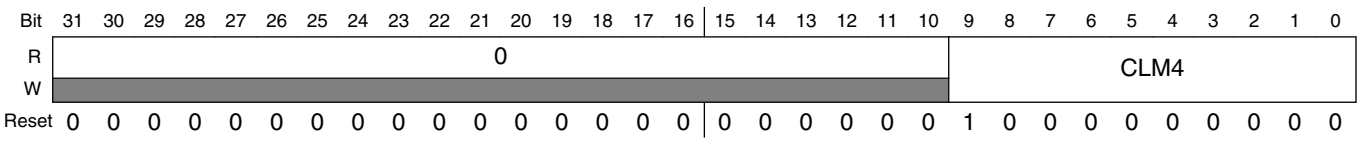
ADCx_CLMS field descriptions

Field	Description
31–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLMS	Calibration Value Calibration Value

43.4.20 ADC Minus-Side General Calibration Value Register (ADCx_CLM4)

For more information, see CLMD register description.

Address: 4003_B000h base + 5Ch offset = 4003_B05Ch



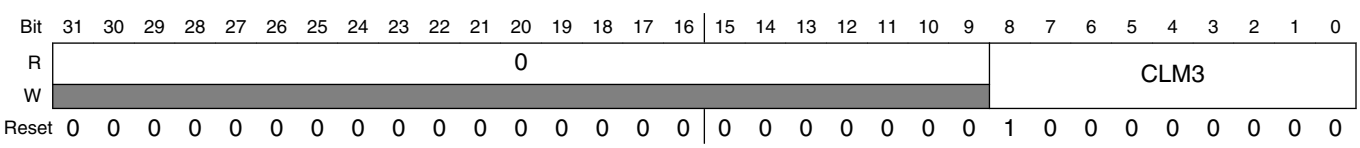
ADCx_CLM4 field descriptions

Field	Description
31–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLM4	Calibration Value Calibration Value

43.4.21 ADC Minus-Side General Calibration Value Register (ADCx_CLM3)

For more information, see CLMD register description.

Address: 4003_B000h base + 60h offset = 4003_B060h



ADCx_CLM3 field descriptions

Field	Description
31–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

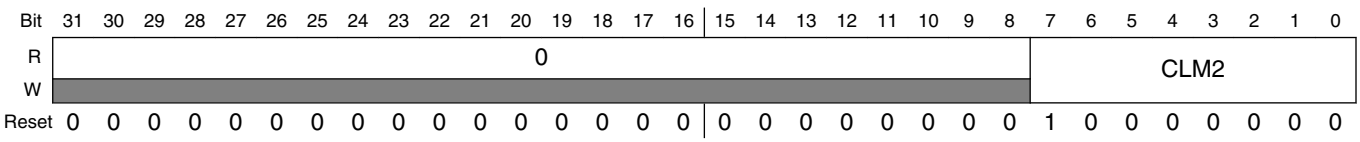
ADCx_CLM3 field descriptions (continued)

Field	Description
CLM3	Calibration Value Calibration Value

43.4.22 ADC Minus-Side General Calibration Value Register (ADCx_CLM2)

For more information, see CLMD register description.

Address: 4003_B000h base + 64h offset = 4003_B064h



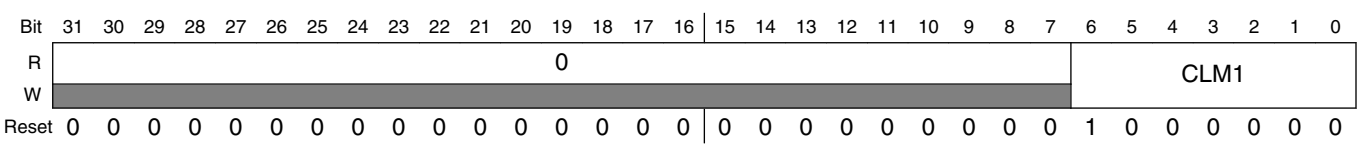
ADCx_CLM2 field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLM2	Calibration Value Calibration Value

43.4.23 ADC Minus-Side General Calibration Value Register (ADCx_CLM1)

For more information, see CLMD register description.

Address: 4003_B000h base + 68h offset = 4003_B068h



ADCx_CLM1 field descriptions

Field	Description
31–7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLM1	Calibration Value Calibration Value

43.4.24 ADC Minus-Side General Calibration Value Register (ADCx_CLM0)

For more information, see CLMD register description.

Address: 4003_B000h base + 6Ch offset = 4003_B06Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																										CLM0					
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

ADCx_CLM0 field descriptions

Field	Description
31–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLM0	Calibration Value Calibration Value

43.5 Functional description

The ADC module is disabled during reset, in Low-Power Stop mode, or when SC1n[ADCH] are all high; see the power management information for details. The module is idle when a conversion has completed and another conversion has not been initiated. When it is idle and the asynchronous clock output enable is disabled, or CFG2[ADACKEN]= 0, the module is in its lowest power state. The ADC can perform an analog-to-digital conversion on any of the software selectable channels. All modes perform conversion by a successive approximation algorithm.

To meet accuracy specifications, the ADC module must be calibrated using the on-chip calibration function.

See Calibration function for details on how to perform calibration.

When the conversion is completed, the result is placed in the Rn data registers. The respective SC1n[COCO] is then set and an interrupt is generated if the respective conversion complete interrupt has been enabled, or, when SC1n[AIEN]=1.

The ADC module has the capability of automatically comparing the result of a conversion with the contents of the CV1 and CV2 registers. The compare function is enabled by setting SC2[ACFE] and operates in any of the conversion modes and configurations.

The ADC module has the capability of automatically averaging the result of multiple conversions. The hardware average function is enabled by setting SC3[AVGE] and operates in any of the conversion modes and configurations.

NOTE

For the chip specific modes of operation, see the power management information of this MCU.

43.5.1 Clock select and divide control

One of four clock sources can be selected as the clock source for the ADC module.

This clock source is then divided by a configurable value to generate the input clock ADCK, to the module. The clock is selected from one of the following sources by means of CFG1[ADICLK].

- Bus clock. This is the default selection following reset.
- ALTCLK2: As defined for this MCU. See the chip configuration information. Conversions are possible using ALTCLK2 as the input clock source while the MCU is in Normal Stop mode.
- ALTCLK: As defined for this MCU. See the chip configuration information. Conversions are possible using ALTCLK as the input clock source while the MCU is in Normal Stop mode.
- Asynchronous clock (ADACK): This clock is generated from a clock source within the ADC module. When the ADACK clock source is selected, it is not required to be active prior to conversion start. When it is selected and it is not active prior to a conversion start CFG2[ADACKEN]=0, ADACK is activated at the start of a conversion and deactivated when conversions are terminated. In this case, there is an associated clock startup delay each time the clock source is re-activated. To avoid the conversion time variability and latency associated with the ADACK clock startup, set CFG2[ADACKEN]=1 and wait the worst-case startup time of 5 µs prior to initiating any conversions using the ADACK clock source. Conversions are possible using ADACK as the input clock source while the MCU is in Normal Stop mode. See Power Control for more information.

Whichever clock is selected, its frequency must fall within the specified frequency range for ADCK. If the available clocks are too slow, the ADC may not perform according to specifications. If the available clocks are too fast, the clock must be divided to the appropriate frequency. This divider is specified by CFG1[ADIV] and can be divide-by 1, 2, 4, or 8.

43.5.2 Voltage reference selection

The ADC can be configured to accept one of the two voltage reference pairs as the reference voltage (V_{REFSH} and V_{REFSL}) used for conversions.

Each pair contains a positive reference that must be between the minimum Ref Voltage High and V_{DDA}, and a ground reference that must be at the same potential as V_{SSA}. The two pairs are external (V_{REFH} and V_{REFL}) and alternate (V_{ALTH} and V_{ALTL}). These voltage references are selected using SC2[REFSEL]. The alternate (V_{ALTH} and V_{ALTL}) voltage reference pair may select additional external pins or internal sources depending on MCU configuration. See the chip configuration information on the voltage references specific to this MCU.

43.5.3 Hardware trigger and channel selects

The ADC module has a selectable asynchronous hardware conversion trigger, ADHWT, that is enabled when SC2[ADTRG] is set and a hardware trigger select event, ADHWTSn, has occurred.

This source is not available on all MCUs. See the chip-specific ADC information for information on the ADHWT source and the ADHWTSn configurations specific to this MCU.

When an ADHWT source is available and hardware trigger is enabled, that is SC2[ADTRG]=1, a conversion is initiated on the rising-edge of ADHWT after a hardware trigger select event, that is, ADHWTSn, has occurred. If a conversion is in progress when a rising-edge of a trigger occurs, the rising-edge is ignored. In continuous convert configuration, only the initial rising-edge to launch continuous conversions is observed, and until conversion is aborted, the ADC continues to do conversions on the same SCn register that initiated the conversion. The hardware trigger function operates in conjunction with any of the conversion modes and configurations.

The hardware trigger select event, ADHWTSn, must be set prior to the receipt of the ADHWT signal. If these conditions are not met, the converter may ignore the trigger or use the incorrect configuration. If a hardware trigger select event is asserted during a conversion, it must stay asserted until the end of current conversion and remain set until the receipt of the ADHWT signal to trigger a new conversion. The channel and status fields selected for the conversion depend on the active trigger select signal:

- ADHWTSA active selects SC1A.
- ADHWTSn active selects SC1n.

Note

Asserting more than one hardware trigger select signal (ADHWTSn) at the same time results in unknown results. To avoid this, select only one hardware trigger select signal (ADHWTSn) prior to the next intended conversion.

When the conversion is completed, the result is placed in the Rn registers associated with the ADHWTSn received. For example:

- ADHWTSA active selects RA register
- ADHWTSn active selects Rn register

The conversion complete flag associated with the ADHWTSn received, that is, SC1n[COCO], is then set and an interrupt is generated if the respective conversion complete interrupt has been enabled, that is, SC1[AIEN]=1.

43.5.4 Conversion control

Conversions can be performed as determined by CFG1[MODE] and SC1n[DIFF] as shown in the description of CFG1[MODE].

Conversions can be initiated by a software or hardware trigger.

In addition, the ADC module can be configured for:

- Low-power operation
- Long sample time
- Continuous conversion
- Hardware average
- Automatic compare of the conversion result to a software determined compare value

43.5.4.1 Initiating conversions

A conversion is initiated:

- Following a write to SC1A, with SC1n[ADCH] not all 1's, if software triggered operation is selected, that is, when SC2[ADTRG]=0.
- Following a hardware trigger, or ADHWT event, if hardware triggered operation is selected, that is, SC2[ADTRG]=1, and a hardware trigger select event, ADHWTSn, has occurred. The channel and status fields selected depend on the active trigger select signal:
  - ADHWTSA active selects SC1A.

- ADHWTSn active selects SC1n.
- if neither is active, the off condition is selected

Note

Selecting more than one ADHWTSn prior to a conversion completion will result in unknown results. To avoid this, select only one ADHWTSn prior to a conversion completion.

- Following the transfer of the result to the data registers when continuous conversion is enabled, that is, when SC3[ADCO] = 1.

If continuous conversions are enabled, a new conversion is automatically initiated after the completion of the current conversion. In software triggered operation, that is, when SC2[ADTRG] = 0, continuous conversions begin after SC1A is written and continue until aborted. In hardware triggered operation, that is, when SC2[ADTRG] = 1 and one ADHWTSn event has occurred, continuous conversions begin after a hardware trigger event and continue until aborted.

If hardware averaging is enabled, a new conversion is automatically initiated after the completion of the current conversion until the correct number of conversions are completed. In software triggered operation, conversions begin after SC1A is written. In hardware triggered operation, conversions begin after a hardware trigger. If continuous conversions are also enabled, a new set of conversions to be averaged are initiated following the last of the selected number of conversions.

43.5.4.2 Completing conversions

A conversion is completed when the result of the conversion is transferred into the data result registers, Rn. If the compare functions are disabled, this is indicated by setting of SC1n[COCO]. If hardware averaging is enabled, the respective SC1n[COCO] sets only if the last of the selected number of conversions is completed. If the compare function is enabled, the respective SC1n[COCO] sets and conversion result data is transferred only if the compare condition is true. If both hardware averaging and compare functions are enabled, then the respective SC1n[COCO] sets only if the last of the selected number of conversions is completed and the compare condition is true. An interrupt is generated if the respective SC1n[AIEN] is high at the time that the respective SC1n[COCO] is set.

43.5.4.3 Aborting conversions

Any conversion in progress is aborted when:

- Writing to SC1A while it is actively controlling a conversion, aborts the current conversion. In Software Trigger mode, when SC2[ADTRG]=0, a write to SC1A initiates a new conversion if SC1A[ADCH] is equal to a value other than all 1s. Writing to any of the SC1B–SC1n registers while that specific SC1B–SC1n register is actively controlling a conversion aborts the current conversion. The SC1(B-n) registers are not used for software trigger operation and therefore writes to the SC1(B-n) registers do not initiate a new conversion.
- A write to any ADC register besides the SC1A-SC1n registers occurs. This indicates that a change in mode of operation has occurred and the current conversion is therefore invalid.
- The MCU is reset or enters Low-Power Stop modes.
- The MCU enters Normal Stop mode with ADACK or Alternate Clock Sources not enabled.

When a conversion is aborted, the contents of the data registers, Rn, are not altered. The data registers continue to be the values transferred after the completion of the last successful conversion. If the conversion was aborted by a reset or Low-Power Stop modes, RA and Rn return to their reset states.

43.5.4.4 Power control

The ADC module remains in its idle state until a conversion is initiated. If ADACK is selected as the conversion clock source, but the asynchronous clock output is disabled, that is CFG2[ADACKEN]=0, the ADACK clock generator also remains in its idle state (disabled) until a conversion is initiated. If the asynchronous clock output is enabled, that is, CFG2[ADACKEN]=1, it remains active regardless of the state of the ADC or the MCU power mode.

Power consumption when the ADC is active can be reduced by setting CFG1[ADLPC]. This results in a lower maximum value for f_{ADCK}.

43.5.4.5 Sample time and total conversion time

For short sample, that is, when CFG1[ADLSMP]=0, there is a 2-cycle adder for first conversion over the base sample time of four ADCK cycles. For high-speed conversions, that is, when CFG2[ADHSC]=1, there is an additional 2-cycle adder on any conversion. The table below summarizes sample times for the possible ADC configurations.

ADC configuration			Sample time (ADCK cycles)	
CFG1[ADLSMP]	CFG2[ADLSTS]	CFG2[ADHSC]	First or Single	Subsequent
0	X	0	6	4
1	00	0	24	
1	01	0	16	
1	10	0	10	
1	11	0	6	
0	X	1	8	6
1	00	1	26	
1	01	1	18	
1	10	1	12	
1	11	1	8	

The total conversion time depends upon:

- The sample time as determined by CFG1[ADLSMP] and CFG2[ADLSTS]
- The MCU bus frequency
- The conversion mode, as determined by CFG1[MODE] and SC1n[DIFF]
- The high-speed configuration, that is, CFG2[ADHSC]
- The frequency of the conversion clock, that is, f_{ADCK}.

CFG2[ADHSC] is used to configure a higher clock input frequency. This will allow faster overall conversion times. To meet internal ADC timing requirements, CFG2[ADHSC] adds additional ADCK cycles. Conversions with CFG2[ADHSC]=1 take two more ADCK cycles. CFG2[ADHSC] must be used when the ADCLK exceeds the limit for CFG2[ADHSC]=0.

After the module becomes active, sampling of the input begins.

1. CFG1[ADLSMP] and CFG2[ADLSTS] select between sample times based on the conversion mode that is selected.
2. When sampling is completed, the converter is isolated from the input channel and a successive approximation algorithm is applied to determine the digital value of the analog signal.
3. The result of the conversion is transferred to Rn upon completion of the conversion algorithm.

If the bus frequency is less than f_{ADCK}, precise sample time for continuous conversions cannot be guaranteed when short sample is enabled, that is, when CFG1[ADLSMP]=0.

The maximum total conversion time is determined by the clock source chosen and the divide ratio selected. The clock source is selectable by CFG1[ADICLK], and the divide ratio is specified by CFG1[ADIV].

The maximum total conversion time for all configurations is summarized in the equation below. See the following tables for the variables referenced in the equation.

$$\text{ConversionTime} = \text{SFCAdder} + \text{AverageNum} \times (\text{BCT} + \text{LSTAdder} + \text{HSCAdder})$$

Equation 1. Conversion time equation

Table 43-6. Single or first continuous time adder (SFCAdder)

CFG1[ADLSMP]	CFG2[ADACKEN]	CFG1[ADICLK]	Single or first continuous time adder (SFCAdder)
1	x	0x, 10	3 ADCK cycles + 5 bus clock cycles
1	1	11	3 ADCK cycles + 5 bus clock cycles[1]
1	0	11	5 µs + 3 ADCK cycles + 5 bus clock cycles
0	x	0x, 10	5 ADCK cycles + 5 bus clock cycles
0	1	11	5 ADCK cycles + 5 bus clock cycles[1]
0	0	11	5 µs + 5 ADCK cycles + 5 bus clock cycles

1. To achieve this time, CFG2[ADACKEN] must be 1 for at least 5 µs prior to the conversion is initiated.

Table 43-7. Average number factor (AverageNum)

SC3[AVGE]	SC3[AVGS]	Average number factor (AverageNum)
0	xx	1
1	00	4
1	01	8
1	10	16
1	11	32

Table 43-8. Base conversion time (BCT)

Mode	Base conversion time (BCT)
8b single-ended	17 ADCK cycles
9b differential	27 ADCK cycles
10b single-ended	20 ADCK cycles
11b differential	30 ADCK cycles
12b single-ended	20 ADCK cycles
13b differential	30 ADCK cycles

Table continues on the next page...

Table 43-8. Base conversion time (BCT) (continued)

Mode	Base conversion time (BCT)
16b single-ended	25 ADCK cycles
16b differential	34 ADCK cycles

Table 43-9. Long sample time adder (LSTAdder)

CFG1[ADLSMP]	CFG2[ADLSTS]	Long sample time adder (LSTAdder)
0	xx	0 ADCK cycles
1	00	20 ADCK cycles
1	01	12 ADCK cycles
1	10	6 ADCK cycles
1	11	2 ADCK cycles

Table 43-10. High-speed conversion time adder (HSCAdder)

CFG2[ADHSC]	High-speed conversion time adder (HSCAdder)
0	0 ADCK cycles
1	2 ADCK cycles

Note

The ADCK frequency must be between f_{ADCK} minimum and f_{ADCK} maximum to meet ADC specifications.

43.5.4.6 Conversion time examples

The following examples use the Equation 1 on page 1369, and the information provided in Table 43-6 through Table 43-10.

43.5.4.6.1 Typical conversion time configuration

A typical configuration for ADC conversion is:

- 10-bit mode, with the bus clock selected as the input clock source
- The input clock divide-by-1 ratio selected
- Bus frequency of 8 MHz
- Long sample time disabled
- High-speed conversion disabled

The conversion time for a single conversion is calculated by using the Equation 1 on page 1369, and the information provided in Table 43-6 through Table 43-10. The table below lists the variables of Equation 1 on page 1369.

Table 43-11. Typical conversion time

Variable	Time
SFCAdder	5 ADCK cycles + 5 bus clock cycles
AverageNum	1
BCT	20 ADCK cycles
LSTAdder	0
HSCAdder	0

The resulting conversion time is generated using the parameters listed in the preceding table. Therefore, for a bus clock and an ADCK frequency equal to 8 MHz, the resulting conversion time is 3.75 µs.

43.5.4.6.2 Long conversion time configuration

A configuration for long ADC conversion is:

- 16-bit differential mode with the bus clock selected as the input clock source
- The input clock divide-by-8 ratio selected
- Bus frequency of 8 MHz
- Long sample time enabled
- Configured for longest adder
- High-speed conversion disabled
- Average enabled for 32 conversions

The conversion time for this conversion is calculated by using the Equation 1 on page 1369, and the information provided in Table 43-6 through Table 43-10. The following table lists the variables of the Equation 1 on page 1369.

Table 43-12. Typical conversion time

Variable	Time
SFCAdder	3 ADCK cycles + 5 bus clock cycles
AverageNum	32
BCT	34 ADCK cycles
LSTAdder	20 ADCK cycles
HSCAdder	0

The resulting conversion time is generated using the parameters listed in the preceding table. Therefore, for bus clock equal to 8 MHz and ADCK equal to 1 MHz, the resulting conversion time is 57.625 µs, that is, AverageNum. This results in a total conversion time of 1.844 ms.

43.5.4.6.3 Short conversion time configuration

A configuration for short ADC conversion is:

- 8-bit Single-Ended mode with the bus clock selected as the input clock source
- The input clock divide-by-1 ratio selected
- Bus frequency of 20 MHz
- Long sample time disabled
- High-speed conversion enabled

The conversion time for this conversion is calculated by using the Equation 1 on page 1369, and the information provided in Table 43-6 through Table 43-10. The table below lists the variables of Equation 1 on page 1369.

Table 43-13. Typical conversion time

Variable	Time
SFCAdder	5 ADCK cycles + 5 bus clock cycles
AverageNum	1
BCT	17 ADCK cycles
LSTAdder	0 ADCK cycles
HSCAdder	2

The resulting conversion time is generated using the parameters listed in in the preceding table. Therefore, for bus clock and ADCK frequency equal to 20 MHz, the resulting conversion time is 1.45 µs.

43.5.4.7 Hardware average function

The hardware average function can be enabled by setting SC3[AVGE]=1 to perform a hardware average of multiple conversions. The number of conversions is determined by the AVGS[1:0] bits, which can select 4, 8, 16, or 32 conversions to be averaged. While the hardware average function is in progress, SC2[ADACT] will be set.

After the selected input is sampled and converted, the result is placed in an accumulator from which an average is calculated once the selected number of conversions have been completed. When hardware averaging is selected, the completion of a single conversion will not set SC1n[COCO].

If the compare function is either disabled or evaluates true, after the selected number of conversions are completed, the average conversion result is transferred into the data result registers, Rn, and SC1n[COCO] is set. An ADC interrupt is generated upon the setting of SC1n[COCO] if the respective ADC interrupt is enabled, that is, SC1n[AIEN]=1.

Note

The hardware average function can perform conversions on a channel while the MCU is in Wait or Normal Stop modes. The ADC interrupt wakes the MCU when the hardware average is completed if SC1n[AIEN] is set.

43.5.5 Automatic compare function

The compare function can be configured to check whether the result is less than or greater-than-or-equal-to a single compare value, or, if the result falls within or outside a range determined by two compare values.

The compare mode is determined by SC2[ACFGT], SC2[ACREN], and the values in the compare value registers, CV1 and CV2. After the input is sampled and converted, the compare values in CV1 and CV2 are used as described in the following table. There are six Compare modes as shown in the following table.

Table 43-14. Compare modes

SC2[ACFGT]	SC2[ACREN]	ADCCV1 relative to ADCCV2	Function	Compare mode description
0	0	—	Less than threshold	Compare true if the result is less than the CV1 registers.
1	0	—	Greater than or equal to threshold	Compare true if the result is greater than or equal to CV1 registers.
0	1	Less than or equal	Outside range, not inclusive	Compare true if the result is less than CV1 **Or** the result is greater than CV2.
0	1	Greater than	Inside range, not inclusive	Compare true if the result is less than CV1 **And** the result is greater than CV2.
1	1	Less than or equal	Inside range, inclusive	Compare true if the result is greater than or equal to CV1 **And** the result is less than or equal to CV2.
1	1	Greater than	Outside range, inclusive	Compare true if the result is greater than or equal to CV1 **Or** the result is less than or equal to CV2.

With SC2[ACREN] =1, and if the value of CV1 is less than or equal to the value of CV2, then setting SC2[ACFGT] will select a trigger-if-inside-compare-range inclusive-of-endpoints function. Clearing SC2[ACFGT] will select a trigger-if-outside-compare-range, not-inclusive-of-endpoints function.

If CV1 is greater than CV2, setting SC2[ACFGT] will select a trigger-if-outside-compare-range, inclusive-of-endpoints function. Clearing SC2[ACFGT] will select a trigger-if-inside-compare-range, not-inclusive-of-endpoints function.

If the condition selected evaluates true, SC1n[COCO] is set.

Upon completion of a conversion while the compare function is enabled, if the compare condition is not true, SC1n[COCO] is not set and the conversion result data will not be transferred to the result register, Rn. If the hardware averaging function is enabled, the compare function compares the averaged result to the compare values. The same compare function definitions apply. An ADC interrupt is generated when SC1n[COCO] is set and the respective ADC interrupt is enabled, that is, SC1n[AIEN]=1.

Note

The compare function can monitor the voltage on a channel while the MCU is in Wait or Normal Stop modes. The ADC interrupt wakes the MCU when the compare condition is met.

43.5.6 Calibration function

The ADC contains a self-calibration function that is required to achieve the specified accuracy.

Calibration must be run, or valid calibration values written, after any reset and before a conversion is initiated. The calibration function sets the offset calibration value, the minus-side calibration values, and the plus-side calibration values. The offset calibration value is automatically stored in the ADC offset correction register (OFS), and the plus-side and minus-side calibration values are automatically stored in the ADC plus-side and minus-side calibration registers, CLPx and CLMx. The user must configure the ADC correctly prior to calibration, and must generate the plus-side and minus-side gain calibration results and store them in the ADC plus-side gain register (PG) after the calibration function completes.

Prior to calibration, the user must configure the ADC's clock source and frequency, low power configuration, voltage reference selection, sample time, and high speed configuration according to the application's clock source availability and needs. If the

application uses the ADC in a wide variety of configurations, the configuration for which the highest accuracy is required should be selected, or multiple calibrations can be done for the different configurations. For best calibration results:

- Set hardware averaging to maximum, that is, SC3[AVGE]=1 and SC3[AVGS]=11 for an average of 32
- Set ADC clock frequency f_{ADCK} less than or equal to 4 MHz
- $V_{REFH}=V_{DDA}$
- Calibrate at nominal voltage and temperature

The input channel, conversion mode continuous function, compare function, resolution mode, and differential/single-ended mode are all ignored during the calibration function.

To initiate calibration, the user sets SC3[CAL] and the calibration will automatically begin if the SC2[ADTRG] is 0. If SC2[ADTRG] is 1, SC3[CAL] will not get set and SC3[CALF] will be set. While calibration is active, no ADC register can be written and no stop mode may be entered, or the calibration routine will be aborted causing SC3[CAL] to clear and SC3[CALF] to set. At the end of a calibration sequence, SC1n[COCO] will be set. SC1n[AIEN] can be used to allow an interrupt to occur at the end of a calibration sequence. At the end of the calibration routine, if SC3[CALF] is not set, the automatic calibration routine is completed successfully.

To complete calibration, the user must generate the gain calibration values using the following procedure:

1. Initialize or clear a 16-bit variable in RAM.
2. Add the plus-side calibration results CLP0, CLP1, CLP2, CLP3, CLP4, and CLPS to the variable.
3. Divide the variable by two.
4. Set the MSB of the variable.
5. The previous two steps can be achieved by setting the carry bit, rotating to the right through the carry bit on the high byte and again on the low byte.
6. Store the value in the plus-side gain calibration register PG.
7. Repeat the procedure for the minus-side gain calibration value.

When calibration is complete, the user may reconfigure and use the ADC as desired. A second calibration may also be performed, if desired, by clearing and again setting SC3[CAL].

Overall, the calibration routine may take as many as 14k ADCK cycles and 100 bus cycles, depending on the results and the clock source chosen. For an 8 MHz clock source, this length amounts to about 1.7 ms. To reduce this latency, the calibration values, which are offset, plus-side and minus-side gain, and plus-side and minus-side calibration values, may be stored in flash memory after an initial calibration and recovered prior to the first ADC conversion. This method can reduce the calibration latency to 20 register store operations on all subsequent power, reset, or Low-Power Stop mode recoveries.

Further information on the calibration procedure can be found in the Calibration section of AN3949: ADC16 Calibration Procedure and Programmable Delay Block Synchronization.

43.5.7 User-defined offset function

OFS contains the user-selected or calibration-generated offset error correction value.

This register is a 2's complement, left-justified. The value in OFS is subtracted from the conversion and the result is transferred into the result registers, Rn. If the result is greater than the maximum or less than the minimum result value, it is forced to the appropriate limit for the current mode of operation.

The formatting of the OFS is different from the data result register, Rn, to preserve the resolution of the calibration value regardless of the conversion mode selected. Lower order bits are ignored in lower resolution modes. For example, in 8-bit single-ended mode, OFS[14:7] are subtracted from D[7:0]; OFS[15] indicates the sign (negative numbers are effectively added to the result) and OFS[6:0] are ignored. The same bits are used in 9-bit differential mode because OFS[15] indicates the sign bit, which maps to D[8]. For 16-bit differential mode, OFS[15:0] are directly subtracted from the conversion result data D[15:0]. In 16-bit single-ended mode, there is no field in the OFS corresponding to the least significant result D[0], so odd values, such as -1 or +1, cannot be subtracted from the result.

OFS is automatically set according to calibration requirements once the self-calibration sequence is done, that is, SC3[CAL] is cleared. The user may write to OFS to override the calibration result if desired. If the OFS is written by the user to a value that is different from the calibration value, the ADC error specifications may not be met. Storing the value generated by the calibration function in memory before overwriting with a user-specified value is recommended.

Note

There is an effective limit to the values of offset that can be set by the user. If the magnitude of the offset is too high, the results of the conversions will cap off at the limits.

The offset calibration function may be employed by the user to remove application offsets or DC bias values. OFS may be written with a number in 2's complement format and this offset will be subtracted from the result, or hardware averaged value. To add an offset, store the negative offset in 2's complement format and the effect will be an addition. An offset correction that results in an out-of-range value will be forced to the minimum or maximum value. The minimum value for single-ended conversions is 0x0000; for a differential conversion it is 0x8000.

To preserve accuracy, the calibrated offset value initially stored in OFS must be added to the user-defined offset. For applications that may change the offset repeatedly during operation, store the initial offset calibration value in flash so it can be recovered and added to any user offset adjustment value and the sum stored in OFS.

43.5.8 Temperature sensor

The ADC module includes a temperature sensor whose output is connected to one of the ADC analog channel inputs.

The following equation provides an approximate transfer function of the temperature sensor.

$$Temp = 25 - \left(\left(V_{TEMP} - V_{TEMP25} \right) \div m \right)$$

Equation 2. Approximate transfer function of the temperature sensor

where:

- V_{TEMP} is the voltage of the temperature sensor channel at the ambient temperature.
- V_{TEMP25} is the voltage of the temperature sensor channel at 25 °C.
- m is referred as temperature sensor slope in the device data sheet. It is the hot or cold voltage versus temperature slope in V/°C.

For temperature calculations, use the V_{TEMP25} and temperature sensor slope values from the ADC Electricals table.

In application code, the user reads the temperature sensor channel, calculates V_{TEMP}, and compares to V_{TEMP25}. If V_{TEMP} is greater than V_{TEMP25} the cold slope value is applied in the preceding equation. If V_{TEMP} is less than V_{TEMP25}, the hot slope value is applied in the preceding equation. ADC Electricals table may only specify one temperature sensor slope value. In that case, the user could use the same slope for the calculation across the operational temperature range.

For more information on using the temperature sensor, see the application note titled *Temperature Sensor for the HCS08 Microcontroller Family* (document AN3031).

43.5.9 MCU wait mode operation

Wait mode is a lower-power consumption Standby mode from which recovery is fast because the clock sources remain active.

If a conversion is in progress when the MCU enters Wait mode, it continues until completion. Conversions can be initiated while the MCU is in Wait mode by means of the hardware trigger or if continuous conversions are enabled.

The bus clock, ADACK, and Alternate Clock sources are available as conversion clock sources while in Wait mode. The use of ALTCLK as the conversion clock source in Wait is dependent on the definition of ALTCLK for this MCU. See the Chip Configuration information on ALTCLK specific to this MCU.

If the compare and hardware averaging functions are disabled, a conversion complete event sets SC1n[COCO] and generates an ADC interrupt to wake the MCU from Wait mode if the respective ADC interrupt is enabled, that is, when SC1n[AIEN]=1. If the hardware averaging function is enabled, SC1n[COCO] will set, and generate an interrupt if enabled, when the selected number of conversions are completed. If the compare function is enabled, SC1n[COCO] will set, and generate an interrupt if enabled, only if the compare conditions are met. If a single conversion is selected and the compare trigger is not met, the ADC will return to its idle state and cannot wake the MCU from Wait mode unless a new conversion is initiated by the hardware trigger.

43.5.10 MCU Normal Stop mode operation

Stop mode is a low-power consumption Standby mode during which most or all clock sources on the MCU are disabled.

43.5.10.1 Normal Stop mode with Bus Clock selected

If the Bus Clock is selected as the conversion clock, executing a stop instruction aborts the current conversion and places the ADC in its Idle state. The contents of the ADC registers, including Rn, are unaffected by Normal Stop mode. After exiting from Normal Stop mode, a software or hardware trigger is required to resume conversions.

43.5.10.2 Normal Stop mode with ADACK or Alternate clock sources enabled

If ADACK or an Alternate clock source is selected as the conversion clock, the ADC continues operation during Normal Stop mode. See the chip-specific ADC information for configuration information for this device.

If a conversion is in progress when the MCU enters Normal Stop mode, it continues until completion. Conversions can be initiated while the MCU is in Normal Stop mode by means of the hardware trigger or if continuous conversions are enabled.

If the compare and hardware averaging functions are disabled, a conversion complete event sets SC1n[COCO] and generates an ADC interrupt to wake the MCU from Normal Stop mode if the respective ADC interrupt is enabled, that is, when SC1n[AIEN]=1. The result register, Rn, will contain the data from the first completed conversion that occurred during Normal Stop mode. If the hardware averaging function is enabled, SC1n[COCO] will set, and generate an interrupt if enabled, when the selected number of conversions are completed. If the compare function is enabled, SC1n[COCO] will set, and generate an interrupt if enabled, only if the compare conditions are met. If a single conversion is selected and the compare is not true, the ADC will return to its idle state and cannot wake the MCU from Normal Stop mode unless a new conversion is initiated by another hardware trigger.

43.5.11 MCU Low-Power Stop mode operation

The ADC module is automatically disabled when the MCU enters Low-Power Stop mode.

All module registers contain their reset values following exit from Low-Power Stop mode. Therefore, the module must be re-enabled and re-configured following exit from Low-Power Stop mode.

NOTE

For the chip specific modes of operation, see the power management information for the device.

43.6 Initialization information

This section gives an example that provides some basic direction on how to initialize and configure the ADC module.

The user can configure the module for 16-bit, 12-bit, 10-bit, or 8-bit single-ended resolution or 16-bit, 13-bit, 11-bit, or 9-bit differential resolution, single or continuous conversion, and a polled or interrupt approach, among many other options. For information used in this example, refer to Table 43-9, Table 43-10, and Table 43-11.

Note

Hexadecimal values are designated by a preceding 0x, binary values designated by a preceding %, and decimal values have no preceding character.

43.6.1 ADC module initialization example

43.6.1.1 Initialization sequence

Before the ADC module can be used to complete conversions, an initialization procedure must be performed. A typical sequence is:

1. Calibrate the ADC by following the calibration instructions in Calibration function.
2. Update CFG to select the input clock source and the divide ratio used to generate ADCK. This register is also used for selecting sample time and low-power configuration.
3. Update SC2 to select the conversion trigger, hardware or software, and compare function options, if enabled.
4. Update SC3 to select whether conversions will be continuous or completed only once (ADCO) and whether to perform hardware averaging.
5. Update SC1:SC1n registers to select whether conversions will be single-ended or differential and to enable or disable conversion complete interrupts. Also, select the input channel which can be used to perform conversions.

43.6.1.2 Pseudo-code example

In this example, the ADC module is set up with interrupts enabled to perform a single 10-bit conversion at low-power with a long sample time on input channel 1, where ADCK is derived from the bus clock divided by 1.

CFG1 = 0x98 (%10011000)

```
        Bit 7   ADLPC   1       Configures for low power, lowers maximum clock speed.
        Bit 6:5 ADIV    00      Sets the ADCK to the input clock ÷ 1.
        Bit 4   ADLSMP  1       Configures for long sample time.
        Bit 3:2   MODE   10     Selects the single-ended 10-bit conversion, differential 11-
bit conversion.
        Bit 1:0   ADICLK   00    Selects the bus clock.
```

SC2 = 0x00 (%00000000)

```
        Bit 7   ADACT   0        Flag indicates if a conversion is in progress.
        Bit 6   ADTRG   0        Software trigger selected.
        Bit 5   ACFE    0        Compare function disabled.
        Bit 4   ACFGT   0        Not used in this example.
        Bit 3   ACREN   0       Compare range disabled.
 Bit 2 DMAEN 0 DMA request disabled.
        Bit 1:0 REFSEL  00      Selects default voltage reference pin pair (External pins
VREFH and VREFL).
```

SC1A = 0x41 (%01000001)

```
        Bit 7   COCO    0       Read-only flag which is set when a conversion completes.
        Bit 6   AIEN    1       Conversion complete interrupt enabled.
 Bit 5 DIFF 0 Single-ended conversion selected.
        Bit 4:0 ADCH    00001   Input channel 1 selected as ADC input channel.
```

RA = 0xxx

```
        Holds results of conversion.
```

CV = 0xxx

```
        Holds compare value when compare function enabled.
```

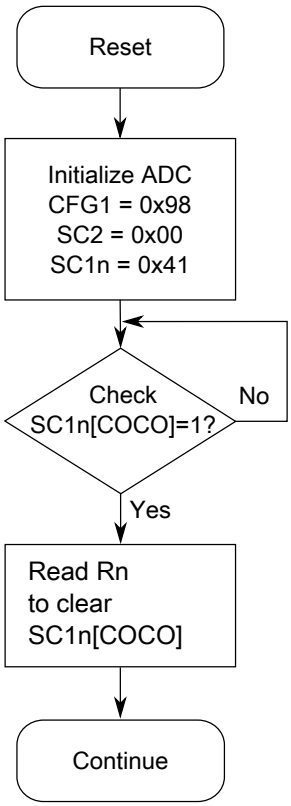


Figure 43-3. Initialization flowchart example

43.7 Application information

The ADC has been designed to be integrated into a microcontroller for use in embedded control applications requiring an ADC.

For guidance on selecting optimum external component values and converter parameters see AN4373: Cookbook for SAR ADC Measurements.

43.7.1 External pins and routing

43.7.1.1 Analog supply pins

Depending on the device, the analog power and ground supplies, V_{DDA} and V_{SSA}, of the ADC module are available as:

- V_{DDA} and V_{SSA} available as separate pins—When available on a separate pin, both V_{DDA} and V_{SSA} must be connected to the same voltage potential as their corresponding MCU digital supply, V_{DD} and V_{SS}, and must be routed carefully for maximum noise immunity and bypass capacitors placed as near as possible to the package.

- V_{SSA} is shared on the same pin as the MCU digital V_{SS}.
- V_{SSA} and V_{DDA} are shared with the MCU digital supply pins—In these cases, there are separate pads for the analog supplies bonded to the same pin as the corresponding digital supply so that some degree of isolation between the supplies is maintained.

If separate power supplies are used for analog and digital power, the ground connection between these supplies must be at the V_{SSA} pin. This must be the only ground connection between these supplies, if possible. V_{SSA} makes a good single point ground location.

43.7.1.2 Analog voltage reference pins

In addition to the analog supplies, the ADC module has connections for two reference voltage inputs used by the converter:

- V_{REFSH} is the high reference voltage for the converter.
- V_{REFSL} is the low reference voltage for the converter.

The ADC can be configured to accept one of two voltage reference pairs for V_{REFSH} and V_{REFSL}. Each pair contains a positive reference and a ground reference. The two pairs are external, V_{REFH} and V_{REFL} and alternate, V_{ALTH} and V_{ALTL}. These voltage references are selected using SC2[REFSEL]. The alternate voltage reference pair, V_{ALTH} and V_{ALTL}, may select additional external pins or internal sources based on MCU configuration. See the chip configuration information on the voltage references specific to this MCU.

In some packages, the external or alternate pairs are connected in the package to V_{DDA} and V_{SSA}, respectively. One of these positive references may be shared on the same pin as V_{DDA} on some devices. One of these ground references may be shared on the same pin as V_{SSA} on some devices.

If externally available, the positive reference may be connected to the same potential as V_{DDA} or may be driven by an external source to a level between the minimum Ref Voltage High and the V_{DDA} potential. The positive reference must never exceed V_{DDA}. If externally available, the ground reference must be connected to the same voltage potential as V_{SSA}. The voltage reference pairs must be routed carefully for maximum noise immunity and bypass capacitors placed as near as possible to the package.

AC current in the form of current spikes required to supply charge to the capacitor array at each successive approximation step is drawn through the V_{REFH} and V_{REFL} loop. The best external component to meet this current demand is a 0.1 µF capacitor with good

high-frequency characteristics. This capacitor is connected between V_{REFH} and V_{REFL} and must be placed as near as possible to the package pins. Resistance in the path is not recommended because the current causes a voltage drop that could result in conversion errors. Inductance in this path must be minimum, that is, parasitic only.

43.7.1.3 Analog input pins

The external analog inputs are typically shared with digital I/O pins on MCU devices.

Empirical data shows that capacitors on the analog inputs improve performance in the presence of noise or when the source impedance is high. Use of 0.01 µF capacitors with good high-frequency characteristics is sufficient. These capacitors are not necessary in all cases, but when used, they must be placed as near as possible to the package pins and be referenced to V_{SSA}.

For proper conversion, the input voltage must fall between V_{REFH} and V_{REFL}. If the input is equal to or exceeds V_{REFH}, the converter circuit converts the signal to 0xFFF, which is full scale 12-bit representation, 0x3FF, which is full scale 10-bit representation, or 0xFF, which is full scale 8-bit representation. If the input is equal to or less than V_{REFL}, the converter circuit converts it to 0x000. Input voltages between V_{REFH} and V_{REFL} are straight-line linear conversions. There is a brief current associated with V_{REFL} when the sampling capacitor is charging.

For minimal loss of accuracy due to current injection, pins adjacent to the analog input pins must not be transitioning during conversions.

43.7.2 Sources of error

43.7.2.1 Sampling error

For proper conversions, the input must be sampled long enough to achieve the proper accuracy.

$$RAS + RADIN = SC / (FMAX * NUMTAU * CADIN)$$

Figure 43-4. Sampling equation

Where:

RAS = External analog source resistance

SC = Number of ADCK cycles used during sample window

CADIN = Internal ADC input capacitance

NUMTAU = -ln(LSBERR / 2^N)

LSBERR = value of acceptable sampling error in LSBs

N = 8 in 8-bit mode, 10 in 10-bit mode, 12 in 12-bit mode or 16 in 16-bit mode

Higher source resistances or higher-accuracy sampling is possible by setting CFG1[ADLSMP] and changing CFG2[ADLSTS] to increase the sample window, or decreasing ADCK frequency to increase sample time.

43.7.2.2 Pin leakage error

Leakage on the I/O pins can cause conversion error if the external analog source resistance, R_{AS}, is high. If this error cannot be tolerated by the application, keep R_{AS} lower than V_{REFH} / (4 × I_{LEAK} × 2^N) for less than 1/4 LSB leakage error, where N = 8 in 8-bit mode, 10 in 10-bit mode, 12 in 12-bit mode, or 16 in 16-bit mode.

43.7.2.3 Noise-induced errors

System noise that occurs during the sample or conversion process can affect the accuracy of the conversion. The ADC accuracy numbers are guaranteed as specified only if the following conditions are met:

- There is a 0.1 µF low-ESR capacitor from V_{REFH} to V_{REFL}.
- There is a 0.1 µF low-ESR capacitor from V_{DDA} to V_{SSA}.
- If inductive isolation is used from the primary supply, an additional 1 µF capacitor is placed from V_{DDA} to V_{SSA}.
- V_{SSA}, and V_{REFL}, if connected, is connected to V_{SS} at a quiet point in the ground plane.
- Operate the MCU in Wait or Normal Stop mode before initiating (hardware-triggered conversions) or immediately after initiating (hardware- or software-triggered conversions) the ADC conversion.

- For software triggered conversions, immediately follow the write to SC1 with a Wait instruction or Stop instruction.
- For Normal Stop mode operation, select ADACK or an Alternate clock as the clock source. Operation in Normal Stop reduces V_{DD} noise but increases effective conversion time due to stop recovery.

- There is no I/O switching, input or output, on the MCU during the conversion.

There are some situations where external system activity causes radiated or conducted noise emissions or excessive V_{DD} noise is coupled into the ADC. In these situations, or when the MCU cannot be placed in Wait or Normal Stop mode, or I/O activity cannot be halted, the following actions may reduce the effect of noise on the accuracy:

- Place a 0.01 µF capacitor (C_{AS}) on the selected input channel to V_{REFL} or V_{SSA}. This improves noise issues, but affects the sample rate based on the external analog source resistance.
- Average the result by converting the analog input many times in succession and dividing the sum of the results. Four samples are required to eliminate the effect of a 1 LSB, one-time error.
- Reduce the effect of synchronous noise by operating off the asynchronous clock, that is, ADACK, and averaging. Noise that is synchronous to ADCK cannot be averaged out.

43.7.2.4 Code width and quantization error

The ADC quantizes the ideal straight-line transfer function into 65536 steps in the 16-bit mode.. Each step ideally has the same height, that is, 1 code, and width. The width is defined as the delta between the transition points to one code and the next. The ideal code width for an N-bit converter, where N can be 16, 12, 10, or 8, defined as 1 LSB, is:

$$1LSB=\left(V_{REFH}\right)/2^{N}$$

Equation 3. Ideal code width for an N-bit converter

There is an inherent quantization error due to the digitization of the result. For 8-bit, 10-bit, or 12-bit conversions, the code transitions when the voltage is at the midpoint between the points where the straight line transfer function is exactly represented by the actual transfer function. Therefore, the quantization error will be ± 1/2 LSB in 8-bit, 10-bit, or 12-bit modes. As a consequence, however, the code width of the first (0x000) conversion is only 1/2 LSB and the code width of the last (0xFF or 0x3FF) is 1.5 LSB.

For 16-bit conversions, the code transitions only after the full code width is present, so the quantization error is -1 LSB to 0 LSB and the code width of each step is 1 LSB.

43.7.2.5 Linearity errors

The ADC may also exhibit non-linearity of several forms. Every effort has been made to reduce these errors, but the system designers must be aware of these errors because they affect overall accuracy:

- Zero-scale error (E_{ZS}), sometimes called offset: This error is defined as the difference between the actual code width of the first conversion and the ideal code width. This is 1/2 LSB in 8-bit, 10-bit, or 12-bit modes and 1 LSB in 16-bit mode. If the first conversion is 0x001, the difference between the actual 0x001 code width and its ideal (1 LSB) is used.
- Full-scale error (E_{FS}): This error is defined as the difference between the actual code width of the last conversion and the ideal code width. This is 1.5 LSB in 8-bit, 10-bit, or 12-bit modes and 1 LSB in 16-bit mode. If the last conversion is 0x3FE, the difference between the actual 0x3FE code width and its ideal (1 LSB) is used.
- Differential non-linearity (DNL): This error is defined as the worst-case difference between the actual code width and the ideal code width for all conversions.
- Integral non-linearity (INL): This error is defined as the highest-value or absolute value that the running sum of DNL achieves. More simply, this is the worst-case difference of the actual transition voltage to a given code and its corresponding ideal transition voltage, for all codes.
- Total unadjusted error (TUE): This error is defined as the difference between the actual transfer function and the ideal straight-line transfer function and includes all forms of error.

43.7.2.6 Code jitter, non-monotonicity, and missing codes

Analog-to-digital converters are susceptible to three special forms of error:

- Code jitter: Code jitter occurs when a given input voltage converts to one of the two values when sampled repeatedly. Ideally, when the input voltage is infinitesimally smaller than the transition voltage, the converter yields the lower code, and vice-versa. However, even small amounts of system noise can cause the converter to be indeterminate, between two codes, for a range of input voltages around the transition voltage.

This error may be reduced by repeatedly sampling the input and averaging the result. Additionally, the techniques discussed in Noise-induced errors reduces this error.

- Non-monotonicity: Non-monotonicity occurs when, except for code jitter, the converter converts to a lower code for a higher input voltage.
- Missing codes: Missing codes are those values never converted for any input value.

In 8-bit or 10-bit mode, the ADC is guaranteed to be monotonic and have no missing codes.

Chapter 44
Comparator (CMP)

44.1 Chip-specific Comparator information

44.1.1 CMP instantiation information

NOTE

CMP0_out and CMP1_out inter-connected to the RX pin of LPUART0 and LPUART1 on chip. See SIM (link tbd) for details.

NOTE

CMP0_out inter-connects to the RX pin of UART0 on chip. See SIM (link tbd) for details.

44.1.2 CMP input connections

The following table shows the fixed internal connections to the CMP.

Table 44-1. CMP input connections

CMP Inputs	CMP0	CMP1
IN0	CMP0_IN0	CMP1_IN0
IN1	CMP0_IN1	CMP1_IN1
IN2	CMP0_IN2	CMP1_IN2
IN3	CMP0_IN3	12-bit DAC0_OUT/CMP1_IN3
IN4	—	—
IN5	VREF Output/CMP0_IN5	VREF Output/CMP1_IN5
IN6	Bandgap	Bandgap
IN7	6b DAC0 Reference	6b DAC1 Reference

44.1.3 CMP external references

The 6-bit DAC sub-block supports selection of two references. For this device, the references are connected as follows:

- VREF_OUT - V_{in1} input
- VDD - V_{in2} input

44.1.4 External window/sample input

Individual PDB pulse-out signals control each CMP Sample/Window timing.

44.1.5 CMP trigger mode

The CMP and 6-bit DAC sub-block supports trigger mode operation when the CMPx_CR1[TRIGM] is set. When trigger mode is enabled, the trigger event will initiate a compare sequence that must first enable the CMP and DAC prior to performing a CMP operation and capturing the output. In this device, control for this two staged sequencing is provided from the LPTMR. The LPTMR provides a single trigger output to all implemented comparators. Through configuration of the CMPx_CR1[TRIGM] bits the trigger can be used to trigger a single comparator or multiple comparators concurrently. The LPTMR triggering output is always enabled when the LPTMR is enabled. The first signal is supplied to enable the CMP and DAC and is asserted at the same time as the TCF flag is set. The delay to the second signal that triggers the CMP to capture the result of the compare operation is dependent on the LPTMR configuration. In Time Counter mode with prescaler enabled, the delay is 1/2 Prescaler output period. In Time Counter mode with prescaler bypassed, the delay is 1/2 Prescaler clock period.

The delay between the first signal from LPTMR and the second signal from LPTMR must be greater than the Analog comparator initialization delay as defined in the device datasheet.

44.2 Introduction

The comparator (CMP) module provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage, known as rail-to-rail operation.

The Analog MUX (ANMUX) provides a circuit for selecting an analog input signal from eight channels. One signal is provided by the 6-bit digital-to-analog converter (DAC). The mux circuit is designed to operate across the full range of the supply voltage.

The 6-bit DAC is 64-tap resistor ladder network which provides a selectable voltage reference for applications where voltage reference is needed. The 64-tap resistor ladder network divides the supply reference V_{in} into 64 voltage levels. A 6-bit digital signal input selects the output voltage level, which varies from V_{in} to $V_{in}/64$. V_{in} can be selected from two voltage sources, V_{in1} and V_{in2}. The 6-bit DAC from a comparator is available as an on-chip internal signal only and is not available externally to a pin.

44.2.1 CMP features

The CMP has the following features:

- Operational over the entire supply range
- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising or falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as:
  - Sampled
  - Windowed, which is ideal for certain PWM zero-crossing-detection applications
  - Digitally filtered:
    - Filter can be bypassed
    - Can be clocked via external SAMPLE signal or scaled bus clock
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Two software selectable performance levels:
  - Shorter propagation delay at the expense of higher power
  - Low power, with longer propagation delay
- DMA transfer support
  - A comparison event can be selected to trigger a DMA transfer

- Functional in all modes of operation except VLLS0
- The window and filter functions are not available in the following modes:
  - Stop
  - VLPS
  - LLS
  - VLLSx

44.2.2 6-bit DAC key features

The 6-bit DAC has the following features:

- 6-bit resolution
- Selectable supply reference source
- Power Down mode to conserve power when not in use
- Option to route the output to internal comparator input

44.2.3 ANMUX key features

The ANMUX has the following features:

- Two 8-to-1 channel mux
- Operational over the entire supply range

44.2.4 CMP, DAC and ANMUX diagram

The following figure shows the block diagram for the High-Speed Comparator, DAC, and ANMUX modules.

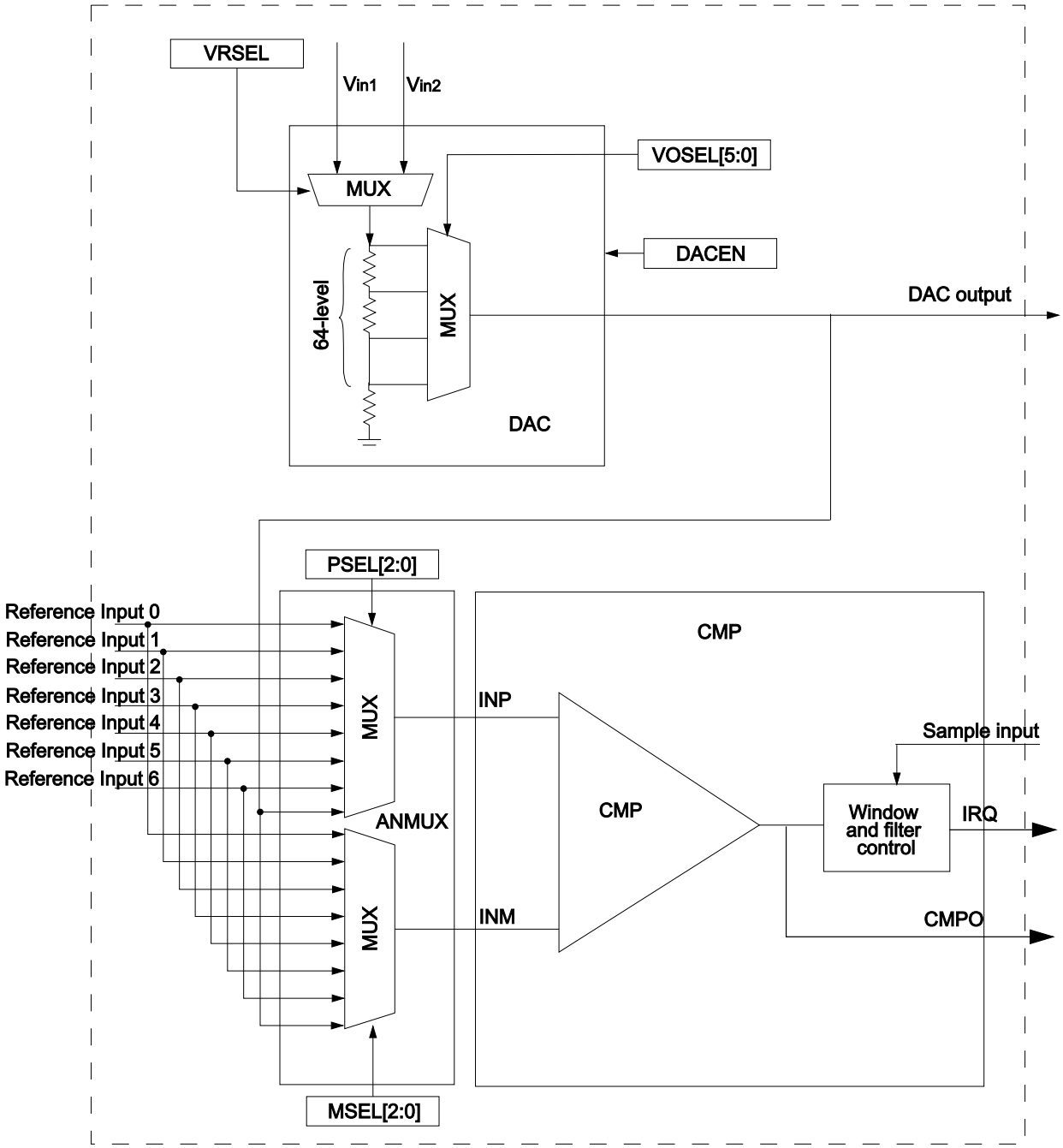


Figure 44-1. CMP, DAC and ANMUX block diagram

44.2.5 CMP block diagram

The following figure shows the block diagram for the CMP module.

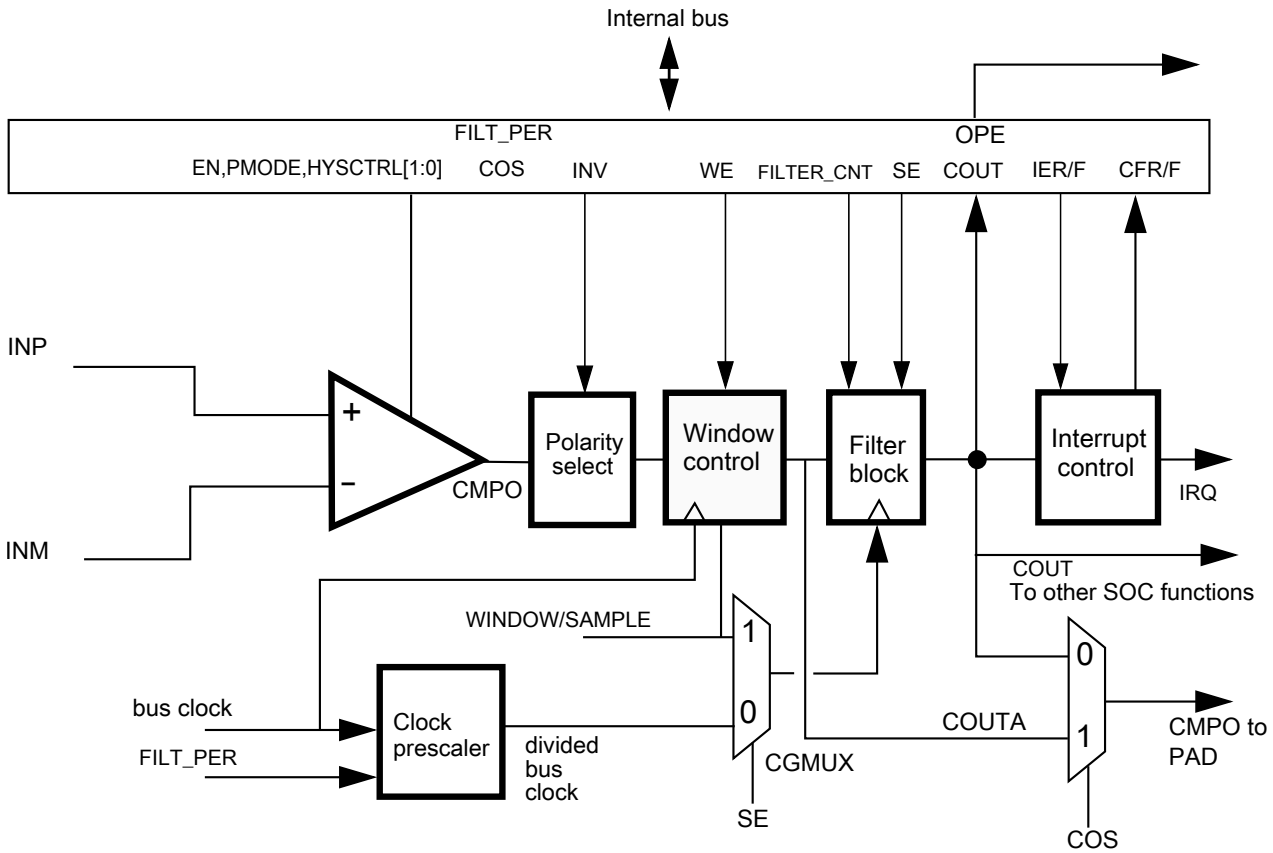


Figure 44-2. Comparator module block diagram

In the CMP block diagram:

- The Window Control block is bypassed when CR1[WE] = 0
- If CR1[WE] = 1, the comparator output will be sampled on every bus clock when WINDOW=1 to generate COUTA. Sampling does NOT occur when WINDOW = 0.
- The Filter block is bypassed when not in use.
- The Filter block acts as a simple sampler if the filter is bypassed and CR0[FILTER_CNT] is set to 0x01.
- The Filter block filters based on multiple samples when the filter is bypassed and CR0[FILTER_CNT] is set greater than 0x01.
  - If CR1[SE] = 1, the external SAMPLE input is used as sampling clock
  - If CR1[SE] = 0, the divided bus clock is used as sampling clock

- If enabled, the Filter block will incur up to one bus clock additional latency penalty on COUT due to the fact that COUT, which is crossing clock domain boundaries, must be resynchronized to the bus clock.
- CR1[WE] and CR1[SE] are mutually exclusive.

44.3 Memory map/register definitions

CMP memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4007_3000	CMP Control Register 0 (CMP0_CR0)	8	R/W	00h	44.3.1/1395
4007_3001	CMP Control Register 1 (CMP0_CR1)	8	R/W	00h	44.3.2/1396
4007_3002	CMP Filter Period Register (CMP0_FPR)	8	R/W	00h	44.3.3/1398
4007_3003	CMP Status and Control Register (CMP0_SCR)	8	R/W	00h	44.3.4/1398
4007_3004	DAC Control Register (CMP0_DACCR)	8	R/W	00h	44.3.5/1399
4007_3005	MUX Control Register (CMP0_MUXCR)	8	R/W	00h	44.3.6/1400
4007_3008	CMP Control Register 0 (CMP1_CR0)	8	R/W	00h	44.3.1/1395
4007_3009	CMP Control Register 1 (CMP1_CR1)	8	R/W	00h	44.3.2/1396
4007_300A	CMP Filter Period Register (CMP1_FPR)	8	R/W	00h	44.3.3/1398
4007_300B	CMP Status and Control Register (CMP1_SCR)	8	R/W	00h	44.3.4/1398
4007_300C	DAC Control Register (CMP1_DACCR)	8	R/W	00h	44.3.5/1399
4007_300D	MUX Control Register (CMP1_MUXCR)	8	R/W	00h	44.3.6/1400

44.3.1 CMP Control Register 0 (CMPx_CR0)

Address: Base address + 0h offset

Bit	7	6	5	4	3	2	1	0
Read	0	FILTER_CNT			0	0	HYSTCTR	
Write								
Reset	0	0	0	0	0	0	0	0

CMPx_CR0 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6–4 FILTER_CNT	Filter Sample Count

Table continues on the next page...

CMPx_CR0 field descriptions (continued)

Field	Description
	Represents the number of consecutive samples that must agree prior to the comparator ouput filter accepting a new output state. For information regarding filter programming and latency, see the Functional description. 000 Filter is disabled. If SE = 1, then COUT is a logic 0. This is not a legal state, and is not recommended. If SE = 0, COUT = COUTA. 001 One sample must agree. The comparator output is simply sampled. 010 2 consecutive samples must agree. 011 3 consecutive samples must agree. 100 4 consecutive samples must agree. 101 5 consecutive samples must agree. 110 6 consecutive samples must agree. 111 7 consecutive samples must agree.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
HYSTCTR	Comparator hard block hysteresis control Defines the programmable hysteresis level. The hysteresis values associated with each level are device-specific. See the Data Sheet of the device for the exact values. 00 Level 0 01 Level 1 10 Level 2 11 Level 3

44.3.2 CMP Control Register 1 (CMPx_CR1)

Address: Base address + 1h offset

Bit	7	6	5	4	3	2	1	0
Read Write	SE	WE	TRIGM	PMODE	INV	COS	OPE	EN
Reset	0	0	0	0	0	0	0	0

CMPx_CR1 field descriptions

Field	Description
7 SE	Sample Enable At any given time, either SE or WE can be set. If a write to this register attempts to set both, then SE is set and WE is cleared. However, avoid writing 1s to both field locations because this "11" case is reserved and may change in future implementations. 0 Sampling mode is not selected. 1 Sampling mode is selected.
6 WE	Windowing Enable

Table continues on the next page...

CMPx_CR1 field descriptions (continued)

Field	Description
	At any given time, either SE or WE can be set. If a write to this register attempts to set both, then SE is set and WE is cleared. However, avoid writing 1s to both field locations because this "11" case is reserved and may change in future implementations. 0 Windowing mode is not selected. 1 Windowing mode is selected.
5 TRIGM	Trigger Mode Enable CMP and DAC are configured to CMP Trigger mode when CMP_CR1[TRIGM] is set to 1. In addition, the CMP should be enabled. If the DAC is to be used as a reference to the CMP, it should also be enabled. CMP Trigger mode depends on an external timer resource to periodically enable the CMP and 6-bit DAC in order to generate a triggered compare. Upon setting TRIGM, the CMP and DAC are placed in a standby state until an external timer resource trigger is received. See the chip configuration for details about the external timer resource. 0 Trigger mode is disabled. 1 Trigger mode is enabled.
4 PMODE	Power Mode Select See the electrical specifications table in the device Data Sheet for details. 0 Low-Speed (LS) Comparison mode selected. In this mode, CMP has slower output propagation delay and lower current consumption. 1 High-Speed (HS) Comparison mode selected. In this mode, CMP has faster output propagation delay and higher current consumption.
3 INV	Comparator INVERT Allows selection of the polarity of the analog comparator function. It is also driven to the COUT output, on both the device pin and as SCR[COUT], when OPE=0. 0 Does not invert the comparator output. 1 Inverts the comparator output.
2 COS	Comparator Output Select 0 Set the filtered comparator output (CMPO) to equal COUT. 1 Set the unfiltered comparator output (CMPO) to equal COUTA.
1 OPE	Comparator Output Pin Enable 0 CMPO is not available on the associated CMPO output pin. If the comparator does not own the pin, this field has no effect. 1 CMPO is available on the associated CMPO output pin. The comparator output (CMPO) is driven out on the associated CMPO output pin if the comparator owns the pin. If the comparator does not own the field, this bit has no effect.
0 EN	Comparator Module Enable Enables the Analog Comparator module. When the module is not enabled, it remains in the off state, and consumes no power. When the user selects the same input from analog mux to the positive and negative port, the comparator is disabled automatically.

Table continues on the next page...

CMPx_CR1 field descriptions (continued)

Field	Description
	0 Analog Comparator is disabled. 1 Analog Comparator is enabled.

44.3.3 CMP Filter Period Register (CMPx_FPR)

Address: Base address + 2h offset

Bit	7	6	5	4	3	2	1	0
Read Write	FILT_PER							
Reset	0	0	0	0	0	0	0	0

CMPx_FPR field descriptions

Field	Description
FILT_PER	Filter Sample Period Specifies the sampling period, in bus clock cycles, of the comparator output filter, when CR1[SE]=0. Setting FILT_PER to 0x0 disables the filter. Filter programming and latency details appear in the Functional description. This field has no effect when CR1[SE]=1. In that case, the external SAMPLE signal is used to determine the sampling period.

44.3.4 CMP Status and Control Register (CMPx_SCR)

Address: Base address + 3h offset

Bit	7	6	5	4	3	2	1	0
Read	0	DMAEN	0	IER	IEF	CFR	CFF	COUT
Write						w1c	w1c	
Reset	0	0	0	0	0	0	0	0

CMPx_SCR field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 DMAEN	DMA Enable Control Enables the DMA transfer triggered from the CMP module. When this field is set, a DMA request is asserted when CFR or CFF is set. 0 DMA is disabled. 1 DMA is enabled.

Table continues on the next page...

CMPx_SCR field descriptions (continued)

Field	Description
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 IER	Comparator Interrupt Enable Rising Enables the CFR interrupt from the CMP. When this field is set, an interrupt will be asserted when CFR is set. 0 Interrupt is disabled. 1 Interrupt is enabled.
3 IEF	Comparator Interrupt Enable Falling Enables the CFF interrupt from the CMP. When this field is set, an interrupt will be asserted when CFF is set. 0 Interrupt is disabled. 1 Interrupt is enabled.
2 CFR	Analog Comparator Flag Rising Detects a rising-edge on COUT, when set, during normal operation. CFR is cleared by writing 1 to it. During Stop modes, CFR is level sensitive . 0 Rising-edge on COUT has not been detected. 1 Rising-edge on COUT has occurred.
1 CFF	Analog Comparator Flag Falling Detects a falling-edge on COUT, when set, during normal operation. CFF is cleared by writing 1 to it. During Stop modes, CFF is level sensitive . 0 Falling-edge on COUT has not been detected. 1 Falling-edge on COUT has occurred.
0 COUT	Analog Comparator Output Returns the current value of the Analog Comparator output, when read. The field is reset to 0 and will read as CR1[INV] when the Analog Comparator module is disabled, that is, when CR1[EN] = 0. Writes to this field are ignored.

44.3.5 DAC Control Register (CMPx_DACCR)

Address: Base address + 4h offset

Bit	7	6	5	4	3	2	1	0
Read Write	DACEN	VRSEL	VOSEL					
Reset	0	0	0	0	0	0	0	0

CMPx_DACCR field descriptions

Field	Description
7 DACEN	DAC Enable Enables the DAC. When the DAC is disabled, it is powered down to conserve power.

Table continues on the next page...

CMPx_DACCR field descriptions (continued)

Field	Description
	0 DAC is disabled. 1 DAC is enabled.
6 VRSEL	Supply Voltage Reference Source Select 0 V_{in1} is selected as resistor ladder network supply reference. 1 V_{in2} is selected as resistor ladder network supply reference.
VOSEL	DAC Output Voltage Select Selects an output voltage from one of 64 distinct levels. `DACO = (V in /64) * (VOSEL[5:0] + 1)` , so the DACO range is from V_{in} /64 to V_{in} .

44.3.6 MUX Control Register (CMPx_MUXCR)

Address: Base address + 5h offset

Bit	7	6	5	4	3	2	1	0
Read	Reserved	0	PSEL			MSEL		
Write								
Reset	0	0	0	0	0	0	0	0

CMPx_MUXCR field descriptions

Field	Description
7 Reserved	Bit can be programmed to zero only . This field is reserved.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5–3 PSEL	Plus Input Mux Control Determines which input is selected for the plus input of the comparator. For INx inputs, see CMP, DAC, and ANMUX block diagrams. **NOTE:** When an inappropriate operation selects the same input for both muxes, the comparator automatically shuts down to prevent itself from becoming a noise generator. 000 IN0 001 IN1 010 IN2 011 IN3 100 IN4 101 IN5 110 IN6 111 IN7
MSEL	Minus Input Mux Control Determines which input is selected for the minus input of the comparator. For INx inputs, see CMP, DAC, and ANMUX block diagrams.

Table continues on the next page...

CMPx_MUXCR field descriptions (continued)

Field	Description
	NOTE: When an inappropriate operation selects the same input for both muxes, the comparator automatically shuts down to prevent itself from becoming a noise generator. 000 IN0 001 IN1 010 IN2 011 IN3 100 IN4 101 IN5 110 IN6 111 IN7

44.4 Functional description

The CMP module can be used to compare two analog input voltages applied to INP and INM.

CMPO is high when the non-inverting input is greater than the inverting input, and is low when the non-inverting input is less than the inverting input. This signal can be selectively inverted by setting CR1[INV] = 1.

SCR[IER] and SCR[IEF] are used to select the condition which will cause the CMP module to assert an interrupt to the processor. SCR[CFF] is set on a falling-edge and SCR[CFR] is set on rising-edge of the comparator output. The optionally filtered CMPO can be read directly through SCR[COUT].

44.4.1 CMP functional modes

There are the following main sub-blocks to the CMP module:

- The comparator itself
- The window function
- The filter function

The filter, CR0[FILTER_CNT], can be clocked from an internal or external clock source. The filter is programmable with respect to the number of samples that must agree before a change in the output is registered. In the simplest case, only one sample must agree. In this case, the filter acts as a simple sampler.

The external sample input is enabled using CR1[SE]. When set, the output of the comparator is sampled only on rising edges of the sample input.

The "windowing mode" is enabled by setting CR1[WE]. When set, the comparator output is sampled only when WINDOW=1. This feature can be used to ignore the comparator output during time periods in which the input voltages are not valid. This is especially useful when implementing zero-crossing-detection for certain PWM applications.

The comparator filter and sampling features can be combined as shown in the following table. Individual modes are discussed below.

Table 44-2. Comparator sample/filter controls

Mode #	CR1[EN]	CR1[WE]	CR1[SE]	CR0[FILTER_CNT]	FPR[FILT_PER]	Operation
1	0	X	X	X	X	**Disabled** See the Disabled mode (# 1).
2A	1	0	0	0x00	X	**Continuous Mode** See the Continuous mode (#s 2A & 2B).
2B	1	0	0	X	0x00	
3A	1	0	1	0x01	X	**Sampled, Non-Filtered mode** See the Sampled, Non-Filtered mode (#s 3A & 3B).
3B	1	0	0	0x01	> 0x00	
4A	1	0	1	> 0x01	X	**Sampled, Filtered mode** See the Sampled, Filtered mode (#s 4A & 4B).
4B	1	0	0	> 0x01	> 0x00	
5A	1	1	0	0x00	X	**Windowed mode** Comparator output is sampled on every rising bus clock edge when SAMPLE=1 to generate COUTA. See the Windowed mode (#s 5A & 5B).
5B	1	1	0	X	0x00	
6	1	1	0	0x01	0x01–0xFF	**Windowed/Resampled mode** Comparator output is sampled on every rising bus clock edge when SAMPLE=1 to generate COUTA, which is then resampled on an interval determined by FILT_PER to generate COUT. See the Windowed/Resampled mode (# 6).
7	1	1	0	> 0x01	0x01–0xFF	**Windowed/Filtered mode** Comparator output is sampled on every rising bus clock edge when SAMPLE=1 to generate COUTA, which is then resampled and filtered to generate COUT. See the Windowed/Filtered mode (#7).
All other combinations of CR1[EN], CR1[WE], CR1[SE], CR0[FILTER_CNT], and FPR[FILT_PER] are illegal.						

For cases where a comparator is used to drive a fault input, for example, for a motor-control module such as FTM, it must be configured to operate in Continuous mode so that an external fault can immediately pass through the comparator to the target fault circuitry.

Note

Filtering and sampling settings must be changed only after setting CR1[SE]=0 and CR0[FILTER_CNT]=0x00. This resets the filter to a known state.

44.4.1.1 Disabled mode (# 1)

In Disabled mode, the analog comparator is non-functional and consumes no power. CMPO is 0 in this mode.

44.4.1.2 Continuous mode (#s 2A & 2B)

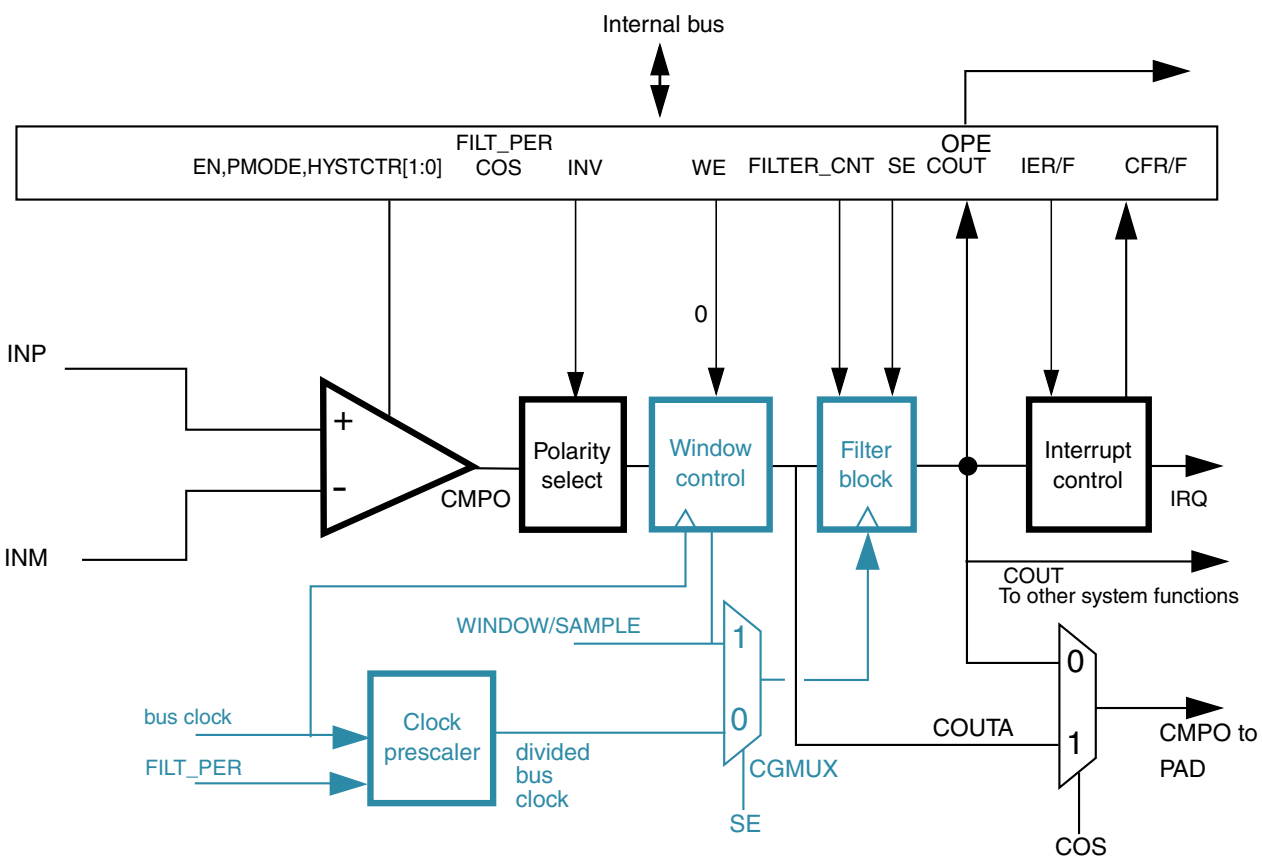


Figure 44-3. Comparator operation in Continuous mode

The analog comparator block is powered and active. CMPO may be optionally inverted, but is not subject to external sampling or filtering. Both window control and filter blocks are completely bypassed. SCR[COUT] is updated continuously. The path from comparator input pins to output pin is operating in combinational unclocked mode. COUT and COUTA are identical.

For control configurations which result in disabling the filter block, see the Filter Block Bypass Logic diagram.

44.4.1.3 Sampled, Non-Filtered mode (#s 3A & 3B)

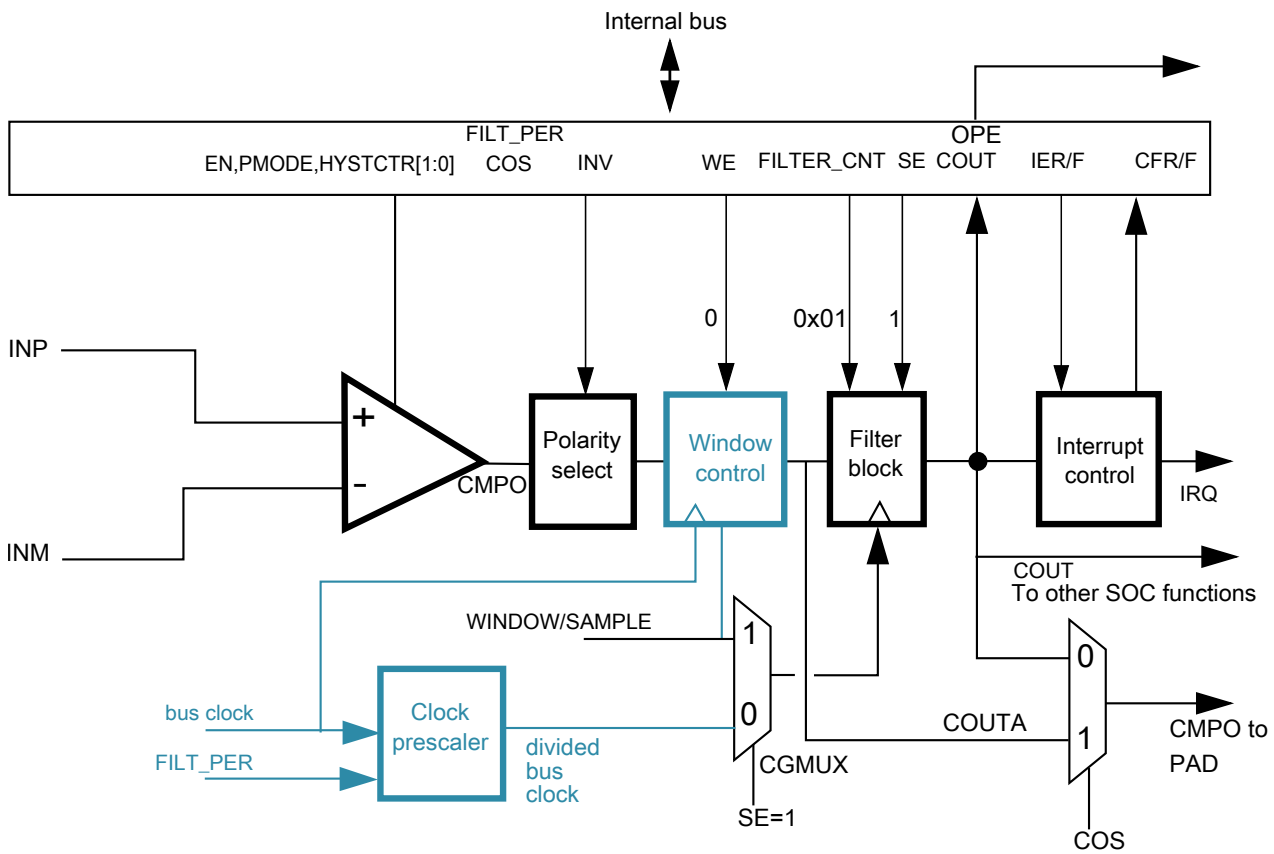


Figure 44-4. Sampled, Non-Filtered (# 3A): sampling point externally driven

In Sampled, Non-Filtered mode, the analog comparator block is powered and active. The path from analog inputs to COUTA is combinational unclocked. Windowing control is completely bypassed. COUTA is sampled whenever a rising-edge is detected on the filter block clock input.

The only difference in operation between Sampled, Non-Filtered (# 3A) and Sampled, Non-Filtered (# 3B) is in how the clock to the filter block is derived. In #3A, the clock to filter block is externally derived while in #3B, the clock to filter block is internally derived.

The comparator filter has no other function than sample/hold of the comparator output in this mode (# 3B).

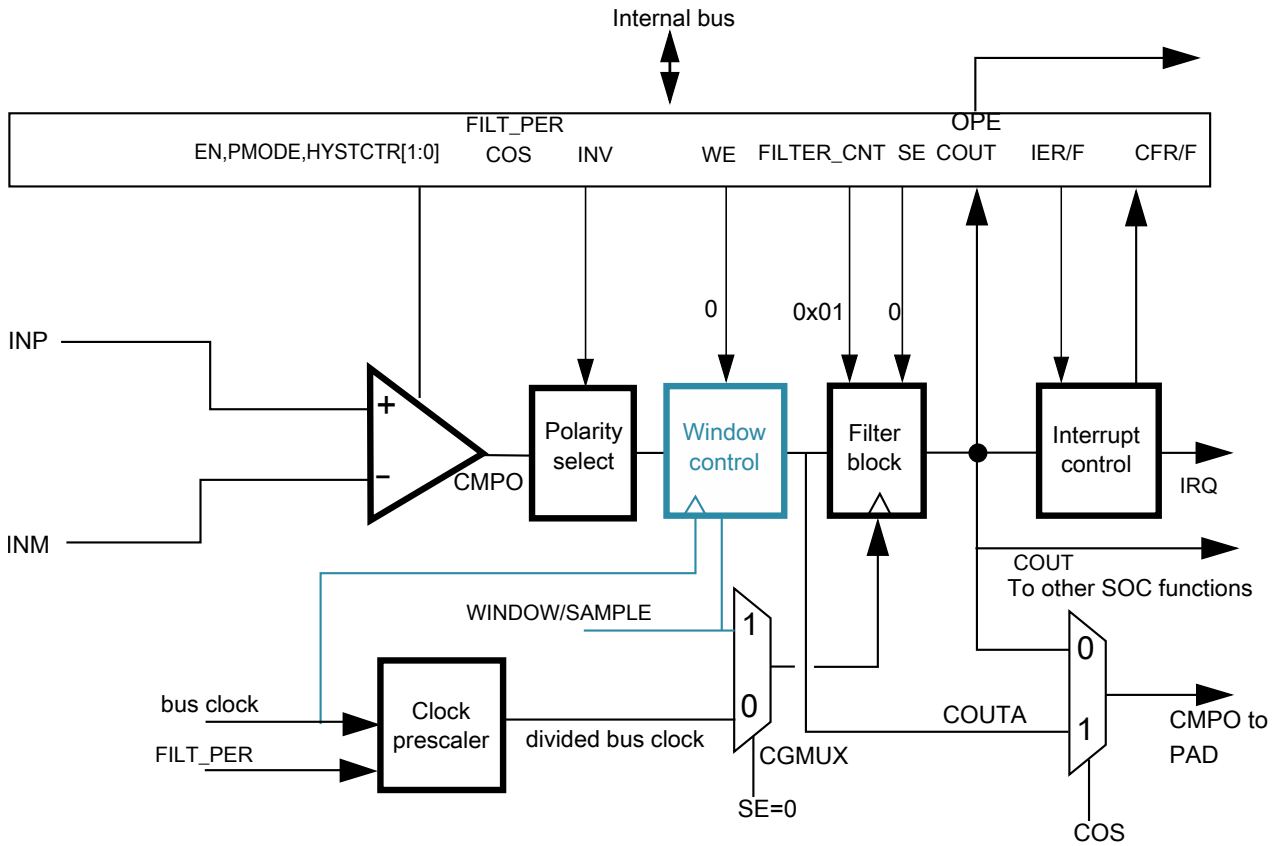


Figure 44-5. Sampled, Non-Filtered (# 3B): sampling interval internally derived

44.4.1.4 Sampled, Filtered mode (#s 4A & 4B)

In Sampled, Filtered mode, the analog comparator block is powered and active. The path from analog inputs to COUTA is combinational unclocked. Windowing control is completely bypassed. COUTA is sampled whenever a rising edge is detected on the filter block clock input.

The only difference in operation between Sampled, Non-Filtered (# 3A) and Sampled, Filtered (# 4A) is that, now, CR0[FILTER_CNT]>1, which activates filter operation.

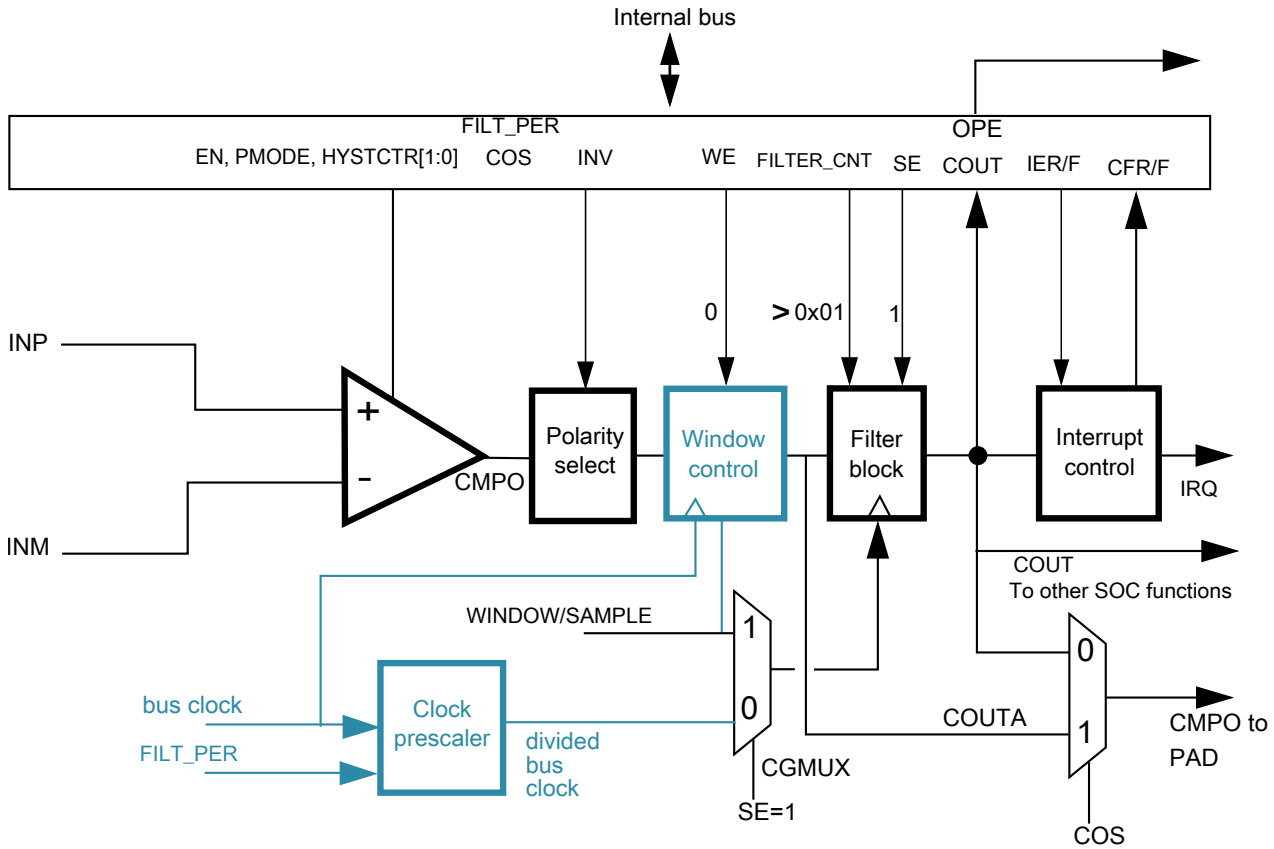


Figure 44-6. Sampled, Filtered (# 4A): sampling point externally driven

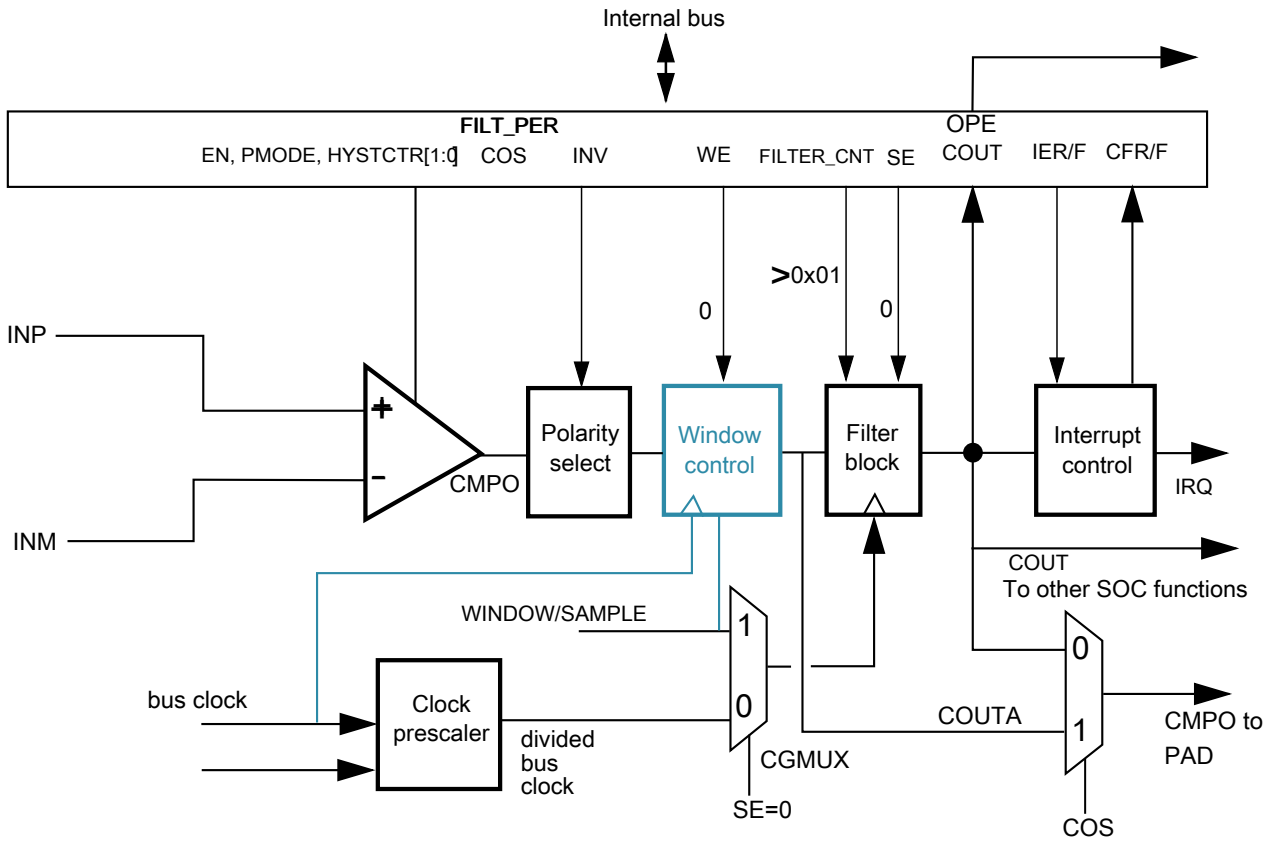


Figure 44-7. Sampled, Filtered (# 4B): sampling point internally derived

The only difference in operation between Sampled, Non-Filtered (# 3B) and Sampled, Filtered (# 4B) is that now, CR0[FILTER_CNT]>1, which activates filter operation.

44.4.1.5 Windowed mode (#s 5A & 5B)

The following figure illustrates comparator operation in the Windowed mode, ignoring latency of the analog comparator, polarity select, and window control block. It also assumes that the polarity select is set to non-inverting state.

NOTE

The analog comparator output is passed to COUTA only when the WINDOW signal is high.

In actual operation, COUTA may lag the analog inputs by up to one bus clock cycle plus the combinational path delay through the comparator and polarity select logic.

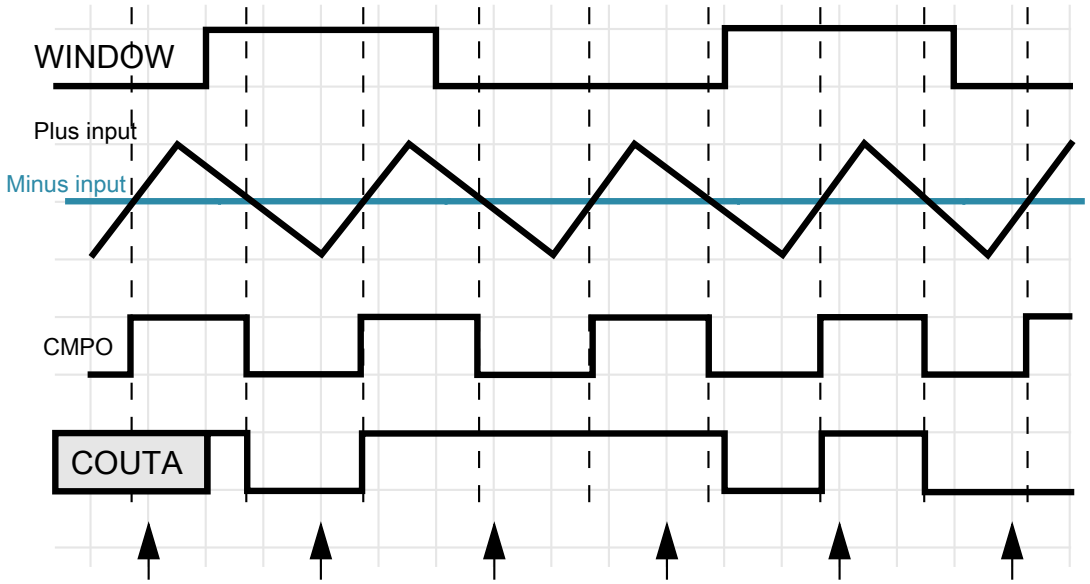


Figure 44-8. Windowed mode operation

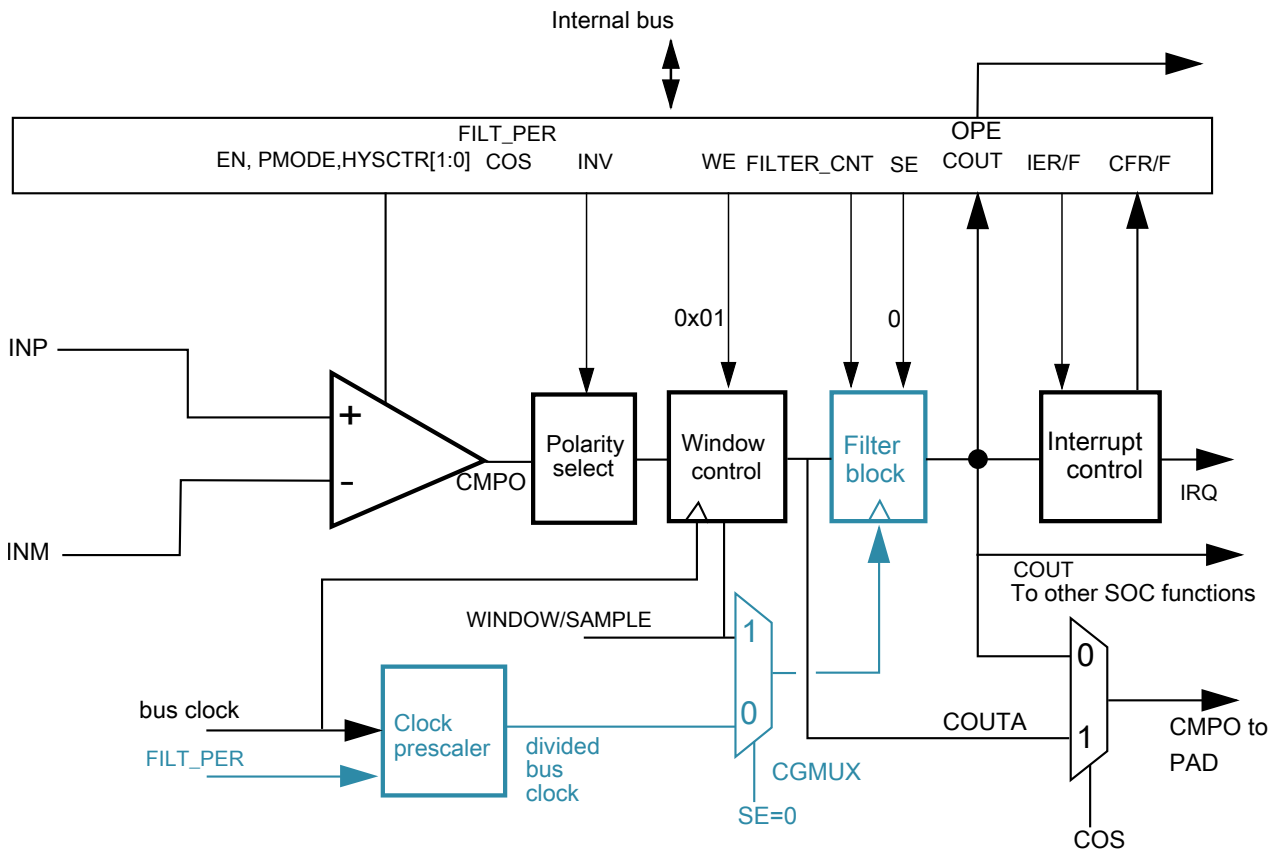


Figure 44-9. Windowed mode

For control configurations which result in disabling the filter block, see Filter Block Bypass Logic diagram.

When any windowed mode is active, COUTA is clocked by the bus clock whenever WINDOW = 1. The last latched value is held when WINDOW = 0.

44.4.1.6 Windowed/Resampled mode (# 6)

The following figure uses the same input stimulus shown in Figure 44-8, and adds resampling of COUTA to generate COUT. Samples are taken at the time points indicated by the arrows in the figure. Again, prop delays and latency are ignored for the sake of clarity.

This example was generated solely to demonstrate operation of the comparator in windowed/resampled mode, and does not reflect any specific application. Depending upon the sampling rate and window placement, COUT may not see zero-crossing events detected by the analog comparator. Sampling period and/or window placement must be carefully considered for a given application.

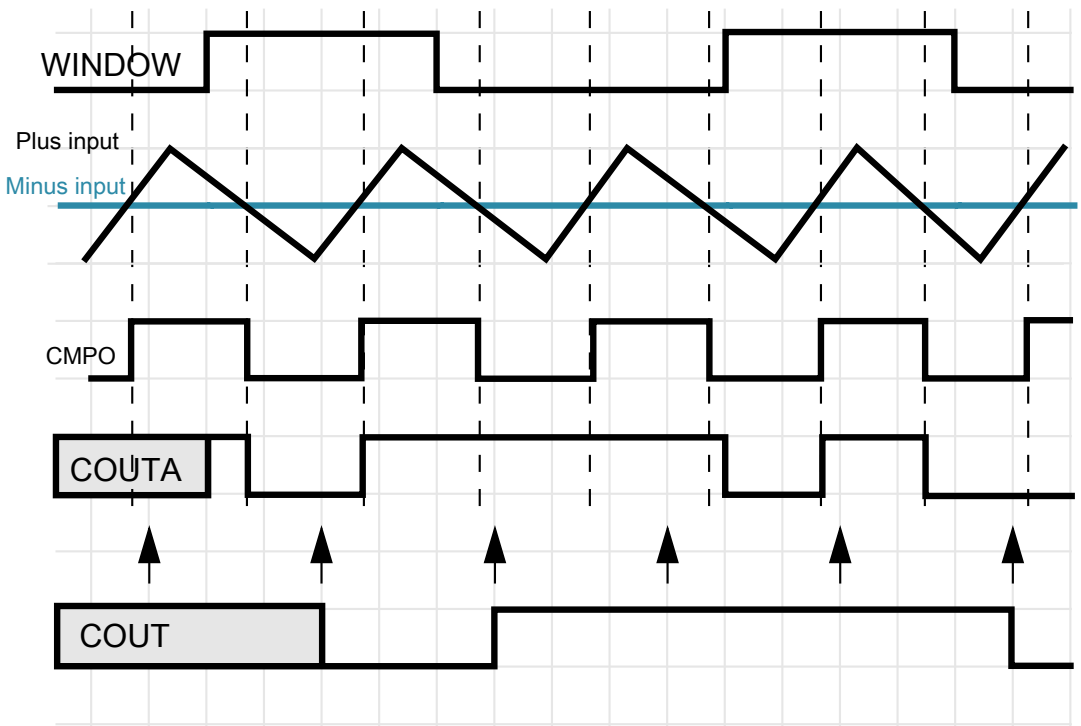


Figure 44-10. Windowed/resampled mode operation

This mode of operation results in an unfiltered string of comparator samples where the interval between the samples is determined by FPR[FILT_PER] and the bus clock rate. Configuration for this mode is virtually identical to that for the Windowed/Filtered Mode shown in the next section. The only difference is that the value of CR0[FILTER_CNT] must be 1.

44.4.1.7 Windowed/Filtered mode (#7)

This is the most complex mode of operation for the comparator block, as it uses both windowing and filtering features. It also has the highest latency of any of the modes. This can be approximated: up to 1 bus clock synchronization in the window function + ((CR0[FILTER_CNT] * FPR[FILT_PER]) + 1) * bus clock for the filter function.

When any windowed mode is active, COUTA is clocked by the bus clock whenever WINDOW = 1. The last latched value is held when WINDOW = 0.

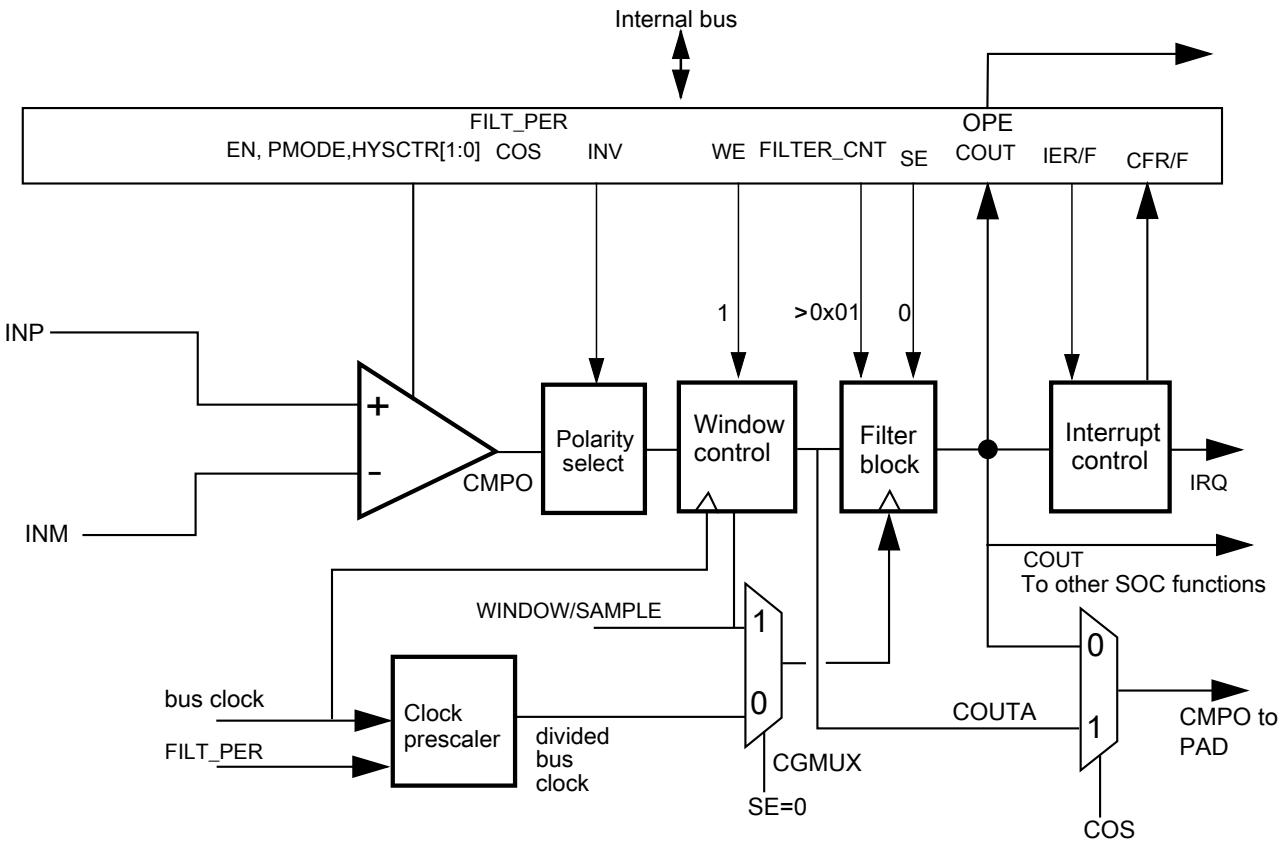


Figure 44-11. Windowed/Filtered mode

44.4.2 Power modes

44.4.2.1 Wait mode operation

During Wait and VLPW modes, the CMP, if enabled, continues to operate normally and a CMP interrupt can wake the MCU.

44.4.2.2 Stop mode operation

Depending on clock restrictions related to the MCU core or core peripherals, the MCU is brought out of stop when a compare event occurs and the corresponding interrupt is enabled. Similarly, if CR1[OPE] is enabled, the comparator output operates as in the normal operating mode and comparator output is placed onto the external pin. In Stop modes, the comparator can be operational in both:

- High-Speed (HS) Comparison mode when CR1[PMODE] = 1
- Low-Speed (LS) Comparison mode when CR1[PMODE] = 0

It is recommended to use the LS mode to minimize power consumption.

If stop is exited with a reset, all comparator registers are put into their reset state.

44.4.2.3 Low-Leakage mode operation

When the chip is in Low-Leakage modes:

- The CMP module is partially functional and is limited to Low-Speed mode, regardless of CR1[PMODE] setting
- Windowed, Sampled, and Filtered modes are not supported
- The CMP output pin is latched and does not reflect the compare output state.

The positive- and negative-input voltage can be supplied from external pins or the DAC output. The MCU can be brought out of the Low-Leakage mode if a compare event occurs and the CMP interrupt is enabled. After wakeup from low-leakage modes, the CMP module is in the reset state except for SCR[CFF] and SCR[CFR].

44.4.3 Startup and operation

A typical startup sequence is listed here.

- The time required to stabilize COUT will be the power-on delay of the comparators plus the largest propagation delay from a selected analog source through the analog comparator, windowing function and filter. See the Data Sheets for power-on delays of the comparators. The windowing function has a maximum of one bus clock period delay. The filter delay is specified in the Low-pass filter.
- During operation, the propagation delay of the selected data paths must always be considered. It may take many bus clock cycles for COUT and SCR[CFR]/SCR[CFF]

to reflect an input change or a configuration change to one of the components involved in the data path.
- When programmed for filtering modes, COUT will initially be equal to 0, until sufficient clock cycles have elapsed to fill all stages of the filter. This occurs even if COUTA is at a logic 1.

44.4.4 Low-pass filter

The low-pass filter operates on the unfiltered and unsynchronized and optionally inverted comparator output COUTA and generates the filtered and synchronized output COUT.

Both COUTA and COUT can be configured as module outputs and are used for different purposes within the system.

Synchronization and edge detection are always used to determine status register bit values. They also apply to COUT for all sampling and windowed modes. Filtering can be performed using an internal timebase defined by FPR[FILT_PER], or using an external SAMPLE input to determine sample time.

The need for digital filtering and the amount of filtering is dependent on user requirements. Filtering can become more useful in the absence of an external hysteresis circuit. Without external hysteresis, high-frequency oscillations can be generated at COUTA when the selected INM and INP input voltages differ by less than the offset voltage of the differential comparator.

44.4.4.1 Enabling filter modes

Filter modes can be enabled by:

- Setting CR0[FILTER_CNT] > 0x01 and
- Setting FPR[FILT_PER] to a nonzero value or setting CR1[SE]=1

If using the divided bus clock to drive the filter, it will take samples of COUTA every FPR[FILT_PER] bus clock cycles.

The filter output will be at logic 0 when first initalized, and will subsequently change when all the consecutive CR0[FILTER_CNT] samples agree that the output value has changed. In other words, SCR[COUT] will be 0 for some initial period, even when COUTA is at logic 1.

Setting both CR1[SE] and FPR[FILT_PER] to 0 disables the filter and eliminates switching current associated with the filtering process.

Note

Always switch to this setting prior to making any changes in filter parameters. This resets the filter to a known state. Switching CR0[FILTER_CNT] on the fly without this intermediate step can result in unexpected behavior.

If CR1[SE]=1, the filter takes samples of COUTA on each positive transition of the sample input. The output state of the filter changes when all the consecutive CR0[FILTER_CNT] samples agree that the output value has changed.

44.4.4.2 Latency issues

The value of FPR[FILT_PER] or SAMPLE period must be set such that the sampling period is just longer than the period of the expected noise. This way a noise spike will corrupt only one sample. The value of CR0[FILTER_CNT] must be chosen to reduce the probability of noisy samples causing an incorrect transition to be recognized. The probability of an incorrect transition is defined as the probability of an incorrect sample raised to the power of CR0[FILTER_CNT].

The values of FPR[FILT_PER] or SAMPLE period and CR0[FILTER_CNT] must also be traded off against the desire for minimal latency in recognizing actual comparator output transitions. The probability of detecting an actual output change within the nominal latency is the probability of a correct sample raised to the power of CR0[FILTER_CNT].

The following table summarizes maximum latency values for the various modes of operation *in the absence of noise*. Filtering latency is restarted each time an actual output transition is masked by noise.

Table 44-3. Comparator sample/filter maximum latencies

Mode #	CR1[EN]	CR1[WE]	CR1[SE]	CR0[FILTER_CNT]	FPR[FILT_PER]	Operation	Maximum latency[1]
1	0	X	X	X	X	Disabled	N/A
2A	1	0	0	0x00	X	Continuous Mode	T_{PD}
2B	1	0	0	X	0x00		
3A	1	0	1	0x01	X	Sampled, Non-Filtered mode	$T_{PD} + T_{SAMPLE} + T_{per}$
3B	1	0	0	0x01	> 0x00		$T_{PD} + (FPR[FILT_PER] * T_{per}) + T_{per}$
4A	1	0	1	> 0x01	X	Sampled, Filtered mode	$T_{PD} + (CR0[FILTER_CNT] * T_{SAMPLE}) + T_{per}$
4B	1	0	0	> 0x01	> 0x00		$T_{PD} + (CR0[FILTER_CNT] * FPR[FILT_PER] \times T_{per}) + T_{per}$

Table continues on the next page...

Table 44-3. Comparator sample/filter maximum latencies (continued)

Mode #	CR1[EN]	CR1[WE]	CR1[SE]	CR0[FILTER_CNT]	FPR[FILT_PER]	Operation	Maximum latency[1]
5A	1	1	0	0x00	X	Windowed mode	$T_{PD} + T_{per}$
5B	1	1	0	X	0x00		$T_{PD} + T_{per}$
6	1	1	0	0x01	0x01 - 0xFF	Windowed / Resampled mode	T_{PD} + (FPR[FILT_PER] * T_{per}) + $2T_{per}$
7	1	1	0	> 0x01	0x01 - 0xFF	Windowed / Filtered mode	T_{PD} + (CR0[FILTER_CNT] * FPR[FILT_PER] x T_{per}) + $2T_{per}$

1. T_{PD} represents the intrinsic delay of the analog component plus the polarity select logic. T_{SAMPLE} is the clock period of the external sample clock. T_{per} is the period of the bus clock.

44.5 CMP interrupts

The CMP module is capable of generating an interrupt on either the rising- or falling-edge of the comparator output, or both.

The following table gives the conditions in which the interrupt request is asserted and deasserted.

When	Then
SCR[IER] and SCR[CFR] are set	The interrupt request is asserted
SCR[IEF] and SCR[CFF] are set	The interrupt request is asserted
SCR[IER] and SCR[CFR] are cleared for a rising-edge interrupt	The interrupt request is deasserted
SCR[IEF] and SCR[CFF] are cleared for a falling-edge interrupt	The interrupt request is deasserted

44.6 DMA support

Normally, the CMP generates a CPU interrupt if there is a change on the COUT. When DMA support is enabled by setting SCR[DMAEN] and the interrupt is enabled by setting SCR[IER], SCR[IEF], or both, the corresponding change on COUT forces a DMA transfer request rather than a CPU interrupt instead. When the DMA has completed the transfer, it sends a transfer completing indicator that deasserts the DMA transfer request and clears the flag to allow a subsequent change on comparator output to occur and force another DMA request.

The comparator can remain functional in STOP modes.

When DMA support is enabled by setting SCR[DMAEN] and the interrupt is enabled by setting SCR[IER], SCR[IEF], or both, the corresponding change on COUT forces a DMA transfer request to wake up the system from STOP modes. After the data transfer has finished, system will go back to STOP modes. Refer to DMA chapters in the device reference manual for the asynchronous DMA function for details.

44.7 CMP Asynchronous DMA support

The comparator can remain functional in STOP modes.

When DMA support is enabled by setting SCR[DMAEN] and the interrupt is enabled by setting SCR[IER], SCR[IEF], or both, the corresponding change on COUT forces a DMA transfer request to wake up the system from STOP modes. After the data transfer has finished, system will go back to STOP modes. Refer to DMA chapters in the device reference manual for the asynchronous DMA function for details.

44.8 Digital-to-analog converter

The figure found here shows the block diagram of the DAC module.

It contains a 64-tap resistor ladder network and a 64-to-1 multiplexer, which selects an output voltage from one of 64 distinct levels that outputs from DACO. It is controlled through the DAC Control Register (DACCR). Its supply reference source can be selected from two sources V_{in1} and V_{in2}. The module can be powered down or disabled when not in use. When in Disabled mode, DACO is connected to the analog ground.

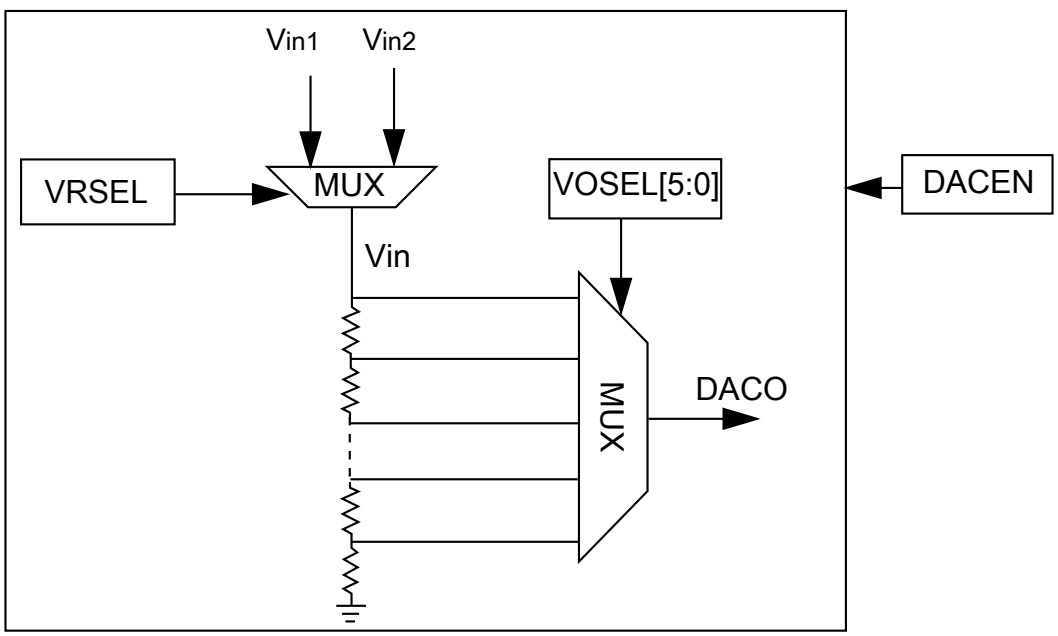


Figure 44-12. 6-bit DAC block diagram

44.9 DAC functional description

This section provides DAC functional description information.

44.9.1 Voltage reference source select

- V_{in1} connects to the primary voltage source as supply reference of 64 tap resistor ladder
- V_{in2} connects to an alternate voltage source

44.10 DAC resets

This module has a single reset input, corresponding to the chip-wide peripheral reset.

44.11 DAC clocks

This module has a single clock input, the bus clock.

44.12 DAC interrupts

This module has no interrupts.

Chapter 45
Voltage Reference (VREFV1)

45.1 Chip-specific VREF information

45.1.1 VREF Overview

This device includes a voltage reference (VREF) to supply an accurate 1.2 V voltage output.

The voltage reference can provide a reference voltage to external peripherals or a reference to analog peripherals, such as the ADC , DAC, or CMP.

NOTE

PMC_REGSC[BGEN] bit must be set if the VREF regulator is required to remain operating in VLPx modes.

NOTE

For either an internal or external reference if the VREF_OUT functionality is being used, VREF_OUT signal must be connected to an output load capacitor. Refer the device data sheet for more details.

45.2 Introduction

The Voltage Reference (VREF) is intended to supply an accurate voltage output that can be trimmed in 0.5 mV steps. The VREF can be used in applications to provide a reference voltage to external devices or used internally as a reference to analog peripherals such as the ADC, DAC, or CMP. The voltage reference has three operating modes that provide different levels of supply rejection and power consumption.

The following figure is a block diagram of the Voltage Reference.

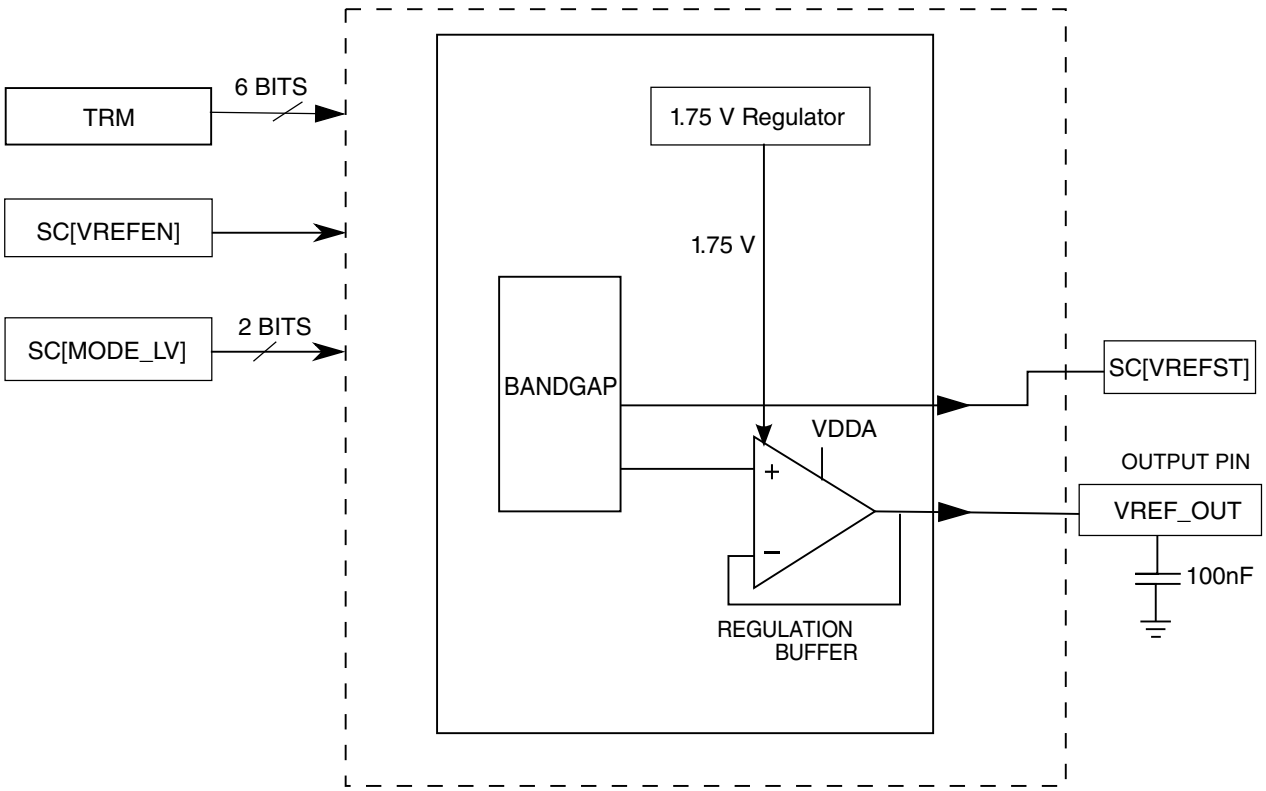


Figure 45-1. Voltage reference block diagram

45.2.1 Overview

The Voltage Reference provides a buffered reference voltage for use as an external reference. In addition, the buffered reference is available internally for use with on chip peripherals such as ADCs and DACs. Refer to the chip configuration details for a description of these options. The reference voltage signal is output on a dedicated output pin when the VREF is enabled. The Voltage Reference output can be trimmed with a resolution of 0.5mV by means of the TRM register TRIM[5:0] bitfield.

45.2.2 Features

The Voltage Reference has the following features:

- Programmable trim register with 0.5 mV steps, automatically loaded with factory trimmed value upon reset
- Programmable buffer mode selection:

- Off
- Bandgap enabled/standby (output buffer disabled)
- Low power buffer mode (output buffer enabled)
- High power buffer mode (output buffer enabled)

- 1.2 V output at room temperature
- Dedicated output pin, VREF_OUT

45.2.3 Modes of Operation

The Voltage Reference continues normal operation in Run, Wait, and Stop modes. The Voltage Reference can also run in Very Low Power Run (VLPR), Very Low Power Wait (VLPW) and Very Low Power Stop (VLPS). If it is desired to use the VREF regulator and/or the chop oscillator in the very low power modes, the system reference voltage (also referred to as the bandgap voltage reference) must be enabled in these modes. Refer to the chip configuration details for information on enabling this mode of operation. Having the VREF regulator enabled does increase current consumption. In very low power modes it may be desirable to disable the VREF regulator to minimize current consumption. Note however that the accuracy of the output voltage will be reduced (by as much as several mVs) when the VREF regulator is not used.

NOTE

The assignment of module modes to core modes is chip-specific. For module-to-core mode assignments, see the chapter that describes how modules are configured.

45.2.4 VREF Signal Descriptions

The following table shows the Voltage Reference signals properties.

Table 45-1. VREF Signal Descriptions

Signal	Description	I/O
VREF_OUT	Internally-generated Voltage Reference output	O

NOTE

When the VREF output buffer is disabled, the status of the VREF_OUT signal is high-impedence.

45.3 Memory Map and Register Definition

VREF memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4007_4000	VREF Trim Register (VREF_TRM)	8	R/W	See section	45.3.1/1422
4007_4001	VREF Status and Control Register (VREF_SC)	8	R/W	00h	45.3.2/1423

45.3.1 VREF Trim Register (VREF_TRM)

This register contains bits that contain the trim data for the Voltage Reference.

Address: 4007_4000h base + 0h offset = 4007_4000h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved	CHOPEN	TRIM					
Reset	x*	0	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

VREF_TRM field descriptions

Field	Description
7 Reserved	This field is reserved. Upon reset this value is loaded with a factory trim value.
6 CHOPEN	Chop oscillator enable. When set, internal chopping operation is enabled and the internal analog offset will be minimized. This bit is set during factory trimming of the VREF voltage. This bit should be written to 1 to achieve the performance stated in the data sheet. If the internal voltage regulator is being used (REGEN bit is set to 1), the chop oscillator must also be enabled. If the chop oscillator is to be used in very low power modes, the system (bandgap) voltage reference must also be enabled. See the chip-specific VREF information (also known as "chip configuration" details) for a description of how this can be achieved. 0 Chop oscillator is disabled. 1 Chop oscillator is enabled.

Table continues on the next page...

VREF_TRM field descriptions (continued)

Field	Description
TRIM	Trim bits These bits change the resulting VREF by approximately ± 0.5 mV for each step. **NOTE:** Min = minimum and max = maximum voltage reference output. For minimum and maximum voltage reference output values, refer to the Data Sheet for this chip. 000000 Min .... 111111 Max

45.3.2 VREF Status and Control Register (VREF_SC)

This register contains the control bits used to enable the internal voltage reference and to select the buffer mode to be used.

Address: 4007_4000h base + 1h offset = 4007_4001h

Bit	7	6	5	4	3	2	1	0
Read	VREFEN	REGEN	ICOMPEN	0	0	VREFST	MODE_LV	
Write								
Reset	0	0	0	0	0	0	0	0

VREF_SC field descriptions

Field	Description
7 VREFEN	Internal Voltage Reference enable This bit is used to enable the bandgap reference within the Voltage Reference module. **NOTE:** After the VREF is enabled, turning off the clock to the VREF module via the corresponding clock gate register will not disable the VREF. VREF must be disabled via this VREFEN bit. 0 The module is disabled. 1 The module is enabled.
6 REGEN	Regulator enable This bit is used to enable the internal 1.75 V regulator to produce a constant internal voltage supply in order to reduce the sensitivity to external supply noise and variation. If it is desired to keep the regulator enabled in very low power modes, refer to the Chip Configuration details for a description on how this can be achieved. This bit should be written to 1 to achieve the performance stated in the data sheet. **NOTE:** See section "Internal voltage regulator" for details on the required sequence to enable the internal regulator.

Table continues on the next page...

VREF_SC field descriptions (continued)

Field	Description
	0 Internal 1.75 V regulator is disabled. 1 Internal 1.75 V regulator is enabled.
5 ICOMPEN	Second order curvature compensation enable This bit should be written to 1 to achieve the performance stated in the data sheet. 0 Disabled 1 Enabled
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 VREFST	Internal Voltage Reference stable This bit indicates that the bandgap reference within the Voltage Reference module has completed its startup and stabilization. **NOTE:** This bit is valid only when the chop oscillator is not being used. 0 The module is disabled or not stable. 1 The module is stable.
MODE_LV	Buffer Mode selection These bits select the buffer modes for the Voltage Reference module. 00 Bandgap on only, for stabilization and startup 01 High power buffer mode enabled 10 Low-power buffer mode enabled 11 Reserved

45.4 Functional Description

The Voltage Reference is a bandgap buffer system. Unity gain amplifiers are used.

The VREF_OUT signal can be used by both internal and external peripherals in low and high power buffer mode. A 100 nF capacitor must always be connected between VREF_OUT and VSSA if the VREF is being used.

The following table shows all possible function configurations of the Voltage Reference.

Table 45-2. Voltage Reference function configurations

SC[VREFEN]	SC[MODE_LV]	Configuration	Functionality
0	X	Voltage Reference disabled	Off
1	00	Voltage Reference enabled, bandgap on only	Startup and standby

Table continues on the next page...

Table 45-2. Voltage Reference function configurations (continued)

SC[VREFEN]	SC[MODE_LV]	Configuration	Functionality
1	01	Voltage Reference enabled, high-power buffer on	VREF_OUT available for internal and external use. 100 nF capacitor is required.
1	10	Voltage Reference enabled, low power buffer on	VREF_OUT available for internal and external use. 100 nF capacitor is required.
1	11	Reserved	Reserved

45.4.1 Voltage Reference Disabled, SC[VREFEN] = 0

When SC[VREFEN] = 0, the Voltage Reference is disabled, the VREF bandgap and the output buffers are disabled. The Voltage Reference is in off mode.

45.4.2 Voltage Reference Enabled, SC[VREFEN] = 1

When SC[VREFEN] = 1, the Voltage Reference is enabled, and different modes should be set by the SC[MODE_LV] bits.

45.4.2.1 SC[MODE_LV]=00

The internal VREF bandgap is enabled to generate an accurate 1.2 V output that can be trimmed with the TRM register's TRIM[5:0] bitfield. The bandgap requires some time for startup and stabilization. SC[VREFST] can be monitored to determine if the stabilization and startup is complete when the chop oscillator is not enabled.

If the chop oscillator is being used, the internal bandgap reference voltage settles within the chop oscillator start up time, Tchop_osc_stup.

The output buffer is disabled in this mode, and there is no buffered voltage output. The Voltage Reference is in standby mode. If this mode is first selected and the low power or high power buffer mode is subsequently enabled, there will be a delay before the buffer output is settled at the final value. This is the buffer start up delay (Tstup) and the value is specified in the appropriate device data sheet.

45.4.2.2 SC[MODE_LV] = 01

The internal VREF bandgap is on. The high power buffer is enabled to generate a buffered 1.2 V voltage to VREF_OUT. It can also be used as a reference to internal analog peripherals such as an ADC channel or analog comparator input.

If this mode is entered from the standby mode (SC[MODE_LV] = 00, SC[VREFEN] = 1) there will be a delay before the buffer output is settled at the final value. This is the buffer start up delay (Tstup) and the value is specified in the appropriate device data sheet. If this mode is entered when the VREF module is enabled then you must wait the longer of Tstup or until SC[VREFST] = 1 when the chop oscillator is not enabled. If the chop oscillator is being used, you must wait the time specified by Tchop_osc_stup (chop oscillator start up time) to ensure the VREF output has stabilized.

In this mode, a 100 nF capacitor is required to connect between the VREF_OUT pin and VSSA.

45.4.2.3 SC[MODE_LV] = 10

The internal VREF bandgap is on. The low power buffer is enabled to generate a buffered 1.2 V voltage to VREF_OUT. It can also be used as a reference to internal analog peripherals such as an ADC channel or analog comparator input.

If this mode is entered from the standby mode (SC[MODE_LV] = 00, SC[VREFEN] = 1) there will be a delay before the buffer output is settled at the final value. This is the buffer start up delay (Tstup) and the value is specified in the appropriate device data sheet. If this mode is entered when the VREF module is enabled then you must wait the longer of Tstup or until SC[VREFST] = 1 when the chop oscillator is not enabled. If the chop oscillator is being used, you must wait the time specified by Tchop_osc_stup (chop oscillator start up time) to ensure the VREF output has stabilized.

In this mode, a 100 nF capacitor is required to connect between the VREF_OUT pin and VSSA.

45.4.2.4 SC[MODE_LV] = 11

Reserved

45.4.3 Internal voltage regulator

The VREF module contains an internal voltage regulator that can be enabled to provide additional supply noise rejection. It is recommended that when possible, this regulator be enabled to provide the optimum VREF performance.

If the internal voltage regulator is being used, the chop oscillator must also be enabled. A specific sequence must be followed when enabling the internal regulator as follows:

1. Enable the chop oscillator (VREF_TRM[CHOPEN] = 1)
2. Configure the VREF_SC register to the desired settings with the internal regulator disabled, VREF_SC[REGEN] = 0
3. Wait > 300ns
4. Enable the internal regulator by setting VREF_SC[REGEN] to 1

45.5 Initialization/Application Information

The Voltage Reference requires some time for startup and stabilization. After SC[VREFEN] = 1, SC[VREFST] can be monitored to determine if the stabilization and startup is completed when the chop oscillator is not enabled. When the chop oscillator is enabled, the settling time of the internal bandgap reference is defined by Tchop_osc_stup (chop oscillator start up time). You must wait this time (Tchop_osc_stup) after the internal bandgap has been enabled to ensure the VREF internal reference voltage has stabilized.

When the Voltage Reference is already enabled and stabilized, changing SC[MODE_LV] will not clear SC[VREFST] but there will be some startup time before the output voltage at the VREF_OUT pin has settled. This is the buffer start up delay (Tstup) and the value is specified in the appropriate device data sheet. Also, there will be some settling time when a step change of the load current is applied to the VREF_OUT pin. When the 1.75V VREF regulator is disabled, the VREF_OUT voltage will be more sensitive to supply voltage variation. It is recommended to use this regulator to achieve optimum VREF_OUT performance.

The TRM[CHOPEN], SC[REGEN] and SC[ICOMPEN] bits must be written to 1 to achieve the performance stated in the device data sheet.

NOTE

See section "Internal voltage regulator" for details on the required sequence to enable the internal regulator.

Chapter 46
12-bit Digital-to-Analog Converter (DAC)

46.1 Chip-specific DAC information

46.1.1 12-bit DAC Overview

This device contains 1 instance of a 12-bit digital-to-analog converter (DAC) with programmable reference generator output. The DAC includes a FIFO for DMA support.

46.1.2 12-bit DAC Output

The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator or ADC.

46.1.3 12-bit DAC Reference

For this device VREF_OUT and VDDA are selectable as the DAC reference. VREF_OUT is connected to the DACREF_1 input and VDDA is connected to the DACREF_2 input. Use DACx_C0[DACRFS] control bit to select between these two options.

Be aware that if the DAC and ADC use the VREF_OUT reference simultaneously, some degradation of ADC accuracy is to be expected due to DAC switching.

46.2 Introduction

The 12-bit digital-to-analog converter (DAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator, op-amps, or ADC.

46.3 Features

The features of the DAC module include:

- On-chip programmable reference generator output. The voltage output range is from 1⁄4096 V_{in} to V_{in}, and the step is 1⁄4096 V_{in}, where V_{in} is the input voltage.
- V_{in} can be selected from two reference sources
- Static operation in Normal Stop mode
- 16-word data buffer supported with configurable watermark and multiple operation modes
- DMA support

46.4 Block diagram

The block diagram of the DAC module is as follows:

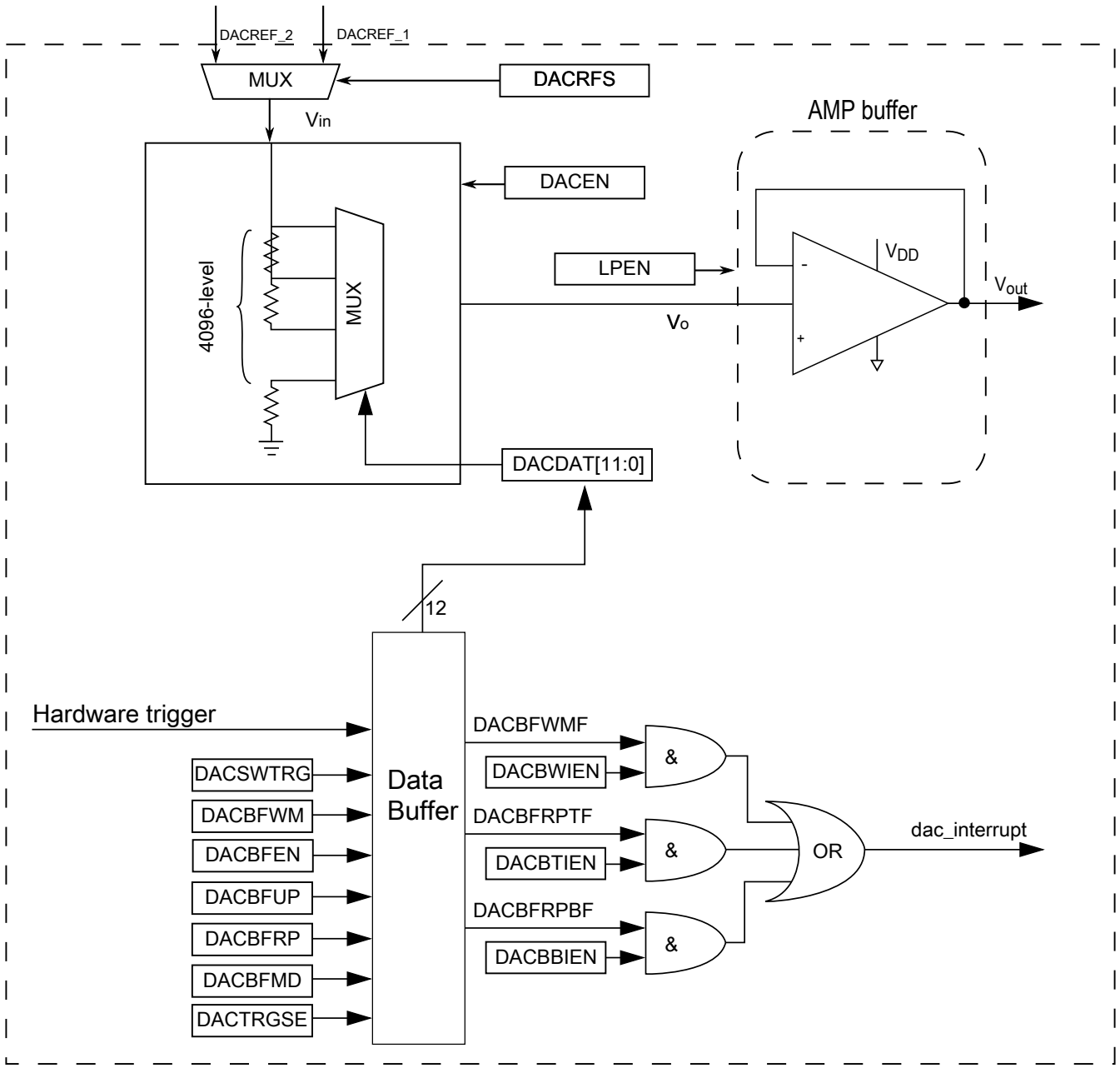


Figure 46-1. DAC block diagram

46.5 Memory map/register definition

The DAC has registers to control analog comparator and programmable voltage divider to perform the digital-to-analog functions.

DAC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400C_C000	DAC Data Low Register (DAC0_DAT0L)	8	R/W	00h	46.5.1/1433
400C_C001	DAC Data High Register (DAC0_DAT0H)	8	R/W	00h	46.5.2/1433
400C_C002	DAC Data Low Register (DAC0_DAT1L)	8	R/W	00h	46.5.1/1433
400C_C003	DAC Data High Register (DAC0_DAT1H)	8	R/W	00h	46.5.2/1433
400C_C004	DAC Data Low Register (DAC0_DAT2L)	8	R/W	00h	46.5.1/1433
400C_C005	DAC Data High Register (DAC0_DAT2H)	8	R/W	00h	46.5.2/1433
400C_C006	DAC Data Low Register (DAC0_DAT3L)	8	R/W	00h	46.5.1/1433
400C_C007	DAC Data High Register (DAC0_DAT3H)	8	R/W	00h	46.5.2/1433
400C_C008	DAC Data Low Register (DAC0_DAT4L)	8	R/W	00h	46.5.1/1433
400C_C009	DAC Data High Register (DAC0_DAT4H)	8	R/W	00h	46.5.2/1433
400C_C00A	DAC Data Low Register (DAC0_DAT5L)	8	R/W	00h	46.5.1/1433
400C_C00B	DAC Data High Register (DAC0_DAT5H)	8	R/W	00h	46.5.2/1433
400C_C00C	DAC Data Low Register (DAC0_DAT6L)	8	R/W	00h	46.5.1/1433
400C_C00D	DAC Data High Register (DAC0_DAT6H)	8	R/W	00h	46.5.2/1433
400C_C00E	DAC Data Low Register (DAC0_DAT7L)	8	R/W	00h	46.5.1/1433
400C_C00F	DAC Data High Register (DAC0_DAT7H)	8	R/W	00h	46.5.2/1433
400C_C010	DAC Data Low Register (DAC0_DAT8L)	8	R/W	00h	46.5.1/1433
400C_C011	DAC Data High Register (DAC0_DAT8H)	8	R/W	00h	46.5.2/1433
400C_C012	DAC Data Low Register (DAC0_DAT9L)	8	R/W	00h	46.5.1/1433
400C_C013	DAC Data High Register (DAC0_DAT9H)	8	R/W	00h	46.5.2/1433
400C_C014	DAC Data Low Register (DAC0_DAT10L)	8	R/W	00h	46.5.1/1433
400C_C015	DAC Data High Register (DAC0_DAT10H)	8	R/W	00h	46.5.2/1433
400C_C016	DAC Data Low Register (DAC0_DAT11L)	8	R/W	00h	46.5.1/1433
400C_C017	DAC Data High Register (DAC0_DAT11H)	8	R/W	00h	46.5.2/1433
400C_C018	DAC Data Low Register (DAC0_DAT12L)	8	R/W	00h	46.5.1/1433
400C_C019	DAC Data High Register (DAC0_DAT12H)	8	R/W	00h	46.5.2/1433
400C_C01A	DAC Data Low Register (DAC0_DAT13L)	8	R/W	00h	46.5.1/1433
400C_C01B	DAC Data High Register (DAC0_DAT13H)	8	R/W	00h	46.5.2/1433
400C_C01C	DAC Data Low Register (DAC0_DAT14L)	8	R/W	00h	46.5.1/1433
400C_C01D	DAC Data High Register (DAC0_DAT14H)	8	R/W	00h	46.5.2/1433
400C_C01E	DAC Data Low Register (DAC0_DAT15L)	8	R/W	00h	46.5.1/1433
400C_C01F	DAC Data High Register (DAC0_DAT15H)	8	R/W	00h	46.5.2/1433
400C_C020	DAC Status Register (DAC0_SR)	8	R/W	02h	46.5.3/1434
400C_C021	DAC Control Register (DAC0_C0)	8	R/W	00h	46.5.4/1435
400C_C022	DAC Control Register 1 (DAC0_C1)	8	R/W	00h	46.5.5/1436
400C_C023	DAC Control Register 2 (DAC0_C2)	8	R/W	0Fh	46.5.6/1437

46.5.1 DAC Data Low Register (DAC*x*_DAT*n*L)

Address: 400C_C000h base + 0h offset + (2d × i), where i=0d to 15d

Bit	7	6	5	4	3	2	1	0
Read Write	DATA0							
Reset	0	0	0	0	0	0	0	0

DAC*x*_DAT*n*L field descriptions

Field	Description
DATA0	DATA0 When the DAC buffer is not enabled, DATA[11:0] controls the output voltage based on the following formula: $V_{out} = V_{in} * (1 + DACDAT0[11:0])/4096$ When the DAC buffer is enabled, DATA is mapped to the 16-word buffer.

46.5.2 DAC Data High Register (DAC*x*_DAT*n*H)

Address: 400C_C000h base + 1h offset + (2d × i), where i=0d to 15d

Bit	7	6	5	4	3	2	1	0
Read	0				DATA1			
Write								
Reset	0	0	0	0	0	0	0	0

DAC*x*_DAT*n*H field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
DATA1	DATA1 When the DAC Buffer is not enabled, DATA[11:0] controls the output voltage based on the following formula. $V_{out} = V_{in} * (1 + DACDAT0[11:0])/4096$ When the DAC buffer is enabled, DATA[11:0] is mapped to the 16-word buffer.

46.5.3 DAC Status Register (DACx_SR)

If DMA is enabled, the flags can be cleared automatically by DMA when the DMA request is done. Writing 0 to a field clears it whereas writing 1 has no effect. After reset, DACBFRPTF is set and can be cleared by software, if needed. The flags are set only when the data buffer status is changed.

Address: 400C_C000h base + 20h offset = 400C_C020h

Bit	7	6	5	4	3	2	1	0
Read	0					DACBFWMF	DACBFRPTF	DACBFRPBF
Write								
Reset	0	0	0	0	0	0	1	0

DACx_SR field descriptions

Field	Description
7–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 DACBFWMF	DAC Buffer Watermark Flag This bit is set if the remaining FIFO data is less than the watermark setting. It is cleared automatically by writing data into FIFO by DMA or CPU. Write to this bit is ignored in FIFO mode. 0 The DAC buffer read pointer has not reached the watermark level. 1 The DAC buffer read pointer has reached the watermark level.
1 DACBFRPTF	DAC Buffer Read Pointer Top Position Flag In FIFO mode, it is FIFO nearly empty flag. It is set when only one data remains in FIFO. Any DAC trigger does not increase the Read Pointer if this bit is set to avoid any possible glitch or abrupt change at DAC output. It is cleared automatically if FIFO is not empty. 0 The DAC buffer read pointer is not zero. 1 The DAC buffer read pointer is zero.
0 DACBFRPBF	DAC Buffer Read Pointer Bottom Position Flag In FIFO mode, it is FIFO FULL status bit. It means FIFO read pointer equals Write Pointer because of Write Pointer increase. If this bit is set, any write to FIFO from either DMA or CPU is ignored by DAC. It is cleared if there is any DAC trigger making the DAC read pointer increase. Write to this bit is ignored in FIFO mode. 0 The DAC buffer read pointer is not equal to C2[DACBFUP]. 1 The DAC buffer read pointer is equal to C2[DACBFUP].

46.5.4 DAC Control Register (DACx_C0)

Address: 400C_C000h base + 21h offset = 400C_C021h

Bit	7	6	5	4	3	2	1	0
Read	DACEN	DACRFS	DACTRGSEL	0	LPEN	DACBWIEN	DACBTIEN	DACBBIEN
Write				DACSWTRG				
Reset	0	0	0	0	0	0	0	0

DACx_C0 field descriptions

Field	Description
7 DACEN	DAC Enable Starts the Programmable Reference Generator operation. 0 The DAC system is disabled. 1 The DAC system is enabled.
6 DACRFS	DAC Reference Select 0 The DAC selects DACREF_1 as the reference voltage. 1 The DAC selects DACREF_2 as the reference voltage.
5 DACTRGSEL	DAC Trigger Select 0 The DAC hardware trigger is selected. 1 The DAC software trigger is selected.
4 DACSWTRG	DAC Software Trigger Active high. This is a write-only field, which always reads 0. If DAC software trigger is selected and buffer is enabled, writing 1 to this field will advance the buffer read pointer once. 0 The DAC soft trigger is not valid. 1 The DAC soft trigger is valid.
3 LPEN	DAC Low Power Control **NOTE:** See the 12-bit DAC electrical characteristics of the device data sheet for details on the impact of the modes below. 0 High-Power mode 1 Low-Power mode
2 DACBWIEN	DAC Buffer Watermark Interrupt Enable 0 The DAC buffer watermark interrupt is disabled. 1 The DAC buffer watermark interrupt is enabled.
1 DACBTIEN	DAC Buffer Read Pointer Top Flag Interrupt Enable 0 The DAC buffer read pointer top flag interrupt is disabled. 1 The DAC buffer read pointer top flag interrupt is enabled.
0 DACBBIEN	DAC Buffer Read Pointer Bottom Flag Interrupt Enable

Table continues on the next page...

DACx_C0 field descriptions (continued)

Field	Description
	0 The DAC buffer read pointer bottom flag interrupt is disabled. 1 The DAC buffer read pointer bottom flag interrupt is enabled.

46.5.5 DAC Control Register 1 (DACx_C1)

Address: 400C_C000h base + 22h offset = 400C_C022h

Bit	7	6	5	4	3	2	1	0
Read	DMAEN	0		DACBFWM		DACBFMD		DACBFEN
Write								
Reset	0	0	0	0	0	0	0	0

DACx_C1 field descriptions

Field	Description
7 DMAEN	DMA Enable Select 0 DMA is disabled. 1 DMA is enabled. When DMA is enabled, the DMA request will be generated by original interrupts. The interrupts will not be presented on this module at the same time.
6–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4–3 DACBFWM	DAC Buffer Watermark Select In normal mode it controls when SR[DACBFWMF] is set. When the DAC buffer read pointer reaches the word defined by this field, which is 1–4 words away from the upper limit (DACBUP), SR[DACBFWMF] will be set. This allows user configuration of the watermark interrupt. In FIFO mode, it is FIFO watermark select field. 00 In normal mode, 1 word . In FIFO mode, 2 or less than 2 data remaining in FIFO will set watermark status bit. 01 In normal mode, 2 words . In FIFO mode, Max/4 or less than Max/4 data remaining in FIFO will set watermark status bit. 10 In normal mode, 3 words . In FIFO mode, Max/2 or less than Max/2 data remaining in FIFO will set watermark status bit. 11 In normal mode, 4 words . In FIFO mode, Max-2 or less than Max-2 data remaining in FIFO will set watermark status bit.
2–1 DACBFMD	DAC Buffer Work Mode Select 00 Normal mode 01 Swing mode 10 One-Time Scan mode 11 FIFO mode
0 DACBFEN	DAC Buffer Enable 0 Buffer read pointer is disabled. The converted data is always the first word of the buffer. 1 Buffer read pointer is enabled. The converted data is the word that the read pointer points to. It means converted data can be from any word of the buffer.

46.5.6 DAC Control Register 2 (DACx_C2)

Address: 400C_C000h base + 23h offset = 400C_C023h

Bit	7	6	5	4	3	2	1	0
Read Write	DACBFRP				DACBFUP			
Reset	0	0	0	0	1	1	1	1

DACx_C2 field descriptions

Field	Description
7–4 DACBFRP	DAC Buffer Read Pointer In normal mode it keeps the current value of the buffer read pointer. FIFO mode, it is the FIFO read pointer. It is writable in FIFO mode. User can configure it to same address to reset FIFO as empty.
DACBFUP	DAC Buffer Upper Limit In normal mode it selects the upper limit of the DAC buffer. The buffer read pointer cannot exceed it. In FIFO mode it is the FIFO write pointer. User cannot set Buffer Up limit in FIFO mode. In Normal mode its reset value is MAX. When IP is configured to FIFO mode, this register becomes Write_Pointer, and its value is initially set to equal READ_POINTER automatically, and the FIFO status is empty. It is writable and user can configure it to the same address to reset FIFO as empty.

46.6 Functional description

The 12-bit DAC module can select one of the two reference inputs—DACREF_1 and DACREF_2 as the DAC reference voltage, V_{in} by C0 [DACRFS]. See the chip-specific DAC information to determine the source options for DACREF_1 and DACREF_2.

When the DAC is enabled, it converts the data in DACDAT0[11:0] or the data from the DAC data buffer to a stepped analog output voltage. The output voltage range is from V_{in} to $V_{in}/4096$, and the step is $V_{in}/4096$.

46.6.1 DAC data buffer operation

When the DAC is enabled and the buffer is not enabled, the DAC module always converts the data in DAT0 to the analog output voltage.

When both the DAC and the buffer are enabled, the DAC converts the data in the data buffer to analog output voltage. The data buffer read pointer advances to the next word whenever a hardware or software trigger event occurs.

The data buffer can be configured to operate in Normal mode, Swing mode, One-Time Scan mode or FIFO mode. When the buffer operation is switched from one mode to another, the read pointer does not change. The read pointer can be set to any value between 0 and C2[DACBFUP] by writing C2[DACBFRP].

46.6.1.1 DAC data buffer interrupts

There are several interrupts and associated flags that can be configured for the DAC buffer. SR[DACBFRPBF] is set when the DAC buffer read pointer reaches the DAC buffer upper limit, that is, C2[DACBFRP] = C2[DACBFUP]. SR[DACBFRPTF] is set when the DAC read pointer is equal to the start position, 0. Finally, SR[DACBFWMF] is set when the DAC buffer read pointer has reached the position defined by C1[DACBFWM]. C1[DACBFWM] can be used to generate an interrupt when the DAC buffer read pointer is between 1 to 4 words from C2[DACBFUP].

46.6.1.2 Modes of DAC data buffer operation

The following table describes the different modes of data buffer operation for the DAC module.

Table 46-1. Modes of DAC data buffer operation

Modes	Description
Buffer Normal mode	This is the default mode. The buffer works as a circular buffer. The read pointer increases by one, every time the trigger occurs. When the read pointer reaches the upper limit, it goes to 0 directly in the next trigger event.
Buffer Swing mode	This mode is similar to the normal mode. However, when the read pointer reaches the upper limit, it does not go to 0. It will descend by 1 in the next trigger events until 0 is reached.
Buffer One-time Scan mode	The read pointer increases by 1 every time the trigger occurs. When it reaches the upper limit, it stops there. If read pointer is reset to the address other than the upper limit, it will increase to the upper address and stop there again. **NOTE:** If the software set the read pointer to the upper limit, the read pointer will not advance in this mode.
FIFO Mode	In FIFO mode, the buffer is organized as a FIFO. For a valid write to any DACDATx, the data is put into the FIFO, and the write pointer is automatically incremented. The module is connected internally to a 32bit interface. For any 16bit or 8bit FIFO access, address bit[1] needs to be 0; otherwise, the write is ignored. For any 32bit FIFO access, the Write_Pointer needs to be an EVEN number; otherwise, the write is ignored.

Table 46-1. Modes of DAC data buffer operation

Modes	Description
	NOTE: A successful 32bit FIFO write will increase the write pointer by 2. Any write will cause the FIFO over-flow will be ignored, the cases includes: 1.FIFO is full, the write will be ignored. 2.FIFO is nearly full (FIFO_SIZE-1), 32bit write will be ignored. **NOTE:** For 8bit write, address bit[0] determine which byte lane will be written to the FIFO according to little endian alignment. Only both byte lanes are written will the write pointer increase. User need to make sure 8bit access happened in pair and both upper & lower bytes are written. There is no requirement on which byte write first. In FIFO mode, there is no change to read access of DACDATx (from normal mode), read to DACDATx will return the DATA addressed by the access address to the data buffer, and both write pointer and read pointer in FIFO mode will NOT be changed by read access. FIFO write can be happened when DAC is not enabled for 1st data conversion enable. But FIFO mode need to work at buffer Enabled at DACC1[DACBFEN]. In FIFO mode, the DATA BUF will be organized as FIFO.

46.6.2 DMA operation

When DMA is enabled, DMA requests are generated instead of interrupt requests. The DMA Done signal clears the DMA request.

The status register flags are still set and are cleared automatically when the DMA completes.

46.6.3 Resets

During reset, the DAC is configured in the default mode and is disabled.

46.6.4 Low-Power mode operation

The following table shows the wait mode and the stop mode operation of the DAC module.

Table 46-2. Modes of operation

Modes of operation	Description
Wait mode	The DAC will operate normally, if enabled.
Stop mode	If enabled, the DAC module continues to operate in Normal Stop mode and the output voltage will hold the value before stop. In low-power stop modes, the DAC is fully shut down.

NOTE

The assignment of module modes to core modes is chip-specific. For module-to-core mode assignments, see the chapter that describes how modules are configured.

Chapter 47
FlexTimer Module (FTM)

47.1 Chip-specific FTM information

47.1.1 Instantiation Information

This device contains FlexTimer modules:

- FTM0
- FTM1
- FTM2
- FTM3

The following table shows how these modules are configured.

Table 47-1. FTM Instantiations

FTM instance	Number of channels	Features/usage
FTM0	8	3-phase motor + 2 general purpose or stepper motor
FTM1	2	Quadrature decoder or general purpose
FTM2	2[1]	Quadrature decoder or general purpose
FTM3	8	3-phase motor + 2 general purpose or stepper motor

1. Only channels 0 and 1 are available.

The configuration of FTM1 and FTM2 adds the Quadrature decoder feature and reduces the number of channels.

47.1.2 External Clock Options

By default each FTM is clocked by the internal bus clock (the FTM refers to it as system clock). Each module contains a register setting that allows the module to be clocked from an external clock instead. There are two external FTM_CLKINx pins that can be selected by any FTM module via the SIM_SOPT4 register.

47.1.3 Fixed frequency clock

The fixed frequency clock for each FTM is MCGFFCLK.

47.1.4 FTM Interrupts

The FlexTimer has multiple sources of interrupts. However, these sources are OR'd together to generate a single interrupt request per FTM module to the interrupt controller. When an FTM interrupt occurs, read the FTM status registers (FMS, SC, and STATUS) to determine the exact interrupt source.

47.1.5 FTM Fault Detection Inputs

The following fault detection input options for the FTM modules are selected via the SIM_SOPT4 register. The external pin option is selected by default.

- FTM0 FAULT0 = FTM0_FLT0 pin or CMP0 output
- FTM0 FAULT1 = FTM0_FLT1 pin or CMP1 output
- FTM0 FAULT2 = FTM0_FLT2 pin
- FTM0 FAULT3 = FTM0_FLT3 pin

- FTM1 FAULT0 = FTM1_FLT0 pin or CMP0 output
- FTM1 FAULT1 = CMP1 output

- FTM2 FAULT0 = FTM2_FLT0 pin or CMP0 output
- FTM2 FAULT1 = CMP1 output

- FTM3 FAULT0 = FTM3_FLT0 pin or CMP0 output

47.1.6 FTM Hardware Triggers

The FTM synchronization hardware triggers are connected in the chip as follows:

- FTM0 hardware trigger 0 = SIM_SOPT8[FTM0SYNCBIT] orCMP0 Outputor FTM1 Match (when enabled in the FTM1 External Trigger (EXTTRIG) register)
- FTM0 hardware trigger 1 = PDB channel 1 Trigger Output or FTM2 Match (when enabled in the FTM2 External Trigger (EXTTRIG) register)
- FTM0 hardware trigger 2 = FTM0_FLT0 pin

- FTM1 hardware trigger 0 = SIM_SOPT8[FTM1SYNCBIT] or CMP0 Output
- FTM1 hardware trigger 1 = CMP1 Output
- FTM1 hardware trigger 2 = FTM1_FLT0 pin

- FTM2 hardware trigger 0 = SIM_SOPT8[FTM2SYNCBIT] or CMP0 Output
- FTM2 hardware trigger 1 = CMP2 Output
- FTM2 hardware trigger 2 = FTM2_FLT0 pin

- FTM3 hardware trigger 0 = SIM_SOPT8[FTM3SYNCBIT] or FTM1 Match (when enabled in the FTM1 External Trigger (EXTTRIG) register)
- FTM3 hardware trigger 1 = FTM2 Match (when enabled in the FTM2 External Trigger (EXTTRIG) register)
- FTM3 hardware trigger 2 = FTM3_FLT0 pin

Having FTMxSYNCBIT fields in the same SOPTx register allows the user to synchronise all FTM timers via their respective TRIG0 input. For the triggers with more than one additional option, the SIM_SOPT4 register implements control fields for selecting the option.

47.1.7 Input capture options for FTM module instances

The following channel 0 input capture source options are selected via SIM_SOPT4. The external pin option is selected by default.

- FTM1 channel 0 input capture = FTM1_CH0 pin or CMP0 output or CMP1 output or USB start of frame pulse
- FTM2 channel 0 input capture = FTM2_CH0 pin or CMP0 output or CMP1 output
- FTM2 channel 1 input capture = FTM2_CH1 pin or exclusive OR of FTM2_CH0, FTM2_CH1, and FTM1_CH1. See FTM Hall sensor support.

NOTE

When the USB start of frame pulse option is selected as an FTM channel input capture, disable the USB SOF token interrupt in the USB Interrupt Enable register (INTEN[SOFTOKEN]) to avoid USB enumeration conflicts.

47.1.8 FTM Hall sensor support

For 3 phase motor control sensor-ed applications the use of Hall sensors, generally 3 sensors placed 120 degrees apart around the rotor, are deployed to detect position and speed. Each of the 3 sensors provides a pulse that applied to an input capture pin, can then be analyzed and both speed and position can be deduced. This device has two 2-channel FTMs. (FTM1 and FTM2) and thus provides 4 input capture pins. To simplify the calculations required by the CPU on each hall sensor's input, if all 3 inputs are "exclusively OR'd " into one timer channel and the free running counter is refreshed on every edge then this can simplify the speed calculation.

Via the SIM module and SIM_SOPT4 register the FTM2CH1SRC bit provides the choice of normal FTM2_CH1 input or the XOR of FTM2_CH0, FTM2_CH1 and FTM1_CH1 pins that will be applied to FTM2_CH1.

Note: If the user utilizes FTM1_CH1 to be an input to FTM2_CH1, FTM1_CH0 can still be utilized for other functions.

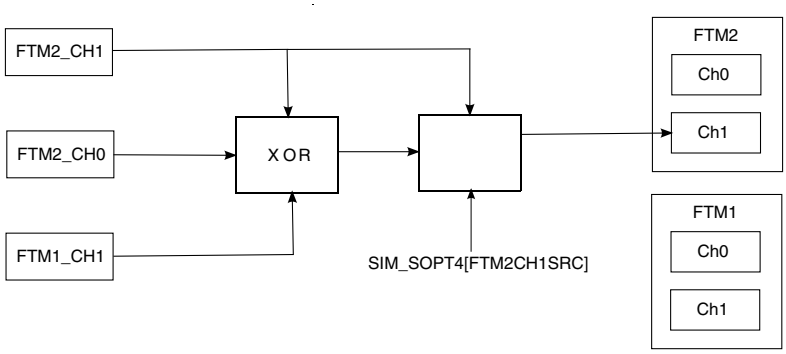


Figure 47-1. FTM Hall Sensor Configuration

47.1.9 FTM modulation implementation

FTM0 and FTM3 support a modulation function where the output channels when configured as PWM or Output Compare mode modulate another timer output when the channel signal is asserted. Any of the 8 channels of FTM0 and any of the 8 channels of FTM3 can be configured to support this modulation function.

The SIM_SOPT8 register has eight control bits (FTM0CHySRC) that allow the user to select normal PWM/Output Compare mode on the corresponding FTM timer channel or modulate with FTM1_CH1. The diagram below shows the implementation for FTM0.

FTM3 has similar implementation controlled by SIM_SOPT8[FTM3CHySRC] on each of its 8 channels with modulation possible via FTM2_CH1. See SIM Block Guide for further information.

When FTM1_CH1 is used to modulate an FTM0 channel, then the user must configure FTM1_CH1 to provide a signal that has a higher frequency than the modulated FTM0 channel output. Also it limits the use of the FTM1_CH0 function, as the FTM1_CH1 will be programmed to provide a 50% duty PWM signal and limit the start and modulus values for the free running counter. FTM2 has a similar restriction when FTM2_CH1 is used for modulating an FTM3 channel.

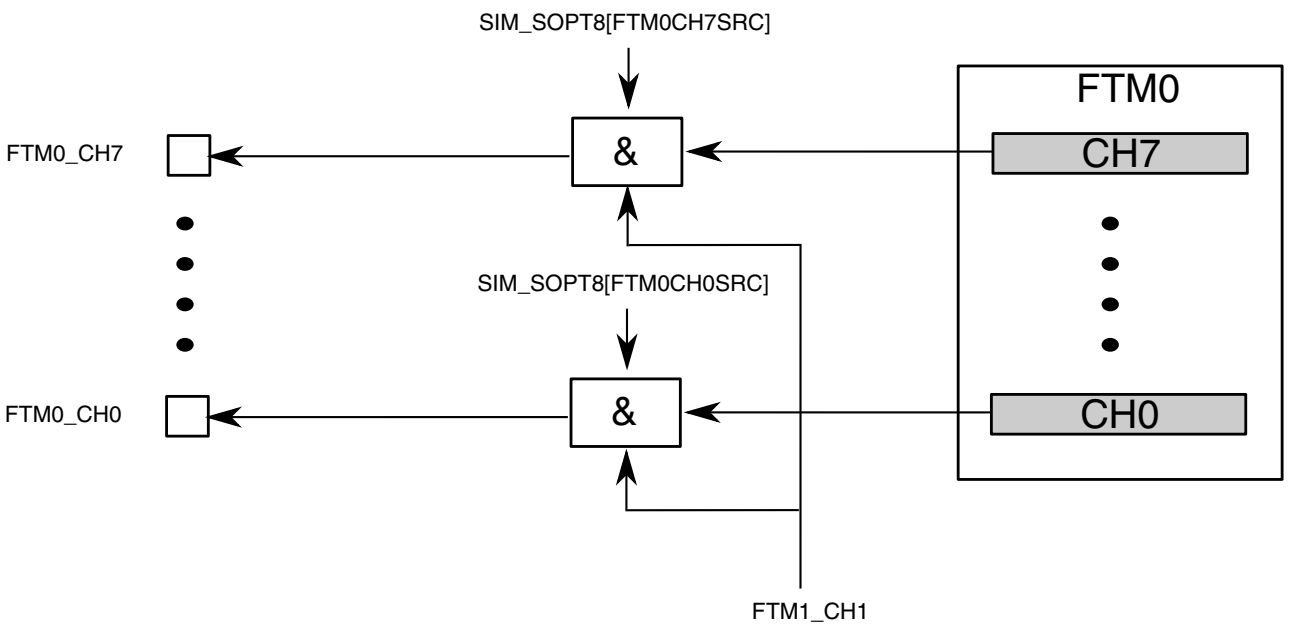


Figure 47-2. FTM Output Modulation

47.1.10 FTM output triggers for other modules

FTM output triggers can be selected as input triggers for the PDB and ADC modules. See PDB Instantiation and ADC triggers.

47.1.11 FTM Global Time Base

This chip provides the optional FTM global time base feature (see Global time base (GTB)).

FTM0 provides the only source for the FTM global time base. The other FTM modules can share the time base as shown in the following figure:

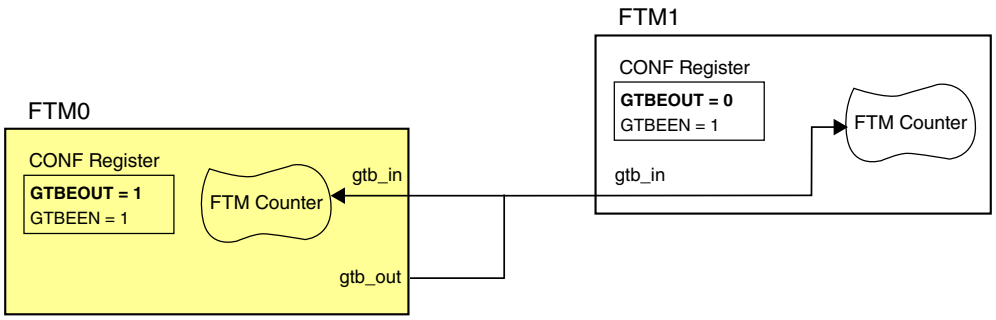


Figure 47-3. FTM Global Time Base Configuration

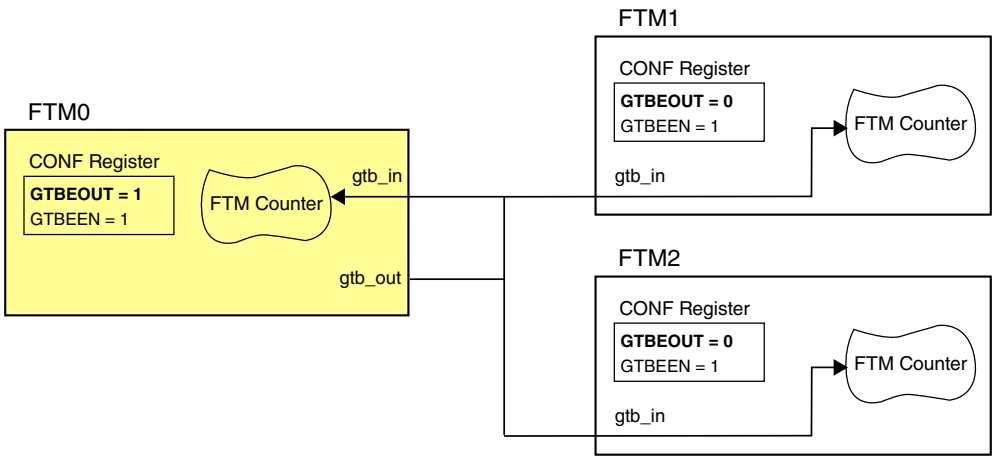


Figure 47-4. FTM Global Time Base Configuration

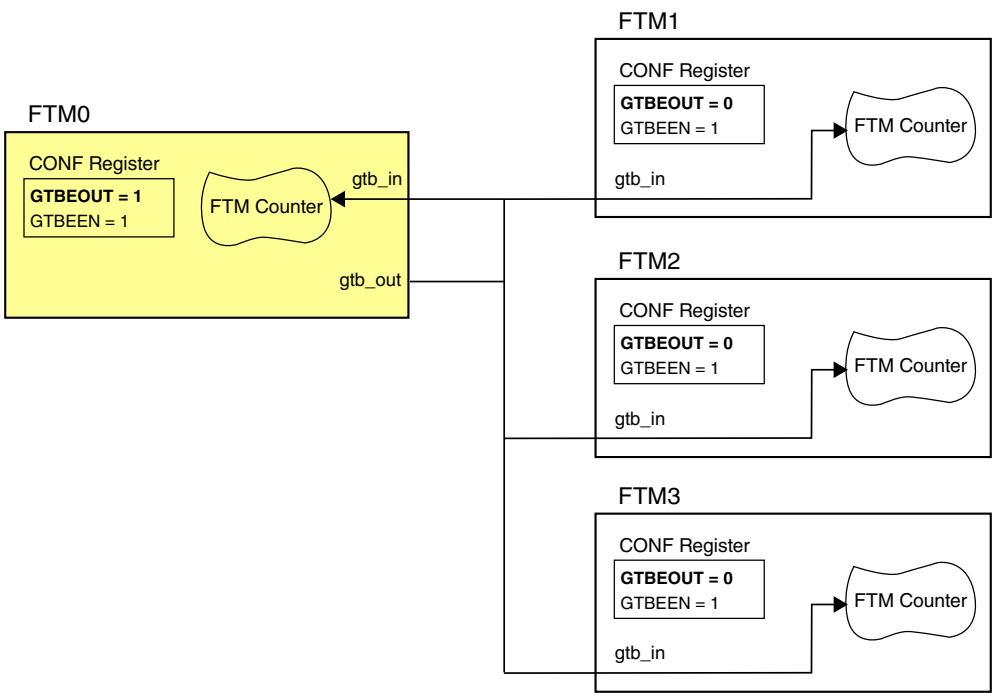


Figure 47-5. FTM Global Time Base Configuration

47.1.12 FTM BDM and debug halt mode

In the FTM chapter, references to the chip being in "BDM" are the same as the chip being in “debug halt mode".

47.2 Introduction

The FlexTimer module (FTM) is a two-to-eight channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The FTM time reference is a 16-bit counter that can be used as an unsigned or signed counter.

NOTE

The number of channels supported can vary for each instance of the FTM module on a chip. See the chip-specific FTM information to see how many channels are supported for each module instance. For example, if a module instance supports only six channels, references to channel numbers 6 and 7 do not apply for that instance.

47.2.1 FlexTimer philosophy

The FlexTimer is built upon a simple timer, the HCS08 Timer PWM Module – TPM, used for many years on Freescale's 8-bit microcontrollers. The FlexTimer extends the functionality to meet the demands of motor control, digital lighting solutions, and power conversion, while providing low cost and backwards compatibility with the TPM module.

Several key enhancements are made:

- Signed up counter
- Deadtime insertion hardware
- Fault control inputs
- Enhanced triggering functionality
- Initialization and polarity control

All of the features common with the TPM have fully backwards compatible register assignments. The FlexTimer can also use code on the same core platform without change to perform the same functions.

Motor control and power conversion features have been added through a dedicated set of registers and defaults turn off all new features. The new features, such as hardware deadtime insertion, polarity, fault control, and output forcing and masking, greatly reduce loading on the execution software and are usually each controlled by a group of registers.

FlexTimer input triggers can be from comparators, ADC, or other submodules to initiate timer functions automatically. These triggers can be linked in a variety of ways during integration of the sub modules so please note the options available for used FlexTimer configuration.

More than one FlexTimers may be synchronized to provide a larger timer with their counters incrementing in unison, assuming the initialization, the input clocks, the initial and final counting values are the same in each FlexTimer.

All main user access registers are buffered to ease the load on the executing software. A number of trigger options exist to determine which registers are updated with this user defined data.

47.2.2 Features

The FTM features include:

- FTM source clock is selectable.
  - The source clock can be the system clock, the fixed frequency clock, or an external clock
  - Fixed frequency clock is an additional clock input to allow the selection of an on chip clock source other than the system clock
  - Selecting external clock connects FTM clock to a chip level input pin therefore allowing to synchronize the FTM counter with an off chip clock source
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- 16-bit counter
  - It can be a free-running counter or a counter with initial and final value
  - The counting can be up or up-down
- Each channel can be configured for input capture, output compare, or edge-aligned PWM mode
- In Input Capture mode:
  - The capture can occur on rising edges, falling edges or both edges
  - An input filter can be selected for some channels

- In Output Compare mode the output signal can be set, cleared, or toggled on match
- All channels can be configured for center-aligned PWM mode
- Each pair of channels can be combined to generate a PWM signal with independent control of both edges of PWM signal
- The FTM channels can operate as pairs with equal outputs, pairs with complementary outputs, or independent channels with independent outputs
- The deadtime insertion is available for each complementary pair
- Generation of match triggers
- Initialization trigger
- Software control of PWM outputs
- Up to 4 fault inputs for global fault control
- The polarity of each channel is configurable
- The generation of an interrupt per channel
- The generation of an interrupt when the counter overflows
- The generation of an interrupt when the fault condition is detected
- Synchronized loading of write buffered FTM registers
- Write protection for critical registers
- Backwards compatible with TPM
- Testing of input captures for a stuck at zero and one conditions
- Dual edge capture for pulse and period width measurement
- Quadrature decoder with input filters, relative position counting, and interrupt on position count or capture of position count on external event

47.2.3 Modes of operation

When the chip is in an active BDM mode, the FTM temporarily suspends all counting until the chip returns to normal user operating mode. During Stop mode, all FTM input clocks are stopped, so the FTM is effectively disabled until clocks resume. During Wait mode, the FTM continues to operate normally. If the FTM does not need to produce a

real time reference or provide the interrupt sources needed to wake the chip from Wait mode, the power can then be saved by disabling FTM functions before entering Wait mode.

47.2.4 Block diagram

The FTM uses one input/output (I/O) pin per channel, CHn (FTM channel (n)) where n is the channel number (0–7).

The following figure shows the FTM structure. The central component of the FTM is the 16-bit counter with programmable initial and final values and its counting can be up or up-down.

NOTE

The number of channels supported can vary for each instance of the FTM module on a chip. See the chip-specific FTM information to see how many channels are supported for each module instance. For example, if a module instance supports only six channels, references to channel numbers 6 and 7 do not apply for that instance.

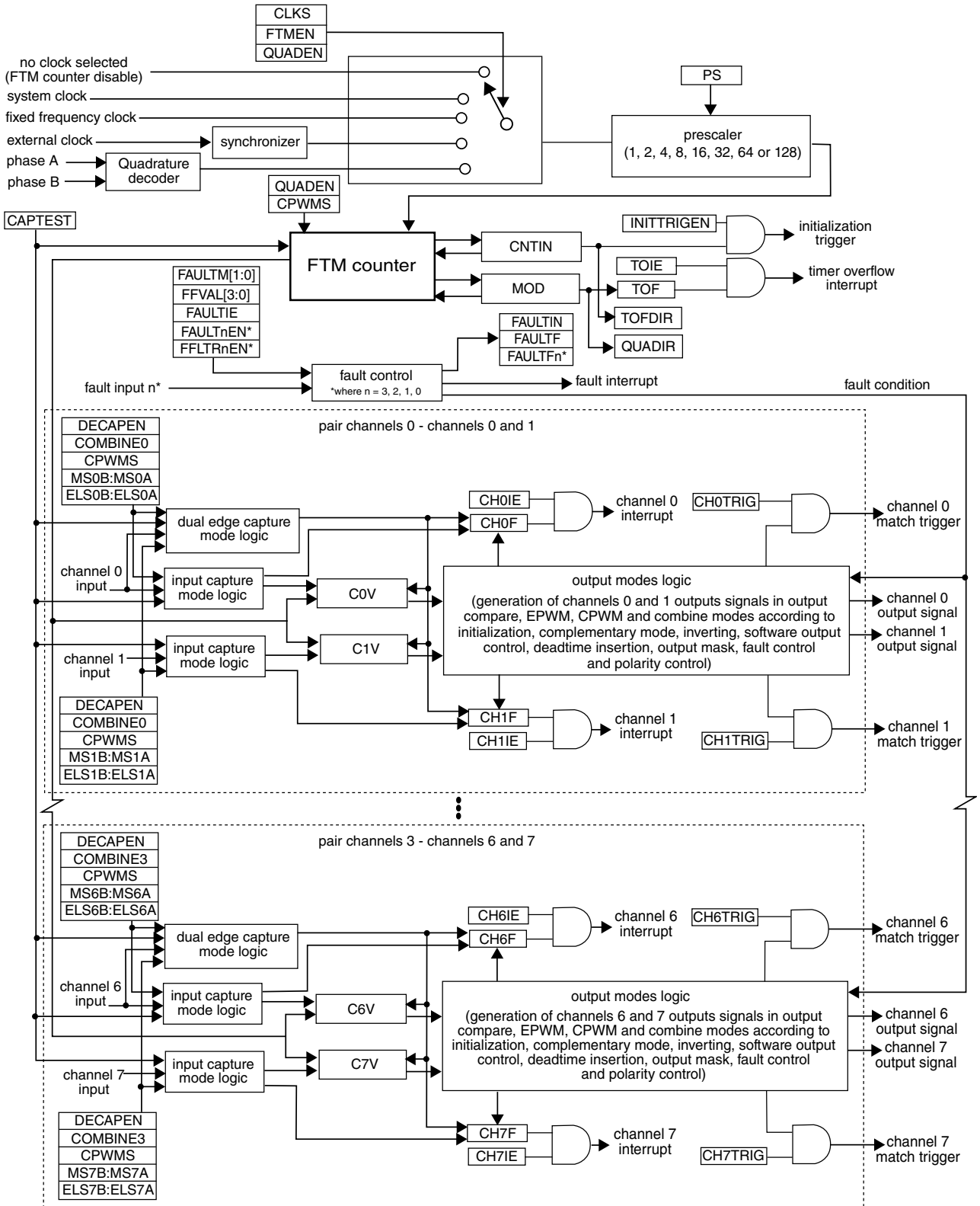


Figure 47-6. FTM block diagram

47.3 FTM signal descriptions

Table 47-2 shows the user-accessible signals for the FTM.

Table 47-2. FTM signal descriptions

Signal	Description	I/O	Function
EXTCLK	External clock. FTM external clock can be selected to drive the FTM counter.	I	The external clock input signal is used as the FTM counter clock if selected by CLKS[1:0] bits in the SC register. This clock signal must not exceed 1/4 of system clock frequency. The FTM counter prescaler selection and settings are also used when an external clock is selected.
CHn	FTM channel (n), where n can be 7-0	I/O	Each FTM channel can be configured to operate either as input or output. The direction associated with each channel, input or output, is selected according to the mode assigned for that channel.
FAULTj	Fault input (j), where j can be 3-0	I	The fault input signals are used to control the CHn channel output state. If a fault is detected, the FAULTj signal is asserted and the channel output is put in a safe state. The behavior of the fault logic is defined by the FAULTM[1:0] control bits in the MODE register and FAULTEN bit in the COMBINEm register. Note that each FAULTj input may affect all channels selectively since FAULTM[1:0] and FAULTEN control bits are defined for each pair of channels. Because there are several FAULTj inputs, maximum of 4 for the FTM module, each one of these inputs is activated by the FAULTjEN bit in the FLTCTRL register.
PHA	Quadrature decoder phase A input. Input pin associated with quadrature decoder phase A.	I	The quadrature decoder phase A input is used as the Quadrature Decoder mode is selected. The phase A input signal is one of the signals that control the FTM counter increment or decrement in the Quadrature Decoder mode.
PHB	Quadrature decoder phase B input. Input pin associated with quadrature decoder phase B.	I	The quadrature decoder phase B input is used as the Quadrature Decoder mode is selected. The phase B input signal is one of the signals that control the FTM counter increment or decrement in the Quadrature Decoder mode.

47.4 Memory map and register definition

47.4.1 Memory map

This section presents a high-level summary of the FTM registers and how they are mapped.

The registers and bits of an unavailable function in the FTM remain in the memory map and in the reset value, but they have no active function.

Note

Do not write in the region from the CNTIN register through the PWMLOAD register when FTMEN = 0.

NOTE

The number of channels supported can vary for each instance of the FTM module on a chip. See the chip-specific FTM information to see how many channels are supported for each module instance. For example, if a module instance supports only six channels, references to channel numbers 6 and 7 do not apply for that instance.

47.4.2 Register descriptions

Accesses to reserved addresses result in transfer errors. Registers for absent channels are considered reserved.

FTM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_8000	Status And Control (FTM0_SC)	32	R/W	0000_0000h	47.4.3/1459
4003_8004	Counter (FTM0_CNT)	32	R/W	0000_0000h	47.4.4/1460
4003_8008	Modulo (FTM0_MOD)	32	R/W	0000_0000h	47.4.5/1461
4003_800C	Channel (n) Status And Control (FTM0_C0SC)	32	R/W	0000_0000h	47.4.6/1462
4003_8010	Channel (n) Value (FTM0_C0V)	32	R/W	0000_0000h	47.4.7/1465
4003_8014	Channel (n) Status And Control (FTM0_C1SC)	32	R/W	0000_0000h	47.4.6/1462
4003_8018	Channel (n) Value (FTM0_C1V)	32	R/W	0000_0000h	47.4.7/1465
4003_801C	Channel (n) Status And Control (FTM0_C2SC)	32	R/W	0000_0000h	47.4.6/1462
4003_8020	Channel (n) Value (FTM0_C2V)	32	R/W	0000_0000h	47.4.7/1465
4003_8024	Channel (n) Status And Control (FTM0_C3SC)	32	R/W	0000_0000h	47.4.6/1462
4003_8028	Channel (n) Value (FTM0_C3V)	32	R/W	0000_0000h	47.4.7/1465
4003_802C	Channel (n) Status And Control (FTM0_C4SC)	32	R/W	0000_0000h	47.4.6/1462
4003_8030	Channel (n) Value (FTM0_C4V)	32	R/W	0000_0000h	47.4.7/1465
4003_8034	Channel (n) Status And Control (FTM0_C5SC)	32	R/W	0000_0000h	47.4.6/1462
4003_8038	Channel (n) Value (FTM0_C5V)	32	R/W	0000_0000h	47.4.7/1465
4003_803C	Channel (n) Status And Control (FTM0_C6SC)	32	R/W	0000_0000h	47.4.6/1462
4003_8040	Channel (n) Value (FTM0_C6V)	32	R/W	0000_0000h	47.4.7/1465
4003_8044	Channel (n) Status And Control (FTM0_C7SC)	32	R/W	0000_0000h	47.4.6/1462
4003_8048	Channel (n) Value (FTM0_C7V)	32	R/W	0000_0000h	47.4.7/1465
4003_804C	Counter Initial Value (FTM0_CNTIN)	32	R/W	0000_0000h	47.4.8/1465

Table continues on the next page...

FTM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_8050	Capture And Compare Status (FTM0_STATUS)	32	R/W	0000_0000h	47.4.9/1466
4003_8054	Features Mode Selection (FTM0_MODE)	32	R/W	0000_0004h	47.4.10/ 1468
4003_8058	Synchronization (FTM0_SYNC)	32	R/W	0000_0000h	47.4.11/ 1470
4003_805C	Initial State For Channels Output (FTM0_OUTINIT)	32	R/W	0000_0000h	47.4.12/ 1472
4003_8060	Output Mask (FTM0_OUTMASK)	32	R/W	0000_0000h	47.4.13/ 1473
4003_8064	Function For Linked Channels (FTM0_COMBINE)	32	R/W	0000_0000h	47.4.14/ 1475
4003_8068	Deadtime Insertion Control (FTM0_DEADTIME)	32	R/W	0000_0000h	47.4.15/ 1480
4003_806C	FTM External Trigger (FTM0_EXTTRIG)	32	R/W	0000_0000h	47.4.16/ 1481
4003_8070	Channels Polarity (FTM0_POL)	32	R/W	0000_0000h	47.4.17/ 1483
4003_8074	Fault Mode Status (FTM0_FMS)	32	R/W	0000_0000h	47.4.18/ 1485
4003_8078	Input Capture Filter Control (FTM0_FILTER)	32	R/W	0000_0000h	47.4.19/ 1487
4003_807C	Fault Control (FTM0_FLTCTRL)	32	R/W	0000_0000h	47.4.20/ 1488
4003_8080	Quadrature Decoder Control And Status (FTM0_QDCTRL)	32	R/W	0000_0000h	47.4.21/ 1491
4003_8084	Configuration (FTM0_CONF)	32	R/W	0000_0000h	47.4.22/ 1493
4003_8088	FTM Fault Input Polarity (FTM0_FLTPOL)	32	R/W	0000_0000h	47.4.23/ 1494
4003_808C	Synchronization Configuration (FTM0_SYNCONF)	32	R/W	0000_0000h	47.4.24/ 1495
4003_8090	FTM Inverting Control (FTM0_INVCTRL)	32	R/W	0000_0000h	47.4.25/ 1497
4003_8094	FTM Software Output Control (FTM0_SWOCTRL)	32	R/W	0000_0000h	47.4.26/ 1498
4003_8098	FTM PWM Load (FTM0_PWMLOAD)	32	R/W	0000_0000h	47.4.27/ 1501
4003_9000	Status And Control (FTM1_SC)	32	R/W	0000_0000h	47.4.3/1459
4003_9004	Counter (FTM1_CNT)	32	R/W	0000_0000h	47.4.4/1460
4003_9008	Modulo (FTM1_MOD)	32	R/W	0000_0000h	47.4.5/1461
4003_900C	Channel (n) Status And Control (FTM1_C0SC)	32	R/W	0000_0000h	47.4.6/1462
4003_9010	Channel (n) Value (FTM1_C0V)	32	R/W	0000_0000h	47.4.7/1465
4003_9014	Channel (n) Status And Control (FTM1_C1SC)	32	R/W	0000_0000h	47.4.6/1462

Table continues on the next page...

FTM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_9018	Channel (n) Value (FTM1_C1V)	32	R/W	0000_0000h	47.4.7/1465
4003_901C	Channel (n) Status And Control (FTM1_C2SC)	32	R/W	0000_0000h	47.4.6/1462
4003_9020	Channel (n) Value (FTM1_C2V)	32	R/W	0000_0000h	47.4.7/1465
4003_9024	Channel (n) Status And Control (FTM1_C3SC)	32	R/W	0000_0000h	47.4.6/1462
4003_9028	Channel (n) Value (FTM1_C3V)	32	R/W	0000_0000h	47.4.7/1465
4003_902C	Channel (n) Status And Control (FTM1_C4SC)	32	R/W	0000_0000h	47.4.6/1462
4003_9030	Channel (n) Value (FTM1_C4V)	32	R/W	0000_0000h	47.4.7/1465
4003_9034	Channel (n) Status And Control (FTM1_C5SC)	32	R/W	0000_0000h	47.4.6/1462
4003_9038	Channel (n) Value (FTM1_C5V)	32	R/W	0000_0000h	47.4.7/1465
4003_903C	Channel (n) Status And Control (FTM1_C6SC)	32	R/W	0000_0000h	47.4.6/1462
4003_9040	Channel (n) Value (FTM1_C6V)	32	R/W	0000_0000h	47.4.7/1465
4003_9044	Channel (n) Status And Control (FTM1_C7SC)	32	R/W	0000_0000h	47.4.6/1462
4003_9048	Channel (n) Value (FTM1_C7V)	32	R/W	0000_0000h	47.4.7/1465
4003_904C	Counter Initial Value (FTM1_CNTIN)	32	R/W	0000_0000h	47.4.8/1465
4003_9050	Capture And Compare Status (FTM1_STATUS)	32	R/W	0000_0000h	47.4.9/1466
4003_9054	Features Mode Selection (FTM1_MODE)	32	R/W	0000_0004h	47.4.10/ 1468
4003_9058	Synchronization (FTM1_SYNC)	32	R/W	0000_0000h	47.4.11/ 1470
4003_905C	Initial State For Channels Output (FTM1_OUTINIT)	32	R/W	0000_0000h	47.4.12/ 1472
4003_9060	Output Mask (FTM1_OUTMASK)	32	R/W	0000_0000h	47.4.13/ 1473
4003_9064	Function For Linked Channels (FTM1_COMBINE)	32	R/W	0000_0000h	47.4.14/ 1475
4003_9068	Deadtime Insertion Control (FTM1_DEADTIME)	32	R/W	0000_0000h	47.4.15/ 1480
4003_906C	FTM External Trigger (FTM1_EXTTRIG)	32	R/W	0000_0000h	47.4.16/ 1481
4003_9070	Channels Polarity (FTM1_POL)	32	R/W	0000_0000h	47.4.17/ 1483
4003_9074	Fault Mode Status (FTM1_FMS)	32	R/W	0000_0000h	47.4.18/ 1485
4003_9078	Input Capture Filter Control (FTM1_FILTER)	32	R/W	0000_0000h	47.4.19/ 1487
4003_907C	Fault Control (FTM1_FLTCTRL)	32	R/W	0000_0000h	47.4.20/ 1488
4003_9080	Quadrature Decoder Control And Status (FTM1_QDCTRL)	32	R/W	0000_0000h	47.4.21/ 1491
4003_9084	Configuration (FTM1_CONF)	32	R/W	0000_0000h	47.4.22/ 1493

Table continues on the next page...

FTM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_9088	FTM Fault Input Polarity (FTM1_FLTPOL)	32	R/W	0000_0000h	47.4.23/ 1494
4003_908C	Synchronization Configuration (FTM1_SYNCONF)	32	R/W	0000_0000h	47.4.24/ 1495
4003_9090	FTM Inverting Control (FTM1_INVCTRL)	32	R/W	0000_0000h	47.4.25/ 1497
4003_9094	FTM Software Output Control (FTM1_SWOCTRL)	32	R/W	0000_0000h	47.4.26/ 1498
4003_9098	FTM PWM Load (FTM1_PWMLOAD)	32	R/W	0000_0000h	47.4.27/ 1501
4003_A000	Status And Control (FTM2_SC)	32	R/W	0000_0000h	47.4.3/1459
4003_A004	Counter (FTM2_CNT)	32	R/W	0000_0000h	47.4.4/1460
4003_A008	Modulo (FTM2_MOD)	32	R/W	0000_0000h	47.4.5/1461
4003_A00C	Channel (n) Status And Control (FTM2_C0SC)	32	R/W	0000_0000h	47.4.6/1462
4003_A010	Channel (n) Value (FTM2_C0V)	32	R/W	0000_0000h	47.4.7/1465
4003_A014	Channel (n) Status And Control (FTM2_C1SC)	32	R/W	0000_0000h	47.4.6/1462
4003_A018	Channel (n) Value (FTM2_C1V)	32	R/W	0000_0000h	47.4.7/1465
4003_A01C	Channel (n) Status And Control (FTM2_C2SC)	32	R/W	0000_0000h	47.4.6/1462
4003_A020	Channel (n) Value (FTM2_C2V)	32	R/W	0000_0000h	47.4.7/1465
4003_A024	Channel (n) Status And Control (FTM2_C3SC)	32	R/W	0000_0000h	47.4.6/1462
4003_A028	Channel (n) Value (FTM2_C3V)	32	R/W	0000_0000h	47.4.7/1465
4003_A02C	Channel (n) Status And Control (FTM2_C4SC)	32	R/W	0000_0000h	47.4.6/1462
4003_A030	Channel (n) Value (FTM2_C4V)	32	R/W	0000_0000h	47.4.7/1465
4003_A034	Channel (n) Status And Control (FTM2_C5SC)	32	R/W	0000_0000h	47.4.6/1462
4003_A038	Channel (n) Value (FTM2_C5V)	32	R/W	0000_0000h	47.4.7/1465
4003_A03C	Channel (n) Status And Control (FTM2_C6SC)	32	R/W	0000_0000h	47.4.6/1462
4003_A040	Channel (n) Value (FTM2_C6V)	32	R/W	0000_0000h	47.4.7/1465
4003_A044	Channel (n) Status And Control (FTM2_C7SC)	32	R/W	0000_0000h	47.4.6/1462
4003_A048	Channel (n) Value (FTM2_C7V)	32	R/W	0000_0000h	47.4.7/1465
4003_A04C	Counter Initial Value (FTM2_CNTIN)	32	R/W	0000_0000h	47.4.8/1465
4003_A050	Capture And Compare Status (FTM2_STATUS)	32	R/W	0000_0000h	47.4.9/1466
4003_A054	Features Mode Selection (FTM2_MODE)	32	R/W	0000_0004h	47.4.10/ 1468
4003_A058	Synchronization (FTM2_SYNC)	32	R/W	0000_0000h	47.4.11/ 1470
4003_A05C	Initial State For Channels Output (FTM2_OUTINIT)	32	R/W	0000_0000h	47.4.12/ 1472
4003_A060	Output Mask (FTM2_OUTMASK)	32	R/W	0000_0000h	47.4.13/ 1473
4003_A064	Function For Linked Channels (FTM2_COMBINE)	32	R/W	0000_0000h	47.4.14/ 1475

Table continues on the next page...

FTM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_A068	Deadtime Insertion Control (FTM2_DEADTIME)	32	R/W	0000_0000h	47.4.15/ 1480
4003_A06C	FTM External Trigger (FTM2_EXTTRIG)	32	R/W	0000_0000h	47.4.16/ 1481
4003_A070	Channels Polarity (FTM2_POL)	32	R/W	0000_0000h	47.4.17/ 1483
4003_A074	Fault Mode Status (FTM2_FMS)	32	R/W	0000_0000h	47.4.18/ 1485
4003_A078	Input Capture Filter Control (FTM2_FILTER)	32	R/W	0000_0000h	47.4.19/ 1487
4003_A07C	Fault Control (FTM2_FLTCTRL)	32	R/W	0000_0000h	47.4.20/ 1488
4003_A080	Quadrature Decoder Control And Status (FTM2_QDCTRL)	32	R/W	0000_0000h	47.4.21/ 1491
4003_A084	Configuration (FTM2_CONF)	32	R/W	0000_0000h	47.4.22/ 1493
4003_A088	FTM Fault Input Polarity (FTM2_FLTPOL)	32	R/W	0000_0000h	47.4.23/ 1494
4003_A08C	Synchronization Configuration (FTM2_SYNCONF)	32	R/W	0000_0000h	47.4.24/ 1495
4003_A090	FTM Inverting Control (FTM2_INVCTRL)	32	R/W	0000_0000h	47.4.25/ 1497
4003_A094	FTM Software Output Control (FTM2_SWOCTRL)	32	R/W	0000_0000h	47.4.26/ 1498
4003_A098	FTM PWM Load (FTM2_PWMLOAD)	32	R/W	0000_0000h	47.4.27/ 1501
400B_9000	Status And Control (FTM3_SC)	32	R/W	0000_0000h	47.4.3/1459
400B_9004	Counter (FTM3_CNT)	32	R/W	0000_0000h	47.4.4/1460
400B_9008	Modulo (FTM3_MOD)	32	R/W	0000_0000h	47.4.5/1461
400B_900C	Channel (n) Status And Control (FTM3_C0SC)	32	R/W	0000_0000h	47.4.6/1462
400B_9010	Channel (n) Value (FTM3_C0V)	32	R/W	0000_0000h	47.4.7/1465
400B_9014	Channel (n) Status And Control (FTM3_C1SC)	32	R/W	0000_0000h	47.4.6/1462
400B_9018	Channel (n) Value (FTM3_C1V)	32	R/W	0000_0000h	47.4.7/1465
400B_901C	Channel (n) Status And Control (FTM3_C2SC)	32	R/W	0000_0000h	47.4.6/1462
400B_9020	Channel (n) Value (FTM3_C2V)	32	R/W	0000_0000h	47.4.7/1465
400B_9024	Channel (n) Status And Control (FTM3_C3SC)	32	R/W	0000_0000h	47.4.6/1462
400B_9028	Channel (n) Value (FTM3_C3V)	32	R/W	0000_0000h	47.4.7/1465
400B_902C	Channel (n) Status And Control (FTM3_C4SC)	32	R/W	0000_0000h	47.4.6/1462
400B_9030	Channel (n) Value (FTM3_C4V)	32	R/W	0000_0000h	47.4.7/1465
400B_9034	Channel (n) Status And Control (FTM3_C5SC)	32	R/W	0000_0000h	47.4.6/1462
400B_9038	Channel (n) Value (FTM3_C5V)	32	R/W	0000_0000h	47.4.7/1465
400B_903C	Channel (n) Status And Control (FTM3_C6SC)	32	R/W	0000_0000h	47.4.6/1462

Table continues on the next page...

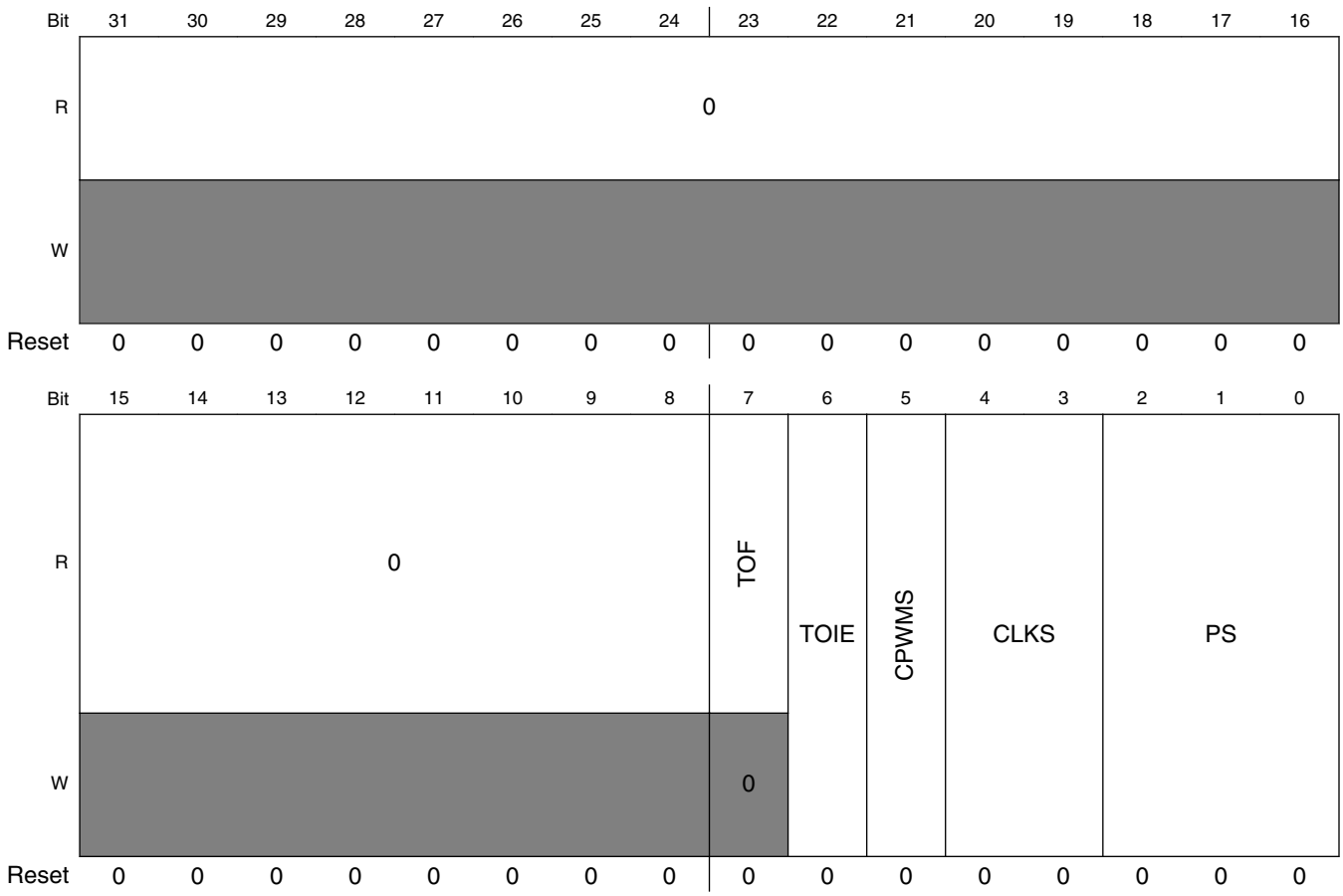
FTM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400B_9040	Channel (n) Value (FTM3_C6V)	32	R/W	0000_0000h	47.4.7/1465
400B_9044	Channel (n) Status And Control (FTM3_C7SC)	32	R/W	0000_0000h	47.4.6/1462
400B_9048	Channel (n) Value (FTM3_C7V)	32	R/W	0000_0000h	47.4.7/1465
400B_904C	Counter Initial Value (FTM3_CNTIN)	32	R/W	0000_0000h	47.4.8/1465
400B_9050	Capture And Compare Status (FTM3_STATUS)	32	R/W	0000_0000h	47.4.9/1466
400B_9054	Features Mode Selection (FTM3_MODE)	32	R/W	0000_0004h	47.4.10/ 1468
400B_9058	Synchronization (FTM3_SYNC)	32	R/W	0000_0000h	47.4.11/ 1470
400B_905C	Initial State For Channels Output (FTM3_OUTINIT)	32	R/W	0000_0000h	47.4.12/ 1472
400B_9060	Output Mask (FTM3_OUTMASK)	32	R/W	0000_0000h	47.4.13/ 1473
400B_9064	Function For Linked Channels (FTM3_COMBINE)	32	R/W	0000_0000h	47.4.14/ 1475
400B_9068	Deadtime Insertion Control (FTM3_DEADTIME)	32	R/W	0000_0000h	47.4.15/ 1480
400B_906C	FTM External Trigger (FTM3_EXTTRIG)	32	R/W	0000_0000h	47.4.16/ 1481
400B_9070	Channels Polarity (FTM3_POL)	32	R/W	0000_0000h	47.4.17/ 1483
400B_9074	Fault Mode Status (FTM3_FMS)	32	R/W	0000_0000h	47.4.18/ 1485
400B_9078	Input Capture Filter Control (FTM3_FILTER)	32	R/W	0000_0000h	47.4.19/ 1487
400B_907C	Fault Control (FTM3_FLTCTRL)	32	R/W	0000_0000h	47.4.20/ 1488
400B_9080	Quadrature Decoder Control And Status (FTM3_QDCTRL)	32	R/W	0000_0000h	47.4.21/ 1491
400B_9084	Configuration (FTM3_CONF)	32	R/W	0000_0000h	47.4.22/ 1493
400B_9088	FTM Fault Input Polarity (FTM3_FLTPOL)	32	R/W	0000_0000h	47.4.23/ 1494
400B_908C	Synchronization Configuration (FTM3_SYNCONF)	32	R/W	0000_0000h	47.4.24/ 1495
400B_9090	FTM Inverting Control (FTM3_INVCTRL)	32	R/W	0000_0000h	47.4.25/ 1497
400B_9094	FTM Software Output Control (FTM3_SWOCTRL)	32	R/W	0000_0000h	47.4.26/ 1498
400B_9098	FTM PWM Load (FTM3_PWMLOAD)	32	R/W	0000_0000h	47.4.27/ 1501

47.4.3 Status And Control (FTMx_SC)

SC contains the overflow status flag and control bits used to configure the interrupt enable, FTM configuration, clock source, and prescaler factor. These controls relate to all channels within this module.

Address: Base address + 0h offset



FTMx_SC field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 TOF	Timer Overflow Flag Set by hardware when the FTM counter passes the value in the MOD register. The TOF bit is cleared by reading the SC register while TOF is set and then writing a 0 to TOF bit. Writing a 1 to TOF has no effect. If another FTM overflow occurs between the read and write operations, the write operation has no effect; therefore, TOF remains set indicating an overflow has occurred. In this case, a TOF interrupt request is not lost due to the clearing sequence for a previous TOF. 0 FTM counter has not overflowed. 1 FTM counter has overflowed.

Table continues on the next page...

FTMx_SC field descriptions (continued)

Field	Description
6 TOIE	Timer Overflow Interrupt Enable Enables FTM overflow interrupts. 0 Disable TOF interrupts. Use software polling. 1 Enable TOF interrupts. An interrupt is generated when TOF equals one.
5 CPWMS	Center-Aligned PWM Select Selects CPWM mode. This mode configures the FTM to operate in Up-Down Counting mode. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 FTM counter operates in Up Counting mode. 1 FTM counter operates in Up-Down Counting mode.
4–3 CLKS	Clock Source Selection Selects FTM counter clock sources. This field is write protected. It can be written only when MODE[WPDIS] = 1. 00 No clock selected. This in effect disables the FTM counter. 01 System clock 10 Fixed frequency clock 11 External clock
PS	Prescale Factor Selection Selects one of 8 division factors for the clock source selected by CLKS. The new prescaler factor affects the clock source on the next system clock cycle after the new value is updated into the register bits. This field is write protected. It can be written only when MODE[WPDIS] = 1. 000 Divide by 1 001 Divide by 2 010 Divide by 4 011 Divide by 8 100 Divide by 16 101 Divide by 32 110 Divide by 64 111 Divide by 128

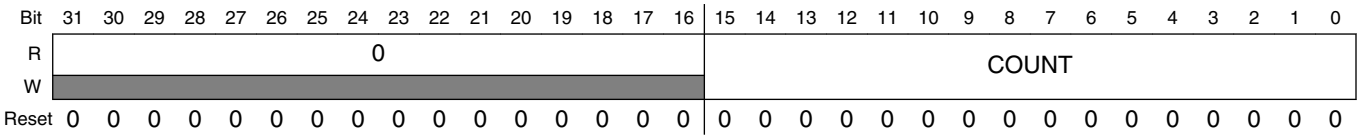
47.4.4 Counter (FTMx_CNT)

The CNT register contains the FTM counter value.

Reset clears the CNT register. Writing any value to COUNT updates the counter with its initial value, CNTIN.

When BDM is active, the FTM counter is frozen. This is the value that you may read.

Address: Base address + 4h offset



FTMx_CNT field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
COUNT	Counter Value

47.4.5 Modulo (FTMx_MOD)

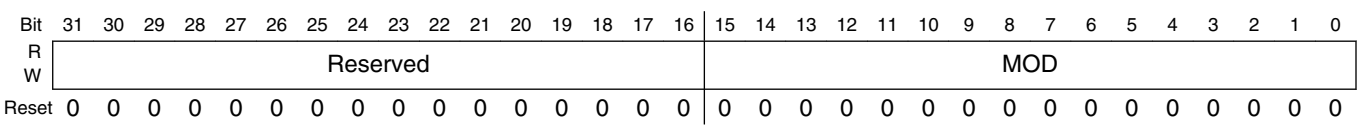
The Modulo register contains the modulo value for the FTM counter. After the FTM counter reaches the modulo value, the overflow flag (TOF) becomes set at the next clock, and the next value of FTM counter depends on the selected counting method; see Counter.

Writing to the MOD register latches the value into a buffer. The MOD register is updated with the value of its write buffer according to Registers updated from write buffers.

If FTMEN = 0, this write coherency mechanism may be manually reset by writing to the SC register whether BDM is active or not.

Initialize the FTM counter, by writing to CNT, before writing to the MOD register to avoid confusion about when the first counter overflow will occur.

Address: Base address + 8h offset



FTMx_MOD field descriptions

Field	Description
31–16 Reserved	This field is reserved.
MOD	Modulo Value

47.4.6 Channel (n) Status And Control (FTMx_C*n*SC)

CnSC contains the channel-interrupt-status flag and control bits used to configure the interrupt enable, channel configuration, and pin function.

Table 47-3. Mode, edge, and level selection

DECAPEN	COMBINE	CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
X	X	X	XX	00	Pin not used for FTM—revert the channel pin to general purpose I/O or other peripheral control	
0	0	0	00	01	Input Capture	Capture on Rising Edge Only
				10		Capture on Falling Edge Only
				11		Capture on Rising or Falling Edge
			01	01	Output Compare	Toggle Output on match
				10		Clear Output on match
				11		Set Output on match
			1X	10	Edge-Aligned PWM	High-true pulses (clear Output on match)
				X1		Low-true pulses (set Output on match)
		1	XX	10	Center-Aligned PWM	High-true pulses (clear Output on match-up)
				X1		Low-true pulses (set Output on match-up)
	1	0	XX	10	Combine PWM	High-true pulses (set on channel (n) match, and clear on channel (n+1) match)
				X1		Low-true pulses (clear on channel (n) match, and set on channel (n +1) match)

Table continues on the next page...

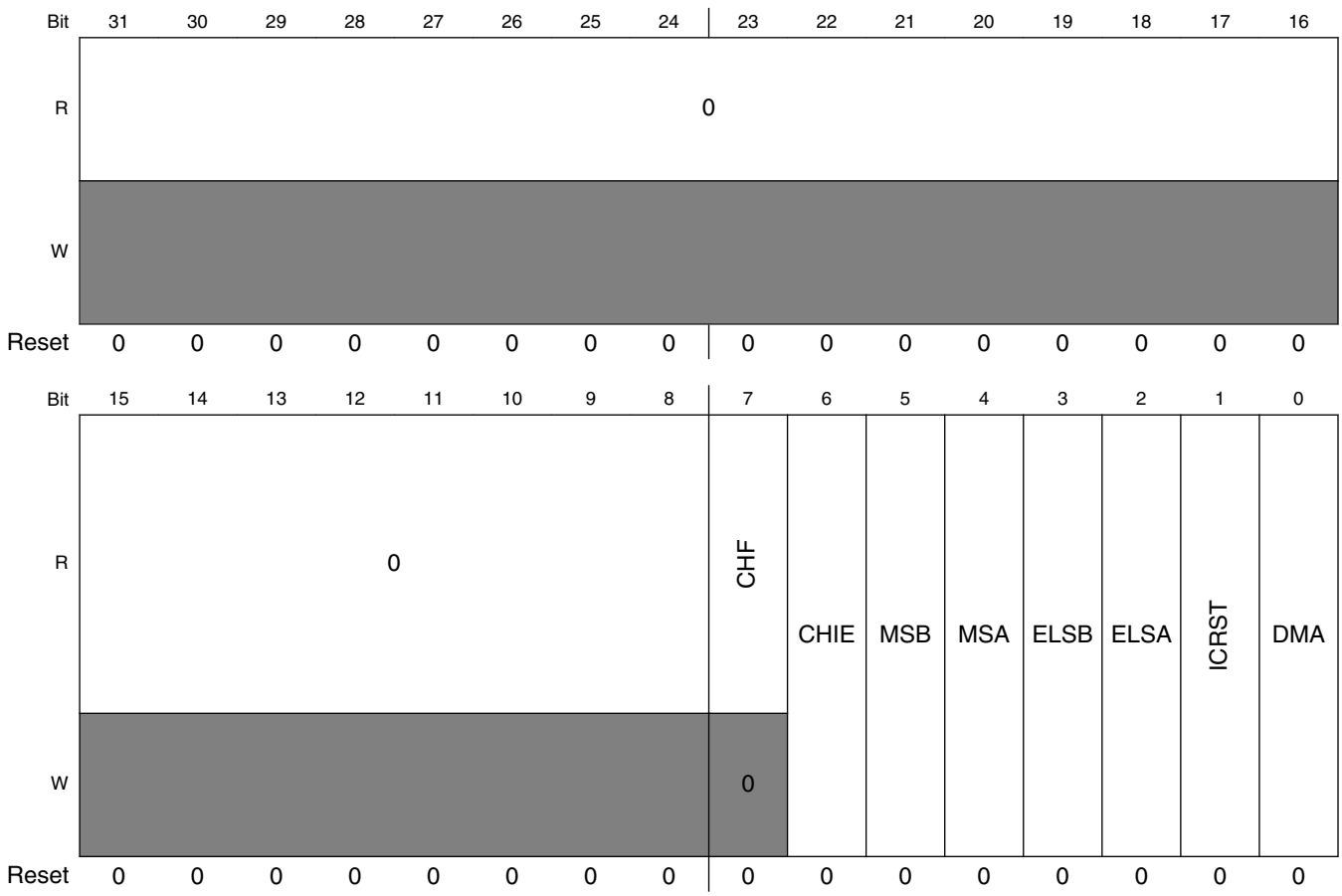
Table 47-3. Mode, edge, and level selection (continued)

DECAPEN	COMBINE	CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
1	0	0	X0	See the following table (Table 47-4).	Dual Edge Capture	One-Shot Capture mode
			X1			Continuous Capture mode

Table 47-4. Dual Edge Capture mode — edge polarity selection

ELSnB	ELSnA	Channel Port Enable	Detected Edges
0	0	Disabled	No edge
0	1	Enabled	Rising edge
1	0	Enabled	Falling edge
1	1	Enabled	Rising and falling edges

Address: Base address + Ch offset + (8d × i), where i=0d to 7d



FTMx_C*n*SC field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 CHF	Channel Flag Set by hardware when an event occurs on the channel. CHF is cleared by reading the CSC register while CHnF is set and then writing a 0 to the CHF bit. Writing a 1 to CHF has no effect. If another event occurs between the read and write operations, the write operation has no effect; therefore, CHF remains set indicating an event has occurred. In this case a CHF interrupt request is not lost due to the clearing sequence for a previous CHF. 0 No channel event has occurred. 1 A channel event has occurred.
6 CHIE	Channel Interrupt Enable Enables channel interrupts. 0 Disable channel interrupts. Use software polling. 1 Enable channel interrupts.
5 MSB	Channel Mode Select Used for further selections in the channel logic. Its functionality is dependent on the channel mode. See Table 47-3 . This field is write protected. It can be written only when MODE[WPDIS] = 1.
4 MSA	Channel Mode Select Used for further selections in the channel logic. Its functionality is dependent on the channel mode. See Table 47-3 . This field is write protected. It can be written only when MODE[WPDIS] = 1.
3 ELSB	Edge or Level Select The functionality of ELSB and ELSA depends on the channel mode. See Table 47-3 . This field is write protected. It can be written only when MODE[WPDIS] = 1.
2 ELSA	Edge or Level Select The functionality of ELSB and ELSA depends on the channel mode. See Table 47-3 . This field is write protected. It can be written only when MODE[WPDIS] = 1.
1 ICRST	FTM counter reset by the selected input capture event. FTM counter reset is driven by the selected event of the channel (n) in the Input Capture mode. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 FTM counter is not reset when the selected channel (n) input event is detected. 1 FTM counter is reset when the selected channel (n) input event is detected.
0 DMA	DMA Enable Enables DMA transfers for the channel. 0 Disable DMA transfers. 1 Enable DMA transfers.

47.4.7 Channel (n) Value (FTMx_CnV)

These registers contain the captured FTM counter value for the input modes or the match value for the output modes.

In Input Capture, Capture Test, and Dual Edge Capture modes, any write to a CnV register is ignored.

In output modes, writing to a CnV register latches the value into a buffer. A CnV register is updated with the value of its write buffer according to Registers updated from write buffers.

If FTMEN = 0, this write coherency mechanism may be manually reset by writing to the CnSC register whether BDM mode is active or not.

Address: Base address + 10h offset + (8d × i), where i=0d to 7d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																VAL															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FTMx_CnV field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
VAL	Channel Value Captured FTM counter value of the input modes or the match value for the output modes

47.4.8 Counter Initial Value (FTMx_CNTIN)

The Counter Initial Value register contains the initial value for the FTM counter.

Writing to the CNTIN register latches the value into a buffer. The CNTIN register is updated with the value of its write buffer according to Registers updated from write buffers.

When the FTM clock is initially selected, by writing a non-zero value to the CLKS bits, the FTM counter starts with the value 0x0000. To avoid this behavior, before the first write to select the FTM clock, write the new value to the the CNTIN register and then initialize the FTM counter by writing any value to the CNT register.

Address: Base address + 4Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved																INIT															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FTMx_CNTIN field descriptions

Field	Description
31–16 Reserved	This field is reserved.
INIT	Initial Value Of The FTM Counter

47.4.9 Capture And Compare Status (FTMx_STATUS)

The STATUS register contains a copy of the status flag CHnF bit in CnSC for each FTM channel for software convenience.

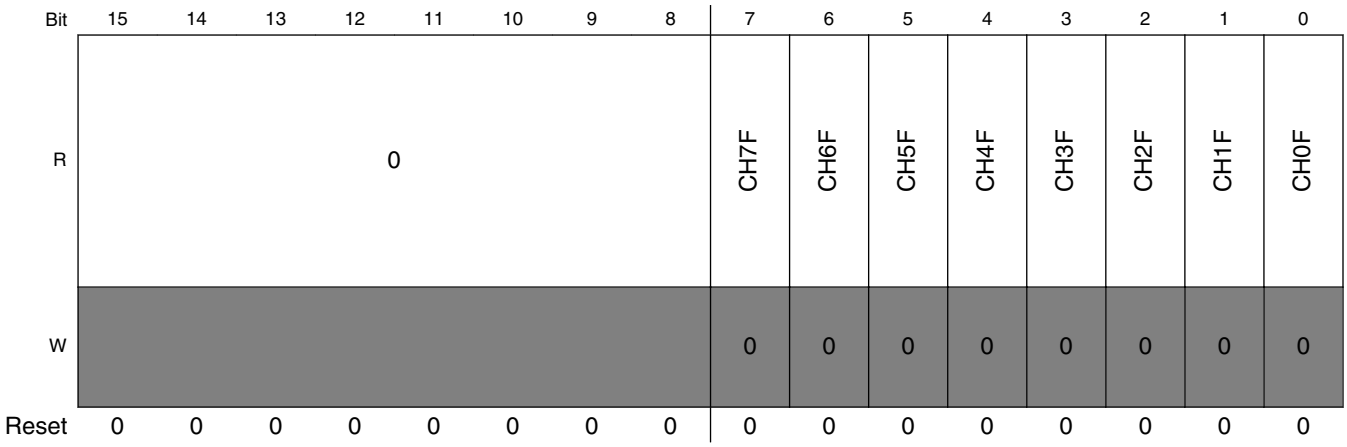
Each CHnF bit in STATUS is a mirror of CHnF bit in CnSC. All CHnF bits can be checked using only one read of STATUS. All CHnF bits can be cleared by reading STATUS followed by writing 0x00 to STATUS.

Hardware sets the individual channel flags when an event occurs on the channel. CHnF is cleared by reading STATUS while CHnF is set and then writing a 0 to the CHnF bit. Writing a 1 to CHnF has no effect.

If another event occurs between the read and write operations, the write operation has no effect; therefore, CHnF remains set indicating an event has occurred. In this case, a CHnF interrupt request is not lost due to the clearing sequence for a previous CHnF.

Address: Base address + 50h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



FTMx_STATUS field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 CH7F	Channel 7 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
6 CH6F	Channel 6 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
5 CH5F	Channel 5 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
4 CH4F	Channel 4 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
3 CH3F	Channel 3 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
2 CH2F	Channel 2 Flag See the register description.

Table continues on the next page...

FTMx_STATUS field descriptions (continued)

Field	Description
	0 No channel event has occurred. 1 A channel event has occurred.
1 CH1F	Channel 1 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
0 CH0F	Channel 0 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.

47.4.10 Features Mode Selection (FTMx_MODE)

This register contains the global enable bit for FTM-specific features and the control bits used to configure:

- Fault control mode and interrupt
- Capture Test mode
- PWM synchronization
- Write protection
- Channel output initialization

These controls relate to all channels within this module.

Address: Base address + 54h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								FAULTIE	FAULTM		CAPTEST	PWMSYNC	WPDIS	INIT	FTMEN
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

FTMx_MODE field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 FAULTIE	Fault Interrupt Enable Enables the generation of an interrupt when a fault is detected by FTM and the FTM fault control is enabled. 0 Fault control interrupt is disabled. 1 Fault control interrupt is enabled.
6–5 FAULTM	Fault Control Mode Defines the FTM fault control mode. This field is write protected. It can be written only when MODE[WPDIS] = 1. 00 Fault control is disabled for all channels. 01 Fault control is enabled for even channels only (channels 0, 2, 4, and 6), and the selected mode is the manual fault clearing. 10 Fault control is enabled for all channels, and the selected mode is the manual fault clearing. 11 Fault control is enabled for all channels, and the selected mode is the automatic fault clearing.
4 CAPTEST	Capture Test Mode Enable Enables the capture test mode. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Capture test mode is disabled. 1 Capture test mode is enabled.
3 PWMSYNC	PWM Synchronization Mode Selects which triggers can be used by MOD, CnV, OUTMASK, and FTM counter synchronization. See PWM synchronization. The PWMSYNC bit configures the synchronization when SYNCMODE is 0. 0 No restrictions. Software and hardware triggers can be used by MOD, CnV, OUTMASK, and FTM counter synchronization. 1 Software trigger can only be used by MOD and CnV synchronization, and hardware triggers can only be used by OUTMASK and FTM counter synchronization.
2 WPDIS	Write Protection Disable When write protection is enabled (WPDIS = 0), write protected bits cannot be written. When write protection is disabled (WPDIS = 1), write protected bits can be written. The WPDIS bit is the negation of the WPEN bit. WPDIS is cleared when 1 is written to WPEN. WPDIS is set when WPEN bit is read as a 1 and then 1 is written to WPDIS. Writing 0 to WPDIS has no effect. 0 Write protection is enabled. 1 Write protection is disabled.
1 INIT	Initialize The Channels Output When a 1 is written to INIT bit the channels output is initialized according to the state of their corresponding bit in the OUTINIT register. Writing a 0 to INIT bit has no effect. The INIT bit is always read as 0.
0 FTMEN	FTM Enable This field is write protected. It can be written only when MODE[WPDIS] = 1.

Table continues on the next page...

FTMx_MODE field descriptions (continued)

Field	Description
	0 TPM compatibility. Free running counter and synchronization compatible with TPM. 1 Free running counter and synchronization are different from TPM behavior.

47.4.11 Synchronization (FTMx_SYNC)

This register configures the PWM synchronization.

A synchronization event can perform the synchronized update of MOD, CV, and OUTMASK registers with the value of their write buffer and the FTM counter initialization.

NOTE

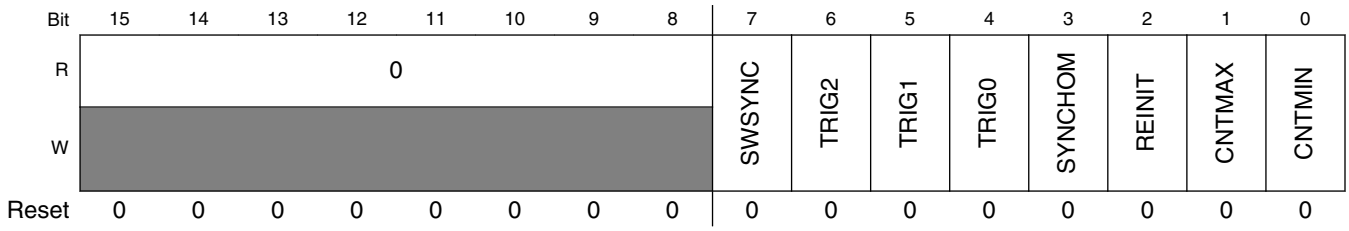
The software trigger, SWSYNC bit, and hardware triggers TRIG0, TRIG1, and TRIG2 bits have a potential conflict if used together when SYNCMODE = 0. Use only hardware or software triggers but not both at the same time, otherwise unpredictable behavior is likely to happen.

The selection of the loading point, CNTMAX and CNTMIN bits, is intended to provide the update of MOD, CNTIN, and CnV registers across all enabled channels simultaneously. The use of the loading point selection together with SYNCMODE = 0 and hardware trigger selection, TRIG0, TRIG1, or TRIG2 bits, is likely to result in unpredictable behavior.

The synchronization event selection also depends on the PWMSYNC (MODE register) and SYNCMODE (SYNCONF register) bits. See PWM synchronization.

Address: Base address + 58h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



FTMx_SYNC field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 SWSYNC	PWM Synchronization Software Trigger Selects the software trigger as the PWM synchronization trigger. The software trigger happens when a 1 is written to SWSYNC bit. 0 Software trigger is not selected. 1 Software trigger is selected.
6 TRIG2	PWM Synchronization Hardware Trigger 2 Enables hardware trigger 2 to the PWM synchronization. Hardware trigger 2 happens when a rising edge is detected at the trigger 2 input signal. 0 Trigger is disabled. 1 Trigger is enabled.
5 TRIG1	PWM Synchronization Hardware Trigger 1 Enables hardware trigger 1 to the PWM synchronization. Hardware trigger 1 happens when a rising edge is detected at the trigger 1 input signal. 0 Trigger is disabled. 1 Trigger is enabled.
4 TRIG0	PWM Synchronization Hardware Trigger 0 Enables hardware trigger 0 to the PWM synchronization. Hardware trigger 0 occurs when a rising edge is detected at the trigger 0 input signal. 0 Trigger is disabled. 1 Trigger is enabled.
3 SYNCHOM	Output Mask Synchronization Selects when the OUTMASK register is updated with the value of its buffer. 0 OUTMASK register is updated with the value of its buffer in all rising edges of the system clock. 1 OUTMASK register is updated with the value of its buffer only by the PWM synchronization.
2 REINIT	FTM Counter Reinitialization By Synchronization (FTM counter synchronization) Determines if the FTM counter is reinitialized when the selected trigger for the synchronization is detected. The REINIT bit configures the synchronization when SYNCMODE is zero. 0 FTM counter continues to count normally. 1 FTM counter is updated with its initial value when the selected trigger is detected.

Table continues on the next page...

FTMx_SYNC field descriptions (continued)

Field	Description
1 CNTMAX	Maximum Loading Point Enable Selects the maximum loading point to PWM synchronization. See Boundary cycle and loading points. If CNTMAX is 1, the selected loading point is when the FTM counter reaches its maximum value (MOD register). 0 The maximum loading point is disabled. 1 The maximum loading point is enabled.
0 CNTMIN	Minimum Loading Point Enable Selects the minimum loading point to PWM synchronization. See Boundary cycle and loading points. If CNTMIN is one, the selected loading point is when the FTM counter reaches its minimum value (CNTIN register). 0 The minimum loading point is disabled. 1 The minimum loading point is enabled.

47.4.12 Initial State For Channels Output (FTMx_OUTINIT)

Address: Base address + 5Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								CH7OI	CH6OI	CH5OI	CH4OI	CH3OI	CH2OI	CH1OI	CH0OI
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FTMx_OUTINIT field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 CH7OI	Channel 7 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
6 CH6OI	Channel 6 Output Initialization Value

Table continues on the next page...

FTMx_OUTINIT field descriptions (continued)

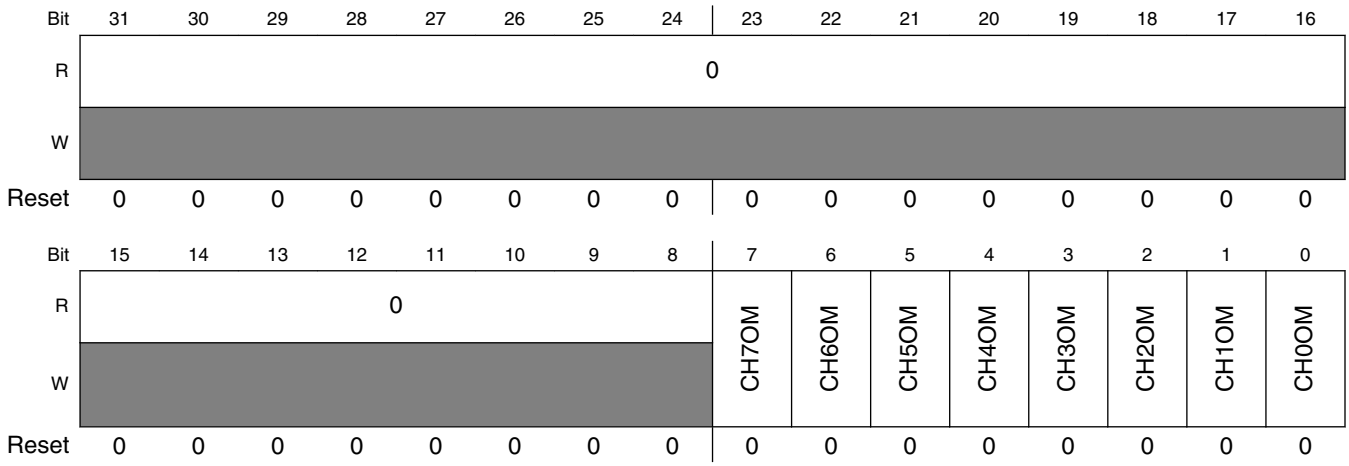
Field	Description
	Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
5 CH5OI	Channel 5 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
4 CH4OI	Channel 4 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
3 CH3OI	Channel 3 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
2 CH2OI	Channel 2 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
1 CH1OI	Channel 1 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
0 CH0OI	Channel 0 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.

47.4.13 Output Mask (FTMx_OUTMASK)

This register provides a mask for each FTM channel. The mask of a channel determines if its output responds, that is, it is masked or not, when a match occurs. This feature is used for BLDC control where the PWM signal is presented to an electric motor at specific times to provide electronic commutation.

Any write to the OUTMASK register, stores the value in its write buffer. The register is updated with the value of its write buffer according to PWM synchronization.

Address: Base address + 60h offset



FTMx_OUTMASK field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 CH7OM	Channel 7 Output Mask Defines if the channel output is masked or unmasked. 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
6 CH6OM	Channel 6 Output Mask Defines if the channel output is masked or unmasked. 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
5 CH5OM	Channel 5 Output Mask Defines if the channel output is masked or unmasked. 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
4 CH4OM	Channel 4 Output Mask Defines if the channel output is masked or unmasked. 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
3 CH3OM	Channel 3 Output Mask Defines if the channel output is masked or unmasked.

Table continues on the next page...

FTMx_OUTMASK field descriptions (continued)

Field	Description
	0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
2 CH2OM	Channel 2 Output Mask Defines if the channel output is masked or unmasked. 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
1 CH1OM	Channel 1 Output Mask Defines if the channel output is masked or unmasked. 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
0 CH0OM	Channel 0 Output Mask Defines if the channel output is masked or unmasked. 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.

47.4.14 Function For Linked Channels (FTMx_COMBINE)

This register contains the control bits used to configure the fault control, synchronization, deadtime insertion, Dual Edge Capture mode, Complementary, and Combine mode for each pair of channels (n) and (n+1), where n equals 0, 2, 4, and 6.

Address: Base address + 64h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	FAULTEN3	SYNCEN3	DTEN3	DECAP3	DECAPEN3	COMP3	COMBINE3	0	FAULTEN2	SYNCEN2	DTEN2	DECAP2	DECAPEN2	COMP2	COMBINE2
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	FAULTEN1	SYNCEN1	DTEN1	DECAP1	DECAPEN1	COMP1	COMBINE1	0	FAULTEN0	SYNCEN0	DTEN0	DECAP0	DECAPEN0	COMP0	COMBINE0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FTMx_COMBINE field descriptions

Field	Description
31 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
30 FAULTEN3	Fault Control Enable For n = 6 Enables the fault control in channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The fault control in this pair of channels is disabled. 1 The fault control in this pair of channels is enabled.
29 SYNCEN3	Synchronization Enable For n = 6 Enables PWM synchronization of registers C(n)V and C(n+1)V. 0 The PWM synchronization in this pair of channels is disabled. 1 The PWM synchronization in this pair of channels is enabled.
28 DTEN3	Deadtime Enable For n = 6 Enables the deadtime insertion in the channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The deadtime insertion in this pair of channels is disabled. 1 The deadtime insertion in this pair of channels is enabled.
27 DECAP3	Dual Edge Capture Mode Captures For n = 6 Enables the capture of the FTM counter value according to the channel (n) input event and the configuration of the dual edge capture bits. This field applies only when DECAPEN = 1. DECAP bit is cleared automatically by hardware if dual edge capture – one-shot mode is selected and when the capture of channel (n+1) event is made. 0 The dual edge captures are inactive. 1 The dual edge captures are active.
26 DECAPEN3	Dual Edge Capture Mode Enable For n = 6 Enables the Dual Edge Capture mode in the channels (n) and (n+1). This bit reconfigures the function of MSnA, ELSnB:ELSnA and ELS(n+1)B:ELS(n+1)A bits in Dual Edge Capture mode according to Table 47-3. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The Dual Edge Capture mode in this pair of channels is disabled. 1 The Dual Edge Capture mode in this pair of channels is enabled.
25 COMP3	Complement Of Channel (n) for n = 6 Enables Complementary mode for the combined channels. In Complementary mode the channel (n+1) output is the inverse of the channel (n) output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel (n+1) output is the same as the channel (n) output. 1 The channel (n+1) output is the complement of the channel (n) output.

Table continues on the next page...

FTMx_COMBINE field descriptions (continued)

Field	Description
24 COMBINE3	Combine Channels For n = 6 Enables the combine feature for channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Channels (n) and (n+1) are independent. 1 Channels (n) and (n+1) are combined.
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 FAULTEN2	Fault Control Enable For n = 4 Enables the fault control in channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The fault control in this pair of channels is disabled. 1 The fault control in this pair of channels is enabled.
21 SYNCEN2	Synchronization Enable For n = 4 Enables PWM synchronization of registers C(n)V and C(n+1)V. 0 The PWM synchronization in this pair of channels is disabled. 1 The PWM synchronization in this pair of channels is enabled.
20 DTEN2	Deadtime Enable For n = 4 Enables the deadtime insertion in the channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The deadtime insertion in this pair of channels is disabled. 1 The deadtime insertion in this pair of channels is enabled.
19 DECAP2	Dual Edge Capture Mode Captures For n = 4 Enables the capture of the FTM counter value according to the channel (n) input event and the configuration of the dual edge capture bits. This field applies only when DECAPEN = 1. DECAP bit is cleared automatically by hardware if dual edge capture – one-shot mode is selected and when the capture of channel (n+1) event is made. 0 The dual edge captures are inactive. 1 The dual edge captures are active.
18 DECAPEN2	Dual Edge Capture Mode Enable For n = 4 Enables the Dual Edge Capture mode in the channels (n) and (n+1). This bit reconfigures the function of MSnA, ELSnB:ELSnA and ELS(n+1)B:ELS(n+1)A bits in Dual Edge Capture mode according to Table 47-3. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The Dual Edge Capture mode in this pair of channels is disabled. 1 The Dual Edge Capture mode in this pair of channels is enabled.
17 COMP2	Complement Of Channel (n) For n = 4

Table continues on the next page...

FTMx_COMBINE field descriptions (continued)

Field	Description
	Enables Complementary mode for the combined channels. In Complementary mode the channel (n+1) output is the inverse of the channel (n) output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel (n+1) output is the same as the channel (n) output. 1 The channel (n+1) output is the complement of the channel (n) output.
16 COMBINE2	Combine Channels For n = 4 Enables the combine feature for channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Channels (n) and (n+1) are independent. 1 Channels (n) and (n+1) are combined.
15 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
14 FAULTEN1	Fault Control Enable For n = 2 Enables the fault control in channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The fault control in this pair of channels is disabled. 1 The fault control in this pair of channels is enabled.
13 SYNCEN1	Synchronization Enable For n = 2 Enables PWM synchronization of registers C(n)V and C(n+1)V. 0 The PWM synchronization in this pair of channels is disabled. 1 The PWM synchronization in this pair of channels is enabled.
12 DTEN1	Deadtime Enable For n = 2 Enables the deadtime insertion in the channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The deadtime insertion in this pair of channels is disabled. 1 The deadtime insertion in this pair of channels is enabled.
11 DECAP1	Dual Edge Capture Mode Captures For n = 2 Enables the capture of the FTM counter value according to the channel (n) input event and the configuration of the dual edge capture bits. This field applies only when DECAPEN = 1. DECAP bit is cleared automatically by hardware if Dual Edge Capture – One-Shot mode is selected and when the capture of channel (n+1) event is made. 0 The dual edge captures are inactive. 1 The dual edge captures are active.
10 DECAPEN1	Dual Edge Capture Mode Enable For n = 2 Enables the Dual Edge Capture mode in the channels (n) and (n+1). This bit reconfigures the function of MSnA, ELSnB:ELSnA and ELS(n+1)B:ELS(n+1)A bits in Dual Edge Capture mode according to Table 47-3.

Table continues on the next page...

FTMx_COMBINE field descriptions (continued)

Field	Description
	This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The Dual Edge Capture mode in this pair of channels is disabled. 1 The Dual Edge Capture mode in this pair of channels is enabled.
9 COMP1	Complement Of Channel (n) For n = 2 Enables Complementary mode for the combined channels. In Complementary mode the channel (n+1) output is the inverse of the channel (n) output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel (n+1) output is the same as the channel (n) output. 1 The channel (n+1) output is the complement of the channel (n) output.
8 COMBINE1	Combine Channels For n = 2 Enables the combine feature for channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Channels (n) and (n+1) are independent. 1 Channels (n) and (n+1) are combined.
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 FAULTEN0	Fault Control Enable For n = 0 Enables the fault control in channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The fault control in this pair of channels is disabled. 1 The fault control in this pair of channels is enabled.
5 SYNCEN0	Synchronization Enable For n = 0 Enables PWM synchronization of registers C(n)V and C(n+1)V. 0 The PWM synchronization in this pair of channels is disabled. 1 The PWM synchronization in this pair of channels is enabled.
4 DTEN0	Deadtime Enable For n = 0 Enables the deadtime insertion in the channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The deadtime insertion in this pair of channels is disabled. 1 The deadtime insertion in this pair of channels is enabled.
3 DECAP0	Dual Edge Capture Mode Captures For n = 0 Enables the capture of the FTM counter value according to the channel (n) input event and the configuration of the dual edge capture bits. This field applies only when DECAPEN = 1. DECAP bit is cleared automatically by hardware if dual edge capture – one-shot mode is selected and when the capture of channel (n+1) event is made. 0 The dual edge captures are inactive. 1 The dual edge captures are active.

Table continues on the next page...

FTMx_COMBINE field descriptions (continued)

Field	Description
2 DECAPEN0	Dual Edge Capture Mode Enable For n = 0 Enables the Dual Edge Capture mode in the channels (n) and (n+1). This bit reconfigures the function of MSnA, ELSnB:ELSnA and ELS(n+1)B:ELS(n+1)A bits in Dual Edge Capture mode according to Table 47-3. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The Dual Edge Capture mode in this pair of channels is disabled. 1 The Dual Edge Capture mode in this pair of channels is enabled.
1 COMP0	Complement Of Channel (n) For n = 0 Enables Complementary mode for the combined channels. In Complementary mode the channel (n+1) output is the inverse of the channel (n) output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel (n+1) output is the same as the channel (n) output. 1 The channel (n+1) output is the complement of the channel (n) output.
0 COMBINE0	Combine Channels For n = 0 Enables the combine feature for channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Channels (n) and (n+1) are independent. 1 Channels (n) and (n+1) are combined.

47.4.15 Deadtime Insertion Control (FTMx_DEADTIME)

This register selects the deadtime prescaler factor and deadtime value. All FTM channels use this clock prescaler and this deadtime value for the deadtime insertion.

Address: Base address + 68h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																								DTPS		DTVAL					
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FTMx_DEADTIME field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7–6 DTPS	Deadtime Prescaler Value Selects the division factor of the system clock. This prescaled clock is used by the deadtime counter. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0x Divide the system clock by 1.

Table continues on the next page...

FTMx_DEADTIME field descriptions (continued)

Field	Description
	10 Divide the system clock by 4. 11 Divide the system clock by 16.
DTVAL	Deadtime Value Selects the deadtime insertion value for the deadtime counter. The deadtime counter is clocked by a scaled version of the system clock. See the description of DTPS. Deadtime insert value = (DTPS × DTVAL). DTVAL selects the number of deadtime counts inserted as follows: When DTVAL is 0, no counts are inserted. When DTVAL is 1, 1 count is inserted. When DTVAL is 2, 2 counts are inserted. This pattern continues up to a possible 63 counts. This field is write protected. It can be written only when MODE[WPDIS] = 1.

47.4.16 FTM External Trigger (FTMx_EXTTRIG)

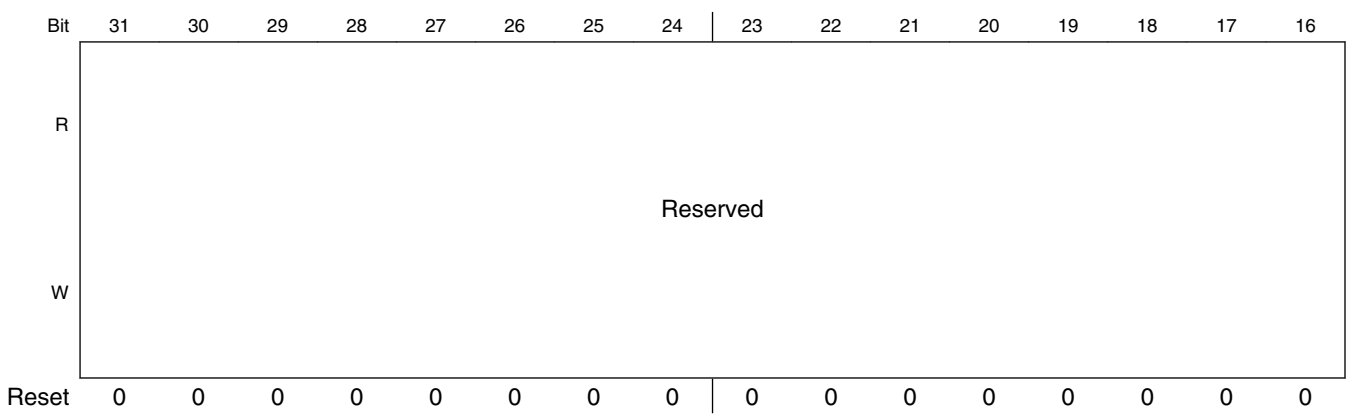
This register:

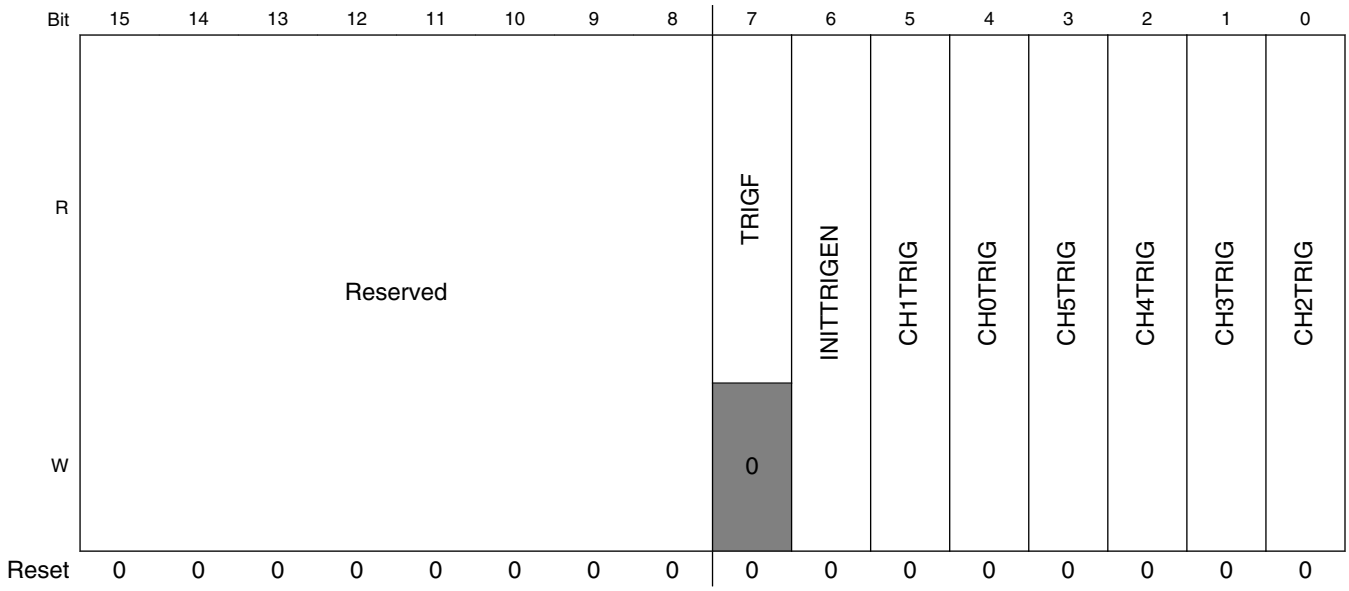
- Indicates when a channel trigger was generated
- Enables the generation of a trigger when the FTM counter is equal to its initial value
- Selects which channels are used in the generation of the channel triggers

Several channels can be selected to generate multiple triggers in one PWM period. See Channel trigger output and Initialization trigger.

Channels 6 and 7 are not used to generate channel triggers.

Address: Base address + 6Ch offset





FTMx_EXTTRIG field descriptions

Field	Description
31–8 Reserved	This field is reserved.
7 TRIGF	Channel Trigger Flag Set by hardware when a channel trigger is generated. Clear TRIGF by reading EXTTRIG while TRIGF is set and then writing a 0 to TRIGF. Writing a 1 to TRIGF has no effect. If another channel trigger is generated before the clearing sequence is completed, the sequence is reset so TRIGF remains set after the clear sequence is completed for the earlier TRIGF. 0 No channel trigger was generated. 1 A channel trigger was generated.
6 INITTRIGEN	Initialization Trigger Enable Enables the generation of the trigger when the FTM counter is equal to the CNTIN register. 0 The generation of initialization trigger is disabled. 1 The generation of initialization trigger is enabled.
5 CH1TRIG	Channel 1 Trigger Enable Enables the generation of the channel trigger when the FTM counter is equal to the CnV register. 0 The generation of the channel trigger is disabled. 1 The generation of the channel trigger is enabled.
4 CH0TRIG	Channel 0 Trigger Enable Enables the generation of the channel trigger when the FTM counter is equal to the CnV register. 0 The generation of the channel trigger is disabled. 1 The generation of the channel trigger is enabled.
3 CH5TRIG	Channel 5 Trigger Enable

Table continues on the next page...

FTMx_EXTTRIG field descriptions (continued)

Field	Description
	Enables the generation of the channel trigger when the FTM counter is equal to the CnV register. 0 The generation of the channel trigger is disabled. 1 The generation of the channel trigger is enabled.
2 CH4TRIG	Channel 4 Trigger Enable Enables the generation of the channel trigger when the FTM counter is equal to the CnV register. 0 The generation of the channel trigger is disabled. 1 The generation of the channel trigger is enabled.
1 CH3TRIG	Channel 3 Trigger Enable Enables the generation of the channel trigger when the FTM counter is equal to the CnV register. 0 The generation of the channel trigger is disabled. 1 The generation of the channel trigger is enabled.
0 CH2TRIG	Channel 2 Trigger Enable Enables the generation of the channel trigger when the FTM counter is equal to the CnV register. 0 The generation of the channel trigger is disabled. 1 The generation of the channel trigger is enabled.

47.4.17 Channels Polarity (FTMx_POL)

This register defines the output polarity of the FTM channels.

NOTE

The safe value that is driven in a channel output when the fault control is enabled and a fault condition is detected is the inactive state of the channel. That is, the safe value of a channel is the value of its POL bit.

Address: Base address + 70h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved								POL7	POL6	POL5	POL4	POL3	POL2	POL1	POL0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FTMx_POL field descriptions

Field	Description
31–8 Reserved	This field is reserved.
7 POL7	Channel 7 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
6 POL6	Channel 6 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
5 POL5	Channel 5 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
4 POL4	Channel 4 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
3 POL3	Channel 3 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
2 POL2	Channel 2 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
1 POL1	Channel 1 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1.

Table continues on the next page...

FTMx_POL field descriptions (continued)

Field	Description
	0 The channel polarity is active high. 1 The channel polarity is active low.
0 POL0	Channel 0 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.

47.4.18 Fault Mode Status (FTMx_FMS)

This register contains the fault detection flags, write protection enable bit, and the logic OR of the enabled fault inputs.

Address: Base address + 74h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								FAULTF	WPEN	FAULTIN	0	FAULTF3	FAULTF2	FAULTF1	FAULTF0
W									0				0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FTMx_FMS field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 FAULTF	Fault Detection Flag Represents the logic OR of the individual FAULTFj bits where j = 3, 2, 1, 0. Clear FAULTF by reading the FMS register while FAULTF is set and then writing a 0 to FAULTF while there is no existing fault condition at the enabled fault inputs. Writing a 1 to FAULTF has no effect. If another fault condition is detected in an enabled fault input before the clearing sequence is completed, the sequence is reset so FAULTF remains set after the clearing sequence is completed for the earlier fault condition. FAULTF is also cleared when FAULTFj bits are cleared individually. 0 No fault condition was detected. 1 A fault condition was detected.
6 WPEN	Write Protection Enable The WPEN bit is the negation of the WPDIS bit. WPEN is set when 1 is written to it. WPEN is cleared when WPEN bit is read as a 1 and then 1 is written to WPDIS. Writing 0 to WPEN has no effect. 0 Write protection is disabled. Write protected bits can be written. 1 Write protection is enabled. Write protected bits cannot be written.
5 FAULTIN	Fault Inputs Represents the logic OR of the enabled fault inputs after their filter (if their filter is enabled) when fault control is enabled. 0 The logic OR of the enabled fault inputs is 0. 1 The logic OR of the enabled fault inputs is 1.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 FAULTF3	Fault Detection Flag 3 Set by hardware when fault control is enabled, the corresponding fault input is enabled and a fault condition is detected at the fault input. Clear FAULTF3 by reading the FMS register while FAULTF3 is set and then writing a 0 to FAULTF3 while there is no existing fault condition at the corresponding fault input. Writing a 1 to FAULTF3 has no effect. FAULTF3 bit is also cleared when FAULTF bit is cleared. If another fault condition is detected at the corresponding fault input before the clearing sequence is completed, the sequence is reset so FAULTF3 remains set after the clearing sequence is completed for the earlier fault condition. 0 No fault condition was detected at the fault input. 1 A fault condition was detected at the fault input.
2 FAULTF2	Fault Detection Flag 2 Set by hardware when fault control is enabled, the corresponding fault input is enabled and a fault condition is detected at the fault input. Clear FAULTF2 by reading the FMS register while FAULTF2 is set and then writing a 0 to FAULTF2 while there is no existing fault condition at the corresponding fault input. Writing a 1 to FAULTF2 has no effect. FAULTF2 bit is also cleared when FAULTF bit is cleared.

Table continues on the next page...

FTMx_FMS field descriptions (continued)

Field	Description
	If another fault condition is detected at the corresponding fault input before the clearing sequence is completed, the sequence is reset so FAULTF2 remains set after the clearing sequence is completed for the earlier fault condition. 0 No fault condition was detected at the fault input. 1 A fault condition was detected at the fault input.
1 FAULTF1	Fault Detection Flag 1 Set by hardware when fault control is enabled, the corresponding fault input is enabled and a fault condition is detected at the fault input. Clear FAULTF1 by reading the FMS register while FAULTF1 is set and then writing a 0 to FAULTF1 while there is no existing fault condition at the corresponding fault input. Writing a 1 to FAULTF1 has no effect. FAULTF1 bit is also cleared when FAULTF bit is cleared. If another fault condition is detected at the corresponding fault input before the clearing sequence is completed, the sequence is reset so FAULTF1 remains set after the clearing sequence is completed for the earlier fault condition. 0 No fault condition was detected at the fault input. 1 A fault condition was detected at the fault input.
0 FAULTF0	Fault Detection Flag 0 Set by hardware when fault control is enabled, the corresponding fault input is enabled and a fault condition is detected at the fault input. Clear FAULTF0 by reading the FMS register while FAULTF0 is set and then writing a 0 to FAULTF0 while there is no existing fault condition at the corresponding fault input. Writing a 1 to FAULTF0 has no effect. FAULTF0 bit is also cleared when FAULTF bit is cleared. If another fault condition is detected at the corresponding fault input before the clearing sequence is completed, the sequence is reset so FAULTF0 remains set after the clearing sequence is completed for the earlier fault condition. 0 No fault condition was detected at the fault input. 1 A fault condition was detected at the fault input.

47.4.19 Input Capture Filter Control (FTMx_FILTER)

This register selects the filter value for the inputs of channels.

Channels 4, 5, 6 and 7 do not have an input filter.

NOTE

Writing to the FILTER register has immediate effect and must be done only when the channels 0, 1, 2, and 3 are not in input modes. Failure to do this could result in a missing valid signal.

Address: Base address + 78h offset

Bit	31–16	15–12	11–8	7–4	3–0
R W	Reserved	CH3FVAL	CH2FVAL	CH1FVAL	CH0FVAL
Reset	0000 0000 0000 0000	0000	0000	0000	0000

FTMx_FILTER field descriptions

Field	Description
31–16 Reserved	This field is reserved.
15–12 CH3FVAL	Channel 3 Input Filter Selects the filter value for the channel input. The filter is disabled when the value is zero.
11–8 CH2FVAL	Channel 2 Input Filter Selects the filter value for the channel input. The filter is disabled when the value is zero.
7–4 CH1FVAL	Channel 1 Input Filter Selects the filter value for the channel input. The filter is disabled when the value is zero.
CH0FVAL	Channel 0 Input Filter Selects the filter value for the channel input. The filter is disabled when the value is zero.

47.4.20 Fault Control (FTMx_FLTCTRL)

This register selects the filter value for the fault inputs, enables the fault inputs and the fault inputs filter.

Address: Base address + 7Ch offset

Bit	31–24	23–16
R	0	
W		
Reset	0000 0000	0000 0000

Bit	15–12	11–8	7	6	5	4	3	2	1	0
R	0	FFVAL	FFLTR3EN	FFLTR2EN	FFLTR1EN	FFLTR0EN	FAULT3EN	FAULT2EN	FAULT1EN	FAULT0EN
W										
Reset	0000	0000	0	0	0	0	0	0	0	0

FTMx_FLTCTRL field descriptions

Field	Description
31–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11–8 FFVAL	Fault Input Filter Selects the filter value for the fault inputs. The fault filter is disabled when the value is zero. **NOTE:** Writing to this field has immediate effect and must be done only when the fault control or all fault inputs are disabled. Failure to do this could result in a missing fault detection.
7 FFLTR3EN	Fault Input 3 Filter Enable Enables the filter for the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input filter is disabled. 1 Fault input filter is enabled.
6 FFLTR2EN	Fault Input 2 Filter Enable Enables the filter for the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input filter is disabled. 1 Fault input filter is enabled.
5 FFLTR1EN	Fault Input 1 Filter Enable Enables the filter for the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input filter is disabled. 1 Fault input filter is enabled.
4 FFLTR0EN	Fault Input 0 Filter Enable Enables the filter for the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input filter is disabled. 1 Fault input filter is enabled.
3 FAULT3EN	Fault Input 3 Enable Enables the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input is disabled. 1 Fault input is enabled.
2 FAULT2EN	Fault Input 2 Enable Enables the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input is disabled. 1 Fault input is enabled.

Table continues on the next page...

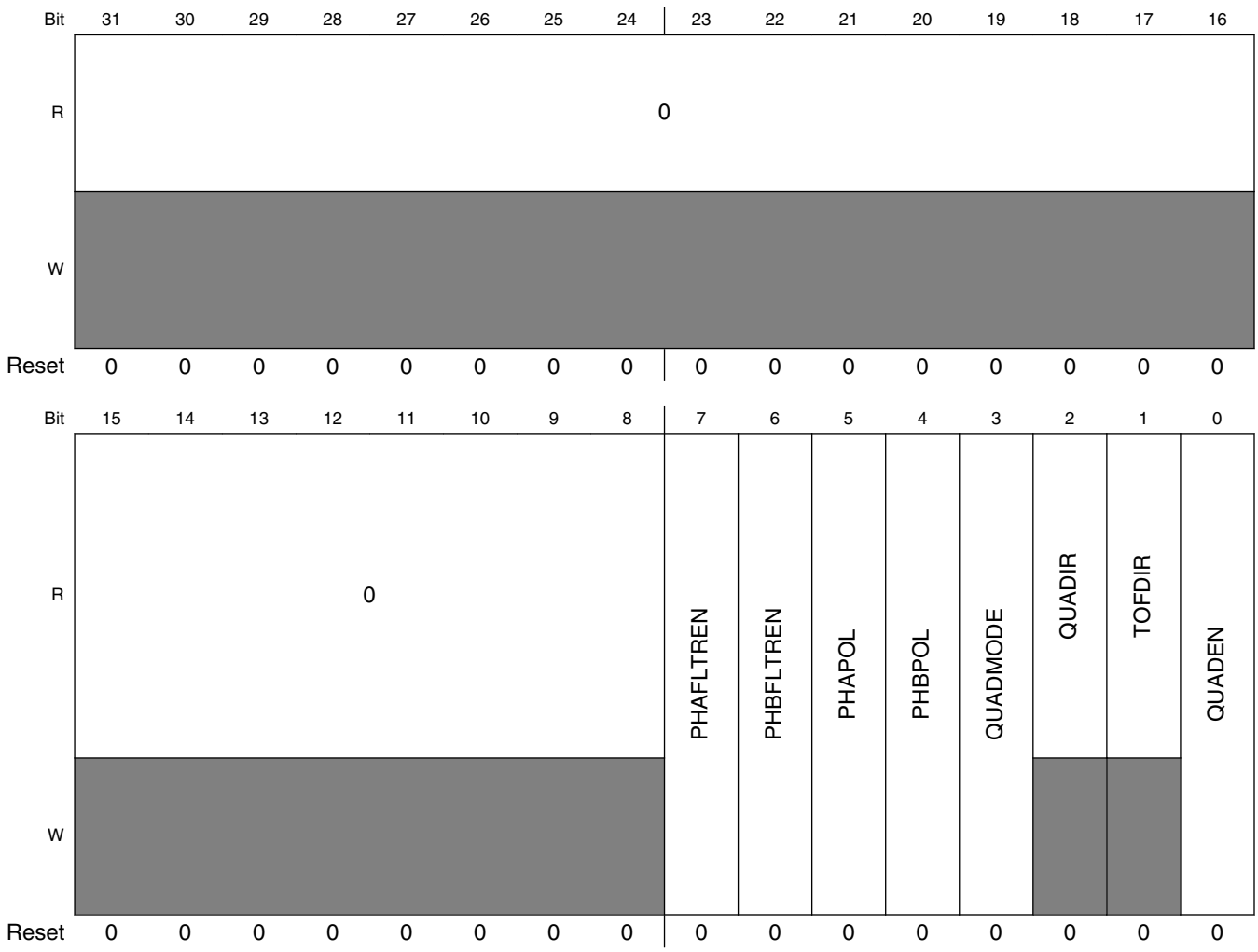
FTMx_FLTCTRL field descriptions (continued)

Field	Description
1 FAULT1EN	Fault Input 1 Enable Enables the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input is disabled. 1 Fault input is enabled.
0 FAULT0EN	Fault Input 0 Enable Enables the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input is disabled. 1 Fault input is enabled.

47.4.21 Quadrature Decoder Control And Status (FTMx_QDCTRL)

This register has the control and status bits for the Quadrature Decoder mode.

Address: Base address + 80h offset



FTMx_QDCTRL field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 PHAFLTREN	Phase A Input Filter Enable Enables the filter for the quadrature decoder phase A input. The filter value for the phase A input is defined by the CH0FVAL field of FILTER. The phase A filter is also disabled when CH0FVAL is zero. 0 Phase A input filter is disabled. 1 Phase A input filter is enabled.

Table continues on the next page...

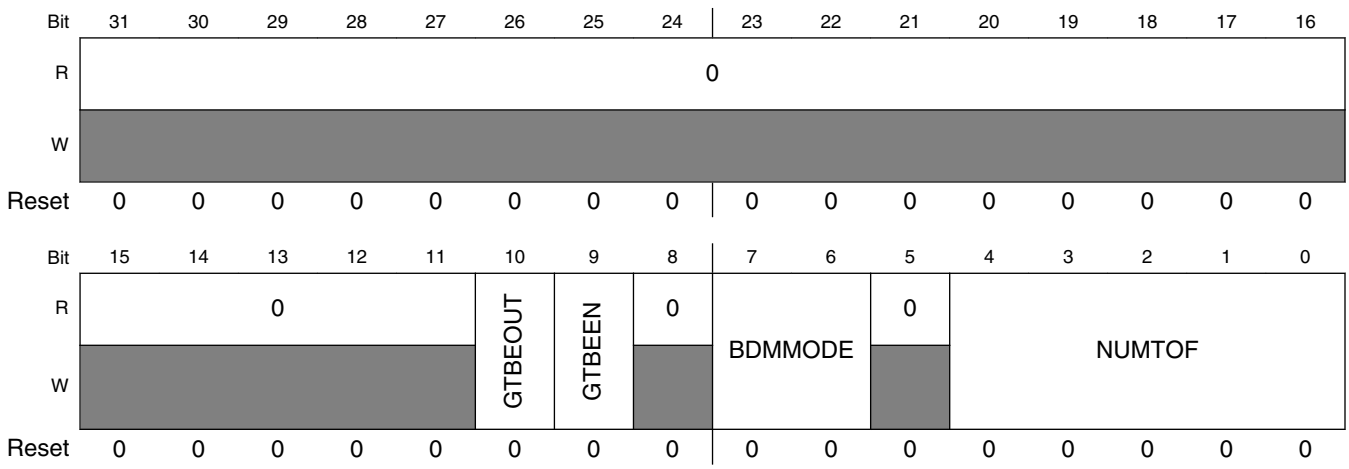
FTMx_QDCTRL field descriptions (continued)

Field	Description
6 PHBFLTREN	Phase B Input Filter Enable Enables the filter for the quadrature decoder phase B input. The filter value for the phase B input is defined by the CH1FVAL field of FILTER. The phase B filter is also disabled when CH1FVAL is zero. 0 Phase B input filter is disabled. 1 Phase B input filter is enabled.
5 PHAPOL	Phase A Input Polarity Selects the polarity for the quadrature decoder phase A input. 0 Normal polarity. Phase A input signal is not inverted before identifying the rising and falling edges of this signal. 1 Inverted polarity. Phase A input signal is inverted before identifying the rising and falling edges of this signal.
4 PHBPOL	Phase B Input Polarity Selects the polarity for the quadrature decoder phase B input. 0 Normal polarity. Phase B input signal is not inverted before identifying the rising and falling edges of this signal. 1 Inverted polarity. Phase B input signal is inverted before identifying the rising and falling edges of this signal.
3 QUADMODE	Quadrature Decoder Mode Selects the encoding mode used in the Quadrature Decoder mode. 0 Phase A and phase B encoding mode. 1 Count and direction encoding mode.
2 QUADIR	FTM Counter Direction In Quadrature Decoder Mode Indicates the counting direction. 0 Counting direction is decreasing (FTM counter decrement). 1 Counting direction is increasing (FTM counter increment).
1 TOFDIR	Timer Overflow Direction In Quadrature Decoder Mode Indicates if the TOF bit was set on the top or the bottom of counting. 0 TOF bit was set on the bottom of counting. There was an FTM counter decrement and FTM counter changes from its minimum value (CNTIN register) to its maximum value (MOD register). 1 TOF bit was set on the top of counting. There was an FTM counter increment and FTM counter changes from its maximum value (MOD register) to its minimum value (CNTIN register).
0 QUADEN	Quadrature Decoder Mode Enable Enables the Quadrature Decoder mode. In this mode, the phase A and B input signals control the FTM counter direction. The Quadrature Decoder mode has precedence over the other modes. See Table 47-3. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Quadrature Decoder mode is disabled. 1 Quadrature Decoder mode is enabled.

47.4.22 Configuration (FTMx_CONF)

This register selects the number of times that the FTM counter overflow should occur before the TOF bit to be set, the FTM behavior in BDM modes, the use of an external global time base, and the global time base signal generation.

Address: Base address + 84h offset



FTMx_CONF field descriptions

Field	Description
31–11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10 GTBEOUT	Global Time Base Output Enables the global time base signal generation to other FTMs. 0 A global time base signal generation is disabled. 1 A global time base signal generation is enabled.
9 GTBEEN	Global Time Base Enable Configures the FTM to use an external global time base signal that is generated by another FTM. 0 Use of an external global time base is disabled. 1 Use of an external global time base is enabled.
8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7–6 BDMMODE	BDM Mode Selects the FTM behavior in BDM mode. See BDM mode.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
NUMTOF	TOF Frequency

Table continues on the next page...

FTMx_CONF field descriptions (continued)

Field	Description
	Selects the ratio between the number of counter overflows to the number of times the TOF bit is set. NUMTOF = 0: The TOF bit is set for each counter overflow. NUMTOF = 1: The TOF bit is set for the first counter overflow but not for the next overflow. NUMTOF = 2: The TOF bit is set for the first counter overflow but not for the next 2 overflows. NUMTOF = 3: The TOF bit is set for the first counter overflow but not for the next 3 overflows. This pattern continues up to a maximum of 31.

47.4.23 FTM Fault Input Polarity (FTMx_FLTPOL)

This register defines the fault inputs polarity.

Address: Base address + 88h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												FLT3POL	FLT2POL	FLT1POL	FLT0POL
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FTMx_FLTPOL field descriptions

Field	Description
31–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 FLT3POL	Fault Input 3 Polarity Defines the polarity of the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The fault input polarity is active high. A 1 at the fault input indicates a fault. 1 The fault input polarity is active low. A 0 at the fault input indicates a fault.
2 FLT2POL	Fault Input 2 Polarity Defines the polarity of the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1.

Table continues on the next page...

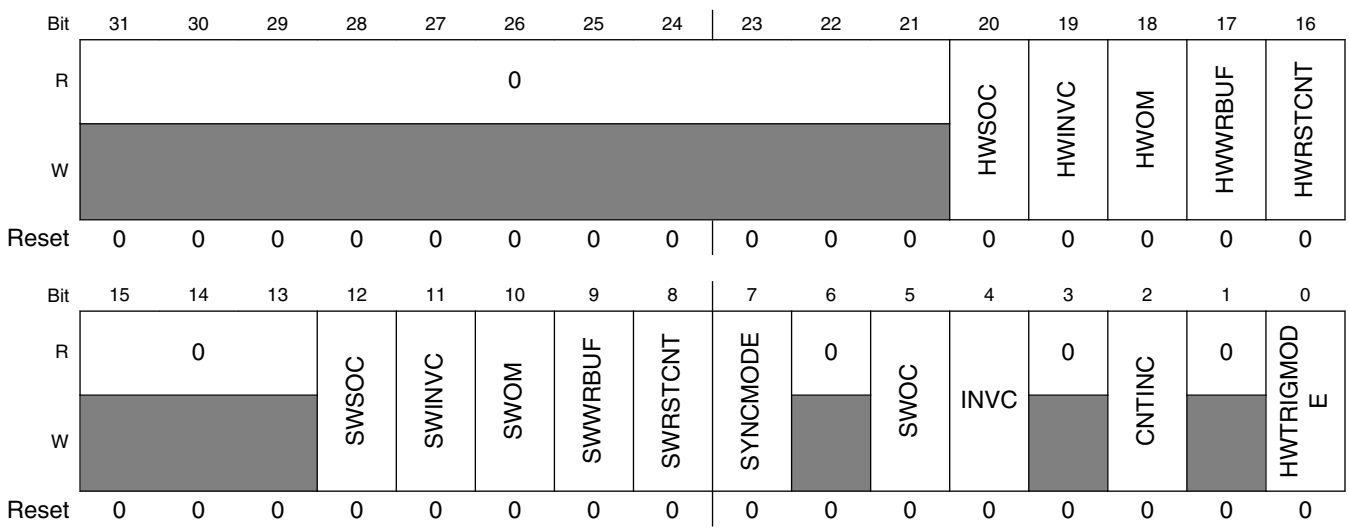
FTMx_FLTPOL field descriptions (continued)

Field	Description
	0 The fault input polarity is active high. A 1 at the fault input indicates a fault. 1 The fault input polarity is active low. A 0 at the fault input indicates a fault.
1 FLT1POL	Fault Input 1 Polarity Defines the polarity of the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The fault input polarity is active high. A 1 at the fault input indicates a fault. 1 The fault input polarity is active low. A 0 at the fault input indicates a fault.
0 FLT0POL	Fault Input 0 Polarity Defines the polarity of the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The fault input polarity is active high. A 1 at the fault input indicates a fault. 1 The fault input polarity is active low. A 0 at the fault input indicates a fault.

47.4.24 Synchronization Configuration (FTMx_SYNCONF)

This register selects the PWM synchronization configuration, SWOCTRL, INVCTRL and CNTIN registers synchronization, if FTM clears the TRIGj bit, where j = 0, 1, 2, when the hardware trigger j is detected.

Address: Base address + 8Ch offset



FTMx_SYNCONF field descriptions

Field	Description
31–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

FTMx_SYNCONF field descriptions (continued)

Field	Description
20 HWSOC	Software output control synchronization is activated by a hardware trigger. 0 A hardware trigger does not activate the SWOCTRL register synchronization. 1 A hardware trigger activates the SWOCTRL register synchronization.
19 HWINVC	Inverting control synchronization is activated by a hardware trigger. 0 A hardware trigger does not activate the INVCTRL register synchronization. 1 A hardware trigger activates the INVCTRL register synchronization.
18 HWOM	Output mask synchronization is activated by a hardware trigger. 0 A hardware trigger does not activate the OUTMASK register synchronization. 1 A hardware trigger activates the OUTMASK register synchronization.
17 HWWRBUF	MOD, CNTIN, and CV registers synchronization is activated by a hardware trigger. 0 A hardware trigger does not activate MOD, CNTIN, and CV registers synchronization. 1 A hardware trigger activates MOD, CNTIN, and CV registers synchronization.
16 HWRSTCNT	FTM counter synchronization is activated by a hardware trigger. 0 A hardware trigger does not activate the FTM counter synchronization. 1 A hardware trigger activates the FTM counter synchronization.
15–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12 SWSOC	Software output control synchronization is activated by the software trigger. 0 The software trigger does not activate the SWOCTRL register synchronization. 1 The software trigger activates the SWOCTRL register synchronization.
11 SWINVC	Inverting control synchronization is activated by the software trigger. 0 The software trigger does not activate the INVCTRL register synchronization. 1 The software trigger activates the INVCTRL register synchronization.
10 SWOM	Output mask synchronization is activated by the software trigger. 0 The software trigger does not activate the OUTMASK register synchronization. 1 The software trigger activates the OUTMASK register synchronization.
9 SWWRBUF	MOD, CNTIN, and CV registers synchronization is activated by the software trigger. 0 The software trigger does not activate MOD, CNTIN, and CV registers synchronization. 1 The software trigger activates MOD, CNTIN, and CV registers synchronization.
8 SWRSTCNT	FTM counter synchronization is activated by the software trigger. 0 The software trigger does not activate the FTM counter synchronization. 1 The software trigger activates the FTM counter synchronization.
7 SYNCMODE	Synchronization Mode Selects the PWM Synchronization mode. 0 Legacy PWM synchronization is selected. 1 Enhanced PWM synchronization is selected.

Table continues on the next page...

FTMx_SYNCONF field descriptions (continued)

Field	Description
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 SWOC	SWOCTRL Register Synchronization 0 SWOCTRL register is updated with its buffer value at all rising edges of system clock. 1 SWOCTRL register is updated with its buffer value by the PWM synchronization.
4 INVC	INVCTRL Register Synchronization 0 INVCTRL register is updated with its buffer value at all rising edges of system clock. 1 INVCTRL register is updated with its buffer value by the PWM synchronization.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 CNTINC	CNTIN Register Synchronization 0 CNTIN register is updated with its buffer value at all rising edges of system clock. 1 CNTIN register is updated with its buffer value by the PWM synchronization.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 HWTRIGMODE	Hardware Trigger Mode 0 FTM clears the TRIGj bit when the hardware trigger j is detected, where j = 0, 1,2. 1 FTM does not clear the TRIGj bit when the hardware trigger j is detected, where j = 0, 1,2.

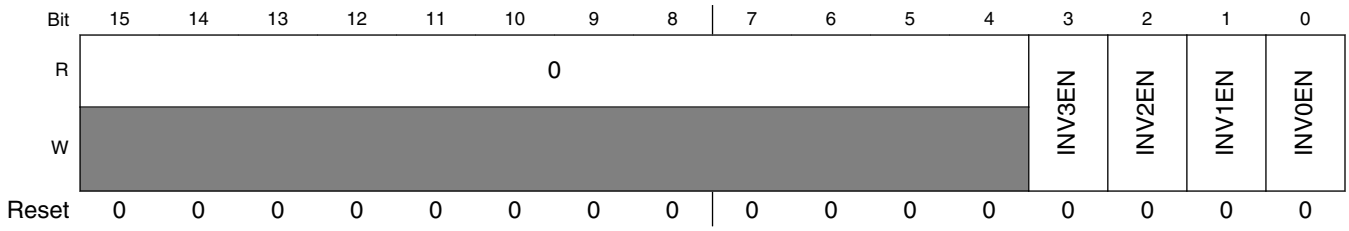
47.4.25 FTM Inverting Control (FTMx_INVCTRL)

This register controls when the channel (n) output becomes the channel (n+1) output, and channel (n+1) output becomes the channel (n) output. Each INVmEN bit enables the inverting operation for the corresponding pair channels m.

This register has a write buffer. The INVmEN bit is updated by the INVCTRL register synchronization.

Address: Base address + 90h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



FTMx_INVCTRL field descriptions

Field	Description
31–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 INV3EN	Pair Channels 3 Inverting Enable 0 Inverting is disabled. 1 Inverting is enabled.
2 INV2EN	Pair Channels 2 Inverting Enable 0 Inverting is disabled. 1 Inverting is enabled.
1 INV1EN	Pair Channels 1 Inverting Enable 0 Inverting is disabled. 1 Inverting is enabled.
0 INV0EN	Pair Channels 0 Inverting Enable 0 Inverting is disabled. 1 Inverting is enabled.

47.4.26 FTM Software Output Control (FTMx_SWOCTRL)

This register enables software control of channel (n) output and defines the value forced to the channel (n) output:

- The CHnOC bits enable the control of the corresponding channel (n) output by software.
- The CHnOCV bits select the value that is forced at the corresponding channel (n) output.

This register has a write buffer. The fields are updated by the SWOCTRL register synchronization.

Address: Base address + 94h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CH7OCV	CH6OCV	CH5OCV	CH4OCV	CH3OCV	CH2OCV	CH1OCV	CH0OCV	CH7OC	CH6OC	CH5OC	CH4OC	CH3OC	CH2OC	CH1OC	CH0OC
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FTMx_SWOCTRL field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15 CH7OCV	Channel 7 Software Output Control Value 0 The software output control forces 0 to the channel output. 1 The software output control forces 1 to the channel output.
14 CH6OCV	Channel 6 Software Output Control Value 0 The software output control forces 0 to the channel output. 1 The software output control forces 1 to the channel output.
13 CH5OCV	Channel 5 Software Output Control Value 0 The software output control forces 0 to the channel output. 1 The software output control forces 1 to the channel output.
12 CH4OCV	Channel 4 Software Output Control Value 0 The software output control forces 0 to the channel output. 1 The software output control forces 1 to the channel output.
11 CH3OCV	Channel 3 Software Output Control Value 0 The software output control forces 0 to the channel output. 1 The software output control forces 1 to the channel output.
10 CH2OCV	Channel 2 Software Output Control Value 0 The software output control forces 0 to the channel output. 1 The software output control forces 1 to the channel output.
9 CH1OCV	Channel 1 Software Output Control Value 0 The software output control forces 0 to the channel output. 1 The software output control forces 1 to the channel output.
8 CH0OCV	Channel 0 Software Output Control Value

Table continues on the next page...

FTMx_SWOCTRL field descriptions (continued)

Field	Description
	0 The software output control forces 0 to the channel output. 1 The software output control forces 1 to the channel output.
7 CH7OC	Channel 7 Software Output Control Enable 0 The channel output is not affected by software output control. 1 The channel output is affected by software output control.
6 CH6OC	Channel 6 Software Output Control Enable 0 The channel output is not affected by software output control. 1 The channel output is affected by software output control.
5 CH5OC	Channel 5 Software Output Control Enable 0 The channel output is not affected by software output control. 1 The channel output is affected by software output control.
4 CH4OC	Channel 4 Software Output Control Enable 0 The channel output is not affected by software output control. 1 The channel output is affected by software output control.
3 CH3OC	Channel 3 Software Output Control Enable 0 The channel output is not affected by software output control. 1 The channel output is affected by software output control.
2 CH2OC	Channel 2 Software Output Control Enable 0 The channel output is not affected by software output control. 1 The channel output is affected by software output control.
1 CH1OC	Channel 1 Software Output Control Enable 0 The channel output is not affected by software output control. 1 The channel output is affected by software output control.
0 CH0OC	Channel 0 Software Output Control Enable 0 The channel output is not affected by software output control. 1 The channel output is affected by software output control.

47.4.27 FTM PWM Load (FTMx_PWMLOAD)

Enables the loading of the MOD, CNTIN, C(n)V, and C(n+1)V registers with the values of their write buffers when the FTM counter changes from the MOD register value to its next value or when a channel (j) match occurs. A match occurs for the channel (j) when FTM counter = C(j)V.

Address: Base address + 98h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0						LDOK	0	CH7SEL	CH6SEL	CH5SEL	CH4SEL	CH3SEL	CH2SEL	CH1SEL	CH0SEL
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FTMx_PWMLOAD field descriptions

Field	Description
31–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9 LDOK	Load Enable Enables the loading of the MOD, CNTIN, and CV registers with the values of their write buffers. 0 Loading updated values is disabled. 1 Loading updated values is enabled.
8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 CH7SEL	Channel 7 Select 0 Do not include the channel in the matching process. 1 Include the channel in the matching process.
6 CH6SEL	Channel 6 Select 0 Do not include the channel in the matching process. 1 Include the channel in the matching process.
5 CH5SEL	Channel 5 Select 0 Do not include the channel in the matching process. 1 Include the channel in the matching process.

Table continues on the next page...

FTMx_PWMLOAD field descriptions (continued)

Field	Description
4 CH4SEL	Channel 4 Select 0 Do not include the channel in the matching process. 1 Include the channel in the matching process.
3 CH3SEL	Channel 3 Select 0 Do not include the channel in the matching process. 1 Include the channel in the matching process.
2 CH2SEL	Channel 2 Select 0 Do not include the channel in the matching process. 1 Include the channel in the matching process.
1 CH1SEL	Channel 1 Select 0 Do not include the channel in the matching process. 1 Include the channel in the matching process.
0 CH0SEL	Channel 0 Select 0 Do not include the channel in the matching process. 1 Include the channel in the matching process.

47.5 Functional description

The notation used in this document to represent the counters and the generation of the signals is shown in the following figure.

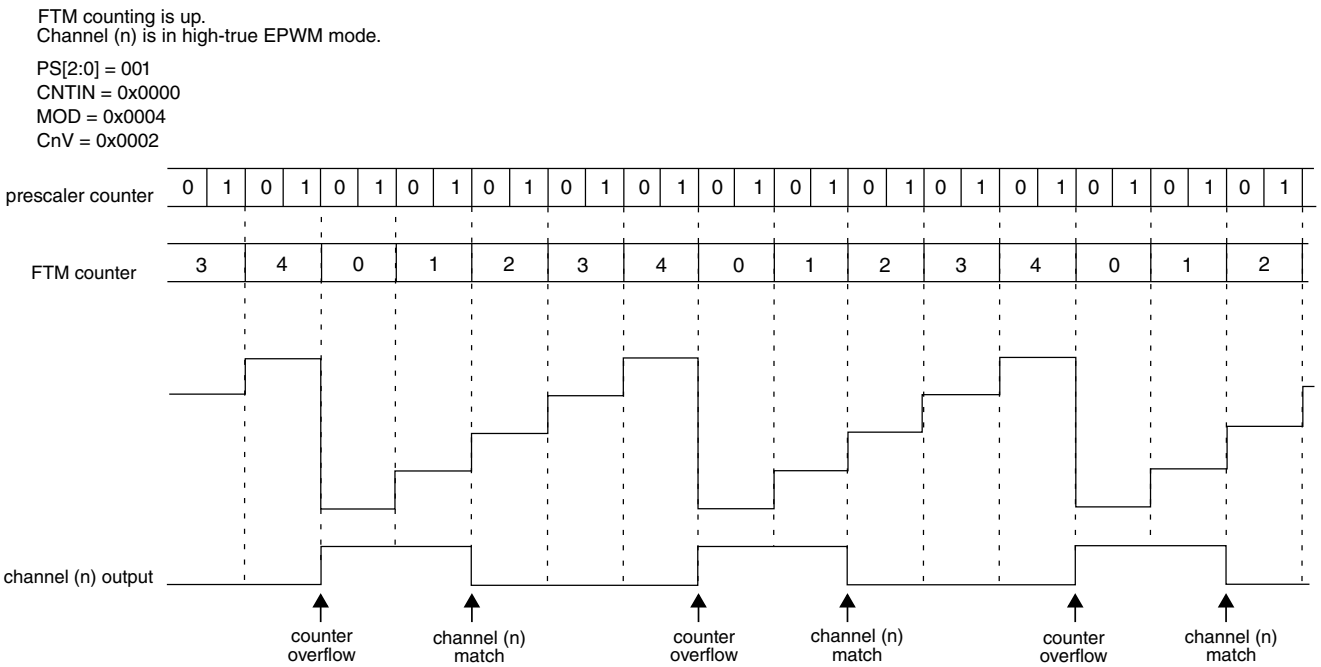


Figure 47-7. Notation used

47.5.1 Clock source

The FTM has only one clock domain: the system clock.

47.5.1.1 Counter clock source

The CLKS[1:0] bits in the SC register selects clock sources for the FTM counter or disables the FTM counter. After any chip reset, CLKS[1:0] = 0:0 so no clock source is selected.

The CLKS[1:0] bits may be read or written at any time. Disabling the FTM counter by writing 0:0 to the CLKS[1:0] bits does not affect the FTM counter value or other registers.

The fixed frequency clock is an alternative clock source for the FTM counter that allows the selection of a clock other than the system clock or an external clock. This clock input is defined by chip integration; see the chip-specific FTM information for further details. Due to FTM hardware implementation limitations, the frequency of the fixed frequency clock must not exceed 1/2 of the system clock frequency.

The external clock passes through a synchronizer clocked by the system clock to assure that counter transitions are properly aligned to system clock transitions.Therefore, to meet Nyquist criteria considering also jitter, the frequency of the external clock source must not exceed 1/4 of the system clock frequency.

47.5.2 Prescaler

The selected counter clock source passes through a prescaler that is a 7-bit counter. The value of the prescaler is selected by the PS[2:0] bits. The following figure shows an example of the prescaler counter and FTM counter.

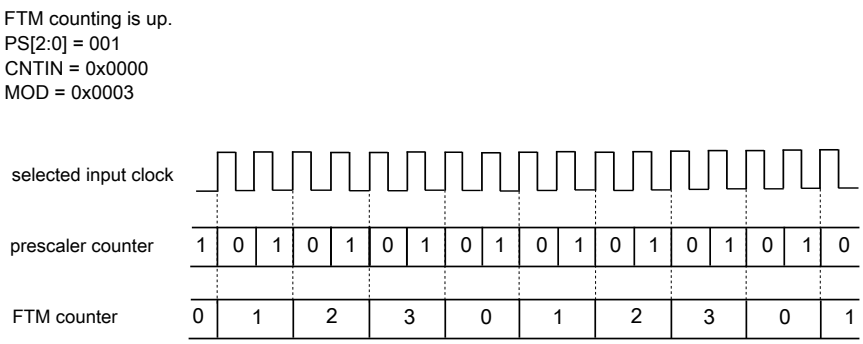


Figure 47-8. Example of the prescaler counter

47.5.3 Counter

The FTM has a 16-bit counter that is used by the channels either for input or output modes. The FTM counter clock is the selected clock divided by the prescaler.

The FTM counter has these modes of operation:

- Up counting
- Up-down counting
- Quadrature Decoder mode

47.5.3.1 Up counting

Up counting is selected when:

- QUADEN = 0, and
- CPWMS = 0

CNTIN defines the starting value of the count and MOD defines the final value of the count, see the following figure. The value of CNTIN is loaded into the FTM counter, and the counter increments until the value of MOD is reached, at which point the counter is reloaded with the value of CNTIN.

The FTM period when using up counting is (MOD – CNTIN + 0x0001) × period of the FTM counter clock.

The TOF bit is set when the FTM counter changes from MOD to CNTIN.

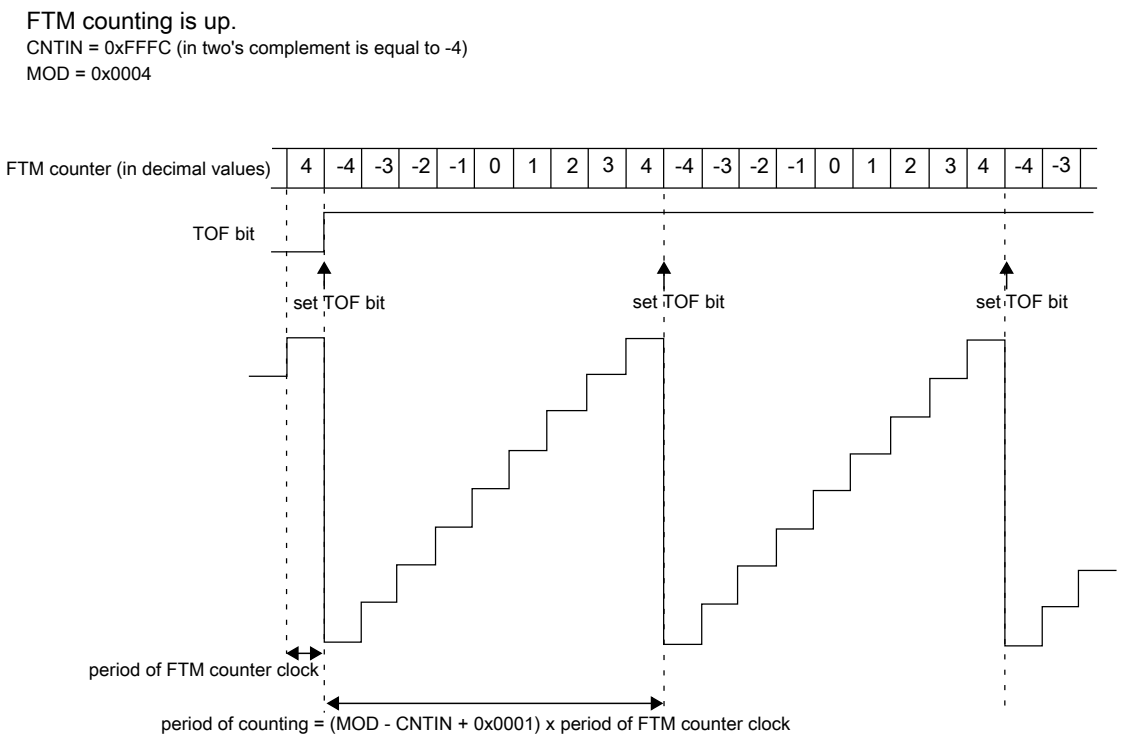


Figure 47-9. Example of FTM up and signed counting

Table 47-5. FTM counting based on CNTIN value

When	Then
CNTIN = 0x0000	The FTM counting is equivalent to TPM up counting, that is, up and unsigned counting. See the following figure.
CNTIN[15] = 1	The initial value of the FTM counter is a negative number in two's complement, so the FTM counting is up and signed.
CNTIN[15] = 0 and CNTIN ≠ 0x0000	The initial value of the FTM counter is a positive number, so the FTM counting is up and unsigned.

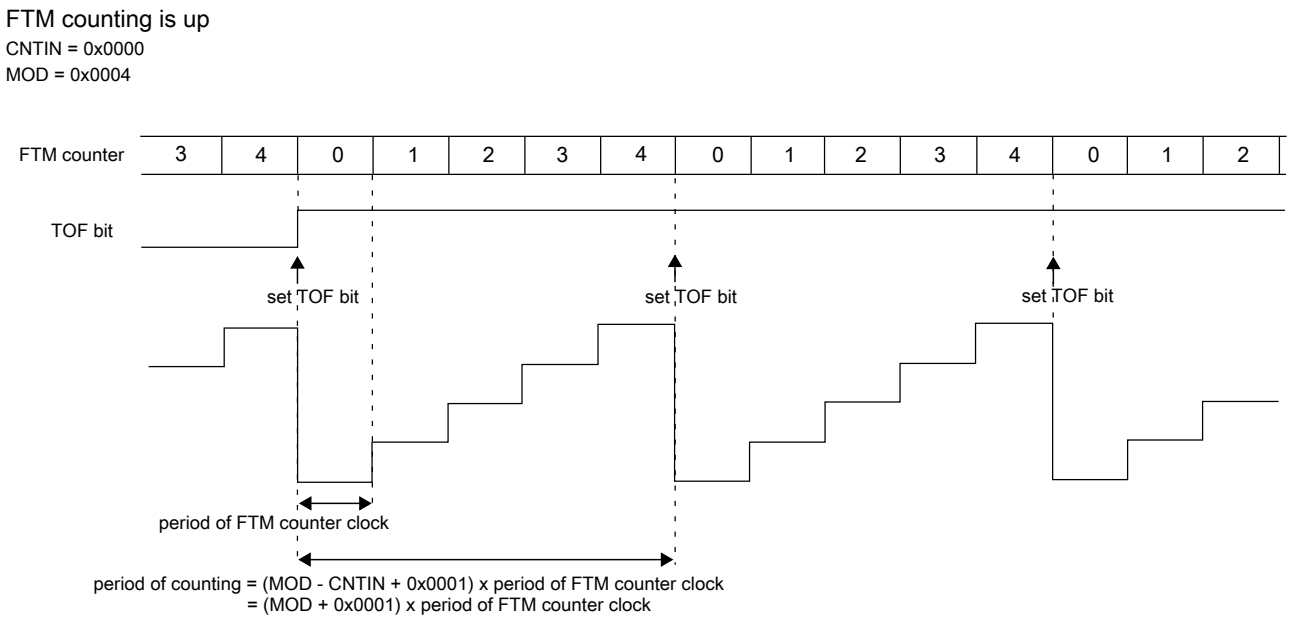


Figure 47-10. Example of FTM up counting with CNTIN = 0x0000

Note

- FTM operation is only valid when the value of the CNTIN register is less than the value of the MOD register, either in the unsigned counting or signed counting. It is the responsibility of the software to ensure that the values in the CNTIN and MOD registers meet this requirement. Any values of CNTIN and MOD that do not satisfy this criteria can result in unpredictable behavior.
- MOD = CNTIN is a redundant condition. In this case, the FTM counter is always equal to MOD and the TOF bit is set in each rising edge of the FTM counter clock.
- When MOD = 0x0000, CNTIN = 0x0000, for example after reset, and FTMEN = 1, the FTM counter remains stopped at 0x0000 until a non-zero value is written into the MOD or CNTIN registers.
- Setting CNTIN to be greater than the value of MOD is not recommended as this unusual setting may make the FTM operation difficult to comprehend. However, there is no restriction on this configuration, and an example is shown in the following figure.

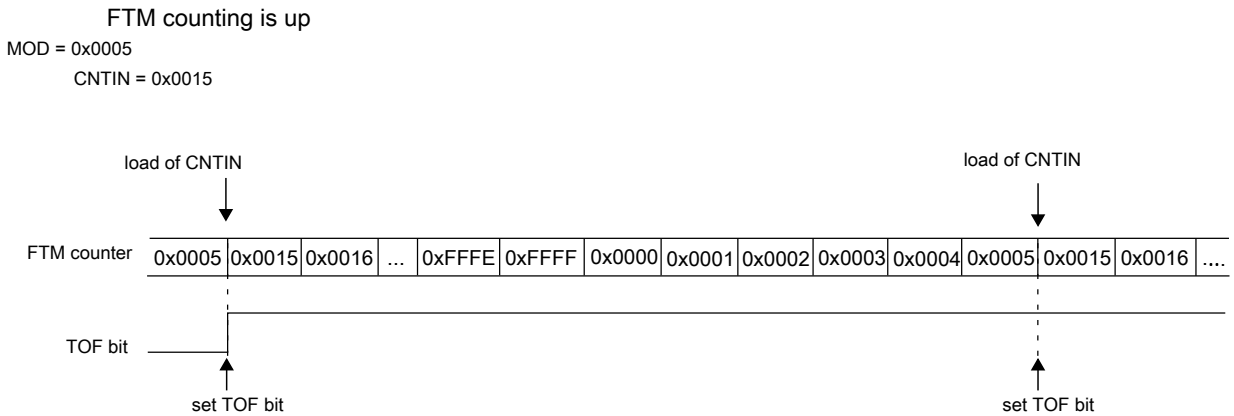


Figure 47-11. Example of up counting when the value of CNTIN is greater than the value of MOD

47.5.3.2 Up-down counting

Up-down counting is selected when:

- QUADEN = 0, and
- CPWMS = 1

CNTIN defines the starting value of the count and MOD defines the final value of the count. The value of CNTIN is loaded into the FTM counter, and the counter increments until the value of MOD is reached, at which point the counter is decremented until it returns to the value of CNTIN and the up-down counting restarts.

The FTM period when using up-down counting is 2 × (MOD – CNTIN) × period of the FTM counter clock.

The TOF bit is set when the FTM counter changes from MOD to (MOD – 1).

If (CNTIN = 0x0000), the FTM counting is equivalent to TPM up-down counting, that is, up-down and unsigned counting. See the following figure.

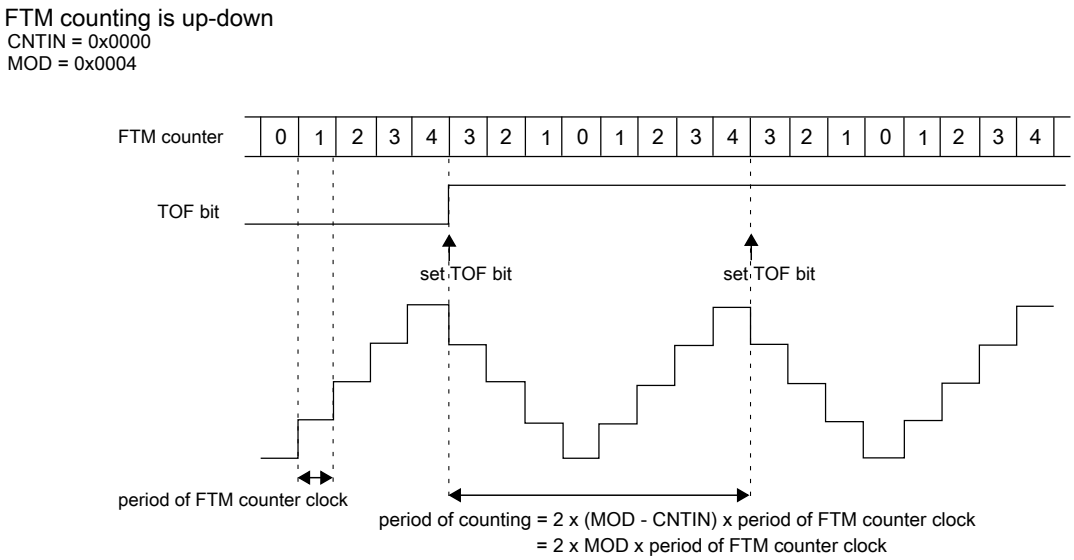


Figure 47-12. Example of up-down counting when CNTIN = 0x0000

Note

When CNTIN is different from zero in the up-down counting, a valid CPWM signal is generated:

- if CnV > CNTIN, or
- if CnV = 0 or if CnV[15] = 1. In this case, 0% CPWM is generated.

47.5.3.3 Free running counter

If (FTMEN = 0) and (MOD = 0x0000 or MOD = 0xFFFF), the FTM counter is a free running counter. In this case, the FTM counter runs free from 0x0000 through 0xFFFF and the TOF bit is set when the FTM counter changes from 0xFFFF to 0x0000. See the following figure.

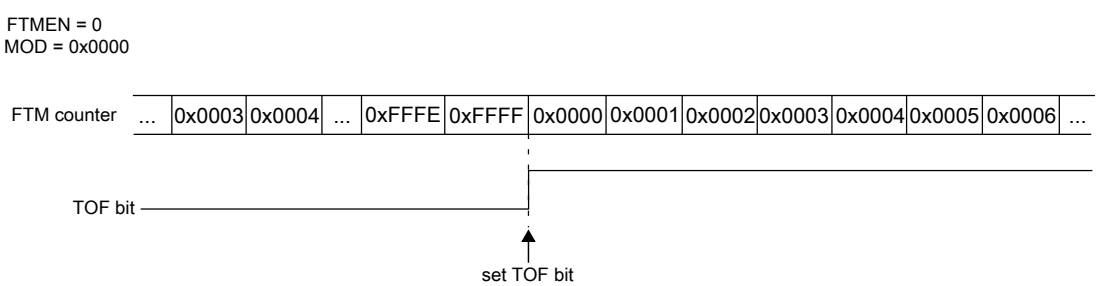


Figure 47-13. Example when the FTM counter is free running

The FTM counter is also a free running counter when:

- FTMEN = 1
- QUADEN = 0
- CPWMS = 0
- CNTIN = 0x0000, and
- MOD = 0xFFFF

47.5.3.4 Counter reset

Any one of the following cases resets the FTM counter to the value in the CNTIN register and the channels output to its initial value, except for channels in Output Compare mode.

- Any write to CNT.
- FTM counter synchronization.
- A channel in Input Capture mode with ICRST = 1 (FTM Counter Reset in Input Capture Mode).

47.5.3.5 When the TOF bit is set

The NUMTOF[4:0] bits define the number of times that the FTM counter overflow should occur before the TOF bit to be set. If NUMTOF[4:0] = 0x00, then the TOF bit is set at each FTM counter overflow.

Initialize the FTM counter, by writing to CNT, after writing to the NUMTOF[4:0] bits to avoid confusion about when the first counter overflow will occur.

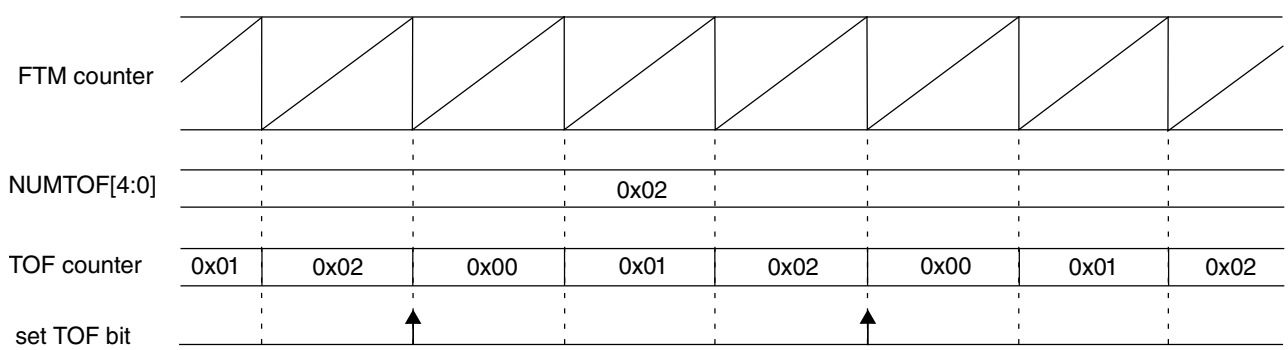


Figure 47-14. Periodic TOF when NUMTOF = 0x02

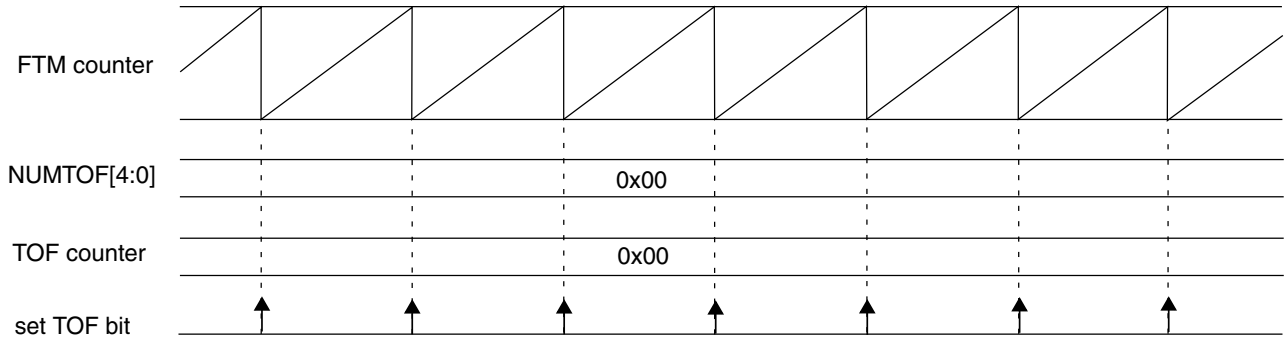


Figure 47-15. Periodic TOF when NUMTOF = 0x00

47.5.4 Input Capture mode

The Input Capture mode is selected when:

- DECAPEN = 0
- COMBINE = 0
- CPWMS = 0
- MSnB:MSnA = 0:0, and
- ELSnB:ELSnA ≠ 0:0

When a selected edge occurs on the channel input, the current value of the FTM counter is captured into the CnV register, at the same time the CHnF bit is set and the channel interrupt is generated if enabled by CHnIE = 1. See the following figure.

When a channel is configured for input capture, the FTMxCHn pin is an edge-sensitive input. ELSnB:ELSnA control bits determine which edge, falling or rising, triggers input-capture event. Note that the maximum frequency for the channel input signal to be detected correctly is system clock divided by 4, which is required to meet Nyquist criteria for signal sampling.

Writes to the CnV register is ignored in Input Capture mode.

While in BDM, the input capture function works as configured. When a selected edge event occurs, the FTM counter value, which is frozen because of BDM, is captured into the CnV register and the CHnF bit is set.

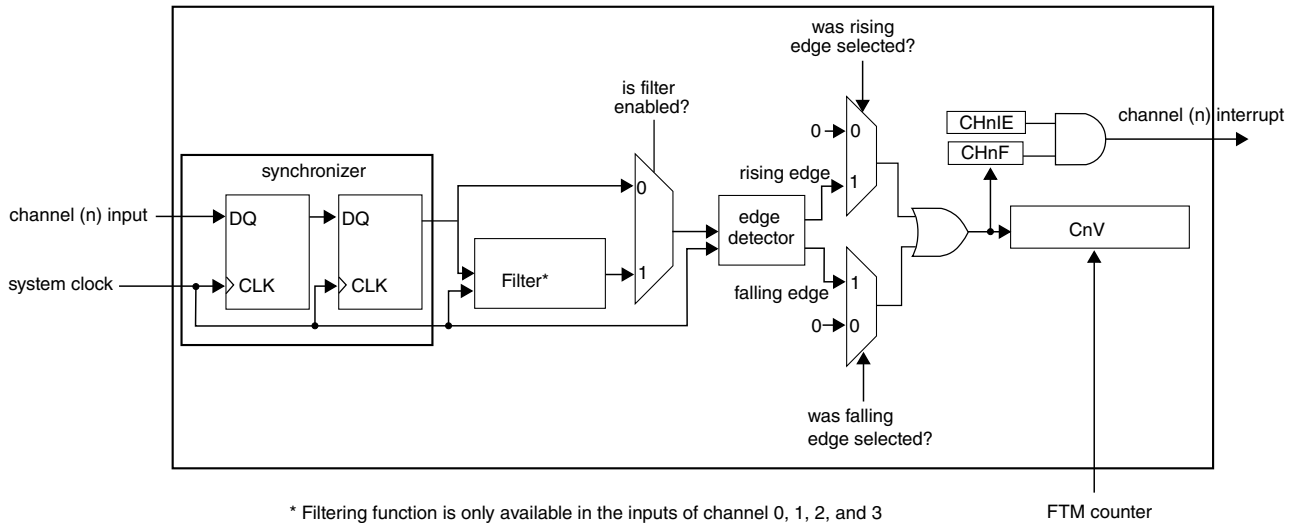


Figure 47-16. Input Capture mode

If the channel input does not have a filter enabled, then the input signal is always delayed 3 rising edges of the system clock, that is, two rising edges to the synchronizer plus one more rising edge to the edge detector. In other words, the CHnF bit is set on the third rising edge of the system clock after a valid edge occurs on the channel input.

47.5.4.1 Filter for Input Capture mode

The filter function is only available on channels 0, 1, 2, and 3.

First, the input signal is synchronized by the system clock. Following synchronization, the input signal enters the filter block. See the following figure.

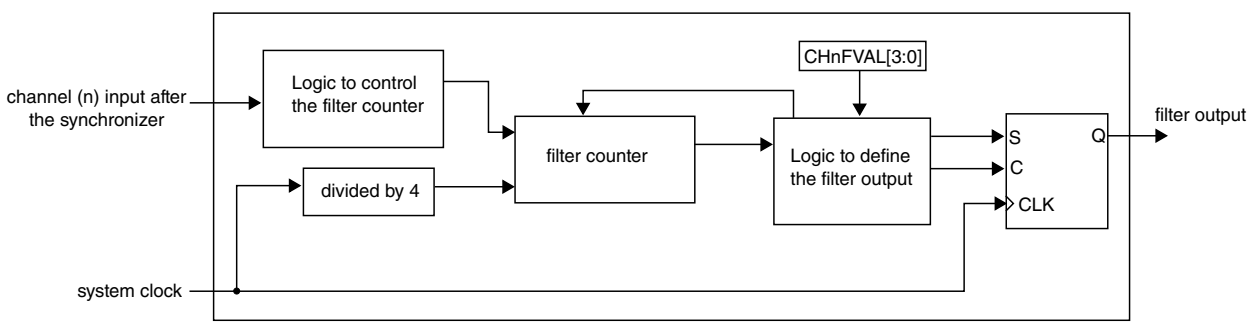


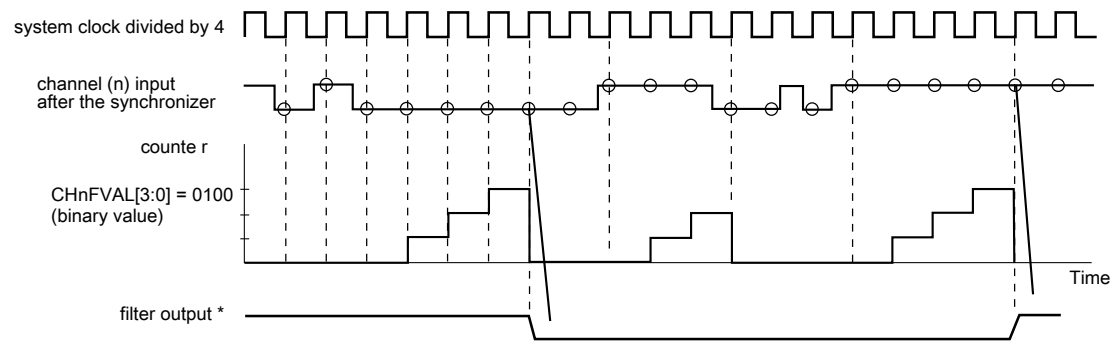
Figure 47-17. Channel input filter

When there is a state change in the input signal, the counter is reset and starts counting up. As long as the new state is stable on the input, the counter continues to increment. When the counter is equal to CHnFVAL[3:0], the state change of the input signal is validated. It is then transmitted as a pulse edge to the edge detector.

If the opposite edge appears on the input signal before it can be validated, the counter is reset. At the next input transition, the counter starts counting again. Any pulse that is shorter than the minimum value selected by CHnFVAL[3:0] (× 4 system clocks) is regarded as a glitch and is not passed on to the edge detector. A timing diagram of the input filter is shown in the following figure.

The filter function is disabled when CHnFVAL[3:0] bits are zero. In this case, the input signal is delayed 3 rising edges of the system clock. If (CHnFVAL[3:0] ≠ 0000), then the input signal is delayed by the minimum pulse width (CHnFVAL[3:0] × 4 system clocks) plus a further 4 rising edges of the system clock: two rising edges to the synchronizer, one rising edge to the filter output, plus one more to the edge detector. In other words, CHnF is set (4 + 4 × CHnFVAL[3:0]) system clock periods after a valid edge occurs on the channel input.

The clock for the counter in the channel input filter is the system clock divided by 4.



* Note: Filter output is delayed one system clock of filter counter logic output.

Figure 47-18. Channel input filter example

The figure below shows an example of input capture with filter enabled and the delay added by each part of the input capture logic. Note that the input signal is delayed only by the synchronizer and edge dector logic if the filter is disabled.

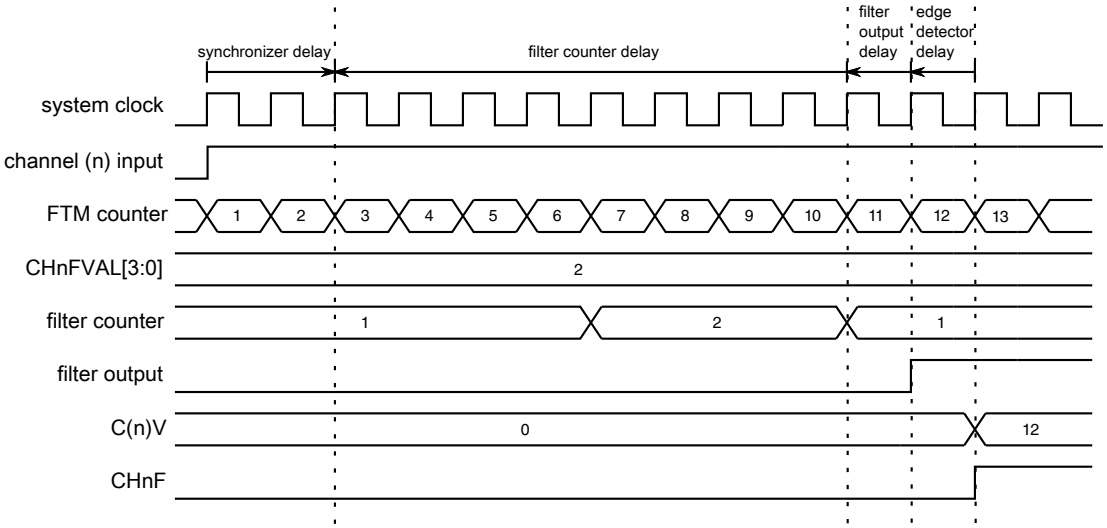


Figure 47-19. Input capture example

47.5.4.2 FTM Counter Reset in Input Capture Mode

If the channel (n) is in input capture mode and FTMx_CnSC [ICRST = 1], then when the selected input capture event occurs in the channel (n) input signal, the current value of the FTM counter is captured into the CnV register, the CHnF bit is set, the channel (n) interrupt is generated (if CHnIE = 1) and the FTM counter is reset to the CNTIN register value.

This allows the FTM to measure a period/pulse being applied to FTM_CHn (counts of the FTM clock input) without having to implement a subtraction calculation in software subsequent to the event occurring.

The figure below shows the FTM counter reset when the selected input capture event is detected in a channel in input capture mode with ICRST = 1.

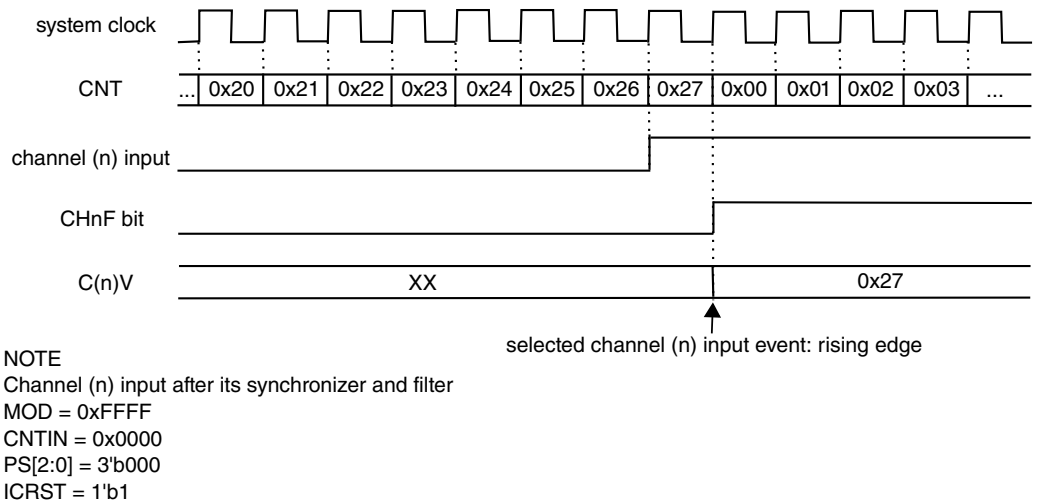


Figure 47-20. Example of the Input Capture mode with ICRST = 1

NOTE

- It is expected that the ICRST bit be set only when the channel is in input capture mode.
- In this case, if the FTM counter is reset, then the prescaler counter (Prescaler) and the TOF counter (When the TOF bit is set) also are reset.

47.5.5 Output Compare mode

The Output Compare mode is selected when:

- DECAPEN = 0
- COMBINE = 0
- CPWMS = 0, and
- MSnB:MSnA = 0:1

In Output Compare mode, the FTM can generate timed pulses with programmable position, polarity, duration, and frequency. When the counter matches the value in the CnV register of an output compare channel, the channel (n) output can be set, cleared, or toggled.

When a channel is initially configured to Toggle mode, the previous value of the channel output is held until the first output compare event occurs.

The CHnF bit is set and the channel (n) interrupt is generated if CHnIE = 1 at the channel (n) match (FTM counter = CnV).

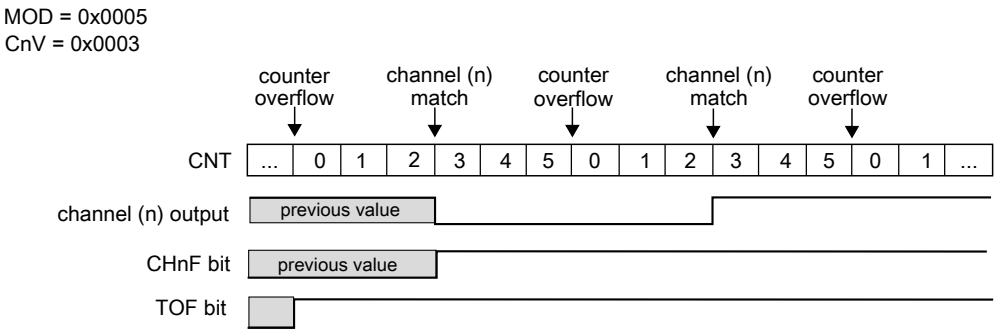


Figure 47-21. Example of the Output Compare mode when the match toggles the channel output

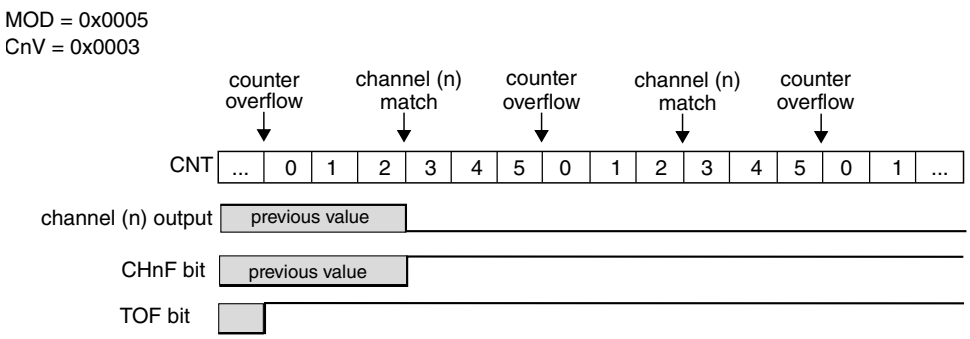


Figure 47-22. Example of the Output Compare mode when the match clears the channel output

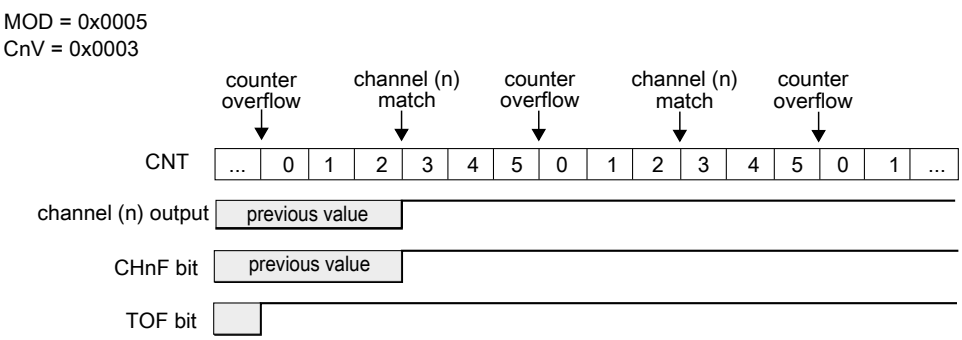


Figure 47-23. Example of the Output Compare mode when the match sets the channel output

If (ELSnB:ELSnA = 0:0) when the counter reaches the value in the CnV register, the CHnF bit is set and the channel (n) interrupt is generated if CHnIE = 1, however the channel (n) output is not modified and controlled by FTM.

47.5.6 Edge-Aligned PWM (EPWM) mode

The Edge-Aligned mode is selected when:

- QUADEN = 0

- DECAPEN = 0
- COMBINE = 0
- CPWMS = 0, and
- MSnB = 1

The EPWM period is determined by (MOD – CNTIN + 0x0001) and the pulse width (duty cycle) is determined by (CnV – CNTIN).

The CHnF bit is set and the channel (n) interrupt is generated if CHnIE = 1 at the channel (n) match (FTM counter = CnV), that is, at the end of the pulse width.

This type of PWM signal is called edge-aligned because the leading edges of all PWM signals are aligned with the beginning of the period, which is the same for all channels within an FTM.

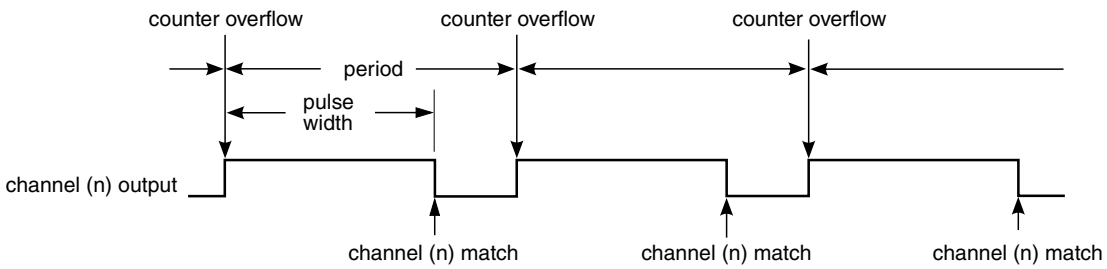


Figure 47-24. EPWM period and pulse width with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = 0:0) when the counter reaches the value in the CnV register, the CHnF bit is set and the channel (n) interrupt is generated if CHnIE = 1, however the channel (n) output is not controlled by FTM.

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced high at the counter overflow when the CNTIN register value is loaded into the FTM counter, and it is forced low at the channel (n) match (FTM counter = CnV). See the following figure.

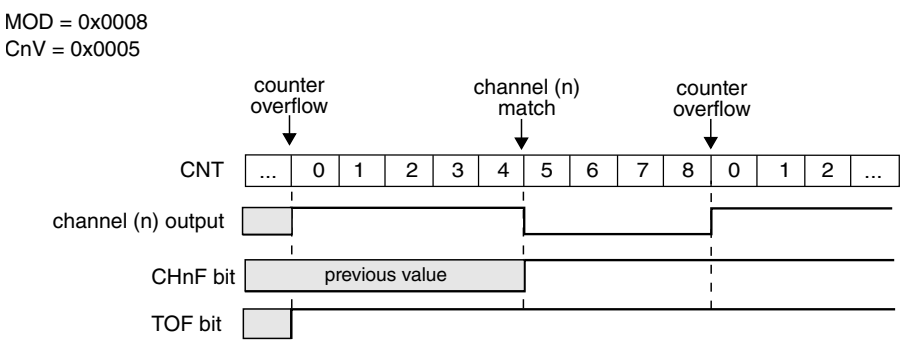


Figure 47-25. EPWM signal with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced low at the counter overflow when the CNTIN register value is loaded into the FTM counter, and it is forced high at the channel (n) match (FTM counter = CnV). See the following figure.

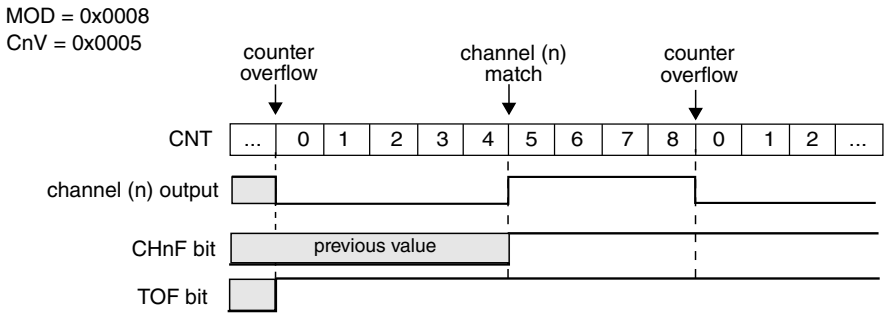


Figure 47-26. EPWM signal with ELSnB:ELSnA = X:1

If (CnV = 0x0000), then the channel (n) output is a 0% duty cycle EPWM signal and CHnF bit is not set even when there is the channel (n) match.

If (CnV > MOD), then the channel (n) output is a 100% duty cycle EPWM signal and CHnF bit is not set.Therefore, MOD must be less than 0xFFFF in order to get a 100% duty cycle EPWM signal.

Note

When CNTIN is different from zero the following EPWM signals can be generated:

- 0% EPWM signal if CnV = CNTIN,
- EPWM signal between 0% and 100% if CNTIN < CnV <= MOD,
- 100% EPWM signal when CNTIN > CnV or CnV > MOD.

47.5.7 Center-Aligned PWM (CPWM) mode

The Center-Aligned mode is selected when:

- QUADEN = 0
- DECAPEN = 0
- COMBINE = 0, and
- CPWMS = 1

The CPWM pulse width (duty cycle) is determined by 2 × (CnV − CNTIN) and the period is determined by 2 × (MOD − CNTIN). See the following figure. MOD must be kept in the range of 0x0001 to 0x7FFF because values outside this range can produce ambiguous results.

In the CPWM mode, the FTM counter counts up until it reaches MOD and then counts down until it reaches CNTIN.

The CHnF bit is set and channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (FTM counter = CnV) when the FTM counting is down (at the begin of the pulse width) and when the FTM counting is up (at the end of the pulse width).

This type of PWM signal is called center-aligned because the pulse width centers for all channels are aligned with the value of CNTIN.

The other channel modes are not compatible with the up-down counter (CPWMS = 1). Therefore, all FTM channels must be used in CPWM mode when (CPWMS = 1).

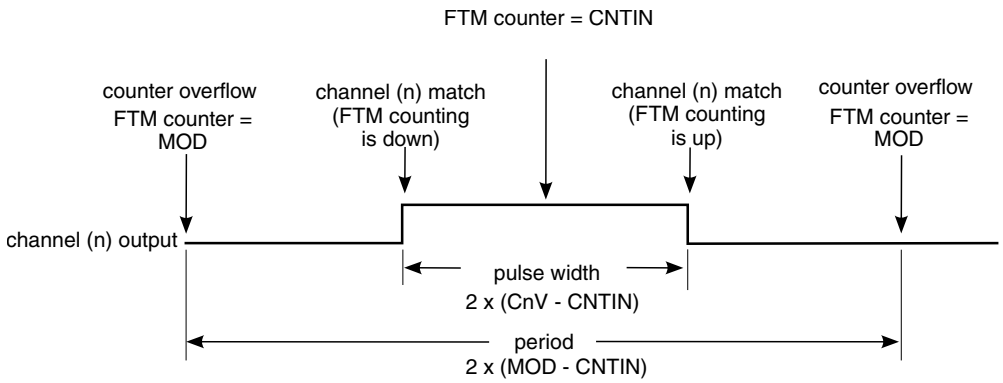


Figure 47-27. CPWM period and pulse width with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = 0:0) when the FTM counter reaches the value in the CnV register, the CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1), however the channel (n) output is not controlled by FTM.

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced high at the channel (n) match (FTM counter = CnV) when counting down, and it is forced low at the channel (n) match when counting up. See the following figure.

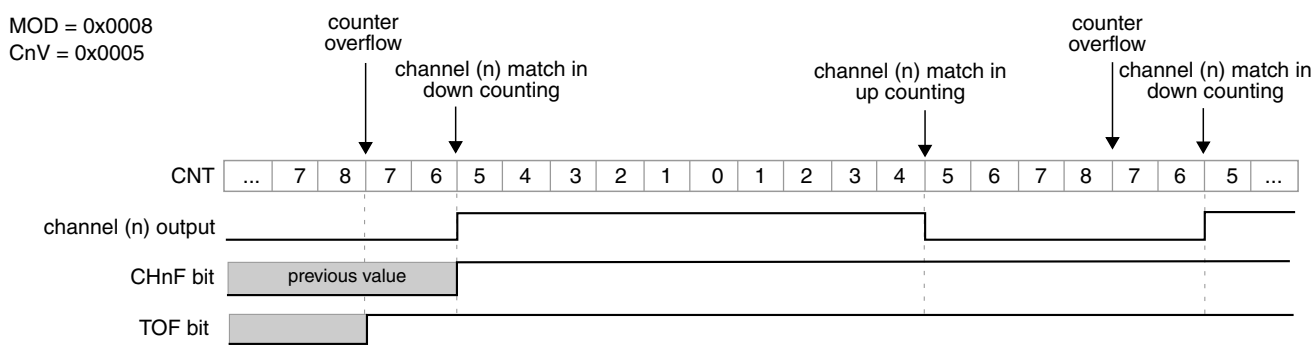


Figure 47-28. CPWM signal with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced low at the channel (n) match (FTM counter = CnV) when counting down, and it is forced high at the channel (n) match when counting up. See the following figure.

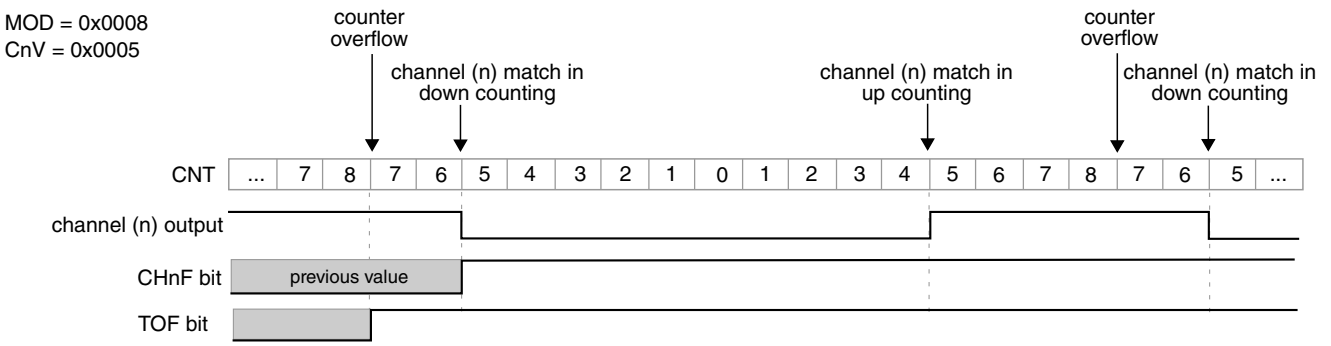


Figure 47-29. CPWM signal with ELSnB:ELSnA = X:1

If (CnV = 0x0000) or CnV is a negative value, that is (CnV[15] = 1), then the channel (n) output is a 0% duty cycle CPWM signal and CHnF bit is not set even when there is the channel (n) match.

If CnV is a positive value, that is (CnV[15] = 0), (CnV ≥ MOD), and (MOD ≠ 0x0000), then the channel (n) output is a 100% duty cycle CPWM signal and CHnF bit is not set even when there is the channel (n) match. This implies that the usable range of periods set by MOD is 0x0001 through 0x7FFE, 0x7FFF if you do not need to generate a 100% duty cycle CPWM signal. This is not a significant limitation because the resulting period is much longer than required for normal applications.

The CPWM mode must not be used when the FTM counter is a free running counter.

47.5.8 Combine mode

The Combine mode is selected when:

- QUADEN = 0
- DECAPEN = 0
- COMBINE = 1, and
- CPWMS = 0

In Combine mode, an even channel (n) and adjacent odd channel (n+1) are combined to generate a PWM signal in the channel (n) output.

In the Combine mode, the PWM period is determined by (MOD − CNTIN + 0x0001) and the PWM pulse width (duty cycle) is determined by (|C(n+1)V − C(n)V|).

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (FTM counter = C(n)V). The CH(n+1)F bit is set and the channel (n +1) interrupt is generated, if CH(n+1)IE = 1, at the channel (n+1) match (FTM counter = C(n+1)V).

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced low at the beginning of the period (FTM counter = CNTIN) and at the channel (n+1) match (FTM counter = C(n+1)V). It is forced high at the channel (n) match (FTM counter = C(n)V). See the following figure.

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced high at the beginning of the period (FTM counter = CNTIN) and at the channel (n+1) match (FTM counter = C(n+1)V). It is forced low at the channel (n) match (FTM counter = C(n)V). See the following figure.

In Combine mode, the ELS(n+1)B and ELS(n+1)A bits are not used in the generation of the channels (n) and (n+1) output. However, if (ELSnB:ELSnA = 0:0) then the channel (n) output is not controlled by FTM, and if (ELS(n+1)B:ELS(n+1)A = 0:0) then the channel (n+1) output is not controlled by FTM.

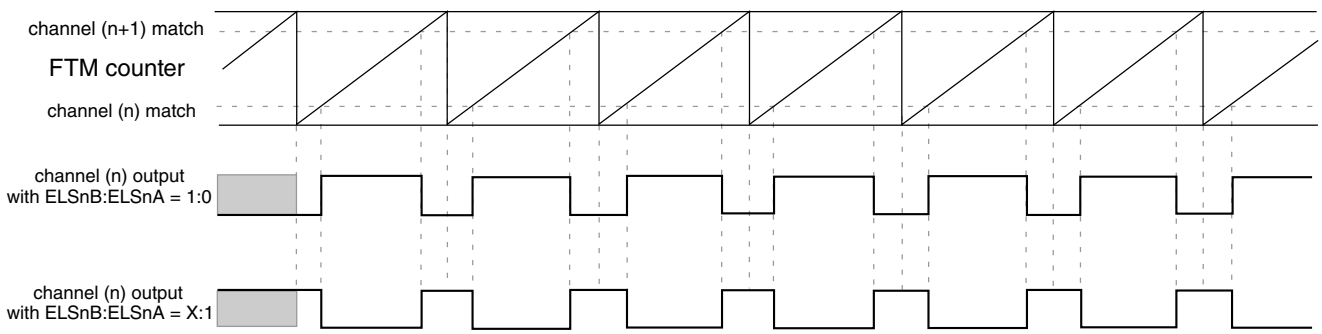


Figure 47-30. Combine mode

The following figures illustrate the PWM signals generation using Combine mode.

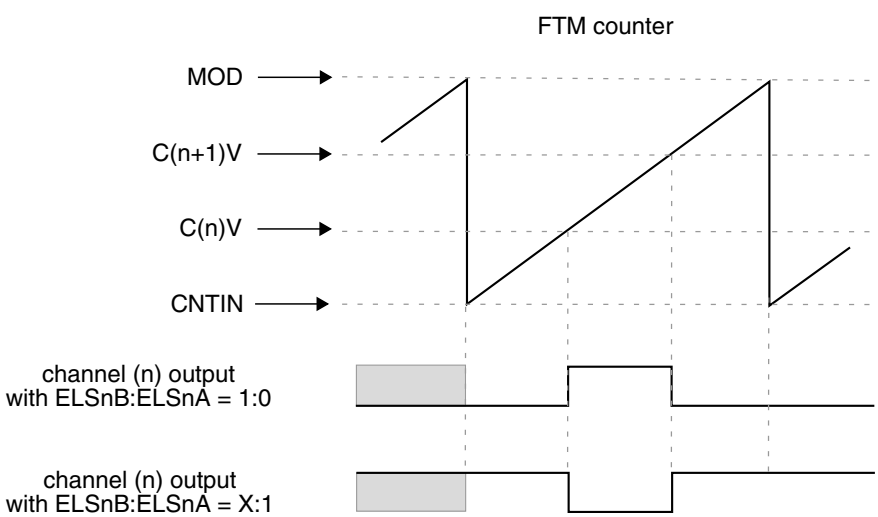


Figure 47-31. Channel (n) output if (CNTIN < C(n)V < MOD) and (CNTIN < C(n+1)V < MOD) and (C(n)V < C(n+1)V)

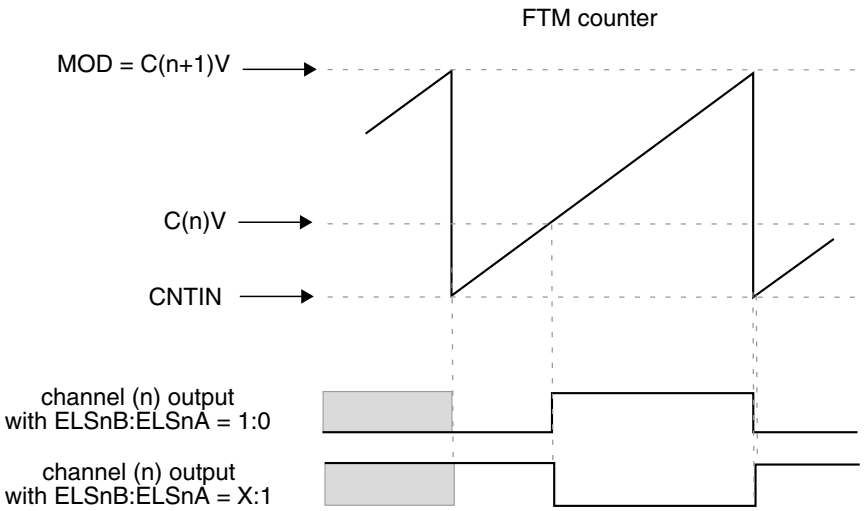


Figure 47-32. Channel (n) output if (CNTIN < C(n)V < MOD) and (C(n+1)V = MOD)

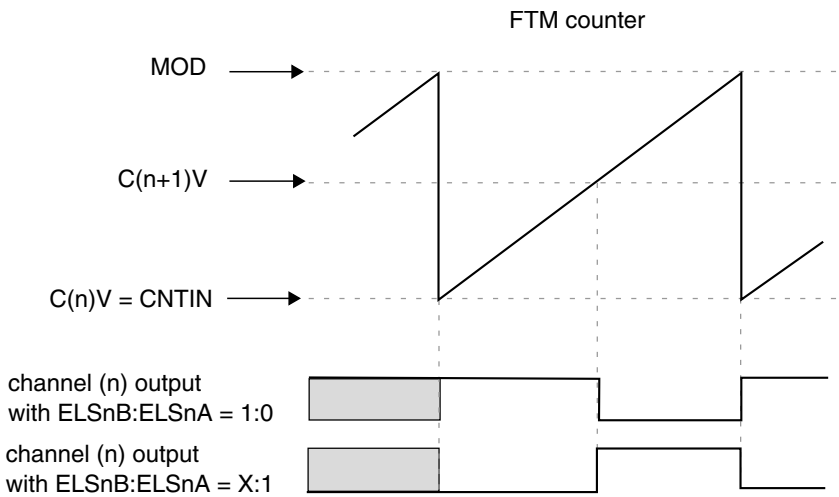


Figure 47-33. Channel (n) output if (C(n)V = CNTIN) and (CNTIN < C(n+1)V < MOD)

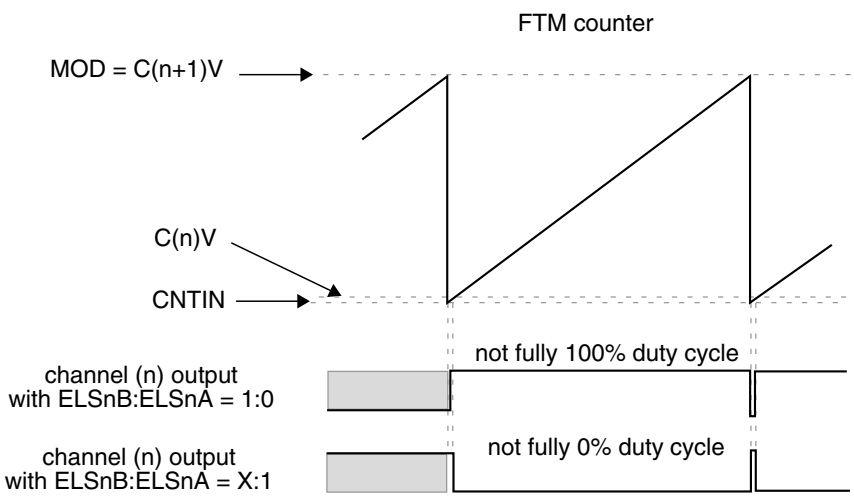


Figure 47-34. Channel (n) output if (CNTIN < C(n)V < MOD) and (C(n)V is Almost Equal to CNTIN) and (C(n+1)V = MOD)

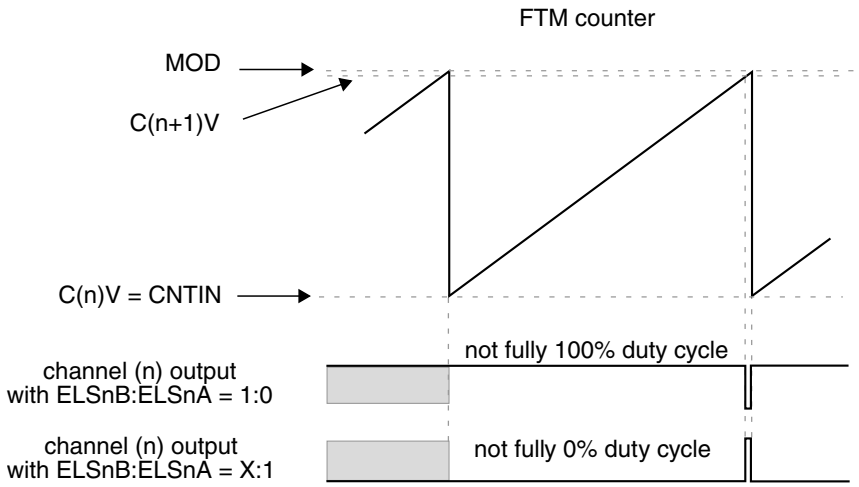


Figure 47-35. Channel (n) output if (C(n)V = CNTIN) and (CNTIN < C(n+1)V < MOD) and (C(n+1)V is Almost Equal to MOD)

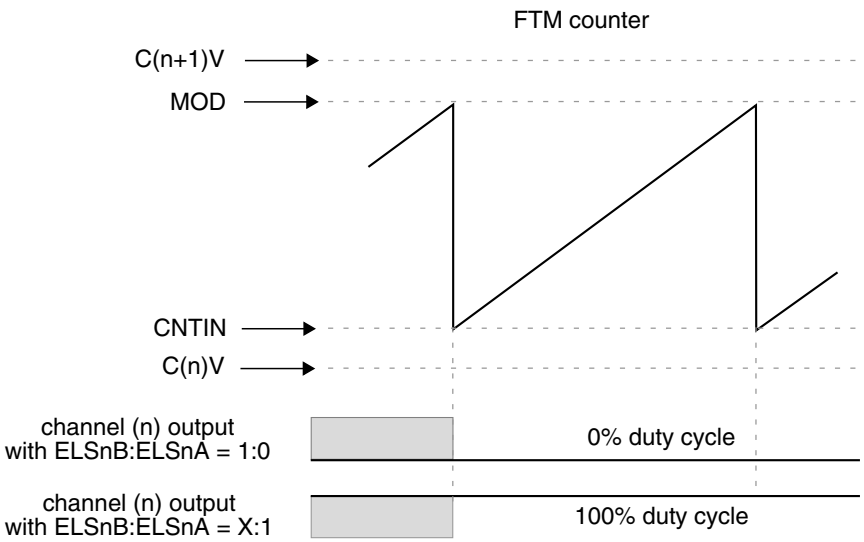


Figure 47-36. Channel (n) output if C(n)V and C(n+1)V are not between CNTIN and MOD

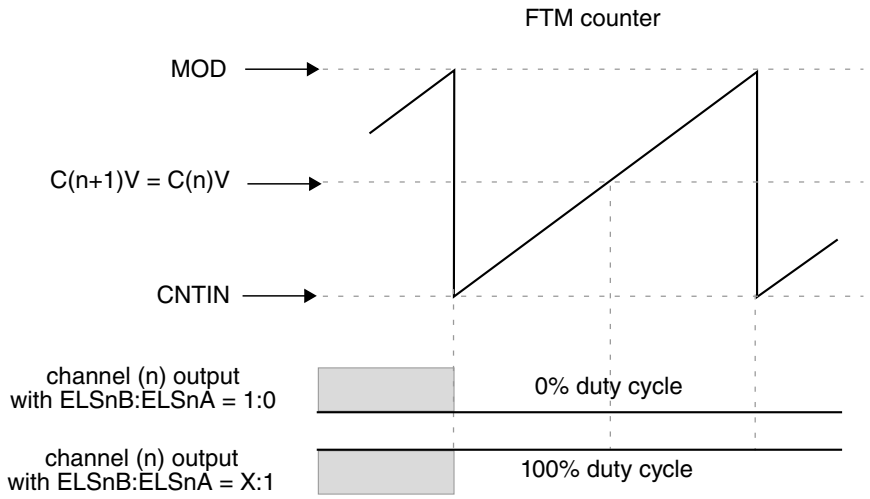


Figure 47-37. Channel (n) output if (CNTIN < C(n)V < MOD) and (CNTIN < C(n+1)V < MOD) and (C(n)V = C(n+1)V)

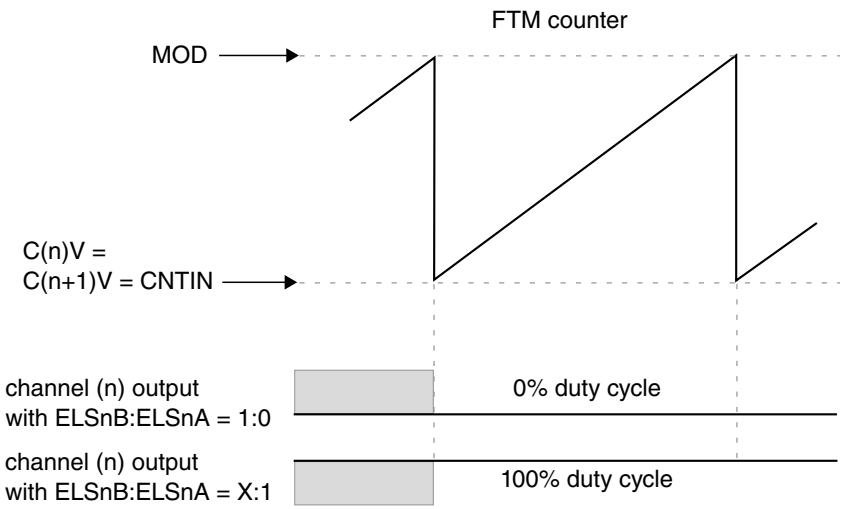


Figure 47-38. Channel (n) output if (C(n)V = C(n+1)V = CNTIN)

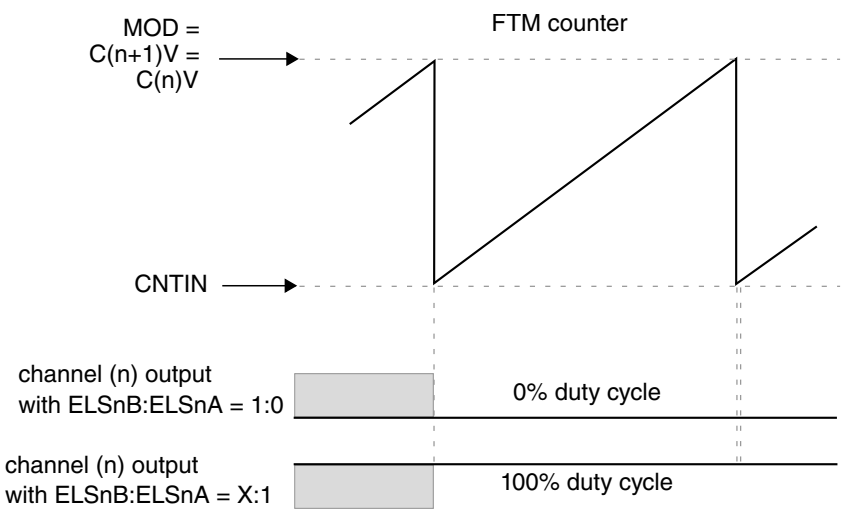


Figure 47-39. Channel (n) output if (C(n)V = C(n+1)V = MOD)

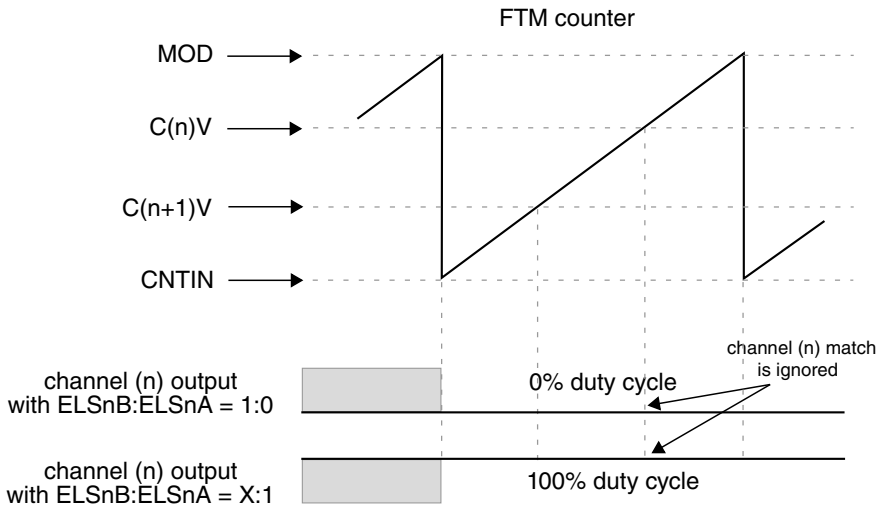


Figure 47-40. Channel (n) output if (CNTIN < C(n)V < MOD) and (CNTIN < C(n+1)V < MOD) and (C(n)V > C(n+1)V)

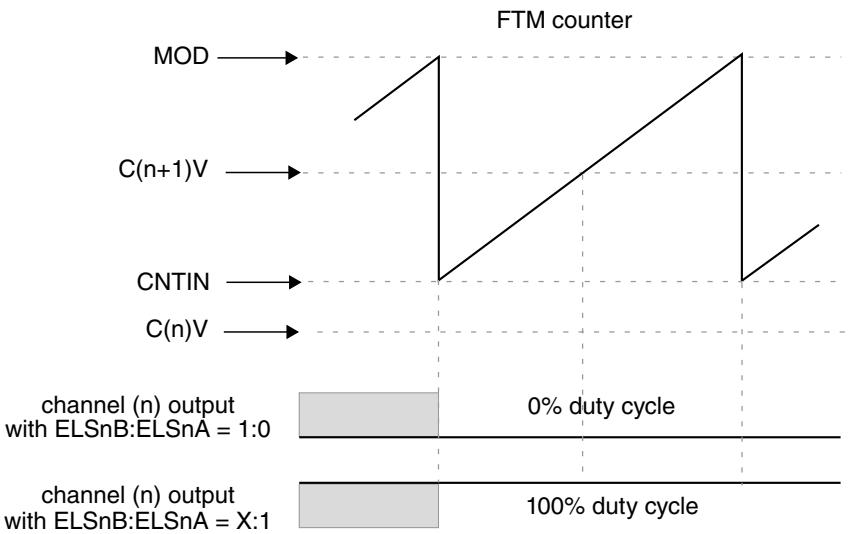


Figure 47-41. Channel (n) output if (C(n)V < CNTIN) and (CNTIN < C(n+1)V < MOD)

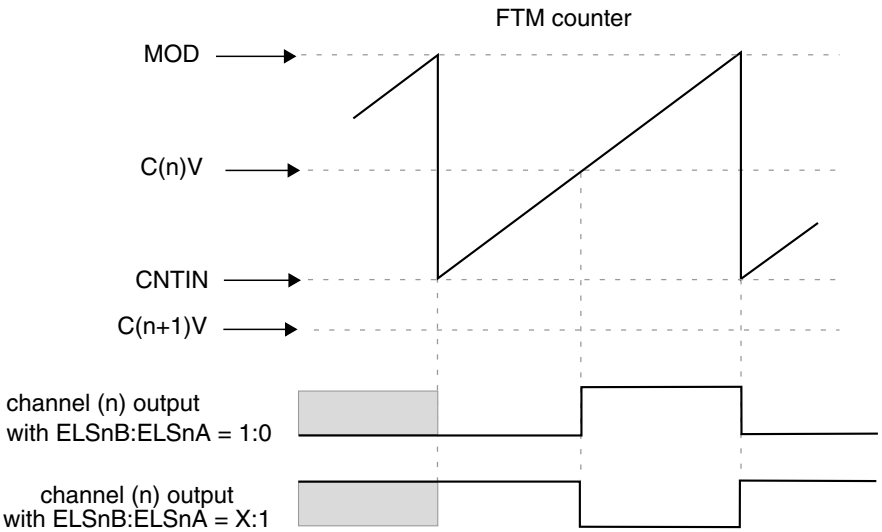


Figure 47-42. Channel (n) output if (C(n+1)V < CNTIN) and (CNTIN < C(n)V < MOD)

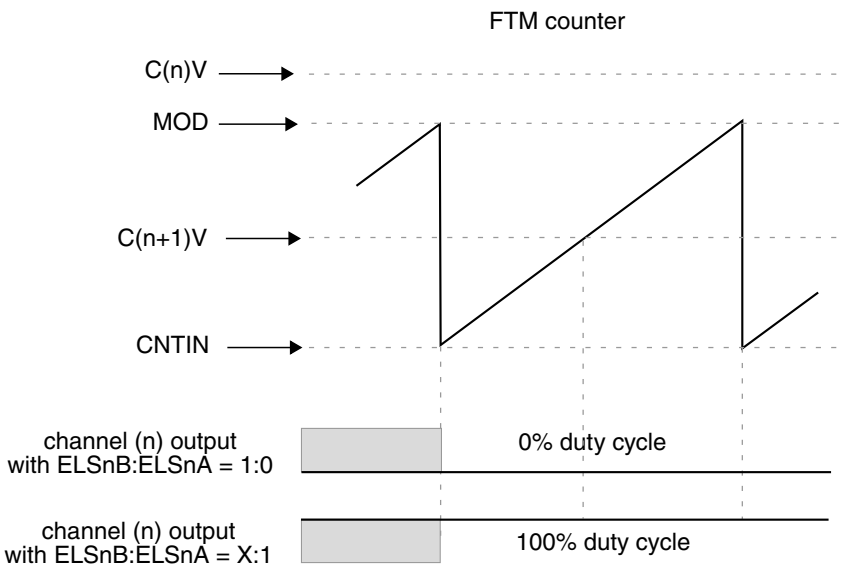


Figure 47-43. Channel (n) output if (C(n)V > MOD) and (CNTIN < C(n+1)V < MOD)

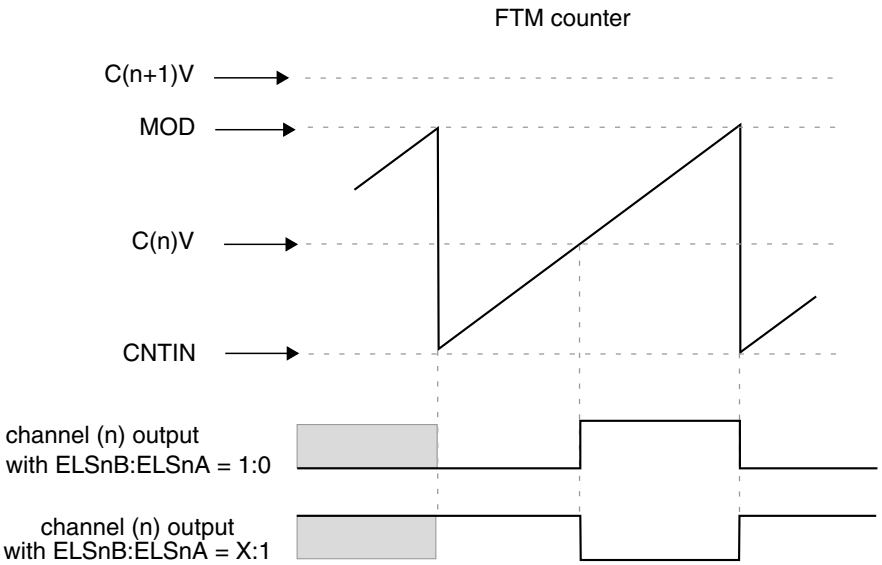


Figure 47-44. Channel (n) output if (C(n+1)V > MOD) and (CNTIN < C(n)V < MOD)

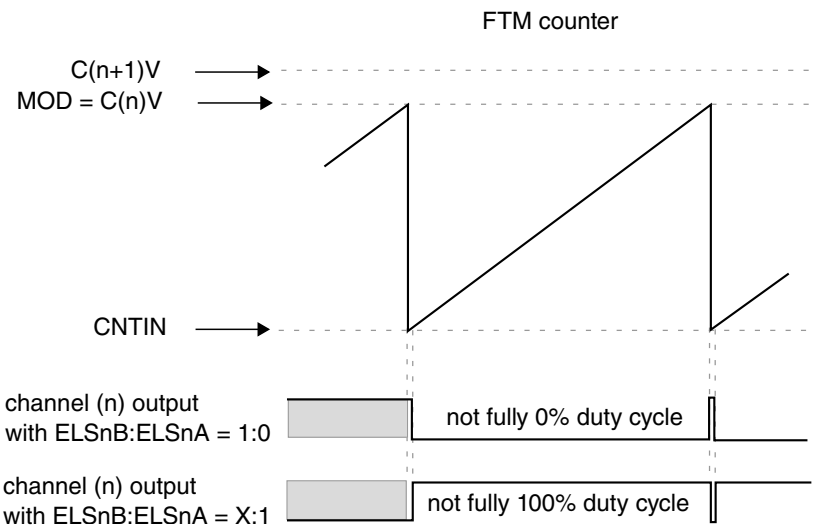


Figure 47-45. Channel (n) output if (C(n+1)V > MOD) and (CNTIN < C(n)V = MOD)

47.5.8.1 Asymmetrical PWM

In Combine mode, the control of the PWM signal first edge, when the channel (n) match occurs, that is, FTM counter = C(n)V, is independent of the control of the PWM signal second edge, when the channel (n+1) match occurs, that is, FTM counter = C(n+1)V. So, Combine mode allows the generation of asymmetrical PWM signals.

47.5.9 Complementary mode

The Complementary mode is selected when:

- QUADEN = 0
- DECAPEN = 0
- COMP = 1

In Complementary mode, the channel (n+1) output is the inverse of the channel (n) output.

So, the channel (n+1) output is the same as the channel (n) output when:

- QUADEN = 0
- DECAPEN = 0
- COMP = 0

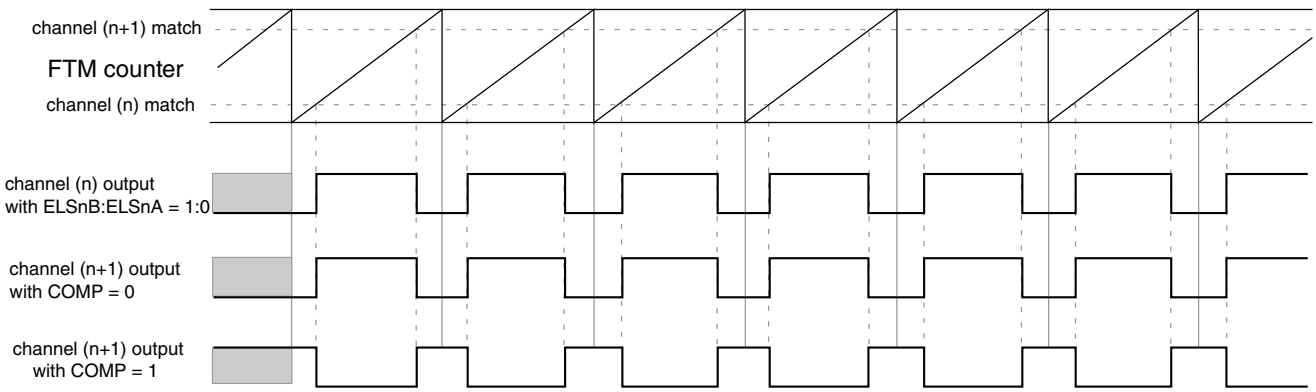


Figure 47-46. Channel (n+1) output in Complementary mode with (ELSnB:ELSnA = 1:0)

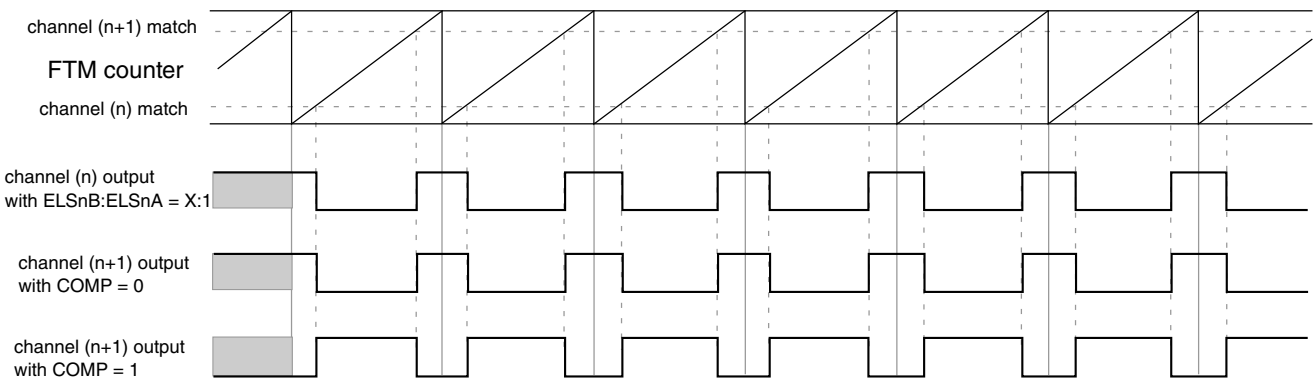


Figure 47-47. Channel (n+1) output in Complementary mode with (ELSnB:ELSnA = X:1)

NOTE

The complementary mode is not available in Output Compare mode.

47.5.10 Registers updated from write buffers

47.5.10.1 CNTIN register update

The following table describes when CNTIN register is updated:

Table 47-6. CNTIN register update

When	Then CNTIN register is updated
CLKS[1:0] = 0:0	When CNTIN register is written, independent of FTMEN bit.
• FTMEN = 0, or • CNTINC = 0	At the next system clock after CNTIN was written.
• FTMEN = 1, • SYNCMODE = 1, and • CNTINC = 1	By the CNTIN register synchronization.

47.5.10.2 MOD register update

The following table describes when MOD register is updated:

Table 47-7. MOD register update

When	Then MOD register is updated
CLKS[1:0] = 0:0	When MOD register is written, independent of FTMEN bit.
• CLKS[1:0] ≠ 0:0, and • FTMEN = 0	According to the CPWMS bit, that is: • If the selected mode is not CPWM then MOD register is updated after MOD register was written and the FTM counter changes from MOD to CNTIN. If the FTM counter is at free-running counter mode then this update occurs when the FTM counter changes from 0xFFFF to 0x0000. • If the selected mode is CPWM then MOD register is updated after MOD register was written and the FTM counter changes from MOD to (MOD – 0x0001).
• CLKS[1:0] ≠ 0:0, and • FTMEN = 1	By the MOD register synchronization.

47.5.10.3 CnV register update

The following table describes when CnV register is updated:

Table 47-8. CnV register update

When	Then CnV register is updated
CLKS[1:0] = 0:0	When CnV register is written, independent of FTMEN bit.
• CLKS[1:0] ≠ 0:0, and • FTMEN = 0	According to the selected mode, that is:

Table continues on the next page...

Table 47-8. CnV register update (continued)

When	Then CnV register is updated
	• If the selected mode is Output Compare, then CnV register is updated on the next FTM counter change, end of the prescaler counting, after CnV register was written. • If the selected mode is EPWM, then CnV register is updated after CnV register was written and the FTM counter changes from MOD to CNTIN. If the FTM counter is at free-running counter mode then this update occurs when the FTM counter changes from 0xFFFF to 0x0000. • If the selected mode is CPWM, then CnV register is updated after CnV register was written and the FTM counter changes from MOD to (MOD – 0x0001).
• CLKS[1:0] ≠ 0:0, and • FTMEN = 1	According to the selected mode, that is: • If the selected mode is output compare then CnV register is updated according to the SYNCEN bit. If (SYNCEN = 0) then CnV register is updated after CnV register was written at the next change of the FTM counter, the end of the prescaler counting. If (SYNCEN = 1) then CnV register is updated by the C(n)V and C(n+1)V register synchronization. • If the selected mode is not output compare and (SYNCEN = 1) then CnV register is updated by the C(n)V and C(n+1)V register synchronization.

47.5.11 PWM synchronization

The PWM synchronization provides an opportunity to update the MOD, CNTIN, CnV, OUTMASK, INVCTRL and SWOCTRL registers with their buffered value and force the FTM counter to the CNTIN register value.

Note

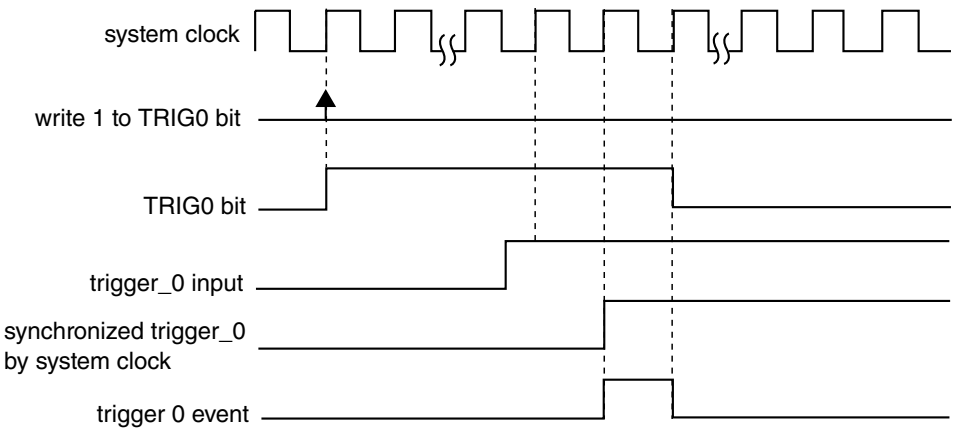
The legacy PWM synchronization (SYNCMODE = 0) is a subset of the enhanced PWM synchronization (SYNCMODE = 1). Thus, only the enhanced PWM synchronization must be used.

47.5.11.1 Hardware trigger

Three hardware trigger signal inputs of the FTM module are enabled when TRIGn = 1, where n = 0, 1 or 2 corresponding to each one of the input signals, respectively. The hardware trigger input n is synchronized by the system clock. The PWM synchronization with hardware trigger is initiated when a rising edge is detected at the enabled hardware trigger inputs.

If (HWTRIGMODE = 0) then the TRIGn bit is cleared when 0 is written to it or when the trigger n event is detected.

In this case, if two or more hardware triggers are enabled (for example, TRIG0 and TRIG1 = 1) and only trigger 1 event occurs, then only TRIG1 bit is cleared. If a trigger n event occurs together with a write setting TRIGn bit, then the synchronization is initiated, but TRIGn bit remains set due to the write operation.



Note
All hardware trigger inputs have the same behavior.

Figure 47-48. Hardware trigger event with HWTRIGMODE = 0

If HWTRIGMODE = 1, then the TRIGn bit is only cleared when 0 is written to it.

NOTE

The HWTRIGMODE bit must be 1 only with enhanced PWM synchronization (SYNCMODE = 1).

47.5.11.2 Software trigger

A software trigger event occurs when 1 is written to the SYNC[SWSYNC] bit. The SWSYNC bit is cleared when 0 is written to it or when the PWM synchronization, initiated by the software event, is completed.

If another software trigger event occurs (by writing another 1 to the SWSYNC bit) at the same time the PWM synchronization initiated by the previous software trigger event is ending, a new PWM synchronization is started and the SWSYNC bit remains equal to 1.

If SYNCMODE = 0 then the SWSYNC bit is also cleared by FTM according to PWMSYNC and REINIT bits. In this case if (PWMSYNC = 1) or (PWMSYNC = 0 and REINIT = 0) then SWSYNC bit is cleared at the next selected loading point after that the software trigger event occurred; see Boundary cycle and loading points and the following figure. If (PWMSYNC = 0) and (REINIT = 1) then SWSYNC bit is cleared when the software trigger event occurs.

If SYNCMODE = 1 then the SWSYNC bit is also cleared by FTM according to the SWRSTCNT bit. If SWRSTCNT = 0 then SWSYNC bit is cleared at the next selected loading point after that the software trigger event occurred; see the following figure. If SWRSTCNT = 1 then SWSYNC bit is cleared when the software trigger event occurs.

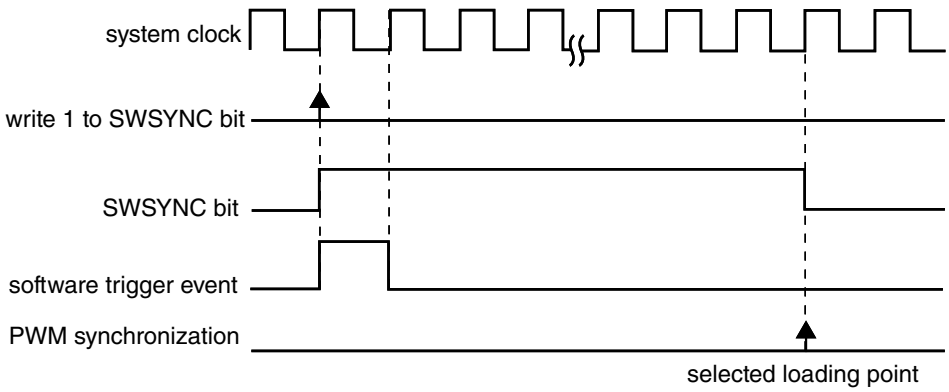


Figure 47-49. Software trigger event

47.5.11.3 Boundary cycle and loading points

The boundary cycle definition is important for the loading points for the registers MOD, CNTIN, and C(n)V.

In Up counting mode, the boundary cycle is defined as when the counter wraps to its initial value (CNTIN). If in Up-down counting mode, then the boundary cycle is defined as when the counter turns from down to up counting and when from up to down counting.

The following figure shows the boundary cycles and the loading points for the registers. In the Up Counting mode, the loading points are enabled if one of CNTMIN or CTMAX bits are 1. In the Up-Down Counting mode, the loading points are selected by CNTMIN and CNTMAX bits, as indicated in the figure. These loading points are safe places for register updates thus allowing a smooth transitions in PWM waveform generation.

For both counting modes, if neither CNTMIN nor CNTMAX are 1, then the boundary cycles are not used as loading points for registers updates. See the register synchronization descriptions in the following sections for details.

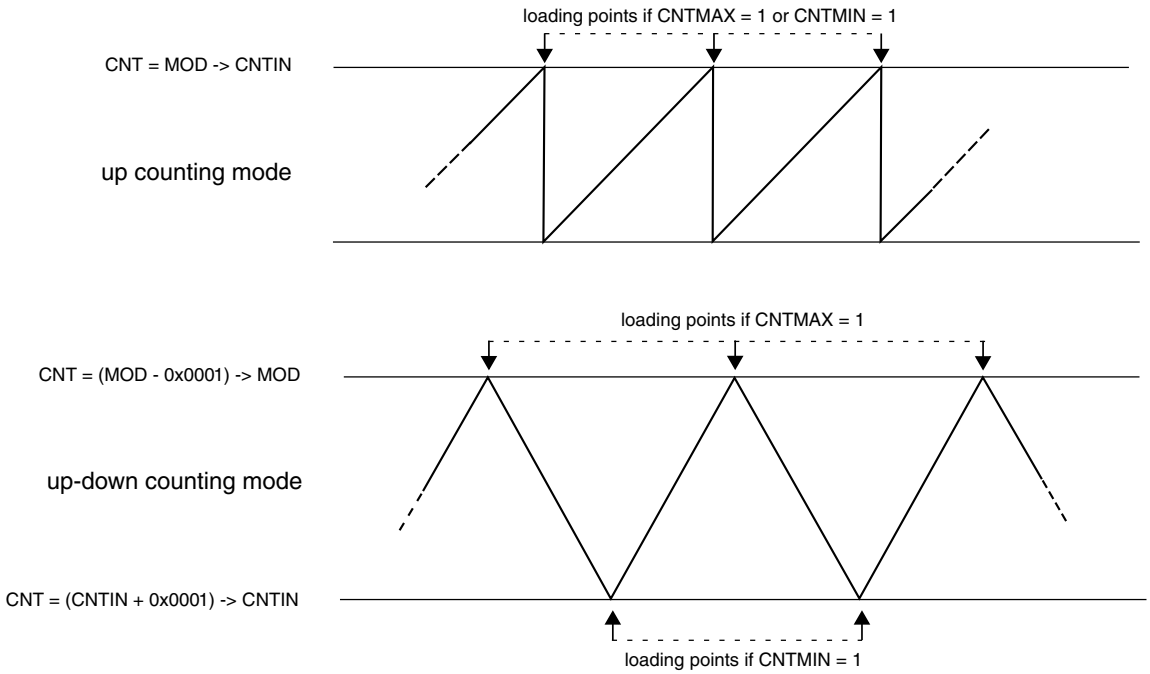


Figure 47-50. Boundary cycles and loading points

47.5.11.4 MOD register synchronization

The MOD register synchronization updates the MOD register with its buffer value. This synchronization is enabled if (FTMEN = 1).

The MOD register synchronization can be done by either the enhanced PWM synchronization (SYNCMODE = 1) or the legacy PWM synchronization (SYNCMODE = 0). However, it is expected that the MOD register be synchronized only by the enhanced PWM synchronization.

In the case of enhanced PWM synchronization, the MOD register synchronization depends on SWWRBUF, SWRSTCNT, HWWRBUF, and HWRSTCNT bits according to this flowchart:

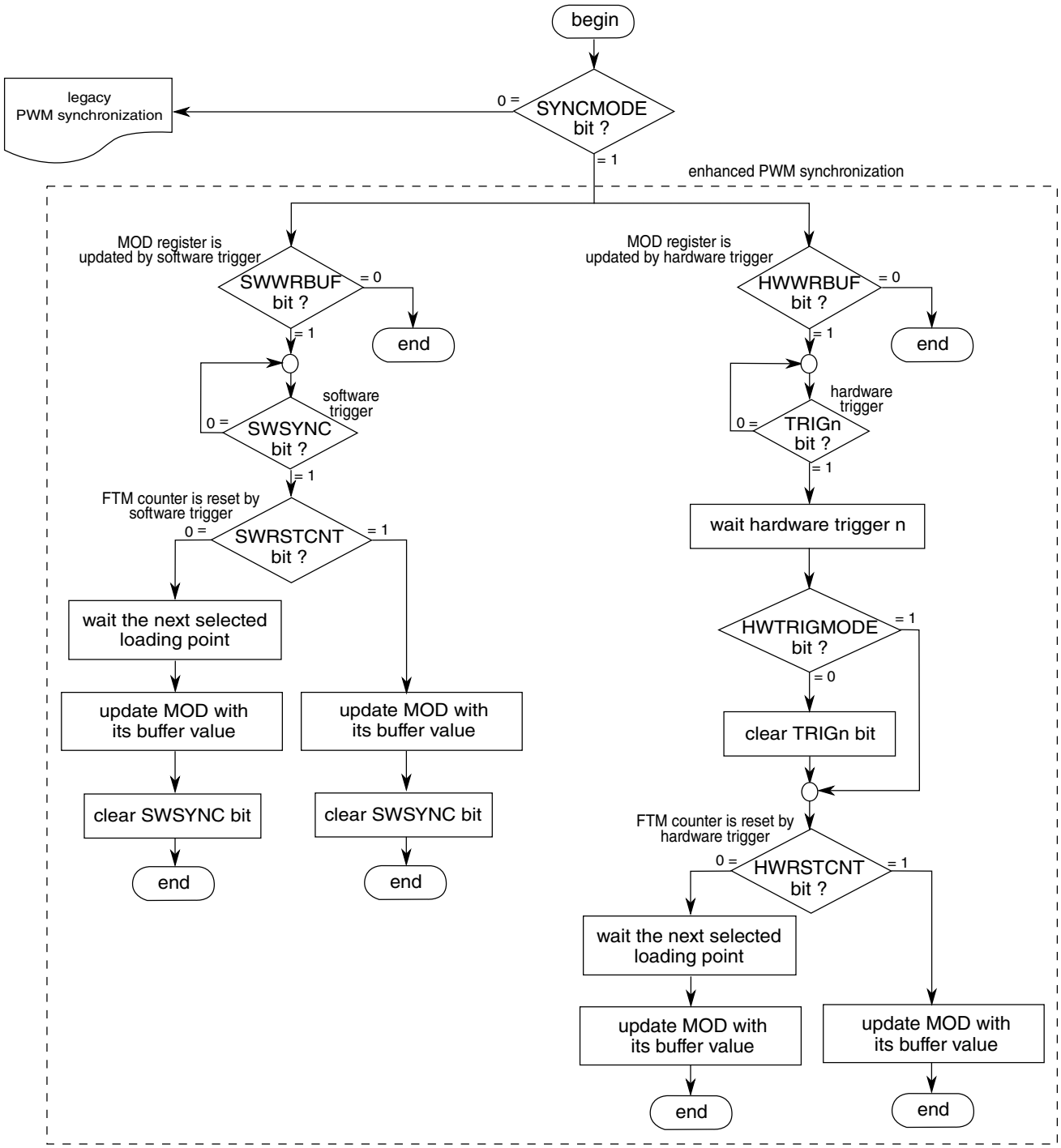


Figure 47-51. MOD register synchronization flowchart

In the case of legacy PWM synchronization, the MOD register synchronization depends on PWMSYNC and REINIT bits according to the following description.

If (SYNCMODE = 0), (PWMSYNC = 0), and (REINIT = 0), then this synchronization is made on the next selected loading point after an enabled trigger event takes place. If the trigger event was a software trigger, then the SWSYNC bit is cleared on the next selected

loading point. If the trigger event was a hardware trigger, then the trigger enable bit (TRIGn) is cleared according to Hardware trigger. Examples with software and hardware triggers follow.

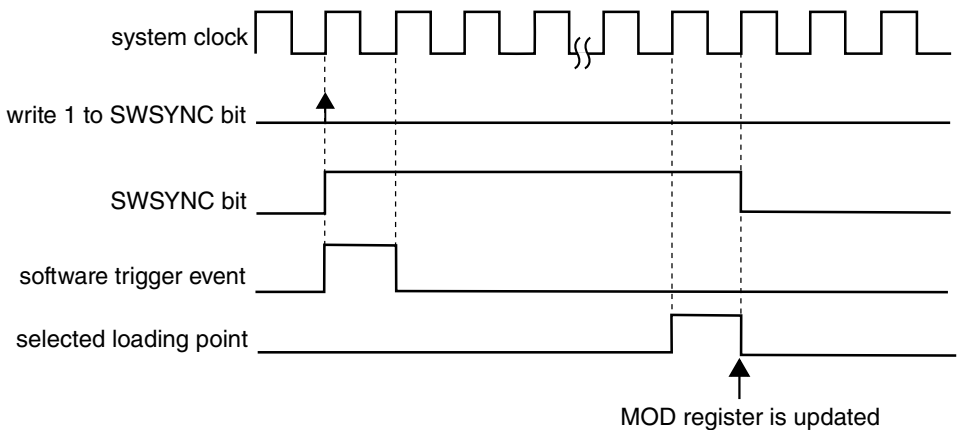


Figure 47-52. MOD synchronization with (SYNCMODE = 0), (PWMSYNC = 0), (REINIT = 0), and software trigger was used

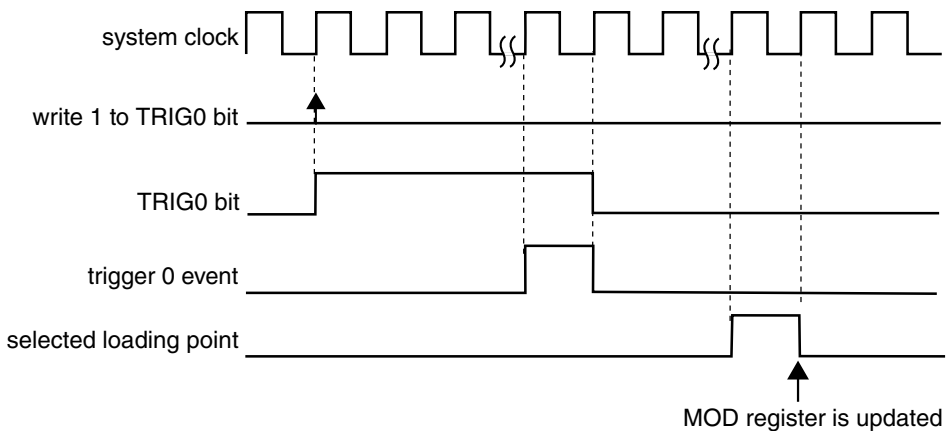


Figure 47-53. MOD synchronization with (SYNCMODE = 0), (HWTRIGMODE = 0), (PWMSYNC = 0), (REINIT = 0), and a hardware trigger was used

If (SYNCMODE = 0), (PWMSYNC = 0), and (REINIT = 1), then this synchronization is made on the next enabled trigger event. If the trigger event was a software trigger, then the SWSYNC bit is cleared according to the following example. If the trigger event was a hardware trigger, then the TRIGn bit is cleared according to Hardware trigger. Examples with software and hardware triggers follow.

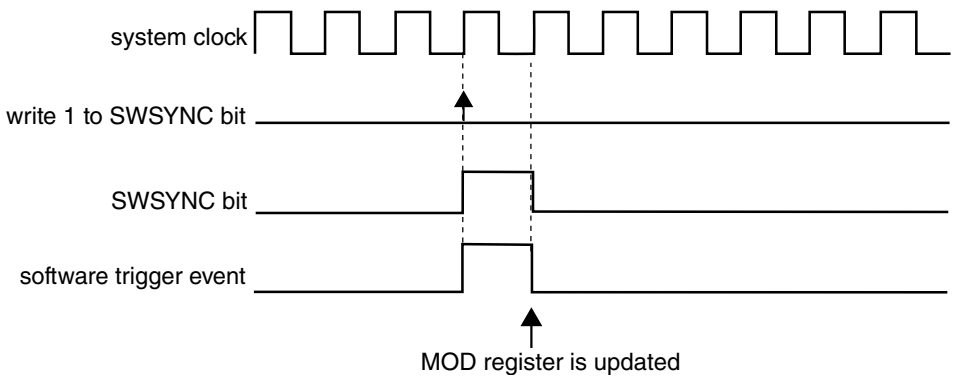


Figure 47-54. MOD synchronization with (SYNCMODE = 0), (PWMSYNC = 0), (REINIT = 1), and software trigger was used

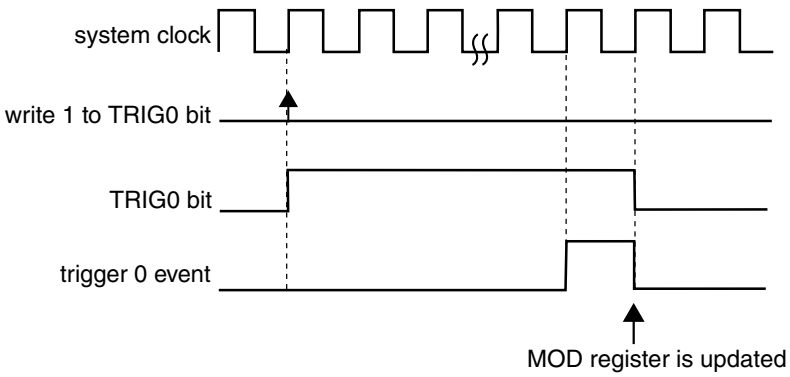


Figure 47-55. MOD synchronization with (SYNCMODE = 0), (HWTRIGMODE = 0), (PWMSYNC = 0), (REINIT = 1), and a hardware trigger was used

If (SYNCMODE = 0) and (PWMSYNC = 1), then this synchronization is made on the next selected loading point after the software trigger event takes place. The SWSYNC bit is cleared on the next selected loading point:

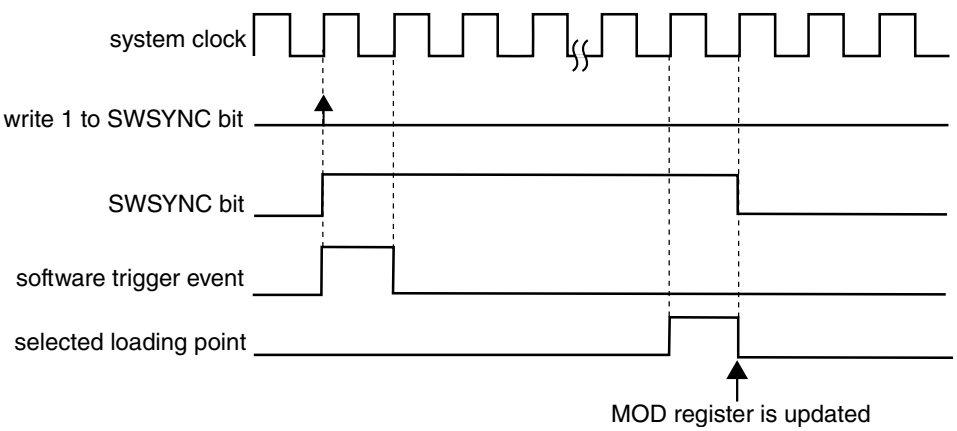


Figure 47-56. MOD synchronization with (SYNCMODE = 0) and (PWMSYNC = 1)

47.5.11.5 CNTIN register synchronization

The CNTIN register synchronization updates the CNTIN register with its buffer value.

This synchronization is enabled if (FTMEN = 1), (SYNCMODE = 1), and (CNTINC = 1). The CNTIN register synchronization can be done only by the enhanced PWM synchronization (SYNCMODE = 1). The synchronization mechanism is the same as the MOD register synchronization done by the enhanced PWM synchronization; see MOD register synchronization.

47.5.11.6 C(n)V and C(n+1)V register synchronization

The C(n)V and C(n+1)V registers synchronization updates the C(n)V and C(n+1)V registers with their buffer values.

This synchronization is enabled if (FTMEN = 1) and (SYNCEN = 1). The synchronization mechanism is the same as the MOD register synchronization. However, it is expected that the C(n)V and C(n+1)V registers be synchronized only by the enhanced PWM synchronization (SYNCMODE = 1).

47.5.11.7 OUTMASK register synchronization

The OUTMASK register synchronization updates the OUTMASK register with its buffer value.

The OUTMASK register can be updated at each rising edge of system clock (SYNCHOM = 0), by the enhanced PWM synchronization (SYNCHOM = 1 and SYNCMODE = 1) or by the legacy PWM synchronization (SYNCHOM = 1 and SYNCMODE = 0). However, it is expected that the OUTMASK register be synchronized only by the enhanced PWM synchronization.

In the case of enhanced PWM synchronization, the OUTMASK register synchronization depends on SWOM and HWOM bits. See the following flowchart:

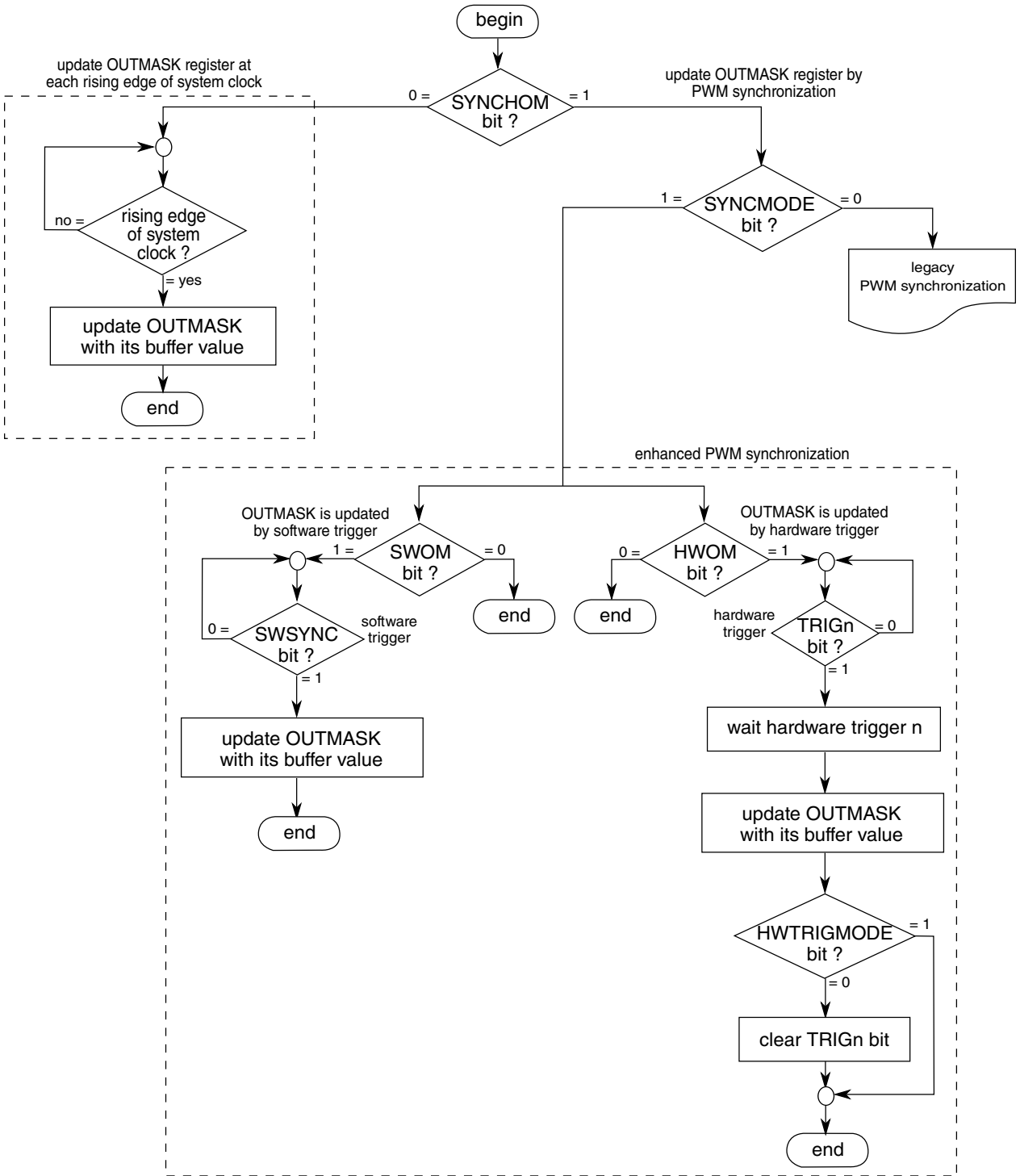


Figure 47-57. OUTMASK register synchronization flowchart

In the case of legacy PWM synchronization, the OUTMASK register synchronization depends on PWMSYNC bit according to the following description.

If (SYNCMODE = 0), (SYNCHOM = 1), and (PWMSYNC = 0), then this synchronization is done on the next enabled trigger event. If the trigger event was a software trigger, then the SWSYNC bit is cleared on the next selected loading point. If the trigger event was a hardware trigger, then the TRIGn bit is cleared according to Hardware trigger. Examples with software and hardware triggers follow.

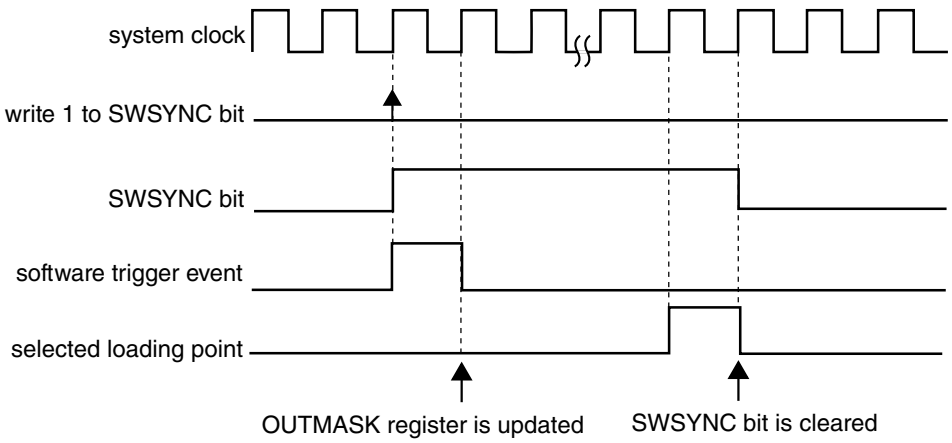


Figure 47-58. OUTMASK synchronization with (SYNCMODE = 0), (SYNCHOM = 1), (PWMSYNC = 0) and software trigger was used

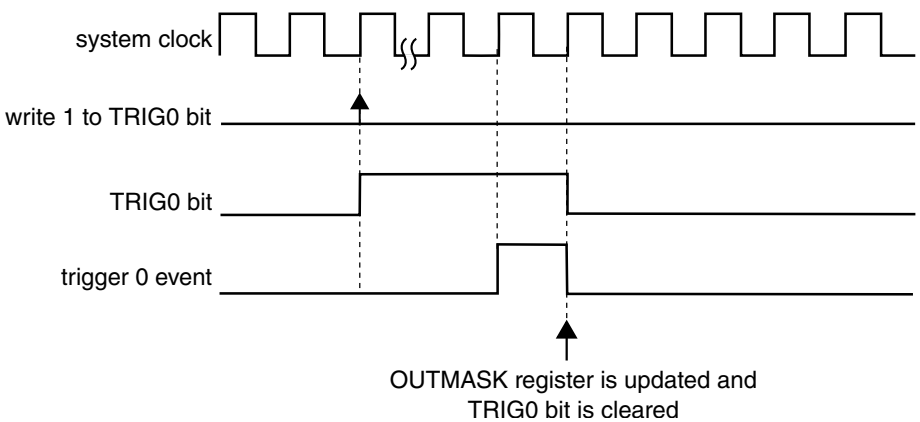


Figure 47-59. OUTMASK synchronization with (SYNCMODE = 0), (HWTRIGMODE = 0), (SYNCHOM = 1), (PWMSYNC = 0), and a hardware trigger was used

If (SYNCMODE = 0), (SYNCHOM = 1), and (PWMSYNC = 1), then this synchronization is made on the next enabled hardware trigger. The TRIGn bit is cleared according to Hardware trigger. An example with a hardware trigger follows.

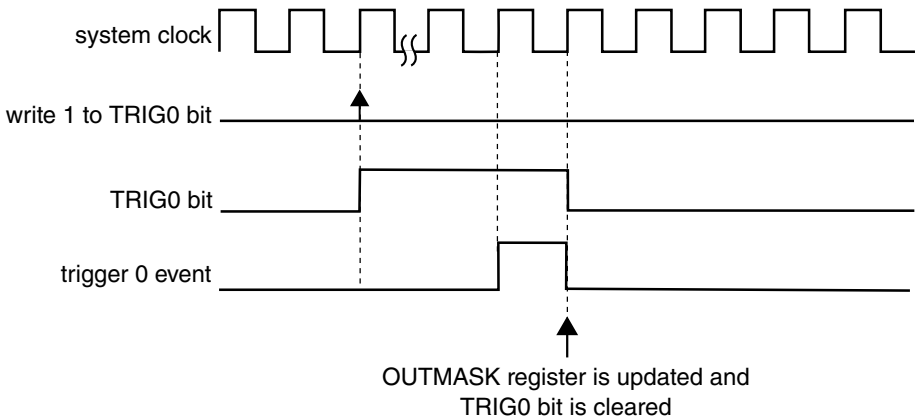


Figure 47-60. OUTMASK synchronization with (SYNCMODE = 0), (HWTRIGMODE = 0), (SYNCHOM = 1), (PWMSYNC = 1), and a hardware trigger was used

47.5.11.8 INVCTRL register synchronization

The INVCTRL register synchronization updates the INVCTRL register with its buffer value.

The INVCTRL register can be updated at each rising edge of system clock (INVC = 0) or by the enhanced PWM synchronization (INVC = 1 and SYNCMODE = 1) according to the following flowchart.

In the case of enhanced PWM synchronization, the INVCTRL register synchronization depends on SWINVC and HWINVC bits.

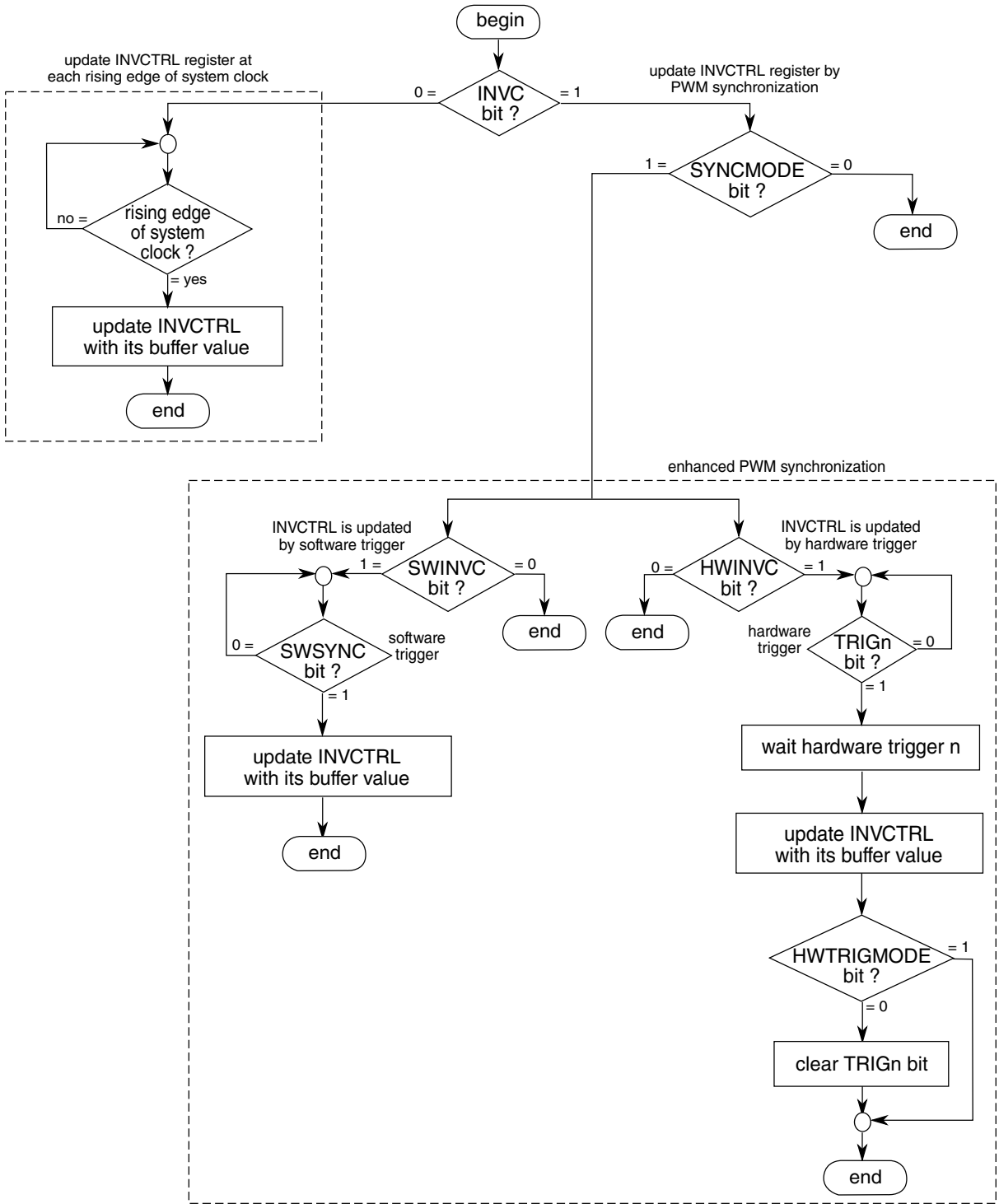


Figure 47-61. INVCTRL register synchronization flowchart

47.5.11.9 SWOCTRL register synchronization

The SWOCTRL register synchronization updates the SWOCTRL register with its buffer value.

The SWOCTRL register can be updated at each rising edge of system clock (SWOC = 0) or by the enhanced PWM synchronization (SWOC = 1 and SYNCMODE = 1) according to the following flowchart.

In the case of enhanced PWM synchronization, the SWOCTRL register synchronization depends on SWSOC and HWSOC bits.

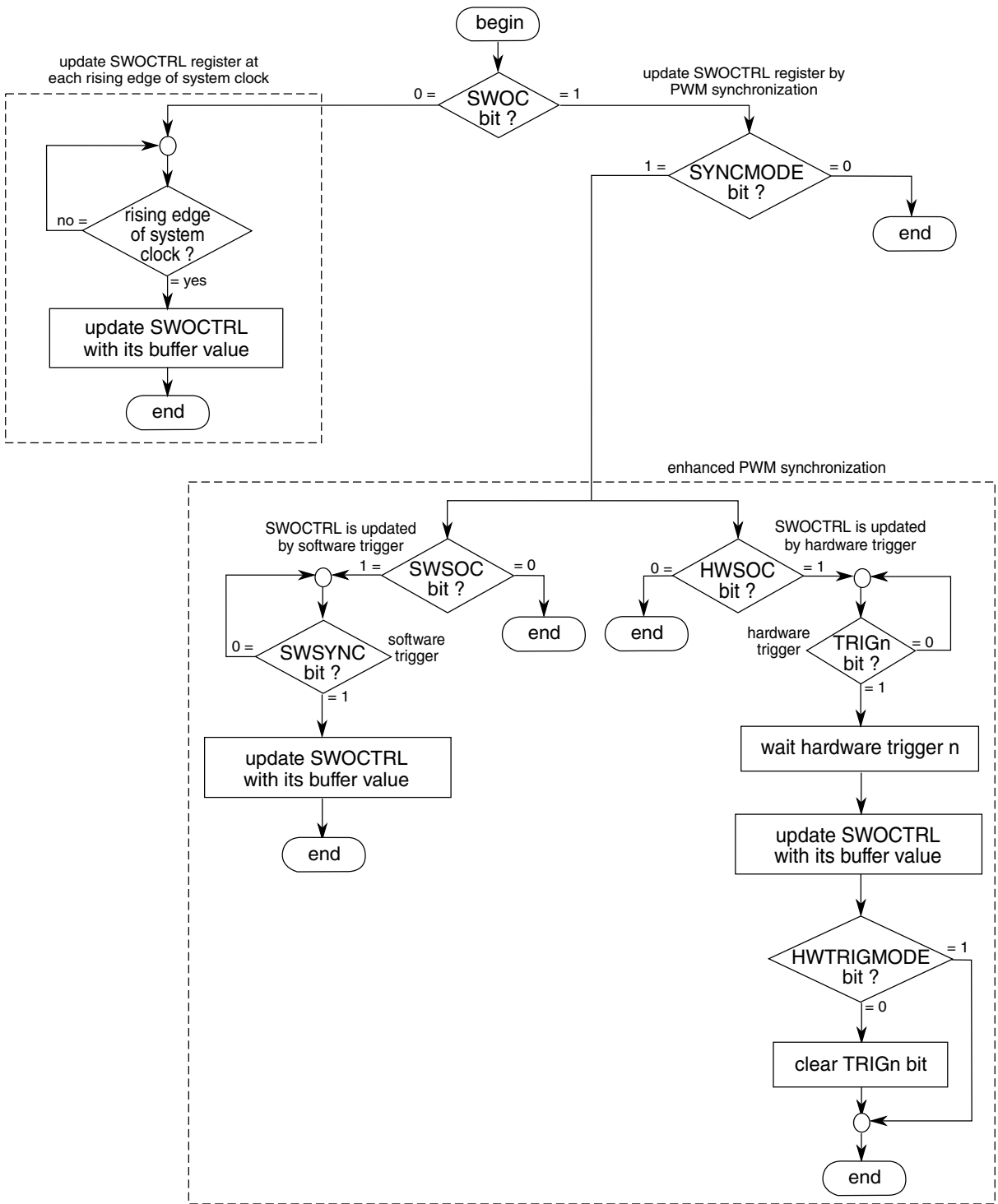


Figure 47-62. SWOCTRL register synchronization flowchart

47.5.11.10 FTM counter synchronization

The FTM counter synchronization is a mechanism that allows the FTM to restart the PWM generation at a certain point in the PWM period. The channels outputs are forced to their initial value, except for channels in Output Compare mode, and the FTM counter is forced to its initial counting value defined by CNTIN register.

The following figure shows the FTM counter synchronization. Note that after the synchronization event occurs, the channel (n) is set to its initial value and the channel (n +1) is not set to its initial value due to a specific timing of this figure in which the deadtime insertion prevents this channel output from transitioning to 1. If no deadtime insertion is selected, then the channel (n+1) transitions to logical value 1 immediately after the synchronization event occurs.

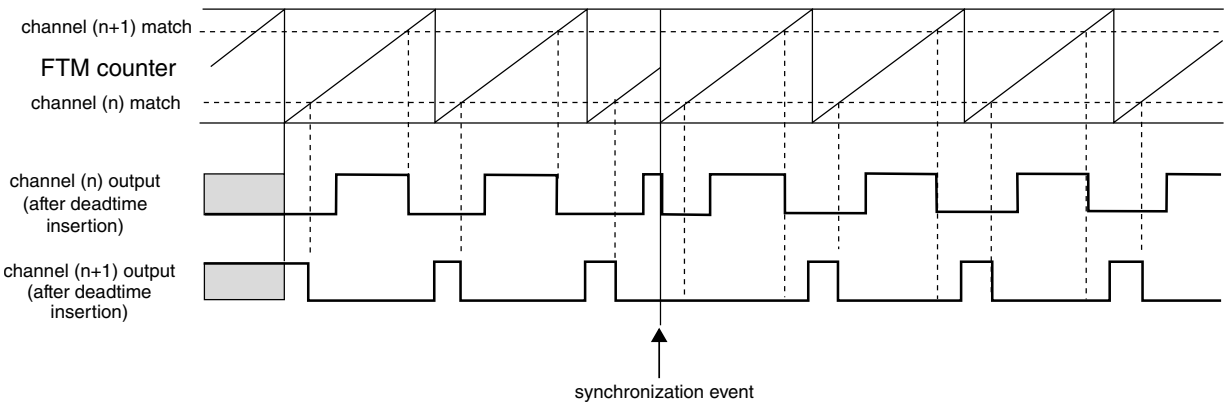


Figure 47-63. FTM counter synchronization

The FTM counter synchronization can be done by either the enhanced PWM synchronization (SYNCMODE = 1) or the legacy PWM synchronization (SYNCMODE = 0). However, the FTM counter must be synchronized only by the enhanced PWM synchronization.

In the case of enhanced PWM synchronization, the FTM counter synchronization depends on SWRSTCNT and HWRSTCNT bits according to the following flowchart.

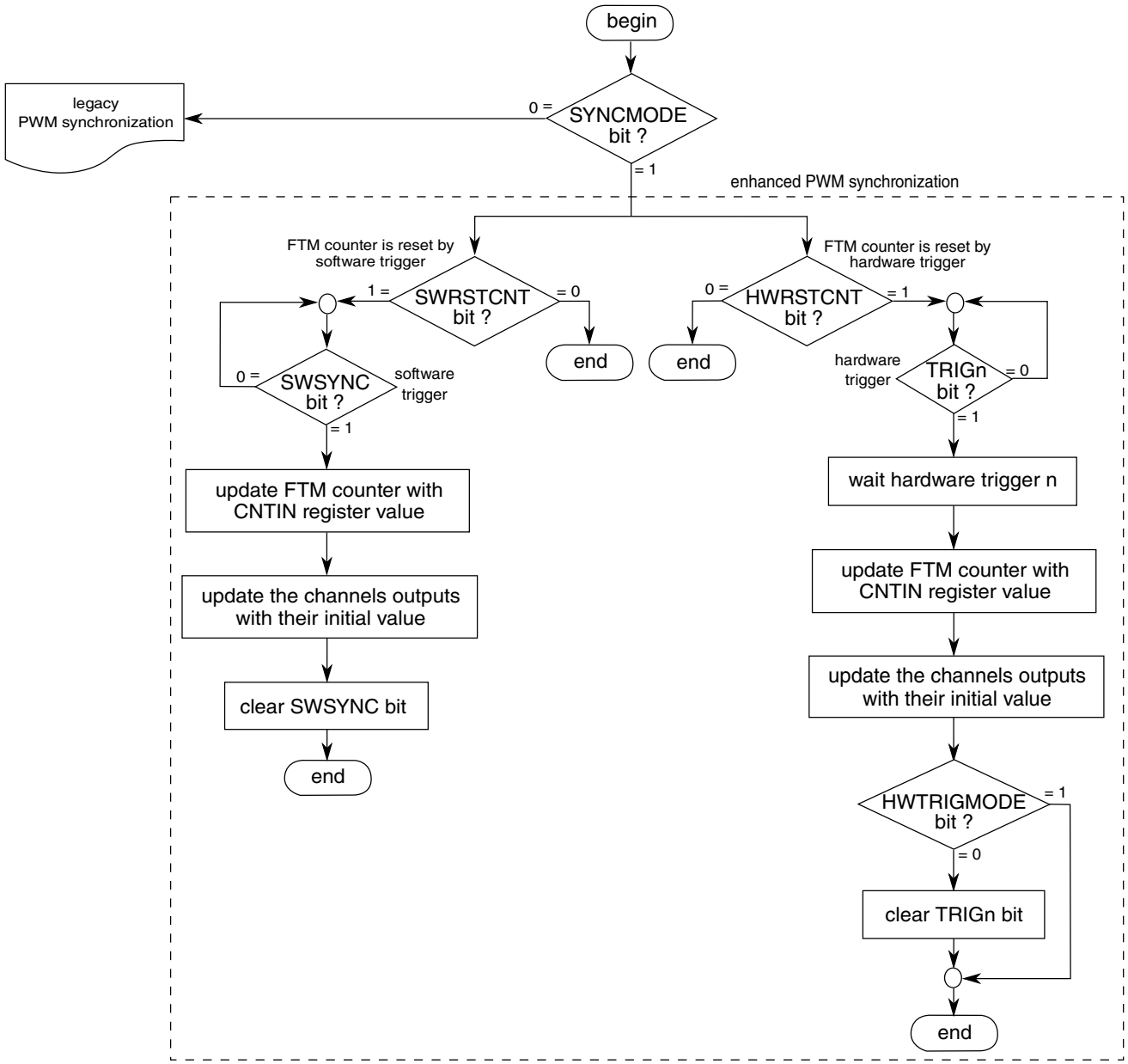


Figure 47-64. FTM counter synchronization flowchart

In the case of legacy PWM synchronization, the FTM counter synchronization depends on REINIT and PWMSYNC bits according to the following description.

If (SYNCMODE = 0), (REINIT = 1), and (PWMSYNC = 0) then this synchronization is made on the next enabled trigger event. If the trigger event was a software trigger then the SWSYNC bit is cleared according to the following example. If the trigger event was a hardware trigger then the TRIGn bit is cleared according to Hardware trigger. Examples with software and hardware triggers follow.

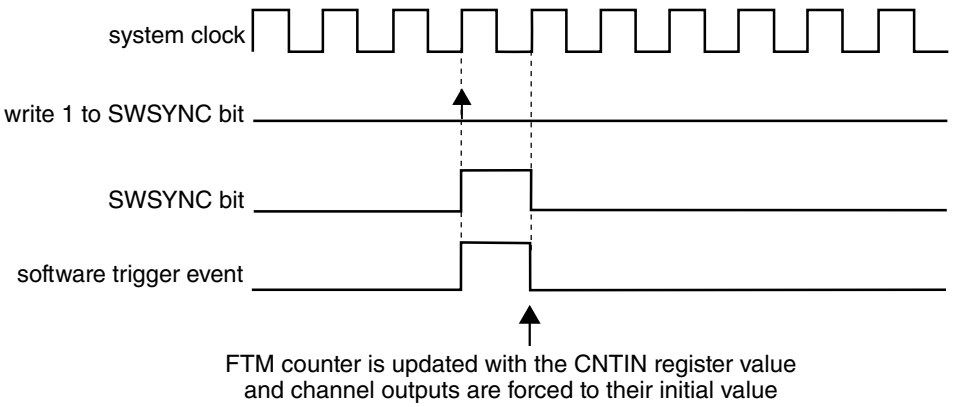


Figure 47-65. FTM counter synchronization with (SYNCMODE = 0), (REINIT = 1), (PWMSYNC = 0), and software trigger was used

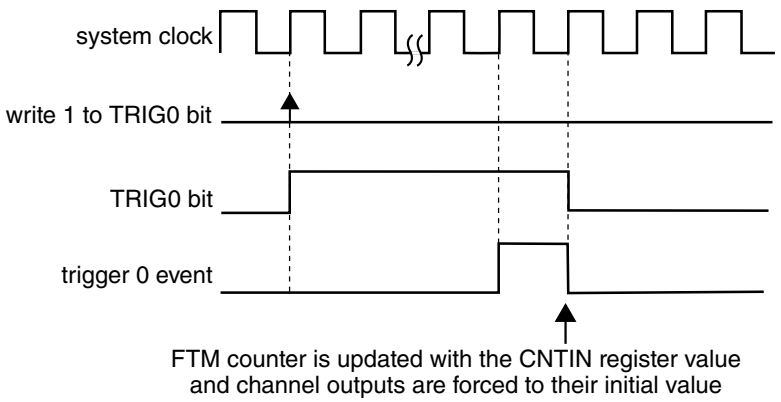


Figure 47-66. FTM counter synchronization with (SYNCMODE = 0), (HWTRIGMODE = 0), (REINIT = 1), (PWMSYNC = 0), and a hardware trigger was used

If (SYNCMODE = 0), (REINIT = 1), and (PWMSYNC = 1) then this synchronization is made on the next enabled hardware trigger. The TRIGn bit is cleared according to Hardware trigger.

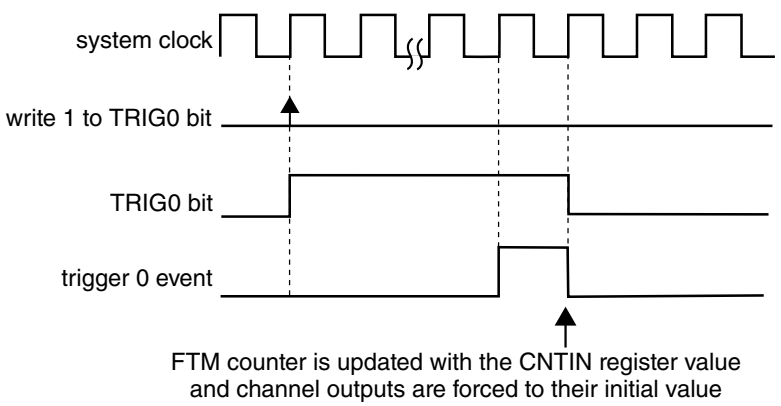


Figure 47-67. FTM counter synchronization with (SYNCMODE = 0), (HWTRIGMODE = 0), (REINIT = 1), (PWMSYNC = 1), and a hardware trigger was used

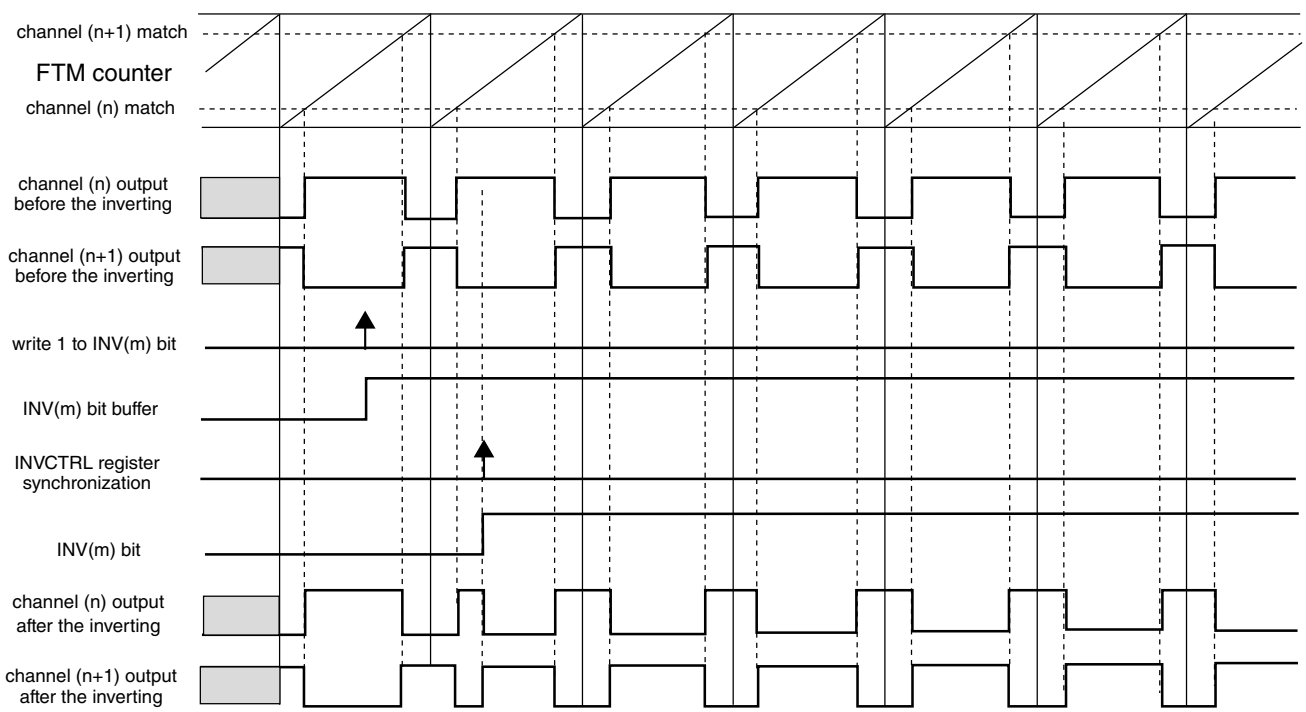
47.5.12 Inverting

The invert functionality swaps the signals between channel (n) and channel (n+1) outputs. The inverting operation is selected when:

- QUADEN = 0
- DECAPEN = 0
- COMP = 1, and
- INVm = 1 (where m represents a channel pair)

The INVm bit in INVCTRL register is updated with its buffer value according to INVCTRL register synchronization

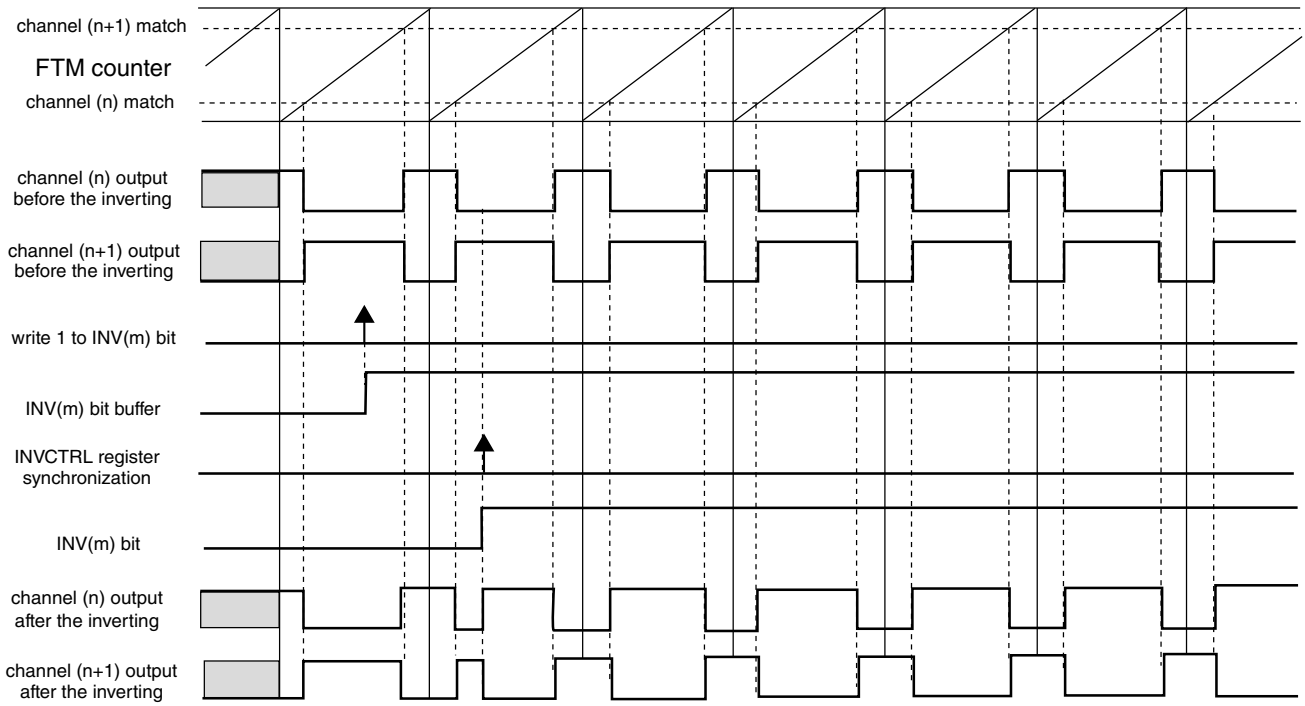
In High-True (ELSnB:ELSnA = 1:0) Combine mode, the channel (n) output is forced low at the beginning of the period (FTM counter = CNTIN), forced high at the channel (n) match and forced low at the channel (n+1) match. If the inverting is selected, the channel (n) output behavior is changed to force high at the beginning of the PWM period, force low at the channel (n) match and force high at the channel (n+1) match. See the following figure.



NOTE
INV(m) bit selects the inverting to the pair channels (n) and (n+1).

Figure 47-68. Channels (n) and (n+1) outputs after the inverting in High-True (ELSnB:ELSnA = 1:0) Combine mode

Note that the ELSnB:ELSnA bits value should be considered because they define the active state of the channels outputs. In Low-True (ELSnB:ELSnA = X:1) Combine mode, the channel (n) output is forced high at the beginning of the period, forced low at the channel (n) match and forced high at the channel (n+1) match. When inverting is selected, the channels (n) and (n+1) present waveforms as shown in the following figure.



NOTE
INV(m) bit selects the inverting to the pair channels (n) and (n+1).

Figure 47-69. Channels (n) and (n+1) outputs after the inverting in Low-True (ELSnB:ELSnA = X:1) Combine mode

Note

The inverting feature is not available in Output Compare mode.

47.5.13 Software output control

The software output control forces the channel output according to software defined values at a specific time in the PWM generation.

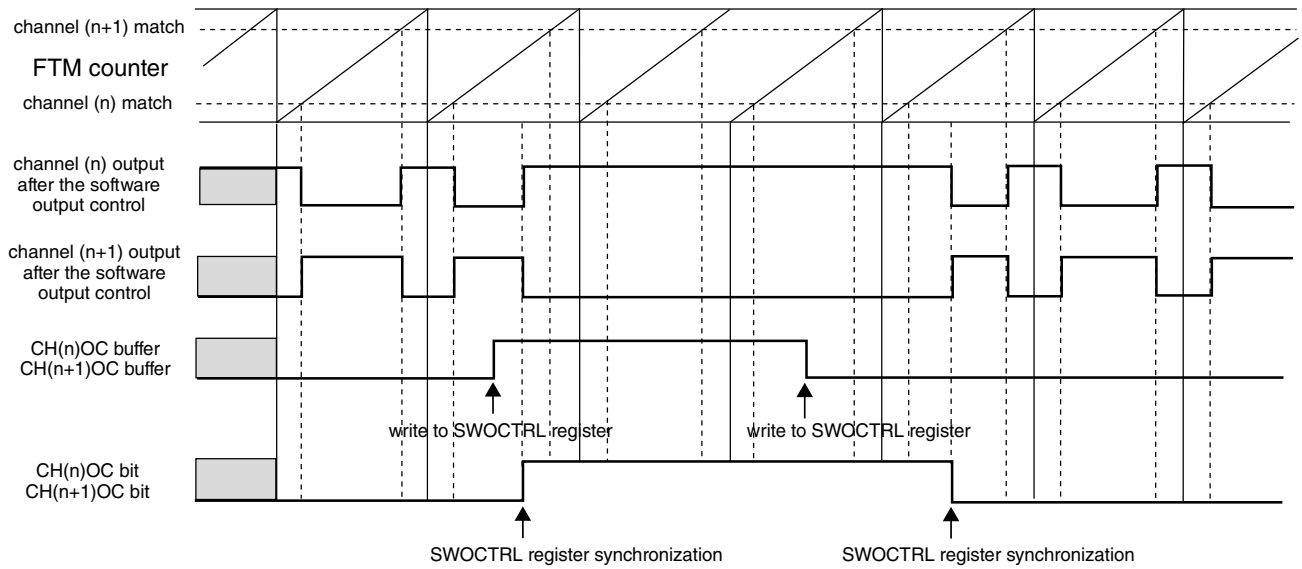
The software output control is selected when:

- QUADEN = 0
- DECAPEN = 0, and
- CHnOC = 1

The CHnOC bit enables the software output control for a specific channel output and the CHnOCV selects the value that is forced to this channel output.

Both CHnOC and CHnOCV bits in SWOCTRL register are buffered and updated with their buffer value according to SWOCTRL register synchronization.

The following figure shows the channels (n) and (n+1) outputs signals when the software output control is used. In this case the channels (n) and (n+1) are set to Combine and Complementary mode.



NOTE
CH(n)OCV = 1 and CH(n+1)OCV = 0.

Figure 47-70. Example of software output control in Combine and Complementary mode

Software output control forces the following values on channels (n) and (n+1) when the COMP bit is zero.

Table 47-9. Software ouput control behavior when (COMP = 0)

CH(n)OC	CH(n+1)OC	CH(n)OCV	CH(n+1)OCV	Channel (n) Output	Channel (n+1) Output
0	0	X	X	is not modified by SWOC	is not modified by SWOC
1	1	0	0	is forced to zero	is forced to zero
1	1	0	1	is forced to zero	is forced to one
1	1	1	0	is forced to one	is forced to zero
1	1	1	1	is forced to one	is forced to one

Software output control forces the following values on channels (n) and (n+1) when the COMP bit is one.

Table 47-10. Software ouput control behavior when (COMP = 1)

CH(n)OC	CH(n+1)OC	CH(n)OCV	CH(n+1)OCV	Channel (n) Output	Channel (n+1) Output
0	0	X	X	is not modified by SWOC	is not modified by SWOC
1	1	0	0	is forced to zero	is forced to zero
1	1	0	1	is forced to zero	is forced to one
1	1	1	0	is forced to one	is forced to zero
1	1	1	1	is forced to one	is forced to zero

Note

- The CH(n)OC and CH(n+1)OC bits should be equal.
- The COMP bit must not be modified when software output control is enabled, that is, CH(n)OC = 1 and/or CH(n +1)OC = 1.
- Software output control has the same behavior with disabled or enabled FTM counter (see the CLKS field description in the Status and Control register).

47.5.14 Deadtime insertion

The deadtime insertion is enabled when (DTEN = 1) and (DTVAL[5:0] is non- zero).

DEADTIME register defines the deadtime delay that can be used for all FTM channels. The DTPS[1:0] bits define the prescaler for the system clock and the DTVAL[5:0] bits define the deadtime modulo, that is, the number of the deadtime prescaler clocks.

The deadtime delay insertion ensures that no two complementary signals (channels (n) and (n+1)) drive the active state at the same time.

If POL(n) = 0, POL(n+1) = 0, and the deadtime is enabled, then when the channel (n) match (FTM counter = C(n)V) occurs, the channel (n) output remains at the low value until the end of the deadtime delay when the channel (n) output is set. Similarly, when the channel (n+1) match (FTM counter = C(n+1)V) occurs, the channel (n+1) output remains at the low value until the end of the deadtime delay when the channel (n+1) output is set. See the following figures.

If POL(n) = 1, POL(n+1) = 1, and the deadtime is enabled, then when the channel (n) match (FTM counter = C(n)V) occurs, the channel (n) output remains at the high value until the end of the deadtime delay when the channel (n) output is cleared. Similarly,

when the channel (n+1) match (FTM counter = C(n+1)V) occurs, the channel (n+1) output remains at the high value until the end of the deadtime delay when the channel (n +1) output is cleared.

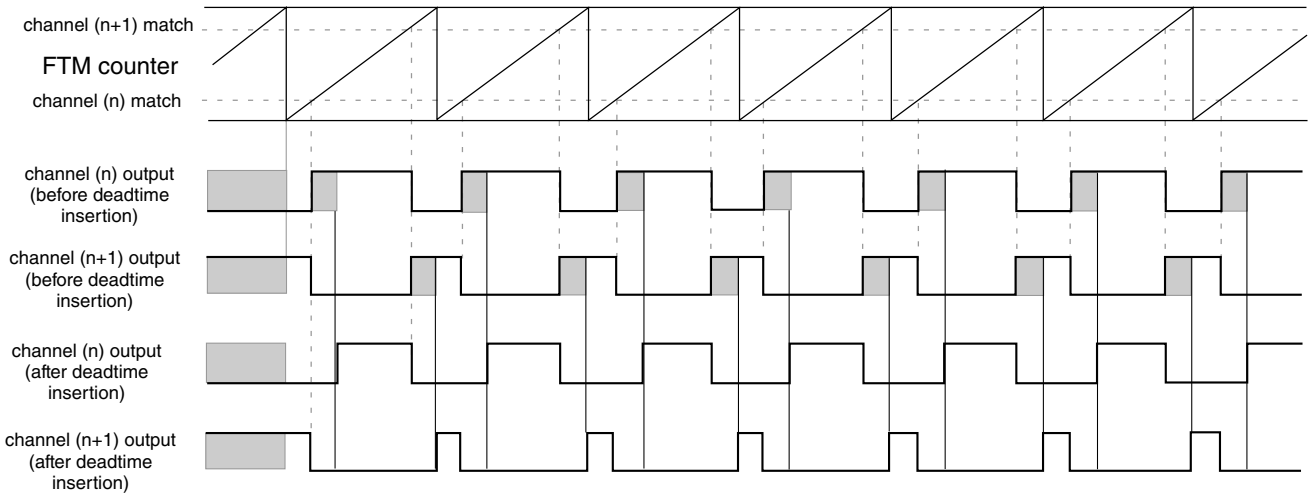


Figure 47-71. Deadtime insertion with ELSnB:ELSnA = 1:0, POL(n) = 0, and POL(n+1) = 0

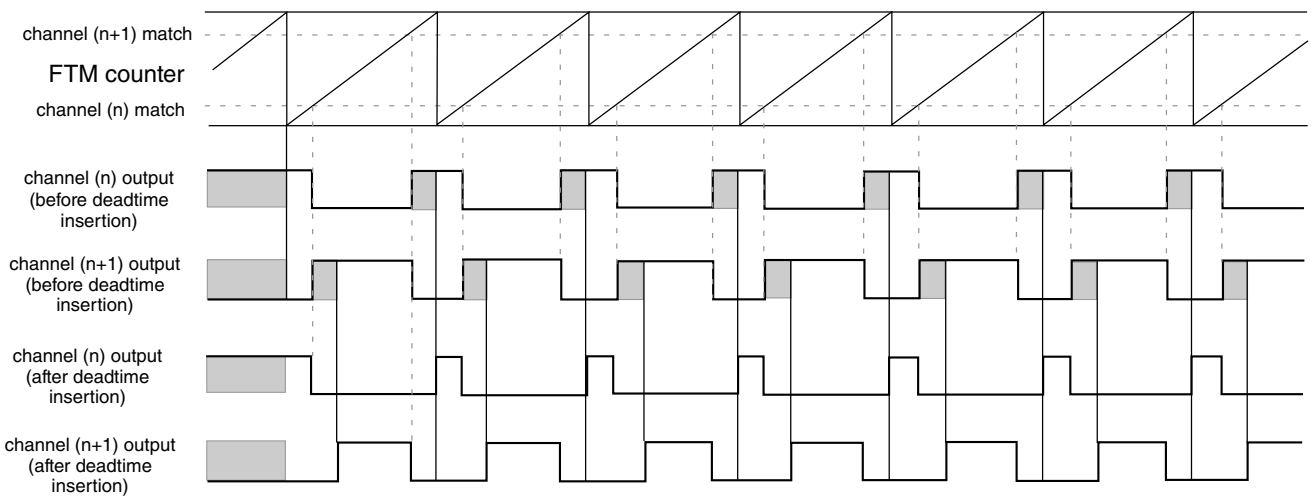


Figure 47-72. Deadtime insertion with ELSnB:ELSnA = X:1, POL(n) = 0, and POL(n+1) = 0

NOTE

- The deadtime feature must be used only in Complementary mode.
- The deadtime feature is not available in Output Compare mode.

47.5.14.1 Deadtime insertion corner cases

If (PS[2:0] is cleared), (DTPS[1:0] = 0:0 or DTPS[1:0] = 0:1):

- and the deadtime delay is greater than or equal to the channel (n) duty cycle ((C(n +1)V – C(n)V) × system clock), then the channel (n) output is always the inactive value (POL(n) bit value).
- and the deadtime delay is greater than or equal to the channel (n+1) duty cycle ((MOD – CNTIN + 1 – (C(n+1)V – C(n)V)) × system clock), then the channel (n+1) output is always the inactive value (POL(n+1) bit value).

Although, in most cases the deadtime delay is not comparable to channels (n) and (n+1) duty cycle, the following figures show examples where the deadtime delay is comparable to the duty cycle.

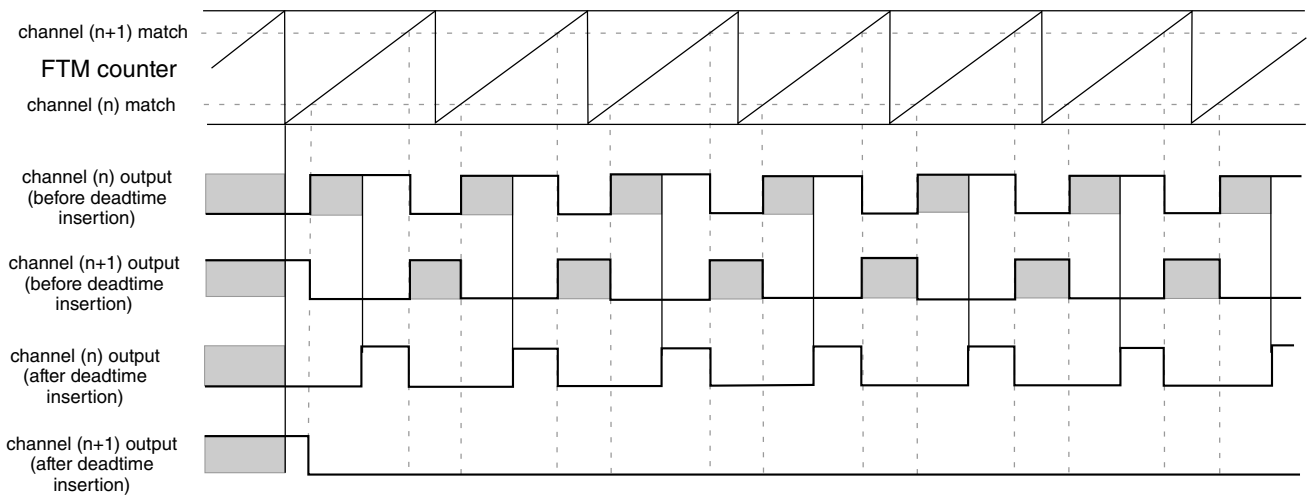


Figure 47-73. Example of the deadtime insertion (ELSnB:ELSnA = 1:0, POL(n) = 0, and POL(n+1) = 0) when the deadtime delay is comparable to channel (n+1) duty cycle

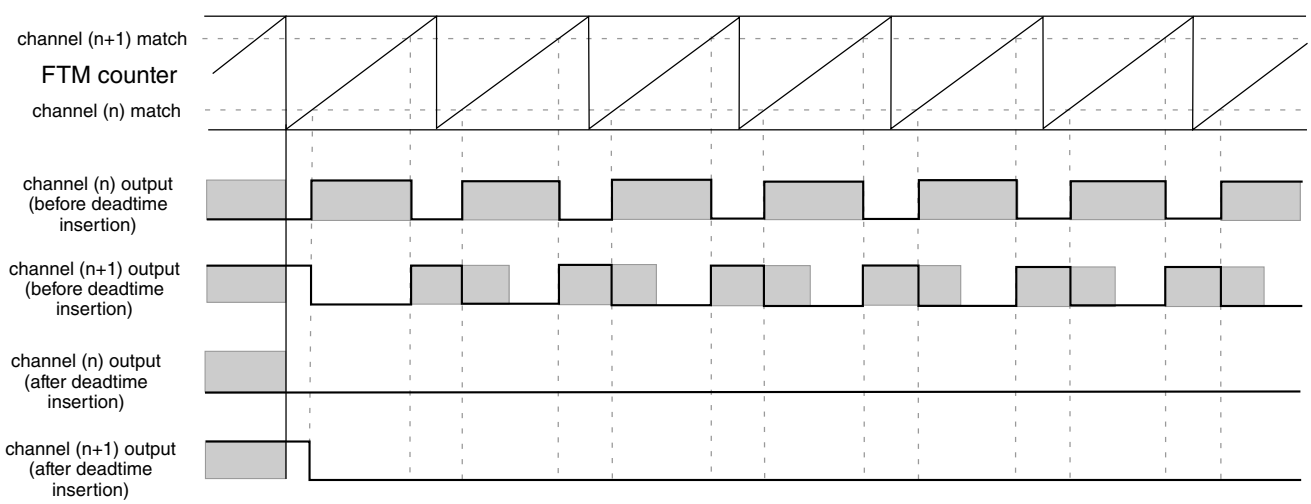


Figure 47-74. Example of the deadtime insertion (ELSnB:ELSnA = 1:0, POL(n) = 0, and POL(n+1) = 0) when the deadtime delay is comparable to channels (n) and (n+1) duty cycle

47.5.15 Output mask

The output mask can be used to force channels output to their inactive state through software. For example: to control a BLDC motor.

Any write to the OUTMASK register updates its write buffer. The OUTMASK register is updated with its buffer value by PWM synchronization; see OUTMASK register synchronization.

If CHnOM = 1, then the channel (n) output is forced to its inactive state (POLn bit value). If CHnOM = 0, then the channel (n) output is unaffected by the output mask. See the following figure.

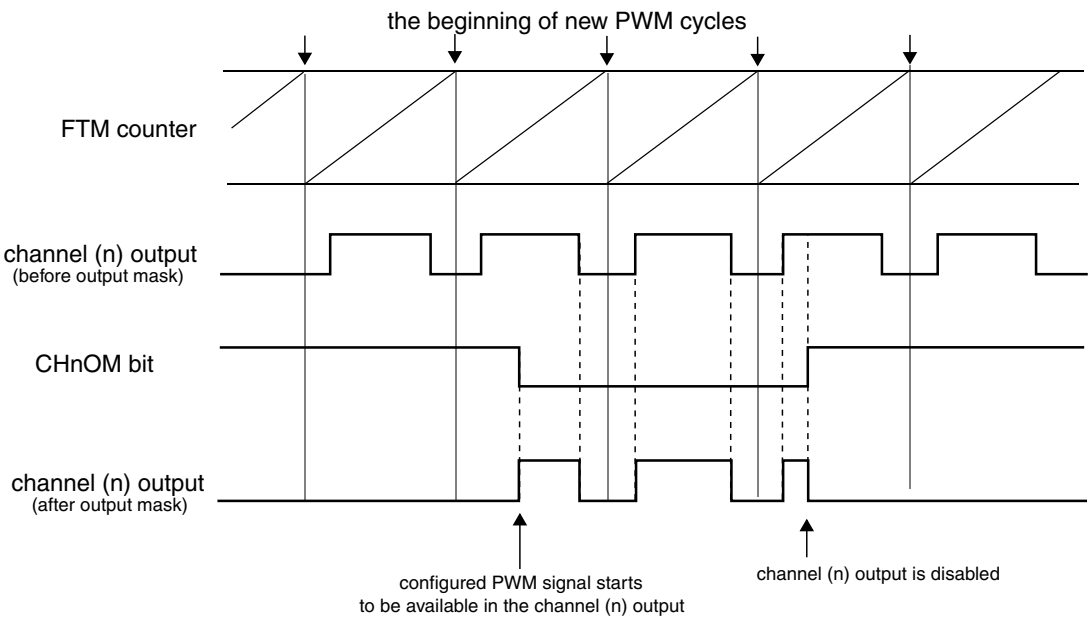


Figure 47-75. Output mask with POLn = 0

The following table shows the output mask result before the polarity control.

Table 47-11. Output mask result for channel (n) before the polarity control

CHnOM	Output Mask Input	Output Mask Result
0	inactive state	inactive state
	active state	active state
1	inactive state	inactive state
	active state	

47.5.16 Fault control

The fault control is enabled if (FAULTM[1:0] ≠ 0:0).

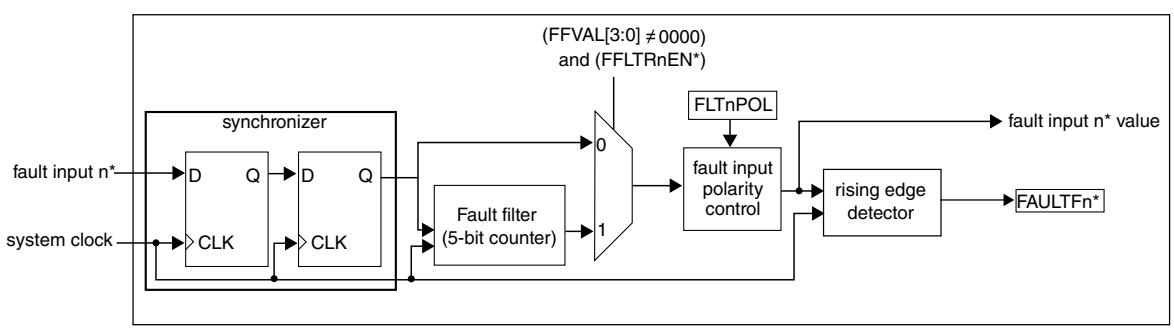
FTM can have up to four fault inputs. FAULTnEN bit (where n = 0, 1, 2, 3) enables the fault input n and FFLTRnEN bit enables the fault input n filter. FFVAL[3:0] bits select the value of the enabled filter in each enabled fault input.

First, each fault input signal is synchronized by the system clock; see the synchronizer block in the following figure. Following synchronization, the fault input n signal enters the filter block. When there is a state change in the fault input n signal, the 5-bit counter is reset and starts counting up. As long as the new state is stable on the fault input n, the counter continues to increment. If the 5-bit counter overflows, that is, the counter exceeds the value of the FFVAL[3:0] bits, the new fault input n value is validated. It is then transmitted as a pulse edge to the edge detector.

If the opposite edge appears on the fault input n signal before validation (counter overflow), the counter is reset. At the next input transition, the counter starts counting again. Any pulse that is shorter than the minimum value selected by FFVAL[3:0] bits (× system clock) is regarded as a glitch and is not passed on to the edge detector.

The fault input n filter is disabled when the FFVAL[3:0] bits are zero or when FAULTnEN = 0. In this case, the fault input n signal is delayed 2 rising edges of the system clock and the FAULTFn bit is set on 3th rising edge of the system clock after a rising edge occurs on the fault input n.

If FFVAL[3:0] ≠ 0000 and FAULTnEN = 1, then the fault input n signal is delayed (3 + FFVAL[3:0]) rising edges of the system clock, that is, the FAULTFn bit is set (4 + FFVAL[3:0]) rising edges of the system clock after a rising edge occurs on the fault input n.



* where n = 3, 2, 1, 0

Figure 47-76. Fault input n control block diagram

If the fault control and fault input n are enabled and a rising edge at the fault input n signal is detected, a fault condition has occurred and the FAULTFn bit is set. The FAULTF bit is the logic OR of FAULTFn[3:0] bits. See the following figure.

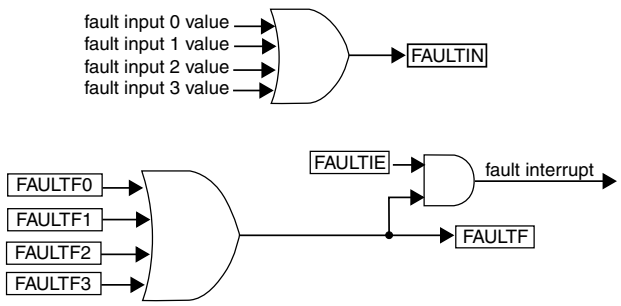


Figure 47-77. FAULTF and FAULTIN bits and fault interrupt

If the fault control is enabled (FAULTM[1:0] ≠ 0:0), a fault condition has occurred and (FAULTEN = 1), then outputs are forced to their safe values:

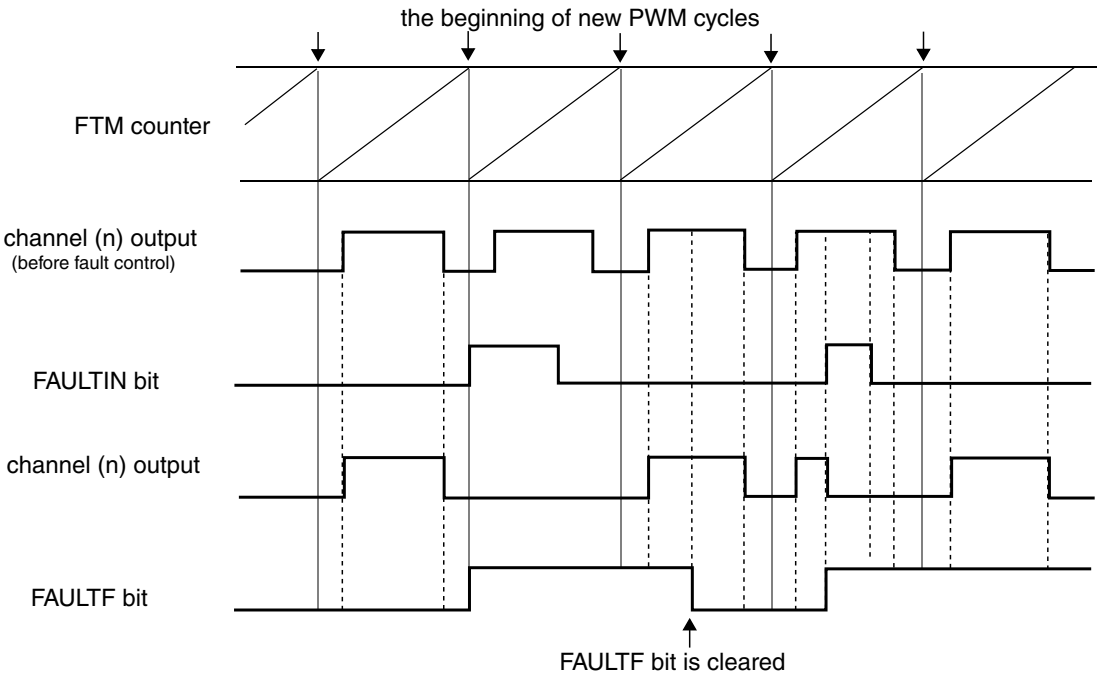
- Channel (n) output takes the value of POL(n)
- Channel (n+1) takes the value of POL(n+1)

The fault interrupt is generated when (FAULTF = 1) and (FAULTIE = 1). This interrupt request remains set until:

- Software clears the FAULTF bit by reading FAULTF bit as 1 and writing 0 to it
- Software clears the FAULTIE bit
- A reset occurs

47.5.16.1 Automatic fault clearing

If the automatic fault clearing is selected (FAULTM[1:0] = 1:1), then the channels output disabled by fault control is again enabled when the fault input signal (FAULTIN) returns to zero and a new PWM cycle begins. See the following figure.

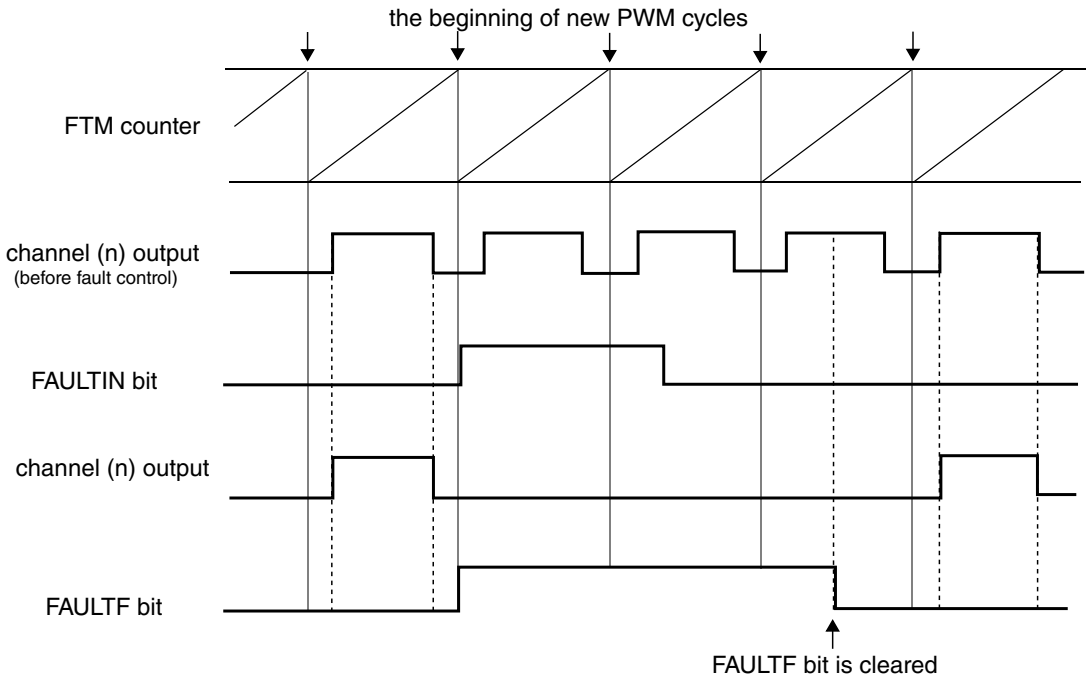


NOTE
The channel (n) output is after the fault control with automatic fault clearing and POLn = 0.

Figure 47-78. Fault control with automatic fault clearing

47.5.16.2 Manual fault clearing

If the manual fault clearing is selected (FAULTM[1:0] = 0:1 or 1:0), then the channels output disabled by fault control is again enabled when the FAULTF bit is cleared and a new PWM cycle begins. See the following figure.



NOTE
The channel (n) output is after the fault control with manual fault clearing and POLn = 0.

Figure 47-79. Fault control with manual fault clearing

47.5.16.3 Fault inputs polarity control

The FLTjPOL bit selects the fault input j polarity, where j = 0, 1, 2, 3:

- If FLTjPOL = 0, the fault j input polarity is high, so the logical one at the fault input j indicates a fault.
- If FLTjPOL = 1, the fault j input polarity is low, so the logical zero at the fault input j indicates a fault.

47.5.17 Polarity control

The POLn bit selects the channel (n) output polarity:

- If POLn = 0, the channel (n) output polarity is high, so the logical one is the active state and the logical zero is the inactive state.
- If POLn = 1, the channel (n) output polarity is low, so the logical zero is the active state and the logical one is the inactive state.

47.5.18 Initialization

The initialization forces the CHnOI bit value to the channel (n) output when a one is written to the INIT bit.

The initialization depends on COMP and DTEN bits. The following table shows the values that channels (n) and (n+1) are forced by initialization when the COMP and DTEN bits are zero.

Table 47-12. Initialization behavior when (COMP = 0 and DTEN = 0)

CH(n)OI	CH(n+1)OI	Channel (n) Output	Channel (n+1) Output
0	0	is forced to zero	is forced to zero
0	1	is forced to zero	is forced to one
1	0	is forced to one	is forced to zero
1	1	is forced to one	is forced to one

The following table shows the values that channels (n) and (n+1) are forced by initialization when (COMP = 1) or (DTEN = 1).

Table 47-13. Initialization behavior when (COMP = 1 or DTEN = 1)

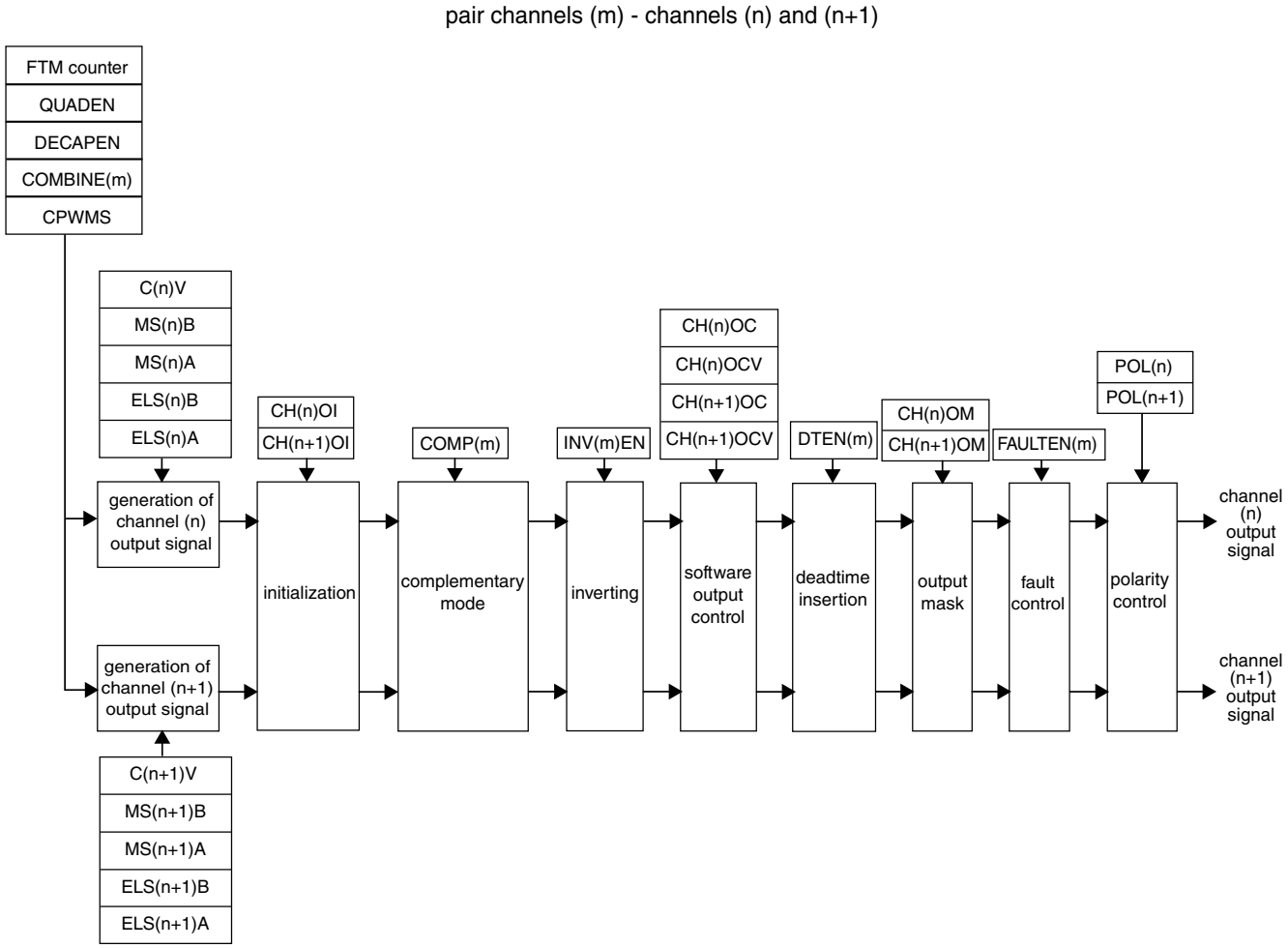
CH(n)OI	CH(n+1)OI	Channel (n) Output	Channel (n+1) Output
0	X	is forced to zero	is forced to one
1	X	is forced to one	is forced to zero

Note

The initialization feature must be used only with disabled FTM counter. See the description of the CLKS field in the Status and Control register.

47.5.19 Features priority

The following figure shows the priority of the features used at the generation of channels (n) and (n+1) outputs signals.



NOTE

The channels (n) and (n+1) are in output compare, EPWM, CPWM or combine modes.

Figure 47-80. Priority of the features used at the generation of channels (n) and (n+1) outputs signals

Note

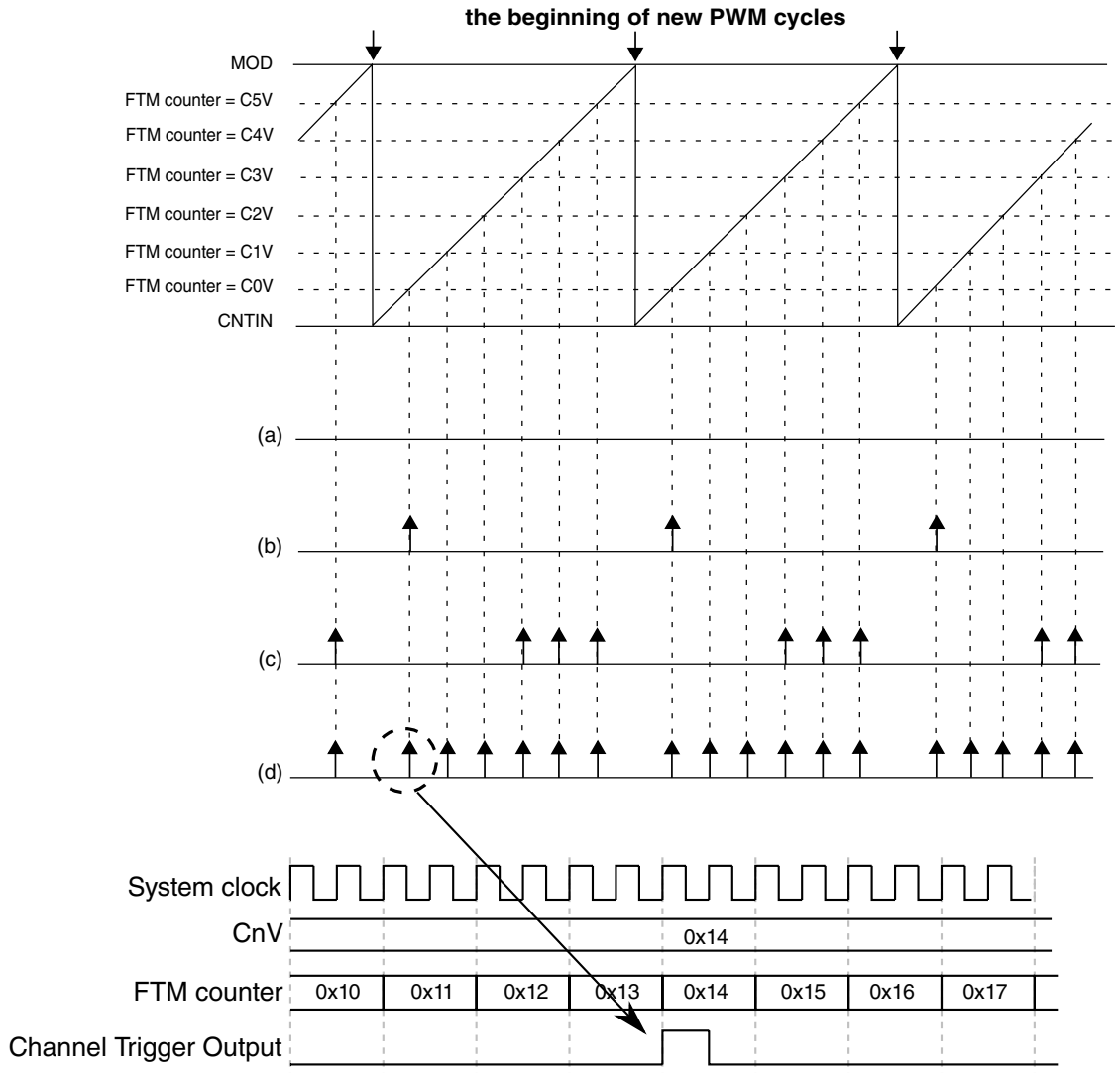
The Initialization feature must not be used with Inverting and Software output control features.

47.5.20 Channel trigger output

If CH(j)TRIG bit of the FTM External Trigger (FTM_EXTTRIG) register is set, where j = 0, 1, 2, 3, 4, or 5, then the FTM generates a trigger when the channel (j) match occurs (FTM counter = C(j)V).

The channel trigger output provides a trigger signal which has one FTM clock period width and is used for on-chip modules.

The FTM is able to generate multiple triggers in one PWM period. Because each trigger is generated for a specific channel, several channels are required to implement this functionality. This behavior is described in the following figure.



NOTE

(a) CH0TRIG = 0, CH1TRIG = 0, CH2TRIG = 0, CH3TRIG = 0, CH4TRIG = 0, CH5TRIG = 0
(b) CH0TRIG = 1, CH1TRIG = 0, CH2TRIG = 0, CH3TRIG = 0, CH4TRIG = 0, CH5TRIG = 0
(c) CH0TRIG = 0, CH1TRIG = 0, CH2TRIG = 0, CH3TRIG = 1, CH4TRIG = 1, CH5TRIG = 1
(d) CH0TRIG = 1, CH1TRIG = 1, CH2TRIG = 1, CH3TRIG = 1, CH4TRIG = 1, CH5TRIG = 1

Figure 47-81. Channel match trigger

47.5.21 Initialization trigger

If INITTRIGEN = 1, then the FTM generates a trigger when the FTM counter is updated with the CNTIN register value in the following cases.

- The FTM counter is automatically updated with the CNTIN register value by the selected counting mode.
- When there is a write to CNT register.
- When there is the FTM counter synchronization.
- If (CNT = CNTIN), (CLKS[1:0] = 0:0), and a value different from zero is written to CLKS[1:0] bits.
- If the channel (n) is in Input Capture mode, (ICRST = 1) and the selected input capture event occurs in the channel (n) input.

The following figures show these cases.

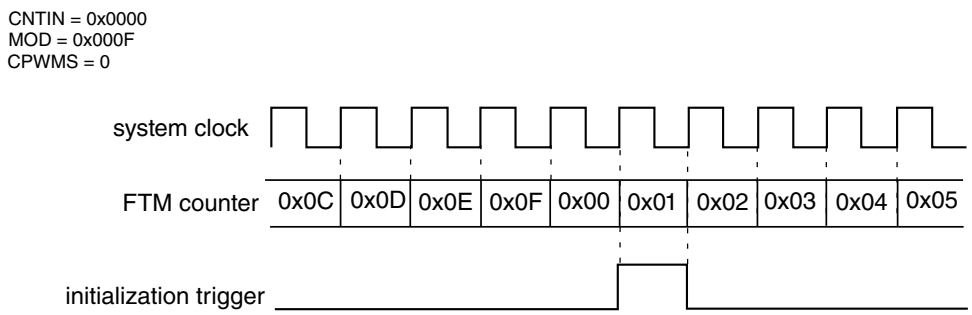


Figure 47-82. Initialization trigger is generated when the FTM counting achieves the CNTIN register value

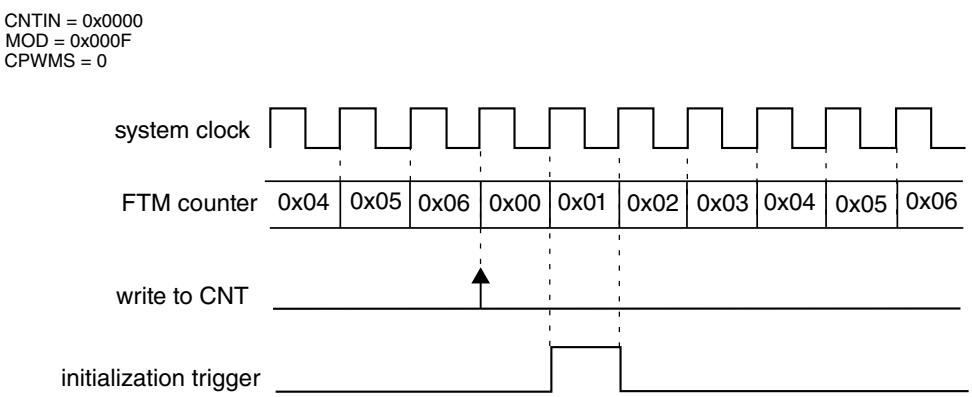


Figure 47-83. Initialization trigger is generated when there is a write to CNT register

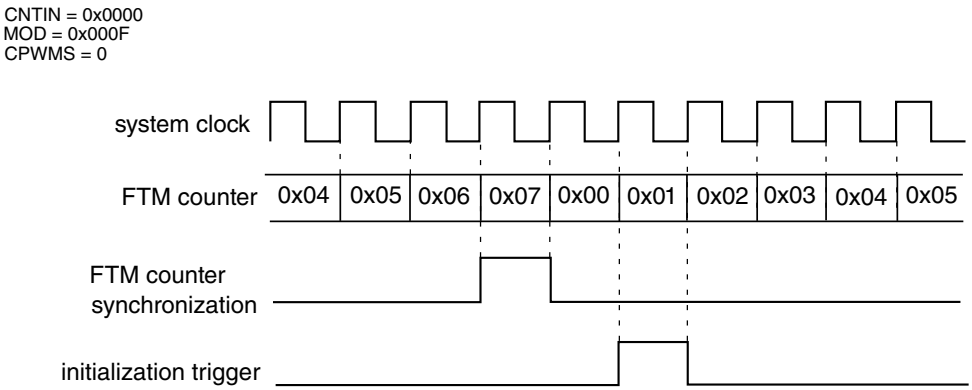


Figure 47-84. Initialization trigger is generated when there is the FTM counter synchronization

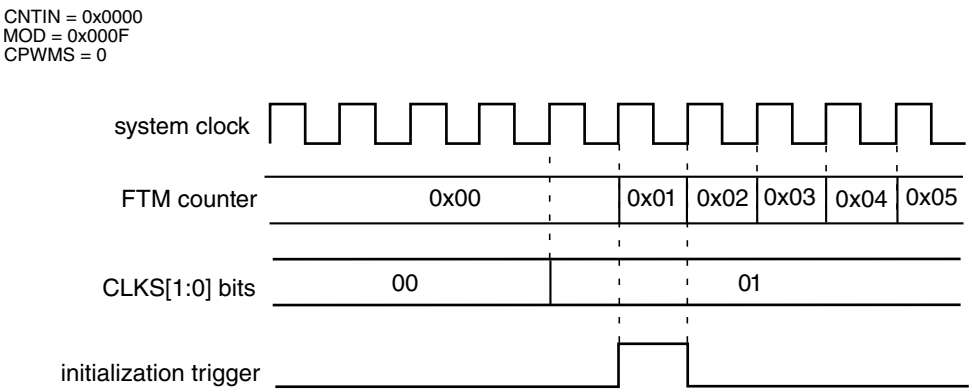
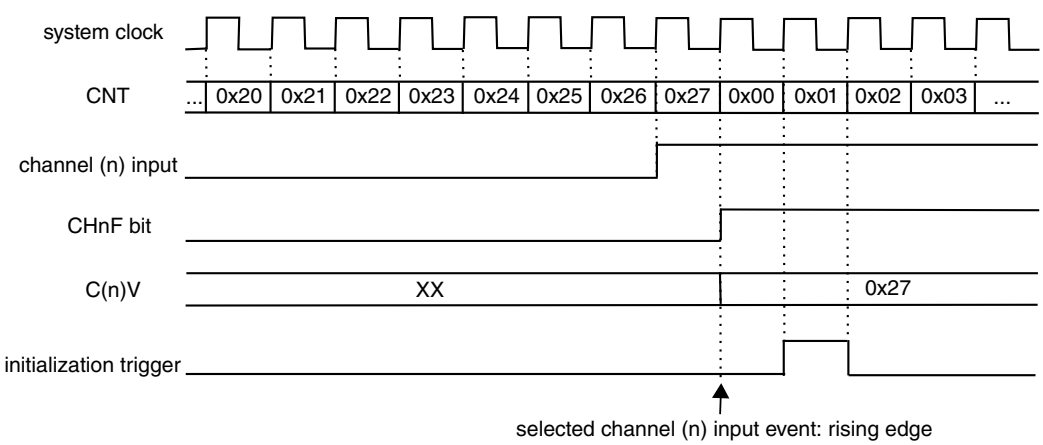


Figure 47-85. Initialization trigger is generated if (CNT = CNTIN), (CLKS[1:0] = 0:0), and a value different from zero is written to CLKS[1:0] bits



NOTE
Channel (n) input after its synchronizer and filter
MOD = 0xFFFF
CNTIN = 0x0000
PS[2:0] = 3'b000
ICRST = 1'b1

Figure 47-86. Initialization trigger is generated if the channel (n) is in Input Capture mode, ICRST = 1 and the selected input capture event occurs in the channel (n) input

The initialization trigger output provides a trigger signal that is used for on-chip modules.

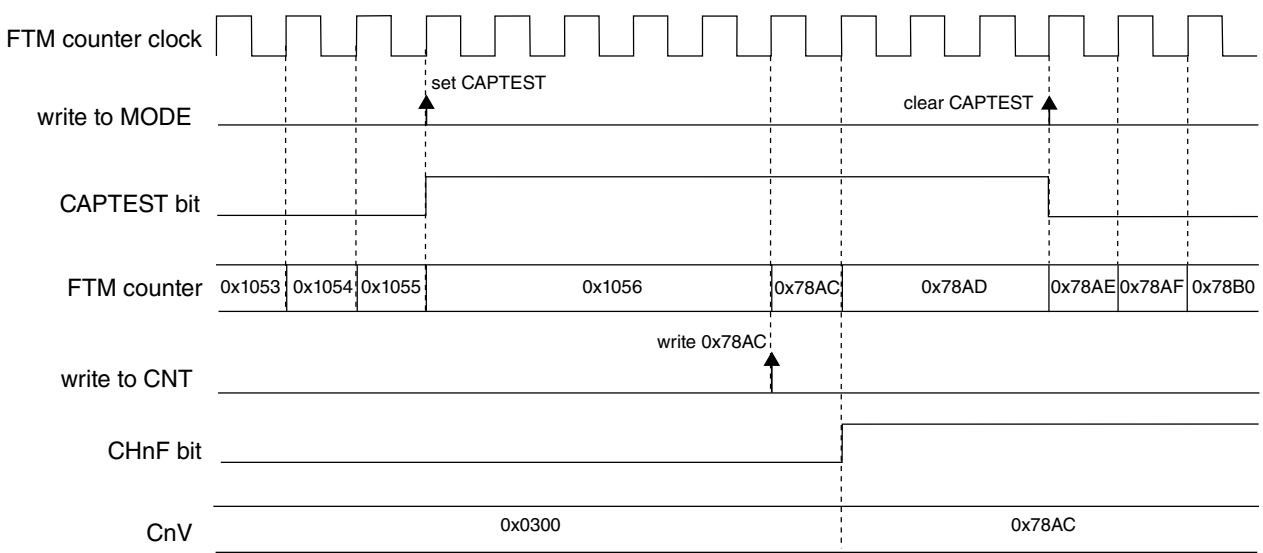
47.5.22 Capture Test mode

The Capture Test mode allows to test the CnV registers, the FTM counter and the interconnection logic between the FTM counter and CnV registers.

In this test mode, all channels must be configured for Input Capture mode and FTM counter must be configured to the Up counting.

When the Capture Test mode is enabled (CAPTEST = 1), the FTM counter is frozen and any write to CNT register updates directly the FTM counter; see the following figure. After it was written, all CnV registers are updated with the written value to CNT register and CHnF bits are set. Therefore, the FTM counter is updated with its next value according to its configuration. Its next value depends on CNTIN, MOD, and the written value to FTM counter.

The next reads of CnV registers return the written value to the FTM counter and the next reads of CNT register return FTM counter next value.



NOTE
- FTM counter configuration: (FTMEN = 1), (QUADEN = 0), (CAPTEST = 1), (CPWMS = 0), (CNTIN = 0x0000), and (MOD = 0xFFFF)
- FTM channel n configuration: input capture mode - (DECAPEN = 0), (COMBINE = 0), and (MSnB:MSnA = 0:0)

Figure 47-87. Capture Test mode

47.5.23 DMA

The channel generates a DMA transfer request according to DMA and CHnIE bits. See the following table.

Table 47-14. Channel DMA transfer request

DMA	CHnIE	Channel DMA Transfer Request	Channel Interrupt
0	0	The channel DMA transfer request is not generated.	The channel interrupt is not generated.
0	1	The channel DMA transfer request is not generated.	The channel interrupt is generated if (CHnF = 1).
1	0	The channel DMA transfer request is not generated.	The channel interrupt is not generated.
1	1	The channel DMA transfer request is generated if (CHnF = 1).	The channel interrupt is not generated.

If DMA = 1, the CHnF bit is cleared either by channel DMA transfer done or reading CnSC while CHnF is set and then writing a zero to CHnF bit according to CHnIE bit. See the following table.

Table 47-15. Clear CHnF bit when DMA = 1

CHnIE	How CHnF Bit Can Be Cleared
0	CHnF bit is cleared either when the channel DMA transfer is done or by reading CnSC while CHnF is set and then writing a 0 to CHnF bit.
1	CHnF bit is cleared when the channel DMA transfer is done.

47.5.24 Dual Edge Capture mode

The Dual Edge Capture mode is selected if DECAPEN = 1. This mode allows to measure a pulse width or period of the signal on the input of channel (n) of a channel pair. The channel (n) filter can be active in this mode when n is 0 or 2.

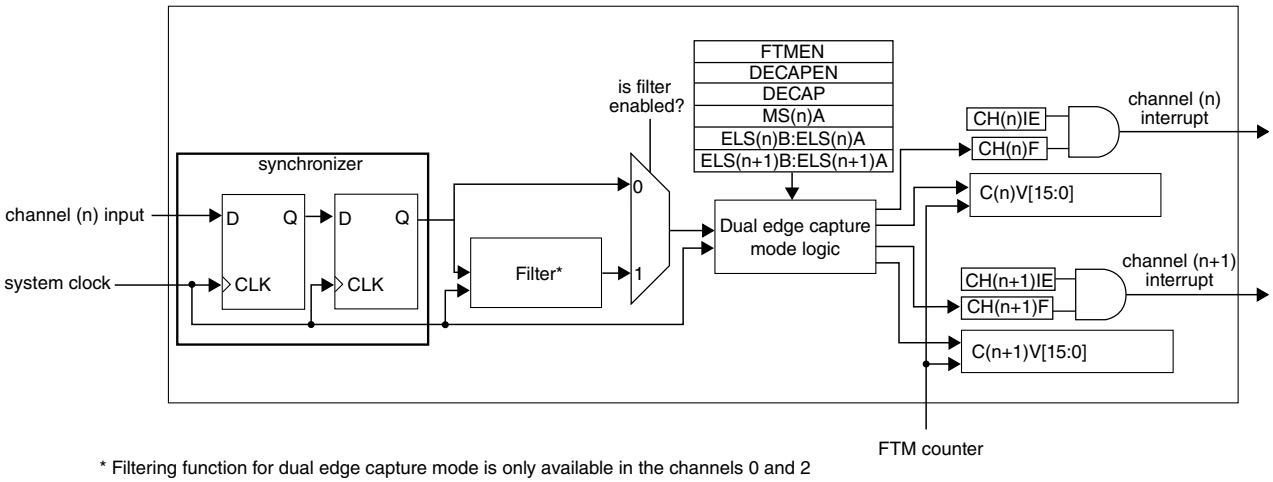


Figure 47-88. Dual Edge Capture mode block diagram

The MS(n)A bit defines if the Dual Edge Capture mode is one-shot or continuous.

The ELS(n)B:ELS(n)A bits select the edge that is captured by channel (n), and ELS(n +1)B:ELS(n+1)A bits select the edge that is captured by channel (n+1). If both ELS(n)B:ELS(n)A and ELS(n+1)B:ELS(n+1)A bits select the same edge, then it is the period measurement. If these bits select different edges, then it is a pulse width measurement.

In the Dual Edge Capture mode, only channel (n) input is used and channel (n+1) input is ignored.

If the selected edge by channel (n) bits is detected at channel (n) input, then CH(n)F bit is set and the channel (n) interrupt is generated (if CH(n)IE = 1). If the selected edge by channel (n+1) bits is detected at channel (n) input and (CH(n)F = 1), then CH(n+1)F bit is set and the channel (n+1) interrupt is generated (if CH(n+1)IE = 1).

The C(n)V register stores the value of FTM counter when the selected edge by channel (n) is detected at channel (n) input. The C(n+1)V register stores the value of FTM counter when the selected edge by channel (n+1) is detected at channel (n) input.

In this mode, a coherency mechanism ensures coherent data when the C(n)V and C(n +1)V registers are read. The only requirement is that C(n)V must be read before C(n +1)V.

Note

- The CH(n)F, CH(n)IE, MS(n)A, ELS(n)B, and ELS(n)A bits are channel (n) bits.

- The CH(n+1)F, CH(n+1)IE, MS(n+1)A, ELS(n+1)B, and ELS(n+1)A bits are channel (n+1) bits.
- The Dual Edge Capture mode must be used with ELS(n)B:ELS(n)A = 0:1 or 1:0, ELS(n+1)B:ELS(n+1)A = 0:1 or 1:0 and the FTM counter in Free running counter.

47.5.24.1 One-Shot Capture mode

The One-Shot Capture mode is selected when (DECAPEN = 1), and (MS(n)A = 0). In this capture mode, only one pair of edges at the channel (n) input is captured. The ELS(n)B:ELS(n)A bits select the first edge to be captured, and ELS(n+1)B:ELS(n+1)A bits select the second edge to be captured.

The edge captures are enabled while DECAP bit is set. For each new measurement in One-Shot Capture mode, first the CH(n)F and CH(n+1) bits must be cleared, and then the DECAP bit must be set.

In this mode, the DECAP bit is automatically cleared by FTM when the edge selected by channel (n+1) is captured. Therefore, while DECAP bit is set, the one-shot capture is in process. When this bit is cleared, both edges were captured and the captured values are ready for reading in the C(n)V and C(n+1)V registers.

Similarly, when the CH(n+1)F bit is set, both edges were captured and the captured values are ready for reading in the C(n)V and C(n+1)V registers.

47.5.24.2 Continuous Capture mode

The Continuous Capture mode is selected when (DECAPEN = 1), and (MS(n)A = 1). In this capture mode, the edges at the channel (n) input are captured continuously. The ELS(n)B:ELS(n)A bits select the initial edge to be captured, and ELS(n+1)B:ELS(n+1)A bits select the final edge to be captured.

The edge captures are enabled while DECAP bit is set. For the initial use, first the CH(n)F and CH(n+1)F bits must be cleared, and then DECAP bit must be set to start the continuous measurements.

When the CH(n+1)F bit is set, both edges were captured and the captured values are ready for reading in the C(n)V and C(n+1)V registers. The latest captured values are always available in these registers even after the DECAP bit is cleared.

In this mode, it is possible to clear only the CH(n+1)F bit. Therefore, when the CH(n+1)F bit is set again, the latest captured values are available in C(n)V and C(n+1)V registers.

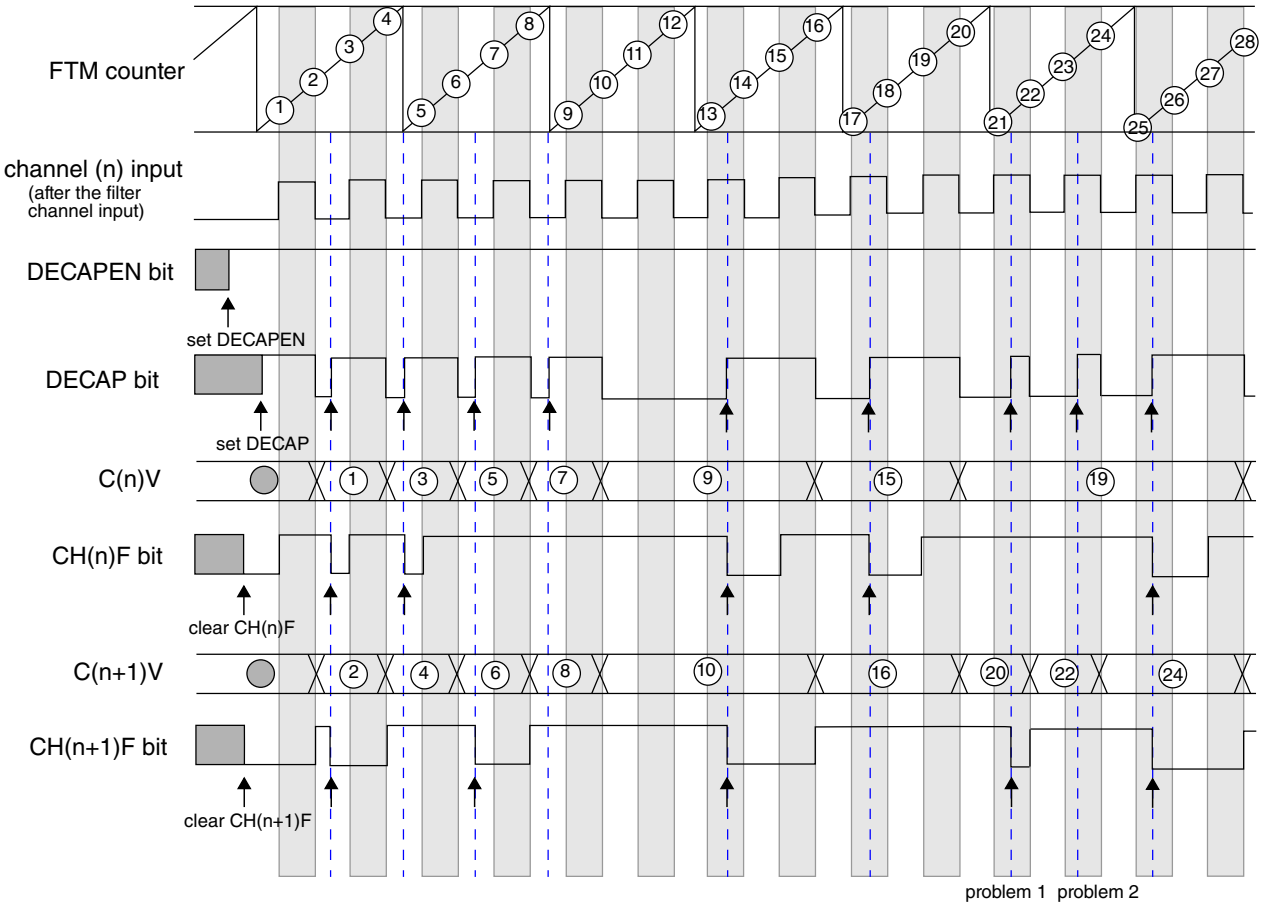
For a new sequence of the measurements in the Dual Edge Capture – Continuous mode, clear the CH(n)F and CH(n+1)F bits to start new measurements.

47.5.24.3 Pulse width measurement

If the channel (n) is configured to capture rising edges (ELS(n)B:ELS(n)A = 0:1) and the channel (n+1) to capture falling edges (ELS(n+1)B:ELS(n+1)A = 1:0), then the positive polarity pulse width is measured. If the channel (n) is configured to capture falling edges (ELS(n)B:ELS(n)A = 1:0) and the channel (n+1) to capture rising edges (ELS(n +1)B:ELS(n+1)A = 0:1), then the negative polarity pulse width is measured.

The pulse width measurement can be made in One-Shot Capture mode or Continuous Capture mode.

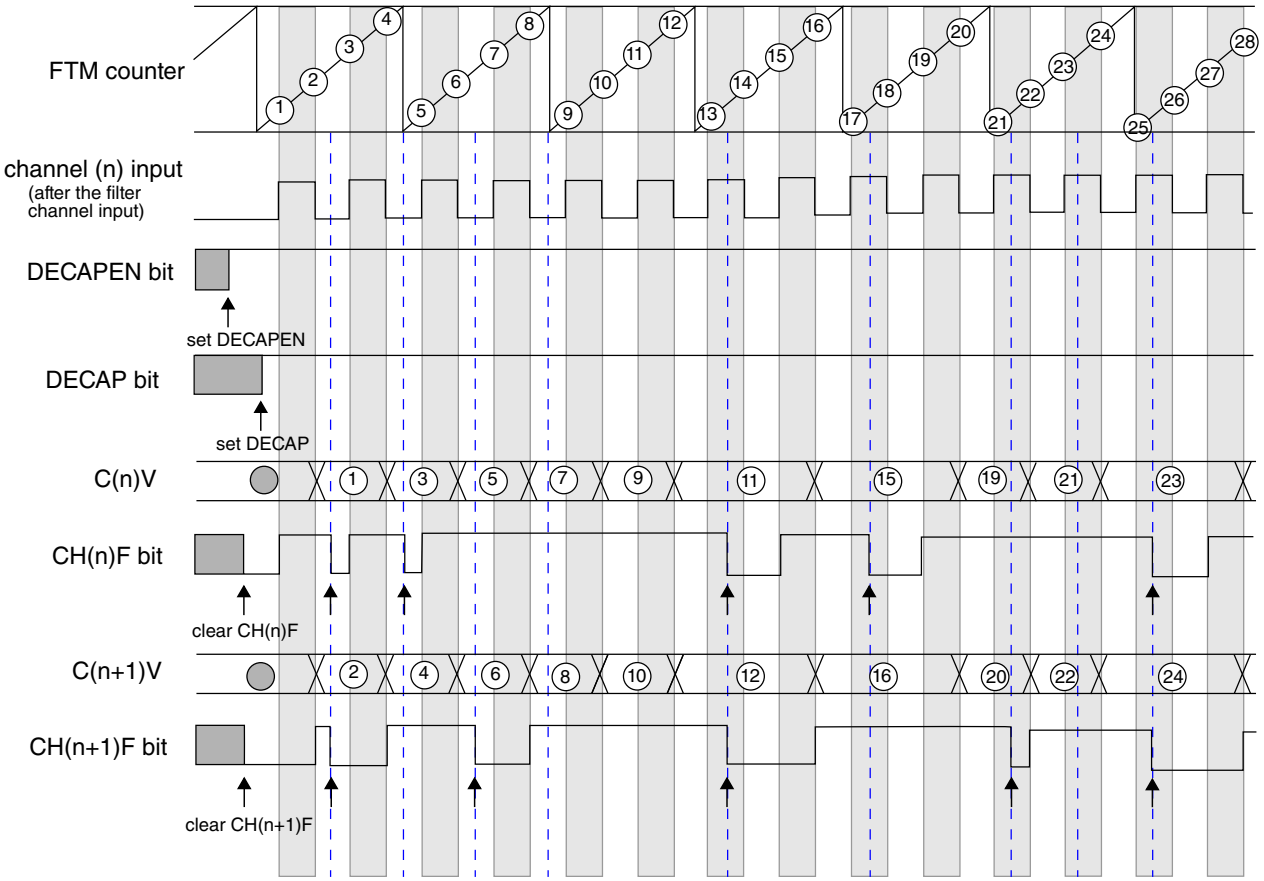
The following figure shows an example of the Dual Edge Capture – One-Shot mode used to measure the positive polarity pulse width. The DECAPEN bit selects the Dual Edge Capture mode, so it remains set. The DECAP bit is set to enable the measurement of next positive polarity pulse width. The CH(n)F bit is set when the first edge of this pulse is detected, that is, the edge selected by ELS(n)B:ELS(n)A bits. The CH(n+1)F bit is set and DECAP bit is cleared when the second edge of this pulse is detected, that is, the edge selected by ELS(n+1)B:ELS(n+1)A bits. Both DECAP and CH(n+1)F bits indicate when two edges of the pulse were captured and the C(n)V and C(n+1)V registers are ready for reading.



Note
- The commands set DECAPEN, set DECAP, clear CH(n)F, and clear CH(n+1)F are made by the user.
- Problem 1: channel (n) input = 1, set DECAP, not clear CH(n)F, and clear CH(n+1)F.
- Problem 2: channel (n) input = 1, set DECAP, not clear CH(n)F, and not clear CH(n+1)F.

Figure 47-89. Dual Edge Capture – One-Shot mode for positive polarity pulse width measurement

The following figure shows an example of the Dual Edge Capture – Continuous mode used to measure the positive polarity pulse width. The DECAPEN bit selects the Dual Edge Capture mode, so it remains set. While the DECAP bit is set the configured measurements are made. The CH(n)F bit is set when the first edge of the positive polarity pulse is detected, that is, the edge selected by ELS(n)B:ELS(n)A bits. The CH(n+1)F bit is set when the second edge of this pulse is detected, that is, the edge selected by ELS(n +1)B:ELS(n+1)A bits. The CH(n+1)F bit indicates when two edges of the pulse were captured and the C(n)V and C(n+1)V registers are ready for reading.



Note
- The commands set DECAPEN, set DECAP, clear CH(n)F, and clear CH(n+1)F are made by the user.

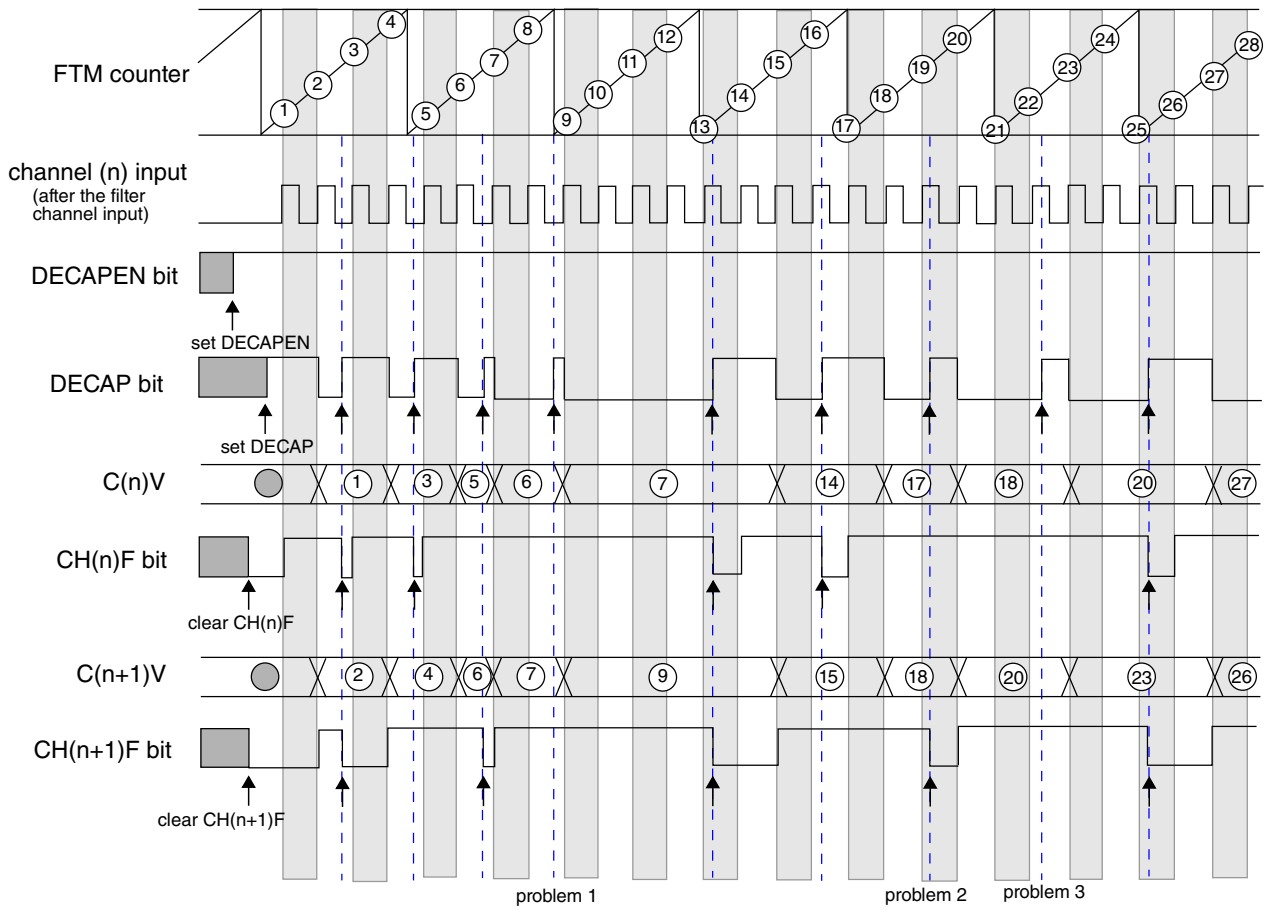
Figure 47-90. Dual Edge Capture – Continuous mode for positive polarity pulse width measurement

47.5.24.4 Period measurement

If the channels (n) and (n+1) are configured to capture consecutive edges of the same polarity, then the period of the channel (n) input signal is measured. If both channels (n) and (n+1) are configured to capture rising edges (ELS(n)B:ELS(n)A = 0:1 and ELS(n +1)B:ELS(n+1)A = 0:1), then the period between two consecutive rising edges is measured. If both channels (n) and (n+1) are configured to capture falling edges (ELS(n)B:ELS(n)A = 1:0 and ELS(n+1)B:ELS(n+1)A = 1:0), then the period between two consecutive falling edges is measured.

The period measurement can be made in One-Shot Capture mode or Continuous Capture mode.

The following figure shows an example of the Dual Edge Capture – One-Shot mode used to measure the period between two consecutive rising edges. The DECAPEN bit selects the Dual Edge Capture mode, so it remains set. The DECAP bit is set to enable the measurement of next period. The CH(n)F bit is set when the first rising edge is detected, that is, the edge selected by ELS(n)B:ELS(n)A bits. The CH(n+1)F bit is set and DECAP bit is cleared when the second rising edge is detected, that is, the edge selected by ELS(n+1)B:ELS(n+1)A bits. Both DECAP and CH(n+1)F bits indicate when two selected edges were captured and the C(n)V and C(n+1)V registers are ready for reading.

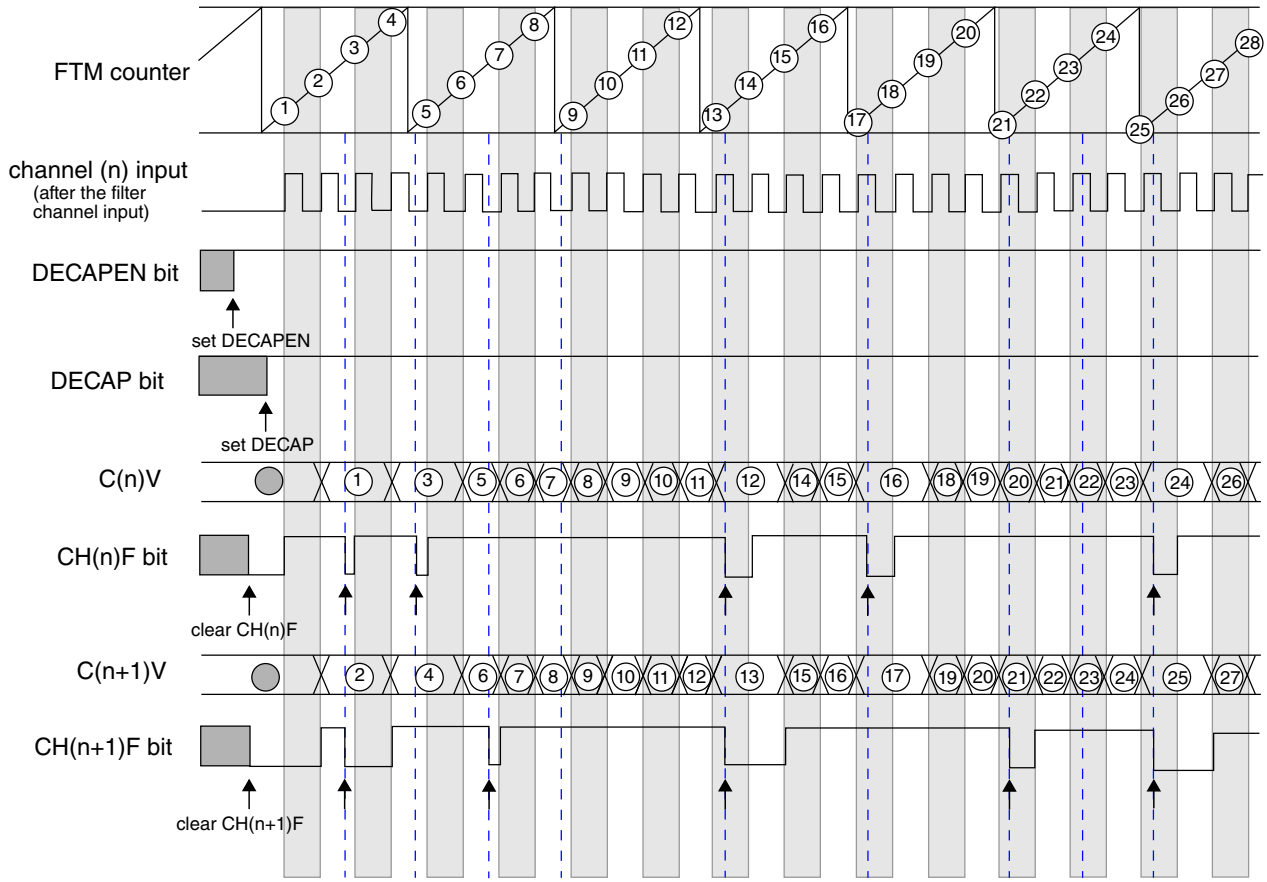


Note
- The commands set DECAPEN, set DECAP, clear CH(n)F, and clear CH(n+1)F are made by the user.
- Problem 1: channel (n) input = 0, set DECAP, not clear CH(n)F, and not clear CH(n+1)F.
- Problem 2: channel (n) input = 1, set DECAP, not clear CH(n)F, and clear CH(n+1)F.
- Problem 3: channel (n) input = 1, set DECAP, not clear CH(n)F, and not clear CH(n+1)F.

Figure 47-91. Dual Edge Capture – One-Shot mode to measure of the period between two consecutive rising edges

The following figure shows an example of the Dual Edge Capture – Continuous mode used to measure the period between two consecutive rising edges. The DECAPEN bit selects the Dual Edge Capture mode, so it remains set. While the DECAP bit is set the configured measurements are made. The CH(n)F bit is set when the first rising edge is detected, that is, the edge selected by ELS(n)B:ELS(n)A bits. The CH(n+1)F bit is set

when the second rising edge is detected, that is, the edge selected by ELS(n+1)B:ELS(n +1)A bits. The CH(n+1)F bit indicates when two edges of the period were captured and the C(n)V and C(n+1)V registers are ready for reading.



Note
- The commands set DECAPEN, set DECAP, clear CH(n)F, and clear CH(n+1)F are made by the user.

Figure 47-92. Dual Edge Capture – Continuous mode to measure of the period between two consecutive rising edges

47.5.24.5 Read coherency mechanism

The Dual Edge Capture mode implements a read coherency mechanism between the FTM counter value captured in C(n)V and C(n+1)V registers. The read coherency mechanism is illustrated in the following figure. In this example, the channels (n) and (n +1) are in Dual Edge Capture – Continuous mode for positive polarity pulse width measurement. Thus, the channel (n) is configured to capture the FTM counter value when there is a rising edge at channel (n) input signal, and channel (n+1) to capture the FTM counter value when there is a falling edge at channel (n) input signal.

When a rising edge occurs in the channel (n) input signal, the FTM counter value is captured into channel (n) capture buffer. The channel (n) capture buffer value is transferred to C(n)V register when a falling edge occurs in the channel (n) input signal. C(n)V register has the FTM counter value when the previous rising edge occurred, and the channel (n) capture buffer has the FTM counter value when the last rising edge occurred.

When a falling edge occurs in the channel (n) input signal, the FTM counter value is captured into channel (n+1) capture buffer. The channel (n+1) capture buffer value is transferred to C(n+1)V register when the C(n)V register is read.

In the following figure, the read of C(n)V returns the FTM counter value when the event 1 occurred and the read of C(n+1)V returns the FTM counter value when the event 2 occurred.

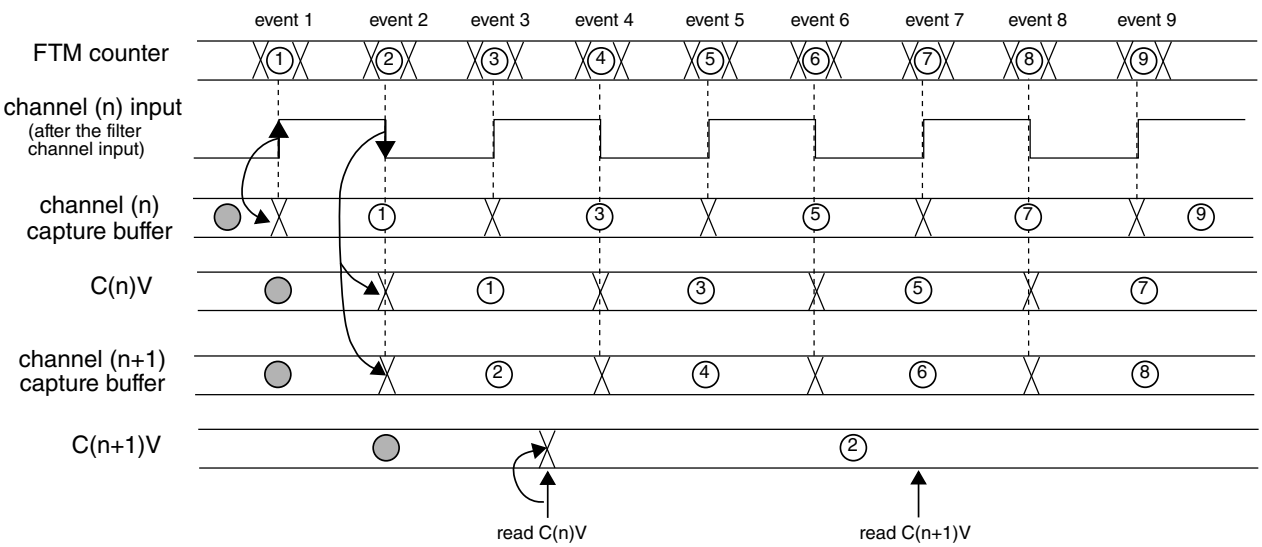


Figure 47-93. Dual Edge Capture mode read coherency mechanism

C(n)V register must be read prior to C(n+1)V register in dual edge capture one-shot and continuous modes for the read coherency mechanism works properly.

47.5.25 Quadrature Decoder mode

The Quadrature Decoder mode is selected if (QUADEN = 1). The Quadrature Decoder mode uses the input signals phase A and B to control the FTM counter increment and decrement. The following figure shows the quadrature decoder block diagram.

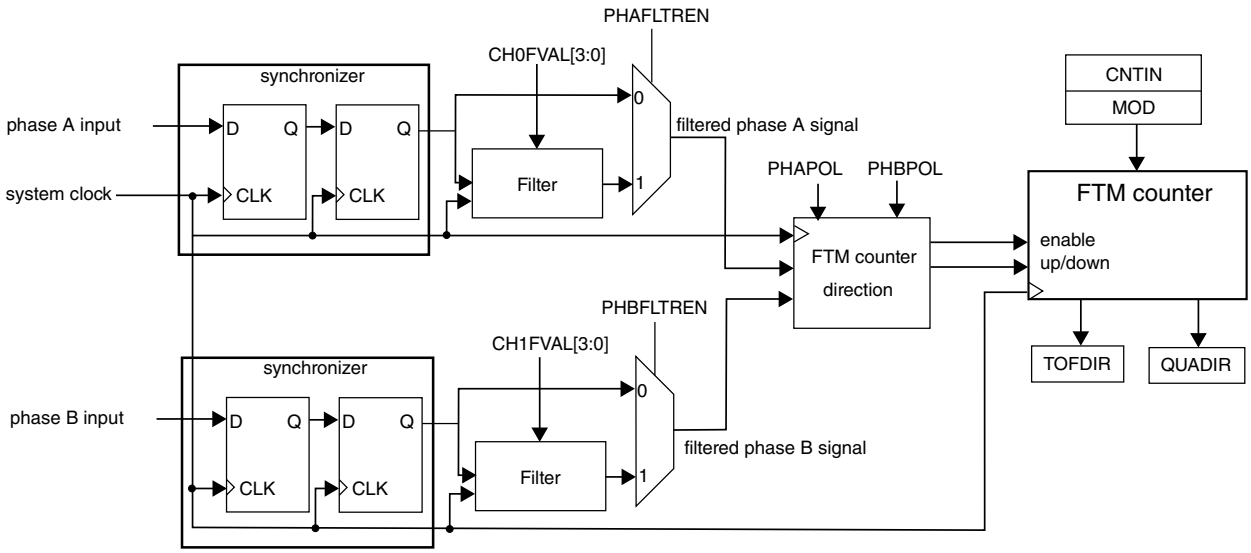


Figure 47-94. Quadrature Decoder block diagram

Each one of input signals phase A and B has a filter that is equivalent to the filter used in the channels input; Filter for Input Capture mode. The phase A input filter is enabled by PHAFLTREN bit and this filter's value is defined by CH0FVAL[3:0] bits (CH(n)FVAL[3:0] bits in FILTER0 register). The phase B input filter is enabled by PHBFLTREN bit and this filter's value is defined by CH1FVAL[3:0] bits (CH(n +1)FVAL[3:0] bits in FILTER0 register).

Except for CH0FVAL[3:0] and CH1FVAL[3:0] bits, no channel logic is used in Quadrature Decoder mode.

Note

Notice that the FTM counter is clocked by the phase A and B input signals when quadrature decoder mode is selected. Therefore it is expected that the Quadrature Decoder be used only with the FTM channels in input capture or output compare modes.

Note

An edge at phase A must not occur together an edge at phase B and vice-versa.

The PHAPOL bit selects the polarity of the phase A input, and the PHBPOL bit selects the polarity of the phase B input.

The QUADMODE selects the encoding mode used in the Quadrature Decoder mode. If QUADMODE = 1, then the count and direction encoding mode is enabled; see the following figure. In this mode, the phase B input value indicates the counting direction, and the phase A input defines the counting rate. The FTM counter is updated when there is a rising edge at phase A input signal.

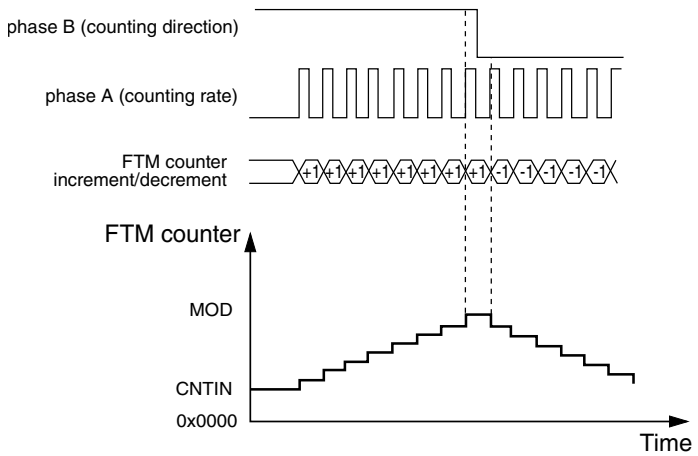


Figure 47-95. Quadrature Decoder – Count and Direction Encoding mode

If QUADMODE = 0, then the Phase A and Phase B Encoding mode is enabled; see the following figure. In this mode, the relationship between phase A and B signals indicates the counting direction, and phase A and B signals define the counting rate. The FTM counter is updated when there is an edge either at the phase A or phase B signals.

If PHAPOL = 0 and PHBPOL = 0, then the FTM counter increment happens when:

- there is a rising edge at phase A signal and phase B signal is at logic zero;
- there is a rising edge at phase B signal and phase A signal is at logic one;
- there is a falling edge at phase B signal and phase A signal is at logic zero;
- there is a falling edge at phase A signal and phase B signal is at logic one;

and the FTM counter decrement happens when:

- there is a falling edge at phase A signal and phase B signal is at logic zero;
- there is a falling edge at phase B signal and phase A signal is at logic one;
- there is a rising edge at phase B signal and phase A signal is at logic zero;
- there is a rising edge at phase A signal and phase B signal is at logic one.

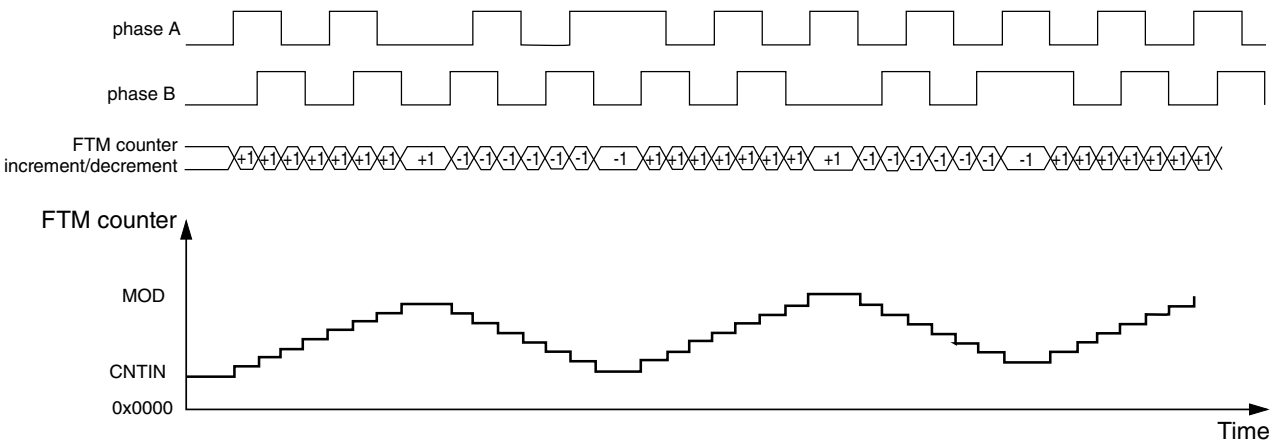


Figure 47-96. Quadrature Decoder – Phase A and Phase B Encoding mode

The following figure shows the FTM counter overflow in up counting. In this case, when the FTM counter changes from MOD to CNTIN, TOF and TOFDIR bits are set. TOF bit indicates the FTM counter overflow occurred. TOFDIR indicates the counting was up when the FTM counter overflow occurred.

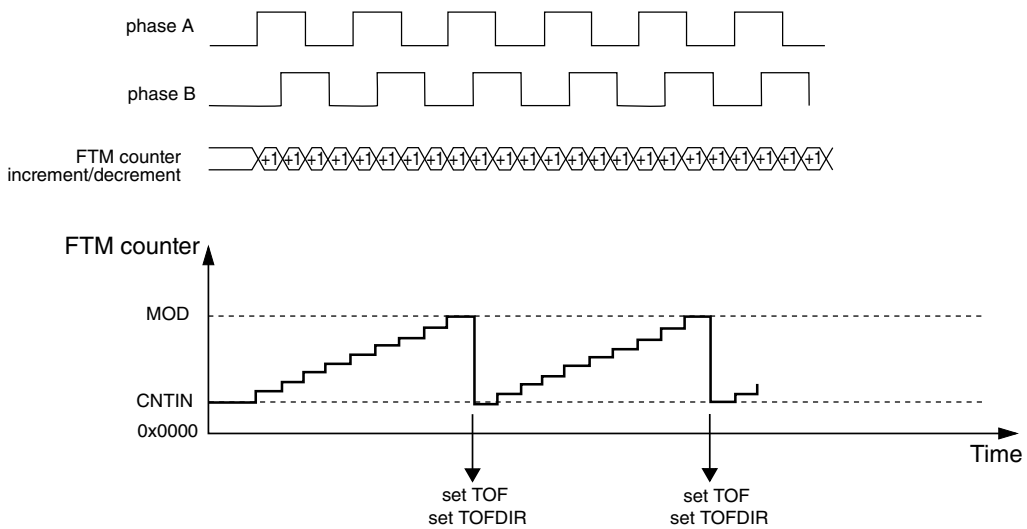


Figure 47-97. FTM Counter overflow in up counting for Quadrature Decoder mode

The following figure shows the FTM counter overflow in down counting. In this case, when the FTM counter changes from CNTIN to MOD, TOF bit is set and TOFDIR bit is cleared. TOF bit indicates the FTM counter overflow occurred. TOFDIR indicates the counting was down when the FTM counter overflow occurred.

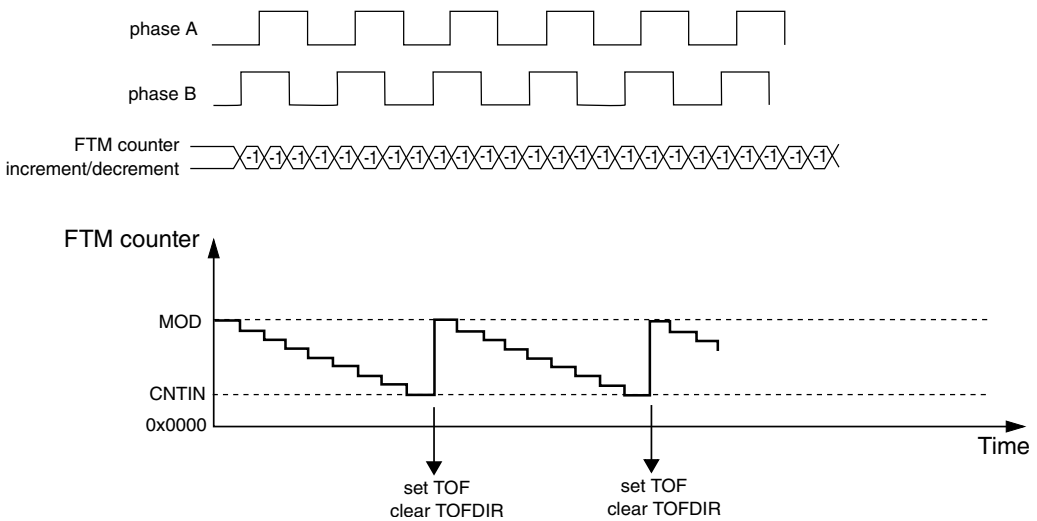


Figure 47-98. FTM counter overflow in down counting for Quadrature Decoder mode

47.5.25.1 Quadrature Decoder boundary conditions

The following figures show the FTM counter responding to motor jittering typical in motor position control applications.

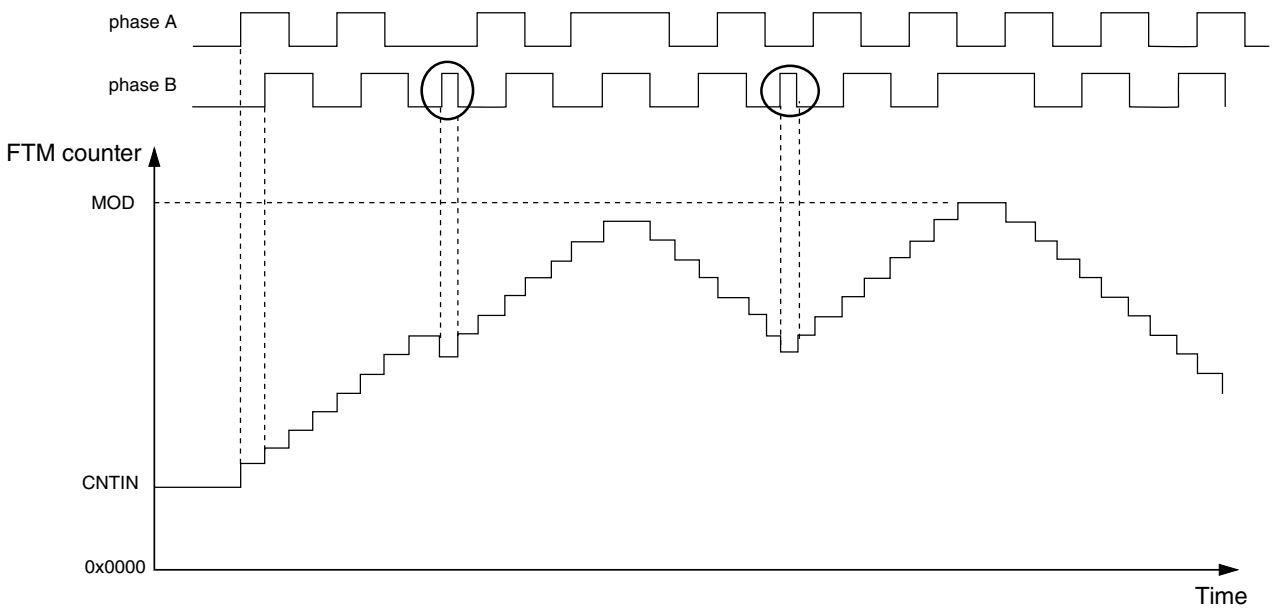


Figure 47-99. Motor position jittering in a mid count value

The following figure shows motor jittering produced by the phase B and A pulses respectively:

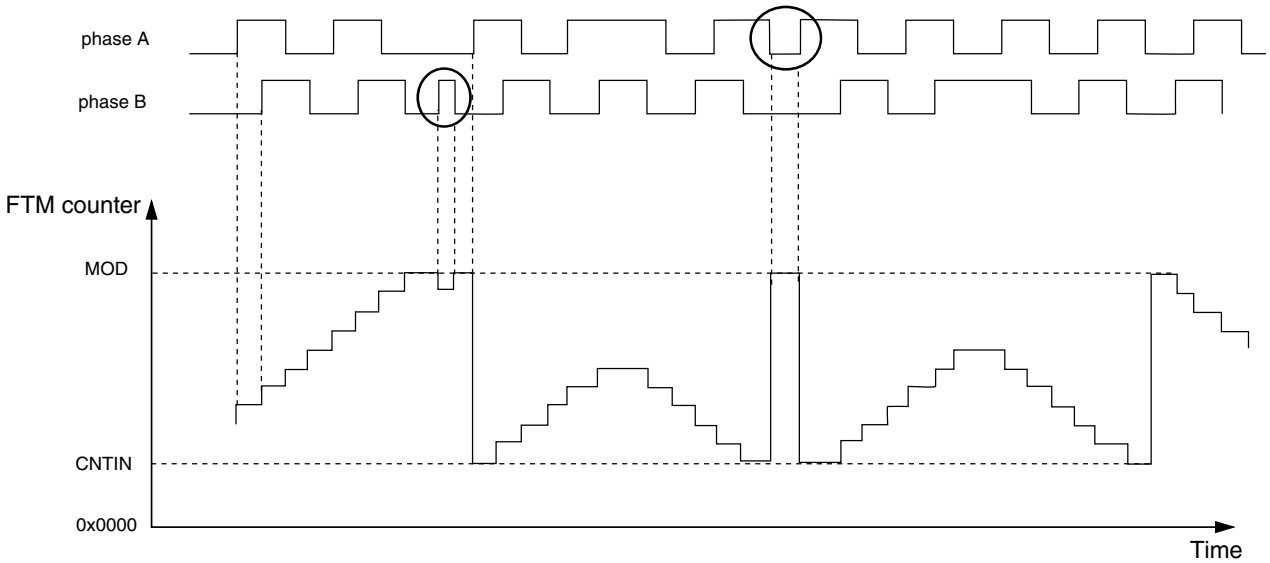


Figure 47-100. Motor position jittering near maximum and minimum count value

The first highlighted transition causes a jitter on the FTM counter value near the maximum count value (MOD). The second indicated transition occurs on phase A and causes the FTM counter transition between the maximum and minimum count values which are defined by MOD and CNTIN registers.

The appropriate settings of the phase A and phase B input filters are important to avoid glitches that may cause oscillation on the FTM counter value. The preceding figures show examples of oscillations that can be caused by poor input filter setup. Thus, it is important to guarantee a minimum pulse width to avoid these oscillations.

47.5.26 BDM mode

When the chip is in BDM mode, the BDMMODE[1:0] bits select the behavior of the FTM counter, the CH(n)F bit, the channels output, and the writes to the MOD, CNTIN, and C(n)V registers according to the following table.

Table 47-16. FTM behavior when the chip Is in BDM mode

BDMMODE	FTM Counter	CH(n)F Bit	FTM Channels Output	Writes to MOD, CNTIN, and C(n)V Registers
00	Stopped	can be set	Functional mode	Writes to these registers bypass the registers buffers
01	Stopped	is not set	The channels outputs are forced to their safe value according to POLn bit	Writes to these registers bypass the registers buffers
10	Stopped	is not set	The channels outputs are frozen when the chip enters in BDM mode	Writes to these registers bypass the registers buffers

Table continues on the next page...

Table 47-16. FTM behavior when the chip Is in BDM mode (continued)

BDMMODE	FTM Counter	CH(n)F Bit	FTM Channels Output	Writes to MOD, CNTIN, and C(n)V Registers
11	Functional mode	can be set	Functional mode	Functional mode

Note that if BDMMODE[1:0] = 2’b00 then the channels outputs remain at the value when the chip enters in BDM mode, because the FTM counter is stopped. However, the following situations modify the channels outputs in this BDM mode.

- Write any value to CNT register; see Counter reset. In this case, the FTM counter is updated with the CNTIN register value and the channels outputs are updated to the initial value – except for those channels set to Output Compare mode.
- FTM counter is reset by PWM Synchronization mode; see FTM counter synchronization. In this case, the FTM counter is updated with the CNTIN register value and the channels outputs are updated to the initial value – except for channels in Output Compare mode.
- In the channels outputs initialization, the channel (n) output is forced to the CH(n)OI bit value when the value 1 is written to INIT bit. See Initialization.

Note

The BDMMODE[1:0] = 2’b00 must not be used with the Fault control. Even if the fault control is enabled and a fault condition exists, the channels outputs values are updated as above.

Note

If CLKS[1:0] = 2'b00 in BDM, a non-zero value is written to CLKS in BDM, and CnV = CNTIN when the BDM is disabled, then the CHnF bit is set (since if the channel is a 0% EPWM signal) when the BDM is disabled.

47.5.27 Intermediate load

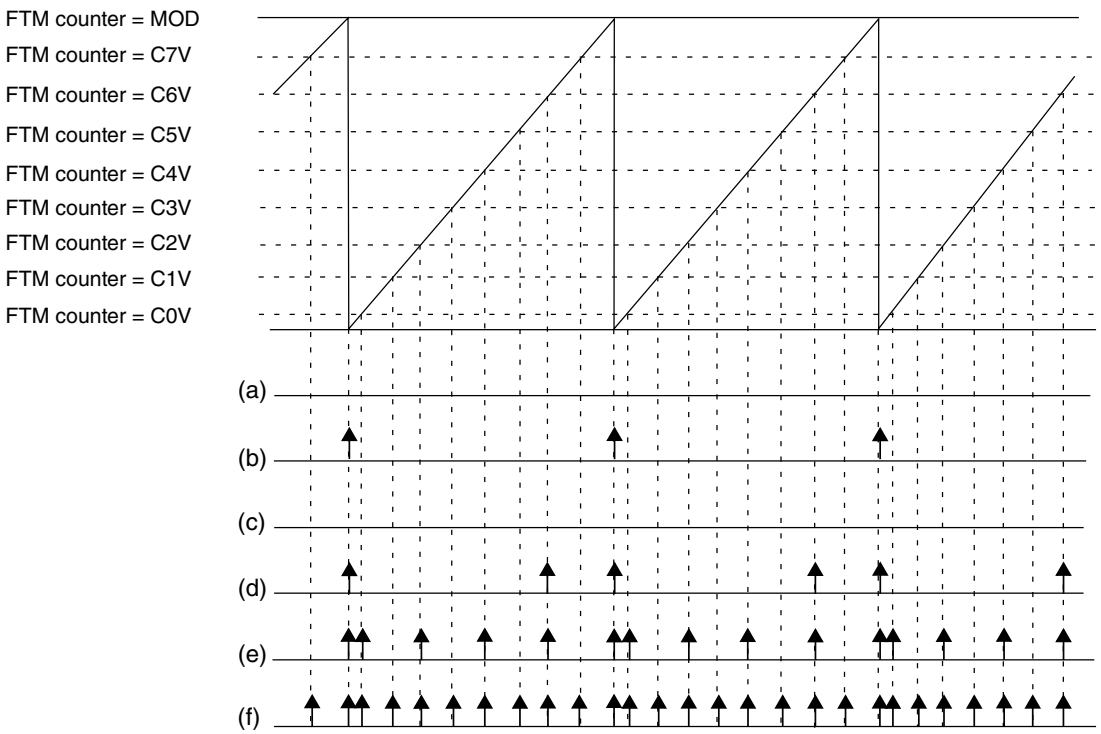
The PWMLOAD register allows to update the MOD, CNTIN, and C(n)V registers with the content of the register buffer at a defined load point. In this case, it is not required to use the PWM synchronization.

There are multiple possible loading points for intermediate load:

Table 47-17. When possible loading points are enabled

Loading point	Enabled
When the FTM counter wraps from MOD value to CNTIN value	Always
At the channel (j) match (FTM counter = C(j)V)	When CHjSEL = 1

The following figure shows some examples of enabled loading points.



NOTE

(a) LDOK = 0, CH0SEL = 0, CH1SEL = 0, CH2SEL = 0, CH3SEL = 0, CH4SEL = 0, CH5SEL = 0, CH6SEL = 0, CH7SEL = 0
(b) LDOK = 1, CH0SEL = 0, CH1SEL = 0, CH2SEL = 0, CH3SEL = 0, CH4SEL = 0, CH5SEL = 0, CH6SEL = 0, CH7SEL = 0
(c) LDOK = 0, CH0SEL = 0, CH1SEL = 0, CH2SEL = 0, CH3SEL = 1, CH4SEL = 0, CH5SEL = 0, CH6SEL = 0, CH7SEL = 0
(d) LDOK = 1, CH0SEL = 0, CH1SEL = 0, CH2SEL = 0, CH3SEL = 0, CH4SEL = 0, CH5SEL = 0, CH6SEL = 1, CH7SEL = 0
(e) LDOK = 1, CH0SEL = 1, CH1SEL = 0, CH2SEL = 1, CH3SEL = 0, CH4SEL = 1, CH5SEL = 0, CH6SEL = 1, CH7SEL = 0
(f) LDOK = 1, CH0SEL = 1, CH1SEL = 1, CH2SEL = 1, CH3SEL = 1, CH4SEL = 1, CH5SEL = 1, CH6SEL = 1, CH7SEL = 1

Figure 47-101. Loading points for intermediate load

After enabling the loading points, the LDOK bit must be set for the load to occur. In this case, the load occurs at the next enabled loading point according to the following conditions:

Table 47-18. Conditions for loads occurring at the next enabled loading point

When a new value was written	Then
To the MOD register	The MOD register is updated with its write buffer value.

Table continues on the next page...

Table 47-18. Conditions for loads occurring at the next enabled loading point (continued)

When a new value was written	Then
To the CNTIN register and CNTINC = 1	The CNTIN register is updated with its write buffer value.
To the C(n)V register and SYNCENm = 1 – where m indicates the pair channels (n) and (n+1)	The C(n)V register is updated with its write buffer value.
To the C(n+1)V register and SYNCENm = 1 – where m indicates the pair channels (n) and (n+1)	The C(n+1)V register is updated with its write buffer value.

NOTE

- If ELSjB and ELSjA bits are different from zero, then the channel (j) output signal is generated according to the configured output mode. If ELSjB and ELSjA bits are zero, then the generated signal is not available on channel (j) output.
- If CHjIE = 1, then the channel (j) interrupt is generated when the channel (j) match occurs.
- At the intermediate load neither the channels outputs nor the FTM counter are changed. Software must set the intermediate load at a safe point in time.

47.5.28 Global time base (GTB)

The global time base (GTB) is a FTM function that allows the synchronization of multiple FTM modules on a chip. The following figure shows an example of the GTB feature used to synchronize two FTM modules. In this case, the FTM A and B channels can behave as if just one FTM module was used, that is, a global time base.

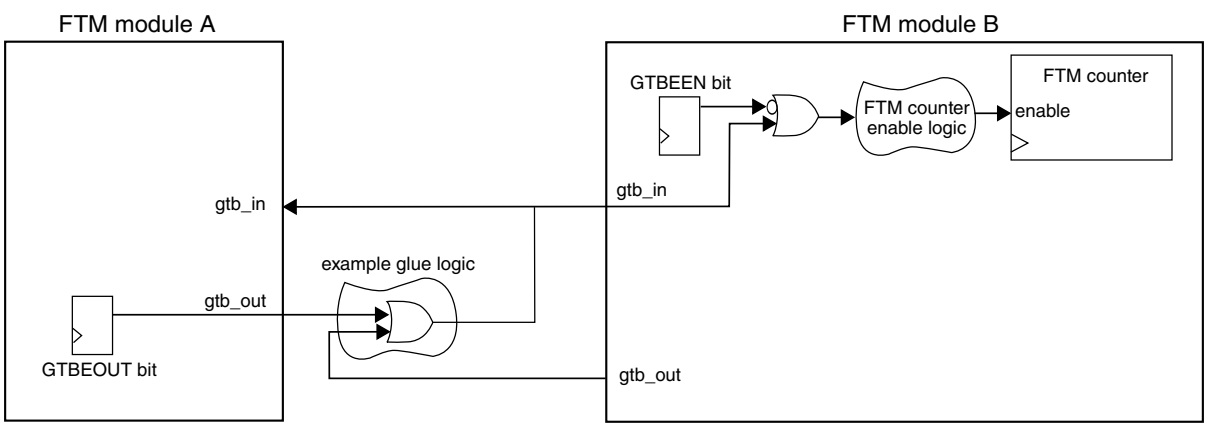


Figure 47-102. Global time base (GTB) block diagram

The GTB functionality is implemented by the GTBEEN and GTBEOUT bits in the CONF register, the input signal *gtb_in*, and the output signal *gtb_out*. The GTBEEN bit enables gtb_in to control the FTM counter enable signal:

- If GTBEEN = 0, each one of FTM modules works independently according to their configured mode.
- If GTBEEN = 1, the FTM counter update is enabled only when gtb_in is 1.

In the configuration described in the preceding figure, FTM modules A and B have their FTM counters enabled if at least one of the gtb_out signals from one of the FTM modules is 1. There are several possible configurations for the interconnection of the gtb_in and gtb_out signals, represented by the example glue logic shown in the figure. Note that these configurations are chip-dependent and implemented outside of the FTM modules. See the chip-specific FTM information for the chip's specific implementation.

NOTE

- In order to use the GTB signals to synchronize the FTM counter of different FTM modules, the configuration of each FTM module should guarantee that its FTM counter starts counting as soon as the gtb_in signal is 1.
- The GTB feature does not provide continuous synchronization of FTM counters, meaning that the FTM counters may lose synchronization during FTM operation. The GTB feature only allows the FTM counters to *start* their operation synchronously.

47.5.28.1 Enabling the global time base (GTB)

To enable the GTB feature, follow these steps for each participating FTM module:

1. Stop the FTM counter: Write 00b to SC[CLKS].
2. Program the FTM to the intended configuration. The FTM counter mode needs to be consistent across all participating modules.
3. Write 1 to CONF[GTBEEN] and write 0 to CONF[GTBEOUT] at the same time.
4. Select the intended FTM counter clock source in SC[CLKS]. The clock source needs to be consistent across all participating modules.
5. Reset the FTM counter: Write any value to the CNT register.

To initiate the GTB feature in the configuration described in the preceding figure, write 1 to CONF[GTBEOUT] in the FTM module used as the time base.

47.6 Reset overview

The FTM is reset whenever any chip reset occurs.

When the FTM exits from reset:

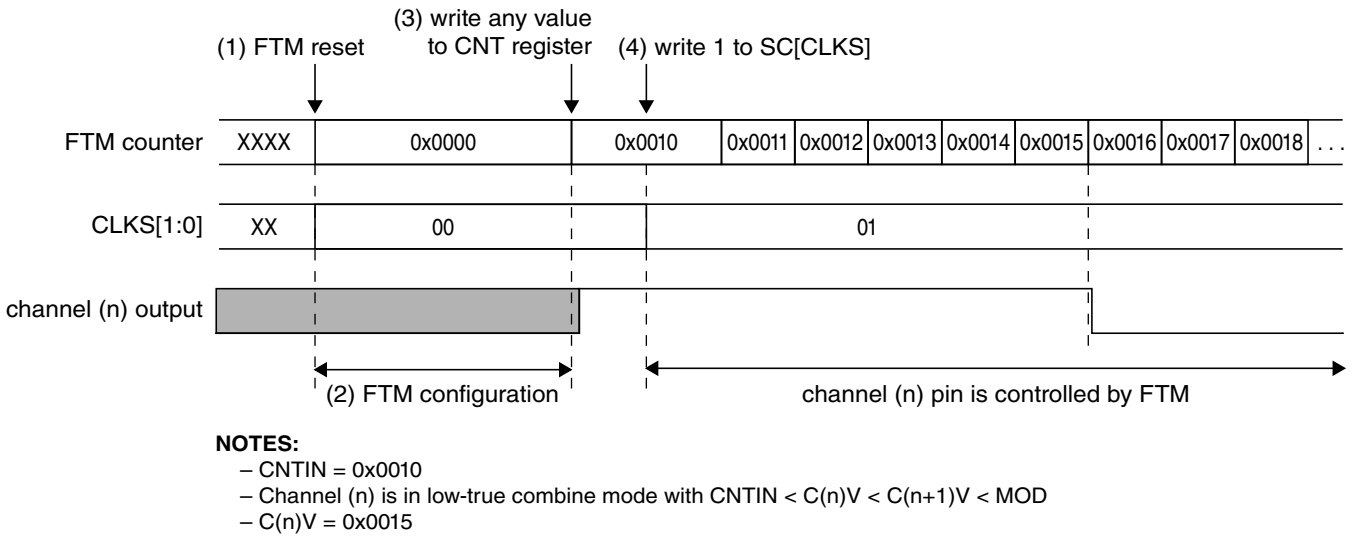
- the FTM counter and the prescaler counter are zero and are stopped (CLKS[1:0] = 00b);
- the timer overflow interrupt is zero, see Timer Overflow Interrupt;
- the channels interrupts are zero, see Channel (n) Interrupt;
- the fault interrupt is zero, see Fault Interrupt;
- the channels are in input capture mode, see Input Capture mode;
- the channels outputs are zero;
- the channels pins are not controlled by FTM (ELS(n)B:ELS(n)A = 0:0) (See the table in the description of CnSC register).

The following figure shows the FTM behavior after the reset. At the reset (item 1), the FTM counter is disabled (see the description of the CLKS field in the Status and Control register), its value is updated to zero and the pins are not controlled by FTM (See the table in the description of CnSC register).

After the reset, the FTM should be configurated (item 2). It is necessary to define the FTM counter mode, the FTM counting limits (MOD and CNTIN registers value), the channels mode and CnV registers value according to the channels mode.

Thus, it is recommended to write any value to CNT register (item 3). This write updates the FTM counter with the CNTIN register value and the channels output with its initial value (except for channels in output compare mode) (Counter reset).

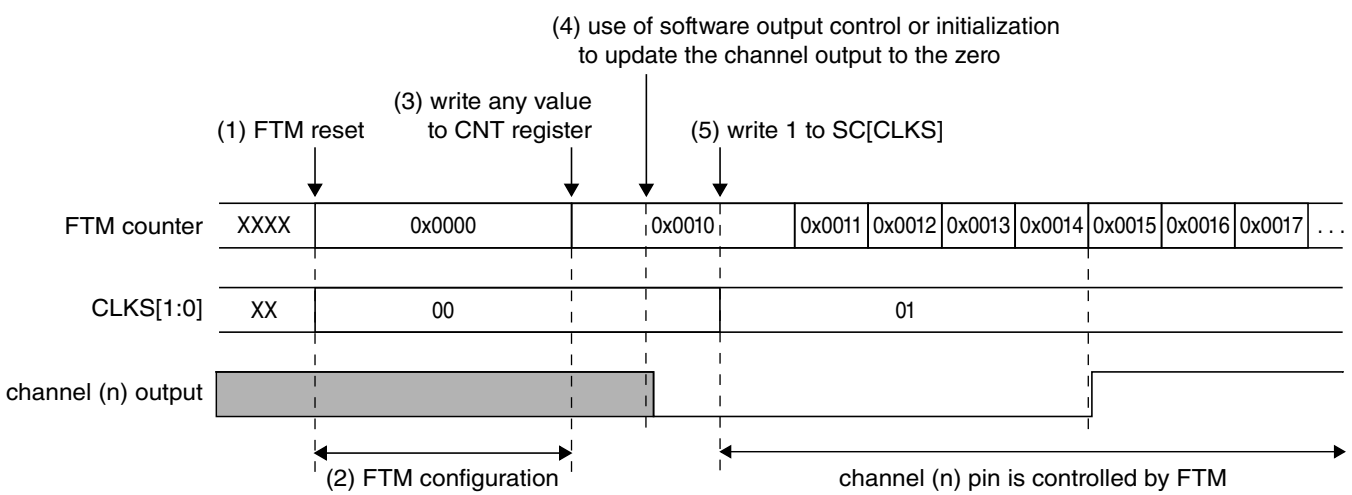
The next step is to select the FTM counter clock by the CLKS[1:0] bits (item 4). It is important to highlight that the pins are only controlled by FTM when CLKS[1:0] bits are different from zero (See the table in the description of CnSC register).



NOTES:
– CNTIN = 0x0010
– Channel (n) is in low-true combine mode with CNTIN < C(n)V < C(n+1)V < MOD
– C(n)V = 0x0015

Figure 47-103. FTM behavior after reset when the channel (n) is in Combine mode

The following figure shows an example when the channel (n) is in Output Compare mode and the channel (n) output is toggled when there is a match. In the Output Compare mode, the channel output is not updated to its initial value when there is a write to CNT register (item 3). In this case, use the software output control (Software output control) or the initialization (Initialization) to update the channel output to the selected value (item 4).



NOTES:
– CNTIN = 0x0010
– Channel (n) is in output compare and the channel (n) output is toggled when there is a match
– C(n)V = 0x0014

Figure 47-104. FTM behavior after reset when the channel (n) is in Output Compare mode

47.7 FTM Interrupts

47.7.1 Timer Overflow Interrupt

The timer overflow interrupt is generated when (TOIE = 1) and (TOF = 1).

47.7.2 Channel (n) Interrupt

The channel (n) interrupt is generated when (CHnIE = 1) and (CHnF = 1).

47.7.3 Fault Interrupt

The fault interrupt is generated when (FAULTIE = 1) and (FAULTF = 1).

47.8 Initialization Procedure

The following initialization procedure is recommended to configure the FlexTimer operation. This procedure can also be used to do a new configuration of the FlexTimer operation.

- Define the POL bits.
- Mask the channels outputs using SYNCHOM = 0. Two clocks after the write to OUTMASK, the channels output are in the safe value.
- (Re)Configuration FTM counter and channels to generation of periodic signals - Disable the clock. If the selected mode is Quadrature Decoder, then disable this mode. Examples of the (re)configuration:
  - Write to MOD.
  - Write to CNTIN.
  - Select OC, EPWM, CPWM, Combine, Complement modes for all channels that will be used
  - Select the high-true and low-true channels modes.
  - Write to CnV for all channels that will be used .
  - (Re)Configure deadtime and fault control.
  - Do not use the SWOC without SW synchronization (see item 6).
  - Do not use the Inverting without SW synchronization (see item 6).
  - Do not use the Initialization.
  - Do not change the polarity control.
  - Do not configure the HW synchronization

- Write any value to CNT. The FTM Counter is reset and the channels output are updated according to new configuration.
- Enable the clock. Write to CLKS[1:0] bits a value different from zero. If in the Quadrature Decoder mode, enable this mode.
- Configure the SW synchronization for SWOC (if it is necessary), Inverting (if it is necessary) and Output Mask (always)
  - Select synchronization for Output Mask Write to SYNC (SWSYNC = 0, TRIG2 = 0, TRIG1 = 0, TRIG0 = 0, SYNCHOM = 1, REINIT = 0, CNTMAX = 0, CNTMIN = 0)
  - Write to SYNCONF.
    - HW Synchronization can not be enabled (HWSOC = 0, HWINVC = 0, HWOM = 0, HWWRBUF = 0, HWRSTCNT = 0, HWTRIGMODE = 0).
    - SW Synchronization for SWOC (if it is necessary): SWSOC = [0/1] and SWOC = [0/1].
    - SW Synchronization for Inverting (if it is necessary): SWINVC = [0/1] and INVC = [0/1].
    - SW Synchronization for SWOM (always): SWOM = 1. No enable the SW Synchronization for write buffers (because the writes to registers with write buffer are done using CLKS[1:0] = 2’b00): SWWRBUF = 0 and CNTINC = 0 .
    - SW Synchronization for counter reset (always): SWRSTCNT = 1.
    - Enhanced synchronization (always): SYNCMODE = 1
  - If the SWOC is used (SWSOC = 1 and SWOC = 1), then write to SWOCTRL register.
  - If the Inverting is used (SWINVC = 1 and INVC = 1), then write to INVCTRL register.
  - Write to OUTMASK to enable the masked channels.
- Generate the Software Trigger Write to SYNC (SWSYNC = 1, TRIG2 = 0, TRIG1 = 0, TRIG0 = 0, SYNCHOM = 1, REINIT = 0, CNTMAX = 0, CNTMIN = 0)

Chapter 48
Timer/PWM Module (TPM)

48.1 Chip-specific TPM information

48.1.1 TPM Instantiation Information

This device contains 2 Low Power TPM module(s) (TPM). All TPM modules in the device are configured with basic TPM functionality with quadrature decoder function and all can be functional in Stop/VLPS mode. The clock source is either external or internal in Stop/VLPS mode.

The following table shows how these modules are configured.

Table 48-1. TPM configuration

TPM instance	Number of channels	Features/usage
TPM1	2	Basic TPM,functional in Stop/VLPS mode
TPM2	2	Basic TPM,functional in Stop/VLPS mode

48.1.2 Clock Options

The TPM blocks are clocked from a single TPM clock that can be selected from OSCERCLK, MCGIRCLK , MCGPLLCLK, or MCGFLLCLK. The selected source is controlled by SIM_SOPT2[TPMSRC] and SIM_SOPT2[PLLFLLSEL]control registers.

Each TPM also supports an external clock mode (TPM_SC[CMOD]=1x) in which the counter increments after a synchronized (to the selected TPM clock source) rising edge detect of an external clock input. The available external clock (either TPM_CLKIN0 or

TPM_CLKIN1) is selected by SIM_SOPT9[TPMxCLKSEL] control register. To guarantee valid operation the selected external clock must be less than half the frequency of the selected TPM clock source.

48.1.3 Trigger Options

Each TPM has a selectable trigger input source controlled by the TPMx_CONF[TRGSEL] field to use for starting the counter and/or reloading the counter. The options available are shown in the following table.

Table 48-2. TPM trigger options

TPMx_CONF[TRGSEL]	Selected source
0000	External Trigger
0001	CMP 0
0010	CMP 1Reserved
0011	Reserved
0100	PIT Ch 0 Output
0101	PIT Ch 1 Output
0110	PIT Ch 2 Output
0111	PIT Ch 3 Output
1000	FTM0 initialization trigger and channel triggers, as programmed in the FTM external trigger register (EXTTRIG)
1001	FTM1 initialization trigger and channel triggers, as programmed in the FTM external trigger register (EXTTRIG)
1010	FTM2 initialization trigger and channel triggers, as programmed in the FTM external trigger register (EXTTRIG)
1011	FTM3 initialization trigger and channel triggers, as programmed in the FTM external trigger register (EXTTRIG)
1100	RTC Alarm
1101	RTC Seconds
1110	LPTMR Output
1111	Software Trigger

48.1.4 Global Timebase

Each TPM has a global timebase feature controlled by the TPMx_CONF[GTBEEN] bit. TPM1 is configured as the global time when this option is enabled.

48.1.5 TPM Interrupts

The TPM has multiple sources of interrupt. However, these sources are OR'd together to generate a single interrupt request to the interrupt controller. When an TPM interrupt occurs, read the TPM status registers to determine the exact interrupt source.

48.2 Introduction

The TPM (Timer/PWM Module) is a 2- to 8-channel timer which supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications.

The counter, compare and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes. An example of using the TPM with the asynchronous DMA is described in AN4631:Using the Asynchronous DMA features of the Kinetis L Series .

48.2.1 TPM Philosophy

The TPM is built upon a very simple timer (HCS08 Timer PWM Module – TPM) used for many years on Freescale's 8-bit microcontrollers. The TPM extends the functionality to support operation in low power modes by clocking the counter, compare and capture registers from an asynchronous clock that can remain functional in low power modes.

48.2.2 Features

The TPM features include:

- TPM clock mode is selectable
  - Can increment on every edge of the asynchronous counter clock
  - Can increment on rising edge of an external clock input synchronized to the asynchronous counter clock
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- TPM includes a 16-bit counter
  - It can be a free-running counter or modulo counter
  - The counting can be up or up-down

- Includes 2 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
  - In input capture mode the capture can occur on rising edges, falling edges or both edges
  - In output compare mode the output signal can be set, cleared, pulsed, or toggled on match
  - All channels can be configured for edge-aligned PWM mode or center-aligned PWM mode
- Support the generation of an interrupt and/or DMA request per channel
- Support the generation of an interrupt and/or DMA request when the counter overflows
- Support selectable trigger input to optionally reset or cause the counter to start incrementing.
  - The counter can also optionally stop incrementing on counter overflow
- Support the generation of hardware triggers when the counter overflows and per channel

48.2.3 Modes of operation

During debug mode, the TPM can can be configured to temporarily pause all counting until the core returns to normal user operating mode or to operate normally. When the counter is paused, trigger inputs and input capture events are ignored.

During doze mode, the TPM can be configured to operate normally or to pause all counting for the duration of doze mode. When the counter is paused, trigger inputs and input capture events are ignored.

During stop mode, the TPM counter clock can remain functional and the TPM can generate an asynchronous interrupt to exit the MCU from stop mode.

48.2.4 Block diagram

The TPM uses one input/output (I/O) pin per channel, CHn (TPM channel (n)) where n is the channel number.

The following figure shows the TPM structure. The central component of the TPM is the 16-bit counter with programmable final value and its counting can be up or up-down.

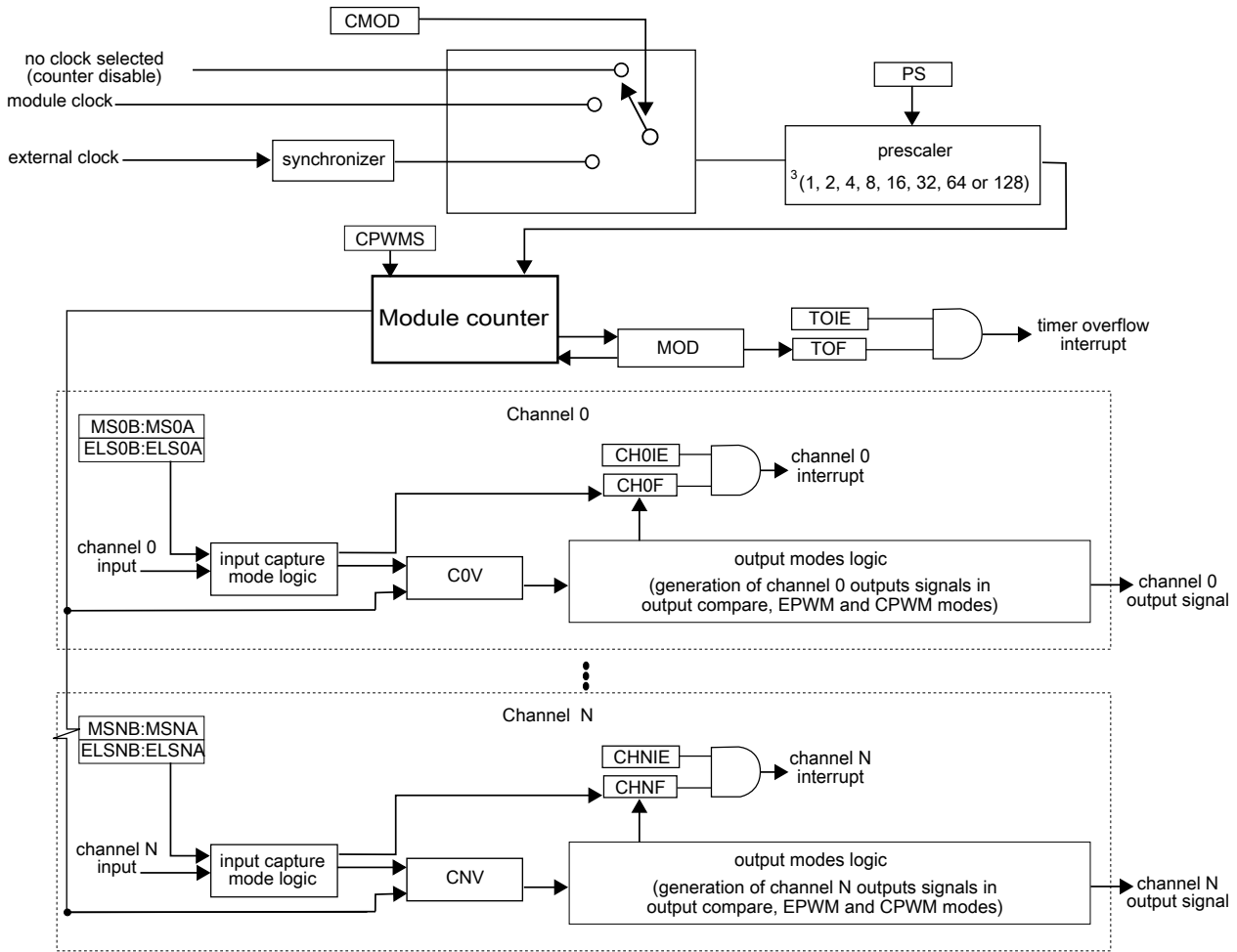


Figure 48-1. TPM block diagram

48.3 TPM Signal Descriptions

Table 48-3 shows the user-accessible signals for the TPM.

Table 48-3. TPM signal descriptions

Signal	Description	I/O
TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM_CHn	TPM channel (n = 1 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

48.3.1 TPM_EXTCLK — TPM External Clock

The rising edge of the external input signal is used to increment the TPM counter if selected by CMOD[1:0] bits in the SC register. This input signal must be less than half of the TPM counter clock frequency. The TPM counter prescaler selection and settings are also used when an external input is selected.

48.3.2 TPM_CHn — TPM Channel (n) I/O Pin

Each TPM channel can be configured to operate either as input or output. The direction associated with each channel, input or output, is selected according to the mode assigned for that channel.

48.4 Memory Map and Register Definition

This section provides a detailed description of all TPM registers.

Attempting to access a reserved register location in the TPM memory map will generate a bus error.

TPM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400C_9000	Status and Control (TPM1_SC)	32	R/W	0000_0000h	48.4.1/1592
400C_9004	Counter (TPM1_CNT)	32	R/W	0000_0000h	48.4.2/1593
400C_9008	Modulo (TPM1_MOD)	32	R/W	0000_FFFFh	48.4.3/1594
400C_900C	Channel (n) Status and Control (TPM1_C0SC)	32	R/W	0000_0000h	48.4.4/1595
400C_9010	Channel (n) Value (TPM1_C0V)	32	R/W	0000_0000h	48.4.5/1597
400C_9014	Channel (n) Status and Control (TPM1_C1SC)	32	R/W	0000_0000h	48.4.4/1595
400C_9018	Channel (n) Value (TPM1_C1V)	32	R/W	0000_0000h	48.4.5/1597
400C_9050	Capture and Compare Status (TPM1_STATUS)	32	R/W	0000_0000h	48.4.6/1597
400C_9064	Combine Channel Register (TPM1_COMBINE)	32	R/W	0000_0000h	48.4.7/1599
400C_9070	Channel Polarity (TPM1_POL)	32	R/W	0000_0000h	48.4.8/1600
400C_9078	Filter Control (TPM1_FILTER)	32	R/W	0000_0000h	48.4.9/1600
400C_9080	Quadrature Decoder Control and Status (TPM1_QDCTRL)	32	R/W	0000_0000h	48.4.10/ 1601
400C_9084	Configuration (TPM1_CONF)	32	R/W	0000_0000h	48.4.11/ 1603

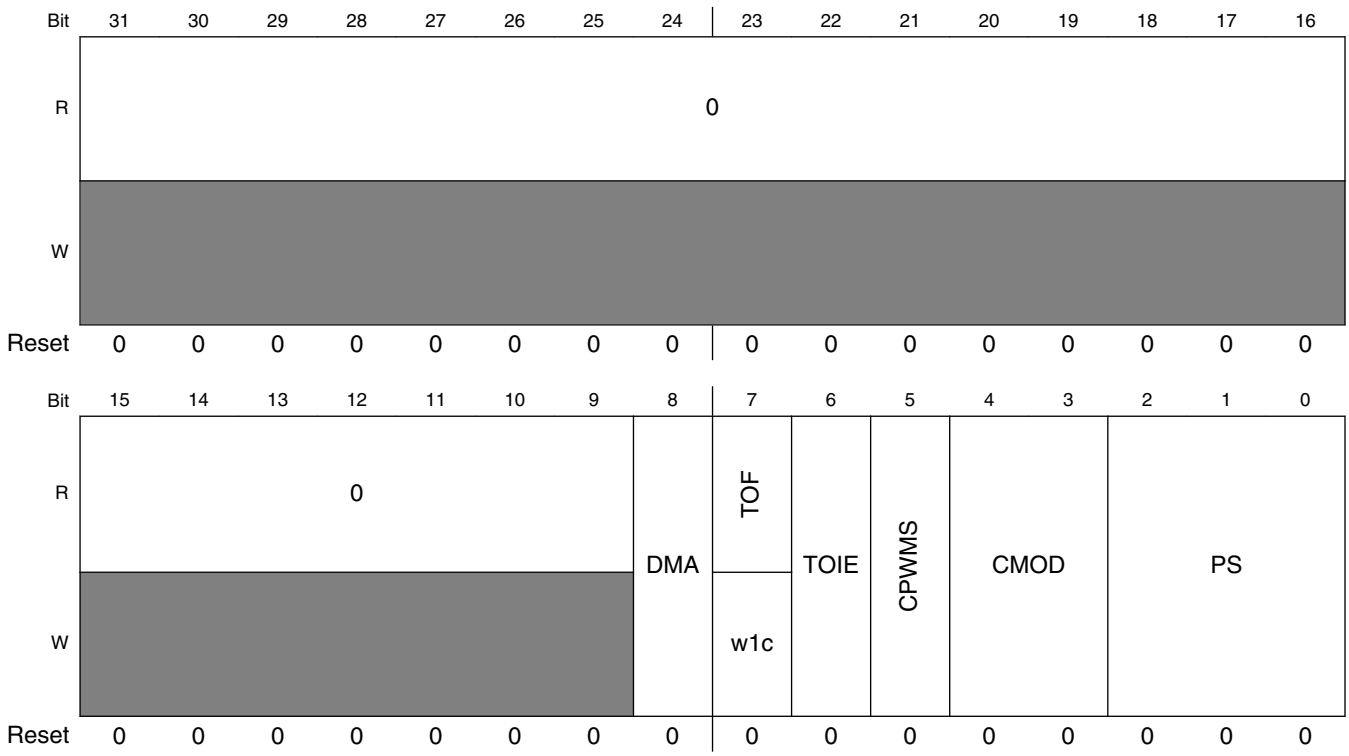
TPM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400C_A000	Status and Control (TPM2_SC)	32	R/W	0000_0000h	48.4.1/1592
400C_A004	Counter (TPM2_CNT)	32	R/W	0000_0000h	48.4.2/1593
400C_A008	Modulo (TPM2_MOD)	32	R/W	0000_FFFFh	48.4.3/1594
400C_A00C	Channel (n) Status and Control (TPM2_C0SC)	32	R/W	0000_0000h	48.4.4/1595
400C_A010	Channel (n) Value (TPM2_C0V)	32	R/W	0000_0000h	48.4.5/1597
400C_A014	Channel (n) Status and Control (TPM2_C1SC)	32	R/W	0000_0000h	48.4.4/1595
400C_A018	Channel (n) Value (TPM2_C1V)	32	R/W	0000_0000h	48.4.5/1597
400C_A050	Capture and Compare Status (TPM2_STATUS)	32	R/W	0000_0000h	48.4.6/1597
400C_A064	Combine Channel Register (TPM2_COMBINE)	32	R/W	0000_0000h	48.4.7/1599
400C_A070	Channel Polarity (TPM2_POL)	32	R/W	0000_0000h	48.4.8/1600
400C_A078	Filter Control (TPM2_FILTER)	32	R/W	0000_0000h	48.4.9/1600
400C_A080	Quadrature Decoder Control and Status (TPM2_QDCTRL)	32	R/W	0000_0000h	48.4.10/ 1601
400C_A084	Configuration (TPM2_CONF)	32	R/W	0000_0000h	48.4.11/ 1603

48.4.1 Status and Control (TPMx_SC)

SC contains the overflow status flag and control bits used to configure the interrupt enable, module configuration and prescaler factor. These controls relate to all channels within this module.

Address: Base address + 0h offset



TPMx_SC field descriptions

Field	Description
31–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 DMA	DMA Enable Enables DMA transfers for the overflow flag. 0 Disables DMA transfers. 1 Enables DMA transfers.
7 TOF	Timer Overflow Flag Set by hardware when the TPM counter equals the value in the MOD register and increments. Writing a 1 to TOF clears it. Writing a 0 to TOF has no effect. If another TPM overflow occurs between the flag setting and the flag clearing, the write operation has no effect; therefore, TOF remains set indicating another overflow has occurred. In this case a TOF interrupt request is not lost due to a delay in clearing the previous TOF.

Table continues on the next page...

TPMx_SC field descriptions (continued)

Field	Description
	0 TPM counter has not overflowed. 1 TPM counter has overflowed.
6 TOIE	Timer Overflow Interrupt Enable Enables TPM overflow interrupts. 0 Disable TOF interrupts. Use software polling or DMA request. 1 Enable TOF interrupts. An interrupt is generated when TOF equals one.
5 CPWMS	Center-Aligned PWM Select Selects CPWM mode. This mode configures the TPM to operate in up-down counting mode. This field is write protected. It can be written only when the counter is disabled. 0 TPM counter operates in up counting mode. 1 TPM counter operates in up-down counting mode.
4–3 CMOD	Clock Mode Selection Selects the TPM counter clock modes. When disabling the counter, this field remain set until acknolwedged in the TPM clock domain. 00 TPM counter is disabled 01 TPM counter increments on every TPM counter clock 10 TPM counter increments on rising edge of TPM_EXTCLK synchronized to the TPM counter clock 11 Reserved.
PS	Prescale Factor Selection Selects one of 8 division factors for the clock mode selected by CMOD. This field is write protected. It can be written only when the counter is disabled. 000 Divide by 1 001 Divide by 2 010 Divide by 4 011 Divide by 8 100 Divide by 16 101 Divide by 32 110 Divide by 64 111 Divide by 128

48.4.2 Counter (TPMx_CNT)

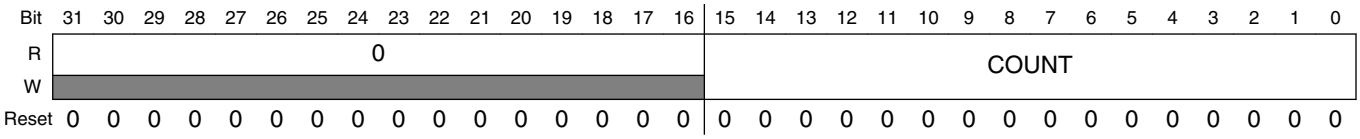
The CNT register contains the TPM counter value.

Reset clears the CNT register. Writing any value to COUNT also clears the counter.

When debug is active, the TPM counter does not increment unless configured otherwise.

Reading the CNT register adds two wait states to the register access due to synchronization delays.

Address: Base address + 4h offset



TPMx_CNT field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
COUNT	Counter value

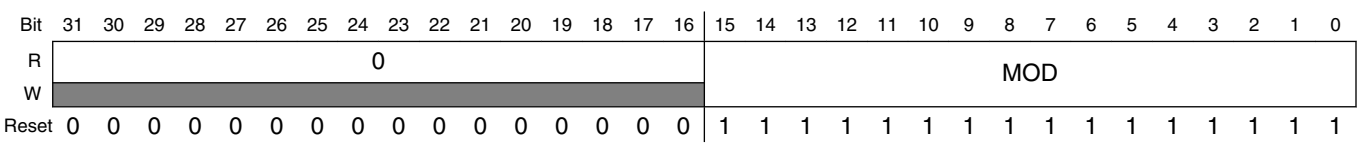
48.4.3 Modulo (TPMx_MOD)

The Modulo register contains the modulo value for the TPM counter. When the TPM counter reaches the modulo value and increments, the overflow flag (TOF) is set and the next value of TPM counter depends on the selected counting method (see Counter).

Writing to the MOD register latches the value into a buffer. The MOD register is updated with the value of its write buffer according to MOD Register Update . Additional writes to the MOD write buffer are ignored until the register has been updated.

It is recommended to initialize the TPM counter (write to CNT) before writing to the MOD register to avoid confusion about when the first counter overflow will occur.

Address: Base address + 8h offset



TPMx_MOD field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
MOD	Modulo value This field must be written with single 16-bit or 32-bit access.

48.4.4 Channel (n) Status and Control (TPMx_C*n*SC)

CnSC contains the channel-interrupt-status flag and control bits used to configure the interrupt enable, channel configuration, and pin function. When switching from one channel mode to a different channel mode, the channel must first be disabled and this must be acknowledged in the TPM counter clock domain.

Table 48-4. Mode, Edge, and Level Selection

CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
X	00	00	None	Channel disabled
X	01	00	Software compare	Pin not used for TPM
0	00	01	Input capture	Capture on Rising Edge Only
		10		Capture on Falling Edge Only
		11		Capture on Rising or Falling Edge
	01	01	Output compare	Toggle Output on match
		10		Clear Output on match
		11		Set Output on match
	10	10	Edge-aligned PWM	High-true pulses (clear Output on match, set Output on reload)
		X1		Low-true pulses (set Output on match, clear Output on reload)
	11	10	Output compare	Pulse Output low on match
		01		Pulse Output high on match
1	10	10	Center-aligned PWM	High-true pulses (clear Output on match-up, set Output on match-down)
		01		Low-true pulses (set Output on match-up, clear Output on match-down)

Address: Base address + Ch offset + (8d × i), where i=0d to 1d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								CHF	CHIE	MSB	MSA	ELSB	ELSA	0	DMA
W									w1c							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TPMx_CnSC field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 CHF	Channel Flag Set by hardware when an event occurs on the channel. CHF is cleared by writing a 1 to the CHF bit. Writing a 0 to CHF has no effect. If another event occurs between the CHF sets and the write operation, the write operation has no effect; therefore, CHF remains set indicating another event has occurred. In this case a CHF interrupt request is not lost due to the delay in clearing the previous CHF. 0 No channel event has occurred. 1 A channel event has occurred.
6 CHIE	Channel Interrupt Enable Enables channel interrupts. 0 Disable channel interrupts. 1 Enable channel interrupts.
5 MSB	Channel Mode Select Used for further selections in the channel logic. Its functionality is dependent on the channel mode. When a channel is disabled, this field will not change state until acknowledged in the TPM counter clock domain.
4 MSA	Channel Mode Select Used for further selections in the channel logic. Its functionality is dependent on the channel mode. When a channel is disabled, this field will not change state until acknowledged in the TPM counter clock domain.
3 ELSB	Edge or Level Select The functionality of ELSB and ELSA depends on the channel mode. When a channel is disabled, this field will not change state until acknowledged in the TPM counter clock domain.
2 ELSA	Edge or Level Select The functionality of ELSB and ELSA depends on the channel mode. When a channel is disabled, this field will not change state until acknowledged in the TPM counter clock domain.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 DMA	DMA Enable Enables DMA transfers for the channel. 0 Disable DMA transfers. 1 Enable DMA transfers.

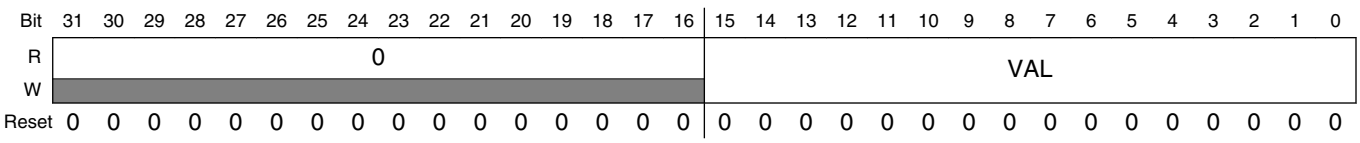
48.4.5 Channel (n) Value (TPMx_CnV)

These registers contain the captured TPM counter value for the input modes or the match value for the output modes.

In input capture mode, any write to a CnV register is ignored.

In compare modes, writing to a CnV register latches the value into a buffer. A CnV register is updated with the value of its write buffer according to CnV Register Update . Additional writes to the CnV write buffer are ignored until the register has been updated.

Address: Base address + 10h offset + (8d × i), where i=0d to 1d



TPMx_CnV field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
VAL	Channel Value Captured TPM counter value of the input modes or the match value for the output modes. This field must be written with single 16-bit or 32-bit access.

48.4.6 Capture and Compare Status (TPMx_STATUS)

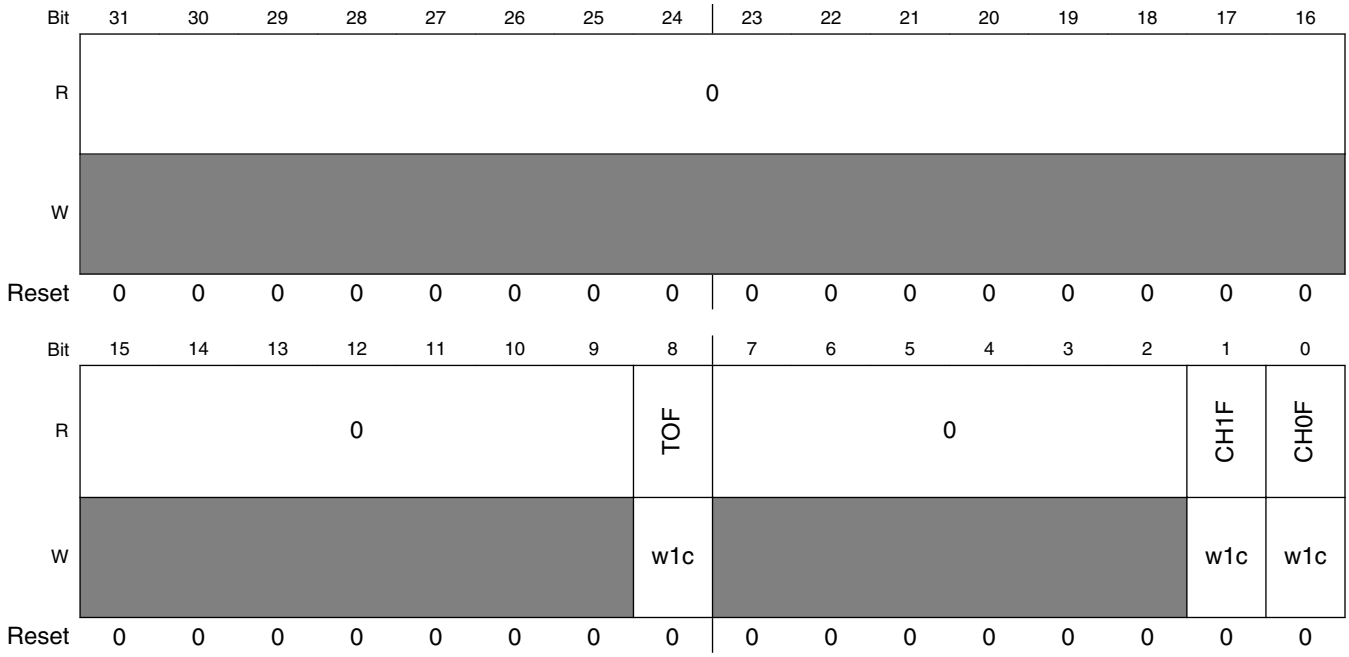
The STATUS register contains a copy of the status flag, CnSC[CHnF] for each TPM channel, as well as SC[TOF], for software convenience.

Each CHnF bit in STATUS is a mirror of CHnF bit in CnSC. All CHnF bits can be checked using only one read of STATUS. All CHnF bits can be cleared by writing all ones to STATUS.

Hardware sets the individual channel flags when an event occurs on the channel. Writing a 1 to CHF clears it. Writing a 0 to CHF has no effect.

If another event occurs between the flag setting and the write operation, the write operation has no effect; therefore, CHF remains set indicating another event has occurred. In this case a CHF interrupt request is not lost due to the clearing sequence for a previous CHF.

Address: Base address + 50h offset



TPMx_STATUS field descriptions

Field	Description
31–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 TOF	Timer Overflow Flag See register description 0 TPM counter has not overflowed. 1 TPM counter has overflowed.
7–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 CH1F	Channel 1 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
0 CH0F	Channel 0 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.

48.4.7 Combine Channel Register (TPMx_COMBINE)

This register contains the control bits used to configure the combine channel modes for each pair of channels (n) and (n+1), where n is all the even numbered channels.

Address: Base address + 64h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								0						COMSWAP0	COMBINE0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TPMx_COMBINE field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 COMSWAP0	Combine Channel 0 and 1 Swap When set in combine mode, the even channel is used for the input capture and 1st compare, the odd channel is used for the 2nd compare. 0 Even channel is used for input capture and 1st compare. 1 Odd channel is used for input capture and 1st compare.
0 COMBINE0	Combine Channels 0 and 1 Enables the combine feature for channels 0 and 1. In input capture mode, the combined channels use the even channel input. In software compare modes, the even channel match asserts the output trigger and the odd channel match negates the output trigger. In PWM modes, the even channel match is used for the 1st compare and odd channel match for the 2nd compare. 0 Channels 0 and 1 are independent. 1 Channels 0 and 1 are combined.

48.4.8 Channel Polarity (TPMx_POL)

This register defines the input and output polarity of each of the channels.

Address: Base address + 70h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0														POL1	POL0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TPMx_POL field descriptions

Field	Description
31–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 POL1	Channel 1 Polarity 0 The channel polarity is active high. 1 The channel polarity is active low.
0 POL0	Channel 0 Polarity 0 The channel polarity is active high. 1 The channel polarity is active low.

48.4.9 Filter Control (TPMx_FILTER)

This register selects the filter value of the channel inputs, and an additional output delay value for the channel outputs. In PWM combine modes, the filter can effectively implements deadtime insertion.

Address: Base address + 78h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																								CH1FVAL				CH0FVAL			
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TPMx_FILTER field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

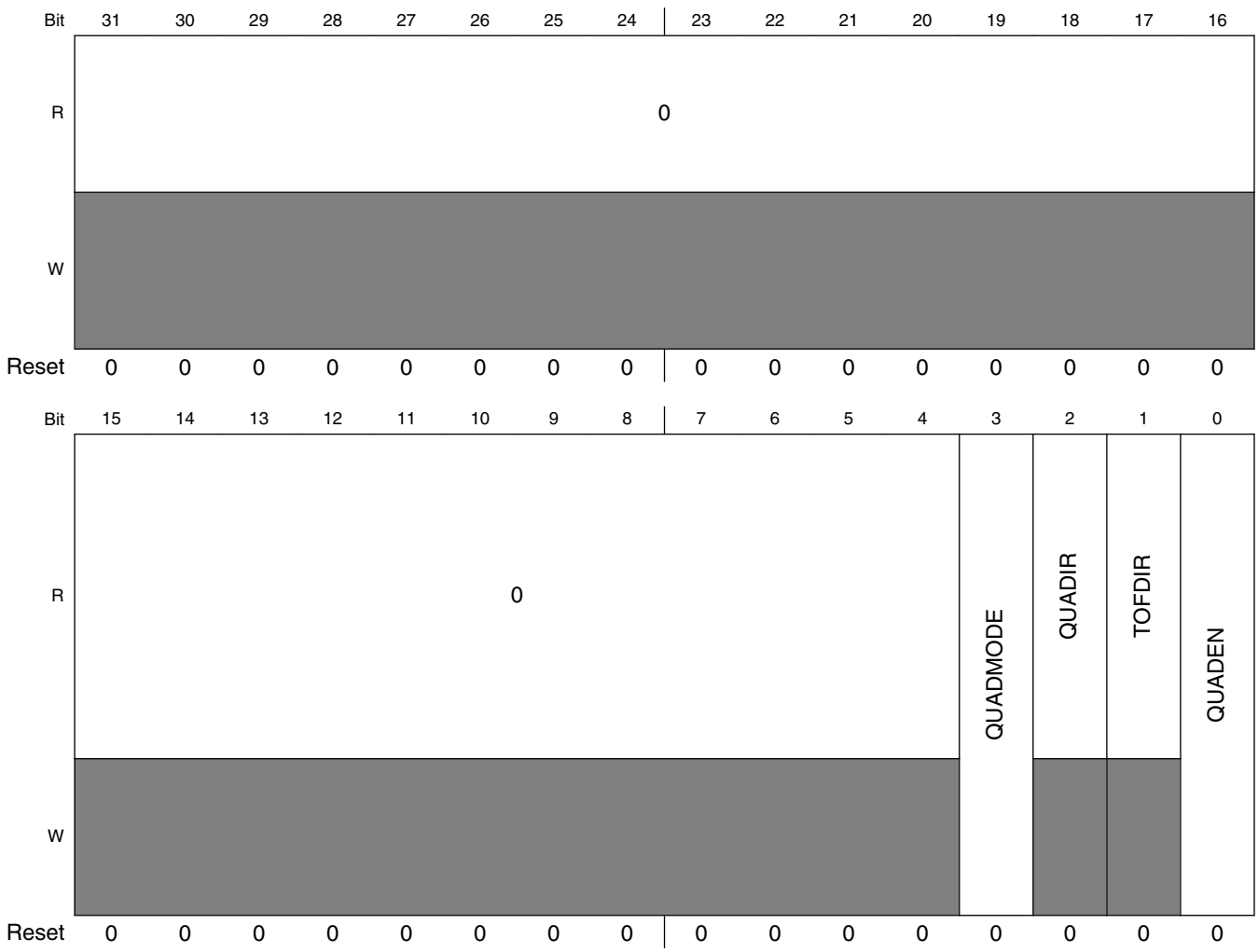
TPMx_FILTER field descriptions (continued)

Field	Description
7–4 CH1FVAL	Channel 1 Filter Value Selects the filter value for the channel input and the delay value for the channel output. The filter/delay is disabled when the value is zero, otherwise the filter/delay is configured as (CH1FVAL * 4) clock cycles.
CH0FVAL	Channel 0 Filter Value Selects the filter value for the channel input and the delay value for the channel output. The filter/delay is disabled when the value is zero, otherwise the filter/delay is configured as (CH0FVAL * 4) clock cycles.

48.4.10 Quadrature Decoder Control and Status (TPMx_QDCTRL)

This register has the control and status bits for the quadrature decoder mode.

Address: Base address + 80h offset



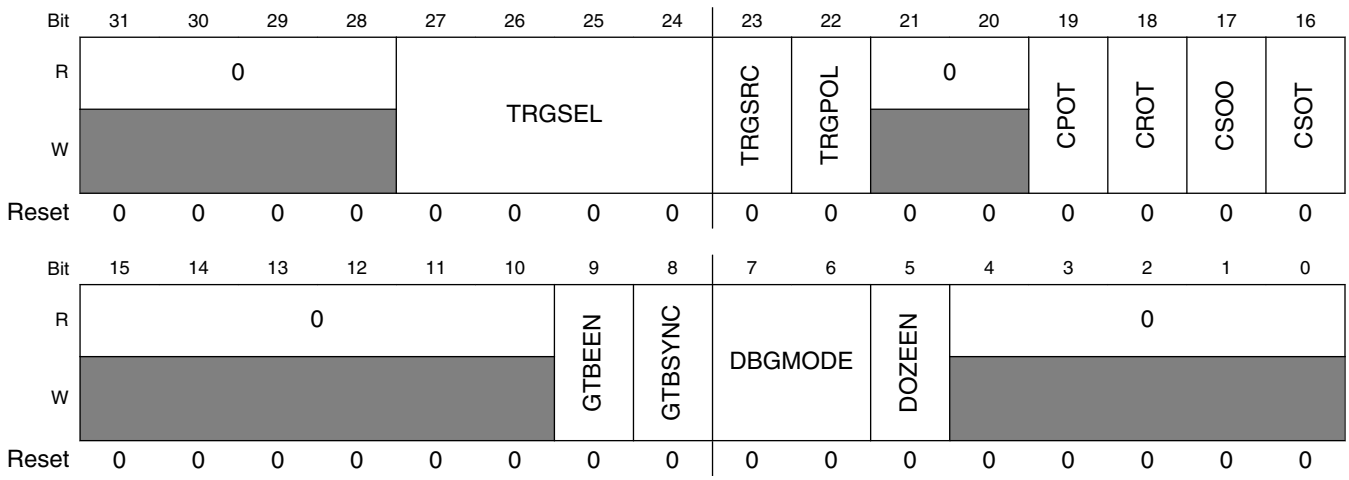
TPMx_QDCTRL field descriptions

Field	Description
31–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 QUADMODE	Quadrature Decoder Mode Selects the encoding mode used in the quadrature decoder mode. 0 Phase encoding mode. 1 Count and direction encoding mode.
2 QUADIR	Counter Direction in Quadrature Decode Mode Indicates the counting direction. 0 Counter direction is decreasing (counter decrement). 1 Counter direction is increasing (counter increment).
1 TOFDIR	Indicates if the TOF bit was set on the top or the bottom of counting. 0 TOF bit was set on the bottom of counting. There was an FTM counter decrement and FTM counter changes from its minimum value (zero) to its maximum value (MOD register). 1 TOF bit was set on the top of counting. There was an FTM counter increment and FTM counter changes from its maximum value (MOD register) to its minimum value (zero).
0 QUADEN	Enables the quadrature decoder mode. In this mode, the channel 0 and channel 1 inputs control the TPM counter direction and can only be used for software compare. The quadrature decoder mode has precedence over the other modes. 0 Quadrature decoder mode is disabled. 1 Quadrature decoder mode is enabled.

48.4.11 Configuration (TPMx_CONF)

This register selects the behavior in debug and wait modes and the use of an external global time base.

Address: Base address + 84h offset



TPMx_CONF field descriptions

Field	Description
31–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27–24 TRGSEL	Trigger Select Selects the input trigger to use for starting, reloading and/or pausing the counter. The source of the trigger (external or internal to the TPM) is configured by the TRGSRC field. This field should only be changed when the TPM counter is disabled. Refer to the chip configuration section for available external trigger options. The available internal trigger sources are listed below. 0001 Channel 0 pin input capture 0010 Channel 1 pin input capture 0011 Channel 0 or Channel 1 pin input capture
23 TRGSRC	Trigger Source Selects between internal (channel pin input capture) or external trigger sources. When selecting an internal trigger, the channel selected should be configured for input capture. Only a rising edge input capture can be used to initially start the counter using the CSOT configuration; either rising edge or falling edge input capture can be used to reload the counter using the CROT configuration; and the state of the channel input pin is used to pause the counter using the CPOT configuration. The channel polarity register can be used to invert the polarity of the channel input pins. This field should only be changed when the TPM counter is disabled.

Table continues on the next page...

TPMx_CONF field descriptions (continued)

Field	Description
	0 Trigger source selected by TRGSEL is external. 1 Trigger source selected by TRGSEL is internal (channel pin input capture).
22 TRGPOL	Trigger Polarity Selects the polarity of the external trigger source. This field should only be changed when the TPM counter is disabled. 0 Trigger is active high. 1 Trigger is active low.
21–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19 CPOT	Counter Pause On Trigger When enabled, the counter will pause incrementing while the trigger remains asserted (level sensitive). This field should only be changed when the TPM counter is disabled.
18 CROT	Counter Reload On Trigger When set, the TPM counter will reload with 0 (and initialize PWM outputs to their default value) when a rising edge is detected on the selected trigger input. The trigger input is ignored if the TPM counter is paused during debug mode or doze mode. This field should only be changed when the TPM counter is disabled. 0 Counter is not reloaded due to a rising edge on the selected input trigger 1 Counter is reloaded when a rising edge is detected on the selected input trigger
17 CSOO	Counter Stop On Overflow When set, the TPM counter will stop incrementing once the counter equals the MOD value and incremented (this also sets the TOF). Reloading the counter with 0 due to writing to the counter register or due to a trigger input does not cause the counter to stop incrementing. Once the counter has stopped incrementing, the counter will not start incrementing unless it is disabled and then enabled again, or a rising edge on the selected trigger input is detected when CSOT set. This field should only be changed when the TPM counter is disabled. 0 TPM counter continues incrementing or decrementing after overflow 1 TPM counter stops incrementing or decrementing after overflow.
16 CSOT	Counter Start on Trigger When set, the TPM counter will not start incrementing after it is enabled until a rising edge on the selected trigger input is detected. If the TPM counter is stopped due to an overflow, a rising edge on the selected trigger input will also cause the TPM counter to start incrementing again. The trigger input is ignored if the TPM counter is paused during debug mode or doze mode. This field should only be changed when the TPM counter is disabled. 0 TPM counter starts to increment immediately, once it is enabled. 1 TPM counter only starts to increment when it a rising edge on the selected input trigger is detected, after it has been enabled or after it has stopped due to overflow.
15–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9 GTBEEN	Global time base enable

Table continues on the next page...

TPMx_CONF field descriptions (continued)

Field	Description
	Configures the TPM to use an externally generated global time base counter. When an externally generated timebase is used, the internal TPM counter is not used by the channels but can be used to generate a periodic interruptor DMA request using the Modulo register and timer overflow flag. 0 All channels use the internally generated TPM counter as their timebase 1 All channels use an externally generated global timebase as their timebase
8 GTBSYNC	Global Time Base Synchronization When enabled, the TPM counter is synchronized to the global time base. It uses the global timebase enable, trigger and overflow to ensure the TPM counter starts incrementing at the same time as the global timebase, stops incrementing at the same time as the global timebase and is reset at the same time as the global timebase. This field should only be changed when the TPM counter is disabled. 0 Global timebase synchronization disabled. 1 Global timebase synchronization enabled.
7–6 DBGMODE	Debug Mode Configures the TPM behavior in debug mode. All other configurations are reserved. 00 TPM counter is paused and does not increment during debug mode. Trigger inputs and input capture events are also ignored. 11 TPM counter continues in debug mode.
5 DOZEEN	Doze Enable Configures the TPM behavior in wait mode. 0 Internal TPM counter continues in Doze mode. 1 Internal TPM counter is paused and does not increment during Doze mode. Trigger inputs and input capture events are also ignored.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

48.5 Functional description

The following sections describe the TPM features.

48.5.1 Clock domains

The TPM module supports two clock domains.

The bus clock domain is used by the register interface and for synchronizing interrupts and DMA requests.

The TPM counter clock domain is used to clock the counter and prescaler along with the output compare and input capture logic. The TPM counter clock is considered asynchronous to the bus clock, can be a higher or lower frequency than the bus clock and can remain operational in Stop mode. Multiple TPM instances are all clocked by the same TPM counter clock in support of the external timebase feature.

48.5.1.1 Counter Clock Mode

The CMOD[1:0] bits in the SC register either disable the TPM counter or select one of two possible clock modes for the TPM counter. After any reset, CMOD[1:0] = 0:0 so the TPM counter is disabled.

The CMOD[1:0] bits may be read or written at any time. Disabling the TPM counter by writing zero to the CMOD[1:0] bits does not affect the TPM counter value or other registers, but must be acknowledged by the TPM counter clock domain before they read as zero.

The external clock input passes through a synchronizer clocked by the TPM counter clock to assure that counter transitions are properly aligned to counter clock transitions. Therefore, to meet Nyquist criteria considering also jitter, the frequency of the external clock source must be less than half of the counter clock frequency.

48.5.2 Prescaler

The selected counter clock source passes through a prescaler that is a 7-bit counter.

The value of the prescaler is selected by the PS[2:0] bits. The following figure shows an example of the prescaler counter and TPM counter.

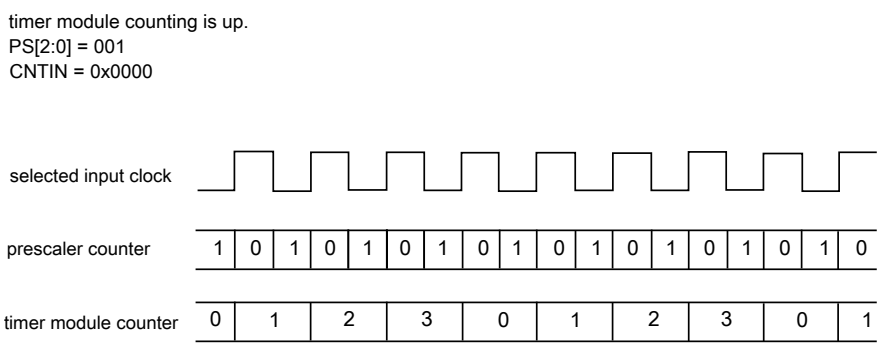


Figure 48-2. Example of the Prescaler Counter

48.5.3 Counter

The TPM has a 16-bit counter that is used by the channels either for input or output modes.

The counter updates from the selected clock divided by the prescaler.

The TPM counter has these modes of operation:

- up counting (see Up counting)
- up-down counting (see Up-down counting)

48.5.3.1 Up counting

Up counting is selected when SC[CPWMS] = 0.

The value of zero is loaded into the TPM counter, and the counter increments until the value of MOD is reached, at which point the counter is reloaded with zero.

The TPM period when using up counting is (MOD + 0x0001) × period of the TPM counter clock.

The TOF bit is set when the TPM counter changes from MOD to zero.

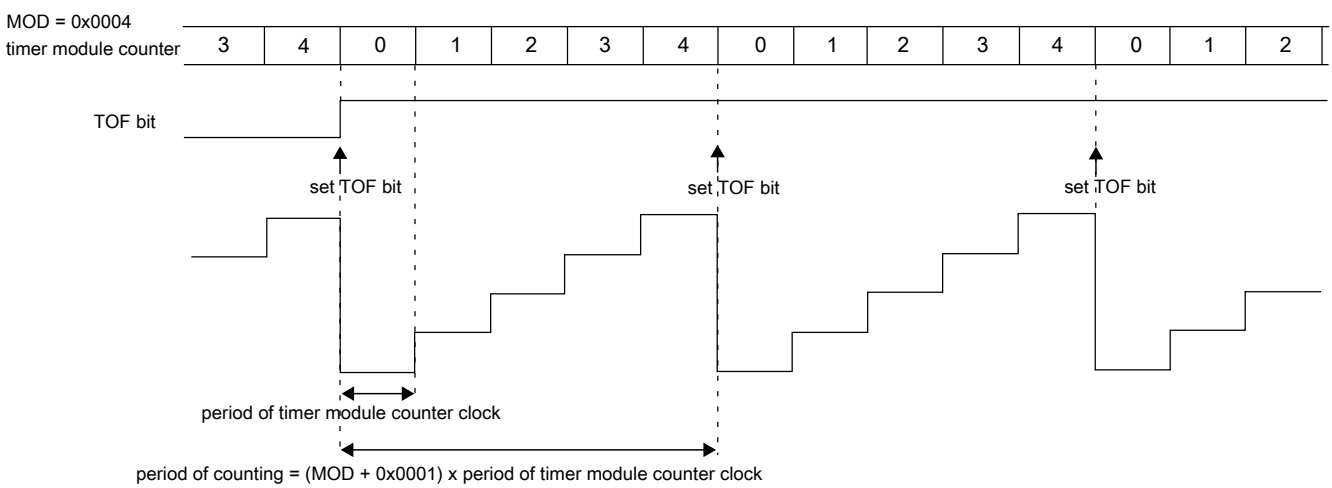


Figure 48-3. Example of TPM Up Counting

Note

- MOD = 0000 is a redundant condition. In this case, the TPM counter is always equal to MOD and the TOF bit is set in each rising edge of the TPM counter clock.

48.5.3.2 Up-down counting

Up-down counting is selected when SC[CPWMS] = 1. When configured for up-down counting, configuring CONF[MOD] to less than 2 is not supported.

The value of 0 is loaded into the TPM counter, and the counter increments until the value of MOD is reached, at which point the counter is decremented until it returns to zero and the up-down counting restarts.

The TPM period when using up-down counting is 2 × MOD × period of the TPM counter clock.

The TOF bit is set when the TPM counter changes from MOD to (MOD – 1).

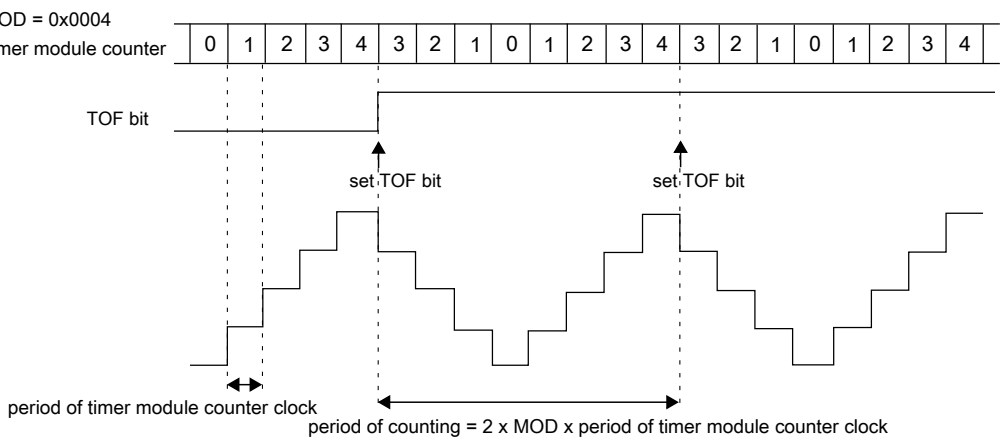


Figure 48-4. Example of up-down counting

48.5.3.3 Counter Reset

Any write to CNT resets the TPM counter and the channel outputs to their initial values (except for channels in output compare mode).

48.5.3.4 Global time base (GTB)

The global time base (GTB) is a TPM function that allows multiple TPM modules to share the same timebase. When the global time base is enabled (CONF[GTBEEN] = 1), the local TPM channels use the counter value, counter enable and overflow indication from the TPM generating the global time base. If the local TPM counter is not generating the global time base, then it can be used as an independent counter or pulse accumulator.

The local TPM counter can also be configured to synchronize to the global time base, by configuring (GTBSYNC = 1). When synchronized to the global time base, the local counter will use the counter enable and counter overflow indication from the TPM

generating the global time base. This enables multiple TPM to be configured with the same phase, but with different periods (although the global time base must be configured with the longest period).

48.5.3.5 Counter trigger

The TPM counter can be configured to start, stop or reset in response to a hardware trigger input. The trigger input is synchronized to the asynchronous counter clock, so there is a 3 counter clock delay between the trigger assertion and the counter responding.

- When (CSOT = 1), the counter will not start incrementing until a rising edge is detected on the trigger input.
- When (CSOO= 1), the counter will stop incrementing whenever the TOF flag is set. The counter does not increment again unless it is disabled, or if CSOT = 1 and a rising edge is detected on the trigger input.
- When (CROT= 1), the counter will reset to zero as if an overflow occurred whenever a rising edge is detected on the trigger input.
- When (CPOT = 1), the counter will pause incrementing whenever the trigger input is asserted. The counter will continue incrementing when the trigger input negates.

The polarity of the external input trigger can be configured by the TRGPOL register bit.

When an internal trigger source is selected, the trigger input is selected from one or more channel input capture events. The input capture filters are used with the internal trigger sources and the POLn bits can be used to invert the polarity of the input channels. Note that following restrictions apply with input capture channel sources.

- When (CSOT = 1), the counter will only start incrementing on a rising edge on the channel input, provided ELSnA = 1.
- When (CROT= 1), the counter will reset to zero on either edge of the channel input, as configured by ELSnB:ELSnA.
- When (CPOT = 1), the counter will pause incrementing whenever the channel input is asserted.

48.5.4 Input Capture Mode

The input capture mode is selected when (CPWMS = 0), (MSnB:MSnA = 0:0), and (ELSnB:ELSnA ≠ 0:0).

When a selected edge occurs on the channel input, the current value of the TPM counter is captured into the CnV register, at the same time the CHnF bit is set and the channel interrupt is generated if enabled by CHnIE = 1 (see the following figure).

When a channel is configured for input capture, the TPM_CHn pin is an edge-sensitive input. ELSnB:ELSnA control bits determine which edge, falling or rising, triggers input-capture event. Note that the maximum frequency for the channel input signal to be detected correctly is counter clock divided by 4, which is required to meet Nyquist criteria for signal sampling.

Writes to the CnV register are ignored in input capture mode.

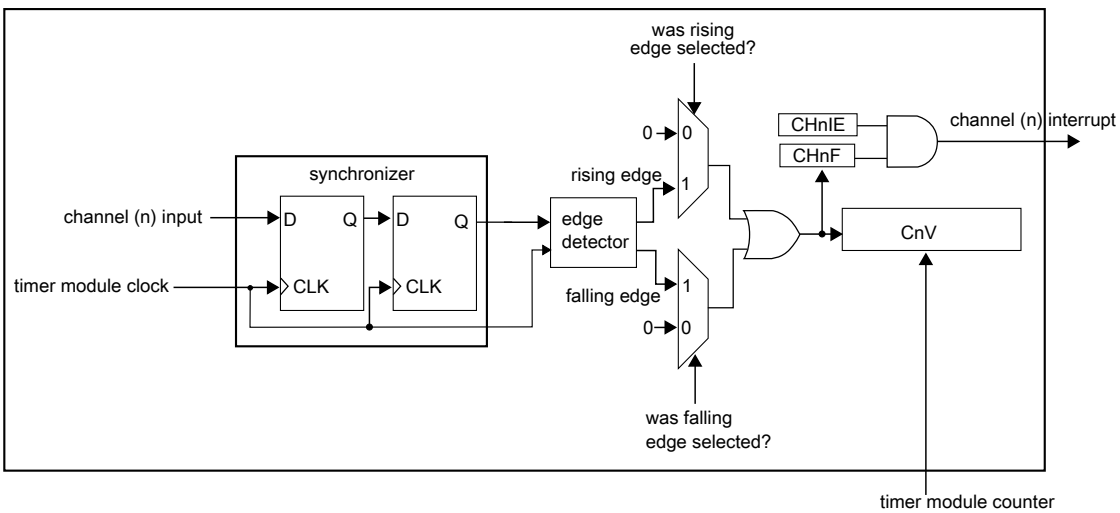


Figure 48-5. Input capture mode

The CHnF bit is set on the third rising edge of the counter clock after a valid edge occurs on the channel input.

48.5.5 Output Compare Mode

The output compare mode is selected when (CPWMS = 0), and (MSnB:MSnA = X:1).

In output compare mode, the TPM can generate timed pulses with programmable position, polarity, duration, and frequency. When the counter matches the value in the CnV register of an output compare channel, the channel (n) output can be set, cleared or toggled if MSnB is clear. If MSnB is set then the channel (n) output is pulsed high or low for as long as the counter matches the value in the CnV register.

When a channel is initially configured to output compare mode, the channel output updates with its negated value (logic 0 for set/toggle/pulse high and logic one for clear/pulse low).

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (TPM counter = CnV).

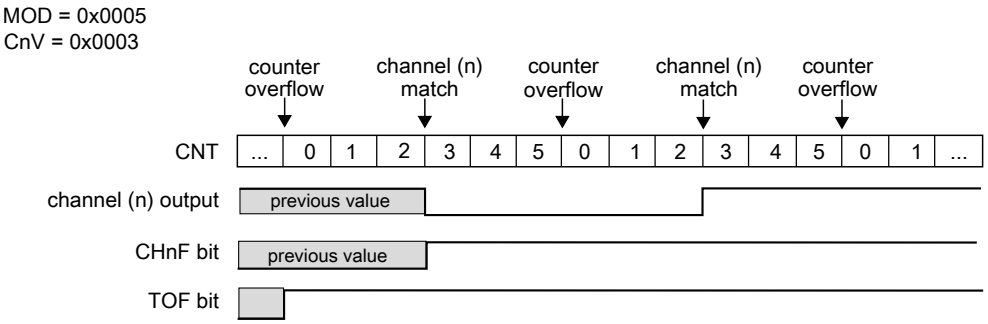


Figure 48-6. Example of the output compare mode when the match toggles the channel output

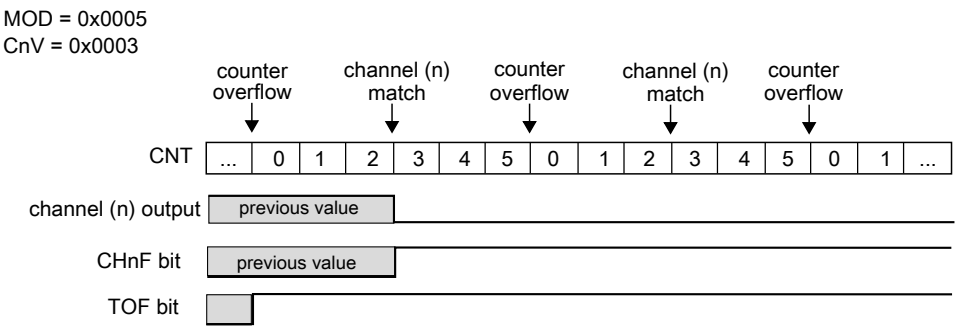


Figure 48-7. Example of the output compare mode when the match clears the channel output

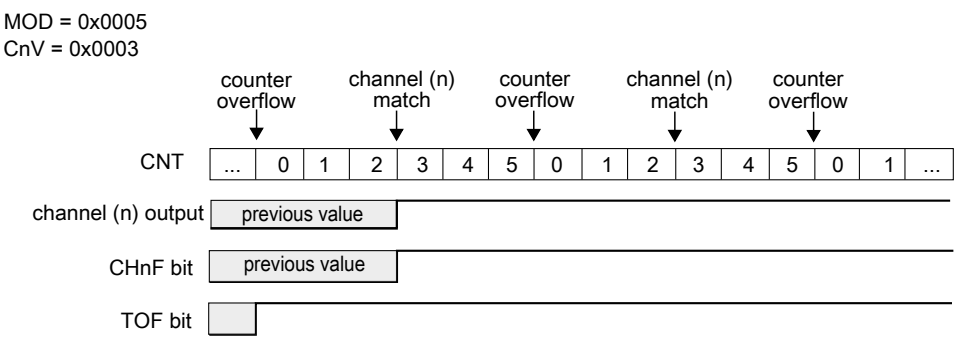


Figure 48-8. Example of the output compare mode when the match sets the channel output

It is possible to use the output compare mode with (ELSnB:ELSnA = 0:0). In this case, when the counter reaches the value in the CnV register, the CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1), however the channel (n) output is not modified and controlled by TPM.

48.5.6 Edge-Aligned PWM (EPWM) Mode

The edge-aligned mode is selected when (CPWMS = 0), and (MSnB:MSnA = 1:0).

The EPWM period is determined by (MOD + 0x0001) and the pulse width (duty cycle) is determined by CnV.

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (TPM counter = CnV), that is, at the end of the pulse width.

This type of PWM signal is called edge-aligned because the leading edges of all PWM signals are aligned with the beginning of the period, which is the same for all channels within an TPM.

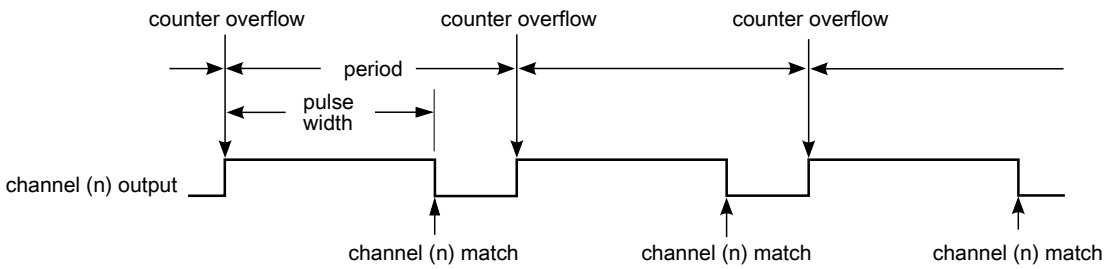


Figure 48-9. EPWM period and pulse width with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = 0:0) when the counter reaches the value in the CnV register, the CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1), however the channel (n) output is not controlled by TPM.

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced high at the counter overflow (when the zero is loaded into the TPM counter), and it is forced low at the channel (n) match (TPM counter = CnV) (see the following figure).

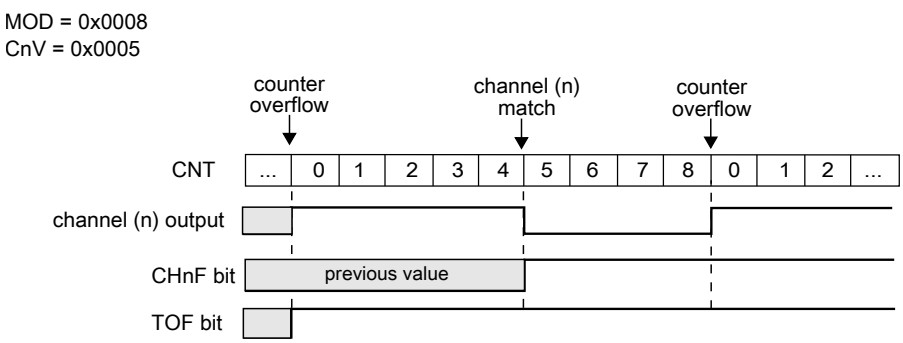


Figure 48-10. EPWM signal with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced low at the counter overflow (when zero is loaded into the TPM counter), and it is forced high at the channel (n) match (TPM counter = CnV) (see the following figure).

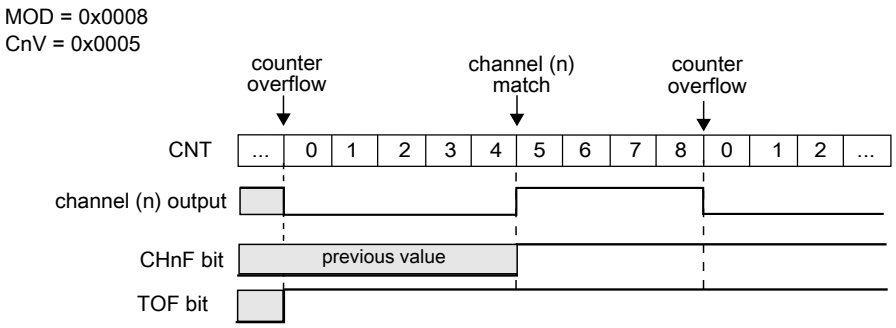


Figure 48-11. EPWM signal with ELSnB:ELSnA = X:1

If (CnV = 0x0000), then the channel (n) output is a 0% duty cycle EPWM signal. If (CnV > MOD), then the channel (n) output is a 100% duty cycle EPWM signal and CHnF bit is not set since there is never a channel (n) match. Therefore, MOD must be less than 0xFFFF in order to get a 100% duty cycle EPWM signal.

48.5.7 Center-Aligned PWM (CPWM) Mode

The center-aligned mode is selected when (CPWMS = 1) and (MSnB:MSnA = 1:0).

The CPWM pulse width (duty cycle) is determined by 2 × CnV and the period is determined by 2 × MOD (see the following figure). MOD must be kept in the range of 0x0001 to 0x7FFF because values outside this range can produce ambiguous results.

In the CPWM mode, the TPM counter counts up until it reaches MOD and then counts down until it reaches zero.

The CHnF bit is set and channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (TPM counter = CnV) when the TPM counting is down (at the begin of the pulse width) and when the TPM counting is up (at the end of the pulse width).

This type of PWM signal is called center-aligned because the pulse width centers for all channels are when the TPM counter is zero.

The other channel modes are not designed to be used with the up-down counter (CPWMS = 1). Therefore, all TPM channels should be used in CPWM mode when (CPWMS = 1).

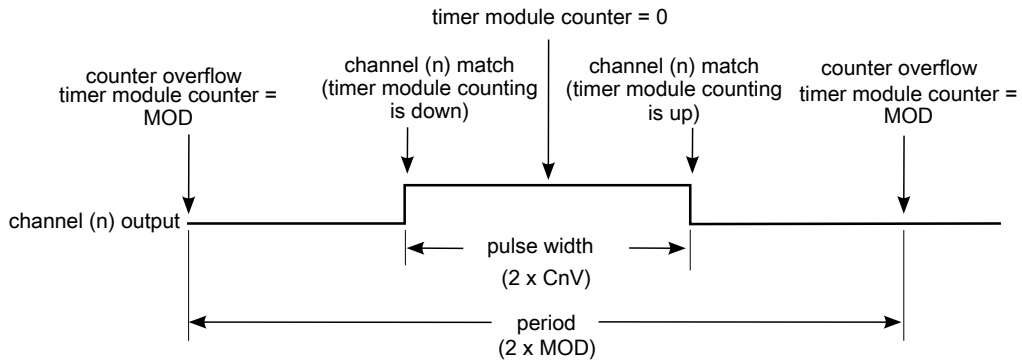


Figure 48-12. CPWM period and pulse width with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = 0:0) when the TPM counter reaches the value in the CnV register, the CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1), however the channel (n) output is not controlled by TPM.

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced high at the channel (n) match (TPM counter = CnV) when counting down, and it is forced low at the channel (n) match when counting up (see the following figure).

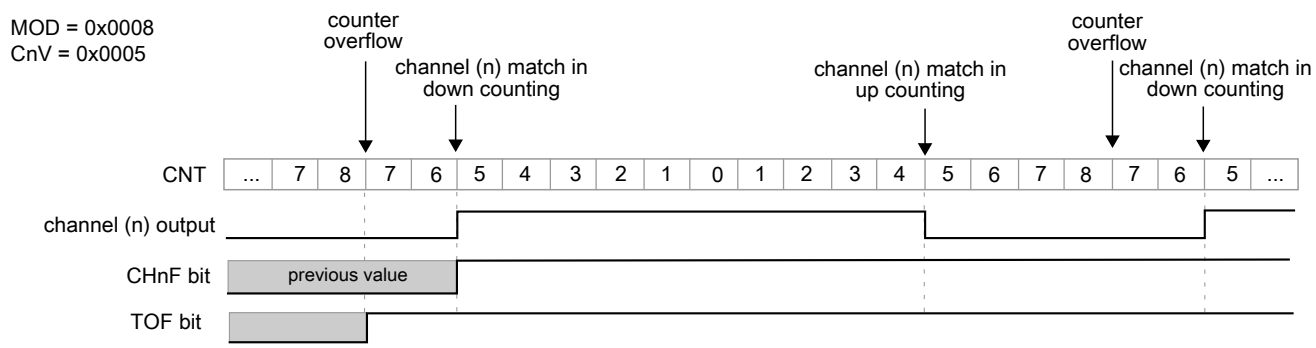


Figure 48-13. CPWM signal with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced low at the channel (n) match (TPM counter = CnV) when counting down, and it is forced high at the channel (n) match when counting up (see the following figure).

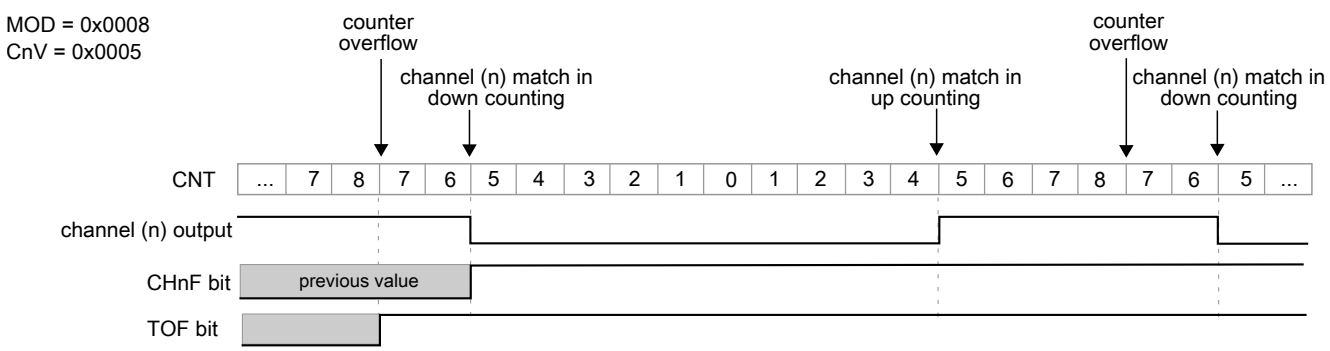


Figure 48-14. CPWM signal with ELSnB:ELSnA = X:1

If (CnV = 0x0000) then the channel (n) output is a 0% duty cycle CPWM signal.

If (CnV > MOD), then the channel (n) output is a 100% duty cycle CPWM signal, although the CHnF bit is set when the counter changes from incrementing to decrementing. Therefore, MOD must be less than 0xFFFF in order to get a 100% duty cycle CPWM signal.

48.5.8 Combine PWM mode

The Combine PWM mode is selected when:

- MSnB:MSnA = 10
- COMBINEn = 1
- QUADEN = 0, and
- CPWMS = 0

In Combine PWM mode, an even channel (n) and adjacent odd channel (n+1) are combined to generate a PWM signal in the channel (n) output.

In the Combine mode, the PWM period is determined by (MOD + 0x0001) and the PWM pulse width (duty cycle) is determined by (|C(n+1)V − C(n)V|).

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (TPM counter = C(n)V). The CH(n+1)F bit is set and the channel (n +1) interrupt is generated, if CH(n+1)IE = 1, at the channel (n+1) match (TPM counter = C(n+1)V).

If channel (n) (ELSnB:ELSnA = X:1), then the channel (n) output is forced low at the beginning of the period (TPM counter is zero) and at the channel (n+1) match (TPM counter = C(n+1)V). It is forced high at the channel (n) match (TPM counter = C(n)V).

If channel (n) (ELSnB:ELSnA = 1:0), then the channel (n) output is forced high at the beginning of the period (TPM counter is zero) and at the channel (n+1) match (TPM counter = C(n+1)V). It is forced low at the channel (n) match (TPM counter = C(n)V).

When (COMSWAPn = 1), then the channel (n) output is forced low or high at the beginning of the period (TPM counter is zero) and at the channel (n) match (TPM counter = C(n)V). It is forced high or low at the channel (n+1) match (TPM counter = C(n+1)V).

The channel (n+1) output is generated the same as the channel (n) output, but the output polarity is controlled by the channel (n+1) ELSnB:ELSnA configuration.

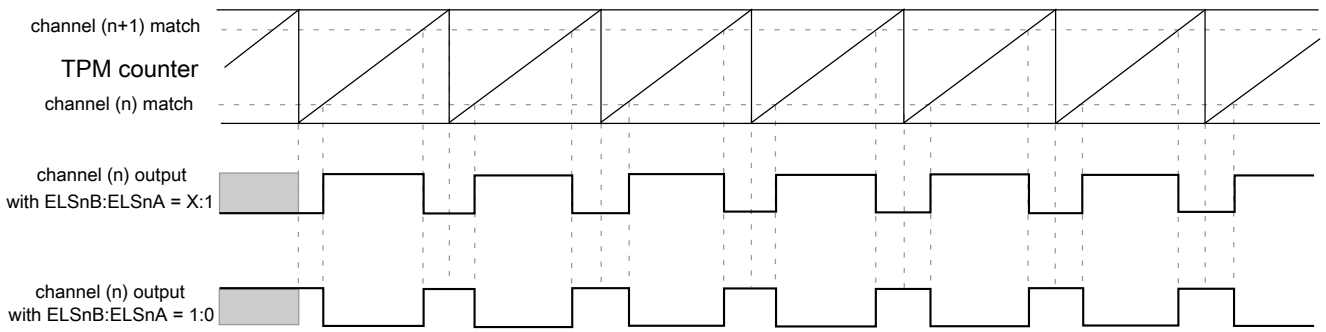


Figure 48-15. Combine mode

The following figures illustrate the PWM signals generation using Combine mode.

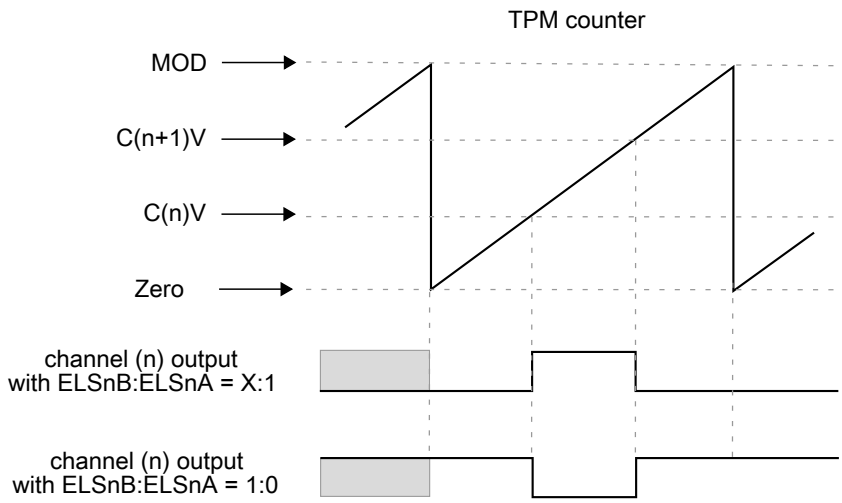


Figure 48-16. Channel (n) output if (C(n)V < MOD) and (C(n+1)V < MOD) and (C(n)V < C(n+1)V)

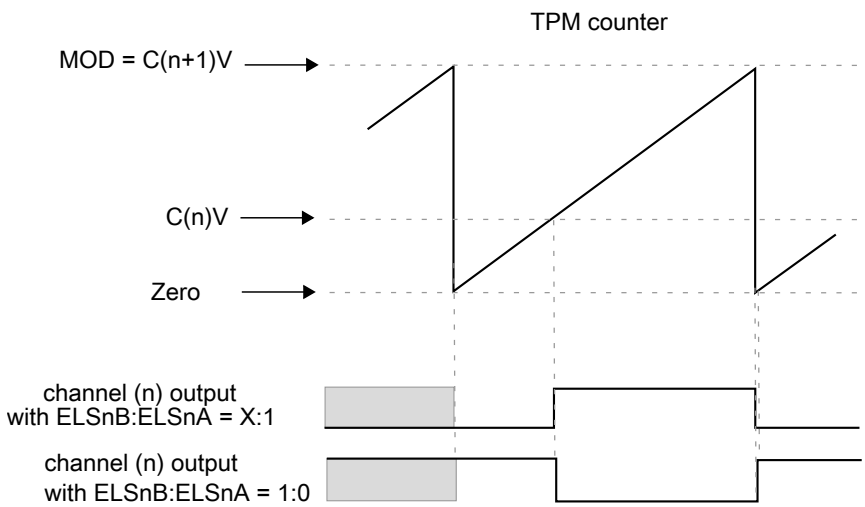


Figure 48-17. Channel (n) output if (C(n)V < MOD) and (C(n+1)V = MOD)

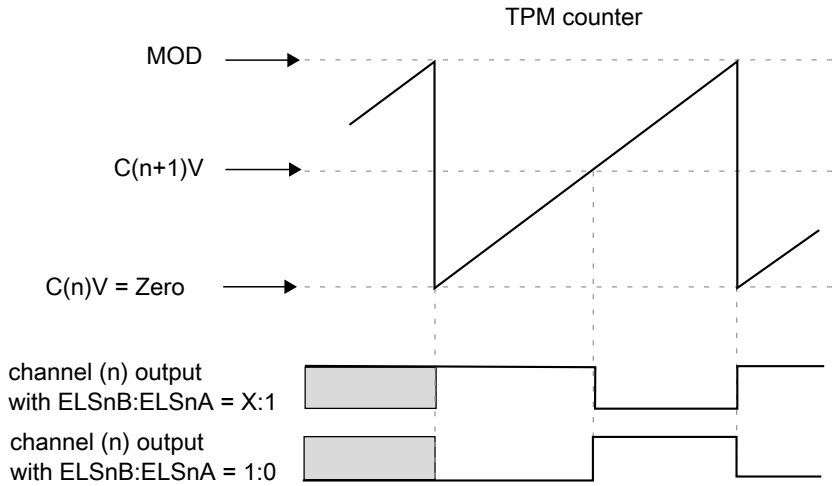


Figure 48-18. Channel (n) output if (C(n)V = zero) and (C(n+1)V < MOD)

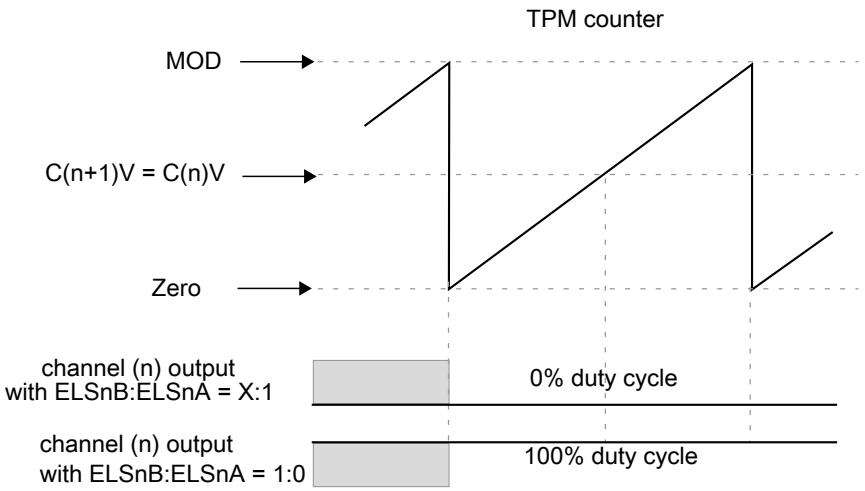


Figure 48-19. Channel (n) output if (C(n)V < MOD) and (C(n+1)V < MOD) and (C(n)V = C(n+1)V)

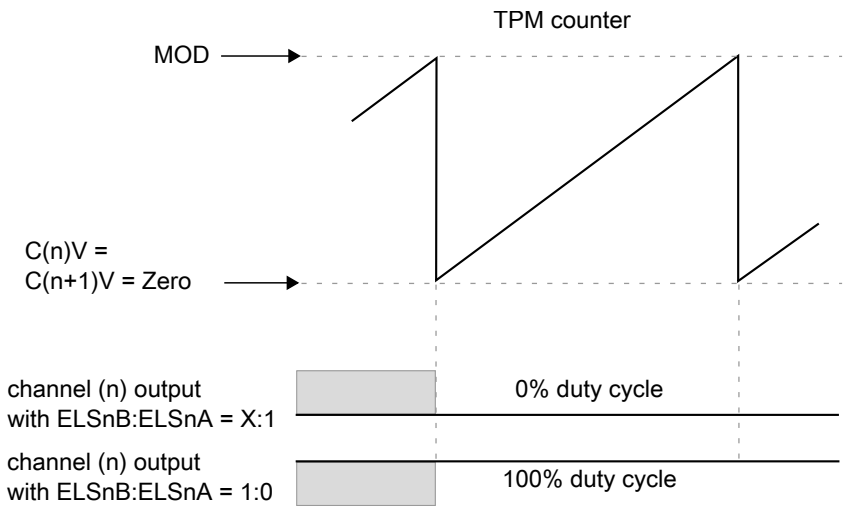


Figure 48-20. Channel (n) output if (C(n)V = C(n+1)V = zero)

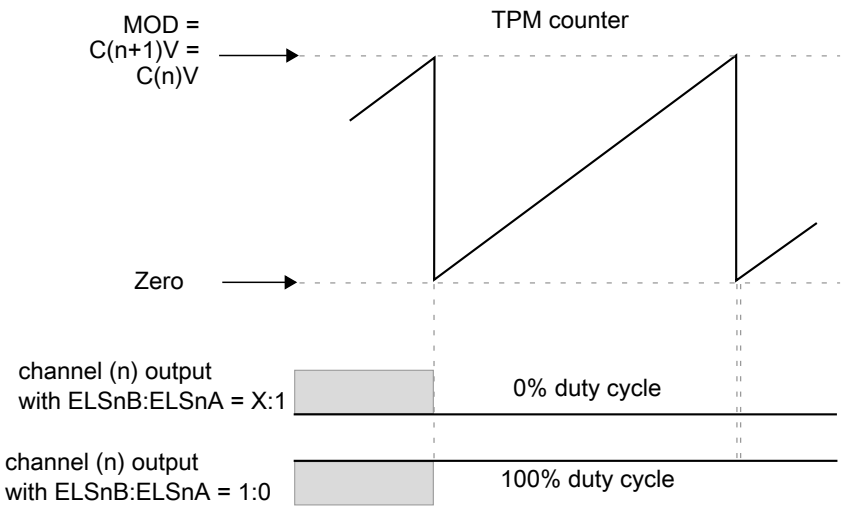


Figure 48-21. Channel (n) output if (C(n)V = C(n+1)V = MOD)

48.5.9 Combine Input Capture mode

The Combine Input Capture mode is selected if COMBINEn= 1 and MSnB:MSnA = 00 and ELSnB:ELSnA != 00. This mode allows to measure a pulse width of the signal on the input of channel (n) of a channel pair. The channel (n) filter can be active in this mode.

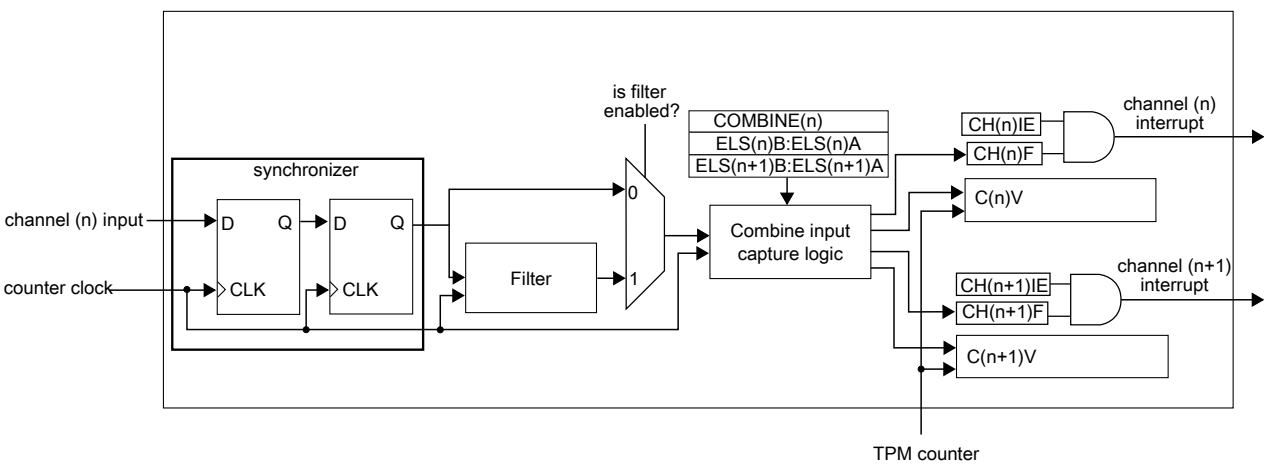


Figure 48-22. Combine Input Capture mode block diagram

The ELS(n)B:ELS(n)A bits select the edge that is captured by channel (n), and ELS(n +1)B:ELS(n+1)A bits select the edge that is captured by channel (n+1).

In the Combine Input Capture mode, only channel (n) input is used and channel (n+1) input is ignored, when COMSWAPn=1 then only channel (n+1) input is used and channel (n) input is ignored.

If the selected edge by channel (n) bits is detected at channel (n) input, then CH(n)F bit is set and the channel (n) interrupt is generated (if CH(n)IE = 1). If the selected edge by channel (n+1) bits is detected at channel (n) input, then CH(n+1)F bit is set and the channel (n+1) interrupt is generated (if CH(n+1)IE = 1).

The C(n)V register stores the value of TPM counter when the selected edge by channel (n) is detected at channel (n) input. The C(n+1)V register stores the value of TPM counter when the selected edge by channel (n+1) is detected at channel (n) input.

Note

- The CH(n)F, CH(n)IE, MS(n)A, ELS(n)B, and ELS(n)A bits are channel (n) bits.
- The CH(n+1)F, CH(n+1)IE, MS(n+1)A, ELS(n+1)B, and ELS(n+1)A bits are channel (n+1) bits.
- The Combine Input Capture mode must be used with ELS(n)B:ELS(n)A = 0:1 or 1:0, ELS(n+1)B:ELS(n+1)A = 0:1 or 1:0.

48.5.10 Input Capture Filter

The input capture filter function is only in input capture mode, or in software compare mode when quadrature decoder mode is enabled.

First, the input signal is synchronized by the counter clock. Following synchronization, the input signal enters the filter block. See the following figure.

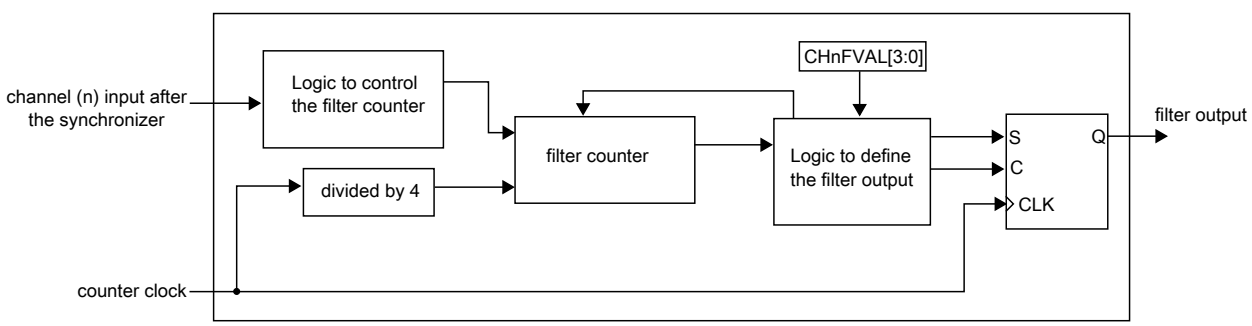


Figure 48-23. Channel input filter

When there is a state change in the input signal, the counter is reset and starts counting up. As long as the new state is stable on the input, the counter continues to increment. When the counter is equal to (CHnFVAL[3:0] × 4), the state change of the input signal is validated.

If the opposite edge appears on the input signal before it can be validated, the counter is reset. At the next input transition, the counter starts counting again. Any pulse that is shorter than the minimum value selected by (CHnFVAL[3:0] × 4 counter clocks) is regarded as a glitch and is not passed through the filter. A timing diagram of the input filter is shown in the following figure.

The filter function is disabled when CHnFVAL[3:0] bits are zero. In this case, the input signal is delayed by 2 rising edges of the counter clock. If (CHnFVAL[3:0] ≠ 0000), then the input signal is delayed by the minimum pulse width (CHnFVAL[3:0] × 4 system clocks) plus a further 3 rising edges of the system clock: two rising edges to the synchronizer, plus one more to the edge detector. In other words, CHnF is set (3 + 4 × CHnFVAL[3:0]) counter clock periods after a valid edge occurs on the channel input.

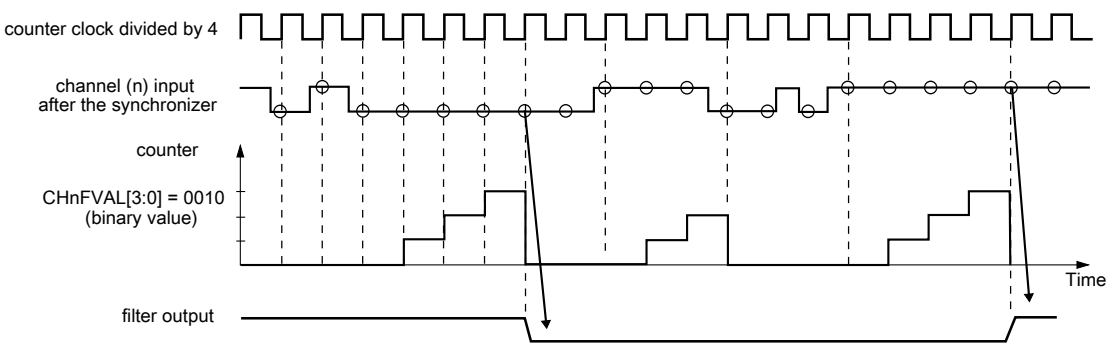


Figure 48-24. Channel input filter example

48.5.11 Deadtime insertion

The deadtime insertion is enabled in PWM combine modes when CHnFVAL is non-zero. The deadtime delay that is used for each TPM channel is defined as (CHnFVAL[3:0] x 4).

The deadtime delay insertion ensures that no two complementary signals (channels (n) and (n+1)) drive the active state at the same time.

If POL(n) = 0, POL(n+1) = 1, and the deadtime is enabled, then when the channel (n) match (TPM counter = C(n)V) occurs, the channel (n) output remains at the low value until the end of the deadtime delay when the channel (n) output is set. Similarly, when the channel (n+1) match (TPM counter = C(n+1)V) occurs, the channel (n+1) output remains at the low value until the end of the deadtime delay when the channel (n+1) output is set. See the following figures.

If POL(n) = 1, POL(n+1) = 0, and the deadtime is enabled, then when the channel (n) match (TPM counter = C(n)V) occurs, the channel (n) output remains at the high value until the end of the deadtime delay when the channel (n) output is cleared. Similarly,

when the channel (n+1) match (TPM counter = C(n+1)V) occurs, the channel (n+1) output remains at the high value until the end of the deadtime delay when the channel (n +1) output is cleared.

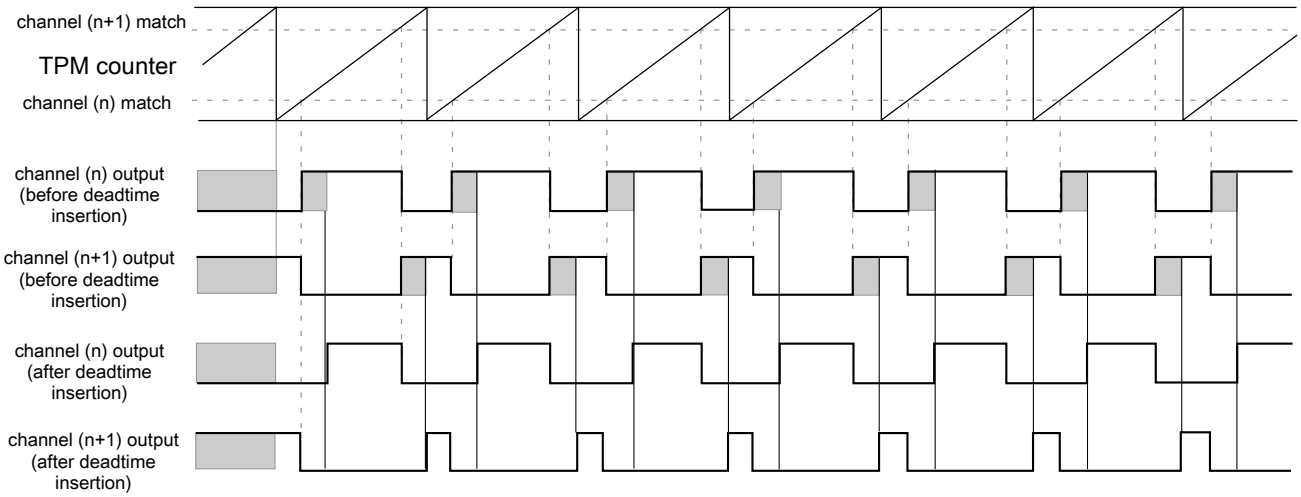


Figure 48-25. Deadtime insertion with ELSnB:ELSnA = X:1, POL(n) = 0, and POL(n+1) = 1

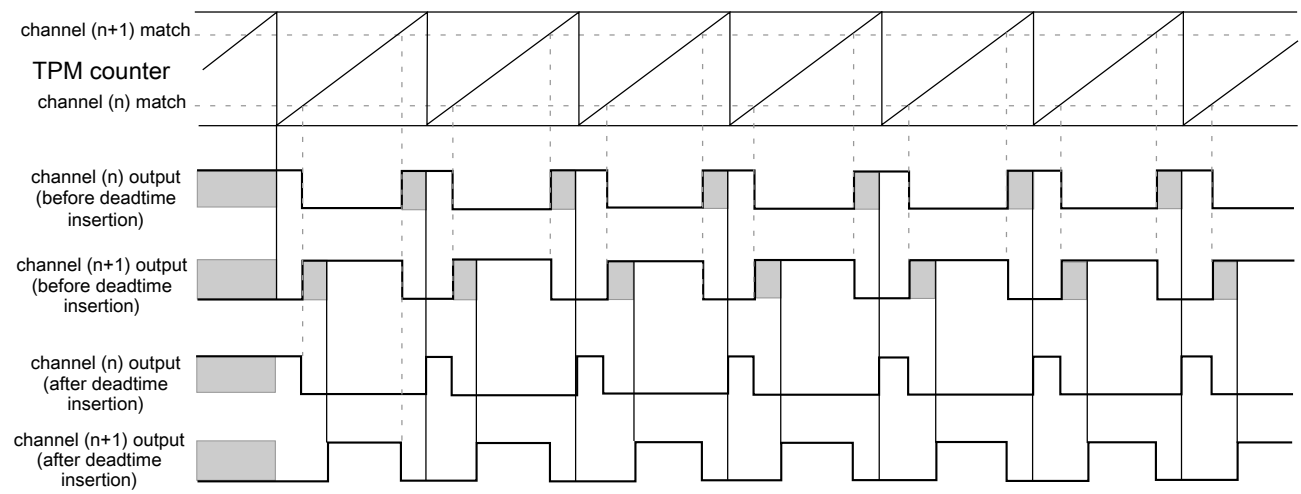


Figure 48-26. Deadtime insertion with ELSnB:ELSnA = 1:0, POL(n) = 0, and POL(n+1) = 1

48.5.12 Quadrature Decoder mode

The Quadrature Decoder mode is selected if (QUADEN = 1). The Quadrature Decoder mode uses the channel 0 (phase A) and channel 1 (phase B) input signals to control the TPM counter increment and decrement. The following figure shows the quadrature decoder block diagram.

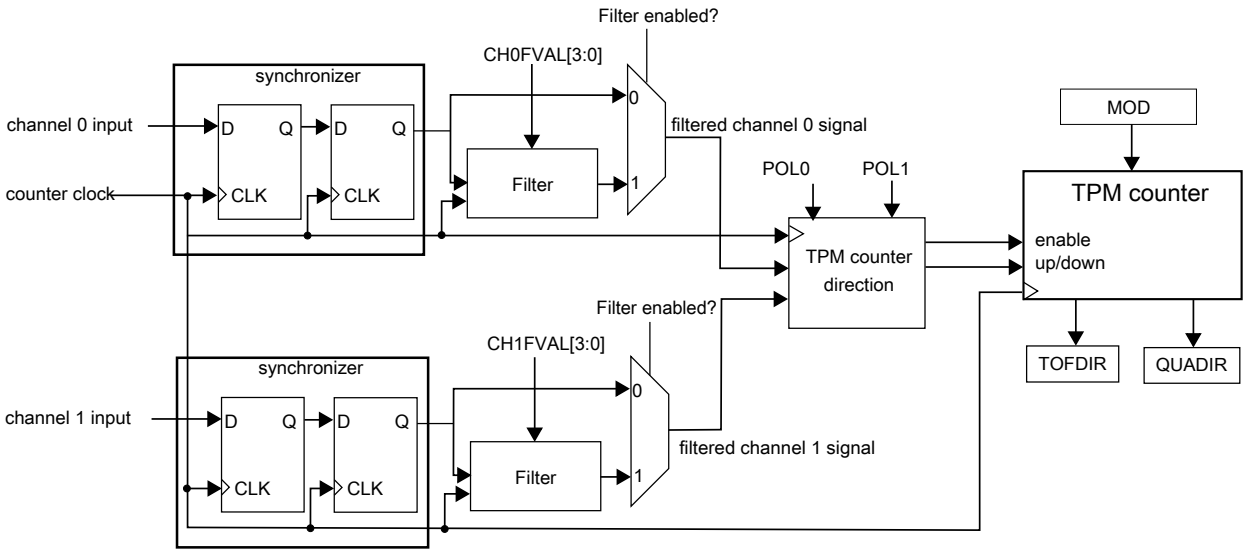


Figure 48-27. Quadrature Decoder block diagram

The input capture filter and channel polarity registers are used to configure the input filter and polarity for the channel 0 and channel 1 inputs in quadrature decode mode.

Note

Notice that the TPM counter is clocked by the channel 0 and channel 1 input signals when quadrature decoder mode is selected. Therefore In quadrature decoder mode, channel 0 and channel 1 can only be used in software compare mode and other TPM channels can only be used in input capture or output compare modes.

The QUADMODE selects the encoding mode used in the Quadrature Decoder mode. If QUADMODE = 1, then the count and direction encoding mode is enabled; see the following figure. In this mode, the channel 1 input value indicates the counting direction, and the channel 0 input defines the counting rate. The TPM counter is updated when there is a rising edge at channel 0 input signal.

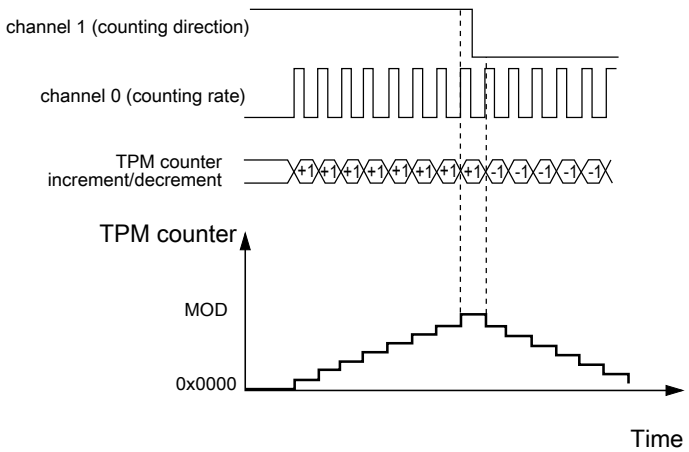


Figure 48-28. Quadrature Decoder – Count and Direction Encoding mode

If QUADMODE = 0, then the Phase Encoding mode is enabled; see the following figure. In this mode, the relationship between channel 0 and channel 1 signals indicates the counting direction, and channel 0 and channel 1 signals define the counting rate. The TPM counter is updated when there is an edge either at the channel 0 or channel 1 signals.

If CH0POL= 0 and CH1POL = 0, then the TPM counter increment happens when:

- there is a rising edge at channel 0 signal and channel 1 signal is at logic zero;
- there is a rising edge at channel 1 signal and channel 0 signal is at logic one;
- there is a falling edge at channel 1 signal and channel 0 signal is at logic zero;
- there is a falling edge at channel 0 signal and channel 1 signal is at logic one;

and the TPM counter decrement happens when:

- there is a falling edge at channel 0 signal and channel 1 signal is at logic zero;
- there is a falling edge at channel 1 signal and channel 0 signal is at logic one;
- there is a rising edge at channel 1 signal and channel 0 signal is at logic zero;
- there is a rising edge at channel 0 signal and channel 1 signal is at logic one.

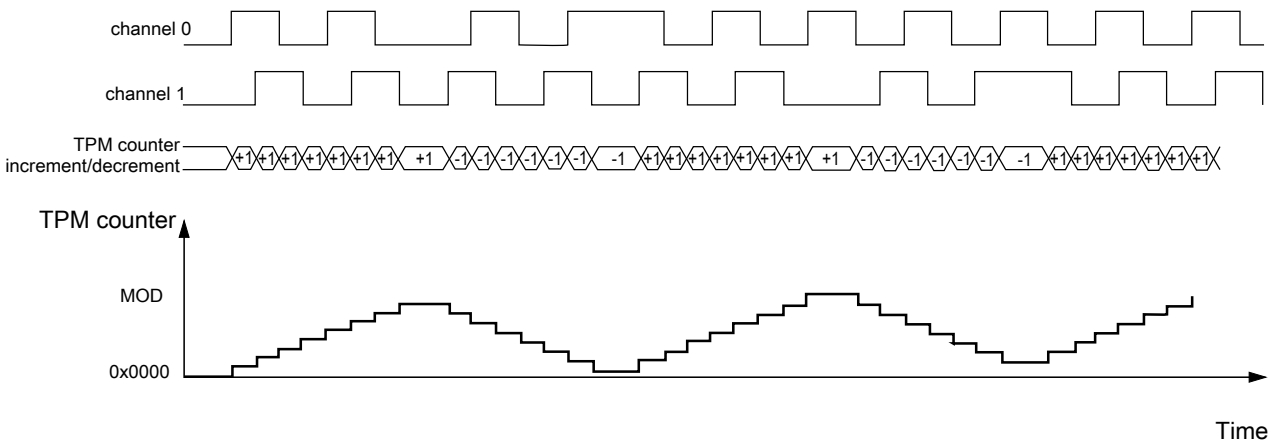


Figure 48-29. Quadrature Decoder – Phase Encoding mode

The following figure shows the TPM counter overflow in up counting. In this case, when the TPM counter changes from MOD to zero, TOF and TOFDIR bits are set. TOF bit indicates the TPM counter overflow occurred. TOFDIR indicates the counting was up when the TPM counter overflow occurred.

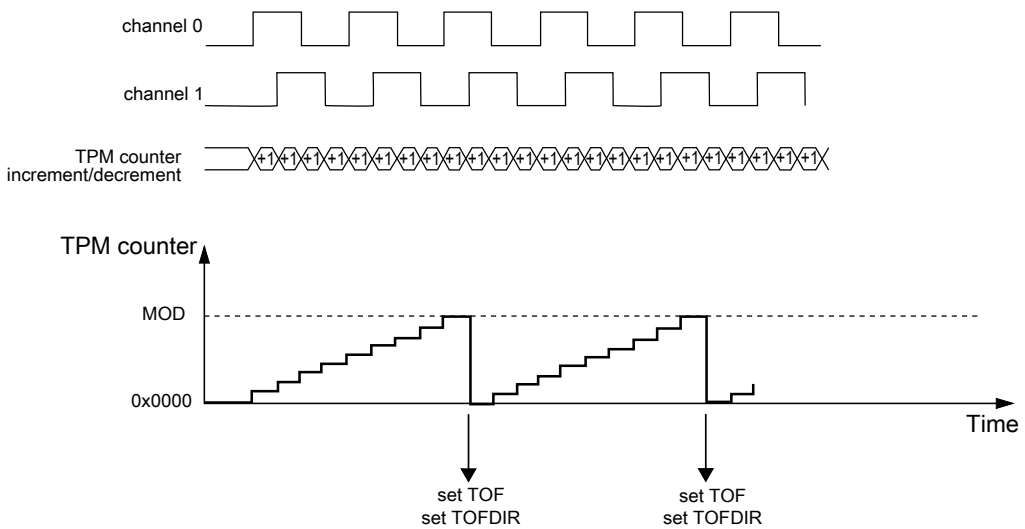


Figure 48-30. TPM Counter overflow in up counting for Quadrature Decoder mode

The following figure shows the TPM counter overflow in down counting. In this case, when the TPM counter changes from zero to MOD, TOF bit is set and TOFDIR bit is cleared. TOF bit indicates the TPM counter overflow occurred. TOFDIR indicates the counting was down when the TPM counter overflow occurred.

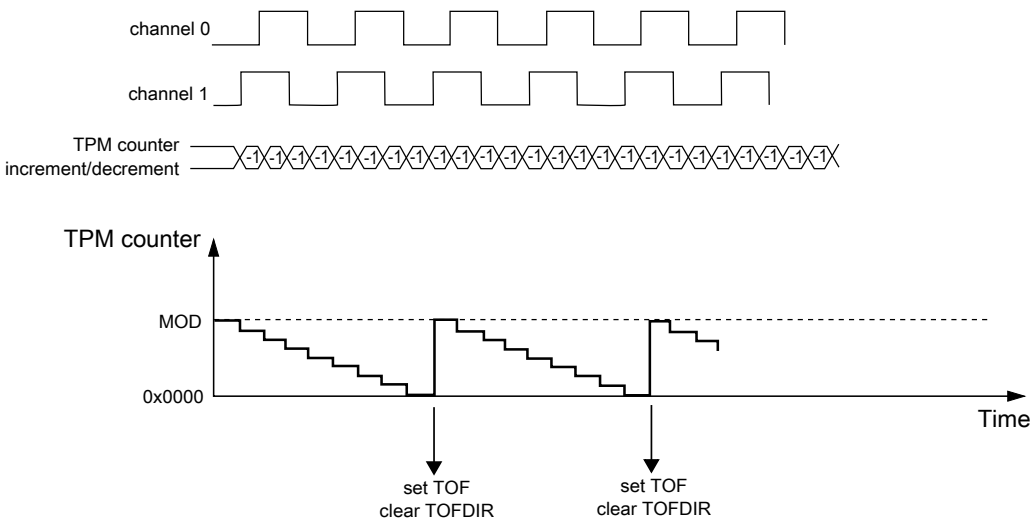


Figure 48-31. TPM counter overflow in down counting for Quadrature Decoder mode

48.5.13 Registers Updated from Write Buffers

48.5.13.1 MOD Register Update

If (CMOD[1:0] = 0:0) then MOD register is updated when MOD register is written.

If (CMOD[1:0] ≠ 0:0), then MOD register is updated according to the CPWMS bit, that is:

- If the selected mode is not CPWM then MOD register is updated after MOD register was written and the TPM counter changes from MOD to zero.
- If the selected mode is CPWM then MOD register is updated after MOD register was written and the TPM counter changes from MOD to (MOD – 1).

48.5.13.2 CnV Register Update

If (CMOD[1:0] = 0:0) then CnV register is updated when CnV register is written.

If (CMOD[1:0] ≠ 0:0), then CnV register is updated according to the selected mode, that is:

- If the selected mode is output compare then CnV register is updated on the next TPM counter increment (end of the prescaler counting) after CnV register was written.

- If the selected mode is EPWM then CnV register is updated after CnV register was written and the TPM counter changes from MOD to zero.
- If the selected mode is CPWM then CnV register is updated after CnV register was written and the TPM counter changes from MOD to (MOD – 1).

48.5.14 DMA

The channel and overflow flags generate a DMA transfer request according to DMA and CHnIE/TOIE bits.

See the following table for more information.

Table 48-5. DMA Transfer Request

DMA	CHnIE/ TOIE	Channel/Overflow DMA Transfer Request	Channel/Overflow Interrupt
0	0	The channel/overflow DMA transfer request is not generated.	The channel/overflow interrupt is not generated.
0	1	The channel/overflow DMA transfer request is not generated.	The channel/overflow interrupt is generated if (CHnF/TOF = 1).
1	0	The channel/overflow DMA transfer request is generated if (CHnF/TOF = 1).	The channel/overflow interrupt is not generated.
1	1	The channel/overflow DMA transfer request is generated if (CHnF/TOF = 1).	The channel/overflow interrupt is generated if (CHnF/TOF = 1).

If DMA = 1, the CHnF/TOF bit can be cleared either by DMA transfer done or writing a one to CHnF/TOF bit (see the following table).

Table 48-6. Clear CHnF/TOF Bit

DMA	How CHnF/TOF Bit Can Be Cleared
0	CHnF/TOF bit is cleared by writing a 1 to CHnF/TOF bit.
1	CHnF/TOF bit is cleared either when the DMA transfer is done or by writing a 1 to CHnF/TOF bit.

48.5.15 Output triggers

The TPM generates output triggers for the counter and each channel that can be used to trigger events in other peripherals.

The counter trigger asserts whenever the TOF is set and remains asserted until the next increment.

Each TPM channel generates both a pre-trigger output and a trigger output. The pre-trigger output asserts whenever the CHnF is set, the trigger output asserts on the first counter increment after the pre-trigger asserts, and then both the trigger and pre-trigger negate on the first counter increment after the trigger asserts.

When (COMBINEn = 1) in output compare modes, the pre-trigger output for both channel (n) and channel (n+1) will assert when CH(n)F is set and will negate when CH(n+1)F is set. The trigger continues to assert on the first counter increment after the pre-trigger asserts and negates at the same time as the pre-trigger negation.

48.5.16 Reset Overview

The TPM is reset whenever any chip reset occurs.

When the TPM exits from reset:

- the TPM counter and the prescaler counter are zero and are stopped (CMOD[1:0] = 0:0);
- the timer overflow interrupt is zero;
- the channels interrupts are zero;
- the channels are in input capture mode;
- the channels outputs are zero;
- the channels pins are not controlled by TPM (ELS(n)B:ELS(n)A = 0:0).

48.5.17 TPM Interrupts

This section describes TPM interrupts.

48.5.17.1 Timer Overflow Interrupt

The timer overflow interrupt is generated when (TOIE = 1) and (TOF = 1).

48.5.17.2 Channel (n) Interrupt

The channel (n) interrupt is generated when (CHnIE = 1) and (CHnF = 1).

Chapter 49
Low-Power Timer (LPTMR)

49.1 Chip-specific LPTMR information

49.1.1 Low power timer instantiations

This device contains 2 LPTMR modules with one 16-bit channel for each module.

LPT/HSCMP0 pulse counting:

LPTMR0_ALT0 input is the selectable source to count pulses resulting from HSCMP0 Output (LPT_ALT0 = HSCMP0 Output).

LPTMR1_ALT0 input can be configured to count the trigger out pulse from LPTMR0, so that LPTMR1 and LPTMR0 can be cascaded as one 32-bit timer.

49.1.2 LPTMRx prescaler/glitch filter clocking options

The prescaler and glitch filter of the LPTMR module can be clocked from one of four sources determined by the LPTMRx_PSR[PCS] bitfield. The following table shows the chip-specific clock assignments for this bitfield.

NOTE

The chosen clock must remain enabled if the LPTMR is to continue operating in all required low-power modes.

LPTMRx_PSR[PCS]	Prescaler/glitch filter clock number	Chip clock
00	0	MCGIRCLK — internal reference clock (not available in VLPS/LLS/VLLS modes)

Table continues on the next page...

LPTMRx_PSR[PCS]	Prescaler/glitch filter clock number	Chip clock
01	1	LPO — 1 kHz clock (not available in VLLS0 mode)
10	2	ERCLK32K — secondary external reference clock
11	3	OSCERCLK — external reference clock (not available in VLLS0 mode)

See Clock Distribution for more details on these clocks.

49.1.3 LPTMRx pulse counter input options

The LPTMRx_CSR[TPS] bitfield configures the input source used in pulse counter mode. The following table shows the chip-specific input assignments for this bitfield.

LPTMRx_CSR[TPS]	Pulse counter input number	Chip input
00	0	CMP0 output
01	1	LPTMRx_ALT1 pin
10	2	LPTMRx_ALT2 pin
11	3	LPTMRx_ALT3 pin

49.2 Introduction

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

49.2.1 Features

The features of the LPTMR module include:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

- Rising-edge or falling-edge

49.2.2 Modes of operation

The following table describes the operation of the LPTMR module in various modes.

Table 49-1. Modes of operation

Modes	Description
Run	The LPTMR operates normally.
Wait	The LPTMR continues to operate normally and may be configured to exit the low-power mode by generating an interrupt request.
Stop	The LPTMR continues to operate normally and may be configured to exit the low-power mode by generating an interrupt request.
Low-Leakage	The LPTMR continues to operate normally and may be configured to exit the low-power mode by generating an interrupt request.
Debug	The LPTMR operates normally in Pulse Counter mode, but counter does not increment in Time Counter mode.

49.3 LPTMR signal descriptions

Table 49-2. LPTMR signal descriptions

Signal	I/O	Description
LPTMR0_ALT*n*	I	Pulse Counter Input pin

49.3.1 Detailed signal descriptions

Table 49-3. LPTMR interface—detailed signal descriptions

Signal	I/O	Description	
LPTMR_ALT*n*	I	Pulse Counter Input The LPTMR can select one of the input pins to be used in Pulse Counter mode.	
		State meaning	Assertion—If configured for pulse counter mode with active-high input, then assertion causes the CNR to increment. Deassertion—If configured for pulse counter mode with active-low input, then deassertion causes the CNR to increment.

Table continues on the next page...

Table 49-3. LPTMR interface—detailed signal descriptions (continued)

Signal	I/O	Description	
		Timing	Assertion or deassertion may occur at any time; input may assert asynchronously to the bus clock.

49.4 Memory map and register definition

NOTE

The LPTMR registers are reset only on a POR or LVD event. See LPTMR power and reset for more details.

LPTMR memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4004_0000	Low Power Timer Control Status Register (LPTMR0_CSR)	32	R/W	0000_0000h	49.4.1/1632
4004_0004	Low Power Timer Prescale Register (LPTMR0_PSR)	32	R/W	0000_0000h	49.4.2/1634
4004_0008	Low Power Timer Compare Register (LPTMR0_CMR)	32	R/W	0000_0000h	49.4.3/1635
4004_000C	Low Power Timer Counter Register (LPTMR0_CNR)	32	R/W	0000_0000h	49.4.4/1636
4004_4000	Low Power Timer Control Status Register (LPTMR1_CSR)	32	R/W	0000_0000h	49.4.1/1632
4004_4004	Low Power Timer Prescale Register (LPTMR1_PSR)	32	R/W	0000_0000h	49.4.2/1634
4004_4008	Low Power Timer Compare Register (LPTMR1_CMR)	32	R/W	0000_0000h	49.4.3/1635
4004_400C	Low Power Timer Counter Register (LPTMR1_CNR)	32	R/W	0000_0000h	49.4.4/1636

49.4.1 Low Power Timer Control Status Register (LPTMRx_CSR)

Address: Base address + 0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

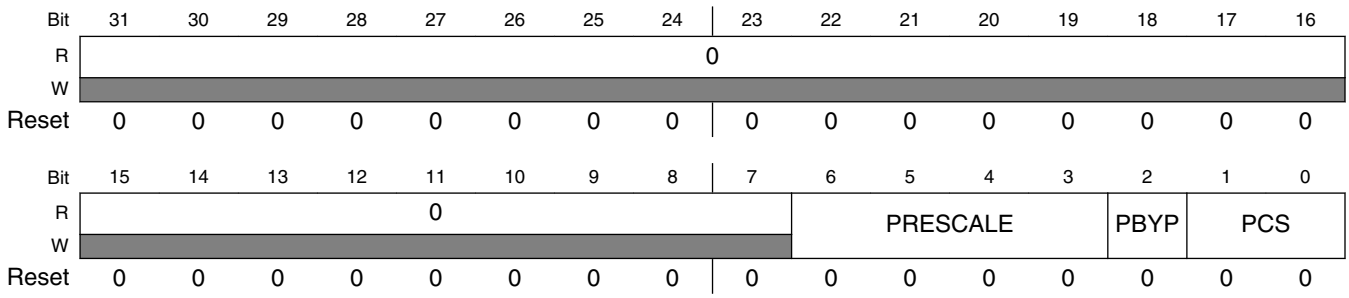
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								TCF	TIE	TPS		TPP	TFC	TMS	TEN
W									w1c							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LPTMRx_CSR field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 TCF	Timer Compare Flag TCF is set when the LPTMR is enabled and the CNR equals the CMR and increments. TCF is cleared when the LPTMR is disabled or a logic 1 is written to it. 0 The value of CNR is not equal to CMR and increments. 1 The value of CNR is equal to CMR and increments.
6 TIE	Timer Interrupt Enable When TIE is set, the LPTMR Interrupt is generated whenever TCF is also set. 0 Timer interrupt disabled. 1 Timer interrupt enabled.
5–4 TPS	Timer Pin Select Configures the input source to be used in Pulse Counter mode. TPS must be altered only when the LPTMR is disabled. The input connections vary by device. See the for information on the connections to these inputs. 00 Pulse counter input 0 is selected. 01 Pulse counter input 1 is selected. 10 Pulse counter input 2 is selected. 11 Pulse counter input 3 is selected.
3 TPP	Timer Pin Polarity Configures the polarity of the input source in Pulse Counter mode. TPP must be changed only when the LPTMR is disabled. 0 Pulse Counter input source is active-high, and the CNR will increment on the rising-edge. 1 Pulse Counter input source is active-low, and the CNR will increment on the falling-edge.
2 TFC	Timer Free-Running Counter When clear, TFC configures the CNR to reset whenever TCF is set. When set, TFC configures the CNR to reset on overflow. TFC must be altered only when the LPTMR is disabled. 0 CNR is reset whenever TCF is set. 1 CNR is reset on overflow.
1 TMS	Timer Mode Select Configures the mode of the LPTMR. TMS must be altered only when the LPTMR is disabled. 0 Time Counter mode. 1 Pulse Counter mode.
0 TEN	Timer Enable When TEN is clear, it resets the LPTMR internal logic, including the CNR and TCF. When TEN is set, the LPTMR is enabled. While writing 1 to this field, CSR[5:1] must not be altered. 0 LPTMR is disabled and internal logic is reset. 1 LPTMR is enabled.

49.4.2 Low Power Timer Prescale Register (LPTMRx_PSR)

Address: Base address + 4h offset



LPTMRx_PSR field descriptions

Field	Description
31–7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6–3 PRESCALE	Prescale Value Configures the size of the Prescaler in Time Counter mode or width of the glitch filter in Pulse Counter mode. PRESCALE must be altered only when the LPTMR is disabled. 0000 Prescaler divides the prescaler clock by 2; glitch filter does not support this configuration. 0001 Prescaler divides the prescaler clock by 4; glitch filter recognizes change on input pin after 2 rising clock edges. 0010 Prescaler divides the prescaler clock by 8; glitch filter recognizes change on input pin after 4 rising clock edges. 0011 Prescaler divides the prescaler clock by 16; glitch filter recognizes change on input pin after 8 rising clock edges. 0100 Prescaler divides the prescaler clock by 32; glitch filter recognizes change on input pin after 16 rising clock edges. 0101 Prescaler divides the prescaler clock by 64; glitch filter recognizes change on input pin after 32 rising clock edges. 0110 Prescaler divides the prescaler clock by 128; glitch filter recognizes change on input pin after 64 rising clock edges. 0111 Prescaler divides the prescaler clock by 256; glitch filter recognizes change on input pin after 128 rising clock edges. 1000 Prescaler divides the prescaler clock by 512; glitch filter recognizes change on input pin after 256 rising clock edges. 1001 Prescaler divides the prescaler clock by 1024; glitch filter recognizes change on input pin after 512 rising clock edges. 1010 Prescaler divides the prescaler clock by 2048; glitch filter recognizes change on input pin after 1024 rising clock edges. 1011 Prescaler divides the prescaler clock by 4096; glitch filter recognizes change on input pin after 2048 rising clock edges. 1100 Prescaler divides the prescaler clock by 8192; glitch filter recognizes change on input pin after 4096 rising clock edges. 1101 Prescaler divides the prescaler clock by 16,384; glitch filter recognizes change on input pin after 8192 rising clock edges.

Table continues on the next page...

LPTMRx_PSR field descriptions (continued)

Field	Description
	1110 Prescaler divides the prescaler clock by 32,768; glitch filter recognizes change on input pin after 16,384 rising clock edges. 1111 Prescaler divides the prescaler clock by 65,536; glitch filter recognizes change on input pin after 32,768 rising clock edges.
2 PBYP	Prescaler Bypass When PBYP is set, the selected prescaler clock in Time Counter mode or selected input source in Pulse Counter mode directly clocks the CNR. When PBYP is clear, the CNR is clocked by the output of the prescaler/glitch filter. PBYP must be altered only when the LPTMR is disabled. 0 Prescaler/glitch filter is enabled. 1 Prescaler/glitch filter is bypassed.
PCS	Prescaler Clock Select Selects the clock to be used by the LPTMR prescaler/glitch filter. PCS must be altered only when the LPTMR is disabled. The clock connections vary by device. **NOTE:** See the chip configuration details for information on the connections to these inputs. 00 Prescaler/glitch filter clock 0 selected. 01 Prescaler/glitch filter clock 1 selected. 10 Prescaler/glitch filter clock 2 selected. 11 Prescaler/glitch filter clock 3 selected.

49.4.3 Low Power Timer Compare Register (LPTMRx_CMR)

Address: Base address + 8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																COMPARE															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LPTMRx_CMR field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
COMPARE	Compare Value When the LPTMR is enabled and the CNR equals the value in the CMR and increments, TCF is set and the hardware trigger asserts until the next time the CNR increments. If the CMR is 0, the hardware trigger will remain asserted until the LPTMR is disabled. If the LPTMR is enabled, the CMR must be altered only when TCF is set.

49.4.4 Low Power Timer Counter Register (LPTMRx_CNR)

NOTE

See LPTMR counter for details on how to read counter value.

Address: Base address + Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																COUNTER															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LPTMRx_CNR field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
COUNTER	Counter Value

49.5 Functional description

49.5.1 LPTMR power and reset

The LPTMR remains powered in all power modes, including low-leakage modes. If the LPTMR is not required to remain operating during a low-power mode, then it must be disabled before entering the mode.

The LPTMR is reset only on global Power On Reset (POR) or Low Voltage Detect (LVD). When configuring the LPTMR registers, the CSR must be initially written with the timer disabled, before configuring the PSR and CMR. Then, CSR[TIE] must be set as the last step in the initialization. This ensures the LPTMR is configured correctly and the LPTMR counter is reset to zero following a warm reset.

49.5.2 LPTMR clocking

The LPTMR prescaler/glitch filter can be clocked by one of the four clocks. The clock source must be enabled before the LPTMR is enabled.

NOTE

The clock source selected need to be configured to remain enabled in low-power modes, otherwise the LPTMR will not operate during low-power modes.

In Pulse Counter mode with the prescaler/glitch filter bypassed, the selected input source directly clocks the CNR and no other clock source is required. To minimize power in this case, configure the prescaler clock source for a clock that is not toggling.

NOTE

The clock source or pulse input source selected for the LPTMR should not exceed the frequency f_{LPTMR} defined in the device datasheet.

49.5.3 LPTMR prescaler/glitch filter

The LPTMR prescaler and glitch filter share the same logic which operates as a prescaler in Time Counter mode and as a glitch filter in Pulse Counter mode.

NOTE

The prescaler/glitch filter configuration must not be altered when the LPTMR is enabled.

49.5.3.1 Prescaler enabled

In Time Counter mode, when the prescaler is enabled, the output of the prescaler directly clocks the CNR. When the LPTMR is enabled, the CNR will increment every 2^2 to 2^{16} prescaler clock cycles. After the LPTMR is enabled, the first increment of the CNR will take an additional one or two prescaler clock cycles due to synchronization logic.

49.5.3.2 Prescaler bypassed

In Time Counter mode, when the prescaler is bypassed, the selected prescaler clock increments the CNR on every clock cycle. When the LPTMR is enabled, the first increment will take an additional one or two prescaler clock cycles due to synchronization logic.

49.5.3.3 Glitch filter

In Pulse Counter mode, when the glitch filter is enabled, the output of the glitch filter directly clocks the CNR. When the LPTMR is first enabled, the output of the glitch filter is asserted, that is, logic 1 for active-high and logic 0 for active-low. The following table shows the change in glitch filter output with the selected input source.

If	Then
The selected input source remains deasserted for at least 2^1 to 2^{15} consecutive prescaler clock rising edges	The glitch filter output will also deassert.
The selected input source remains asserted for at least 2^1 to 2^{15} consecutive prescaler clock rising-edges	The glitch filter output will also assert.

NOTE

The input is only sampled on the rising clock edge.

The CNR will increment each time the glitch filter output asserts. In Pulse Counter mode, the maximum rate at which the CNR can increment is once every 2^2 to 2^{16} prescaler clock edges. When first enabled, the glitch filter will wait an additional one or two prescaler clock edges due to synchronization logic.

49.5.3.4 Glitch filter bypassed

In Pulse Counter mode, when the glitch filter is bypassed, the selected input source increments the CNR every time it asserts. Before the LPTMR is first enabled, the selected input source is forced to be asserted. This prevents the CNR from incrementing if the selected input source is already asserted when the LPTMR is first enabled.

49.5.4 LPTMR compare

When the CNR equals the value of the CMR and increments, the following events occur:

- CSR[TCF] is set.
- LPTMR interrupt is generated if CSR[TIE] is also set.
- LPTMR hardware trigger is generated.
- CNR is reset if CSR[TFC] is clear.

When the LPTMR is enabled, the CMR can be altered only when CSR[TCF] is set. When updating the CMR, the CMR must be written and CSR[TCF] must be cleared before the LPTMR counter has incremented past the new LPTMR compare value.

49.5.5 LPTMR counter

The CNR increments by one on every:

- Prescaler clock in Time Counter mode with prescaler bypassed
- Prescaler output in Time Counter mode with prescaler enabled
- Input source assertion in Pulse Counter mode with glitch filter bypassed
- Glitch filter output in Pulse Counter mode with glitch filter enabled

The CNR is reset when the LPTMR is disabled or if the counter register overflows. If CSR[TFC] is cleared, then the CNR is also reset whenever CSR[TCF] is set.

The CNR continues incrementing when the core is halted in Debug mode when configured for Pulse Counter mode, the CNR will stop incrementing when the core is halted in Debug mode when configured for Time Counter mode.

The CNR cannot be initialized, but can be read at any time. On each read of the CNR, software must first write to the CNR with any value. This will synchronize and register the current value of the CNR into a temporary register. The contents of the temporary register are returned on each read of the CNR.

When reading the CNR, the bus clock must be at least two times faster than the rate at which the LPTMR counter is incrementing, otherwise incorrect data may be returned.

49.5.6 LPTMR hardware trigger

The LPTMR hardware trigger asserts at the same time the CSR[TCF] is set and can be used to trigger hardware events in other peripherals without software intervention. The hardware trigger is always enabled.

When	Then
The CMR is set to 0 with CSR[TFC] clear	The LPTMR hardware trigger will assert on the first compare and does not deassert.
The CMR is set to a nonzero value, or, if CSR[TFC] is set	The LPTMR hardware trigger will assert on each compare and deassert on the following increment of the CNR.

49.5.7 LPTMR interrupt

The LPTMR interrupt is generated whenever CSR[TIE] and CSR[TCF] are set. CSR[TCF] is cleared by disabling the LPTMR or by writing a logic 1 to it.

CSR[TIE] can be altered and CSR[TCF] can be cleared while the LPTMR is enabled.

The LPTMR interrupt is generated asynchronously to the system clock and can be used to generate a wakeup from any low-power mode, including the low-leakage modes, provided the LPTMR is enabled as a wakeup source.

Chapter 50
Carrier Modulator Transmitter (CMT)

50.1 Chip-specific CMT information

50.1.1 Instantiation Information

This device contains one CMT module.

50.2 Introduction

The carrier modulator transmitter (CMT) module provides the means to generate the protocol timing and carrier signals for a wide variety of encoding schemes. The CMT incorporates hardware to off-load the critical and/or lengthy timing requirements associated with signal generation from the CPU, releasing much of its bandwidth to handle other tasks such as:

- Code data generation
- Data decompression, or,
- Keyboard scanning

The CMT does not include dedicated hardware configurations for specific protocols, but is intended to be sufficiently programmable in its function to handle the timing requirements of most protocols with minimal CPU intervention.

When the modulator is disabled, certain CMT registers can be used to change the state of the infrared output (IRO) signal directly. This feature allows for the generation of future protocol timing signals not readily producible by the current architecture.

50.3 Features

The features of this module include:

- Four modes of operation:
  - Time; with independent control of high and low times
  - Baseband
  - Frequency-shift key (FSK)
  - Direct software control of the IRO signal
- Extended space operation in Time, Baseband, and FSK modes
- Selectable input clock divider
- Interrupt on end-of-cycle
  - Ability to disable the IRO signal and use as timer interrupt

50.4 Block diagram

The following figure presents the block diagram of the CMT module.

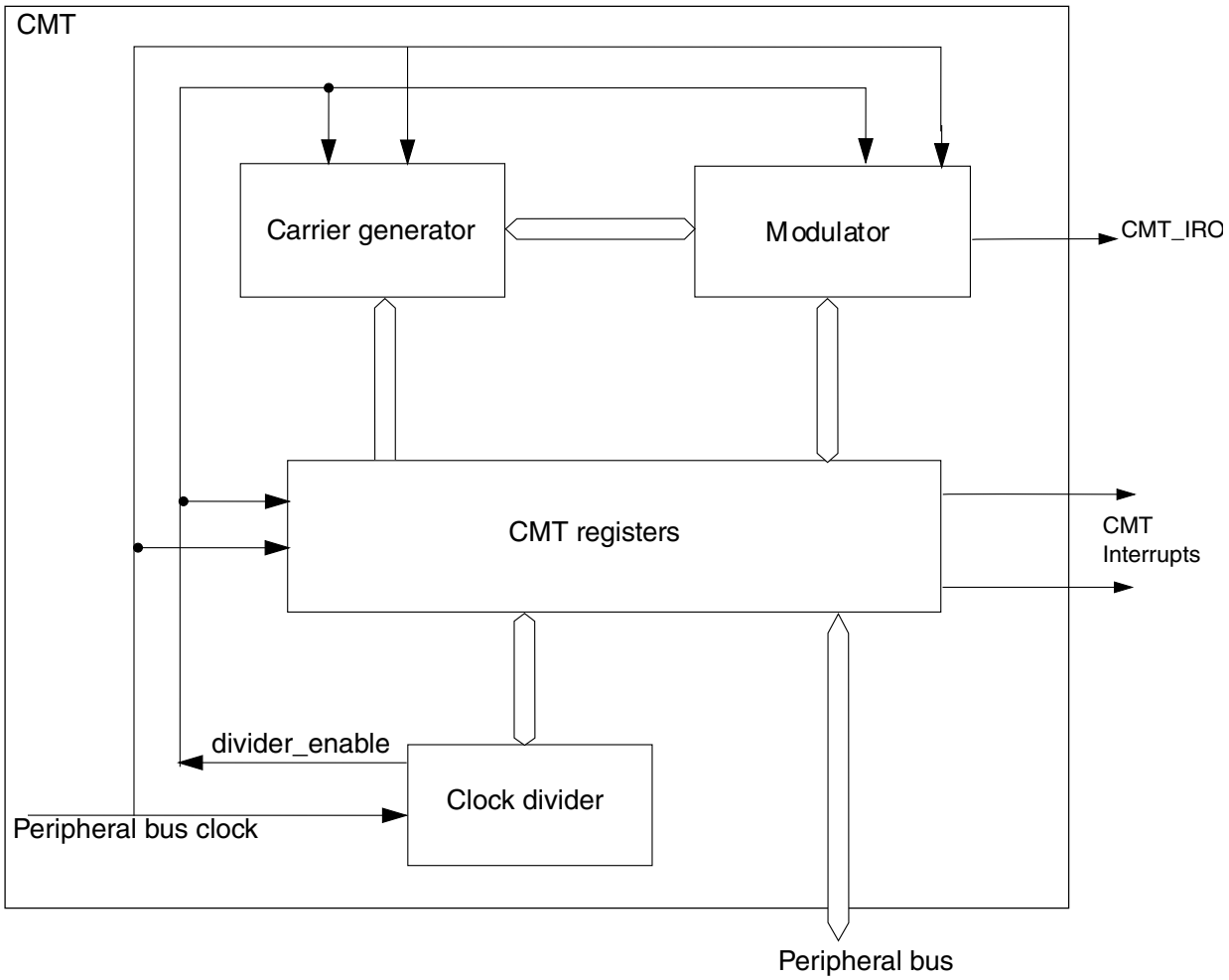


Figure 50-1. CMT module block diagram

50.5 Modes of operation

The following table describes the operation of the CMT module operates in various modes.

Table 50-1. Modes of operation

Modes	Description
Time	In Time mode, the user independently defines the high and low times of the carrier signal to determine both period and duty cycle
Baseband	When MSC[BASE] is set, the carrier output (f_{cg}) to the modulator is held high continuously to allow for the generation of baseband protocols.

Table continues on the next page...

Table 50-1. Modes of operation (continued)

Modes	Description
Frequency-shift key	This mode allows the carrier generator to alternate between two sets of high and low times. When operating in FSK mode, the generator will toggle between the two sets when instructed by the modulator, allowing the user to dynamically switch between two carrier frequencies without CPU intervention.

The following table summarizes the modes of operation of the CMT module.

Table 50-2. CMT modes of operation

Mode	MSC[MCGEN][1]	MSC[BASE]	MSC[FSK][2]	MSC[EXSPC]	Comment
Time	1	0	0	0	f_{cg} controlled by primary high and low registers. f_{cg} transmitted to the IRO signal when modulator gate is open.
Baseband	1	1	X	0	f_{cg} is always high. The IRO signal is high when the modulator gate is open.
FSK	1	0	1	0	f_{cg} control alternates between primary high/low registers and secondary high/low registers. f_{cg} transmitted to the IRO signal when modulator gate is open.
Extended Space	1	X	X	1	Setting MSC[EXSPC] causes subsequent modulator cycles to be spaces (modulator out not asserted) for the duration of the modulator period (mark and space times).
IRO Latch	0	X	X	X	OC[IROL] controls the state of the IRO signal.

1. To prevent spurious operation, initialize all data and control registers before beginning a transmission when MSC[MCGEN]=1.
2. This field is not double-buffered and must not be changed during a transmission while MSC[MCGEN]=1.

NOTE

The assignment of module modes to core modes is chip-specific. For module-to-core mode assignments, see the chapter that describes how modules are configured.

50.5.1 Wait mode operation

During Wait mode, the CMT if enabled, will continue to operate normally. However, there is no change in operating modes of CMT during Wait mode, because the CPU is not operating.

50.5.2 Stop mode operation

This section describes the CMT Stop mode operations.

50.5.2.1 Normal Stop mode operation

During Normal Stop mode, clocks to the CMT module are halted. No registers are affected.

The CMT module will resume upon exit from Normal Stop mode because the clocks are halted. Software must ensure that the Normal Stop mode is not entered while the modulator is still in operation so as to prevent the IRO signal from being asserted while in Normal Stop mode. This may require a timeout period from the time that MSC[MCGEN] is cleared to allow the last modulator cycle to complete.

50.5.2.2 Low-Power Stop mode operation

During Low-Power Stop mode, the CMT module is completely powered off internally and the IRO signal state is latched and held at the time when the CMT enters this mode. To prevent the IRO signal from being asserted during Low-Power Stop mode, the software must assure that the signal is not active when entering Low-Power Stop mode. Upon wakeup from Low-Power Stop mode, the CMT module will be in the reset state.

50.6 CMT external signal descriptions

The following table shows the description of the external signal.

Table 50-3. CMT signal description

Signal	Description	I/O
CMT_IRO	Infrared Output	O

50.6.1 CMT_IRO — Infrared Output

This output signal is driven by the modulator output when MSC[MCGEN] and OC[IROPEN] are set. The IRO signal starts a valid transmission with a delay, after MSC[MCGEN] bit be asserted to high, that can be calculated based on two register bits. Table 50-4 shows how to calculate this delay.

The following table describes conditions for the IRO signal to be active.

If	Then
MSC[MCGEN] is cleared and OC[IROPEN] is set	The signal is driven by OC[IROL] . This enables user software to directly control the state of the IRO signal by writing to OC[IROL] .
OC[IROPEN] is cleared	The signal is disabled and is not driven by the CMT module. Therefore, CMT can be configured as a modulo timer for generating periodic interrupts without causing signal activity.

Table 50-4. CMT_IRO signal delay calculation

Condition	Delay (bus clock cycles)
MSC[CMTDIV] = 0	PPS[PPSDIV] + 2
MSC[CMTDIV] > 0	(PPS[PPSDIV] *2) + 3

50.7 Memory map/register definition

The following registers control and monitor the CMT operation.

The address of a register is the sum of a base address and an address offset. The base address is defined at the chip level. The address offset is defined at the module level.

CMT memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4006_2000	CMT Carrier Generator High Data Register 1 (CMT_CGH1)	8	R/W	Undefined	50.7.1/1647
4006_2001	CMT Carrier Generator Low Data Register 1 (CMT_CGL1)	8	R/W	Undefined	50.7.2/1648
4006_2002	CMT Carrier Generator High Data Register 2 (CMT_CGH2)	8	R/W	Undefined	50.7.3/1648
4006_2003	CMT Carrier Generator Low Data Register 2 (CMT_CGL2)	8	R/W	Undefined	50.7.4/1649
4006_2004	CMT Output Control Register (CMT_OC)	8	R/W	00h	50.7.5/1649
4006_2005	CMT Modulator Status and Control Register (CMT_MSC)	8	R/W	00h	50.7.6/1650
4006_2006	CMT Modulator Data Register Mark High (CMT_CMD1)	8	R/W	Undefined	50.7.7/1652

Table continues on the next page...

CMT memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4006_2007	CMT Modulator Data Register Mark Low (CMT_CMD2)	8	R/W	Undefined	50.7.8/1653
4006_2008	CMT Modulator Data Register Space High (CMT_CMD3)	8	R/W	Undefined	50.7.9/1653
4006_2009	CMT Modulator Data Register Space Low (CMT_CMD4)	8	R/W	Undefined	50.7.10/ 1654
4006_200A	CMT Primary Prescaler Register (CMT_PPS)	8	R/W	00h	50.7.11/ 1654
4006_200B	CMT Direct Memory Access Register (CMT_DMA)	8	R/W	00h	50.7.12/ 1655

50.7.1 CMT Carrier Generator High Data Register 1 (CMT_CGH1)

This data register contains the primary high value for generating the carrier output.

Address: 4006_2000h base + 0h offset = 4006_2000h

Bit	7	6	5	4	3	2	1	0
Read Write	PH							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

CMT_CGH1 field descriptions

Field	Description
PH	Primary Carrier High Time Data Value Contains the number of input clocks required to generate the carrier high time period. When operating in Time mode, this register is always selected. When operating in FSK mode, this register and the secondary register pair are alternately selected under the control of the modulator. The primary carrier high time value is undefined out of reset. This register must be written to nonzero values before the carrier generator is enabled to avoid spurious results.

50.7.2 CMT Carrier Generator Low Data Register 1 (CMT_CGL1)

This data register contains the primary low value for generating the carrier output.

Address: 4006_2000h base + 1h offset = 4006_2001h

Bit	7	6	5	4	3	2	1	0
Read Write	PL							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

CMT_CGL1 field descriptions

Field	Description
PL	Primary Carrier Low Time Data Value Contains the number of input clocks required to generate the carrier low time period. When operating in Time mode, this register is always selected. When operating in FSK mode, this register and the secondary register pair are alternately selected under the control of the modulator. The primary carrier low time value is undefined out of reset. This register must be written to nonzero values before the carrier generator is enabled to avoid spurious results.

50.7.3 CMT Carrier Generator High Data Register 2 (CMT_CGH2)

This data register contains the secondary high value for generating the carrier output.

Address: 4006_2000h base + 2h offset = 4006_2002h

Bit	7	6	5	4	3	2	1	0
Read Write	SH							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

CMT_CGH2 field descriptions

Field	Description
SH	Secondary Carrier High Time Data Value Contains the number of input clocks required to generate the carrier high time period. When operating in Time mode, this register is never selected. When operating in FSK mode, this register and the primary register pair are alternately selected under control of the modulator.

CMT_CGH2 field descriptions (continued)

Field	Description
	The secondary carrier high time value is undefined out of reset. This register must be written to nonzero values before the carrier generator is enabled when operating in FSK mode.

50.7.4 CMT Carrier Generator Low Data Register 2 (CMT_CGL2)

This data register contains the secondary low value for generating the carrier output.

Address: 4006_2000h base + 3h offset = 4006_2003h

Bit	7	6	5	4	3	2	1	0
Read Write	SL							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

CMT_CGL2 field descriptions

Field	Description
SL	Secondary Carrier Low Time Data Value Contains the number of input clocks required to generate the carrier low time period. When operating in Time mode, this register is never selected. When operating in FSK mode, this register and the primary register pair are alternately selected under the control of the modulator. The secondary carrier low time value is undefined out of reset. This register must be written to nonzero values before the carrier generator is enabled when operating in FSK mode.

50.7.5 CMT Output Control Register (CMT_OC)

This register is used to control the IRO signal of the CMT module.

Address: 4006_2000h base + 4h offset = 4006_2004h

Bit	7	6	5	4	3	2	1	0
Read	IROL	CMTPOL	IROPEN	0				
Write								
Reset	0	0	0	0	0	0	0	0

CMT_OC field descriptions

Field	Description
7 IROL	IRO Latch Control Reads the state of the IRO latch. Writing to IROL changes the state of the IRO signal when MSC[MCGEN] is cleared and IROPEN is set.
6 CMTPOL	CMT Output Polarity Controls the polarity of the IRO signal. 0 The IRO signal is active-low. 1 The IRO signal is active-high.
5 IROPEN	IRO Pin Enable Enables and disables the IRO signal. When the IRO signal is enabled, it is an output that drives out either the CMT transmitter output or the state of IROL depending on whether MSC[MCGEN] is set or not. Also, the state of output is either inverted or non-inverted, depending on the state of CMTPOL. When the IRO signal is disabled, it is in a high-impedance state and is unable to draw any current. This signal is disabled during reset. 0 The IRO signal is disabled. 1 The IRO signal is enabled as output.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

50.7.6 CMT Modulator Status and Control Register (CMT_MSC)

This register contains the modulator and carrier generator enable (MCGEN), end of cycle interrupt enable (EOCIE), FSK mode select (FSK), baseband enable (BASE), extended space (EXSPC), prescaler (CMTDIV) bits, and the end of cycle (EOCF) status bit.

Address: 4006_2000h base + 5h offset = 4006_2005h

Bit	7	6	5	4	3	2	1	0
Read	EOCF	CMTDIV		EXSPC	BASE	FSK	EOCIE	MCGEN
Write								
Reset	0	0	0	0	0	0	0	0

CMT_MSC field descriptions

Field	Description
7 EOCF	End Of Cycle Status Flag Sets when:

Table continues on the next page...

CMT_MSC field descriptions (continued)

Field	Description
	• The modulator is not currently active and MCGEN is set to begin the initial CMT transmission. • At the end of each modulation cycle while MCGEN is set. This is recognized when a match occurs between the contents of the space period register and the down counter. At this time, the counter is initialized with, possibly new contents of the mark period buffer, CMD1 and CMD2, and the space period register is loaded with, possibly new contents of the space period buffer, CMD3 and CMD4. This flag is cleared by reading MSC followed by an access of CMD2 or CMD4, or by the DMA transfer. 0 End of modulation cycle has not occured since the flag last cleared. 1 End of modulator cycle has occurred.
6–5 CMTDIV	CMT Clock Divide Prescaler Causes the CMT to be clocked at the IF signal frequency, or the IF frequency divided by 2 ,4, or 8 . This field must not be changed during a transmission because it is not double-buffered. 00 IF ÷ 1 01 IF ÷ 2 10 IF ÷ 4 11 IF ÷ 8
4 EXSPC	Extended Space Enable Enables the extended space operation. 0 Extended space is disabled. 1 Extended space is enabled.
3 BASE	Baseband Enable When set, BASE disables the carrier generator and forces the carrier output high for generation of baseband protocols. When BASE is cleared, the carrier generator is enabled and the carrier output toggles at the frequency determined by values stored in the carrier data registers. This field is cleared by reset. This field is not double-buffered and must not be written to during a transmission. 0 Baseband mode is disabled. 1 Baseband mode is enabled.
2 FSK	FSK Mode Select Enables FSK operation. 0 The CMT operates in Time or Baseband mode. 1 The CMT operates in FSK mode.
1 EOCIE	End of Cycle Interrupt Enable Requests to enable a CPU interrupt when EOCF is set if EOCIE is high.

Table continues on the next page...

CMT_MSC field descriptions (continued)

Field	Description
	0 CPU interrupt is disabled. 1 CPU interrupt is enabled.
0 MCGEN	Modulator and Carrier Generator Enable Setting MCGEN will initialize the carrier generator and modulator and will enable all clocks. When enabled, the carrier generator and modulator will function continuously. When MCGEN is cleared, the current modulator cycle will be allowed to expire before all carrier and modulator clocks are disabled to save power and the modulator output is forced low. **NOTE:** To prevent spurious operation, the user should initialize all data and control registers before enabling the system. 0 Modulator and carrier generator disabled 1 Modulator and carrier generator enabled

50.7.7 CMT Modulator Data Register Mark High (CMT_CMD1)

The contents of this register are transferred to the modulator down counter upon the completion of a modulation period.

Address: 4006_2000h base + 6h offset = 4006_2006h

Bit	7	6	5	4	3	2	1	0
Read Write	MB[15:8]							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

CMT_CMD1 field descriptions

Field	Description
MB[15:8]	MB[15:8] Controls the upper mark periods of the modulator for all modes.

50.7.8 CMT Modulator Data Register Mark Low (CMT_CMD2)

The contents of this register are transferred to the modulator down counter upon the completion of a modulation period.

Address: 4006_2000h base + 7h offset = 4006_2007h

Bit	7	6	5	4	3	2	1	0
Read Write	MB[7:0]							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

CMT_CMD2 field descriptions

Field	Description
MB[7:0]	MB[7:0] Controls the lower mark periods of the modulator for all modes.

50.7.9 CMT Modulator Data Register Space High (CMT_CMD3)

The contents of this register are transferred to the space period register upon the completion of a modulation period.

Address: 4006_2000h base + 8h offset = 4006_2008h

Bit	7	6	5	4	3	2	1	0
Read Write	SB[15:8]							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

CMT_CMD3 field descriptions

Field	Description
SB[15:8]	SB[15:8] Controls the upper space periods of the modulator for all modes.

50.7.10 CMT Modulator Data Register Space Low (CMT_CMD4)

The contents of this register are transferred to the space period register upon the completion of a modulation period.

Address: 4006_2000h base + 9h offset = 4006_2009h

Bit	7	6	5	4	3	2	1	0
Read Write	SB[7:0]							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

CMT_CMD4 field descriptions

Field	Description
SB[7:0]	SB[7:0] Controls the lower space periods of the modulator for all modes.

50.7.11 CMT Primary Prescaler Register (CMT_PPS)

This register is used to set the Primary Prescaler Divider field (PPSDIV).

Address: 4006_2000h base + Ah offset = 4006_200Ah

Bit	7	6	5	4	3	2	1	0
Read	0				PPSDIV			
Write								
Reset	0	0	0	0	0	0	0	0

CMT_PPS field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
PPSDIV	Primary Prescaler Divider Divides the CMT clock to generate the Intermediate Frequency clock enable to the secondary prescaler. 0000 Bus clock ÷ 1 0001 Bus clock ÷ 2 0010 Bus clock ÷ 3

Table continues on the next page...

CMT_PPS field descriptions (continued)

Field	Description
	0011 Bus clock ÷ 4 0100 Bus clock ÷ 5 0101 Bus clock ÷ 6 0110 Bus clock ÷ 7 0111 Bus clock ÷ 8 1000 Bus clock ÷ 9 1001 Bus clock ÷ 10 1010 Bus clock ÷ 11 1011 Bus clock ÷ 12 1100 Bus clock ÷ 13 1101 Bus clock ÷ 14 1110 Bus clock ÷ 15 1111 Bus clock ÷ 16

50.7.12 CMT Direct Memory Access Register (CMT_DMA)

This register is used to enable/disable direct memory access (DMA).

Address: 4006_2000h base + Bh offset = 4006_200Bh

Bit	7	6	5	4	3	2	1	0
Read	0							DMA
Write								
Reset	0	0	0	0	0	0	0	0

CMT_DMA field descriptions

Field	Description
7–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 DMA	DMA Enable Enables the DMA protocol. 0 DMA transfer request and done are disabled. 1 DMA transfer request and done are enabled.

50.8 Functional description

The CMT module primarily consists of clock divider, carrier generator, and modulator.

50.8.1 Clock divider

The CMT was originally designed to be based on an 8 MHz bus clock that could be divided by 1, 2, 4, or 8 according to the specification. To be compatible with higher bus frequency, the primary prescaler (PPS) was developed to receive a higher frequency and generate a clock enable signal called intermediate frequency (IF). This IF must be approximately equal to 8 MHz and will work as a clock enable to the secondary prescaler. The following figure shows the clock divider block diagram.

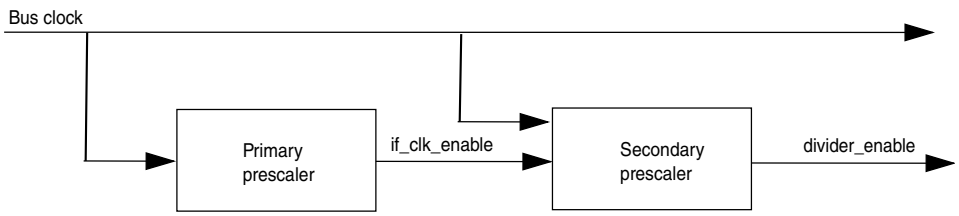


Figure 50-2. Clock divider block diagram

For compatibility with previous versions of CMT, when bus clock = 8 MHz, the PPS must be configured to zero. The PPS counter is selected according to the bus clock to generate an intermediate frequency approximately equal to 8 MHz.

50.8.2 Carrier generator

The carrier generator resolution is 125 ns when operating with an 8 MHz intermediate frequency signal and the secondary prescaler is set to divide by 1, or, when MSC[CMTDIV] = 00. The carrier generator can generate signals with periods between 250 ns (4 MHz) and 127.5 µs (7.84 kHz) in steps of 125 ns. The following table shows the relationship between the clock divide bits and the carrier generator resolution, minimum carrier generator period, and minimum modulator period.

Table 50-5. Clock divider

Bus clock (MHz)	MSC[CMTDIV]	Carrier generator resolution (µs)	Min. carrier generator period (µs)	Min. modulator period (µs)
8	00	0.125	0.25	1.0
8	01	0.25	0.5	2.0
8	10	0.5	1.0	4.0
8	11	1.0	2.0	8.0

The possible duty cycle options depend upon the number of counts required to complete the carrier period. For example, 1.6 MHz signal has a period of 625 ns and will therefore require 5 x 125 ns counts to generate. These counts may be split between high and low times, so the duty cycles available will be:

- 20% with one high and four low times
- 40% with two high and three low times
- 60% with three high and two low times, and
- 80% with four high and one low time

.

For low-frequency signals with large periods, high-resolution duty cycles as a percentage of the total period, are possible.

The carrier signal is generated by counting a register-selected number of input clocks (125 ns for an 8 MHz bus) for both the carrier high time and the carrier low time. The period is determined by the total number of clocks counted. The duty cycle is determined by the ratio of high-time clocks to total clocks counted. The high and low time values are user-programmable and are held in two registers.

An alternate set of high/low count values is held in another set of registers to allow the generation of dual-frequency FSK protocols without CPU intervention.

Note

Only nonzero data values are allowed. The carrier generator will not work if any of the count values are equal to zero.

MSC[MCGEN] must be set and MSC[BASE] must be cleared to enable carrier generator clocks. When MSC[BASE] is set, the carrier output to the modulator is held high continuously. The following figure represents the block diagram of the clock generator.

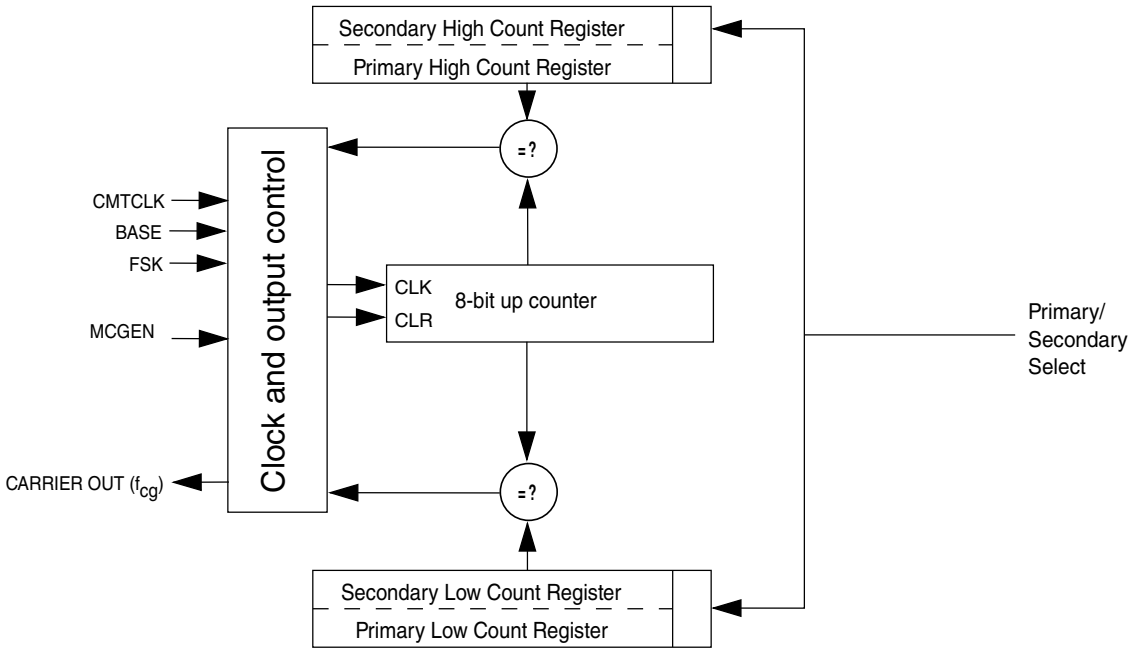


Figure 50-3. Carrier generator block diagram

The high/low time counter is an 8-bit up counter. After each increment, the contents of the counter are compared with the appropriate high or low count value register. When the compare value is reached, the counter is reset to a value of 0x01, and the compare is redirected to the other count value register.

Assuming that the high time count compare register is currently active, a valid compare will cause the carrier output to be driven low. The counter will continue to increment starting at the reset value of 0x01. When the value stored in the selected low count value register is reached, the counter will again be reset and the carrier output will be driven high.

The cycle repeats, automatically generating a periodic signal which is directed to the modulator. The lower frequency with maximum period, f_{max}, and highest frequency with minimum period, f_{min}, which can be generated, are defined as:

$f_{max} = f_{CMTCLK} \div (2 * 1)$ Hz

$f_{min} = f_{CMTCLK} \div (2 * (2^8 - 1))$ Hz

In the general case, the carrier generator output frequency is:

$f_{cg} = f_{CMTCLK} \div$ (High count + Low count) Hz

Where: 0 < High count < 256 and

0 < Low count < 256

The duty cycle of the carrier signal is controlled by varying the ratio of high time to low + high time. As the input clock period is fixed, the duty cycle resolution will be proportional to the number of counts required to generate the desired carrier period.

$$\text{DutyCycle} = \frac{\text{Highcount}}{\text{Highcount+Lowcount}}$$

50.8.3 Modulator

The modulator block controls the state of the infrared out signal (IRO). The modulator output is gated on to the IRO signal when the modulator/carrier generator is enabled. . When the modulator/carrier generator is disabled, the IRO signal is controlled by the state of the IRO latch. OC[CMTPOL] enables the IRO signal to be active-high or active-low.

The following table describes the functions of the modulators in different modes:

Table 50-6. Mode functions

Mode	Function
Time	The modulator can gate the carrier onto the modulator output.
Baseband	The modulator can control the logic level of the modulator output.
FSK	The modulator can count carrier periods and instruct the carrier generator to alternate between two carrier frequencies whenever a modulation period consisting of mark and space counts, expires.

The modulator provides a simple method to control protocol timing. The modulator has a minimum resolution of 1.0 µs with an 8 MHz. It can count bus clocks to provide real-time control, or carrier clocks for self-clocked protocols.

The modulator includes a 17-bit down counter with underflow detection. The counter is loaded from the 16-bit modulation mark period buffer registers, CMD1 and CMD2. The most significant bit is loaded with a logic 0 and serves as a sign bit.

When	Then
The counter holds a positive value	The modulator gate is open and the carrier signal is driven to the transmitter block.
The counter underflows	The modulator gate is closed and a 16-bit comparator is enabled which compares the logical complement of the value of the down counter with the contents of the modulation space period register which has been loaded from the registers, CMD3 and CMD4.

When a match is obtained, the cycle repeats by opening the modulator gate, reloading the counter with the contents of CMD1 and CMD2, and reloading the modulation space period register with the contents of CMD3 and CMD4.

The modulation space period is activated when the carrier signal is low to prohibit cutting off the high pulse of a carrier signal. If the carrier signal is high, the modulator extends the mark period until the carrier signal becomes low. To deassert the space period and assert the mark period, the carrier signal must have gone low to ensure that a space period is not erroneously shortened.

If the contents of the modulation space period register are all zeroes, the match will be immediate and no space period will be generated, for instance, for FSK protocols that require successive bursts of different frequencies).

MSC[MCGEN] must be set to enable the modulator timer.

The following figure presents the block diagram of the modulator.

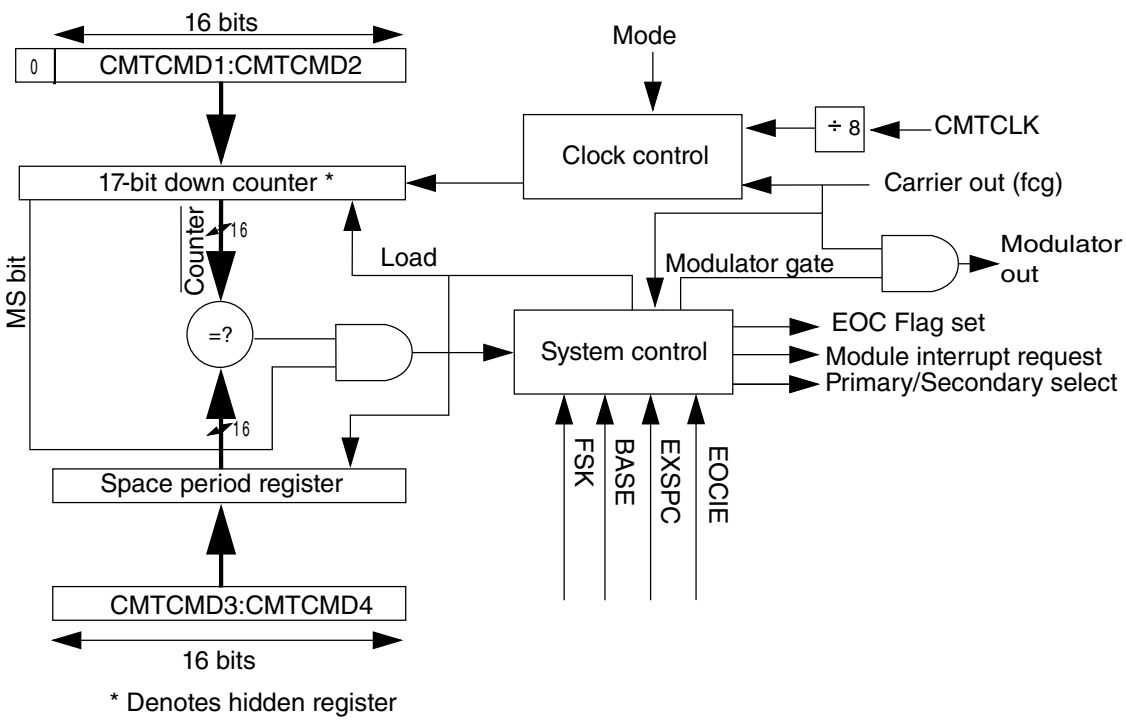


Figure 50-4. Modulator block diagram

50.8.3.1 Time mode

When the modulator operates in Time mode, or, when MSC[MCGEN] is set, and MSC[BASE] and MSC[FSK] are cleared:

- The modulation mark period consists of an integer number of (CMTCLK ÷ 8) clock periods.
- The modulation space period consists of 0 or an integer number of (CMTCLK ÷ 8) clock periods.

With an 8 MHz IF and MSC[CMTDIV] = 00, the modulator resolution is 1 µs and has a maximum mark and space period of about 65.535 ms each . See Figure 50-5 for an example of the Time and Baseband mode outputs.

The mark and space time equations for Time and Baseband mode are:

t_{mark} = (CMD1:CMD2 + 1) ÷ (f_{CMTCLK} ÷ 8)

t_{space} = CMD3:CMD4 ÷ (f_{CMTCLK} ÷ 8)

where CMD1:CMD2 and CMD3:CMD4 are the decimal values of the concatenated registers.

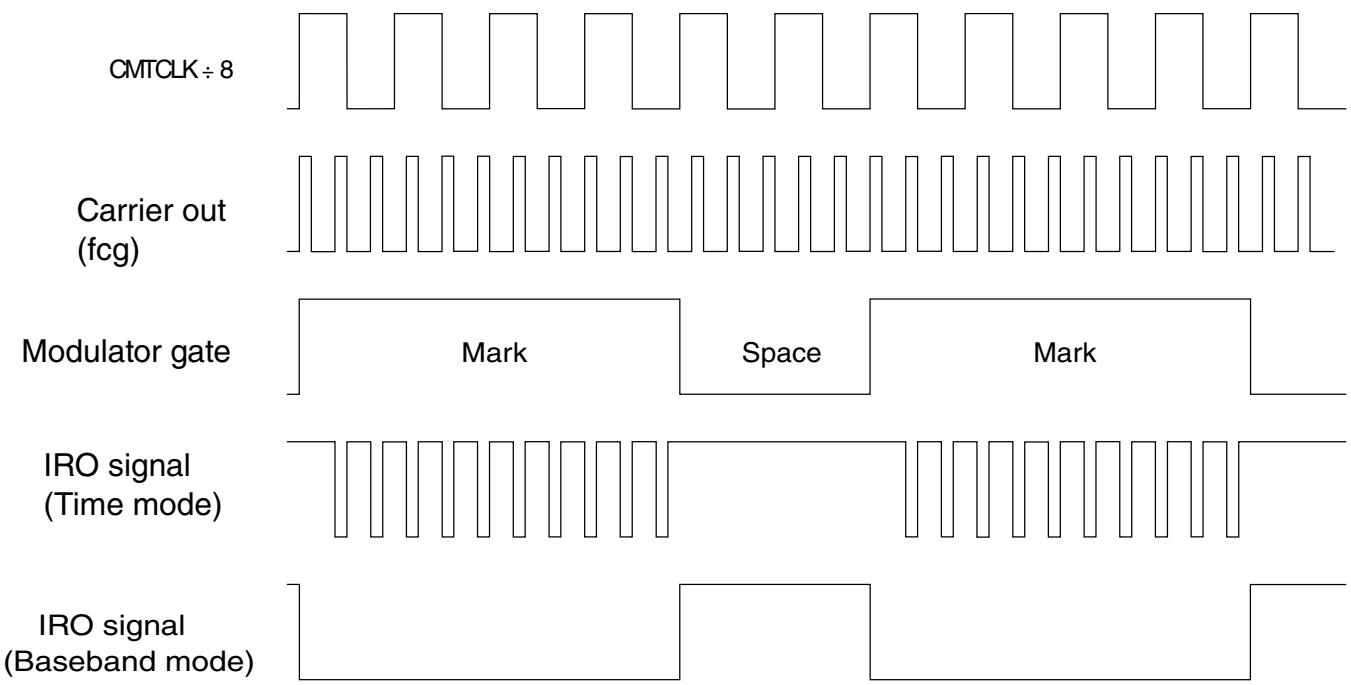


Figure 50-5. Example: CMT output in Time and Baseband modes with OC[CMTPOL]=0

50.8.3.2 Baseband mode

Baseband mode, that is, when MSC[MCGEN] and MSC[BASE] are set, is a derivative of Time mode, where the mark and space period is based on (CMTCLK ÷ 8) counts. The mark and space calculations are the same as in Time mode.

In this mode, the modulator output will be at a logic 1 for the duration of the mark period and at a logic 0 for the duration of a space period. See Figure 50-5 for an example of the output for both Baseband and Time modes. In the example, the carrier out frequency (f_{cg}) is generated with a high count of 0x01 and a low count of 0x02 that results in a divide of 3 of CMTCLK with a 33% duty cycle. The modulator down counter was loaded with the value 0x0003 and the space period register with 0x0002.

Note

The waveforms in Figure 50-5 and Figure 50-6 are for the purpose of conceptual illustration and are not meant to represent precise timing relationships between the signals shown.

50.8.3.3 FSK mode

When the modulator operates in FSK mode, that is, when MSC[MCGEN] and MSC[FSK] are set, and MSC[BASE] is cleared:

- The modulation mark and space periods consist of an integer number of carrier clocks (space period can be zero).
- When the mark period expires, the space period is transparently started as in Time mode.
- The carrier generator toggles between primary and secondary data register values whenever the modulator space period expires.

The space period provides an interpulse gap (no carrier). If CMD3:CMD4 = 0x0000, then the modulator and carrier generator will switch between carrier frequencies without a gap or any carrier glitches (zero space).

Using timing data for carrier burst and interpulse gap length calculated by the CPU, FSK mode can automatically generate a phase-coherent, dual-frequency FSK signal with programmable burst and interburst gaps.

The mark and space time equations for FSK mode are:

t_{mark} = (CMD1:CMD2 + 1) ÷ f_{cg}

t_{space} = (CMD3:CMD4) ÷ f_{cg}

Where f_{cg} is the frequency output from the carrier generator. The example in Figure 50-6 shows what the IRO signal looks like in FSK mode with the following values:

- CMD1:CMD2 = 0x0003
- CMD3:CMD4 = 0x0002
- Primary carrier high count = 0x01
- Primary carrier low count = 0x02

- Secondary carrier high count = 0x03
- Secondary carrier low count = 0x01

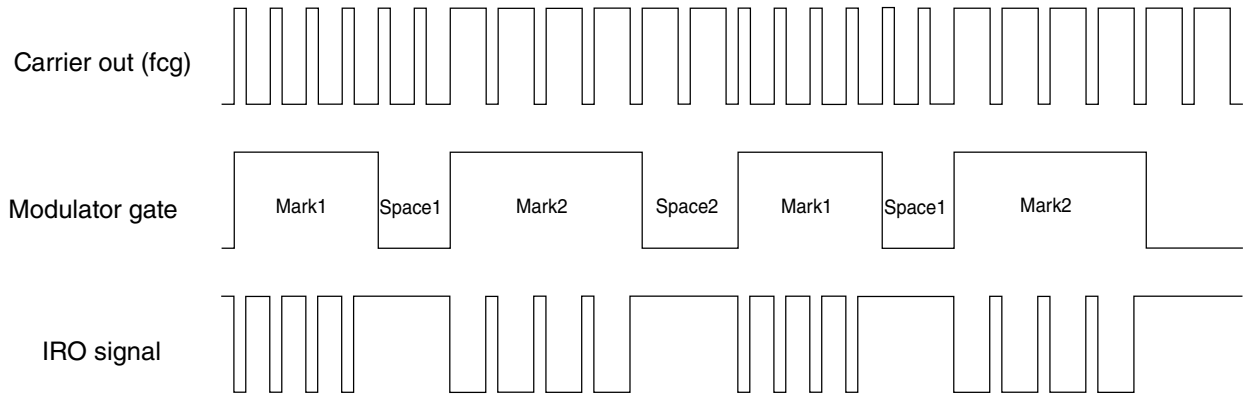


Figure 50-6. Example: CMT output in FSK mode

50.8.4 Extended space operation

In either Time, Baseband, or FSK mode, the space period can be made longer than the maximum possible value of the space period register. Setting MSC[EXSPC] will force the modulator to treat the next modulation period beginning with the next load of the counter and space period register, as a space period equal in length to the mark and space counts combined. Subsequent modulation periods will consist entirely of these extended space periods with no mark periods. Clearing MSC[EXSPC] will return the modulator to standard operation at the beginning of the next modulation period.

50.8.4.1 EXSPC operation in Time mode

To calculate the length of an extended space in Time or Baseband mode, add the mark and space times and multiply by the number of modulation periods when MSC[EXSPC] is set.

$t_{exspace} = (t_{mark} + t_{space})$ * (number of modulation periods)

For an example of extended space operation, see Figure 50-7.

Note

The extended space enable feature can be used to emulate a zero mark event.

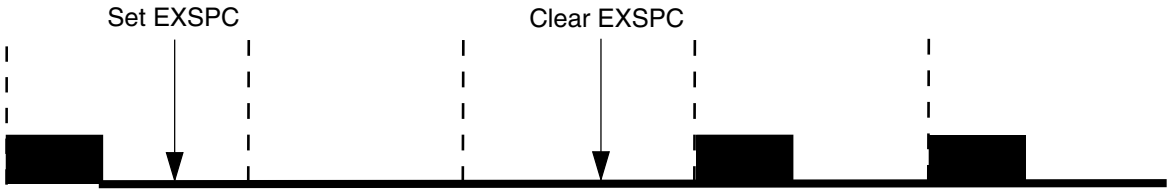


Figure 50-7. Extended space operation

50.8.4.2 EXSPC operation in FSK mode

In FSK mode, the modulator continues to count carrier out clocks, alternating between the primary and secondary registers at the end of each modulation period.

To calculate the length of an extended space in FSK mode, it is required to know whether MSC[EXSPC] was set on a primary or secondary modulation period, and the total number of both primary and secondary modulation periods completed while MSC[EXSPC] is high. A status bit for the current modulation is not accessible to the CPU. If necessary, software must maintain tracking of the current primary or secondary modulation cycle. The extended space period ends at the completion of the space period time of the modulation period during which MSC[EXSPC]is cleared.

The following table depicts the equations which can be used to calculate the extended space period depending on when MSC[EXSPC] is set.

If	Then
MSC[EXSPC] was set during a primary modulation cycle	Use the equation: $t_{exspace} = (t_{space})_p + (t_{mark} + t_{space})_s + (t_{mark} + t_{space})_p + ...$
MSC[EXSPC] bit was set during a secondary modulation cycle	Use the equation: $t_{exspace} = (t_{space})_s + (t_{mark} + t_{space})_p + (t_{mark} + t_{space})_s + ...$

Where the subscripts p and s refer to mark and space times for the primary and secondary modulation cycles.

50.9 CMT interrupts and DMA

The CMT generates an interrupt request or a DMA transfer request according to MSC[EOCIE], MSC[EOCF], DMA[DMA] bits.

Table 50-7. DMA transfer request x CMT interrupt request

MSC[EOCF]	DMA[DMA]	MSC[EOCIE]	DMA transfer request	CMT interrupt request
0	X	X	0	0
1	X	0	0	0
1	0	1	0	1
1	1	1	1	0

MSC[EOCF] is set:

- When the modulator is not currently active and MSC[MCGEN] is set to begin the initial CMT transmission.
- At the end of each modulation cycle when the counter is reloaded from CMD1:CMD2, while MSC[MCGEN] is set.

When MSC[MCGEN] is cleared and then set before the end of the modulation cycle, MSC[EOCF] will not be set when MSC[MCGEN] is set, but will become set at the end of the current modulation cycle.

When MSC[MCGEN] becomes disabled, the CMT module does not set MSC[EOCF] at the end of the last modulation cycle.

If MSC[EOCIE] is high when MSC[EOCF] is set, the CMT module will generate an interrupt request or a DMA transfer request.

MSC[EOCF] must be cleared to prevent from being generated by another event like interrupt or DMA request, after exiting the service routine. See the following table.

Table 50-8. How to clear MSC[EOCF]

DMA[DMA]	MSC[EOCIE]	Description
0	X	MSC[EOCF] is cleared by reading MSC followed by an access of CMD2 or CMD4.
1	X	MSC[EOCF] is cleared by the CMT DMA transfer done.

The EOC interrupt is coincident with:

- Loading the down-counter with the contents of CMD1:CMD2
- Loading the space period register with the contents of CMD3:CMD4

The EOC interrupt provides a means for the user to reload new mark/space values into the modulator data registers. Modulator data register updates will take effect at the end of the current modulation cycle.

NOTE

The down-counter and space period register are updated at the end of every modulation cycle, irrespective of interrupt handling and the state of MSC[EOCF].

Chapter 51
Programmable Delay Block (PDB)

51.1 Chip-specific PDB information

51.1.1 PDB Instantiation

51.1.1.1 PDB Output Triggers

Table 51-1. PDB output triggers

Number of PDB channels for ADC trigger	1 for ADC0
Number of pre-triggers per PDB channel	2
Number of DAC triggers	1 for DAC0
Number of PulseOut	1 per CMP

51.1.1.2 PDB Input Trigger Connections

Table 51-2. PDB Input Trigger Options

PDB Trigger	PDB Input
0000	External Trigger
0001	CMP 0
0010	CMP 1
0011	Reserved
0100	PIT Ch 0 Output
0101	PIT Ch 1 Output
0110	PIT Ch 2 Output
0111	PIT Ch 3 Output

Table continues on the next page...

Table 51-2. PDB Input Trigger Options (continued)

PDB Trigger	PDB Input
1000	FTM0 initialization trigger and channel triggers, as programmed in the FTM external trigger register (EXTTRIG)
1001	FTM1 initialization trigger and channel triggers, as programmed in the FTM external trigger register (EXTTRIG)
1010	FTM2 initialization trigger and channel triggers, as programmed in the FTM external trigger register (EXTTRIG)
1011	FTM3 initialization trigger and channel triggers, as programmed in the FTM external trigger register (EXTTRIG)
1100	RTC Alarm
1101	RTC Seconds
1110	LPTMR Output
1111	Software Trigger

51.1.2 PDB Module Interconnections

PDB trigger outputs	Connection
Channel 0 triggers	ADC0 trigger
Channel 1 triggers	synchronous input 1 of FTM0
DAC triggers	DAC0 trigger
Pulse-out	Pulse-out connected to each CMP module's sample/window input to control sample operation

51.1.3 Back-to-back acknowledgement connections

In this MCU, PDB back-to-back operation acknowledgment connections are implemented as follows:

- PDB channel 0 pre-trigger 0 acknowledgement input: ADC0SC1B_COCO
- PDB channel 0 pre-trigger 1 acknowledgement input: ADC0SC1A_COCO
- PDB channel 1 pre-trigger 0 acknowledgement input: Not Used
- PDB channel 1 pre-trigger 1 acknowledgement input: Not Used

So, the back-to-back chain is connected as a ring:

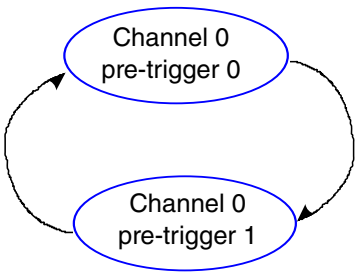


Figure 51-1. PDB back-to-back chain

The application code can set the PDB*x*_CH*n*C1[BB] bits to configure the PDB pre-triggers as a single chain or several chains.

51.1.4 PDB Interval Trigger Connections to DAC

In this MCU, PDB interval trigger connections to DAC are implemented as follows.

- PDB interval trigger 0 connects to DAC0 hardware trigger input.

51.1.5 DAC External Trigger Input Connections

In this MCU, the following DAC external trigger inputs are implemented.

- DAC external trigger input 0: ADC0SC1A_COCO

NOTE

Application code can set the PDBx_DACINTCn[EXT] bit to allow DAC external trigger input when the corresponding ADC Conversion complete flag, ADCx_SC1n[COCO], is set.

51.1.6 Pulse-Out Connection

Individual PDB Pulse-Out signals are connected to each CMP block and used for sample window.

51.1.7 Pulse-Out Enable Register Implementation

The following table shows the comparison of pulse-out enable register at the module and chip level.

Table 51-3. PDB pulse-out enable register

Register	Module implementation	Chip implementation
POnEN	7:0 - POEN 31:8 - Reserved	0 - POEN[0] for CMP0 1 - POEN[1] for CMP1 31:2 - Reserved

51.2 Introduction

The Programmable Delay Block (PDB) provides controllable delays from either an internal or an external trigger, or a programmable interval tick, to the hardware trigger inputs of ADCs and/or generates the interval triggers to DACs, so that the precise timing between ADC conversions and/or DAC updates can be achieved. The PDB can optionally provide pulse outputs (Pulse-Out's) that are used as the sample window in the CMP block.

51.2.1 Features

- Up to 15 trigger input sources and one software trigger source
- Up to 8 configurable PDB channels for ADC hardware trigger
  - One PDB channel is associated with one ADC
  - One trigger output for ADC hardware trigger and up to 8 pre-trigger outputs for ADC trigger select per PDB channel
  - Trigger outputs can be enabled or disabled independently
  - One 16-bit delay register per pre-trigger output
  - Optional bypass of the delay registers of the pre-trigger outputs
  - Operation in One-Shot or Continuous modes
  - Optional back-to-back mode operation, which enables the ADC conversions complete to trigger the next PDB channel
  - One programmable delay interrupt

    - One sequence error interrupt
    - One channel flag and one sequence error flag per pre-trigger
    - DMA support
- Up to 8 DAC interval triggers
    - One interval trigger output per DAC
    - One 16-bit delay interval register per DAC trigger output
    - Optional bypass of the delay interval trigger registers
    - Optional external triggers
- Up to 8 pulse outputs (pulse-out's)
    - Pulse-out's can be enabled or disabled independently
    - Programmable pulse width

NOTE

The number of PDB input and output triggers are chip-specific. See the chip-specific PDB information for details.

51.2.2 Implementation

In this section, the following letters refer to the number of output triggers:

- N—Total available number of PDB channels.
- n—PDB channel number, valid from 0 to *N*-1.
- M—Total available pre-trigger per PDB channel.
- m—Pre-trigger number, valid from 0 to *M*-1.
- X—Total number of DAC interval triggers.
- x—DAC interval trigger output number, valid from 0 to *X*-1.
- Y—Total number of Pulse-Out's.
- y—Pulse-Out number, valid value is from 0 to *Y*-1.

NOTE

The number of module output triggers to core is chip-specific. For module to core output triggers implementation, see the chip configuration information.

51.2.3 Back-to-back acknowledgment connections

PDB back-to-back operation acknowledgment connections are chip-specific. For implementation, see the chip configuration information.

51.2.4 DAC External Trigger Input Connections

The implementation of DAC external trigger inputs is chip-specific. See the chip configuration information for details.

51.2.5 Block diagram

This diagram illustrates the major components of the PDB.

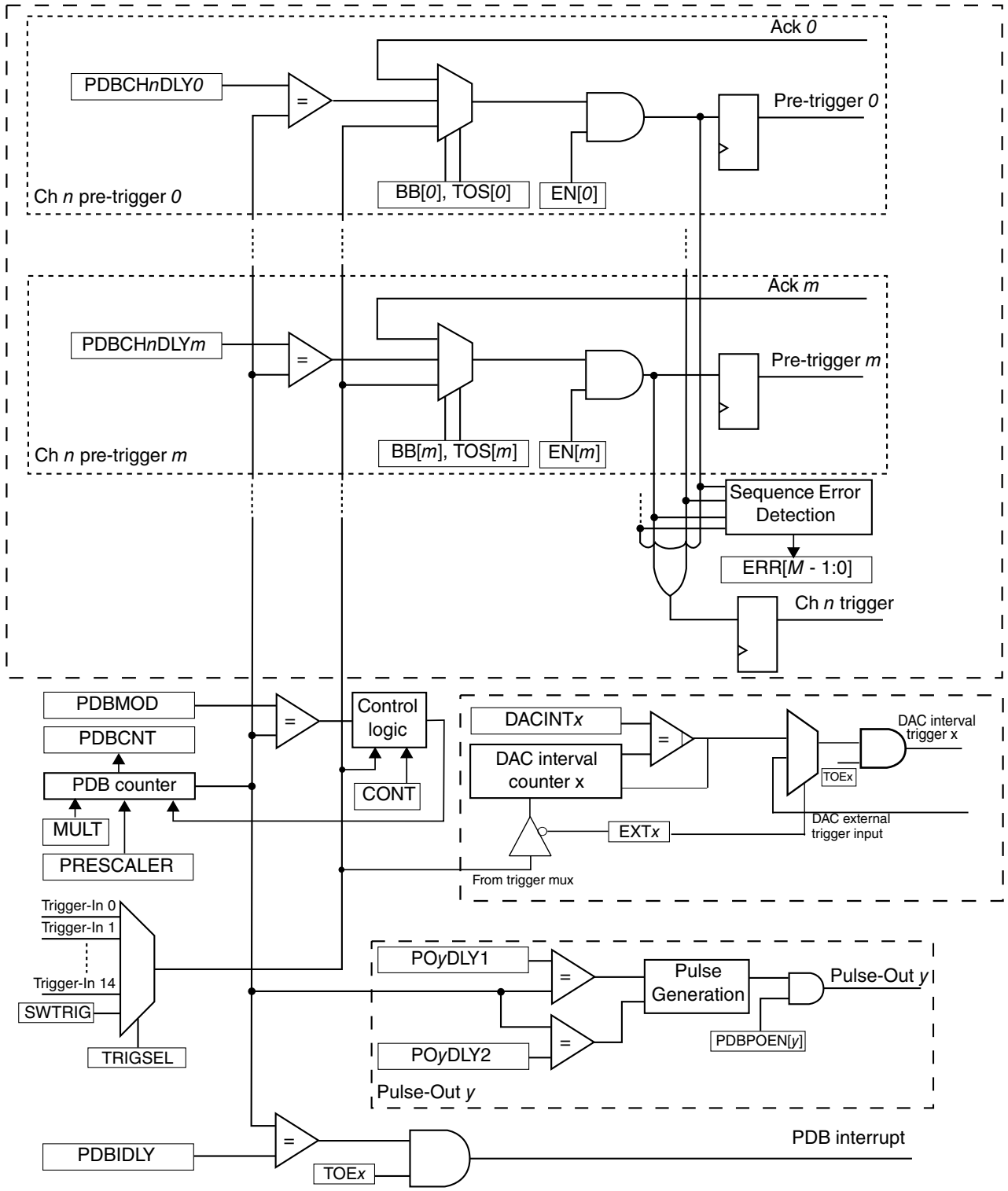


Figure 51-2. PDB block diagram

In this diagram, only one PDB channel *n*, one DAC interval trigger *x*, and one Pulse-Out *y* are shown. The PDB-enabled control logic and the sequence error interrupt logic are not shown.

51.2.6 Modes of operation

PDB ADC trigger operates in the following modes:

- Disabled—Counter is off, all pre-trigger and trigger outputs are low if PDB is not in back-to-back operation of Bypass mode.
- Debug—Counter is paused when processor is in Debug mode, and the counter for the DAC trigger is also paused in Debug mode.
- Enabled One-Shot—Counter is enabled and restarted at count zero upon receiving a positive edge on the selected trigger input source or software trigger is selected and SC[SWTRIG] is written with 1. In each PDB channel, an enabled pre-trigger asserts once per trigger input event. The trigger output asserts whenever any of the pre-triggers is asserted.
- Enabled Continuous—Counter is enabled and restarted at count zero. The counter is rolled over to zero again when the count reaches the value specified in the modulus register, and the counting is restarted. This enables a continuous stream of pre-triggers/trigger outputs as a result of a single trigger input event.
- Enabled Bypassed—The pre-trigger and trigger outputs assert immediately after a positive edge on the selected trigger input source or software trigger is selected and SC[SWTRIG] is written with 1, that is the delay registers are bypassed. It is possible to bypass any one or more of the delay registers; therefore, this mode can be used in conjunction with One-Shot or Continuous mode.

51.3 PDB signal descriptions

This table shows the detailed description of the external signal.

Table 51-4. PDB signal descriptions

Signal	Description	I/O
EXTRG	External Trigger Input Source If the PDB is enabled and external trigger input source is selected, a positive edge on the EXTRG signal resets and starts the counter.	I

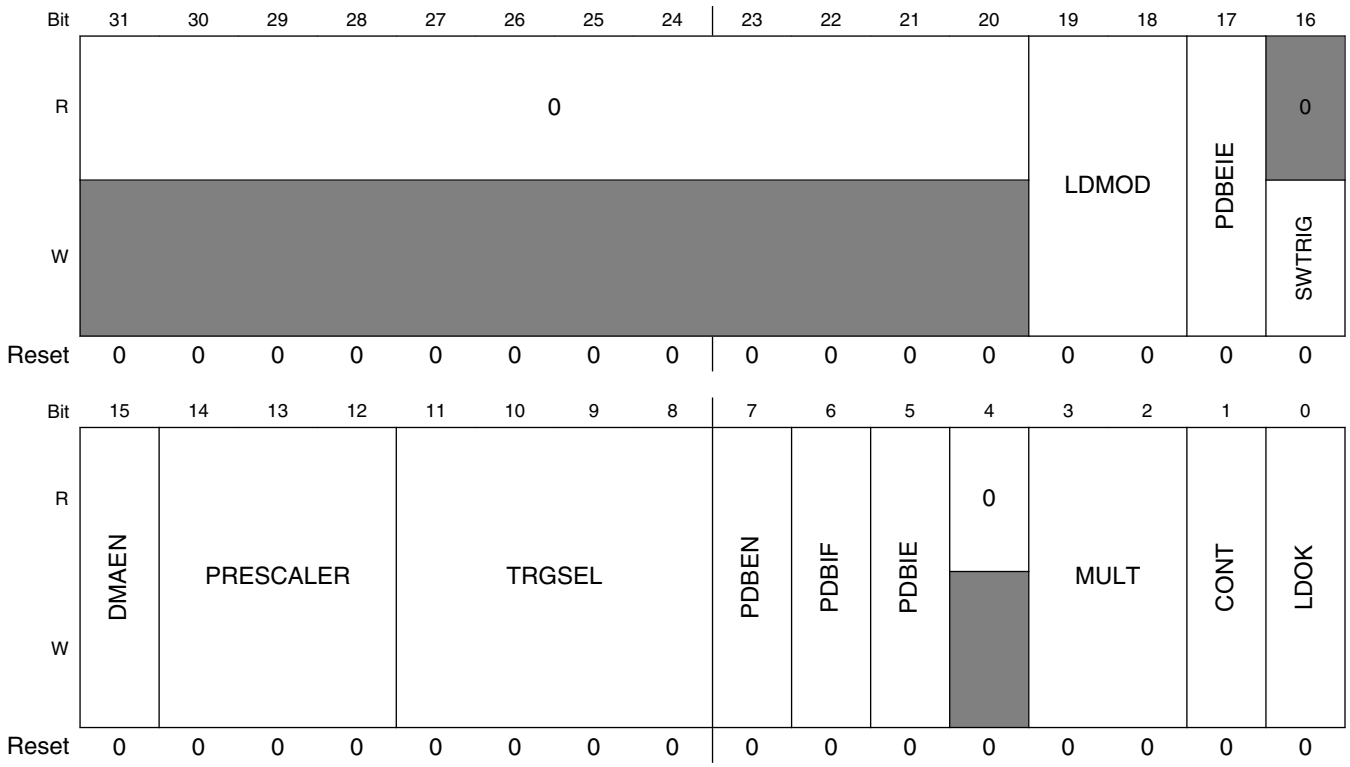
51.4 Memory map and register definition

PDB memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_6000	Status and Control register (PDB0_SC)	32	R/W	0000_0000h	51.4.1/1676
4003_6004	Modulus register (PDB0_MOD)	32	R/W	0000_FFFFh	51.4.2/1678
4003_6008	Counter register (PDB0_CNT)	32	R	0000_0000h	51.4.3/1679
4003_600C	Interrupt Delay register (PDB0_IDLY)	32	R/W	0000_FFFFh	51.4.4/1679
4003_6010	Channel n Control register 1 (PDB0_CH0C1)	32	R/W	0000_0000h	51.4.5/1680
4003_6014	Channel n Status register (PDB0_CH0S)	32	R/W	0000_0000h	51.4.6/1681
4003_6018	Channel n Delay 0 register (PDB0_CH0DLY0)	32	R/W	0000_0000h	51.4.7/1681
4003_601C	Channel n Delay 1 register (PDB0_CH0DLY1)	32	R/W	0000_0000h	51.4.8/1682
4003_6150	DAC Interval Trigger n Control register (PDB0_DACINTC0)	32	R/W	0000_0000h	51.4.9/1682
4003_6154	DAC Interval n register (PDB0_DACINT0)	32	R/W	0000_0000h	51.4.10/ 1683
4003_6190	Pulse-Out n Enable register (PDB0_POEN)	32	R/W	0000_0000h	51.4.11/ 1683
4003_6194	Pulse-Out n Delay register (PDB0_PO0DLY)	32	R/W	0000_0000h	51.4.12/ 1684
4003_6198	Pulse-Out n Delay register (PDB0_PO1DLY)	32	R/W	0000_0000h	51.4.12/ 1684

51.4.1 Status and Control register (PDBx_SC)

Address: 4003_6000h base + 0h offset = 4003_6000h



PDBx_SC field descriptions

Field	Description
31–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–18 LDMOD	Load Mode Select Selects the mode to load the MOD, IDLY, CH*n*DLY*m*, INT*x*, and PO*y*DLY registers, after 1 is written to LDOK. 00 The internal registers are loaded with the values from their buffers immediately after 1 is written to LDOK. 01 The internal registers are loaded with the values from their buffers when the PDB counter reaches the MOD register value after 1 is written to LDOK. 10 The internal registers are loaded with the values from their buffers when a trigger input event is detected after 1 is written to LDOK. 11 The internal registers are loaded with the values from their buffers when either the PDB counter reaches the MOD register value or a trigger input event is detected, after 1 is written to LDOK.
17 PDBEIE	PDB Sequence Error Interrupt Enable Enables the PDB sequence error interrupt. When this field is set, any of the PDB channel sequence error flags generates a PDB sequence error interrupt.

Table continues on the next page...

PDBx_SC field descriptions (continued)

Field	Description
	0 PDB sequence error interrupt disabled. 1 PDB sequence error interrupt enabled.
16 SWTRIG	Software Trigger When PDB is enabled and the software trigger is selected as the trigger input source, writing 1 to this field resets and restarts the counter. Writing 0 to this field has no effect. Reading this field results 0.
15 DMAEN	DMA Enable When DMA is enabled, the PDBIF flag generates a DMA request instead of an interrupt. 0 DMA disabled. 1 DMA enabled.
14–12 PRESCALER	Prescaler Divider Select 000 Counting uses the peripheral clock divided by multiplication factor selected by MULT. 001 Counting uses the peripheral clock divided by twice of the multiplication factor selected by MULT. 010 Counting uses the peripheral clock divided by four times of the multiplication factor selected by MULT. 011 Counting uses the peripheral clock divided by eight times of the multiplication factor selected by MULT. 100 Counting uses the peripheral clock divided by 16 times of the multiplication factor selected by MULT. 101 Counting uses the peripheral clock divided by 32 times of the multiplication factor selected by MULT. 110 Counting uses the peripheral clock divided by 64 times of the multiplication factor selected by MULT. 111 Counting uses the peripheral clock divided by 128 times of the multiplication factor selected by MULT.
11–8 TRGSEL	Trigger Input Source Select Selects the trigger input source for the PDB. The trigger input source can be internal or external (EXTRG pin), or the software trigger. Refer to chip configuration details for the actual PDB input trigger connections. 0000 Trigger-In 0 is selected. 0001 Trigger-In 1 is selected. 0010 Trigger-In 2 is selected. 0011 Trigger-In 3 is selected. 0100 Trigger-In 4 is selected. 0101 Trigger-In 5 is selected. 0110 Trigger-In 6 is selected. 0111 Trigger-In 7 is selected. 1000 Trigger-In 8 is selected. 1001 Trigger-In 9 is selected. 1010 Trigger-In 10 is selected. 1011 Trigger-In 11 is selected. 1100 Trigger-In 12 is selected. 1101 Trigger-In 13 is selected. 1110 Trigger-In 14 is selected. 1111 Software trigger is selected.

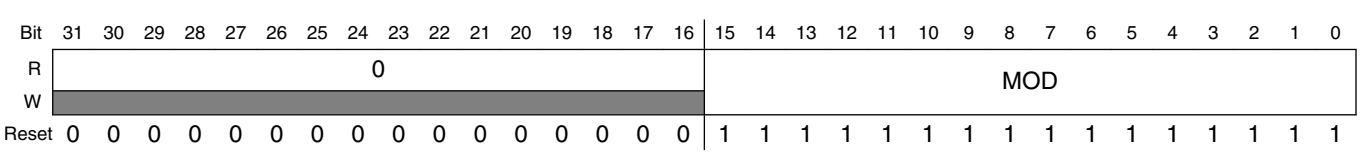
Table continues on the next page...

PDBx_SC field descriptions (continued)

Field	Description
7 PDBEN	PDB Enable 0 PDB disabled. Counter is off. 1 PDB enabled.
6 PDBIF	PDB Interrupt Flag This field is set when the counter value is equal to the IDLY register. Writing zero clears this field.
5 PDBIE	PDB Interrupt Enable Enables the PDB interrupt. When this field is set and DMAEN is cleared, PDBIF generates a PDB interrupt. 0 PDB interrupt disabled. 1 PDB interrupt enabled.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3–2 MULT	Multiplication Factor Select for Prescaler Selects the multiplication factor of the prescaler divider for the counter clock. 00 Multiplication factor is 1. 01 Multiplication factor is 10. 10 Multiplication factor is 20. 11 Multiplication factor is 40.
1 CONT	Continuous Mode Enable Enables the PDB operation in Continuous mode. 0 PDB operation in One-Shot mode 1 PDB operation in Continuous mode
0 LDOK	Load OK Writing 1 to this bit updates the internal registers of MOD, IDLY, CHnDLYm, DACINTx,and POyDLY with the values written to their buffers. The MOD, IDLY, CHnDLYm, DACINTx, and POyDLY will take effect according to the LDMOD. After 1 is written to the LDOK field, the values in the buffers of above registers are not effective and the buffers cannot be written until the values in buffers are loaded into their internal registers. LDOK can be written only when PDBEN is set or it can be written at the same time with PDBEN being written to 1. It is automatically cleared when the values in buffers are loaded into the internal registers or the PDBEN is cleared. Writing 0 to it has no effect.

51.4.2 Modulus register (PDBx_MOD)

Address: 4003_6000h base + 4h offset = 4003_6004h



PDBx_MOD field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
MOD	PDB Modulus Specifies the period of the counter. When the counter reaches this value, it will be reset back to zero. If the PDB is in Continuous mode, the count begins anew. Reading this field returns the value of the internal register that is effective for the current cycle of PDB.

51.4.3 Counter register (PDBx_CNT)

Address: 4003_6000h base + 8h offset = 4003_6008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																CNT															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PDBx_CNT field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CNT	PDB Counter Contains the current value of the counter.

51.4.4 Interrupt Delay register (PDBx_IDLY)

Address: 4003_6000h base + Ch offset = 4003_600Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																IDLY															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

PDBx_IDLY field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
IDLY	PDB Interrupt Delay Specifies the delay value to schedule the PDB interrupt. It can be used to schedule an independent interrupt at some point in the PDB cycle. If enabled, a PDB interrupt is generated, when the counter is

Table continues on the next page...

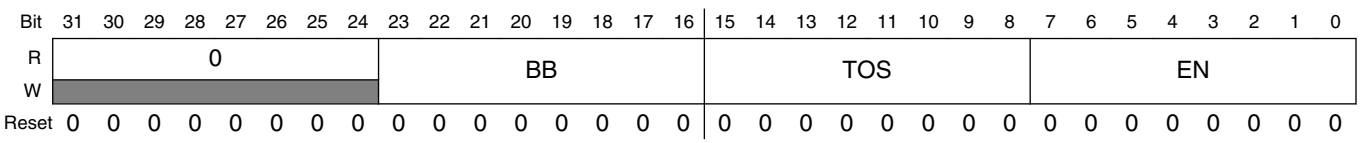
PDBx_IDLY field descriptions (continued)

Field	Description
	equal to the IDLY. Reading this field returns the value of internal register that is effective for the current cycle of the PDB.

51.4.5 Channel n Control register 1 (PDBx_CH*n*C1)

Each PDB channel has one control register, CHnC1. The fields in this register control the functionality of each PDB channel operation.

Address: 4003_6000h base + 10h offset + (40d × i), where i=0d to 0d

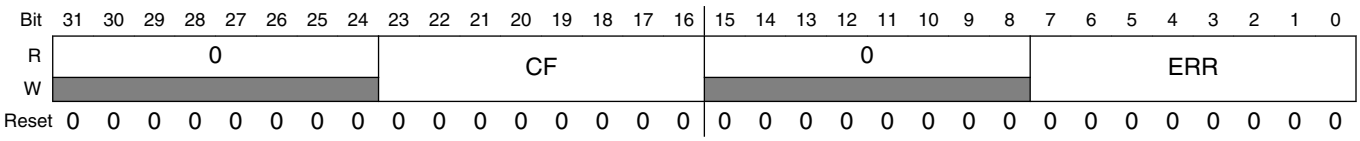


PDBx_CH*n*C1 field descriptions

Field	Description
31–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23–16 BB	PDB Channel Pre-Trigger Back-to-Back Operation Enable Enables the PDB ADC pre-trigger operation as back-to-back mode. Only lower M pre-trigger bits are implemented in this MCU. Back-to-back operation enables the ADC conversions complete to trigger the next PDB channel pre-trigger and trigger output, so that the ADC conversions can be triggered on the next set of configuration and results registers. Application code must enable only the back-to-back operation of the PDB pre-triggers at the leading of the back-to-back connection chain. 0 PDB channel's corresponding pre-trigger back-to-back operation disabled. 1 PDB channel's corresponding pre-trigger back-to-back operation enabled.
15–8 TOS	PDB Channel Pre-Trigger Output Select These bits select the PDB ADC pre-trigger outputs. Only lower M pre-trigger bits are implemented in this MCU. 0 PDB channel's corresponding pre-trigger is in bypassed mode. The pre-trigger asserts one peripheral clock cycle after a rising edge is detected on selected trigger input source or software trigger is selected and SWTRIG is written with 1. 1 PDB channel's corresponding pre-trigger asserts when the counter reaches the channel delay register plus one peripheral clock cycle after a rising edge is detected on selected trigger input source or software trigger is selected and SETRIG is written with 1.
EN	PDB Channel Pre-Trigger Enable Enables the PDB ADC pre-trigger outputs. Only lower M pre-trigger fields are implemented in this MCU. 0 PDB channel's corresponding pre-trigger disabled. 1 PDB channel's corresponding pre-trigger enabled.

51.4.6 Channel n Status register (PDBx_CHnS)

Address: 4003_6000h base + 14h offset + (40d × i), where i=0d to 0d

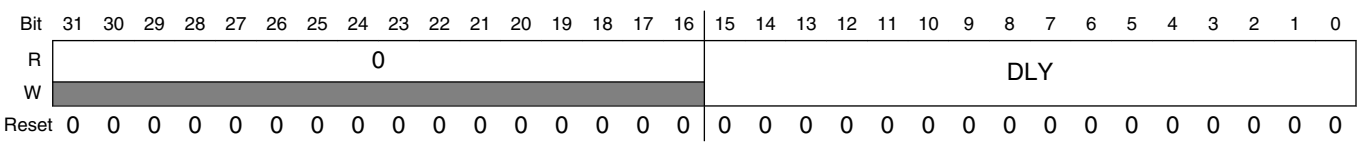


PDBx_CHnS field descriptions

Field	Description
31–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23–16 CF	PDB Channel Flags The CF[*m*] field is set when the PDB counter matches the CH*n*DLY*m*. Write 0 to clear these bits.
15–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
ERR	PDB Channel Sequence Error Flags Only the lower M bits are implemented in this MCU. 0 Sequence error not detected on PDB channel's corresponding pre-trigger. 1 Sequence error detected on PDB channel's corresponding pre-trigger. ADCn block can be triggered for a conversion by one pre-trigger from PDB channel *n*. When one conversion, which is triggered by one of the pre-triggers from PDB channel *n*, is in progress, new trigger from PDB channel's corresponding pre-trigger m cannot be accepted by ADCn, and ERR[m] is set. Writing 0's to clear the sequence error flags.

51.4.7 Channel n Delay 0 register (PDBx_CHnDLY0)

Address: 4003_6000h base + 18h offset + (40d × i), where i=0d to 0d



PDBx_CHnDLY0 field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
DLY	PDB Channel Delay Specifies the delay value for the channel's corresponding pre-trigger. The pre-trigger asserts when the counter is equal to DLY. Reading this field returns the value of internal register that is effective for the current PDB cycle.

51.4.8 Channel n Delay 1 register (PDBx_CHnDLY1)

Address: 4003_6000h base + 1Ch offset + (40d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																DLY															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PDBx_CHnDLY1 field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
DLY	PDB Channel Delay These bits specify the delay value for the channel's corresponding pre-trigger. The pre-trigger asserts when the counter is equal to DLY. Reading these bits returns the value of internal register that is effective for the current PDB cycle.

51.4.9 DAC Interval Trigger n Control register (PDBx_DACINTCn)

Address: 4003_6000h base + 150h offset + (8d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0														EXT	TOE
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PDBx_DACINTCn field descriptions

Field	Description
31–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 EXT	DAC External Trigger Input Enable This bit enables the external trigger for DAC interval counter. 0 DAC external trigger input disabled. DAC interval counter is reset and started counting when a rising edge is detected on selected trigger input source or software trigger is selected and SWTRIG is written with 1. 1 DAC external trigger input enabled. DAC interval counter is bypassed and DAC external trigger input triggers the DAC interval trigger.

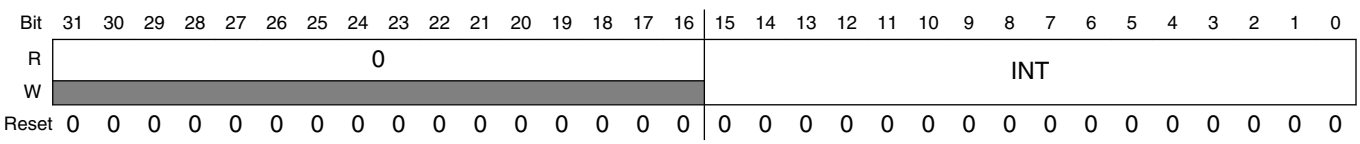
Table continues on the next page...

PDBx_DACINTC*n* field descriptions (continued)

Field	Description
0 TOE	DAC Interval Trigger Enable Enables the DAC interval trigger. 0 DAC interval trigger disabled. 1 DAC interval trigger enabled.

51.4.10 DAC Interval n register (PDBx_DACINT*n*)

Address: 4003_6000h base + 154h offset + (8d × i), where i=0d to 0d

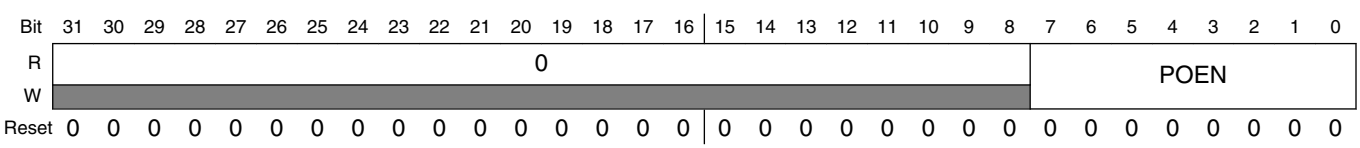


PDBx_DACINT*n* field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
INT	DAC Interval These bits specify the interval value for DAC interval trigger. DAC interval trigger triggers DAC[1:0] update when the DAC interval counter is equal to the DACINT. Reading these bits returns the value of internal register that is effective for the current PDB cycle.

51.4.11 Pulse-Out n Enable register (PDBx_POEN)

Address: 4003_6000h base + 190h offset = 4003_6190h



PDBx_POEN field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
POEN	PDB Pulse-Out Enable Enables the pulse output. Only lower Y bits are implemented in this MCU.

Table continues on the next page...

PDBx_POEN field descriptions (continued)

Field	Description
	0 PDB Pulse-Out disabled 1 PDB Pulse-Out enabled

51.4.12 Pulse-Out n Delay register (PDBx_POnDLY)

Address: 4003_6000h base + 194h offset + (4d × i), where i=0d to 1d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	DLY1																DLY2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PDBx_POnDLY field descriptions

Field	Description
31–16 DLY1	PDB Pulse-Out Delay 1 Specifies the delay 1 value for the PDB Pulse-Out. Pulse-Out goes high when the PDB counter is equal to the DLY1. Reading this field returns the value of internal register that is effective for the current PDB cycle.
DLY2	PDB Pulse-Out Delay 2 Specifies the delay 2 value for the PDB Pulse-Out. Pulse-Out goes low when the PDB counter is equal to the DLY2. Reading this field returns the value of internal register that is effective for the current PDB cycle.

51.5 Functional description

51.5.1 PDB pre-trigger and trigger outputs

The PDB contains a counter whose output is compared to several different digital values. If the PDB is enabled, then a trigger input event will reset the counter and make it start to count. A trigger input event is defined as a rising edge being detected on a selected trigger input source, or if a software trigger is selected and SC[SWTRIG] is written with 1. For each channel, a delay *m* determines the time between assertion of the trigger input event to the time at which changes in the pre-trigger *m* output signal are started. The time is defined as:

- Trigger input event to pre-trigger *m* = (prescaler × multiplication factor × delay *m*) + 2 peripheral clock cycles
- Add 1 additional peripheral clock cycle to determine the time when the channel trigger output changes.

Each channel is associated with 1 ADC block. PDB channel n pre-trigger outputs 0 to *M*; each pre-trigger output is connected to ADC hardware trigger select and hardware trigger inputs. The pre-triggers are used to precondition the ADC block before the actual trigger occurs. When the ADC receives the rising edge of the trigger, the ADC will start the conversion according to the precondition determined by the pre-triggers. The ADC contains *M* sets of configuration and result registers, allowing it to alternate conversions between *M* different analog sources (like a ping-pong game). The pre-trigger outputs are used to specify which signal will be sampled next. When a pre-trigger *m* is asserted, the ADC conversion is triggered with set *m* of the configuration and result registers.

The waveforms shown in the following diagram show the pre-trigger and trigger outputs of PDB channel *n*. The delays can be independently set using the CH*n*DLY*m* registers, and the pre-triggers can be enabled or disabled in CH*n*C1[EN[*m*]].

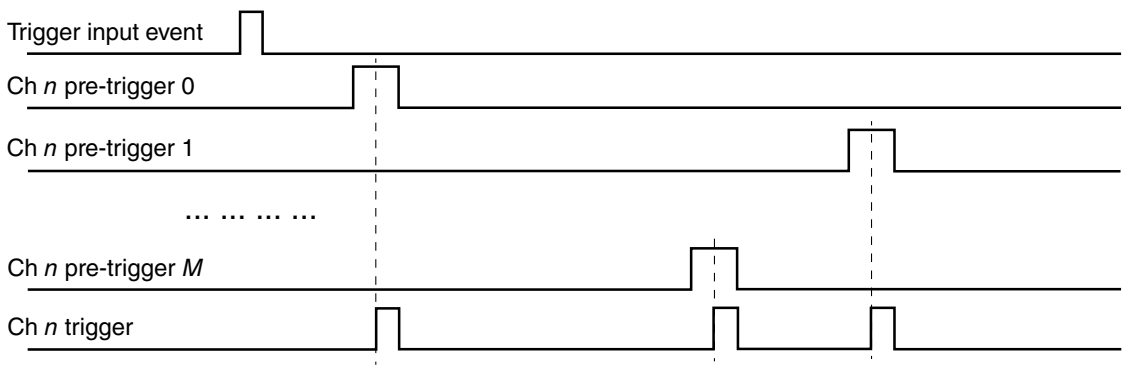


Figure 51-3. Pre-trigger and trigger outputs

The delay in CH*n*DLY*m* register can be optionally bypassed, if CH*n*C1[TOS[*m*]] is cleared. In this case, when the trigger input event occurs, the pre-trigger *m* is asserted after 2 peripheral clock cycles.

The PDB can be configured for back-to-back operation. Back-to-back operation enables the ADC conversion completions to trigger the next PDB channel pre-trigger and trigger outputs, so that the ADC conversions can be triggered on the next set of configuration and results registers. When back-to-back operation is enabled by setting CH*n*C1[BB[*m*]], then the delay *m* is ignored and the pre-trigger *m* is asserted 2 peripheral cycles after the acknowledgment *m* is received. The acknowledgment connections in this MCU are described in Back-to-back acknowledgment connections.

When a pre-trigger from a PDB channel *n* is asserted, the associated lock of the pre-trigger becomes active. The associated lock is released by the rising edge of the corresponding ADC*n*SC1[COCO]; the ADC*n*SC1[COCO] should be cleared after the conversion result is read, so that the next rising edge of ADC*n*SC1[COCO] can be generated to clear the lock later. The lock becomes inactive when:

- the rising edge of corresponding ADC*n*SC1[COCO] occurs,
- or the corresponding PDB pre-trigger is disabled,
- or the PDB is disabled

The channel *n* trigger output is suppressed when any of the locks of the pre-triggers in channel *n* is active. If a new pre-trigger *m* asserts when there is active lock in the PDB channel *n*, then a register flag bit CH*n*S[ERR[*m*]] (associated with the pre-trigger *m*) is set. If SC[PDBEIE] is set, then the sequence error interrupt is generated. A sequence error typically happens because the delay *m* is set too short and the pre-trigger *m* asserts before the previously triggered ADC conversion finishes.

When the PDB counter reaches the value set in IDLY register, the SC[PDBIF] flag is set. A PDB interrupt can be generated if SC[PDBIE] is set and SC[DMAEN] is cleared. If SC[DMAEN] is set, then the PDB requests a DMA transfer when the SC[PDBIF] flag is set.

The modulus value in the MOD register is used to reset the counter back to zero at the end of the count. If SC[CONT] is set, then the counter will then resume a new count; otherwise, the counter operation will stop until the next trigger input event occurs.

51.5.2 PDB trigger input source selection

The PDB has up to 15 trigger input sources, namely Trigger-In 0 to Trigger-In 14. They are connected to on-chip or off-chip event sources. The PDB can be triggered by software through SC[SWTRIG]. SC[TRIGSEL] selects the active trigger input source or software trigger.

For the trigger input sources implemented in this MCU, see chip configuration information.

51.5.3 DAC interval trigger outputs

PDB can generate the interval triggers for DACs to update their outputs periodically. DAC interval counter *x* is reset and started when a trigger input event occurs if DACINTC*x*[EXT] is cleared. When the interval counter *x* is equal to the value set in DACINT*x* register, the DAC interval trigger *x* output generates a pulse of one peripheral

clock cycle width to update the DAC*x*. If DACINTC*x*[EXT] is set, the DAC interval counter is bypassed and the interval trigger output *x* generates a pulse following the detection of a rising edge on the DAC external trigger input. The counter and interval trigger can be disabled by clearing the DACINTC*x*[TOE].

DAC interval counters are also reset when the PDB counter reaches the MOD register value; therefore, when the PDB counter rolls over to zero, the DAC interval counters starts anew.

The DAC interval trigger pulse and the ADC pre-trigger/trigger pulses together allow precise timing of DAC updates and ADC measurements. This is outlined in the typical use case described in the following diagram.

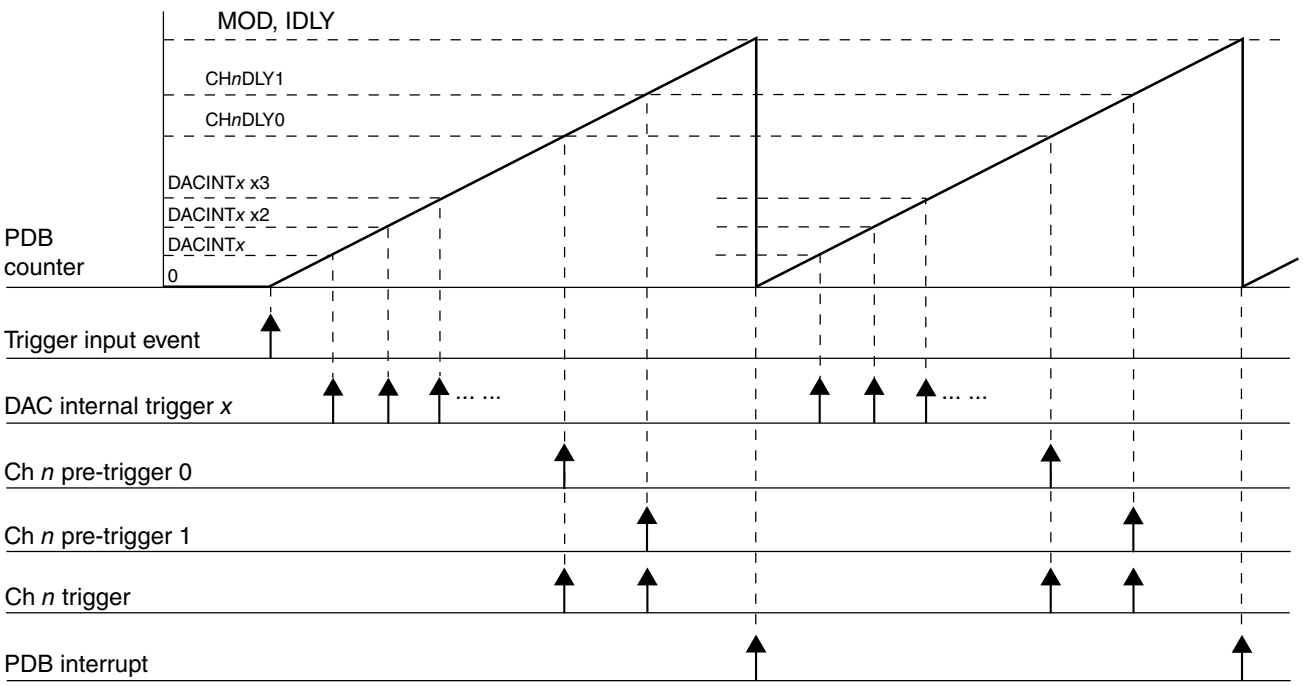


Figure 51-4. PDB ADC triggers and DAC interval triggers use case

NOTE

Because the DAC interval counters share the prescaler with PDB counter, PDB must be enabled if the DAC interval trigger outputs are used in the applications.

51.5.4 Pulse-Out's

PDB can generate pulse outputs of configurable width. When PDB counter reaches the value set in PO*y*DLY[DLY1], the Pulse-Out goes high; when the counter reaches PO*y*DLY[DLY2], it goes low. PO*y*DLY[DLY2] can be set either greater or less than PO*y*DLY[DLY1].

ADC pre-trigger/trigger outputs and Pulse-Out generation have the same time base, because they both share the PDB counter.

The pulse-out connections implemented in this MCU are described in the device's chip configuration details.

51.5.5 Updating the delay registers

The following registers control the timing of the PDB operation; and in some of the applications, they may need to become effective at the same time.

- PDB Modulus register (MOD)
- PDB Interrupt Delay register (IDLY)
- PDB Channel *n* Delay *m* register (CH*n*DLY*m*)
- DAC Interval *x* register (DACINT*x*)
- PDB Pulse-Out *y* Delay register (PO*y*DLY)

The internal registers of them are buffered and any values written to them are written first to their buffers. The circumstances that cause their internal registers to be updated with the values from the buffers are summarized as shown in the table below.

Table 51-5. Circumstances of update to the delay registers

SC[LDMOD]	Update to the delay registers
00	The internal registers are loaded with the values from their buffers immediately after 1 is written to SC[LDOK].
01	The PDB counter reaches the MOD register value after 1 is written to SC[LDOK].
10	A trigger input event is detected after 1 is written to SC[LDOK].
11	Either the PDB counter reaches the MOD register value, or a trigger input event is detected, after 1 is written to SC[LDOK].

After 1 is written to SC[LDOK], the buffers cannot be written until the values in buffers are loaded into their internal registers. SC[LDOK] is self-cleared when the internal registers are loaded, so the application code can read it to determine the updates to the internal registers.

The following diagrams show the cases of the internal registers being updated with SC[LDMOD] is 00 and x1.

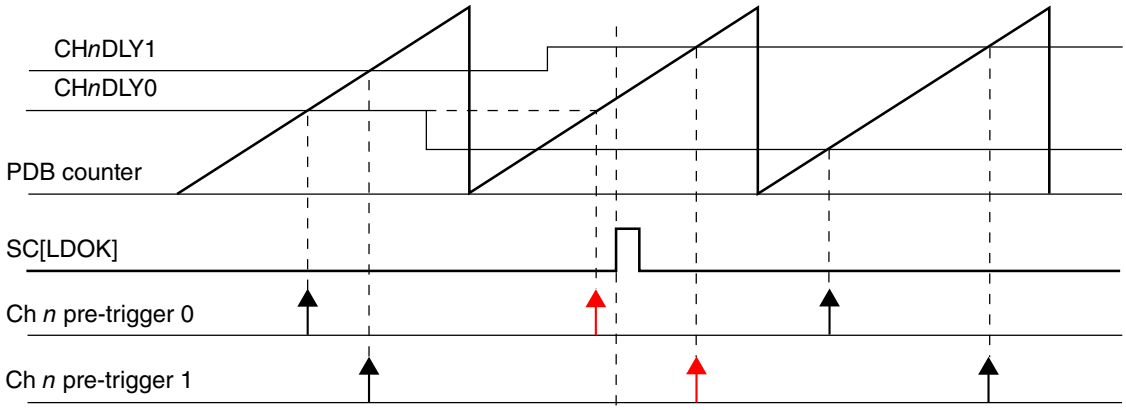


Figure 51-5. Registers update with SC[LDMOD] = 00

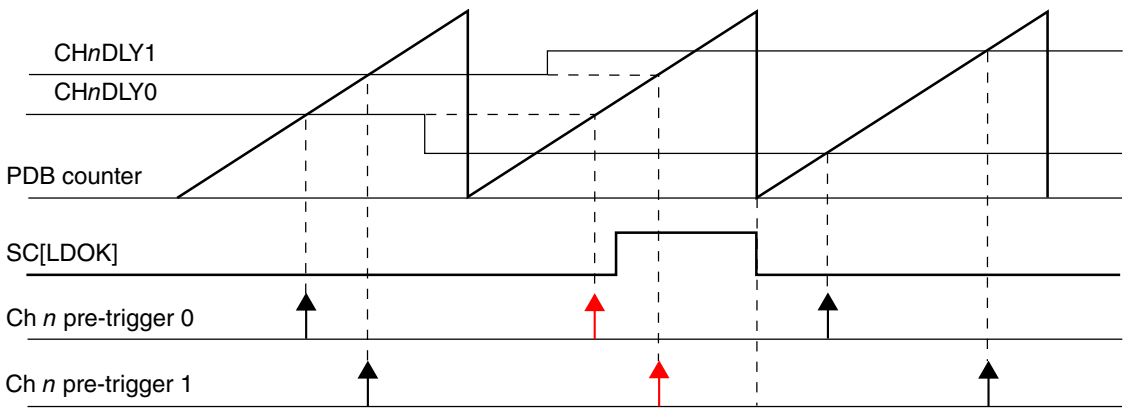


Figure 51-6. Registers update with SC[LDMOD] = x1

51.5.6 Interrupts

PDB can generate two interrupts: PDB interrupt and PDB sequence error interrupt. The following table summarizes the interrupts.

Table 51-6. PDB interrupt summary

Interrupt	Flags	Enable bit
PDB Interrupt	SC[PDBIF]	SC[PDBIE] = 1 and SC[DMAEN] = 0
PDB Sequence Error Interrupt	CH*n*S[ERR*m*]	SC[PDBEIE] = 1

51.5.7 DMA

If SC[DMAEN] is set, PDB can generate a DMA transfer request when SC[PDBIF] is set. When DMA is enabled, the PDB interrupt is not issued.

51.6 Application information

51.6.1 Impact of using the prescaler and multiplication factor on timing resolution

Use of prescaler and multiplication factor greater than 1 limits the count/delay accuracy in terms of peripheral clock cycles (to the modulus of the prescaler X multiplication factor). If the multiplication factor is set to 1 and the prescaler is set to 2 then the only values of total peripheral clocks that can be detected are even values; if prescaler is set to 4 then the only values of total peripheral clocks that can be decoded as detected are mod(4) and so forth. If the applications need a really long delay value and use a prescaler set to 128, then the resolution would be limited to 128 peripheral clock cycles.

Therefore, use the lowest possible prescaler and multiplication factor for a given application.

Chapter 52
Periodic Interrupt Timer (PIT)

52.1 Chip-specific PIT information

52.1.1 PIT Instantiations

This device contains one PIT module with four channels.

52.1.2 PIT/DMA Periodic Trigger Assignments

The PIT generates periodic trigger events to the DMA Mux as shown in the table below.

Table 52-1. PIT channel assignments for periodic DMA triggering

DMA Channel Number	PIT Channel
DMA Channel 0	PIT Channel 0
DMA Channel 1	PIT Channel 1
DMA Channel 2	PIT Channel 2
DMA Channel 3	PIT Channel 3

52.1.3 PIT/ADC Triggers

PIT triggers are selected as ADCx trigger sources using the SIM_SOPT7[ADCxTRGSEL] fields. For more details, refer to SIM chapter.

52.2 Introduction

The PIT module is an array of timers that can be used to raise interrupts and trigger DMA channels.

52.2.1 Block diagram

The following figure shows the block diagram of the PIT module.

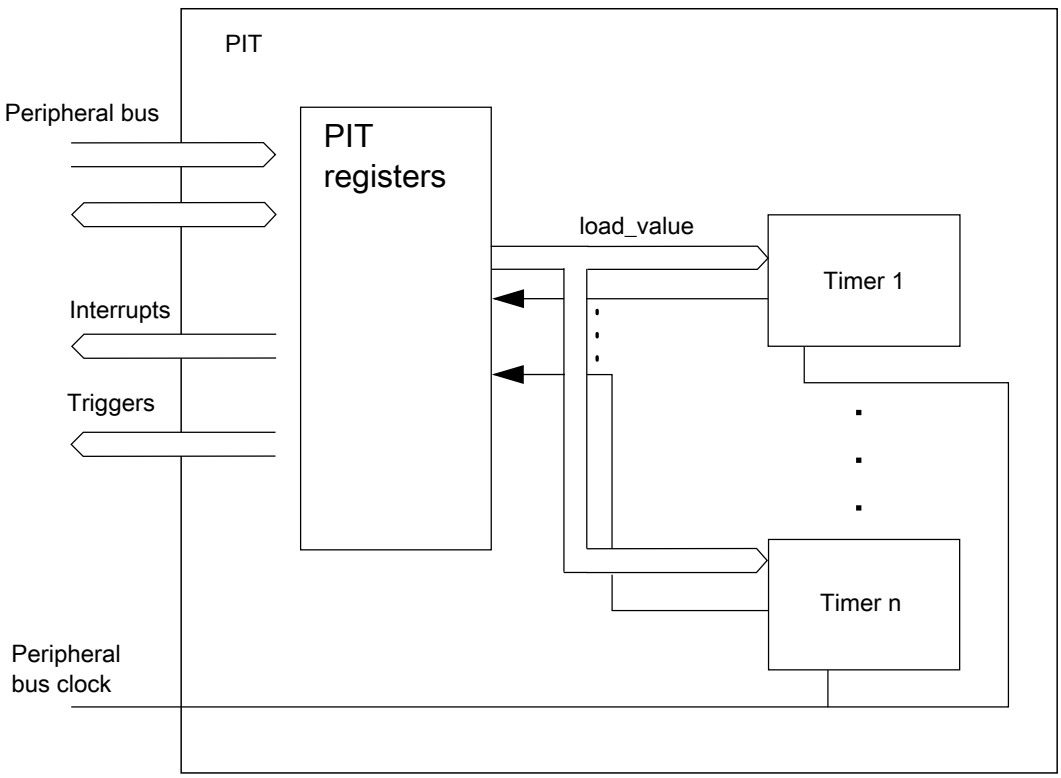


Figure 52-1. Block diagram of the PIT

NOTE

See the chip-specific PIT information for the number of PIT channels used in this MCU.

52.2.2 Features

The main features of this block are:

- Ability of timers to generate DMA trigger pulses

- Ability of timers to generate interrupts
- Maskable interrupts
- Independent timeout periods for each timer

52.3 Signal description

The PIT module has no external pins.

52.4 Memory map/register description

This section provides a detailed description of all registers accessible in the PIT module.

- Reserved registers will read as 0, writes will have no effect.
- See the chip-specific PIT information for the number of PIT channels used in this MCU.

PIT memory map

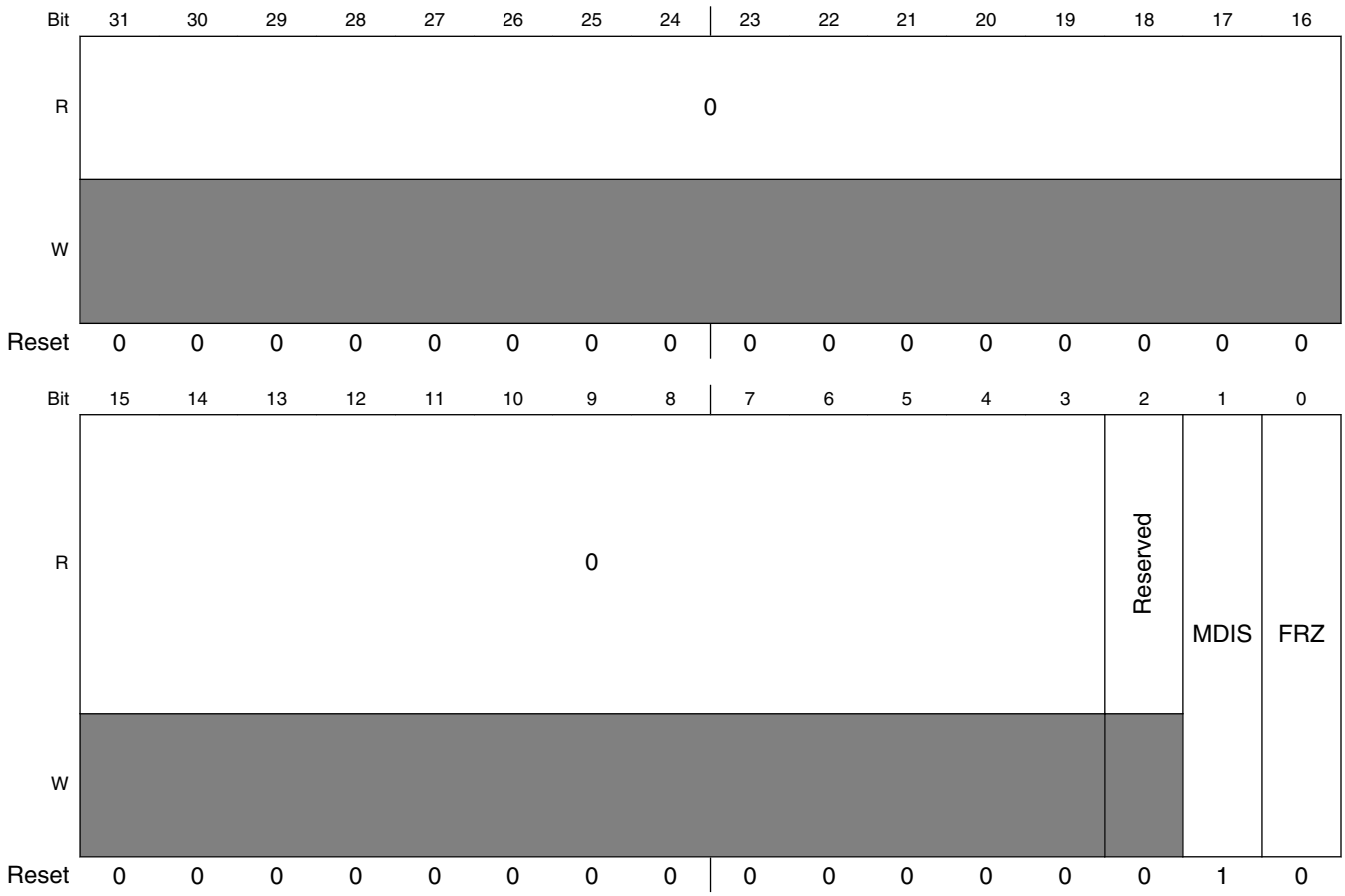
Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_7000	PIT Module Control Register (PIT0_MCR)	32	R/W	0000_0002h	52.4.1/1694
4003_70E0	PIT Upper Lifetime Timer Register (PIT0_LTMR64H)	32	R	0000_0000h	52.4.2/1695
4003_70E4	PIT Lower Lifetime Timer Register (PIT0_LTMR64L)	32	R	0000_0000h	52.4.3/1695
4003_7100	Timer Load Value Register (PIT0_LDVAL0)	32	R/W	0000_0000h	52.4.4/1696
4003_7104	Current Timer Value Register (PIT0_CVAL0)	32	R	0000_0000h	52.4.5/1696
4003_7108	Timer Control Register (PIT0_TCTRL0)	32	R/W	0000_0000h	52.4.6/1697
4003_710C	Timer Flag Register (PIT0_TFLG0)	32	R/W	0000_0000h	52.4.7/1698
4003_7110	Timer Load Value Register (PIT0_LDVAL1)	32	R/W	0000_0000h	52.4.4/1696
4003_7114	Current Timer Value Register (PIT0_CVAL1)	32	R	0000_0000h	52.4.5/1696
4003_7118	Timer Control Register (PIT0_TCTRL1)	32	R/W	0000_0000h	52.4.6/1697
4003_711C	Timer Flag Register (PIT0_TFLG1)	32	R/W	0000_0000h	52.4.7/1698
4003_7120	Timer Load Value Register (PIT0_LDVAL2)	32	R/W	0000_0000h	52.4.4/1696
4003_7124	Current Timer Value Register (PIT0_CVAL2)	32	R	0000_0000h	52.4.5/1696
4003_7128	Timer Control Register (PIT0_TCTRL2)	32	R/W	0000_0000h	52.4.6/1697
4003_712C	Timer Flag Register (PIT0_TFLG2)	32	R/W	0000_0000h	52.4.7/1698
4003_7130	Timer Load Value Register (PIT0_LDVAL3)	32	R/W	0000_0000h	52.4.4/1696
4003_7134	Current Timer Value Register (PIT0_CVAL3)	32	R	0000_0000h	52.4.5/1696
4003_7138	Timer Control Register (PIT0_TCTRL3)	32	R/W	0000_0000h	52.4.6/1697
4003_713C	Timer Flag Register (PIT0_TFLG3)	32	R/W	0000_0000h	52.4.7/1698

52.4.1 PIT Module Control Register (PITx_MCR)

This register enables or disables the PIT timer clocks and controls the timers when the PIT enters the Debug mode.

Access: User read/write

Address: 4003_7000h base + 0h offset = 4003_7000h



PITx_MCR field descriptions

Field	Description
31–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 Reserved	This field is reserved.
1 MDIS	Module Disable - (PIT section) Disables the standard timers. This field must be enabled before any other setup is done. 0 Clock for standard PIT timers is enabled. 1 Clock for standard PIT timers is disabled.

Table continues on the next page...

PITx_MCR field descriptions (continued)

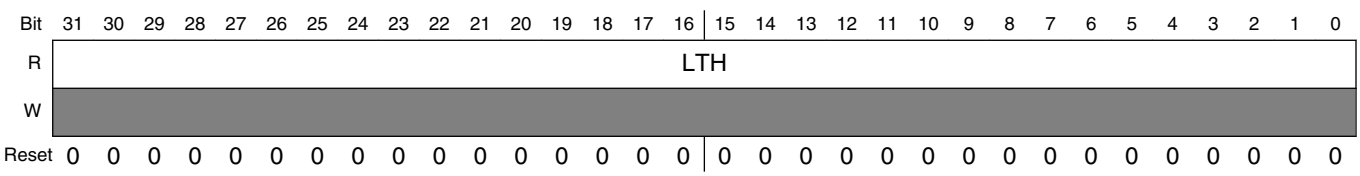
Field	Description
0 FRZ	Freeze Allows the timers to be stopped when the device enters the Debug mode. 0 Timers continue to run in Debug mode. 1 Timers are stopped in Debug mode.

52.4.2 PIT Upper Lifetime Timer Register (PITx_LTMR64H)

This register is intended for applications that chain timer 0 and timer 1 to build a 64-bit lifetimer.

Access: User read only

Address: 4003_7000h base + E0h offset = 4003_70E0h



PITx_LTMR64H field descriptions

Field	Description
LTH	Life Timer value Shows the timer value of timer 1. If this register is read at a time t1, LTMR64L shows the value of timer 0 at time t1.

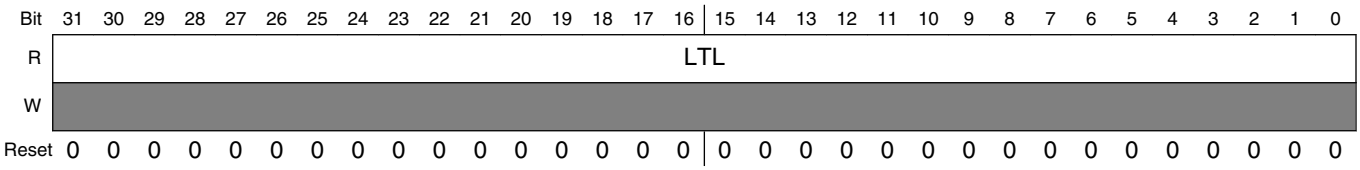
52.4.3 PIT Lower Lifetime Timer Register (PITx_LTMR64L)

This register is intended for applications that chain timer 0 and timer 1 to build a 64-bit lifetimer.

To use LTMR64H and LTMR64L, timer 0 and timer 1 need to be chained. To obtain the correct value, first read LTMR64H and then LTMR64L. LTMR64H will have the value of CVAL1 at the time of the first access, LTMR64L will have the value of CVAL0 at the time of the first access, therefore the application does not need to worry about carry-over effects of the running counter.

Access: User read only

Address: 4003_7000h base + E4h offset = 4003_70E4h



PITx_LTMR64L field descriptions

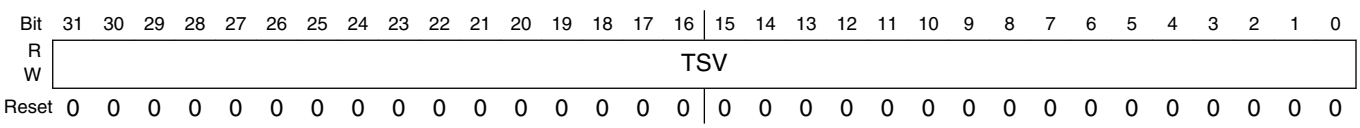
Field	Description
LTL	Life Timer value Shows the value of timer 0 at the time LTMR64H was last read. It will only update if LTMR64H is read.

52.4.4 Timer Load Value Register (PITx_LDVAL*n*)

These registers select the timeout period for the timer interrupts.

Access: User read/write

Address: 4003_7000h base + 100h offset + (16d × i), where i=0d to 3d



PITx_LDVAL*n* field descriptions

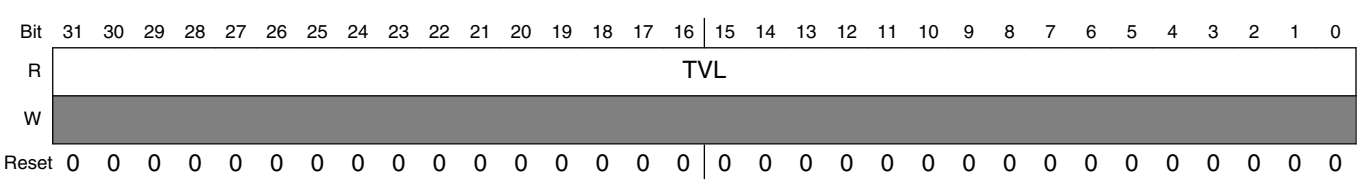
Field	Description
TSV	Timer Start Value Sets the timer start value. The timer will count down until it reaches 0, then it will generate an interrupt and load this register value again. Writing a new value to this register will not restart the timer; instead the value will be loaded after the timer expires. To abort the current cycle and start a timer period with the new value, the timer must be disabled and enabled again.

52.4.5 Current Timer Value Register (PITx_CVAL*n*)

These registers indicate the current timer position.

Access: User read only

Address: 4003_7000h base + 104h offset + (16d × i), where i=0d to 3d



PITx_CVAL*n* field descriptions

Field	Description
TVL	Current Timer Value Represents the current timer value, if the timer is enabled. **NOTE:** • If the timer is disabled, do not use this field as its value is unreliable. • The timer uses a downcounter. The timer values are frozen in Debug mode if MCR[FRZ] is set.

52.4.6 Timer Control Register (PITx_TCTRL*n*)

These registers contain the control bits for each timer.

Access: User read/write

Address: 4003_7000h base + 108h offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0													CHN	TIE	TEN
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PITx_TCTRL*n* field descriptions

Field	Description
31–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 CHN	Chain Mode When activated, Timer n-1 needs to expire before timer n can decrement by 1. Timer 0 cannot be chained. 0 Timer is not chained. 1 Timer is chained to previous timer. For example, for Channel 2, if this field is set, Timer 2 is chained to Timer 1.
1 TIE	Timer Interrupt Enable When an interrupt is pending, or, TFLGn[TIF] is set, enabling the interrupt will immediately cause an interrupt event. To avoid this, the associated TFLGn[TIF] must be cleared first. 0 Interrupt requests from Timer n are disabled. 1 Interrupt will be requested whenever TIF is set.
0 TEN	Timer Enable Enables or disables the timer.

Table continues on the next page...

PITx_TCTRL*n* field descriptions (continued)

Field	Description
	0 Timer n is disabled. 1 Timer n is enabled.

52.4.7 Timer Flag Register (PITx_TFLG*n*)

These registers hold the PIT interrupt flags.

Access: User read/write

Address: 4003_7000h base + 10Ch offset + (16d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															TIF
W																w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PITx_TFLG*n* field descriptions

Field	Description
31–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 TIF	Timer Interrupt Flag Sets to 1 at the end of the timer period. Writing 1 to this flag clears it. Writing 0 has no effect. If enabled, or, when TCTRLn[TIE] = 1, TIF causes an interrupt request. 0 Timeout has not yet occurred. 1 Timeout has occurred.

52.5 Functional description

This section provides the functional description of the module.

52.5.1 General operation

This section gives detailed information on the internal operation of the module. Each timer can be used to generate trigger pulses and interrupts. Each interrupt is available on a separate interrupt line.

52.5.1.1 Timers

The timers generate triggers at periodic intervals, when enabled. The timers load the start values as specified in their LDVAL registers, count down to 0 and then load the respective start value again. Each time a timer reaches 0, it will generate a trigger pulse and set the interrupt flag.

All interrupts can be enabled or masked by setting TCTRLn[TIE]. A new interrupt can be generated only after the previous one is cleared.

If desired, the current counter value of the timer can be read via the CVAL registers.

The counter period can be restarted, by first disabling, and then enabling the timer with TCTRLn[TEN]. See the following figure.

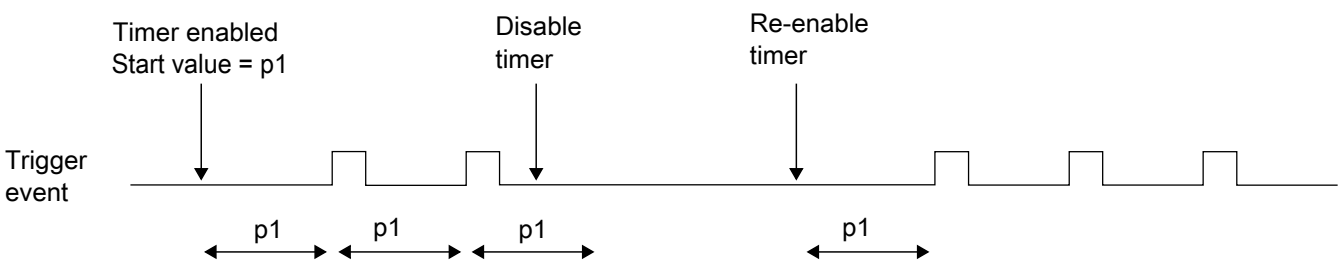


Figure 52-2. Stopping and starting a timer

The counter period of a running timer can be modified, by first disabling the timer, setting a new load value, and then enabling the timer again. See the following figure.

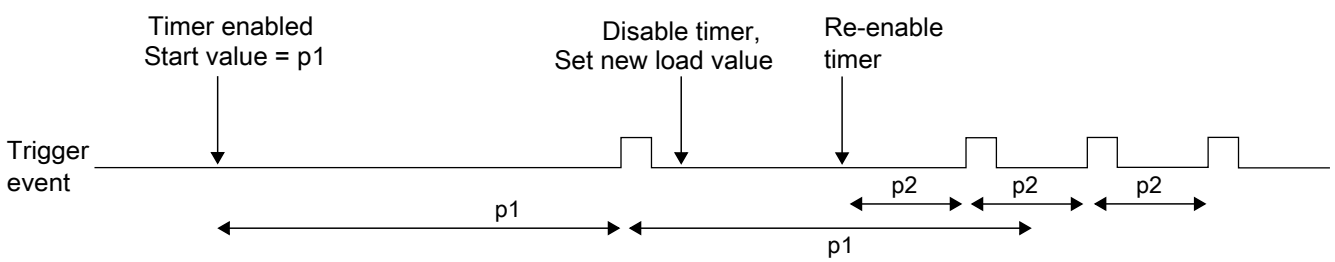


Figure 52-3. Modifying running timer period

It is also possible to change the counter period without restarting the timer by writing LDVAL with the new load value. This value will then be loaded after the next trigger event. See the following figure.

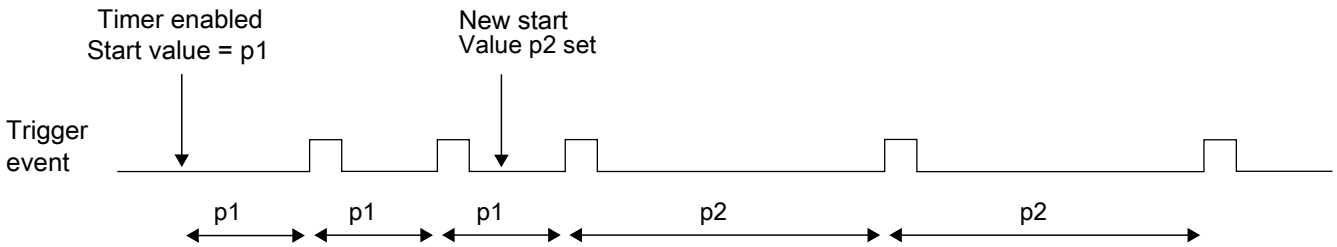


Figure 52-4. Dynamically setting a new load value

52.5.1.2 Debug mode

In Debug mode, the timers will be frozen based on MCR[FRZ]. This is intended to aid software development, allowing the developer to halt the processor, investigate the current state of the system, for example, the timer values, and then continue the operation.

52.5.2 Interrupts

All the timers support interrupt generation. See the MCU specification for related vector addresses and priorities.

Timer interrupts can be enabled by setting TCTRLn[TIE]. TFLGn[TIF] are set to 1 when a timeout occurs on the associated timer, and are cleared to 0 by writing a 1 to the corresponding TFLGn[TIF].

52.5.3 Chained timers

When a timer has chain mode enabled, it will only count after the previous timer has expired. So if timer n-1 has counted down to 0, counter n will decrement the value by one. This allows to chain some of the timers together to form a longer timer. The first timer (timer 0) cannot be chained to any other timer.

52.6 Initialization and application information

In the example configuration:

- The PIT clock has a frequency of 50 MHz.

- Timer 1 creates an interrupt every 5.12 ms.
- Timer 3 creates a trigger event every 30 ms.

The PIT module must be activated by writing a 0 to MCR[MDIS].

The 50 MHz clock frequency equates to a clock period of 20 ns. Timer 1 needs to trigger every 5.12 ms/20 ns = 256,000 cycles and Timer 3 every 30 ms/20 ns = 1,500,000 cycles. The value for the LDVAL register trigger is calculated as:

LDVAL trigger = (period / clock period) -1

This means LDVAL1 and LDVAL3 must be written with 0x0003E7FF and 0x0016E35F respectively.

The interrupt for Timer 1 is enabled by setting TCTRL1[TIE]. The timer is started by writing 1 to TCTRL1[TEN].

Timer 3 shall be used only for triggering. Therefore, Timer 3 is started by writing a 1 to TCTRL3[TEN]. TCTRL3[TIE] stays at 0.

The following example code matches the described setup:

```
// turn on PIT
PIT_MCR = 0x00;


// Timer 1
PIT_LDVAL1 = 0x0003E7FF; // setup timer 1 for 256000 cycles
PIT_TCTRL1 = TIE; // enable Timer 1 interrupts
PIT_TCTRL1 |= TEN; // start Timer 1


// Timer 3
PIT_LDVAL3 = 0x0016E35F; // setup timer 3 for 1500000 cycles
PIT_TCTRL3 |= TEN; // start Timer 3
```

52.7 Example configuration for chained timers

In the example configuration:

- The PIT clock has a frequency of 100 MHz.
- Timers 1 and 2 are available.
- An interrupt shall be raised every 1 minute.

The PIT module needs to be activated by writing a 0 to MCR[MDIS].

The 100 MHz clock frequency equates to a clock period of 10 ns, so the PIT needs to count for 6000 million cycles, which is more than a single timer can do. So, Timer 1 is set up to trigger every 6 s (600 million cycles). Timer 2 is chained to Timer 1 and programmed to trigger 10 times.

The value for the LDVAL register trigger is calculated as number of cycles-1, so LDVAL1 receives the value 0x23C345FF and LDVAL2 receives the value 0x00000009.

The interrupt for Timer 2 is enabled by setting TCTRL2[TIE], the Chain mode is activated by setting TCTRL2[CHN], and the timer is started by writing a 1 to TCTRL2[TEN]. TCTRL1[TEN] needs to be set, and TCTRL1[CHN] and TCTRL1[TIE] are cleared.

The following example code matches the described setup:

```
// turn on PIT
PIT_MCR = 0x00;


// Timer 2
PIT_LDVAL2 = 0x00000009; // setup Timer 2 for 10 counts
PIT_TCTRL2 = TIE; // enable Timer 2 interrupt
PIT_TCTRL2 |= CHN; // chain Timer 2 to Timer 1
PIT_TCTRL2 |= TEN; // start Timer 2


// Timer 1
PIT_LDVAL1 = 0x23C345FF; // setup Timer 1 for 600 000 000 cycles
PIT_TCTRL1 = TEN; // start Timer 1
```

52.8 Example configuration for the lifetime timer

To configure the lifetimer timer, channels 0 and 1 need to be chained together.

First the PIT module needs to be activated by writing a 0 to the MDIS bit in the CTRL register, then the LDVAL registers need to be set to the maximum value.

The timer is a downcounter.

The following example code matches the described setup:

```
// turn on PIT
PIT_MCR = 0x00;


// Timer 1
PIT_LDVAL1 = 0xFFFFFFFF; // setup timer 1 for maximum counting period
PIT_TCTRL1 = 0x0; // disable timer 1 interrupts
PIT_TCTRL1 |= CHN; // chain timer 1 to timer 0
PIT_TCTRL1 |= TEN; // start timer 1


// Timer 0
```

```
PIT_LDVAL0 = 0xFFFFFFFF; // setup timer 0 for maximum counting period
PIT_TCTRL0 = TEN; // start timer 0
```

To access the lifetime, read first LTMR64H and then LTMR64L.

```
current_uptime = PIT_LTMR64H<<32;
current_uptime = current_uptime + PIT_LTMR64L;
```

Chapter 53
Real Time Clock (RTC)

53.1 Chip-specific RTC information

53.1.1 RTC_CLKOUT signal

When the RTC is enabled and the port control module selects the RTC_CLKOUT function, the RTC_CLKOUT signal outputs a 1 Hz or 32 kHz output derived from RTC oscillator as shown below.

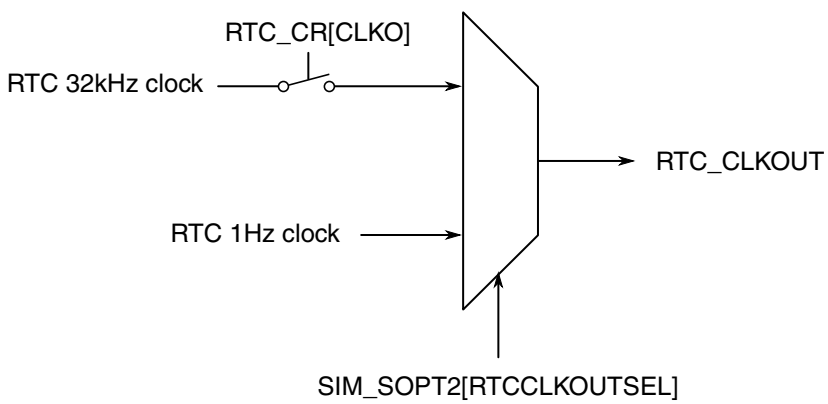


Figure 53-1. RTC_CLKOUT generation

NOTE

It is possible on variants of this device with RTC_WAKEUP pin to output the RTC clock signal to the RTC_WAKEUP pin. Please refer to the RTC Control Register for details.

53.2 Introduction

53.2.1 Features

The RTC module features include:

- Independent power supply, POR, and 32 kHz crystal oscillator
- 32-bit seconds counter with roll-over protection and 32-bit alarm
- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register write protection
  - Lock register requires VBAT POR or software reset to enable write access
  - Access control registers require system reset to enable read and/or write access
- 1 Hz square wave output with optional interrupt

53.2.2 Modes of operation

The RTC remains functional in all low power modes and can generate an interrupt to exit any low power mode. It operates in one of two modes of operation: chip power-up and chip power-down.

During chip power-down, RTC is powered from the backup power supply (VBAT) and is electrically isolated from the rest of the chip but continues to increment the time counter (if enabled) and retain the state of the RTC registers. The RTC registers are not accessible.

During chip power-up, RTC remains powered from the backup power supply (VBAT). All RTC registers are accessible by software and all functions are operational. If enabled, the 32.768 kHz clock can be supplied to the rest of the chip.

53.2.3 RTC signal descriptions

Table 53-1. RTC signal descriptions

Signal	Description	I/O
EXTAL32	32.768 kHz oscillator input	I
XTAL32	32.768 kHz oscillator output	O
RTC_CLKOUT	1 Hz square-wave output or OSCERCLK	O
$\overline{\text{RTC_WAKEUP}}$	Wakeup for external device	O

53.2.3.1 RTC clock output

The clock to the seconds counter is available on the RTC_CLKOUT signal. It is a 1 Hz square wave output. See RTC_CLKOUT options for details.

53.2.3.2 RTC wakeup pin

The RTC wakeup pin is an open drain, active low, output that allows the RTC to wakeup the chip via an external component. The wakeup pin asserts when the wakeup pin enable is set and either the RTC interrupt is asserted or the wakeup pin is turned on via a register bit. The wakeup pin does not assert from the RTC seconds interrupt.

NOTE

The wakeup pin is optional and may not be implemented on all devices.

53.3 Register definition

All registers must be accessed using 32-bit writes and all register accesses incur three wait states.

Write accesses to any register by non-supervisor mode software, when the supervisor access bit in the control register is clear, will terminate with a bus error.

Read accesses by non-supervisor mode software complete as normal.

Writing to a register protected by the write access register or lock register does not generate a bus error, but the write will not complete.

Reading a register protected by the read access register does not generate a bus error, but the register will read zero.

RTC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_D000	RTC Time Seconds Register (RTC_TSR)	32	R/W	0000_0000h	53.3.1/1708
4003_D004	RTC Time Prescaler Register (RTC_TPR)	32	R/W	0000_0000h	53.3.2/1708
4003_D008	RTC Time Alarm Register (RTC_TAR)	32	R/W	0000_0000h	53.3.3/1709
4003_D00C	RTC Time Compensation Register (RTC_TCR)	32	R/W	0000_0000h	53.3.4/1709

Table continues on the next page...

RTC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_D010	RTC Control Register (RTC_CR)	32	R/W	0000_0000h	53.3.5/1711
4003_D014	RTC Status Register (RTC_SR)	32	R/W	0000_0001h	53.3.6/1713
4003_D018	RTC Lock Register (RTC_LR)	32	R/W	0000_00FFh	53.3.7/1714
4003_D01C	RTC Interrupt Enable Register (RTC_IER)	32	R/W	0000_0007h	53.3.8/1715
4003_D800	RTC Write Access Register (RTC_WAR)	32	R/W	0000_00FFh	53.3.9/1716
4003_D804	RTC Read Access Register (RTC_RAR)	32	R/W	0000_00FFh	53.3.10/ 1717

53.3.1 RTC Time Seconds Register (RTC_TSR)

Address: 4003_D000h base + 0h offset = 4003_D000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	TSR																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTC_TSR field descriptions

Field	Description
TSR	Time Seconds Register When the time counter is enabled, the TSR is read only and increments once a second provided SR[TOF] or SR[TIF] are not set. The time counter will read as zero when SR[TOF] or SR[TIF] are set. When the time counter is disabled, the TSR can be read or written. Writing to the TSR when the time counter is disabled will clear the SR[TOF] and/or the SR[TIF]. Writing to TSR with zero is supported, but not recommended because TSR will read as zero when SR[TIF] or SR[TOF] are set (indicating the time is invalid).

53.3.2 RTC Time Prescaler Register (RTC_TPR)

Address: 4003_D000h base + 4h offset = 4003_D004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																TPR															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTC_TPR field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

RTC_TPR field descriptions (continued)

Field	Description
TPR	Time Prescaler Register When the time counter is enabled, the TPR is read only and increments every 32.768 kHz clock cycle. The time counter will read as zero when SR[TOF] or SR[TIF] are set. When the time counter is disabled, the TPR can be read or written. The TSR[TSR] increments when bit 14 of the TPR transitions from a logic one to a logic zero.

53.3.3 RTC Time Alarm Register (RTC_TAR)

Address: 4003_D000h base + 8h offset = 4003_D008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	TAR																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTC_TAR field descriptions

Field	Description
TAR	Time Alarm Register When the time counter is enabled, the SR[TAF] is set whenever the TAR[TAR] equals the TSR[TSR] and the TSR[TSR] increments. Writing to the TAR clears the SR[TAF].

53.3.4 RTC Time Compensation Register (RTC_TCR)

Address: 4003_D000h base + Ch offset = 4003_D00Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CIC								TCV								CIR								TCR							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTC_TCR field descriptions

Field	Description
31–24 CIC	Compensation Interval Counter Current value of the compensation interval counter. If the compensation interval counter equals zero then it is loaded with the contents of the CIR. If the CIC does not equal zero then it is decremented once a second.
23–16 TCV	Time Compensation Value Current value used by the compensation logic for the present second interval. Updated once a second if the CIC equals 0 with the contents of the TCR field. If the CIC does not equal zero then it is loaded with zero (compensation is not enabled for that second increment).

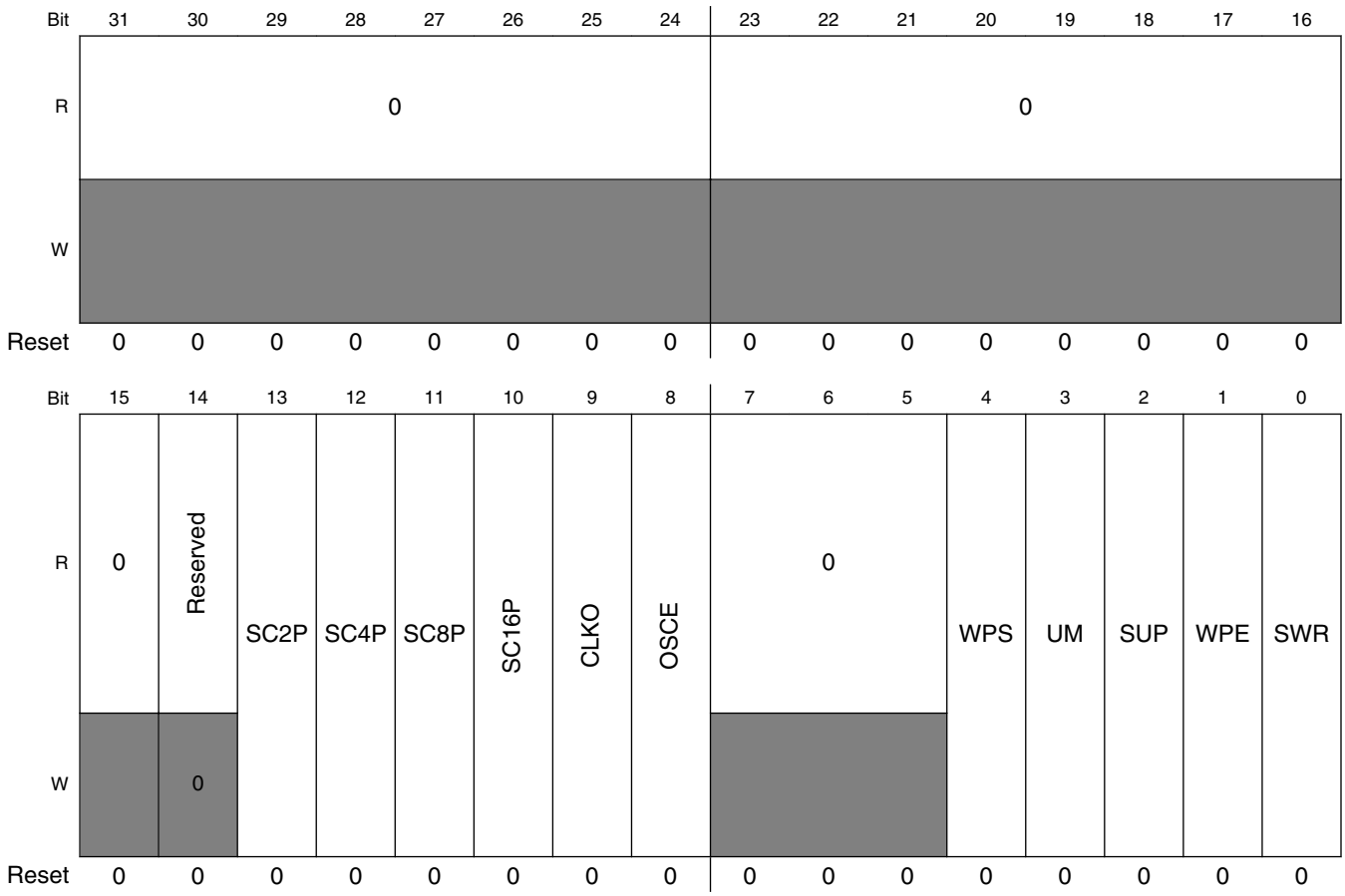
Table continues on the next page...

RTC_TCR field descriptions (continued)

Field	Description
15–8 CIR	Compensation Interval Register Configures the compensation interval in seconds from 1 to 256 to control how frequently the TCR should adjust the number of 32.768 kHz cycles in each second. The value written should be one less than the number of seconds. For example, write zero to configure for a compensation interval of one second. This register is double buffered and writes do not take affect until the end of the current compensation interval.
TCR	Time Compensation Register Configures the number of 32.768 kHz clock cycles in each second. This register is double buffered and writes do not take affect until the end of the current compensation interval. 80h Time Prescaler Register overflows every 32896 clock cycles. ... ... FFh Time Prescaler Register overflows every 32769 clock cycles. 00h Time Prescaler Register overflows every 32768 clock cycles. 01h Time Prescaler Register overflows every 32767 clock cycles. .... 7Fh Time Prescaler Register overflows every 32641 clock cycles.

53.3.5 RTC Control Register (RTC_CR)

Address: 4003_D000h base + 10h offset = 4003_D010h



RTC_CR field descriptions

Field	Description
31–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23–15 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
14 Reserved	This field is reserved. It must always be written to 0.
13 SC2P	Oscillator 2pF Load Configure 0 Disable the load. 1 Enable the additional load.
12 SC4P	Oscillator 4pF Load Configure 0 Disable the load. 1 Enable the additional load.

Table continues on the next page...

RTC_CR field descriptions (continued)

Field	Description
11 SC8P	Oscillator 8pF Load Configure 0 Disable the load. 1 Enable the additional load.
10 SC16P	Oscillator 16pF Load Configure 0 Disable the load. 1 Enable the additional load.
9 CLKO	Clock Output 0 The 32 kHz clock is output to other peripherals. 1 The 32 kHz clock is not output to other peripherals.
8 OSCE	Oscillator Enable 0 32.768 kHz oscillator is disabled. 1 32.768 kHz oscillator is enabled. After setting this bit, wait the oscillator startup time before enabling the time counter to allow the 32.768 kHz clock time to stabilize.
7–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 WPS	Wakeup Pin Select The wakeup pin is optional and not available on all devices. 0 Wakeup pin asserts (active low, open drain) if the RTC interrupt asserts or the wakeup pin is turned on. 1 Wakeup pin instead outputs the RTC 32kHz clock, provided the wakeup pin is turned on and the 32kHz clock is output to other peripherals.
3 UM	Update Mode Allows SR[TCE] to be written even when the Status Register is locked. When set, the SR[TCE] can always be written if the SR[TIF] or SR[TOF] are set or if the SR[TCE] is clear. 0 Registers cannot be written when locked. 1 Registers can be written when locked under limited conditions.
2 SUP	Supervisor Access 0 Non-supervisor mode write accesses are not supported and generate a bus error. 1 Non-supervisor mode write accesses are supported.
1 WPE	Wakeup Pin Enable The wakeup pin is optional and not available on all devices. 0 Wakeup pin is disabled. 1 Wakeup pin is enabled and wakeup pin asserts if the RTC interrupt asserts or the wakeup pin is turned on.
0 SWR	Software Reset 0 No effect. 1 Resets all RTC registers except for the SWR bit and the RTC_WAR and RTC_RAR registers . The SWR bit is cleared by VBAT POR and by software explicitly clearing it.

53.3.6 RTC Status Register (RTC_SR)

Address: 4003_D000h base + 14h offset = 4003_D014h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

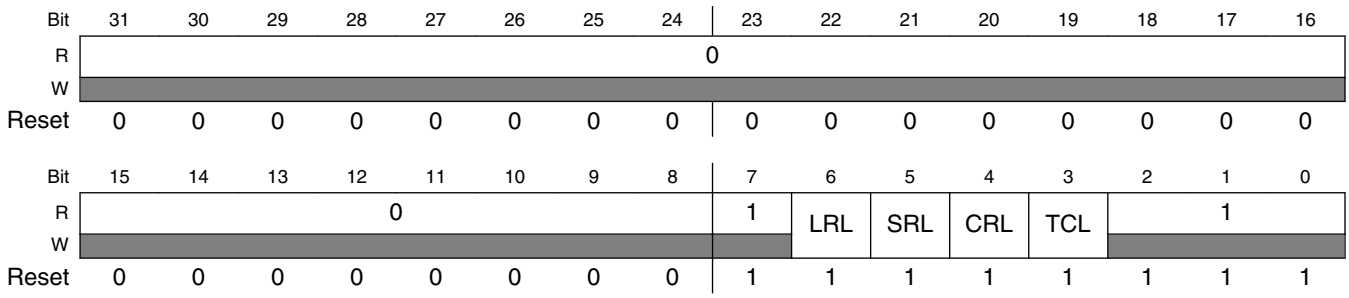
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0											TCE	0	TAF	TOF	TIF
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

RTC_SR field descriptions

Field	Description
31–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 TCE	Time Counter Enable When time counter is disabled the TSR register and TPR register are writeable, but do not increment. When time counter is enabled the TSR register and TPR register are not writeable, but increment. 0 Time counter is disabled. 1 Time counter is enabled.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 TAF	Time Alarm Flag Time alarm flag is set when the TAR[TAR] equals the TSR[TSR] and the TSR[TSR] increments. This bit is cleared by writing the TAR register. 0 Time alarm has not occurred. 1 Time alarm has occurred.
1 TOF	Time Overflow Flag Time overflow flag is set when the time counter is enabled and overflows. The TSR and TPR do not increment and read as zero when this bit is set. This bit is cleared by writing the TSR register when the time counter is disabled. 0 Time overflow has not occurred. 1 Time overflow has occurred and time counter is read as zero.
0 TIF	Time Invalid Flag The time invalid flag is set on VBAT POR or software reset. The TSR and TPR do not increment and read as zero when this bit is set. This bit is cleared by writing the TSR register when the time counter is disabled. 0 Time is valid. 1 Time is invalid and time counter is read as zero.

53.3.7 RTC Lock Register (RTC_LR)

Address: 4003_D000h base + 18h offset = 4003_D018h

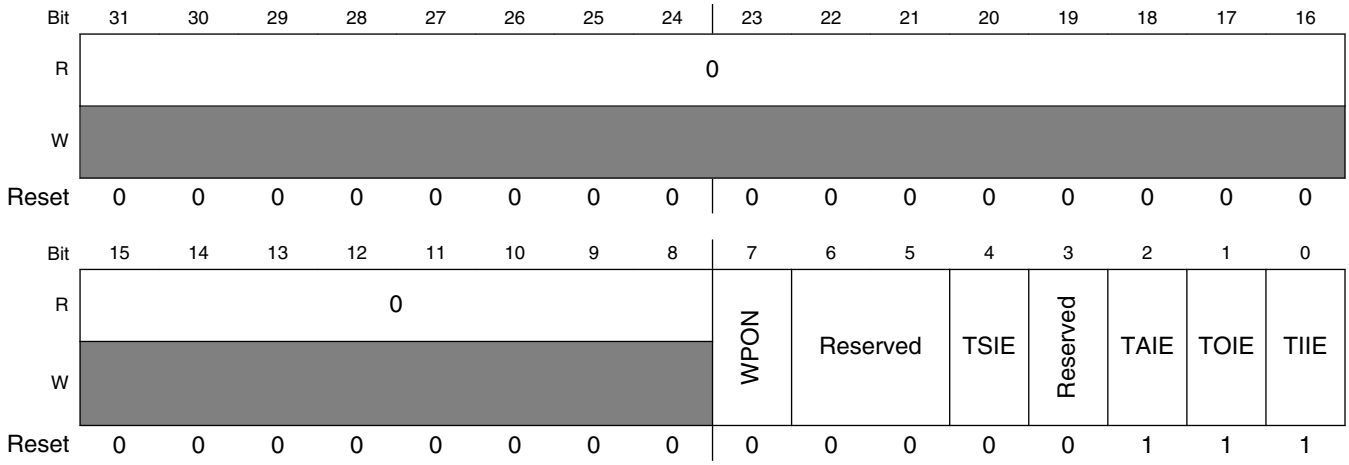


RTC_LR field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
6 LRL	Lock Register Lock After being cleared, this bit can be set only by VBAT POR or software reset. 0 Lock Register is locked and writes are ignored. 1 Lock Register is not locked and writes complete as normal.
5 SRL	Status Register Lock After being cleared, this bit can be set only by VBAT POR or software reset. 0 Status Register is locked and writes are ignored. 1 Status Register is not locked and writes complete as normal.
4 CRL	Control Register Lock After being cleared, this bit can only be set by VBAT POR. 0 Control Register is locked and writes are ignored. 1 Control Register is not locked and writes complete as normal.
3 TCL	Time Compensation Lock After being cleared, this bit can be set only by VBAT POR or software reset. 0 Time Compensation Register is locked and writes are ignored. 1 Time Compensation Register is not locked and writes complete as normal.
Reserved	This field is reserved. This read-only field is reserved and always has the value 1.

53.3.8 RTC Interrupt Enable Register (RTC_IER)

Address: 4003_D000h base + 1Ch offset = 4003_D01Ch



RTC_IER field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 WPON	Wakeup Pin On The wakeup pin is optional and not available on all devices. Whenever the wakeup pin is enabled and this bit is set, the wakeup pin will assert. 0 No effect. 1 If the wakeup pin is enabled, then the wakeup pin will assert.
6–5 Reserved	This field is reserved.
4 TSIE	Time Seconds Interrupt Enable The seconds interrupt is an edge-sensitive interrupt with a dedicated interrupt vector. It is generated once a second and requires no software overhead (there is no corresponding status flag to clear). 0 Seconds interrupt is disabled. 1 Seconds interrupt is enabled.
3 Reserved	This field is reserved.
2 TAIE	Time Alarm Interrupt Enable 0 Time alarm flag does not generate an interrupt. 1 Time alarm flag does generate an interrupt.
1 TOIE	Time Overflow Interrupt Enable

Table continues on the next page...

RTC_IER field descriptions (continued)

Field	Description
	0 Time overflow flag does not generate an interrupt. 1 Time overflow flag does generate an interrupt.
0 TIIE	Time Invalid Interrupt Enable 0 Time invalid flag does not generate an interrupt. 1 Time invalid flag does generate an interrupt.

53.3.9 RTC Write Access Register (RTC_WAR)

Address: 4003_D000h base + 800h offset = 4003_D800h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								IERW	LRW	SRW	CRW	TCRW	TARW	TPRW	TSRW
W																
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

RTC_WAR field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 IERW	Interrupt Enable Register Write After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Writes to the Interupt Enable Register are ignored. 1 Writes to the Interrupt Enable Register complete as normal.
6 LRW	Lock Register Write After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Writes to the Lock Register are ignored. 1 Writes to the Lock Register complete as normal.
5 SRW	Status Register Write After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset.

Table continues on the next page...

RTC_WAR field descriptions (continued)

Field	Description
	0 Writes to the Status Register are ignored. 1 Writes to the Status Register complete as normal.
4 CRW	Control Register Write After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Writes to the Control Register are ignored. 1 Writes to the Control Register complete as normal.
3 TCRW	Time Compensation Register Write After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Writes to the Time Compensation Register are ignored. 1 Writes to the Time Compensation Register complete as normal.
2 TARW	Time Alarm Register Write After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Writes to the Time Alarm Register are ignored. 1 Writes to the Time Alarm Register complete as normal.
1 TPRW	Time Prescaler Register Write After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Writes to the Time Prescaler Register are ignored. 1 Writes to the Time Prescaler Register complete as normal.
0 TSRW	Time Seconds Register Write After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Writes to the Time Seconds Register are ignored. 1 Writes to the Time Seconds Register complete as normal.

53.3.10 RTC Read Access Register (RTC_RAR)

Address: 4003_D000h base + 804h offset = 4003_D804h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								IERR	LRR	SRR	CRR	TCRR	TARR	TPRR	TSRR
W																
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

RTC_RAR field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 IERR	Interrupt Enable Register Read After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Reads to the Interrupt Enable Register are ignored. 1 Reads to the Interrupt Enable Register complete as normal.
6 LRR	Lock Register Read After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Reads to the Lock Register are ignored. 1 Reads to the Lock Register complete as normal.
5 SRR	Status Register Read After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Reads to the Status Register are ignored. 1 Reads to the Status Register complete as normal.
4 CRR	Control Register Read After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Reads to the Control Register are ignored. 1 Reads to the Control Register complete as normal.
3 TCRR	Time Compensation Register Read After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Reads to the Time Compensation Register are ignored. 1 Reads to the Time Compensation Register complete as normal.
2 TARR	Time Alarm Register Read After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Reads to the Time Alarm Register are ignored. 1 Reads to the Time Alarm Register complete as normal.
1 TPRR	Time Prescaler Register Read After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Reads to the Time Pprescaler Register are ignored. 1 Reads to the Time Prescaler Register complete as normal.
0 TSRR	Time Seconds Register Read After being cleared, this bit is set only by system reset. It is not affected by VBAT POR or software reset. 0 Reads to the Time Seconds Register are ignored. 1 Reads to the Time Seconds Register complete as normal.

53.4 Functional description

53.4.1 Power, clocking, and reset

The RTC is an always powered block that remains active in all low power modes and is powered by the battery power supply (VBAT). The battery power supply ensures that the RTC registers retain their state during chip power-down and that the RTC time counter remains operational.

The time counter within the RTC is clocked by a 32.768 kHz clock and can supply this clock to other peripherals. The 32.768 kHz clock can only be sourced from an external crystal using the oscillator that is part of the RTC module.

The RTC includes its own analog POR block, which generates a VBAT power-on-reset signal whenever the RTC module is powered up and initializes all RTC registers to their default state. A software reset bit can also initialize all RTC registers. The RTC also monitors the chip power supply and electrically isolates itself when the rest of the chip is powered down.

NOTE

An attempt to access an RTC register, except the access control registers, results in a bus error when:

- VBAT is powered down,
- the RTC is electrically isolated, or
- VBAT POR is asserted.

53.4.1.1 Oscillator control

The 32.768 kHz crystal oscillator is disabled at VBAT POR and must be enabled by software. After enabling the cystal oscillator, wait the oscillator startup time before setting SR[TCE] or using the oscillator clock external to the RTC.

The crystal oscillator includes tunable capacitors that can be configured by software. Do not change the capacitance unless the oscillator is disabled.

53.4.1.2 Software reset

Writing 1 to CR[SWR] forces the equivalent of a VBAT POR to the rest of the RTC module. CR[SWR] is not affected by the software reset and must be cleared by software. The access control registers are not affected by either VBAT POR or the software reset; they are reset by the chip reset.

53.4.1.3 Supervisor access

When the supervisor access control bit is clear, only supervisor mode software can write to the RTC registers, non-supervisor mode software will generate a bus error. Both supervisor and non-supervisor mode software can always read the RTC registers.

53.4.2 Time counter

The time counter consists of a 32-bit seconds counter that increments once every second and a 16-bit prescaler register that increments once every 32.768 kHz clock cycle.

Reading the time counter (either seconds or prescaler) while it is incrementing may return invalid data due to synchronization of the read data bus. If it is necessary for software to read the prescaler or seconds counter when they could be incrementing, it is recommended that two read accesses are performed and that software verifies that the same data was returned for both reads.

The time seconds register and time prescaler register can be written only when SR[TCE] is clear. Always write to the prescaler register before writing to the seconds register, because the seconds register increments on the falling edge of bit 14 of the prescaler register.

The time prescaler register increments provided SR[TCE] is set, SR[TIF] is clear, SR[TOF] is clear, and the 32.768 kHz clock source is present. After enabling the oscillator, wait the oscillator startup time before setting SR[TCE] to allow time for the oscillator clock output to stabilize.

If the time seconds register overflows then the SR[TOF] will set and the time prescaler register will stop incrementing. Clear SR[TOF] by initializing the time seconds register. The time seconds register and time prescaler register read as zero whenever SR[TOF] is set.

SR[TIF] is set on VBAT POR and software reset and is cleared by initializing the time seconds register. The time seconds register and time prescaler register read as zero whenever SR[TIF] is set.

53.4.3 Compensation

The compensation logic provides an accurate and wide compensation range and can correct errors as high as 3906 ppm and as low as 0.12 ppm. The compensation factor must be calculated externally to the RTC and supplied by software to the compensation register. The RTC itself does not calculate the amount of compensation that is required, although the 1 Hz clock is output to an external pin in support of external calibration logic.

Crystal compensation can be supported by using firmware and crystal characteristics to determine the compensation amount. Temperature compensation can be supported by firmware that periodically measures the external temperature via ADC and updates the compensation register based on a look-up table that specifies the change in crystal frequency over temperature.

The compensation logic alters the number of 32.768 kHz clock cycles it takes for the prescaler register to overflow and increment the time seconds counter. The time compensation value is used to adjust the number of clock cycles between -127 and +128. Cycles are added or subtracted from the prescaler register when the prescaler register equals 0x3FFF and then increments. The compensation interval is used to adjust the frequency at which the time compensation value is used, that is, from once a second to once every 256 seconds.

Updates to the time compensation register will not take effect until the next time the time seconds register increments and provided the previous compensation interval has expired. When the compensation interval is set to other than once a second then the compensation is applied in the first second interval and the remaining second intervals receive no compensation.

Compensation is disabled by configuring the time compensation register to zero.

53.4.4 Time alarm

The Time Alarm register (TAR), SR[TAF], and IER[TAIE] allow the RTC to generate an interrupt at a predefined time. The 32-bit TAR is compared with the 32-bit Time Seconds register (TSR) each time it increments. SR[TAF] will set when TAR equals TSR and TSR increments.

SR[TAF] is cleared by writing TAR. This will usually be the next alarm value, although writing a value that is less than TSR, such as 0, will prevent SR[TAF] from setting again. SR[TAF] cannot otherwise be disabled, although the interrupt it generates is enabled or disabled by IER[TAIE].

53.4.5 Update mode

The Update Mode field in the Control register (CR[UM]) configures software write access to the Time Counter Enable (SR[TCE]) field. When CR[UM] is clear, SR[TCE] can be written only when LR[SRL] is set. When CR[UM] is set, SR[TCE] can also be written when SR[TCE] is clear or when SR[TIF] or SR[TOF] are set. This allows the time seconds and prescaler registers to be initialized whenever time is invalidated, while preventing the time seconds and prescaler registers from being changed on the fly. When LR[SRL] is set, CR[UM] has no effect on SR[TCE].

53.4.6 Register lock

The Lock register (LR) can be used to block write accesses to certain registers until the next VBAT POR or software reset. Locking the Control register (CR) will disable the software reset. Locking LR will block future updates to LR.

Write accesses to a locked register are ignored and do not generate a bus error.

53.4.7 Access control

The read access and write access registers are implemented in the chip power domain and reset on the chip reset. They are not affected by the VBAT POR or the software reset. They are used to block read or write accesses to each register until the next chip system reset. When accesses are blocked, the bus access is not seen in the VBAT power supply and does not generate a bus error.

53.4.8 Interrupt

The RTC interrupt is asserted whenever a status flag and the corresponding interrupt enable bit are both set. It is always asserted on VBAT POR, and software reset, and when the VBAT power supply is powered down. The RTC interrupt is enabled at the chip level

by enabling the chip-specific RTC clock gate control bit. The RTC interrupt can be used to wakeup the chip from any low-power mode. If the RTC wakeup pin is enabled and the chip is powered down, the RTC interrupt will cause the wakeup pin to assert.

The optional RTC seconds interrupt is an edge-sensitive interrupt with a dedicated interrupt vector that is generated once a second and requires no software overhead (there is no corresponding status flag to clear). It is enabled in the RTC by the time seconds interrupt enable bit and enabled at the chip level by setting the chip-specific RTC clock gate control bit. The RTC seconds interrupt does not cause the RTC wakeup pin to assert. This interrupt is optional and may not be implemented on all devices.

Chapter 54
Universal Serial Bus Full Speed OTG Controller (USBFSOTG)

54.1 Chip-specific USBFSOTG information

54.1.1 Universal Serial Bus (USB) FS Subsystem

The USB FS subsystem includes these components:

- Dual-role USB OTG-capable (On-The-Go) controller that supports a full-speed (FS) device or FS/LS host. The module complies with the USB 2.0 specification.
- USB transceiver that includes internal 15 kΩ pulldowns on the D+ and D- lines for host mode functionality and a 1.5 kΩ pullup on the D+ line for device mode functionality.
- A 3.3V regulator
- USB device charger detection module
- Status detection and wakeup functions for USB data pins, VBUS/VREGIN pins, and OTG ID pins.
- IRC48 with clock recovery block to eliminate the 48MHz crystal. This is available for USB device mode only.
- A configurable connection to allow LPUART2 transmit and receive pins to be connected to the Full Speed USB physical layer.

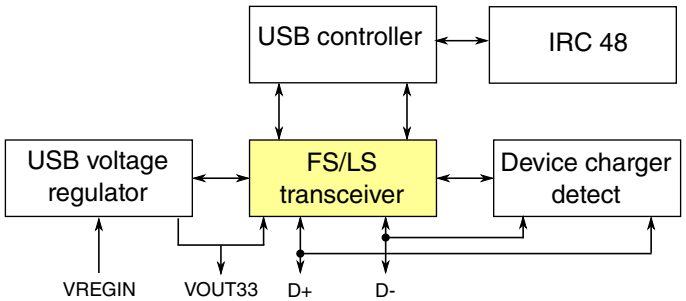


Figure 54-1. USB FS/LS Subsystem Overview

NOTE

Use the following code sequence to select USB clock source, USB clock divide ratio, and enable its clock gate to avoid potential clock glitches which may result in USB enumeration stage failure.

1. Select the USB clock source by configuring SIM_SOPT2.
2. Select the desired clock divide ratio by configuring SIM_CLKDIV2.
3. Enable USB clock gate by setting SIM_SCGC4.

54.1.2 FS/LS USB OTG Instantiation

54.1.2.1 LPUART Over USB Capability

This device supports a connection whereby LPUART2 may be connected to the FS USB physical layer (and the USB controller disconnected) to allow simple debugging capabilities for applications which do not have direct physical access to LPUART2.

By setting the UARTSEL bit in the USBx_USBCTRL register, LPUART2 will be connected to the FS USB physical layer. This configures the FS USB DP/DM signals to be configured as normal LPUART2 signals, which do not operate in differential mode. When UARTCHLS bit in the USBx_USBCTRL register is set to 1’b0, FS USB DP/DM signal pins will be used as LPUART2 TX/RX. When UARTCHLS bit in the USBx_USBCTRL register is set to 1’b1, FS USB DP/DM signal pins will be used as LPUART2 RX/TX.

54.1.3 USB and VREGIN pin status detection and wakeup interrupt features

This device does not have a dedicated VBUS detect pin. For VBUS detection, use either VREGIN for bus-powered USB cases or a GPIO pin for both bus-powered and self-powered USB cases. Because the GPIO pins on this device do not directly support a 5V input, use an external resistive voltage divider to keep the input voltage within the valid range if a GPIO pin is used for VBUS detection.

This device does not have a dedicated OTG ID detect pin. For OTG ID pin detection, if needed, use a GPIO configured as an input pin with pullup enabled.

When the USB detects that there is no activity on the USB bus for more than 3 ms, the USBx_ISTAT[SLEEP] bit is set. This bit can cause an interrupt and software decides the appropriate action.

Waking from a low power mode (except in LLS/VLLS mode where USB is not powered) occurs through an asynchronous interrupt triggered by activity on the USB bus. Setting the USBx_USBTRC0[USBRESMEN] bit enables this function.

The following wakeup features are also supported:

- In Stop/VLPS, the USB controller can generate an interrupt on VREGIN detection using the USBx_MISCCTRL[VFEDG_EN, VREDG_EN] and USBx_USBTRC0[VFEDG_DET, VREDG_DET] fields.
- In LLS/VLLS except VLLS1/0, VREGIN is an input pin to the LLWU and a transition on it can generate a wakeup.
- In LLS/VLLS, USB0_DP and USB0_DM are input pins to the LLWU and a transition on those pins can generate a wakeup provided the USB is powered and in host mode.
- In LLS/VLLS, the GPIO pins chosen to detect VBUS and OTG ID are also input to the LLWU, so transitions on them can generate a wakeup.

54.1.4 USB Power Distribution

This device includes an internal 5 V to 3.3 V USB regulator that always powers the USB transceiver and the USB device charger detection module. The regulator output may optionally be used to supply power to the device itself (by connecting to VDD).

54.1.4.1 AA/AAA cells power supply

The chip can be powered by two AA/AAA cells. In this case, the MCU is powered through VDD which is within the 1.8 to 3.0 V range. After USB cable insertion is detected, the USB regulator is enabled to power the USB transceiver.

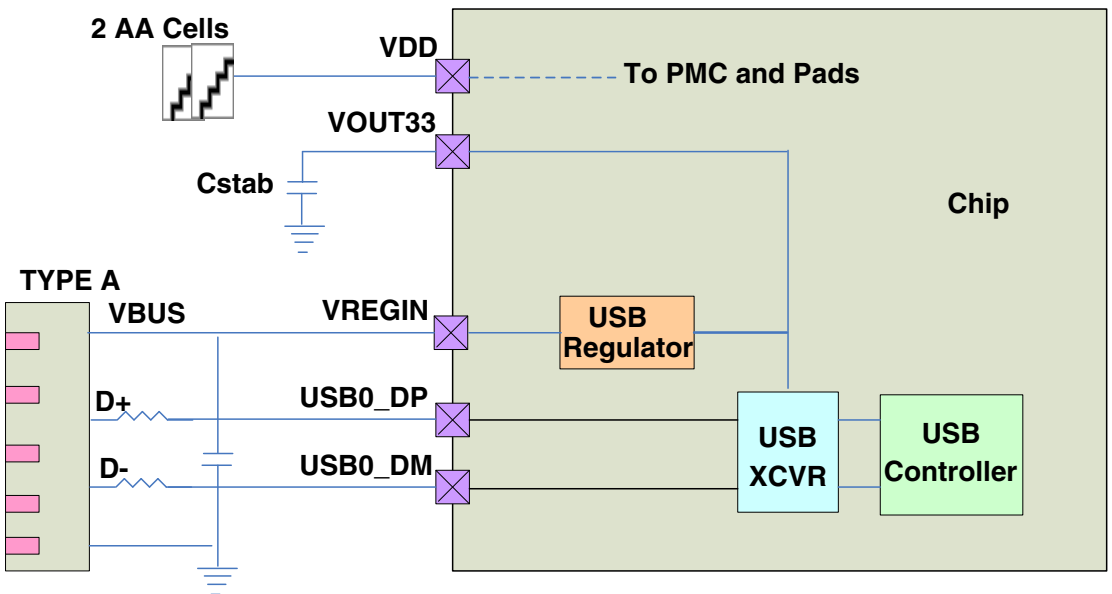


Figure 54-2. USB regulator AA cell usecase

54.1.4.2 Li-Ion battery power supply

The chip can also be powered by a single Li-ion battery. In this case, VOUT33 is connected to VDD. The USB regulator must be enabled by default to power the MCU. When connected to a USB host, the input source of this regulator is switched to the USB bus supply from the Li-ion battery. To charge the battery, the MCU can configure the battery charger according to the charger detection information.

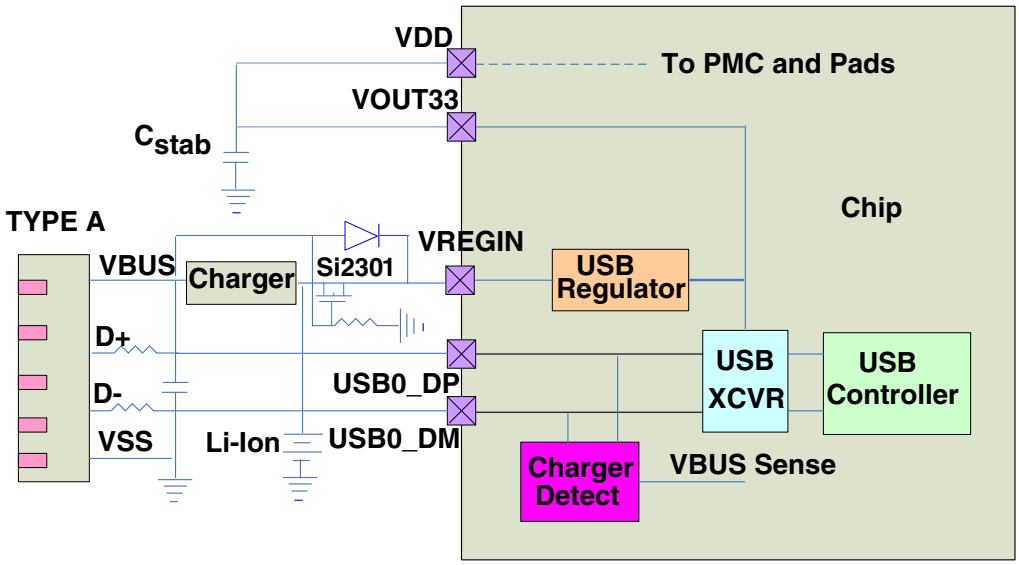


Figure 54-3. USB regulator Li-ion usecase

54.1.4.3 USB bus power supply

The chip can also be powered by the USB bus directly. In this case, VOUT33 is connected to VDD. The USB regulator must be enabled by default to power the MCU, then to power USB transceiver or external sensor.

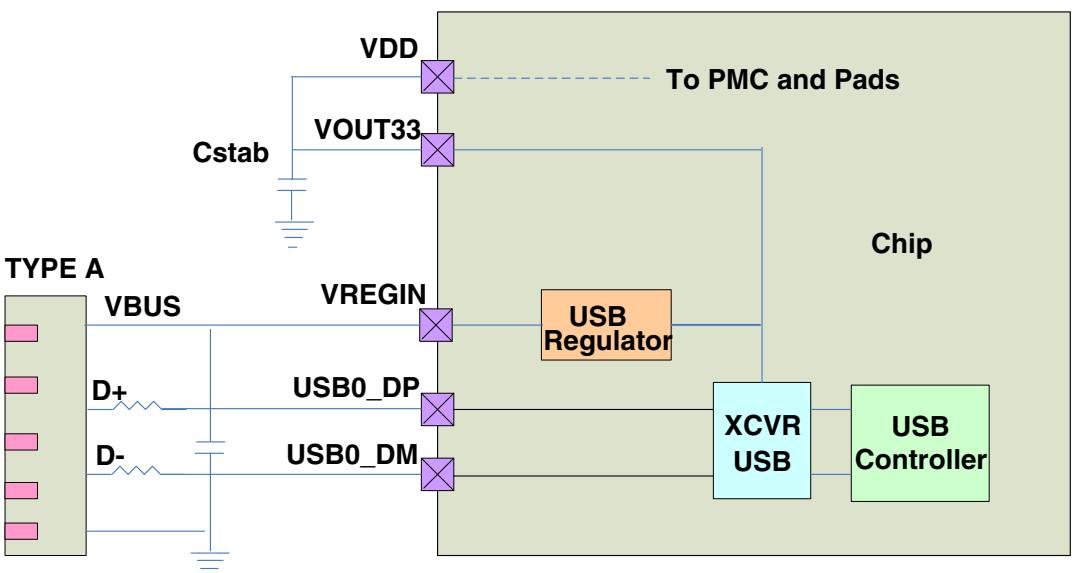


Figure 54-4. USB regulator bus supply

54.1.5 USB power management

The regulator should be put into STANDBY mode whenever the chip is in Stop mode and the USB bus is not in use. The regulator must remain in RUN mode for all USB communication including Suspend, Resume and Reset signaling.

54.2 Introduction

This chapter describes the USB full speed OTG controller. The OTG implementation in this module provides limited host functionality and device solutions for implementing a USB 2.0 full-speed/low-speed compliant peripheral. The OTG logic implements features required by the *On-The-Go and Embedded Host Supplement to the USB 2.0 Specification* (usb.org, 2008). The USB full speed controller interfaces to a USBFS/LS transceiver.

NOTE

This chapter describes the following registers that have similar names: USB_OTGCTL, USB_CTL, USB_CTRL, and USB_CONTROL. These are all separate registers.

54.2.1 References

The following publications are referenced in this document. For copies or updates to these specifications, see the USB Implementers Forum, Inc. website at http://www.usb.org.

- *Universal Serial Bus Specification, Revision 2.0* , 2000, with amendments including those listed below
- *Errata for "USB Revision 2.0 April 27, 2000" as of 12/7/2000*
- *Errata for "USB Revision 2.0 April 27, 2000" as of 12/7/2000*
- *Pull-up / Pull-down Resistors* (USB Engineering Change Notice)
- *Suspend Current Limit Changes* (USB Engineering Change Notice)
- *Device Capacitance* (USB Engineering Change Notice)
- *USB 2.0 Connect Timing Update* (USB Engineering Change Notice as of April 4, 2013)
- *USB 2.0 VBUS Max Limit* (USB Engineering Change Notice)

- *On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification*, Revision 2.0 version 1.1a, July 27, 2012
- *Maximum VBUS Voltage* (USB OTGEH Engineering Change Notice)
- *Universal Serial Bus Micro-USB Cables and Connectors Specification*, Revision 1.01, 2007

54.2.2 USB—Overview

The USB is a cable bus that supports data exchange between a host computer and a wide range of simultaneously accessible peripherals. The attached peripherals share USB bandwidth through a host-scheduled, token-based protocol. The bus allows peripherals to be attached, configured, used, and detached while the host and other peripherals are in operation.

USB software provides a uniform view of the system for all application software, hiding implementation details to make application software more portable. It manages the dynamic attach and detach of peripherals.

There is only one host in any USB system. The USB interface to the host computer system is referred to as the Host Controller.

There may be multiple USB devices in any system such as human interface devices, speakers, printers, etc. USB devices present a standard USB interface in terms of comprehension, response, and standard capability.

The host initiates transactions to specific peripherals, whereas the device responds to control transactions. The device sends and receives data to and from the host using a standard USB data format. USB 2.0 full-speed /low-speed peripherals operate at 12Mbit/s or 1.5 Mbit/s.

For additional information, see the USB 2.0 specification.

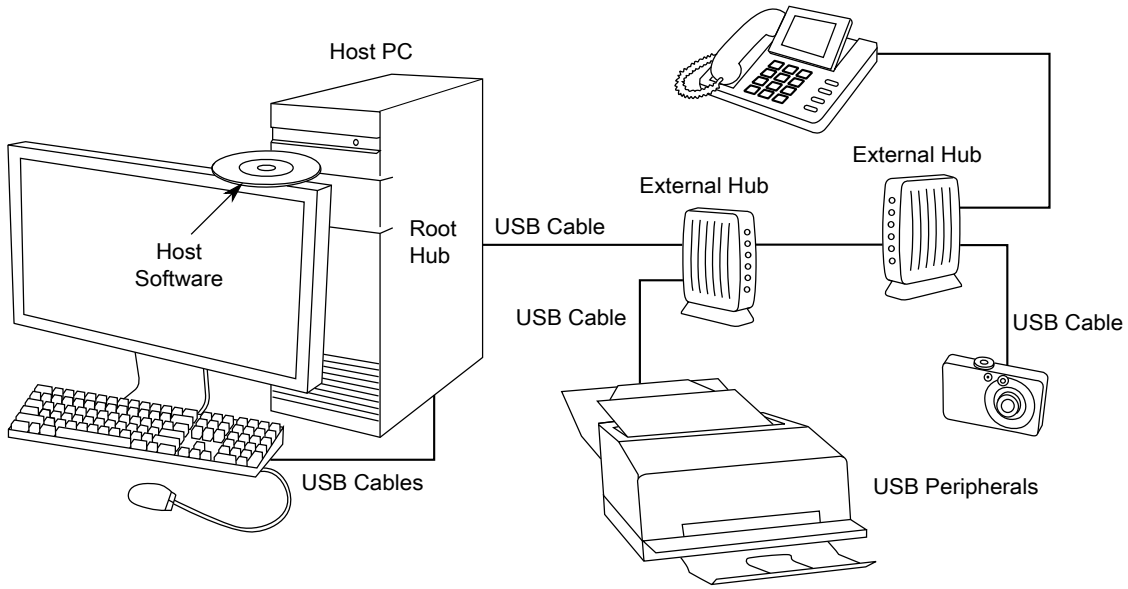


Figure 54-5. Example USB 2.0 system configuration

54.2.3 USB On-The-Go

USB is a popular standard for connecting peripherals and portable consumer electronic devices such as digital cameras and tablets to host PCs. The On-The-Go (OTG) Supplement to the USB Specification extends USB to peer-to-peer application. Using USB OTG technology, consumer electronics, peripherals, and portable devices can connect to each other to exchange data. For example, a digital camera can connect directly to a printer, or a keyboard can connect to a tablet to exchange data.

With the USB On-The-Go product, you can develop a fully USB-compliant peripheral device that can also assume the role of a USB host. Software determines the role of the device based on hardware signals, and then initializes the device in the appropriate mode of operation (host or peripheral) based on how it is connected. After connecting, the devices can negotiate using the OTG protocols to assume the role of host or peripheral based on the task to be accomplished.

For additional information, see the *On-The-Go and Embedded Host Supplement to the USB 2.0 Specification*.

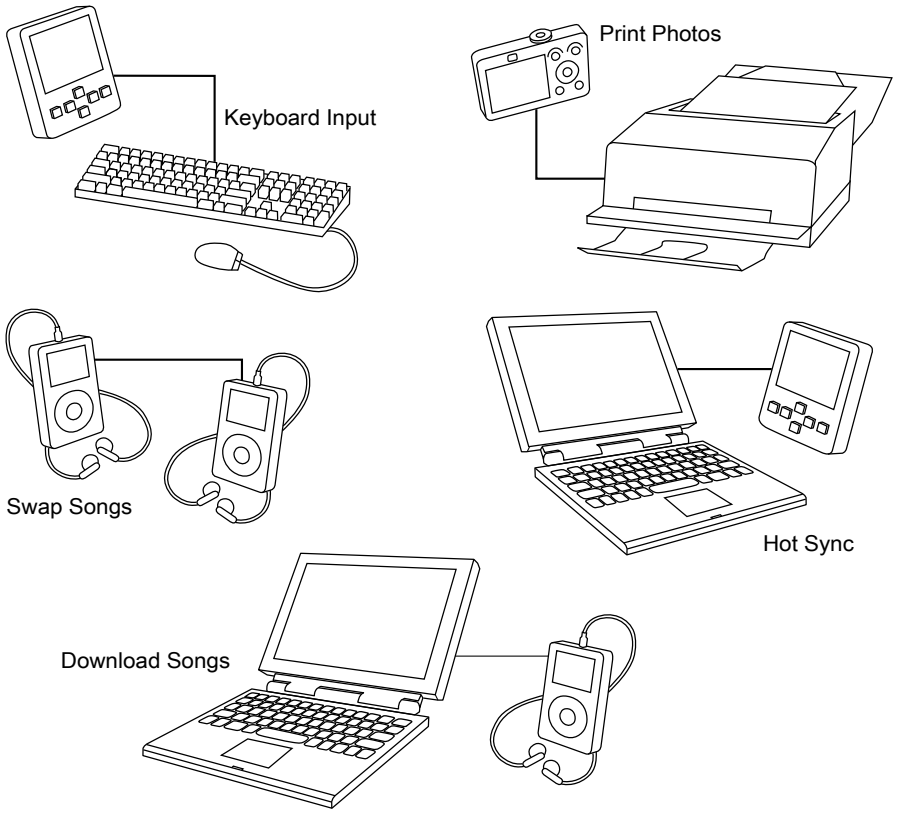


Figure 54-6. Example USB 2.0 On-The-Go configurations

54.2.4 USBFS Features

- USB 1.1 and 2.0 compatible FS device and FS/LS host controller with On-The-Go protocol logic
- 16 bidirectional endpoints
- DMA or FIFO data stream interfaces
- Low-power consumption
- IRC48M with clock-recovery is supported to eliminate the 48 MHz crystal. It is used for USB device-only implementation.

54.3 Functional description

USBOTG communicates with the processor core through status registers, control registers, and data structures in memory.

54.3.1 Data Structures

To efficiently manage USB endpoint communications, USBFS implements a Buffer Descriptor Table (BDT) in system memory. See Figure 54-10.

54.3.2 On-chip transceiver required external components

USB system operation requires external components to ensure that driver output impedance, eye diagram, and VBUS cable fault tolerance requirements are met. DM and DP I/O pads must connect through series resistors (approximately 33 Ω each) to the USB connector on the application printed circuit board (PCB). Additionally, signal quality optimizes when these 33 Ω resistors are mounted closer to the processor than to the USB board-level connector. The USB transceiver includes:

- An internal 1.5 kΩ pullup resistor on the USB_DP line for full-speed device (controlled by USB_CONTROL[DPPULLUPNONOTG] or USB_OTGCTL[DPHIGH])
- Internal 15 kΩ pulldown resistors on the USB_DP and USB_DM signals, which are primarily intended for Host mode operation but are also useful in Device mode as explained below.

NOTE

For device operation, the internal 15 kΩ pulldowns should be enabled to keep the DP and DM ports in a known quiescent state when the VBUS detection software determines that the USB connection is not activated, including the cases when no cable to a host is present or when the USB port is not used. The internal 15 kΩ pulldowns should be controlled by USB_CTRL[PDE] in this case.

For host operation, the internal 15 kΩ pulldowns are enabled automatically, as required by the USB 2.0 specification, when USB_CTL[HOSTMODEEN] is asserted high.

The following diagrams provide overviews of host-only, device-only, and dual-role connections, respectively. For more details, see the *Kinetis Peripheral Module Quick Reference*(KQRUG).

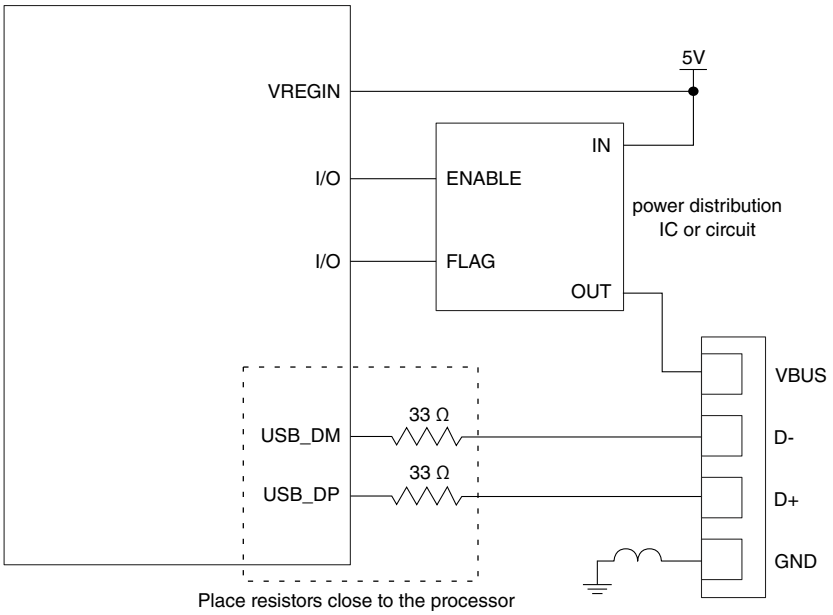


Figure 54-7. Host-only diagram

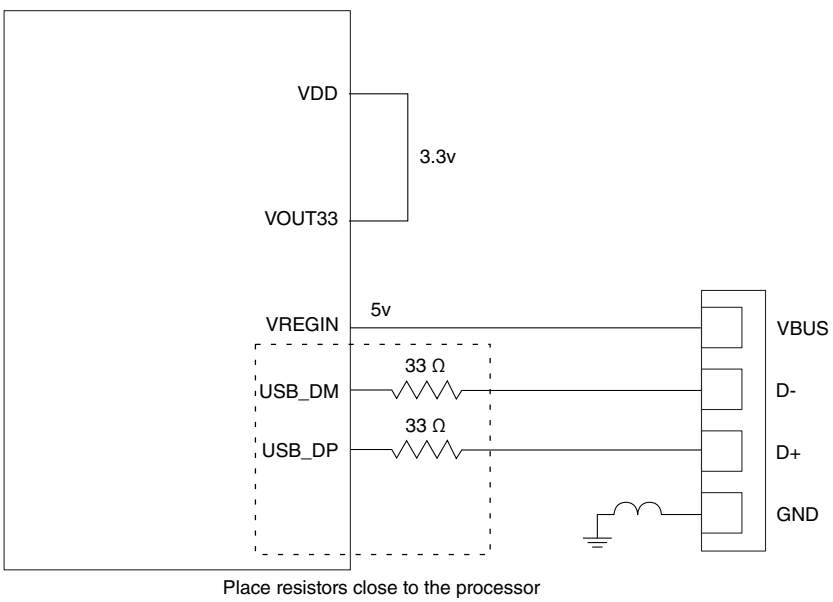


Figure 54-8. Typical Device-only diagram (bus-powered)

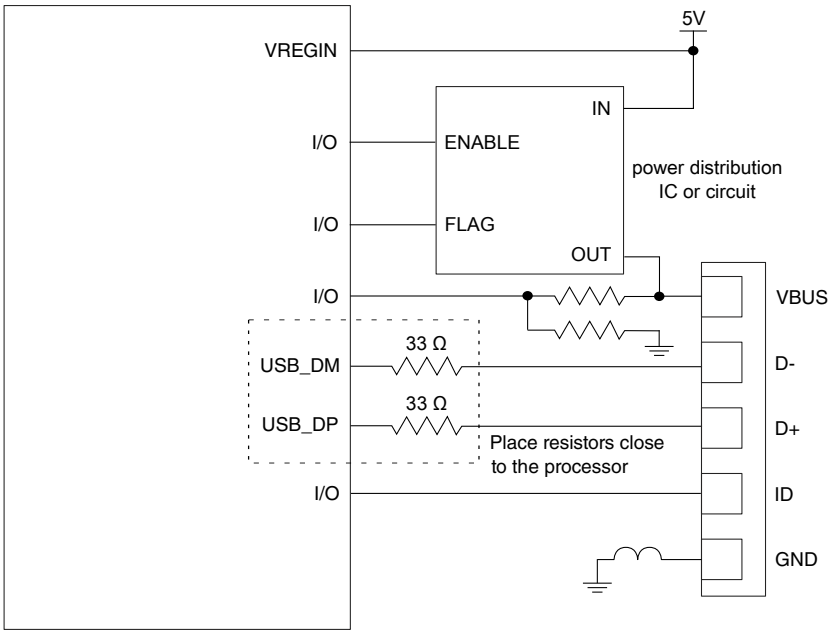


Figure 54-9. Dual-role diagram

54.4 Programmers interface

This section discusses the major components of the programming model for the USB module.

54.4.1 Buffer Descriptor Table

To efficiently manage USB endpoint communications USBFS implements a Buffer Descriptor Table (BDT) in system memory. The BDT resides on a 512-byte boundary in system memory and is pointed to by the BDT Page Registers. Every endpoint direction requires two 8-byte Buffer Descriptor (BD) entries. Therefore, a system with 16 fully bidirectional endpoints would require 512 bytes of system memory to implement the BDT. The two BD entries allows for an EVEN BD and ODD BD entry for each endpoint direction. This allows the microprocessor to process one BD while USBFS is processing the other BD. Double buffering BDs in this way allows USBFS to transfer data easily at the maximum throughput provided by USB.

Software should manage buffers for USBFS by updating the BDT when needed. This allows USBFS to efficiently manage data transmission and reception, while the microprocessor performs communication overhead processing and other function dependent applications. Because the buffers are shared between the microprocessor and

USBFS, a simple semaphore mechanism is used to distinguish who is allowed to update the BDT and buffers in system memory. A semaphore, the OWN bit, is cleared to 0 when the BD entry is owned by the microprocessor. The microprocessor is allowed read and write access to the BD entry and the buffer in system memory when the OWN bit is 0. When the OWN bit is set to 1, the BD entry and the buffer in system memory are owned by USBFS. USBFS now has full read and write access and the microprocessor must not modify the BD or its corresponding data buffer. The BD also contains indirect address pointers to where the actual buffer resides in system memory. This indirect address mechanism is shown in the following diagram.

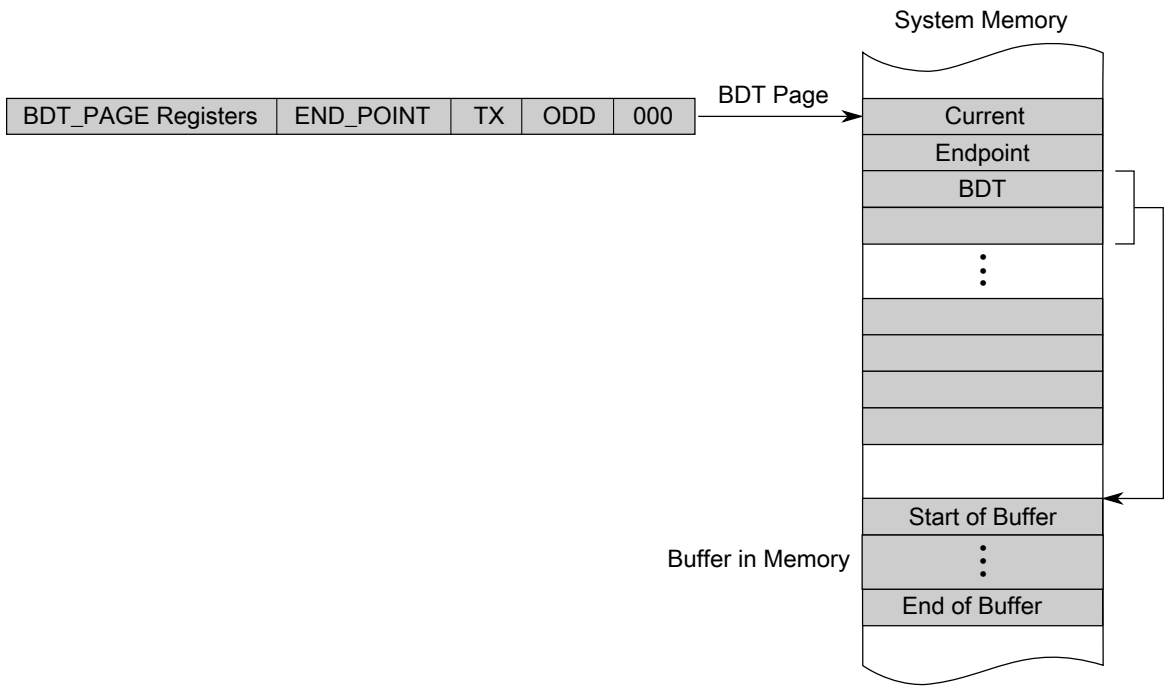


Figure 54-10. Buffer descriptor table

54.4.2 RX vs. TX as a USB peripheral device or USB host

The USBFS core uses software control to switch between two modes of operation:

- USB peripheral device
- USB hosts

In either mode, USB host or USB peripheral device, the same data paths and buffer descriptors are used for the transmission and reception of data. For this reason, a USBFS core-centric nomenclature is used to describe the direction of the data transfer between the USBFS core and USB:

- "RX" (or "receive") describes transfers that move data from USB to memory.
- "TX" (or "transmit") describes transfers that move data from memory to USB.

The following table shows how the data direction corresponds to the USB token type in host and peripheral device applications.

Table 54-1. Data direction for USB host or USB peripheral device

	RX	TX
Device	OUT or SETUP	IN
Host	IN	OUT or SETUP

54.4.3 Addressing BDT entries

An understanding of the addressing mechanism of the Buffer Descriptor Table is useful when accessing endpoint data via USBFS or microprocessor. Some points of interest are:

- The BDT occupies up to 512 bytes of system memory.
- 16 bidirectional endpoints can be supported with a full BDT of 512 bytes.
- 16 bytes are needed for each USB endpoint direction.
- Applications with fewer than 16 endpoints require less RAM to implement the BDT.
- The BDT Page Registers (BDT_PAGE) point to the starting location of the BDT.
- The BDT must be located on a 512-byte boundary in system memory.
- All enabled TX and RX endpoint BD entries are indexed into the BDT to allow easy access via USBFS or MCU core.

When a USB token on an enabled endpoint is received, USBFS uses its integrated DMA controller to interrogate the BDT. USBFS reads the corresponding endpoint BD entry to determine whether it owns the BD and corresponding buffer in system memory.

To compute the entry point into the BDT, the BDT_PAGE registers are concatenated with the current endpoint and the TX and ODD fields to form a 32-bit address. This address mechanism is shown in the following tables:

Table 54-2. BDT Address Calculation

31:24	23:16	15:9	8:5	4	3	2:0
BDT_PAGE_03	BDT_PAGE_02	BDT_PAGE_01[7:1]	Endpoint	TX	ODD	000

Table 54-3. BDT address calculation fields

Field	Description
BDT_PAGE	BDT_PAGE registers in the Control Register Block
ENDPOINT	ENDPOINT field from the USB TOKEN
TX	1 for transmit transfers and 0 for receive transfers

Table continues on the next page...

Table 54-3. BDT address calculation fields (continued)

Field	Description
ODD	Maintained within the USBFS SIE. It corresponds to the buffer currently in use. The buffers are used in a ping-pong fashion.

54.4.4 Buffer Descriptors (BDs)

A buffer descriptor provides endpoint buffer control information for USBFS and the processor. The Buffer Descriptors have different meaning based on whether it is USBFS or the processor reading the BD in memory.

The USBFS Controller uses the data stored in the BDs to determine:

- Who owns the buffer in system memory
- Data0 or Data1 PID
- Whether to release ownership upon packet completion
- No address increment (FIFO mode)
- Whether data toggle synchronization is enabled
- How much data is to be transmitted or received
- Where the buffer resides in system memory

While the processor uses the data stored in the BDs to determine:

- Who owns the buffer in system memory
- Data0 or Data1 PID
- The received TOKEN PID
- How much data was transmitted or received
- Where the buffer resides in system memory

The format for the BD is shown in the following figure.

Table 54-4. Buffer descriptor format

31:26	25:16	15:8	7	6	5	4	3	2	1	0
RSVD	BC (10 bits)	RSVD	OWN	DATA0/1	KEEP/ TOK_PID[3]	NINC/ TOK_PID[2]	DTS/ TOK_PID[1]	BDT_STALL/ TOK_PID[0]	0	0

Table continues on the next page...

Table 54-4. Buffer descriptor format (continued)

Buffer Address (32-Bits)

Table 54-5. Buffer descriptor fields

Field	Description
31–26 RSVD	Reserved
25–16 BC	Byte Count Represents the 10-bit byte count. The USBFS SIE changes this field upon the completion of a RX transfer with the byte count of the data received.
15–8 RSVD	Reserved
7 OWN	Determines whether the processor or USBFS currently owns the buffer. Except when KEEP=1, the SIE hands ownership back to the processor after completing the token by clearing this bit. This must always be the last byte of the BD that the processor updates when it initializes a BD. 0 The processor has access to the BD. USBFS ignores all other fields in the BD. 1 USBFS has access to the BD. While USBFS owns the BD, the processor should not modify any other fields in the BD.
6 DATA0/1	Defines whether a DATA0 field (DATA0/1=0) or a DATA1 (DATA0/1=1) field was transmitted or received. It is unchanged by USBFS.
5 KEEP/ TOK_PID[3]	This bit has two functions: • KEEP bit—When written by the processor, it serves as the KEEP bit. Typically, this bit is 1 with ISO endpoints feeding a FIFO. The microprocessor is not informed that a token has been processed, the data is simply transferred to or from the FIFO. When KEEP is set, normally the NINC bit is also set to prevent address increment. 0 Allows USBFS to release the BD when a token has been processed. 1 This bit is unchanged by USBFS. Bit 3 of the current token PID is written back to the BD by USBFS. • TOK_PID[3]—If the OWN bit is also set, the BD remains owned by USBFS indefinitely; when written by USB, it serves as the TOK_PID[3] bit. 0 or 1 Bit 3 of the current token PID is written back to the BD by USBFS. Typically, this bit is 1 with ISO endpoints feeding a FIFO. The microprocessor is not informed that a token has been processed, the data is simply transferred to or from the FIFO. When KEEP is set, normally the NINC bit is also set to prevent address increment.
4 NINC/ TOK_PID[2]	No Increment (NINC) Disables the DMA engine address increment. This forces the DMA engine to read or write from the same address. This is useful for endpoints when data needs to be read from or written to a single location such as a FIFO. Typically this bit is set with the KEEP bit for ISO endpoints that are interfacing to a FIFO. 0 USBFS writes bit 2 of the current token PID to the BD. 1 This bit is unchanged by USBFS.
3 DTS/	Setting this bit enables USBFS to perform Data Toggle Synchronization.

Table continues on the next page...

Table 54-5. Buffer descriptor fields (continued)

Field	Description
TOK_PID[1]	• If KEEP=0, bit 1 of the current token PID is written back to the BD. • If KEEP=1, this bit is unchanged by USBFS. 0 Data Toggle Synchronization is disabled. 1 Enables USBFS to perform Data Toggle Synchronization.
2 BDT_STALL TOK_PID[0]	Setting this bit causes USBFS to issue a STALL handshake if a token is received by the SIE that would use the BDT in this location. The BDT is not consumed by the SIE (the owns bit remains set and the rest of the BDT is unchanged) when a BDT_STALL bit is set. • If KEEP=0, bit 0 of the current token PID is written back to the BD. • If KEEP=1, this bit is unchanged by USBFS. 0 No stall issued. 1 The BDT is not consumed by the SIE (the OWN bit remains set and the rest of the BDT is unchanged). Setting BDT_STALL also causes the corresponding USB_ENDPT*n*[EPSTALL] bit to set. This causes USBOTG to issue a STALL handshake for both directions of the associated endpoint. To clear the stall condition: 1. Clear the associated USB_ENDPT*n*[EPSTALL] bit. 2. Write the BDT to clear OWN and BDT_STALL.
TOK_PID[n]	Bits [5:2] can also represent the current token PID. The current token PID is written back in to the BD by USBFS when a transfer completes. The values written back are the token PID values from the USB specification: • 0x1h for an OUT token. • 0x9h for an IN token. • 0xDh for a SETUP token. In host mode, this field is used to report the last returned PID or a transfer status indication. The possible values returned are: • 0x3h DATA0 • 0xBh DATA1 • 0x2h ACK • 0xEh STALL • 0xAh NAK • 0x0h Bus Timeout • 0xFh Data Error
1–0 Reserved	Reserved, should read as zeroes.
ADDR[31:0]	Address Represents the 32-bit buffer address in system memory. These bits are unchanged by USBFS.

54.4.5 USB transaction

When USBFS transmits or receives data, it computes the BDT address using the address generation shown in "Addressing Buffer Descriptor Entries" table.

If OWN =1, the following process occurs:

1. USBFS reads the BDT.
2. The SIE transfers the data via the DMA to or from the buffer pointed to by the ADDR field of the BD.
3. When the TOKEN is complete, USBFS updates the BDT and, if KEEP=0, changes the OWN bit to 0.
4. The STAT register is updated and the TOK_DNE interrupt is set.
5. When the processor processes the TOK_DNE interrupt, it reads from the status register all the information needed to process the endpoint.
6. At this point, the processor allocates a new BD so that additional USB data can be transmitted or received for that endpoint, and then processes the last BD.

The following figure shows a timeline of how a typical USB token is processed after the BDT is read and OWN=1.

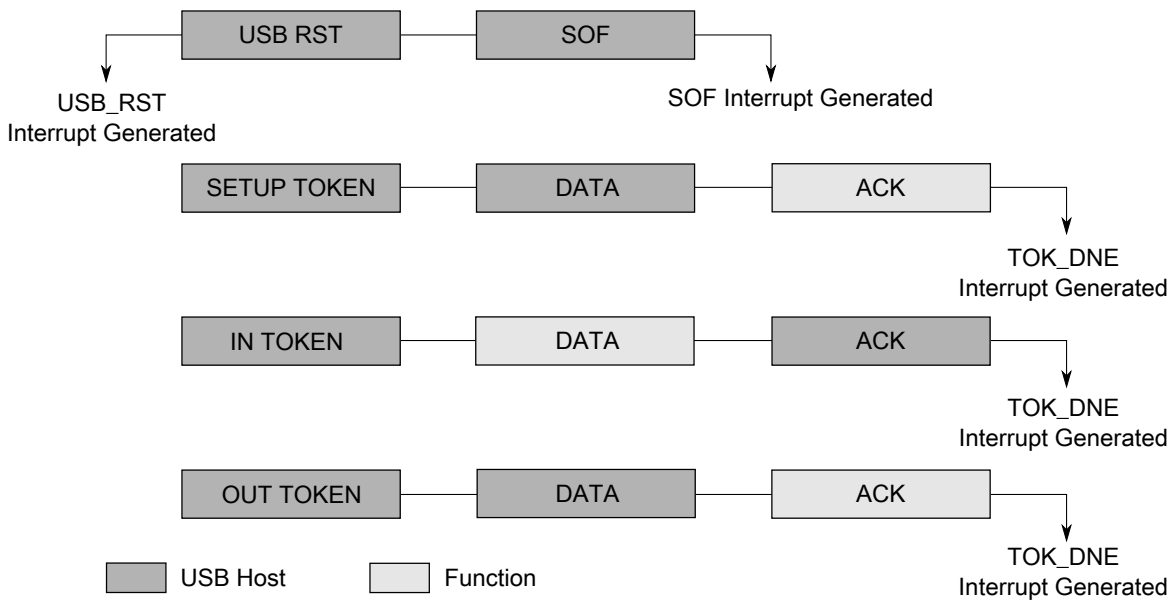


Figure 54-11. USB token transaction

The USB has two sources for the DMA overrun error:

Memory Latency

The memory latency may be too high and cause the receive FIFO to overflow. This is predominantly a hardware performance issue, usually caused by transient memory access issues.

Oversized Packets

The packet received may be larger than the negotiated *MaxPacket* size. Typically, this is caused by a software bug. For DMA overrun errors due to oversized data packets, the USB specification is ambiguous. It assumes correct software drivers on both sides.

NAKing the packet can result in retransmission of the already oversized packet data. Therefore, in response to oversized packets, the USB core continues ACKing the packet for non-isochronous transfers.

Table 54-6. USB responses to DMA overrun errors

Errors due to Memory Latency	Errors due to Oversized Packets
Non-Acknowledgment (NAK) or Bus Timeout (BTO) — See bit 4 in "Error Interrupt Status Register (ERRSTAT)" as appropriate for the class of transaction.	Continues acknowledging (ACKing) the packet for non-isochronous transfers.
—	The data written to memory is clipped to the MaxPacket size so as not to corrupt system memory.
The DMAERR bit is set in the ERRSTAT register for host and device modes of operation. Depending on the values of the INTENB and ERRENB register, the core may assert an interrupt to notify the processor of the DMA error.	Asserts ERRSTAT[DMAERR] ,which can trigger an interrupt and TOKDNE interrupt fires. Note: The TOK_PID field of the BDT is not 1111 because the DMAERR is not due to latency.
• For host mode, the TOKDNE interrupt is generated and the TOK_PID field of the BDT is 1111 to indicate the DMA latency error. Host mode software can decide to retry or move to next scheduled item. • In device mode, the BDT is not written back nor is the TOKDNE interrupt triggered because it is assumed that a second attempt is queued and will succeed in the future.	The packet length field written back to the BDT is the MaxPacket value that represents the length of the clipped data actually written to memory.
From here, the software can decide an appropriate course of action for future transactions such as stalling the endpoint, canceling the transfer, disabling the endpoint, etc.	

54.5 Memory map/Register definitions

This section provides the memory map and detailed descriptions of all USB interface registers.

USB memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4007_2000	Peripheral ID register (USB0_PERID)	8	R	04h	54.5.1/1746
4007_2004	Peripheral ID Complement register (USB0_IDCOMP)	8	R	FBh	54.5.2/1746
4007_2008	Peripheral Revision register (USB0_REV)	8	R	33h	54.5.3/1747
4007_200C	Peripheral Additional Info register (USB0_ADDINFO)	8	R	01h	54.5.4/1747
4007_2010	OTG Interrupt Status register (USB0_OTGISTAT)	8	R/W	00h	54.5.5/1748
4007_2014	OTG Interrupt Control register (USB0_OTGICR)	8	R/W	00h	54.5.6/1749
4007_2018	OTG Status register (USB0_OTGSTAT)	8	R/W	00h	54.5.7/1750
4007_201C	OTG Control register (USB0_OTGCTL)	8	R/W	00h	54.5.8/1751
4007_2080	Interrupt Status register (USB0_ISTAT)	8	R/W	00h	54.5.9/1752

Table continues on the next page...

USB memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4007_2084	Interrupt Enable register (USB0_INTEN)	8	R/W	00h	54.5.10/ 1753
4007_2088	Error Interrupt Status register (USB0_ERRSTAT)	8	R/W	00h	54.5.11/ 1754
4007_208C	Error Interrupt Enable register (USB0_ERREN)	8	R/W	00h	54.5.12/ 1755
4007_2090	Status register (USB0_STAT)	8	R	00h	54.5.13/ 1756
4007_2094	Control register (USB0_CTL)	8	R/W	00h	54.5.14/ 1757
4007_2098	Address register (USB0_ADDR)	8	R/W	00h	54.5.15/ 1758
4007_209C	BDT Page register 1 (USB0_BDTPAGE1)	8	R/W	00h	54.5.16/ 1759
4007_20A0	Frame Number register Low (USB0_FRMNUML)	8	R/W	00h	54.5.17/ 1759
4007_20A4	Frame Number register High (USB0_FRMNUMH)	8	R/W	00h	54.5.18/ 1760
4007_20A8	Token register (USB0_TOKEN)	8	R/W	00h	54.5.19/ 1760
4007_20AC	SOF Threshold register (USB0_SOFTHLD)	8	R/W	00h	54.5.20/ 1761
4007_20B0	BDT Page Register 2 (USB0_BDTPAGE2)	8	R/W	00h	54.5.21/ 1762
4007_20B4	BDT Page Register 3 (USB0_BDTPAGE3)	8	R/W	00h	54.5.22/ 1762
4007_20C0	Endpoint Control register (USB0_ENDPT0)	8	R/W	00h	54.5.23/ 1763
4007_20C4	Endpoint Control register (USB0_ENDPT1)	8	R/W	00h	54.5.23/ 1763
4007_20C8	Endpoint Control register (USB0_ENDPT2)	8	R/W	00h	54.5.23/ 1763
4007_20CC	Endpoint Control register (USB0_ENDPT3)	8	R/W	00h	54.5.23/ 1763
4007_20D0	Endpoint Control register (USB0_ENDPT4)	8	R/W	00h	54.5.23/ 1763
4007_20D4	Endpoint Control register (USB0_ENDPT5)	8	R/W	00h	54.5.23/ 1763
4007_20D8	Endpoint Control register (USB0_ENDPT6)	8	R/W	00h	54.5.23/ 1763
4007_20DC	Endpoint Control register (USB0_ENDPT7)	8	R/W	00h	54.5.23/ 1763
4007_20E0	Endpoint Control register (USB0_ENDPT8)	8	R/W	00h	54.5.23/ 1763

Table continues on the next page...

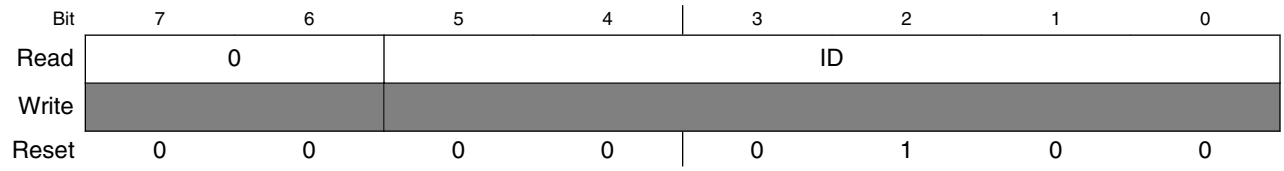
USB memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4007_20E4	Endpoint Control register (USB0_ENDPT9)	8	R/W	00h	54.5.23/ 1763
4007_20E8	Endpoint Control register (USB0_ENDPT10)	8	R/W	00h	54.5.23/ 1763
4007_20EC	Endpoint Control register (USB0_ENDPT11)	8	R/W	00h	54.5.23/ 1763
4007_20F0	Endpoint Control register (USB0_ENDPT12)	8	R/W	00h	54.5.23/ 1763
4007_20F4	Endpoint Control register (USB0_ENDPT13)	8	R/W	00h	54.5.23/ 1763
4007_20F8	Endpoint Control register (USB0_ENDPT14)	8	R/W	00h	54.5.23/ 1763
4007_20FC	Endpoint Control register (USB0_ENDPT15)	8	R/W	00h	54.5.23/ 1763
4007_2100	USB Control register (USB0_USBCTRL)	8	R/W	C0h	54.5.24/ 1764
4007_2104	USB OTG Observe register (USB0_OBSERVE)	8	R	50h	54.5.25/ 1765
4007_2108	USB OTG Control register (USB0_CONTROL)	8	R/W	00h	54.5.26/ 1766
4007_210C	USB Transceiver Control register 0 (USB0_USBTRC0)	8	R/W	00h	54.5.27/ 1766
4007_2114	Frame Adjust Register (USB0_USBFRMADJUST)	8	R/W	00h	54.5.28/ 1768
4007_212C	Miscellaneous Control register (USB0_MISCCTRL)	8	R/W	00h	54.5.29/ 1768
4007_2140	USB Clock recovery control (USB0_CLK_RECOVER_CTRL)	8	R/W	00h	54.5.30/ 1769
4007_2144	IRC48M oscillator enable register (USB0_CLK_RECOVER_IRC_EN)	8	R/W	01h	54.5.31/ 1770
4007_2154	Clock recovery combined interrupt enable (USB0_CLK_RECOVER_INT_EN)	8	R/W	10h	54.5.32/ 1771
4007_215C	Clock recovery separated interrupt status (USB0_CLK_RECOVER_INT_STATUS)	8	w1c	00h	54.5.33/ 1772

54.5.1 Peripheral ID register (USBx_PERID)

Reads back the value of 0x04. This value is defined for the USB peripheral.

Address: 4007_2000h base + 0h offset = 4007_2000h



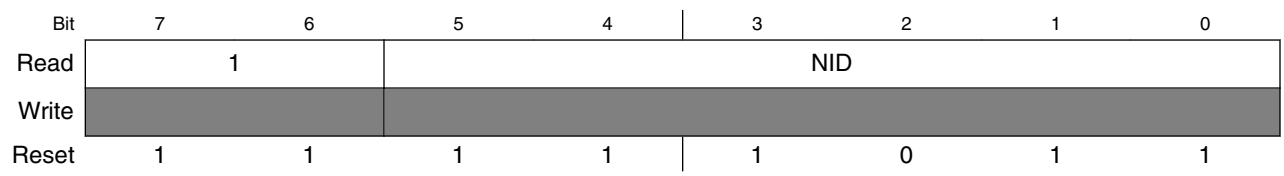
USBx_PERID field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
ID	Peripheral Identification This field always reads 0x4h.

54.5.2 Peripheral ID Complement register (USBx_IDCOMP)

Reads back the complement of the Peripheral ID register. For the USB peripheral, the value is 0xFB.

Address: 4007_2000h base + 4h offset = 4007_2004h



USBx_IDCOMP field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
NID	Ones' complement of PERID[ID] bits.

54.5.3 Peripheral Revision register (USBx_REV)

Contains the revision number of the USB module.

Address: 4007_2000h base + 8h offset = 4007_2008h

Bit	7	6	5	4	3	2	1	0
Read	REV							
Write								
Reset	0	0	1	1	0	0	1	1

USBx_REV field descriptions

Field	Description
REV	Revision Indicates the revision number of the USB Core.

54.5.4 Peripheral Additional Info register (USBx_ADDINFO)

Reads back the value of the Host Enable bit.

Address: 4007_2000h base + Ch offset = 4007_200Ch

Bit	7	6	5	4	3	2	1	0
Read	0					0		IEHOST
Write								
Reset	0	0	0	0	0	0	0	1

USBx_ADDINFO field descriptions

Field	Description
7–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 IEHOST	This bit is set if host mode is enabled.

54.5.5 OTG Interrupt Status register (USBx_OTGISTAT)

Records changes to the state of the one-millisecond timer and line state stable logic. Software can read this register to determine the event that triggers an interrupt. Only bits that have changed since the last software read are set. Writing a one to a bit clears the associated interrupt.

Address: 4007_2000h base + 10h offset = 4007_2010h

Bit	7	6	5	4	3	2	1	0
Read	Reserved	ONEMSEC	LINE_STATE_CHG	0	Reserved	Reserved	0	Reserved
Write	w1c	w1c	w1c		w1c	w1c		w1c
Reset	0	0	0	0	0	0	0	0

USBx_OTGISTAT field descriptions

Field	Description
7 Reserved	This field is reserved. Software must not change the value of this bitfield.
6 ONEMSEC	This bit is set when the 1 millisecond timer expires. This bit stays asserted until cleared by software. The interrupt must be serviced every millisecond to avoid losing 1msec counts.
5 LINE_STATE_CHG	This interrupt is set when the USB line state (CTL[SE0] and CTL[JSTATE] bits) are stable without change for 1 millisecond, and the value of the line state is different from the last time when the line state was stable. It is set on transitions between SE0 and J-state, SE0 and K-state, and J-state and K-state. Changes in J-state while SE0 is true do not cause an interrupt. This interrupt can be used in detecting Reset, Resume, Connect, and Data Line Pulse signaling.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 Reserved	This field is reserved. Software must not change the value of this bitfield.
2 Reserved	This field is reserved. Software must not change the value of this bitfield.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 Reserved	This field is reserved. Software must not change the value of this bitfield.

54.5.6 OTG Interrupt Control register (USBx_OTGICR)

Enables the corresponding interrupt status bits defined in the OTG Interrupt Status Register.

Address: 4007_2000h base + 14h offset = 4007_2014h

Bit	7	6	5	4	3	2	1	0
Read	Reserved	ONEMSECEN	LINESTATEEN	0	Reserved	Reserved	0	Reserved
Write								
Reset	0	0	0	0	0	0	0	0

USBx_OTGICR field descriptions

Field	Description
7 Reserved	Software must not change the value of this bitfield. This field is reserved.
6 ONEMSECEN	One Millisecond Interrupt Enable 0 Diables the 1ms timer interrupt. 1 Enables the 1ms timer interrupt.
5 LINESTATEEN	Line State Change Interrupt Enable 0 Disables the LINE_STAT_CHG interrupt. 1 Enables the LINE_STAT_CHG interrupt.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 Reserved	Software must not change the value of this bitfield. This field is reserved.
2 Reserved	Software must not change the value of this bitfield. This field is reserved.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 Reserved	Software must not change the value of this bitfield. This field is reserved.

54.5.7 OTG Status register (USBx_OTGSTAT)

Displays the actual value from the one-millisecond timer and line state stable logic.

Address: 4007_2000h base + 18h offset = 4007_2018h

Bit	7	6	5	4
Read	0	ONEMSECEN	LINESTATESTABLE	0
Write				
Reset	0	0	0	0

Bit	3	2	1	0
Read	0	0	0	0
Write				
Reset	0	0	0	0

USBx_OTGSTAT field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 ONEMSECEN	This bit is reserved for the 1ms count, but it is not useful to software.
5 LINESTATESTABLE	Indicates that the internal signals that control the LINE_STATE_CHG field of OTGISTAT are stable for at least 1 ms. This bit is used to provide a hardware debounce of the linestate in detection of Connect, Disconnect and Resume signaling. First read LINE_STATE_CHG field and then read this field. If this field reads as 1, then the value of LINE_STATE_CHG can be considered stable. 0 The LINE_STAT_CHG bit is not yet stable. 1 The LINE_STAT_CHG bit has been debounced and is stable.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

54.5.8 OTG Control register (USBx_OTGCTL)

Controls the operation of VBUS and Data Line termination resistors.

Address: 4007_2000h base + 1Ch offset = 4007_201Ch

Bit	7	6	5	4	3	2	1	0
Read	DPHIGH	0	DPLOW	DMLOW	0	OTGEN	0	
Write								
Reset	0	0	0	0	0	0	0	0

USBx_OTGCTL field descriptions

Field	Description
7 DPHIGH	D+ Data Line pullup resistor enable 0 D+ pullup resistor is not enabled 1 D+ pullup resistor is enabled
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 DPLOW	D+ Data Line pull-down resistor enable This bit should always be enabled together with bit 4 (DMLOW) 0 D+ pulldown resistor is not enabled. 1 D+ pulldown resistor is enabled.
4 DMLOW	D– Data Line pull-down resistor enable 0 D- pulldown resistor is not enabled. 1 D- pulldown resistor is enabled.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 OTGEN	On-The-Go pullup/pulldown resistor enable 0 If USB_EN is 1 and HOST_MODE is 0 in the Control Register (CTL), then the D+ Data Line pull-up resistors are enabled. If HOST_MODE is 1 the D+ and D– Data Line pull-down resistors are engaged. 1 The pull-up and pull-down controls in this register are used.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

54.5.9 Interrupt Status register (USBx_ISTAT)

Contains fields for each of the interrupt sources within the USB Module. Each of these fields are qualified with their respective interrupt enable bits. All fields of this register are logically OR'd together along with the OTG Interrupt Status Register (OTGSTAT) to form a single interrupt source for the processor's interrupt controller. After an interrupt bit has been set it may only be cleared by writing a one to the respective interrupt bit. This register contains the value of 0x00 after a reset.

Address: 4007_2000h base + 80h offset = 4007_2080h

Bit	7	6	5	4	3	2	1	0
Read	STALL	ATTACH	RESUME	SLEEP	TOKDNE	SOFTOK	ERROR	USBRST
Write	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

USBx_ISTAT field descriptions

Field	Description
7 STALL	Stall Interrupt In Device mode this bit is asserted when a STALL handshake is sent by the SIE. In Host mode this bit is set when the USB Module detects a STALL acknowledge during the handshake phase of a USB transaction.This interrupt can be used to determine whether the last USB transaction was completed successfully or stalled.
6 ATTACH	Attach Interrupt This field is set when the USB Module detects an attach of a USB device. This field is only valid if CTL[HOSTMODEEN]=1. This interrupt signifies that a peripheral is now present and must be configured; it is asserted if there have been no transitions on the USB for 2.5 µs and the current bus state is not SE0." 0 No Attach is detected since the last time the ATTACH bit was cleared. 1 A peripheral is now present and must be configured (a stable non-SE0 state is detected for more than 2.5 µs).
5 RESUME	This bit is set when a K-state is observed on the DP/DM signals for 2.5 µs. When not in suspend mode this interrupt must be disabled.
4 SLEEP	This bit is set when the USB Module detects a constant idle on the USB bus for 3 ms. The sleep timer is reset by activity on the USB bus.
3 TOKDNE	This bit is set when the current token being processed has completed. The processor must immediately read the STATUS (STAT) register to determine the EndPoint and BD used for this token. Clearing this bit (by writing a one) causes STAT to be cleared or the STAT holding register to be loaded into the STAT register.
2 SOFTOK	This bit is set when the USB Module receives a Start Of Frame (SOF) token. In Host mode this field is set when the SOF threshold is reached (MISCCTRL[SOFBUSSET]=0), or when the SOF counter reaches 0 (MISCCTRL[SOFBUSSET]=1), so that software can prepare for the next SOF.

Table continues on the next page...

USBx_ISTAT field descriptions (continued)

Field	Description
1 ERROR	This bit is set when any of the error conditions within Error Interrupt Status (ERRSTAT) register occur. The processor must then read the ERRSTAT register to determine the source of the error.
0 USBRST	This bit is set when the USB Module has decoded a valid USB reset. This informs the processor that it should write 0x00 into the address register and enable endpoint 0. USBRST is set after a USB reset has been detected for 2.5 microseconds. It is not asserted again until the USB reset condition has been removed and then reasserted.

54.5.10 Interrupt Enable register (USBx_INTEN)

Contains enable fields for each of the interrupt sources within the USB Module. Setting any of these bits enables the respective interrupt source in the ISTAT register. This register contains the value of 0x00 after a reset.

Address: 4007_2000h base + 84h offset = 4007_2084h

Bit	7	6	5	4	3	2	1	0
Read Write	STALLEN	ATTACHEN	RESUMEEN	SLEEPEN	TOKDNEEN	SOFTOKEN	ERROREN	USBRSTEN
Reset	0	0	0	0	0	0	0	0

USBx_INTEN field descriptions

Field	Description
7 STALLEN	STALL Interrupt Enable 0 Diasbles the STALL interrupt. 1 Enables the STALL interrupt.
6 ATTACHEN	ATTACH Interrupt Enable 0 Disables the ATTACH interrupt. 1 Enables the ATTACH interrupt.
5 RESUMEEN	RESUME Interrupt Enable 0 Disables the RESUME interrupt. 1 Enables the RESUME interrupt.
4 SLEEPEN	SLEEP Interrupt Enable 0 Disables the SLEEP interrupt. 1 Enables the SLEEP interrupt.
3 TOKDNEEN	TOKDNE Interrupt Enable 0 Disables the TOKDNE interrupt. 1 Enables the TOKDNE interrupt.
2 SOFTOKEN	SOFTOK Interrupt Enable 0 Disbles the SOFTOK interrupt. 1 Enables the SOFTOK interrupt.

Table continues on the next page...

USBx_INTEN field descriptions (continued)

Field	Description
1 ERROREN	ERROR Interrupt Enable 0 Disables the ERROR interrupt. 1 Enables the ERROR interrupt.
0 USBRSTEN	USBRST Interrupt Enable 0 Disables the USBRST interrupt. 1 Enables the USBRST interrupt.

54.5.11 Error Interrupt Status register (USBx_ERRSTAT)

Contains enable bits for each of the error sources within the USB Module. Each of these bits are qualified with their respective error enable bits. All bits of this register are logically OR'd together and the result placed in the ERROR bit of the ISTAT register. After an interrupt bit has been set it may only be cleared by writing a one to the respective interrupt bit. Each bit is set as soon as the error condition is detected. Therefore, the interrupt does not typically correspond with the end of a token being processed. This register contains the value of 0x00 after a reset.

Address: 4007_2000h base + 88h offset = 4007_2088h

Bit	7	6	5	4	3	2	1	0
Read	BTSERR	OWNERR	DMAERR	BTOERR	DFN8	CRC16	CRC5EOF	PIDERR
Write	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

USBx_ERRSTAT field descriptions

Field	Description
7 BTSERR	This bit is set when a bit stuff error is detected. If set, the corresponding packet is rejected due to the error.
6 OWNERR	This field is valid when the USB Module is operating in peripheral mode (CTL[HOSTMODEEN]=0). It is set if the USB Module requires a new BD for SETUP, ISO IN, or ISO OUT transfer while a new BD is not available.
5 DMAERR	This bit is set if the USB Module has requested a DMA access to read a new BDT but has not been given the bus before it needs to receive or transmit data. If processing a TX transfer this would cause a transmit data underflow condition. If processing a RX transfer this would cause a receive data overflow condition. This interrupt is useful when developing device arbitration hardware for the microprocessor and the USB module to minimize bus request and bus grant latency. This bit is also set if a data packet to or from the host is larger than the buffer size allocated in the BDT. In this case the data packet is truncated as it is put in buffer memory.
4 BTOERR	This bit is set when a bus turnaround timeout error occurs. The USB module contains a bus turnaround timer that keeps track of the amount of time elapsed between the token and data phases of a SETUP or OUT TOKEN or the data and handshake phases of a IN TOKEN. If more than 16 bit times are counted from the previous EOP before a transition from IDLE, a bus turnaround timeout error occurs.

Table continues on the next page...

USBx_ERRSTAT field descriptions (continued)

Field	Description
3 DFN8	This bit is set if the data field received was not 8 bits in length. USB Specification 1.0 requires that data fields be an integral number of bytes. If the data field was not an integral number of bytes, this bit is set.
2 CRC16	This bit is set when a data packet is rejected due to a CRC16 error.
1 CRC5EOF	This error interrupt has two functions. When the USB Module is operating in peripheral mode (CTL[HOSTMODEEN]=0), this interrupt detects CRC5 errors in the token packets generated by the host. If set the token packet was rejected due to a CRC5 error. When the USB Module is operating in host mode (CTL[HOSTMODEEN]=1), this interrupt detects End Of Frame (EOF) error conditions. This occurs when the USB Module is transmitting or receiving data and the SOF counter reaches zero. This interrupt is useful when developing USB packet scheduling software to ensure that no USB transactions cross the start of the next frame.
0 PIDERR	This bit is set when the PID check field fails.

54.5.12 Error Interrupt Enable register (USBx_ERREN)

Contains enable bits for each of the error interrupt sources within the USB module. Setting any of these bits enables the respective interrupt source in ERRSTAT. Each bit is set as soon as the error condition is detected. Therefore, the interrupt does not typically correspond with the end of a token being processed. This register contains the value of 0x00 after a reset.

Address: 4007_2000h base + 8Ch offset = 4007_208Ch

Bit	7	6	5	4	3	2	1	0
Read Write	BTSERREN	OWNERREN	DMAERREN	BTOERREN	DFN8EN	CRC16EN	CRC5EOFEN	PIDERREN
Reset	0	0	0	0	0	0	0	0

USBx_ERREN field descriptions

Field	Description
7 BTSERREN	BTSERR Interrupt Enable 0 Disables the BTSERR interrupt. 1 Enables the BTSERR interrupt.
6 OWNERREN	OWNERR Interrupt Enable This field is valid when the USB module is operating in peripheral mode (CTL[HOSTMODEEN]=0). 0 Disables the OWNERR interrupt. 1 Enables the OWNERR interrupt.
5 DMAERREN	DMAERR Interrupt Enable 0 Disables the DMAERR interrupt. 1 Enables the DMAERR interrupt.

Table continues on the next page...

USBx_ERREN field descriptions (continued)

Field	Description
4 BTOERREN	BTOERR Interrupt Enable 0 Disables the BTOERR interrupt. 1 Enables the BTOERR interrupt.
3 DFN8EN	DFN8 Interrupt Enable 0 Disables the DFN8 interrupt. 1 Enables the DFN8 interrupt.
2 CRC16EN	CRC16 Interrupt Enable 0 Disables the CRC16 interrupt. 1 Enables the CRC16 interrupt.
1 CRC5EOFEN	CRC5/EOF Interrupt Enable 0 Disables the CRC5/EOF interrupt. 1 Enables the CRC5/EOF interrupt.
0 PIDERREN	PIDERR Interrupt Enable 0 Disables the PIDERR interrupt. 1 Enters the PIDERR interrupt.

54.5.13 Status register (USBx_STAT)

Reports the transaction status within the USB module. When the processor's interrupt controller has received a TOKDNE, interrupt the Status Register must be read to determine the status of the previous endpoint communication. The data in the status register is valid when TOKDNE interrupt is asserted. The Status register is actually a read window into a status FIFO maintained by the USB module. When the USB module uses a BD, it updates the Status register. If another USB transaction is performed before the TOKDNE interrupt is serviced, the USB module stores the status of the next transaction in the STAT FIFO. Thus STAT is actually a four byte FIFO that allows the processor core to process one transaction while the SIE is processing the next transaction. Clearing the TOKDNE bit in the ISTAT register causes the SIE to update STAT with the contents of the next STAT value. If the data in the STAT holding register is valid, the SIE immediately reasserts to TOKDNE interrupt.

Address: 4007_2000h base + 90h offset = 4007_2090h

Bit	7	6	5	4	3	2	1	0
Read	ENDP				TX	ODD	0	
Write								
Reset	0	0	0	0	0	0	0	0

USBx_STAT field descriptions

Field	Description
7–4 ENDP	This four-bit field encodes the endpoint address that received or transmitted the previous token. This allows the processor core to determine the BDT entry that was updated by the last USB transaction.
3 TX	Transmit Indicator 0 The most recent transaction was a receive operation. 1 The most recent transaction was a transmit operation.
2 ODD	This bit is set if the last buffer descriptor updated was in the odd bank of the BDT.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

54.5.14 Control register (USBx_CTL)

Provides various control and configuration information for the USB module.

Address: 4007_2000h base + 94h offset = 4007_2094h

Bit	7	6	5	4
Read Write	JSTATE	SE0	TXSUSPENDTOKENBUSY	RESET
Reset	0	0	0	0

Bit	3	2	1	0
Read Write	HOSTMODEEN	RESUME	ODDRST	USBENSOFEN
Reset	0	0	0	0

USBx_CTL field descriptions

Field	Description
7 JSTATE	Live USB differential receiver JSTATE signal The polarity of this signal is affected by the current state of LSEN .
6 SE0	Live USB Single Ended Zero signal
5 TXSUSPENDTOKENBUSY	In Host mode, TOKEN_BUSY is set when the USB module is busy executing a USB token. Software must not write more token commands to the Token Register when TOKEN_BUSY is set. Software should check this field before writing any tokens to the Token Register to ensure that token commands are not lost. In Device mode, TXD_SUSPEND is set when the SIE has disabled packet transmission and reception. Clearing this bit allows the SIE to continue token processing. This bit is set by the SIE when a SETUP Token is received allowing software to dequeue any pending packet transactions in the BDT before resuming token processing.
4 RESET	Setting this bit enables the USB Module to generate USB reset signaling. This allows the USB Module to reset USB peripherals. This control signal is only valid in Host mode (CTL[HOSTMODEEN]=1). Software must set RESET to 1 for the required amount of time and then clear it to 0 to end reset signaling.

Table continues on the next page...

USBx_CTL field descriptions (continued)

Field	Description
3 HOSTMODEEN	When set to 1, this bit enables the USB Module to operate in Host mode. In host mode, the USB module performs USB transactions under the programmed control of the host processor.
2 RESUME	When set to 1 this bit enables the USB Module to execute resume signaling. This allows the USB Module to perform remote wake-up. Software must set RESUME to 1 for the required amount of time and then clear it to 0. If HOSTMODEENis set, the USB module appends a Low Speed End of Packet to the Resume signaling when the RESUME bit is cleared.
1 ODDRST	Setting this bit to 1 resets all the BDT ODD ping/pong fields to 0, which then specifies the EVEN BDT bank.
0 USBENSOFEN	USB Enable Setting this bit enables the USB-FS to operate; clearing it disables the USB-FS. Setting the bit causes the SIE to reset all of its ODD bits to the BDTs. Therefore, setting this bit resets much of the logic in the SIE. When host mode is enabled, clearing this bit causes the SIE to stop sending SOF tokens. 0 Disables the USB Module. 1 Enables the USB Module.

54.5.15 Address register (USBx_ADDR)

Holds the unique USB address that the USB module decodes when in Peripheral mode (CTL[HOSTMODEEN]=0). When operating in Host mode (CTL[HOSTMODEEN]=1) the USB module transmits this address with a TOKEN packet. This enables the USB module to uniquely address any USB peripheral. In either mode, CTL[USBENSOFEN] must be 1. The Address register is reset to 0x00 after the reset input becomes active or the USB module decodes a USB reset signal. This action initializes the Address register to decode address 0x00 as required by the USB specification.

Address: 4007_2000h base + 98h offset = 4007_2098h

Bit	7	6	5	4	3	2	1	0
Read Write	LSEN	ADDR						
Reset	0	0	0	0	0	0	0	0

USBx_ADDR field descriptions

Field	Description
7 LSEN	Low Speed Enable bit Informs the USB module that the next token command written to the token register must be performed at low speed. This enables the USB module to perform the necessary preamble required for low-speed data transmissions.
ADDR	USB Address

Table continues on the next page...

USBx_ADDR field descriptions (continued)

Field	Description
	Defines the USB address that the USB module decodes in peripheral mode, or transmits when in host mode.

54.5.16 BDT Page register 1 (USBx_BDTPAGE1)

Provides address bits 15 through 9 of the base address where the current Buffer Descriptor Table (BDT) resides in system memory. See Buffer Descriptor Table. The 32-bit BDT Base Address is always aligned on 512-byte boundaries, so bits 8 through 0 of the base address are always zero.

Address: 4007_2000h base + 9Ch offset = 4007_209Ch

Bit	7	6	5	4	3	2	1	0
Read	BDTBA							0
Write								
Reset	0	0	0	0	0	0	0	0

USBx_BDTPAGE1 field descriptions

Field	Description
7–1 BDTBA	Provides address bits 15 through 9 of the BDT base address.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

54.5.17 Frame Number register Low (USBx_FRMNUML)

The Frame Number registers (low and high) contain the 11-bit frame number. These registers are updated with the current frame number whenever a SOF TOKEN is received.

Address: 4007_2000h base + A0h offset = 4007_20A0h

Bit	7	6	5	4	3	2	1	0
Read	FRM[7:0]							
Write								
Reset	0	0	0	0	0	0	0	0

USBx_FRMNUML field descriptions

Field	Description
FRM[7:0]	This 8-bit field and the 3-bit field in the Frame Number Register High are used to compute the address where the current Buffer Descriptor Table (BDT) resides in system memory.

54.5.18 Frame Number register High (USBx_FRMNUMH)

The Frame Number registers (low and high) contain the 11-bit frame number. These registers are updated with the current frame number whenever a SOF TOKEN is received.

Address: 4007_2000h base + A4h offset = 4007_20A4h

Bit	7	6	5	4	3	2	1	0
Read	0					FRM[10:8]		
Write								
Reset	0	0	0	0	0	0	0	0

USBx_FRMNUMH field descriptions

Field	Description
7–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
FRM[10:8]	This 3-bit field and the 8-bit field in the Frame Number Register Low are used to compute the address where the current Buffer Descriptor Table (BDT) resides in system memory.

54.5.19 Token register (USBx_TOKEN)

Used to initiate USB transactions when in host mode (CTL[HOSTMODEEN]=1). When the software needs to execute a USB transaction to a peripheral, it writes the TOKEN type and endpoint to this register. After this register has been written, the USB module begins the specified USB transaction to the address contained in the address register. The processor core must always check that the TOKEN_BUSY bit in the control register is not 1 before writing to the Token Register. This ensures that the token commands are not overwritten before they can be executed. The address register and endpoint control register 0 are also used when performing a token command and therefore must also be written before the Token Register. The address register is used to select the USB peripheral address transmitted by the token command. The endpoint control register determines the handshake and retry policies used during the transfer.

Address: 4007_2000h base + A8h offset = 4007_20A8h

Bit	7	6	5	4	3	2	1	0
Read	TOKENPID				TOKENENDPT			
Write								
Reset	0	0	0	0	0	0	0	0

USBx_TOKEN field descriptions

Field	Description
7–4 TOKENPID	Contains the token type executed by the USB module. 0001 OUT Token. USB Module performs an OUT (TX) transaction. 1001 IN Token. USB Module performs an In (RX) transaction. 1101 SETUP Token. USB Module performs a SETUP (TX) transaction
TOKENENDPT	Holds the Endpoint address for the token command. The four bit value written must be a valid endpoint.

54.5.20 SOF Threshold register (USBx_SOFTHLD)

The SOF Threshold Register is used only in Host mode (CTL[HOSTMODEEN]=1). When in Host mode, the 14-bit SOF counter counts the interval between SOF frames. The SOF must be transmitted every 1ms so therefore the SOF counter is loaded with a value of 12000. When the SOF counter reaches zero, a Start Of Frame (SOF) token is transmitted.

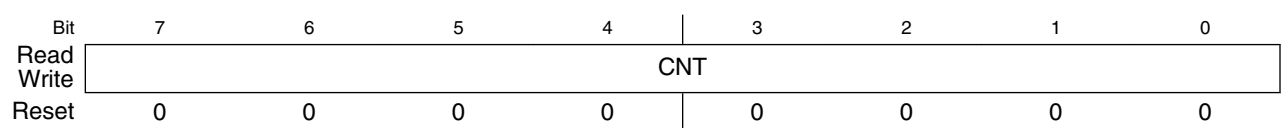
The SOF threshold register is used to program the number of USB byte times when SOFDYNTHLD=0, or 8 byte times when SOFDYNTHLD=1, before the SOF stops initiating token packet transactions. This register must be set to a value that ensures that other packets are not actively being transmitted when the SOF time counts to zero. When the SOF counter reaches the threshold value, no more tokens are transmitted until after the SOF has been transmitted.

The value programmed into the threshold register must reserve enough time to ensure the worst case transaction completes. In general the worst case transaction is an IN token followed by a data packet from the peripheral device followed by the response from the host. The actual time required is a function of the maximum packet size on the bus.

Typical values for the SOF threshold are:

- 64-byte packets=74;
- 32-byte packets=42;
- 16-byte packets=26;
- 8-byte packets=18.

Address: 4007_2000h base + ACh offset = 4007_20ACh



USBx_SOFTHLD field descriptions

Field	Description
CNT	Represents the SOF count threshold in byte times when SOFDYNTHLD=0 or 8 byte times when SOFDYNTHLD=1.

54.5.21 BDT Page Register 2 (USBx_BDTPAGE2)

Contains an 8-bit value used to compute the address where the current Buffer Descriptor Table (BDT) resides in system memory. See Buffer Descriptor Table.

Address: 4007_2000h base + B0h offset = 4007_20B0h

Bit	7	6	5	4	3	2	1	0
Read Write	BDTBA							
Reset	0	0	0	0	0	0	0	0

USBx_BDTPAGE2 field descriptions

Field	Description
BDTBA	Provides address bits 23 through 16 of the BDT base address that defines the location of Buffer Descriptor Table resides in system memory.

54.5.22 BDT Page Register 3 (USBx_BDTPAGE3)

Contains an 8-bit value used to compute the address where the current Buffer Descriptor Table (BDT) resides in system memory. See Buffer Descriptor Table.

Address: 4007_2000h base + B4h offset = 4007_20B4h

Bit	7	6	5	4	3	2	1	0
Read Write	BDTBA							
Reset	0	0	0	0	0	0	0	0

USBx_BDTPAGE3 field descriptions

Field	Description
BDTBA	Provides address bits 31 through 24 of the BDT base address that defines the location of Buffer Descriptor Table resides in system memory.

54.5.23 Endpoint Control register (USB*x*_ENDPT*n*)

Contains the endpoint control bits for each of the 16 endpoints available within the USB module for a decoded address. The format for these registers is shown in the following figure. Endpoint 0 (ENDPT0) is associated with control pipe 0, which is required for all USB functions. Therefore, after a USBRST interrupt occurs the processor core should set ENDPT0 to contain 0x0D.

In Host mode ENDPT0 is used to determine the handshake, retry and low speed characteristics of the host transfer. For Control, Bulk and Interrupt transfers, the EPHSHK bit should be 1. For Isochronous transfers it should be 0. Common values to use for ENDPT0 in host mode are 0x4D for Control, Bulk, and Interrupt transfers, and 0x4C for Isochronous transfers.

The three bits EPCTLDIS, EPRXEN, and EPTXEN define if an endpoint is enabled and define the direction of the endpoint. The endpoint enable/direction control is defined in the following table.

Table 54-7. Endpoint enable and direction control

EPCTLDIS	EPRXEN	EPTXEN	Endpoint enable/direction control
X	0	0	Disable endpoint
X	0	1	Enable endpoint for Tx transfers only
X	1	0	Enable endpoint for Rx transfers only
1	1	1	Enable endpoint for Rx and Tx transfers
0	1	1	Enable Endpoint for RX and TX as well as control (SETUP) transfers.

Address: 4007_2000h base + C0h offset + (4d × i), where i=0d to 15d

Bit	7	6	5	4	3	2	1	0
Read	HOSTWOHUB	RETRYDIS	0	EPCTLDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Write								
Reset	0	0	0	0	0	0	0	0

USB*x*_ENDPT*n* field descriptions

Field	Description
7 HOSTWOHUB	Host without a hub This is a Host mode only field and is present in the control register for endpoint 0 (ENDPT0) only.

Table continues on the next page...

USBx_ENDPTn field descriptions (continued)

Field	Description
	0 Low-speed device connected to Host through a hub. PRE_PID will be generated as required. 1 Low-speed device directly connected. No hub, or no low-speed device attached.
6 RETRYDIS	This is a Host mode only bit and is present in the control register for endpoint 0 (ENDPT0) only. When set this bit causes the host to not retry NAK'ed (Negative Acknowledgement) transactions. When a transaction is NAKed, the BDT PID field is updated with the NAK PID, and the TOKEN_DNE interrupt is set. When this bit is cleared, NAKed transactions are retried in hardware. This bit must be set when the host is attempting to poll an interrupt endpoint.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 EPCTLDIS	This bit, when set, disables control (SETUP) transfers. When cleared, control transfers are enabled. This applies if and only if the EPRXEN and EPTXEN bits are also set. See Table 54-7
3 EPRXEN	This bit, when set, enables the endpoint for RX transfers. See Table 54-7
2 EPTXEN	This bit, when set, enables the endpoint for TX transfers. See Table 54-7
1 EPSTALL	When set, this bit indicates that the endpoint is stalled. This bit has priority over all other control bits in this register, but it is only valid if EPTXEN=1 or EPRXEN=1. Any access to this endpoint causes the USB Module to return a STALL handshake. After an endpoint is stalled it requires intervention from the Host Controller.
0 EPHSHK	When set this bit enables an endpoint to perform handshaking during a transaction to this endpoint. This bit is generally 1 unless the endpoint is Isochronous.

54.5.24 USB Control register (USBx_USBCTRL)

Address: 4007_2000h base + 100h offset = 4007_2100h

Bit	7	6	5	4	3	2	1	0
Read	SUSP	PDE	UARTCHLS	UARTSEL	0			
Write								
Reset	1	1	0	0	0	0	0	0

USBx_USBCTRL field descriptions

Field	Description
7 SUSP	Places the USB transceiver into the suspend state. 0 USB transceiver is not in suspend state. 1 USB transceiver is in suspend state.
6 PDE	Enables the weak pulldowns on the USB transceiver. 0 Weak pulldowns are disabled on D+ and D–. 1 Weak pulldowns are enabled on D+ and D–.
5 UARTCHLS	UART Signal Channel Select This field is valid only when USB signals are selected to be used as UART signals.

Table continues on the next page...

USBx_USBCTRL field descriptions (continued)

Field	Description
	0 USB DP/DM signals used as UART TX/RX. 1 USB DP/DM signals used as UART RX/TX.
4 UARTSEL	Selects USB signals to be used as UART signals. 0 USB signals not used as UART signals. 1 USB signals used as UART signals.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

54.5.25 USB OTG Observe register (USBx_OBSERVE)

Provides visibility on the state of the pull-ups and pull-downs at the transceiver. Useful when interfacing to an external OTG control module via a serial interface.

Address: 4007_2000h base + 104h offset = 4007_2104h

Bit	7	6	5	4	3	2	1	0
Read	DPPU	DPPD	0	DMPD	0			
Write								
Reset	0	1	0	1	0	0	0	0

USBx_OBSERVE field descriptions

Field	Description
7 DPPU	Provides observability of the D+ Pullup enable at the USB transceiver. 0 D+ pullup disabled. 1 D+ pullup enabled.
6 DPPD	Provides observability of the D+ Pulldown enable at the USB transceiver. 0 D+ pulldown disabled. 1 D+ pulldown enabled.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 DMPD	Provides observability of the D- Pulldown enable at the USB transceiver. 0 D– pulldown disabled. 1 D– pulldown enabled.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

54.5.26 USB OTG Control register (USBx_CONTROL)

Address: 4007_2000h base + 108h offset = 4007_2108h

Bit	7	6	5	4
Read	0			DPPULLUPNONOTG
Write				
Reset	0	0	0	0

Bit	3	2	1	0
Read	0			
Write				
Reset	0	0	0	0

USBx_CONTROL field descriptions

Field	Description
7–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 DPPULLUPNONOTG	Provides control of the DP Pullup in USBOTG, if USB is configured in non-OTG device mode. 0 DP Pullup in non-OTG device mode is not enabled. 1 DP Pullup in non-OTG device mode is enabled.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

54.5.27 USB Transceiver Control register 0 (USBx_USBTRC0)

Includes signals for basic operation of the on-chip USB Full Speed transceiver and configuration of the USB data connection that are not otherwise included in the USB Full Speed controller registers. VREGIN interrupt detection using the VFEDG_DET and VREDG_DET bitfields may be used for VBUS detection in bus-powered device use cases when the USB receptacle VBUS pin is connected to VREGIN.

Address: 4007_2000h base + 10Ch offset = 4007_210Ch

Bit	7	6	5	4
Read		0	USBRESMEN	VFEDG_DET
Write	USBRESET			
Reset	0	0	0	0

Bit	3	2	1	0
Read	VREDG_DET	USB_CLK_ RECOVERY_INT	SYNC_DET	USB_RESUME_INT
Write				
Reset	0	0	0	0

USBx_USBTRC0 field descriptions

Field	Description
7 USBRESET	USB Reset Generates a hard reset to USBOTG. After this bit is set and the reset occurs, this bit is automatically cleared. **NOTE: This bit is always read as zero. Wait two USB clock cycles after setting this bit before accessing other USB register bit fields.** 0 Normal USB module operation. 1 Returns the USB module to its reset state.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 USBRESMEN	Asynchronous Resume Interrupt Enable This bit, when set, allows the USB module to send an asynchronous wakeup event to the MCU upon detection of resume signaling on the USB bus. The MCU then re-enables clocks to the USB module. It is used for low-power suspend mode when USB module clocks are stopped or the USB transceiver is in Suspend mode. Async wakeup only works in device mode. 0 USB asynchronous wakeup from suspend mode disabled. 1 USB asynchronous wakeup from suspend mode enabled. The asynchronous resume interrupt differs from the synchronous resume interrupt in that it asynchronously detects K-state using the unfiltered state of the D+ and D– pins. This interrupt should only be enabled when the Transceiver is suspended.
4 VFEDG_DET	VREGIN Falling Edge Interrupt Detect Use USB*x*_MISCCTRL[VFEDG_EN] to enable this bitfield. 0 VREGIN falling edge interrupt has not been detected. 1 VREGIN falling edge interrupt has been detected.
3 VREDG_DET	VREGIN Rising Edge Interrupt Detect Use USB*x*_MISCCTRL[VREDG_EN] to enable this bitfield. 0 VREGIN rising edge interrupt has not been detected. 1 VREGIN rising edge interrupt has been detected.
2 USB_CLK_ RECOVERY_INT	Combined USB Clock Recovery interrupt status This read-only field will be set to value high at 1'b1 when any of USB clock recovery interrupt conditions are detected and those interrupts are unmasked. For customer use the only unmasked USB clock recovery interrupt condition results from an overflow of the frequency trim setting values indicating that the frequency trim calculated is out of the adjustment range of the IRC48M output clock. To clear this bit after it has been set, Write 0xFF to register USB_CLK_RECOVER_INT_STATUS.
1 SYNC_DET	Synchronous USB Interrupt Detect 0 Synchronous interrupt has not been detected. 1 Synchronous interrupt has been detected.
0 USB_RESUME_ INT	USB Asynchronous Interrupt 0 No interrupt was generated. 1 Interrupt was generated because of the USB asynchronous interrupt.

54.5.28 Frame Adjust Register (USBx_USBFRMADJUST)

Address: 4007_2000h base + 114h offset = 4007_2114h

Bit	7	6	5	4	3	2	1	0
Read Write	ADJ							
Reset	0	0	0	0	0	0	0	0

USBx_USBFRMADJUST field descriptions

Field	Description
ADJ	Frame Adjustment In Host mode, the frame adjustment is a twos complement number that adjusts the period of each USB frame in 12-MHz clock periods. A SOF is normally generated every 12,000 12-MHz clock cycles. The Frame Adjust Register can adjust this by -128 to +127 to compensate for inaccuracies in the USB 48-MHz clock. Changes to the ADJ bit take effect at the start of the next frame.

54.5.29 Miscellaneous Control register (USBx_MISCCTRL)

Address: 4007_2000h base + 12Ch offset = 4007_212Ch

Bit	7	6	5	4
Read	0			VFEDG_EN
Write				
Reset	0	0	0	0

Bit	3	2	1	0
Read Write	VREDG_EN	OWNERRISODIS	SOFBUSSET	SOFDYNTHLD
Reset	0	0	0	0

USBx_MISCCTRL field descriptions

Field	Description
7–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 VFEDG_EN	VREGIN Falling Edge Interrupt Enable 0 VREGIN falling edge interrupt disabled. 1 VREGIN falling edge interrupt enabled.
3 VREDG_EN	VREGIN Rising Edge Interrupt Enable 0 VREGIN rising edge interrupt disabled. 1 VREGIN rising edge interrupt enabled.
2 OWNERRISODIS	OWN Error Detect for ISO IN / ISO OUT Disable This field is only valid for Peripheral mode, that is, CTL[HOSTMODEEN]=0.

Table continues on the next page...

USBx_MISCCTRL field descriptions (continued)

Field	Description
	0 OWN error detect for ISO IN / ISO OUT is not disabled. 1 OWN error detect for ISO IN / ISO OUT is disabled.
1 SOFBUSSET	SOF_TOK Interrupt Generation Mode Select This field is only valid for Host mode, that is, CTL[HOSTMODEEN]=1. 0 SOF_TOK interrupt is set according to SOF threshold value. 1 SOF_TOK interrupt is set when SOF counter reaches 0.
0 SOFDYNTHLD	Dynamic SOF Threshold Compare mode This field is only valid for Host mode, that is, CTL[HOSTMODEEN]=1. 0 SOF_TOK interrupt is set when byte times SOF threshold is reached. 1 SOF_TOK interrupt is set when 8 byte times SOF threshold is reached or overstepped.

54.5.30 USB Clock recovery control (USBx_CLK_RECOVER_CTRL)

Signals in this register control the crystal-less USB clock mode in which the internal IRC48M oscillator is tuned to match the clock extracted from the incoming USB data stream.

The IRC48M internal oscillator module must be enabled in register USB_CLK_RECOVER_IRC_EN for this mode.

Address: 4007_2000h base + 140h offset = 4007_2140h

Bit	7	6	5	4	3	2	1	0
Read Write	CLOCK_ RECOVER_ EN	RESET_ RESUME_ ROUGH_EN	RESTART_ IFRTRIM_ EN	Reserved		Reserved	Reserved	Reserved
Reset	0	0	0	0	0	0	0	0

USBx_CLK_RECOVER_CTRL field descriptions

Field	Description
7 CLOCK_ RECOVER_EN	Crystal-less USB enable This bit must be enabled if user wants to use the crystal-less USB mode for the Full Speed USB controller and transceiver. **NOTE: This bit should not be set for USB host mode or OTG.** 0 Disable clock recovery block (default) 1 Enable clock recovery block
6 RESET_ RESUME_ ROUGH_EN	Reset/resume to rough phase enable The clock recovery block tracks the IRC48M to get an accurate 48Mhz clock. It has two phases after user enables clock_recover_en bit, rough phase and tracking phase. The step to fine tune the IRC48M by

Table continues on the next page...

USBx_CLK_RECOVER_CTRL field descriptions (continued)

Field	Description
	adjusting the trim fine value is different during these 2 phases. The step in rough phase is larger than that in tracking phase. Switch back to rough stage whenever USB bus reset or bus resume occurs. 0 Always works in tracking phase after the first time rough to track transition (default) 1 Go back to rough stage whenever bus reset or bus resume occurs
5 RESTART_ IFRTRIM_EN	Restart from IFR trim value IRC48M has a default trim fine value whose default value is factory trimmed (the IFR trim value). Clock recover block tracks the accuracy of the clock 48Mhz and keeps updating the trim fine value accordingly 0 Trim fine adjustment always works based on the previous updated trim fine value (default) 1 Trim fine restarts from the IFR trim value whenever bus_reset/bus_resume is detected or module enable is desasserted
4–3 Reserved	This field is reserved.
2 Reserved	This field is reserved. This bit is for Freescale use only. Customers should not change this bit from its default state.
1 Reserved	This field is reserved. This bit is for Freescale use only. Customers should not change this bit from its default state.
0 Reserved	This field is reserved. Default should not be changed

54.5.31 IRC48M oscillator enable register (USBx_CLK_RECOVER_IRC_EN)

Controls basic operation of the on-chip IRC48M module used to produce nominal 48MHz clocks for USB crystal-less operation and other functions.

See additional information about the IRC48M operation in the Clock Distribution chapter.

Address: 4007_2000h base + 144h offset = 4007_2144h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved						IRC_EN	REG_EN
Reset	0	0	0	0	0	0	0	1

USBx_CLK_RECOVER_IRC_EN field descriptions

Field	Description
7–2 Reserved	This field is reserved.
1 IRC_EN	IRC48M enable This bit is used to enable the on-chip IRC48M module to generate clocks for crystal-less USB. It can be used for FS USB device mode operation. This bit must be set before using the crystal-less USB clock configuration.

Table continues on the next page...

USBx_CLK_RECOVER_IRC_EN field descriptions (continued)

Field	Description
	0 Disable the IRC48M module (default) 1 Enable the IRC48M module
0 REG_EN	IRC48M regulator enable This bit is used to enable the local analog regulator for IRC48M module. This bit must be set if user wants to use the crystal-less USB clock configuration. 0 IRC48M local regulator is disabled 1 IRC48M local regulator is enabled (default)

54.5.32 Clock recovery combined interrupt enable (USBx_CLK_RECOVER_INT_EN)

Enables or masks the individual interrupt flags which are logically OR'ed together to produce the combined interrupt indication on the USB_CLK_RECOVERY_INT bit in the USB_USBTRC0 register if the indicated conditions have been detected in the USB clock recovery algorithm operation.

Address: 4007_2000h base + 154h offset = 4007_2154h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved			OVF_ ERROR_EN	Reserved			
Reset	0	0	0	1	0	0	0	0

USBx_CLK_RECOVER_INT_EN field descriptions

Field	Description
7–5 Reserved	This field is reserved. Should always be written as 0.
4 OVF_ERROR_ EN	Determines whether OVF_ERROR condition signal is used in generation of USB_CLK_RECOVERY_INT. 0 The interrupt will be masked 1 The interrupt will be enabled (default)
Reserved	This field is reserved. Should always be written as 0.

54.5.33 Clock recovery separated interrupt status (USBx_CLK_RECOVER_INT_STATUS)

A Write operation with value high at 1'b1 on any combination of individual bits will clear those bits.

Address: 4007_2000h base + 15Ch offset = 4007_215Ch

Bit	7	6	5	4	3	2	1	0
Read	Reserved			OVF_ERROR	Reserved			
Write	w1c			w1c	w1c			
Reset	0	0	0	0	0	0	0	0

USBx_CLK_RECOVER_INT_STATUS field descriptions

Field	Description
7–5 Reserved	This field is reserved. Should always be written as 0.
4 OVF_ERROR	Indicates that the USB clock recovery algorithm has detected that the frequency trim adjustment needed for the IRC48M output clock is outside the available TRIM_FINE adjustment range for the IRC48M module. 0 No interrupt is reported 1 Unmasked interrupt has been generated
Reserved	This field is reserved. Should always be written as 0.

54.6 OTG and Host mode operation

The Host mode logic allows portable, mobile, and other devices using this SOC to function as a USB Embedded Host (EH) Controller. The OTG logic adds an interface to allow the OTG Host Negotiation and Session Request Protocols (HNP and SRP) to be implemented in software.

Host mode is intended for use in handheld-portable devices to allow easy connection to simple HID class devices such as printers and keyboards. It is not intended to perform the functions of a full OHCI or UHCI compatible host controller found on PC motherboards. Host mode allows bulk, isochronous, interrupt and control transfers. Bulk data transfers are performed at nearly the full USB interface bandwidth. Support is provided for ISO

transfers, but the number of ISO streams that can be practically supported is affected by the interrupt latency of the processor servicing the Token Done interrupts from the SIE. Custom drivers must be written to support Host mode operation.

Setting the HOST_MODE_EN bit in the CTL register enables Host mode. The USB-FS core can only operate as a peripheral device or in Host mode. It cannot operate in both modes simultaneously. When HOST_MODE is enabled, only endpoint zero is used. All other endpoints should be disabled by software.

54.7 Host Mode Operation Examples

The following sections illustrate the steps required to perform USB host functions using the USB-FS core. For more information about these procedures, see the *Universal Serial Bus Specification, Revision 2.0*, "Chapter 9 USB Device Framework."

To enable host mode and discover a connected device:

1. Enable Host Mode (CTL[HOST_MODE_EN]=1). The pull-down resistors are enabled, and pull-up disabled. Start of Frame (SOF) generation begins. SOF counter loaded with 12,000. Disable SOF packet generation to eliminate noise on the USB by writing the USB enable bit to 0 (CTL[USB_EN]=0).
2. Enable the ATTACH interrupt (INTEN[ATTACHEN]=1).
3. Wait for ATTACH interrupt (ISTAT[ATTACH]). Signaled by USB peripheral device pull-up resistor changing the state of DPLUS or DMINUS from 0 to 1 (SE0 to J or K state).
4. Check the state of the JSTATE and SE0 bits in the control register. If the connecting device is low speed (JSTATE bit is 0), set the low-speed bit in the address registers (ADDR[LS_EN]=1) and the Host Without Hub bit in endpoint 0 register control (ENDPT0[HOSTWOHUB]=1).
5. Enable RESET (CTL[RESET]=1) for 10 ms.
6. Enable SOF packet to keep the connected device from going to suspend (CTL[USB_EN=1]).
7. Enumerate the attached device by sending the appropriate commands to the default control pipe of the connected device.

To complete a control transaction to a connected device:

1. Complete all the steps to discover a connected device

2. Set up the endpoint control register for bidirectional control transfers ENDPT0[4:0] = 0x0d.
3. Place a copy of the device framework setup command in a memory buffer.
4. Initialize current even or odd TX EP0 BDT to transfer the 8 bytes of command data for a device framework command (for example, a GET DEVICE DESCRIPTOR).
   - Set the BDT command word to 0x00080080 –Byte count to 8, OWN bit to 1.
   - Set the BDT buffer address field to the start address of the 8 byte command buffer.
5. Set the USB device address of the peripheral device in the address register (ADDR[6:0]). After the USB bus reset, the device USB address is zero. It is set to some other value usually 1 by the Set Address device framework command.
6. Write the TOKEN register with a SETUP to Endpoint 0, the peripheral device default control pipe (TOKEN=0xD0). This initiates a setup token on the bus followed by a data packet. The device handshake is returned in the BDT PID field after the packets complete. When the BDT is written, a Token Done (ISTAT[TOKDNE]) interrupt is asserted. This completes the setup phase of the setup transaction.
7. To initiate the data phase of the setup transaction (that is, get the data for the GET DEVICE DESCRIPTOR command), set up a buffer in memory for the data to be transferred.
8. Initialize the current even or odd TX EP0 BDT to transfer the data.
   - Set the BDT command word to 0x004000C0 – BC to 64 (the byte count of the data buffer in this case), OWN bit to 1, Data toggle to Data1.
   - Set the BDT buffer address field to the start address of the data buffer
9. Write the TOKEN register with an IN or OUT token to Endpoint 0, the peripheral device default control pipe, an IN token for a GET DEVICE DESCRIPTOR command (TOKEN=0x90). This initiates an IN token on the bus followed by a data packet from the device to the host. When the data packet completes, the BDT is written and a Token Done (ISTAT[DNE]) interrupt is asserted. For control transfers with a single packet data phase this completes the data phase of the setup transaction.
10. To initiate the status phase of the setup transaction, set up a buffer in memory to receive or send the zero length status phase data packet.
11. Initialize the current even or odd TX EP0 BDT to transfer the status data.

- Set the BDT command word to 0x00000080 – BC to 0 (the byte count of the data buffer in this case), OWN bit to 1, Data toggle to Data1.
- Set the BDT buffer address field to the start address of the data buffer

12. Write the TOKEN register with a IN or OUT token to Endpoint 0, the peripheral device default control pipe, an OUT token for a GET DEVICE DESCRIPTOR command (TOKEN=0x10). This initiates an OUT token on the bus followed by a zero length data packet from the host to the device. When the data packet completes, the BDT is written with the handshake from the device and a Token Done (ISTAT[TOKDNE]) interrupt is asserted. This completes the data phase of the setup transaction.

To send a full speed bulk data transfer to a peripheral device:

1. Complete all steps to discover a connected device and to configure a connected device. Write the ADDR register with the address of the peripheral device. Typically, there is only one other device on the USB bus in host mode so it is expected that the address is 0x01 and should remain constant.
2. Write 0x1D to ENDPT0 register to enable transmit and receive transfers with handshaking enabled.
3. Setup the even TX EP0 BDT to transfer up to 64 bytes.
4. Set the USB device address of the peripheral device in the address register (ADDR[6:0]).
5. Write the TOKEN register with an OUT token to the desired endpoint. The write to this register triggers the USB-FS transmit state machines to begin transmitting the token and the data.
6. Setup the odd TX EP0 BDT to transfer up to 64 bytes.
7. Write the TOKEN register with an OUT token as in step 4. Two tokens can be queued at a time to allow the packets to be double buffered to achieve maximum throughput.
8. Wait for the TOKDNE interrupt. This indicates that one of the BDTs has been released back to the processor and the transfer has completed. If the peripheral device asserts NAKs, the USB-FS continues to retry the transfer indefinitely without processor intervention unless the ENDPT0[RETRYDIS] is 1. If the retry disable field is set, the handshake (ACK, NAK, STALL, or ERROR (0xf)) is returned in the BDT

PID field. If a stall interrupt occurs, the pending packet must be dequeued and the error condition in the peripheral device cleared. If a Reset interrupt occurs (SE0 for more than 2.5 µs), the peripheral device has detached.

9. After the TOK_DNE interrupt occurs, the BDTs can be examined and the next data packet queued by returning to step 2.

54.8 On-The-Go operation

The USB-OTG core provides sensors and controls to enable On-The-Go (OTG) operation. These sensors are used by the OTG driver software to implement the Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) and give access to the OTG protocol control signals. The following state machines show the OTG operations involved with HNP and SRP protocols from either end of the USB cable.

54.8.1 OTG dual role A device operation

A device is considered the A device because of the type of cable attached. If the USB Type Standard-A or Micro-A plug is plugged into the device, it is considered the A device.

A dual role A device operates as the following flow diagram and state description table illustrates.

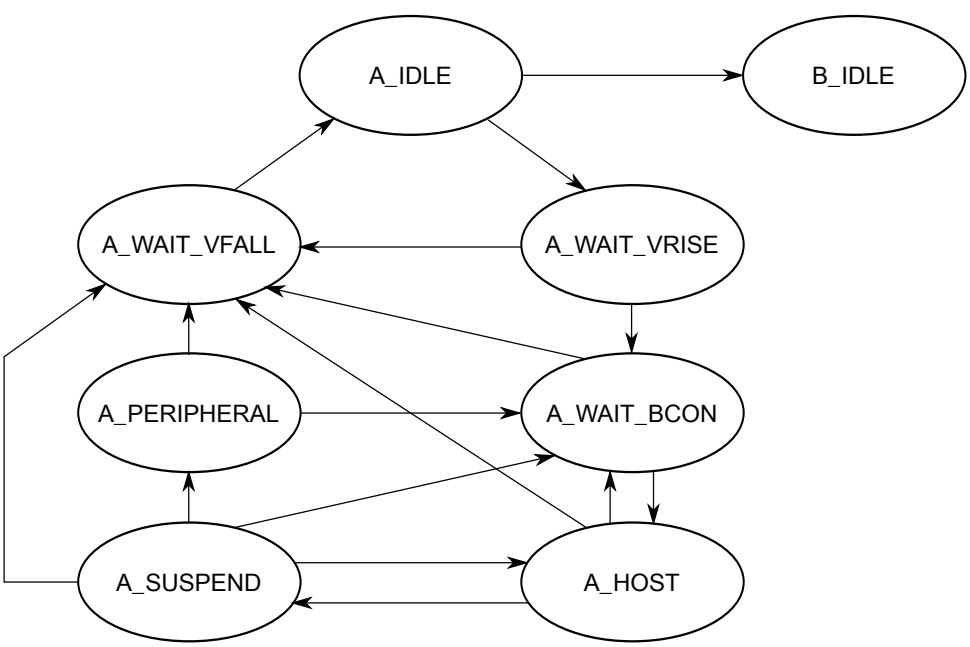


Figure 54-12. Dual role A device flow diagram

Table 54-8. State descriptions for the dual role A device flow

State	Action	Response
A_IDLE	If ID Interrupt. The cable has been unplugged or a Type B cable has been attached. The device now acts as a Type B device.	Go to B_IDLE
	If the A application wants to use the bus or if the B device is doing an SRP as indicated by an A_SESS_VLD Interrupt or Attach or Port Status Change Interrupt check data line for 5 –10 msec pulsing.	Go to A_WAIT_VRISE Turn on DRV_VBUS
A_WAIT_VRISE	If ID Interrupt or if A_VBUS_VLD is false after 100 msec The cable has been changed or the A device cannot support the current required from the B device.	Go to A_WAIT_VFALL Turn off DRV_VBUS
	If A_VBUS_VLD interrupt	Go to A_WAIT_BCON
A_WAIT_BCON	After 200 ms without Attach or ID Interrupt. (This could wait forever if desired.)	Go to A_WAIT_FALL Turn off DRV_VBUS
	A_VBUS_VLD Interrupt and B device attaches	Go to A_HOST Turn on Host mode
A_HOST	Enumerate Device determine OTG Support.	
	If A_VBUS_VLD/ Interrupt or A device is done and does not think it wants to do something soon or the B device disconnects	Go to A_WAIT_VFALL Turn off Host mode Turn off DRV_VBUS
	If the A device is finished with session or if the A device wants to allow the B device to take bus.	Go to A_SUSPEND
	ID Interrupt or the B device disconnects	Go to A_WAIT_BCON
A_SUSPEND	If ID Interrupt, or if 150 ms B disconnect timeout (This timeout value could be longer) or if A_VBUS_VLD\ Interrupt	Go to A_WAIT_VFALL Turn off DRV_VBUS
	If HNP enabled, and B disconnects in 150 ms then B device is becoming the host.	Go to A_PERIPHERAL Turn off Host mode
	If A wants to start another session	Go to A_HOST
A_PERIPHERAL	If ID Interrupt or if A_VBUS_VLD interrupt	Go to A_WAIT_VFALL Turn off DRV_VBUS.
	If 3 –200 ms of Bus Idle	Go to A_WAIT_BCON Turn on Host mode
A_WAIT_VFALL	If ID Interrupt or (A_SESS_VLD/ & b_conn/)	Go to A_IDLE

54.8.2 OTG dual role B device operation

A device is considered a B device if it is connected to the bus with a USB Type Standard-B, Mini-B, or Micro-B plug inserted into the local USB receptacle. The Type Mini-B plug and receptacle are now only allowed for dedicated peripheral devices, not dual role/OTG devices.

A dual role B device operates as the following flow diagram and state description table illustrates.

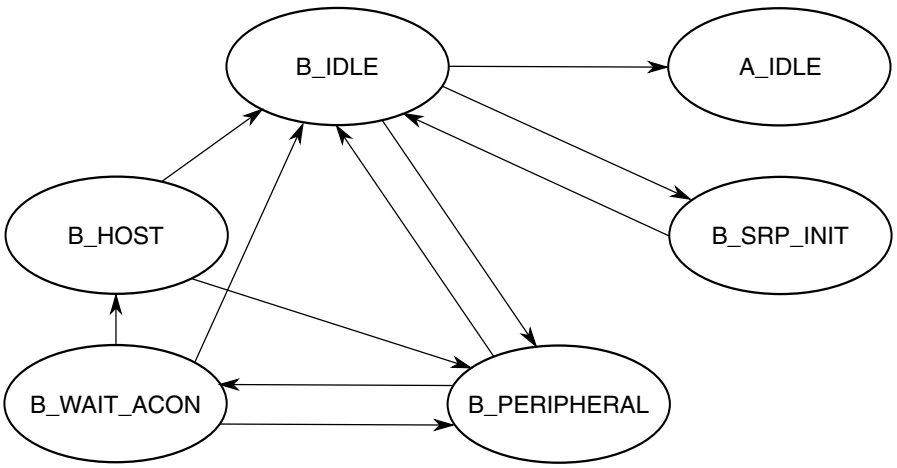


Figure 54-13. Dual role B device flow diagram

Table 54-9. State descriptions for the dual role B device flow

State	Action	Response
B_IDLE	If ID\ Interrupt. A Type A cable has been plugged in and the device should now respond as a Type A device.	Go to A_IDLE
	If B_SESS_VLD Interrupt. The A device has turned on VBUS and begins a session.	Go to B_PERIPHERAL Turn on DP_HIGH
	If B application wants the bus and Bus is Idle for 2 ms and the B_SESS_END bit is set, the B device can perform an SRP.	Go to B_SRP_INIT Pulse CHRG_VBUS Pulse DP_HIGH 5-10 ms
B_SRP_INIT	If ID\ Interrupt or SRP Done (SRP must be done in less than 100 ms.)	Go to B_IDLE
B_PERIPHERAL	If HNP enabled and the bus is suspended and B wants the bus, the B device can become the host.	Go to B_WAIT_ACON Turn off DP_HIGH
B_WAIT_ACON	If A connects, an attach interrupt is received	Go to B_HOST Turn on Host Mode
	If ID\ Interrupt or B_SESS_VLD/ Interrupt If the cable changes or if VBUS goes away, the host doesn't support us. Go to B_IDLE	Go to B_IDLE
	If 3.125 ms expires or if a Resume occurs	Go to B_PERIPHERAL
B_HOST	If ID\ Interrupt or B_SESS_VLD\ Interrupt If the cable changes or if VBUS goes away, the host doesn't support us.	Go to B_IDLE
	If B application is done or A disconnects	Go to B_PERIPHERAL

54.9 Device mode IRC48M operation

The following are the IRC48M initialization code steps:

1. Enable the IRC48M clock: USB_CLK_RECOVER_IRC_EN[IRC_EN] = 1b
2. Enable the USB clock recovery tuning: USB_CLK_RECOVER_CTRL[CLOCK_RECOVER_EN] = 1b
3. Choose the clock source of USB by configuring the muxes and dividers. The IRC48M is muxed by setting SIM_SOPT2[MCGPLLFLL]=11b for USB usage.
4. The selected mux output clock can be divided by the USB clock divider, so set these fields so no clock division is enabled. This is the equation for the divider:

   Divider output clock = Divider input clock × [(USBFRAC+1) / (USBDIV+1)].
   So set SIM_CLKDIV2[USBDIV] = 000b and SIM_CLKDIV2[USBFRAC] = 0b
5. The USB clock source must choose the output of the divided clock.

For chip-specific details, see the USB FS OTG controller clocking information in the "Clock Distribution" chapter.

Chapter 55
USB Device Charger Detection Module (USBDCD)

55.1 Preface

55.1.1 References

The following publications are referenced in this document. For updates to these specifications, see http://www.usb.org.

- *USB Battery Charging Specification Revision 1.1, USB Implementers Forum*
- *USB Battery Charging Specification (Including errata and ECNs through March 15, 2012) Revision 1.2, USB Implementers Forum*
- *Universal Serial Bus Specification Revision 2.0, USB Implementers Forum*
- *USB 2.0 Connect Timing Update ECN, USB Implementers Forum*

55.1.2 Acronyms and abbreviations

The following table contains acronyms and abbreviations used in this document.

Table 55-1. Acronyms and abbreviated terms

Term	Meaning
CDP	Charging Downstream Port, as defined in *USB Battery Charging Specification, Rev. 1.2*
Charging Port	A Charging Port supported by this module is either a CDP or a DCP
DCP	Dedicated Charging Port, as defined in *USB Battery Charging Specification, Rev. 1.2*
FS	Full speed (12 Mbit/s)
HS	High speed (480 Mbit/s)
I_{CFG_MAX}	Current limit for a USB device attached to an SDP, after configuration
I_{DEV_CHG}	Current limit for a USB device attached to a Charging Port

Table continues on the next page...

Table 55-1. Acronyms and abbreviated terms (continued)

Term	Meaning
I_{DM_SINK}	Current sink for the D– line
I_{DP_SINK}	Current sink for the D+ line
I_{DP_SRC}	Current source for the D+ line
I_{SUSP}	Current drawn when the USB device is suspended
LDO	Low dropout
LS	Low Speed (1.5 Mbit/s)
N/A	Not applicable
OTG	On-The-Go
R_{DM_DWN}	D– pulldown resistance for data pin contact detect
SDP	Standard Downstream Port, as defined in *USB Battery Charging Specification, Rev 1.2*
V_{DAT_REF}	Data detect reference voltage for the voltage comparator
V_{DP_SRC}	Voltage source for the D+ line
V_{DM_SRC}	Voltage source for the D– line
V_{LGC}	Threshold voltage for logic high

55.1.3 Glossary

The following table shows a glossary of terms used in this document.

Table 55-2. Glossary of terms

Term	Definition
Transceiver	Module that implements the physical layer of the USB standard (FS or LS only).
PHY	Module that implements the physical layer of the USB standard (HS capable).
Attached	Device is physically plugged into USB port, but has *not enabled* either D+ or D– pullup resistor.
Connected	Device is physically plugged into USB port, and has *enabled* either D+ or D– pullup resistor.
Suspended	After 3 ms of no bus activity, the USB device enters suspend mode.
Component	The hardware and software that make up a subsystem.

55.2 Introduction

The USBDCD module works with the USB transceiver to detect whether the USB device is attached to a Charging Port, either a Dedicated Charging Port (DCP) or a Charging Downstream Port (CDP). System software coordinates the detection activites of the module and controls an off-chip integrated circuit that performs the battery charging.

55.2.1 Block diagram

The following figure is a high level block diagram of the module.

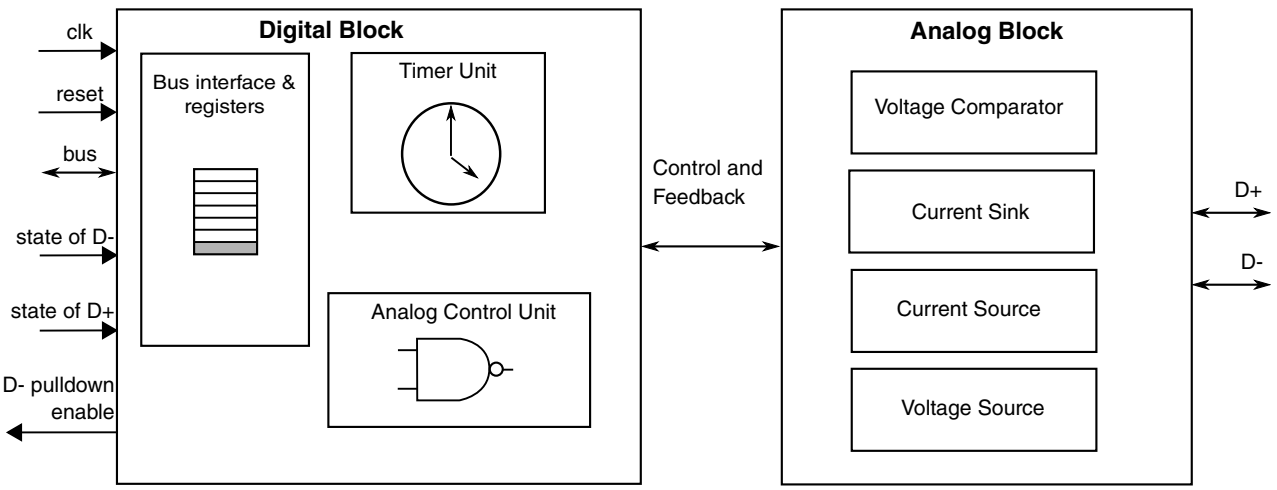


Figure 55-1. Block diagram

The USBDCD module consists of two main blocks:

- A digital block provides the programming interface (memory-mapped registers) and includes the timer unit and the analog control unit.
- An analog block provides the circuitry for the physical detection of the charger, including the voltage source, current source, current sink, and voltage comparator circuitry.

55.2.2 Features

The USBDCD module offers the following features:

- Compliant with the latest industry standard specification: *USB Battery Charging Specification, Revision 1.1 and 1.2*
- Programmable timing parameters default to values required by the industry standards:
  - Having standard default values allows for easy configuration- simply set the clock frequency before enabling the module.
  - Programmability allows the flexibility to meet future updates of the standards.

55.2.3 Modes of operation

The operating modes of the USBDCD module are shown in the following table.

Table 55-3. Module modes and their conditions

Module mode	Description	Conditions when used
Enabled	The module performs the charger detection sequence.	System software should enable the module only when *all* of the following conditions are true: • The system uses a rechargeable battery. • The device is being used in an FS USB device application. • The device has detected that it is attached to the USB cable.
Disabled	The module is not active and is held in a low power state.	System software should disable the module when *either* of the following conditions is true: • The charger detect sequence is complete. • The conditions for being enabled are not met.
Powered Off	The digital supply voltage dvdd is removed.	Low system performance requirements allow putting the device into a very low-power stop mode.

Operating mode transitions are shown in the following table.

Table 55-4. Entering and exiting module modes

Module mode	Entering	Exiting	Mode after exiting
Enabled	Set CONTROL[START].	Set CONTROL[SR].[1]	Disabled
Disabled	Take *either* of the following actions: • Set CONTROL[SR].[1] • Reset the module. By default, the module is disabled.	Set CONTROL[START].	Enabled
Powered Off	Perform the following actions: 1. Put the device into very low-power stop mode. 2. Adjust the supply voltages.	Perform the following actions: 1. Restore the supply voltages. 2. Take the device out of very low-power stop mode.	Disabled

1. The effect of setting the SR bit is immediate; that is, the module is disabled even if the sequence has not completed.

55.3 Module signal descriptions

This section describes the module signals. The following table shows a summary of module signals that interface with the pins of the device.

Table 55-5. Signal descriptions

Signal	Description	I/O
USB_DM	USB D– analog data signal. The analog block interfaces directly to the D– signal on the USB bus.	I/O
USB_DP	USB D+ analog data signal. The analog block interfaces directly to the D+ signal on the USB bus.	I/O
avdd33[1]	3.3 V regulated analog supply	I
vss_bulk	Digital/Analog ground	I
dvdd	1.2 V digital supply	I

1. Voltage must be 3.3 V +/- 10% for full functionality of the module. That is, the charger detection function does not work when this voltage is below 3.0 V, and the CONTROL[START] bit should not be set.

NOTE

The transceiver module also interfaces to the USB_DM and USB_DP signals. Both modules and the USB host/hub use these signals as bidirectional, tristate signals.

Information about the signal integrity aspects of the lines including shielding, isolated return paths, input or output impedance, packaging, suggested external components, ESD, and other protections can be found in the USB 2.0 specification and in Application information.

55.4 Memory map/Register definition

This section describes the memory map and registers for the USBDCD module.

USBDCD memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_5000	Control register (USBDCD_CONTROL)	32	R/W	0001_0000h	55.4.1/1786
4003_5004	Clock register (USBDCD_CLOCK)	32	R/W	0000_00C1h	55.4.2/1788
4003_5008	Status register (USBDCD_STATUS)	32	R	0000_0000h	55.4.3/1789
4003_500C	Signal Override Register (USBDCD_SIGNAL_OVERRIDE)	32	R/W	0000_0000h	55.4.4/1791

Table continues on the next page...

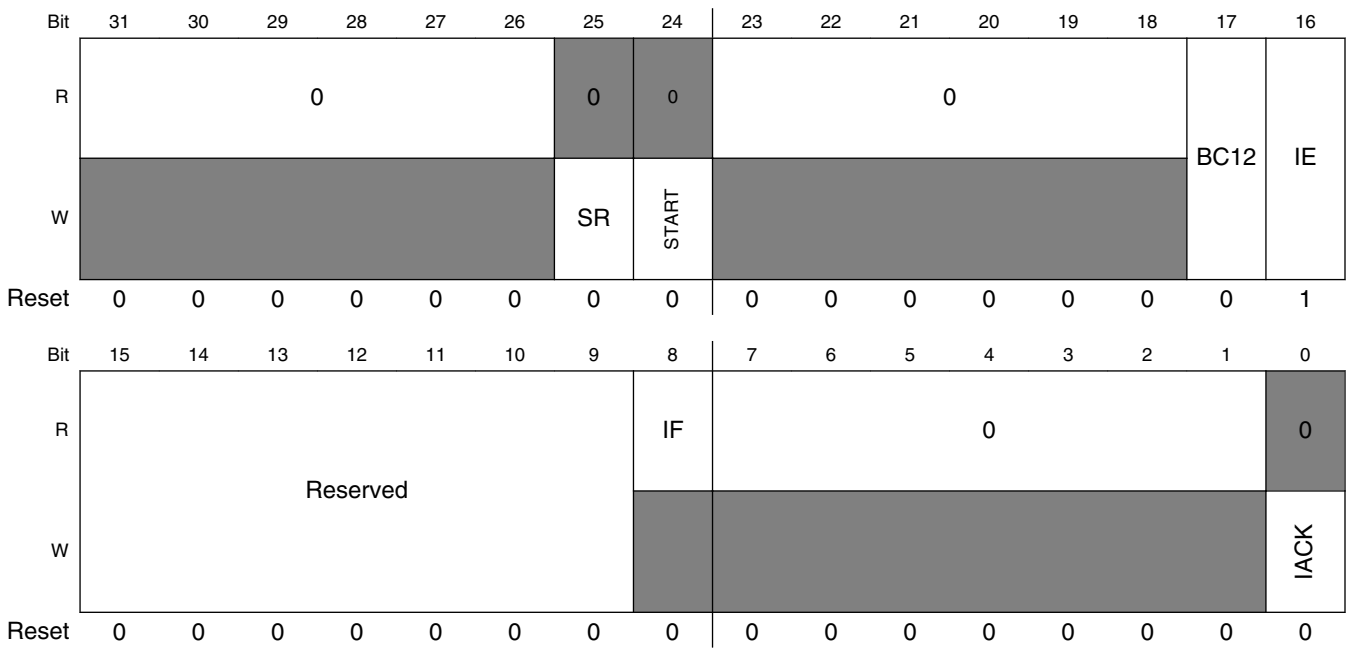
USBDCD memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_5010	TIMER0 register (USBDCD_TIMER0)	32	R/W	0010_0000h	55.4.5/1792
4003_5014	TIMER1 register (USBDCD_TIMER1)	32	R/W	000A_0028h	55.4.6/1793
4003_5018	TIMER2_BC11 register (USBDCD_TIMER2_BC11)	32	R/W	0028_0001h	55.4.7/1793
4003_5018	TIMER2_BC12 register (USBDCD_TIMER2_BC12)	32	R/W	0001_0028h	55.4.8/1794

55.4.1 Control register (USBDCD_CONTROL)

Contains the control and interrupt bit fields.

Address: 4003_5000h base + 0h offset = 4003_5000h



USBDCD_CONTROL field descriptions

Field	Description
31–26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25 SR	Software Reset This is a self-clearing field and always reads 0. Determines whether a software reset is performed. 0 Do not perform a software reset. 1 Perform a software reset.
24 START	Start Change Detection Sequence

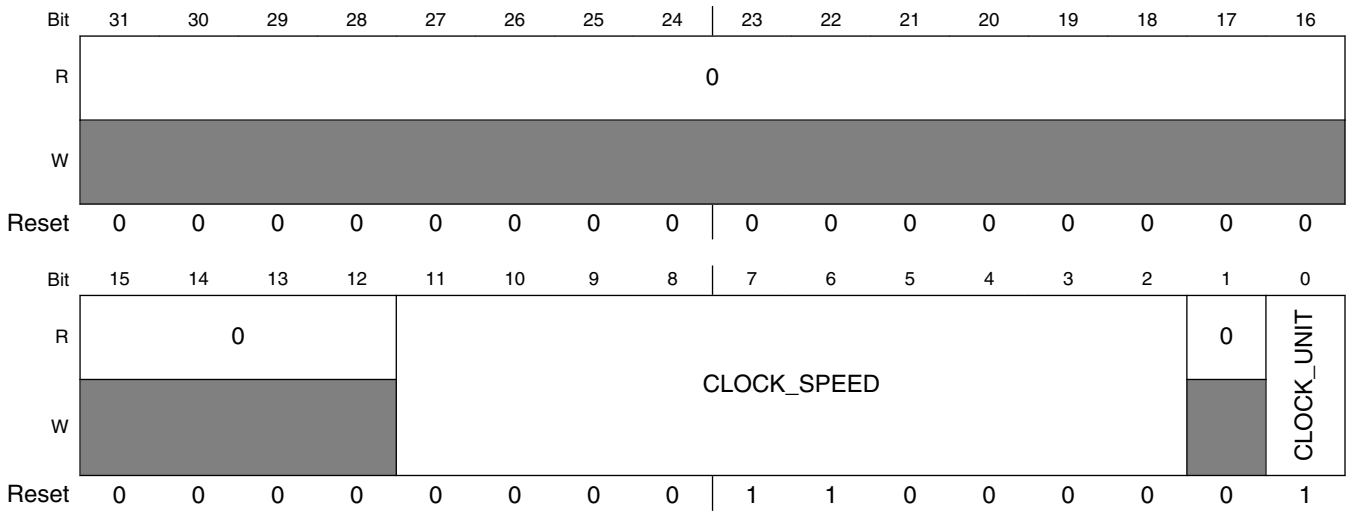
Table continues on the next page...

USBDCD_CONTROL field descriptions (continued)

Field	Description
	This is a self-clearing field and always reads 0. Determines whether the charger detection sequence is initiated. 0 Do not start the sequence. Writes of this value have no effect. 1 Initiate the charger detection sequence. If the sequence is already running, writes of this value have no effect.
23–18 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
17 BC12	BC1.2 compatibility. This bit cannot be changed after start detection. 0 Compatible with BC1.1 (default) 1 Compatible with BC1.2
16 IE	Interrupt Enable Enables/disables interrupts to the system. 0 Disable interrupts to the system. 1 Enable interrupts to the system.
15–9 Reserved	This field is reserved.
8 IF	Interrupt Flag Determines whether an interrupt is pending. 0 No interrupt is pending. 1 An interrupt is pending.
7–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 IACK	Interrupt Acknowledge This is a self-clearing field and always reads 0. Determines whether the interrupt is cleared. 0 Do not clear the interrupt. 1 Clear the IF bit (interrupt flag).

55.4.2 Clock register (USBDCD_CLOCK)

Address: 4003_5000h base + 4h offset = 4003_5004h



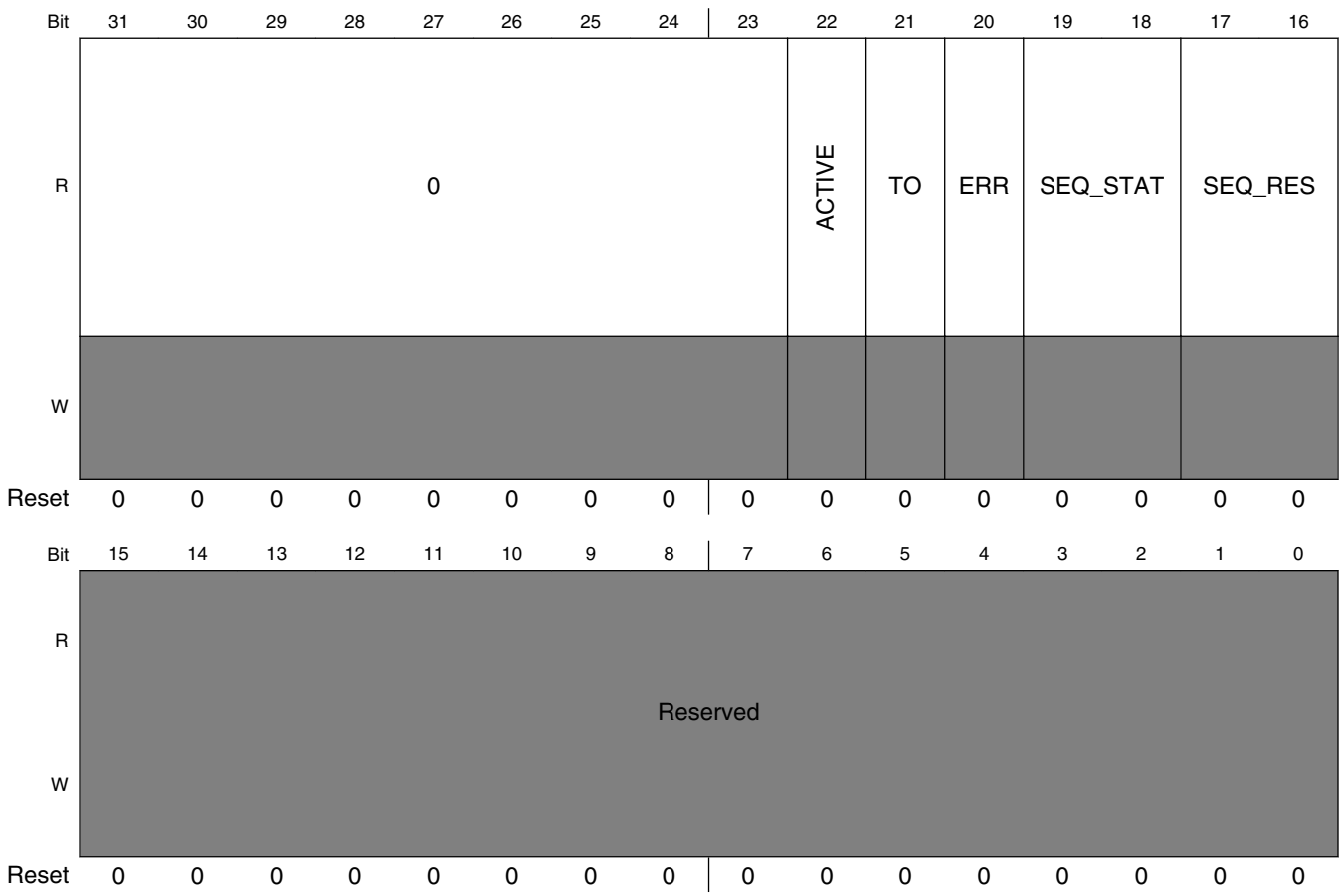
USBDCD_CLOCK field descriptions

Field	Description
31–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11–2 CLOCK_SPEED	Numerical Value of Clock Speed in Binary The unit of measure is programmed in CLOCK_UNIT. The valid range is from 1 to 1023 when clock unit is MHz and 4 to 1023 when clock unit is kHz. Examples with CLOCK_UNIT = 1: • For 48 MHz: 0b00_0011_0000 (48) (Default) • For 24 MHz: 0b00_0001_1000 (24) Examples with CLOCK_UNIT = 0: • For 100 kHz: 0b00_0110_0100 (100) • For 500 kHz: 0b01_1111_0100 (500)
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 CLOCK_UNIT	Unit of Measurement Encoding for Clock Speed Specifies the unit of measure for the clock speed. 0 kHz Speed (between 1 kHz and 1023 kHz) 1 MHz Speed (between 1 MHz and 1023 MHz)

55.4.3 Status register (USBDCD_STATUS)

Provides the current state of the module for system software monitoring.

Address: 4003_5000h base + 8h offset = 4003_5008h



USBDCD_STATUS field descriptions

Field	Description
31–23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 ACTIVE	Active Status Indicator Indicates whether the sequence is running. 0 The sequence is not running. 1 The sequence is running.
21 TO	Timeout Flag Indicates whether the detection sequence has passed the timeout threshhold.

Table continues on the next page...

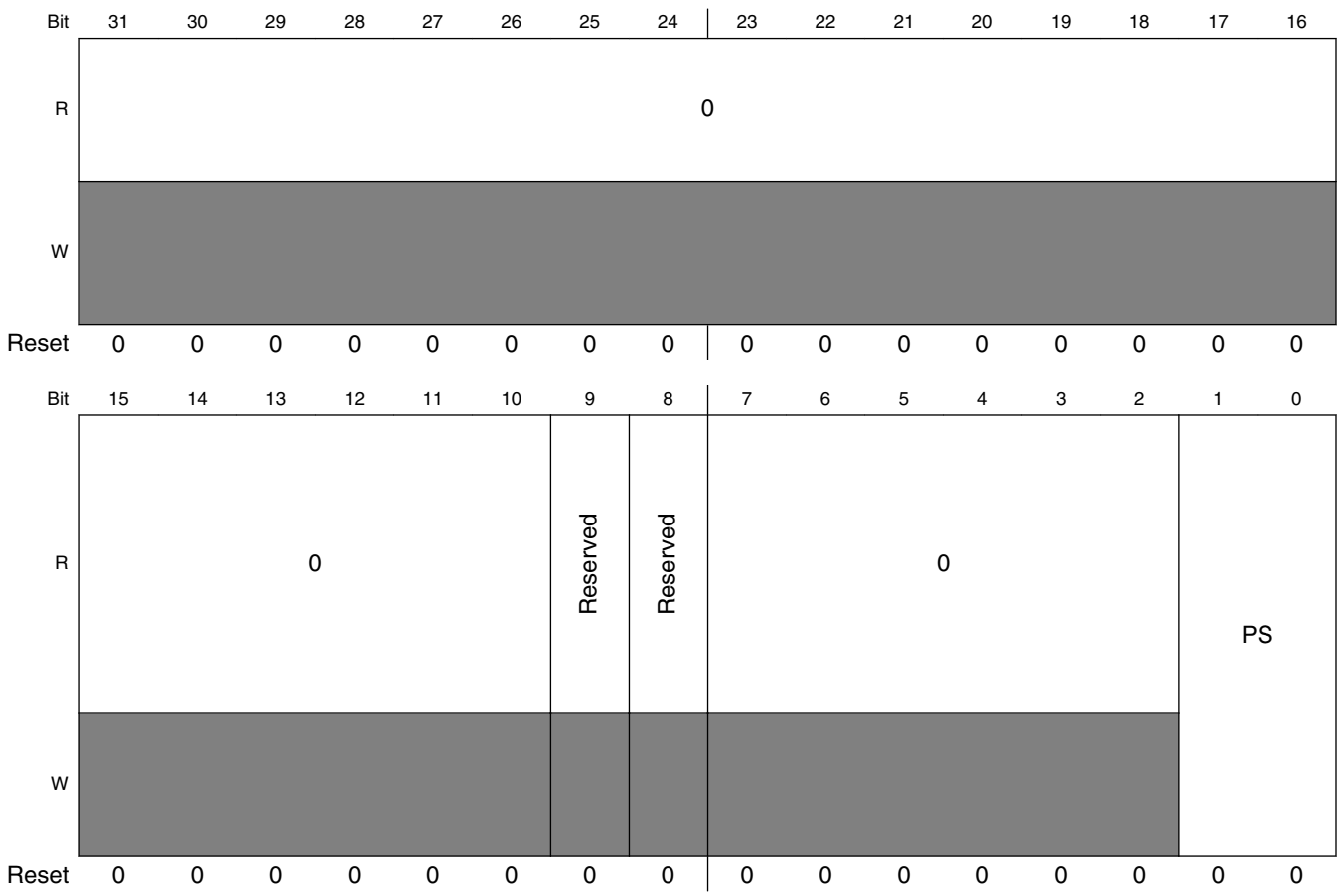
USBDCD_STATUS field descriptions (continued)

Field	Description
	0 The detection sequence has not been running for over 1 s. 1 It has been over 1 s since the data pin contact was detected and debounced.
20 ERR	Error Flag Indicates whether there is an error in the detection sequence. 0 No sequence errors. 1 Error in the detection sequence. See the SEQ_STAT field to determine the phase in which the error occurred.
19–18 SEQ_STAT	Charger Detection Sequence Status Indicates the status of the charger detection sequence. 00 The module is either not enabled, or the module is enabled but the data pins have not yet been detected. 01 Data pin contact detection is complete. 10 Charging port detection is complete. 11 Charger type detection is complete.
17–16 SEQ_RES	Charger Detection Sequence Results Reports how the charger detection is attached. 00 No results to report. 01 Attached to an SDP. Must comply with USB 2.0 by drawing only 2.5 mA (max) until connected. 10 Attached to a charging port. The exact meaning depends on bit 18: • 0: Attached to either a CDP or a DCP. The charger type detection has not completed. • 1: Attached to a CDP. The charger type detection has completed. 11 Attached to a DCP.
Reserved	This field is reserved. **NOTE:** Bits do not always read as 0.

55.4.4 Signal Override Register (USBDCD_SIGNAL_OVERRIDE)

The Signal Override register provides a way for the customer to enable signaling required by the USB BC v1.2 specification after the battery charger detection sequences have completed.

Address: 4003_5000h base + Ch offset = 4003_500Ch



USBDCD_SIGNAL_OVERRIDE field descriptions

Field	Description
31–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9 Reserved	This field is reserved. Reserved, not for customer use. The value of this bit field may change during module operation.
8 Reserved	This field is reserved. Reserved, not for customer use. The value of this bit field may change during module operation.
7–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

USBDCD_SIGNAL_OVERRIDE field descriptions (continued)

Field	Description
PS	Phase Selection Used to enable specified voltage and current source circuits on the USB_DP and USB_DM pins. Customers may set this bit field to 2'b10 for required signaling if attached to a Dedicated Charging Port, or during operation under the Dead Battery Provision. 00 No overrides. Bit field must remain at this value during normal USB data communication to prevent unexpected conditions on USB_DP and USB_DM pins. (Default) 01 Reserved, not for customer use. 10 Enables VDP_SRC voltage source for the USB_DP pin and IDM_SINK current source for the USB_DM pin. 11 Reserved, not for customer use.

55.4.5 TIMER0 register (USBDCD_TIMER0)

TIMER0 has an TSEQ_INIT field that represents the system latency in ms. Latency is measured from the time when VBUS goes active until the time system software initiates charger detection sequence in USBDCD module. When software sets the CONTROL[START] bit, the Unit Connection Timer (TUNITCON) is initialized with the value of TSEQ_INIT.

Valid values are 0–1023, however the USB Battery Charging Specification requires the entire sequence, including TSEQ_INIT, to be completed in 1s or less.

Address: 4003_5000h base + 10h offset = 4003_5010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0						TSEQ_INIT										0				TUNITCON											
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBDCD_TIMER0 field descriptions

Field	Description
31–26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25–16 TSEQ_INIT	Sequence Initiation Time TSEQ_INIT represents the system latency (in ms) measured from the time VBUS goes active to the time system software initiates the charger detection sequence in the USBDCD module. When software sets the CONTROL[START] bit, the Unit Connection Timer (TUNITCON) is initialized with the value of TSEQ_INIT. Valid values are 0-1023, but the USB Battery Charging Specification requires the entire sequence, including TSEQ_INIT, to be completed in 1s or less.
15–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
TUNITCON	Unit Connection Timer Elapse (in ms)

Table continues on the next page...

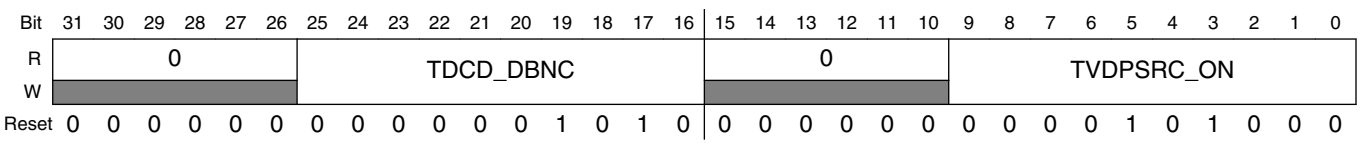
USBDCD_TIMER0 field descriptions (continued)

Field	Description
	Displays the amount of elapsed time since the event of setting the START bit plus the value of TSEQ_INIT. The timer is automatically initialized with the value of TSEQ_INIT before starting to count. This timer enables compliance with the maximum time allowed to connect T_{UNIT_CON} under the USB Battery Charging Specification. If the timer reaches the one second limit, the module triggers an interrupt and sets the error flag STATUS[ERR]. The timer continues counting throughout the charger detection sequence, even when control has been passed to software. As long as the module is active, the timer continues to count until it reaches the maximum value of 0xFFF (4095 ms). The timer does not rollover to zero. A software reset clears the timer.

55.4.6 TIMER1 register (USBDCD_TIMER1)

TIMER1 contains timing parameters. Note that register values can be written that are not compliant with the USB Battery Charging Specification, so care should be taken when overwriting the default values.

Address: 4003_5000h base + 14h offset = 4003_5014h



USBDCD_TIMER1 field descriptions

Field	Description
31–26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25–16 TDCD_DBNC	Time Period to Debounce D+ Signal Sets the time period (ms) to debounce the D+ signal during the data pin contact detection phase. See "Debouncing the data pin contact" Valid values are 1–1023, but the USB Battery Charging Specification requires a minimum value of 10 ms.
15–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
TVDPSRC_ON	Time Period Comparator Enabled This timing parameter is used after detection of the data pin. See "Charging Port Detection". Valid values are 1–1023, but the USB Battery Charging Specification requires a minimum value of 40 ms.

55.4.7 TIMER2_BC11 register (USBDCD_TIMER2_BC11)

TIMER2_BC11 contains timing parameters for USB Battery Charging Specification, v1.1.

NOTE

Register values can be written that are not compliant with the USB Battery Charging Specification, so care should be taken when overwriting the default values.

Address: 4003_5000h base + 18h offset = 4003_5018h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0						TVDPSRC_CON										0												CHECK_DM			
W																																
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

USBDCD_TIMER2_BC11 field descriptions

Field	Description
31–26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25–16 TVDPSRC_CON	Time Period Before Enabling D+ Pullup Sets the time period (ms) that the module waits after charging port detection before system software must enable the D+ pullup to connect to the USB host. Valid values are 1–1023, but the USB Battery Charging Specification requires a minimum value of 40 ms.
15–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CHECK_DM	Time Before Check of D– Line Sets the amount of time (in ms) that the module waits after the device connects to the USB bus until checking the state of the D– line to determine the type of charging port. See "Charger Type Detection." Valid values are 1–15ms.

55.4.8 TIMER2_BC12 register (USBDCD_TIMER2_BC12)

TIMER2_BC12 contains timing parameters for USB Battery Charging Specification, v1.2.

NOTE

Register values can be written that are not compliant with the USB Battery Charging Specification, so care should be taken when overwriting the default values.

Address: 4003_5000h base + 18h offset = 4003_5018h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0						TWAIT_AFTER_PRD										0						TVDMSRC_ON									
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0

USBDCD_TIMER2_BC12 field descriptions

Field	Description
31–26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25–16 TWAIT_AFTER_PRD	Sets the amount of time (in ms) that the module waits after primary detection before start to secondary detection. Valid values are 1–1023ms. Default is 1ms.
15–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
TVDMSRC_ON	Sets the amount of time (in ms) that the module enables the V_{DM_SRC}. Valid values are 0–40ms.

55.5 Functional description

The sequence of detecting the presence of charging port and type of charging port involves several hardware components, coordinated by system software. This collection of interacting hardware and software is called the USB Battery Charging Subsystem. The following figure shows the USBDCD module as a component of the subsystem. The following table describes the components.

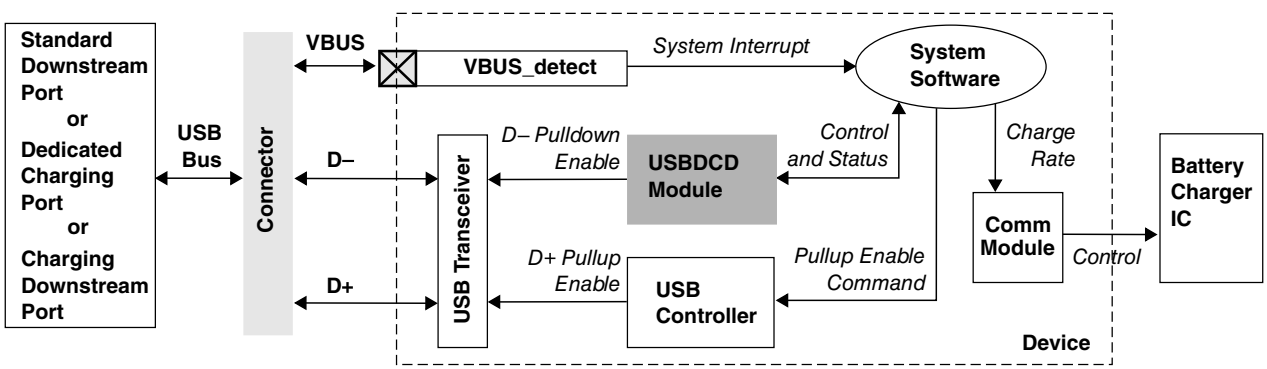


Figure 55-2. USB battery charging subsystem

Table 55-6. USB battery charger subsystem components

Component	Description
Battery Charger IC	The external battery charger IC regulates the charge rate to the rechargable battery. System software is responsible for communicating the appropriate charge rates.

Charger	Maximum current drawn
Standard Downstream Port (SDP)	up to 500 mA (I_{CFG_MAX})
Charging Downstream Port (CDP)	up to 1500 mA (I_{DEV_CHG})
Dedicated Charging Port (DCP)	up to 1500 mA (I_{DEV_CHG})

Table continues on the next page...

Table 55-6. USB battery charger subsystem components (continued)

Component	Description
Comm Module	A communications module on the device can be used to control the charge rate of the battery charger IC.
System software	Coordinates the detection activities of the subsystem.
USB Controller	The D+ pullup enable control signal plays a role during the charger type detection phase. System software must issue a command to the USB controller to assert this signal. After this pullup is enabled, the device is considered to be connected to the USB bus. The host then attempts to enumerate it. **NOTE:** The USB controller must be used only for USB device applications when using the USBDCD module. For USB host applications, the USBDCD module must be disabled.
USB Transceiver	The USB transceiver contains the pullup resistor for the USB D+ signal and the pulldown resistors for the USB D+ and D– signals. The D+ pullup and the D– pulldown are both used during the charger detection sequence in BC1.1, but it is not used during charger detection in BC1.2. The USB transceiver also outputs the digital state of the D+ and D– signals from the USB bus. The pullup and pulldown enable signals are controlled by other modules during the charger detection sequence in BC1.1: The D+ pullup enable is output from the USB controller and is under software control. The USBDCD module controls the D– pulldown enable.
USBDCD Module	Detects whether the device has been plugged into either an SDP, a CDP, or a DCP.
VBUS_detect	This interrupt pin connected to the USB VBUS signal detects when the device has been plugged into or unplugged from the USB bus. If the system requires waking up from a low power mode on being plugged into the USB port, this interrupt should also be a low power wake up source. If this pin multiplexes other functions, such as GPIO, the pin can be configured as an interrupt so that the USB plug or unplug event can be detected.

55.5.1 The charger detection sequence

The following figure illustrates the charger detection sequence in a simplified timing diagram based on the USB Battery Charging Specification Rev. 1.2.

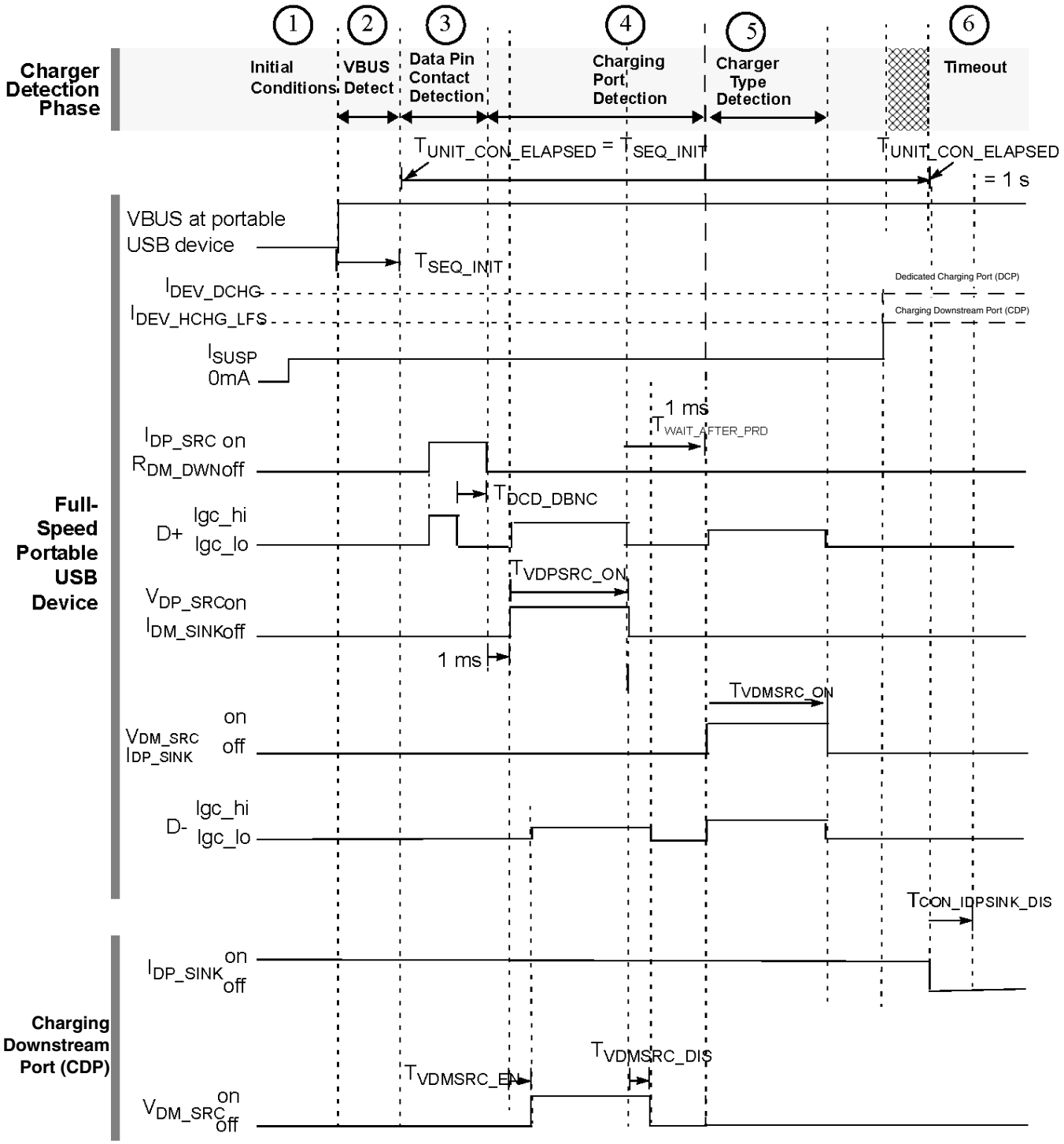


Figure 55-3. Full speed charger detection timing for BC1.2

Timing parameter values used in this module for BC1.2 are listed in the following table.

Table 55-7. Timing parameters for the charger detection sequence for BC1.2

Parameter	USB Battery Charging Spec	Module default	Module programmable range
$T_{DCD_DBNC'}$ [1]	10 ms min (no max)	10 ms	0– 1023 ms
T_{VDPSRC_ON} [1]	40 ms min (no max)	40 ms	0 –1023 ms
$T_{WAIT_AFTER_PRD}$	N/A	1 ms	0– 1023 ms
T_{VDMSRC_ON}	40 ms	40 ms	0 –1023 ms
T_{SEQ_INIT}	N/A	16 ms	0 –1023 ms
T_{UNIT_CON} [1]	1 s	N/A	N/A
T_{VDMSRC_EN} [1]	1– 20 ms	From the USB host	N/A
T_{VDMSRC_DIS} [1]	0 – 20 ms	From the USB host	N/A
$T_{CON_IDPSINK_DIS}$ [1]	0 – 10 ms	From the USB host	N/A

1. This parameter is defined by the *USB Battery Charging Specification, Rev. 1.2*.

The following figure illustrates the charger detection sequence in a simplified timing diagram based on the USB Battery Charging Specification Rev. 1.1.

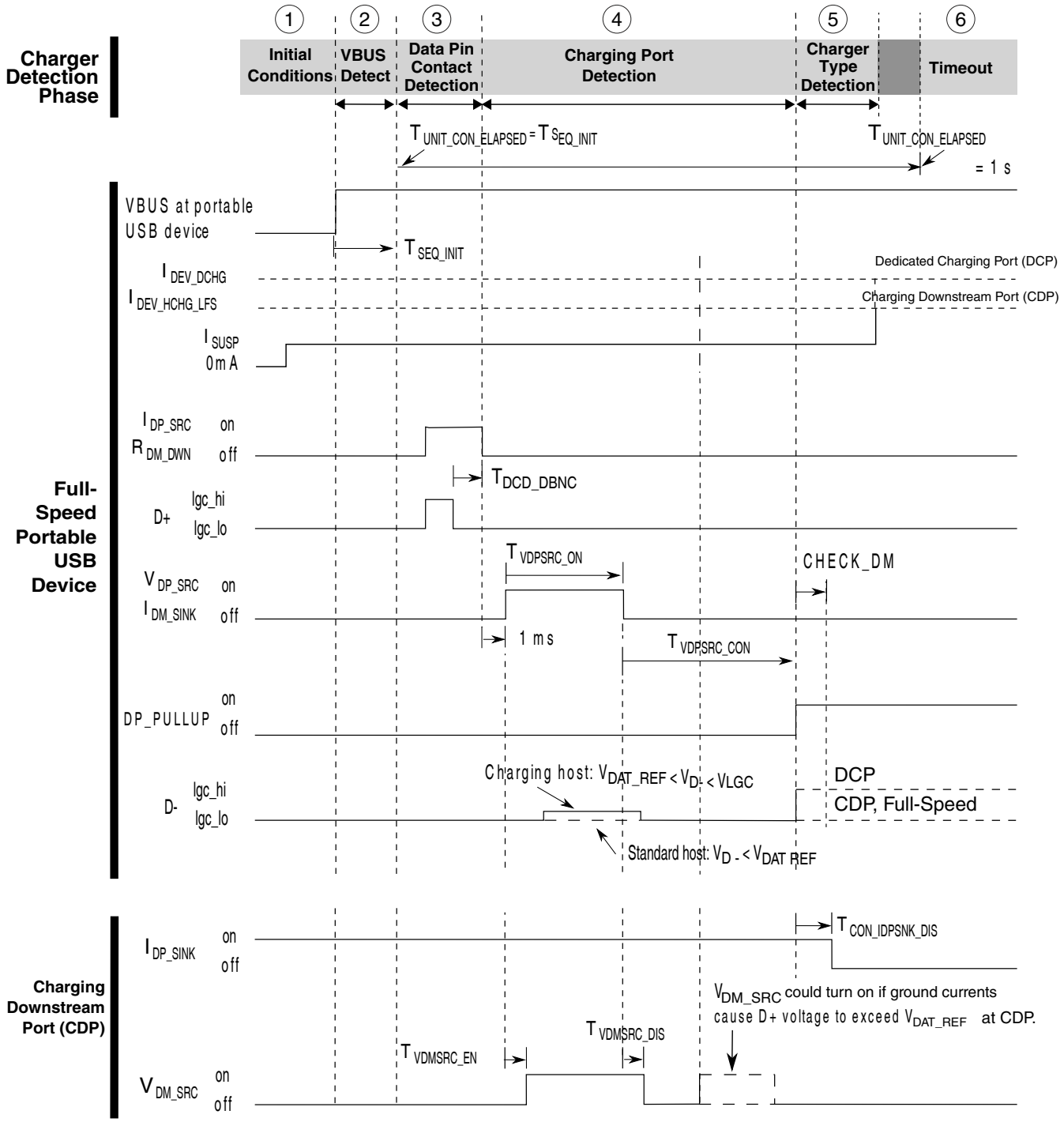


Figure 55-4. Full speed charger detection timing for BC1.1

Timing parameter values used in this module for BC1.1 are listed in the following table.

Table 55-8. Timing parameters for the charger detection sequence for BC1.1

Parameter	USB Battery Charging Spec	Module default	Module programmable range
$T_{DCD_DBNC'}$ [1]	10 ms min (no max)	10 ms	0– 1023 ms
T_{VDPSRC_ON} [1]	40 ms min (no max)	40 ms	0 –1023 ms
T_{VDPSRC_CON} [1]	40 ms min (no max)	40 ms	0 –1023 ms
CHECK_DM	N/A	1 ms	0– 15 ms
T_{SEQ_INIT}	N/A	16 ms	0 –1023 ms
T_{UNIT_CON} [1]	1 s	N/A	N/A
T_{VDMSRC_EN} [1]	1– 20 ms	From the USB host	N/A
T_{VDMSRC_DIS} [1]	0 –20 ms	From the USB host	N/A
$T_{CON_IDPSINK_DIS}$ [1]	0– 20 ms	From the USB host	N/A

1. This parameter is defined by the *USB Battery Charging Specification, Rev. 1.1*.

The following table provides an overview description of the charger detection sequence shown in the preceding figure.

Table 55-9. Overview of the charger detection sequence

Phase		Overview description	Full description
1	Initial Conditions	Initial system conditions that need to be met before the detection sequence is initiated.	Initial System Conditions
2	VBUS Detection	System software detects contact of the VBUS signal with the system interrupt pin VBUS_detect.	VBUS contact detection
3	Data Pin Contact Detection	The USBDCD module detects that the USB data pins D+ and D– have made contact with the USB port.	Data pin contact detection
4	Charging Port Detection	The USBDCD module detects if the port is an SDP or either type of charging port, that is CDP or DCP.	Charging port detection
5	Charger Type Detection	The USBDCD module detects the type of charging port, if applicable.	Charger type detection
6	Sequence Timeout	The USBDCD module did not finish the detection sequence within the timeout interval. The sequence will continue until halted by software.	Charger detection sequence timeout

55.5.1.1 Initial System Conditions

The USBDCD module is intended for use with USB device applications using a rechargable battery. The module does not have support for interfacing with ACA or ACA-Dock equipment as defined in the *USB Battery Charging Specification, Revision 1.2*, and it cannot be used with USB applications that are embedded host or OTG. In addition, before the USBDCD module's charger detection sequence can be initiated, the system must be:

- Powered-up and in run mode. The USBDCD instantiation of this module for a Full-Speed port does not directly depend on the VBUS voltage and can operate as long as the avdd33 supply is in a valid range.
- Recently plugged into a USB port.
- Drawing not more than 2.5 mA total system current from the USB bus, except as allowed by the *USB 2.0 Connect Timing Update ECN*.

Examples of allowable precursors to this set of initial conditions include:

- A powered-down device is subsequently powered-up upon being plugged into the USB bus.
- A device in a low power mode subsequently enters run mode upon being plugged into the USB bus.

55.5.1.2 VBUS contact detection

Once the device is plugged into a USB port, the VBUS_detect system interrupt is triggered. System software must do the following to initialize the module and start the charger detection sequence:

1. Restore power if the module is powered-off.
2. Set CONTROL[SR] to initiate a software reset.
3. Configure the USBDCD module by programming the CLOCK register and the timing parameters as needed.
4. Set CONTROL[IE] to enable interrupts, or clear the bit if software polling method is used.
5. Program CONTROL[BC12] based on which revision of the USB Battery Charging Specification is needed.
6. Set CONTROL[START] to start the charger detection sequence.

55.5.1.3 Data pin contact detection

The module must ensure that the data pins have made contact because the detection sequence depends upon the state of the USB D+ and D- signals. USB plugs and receptables are designed such that when the plug is inserted into the receptable, the power pins make contact before the data pins make contact. See the following figure.

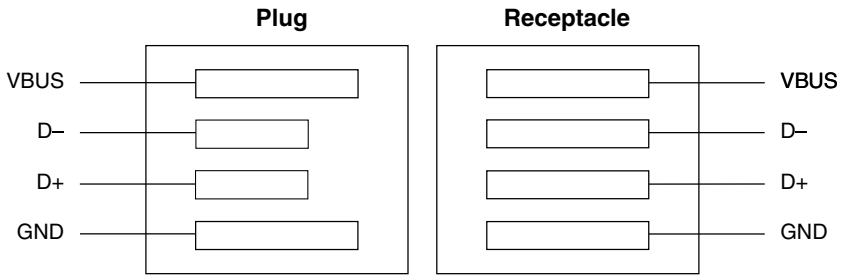


Figure 55-5. Relative pin positions in USB plugs and receptacles

As a result, when a portable USB device is attached to an upstream port, the portable USB device detects VBUS before the data pins have made contact. The time between power pins and data pins making contact depends on how fast the plug is inserted into the receptable. Delays of several hundred milliseconds are possible.

55.5.1.3.1 Debouncing the data pin contact

When system software has initiated the charger detection sequence, as described in Initial System Conditions, the USBDCD module turns on the I_{DP_SRC} current source and enables the R_{DM_DWN} pulldown resistor. If the data pins have not made contact, the D+ line remains high. After the data pins make contact, the D+ line goes low and debouncing begins.

After the D+ line goes low, the module continuously samples the D+ line over the duration of the T_{DCD_DBNC} debounce time interval.By deafult, T_{DCD_DBNC} is 10 ms, but it can be programmed in the TIMER0[TDCD_DBNC] field. See the description of the TIMER0 Register for register information.

When it has remained low for the entire interval, the debouncing is complete. However, if the D+ line returns high during the debounce interval, the module waits until the D+ line goes low again to restart the debouncing. This cycle repeats until either of the following happens:

- The data pin contact has been successfully debounced (see Success in detecting data pin contact (phase completion)).
- A timeout occurs (see Charger detection sequence timeout).

55.5.1.3.2 Success in detecting data pin contact (phase completion)

After successfully debouncing the D+ state, the module does the following:

- Updates the STATUS register to reflect phase completion (See Table 55-13 for field values.)
- Directly proceeds to the next step in the sequence: detection of a charging port (See Charging port detection.)

55.5.1.4 Charging port detection

After it detects that the data pins have made contact, the module waits for a fixed delay of 1 ms, and then attempts to detect whether it is plugged into a charging port. The module connects the following analog units to the USB D+ or D– lines during this phase:

- The voltage source V_{DP_SRC} connects to the D+ line
- The current sink I_{DM_SINK} connects to the D– line
- The voltage comparator connects to the USB D– line, comparing it to the voltage V_{DAT_REF}.

After a time of T_{VDPSRC_ON}, the module samples the D– line. The T_{VDPSRC_ON} parameter is programmable and defaults to 40 ms. After sampling the D– line, the module disconnects the voltage source, current sink, and comparator.

The next steps in the sequence depend on the voltage on the D– line as determined by the voltage comparator. See the following table.

Table 55-10. Sampling D– in the charging port detection phase

If the voltage on D- is...	Then...	See...
Below V_{DAT_REF}	The port is an SDP that does not support using charging currents above I_{CFG_MAX}.	Standard downstream port
Above V_{DAT_REF} but below V_{LGC}	The port is a charging port.	Charging port
Above V_{LGC}	This is an error condition.	Error in charging port detection

55.5.1.4.1 Standard downstream port

As part of the charger detection handshake with a standard USB host, the module does the following without waiting for the interval ($T_{WAIT_AFTER_PRD}$ or T_{VDPSRC_CON}) to elapse:

- Updates the STATUS register to reflect that a standard downstream port (SDP) has been detected with SEQ_RES = 01. See Table 55-13 for field values.
- Sets CONTROL[IF].
- Generates an interrupt if enabled in CONTROL[IE].

At this point, control has been passed to system software via the interrupt. The rest of the sequence, which detects the type of charging port, is not applicable, so software should perform the following steps:

1. Read the STATUS register.
2. Set CONTROL[IACK] to acknowledge the interrupt.
3. Set CONTROL[SR] to issue a software reset to the module.
4. Disable the module.
5. Communicate the appropriate charge rate to the external battery charger IC; see Table 55-6.

55.5.1.4.2 Charging port

As part of the charger detection handshake with any type of USB host, the module waits until the interval ($T_{WAIT_AFTER_PRD}$ or T_{VDPSRC_CON}) has elapsed before it does the following:

- Enables V_{DM_SRC} (for USB Battery Charging Specifications v1.2 only).
- Updates the STATUS register to reflect that a charging port has been detected with SEQ_RES = 10. See Table 55-13 for field values.
- Sets CONTROL[IF].
- Generates an interrupt if enabled in CONTROL[IE].

At this point, control has passed to system software via the interrupt. Software should:

1. Read the STATUS register.
2. Set CONTROL[IACK] to acknowledge the interrupt.
3. Issue a command to the USB controller to pullup the USB D+ line.
4. Wait for the module to complete the final phase of the sequence. See Charger type detection.

55.5.1.4.3 Error in charging port detection

For this error condition, the module does the following:

- Updates the STATUS register to reflect the error with SEQ_RES = 00. See Table 55-13 for field values.
- Sets CONTROL[IF].
- Generates an interrupt if enabled in CONTROL[IE].

Note that in this case the module does not wait for the interval ($T_{WAIT_AFTER_PRD}$ or T_{VDPSRC_CON}) to elapse.

At this point, control has been passed to system software via the interrupt. The rest of the sequence (detecting the type of charging port) is not applicable, so software should:

1. Read the STATUS register.
2. Set CONTROL[IACK] to acknowledge the interrupt.
3. Set CONTROL[SR] to issue a software reset to the module.
4. Disable the module.

55.5.1.5 Charger type detection

For *USB Battery Charging Specification, Rev. 1.2*:

After the USBDCD module enables the V_{DM_SRC}, the module starts the T_{VDMSRC_ON} timer counting down the time interval programmed into the TIMER2[T_{VDMSRC_ON}] field.

Once the T_{VDMSRC_ON} timer has elapsed, the module samples the USB D+ line to determine the type of charger. See the following table.

Table 55-11. Sampling D+ in the charger type detection phase (BC1.2)

If the voltage on D+ is...	Then...	See...
High (D+>V_{DAT_REF})	The port is a DCP.[1]	Dedicated charging port
Low (D+<V_{DAT_REF})	The port is a CDP.[2]	Charging downstream port

1. In a DCP, the D+ and D– lines are shorted together through a small resistor.
2. In a CDP, the D+ and D– lines are not shorted.

For *USB Battery Charging Specification, Rev. 1.1*:

After software enables the D+ pullup resistor, the module is notified automatically (via internal signaling) to start the CHECK_DM timer counting down the time interval programmed in the TIMER2[CHECK_DM] field.

After the CHECK_DM time has elapsed, the module samples the USB D– line to determine the type of charger. See the following table.

Table 55-12. Sampling D– in the charger type detection phase (BC1.1)

If the voltage on D– is...	Then...	See...
High	The port is a DCP.[1]	Dedicated charging port
Low	The port is a CDP.[2]	Charging downstream port

1. In a DCP, the D+ and D– lines are shorted together through a small resistor.
2. In a CDPP, the D+ and D– lines are not shorted.

55.5.1.5.1 Dedicated charging port

For a dedicated charging port (DCP), the module does the following:

- Updates the STATUS register to reflect that a dedicated charging port has been detected with SEQ_RES = 11. See Table 55-13 for field values.
- Sets CONTROL[IF].
- Generates an interrupt if enabled in CONTROL[IE] bit.

The *USB Battery Charging Specification Rev. 1.2* indicates that additionally if the detection sequence determines an attachment to a DCP, then the USB device should signal on the D+ pin by either enabling the D+ pullup resistor or enabling V_{DP_SRC}.

At this point, control has been passed to system software via the interrupt. Software should:

1. Read the STATUS register.
2. Disable the USB controller to prevent transitions on the USB D+ or D– lines from causing spurious interrupt or wakeup events to the system.
3. Set CONTROL[IACK] to acknowledge the interrupt.
4. Set CONTROL[SR] to issue a software reset to the module.
5. Disable the module.

6. Enable signaling on the D+ pin. This can be done by enabling the Transceiver D+ pullup resistor through configuration of register bit fields in the USB controller instance for this USB port.
7. Communicate the appropriate charge rate to the external battery charger IC; see Table 55-6.

55.5.1.5.2 Charging downstream port

For a charging downstream port (CDP), the module does the following:

- Updates the STATUS register to reflect that a CDP has been detected with SEQ_RES = 10. See Table 55-13 for field values.
- Sets CONTROL[IF].
- Generates an interrupt if enabled in CONTROL[IE].

At this point, control has been passed to system software via the interrupt. Software should:

1. Read the STATUS register.
2. Set CONTROL[IACK] to acknowledge the interrupt.
3. Set CONTROL[SR] to issue a software reset to the module.
4. Disable the module.
5. Communicate the appropriate charge rate to the external battery charger IC; see Table 55-6.

55.5.1.6 Charger detection sequence timeout

The maximum time allowed to connect according to the *USB Battery Charging Specification* is one second. If the Unit Connection Timer reaches the one second limit and the sequence is still running as indicated by the STATUS[ACTIVE] bit, the module does the following:

- Updates the STATUS register to reflect that a timeout error has occured. See Table 55-13 for field values.
- Sets the CONTROL[IF] bit.

- Generates an interrupt if enabled in CONTROL[IE].
- The detection sequence continues until explicitly halted by software setting the CONTROL[SR] bit.
- The Unit Connection Timer continues counting. See the description of the TIMER0 Register.

At this point, control has been passed to system software via the interrupt, which has two options: ignore the interrupt and allow more time for the sequence to complete, or halt the sequence. To halt the sequence, software should:

1. Read the STATUS register.
2. Set the CONTROL[IACK] bit to acknowledge the interrupt.
3. Set the CONTROL[SR] bit to issue a software reset to the module.
4. Disable the module.

This timeout function is also useful in case software does not realize that the USB device is unplugged from USB port during the charger detection sequence. If the interrupt occurs but the V_{BUS_DETECT} input is low, software can disable and reset the module.

System software might allow the sequence to run past the timeout interrupt under these conditions:

1. The USB Battery Charging Spec is amended to allow more time. In this case, software should poll TIMER0[$T_{UNITCON}$] periodically to track elapsed time after 1s; or
2. For debug purposes.

Note that the $T_{UNITCON}$ register field will stop incrementing when it reaches its maximum value so it will not rollover to zero and start counting up again.

55.5.1.7 Dead Battery Provision signaling

If the system needs to operate under the Dead Battery Provision of the *USB Battery Charging Specification Revision 1.2*, the USBDCD module must be configured to signal V_{DP_SRC} on the USB1_DP pin.

For information on Dead Battery Provision conditions and signaling, see the Dead or weak battery section later in this chapter.

55.5.2 Interrupts and events

The USBDCD module has an interrupt to alert system software of certain events, which are listed in the following table. All events except the Phase Complete event for the Data Pin Detection phase can trigger an interrupt.

Table 55-13. Events triggering an interrupt by sequence phase

Sequence phase	Event	Event description	STATUS fields[1]	Phase description
Data Pin Detection	Phase Complete	The module has detected data pin contact. *No interrupt occurs*: CONTROL[IF] = 0.	ERR = 0 SEQ_STAT = 01 SEQ_RES = 00 TO = 0	VBUS contact detection
Charging Port Detection	Phase Complete	The module has completed the process of identifying if the USB port is a charging port or not. **NOTE:** This only applies to USB Battery Charging Specification, v1.1.	ERR = 0 SEQ_STAT = 10 SEQ_RES = 01 or 10 TO = 0	Charging port detection
	Error	The module cannot identify the type of port because the D– line is above the USB's VLGC threshold.	ERR = 1 SEQ_STAT = 10 SEQ_RES = 00 TO = 0	Error in charging port detection
Charger Type Detection	Phase Complete	The module has completed the process of identifying the charger type detection. **Note:** The ERR flag always reads zero because no known error conditions are checked during this phase.	ERR = 0 SEQ_STAT = 11 SEQ_RES = 11 or 10 TO = 0	Charger type detection
Sequence Timeout	Error	The timeout interval from the time the USB device attaches to a USB port until it connects has elapsed.	ERR = 1 SEQ_STAT = last value[2] SEQ_RES = last value[2] TO = 1	Charger detection sequence timeout.

1. See the description of the Status register for register information.
2. The SEQ_STAT and SEQ_RES fields retain the values held at the time of the timeout error.

55.5.2.1 Interrupt Handling

Software can read which event caused the interrupt from the STATUS register during the interrupt service routine.

An interrupt is generated only if CONTROL[IE] is set. The CONTROL[IF] bit is always set under interrupt conditions, even if CONTROL[IE] is cleared. In this case, software can poll CONTROL[IF] to determine if an interrupt condition is pending.

Writes to CONTROL[IF] are ignored. To reset CONTROL[IF], set CONTROL[IACK] to acknowledge the interrupt. Writing to CONTROL[IACK] when CONTROL[IF] is cleared has no effect.

55.5.3 Resets

There are two ways to reset various register contents in this module: hardware resets and a software reset.

55.5.3.1 Hardware resets

Hardware resets originate at the system or device level and propagate down to the individual module level. They include start up reset, low-voltage reset, and all other hardware reset sources.

Hardware resets cause the register contents to be restored to their default state as listed in the register descriptions.

55.5.3.2 Software reset

A software reset re-initializes the module's status information, but leaves configuration information unchanged. The software reset allows software to prepare the module without needing to reprogram the same configuration each time the USB device is plugged into a USB port.

Setting CONTROL[SR] initiates a software reset. The following table shows all register fields that are reset to their default values by a software reset.

Table 55-14. Software reset and register fields affected

Register	Fields affected	Fields not affected
CONTROL[1]	IF	IE, START
STATUS	All	None
CLOCK	None	All
TIMER*n*	TUNITCON	All other

1. CONTROL[SR] and CONTROL[IACK] are self-clearing.

A software reset also returns all internal logic, timers, and counters to their reset states. If the module is already active (STATUS[ACTIVE] = 1), a software reset stops the sequence.

Note

Software must always initiate a software reset before starting the sequence to ensure the module is in a known state.

55.6 Initialization information

This module has been designed for minimal configuration while retaining significant programmability. The CLOCK register needs to be initialized to the actual system clock frequency, unless the default value already matches the system requirements.

The other registers generally do not need to be modified, because they default to values that comply with the USB Battery Charging Specification. However, several timing parameters can be changed for a great deal of flexibility if a particular system requires it.

All module configuration must occur *before* initiating the charger detection sequence. Configuration changes made *after* setting CONTROL[START] result in undefined behavior.

55.7 Application information

This section provides application information.

55.7.1 External pullups

Any external pullups applied to the USB D+ or D- data lines must be capable of being disabled to prevent incorrect pullup values or incorrect operation of the USB subsystem.

55.7.2 Dead or weak battery

According to the *USB Battery Charging Specification Revision 1.2*, a USB device with a dead or weak battery that is attached to a downstream port can draw charging current from VBUS without connecting for several minutes, until the battery is charged to the point that the USB device can connect. The conditions for this operation are referred to as the Dead Battery Provision.

The *USB Battery Charging Specification Revision 1.2* limits this charging condition to 100mA for a duration of 45 minutes. The later *USB 2.0 Connect Timing Update ECN* modifies this charging condition to 500mA for a duration of 2 minutes. Customers designing systems to take advantage of the Dead Battery Provision should study both specifications closely.

The USBDCD module is compatible with systems that do not check the strength of the battery. Therefore, this module assumes that the battery is good, so the USB device must immediately connect to the USB bus by pulling the USB_DP pin high after the USBDCD module has determined that the device is attached to an SDP or CDP. (By definition, a DCP does not support connection but still requires a signaling event, see Dedicated charging port section.)

The module is also compatible with systems that have other circuitry to check the strength of the battery. In these systems, if it is known that the battery is weak or dead, software can delay connecting to the USB while charging using the Dead Battery Provision. Once the battery is charged to the good battery threshold, software must then connect to the USB host by pulling the USB_DP pin high.

While using the Dead Battery Provision, the USB_DP pin must signal by enabling V_{DP_SRC}. On this product that signaling can be done most simply by setting the USBDCD_SIGNAL_OVERRIDE[PS] bit field to value 2'b10.

55.7.3 Handling unplug events

If the device is unplugged from the USB bus during the charger detection sequence, the contents of the STATUS register must be ignored and the USBDCD module must get a Software Reset, as described in Software reset.

Chapter 56
USB Voltage Regulator

56.1 Introduction

The USB Voltage Regulator module is a LDO linear voltage regulator to provide 3.3V power from an input power supply varying from 2.7 V to 5.5 V. It consists of one 3.3 V power channel. When the input power supply is below 3.6 V, the regulator goes to pass-through mode. The following figure shows the ideal relation between the regulator output and input power supply.

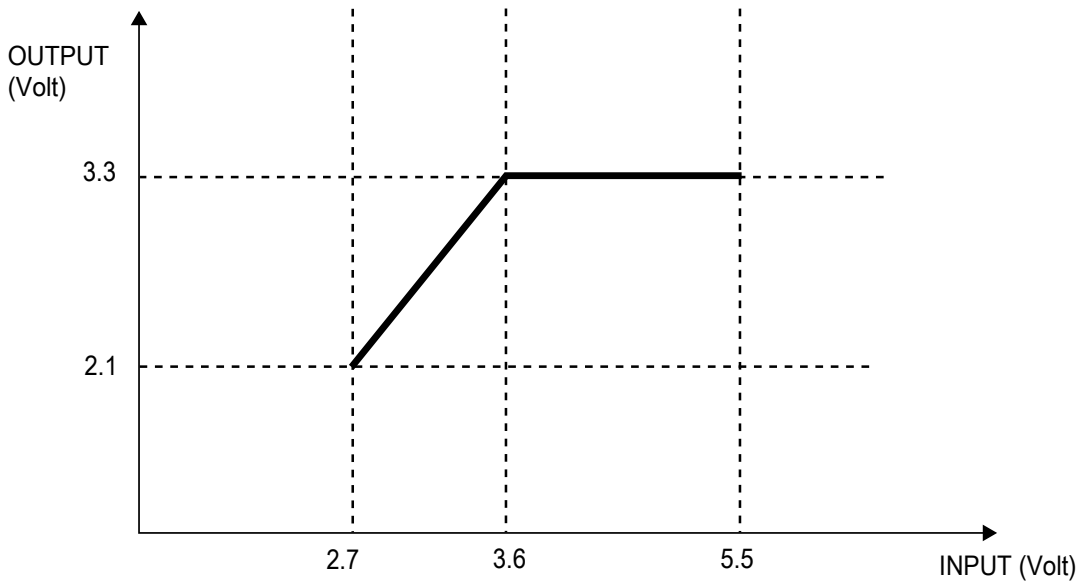


Figure 56-1. Ideal Relation Between the Regulator Output and Input Power Supply

56.1.1 Overview

A simplified block diagram for the USB Voltage Regulator module is shown below.

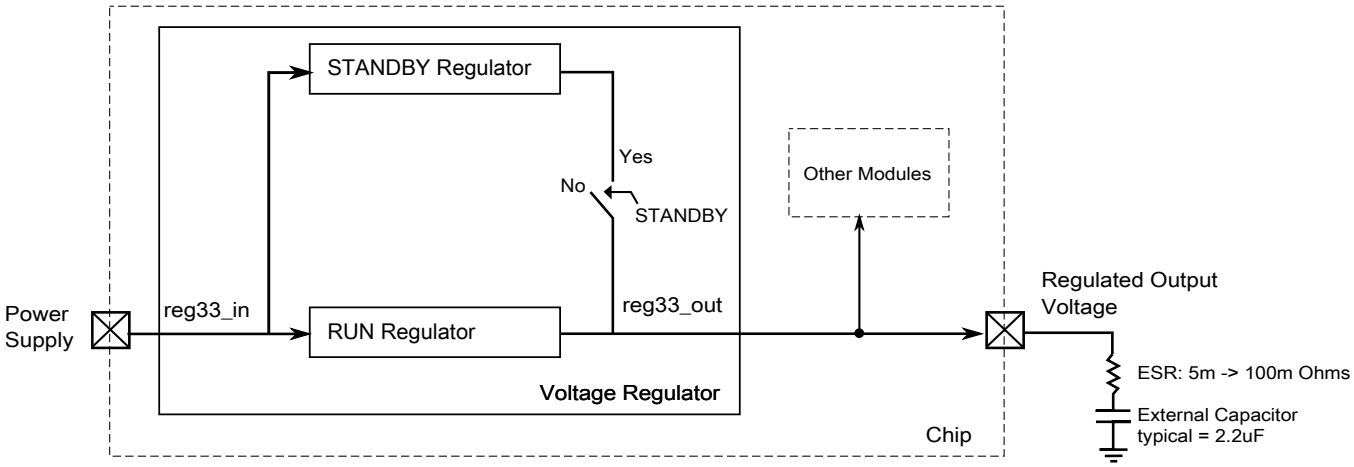


Figure 56-2. USB Voltage Regulator Block Diagram

This module uses 2 regulators in parallel. In run mode, the RUN regulator with the bandgap voltage reference is enabled and can provide up to 120 mA load current. In run mode, the STANDBY regulator and the low power reference are also enabled, but a switch disconnects its output from the external pin. In STANDBY mode, the RUN regulator is disabled and the STANDBY regulator output is connected to the external pin.

Internal power mode signals control whether the module is in RUN or STANDBY mode.

56.1.2 Features

- Low drop-out linear voltage regulator with one power channel (3.3 V).
- Low drop-out voltage: 300 mV.
- Output current: 120 mA.
- Three different power modes: RUN, STANDBY and SHUTDOWN.
- Low quiescent current in RUN mode.
  - Typical value is around 120 µA (one thousand times smaller than the maximum load current).
- Very low quiescent current in STANDBY mode.
  - Typical value is around 1 µA.
- Automatic current limiting if the load current is greater than 290 mA.
- Automatic power-up once some voltage is applied to the regulator input.
- Pass-through mode for regulator input voltages less than 3.6 V

- Small output capacitor: 2.2 µF
- Stable with aluminum, tantalum or ceramic capacitors.

56.1.3 Modes of Operation

The regulator has these power modes:

- RUN—The regulating loop of the RUN regulator and the STANDBY regulator are active, but the switch connecting the STANDBY regulator output to the external pin is open.
- STANDBY—The regulating loop of the RUN regulator is disabled and the standby regulator is active. The switch connecting the STANDBY regulator output to the external pin is closed.
- SHUTDOWN—The module is disabled.

The regulator is enabled by default. This means that once the power supply is provided, the module power-up sequence to RUN mode starts.

56.2 USB Voltage Regulator Module Signal Descriptions

The following table shows the external signals for the regulator.

Table 56-1. USB Voltage Regulator Module Signal Descriptions

Signal	Description	I/O
reg33_in	Unregulated power supply	I
reg33_out	Regulator output voltage	O

Chapter 57
Serial Peripheral Interface (SPI)

57.1 Chip-specific SPI information

57.1.1 SPI Modules Configuration

This device contains 3 SPI modules.

57.1.2 SPI clocking

The SPI module is clocked by the internal bus clock (the DSPI refers to it as system clock). The module has an internal divider, with a minimum divide is two. So, the SPI can run at a maximum frequency of bus clock/2.

57.1.3 Number of CTARs

SPI CTAR registers define different transfer attribute configurations. The SPI module supports up to eight CTAR registers. This device supports two CTARs on all instances of the SPI.

In master mode, the CTAR registers define combinations of transfer attributes, such as frame size, clock phase, clock polarity, data bit ordering, baud rate, and various delays. In slave mode only CTAR0 is used, and a subset of its bitfields sets the slave transfer attributes.

57.1.4 TX FIFO size

Table 57-1. SPI transmit FIFO size

SPI Module	Transmit FIFO size
SPI0	4
SPI1	1
SPI2	1

57.1.5 RX FIFO Size

SPI supports up to 16-bit frame size during reception.

Table 57-2. SPI receive FIFO size

SPI Module	Receive FIFO size
SPI0	4
SPI1	1
SPI2	1

57.1.6 Number of PCS signals

The following table shows the maximum number of peripheral chip select signals available per SPI module. Note that not all chip select signals are available in all device packages. Refer to Pinouts for additional information.

Table 57-3. SPI PCS signals

SPI Module	PCS Signals
SPI0	SPI0_PCS5
	SPI0_PCS4
	SPI0_PCS3
	SPI0_PCS2
	SPI0_PCS1
	SPI0_PCS0
SPI1	SPI1_PCS3
	SPI1_PCS2
	SPI1_PCS1
	SPI1_PCS0
SPI2	SPI2_PCS1
	SPI2_PCS0

57.1.7 SPI Operation in Low Power Modes

In VLPR and VLPW modes the SPI is functional; however, the reduced system frequency also reduces the max frequency of operation for the SPI. In VLPR and VLPW modes the max SPI_CLK frequency is 4 MHz

In stop and VLPS modes, the clocks to the SPI module are disabled. The module is not functional, but it is powered so that it retains state.

There is one way to wake from stop mode via the SPI, which is explained in the following section.

57.1.7.1 Using GPIO Interrupt to Wake from stop mode

Here are the steps to use a GPIO to create a wakeup upon reception of SPI data in slave mode:

1. Point the GPIO interrupt vector to the desired interrupt handler.
2. Enable the GPIO input to generate an interrupt on either the rising or falling edge (depending on the polarity of the chip select signal).
3. Enter Stop or VLPS mode and Wait for the GPIO interrupt.

NOTE

It is likely that in using this approach the first word of data from the SPI host might not be received correctly. This is dependent on the transfer rate used for the SPI, the delay between chip select assertion and presentation of data, and the system interrupt latency.

57.1.8 SPI Doze Mode

The Doze mode for the SPI module is the same as the Wait and VLPW modes for the chip.

57.1.9 SPI Interrupts

The SPI has multiple sources of interrupt requests. However, these sources are OR'd together to generate a single interrupt request per SPI module to the interrupt controller. When an SPI interrupt occurs, read the SPI_SR to determine the exact interrupt source.

57.1.10 SPI clocks

This table shows the SPI module clocks and the corresponding chip clocks.

Table 57-4. SPI clock connections

Module clock	Chip clock
System Clock	Bus Clock

57.1.11 Writing SPI Transmit FIFO

The SPI supports 8-bit or 16-bit writes to the PUSH TX FIFO, allowing a single write to the command word followed by multiple writes to the transmit word. The TX FIFO will save the last command word written, and convert a 8-bit/16-bit write to the transmit word into a 32-bit write that pushes both the command word and transmit word into the TX FIFO (PUSH TX FIFO Register In Master Mode)

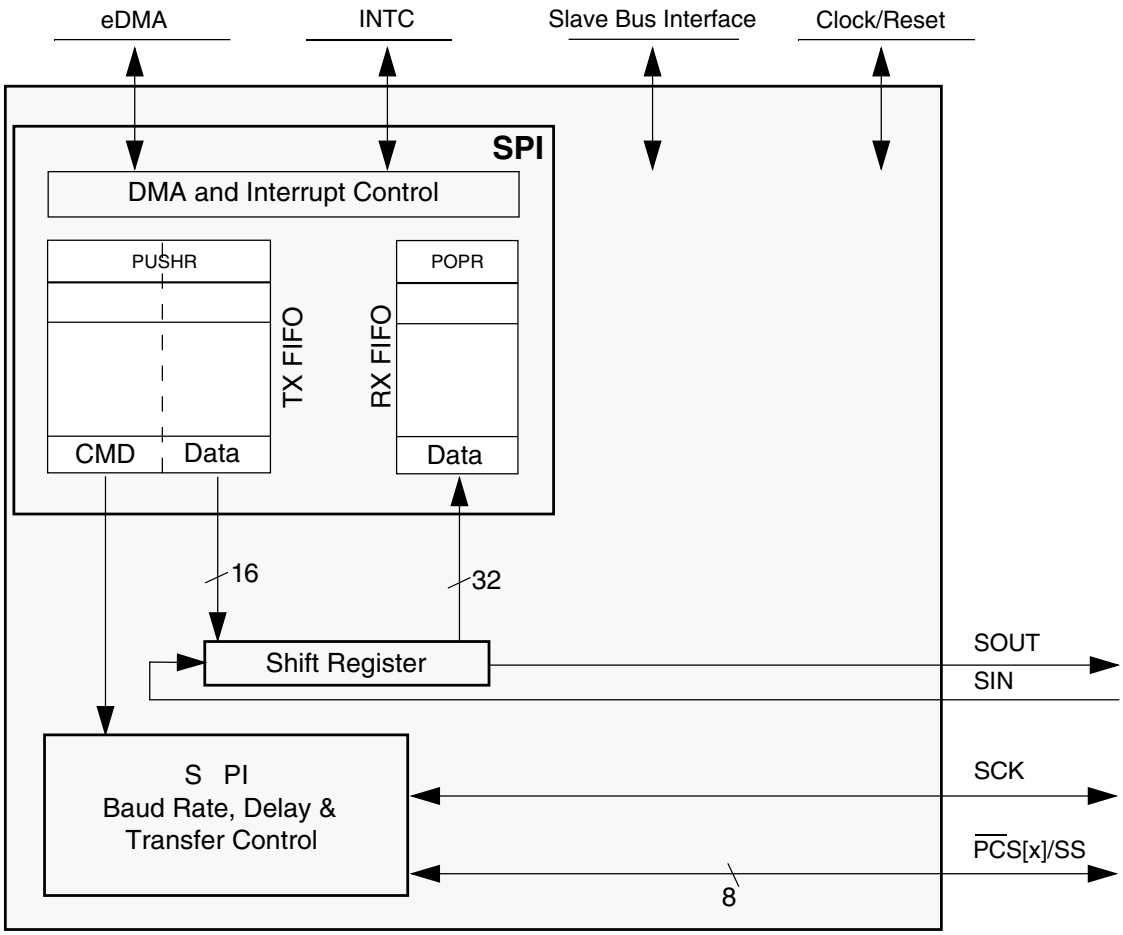
A 32-bit write to the SPI_PUSH register will push all 32-bits to the TX FIFO. An 8-bit or 16-bit write to the 16-bit transmit data field will push the data together with the last written command word. An 8-bit or 16-bit write to the command word does not push data onto the FIFO, but that command word is pushed to the TX FIFO on all subsequent 8-bit or 16-bit writes to the transmit data field. This allows a single 16-bit write to the command word to be used for all subsequent 8-bit or 16-bit writes to the transmit data word. Writing a different 16-bit command word will cause all subsequent 8-bit or 16-bit writes to the transmit data word to be pushed to the TX FIFO with the new command word.

57.2 Introduction

The serial peripheral interface (SPI) module provides a synchronous serial bus for communication between a chip and an external peripheral device.

57.2.1 Block Diagram

The block diagram of this module is as follows:



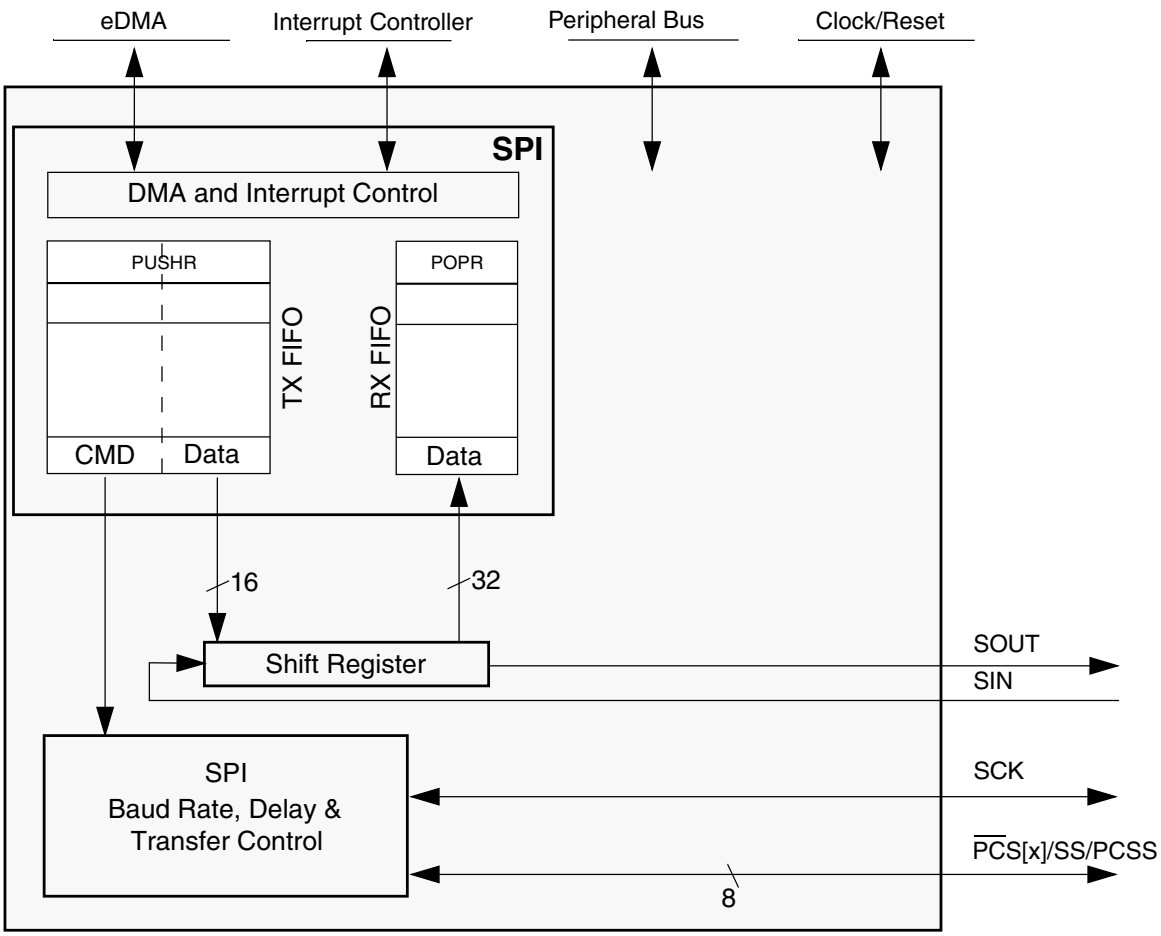


Figure 57-1. SPI Block Diagram

57.2.2 Features

The module supports the following features:

- Full-duplex, three-wire synchronous transfers
- Master mode
- Slave mode
- Data streaming operation in Slave mode with continuous slave selection
- Buffered transmit operation using the transmit first in first out (TX FIFO) with depth of 4 entries
- Buffered receive operation using the receive FIFO (RX FIFO) with depth of 4 entries
- TX and RX FIFOs can be disabled individually for low-latency updates to SPI queues

- Visibility into TX and RX FIFOs for ease of debugging
- Programmable transfer attributes on a per-frame basis:
  - two transfer attribute registers
  - Serial clock (SCK) with programmable polarity and phase
  - Various programmable delays
  - Programmable serial frame size: 4 to 16 bits
    - SPI frames longer than 16 bits can be supported using the continuous selection format.
  - Continuously held chip select capability
- 6 peripheral chip selects (PCSes), expandable to 64 with external demultiplexer
- Deglitching support for up to 32 peripheral chip selects (PCSes) with external demultiplexer
- DMA support for adding entries to TX FIFO and removing entries from RX FIFO:
  - TX FIFO is not full (TFFF)
  - RX FIFO is not empty (RFDF)
- Interrupt conditions:
  - End of Queue reached (EOQF)
  - TX FIFO is not full (TFFF)
  - Transfer of current frame complete (TCF)
  - Attempt to transmit with an empty Transmit FIFO (TFUF)
  - RX FIFO is not empty (RFDF)
  - Frame received while Receive FIFO is full (RFOF)
- Modified SPI transfer formats for communication with slower peripheral devices
- Power-saving architectural features:
  - Support for Stop mode
  - Support for Doze mode

57.2.3 Interface configurations

57.2.3.1 SPI configuration

The Serial Peripheral Interface (SPI) configuration allows the module to send and receive serial data. This configuration allows the module to operate as a basic SPI block with internal FIFOs supporting external queue operation. Transmitted data and received data reside in separate FIFOs. The host CPU or a DMA controller read the received data from the Receive FIFO and write transmit data to the Transmit FIFO.

For queued operations, the SPI queues can reside in system RAM, external to the module. Data transfers between the queues and the module FIFOs are accomplished by a DMA controller or host CPU. The following figure shows a system example with DMA, SPI, and external queues in system RAM.

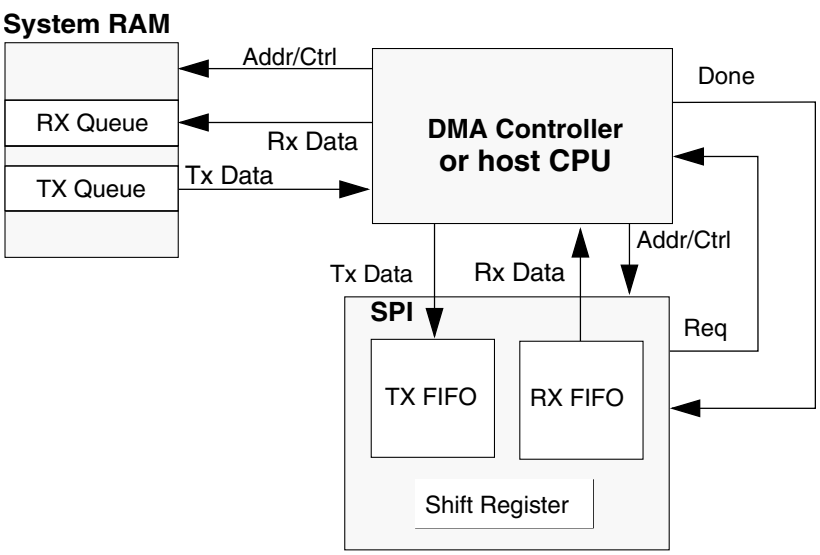


Figure 57-2. SPI with queues and DMA

57.2.4 Modes of Operation

The module supports the following modes of operation that can be divided into two categories:

- Module-specific modes:
  - Master mode

    - Slave mode
    - Module Disable mode
- Chip-specific modes:
    - External Stop mode
    - Debug mode

The module enters module-specific modes when the host writes a module register. The chip-specific modes are controlled by signals external to the module. The chip-specific modes are modes that a chip may enter in parallel to the block-specific modes.

57.2.4.1 Master Mode

Master mode allows the module to initiate and control serial communication. In this mode, these signals are controlled by the module and configured as outputs:

- SCK
- SOUT
- PCS[*x*]

57.2.4.2 Slave Mode

Slave mode allows the module to communicate with SPI bus masters. In this mode, the module responds to externally controlled serial transfers. The SCK signal and the PCS[0]/$\overline{\text{SS}}$ signals are configured as inputs and driven by an SPI bus master.

57.2.4.3 Module Disable Mode

The Module Disable mode can be used for chip power management. The clock to the non-memory mapped logic in the module can be stopped while in the Module Disable mode.

57.2.4.4 External Stop Mode

External Stop mode is used for chip power management. The module supports the Peripheral Bus Stop mode mechanism. When a request is made to enter External Stop mode, it acknowledges the request and completes the transfer that is in progress. When the module reaches the frame boundary, it signals that the protocol clock to the module may be shut off.

57.2.4.5 Debug Mode

Debug mode is used for system development and debugging. The MCR[FRZ] bit controls module behavior in the Debug mode:

- If the bit is set, the module stops all serial transfers, when the chip is in debug mode.
- If the bit is cleared, the chip debug mode has no effect on the module.

57.3 Module signal descriptions

This table describes the signals on the boundary of the module that may connect off chip (in alphabetical order).

Table 57-5. Module signal descriptions

Signal	Master mode	Slave mode	I/O
PCS0/$\overline{SS}$	Peripheral Chip Select 0 (O)	Slave Select (I)	I/O
PCS[1:3]	Peripheral Chip Selects 1–3	(Unused)	O
PCS4	Peripheral Chip Select 4	(Unused)	O
PCS5/ $\overline{PCSS}$	Peripheral Chip Select 5 /Peripheral Chip Select Strobe	(Unused)	O
SCK	Serial Clock (O)	Serial Clock (I)	I/O
SIN	Serial Data In	Serial Data In	I
SOUT	Serial Data Out	Serial Data Out	O

57.3.1 PCS0/$\overline{SS}$—Peripheral Chip Select/Slave Select

Master mode: Peripheral Chip Select 0 (O)—Selects an SPI slave to receive data transmitted from the module.

Slave mode: Slave Select (I)—Selects the module to receive data transmitted from an SPI master.

57.3.2 PCS1–PCS3—Peripheral Chip Selects 1–3

Master mode: Peripheral Chip Selects 1–3 (O)—Select an SPI slave to receive data transmitted by the module.

Slave mode: Unused

57.3.3 PCS4—Peripheral Chip Select 4

Master mode: Peripheral Chip Select 4 (O)—Selects an SPI slave to receive data transmitted by the module.

Slave mode: Unused

57.3.4 PCS5/$\overline{\text{PCSS}}$—Peripheral Chip Select 5/Peripheral Chip Select Strobe

Master mode:

- Peripheral Chip Select 5 (O)—Used only when the peripheral-chip-select strobe is disabled (MCR[PCSSE]). Selects an SPI slave to receive data transmitted by the module.
- Peripheral Chip Select Strobe (O)—Used only when the peripheral-chip-select strobe is enabled (MCR[PCSSE]). Strobes an off-module peripheral-chip-select demultiplexer, which decodes the module's PCS signals other than PCS5, preventing glitches on the demultiplexer outputs.

Slave mode: Unused

57.3.5 SCK—Serial Clock

Master mode: Serial Clock (O)—Supplies a clock signal from the module to SPI slaves.

Slave mode: Serial Clock (I)—Supplies a clock signal to the module from an SPI master.

57.3.6 SIN—Serial Input

Master mode: Serial Input (I)—Receives serial data.

Slave mode: Serial Input (I)—Receives serial data.

57.3.7 SOUT—Serial Output

Master mode: Serial Output (O)—Transmits serial data.

Slave mode: Serial Output (O)—Transmits serial data.

NOTE

Serial Data Out output buffers are controlled through SIU (or SIUL) and cannot be controlled through the module.

57.4 Memory Map/Register Definition

Register accesses to memory addresses that are reserved or undefined result in a transfer error. Write access to the POPR and RXFRn also results in a transfer error.

SPI memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4002_C000	Module Configuration Register (SPI0_MCR)	32	R/W	0000_4001h	57.4.1/1831
4002_C008	Transfer Count Register (SPI0_TCR)	32	R/W	0000_0000h	57.4.2/1834
4002_C00C	Clock and Transfer Attributes Register (In Master Mode) (SPI0_CTAR0)	32	R/W	7800_0000h	57.4.3/1834
4002_C00C	Clock and Transfer Attributes Register (In Slave Mode) (SPI0_CTAR0_SLAVE)	32	R/W	7800_0000h	57.4.4/1839
4002_C010	Clock and Transfer Attributes Register (In Master Mode) (SPI0_CTAR1)	32	R/W	7800_0000h	57.4.3/1834
4002_C02C	Status Register (SPI0_SR)	32	R/W	0200_0000h	57.4.5/1841
4002_C030	DMA/Interrupt Request Select and Enable Register (SPI0_RSER)	32	R/W	0000_0000h	57.4.6/1844
4002_C034	PUSH TX FIFO Register In Master Mode (SPI0_PUSHR)	32	R/W	0000_0000h	57.4.7/1846
4002_C034	PUSH TX FIFO Register In Slave Mode (SPI0_PUSHR_SLAVE)	32	R/W	0000_0000h	57.4.8/1848
4002_C038	POP RX FIFO Register (SPI0_POPR)	32	R	0000_0000h	57.4.9/1848
4002_C03C	Transmit FIFO Registers (SPI0_TXFR0)	32	R	0000_0000h	57.4.10/ 1849
4002_C040	Transmit FIFO Registers (SPI0_TXFR1)	32	R	0000_0000h	57.4.10/ 1849
4002_C044	Transmit FIFO Registers (SPI0_TXFR2)	32	R	0000_0000h	57.4.10/ 1849
4002_C048	Transmit FIFO Registers (SPI0_TXFR3)	32	R	0000_0000h	57.4.10/ 1849

Table continues on the next page...

SPI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4002_C07C	Receive FIFO Registers (SPI0_RXFR0)	32	R	0000_0000h	57.4.11/ 1849
4002_C080	Receive FIFO Registers (SPI0_RXFR1)	32	R	0000_0000h	57.4.11/ 1849
4002_C084	Receive FIFO Registers (SPI0_RXFR2)	32	R	0000_0000h	57.4.11/ 1849
4002_C088	Receive FIFO Registers (SPI0_RXFR3)	32	R	0000_0000h	57.4.11/ 1849
4002_D000	Module Configuration Register (SPI1_MCR)	32	R/W	0000_4001h	57.4.1/1831
4002_D008	Transfer Count Register (SPI1_TCR)	32	R/W	0000_0000h	57.4.2/1834
4002_D00C	Clock and Transfer Attributes Register (In Master Mode) (SPI1_CTAR0)	32	R/W	7800_0000h	57.4.3/1834
4002_D00C	Clock and Transfer Attributes Register (In Slave Mode) (SPI1_CTAR0_SLAVE)	32	R/W	7800_0000h	57.4.4/1839
4002_D010	Clock and Transfer Attributes Register (In Master Mode) (SPI1_CTAR1)	32	R/W	7800_0000h	57.4.3/1834
4002_D02C	Status Register (SPI1_SR)	32	R/W	0200_0000h	57.4.5/1841
4002_D030	DMA/Interrupt Request Select and Enable Register (SPI1_RSER)	32	R/W	0000_0000h	57.4.6/1844
4002_D034	PUSH TX FIFO Register In Master Mode (SPI1_PUSHR)	32	R/W	0000_0000h	57.4.7/1846
4002_D034	PUSH TX FIFO Register In Slave Mode (SPI1_PUSHR_SLAVE)	32	R/W	0000_0000h	57.4.8/1848
4002_D038	POP RX FIFO Register (SPI1_POPR)	32	R	0000_0000h	57.4.9/1848
4002_D03C	Transmit FIFO Registers (SPI1_TXFR0)	32	R	0000_0000h	57.4.10/ 1849
4002_D040	Transmit FIFO Registers (SPI1_TXFR1)	32	R	0000_0000h	57.4.10/ 1849
4002_D044	Transmit FIFO Registers (SPI1_TXFR2)	32	R	0000_0000h	57.4.10/ 1849
4002_D048	Transmit FIFO Registers (SPI1_TXFR3)	32	R	0000_0000h	57.4.10/ 1849
4002_D07C	Receive FIFO Registers (SPI1_RXFR0)	32	R	0000_0000h	57.4.11/ 1849
4002_D080	Receive FIFO Registers (SPI1_RXFR1)	32	R	0000_0000h	57.4.11/ 1849
4002_D084	Receive FIFO Registers (SPI1_RXFR2)	32	R	0000_0000h	57.4.11/ 1849
4002_D088	Receive FIFO Registers (SPI1_RXFR3)	32	R	0000_0000h	57.4.11/ 1849
400A_C000	Module Configuration Register (SPI2_MCR)	32	R/W	0000_4001h	57.4.1/1831
400A_C008	Transfer Count Register (SPI2_TCR)	32	R/W	0000_0000h	57.4.2/1834
400A_C00C	Clock and Transfer Attributes Register (In Master Mode) (SPI2_CTAR0)	32	R/W	7800_0000h	57.4.3/1834

Table continues on the next page...

SPI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400A_C00C	Clock and Transfer Attributes Register (In Slave Mode) (SPI2_CTAR0_SLAVE)	32	R/W	7800_0000h	57.4.4/1839
400A_C010	Clock and Transfer Attributes Register (In Master Mode) (SPI2_CTAR1)	32	R/W	7800_0000h	57.4.3/1834
400A_C02C	Status Register (SPI2_SR)	32	R/W	0200_0000h	57.4.5/1841
400A_C030	DMA/Interrupt Request Select and Enable Register (SPI2_RSER)	32	R/W	0000_0000h	57.4.6/1844
400A_C034	PUSH TX FIFO Register In Master Mode (SPI2_PUSHR)	32	R/W	0000_0000h	57.4.7/1846
400A_C034	PUSH TX FIFO Register In Slave Mode (SPI2_PUSHR_SLAVE)	32	R/W	0000_0000h	57.4.8/1848
400A_C038	POP RX FIFO Register (SPI2_POPR)	32	R	0000_0000h	57.4.9/1848
400A_C03C	Transmit FIFO Registers (SPI2_TXFR0)	32	R	0000_0000h	57.4.10/ 1849
400A_C040	Transmit FIFO Registers (SPI2_TXFR1)	32	R	0000_0000h	57.4.10/ 1849
400A_C044	Transmit FIFO Registers (SPI2_TXFR2)	32	R	0000_0000h	57.4.10/ 1849
400A_C048	Transmit FIFO Registers (SPI2_TXFR3)	32	R	0000_0000h	57.4.10/ 1849
400A_C07C	Receive FIFO Registers (SPI2_RXFR0)	32	R	0000_0000h	57.4.11/ 1849
400A_C080	Receive FIFO Registers (SPI2_RXFR1)	32	R	0000_0000h	57.4.11/ 1849
400A_C084	Receive FIFO Registers (SPI2_RXFR2)	32	R	0000_0000h	57.4.11/ 1849
400A_C088	Receive FIFO Registers (SPI2_RXFR3)	32	R	0000_0000h	57.4.11/ 1849

57.4.1 Module Configuration Register (SPIx_MCR)

Contains bits to configure various attributes associated with the module operations. The HALT and MDIS bits can be changed at any time, but the effect takes place only on the next frame boundary. Only the HALT and MDIS bits in the MCR can be changed, while the module is in the Running state.

Address: Base address + 0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	MSTR	CONT_SCKE	DCONF		FRZ	MTFE	PCSSE	ROOE	Reserved		PCSIS					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DOZE	MDIS	DIS_TXF	DIS_RXF	0	0	SMPL_PT		0					Reserved	Reserved	HALT
W					CLR_TXF	CLR_RXF										
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1

SPIx_MCR field descriptions

Field	Description
31 MSTR	Master/Slave Mode Select Enables either Master mode (if supported) or Slave mode (if supported) operation. 0 Enables Slave mode 1 Enables Master mode
30 CONT_SCKE	Continuous SCK Enable Enables the Serial Communication Clock (SCK) to run continuously.

Table continues on the next page...

SPIx_MCR field descriptions (continued)

Field	Description
	0 Continuous SCK disabled. 1 Continuous SCK enabled.
29–28 DCONF	SPI Configuration. Selects among the different configurations of the module. 00 SPI 01 Reserved 10 Reserved 11 Reserved
27 FRZ	Freeze Enables transfers to be stopped on the next frame boundary when the device enters Debug mode. 0 Do not halt serial transfers in Debug mode. 1 Halt serial transfers in Debug mode.
26 MTFE	Modified Transfer Format Enable Enables a modified transfer format to be used. 0 Modified SPI transfer format disabled. 1 Modified SPI transfer format enabled.
25 PCSSE	Peripheral Chip Select Strobe Enable Enables the PCS5/ $\overline{\text{PCSS}}$ to operate as a PCS Strobe output signal. 0 PCS5/ $\overline{\text{PCSS}}$ is used as the Peripheral Chip Select[5] signal. 1 PCS5/ $\overline{\text{PCSS}}$ is used as an active-low PCS Strobe signal.
24 ROOE	Receive FIFO Overflow Overwrite Enable In the RX FIFO overflow condition, configures the module to ignore the incoming serial data or overwrite existing data. If the RX FIFO is full and new data is received, the data from the transfer, generating the overflow, is ignored or shifted into the shift register. 0 Incoming data is ignored. 1 Incoming data is shifted into the shift register.
23–22 Reserved	Always write the reset value to this field. This field is reserved.
21–16 PCSIS	Peripheral Chip Select x Inactive State Determines the inactive state of PCSx. Refer to the chip-specific SPI information for the number of PCS signals used in this chip. **NOTE:** The effect of this bit only takes place when module is enabled. Ensure that this bit is configured correctly before enabling the DSPI interface. 0 The inactive state of PCSx is low. 1 The inactive state of PCSx is high.
15 DOZE	Doze Enable Provides support for an externally controlled Doze mode power-saving mechanism.

Table continues on the next page...

SPIx_MCR field descriptions (continued)

Field	Description
	0 Doze mode has no effect on the module. 1 Doze mode disables the module.
14 MDIS	Module Disable Allows the clock to be stopped to the non-memory mapped logic in the module effectively putting it in a software-controlled power-saving state. The reset value of the MDIS bit is parameterized, with a default reset value of 1. When the module is used in Slave Mode, it is recommended to leave this bit 0, because a slave doesn't have control over master transactions. 0 Enables the module clocks. 1 Allows external logic to disable the module clocks.
13 DIS_TXF	Disable Transmit FIFO When the TX FIFO is disabled, the transmit part of the module operates as a simplified double-buffered SPI. This bit can be written only when the MDIS bit is cleared. 0 TX FIFO is enabled. 1 TX FIFO is disabled.
12 DIS_RXF	Disable Receive FIFO When the RX FIFO is disabled, the receive part of the module operates as a simplified double-buffered SPI. This bit can only be written when the MDIS bit is cleared. 0 RX FIFO is enabled. 1 RX FIFO is disabled.
11 CLR_TXF	Clear TX FIFO Flushes the TX FIFO. Writing a 1 to CLR_TXF clears the TX FIFO Counter. The CLR_TXF bit is always read as zero. 0 Do not clear the TX FIFO counter. 1 Clear the TX FIFO counter.
10 CLR_RXF	CLR_RXF Flushes the RX FIFO. Writing a 1 to CLR_RXF clears the RX Counter. The CLR_RXF bit is always read as zero. 0 Do not clear the RX FIFO counter. 1 Clear the RX FIFO counter.
9–8 SMPL_PT	Sample Point Controls when the module master samples SIN in Modified Transfer Format. This field is valid only when CPHA bit in CTARn[CPHA] is 0. 00 0 protocol clock cycles between SCK edge and SIN sample 01 1 protocol clock cycle between SCK edge and SIN sample 10 2 protocol clock cycles between SCK edge and SIN sample 11 Reserved
7–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

SPIx_MCR field descriptions (continued)

Field	Description
2 Reserved	This field is reserved.
1 Reserved	This field is reserved.
0 HALT	Halt The HALT bit starts and stops frame transfers. See Start and Stop of Module transfers 0 Start transfers. 1 Stop transfers.

57.4.2 Transfer Count Register (SPIx_TCR)

TCR contains a counter that indicates the number of SPI transfers made. The transfer counter is intended to assist in queue management. Do not write the TCR when the module is in the Running state.

Address: Base address + 8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SPI_TCNT																0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPIx_TCR field descriptions

Field	Description
31–16 SPI_TCNT	SPI Transfer Counter Counts the number of SPI transfers the module makes. The SPI_TCNT field increments every time the last bit of an SPI frame is transmitted. A value written to SPI_TCNT presets the counter to that value. SPI_TCNT is reset to zero at the beginning of the frame when the CTCNT field is set in the executing SPI command. The Transfer Counter wraps around; incrementing the counter past 65535 resets the counter to zero.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

57.4.3 Clock and Transfer Attributes Register (In Master Mode) (SPIx_CTAR*n*)

CTAR registers are used to define different transfer attributes. Do not write to the CTAR registers while the module is in the Running state.

In Master mode, the CTAR registers define combinations of transfer attributes such as frame size, clock phase and polarity, data bit ordering, baud rate, and various delays. In slave mode, a subset of the bitfields in CTAR0 are used to set the slave transfer attributes.

When the module is configured as an SPI master, the CTAS field in the command portion of the TX FIFO entry selects which of the CTAR registers is used. When the module is configured as an SPI bus slave, it uses the CTAR0 register.

Address: Base address + Ch offset + (4d × i), where i=0d to 1d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DBR	FMSZ				CPOL	CPHA	LSBFE	PCSSCK		PASC		PDT		PBR	
W																
Reset	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CSSCK				ASC				DT				BR			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPIx_CTAR*n* field descriptions

Field	Description
31 DBR	Double Baud Rate Doubles the effective baud rate of the Serial Communications Clock (SCK). This field is used only in master mode. It effectively halves the Baud Rate division ratio, supporting faster frequencies, and odd division ratios for the Serial Communications Clock (SCK). When the DBR bit is set, the duty cycle of the Serial Communications Clock (SCK) depends on the value in the Baud Rate Prescaler and the Clock Phase bit as listed in the following table. See the BR field description for details on how to compute the baud rate.

Table 57-6. SPI SCK Duty Cycle

DBR	CPHA	PBR	SCK Duty Cycle
0	any	any	50/50
1	0	00	50/50
1	0	01	33/66
1	0	10	40/60
1	0	11	43/57
1	1	00	50/50
1	1	01	66/33
1	1	10	60/40
1	1	11	57/43

Table continues on the next page...

SPIx_CTAR*n* field descriptions (continued)

Field	Description
	0 The baud rate is computed normally with a 50/50 duty cycle. 1 The baud rate is doubled with the duty cycle depending on the Baud Rate Prescaler.
30–27 FMSZ	Frame Size The number of bits transferred per frame is equal to the FMSZ value plus 1. Regardless of the transmission mode, the minimum valid frame size value is 4.
26 CPOL	Clock Polarity Selects the inactive state of the Serial Communications Clock (SCK). This bit is used in both master and slave mode. For successful communication between serial devices, the devices must have identical clock polarities. When the Continuous Selection Format is selected, switching between clock polarities without stopping the module can cause errors in the transfer due to the peripheral device interpreting the switch of clock polarity as a valid clock edge. **NOTE:** In case of Continuous SCK mode, when the module goes in low power mode(disabled), inactive state of SCK is not guaranted. 0 The inactive state value of SCK is low. 1 The inactive state value of SCK is high.
25 CPHA	Clock Phase Selects which edge of SCK causes data to change and which edge causes data to be captured. This bit is used in both master and slave mode. For successful communication between serial devices, the devices must have identical clock phase settings. In Continuous SCK mode, the bit value is ignored and the transfers are done as if the CPHA bit is set to 1. 0 Data is captured on the leading edge of SCK and changed on the following edge. 1 Data is changed on the leading edge of SCK and captured on the following edge.
24 LSBFE	LSB First Specifies whether the LSB or MSB of the frame is transferred first. 0 Data is transferred MSB first. 1 Data is transferred LSB first.
23–22 PCSSCK	PCS to SCK Delay Prescaler Selects the prescaler value for the delay between assertion of PCS and the first edge of the SCK. See the CSSCK field description for information on how to compute the PCS to SCK Delay. Refer PCS to SCK Delay (t_{CSC}) for more details. 00 PCS to SCK Prescaler value is 1. 01 PCS to SCK Prescaler value is 3. 10 PCS to SCK Prescaler value is 5. 11 PCS to SCK Prescaler value is 7.
21–20 PASC	After SCK Delay Prescaler Selects the prescaler value for the delay between the last edge of SCK and the negation of PCS. See the ASC field description for information on how to compute the After SCK Delay. Refer After SCK Delay (t_{ASC}) for more details. 00 Delay after Transfer Prescaler value is 1. 01 Delay after Transfer Prescaler value is 3.

Table continues on the next page...

SPIx_CTAR*n* field descriptions (continued)

Field	Description
	10 Delay after Transfer Prescaler value is 5. 11 Delay after Transfer Prescaler value is 7.
19–18 PDT	Delay after Transfer Prescaler Selects the prescaler value for the delay between the negation of the PCS signal at the end of a frame and the assertion of PCS at the beginning of the next frame. The PDT field is only used in master mode. See the DT field description for details on how to compute the Delay after Transfer. Refer Delay after Transfer (t_{DT}) for more details. 00 Delay after Transfer Prescaler value is 1. 01 Delay after Transfer Prescaler value is 3. 10 Delay after Transfer Prescaler value is 5. 11 Delay after Transfer Prescaler value is 7.
17–16 PBR	Baud Rate Prescaler Selects the prescaler value for the baud rate. This field is used only in master mode. The baud rate is the frequency of the SCK. The protocol clock is divided by the prescaler value before the baud rate selection takes place. See the BR field description for details on how to compute the baud rate. 00 Baud Rate Prescaler value is 2. 01 Baud Rate Prescaler value is 3. 10 Baud Rate Prescaler value is 5. 11 Baud Rate Prescaler value is 7.
15–12 CSSCK	PCS to SCK Delay Scaler Selects the scaler value for the PCS to SCK delay. This field is used only in master mode. The PCS to SCK Delay is the delay between the assertion of PCS and the first edge of the SCK. The delay is a multiple of the protocol clock period, and it is computed according to the following equation: $t_{CSC} = (1/f_P) \times PCSSCK \times CSSCK$. The following table lists the delay scaler values.

Table 57-7. Delay Scaler Encoding

Field Value	Delay Scaler Value
0000	2
0001	4
0010	8
0011	16
0100	32
0101	64
0110	128
0111	256
1000	512
1001	1024
1010	2048
1011	4096
1100	8192

Table continues on the next page...

SPIx_CTAR*n* field descriptions (continued)

Field	Description
	Table 57-7. Delay Scaler Encoding (continued) **Field Value** / **Delay Scaler Value** 1101 — 16384 1110 — 32768 1111 — 65536 Refer PCS to SCK Delay (t_{CSC}) for more details.
11–8 ASC	After SCK Delay Scaler Selects the scaler value for the After SCK Delay. This field is used only in master mode. The After SCK Delay is the delay between the last edge of SCK and the negation of PCS. The delay is a multiple of the protocol clock period, and it is computed according to the following equation: $t_{ASC} = (1/f_P) \times PASC \times ASC$ See Delay Scaler Encoding table in CTARn[CSSCK] bit field description for scaler values. Refer After SCK Delay (t_{ASC}) for more details.
7–4 DT	Delay After Transfer Scaler Selects the Delay after Transfer Scaler. This field is used only in master mode. The Delay after Transfer is the time between the negation of the PCS signal at the end of a frame and the assertion of PCS at the beginning of the next frame. In the Continuous Serial Communications Clock operation, the DT value is fixed to one SCK clock period, The Delay after Transfer is a multiple of the protocol clock period, and it is computed according to the following equation: $t_{DT} = (1/f_P) \times PDT \times DT$ See Delay Scaler Encoding table in CTARn[CSSCK] bit field description for scaler values.
BR	Baud Rate Scaler Selects the scaler value for the baud rate. This field is used only in master mode. The prescaled protocol clock is divided by the Baud Rate Scaler to generate the frequency of the SCK. The baud rate is computed according to the following equation: SCK baud rate = $(f_P / PBR) \times [(1+DBR)/BR]$ The following table lists the baud rate scaler values. **Table 57-8. Baud Rate Scaler** **CTARn[BR]** / **Baud Rate Scaler Value** 0000 — 2 0001 — 4 0010 — 6 0011 — 8 0100 — 16 0101 — 32 0110 — 64 0111 — 128

Table continues on the next page...

SPIx_CTAR*n* field descriptions (continued)

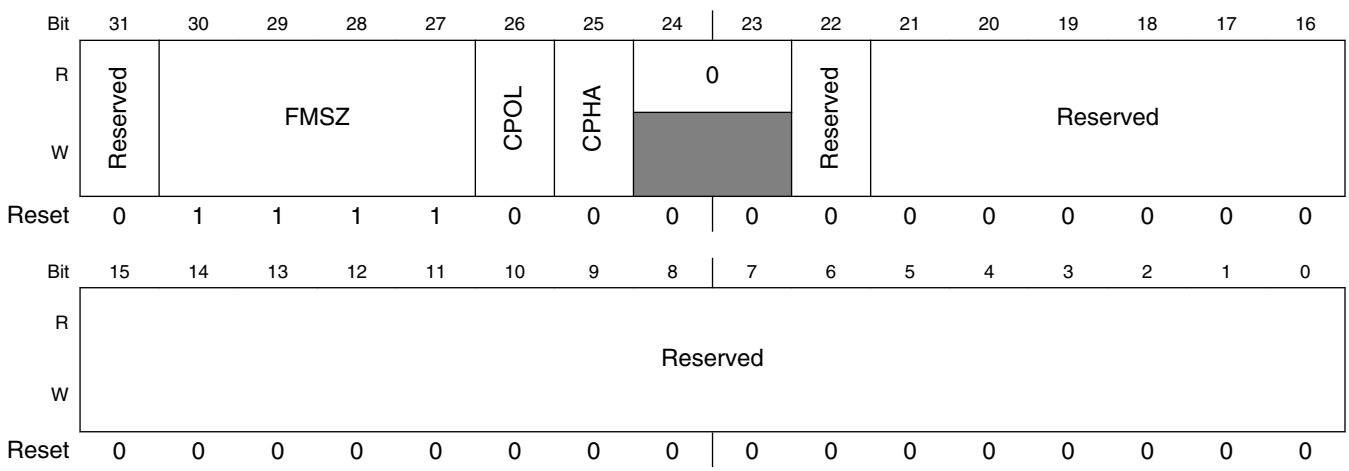
Field	Description
	Table 57-8. Baud Rate Scaler (continued)

CTARn[BR]	Baud Rate Scaler Value
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

57.4.4 Clock and Transfer Attributes Register (In Slave Mode) (SPIx_CTAR*n*_SLAVE)

When the module is configured as an SPI bus slave, the CTAR0 register is used.

Address: Base address + Ch offset + (0d × i), where i=0d to 0d



SPIx_CTAR*n*_SLAVE field descriptions

Field	Description
31 Reserved	Always write the reset value to this field. This field is reserved.
30–27 FMSZ	Frame Size

Table continues on the next page...

SPIx_CTAR*n*_SLAVE field descriptions (continued)

Field	Description
	The number of bits transfered per frame is equal to the FMSZ field value plus 1. Note that the minimum valid value of frame size is 4.
26 CPOL	Clock Polarity Selects the inactive state of the Serial Communications Clock (SCK). **NOTE:** In case of Continuous SCK mode, when the module goes in low power mode(disabled), inactive state of SCK is not guaranted. 0 The inactive state value of SCK is low. 1 The inactive state value of SCK is high.
25 CPHA	Clock Phase Selects which edge of SCK causes data to change and which edge causes data to be captured. This bit is used in both master and slave mode. For successful communication between serial devices, the devices must have identical clock phase settings. In Continuous SCK mode, the bit value is ignored and the transfers are done as if the CPHA bit is set to 1. 0 Data is captured on the leading edge of SCK and changed on the following edge. 1 Data is changed on the leading edge of SCK and captured on the following edge.
24–23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 Reserved	This field is reserved.
Reserved	This field is reserved.

57.4.5 Status Register (SPIx_SR)

SR contains status and flag bits. The bits reflect the status of the module and indicate the occurrence of events that can generate interrupt or DMA requests. Software can clear flag bits in the SR by writing a 1 to them. Writing a 0 to a flag bit has no effect. This register may not be writable in Module Disable mode due to the use of power saving mechanisms.

Address: Base address + 2Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	TCF	TXRXS	0	EOQF	TFUF	0	TFFF	0	0	0	0	0	RFOF	0	RFDF	0
W	w1c	w1c		w1c	w1c		w1c						w1c		w1c	
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	TXCTR				TXNXTPTR				RXCTR				POPNXTPTR			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPIx_SR field descriptions

Field	Description
31 TCF	Transfer Complete Flag Indicates that all bits in a frame have been shifted out. TCF remains set until it is cleared by writing a 1 to it. 0 Transfer not complete. 1 Transfer complete.
30 TXRXS	TX and RX Status Reflects the run status of the module. 0 Transmit and receive operations are disabled (The module is in Stopped state). 1 Transmit and receive operations are enabled (The module is in Running state).
29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

SPIx_SR field descriptions (continued)

Field	Description
28 EOQF	End of Queue Flag Indicates that the last entry in a queue has been transmitted when the module is in Master mode. The EOQF bit is set when the TX FIFO entry has the EOQ bit set in the command halfword and the end of the transfer is reached. The EOQF bit remains set until cleared by writing a 1 to it. When the EOQF bit is set, the TXRXS bit is automatically cleared. 0 EOQ is not set in the executing command. 1 EOQ is set in the executing SPI command.
27 TFUF	Transmit FIFO Underflow Flag Indicates an underflow condition in the TX FIFO. The transmit underflow condition is detected only for SPI blocks operating in Slave mode and SPI configuration. TFUF is set when the TX FIFO of the module operating in SPI Slave mode is empty and an external SPI master initiates a transfer. The TFUF bit remains set until cleared by writing 1 to it. 0 No TX FIFO underflow. 1 TX FIFO underflow has occurred.
26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25 TFFF	Transmit FIFO Fill Flag Provides a method for the module to request more entries to be added to the TX FIFO. The TFFF bit is set while the TX FIFO is not full. The TFFF bit can be cleared by writing 1 to it or by acknowledgement from the DMA controller to the TX FIFO full request. 0 TX FIFO is full. 1 TX FIFO is not full.
24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19 RFOF	Receive FIFO Overflow Flag Indicates an overflow condition in the RX FIFO. The field is set when the RX FIFO and shift register are full and a transfer is initiated. The bit remains set until it is cleared by writing a 1 to it. 0 No Rx FIFO overflow. 1 Rx FIFO overflow has occurred.
18 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
17 RFDF	Receive FIFO Drain Flag

Table continues on the next page...

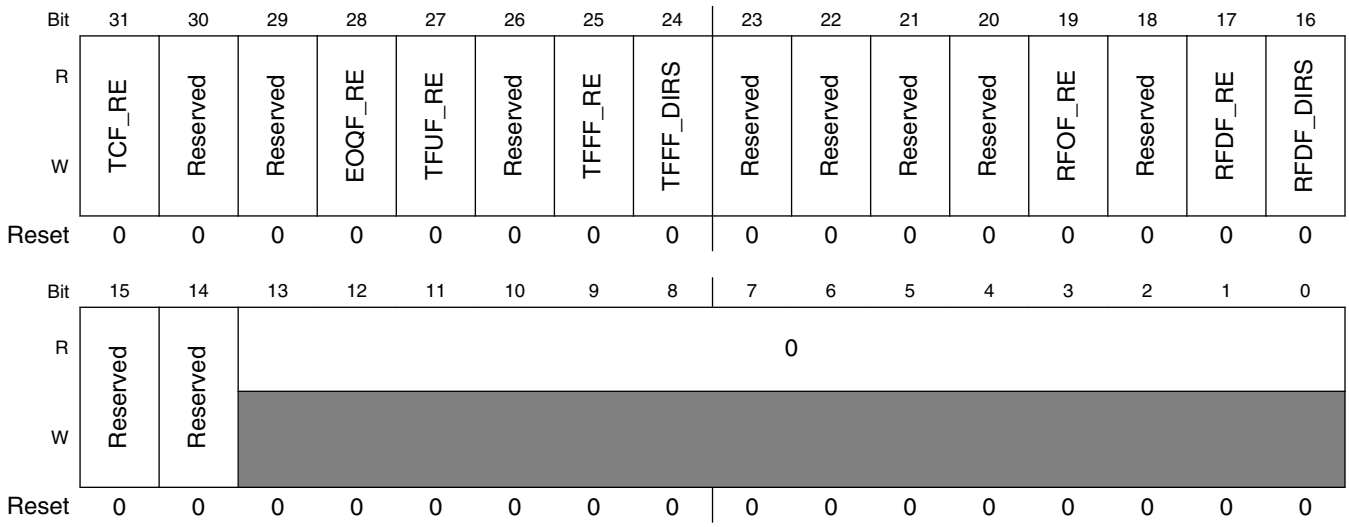
SPIx_SR field descriptions (continued)

Field	Description
	Provides a method for the module to request that entries be removed from the RX FIFO. The bit is set while the RX FIFO is not empty. The RFDF bit can be cleared by writing 1 to it or by acknowledgement from the DMA controller when the RX FIFO is empty. 0 RX FIFO is empty. 1 RX FIFO is not empty.
16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–12 TXCTR	TX FIFO Counter Indicates the number of valid entries in the TX FIFO. The TXCTR is incremented every time the PUSHR is written. The TXCTR is decremented every time an SPI command is executed and the SPI data is transferred to the shift register.
11–8 TXNXTPTR	Transmit Next Pointer Indicates which TX FIFO entry is transmitted during the next transfer. The TXNXTPTR field is updated every time SPI data is transferred from the TX FIFO to the shift register.
7–4 RXCTR	RX FIFO Counter Indicates the number of entries in the RX FIFO. The RXCTR is decremented every time the POPR is read. The RXCTR is incremented every time data is transferred from the shift register to the RX FIFO.
POPNXTPTR	Pop Next Pointer Contains a pointer to the RX FIFO entry to be returned when the POPR is read. The POPNXTPTR is updated when the POPR is read.

57.4.6 DMA/Interrupt Request Select and Enable Register (SPIx_RSER)

RSER controls DMA and interrupt requests. Do not write to the RSER while the module is in the Running state.

Address: Base address + 30h offset



SPIx_RSER field descriptions

Field	Description
31 TCF_RE	Transmission Complete Request Enable Enables TCF flag in the SR to generate an interrupt request. 0 TCF interrupt requests are disabled. 1 TCF interrupt requests are enabled.
30 Reserved	Always write the reset value to this field. This field is reserved.
29 Reserved	Always write the reset value to this field. This field is reserved.
28 EOQF_RE	Finished Request Enable Enables the EOQF flag in the SR to generate an interrupt request. 0 EOQF interrupt requests are disabled. 1 EOQF interrupt requests are enabled.
27 TFUF_RE	Transmit FIFO Underflow Request Enable Enables the TFUF flag in the SR to generate an interrupt request.

Table continues on the next page...

SPIx_RSER field descriptions (continued)

Field	Description
	0 TFUF interrupt requests are disabled. 1 TFUF interrupt requests are enabled.
26 Reserved	Always write the reset value to this field. This field is reserved.
25 TFFF_RE	Transmit FIFO Fill Request Enable Enables the TFFF flag in the SR to generate a request. The TFFF_DIRS bit selects between generating an interrupt request or a DMA request. 0 TFFF interrupts or DMA requests are disabled. 1 TFFF interrupts or DMA requests are enabled.
24 TFFF_DIRS	Transmit FIFO Fill DMA or Interrupt Request Select Selects between generating a DMA request or an interrupt request. When SR[TFFF] and RSER[TFFF_RE] are set, this field selects between generating an interrupt request or a DMA request. 0 TFFF flag generates interrupt requests. 1 TFFF flag generates DMA requests.
23 Reserved	Always write the reset value to this field. This field is reserved.
22 Reserved	Always write the reset value to this field. This field is reserved.
21 Reserved	Always write the reset value to this field. This field is reserved.
20 Reserved	Always write the reset value to this field. This field is reserved.
19 RFOF_RE	Receive FIFO Overflow Request Enable Enables the RFOF flag in the SR to generate an interrupt request. 0 RFOF interrupt requests are disabled. 1 RFOF interrupt requests are enabled.
18 Reserved	Always write the reset value to this field. This field is reserved.
17 RFDF_RE	Receive FIFO Drain Request Enable Enables the RFDF flag in the SR to generate a request. The RFDF_DIRS bit selects between generating an interrupt request or a DMA request. 0 RFDF interrupt or DMA requests are disabled. 1 RFDF interrupt or DMA requests are enabled.
16 RFDF_DIRS	Receive FIFO Drain DMA or Interrupt Request Select

Table continues on the next page...

SPIx_RSER field descriptions (continued)

Field	Description
	Selects between generating a DMA request or an interrupt request. When the RFDF flag bit in the SR is set, and the RFDF_RE bit in the RSER is set, the RFDF_DIRS bit selects between generating an interrupt request or a DMA request. 0 Interrupt request. 1 DMA request.
15 Reserved	Always write the reset value to this field. This field is reserved.
14 Reserved	Always write the reset value to this field. This field is reserved.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

57.4.7 PUSH TX FIFO Register In Master Mode (SPIx_PUSHR)

Specifies data to be transferred to the TX FIFO. An 8- or 16-bit write access transfers all 32 bits to the TX FIFO. In Master mode, the register transfers 16 bits of data and 16 bits of command information. A read access of PUSHR returns the topmost TX FIFO entry.

When the module is disabled, writing to this register does not update the FIFO. Therefore, any reads performed while the module is disabled return the last PUSHR write performed while the module was still enabled.

Address: Base address + 34h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	CONT	CTAS			EOQ	CTCNT	Reserved		Reserved		PCS					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	TXDATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPIx_PUSHR field descriptions

Field	Description
31 CONT	Continuous Peripheral Chip Select Enable Selects a continuous selection format. The bit is used in SPI Master mode. The bit enables the selected PCS signals to remain asserted between transfers. 0 Return PCSn signals to their inactive state between transfers. 1 Keep PCSn signals asserted between transfers.
30–28 CTAS	Clock and Transfer Attributes Select Selects which CTAR to use in master mode to specify the transfer attributes for the associated SPI frame. In SPI Slave mode, CTAR0 is used. See the chip specific section for details to determine how many CTARs this device has. You should not program a value in this field for a register that is not present. 000 CTAR0 001 CTAR1 010 Reserved 011 Reserved 100 Reserved 101 Reserved 110 Reserved 111 Reserved
27 EOQ	End Of Queue Host software uses this bit to signal to the module that the current SPI transfer is the last in a queue. At the end of the transfer, the EOQF bit in the SR is set. 0 The SPI data is not the last data to transfer. 1 The SPI data is the last data to transfer.
26 CTCNT	Clear Transfer Counter Clears the TCNT field in the TCR register. The TCNT field is cleared before the module starts transmitting the current SPI frame. 0 Do not clear the TCR[TCNT] field. 1 Clear the TCR[TCNT] field.
25–24 Reserved	Always write the reset value to this field. This field is reserved.
23–22 Reserved	Always write the reset value to this field. This field is reserved.
21–16 PCS	Select which PCS signals are to be asserted for the transfer. Refer to the chip-specific SPI information for the number of PCS signals used in this chip. 0 Negate the PCS[x] signal. 1 Assert the PCS[x] signal.
TXDATA	Transmit Data Holds SPI data to be transferred according to the associated SPI command.

57.4.8 PUSH TX FIFO Register In Slave Mode (SPIx_PUSHR_SLAVE)

Specifies data to be transferred to the TX FIFO in slave mode. An 8- or 16-bit write access to PUSHR transfers the 16-bit TXDATA field to the TX FIFO.

Address: Base address + 34h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved																TXDATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPIx_PUSHR_SLAVE field descriptions

Field	Description
31–16 Reserved	This field is reserved.
TXDATA	Transmit Data Holds SPI data to be transferred according to the associated SPI command.

57.4.9 POP RX FIFO Register (SPIx_POPR)

POPR is used to read the RX FIFO. Eight- or sixteen-bit read accesses to the POPR have the same effect on the RX FIFO as 32-bit read accesses. A write to this register will generate a Transfer Error.

Address: Base address + 38h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RXDATA																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPIx_POPR field descriptions

Field	Description
RXDATA	Received Data Contains the SPI data from the RX FIFO entry to which the Pop Next Data Pointer points.

57.4.10 Transmit FIFO Registers (SPIx_TXFR*n*)

TXFRn registers provide visibility into the TX FIFO for debugging purposes. Each register is an entry in the TX FIFO. The registers are read-only and cannot be modified. Reading the TXFRx registers does not alter the state of the TX FIFO.

Address: Base address + 3Ch offset + (4d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	TXCMD_TXDATA																TXDATA															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPIx_TXFR*n* field descriptions

Field	Description
31–16 TXCMD_ TXDATA	Transmit Command or Transmit Data In Master mode the TXCMD field contains the command that sets the transfer attributes for the SPI data. In Slave mode, this field is reserved.
TXDATA	Transmit Data Contains the SPI data to be shifted out.

57.4.11 Receive FIFO Registers (SPIx_RXFR*n*)

RXFRn provide visibility into the RX FIFO for debugging purposes. Each register is an entry in the RX FIFO. The RXFR registers are read-only. Reading the RXFRx registers does not alter the state of the RX FIFO.

Address: Base address + 7Ch offset + (4d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RXDATA																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPIx_RXFR*n* field descriptions

Field	Description
RXDATA	Receive Data Contains the received SPI data.

SPIx_RXFR*n* field descriptions (continued)

Field	Description

57.5 Functional description

The module supports full-duplex, synchronous serial communications between chips and peripheral devices. The SPI configuration transfers data serially using a shift register and a selection of programmable transfer attributes.

The module has the following configuration

- The SPI Configuration in which the module operates as a basic SPI or a queued SPI.

The DCONF field in the Module Configuration Register (MCR) determines the module Configuration. SPI configuration is selected when DCONF within SPIx_MCR is 0b00.

The CTARn registers hold clock and transfer attributes. The SPI configuration allows to select which CTAR to use on a frame by frame basis by setting a field in the SPI command.

See Clock and Transfer Attributes Register (In Master Mode) (SPI_CTAR*n*) for information on the fields of CTAR registers.

Typical master to slave connections are shown in the following figure. When a data transfer operation is performed, data is serially shifted a predetermined number of bit positions. Because the modules are linked, data is exchanged between the master and the slave. The data that was in the master shift register is now in the shift register of the slave, and vice versa. At the end of a transfer, the Transfer Control Flag(TCF) bit in the Shift Register(SR) is set to indicate a completed frame transfer.

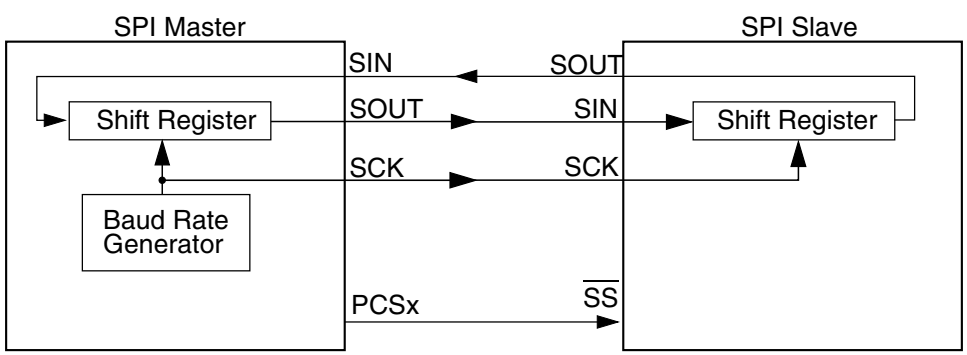


Figure 57-3. Serial protocol overview

Generally, more than one slave device can be connected to the module master. 6 Peripheral Chip Select (PCS) signals of the module masters can be used to select which of the slaves to communicate with. Refer to the chip specific section for details on the number of PCS signals used in this chip.

The SPI configuration shares transfer protocol and timing properties which are described independently of the configuration in Transfer formats. The transfer rate and delay settings are described in Module baud rate and clock delay generation.

57.5.1 Start and Stop of module transfers

The module has two operating states: Stopped and Running. Both the states are independent of it's configuration. The default state of the module is Stopped. In the Stopped state, no serial transfers are initiated in Master mode and no transfers are responded to in Slave mode. The Stopped state is also a safe state for writing the various configuration registers of the module without causing undetermined results. In the Running state serial transfers take place.

The TXRXS bit in the SR indicates the state of module. The bit is set if the module is in Running state.

The module starts or transitions to Running when all of the following conditions are true:

- SR[EOQF] bit is clear
- Chip is not in the Debug mode or the MCR[FRZ] bit is clear
- MCR[HALT] bit is clear

The module stops or transitions from Running to Stopped after the current frame when any one of the following conditions exist:

- SR[EOQF] bit is set
- Chip in the Debug mode and the MCR[FRZ] bit is set
- MCR[HALT] bit is set

State transitions from Running to Stopped occur on the next frame boundary if a transfer is in progress, or immediately if no transfers are in progress.

57.5.2 Serial Peripheral Interface (SPI) configuration

The SPI configuration transfers data serially using a shift register and a selection of programmable transfer attributes. The module is in SPI configuration when the DCONF field in the MCR is 0b00. The SPI frames can be 32 bits long. The host CPU or a DMA controller transfers the SPI data from the external to the module RAM queues to a TX FIFO buffer. The received data is stored in entries in the RX FIFO buffer. The host CPU or the DMA controller transfers the received data from the RX FIFO to memory external to the module. The operation of FIFO buffers is described in the following sections:

- Transmit First In First Out (TX FIFO) buffering mechanism
- Transmit First In First Out (TX FIFO) buffering mechanism
- Receive First In First Out (RX FIFO) buffering mechanism

The interrupt and DMA request conditions are described in Interrupts/DMA requests.

The SPI configuration supports two block-specific modes—Master mode and Slave mode.In Master mode the module initiates and controls the transfer according to the fields of the executing SPI Command. In Slave mode, the module responds only to transfers initiated by a bus master external to it and the SPI command field space is reserved.

57.5.2.1 Master mode

In SPI Master mode, the module initiates the serial transfers by controlling the SCK and the PCS signals. The executing SPI Command determines which CTARs will be used to set the transfer attributes and which PCS signals to assert. The command field also contains various bits that help with queue management and transfer protocol. See PUSH TX FIFO Register In Master Mode (SPI_PUSHR) for details on the SPI command fields. The data in the executing TX FIFO entry is loaded into the shift register and shifted out on the Serial Out (SOUT) pin. In SPI Master mode, each SPI frame to be transmitted has a command associated with it, allowing for transfer attribute control on a frame by frame basis.

57.5.2.2 Slave mode

In SPI Slave mode the module responds to transfers initiated by an SPI bus master. It does not initiate transfers. Certain transfer attributes such as clock polarity, clock phase, and frame size must be set for successful communication with an SPI master. The SPI Slave mode transfer attributes are set in the CTAR0. The data is shifted out with MSB first. Shifting out of LSB is not supported in this mode.

57.5.2.3 FIFO disable operation

The FIFO disable mechanisms allow SPI transfers without using the TX FIFO or RX FIFO. The module operates as a double-buffered simplified SPI when the FIFOs are disabled. The Transmit and Receive side of the FIFOs are disabled separately. Setting the MCR[DIS_TXF] bit disables the TX FIFO, and setting the MCR[DIS_RXF] bit disables the RX FIFO.

The FIFO disable mechanisms are transparent to the user and to host software. Transmit data and commands are written to the PUSHR and received data is read from the POPR.

When the TX FIFO is disabled:

- SR[TFFF], SR[TFUF] and SR[TXCTR] behave as if there is a one-entry FIFO
- The contents of TXFRs, SR[TXNXTPTR] are undefined

Similarly, when the RX FIFO is disabled, the RFDF, RFOF, and RXCTR fields in the SR behave as if there is a one-entry FIFO, but the contents of the RXFR registers and POPNXTPTR are undefined.

57.5.2.4 Transmit First In First Out (TX FIFO) buffering mechanism

The TX FIFO functions as a buffer of SPI data for transmission. The TX FIFO holds 4 words, each consisting of SPI data. The number of entries in the TX FIFO is device-specific. SPI data is added to the TX FIFO by writing to the Data Field of module PUSH FIFO Register (PUSHR). TX FIFO entries can only be removed from the TX FIFO by being shifted out or by flushing the TX FIFO.

The TX FIFO Counter field (TXCTR) in the module Status Register (SR) indicates the number of valid entries in the TX FIFO. The TXCTR is updated every time a 8- or 16-bit write takes place to PUSHR[TXDATA] or SPI data is transferred into the shift register from the TX FIFO.

The TXNXTPTR field indicates the TX FIFO Entry that will be transmitted during the next transfer. The TXNXTPTR field is incremented every time SPI data is transferred from the TX FIFO to the shift register. The maximum value of the field is equal to the maximum implemented TXFR number and it rolls over after reaching the maximum.

57.5.2.4.1 Filling the TX FIFO

Host software or other intelligent blocks can add (push) entries to the TX FIFO by writing to the PUSHR. When the TX FIFO is not full, the TX FIFO Fill Flag (TFFF) in the SR is set. The TFFF bit is cleared when TX FIFO is full and the DMA controller

indicates that a write to PUSHR is complete. Writing a '1' to the TFFF bit also clears it. The TFFF can generate a DMA request or an interrupt request. See Transmit FIFO Fill Interrupt or DMA Request for details.

The module ignores attempts to push data to a full TX FIFO, and the state of the TX FIFO does not change and no error condition is indicated.

57.5.2.4.2 Draining the TX FIFO

The TX FIFO entries are removed (drained) by shifting SPI data out through the shift register. Entries are transferred from the TX FIFO to the shift register and shifted out as long as there are valid entries in the TX FIFO. Every time an entry is transferred from the TX FIFO to the shift register, the TX FIFO Counter decrements by one. At the end of a transfer, the TCF bit in the SR is set to indicate the completion of a transfer. The TX FIFO is flushed by writing a '1' to the CLR_TXF bit in MCR.

If an external bus master initiates a transfer with a module slave while the slave's TX FIFO is empty, the Transmit FIFO Underflow Flag (TFUF) in the slave's SR is set. See Transmit FIFO Underflow Interrupt Request for details.

57.5.2.5 Receive First In First Out (RX FIFO) buffering mechanism

The RX FIFO functions as a buffer for data received on the SIN pin. The RX FIFO holds 4 received SPI data frames. The number of entries in the RX FIFO is device-specific. SPI data is added to the RX FIFO at the completion of a transfer when the received data in the shift register is transferred into the RX FIFO. SPI data are removed (popped) from the RX FIFO by reading the module POP RX FIFO Register (POPR). RX FIFO entries can only be removed from the RX FIFO by reading the POPR or by flushing the RX FIFO.

The RX FIFO Counter field (RXCTR) in the module's Status Register (SR) indicates the number of valid entries in the RX FIFO. The RXCTR is updated every time the POPR is read or SPI data is copied from the shift register to the RX FIFO.

The POPNXTPTR field in the SR points to the RX FIFO entry that is returned when the POPR is read. The POPNXTPTR contains the positive offset from RXFR0 in a number of 32-bit registers. For example, POPNXTPTR equal to two means that the RXFR2 contains the received SPI data that will be returned when the POPR is read. The POPNXTPTR field is incremented every time the POPR is read. The maximum value of the field is equal to the maximum implemented RXFR number and it rolls over after reaching the maximum.

57.5.2.5.1 Filling the RX FIFO

The RX FIFO is filled with the received SPI data from the shift register. While the RX FIFO is not full, SPI frames from the shift register are transferred to the RX FIFO. Every time an SPI frame is transferred to the RX FIFO, the RX FIFO Counter is incremented by one.

If the RX FIFO and shift register are full and a transfer is initiated, the RFOF bit in the SR is set indicating an overflow condition. Depending on the state of the ROOE bit in the MCR, the data from the transfer that generated the overflow is either ignored or shifted in to the shift register. If the ROOE bit is set, the incoming data is shifted in to the shift register. If the ROOE bit is cleared, the incoming data is ignored.

57.5.2.5.2 Draining the RX FIFO

Host CPU or a DMA can remove (pop) entries from the RX FIFO by reading the module POP RX FIFO Register (POPR). A read of the POPR decrements the RX FIFO Counter by one. Attempts to pop data from an empty RX FIFO are ignored and the RX FIFO Counter remains unchanged. The data, read from the empty RX FIFO, is undetermined.

When the RX FIFO is not empty, the RX FIFO Drain Flag (RFDF) in the SR is set. The RFDF bit is cleared when the RX_FIFO is empty and the DMA controller indicates that a read from POPR is complete or by writing a 1 to it.

57.5.3 Module baud rate and clock delay generation

The SCK frequency and the delay values for serial transfer are generated by dividing the system clock frequency by a prescaler and a scaler with the option for doubling the baud rate. The following figure shows conceptually how the SCK signal is generated.

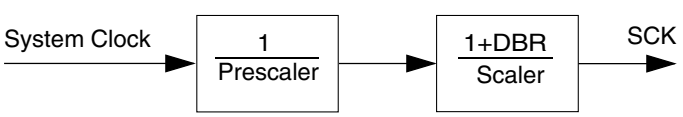


Figure 57-4. Communications clock prescalers and scalers

57.5.3.1 Baud rate generator

The baud rate is the frequency of the SCK. The protocol clock is divided by a prescaler (PBR) and scaler (BR) to produce SCK with the possibility of halving the scaler division. The DBR, PBR, and BR fields in the CTARs select the frequency of SCK by the formula in the BR field description. The following table shows an example of how to compute the baud rate.

Table 57-9. Baud rate computation example

f_P	PBR	Prescaler	BR	Scaler	DBR	Baud rate
100 MHz	0b00	2	0b0000	2	0	25 Mb/s
20 MHz	0b00	2	0b0000	2	1	10 Mb/s

NOTE

The clock frequencies mentioned in the preceding table are given as an example. Refer to the clocking chapter for the frequency used to drive this module in the device.

57.5.3.2 PCS to SCK Delay (t_{CSC})

The PCS to SCK delay is the length of time from assertion of the PCS signal to the first SCK edge. See Figure 57-6 for an illustration of the PCS to SCK delay. The PCSSCK and CSSCK fields in the CTAR*x* registers select the PCS to SCK delay by the formula in the CSSCK field description. The following table shows an example of how to compute the PCS to SCK delay.

Table 57-10. PCS to SCK delay computation example

f_{SYS}	PCSSCK	Prescaler	CSSCK	Scaler	PCS to SCK Delay
100 MHz	0b01	3	0b0100	32	0.96 µs

NOTE

The clock frequency mentioned in the preceding table is given as an example. Refer to the clocking chapter for the frequency used to drive this module in the device.

57.5.3.3 After SCK Delay (t_{ASC})

The After SCK Delay is the length of time between the last edge of SCK and the negation of PCS. See Figure 57-6 and Figure 57-7 for illustrations of the After SCK delay. The PASC and ASC fields in the CTAR*x* registers select the After SCK Delay by the formula in the ASC field description. The following table shows an example of how to compute the After SCK delay.

Table 57-11. After SCK Delay computation example

f_P	PASC	Prescaler	ASC	Scaler	After SCK Delay
100 MHz	0b01	3	0b0100	32	0.96 µs

NOTE

The clock frequency mentioned in the preceding table is given as an example. Refer to the clocking chapter for the frequency used to drive this module in the device.

57.5.3.4 Delay after Transfer (t_{DT})

The Delay after Transfer is the minimum time between negation of the PCS signal for a frame and the assertion of the PCS signal for the next frame. See Figure 57-6 for an illustration of the Delay after Transfer. The PDT and DT fields in the CTAR*x* registers select the Delay after Transfer by the formula in the DT field description. The following table shows an example of how to compute the Delay after Transfer.

Table 57-12. Delay after Transfer computation example

f_P	PDT	Prescaler	DT	Scaler	Delay after Transfer
100 MHz	0b01	3	0b1110	32768	0.98 ms

NOTE

The clock frequency mentioned in the preceding table is given as an example. Refer to the clocking chapter for the frequency used to drive this module in the device.

When in Non-Continuous Clock mode the t_{DT} delay is configured according to the equation specified in the CTAR[DT] field description. When in Continuous Clock mode, the delay is fixed at 1 SCK period.

57.5.3.5 Peripheral Chip Select Strobe Enable ($\overline{\text{PCSS}}$)

The $\overline{\text{PCSS}}$ signal provides a delay to allow the PCS signals to settle after a transition occurs thereby avoiding glitches. When the Module is in Master mode and the PCSSE bit is set in the MCR, $\overline{\text{PCSS}}$ provides a signal for an external demultiplexer to decode peripheral chip selects other than PCS5 into glitch-free PCS signals. The following figure shows the timing of the $\overline{\text{PCSS}}$ signal relative to PCS signals.

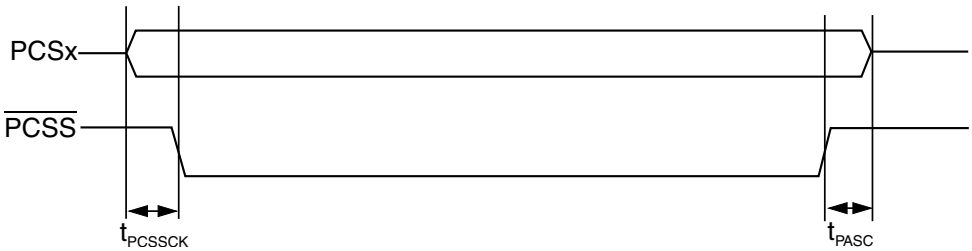


Figure 57-5. Peripheral Chip Select Strobe timing

The delay between the assertion of the PCS signals and the assertion of $\overline{\text{PCSS}}$ is selected by the PCSSCK field in the CTAR based on the following formula:

$$t_{\text{PCSSCK}} = \frac{1}{f_P} \times \text{PCSSCK}$$

At the end of the transfer, the delay between $\overline{\text{PCSS}}$ negation and PCS negation is selected by the PASC field in the CTAR based on the following formula:

$$t_{\text{PASC}} = \frac{1}{f_P} \times \text{PASC}$$

The following table shows an example of how to compute the t_{pcssck} delay.

Table 57-13. Peripheral Chip Select Strobe Assert computation example

f_P	PCSSCK	Prescaler	Delay before Transfer
100 MHz	0b11	7	70.0 ns

The following table shows an example of how to compute the t_{pasc} delay.

Table 57-14. Peripheral Chip Select Strobe Negate computation example

f_P	PASC	Prescaler	Delay after Transfer
100 MHz	0b11	7	70.0 ns

The $\overline{\text{PCSS}}$ signal is not supported when Continuous Serial Communication SCK mode is enabled.

NOTE

The clock frequency mentioned in the preceding tables is given as an example. Refer to the clocking chapter for the frequency used to drive this module in the device.

57.5.4 Transfer formats

The SPI serial communication is controlled by the Serial Communications Clock (SCK) signal and the PCS signals. The SCK signal provided by the master device synchronizes shifting and sampling of the data on the SIN and SOUT pins. The PCS signals serve as enable signals for the slave devices.

In Master mode, the CPOL and CPHA bits in the Clock and Transfer Attributes Registers (CTARn) select the polarity and phase of the serial clock, SCK.

- CPOL - Selects the idle state polarity of the SCK
- CPHA - Selects if the data on SOUT is valid before or on the first SCK edge

Even though the bus slave does not control the SCK signal, in Slave mode the values of CPOL and CPHA must be identical to the master device settings to ensure proper transmission. In SPI Slave mode, only CTAR0 is used.

The module supports four different transfer formats:

- Classic SPI with CPHA=0
- Classic SPI with CPHA=1
- Modified Transfer Format with CPHA = 0
- Modified Transfer Format with CPHA = 1

A modified transfer format is supported to allow for high-speed communication with peripherals that require longer setup times. The module can sample the incoming data later than halfway through the cycle to give the peripheral more setup time. The MTFE bit in the MCR selects between Classic SPI Format and Modified Transfer Format.

In the interface configurations, the module provides the option of keeping the PCS signals asserted between frames. See Continuous Selection Format for details.

57.5.4.1 Classic SPI Transfer Format (CPHA = 0)

The transfer format shown in following figure is used to communicate with peripheral SPI slave devices where the first data bit is available on the first clock edge. In this format, the master and slave sample their SIN pins on the odd-numbered SCK edges and change the data on their SOUT pins on the even-numbered SCK edges.

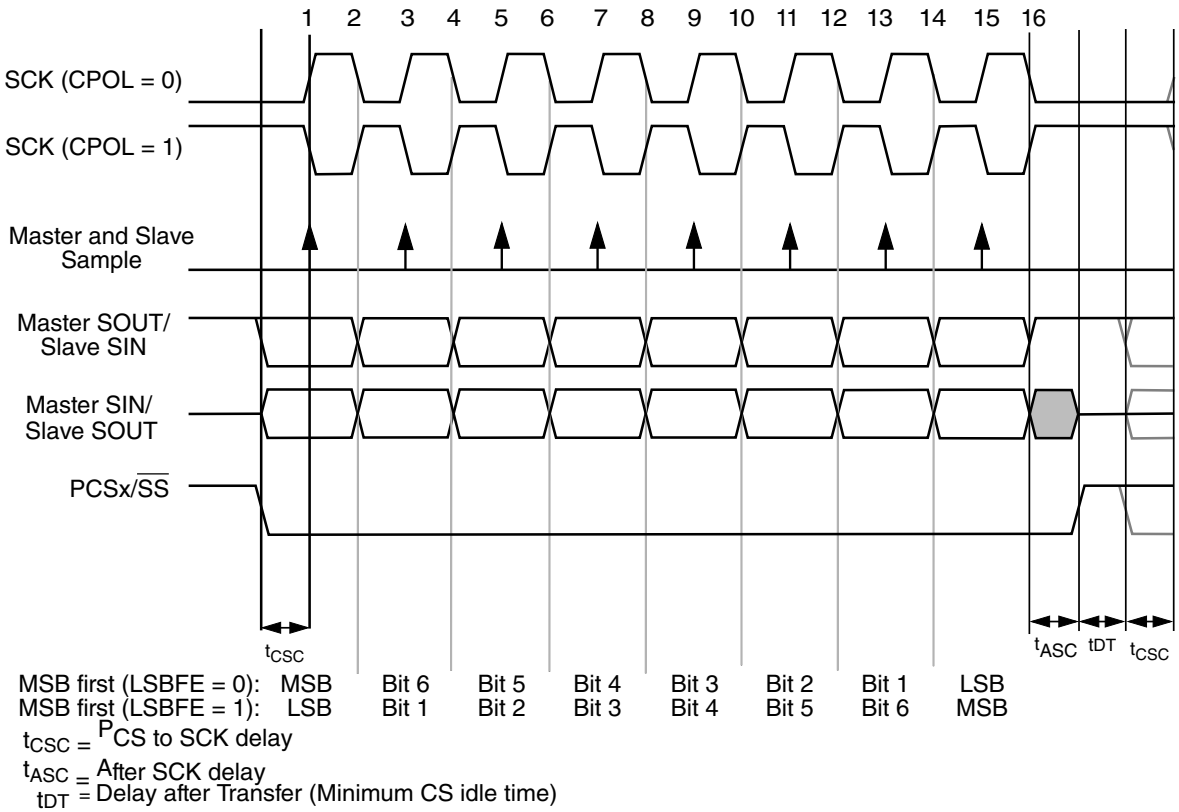


Figure 57-6. Module transfer timing diagram (MTFE=0, CPHA=0, FMSZ=8)

The master initiates the transfer by placing its first data bit on the SOUT pin and asserting the appropriate peripheral chip select signals to the slave device. The slave responds by placing its first data bit on its SOUT pin. After the t_{CSC} delay elapses, the master outputs the first edge of SCK. The master and slave devices use this edge to sample the first input data bit on their serial data input signals. At the second edge of the SCK, the master and slave devices place their second data bit on their serial data output signals. For the rest of the frame the master and the slave sample their SIN pins on the odd-numbered clock edges and changes the data on their SOUT pins on the even-numbered clock edges. After the last clock edge occurs, a delay of t_{ASC} is inserted before the master negates the PCS signals. A delay of t_{DT} is inserted before a new frame transfer can be initiated by the master.

57.5.4.2 Classic SPI Transfer Format (CPHA = 1)

This transfer format shown in the following figure is used to communicate with peripheral SPI slave devices that require the first SCK edge before the first data bit becomes available on the slave SOUT pin. In this format, the master and slave devices change the data on their SOUT pins on the odd-numbered SCK edges and sample the data on their SIN pins on the even-numbered SCK edges.

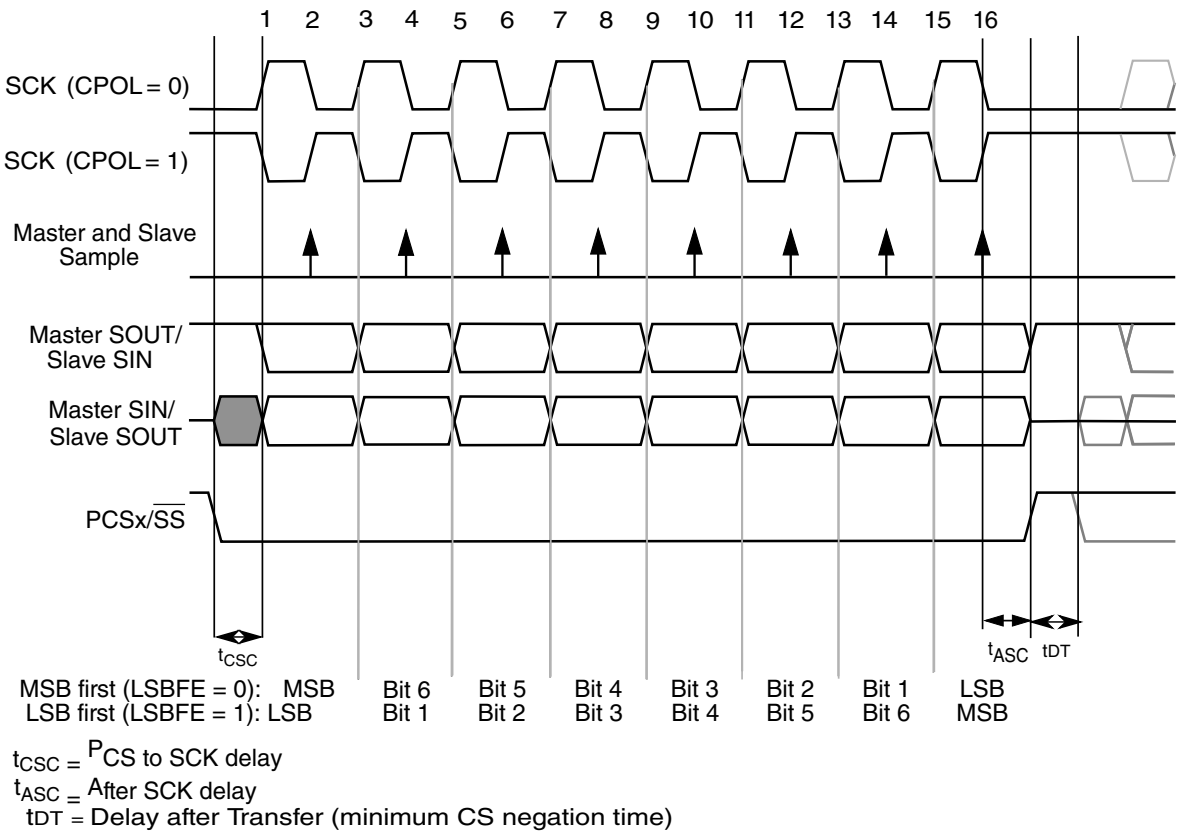


Figure 57-7. Module transfer timing diagram (MTFE=0, CPHA=1, FMSZ=8)

The master initiates the transfer by asserting the PCS signal to the slave. After the t_{CSC} delay has elapsed, the master generates the first SCK edge and at the same time places valid data on the master SOUT pin. The slave responds to the first SCK edge by placing its first data bit on its slave SOUT pin.

At the second edge of the SCK the master and slave sample their SIN pins. For the rest of the frame the master and the slave change the data on their SOUT pins on the odd-numbered clock edges and sample their SIN pins on the even-numbered clock edges. After the last clock edge occurs, a delay of t_{ASC} is inserted before the master negates the PCS signal. A delay of t_{DT} is inserted before a new frame transfer can be initiated by the master.

57.5.4.3 Modified SPI Transfer Format (MTFE = 1, CPHA = 0)

In this Modified Transfer Format both the master and the slave sample later in the SCK period than in Classic SPI mode to allow the logic to tolerate more delays in device pads and board traces. These delays become a more significant fraction of the SCK period as the SCK period decreases with increasing baud rates.

The master and the slave place data on the SOUT pins at the assertion of the PCS signal. After the PCS to SCK delay has elapsed the first SCK edge is generated. The slave samples the master SOUT signal on every odd numbered SCK edge. The DSPI in the slave mode when the MTFE bit is set also places new data on the slave SOUT on every odd numbered clock edge. Regular external slave, configured with CPHA=0 format drives its SOUT output at every even numbered SCK clock edge.

The DSPI master places its second data bit on the SOUT line one protocol clock after odd numbered SCK edge if the protocol clock frequency to SCK frequency ratio is higher than three. If this ratio is below four the master changes SOUT at odd numbered SCK edge. The point where the master samples the SIN is selected by the DSPI_MCR[SMPL_PT] field. The master sample point can be delayed by one or two protocol clock cycles. The SMPL_PT field should be set to 0 if the protocol to SCK frequency ratio is less than 4. However if this ratio is less than 4, the actual sample point is delayed by one protocol clock cycle automatically by the design.

The following timing diagrams illustrate the DSPI operation with MTFE=1. Timing delays shown are:

- T_{csc} - PCS to SCK assertion delay
- T_{acs} - After SCK PCS negation delay
- T_{su_ms} - master SIN setup time
- T_{hd_ms} - master SIN hold time
- T_{vd_sl} - slave data output valid time, time between slave data output SCK driving edge and data becomes valid.
- T_{su_sl} - data setup time on slave data input
- T_{hd_sl} - data hold time on slave data input
- T_{sys} - protocol clock period.

The following figure shows the modified transfer format for CPHA = 0 and Fsys/Fsck = 4. Only the condition where CPOL = 0 is illustrated. Solid triangles show the data sampling clock edges. The two possible slave behavior are shown.

- Signal, marked "SOUT of Ext Slave", presents regular SPI slave serial output.
- Signal, marked "SOUT of DSPI Slave", presents DSPI in the slave mode with MTFE bit set.

Other MTFE = 1 diagrams show DSPI SIN input as being driven by a regular external SPI slave, configured according DSPI master CPHA programming.

Note

In the following diagrams, f_{sys} represents the protocol clock frequency from which the Baud frequency f_{sck} is derived.

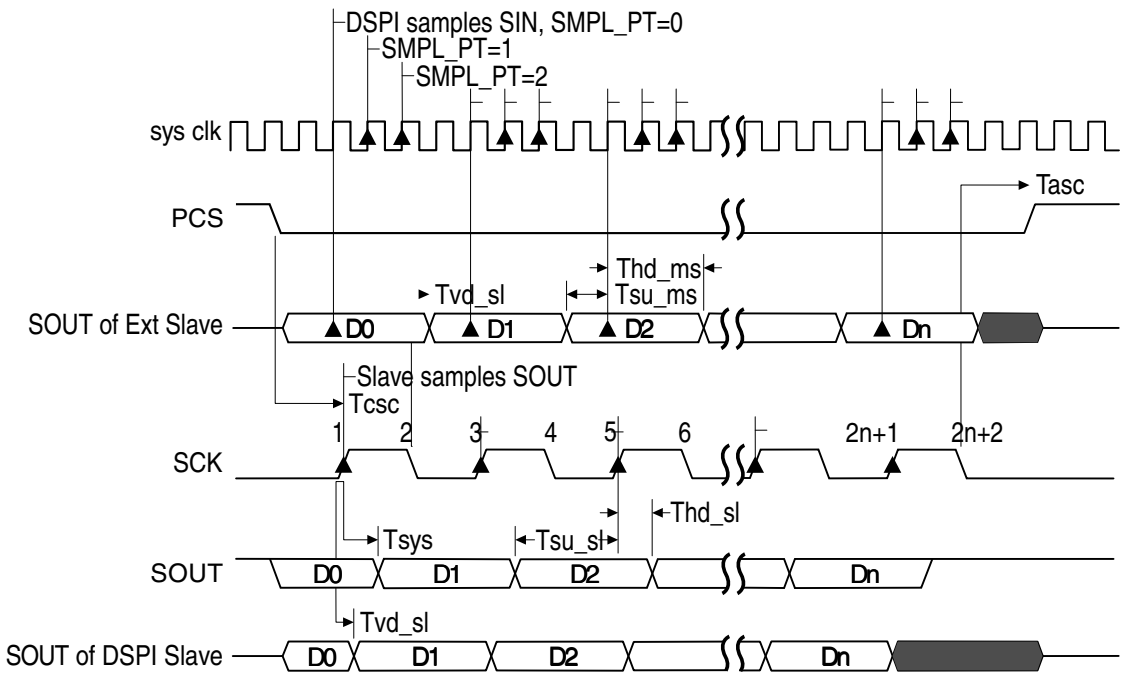


Figure 57-8. DSPI Modified Transfer Format (MTFE=1, CPHA=0, $f_{sck} = f_{sys}/4$)

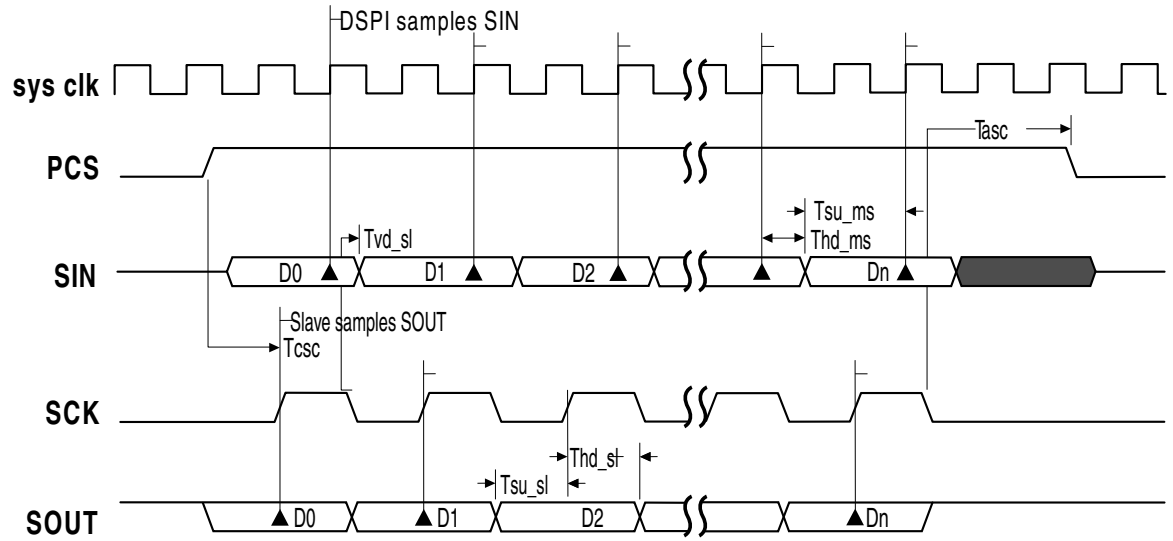


Figure 57-9. DSPI Modified Transfer Format (MTFE=1, CPHA=0, $f_{sck} = f_{sys}/2$)

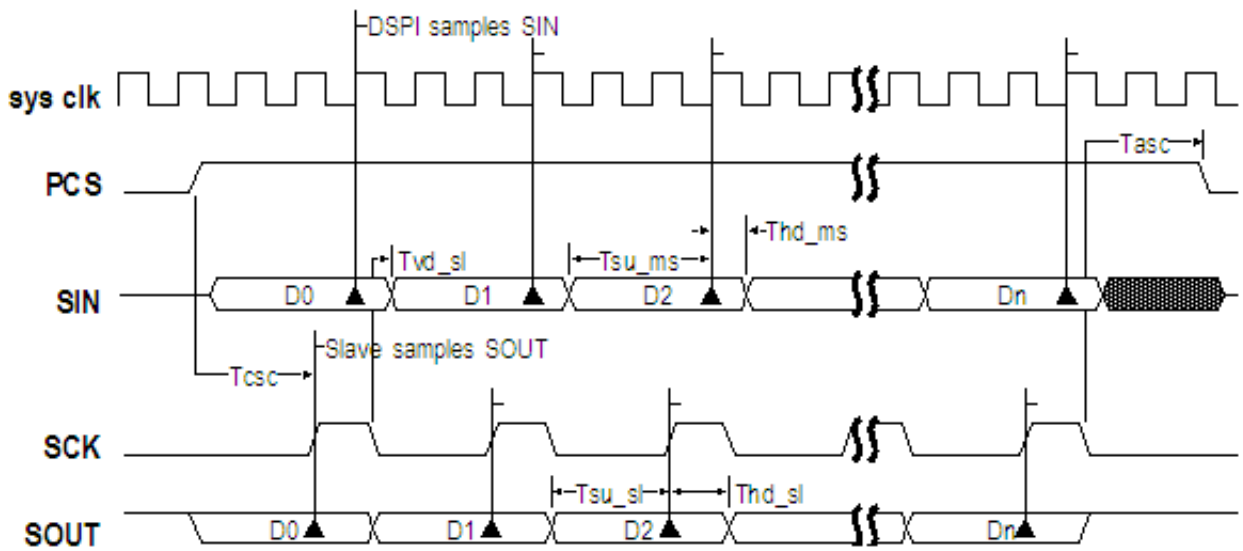


Figure 57-10. DSPI Modified Transfer Format (MTFE=1, CPHA=0, $f_{sck} = f_{sys}/3$)

57.5.4.4 Modified SPI Transfer Format (MTFE = 1, CPHA = 1)

The following figures show the Modified Transfer Format for CPHA = 1. Only the condition, where CPOL = 0 is shown. At the start of a transfer the DSPI asserts the PCS signal to the slave device. After the PCS to SCK delay has elapsed the master and the slave put data on their SOUT pins at the first edge of SCK . The slave samples the master SOUT signal on the even numbered edges of SCK. The master samples the slave SOUT

signal on the odd numbered SCK edges starting with the third SCK edge. The slave samples the last bit on the last edge of the SCK. The master samples the last slave SOUT bit one half SCK cycle after the last edge of SCK. No clock edge will be visible on the master SCK pin during the sampling of the last bit. **The SCK to PCS delay and the After SCK delay must be greater or equal to half of the SCK period.**

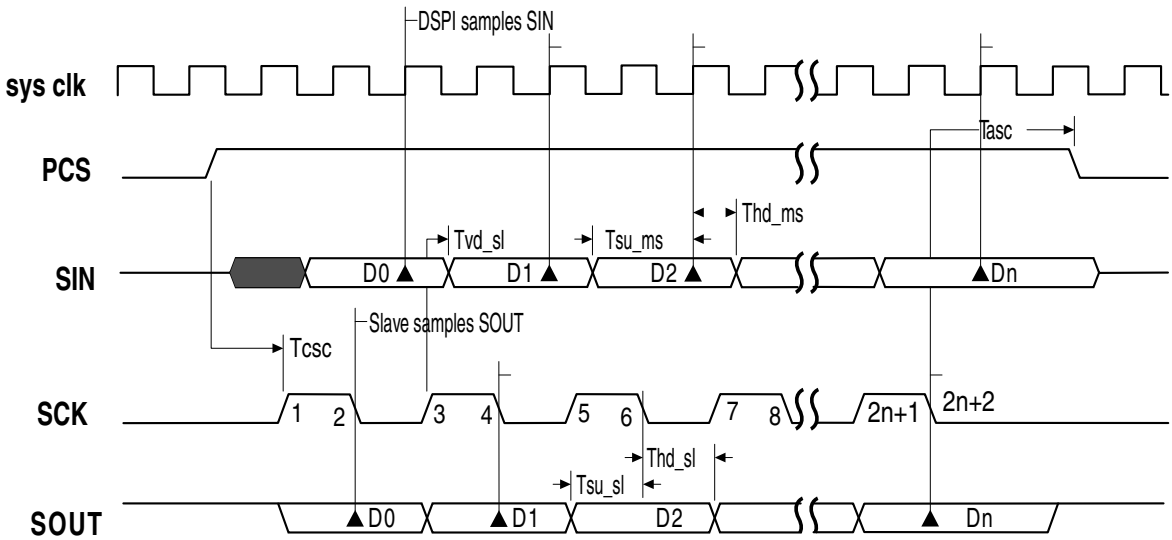


Figure 57-11. DSPI Modified Transfer Format (MTFE=1, CPHA=1, $f_{sck} = f_{sys}/2$)

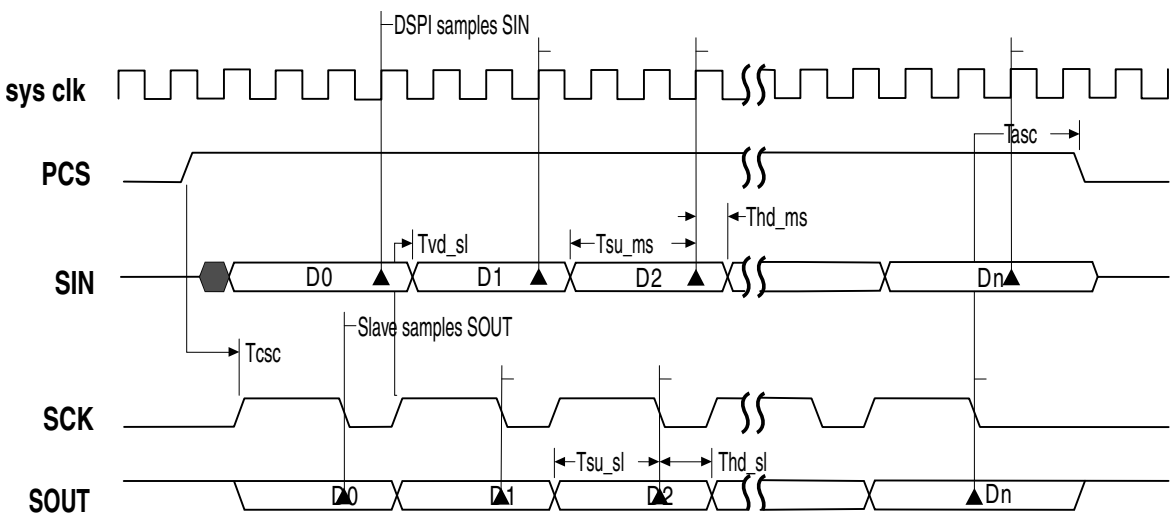


Figure 57-12. DSPI Modified Transfer Format (MTFE=1, CPHA=1, $f_{sck} = f_{sys}/3$)

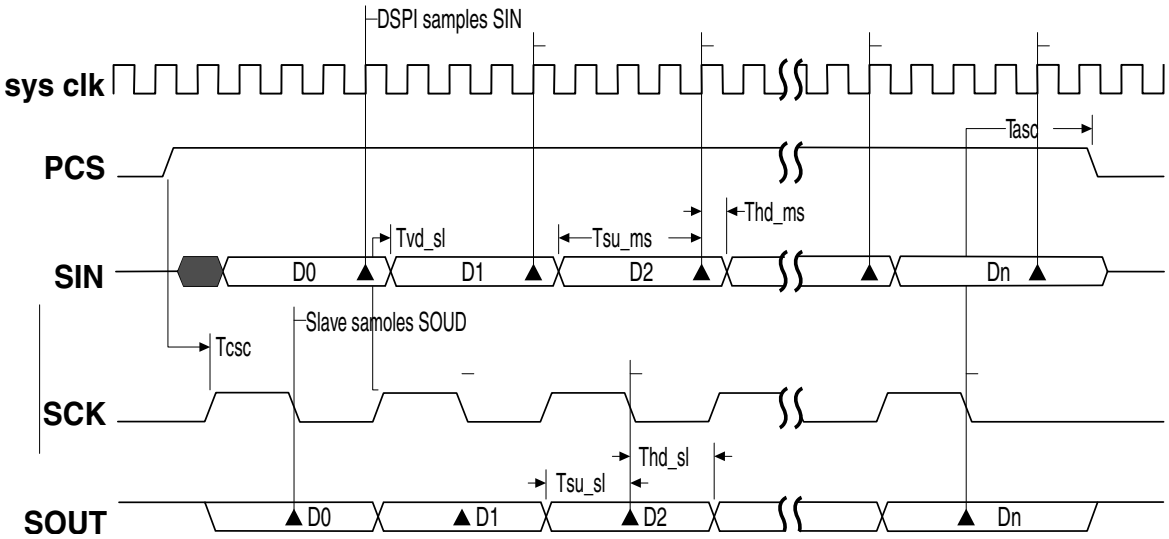


Figure 57-13. DSPI Modified Transfer Format (MTFE=1, CPHA=1, $f_{sck} = f_{sys}/4$)

57.5.4.5 Continuous Selection Format

Some peripherals must be deselected between every transfer. Other peripherals must remain selected between several sequential serial transfers. The Continuous Selection Format provides the flexibility to handle the following case. The Continuous Selection Format is enabled for the SPI configuration by setting the CONT bit in the SPI command.

When the CONT bit = 0, the module drives the asserted Chip Select signals to their idle states in between frames. The idle states of the Chip Select signals are selected by the PCSISn bits in the MCR. The following timing diagram is for two four-bit transfers with CPHA = 1 and CONT = 0.

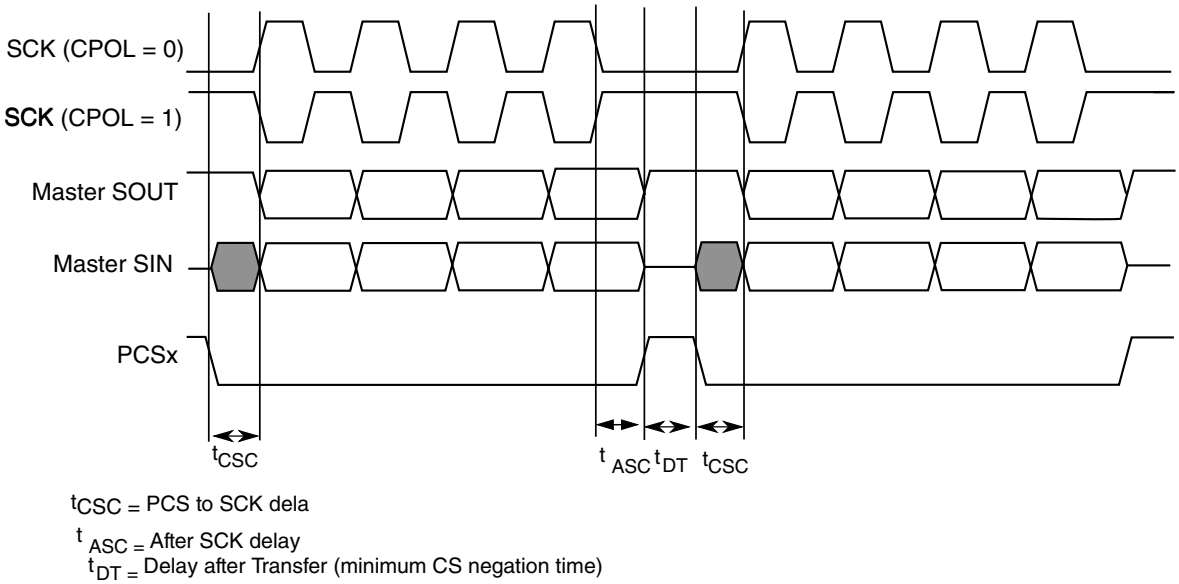


Figure 57-14. Example of non-continuous format (CPHA=1, CONT=0)

When the CONT bit = 1, the PCS signal remains asserted for the duration of the two transfers. The Delay between Transfers (t_{DT}) is not inserted between the transfers. The following figure shows the timing diagram for two four-bit transfers with CPHA = 1 and CONT = 1.

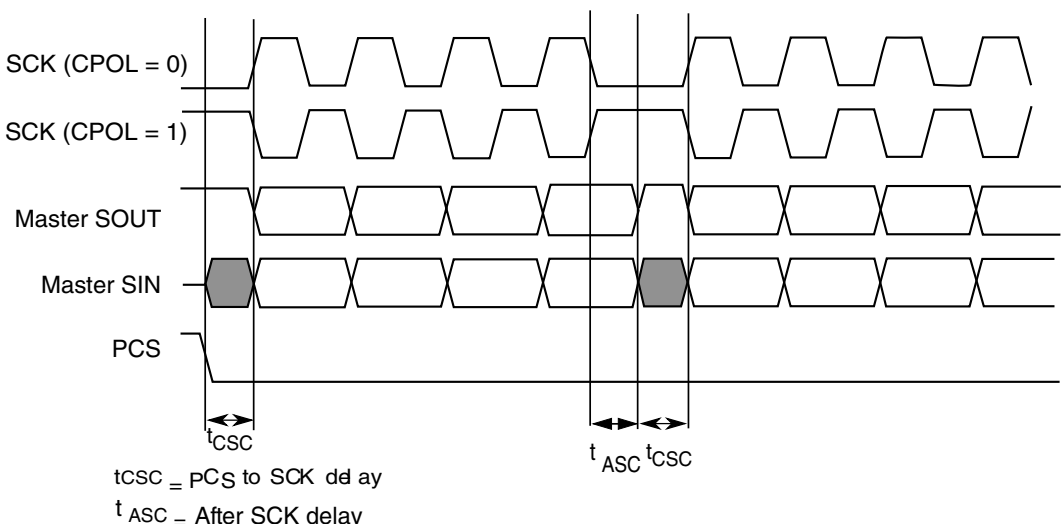


Figure 57-15. Example of continuous transfer (CPHA=1, CONT=1)

When using the module with continuous selection follow these rules:

- All transmit commands must have the same PCSn bits programming.
- The CTARs, selected by transmit commands, must be programmed with the same transfer attributes. Only FMSZ field can be programmed differently in these CTARs.

- When transmitting multiple frames in this mode, the user software must ensure that the last frame has the PUSHR[CONT] bit deasserted in Master mode and the user software must provide sufficient frames in the TX_FIFO to be sent out in Slave mode and the master deasserts the PCSn at end of transmission of the last frame.
- PUSHR[CONT] must be deasserted before asserting MCR[HALT] in master mode. This will make sure that the PCSn signals are deasserted. Asserting MCR[HALT] during continuous transfer will cause the PCSn signals to remain asserted and hence Slave Device cannot transition from Running to Stopped state.

NOTE

User must fill the TX FIFO with the number of entries that will be concatenated together under one PCS assertion for both master and slave before the TX FIFO becomes empty.

When operating in Slave mode, ensure that when the last entry in the TX FIFO is completely transmitted, that is, the corresponding TCF flag is asserted and TXFIFO is empty, the slave is deselected for any further serial communication; otherwise, an underflow error occurs.

57.5.5 Continuous Serial Communications Clock

The module provides the option of generating a Continuous SCK signal for slave peripherals that require a continuous clock.

Continuous SCK is enabled by setting the CONT_SCKE bit in the MCR. Enabling this bit generates the Continuous SCK only if MCR[HALT] bit is low. Continuous SCK is valid in all configurations.

Continuous SCK is only supported for CPHA=1. Clearing CPHA is ignored if the CONT_SCKE bit is set. Continuous SCK is supported for Modified Transfer Format.

Clock and transfer attributes for the Continuous SCK mode are set according to the following rules:

- When the module is in SPI configuration, CTAR0 is used initially. At the start of each SPI frame transfer, the CTAR specified by the CTAS for the frame is used.
- In all configurations, the currently selected CTAR remains in use until the start of a frame with a different CTAR specified, or the Continuous SCK mode is terminated.

It is recommended to keep the baud rate the same while using the Continuous SCK. Switching clock polarity between frames while using Continuous SCK can cause errors in the transfer. Continuous SCK operation is not guaranteed if the module is put into the External Stop mode or Module Disable mode.

Enabling Continuous SCK disables the PCS to SCK delay and the Delay after Transfer (t_{DT}) is fixed to one SCK cycle. The following figure is the timing diagram for Continuous SCK format with Continuous Selection disabled.

NOTE

In Continuous SCK mode, for the SPI transfer CTAR0 should always be used, and the TX FIFO must be cleared using the MCR[CLR_TXF] field before initiating transfer.

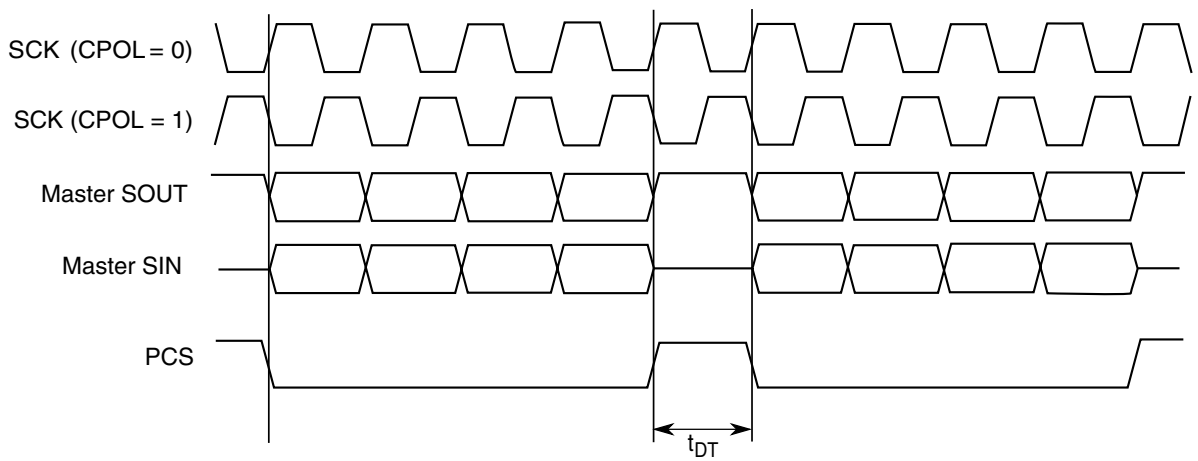


Figure 57-16. Continuous SCK Timing Diagram (CONT=0)

If the CONT bit in the TX FIFO entry is set, PCS remains asserted between the transfers. Under certain conditions, SCK can continue with PCS asserted, but with no data being shifted out of SOUT, that is, SOUT pulled high. This can cause the slave to receive incorrect data. Those conditions include:

- Continuous SCK with CONT bit set, but no data in the TX FIFO.
- Continuous SCK with CONT bit set and entering Stopped state (refer to Start and Stop of module transfers).
- Continuous SCK with CONT bit set and entering Stop mode or Module Disable mode.

The following figure shows timing diagram for Continuous SCK format with Continuous Selection enabled.

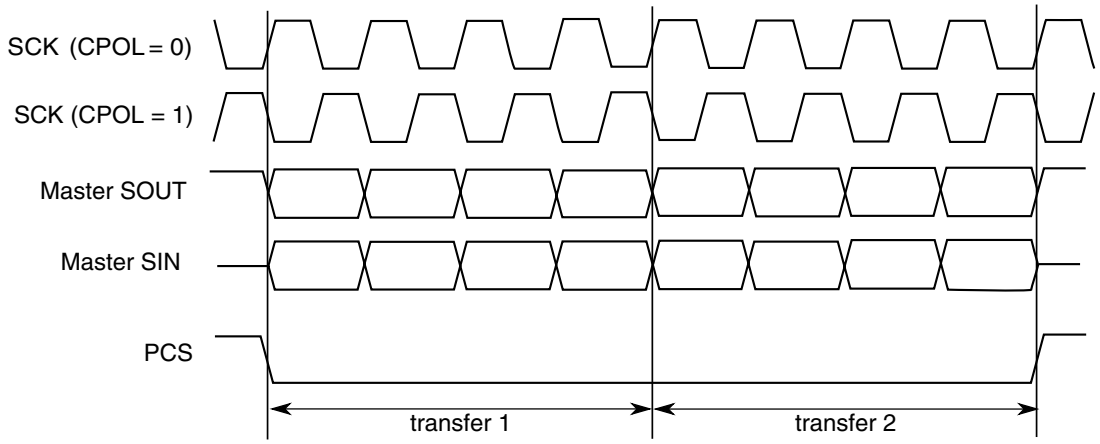


Figure 57-17. Continuous SCK timing diagram (CONT=1)

57.5.6 Slave Mode Operation Constraints

Slave mode logic shift register is buffered. This allows data streaming operation, when the module is permanently selected and data is shifted in with a constant rate.

The transmit data is transferred at second SCK clock edge of the each frame to the shift register if the $\overline{SS}$ signal is asserted and any time when transmit data is ready and $\overline{SS}$ signal is negated.

Received data is transferred to the receive buffer at last SCK edge of each frame, defined by frame size programmed to the CTAR0/1 register. Then the data from the buffer is transferred to the RXFIFO or DDR register.

If the $\overline{SS}$ negates before that last SCK edge, the data from shift register is lost.

57.5.7 Interrupts/DMA requests

The module has several conditions that can generate only interrupt requests and two conditions that can generate interrupt or DMA requests. The following table lists these conditions.

Table 57-15. Interrupt and DMA request conditions

Condition	Flag	Interrupt	DMA
End of Queue (EOQ)	EOQF	Yes	-
TX FIFO Fill	TFFF	Yes	Yes
Transfer Complete	TCF	Yes	-
TX FIFO Underflow	TFUF	Yes	-

Table continues on the next page...

Table 57-15. Interrupt and DMA request conditions (continued)

Condition	Flag	Interrupt	DMA
RX FIFO Drain	RFDF	Yes	Yes
RX FIFO Overflow	RFOF	Yes	-

Each condition has a flag bit in the module Status Register (SR) and a Request Enable bit in the DMA/Interrupt Request Select and Enable Register (RSER). Certain flags (as shown in above table) generate interrupt requests or DMA requests depending on configuration of RSER register.

57.5.7.1 End Of Queue interrupt request

The End Of Queue (EOQ) interrupt request indicates that the end of a transmit queue is reached. The module generates the interrupt request when EOQ interrupt requests are enabled (RSER[EOQF_RE]) and the EOQ bit in the executing SPI command is 1.

The module generates the interrupt request when the last bit of the SPI frame with EOQ bit set is transmitted.

57.5.7.2 Transmit FIFO Fill Interrupt or DMA Request

The Transmit FIFO Fill Request indicates that the TX FIFO is not full. The Transmit FIFO Fill Request is generated when the number of entries in the TX FIFO is less than the maximum number of possible entries, and the TFFF_RE bit in the RSER is set. The TFFF_DIRS bit in the RSER selects whether a DMA request or an interrupt request is generated.

NOTE

TFFF flag clears automatically when DMA is used to fill TX FIFO.

To clear TFFF when not using DMA, follow these steps for every PUSH performed using CPU to fill TX FIFO:

1. Wait until TFFF = 1.
2. Write data to PUSHR using CPU.
3. Clear TFFF by writing a 1 to its location. If TX FIFO is not full, this flag will not clear.

57.5.7.3 Transfer Complete Interrupt Request

The Transfer Complete Request indicates the end of the transfer of a serial frame. The Transfer Complete Request is generated at the end of each frame transfer when the TCF_RE bit is set in the RSER.

57.5.7.4 Transmit FIFO Underflow Interrupt Request

The Transmit FIFO Underflow Request indicates that an underflow condition in the TX FIFO has occurred. The transmit underflow condition is detected only for the module operating in Slave mode and SPI configuration . The TFUF bit is set when the TX FIFO of the module is empty, and a transfer is initiated from an external SPI master. If the TFUF bit is set while the TFUF_RE bit in the RSER is set, an interrupt request is generated.

57.5.7.5 Receive FIFO Drain Interrupt or DMA Request

The Receive FIFO Drain Request indicates that the RX FIFO is not empty. The Receive FIFO Drain Request is generated when the number of entries in the RX FIFO is not zero, and the RFDF_RE bit in the RSER is set. The RFDF_DIRS bit in the RSER selects whether a DMA request or an interrupt request is generated.

57.5.7.6 Receive FIFO Overflow Interrupt Request

The Receive FIFO Overflow Request indicates that an overflow condition in the RX FIFO has occurred. A Receive FIFO Overflow request is generated when RX FIFO and shift register are full and a transfer is initiated. The RFOF_RE bit in the RSER must be set for the interrupt request to be generated.

Depending on the state of the ROOE bit in the MCR, the data from the transfer that generated the overflow is either ignored or shifted in to the shift register. If the ROOE bit is set, the incoming data is shifted in to the shift register. If the ROOE bit is cleared, the incoming data is ignored.

57.5.8 Power saving features

The module supports following power-saving strategies:

- External Stop mode
- Module Disable mode – Clock gating of non-memory mapped logic

57.5.8.1 Stop mode (External Stop mode)

This module supports the Stop mode protocol. When a request is made to enter External Stop mode, the module acknowledges the request . If a serial transfer is in progress, then this module waits until it reaches the frame boundary before it is ready to have its clocks shut off . While the clocks are shut off, this module's memory-mapped logic is not accessible. This also puts the module in STOPPED state. The SR[TXRXS] bit is cleared to indicate STOPPED state. The states of the interrupt and DMA request signals cannot be changed while in External Stop mode.

57.5.8.2 Module Disable mode

Module Disable mode is a block-specific mode that the module can enter to save power. Host CPU can initiate the Module Disable mode by setting the MDIS bit in the MCR. The Module Disable mode can also be initiated by hardware.

When the MDIS bit is set, the module negates the Clock Enable signal at the next frame boundary. Once the Clock Enable signal is negated, it is said to have entered Module Disable Mode. This also puts the module in STOPPED state. The SR[TXRXS] bit is cleared to indicate STOPPED state.If implemented, the Clock Enable signal can stop the clock to the non-memory mapped logic. When Clock Enable is negated, the module is in a dormant state, but the memory mapped registers are still accessible. Certain read or write operations have a different effect when the module is in the Module Disable mode. Reading the RX FIFO Pop Register does not change the state of the RX FIFO. Similarly, writing to the PUSHR Register does not change the state of the TX FIFO. Clearing either of the FIFOs has no effect in the Module Disable mode. Changes to the DIS_TXF and DIS_RXF fields of the MCR have no effect in the Module Disable mode. In the Module Disable mode, all status bits and register flags in the module return the correct values when read, but writing to them has no effect. Writing to the TCR during Module Disable mode has no effect. Interrupt and DMA request signals cannot be cleared while in the Module Disable mode.

57.6 Initialization/application information

This section describes how to initialize the module.

57.6.1 How to manage queues

The queues are not part of the module, but it includes features in support of queue management. Queues are primarily supported in SPI configuration.

1. When module executes last command word from a queue, the EOQ bit in the command word is set to indicate it that this is the last entry in the queue.
2. At the end of the transfer, corresponding to the command word with EOQ set is sampled, the EOQ flag (EOQF) in the SR is set.
3. The setting of the EOQF flag disables serial transmission and reception of data, putting the module in the Stopped state. The TXRXS bit is cleared to indicate the Stopped state.
4. The DMA can continue to fill TX FIFO until it is full or step 5 occurs.
5. Disable DMA transfers by disabling the DMA enable request for the DMA channel assigned to TX FIFO and RX FIFO. This is done by clearing the corresponding DMA enable request bits in the DMA Controller.
6. Ensure all received data in RX FIFO has been transferred to memory receive queue by reading the RXCNT in SR or by checking RFDF in the SR after each read operation of the POPR.
7. Modify DMA descriptor of TX and RX channels for new queues
8. Flush TX FIFO by writing a 1 to the CLR_TXF bit in the MCR. Flush RX FIFO by writing a '1' to the CLR_RXF bit in the MCR.
9. Clear transfer count either by setting CTCNT bit in the command word of the first entry in the new queue or via CPU writing directly to SPI_TCNT field in the TCR.
10. Enable DMA channel by enabling the DMA enable request for the DMA channel assigned to the module TX FIFO, and RX FIFO by setting the corresponding DMA set enable request bit.
11. Enable serial transmission and serial reception of data by clearing the EOQF bit.

57.6.2 Switching Master and Slave mode

When changing modes in the module, follow the steps below to guarantee proper operation.

1. Halt it by setting MCR[HALT].
2. Clear the transmit and receive FIFOs by writing a 1 to the CLR_TXF and CLR_RXF bits in MCR.
3. Set the appropriate mode in MCR[MSTR] and enable it by clearing MCR[HALT].

57.6.3 Initializing Module in Master/Slave Modes

Once the appropriate mode in MCR[MSTR] is configured, the module is enabled by clearing MCR[HALT]. It should be ensured that module Slave is enabled before enabling it's Master. This ensures the Slave is ready to be communicated with, before Master initializes communication.

57.6.4 Baud rate settings

The following table shows the baud rate that is generated based on the combination of the baud rate prescaler PBR and the baud rate scaler BR in the CTARs. The values calculated assume a 100 MHz protocol frequency and the double baud rate DBR bit is cleared.

NOTE

The clock frequency mentioned above is given as an example in this chapter. See the clocking chapter for the frequency used to drive this module in the device.

Table 57-16. Baud rate values (bps)

		Baud rate divider prescaler values			
		2	3	5	7
Baud Rate Scaler Values	2	25.0M	16.7M	10.0M	7.14M
	4	12.5M	8.33M	5.00M	3.57M
	6	8.33M	5.56M	3.33M	2.38M
	8	6.25M	4.17M	2.50M	1.79M
	16	3.12M	2.08M	1.25M	893k
	32	1.56M	1.04M	625k	446k
	64	781k	521k	312k	223k
	128	391k	260k	156k	112k
	256	195k	130k	78.1k	55.8k
	512	97.7k	65.1k	39.1k	27.9k
	1024	48.8k	32.6k	19.5k	14.0k
	2048	24.4k	16.3k	9.77k	6.98k

Table continues on the next page...

Table 57-16. Baud rate values (bps) (continued)

		Baud rate divider prescaler values			
		2	3	5	7
	4096	12.2k	8.14k	4.88k	3.49k
	8192	6.10k	4.07k	2.44k	1.74k
	16384	3.05k	2.04k	1.22k	872
	32768	1.53k	1.02k	610	436

57.6.5 Delay settings

The following table shows the values for the Delay after Transfer (t_{DT}) and CS to SCK Delay (T_{CSC}) that can be generated based on the prescaler values and the scaler values set in the CTARs. The values calculated assume a 100 MHz protocol frequency.

NOTE

The clock frequency mentioned above is given as an example in this chapter. See the clocking chapter for the frequency used to drive this module in the device.

Table 57-17. Delay values

		Delay prescaler values			
		1	3	5	7
Delay scaler values	2	20.0 ns	60.0 ns	100.0 ns	140.0 ns
	4	40.0 ns	120.0 ns	200.0 ns	280.0 ns
	8	80.0 ns	240.0 ns	400.0 ns	560.0 ns
	16	160.0 ns	480.0 ns	800.0 ns	1.1 µs
	32	320.0 ns	960.0 ns	1.6 µs	2.2 µs
	64	640.0 ns	1.9 µs	3.2 µs	4.5 µs
	128	1.3 µs	3.8 µs	6.4 µs	9.0 µs
	256	2.6 µs	7.7 µs	12.8 µs	17.9 µs
	512	5.1 µs	15.4 µs	25.6 µs	35.8 µs
	1024	10.2 µs	30.7 µs	51.2 µs	71.7 µs
	2048	20.5 µs	61.4 µs	102.4 µs	143.4 µs
	4096	41.0 µs	122.9 µs	204.8 µs	286.7 µs
	8192	81.9 µs	245.8 µs	409.6 µs	573.4 µs
	16384	163.8 µs	491.5 µs	819.2 µs	1.1 ms
	32768	327.7 µs	983.0 µs	1.6 ms	2.3 ms
	65536	655.4 µs	2.0 ms	3.3 ms	4.6 ms

57.6.6 Calculation of FIFO pointer addresses

Complete visibility of the FIFO contents is available through the FIFO registers, and valid entries can be identified through a memory-mapped pointer and counter for each FIFO. The pointer to the first-in entry in each FIFO is memory mapped. For the TX FIFO the first-in pointer is the Transmit Next Pointer (TXNXTPTR). For the RX FIFO the first-in pointer is the Pop Next Pointer (POPNXTPTR). The following figure illustrates the concept of first-in and last-in FIFO entries along with the FIFO Counter. The TX FIFO is chosen for the illustration, but the concepts carry over. See Transmit First In First Out (TX FIFO) buffering mechanism and Receive First In First Out (RX FIFO) buffering mechanism for details on the FIFO operation.

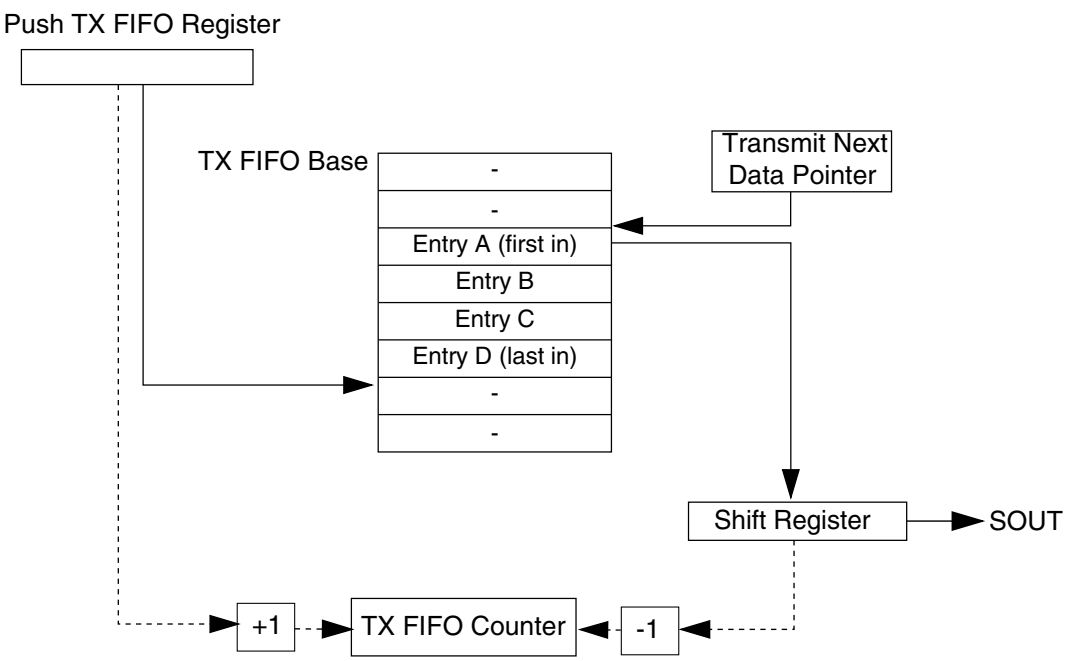


Figure 57-18. TX FIFO pointers and counter

57.6.6.1 Address Calculation for the First-in Entry and Last-in Entry in the TX FIFO

The memory address of the first-in entry in the TX FIFO is computed by the following equation:

$$\text{First-in EntryAddress} = \text{TXFIFOBase} + \left(4 \times \text{TXNXTPTR}\right)$$

The memory address of the last-in entry in the TX FIFO is computed by the following equation:

$$\text{Last-in Entry address} = \text{TXFIFO Base} + 4 \times (\text{TXCTR} + \text{TXNXTPTR} - 1) \bmod (\text{TXFIFO depth})$$

TX FIFO Base - Base address of TX FIFO
TXCTR - TX FIFO Counter
TXNXTPTR - Transmit Next Pointer
TX FIFO Depth - Transmit FIFO depth, implementation specific

57.6.6.2 Address Calculation for the First-in Entry and Last-in Entry in the RX FIFO

The memory address of the first-in entry in the RX FIFO is computed by the following equation:

$$\text{First-in Entry Address} = \text{RX FIFO Base} + (4 \times \text{POPNXTPTR})$$

The memory address of the last-in entry in the RX FIFO is computed by the following equation:

$$\text{Last-in Entry address} = \text{RX FIFO Base} + 4 \times (\text{RXCTR} + \text{POPNXTPTR} - 1) \bmod (\text{RXFIFO depth})$$

RX FIFO Base - Base address of RX FIFO
RXCTR - RX FIFO counter
POPNXTPTR - Pop Next Pointer
RX FIFO Depth - Receive FIFO depth, implementation specific

Chapter 58
Inter-Integrated Circuit (I2C)

58.1 Chip-specific I2C information

58.1.1 Number of I2C modules

This device has 4 I^2C module(s).

The I2C module includes SMBus support and DMA support. It also has optional address match wakeup in Stop/VLPS mode. The digital glitch filter implemented in the IIC module, controlled by the I2Cx_FLT[FLT] registers, is clocked from the bus clock and thus has filter granularity in bus clock cycle counts.

58.2 Introduction

The inter-integrated circuit (I^2C, I2C, or IIC) module provides a method of communication between a number of devices.

The interface is designed to operate up to at least 400 kbit/s with maximum bus loading and timing. The I2C device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF. The I2C module also complies with the *System Management Bus (SMBus) Specification, version 2*.

58.2.1 Features

The I2C module has the following features:

- Compatible with *The I²C-Bus Specification*
- Multimaster operation
- Software programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation and detection
- Repeated START signal generation and detection
- Acknowledge bit generation and detection
- Bus busy detection
- General call recognition
- 10-bit address extension
- Support for *System Management Bus (SMBus) Specification, version 2*
- Programmable input glitch filter
- Low power mode wakeup on slave address match
- Range slave address support
- DMA support
- Double buffering support to achieve higher baud rate

58.2.2 Modes of operation

The I2C module's operation in various low power modes is as follows:

- Run mode: This is the basic mode of operation. To conserve power in this mode, disable the module.
- Wait mode: The module continues to operate when the core is in Wait mode and can provide a wakeup interrupt.
- Stop mode: The module is inactive in Stop mode for reduced power consumption, except that address matching is enabled in Stop mode. The STOP instruction does not affect the I2C module's register states.

58.2.3 Block diagram

The following figure is a functional block diagram of the I2C module.

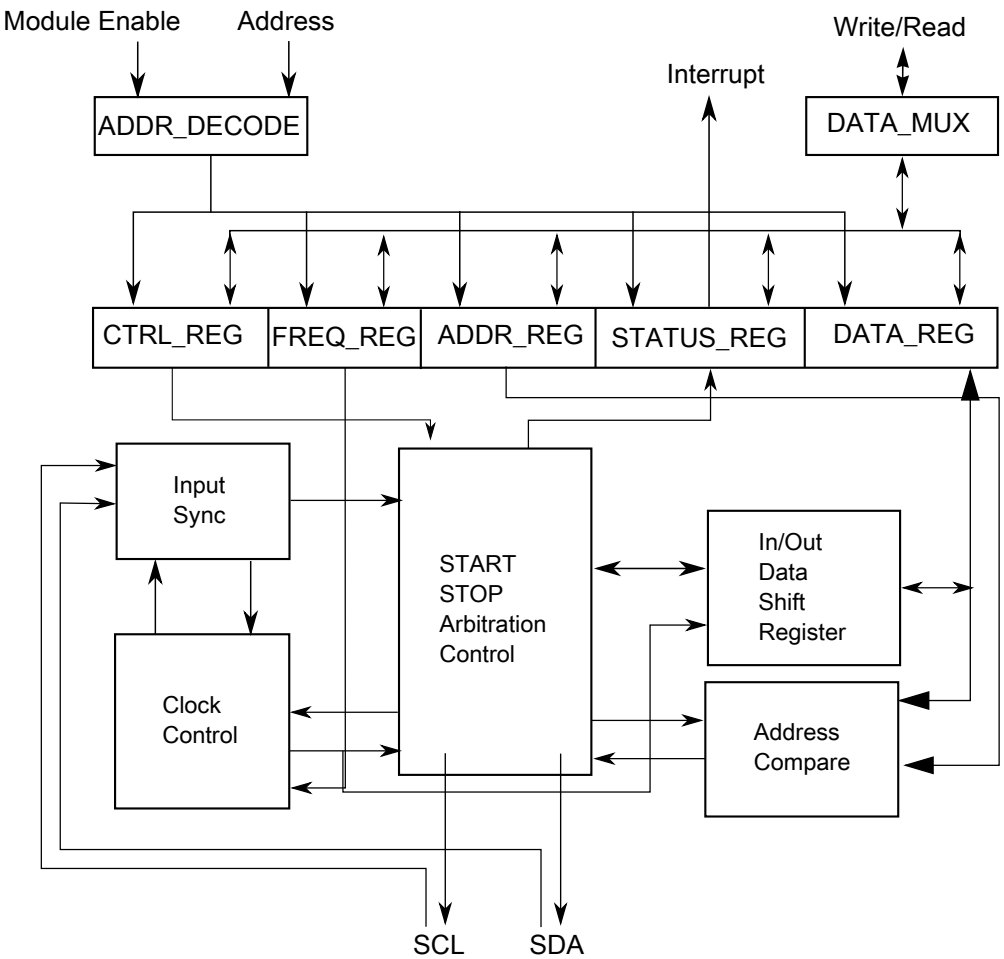


Figure 58-1. I2C Functional block diagram

58.3 I²C signal descriptions

The signal properties of I²C are shown in the table found here.

Table 58-1. I²C signal descriptions

Signal	Description	I/O
SCL	Bidirectional serial clock line of the I²C system.	I/O
SDA	Bidirectional serial data line of the I²C system.	I/O

58.4 Memory map/register definition

This section describes in detail all I2C registers accessible to the end user.

I2C memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4006_6000	I2C Address Register 1 (I2C0_A1)	8	R/W	00h	58.4.1/1884
4006_6001	I2C Frequency Divider register (I2C0_F)	8	R/W	00h	58.4.2/1884
4006_6002	I2C Control Register 1 (I2C0_C1)	8	R/W	00h	58.4.3/1885
4006_6003	I2C Status register (I2C0_S)	8	R/W	80h	58.4.4/1887
4006_6004	I2C Data I/O register (I2C0_D)	8	R/W	00h	58.4.5/1889
4006_6005	I2C Control Register 2 (I2C0_C2)	8	R/W	00h	58.4.6/1889
4006_6006	I2C Programmable Input Glitch Filter Register (I2C0_FLT)	8	R/W	00h	58.4.7/1890
4006_6007	I2C Range Address register (I2C0_RA)	8	R/W	00h	58.4.8/1892
4006_6008	I2C SMBus Control and Status register (I2C0_SMB)	8	R/W	00h	58.4.9/1892
4006_6009	I2C Address Register 2 (I2C0_A2)	8	R/W	C2h	58.4.10/ 1894
4006_600A	I2C SCL Low Timeout Register High (I2C0_SLTH)	8	R/W	00h	58.4.11/ 1894
4006_600B	I2C SCL Low Timeout Register Low (I2C0_SLTL)	8	R/W	00h	58.4.12/ 1895
4006_600C	I2C Status register 2 (I2C0_S2)	8	R/W	01h	58.4.13/ 1895
4006_7000	I2C Address Register 1 (I2C1_A1)	8	R/W	00h	58.4.1/1884
4006_7001	I2C Frequency Divider register (I2C1_F)	8	R/W	00h	58.4.2/1884
4006_7002	I2C Control Register 1 (I2C1_C1)	8	R/W	00h	58.4.3/1885
4006_7003	I2C Status register (I2C1_S)	8	R/W	80h	58.4.4/1887
4006_7004	I2C Data I/O register (I2C1_D)	8	R/W	00h	58.4.5/1889
4006_7005	I2C Control Register 2 (I2C1_C2)	8	R/W	00h	58.4.6/1889
4006_7006	I2C Programmable Input Glitch Filter Register (I2C1_FLT)	8	R/W	00h	58.4.7/1890
4006_7007	I2C Range Address register (I2C1_RA)	8	R/W	00h	58.4.8/1892
4006_7008	I2C SMBus Control and Status register (I2C1_SMB)	8	R/W	00h	58.4.9/1892
4006_7009	I2C Address Register 2 (I2C1_A2)	8	R/W	C2h	58.4.10/ 1894
4006_700A	I2C SCL Low Timeout Register High (I2C1_SLTH)	8	R/W	00h	58.4.11/ 1894
4006_700B	I2C SCL Low Timeout Register Low (I2C1_SLTL)	8	R/W	00h	58.4.12/ 1895
4006_700C	I2C Status register 2 (I2C1_S2)	8	R/W	01h	58.4.13/ 1895

I2C memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400E_6000	I2C Address Register 1 (I2C2_A1)	8	R/W	00h	58.4.1/1884
400E_6001	I2C Frequency Divider register (I2C2_F)	8	R/W	00h	58.4.2/1884
400E_6002	I2C Control Register 1 (I2C2_C1)	8	R/W	00h	58.4.3/1885
400E_6003	I2C Status register (I2C2_S)	8	R/W	80h	58.4.4/1887
400E_6004	I2C Data I/O register (I2C2_D)	8	R/W	00h	58.4.5/1889
400E_6005	I2C Control Register 2 (I2C2_C2)	8	R/W	00h	58.4.6/1889
400E_6006	I2C Programmable Input Glitch Filter Register (I2C2_FLT)	8	R/W	00h	58.4.7/1890
400E_6007	I2C Range Address register (I2C2_RA)	8	R/W	00h	58.4.8/1892
400E_6008	I2C SMBus Control and Status register (I2C2_SMB)	8	R/W	00h	58.4.9/1892
400E_6009	I2C Address Register 2 (I2C2_A2)	8	R/W	C2h	58.4.10/ 1894
400E_600A	I2C SCL Low Timeout Register High (I2C2_SLTH)	8	R/W	00h	58.4.11/ 1894
400E_600B	I2C SCL Low Timeout Register Low (I2C2_SLTL)	8	R/W	00h	58.4.12/ 1895
400E_600C	I2C Status register 2 (I2C2_S2)	8	R/W	01h	58.4.13/ 1895
400E_7000	I2C Address Register 1 (I2C3_A1)	8	R/W	00h	58.4.1/1884
400E_7001	I2C Frequency Divider register (I2C3_F)	8	R/W	00h	58.4.2/1884
400E_7002	I2C Control Register 1 (I2C3_C1)	8	R/W	00h	58.4.3/1885
400E_7003	I2C Status register (I2C3_S)	8	R/W	80h	58.4.4/1887
400E_7004	I2C Data I/O register (I2C3_D)	8	R/W	00h	58.4.5/1889
400E_7005	I2C Control Register 2 (I2C3_C2)	8	R/W	00h	58.4.6/1889
400E_7006	I2C Programmable Input Glitch Filter Register (I2C3_FLT)	8	R/W	00h	58.4.7/1890
400E_7007	I2C Range Address register (I2C3_RA)	8	R/W	00h	58.4.8/1892
400E_7008	I2C SMBus Control and Status register (I2C3_SMB)	8	R/W	00h	58.4.9/1892
400E_7009	I2C Address Register 2 (I2C3_A2)	8	R/W	C2h	58.4.10/ 1894
400E_700A	I2C SCL Low Timeout Register High (I2C3_SLTH)	8	R/W	00h	58.4.11/ 1894
400E_700B	I2C SCL Low Timeout Register Low (I2C3_SLTL)	8	R/W	00h	58.4.12/ 1895
400E_700C	I2C Status register 2 (I2C3_S2)	8	R/W	01h	58.4.13/ 1895

58.4.1 I2C Address Register 1 (I2Cx_A1)

This register contains the slave address to be used by the I2C module.

Address: Base address + 0h offset

Bit	7	6	5	4	3	2	1	0
Read Write	AD[7:1]							0
Reset	0	0	0	0	0	0	0	0

I2Cx_A1 field descriptions

Field	Description
7–1 AD[7:1]	Address Contains the primary slave address used by the I2C module when it is addressed as a slave. This field is used in the 7-bit address scheme and the lower seven bits in the 10-bit address scheme.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

58.4.2 I2C Frequency Divider register (I2Cx_F)

Address: Base address + 1h offset

Bit	7	6	5	4	3	2	1	0
Read Write	MULT		ICR					
Reset	0	0	0	0	0	0	0	0

I2Cx_F field descriptions

Field	Description
7–6 MULT	Multiplier Factor Defines the multiplier factor (mul). This factor is used along with the SCL divider to generate the I2C baud rate. 00 mul = 1 01 mul = 2 10 mul = 4 11 Reserved
ICR	ClockRate Prescales the I2C module clock for bit rate selection. This field and the MULT field determine the I2C baud rate, the SDA hold time, the SCL start hold time, and the SCL stop hold time. For a list of values corresponding to each ICR setting, see I2C divider and hold values. The SCL divider multiplied by multiplier factor (mul) determines the I2C baud rate. `I2C baud rate = I2C module clock speed (Hz)/(mul × SCL divider)`

Table continues on the next page...

I2Cx_F field descriptions (continued)

Field	Description

	The SDA hold time is the delay from the falling edge of SCL (I2C clock) to the changing of SDA (I2C data).
	
	`SDA hold time = I2C module clock period (s) x mul x SDA hold value`
	
	The SCL start hold time is the delay from the falling edge of SDA (I2C data) while SCL is high (start condition) to the falling edge of SCL (I2C clock).
	
	`SCL start hold time = I2C module clock period (s) x mul x SCL start hold value`
	
	The SCL stop hold time is the delay from the rising edge of SCL (I2C clock) to the rising edge of SDA (I2C data) while SCL is high (stop condition).
	
	`SCL stop hold time = I2C module clock period (s) x mul x SCL stop hold value`
	
	For example, if the I2C module clock speed is 8 MHz, the following table shows the possible hold time values with different ICR and MULT selections to achieve an I^2C baud rate of 100 kbit/s.

MULT	ICR	Hold times (µs)		
		SDA	SCL Start	SCL Stop
2h	00h	3.500	3.000	5.500
1h	07h	2.500	4.000	5.250
1h	0Bh	2.250	4.000	5.250
0h	14h	2.125	4.250	5.125
0h	18h	1.125	4.750	5.125

58.4.3 I2C Control Register 1 (I2Cx_C1)

Address: Base address + 2h offset

Bit	7	6	5	4	3	2	1	0
Read	IICEN	IICIE	MST	TX	TXAK	0	WUEN	DMAEN
Write						RSTA		
Reset	0	0	0	0	0	0	0	0

I2Cx_C1 field descriptions

Field	Description
7 IICEN	I2C Enable Enables I2C module operation. 0 Disabled 1 Enabled
6 IICIE	I2C Interrupt Enable Enables I2C interrupt requests.

Table continues on the next page...

I2Cx_C1 field descriptions (continued)

Field	Description
	0 Disabled 1 Enabled
5 MST	Master Mode Select When MST is changed from 0 to 1, a START signal is generated on the bus and master mode is selected. When this bit changes from 1 to 0, a STOP signal is generated and the mode of operation changes from master to slave. 0 Slave mode 1 Master mode
4 TX	Transmit Mode Select Selects the direction of master and slave transfers. In master mode this bit must be set according to the type of transfer required. Therefore, for address cycles, this bit is always set. When addressed as a slave this bit must be set by software according to the SRW bit in the status register. 0 Receive 1 Transmit
3 TXAK	Transmit Acknowledge Enable Specifies the value driven onto the SDA during data acknowledge cycles for both master and slave receivers. The value of SMB[FACK] affects NACK/ACK generation. **NOTE:** SCL is held low until TXAK is written. 0 An acknowledge signal is sent to the bus on the following receiving byte (if FACK is cleared) or the current receiving byte (if FACK is set). 1 No acknowledge signal is sent to the bus on the following receiving data byte (if FACK is cleared) or the current receiving data byte (if FACK is set).
2 RSTA	Repeat START Writing 1 to this bit generates a repeated START condition provided it is the current master. This bit will always be read as 0. Attempting a repeat at the wrong time results in loss of arbitration.
1 WUEN	Wakeup Enable The I2C module can wake the MCU from low power mode with no peripheral bus running when slave address matching occurs. 0 Normal operation. No interrupt generated when address matching in low power mode. 1 Enables the wakeup function in low power mode.
0 DMAEN	DMA Enable Enables or disables the DMA function. 0 All DMA signalling disabled. 1 DMA transfer is enabled. While SMB[FACK] = 0, the following conditions trigger the DMA request: • a data byte is received, and either address or data is transmitted. (ACK/NACK is automatic) • the first byte received matches the A1 register or is a general call address.

Table continues on the next page...

I2Cx_C1 field descriptions (continued)

Field	Description
	If any address matching occurs, S[IAAS] and S[TCF] are set. If the direction of transfer is known from master to slave, then it is not required to check S[SRW]. With this assumption, DMA can also be used in this case. In other cases, if the master reads data from the slave, then it is required to rewrite the C1 register operation. With this assumption, DMA cannot be used. When FACK = 1, an address or a data byte is transmitted.

58.4.4 I2C Status register (I2Cx_S)

Address: Base address + 3h offset

Bit	7	6	5	4	3	2	1	0
Read	TCF	IAAS	BUSY	ARBL	RAM	SRW	IICIF	RXAK
Write				w1c			w1c	
Reset	1	0	0	0	0	0	0	0

I2Cx_S field descriptions

Field	Description
7 TCF	Transfer Complete Flag Acknowledges a byte transfer; TCF is set on the completion of a byte transfer. This bit is valid only during or immediately following a transfer to or from the I2C module. TCF is cleared by reading the I2C data register in receive mode or by writing to the I2C data register in transmit mode. **NOTE:** In the buffer mode, TCF is cleared automatically by internal reading or writing the data register I2C_D, with no need waiting for manually reading/writing the I2C data register in Rx/Tx mode. 0 Transfer in progress 1 Transfer complete
6 IAAS	Addressed As A Slave This bit is set by one of the following conditions: • The calling address matches the programmed primary slave address in the A1 register, or matches the range address in the RA register (which must be set to a nonzero value and under the condition I2C_C2[RMEN] = 1). • C2[GCAEN] is set and a general call is received. • SMB[SIICAEN] is set and the calling address matches the second programmed slave address. • ALERTEN is set and an SMBus alert response address is received • RMEN is set and an address is received that is within the range between the values of the A1 and RA registers. IAAS sets before the ACK bit. The CPU must check the SRW bit and set TX/RX accordingly. Writing the C1 register with any value clears this bit. 0 Not addressed 1 Addressed as a slave
5 BUSY	Bus Busy

Table continues on the next page...

I2Cx_S field descriptions (continued)

Field	Description
	Indicates the status of the bus regardless of slave or master mode. This bit is set when a START signal is detected and cleared when a STOP signal is detected. 0 Bus is idle 1 Bus is busy
4 ARBL	Arbitration Lost This bit is set by hardware when the arbitration procedure is lost. The ARBL bit must be cleared by software, by writing 1 to it. 0 Standard bus operation. 1 Loss of arbitration.
3 RAM	Range Address Match This bit is set to 1 by any of the following conditions, if I2C_C2[RMEN] = 1: • Any nonzero calling address is received that matches the address in the RA register. • The calling address is within the range of values of the A1 and RA registers. **NOTE:** For the RAM bit to be set to 1 correctly, C1[IICIE] must be set to 1. Writing the C1 register with any value clears this bit to 0. 0 Not addressed 1 Addressed as a slave
2 SRW	Slave Read/Write When addressed as a slave, SRW indicates the value of the R/$\overline{W}$ command bit of the calling address sent to the master. 0 Slave receive, master writing to slave 1 Slave transmit, master reading from slave
1 IICIF	Interrupt Flag This bit sets when an interrupt is pending. This bit must be cleared by software by writing 1 to it, such as in the interrupt routine. One of the following events can set this bit: • One byte transfer, including ACK/NACK bit, completes if FACK is 0. An ACK or NACK is sent on the bus by writing 0 or 1 to TXAK after this bit is set in receive mode. • One byte transfer, excluding ACK/NACK bit, completes if FACK is 1. • Match of slave address to calling address including primary slave address, range slave address, alert response address, second slave address, or general call address. • Arbitration lost • In SMBus mode, any timeouts except SCL and SDA high timeouts • I2C bus stop or start detection if the SSIE bit in the Input Glitch Filter register is 1 **NOTE:** To clear the I2C bus stop or start detection interrupt: In the interrupt service routine, first clear the STOPF or STARTF bit in the Input Glitch Filter register by writing 1 to it, and then clear the IICIF bit. If this sequence is reversed, the IICIF bit is asserted again. 0 No interrupt pending 1 Interrupt pending
0 RXAK	Receive Acknowledge

Table continues on the next page...

I2Cx_S field descriptions (continued)

Field	Description
	0 Acknowledge signal was received after the completion of one byte of data transmission on the bus 1 No acknowledge signal detected

58.4.5 I2C Data I/O register (I2Cx_D)

Address: Base address + 4h offset

Bit	7	6	5	4	3	2	1	0
Read Write	DATA							
Reset	0	0	0	0	0	0	0	0

I2Cx_D field descriptions

Field	Description
DATA	Data In master transmit mode, when data is written to this register, a data transfer is initiated. The most significant bit is sent first. In master receive mode, reading this register initiates receiving of the next byte of data. **NOTE:** When making the transition out of master receive mode, switch the I2C mode before reading the Data register to prevent an inadvertent initiation of a master receive data transfer. In slave mode, the same functions are available after an address match occurs. The C1[TX] bit must correctly reflect the desired direction of transfer in master and slave modes for the transmission to begin. For example, if the I2C module is configured for master transmit but a master receive is desired, reading the Data register does not initiate the receive. Reading the Data register returns the last byte received while the I2C module is configured in master receive or slave receive mode. The Data register does not reflect every byte that is transmitted on the I2C bus, and neither can software verify that a byte has been written to the Data register correctly by reading it back. In master transmit mode, the first byte of data written to the Data register following assertion of MST (start bit) or assertion of RSTA (repeated start bit) is used for the address transfer and must consist of the calling address (in bits 7-1) concatenated with the required R/$\overline{W}$ bit (in position bit 0).

58.4.6 I2C Control Register 2 (I2Cx_C2)

Address: Base address + 5h offset

Bit	7	6	5	4	3	2	1	0
Read Write	GCAEN	ADEXT	HDRS	SBRC	RMEN	AD[10:8]		
Reset	0	0	0	0	0	0	0	0

I2Cx_C2 field descriptions

Field	Description
7 GCAEN	General Call Address Enable Enables general call address. 0 Disabled 1 Enabled
6 ADEXT	Address Extension Controls the number of bits used for the slave address. 0 7-bit address scheme 1 10-bit address scheme
5 HDRS	High Drive Select Controls the drive capability of the I2C pads. 0 Normal drive mode 1 High drive mode
4 SBRC	Slave Baud Rate Control Enables independent slave mode baud rate at maximum frequency, which forces clock stretching on SCL in very fast I2C modes. To a slave, an example of a "very fast" mode is when the master transfers at 40 kbit/s but the slave can capture the master's data at only 10 kbit/s. 0 The slave baud rate follows the master baud rate and clock stretching may occur 1 Slave baud rate is independent of the master baud rate
3 RMEN	Range Address Matching Enable This bit controls the slave address matching for addresses between the values of the A1 and RA registers. When this bit is set, a slave address matching occurs for any address greater than the value of the A1 register and less than or equal to the value of the RA register. 0 Range mode disabled. No address matching occurs for an address within the range of values of the A1 and RA registers. 1 Range mode enabled. Address matching occurs when a slave receives an address within the range of values of the A1 and RA registers.
AD[10:8]	Slave Address Contains the upper three bits of the slave address in the 10-bit address scheme. This field is valid only while the ADEXT bit is set.

58.4.7 I2C Programmable Input Glitch Filter Register (I2Cx_FLT)

Address: Base address + 6h offset

Bit	7	6	5	4	3	2	1	0
Read	SHEN	STOPF	SSIE	STARTF	FLT			
Write		w1c		w1c				
Reset	0	0	0	0	0	0	0	0

I2Cx_FLT field descriptions

Field	Description
7 SHEN	Stop Hold Enable Set this bit to hold off entry to stop mode when any data transmission or reception is occurring. The following scenario explains the holdoff functionality: 1. The I2C module is configured for a basic transfer, and the SHEN bit is set to 1. 2. A transfer begins. 3. The MCU signals the I2C module to enter stop mode. 4. The byte currently being transferred, including both address and data, completes its transfer. 5. The I2C slave or master acknowledges that the in-transfer byte completed its transfer and acknowledges the request to enter stop mode. 6. After receiving the I2C module's acknowledgment of the request to enter stop mode, the MCU determines whether to shut off the I2C module's clock. If the SHEN bit is set to 1 and the I2C module is in an idle or disabled state when the MCU signals to enter stop mode, the module immediately acknowledges the request to enter stop mode. If SHEN is cleared to 0 and the overall data transmission or reception that was suspended by stop mode entry was incomplete: To resume the overall transmission or reception after the MCU exits stop mode, software must reinitialize the transfer by resending the address of the slave. If the I2C Control Register 1's IICIE bit was set to 1 before the MCU entered stop mode, system software will receive the interrupt triggered by the I2C Status Register's TCF bit after the MCU wakes from the stop mode. 0 Stop holdoff is disabled. The MCU's entry to stop mode is not gated. 1 Stop holdoff is enabled.
6 STOPF	I2C Bus Stop Detect Flag Hardware sets this bit when the I2C bus's stop status is detected. The STOPF bit must be cleared by writing 1 to it. **NOTE:** The stop flag is only for the matched slave devices, therefore the master will not respond for it. 0 No stop happens on I2C bus 1 Stop detected on I2C bus
5 SSIE	I2C Bus Stop or Start Interrupt Enable This bit enables the interrupt for I2C bus stop or start detection. **NOTE:** To clear the I2C bus stop or start detection interrupt: In the interrupt service routine, first clear the STOPF or STARTF bit by writing 1 to it, and then clear the IICIF bit in the status register. If this sequence is reversed, the IICIF bit is asserted again. 0 Stop or start detection interrupt is disabled 1 Stop or start detection interrupt is enabled
4 STARTF	I2C Bus Start Detect Flag Hardware sets this bit when the I2C bus's start status is detected. The STARTF bit must be cleared by writing 1 to it. 0 No start happens on I2C bus 1 Start detected on I2C bus
FLT	I2C Programmable Filter Factor

Table continues on the next page...

I2Cx_FLT field descriptions (continued)

Field	Description
	Controls the width of the glitch, in terms of I2C module clock cycles, that the filter must absorb. For any glitch whose size is less than or equal to this width setting, the filter does not allow the glitch to pass. 0h No filter/bypass 1-Fh Filter glitches up to width of *n* I2C module clock cycles, where *n*=1-15d

58.4.8 I2C Range Address register (I2Cx_RA)

Address: Base address + 7h offset

Bit	7	6	5	4	3	2	1	0
Read	RAD							0
Write								
Reset	0	0	0	0	0	0	0	0

I2Cx_RA field descriptions

Field	Description
7–1 RAD	Range Slave Address This field contains the slave address to be used by the I2C module. The field is used in the 7-bit address scheme. If I2C_C2[RMEN] is set to 1, any nonzero value write enables this register. This register value can be considered as a maximum boundary in the range matching mode.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

58.4.9 I2C SMBus Control and Status register (I2Cx_SMB)

NOTE

When the SCL and SDA signals are held high for a length of time greater than the high timeout period, the SHTF1 flag sets. Before reaching this threshold, while the system is detecting how long these signals are being held high, a master assumes that the bus is free. However, the SHTF1 bit is set to 1 in the bus transmission process with the idle bus state.

NOTE

When the TCKSEL bit is set, there is no need to monitor the SHTF1 bit because the bus speed is too high to match the protocol of SMBus.

Address: Base address + 8h offset

Bit	7	6	5	4	3	2	1	0
Read	FACK	ALERTEN	SIICAEN	TCKSEL	SLTF	SHTF1	SHTF2	SHTF2IE
Write					w1c		w1c	
Reset	0	0	0	0	0	0	0	0

I2Cx_SMB field descriptions

Field	Description
7 FACK	Fast NACK/ACK Enable For SMBus packet error checking, the CPU must be able to issue an ACK or NACK according to the result of receiving data byte. 0 An ACK or NACK is sent on the following receiving data byte 1 Writing 0 to TXAK after receiving a data byte generates an ACK. Writing 1 to TXAK after receiving a data byte generates a NACK.
6 ALERTEN	SMBus Alert Response Address Enable Enables or disables SMBus alert response address matching. **NOTE:** After the host responds to a device that used the alert response address, you must use software to put the device's address on the bus. The alert protocol is described in the SMBus specification. 0 SMBus alert response address matching is disabled 1 SMBus alert response address matching is enabled
5 SIICAEN	Second I2C Address Enable Enables or disables SMBus device default address. 0 I2C address register 2 matching is disabled 1 I2C address register 2 matching is enabled
4 TCKSEL	Timeout Counter Clock Select Selects the clock source of the timeout counter. 0 Timeout counter counts at the frequency of the I2C module clock / 64 1 Timeout counter counts at the frequency of the I2C module clock
3 SLTF	SCL Low Timeout Flag This bit is set when the SLT register (consisting of the SLTH and SLTL registers) is loaded with a non-zero value (LoValue) and an SCL low timeout occurs. Software clears this bit by writing a logic 1 to it. **NOTE:** The low timeout function is disabled when the SLT register's value is 0. 0 No low timeout occurs 1 Low timeout occurs
2 SHTF1	SCL High Timeout Flag 1 This read-only bit sets when SCL and SDA are held high more than clock × LoValue / 512, which indicates the bus is free. This bit is cleared automatically. 0 No SCL high and SDA high timeout occurs 1 SCL high and SDA high timeout occurs

Table continues on the next page...

I2Cx_SMB field descriptions (continued)

Field	Description
1 SHTF2	SCL High Timeout Flag 2 This bit sets when SCL is held high and SDA is held low more than clock × LoValue / 512. Software clears this bit by writing 1 to it. 0 No SCL high and SDA low timeout occurs 1 SCL high and SDA low timeout occurs
0 SHTF2IE	SHTF2 Interrupt Enable Enables SCL high and SDA low timeout interrupt. 0 SHTF2 interrupt is disabled 1 SHTF2 interrupt is enabled

58.4.10 I2C Address Register 2 (I2Cx_A2)

Address: Base address + 9h offset

Bit	7	6	5	4	3	2	1	0
Read	SAD							0
Write								
Reset	1	1	0	0	0	0	1	0

I2Cx_A2 field descriptions

Field	Description
7–1 SAD	SMBus Address Contains the slave address used by the SMBus. This field is used on the device default address or other related addresses.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

58.4.11 I2C SCL Low Timeout Register High (I2Cx_SLTH)

Address: Base address + Ah offset

Bit	7	6	5	4	3	2	1	0
Read	SSLT[15:8]							
Write								
Reset	0	0	0	0	0	0	0	0

I2Cx_SLTH field descriptions

Field	Description
SSLT[15:8]	SSLT[15:8] Most significant byte of SCL low timeout value that determines the timeout period of SCL low.

58.4.12 I2C SCL Low Timeout Register Low (I2Cx_SLTL)

Address: Base address + Bh offset

Bit	7	6	5	4	3	2	1	0
Read Write	SSLT[7:0]							
Reset	0	0	0	0	0	0	0	0

I2Cx_SLTL field descriptions

Field	Description
SSLT[7:0]	SSLT[7:0] Least significant byte of SCL low timeout value that determines the timeout period of SCL low.

58.4.13 I2C Status register 2 (I2Cx_S2)

Address: Base address + Ch offset

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	ERROR	EMPTY
Write							w1c	
Reset	0	0	0	0	0	0	0	1

I2Cx_S2 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 ERROR	Error flag Indicates if there are read or write errors with the Tx and Rx buffers. 0 The buffer is not full and all write/read operations have no errors. 1 There are 3 or more write/read errors during the data transfer phase (when the Empty flag is not set and the buffer is busy).

Table continues on the next page...

I2Cx_S2 field descriptions (continued)

Field	Description
0 EMPTY	Empty flag Indicates if the Tx or Rx buffer is empty. 0 Tx or Rx buffer is not empty and cannot be written to, that is new data cannot be loaded into the buffer. 1 Tx or Rx buffer is empty and can be written to, that is new data can be loaded into the buffer.

58.5 Functional description

This section provides a comprehensive functional description of the I2C module.

58.5.1 I2C protocol

The I2C bus system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers.

All devices connected to it must have open drain or open collector outputs. A logic AND function is exercised on both lines with external pull-up resistors. The value of these resistors depends on the system.

Normally, a standard instance of communication is composed of four parts:

1. START signal
2. Slave address transmission
3. Data transfer
4. STOP signal

The STOP signal should not be confused with the CPU STOP instruction. The following figure illustrates I2C bus system communication.

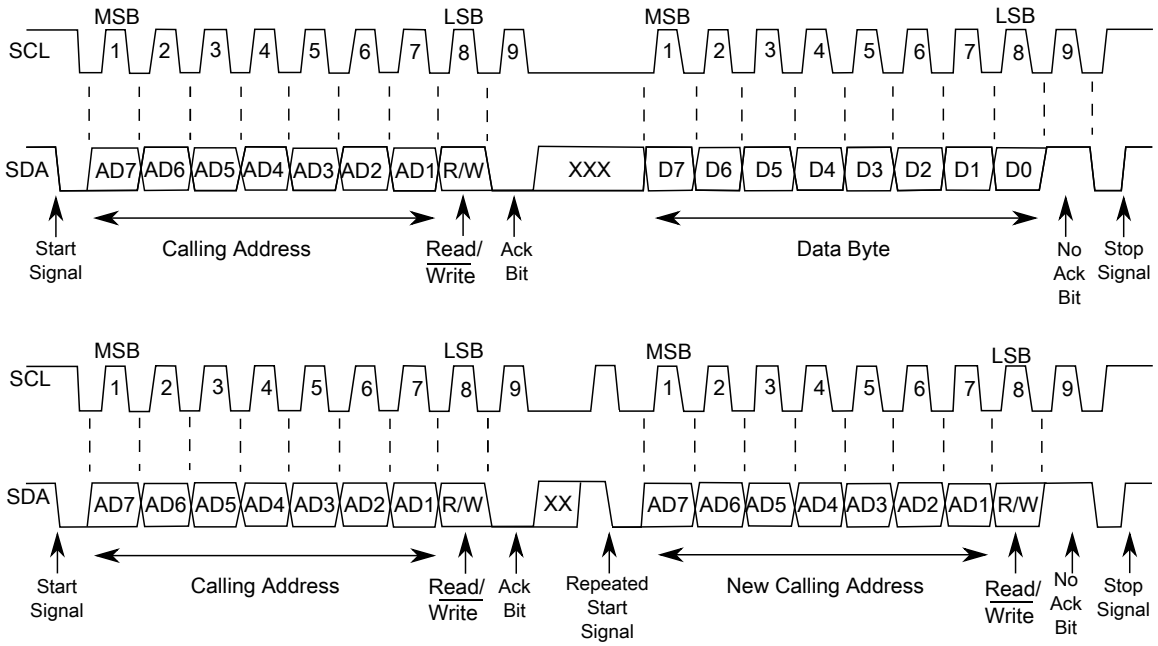


Figure 58-2. I2C bus transmission signals

58.5.1.1 START signal

The bus is free when no master device is engaging the bus (both SCL and SDA are high). When the bus is free, a master may initiate communication by sending a START signal. A START signal is defined as a high-to-low transition of SDA while SCL is high. This signal denotes the beginning of a new data transfer—each data transfer might contain several bytes of data—and brings all slaves out of their idle states.

58.5.1.2 Slave address transmission

Immediately after the START signal, the first byte of a data transfer is the slave address transmitted by the master. This address is a 7-bit calling address followed by an R/$\overline{W}$ bit. The R/$\overline{W}$ bit tells the slave the desired direction of data transfer.

- 1 = Read transfer: The slave transmits data to the master
- 0 = Write transfer: The master transmits data to the slave

Only the slave with a calling address that matches the one transmitted by the master responds by sending an acknowledge bit. The slave sends the acknowledge bit by pulling SDA low at the ninth clock.

No two slaves in the system can have the same address. If the I2C module is the master, it must not transmit an address that is equal to its own slave address. The I2C module cannot be master and slave at the same time. However, if arbitration is lost during an address cycle, the I2C module reverts to slave mode and operates correctly even if it is being addressed by another master.

58.5.1.3 Data transfers

When successful slave addressing is achieved, data transfer can proceed on a byte-by-byte basis in the direction specified by the R/$\overline{W}$ bit sent by the calling master.

All transfers that follow an address cycle are referred to as data transfers, even if they carry subaddress information for the slave device.

Each data byte is 8 bits long. Data may be changed only while SCL is low. Data must be held stable while SCL is high. There is one clock pulse on SCL for each data bit, and the MSB is transferred first. Each data byte is followed by a ninth (acknowledge) bit, which is signaled from the receiving device by pulling SDA low at the ninth clock. In summary, one complete data transfer needs nine clock pulses.

If the slave receiver does not acknowledge the master in the ninth bit, the slave must leave SDA high. The master interprets the failed acknowledgement as an unsuccessful data transfer.

If the master receiver does not acknowledge the slave transmitter after a data byte transmission, the slave interprets it as an end to data transfer and releases the SDA line.

In the case of a failed acknowledgement by either the slave or master, the data transfer is aborted and the master does one of two things:

- Relinquishes the bus by generating a STOP signal.
- Commences a new call by generating a repeated START signal.

58.5.1.4 STOP signal

The master can terminate the communication by generating a STOP signal to free the bus. A STOP signal is defined as a low-to-high transition of SDA while SCL is asserted.

58.5.1.5 Repeated START signal

The master may generate a START signal followed by a calling command without generating a STOP signal first. This action is called a repeated START. The master uses a repeated START to communicate with another slave or with the same slave in a different mode (transmit/receive mode) without releasing the bus.The master needs to send a NACK signal before sending repeated-START in the buffering mode.

58.5.1.6 Arbitration procedure

The I2C bus is a true multimaster bus that allows more than one master to be connected on it.

If two or more masters try to control the bus at the same time, a clock synchronization procedure determines the bus clock. The bus clock's low period is equal to the longest clock low period, and the high period is equal to the shortest one among the masters.

The relative priority of the contending masters is determined by a data arbitration procedure. A bus master loses arbitration if it transmits logic level 1 while another master transmits logic level 0. The losing masters immediately switch to slave receive mode and stop driving SDA output. In this case, the transition from master to slave mode does not generate a STOP condition. Meanwhile, hardware sets a status bit to indicate the loss of arbitration.

58.5.1.7 Clock synchronization

Because wire AND logic is performed on SCL, a high-to-low transition on SCL affects all devices connected on the bus. The devices start counting their low period and, after a device's clock has gone low, that device holds SCL low until the clock reaches its high state. However, the change of low to high in this device clock might not change the state of SCL if another device clock is still within its low period. Therefore, the synchronized clock SCL is held low by the device with the longest low period. Devices with shorter low periods enter a high wait state during this time; see the following diagram. When all applicable devices have counted off their low period, the synchronized clock SCL is released and pulled high. Afterward there is no difference between the device clocks and the state of SCL, and all devices start counting their high periods. The first device to complete its high period pulls SCL low again.

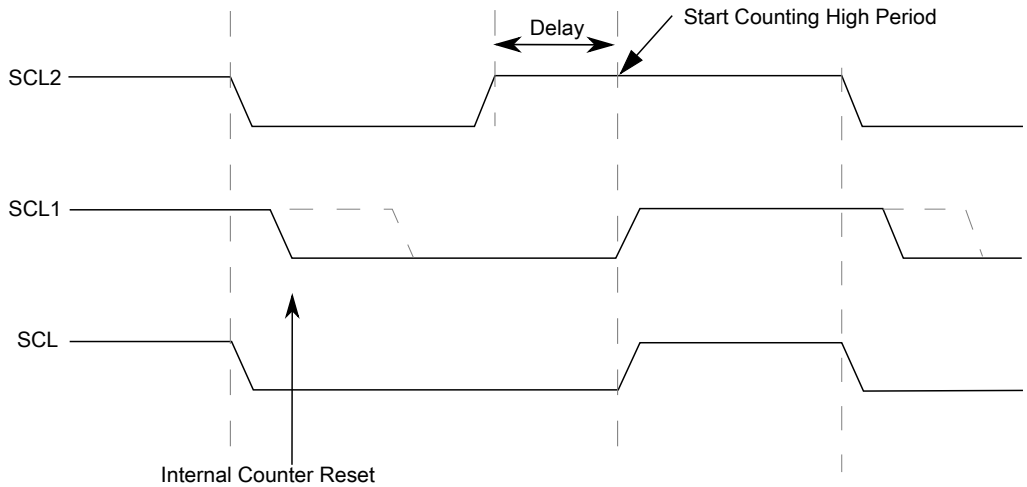


Figure 58-3. I2C clock synchronization

58.5.1.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfers. A slave device may hold SCL low after completing a single byte transfer (9 bits). In this case, it halts the bus clock and forces the master clock into wait states until the slave releases SCL.

58.5.1.9 Clock stretching

The clock synchronization mechanism can be used by slaves to slow down the bit rate of a transfer. After the master drives SCL low, a slave can drive SCL low for the required period and then release it. If the slave's SCL low period is greater than the master's SCL low period, the resulting SCL bus signal's low period is stretched. In other words, the SCL bus signal's low period is increased to be the same length as the slave's SCL low period.

58.5.1.10 I2C divider and hold values

NOTE

For some cases on some devices, the SCL divider value may vary by ±2 or ±4 when ICR's value ranges from 00h to 0Fh. These potentially varying SCL divider values are highlighted in the following table. For the actual SCL divider values for your device, see the chip-specific details about the I2C module.

Table 58-2. I2C divider and hold values

ICR (hex)	SCL divider	SDA hold value	SCL hold (start) value	SCL hold (stop) value	ICR (hex)	SCL divider (clocks)	SDA hold (clocks)	SCL hold (start) value	SCL hold (stop) value
00	20	7	6	11	20	160	17	78	81
01	22	7	7	12	21	192	17	94	97
02	24	8	8	13	22	224	33	110	113
03	26	8	9	14	23	256	33	126	129
04	28	9	10	15	24	288	49	142	145
05	30	9	11	16	25	320	49	158	161
06	34	10	13	18	26	384	65	190	193
07	40	10	16	21	27	480	65	238	241
08	28	7	10	15	28	320	33	158	161
09	32	7	12	17	29	384	33	190	193
0A	36	9	14	19	2A	448	65	222	225
0B	40	9	16	21	2B	512	65	254	257
0C	44	11	18	23	2C	576	97	286	289
0D	48	11	20	25	2D	640	97	318	321
0E	56	13	24	29	2E	768	129	382	385
0F	68	13	30	35	2F	960	129	478	481
10	48	9	18	25	30	640	65	318	321
11	56	9	22	29	31	768	65	382	385
12	64	13	26	33	32	896	129	446	449
13	72	13	30	37	33	1024	129	510	513
14	80	17	34	41	34	1152	193	574	577
15	88	17	38	45	35	1280	193	638	641
16	104	21	46	53	36	1536	257	766	769
17	128	21	58	65	37	1920	257	958	961
18	80	9	38	41	38	1280	129	638	641
19	96	9	46	49	39	1536	129	766	769
1A	112	17	54	57	3A	1792	257	894	897
1B	128	17	62	65	3B	2048	257	1022	1025
1C	144	25	70	73	3C	2304	385	1150	1153
1D	160	25	78	81	3D	2560	385	1278	1281
1E	192	33	94	97	3E	3072	513	1534	1537
1F	240	33	118	121	3F	3840	513	1918	1921

58.5.2 10-bit address

For 10-bit addressing, 0x11110 is used for the first 5 bits of the first address byte. Various combinations of read/write formats are possible within a transfer that includes 10-bit addressing.

58.5.2.1 Master-transmitter addresses a slave-receiver

The transfer direction is not changed. When a 10-bit address follows a START condition, each slave compares the first 7 bits of the first byte of the slave address (11110XX) with its own address and tests whether the eighth bit (R/$\overline{W}$ direction bit) is 0. It is possible that more than one device finds a match and generates an acknowledge (A1). Each slave that finds a match compares the 8 bits of the second byte of the slave address with its own address, but only one slave finds a match and generates an acknowledge (A2). The matching slave remains addressed by the master until it receives a STOP condition (P) or a repeated START condition (Sr) followed by a different slave address.

Table 58-3. Master-transmitter addresses slave-receiver with a 10-bit address

S	Slave address first 7 bits 11110 + AD10 + AD9	R/$\overline{W}$ 0	A1	Slave address second byte AD[8:1]	A2	Data	A	...	Data	A/A	P

After the master-transmitter has sent the first byte of the 10-bit address, the slave-receiver sees an I2C interrupt. User software must ensure that for this interrupt, the contents of the Data register are ignored and not treated as valid data.

58.5.2.2 Master-receiver addresses a slave-transmitter

The transfer direction is changed after the second R/$\overline{W}$ bit. Up to and including acknowledge bit A2, the procedure is the same as that described for a master-transmitter addressing a slave-receiver. After the repeated START condition (Sr), a matching slave remembers that it was addressed before. This slave then checks whether the first seven bits of the first byte of the slave address following Sr are the same as they were after the START condition (S), and it tests whether the eighth (R/$\overline{W}$) bit is 1. If there is a match, the slave considers that it has been addressed as a transmitter and generates acknowledge A3. The slave-transmitter remains addressed until it receives a STOP condition (P) or a repeated START condition (Sr) followed by a different slave address.

After a repeated START condition (Sr), all other slave devices also compare the first seven bits of the first byte of the slave address with their own addresses and test the eighth (R/$\overline{W}$) bit. However, none of them are addressed because R/$\overline{W}$ = 1 (for 10-bit devices), or the 11110XX slave address (for 7-bit devices) does not match.

Table 58-4. Master-receiver addresses a slave-transmitter with a 10-bit address

S	Slave address first 7 bits 11110 + AD10 + AD9	R/$\overline{W}$ 0	A1	Slave address second byte AD[8:1]	A2	Sr	Slave address first 7 bits 11110 + AD10 + AD9	R/$\overline{W}$ 1	A3	Data	A	...	Data	A	P

After the master-receiver has sent the first byte of the 10-bit address, the slave-transmitter sees an I2C interrupt. User software must ensure that for this interrupt, the contents of the Data register are ignored and not treated as valid data.

58.5.3 Address matching

All received addresses can be requested in 7-bit or 10-bit address format.

- AD[7:1] in Address Register 1, which contains the I2C primary slave address, always participates in the address matching process. It provides a 7-bit address.
- If the ADEXT bit is set, AD[10:8] in Control Register 2 participates in the address matching process. It extends the I2C primary slave address to a 10-bit address.

Additional conditions that affect address matching include:

- If the GCAEN bit is set, general call participates the address matching process.
- If the ALERTEN bit is set, alert response participates the address matching process.
- If the SIICAEN bit is set, Address Register 2 participates in the address matching process.
- If the RMEN bit is set, when the Range Address register is programmed to a nonzero value, any address within the range of values of Address Register 1 (excluded) and the Range Address register (included) participates in the address matching process. The Range Address register must be programmed to a value greater than the value of Address Register 1.

When the I2C module responds to one of these addresses, it acts as a slave-receiver and the IAAS bit is set after the address cycle. Software must read the Data register after the first byte transfer to determine that the address is matched.

58.5.4 System management bus specification

SMBus provides a control bus for system and power management related tasks. A system can use SMBus to pass messages to and from devices instead of tripping individual control lines.

Removing the individual control lines reduces pin count. Accepting messages ensures future expandability. With the system management bus, a device can provide manufacturer information, tell the system what its model/part number is, save its state for a suspend event, report different types of errors, accept control parameters, and return its status.

58.5.4.1 Timeouts

The $T_{TIMEOUT,MIN}$ parameter allows a master or slave to conclude that a defective device is holding the clock low indefinitely or a master is intentionally trying to drive devices off the bus. The slave device must release the bus (stop driving the bus and let SCL and SDA float high) when it detects any single clock held low longer than $T_{TIMEOUT,MIN}$. Devices that have detected this condition must reset their communication and be able to receive a new START condition within the timeframe of $T_{TIMEOUT,MAX}$.

SMBus defines a clock low timeout, $T_{TIMEOUT}$, of 35 ms, specifies $T_{LOW:SEXT}$ as the cumulative clock low extend time for a slave device, and specifies $T_{LOW:MEXT}$ as the cumulative clock low extend time for a master device.

58.5.4.1.1 SCL low timeout

If the SCL line is held low by a slave device on the bus, no further communication is possible. Furthermore, the master cannot force the SCL line high to correct the error condition. To solve this problem, the SMBus protocol specifies that devices participating in a transfer must detect any clock cycle held low longer than a timeout value condition. Devices that have detected the timeout condition must reset the communication. When the I2C module is an active master, if it detects that SMBCLK low has exceeded the value of $T_{TIMEOUT,MIN}$, it must generate a stop condition within or after the current data byte in the transfer process. When the I2C module is a slave, if it detects the $T_{TIMEOUT,MIN}$ condition, it resets its communication and is then able to receive a new START condition.

58.5.4.1.2 SCL high timeout

When the I2C module has determined that the SMBCLK and SMBDAT signals have been high for at least $T_{HIGH:MAX}$, it assumes that the bus is idle.

A HIGH timeout occurs after a START condition appears on the bus but before a STOP condition appears on the bus. Any master detecting this scenario can assume the bus is free when either of the following occurs:

- SHTF1 rises.
- The BUSY bit is high and SHTF1 is high.

When the SMBDAT signal is low and the SMBCLK signal is high for a period of time, another kind of timeout occurs. The time period must be defined in software. SHTF2 is used as the flag when the time limit is reached. This flag is also an interrupt resource, so it triggers IICIF.

58.5.4.1.3 CSMBCLK TIMEOUT MEXT and CSMBCLK TIMEOUT SEXT

The following figure illustrates the definition of the timeout intervals $T_{LOW:SEXT}$ and $T_{LOW:MEXT}$. When in master mode, the I2C module must not cumulatively extend its clock cycles for a period greater than $T_{LOW:MEXT}$ within a byte, where each byte is defined as START-to-ACK, ACK-to-ACK, or ACK-to-STOP. When CSMBCLK TIMEOUT MEXT occurs, SMBus MEXT rises and also triggers the SLTF.

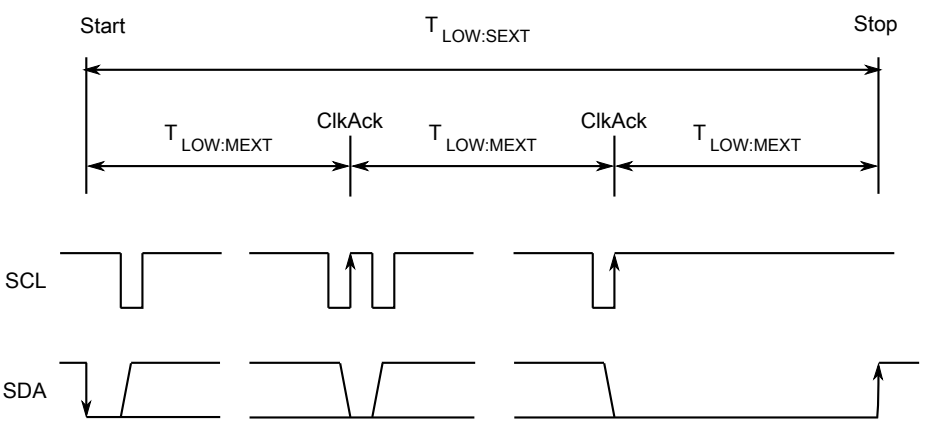


Figure 58-4. Timeout measurement intervals

A master is allowed to abort the transaction in progress to any slave that violates the $T_{LOW:SEXT}$ or $T_{TIMEOUT,MIN}$ specifications. To abort the transaction, the master issues a STOP condition at the conclusion of the byte transfer in progress. When a slave, the I2C module must not cumulatively extend its clock cycles for a period greater than $T_{LOW:SEXT}$ during any message from the initial START to the STOP. When CSMBCLK TIMEOUT SEXT occurs, SEXT rises and also triggers SLTF.

NOTE

CSMBCLK TIMEOUT SEXT and CSMBCLK TIMEOUT MEXT are optional functions that are implemented in the second step.

58.5.4.2 FAST ACK and NACK

To improve reliability and communication robustness, implementation of packet error checking (PEC) by SMBus devices is optional for SMBus devices but required for devices participating in and only during the address resolution protocol (ARP) process. The PEC is a CRC-8 error checking byte, calculated on all the message bytes. The PEC is appended to the message by the device that supplied the last data byte. If the PEC is present but not correct, a NACK is issued by the receiver. Otherwise an ACK is issued. To calculate the CRC-8 by software, this module can hold the SCL line low after receiving the eighth SCL (8th bit) if this byte is a data byte. So software can determine whether an ACK or NACK should be sent to the bus by setting or clearing the TXAK bit if the FACK (fast ACK/NACK enable) bit is enabled.

SMBus requires a device always to acknowledge its own address, as a mechanism to detect the presence of a removable device (such as a battery or docking station) on the bus. In addition to indicating a slave device busy condition, SMBus uses the NACK mechanism to indicate the reception of an invalid command or invalid data. Because such a condition may occur on the last byte of the transfer, SMBus devices are required to have the ability to generate the not acknowledge after the transfer of each byte and before the completion of the transaction. This requirement is important because SMBus does not provide any other resend signaling. This difference in the use of the NACK signaling has implications on the specific implementation of the SMBus port, especially in devices that handle critical system data such as the SMBus host and the SBS components.

NOTE

In the last byte of master receive slave transmit mode, the master must send a NACK to the bus, so FACK must be switched off before the last byte transmits.

58.5.5 Resets

The I2C module is disabled after a reset. The I2C module cannot cause a core reset.

58.5.6 Interrupts

The I2C module generates an interrupt when any of the events in the table found here occur, provided that the IICIE bit is set.

The interrupt is driven by the IICIF bit (of the I2C Status Register) and masked with the IICIE bit (of the I2C Control Register 1). The IICIF bit must be cleared (by software) by writing 1 to it in the interrupt routine. The SMBus timeouts interrupt is driven by SLTF and masked with the IICIE bit. The SLTF bit must be cleared by software by writing 1 to it in the interrupt routine. You can determine the interrupt type by reading the Status Register.

NOTE

In master receive mode, the FACK bit must be set to zero before the last byte transfer.

Table 58-5. Interrupt summary

Interrupt source	Status	Flag	Local enable
Complete 1-byte transfer	TCF	IICIF	IICIE
Match of received calling address	IAAS	IICIF	IICIE
Arbitration lost	ARBL	IICIF	IICIE
I^2C bus stop detection	STOPF	IICIF	IICIE & SSIE
I^2C bus start detection	STARTF	IICIF	IICIE & SSIE
SMBus SCL low timeout	SLTF	IICIF	IICIE
SMBus SCL high SDA low timeout	SHTF2	IICIF	IICIE & SHTF2IE
Wakeup from stop or wait mode	IAAS	IICIF	IICIE & WUEN

58.5.6.1 Byte transfer interrupt

The Transfer Complete Flag (TCF) bit is set at the falling edge of the ninth clock to indicate the completion of a byte and acknowledgement transfer. When FACK is enabled, TCF is then set at the falling edge of eighth clock to indicate the completion of byte.

58.5.6.2 Address detect interrupt

When the calling address matches the programmed slave address (I2C Address Register) or when the GCAEN bit is set and a general call is received, the IAAS bit in the Status Register is set. The CPU is interrupted, provided the IICIE bit is set. The CPU must check the SRW bit and set its Tx mode accordingly.

58.5.6.3 Stop Detect Interrupt

When the stop status is detected on the I^2C bus, the STOPF bit is set to 1. The CPU is interrupted, provided the IICIE and SSIE bits are both set to 1.

58.5.6.4 Exit from low-power/stop modes

The slave receive input detect circuit and address matching feature are still active on low power modes (wait and stop). An asynchronous input matching slave address or general call address brings the CPU out of low power/stop mode if the interrupt is not masked. Therefore, TCF and IAAS both can trigger this interrupt.

58.5.6.5 Arbitration lost interrupt

The I2C is a true multimaster bus that allows more than one master to be connected on it. If two or more masters try to control the bus at the same time, the relative priority of the contending masters is determined by a data arbitration procedure. The I2C module asserts the arbitration-lost interrupt when it loses the data arbitration process and the ARBL bit in the Status Register is set.

Arbitration is lost in the following circumstances:

1. SDA is sampled as low when the master drives high during an address or data transmit cycle.
2. SDA is sampled as low when the master drives high during the acknowledge bit of a data receive cycle.
3. A START cycle is attempted when the bus is busy.
4. A repeated START cycle is requested in slave mode.
5. A STOP condition is detected when the master did not request it.

The ARBL bit must be cleared (by software) by writing 1 to it.

58.5.6.6 Timeout interrupt in SMBus

When the IICIE bit is set, the I2C module asserts a timeout interrupt (outputs SLTF and SHTF2) upon detection of any of the mentioned timeout conditions, with one exception. The SCL high and SDA high TIMEOUT mechanism must not be used to influence the timeout interrupt output, because this timeout indicates an idle condition on the bus. SHTF1 rises when it matches the SCL high and SDA high TIMEOUT and falls automatically just to indicate the bus status. The SHTF2's timeout period is the same as that of SHTF1, which is short compared to that of SLTF, so another control bit, SHTF2IE, is added to enable or disable it.

58.5.7 Programmable input glitch filter

An I2C glitch filter has been added outside legacy I2C modules but within the I2C package. This filter can absorb glitches on the I2C clock and data lines for the I2C module.

The width of the glitch to absorb can be specified in terms of the number of (half) I2C module clock cycles. A single Programmable Input Glitch Filter control register is provided. Effectively, any down-up-down or up-down-up transition on the data line that occurs within the number of clock cycles programmed in this register is ignored by the I2C module. The programmer must specify the size of the glitch (in terms of I2C module clock cycles) for the filter to absorb and not pass.

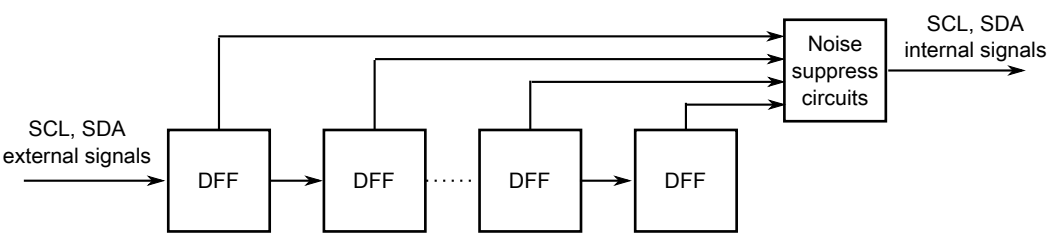


Figure 58-5. Programmable input glitch filter diagram

58.5.8 Address matching wake-up

When a primary, range, or general call address match occurs when the I2C module is in slave receive mode, the MCU wakes from a low power mode where no peripheral bus is running.

Data sent on the bus that is the same as a target device address might also wake the target MCU.

After the address matching IAAS bit is set, an interrupt is sent at the end of address matching to wake the core. The IAAS bit must be cleared after the clock recovery.

NOTE

After the system recovers and is in Run mode, restart the I2C module if it is needed to transfer packets. To avoid I2C transfer problems resulting from the situation, firmware should prevent the MCU execution of a STOP instruction when the I2C module is in the middle of a transfer unless the Stop mode holdoff feature is used during this period (set FLT[SHEN] to 1).

NOTE

After I2C address matching wake-up, the master must wait a time long enough for the slave ISR to finish running and resend start or repeat start signals.

For the SRW bit to function properly, it only supports Address +Write to wake up by I2C address matching. Before entering the next low power mode, Address+Write must be sent to change the SRW status.

58.5.9 DMA support

If the DMAEN bit is cleared and the IICIE bit is set, an interrupt condition generates an interrupt request.

If the DMAEN bit is set and the IICIE bit is set, an interrupt condition generates a DMA request instead. DMA requests are generated by the transfer complete flag (TCF).

If the DMAEN bit is set, only the TCF initiates a DMA request. All other events generate CPU interrupts.

NOTE

Before the last byte of master receive mode, TXAK must be set to send a NACK after the last byte's transfer. Therefore, the DMA must be disabled before the last byte's transfer.

NOTE

In 10-bit address mode transmission, the addresses to send occupy 2–3 bytes. During this transfer period, the DMA must be disabled because the C1 register is written to send a repeat start or to change the transfer direction.

58.5.10 Double buffering mode

In the double buffering mode, the data transfer is processed byte by byte. However, the data can be transferred without waiting for the interrupt or the polling to finish. This means the write/read I2C_D operation will not block the data transfer, as the hardware has already finished the internal write or read. The benefit is that the baud rate is able to achieve higher speed.

There are several items to consider as follows:

- When initiating a double buffering transfer at Tx side, the user can write 2 values to the I2C_D buffer before transfer. However, that is allowed only at one time per package frame (due to the buffer depth, and because two-times writes in each ISR are not allowed). The second write to the I2C_D buffer must wait for the Empty flag. On the other hand, at Rx side the user can read twice in a one-byte transfer (if needed).

NOTE

Check Empty flag before write to I2C_D.

Write twice to the I2C_D buffer ONLY after the address matching byte. Do not write twice (Address+Data) before START or at the beginning of I2C transfer, especially when the baud rate is very slow.

- To write twice in one frame, during the next-to-last ISR, do a dummy read from the I2C_D buffer at Tx side (or the TCF will stay high, because the TCF is cleared by write/read operation). In the next-to-last ISR, do not send data again (the buffer data will be under running).
- To keep new ISRs software-compatible with previous ISRs, the write/read I2C_D operation will not block the internal-hardware-released SCL/SDA signals. At the ACK phase, the bus is released to accept the next byte if the master can send the clock immediately.
- On the slave side, two-times writes to the I2C_D buffer may be limited by the master's clock and START/repeated-START signal. This is not currently supported, and the master's START/repeated-START signal will break data transfers. To release the bus, do a dummy read or write to the I2C_D buffer again. It is suggested to send repeated-START/START during intervals as before.
- The master receive should send a NACK in the next-to-last ISR, if it wants to do the STOP or the repeated-START work. The transmitting slave which receives the NACK, will switch to receive mode, and do a dummy read to release SCL and SDA signals.

58.6 Initialization/application information

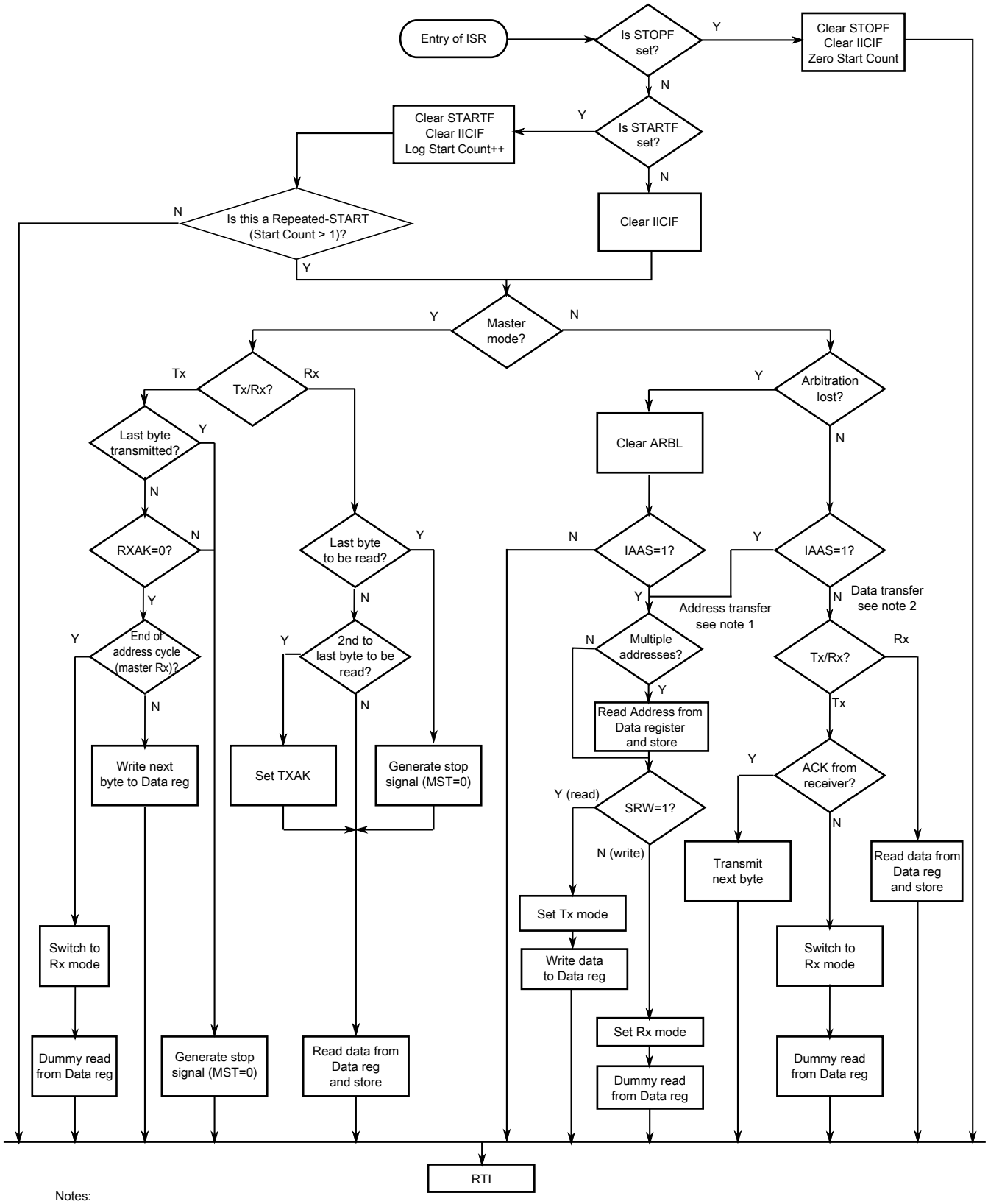
Module Initialization (Slave)

1. Write: Control Register 2
   - to enable or disable general call
   - to select 10-bit or 7-bit addressing mode
2. Write: Address Register 1 to set the slave address
3. Write: Control Register 1 to enable the I2C module and interrupts
4. Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data
5. Initialize RAM variables used to achieve the routine shown in the following figure

Module Initialization (Master)

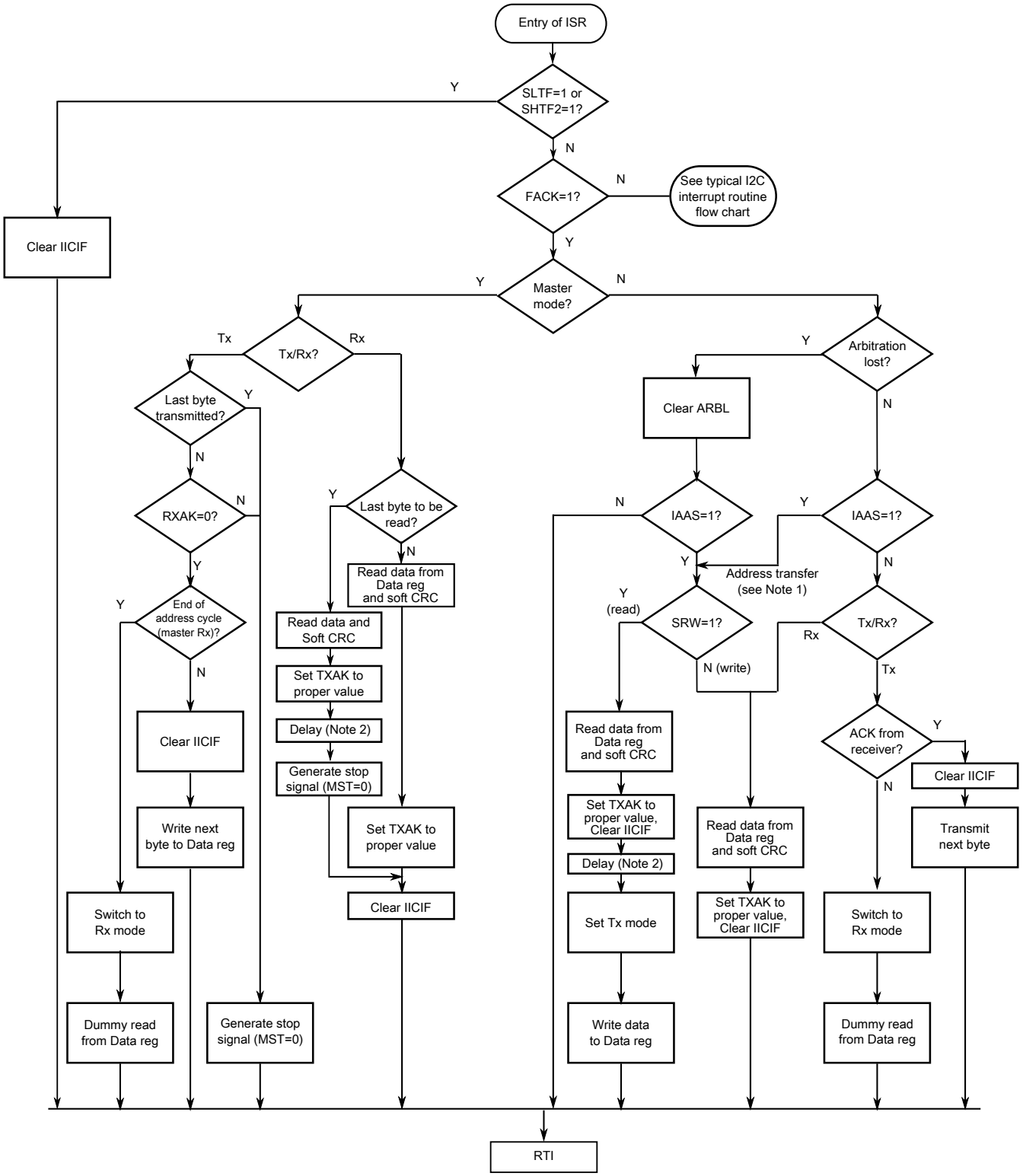
1. Write: Frequency Divider register to set the I2C baud rate (see example in description of ICR)
2. Write: Control Register 1 to enable the I2C module and interrupts
3. Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data
4. Initialize RAM variables used to achieve the routine shown in the following figure
5. Write: Control Register 1 to enable TX
6. Write: Control Register 1 to enable MST (master mode)
7. Write: Data register with the address of the target slave (the LSB of this byte determines whether the communication is master receive or transmit)

The routine shown in the following figure encompasses both master and slave I2C operations. For slave operation, an incoming I2C message that contains the proper address begins I2C communication. For master operation, communication must be initiated by writing the Data register. An example of an I2C driver which implements many of the steps described here is available in AN4342: Using the Inter-Integrated Circuit on ColdFire+ and Kinetis .



Notes:
1. If general call is enabled, check to determine if the received address is a general call address (0x00).
   If the received address is a general call address, the general call must be handled by user software.
2. When 10-bit addressing addresses a slave, the slave sees an interrupt following the first byte of the extended address.
   Ensure that for this interrupt, the contents of the Data register are ignored and not treated as a valid data transfer.

Figure 58-6. Typical I2C interrupt routine



Notes:
1. If general call or SIICAEN is enabled, check to determine if the received address is a general call address (0x00) or an SMBus device default address. In either case, they must be handled by user software.
2. In receive mode, one bit time delay may be needed before the stop signal generation, to wait for the possible longest time period (in worst case) of the 9th SCL cycle.

Figure 58-7. Typical I2C SMBus interrupt routine

Chapter 59
Low Power Universal asynchronous receiver/ transmitter (LPUART)

59.1 Chip-specific LPUART information

59.1.1 LPUART overview

The LPUART module supports basic UART with DMA interface function and x4 to x32 oversampling of baud-rate.

The module can remain functional in Stop and VLPS mode provided the clock it is using remains enabled.

This module supports LIN slave operation.

NOTE

LPUART2 pins can be muxed over USB. See USB chapter for more detail.

59.1.2 LPUART Instantiation

This device contains 5 LPUART modules. This section describes how each module is configured on this device.

Table 59-1. LPUART instantiations

Feature	Receive Buffer Size
LPUARTs instantiated	5
LPUART0 FIFO (RX & TX)	8 Bytes
LPUART1 FIFO (RX & TX)	8 Bytes

Table continues on the next page...

Table 59-1. LPUART instantiations (continued)

Feature	Receive Buffer Size
LPUART2 FIFO (RX & TX)	1 Byte
LPUART3 FIFO (RX & TX)	1 Byte
LPUART4 FIFO (RX & TX)	1 Byte

59.2 Introduction

59.2.1 Features

Features of the LPUART module include:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x
- Transmit and receive baud rate can operate asynchronous to the bus clock:
  - Baud rate can be configured independently of the bus clock frequency
  - Supports operation in Stop modes
- Interrupt, DMA or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
  - Receive data match
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection

- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width
- Independent FIFO structure for transmit and receive
  - Separate configurable watermark for receive and transmit requests
  - Option for receiver to assert request after a configurable number of idle characters if receive FIFO is not empty

59.2.2 Modes of operation

59.2.2.1 Stop mode

The LPUART will remain functional during Stop mode, provided the asynchronous transmit and receive clock remains enabled. The LPUART can generate an interrupt or DMA request to cause a wakeup from Stop mode.

59.2.2.2 Wait mode

The LPUART can be configured to Stop in Wait modes, when the DOZEEN bit is set. The transmitter and receiver will finish transmitting/receiving the current word.

59.2.2.3 Debug mode

The LPUART remains functional in debug mode.

59.2.3 Signal Descriptions

Signal	Description	I/O
LPUART_TX	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O

Table continues on the next page...

Signal	Description	I/O
LPUART_RX	Receive data.	I
LPUART_CTS	Clear to send.	I
LPUART_RTS	Request to send.	O

59.2.4 Block diagram

The following figure shows the transmitter portion of the LPUART.

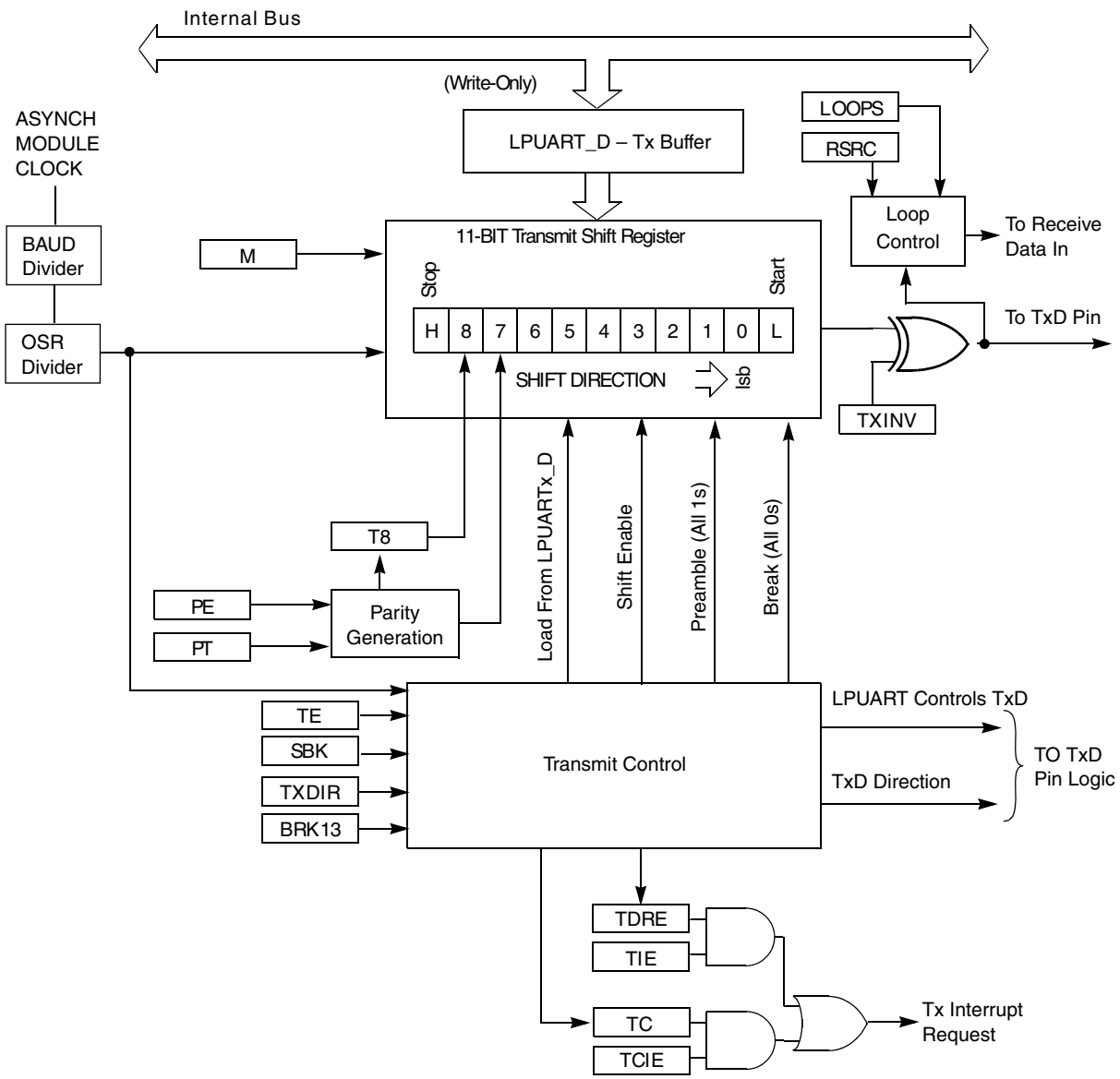


Figure 59-1. LPUART transmitter block diagram

The following figure shows the receiver portion of the LPUART.

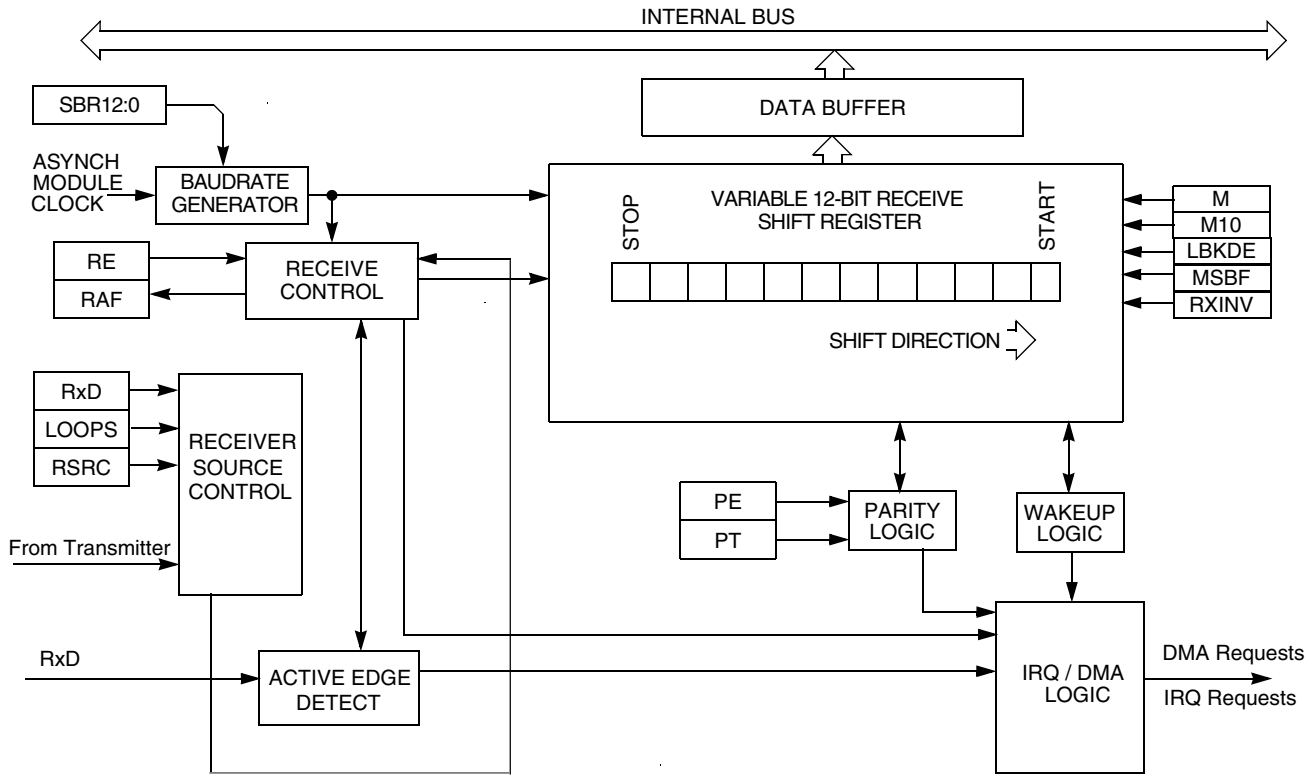


Figure 59-2. LPUART receiver block diagram

59.3 Register definition

The LPUART includes registers to control baud rate, select LPUART options, report LPUART status, and for transmit/receive data. Access to an address outside the valid memory map will generate a bus error.

LPUART memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400C_4000	LPUART Baud Rate Register (LPUART0_BAUD)	32	R/W	0F00_0004h	59.3.1/1921
400C_4004	LPUART Status Register (LPUART0_STAT)	32	R/W	00C0_0000h	59.3.2/1923
400C_4008	LPUART Control Register (LPUART0_CTRL)	32	R/W	0000_0000h	59.3.3/1927
400C_400C	LPUART Data Register (LPUART0_DATA)	32	R/W	0000_1000h	59.3.4/1932
400C_4010	LPUART Match Address Register (LPUART0_MATCH)	32	R/W	0000_0000h	59.3.5/1934
400C_4014	LPUART Modem IrDA Register (LPUART0_MODIR)	32	R/W	0000_0000h	59.3.6/1934
400C_4018	LPUART FIFO Register (LPUART0_FIFO)	32	R/W	See section	59.3.7/1937
400C_401C	LPUART Watermark Register (LPUART0_WATER)	32	R/W	0000_0000h	59.3.8/1940
400C_5000	LPUART Baud Rate Register (LPUART1_BAUD)	32	R/W	0F00_0004h	59.3.1/1921

Table continues on the next page...

LPUART memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400C_5004	LPUART Status Register (LPUART1_STAT)	32	R/W	00C0_0000h	59.3.2/1923
400C_5008	LPUART Control Register (LPUART1_CTRL)	32	R/W	0000_0000h	59.3.3/1927
400C_500C	LPUART Data Register (LPUART1_DATA)	32	R/W	0000_1000h	59.3.4/1932
400C_5010	LPUART Match Address Register (LPUART1_MATCH)	32	R/W	0000_0000h	59.3.5/1934
400C_5014	LPUART Modem IrDA Register (LPUART1_MODIR)	32	R/W	0000_0000h	59.3.6/1934
400C_5018	LPUART FIFO Register (LPUART1_FIFO)	32	R/W	See section	59.3.7/1937
400C_501C	LPUART Watermark Register (LPUART1_WATER)	32	R/W	0000_0000h	59.3.8/1940
400C_6000	LPUART Baud Rate Register (LPUART2_BAUD)	32	R/W	0F00_0004h	59.3.1/1921
400C_6004	LPUART Status Register (LPUART2_STAT)	32	R/W	00C0_0000h	59.3.2/1923
400C_6008	LPUART Control Register (LPUART2_CTRL)	32	R/W	0000_0000h	59.3.3/1927
400C_600C	LPUART Data Register (LPUART2_DATA)	32	R/W	0000_1000h	59.3.4/1932
400C_6010	LPUART Match Address Register (LPUART2_MATCH)	32	R/W	0000_0000h	59.3.5/1934
400C_6014	LPUART Modem IrDA Register (LPUART2_MODIR)	32	R/W	0000_0000h	59.3.6/1934
400C_6018	LPUART FIFO Register (LPUART2_FIFO)	32	R/W	See section	59.3.7/1937
400C_601C	LPUART Watermark Register (LPUART2_WATER)	32	R/W	0000_0000h	59.3.8/1940
400C_7000	LPUART Baud Rate Register (LPUART3_BAUD)	32	R/W	0F00_0004h	59.3.1/1921
400C_7004	LPUART Status Register (LPUART3_STAT)	32	R/W	00C0_0000h	59.3.2/1923
400C_7008	LPUART Control Register (LPUART3_CTRL)	32	R/W	0000_0000h	59.3.3/1927
400C_700C	LPUART Data Register (LPUART3_DATA)	32	R/W	0000_1000h	59.3.4/1932
400C_7010	LPUART Match Address Register (LPUART3_MATCH)	32	R/W	0000_0000h	59.3.5/1934
400C_7014	LPUART Modem IrDA Register (LPUART3_MODIR)	32	R/W	0000_0000h	59.3.6/1934
400C_7018	LPUART FIFO Register (LPUART3_FIFO)	32	R/W	See section	59.3.7/1937
400C_701C	LPUART Watermark Register (LPUART3_WATER)	32	R/W	0000_0000h	59.3.8/1940
400D_6000	LPUART Baud Rate Register (LPUART4_BAUD)	32	R/W	0F00_0004h	59.3.1/1921
400D_6004	LPUART Status Register (LPUART4_STAT)	32	R/W	00C0_0000h	59.3.2/1923
400D_6008	LPUART Control Register (LPUART4_CTRL)	32	R/W	0000_0000h	59.3.3/1927
400D_600C	LPUART Data Register (LPUART4_DATA)	32	R/W	0000_1000h	59.3.4/1932
400D_6010	LPUART Match Address Register (LPUART4_MATCH)	32	R/W	0000_0000h	59.3.5/1934
400D_6014	LPUART Modem IrDA Register (LPUART4_MODIR)	32	R/W	0000_0000h	59.3.6/1934
400D_6018	LPUART FIFO Register (LPUART4_FIFO)	32	R/W	See section	59.3.7/1937
400D_601C	LPUART Watermark Register (LPUART4_WATER)	32	R/W	0000_0000h	59.3.8/1940

59.3.1 LPUART Baud Rate Register (LPUARTx_BAUD)

Address: Base address + 0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	MAEN1	MAEN2	M10	OSR					TDMAE	0	RDMAE	0	MATCFG		BOTHEDGE	RESYNCDIS
W																
Reset	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	LBKDIE	RXEDGIE	SBNS	SBR												
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

LPUARTx_BAUD field descriptions

Field	Description
31 MAEN1	Match Address Mode Enable 1 0 Normal operation. 1 Enables automatic address matching or data matching mode for MATCH[MA1].
30 MAEN2	Match Address Mode Enable 2 0 Normal operation. 1 Enables automatic address matching or data matching mode for MATCH[MA2].
29 M10	10-bit Mode select The M10 bit causes a tenth bit to be part of the serial transmission. This bit should only be changed when the transmitter and receiver are both disabled. 0 Receiver and transmitter use 8-bit or 9-bit data characters. 1 Receiver and transmitter use 10-bit data characters.
28–24 OSR	Oversampling Ratio This field configures the oversampling ratio for the receiver between 4x (00011) and 32x (11111). Writing an invalid oversampling ratio (for example, a value not between 4x and 32x) will default to an oversampling ratio of 16 (01111). The OSR field should only be changed when the transmitter and receiver are both disabled. Note that the oversampling ratio = OSR + 1.
23 TDMAE	Transmitter DMA Enable TDMAE configures the transmit data register empty flag, LPUART_STAT[TDRE], to generate a DMA request. 0 DMA request disabled. 1 DMA request enabled.

Table continues on the next page...

LPUARTx_BAUD field descriptions (continued)

Field	Description
22 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
21 RDMAE	Receiver Full DMA Enable RDMAE configures the receiver data register full flag, LPUART_STAT[RDRF], to generate a DMA request. 0 DMA request disabled. 1 DMA request enabled.
20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–18 MATCFG	Match Configuration Configures the match addressing mode used. 00 Address Match Wakeup 01 Idle Match Wakeup 10 Match On and Match Off 11 Enables RWU on Data Match and Match On/Off for transmitter CTS input
17 BOTHEDGE	Both Edge Sampling Enables sampling of the received data on both edges of the baud rate clock, effectively doubling the number of times the receiver samples the input data for a given oversampling ratio. This bit must be set for oversampling ratios between x4 and x7 and is optional for higher oversampling ratios. This bit should only be changed when the receiver is disabled. 0 Receiver samples input data using the rising edge of the baud rate clock. 1 Receiver samples input data using the rising and falling edge of the baud rate clock.
16 RESYNCDIS	Resynchronization Disable When set, disables the resynchronization of the received data word when a data one followed by data zero transition is detected. This bit should only be changed when the receiver is disabled. 0 Resynchronization during received data word is supported 1 Resynchronization during received data word is disabled
15 LBKDIE	LIN Break Detect Interrupt Enable LBKDIE enables the LIN break detect flag, LBKDIF, to generate interrupt requests. 0 Hardware interrupts from LPUART_STAT[LBKDIF] disabled (use polling). 1 Hardware interrupt requested when LPUART_STAT[LBKDIF] flag is 1.
14 RXEDGIE	RX Input Active Edge Interrupt Enable Enables the receive input active edge, RXEDGIF, to generate interrupt requests. Changing CTRL[LOOP] or CTRL[RSRC] when RXEDGIE is set can cause the RXEDGIF to set. 0 Hardware interrupts from LPUART_STAT[RXEDGIF] disabled (use polling). 1 Hardware interrupt requested when LPUART_STAT[RXEDGIF] flag is 1.
13 SBNS	Stop Bit Number Select SBNS determines whether data characters are one or two stop bits. This bit should only be changed when the transmitter and receiver are both disabled.

Table continues on the next page...

LPUARTx_BAUD field descriptions (continued)

Field	Description
	0 One stop bit. 1 Two stop bits.
SBR	Baud Rate Modulo Divisor. The 13 bits in SBR[12:0] set the modulo divide rate for the baud rate generator. When SBR is 1 - 8191, the baud rate equals "baud clock / ((OSR+1) × SBR)". The 13-bit baud rate setting [SBR12:SBR0] must only be updated when the transmitter and receiver are both disabled (LPUART_CTRL[RE] and LPUART_CTRL[TE] are both 0).

59.3.2 LPUART Status Register (LPUARTx_STAT)

Address: Base address + 4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	LBKDIF	RXEDGIF	MSBF	RXINV	RWUID	BRK13	LBKDE	RAF	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
W	w1c	w1c										w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MA1F	MA2F	0													
W	w1c	w1c														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LPUARTx_STAT field descriptions

Field	Description
31 LBKDIF	LIN Break Detect Interrupt Flag LBKDIF is set when the LIN break detect circuitry is enabled and a LIN break character is detected. LBKDIF is cleared by writing a 1 to it.

Table continues on the next page...

LPUARTx_STAT field descriptions (continued)

Field	Description
	0 No LIN break character has been detected. 1 LIN break character has been detected.
30 RXEDGIF	LPUART_RX Pin Active Edge Interrupt Flag RXEDGIF is set when an active edge, falling if RXINV = 0, rising if RXINV=1, on the LPUART_RX pin occurs. RXEDGIF is cleared by writing a 1 to it. 0 No active edge on the receive pin has occurred. 1 An active edge on the receive pin has occurred.
29 MSBF	MSB First Setting this bit reverses the order of the bits that are transmitted and received on the wire. This bit does not affect the polarity of the bits, the location of the parity bit or the location of the start or stop bits. This bit should only be changed when the transmitter and receiver are both disabled. 0 LSB (bit0) is the first bit that is transmitted following the start bit. Further, the first bit received after the start bit is identified as bit0. 1 MSB (bit9, bit8, bit7 or bit6) is the first bit that is transmitted following the start bit depending on the setting of CTRL[M], CTRL[PE] and BAUD[M10]. Further, the first bit received after the start bit is identified as bit9, bit8, bit7 or bit6 depending on the setting of CTRL[M] and CTRL[PE].
28 RXINV	Receive Data Inversion Setting this bit reverses the polarity of the received data input. **NOTE:** Setting RXINV inverts the LPUART_RX input for all cases: data bits, start and stop bits, break, and idle. 0 Receive data not inverted. 1 Receive data inverted.
27 RWUID	Receive Wake Up Idle Detect For RWU on idle character, RWUID controls whether the idle character that wakes up the receiver sets the IDLE bit. For address match wakeup, RWUID controls if the IDLE bit is set when the address does not match. This bit should only be changed when the receiver is disabled. 0 During receive standby state (RWU = 1), the IDLE bit does not get set upon detection of an idle character. During address match wakeup, the IDLE bit does not get set when an address does not match. 1 During receive standby state (RWU = 1), the IDLE bit gets set upon detection of an idle character. During address match wakeup, the IDLE bit does get set when an address does not match.
26 BRK13	Break Character Generation Length BRK13 selects a longer transmitted break character length. Detection of a framing error is not affected by the state of this bit. This bit should only be changed when the transmitter is disabled. 0 Break character is transmitted with length of 10 bit times (if M = 0, SBNS = 0) or 11 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 12 (if M = 1, SBNS = 1 or M10 = 1, SNBS = 0) or 13 (if M10 = 1, SNBS = 1). 1 Break character is transmitted with length of 13 bit times (if M = 0, SBNS = 0) or 14 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 15 (if M = 1, SBNS = 1 or M10 = 1, SNBS = 0) or 16 (if M10 = 1, SNBS = 1).
25 LBKDE	LIN Break Detection Enable LBKDE selects a longer break character detection length. While LBKDE is set, receive data is not stored in the receive data buffer.

Table continues on the next page...

LPUARTx_STAT field descriptions (continued)

Field	Description
	0 Break character is detected at length 10 bit times (if M = 0, SBNS = 0) or 11 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 12 (if M = 1, SBNS = 1 or M10 = 1, SNBS = 0) or 13 (if M10 = 1, SNBS = 1). 1 Break character is detected at length of 11 bit times (if M = 0, SBNS = 0) or 12 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 14 (if M = 1, SBNS = 1 or M10 = 1, SNBS = 0) or 15 (if M10 = 1, SNBS = 1).
24 RAF	Receiver Active Flag RAF is set when the receiver detects the beginning of a valid start bit, and RAF is cleared automatically when the receiver detects an idle line. 0 LPUART receiver idle waiting for a start bit. 1 LPUART receiver active (LPUART_RX input not idle).
23 TDRE	Transmit Data Register Empty Flag When the transmit FIFO is enabled, TDRE will set when the number of datawords in the transmit FIFO (LPUART_DATA) is equal to or less than the number indicated by LPUART_WATER[TXWATER]). To clear TDRE, write to the LPUART data register (LPUART_DATA) until the number of words in the transmit FIFO is greater than the number indicated by LPUART_WATER[TXWATER]. When the transmit FIFO is disabled,TDRE will set when the transmit data register (LPUART_DATA) is empty. To clear TDRE, write to the LPUART data register (LPUART_DATA). TDRE is not affected by a character that is in the process of being transmitted, it is updated at the start of each transmitted character. 0 Transmit data buffer full. 1 Transmit data buffer empty.
22 TC	Transmission Complete Flag TC is cleared when there is a transmission in progress or when a preamble or break character is loaded. TC is set when the transmit buffer is empty and no data, preamble, or break character is being transmitted. When TC is set, the transmit data output signal becomes idle (logic 1). TC is cleared by writing to LPUART_DATA to transmit new data, queuing a preamble by clearing and then setting LPUART_CTRL[TE], queuing a break character by writing 1 to LPUART_CTRL[SBK]. 0 Transmitter active (sending data, a preamble, or a break). 1 Transmitter idle (transmission activity complete).
21 RDRF	Receive Data Register Full Flag When the receive FIFO is enabled, RDRF is set when the number of datawords in the receive buffer is greater than the number indicated by LPUART_WATER[RXWATER]. To clear RDRF, read LPUART_DATA until the number of datawords in the receive data buffer is equal to or less than the number indicated by LPUART_WATER[RXWATER]. When the receive FIFO is disabled, RDRF is set when the receive buffer (LPUART_DATA) is full. To clear RDRF, read the LPUART_DATA register. A character that is in the process of being received does not cause a change in RDRF until the entire character is received. Even if RDRF is set, the character will continue to be received until an overrun condition occurs once the entire character is received. 0 Receive data buffer empty. 1 Receive data buffer full.
20 IDLE	Idle Line Flag IDLE is set when the LPUART receive line becomes idle for a full character time after a period of activity. When ILT is cleared, the receiver starts counting idle bit times after the start bit. If the receive character is all 1s, these bit times and the stop bits time count toward the full character time of logic high, 10 to 13 bit times, needed for the receiver to detect an idle line. When ILT is set, the receiver doesn't start counting

Table continues on the next page...

LPUARTx_STAT field descriptions (continued)

Field	Description
	idle bit times until after the stop bits. The stop bits and any logic high bit times at the end of the previous character do not count toward the full character time of logic high needed for the receiver to detect an idle line. To clear IDLE, write logic 1 to the IDLE flag. After IDLE has been cleared, it cannot become set again until after a new character has been stored in the receive buffer or a LIN break character has set the LBKDIF flag . IDLE is set only once even if the receive line remains idle for an extended period. 0 No idle line detected. 1 Idle line was detected.
19 OR	Receiver Overrun Flag OR is set when software fails to prevent the receive data register from overflowing with data. The OR bit is set immediately after the stop bit has been completely received for the dataword that overflows the buffer and all the other error flags (FE, NF, and PF) are prevented from setting. The data in the shift register is lost, but the data already in the LPUART data registers is not affected. If LBKDE is enabled and a LIN Break is detected, the OR field asserts if LBKDIF is not cleared before the next data character is received. While the OR flag is set, no additional data is stored in the data buffer even if sufficient room exists. To clear OR, write logic 1 to the OR flag. 0 No overrun. 1 Receive overrun (new LPUART data lost).
18 NF	Noise Flag The advanced sampling technique used in the receiver takes three samples in each of the received bits. If any of these samples disagrees with the rest of the samples within any bit time in the frame then noise is detected for that character. NF is set whenever the next character to be read from LPUART_DATA was received with noise detected within the character. To clear NF, write logic one to the NF. 0 No noise detected. 1 Noise detected in the received character in LPUART_DATA.
17 FE	Framing Error Flag FE is set whenever the next character to be read from LPUART_DATA was received with logic 0 detected where a stop bit was expected. To clear FE, write logic one to the FE. 0 No framing error detected. This does not guarantee the framing is correct. 1 Framing error.
16 PF	Parity Error Flag PF is set whenever the next character to be read from LPUART_DATA was received when parity is enabled (PE = 1) and the parity bit in the received character does not agree with the expected parity value. To clear PF, write a logic one to the PF. 0 No parity error. 1 Parity error.
15 MA1F	Match 1 Flag MA1F is set whenever the next character to be read from LPUART_DATA matches MA1. To clear MA1F, write a logic one to the MA1F. 0 Received data is not equal to MA1 1 Received data is equal to MA1

Table continues on the next page...

LPUARTx_STAT field descriptions (continued)

Field	Description
14 MA2F	Match 2 Flag MA2F is set whenever the next character to be read from LPUART_DATA matches MA2. To clear MA2F, write a logic one to the MA2F. 0 Received data is not equal to MA2 1 Received data is equal to MA2
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

59.3.3 LPUART Control Register (LPUARTx_CTRL)

This read/write register controls various optional features of the LPUART system. This register should only be altered when the transmitter and receiver are both disabled.

Address: Base address + 8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	R8T9	R9T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MA1IE	MA2IE	0			IDLECFG			LOOPS	DOZEEN	RSRC	M	WAKE	ILT	PE	PT
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LPUARTx_CTRL field descriptions

Field	Description
31 R8T9	Receive Bit 8 / Transmit Bit 9 R8 is the ninth data bit received when the LPUART is configured for 9-bit or 10-bit data formats. When reading 9-bit or 10-bit data, read R8 before reading LPUART_DATA. T9 is the tenth data bit received when the LPUART is configured for 10-bit data formats. When writing 10-bit data, write T9 before writing LPUART_DATA. If T9 does not need to change from its previous value, such as when it is used to generate address mark or parity, they it need not be written each time LPUART_DATA is written.
30 R9T8	Receive Bit 9 / Transmit Bit 8

Table continues on the next page...

LPUARTx_CTRL field descriptions (continued)

Field	Description
	R9 is the tenth data bit received when the LPUART is configured for 10-bit data formats. When reading 10-bit data, read R9 before reading LPUART_DATA T8 is the ninth data bit received when the LPUART is configured for 9-bit or 10-bit data formats. When writing 9-bit or 10-bit data, write T8 before writing LPUART_DATA. If T8 does not need to change from its previous value, such as when it is used to generate address mark or parity, they it need not be written each time LPUART_DATA is written.
29 TXDIR	LPUART_TX Pin Direction in Single-Wire Mode When the LPUART is configured for single-wire half-duplex operation (LOOPS = RSRC = 1), this bit determines the direction of data at the LPUART_TX pin. When clearing TXDIR, the transmitter will finish receiving the current character (if any) before the receiver starts receiving data from the LPUART_TX pin. 0 LPUART_TX pin is an input in single-wire mode. 1 LPUART_TX pin is an output in single-wire mode.
28 TXINV	Transmit Data Inversion Setting this bit reverses the polarity of the transmitted data output. **NOTE:** Setting TXINV inverts the LPUART_TX output for all cases: data bits, start and stop bits, break, and idle. 0 Transmit data not inverted. 1 Transmit data inverted.
27 ORIE	Overrun Interrupt Enable This bit enables the overrun flag (OR) to generate hardware interrupt requests. 0 OR interrupts disabled; use polling. 1 Hardware interrupt requested when OR is set.
26 NEIE	Noise Error Interrupt Enable This bit enables the noise flag (NF) to generate hardware interrupt requests. 0 NF interrupts disabled; use polling. 1 Hardware interrupt requested when NF is set.
25 FEIE	Framing Error Interrupt Enable This bit enables the framing error flag (FE) to generate hardware interrupt requests. 0 FE interrupts disabled; use polling. 1 Hardware interrupt requested when FE is set.
24 PEIE	Parity Error Interrupt Enable This bit enables the parity error flag (PF) to generate hardware interrupt requests. 0 PF interrupts disabled; use polling). 1 Hardware interrupt requested when PF is set.
23 TIE	Transmit Interrupt Enable Enables STAT[TDRE] to generate interrupt requests.

Table continues on the next page...

LPUARTx_CTRL field descriptions (continued)

Field	Description
	0 Hardware interrupts from TDRE disabled; use polling. 1 Hardware interrupt requested when TDRE flag is 1.
22 TCIE	Transmission Complete Interrupt Enable for TCIE enables the transmission complete flag, TC, to generate interrupt requests. 0 Hardware interrupts from TC disabled; use polling. 1 Hardware interrupt requested when TC flag is 1.
21 RIE	Receiver Interrupt Enable Enables STAT[RDRF] to generate interrupt requests. 0 Hardware interrupts from RDRF disabled; use polling. 1 Hardware interrupt requested when RDRF flag is 1.
20 ILIE	Idle Line Interrupt Enable ILIE enables the idle line flag, STAT[IDLE], to generate interrupt requests. 0 Hardware interrupts from IDLE disabled; use polling. 1 Hardware interrupt requested when IDLE flag is 1.
19 TE	Transmitter Enable Enables the LPUART transmitter. TE can also be used to queue an idle preamble by clearing and then setting TE. When TE is cleared, this register bit will read as 1 until the transmitter has completed the current character and the LPUART_TX pin is tristated. 0 Transmitter disabled. 1 Transmitter enabled.
18 RE	Receiver Enable Enables the LPUART receiver. When RE is written to 0, this register bit will read as 1 until the receiver finishes receiving the current character (if any). 0 Receiver disabled. 1 Receiver enabled.
17 RWU	Receiver Wakeup Control This field can be set to place the LPUART receiver in a standby state. RWU automatically clears when an RWU event occurs, that is, an IDLE event when CTRL[WAKE] is clear or an address match when CTRL[WAKE] is set with STAT[RWUID] is clear. **NOTE:** RWU must be set only with CTRL[WAKE] = 0 (wakeup on idle) if the channel is currently not idle. This can be determined by STAT[RAF]. If the flag is set to wake up an IDLE event and the channel is already idle, it is possible that the LPUART will discard data. This is because the data must be received or a LIN break detected after an IDLE is detected before IDLE is allowed to be reasserted. 0 Normal receiver operation. 1 LPUART receiver in standby waiting for wakeup condition.
16 SBK	Send Break Writing a 1 and then a 0 to SBK queues a break character in the transmit data stream. Additional break characters of 10 to 13, or 13 to 16 if LPUART_STATBRK13] is set, bit times of logic 0 are queued as long

Table continues on the next page...

LPUARTx_CTRL field descriptions (continued)

Field	Description
	as SBK is set. Depending on the timing of the set and clear of SBK relative to the information currently being transmitted, a second break character may be queued before software clears SBK. 0 Normal transmitter operation. 1 Queue break character(s) to be sent.
15 MA1IE	Match 1 Interrupt Enable 0 MA1F interrupt disabled 1 MA1F interrupt enabled
14 MA2IE	Match 2 Interrupt Enable 0 MA2F interrupt disabled 1 MA2F interrupt enabled
13–11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10–8 IDLECFG	Idle Configuration Configures the number of idle characters that must be received before the IDLE flag is set. 000 1 idle character 001 2 idle characters 010 4 idle characters 011 8 idle characters 100 16 idle characters 101 32 idle characters 110 64 idle characters 111 128 idle characters
7 LOOPS	Loop Mode Select When LOOPS is set, the LPUART_RX pin is disconnected from the LPUART and the transmitter output is internally connected to the receiver input. The transmitter and the receiver must be enabled to use the loop function. 0 Normal operation - LPUART_RX and LPUART_TX use separate pins. 1 Loop mode or single-wire mode where transmitter outputs are internally connected to receiver input (see RSRC bit).
6 DOZEEN	Doze Enable 0 LPUART is enabled in Doze mode. 1 LPUART is disabled in Doze mode.
5 RSRC	Receiver Source Select This field has no meaning or effect unless the LOOPS field is set. When LOOPS is set, the RSRC field determines the source for the receiver shift register input. 0 Provided LOOPS is set, RSRC is cleared, selects internal loop back mode and the LPUART does not use the LPUART_RX pin. 1 Single-wire LPUART mode where the LPUART_TX pin is connected to the transmitter output and receiver input.
4 M	9-Bit or 8-Bit Mode Select

Table continues on the next page...

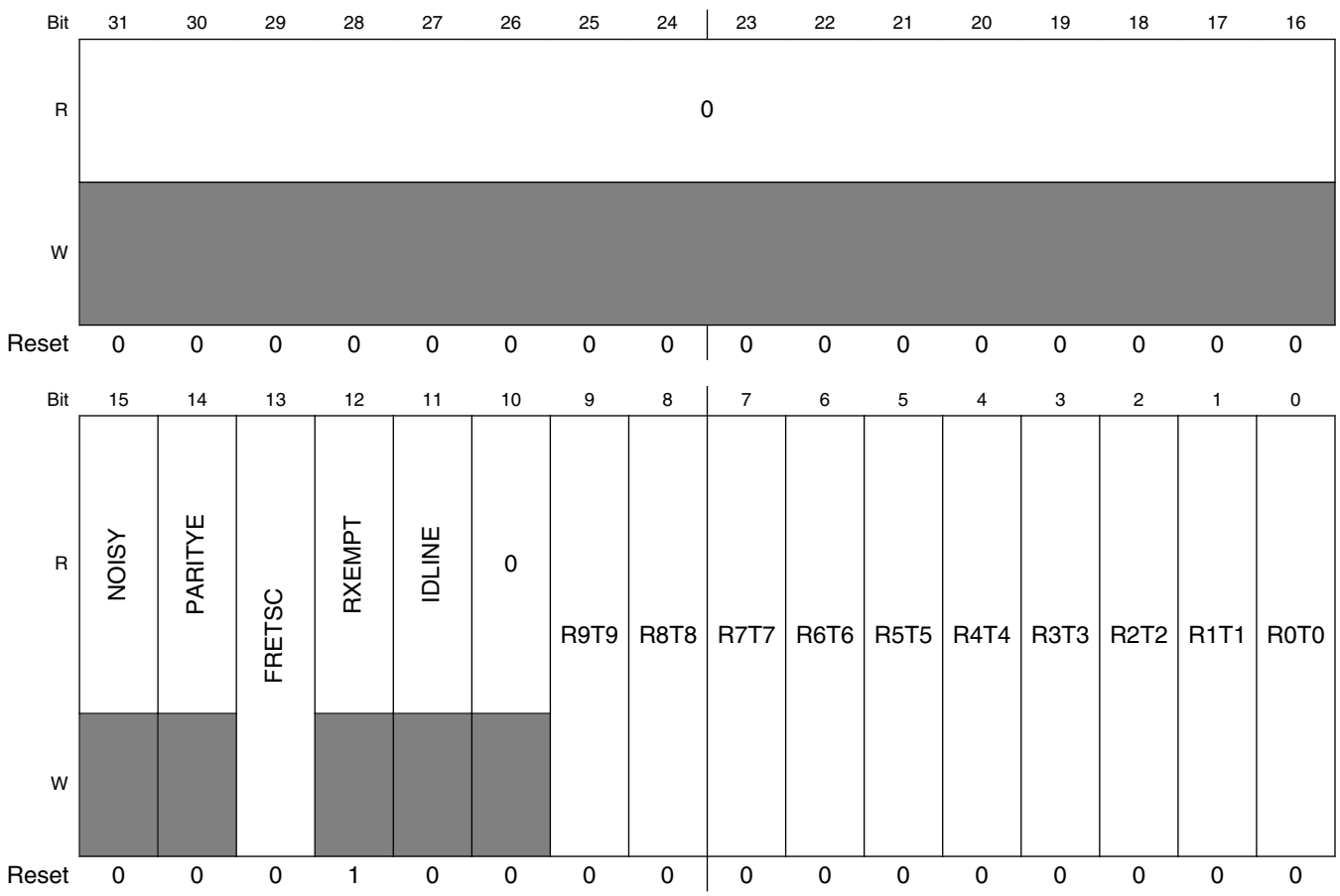
LPUARTx_CTRL field descriptions (continued)

Field	Description
	0 Receiver and transmitter use 8-bit data characters. 1 Receiver and transmitter use 9-bit data characters.
3 WAKE	Receiver Wakeup Method Select Determines which condition wakes the LPUART when RWU=1: • Address mark in the most significant bit position of a received data character, or • An idle condition on the receive pin input signal. 0 Configures RWU for idle-line wakeup. 1 Configures RWU with address-mark wakeup.
2 ILT	Idle Line Type Select Determines when the receiver starts counting logic 1s as idle character bits. The count begins either after a valid start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit can cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions. **NOTE:** In case the LPUART is programmed with ILT = 1, a logic 0 is automatically shifted after a received stop bit, therefore resetting the idle count. 0 Idle character bit count starts after start bit. 1 Idle character bit count starts after stop bit.
1 PE	Parity Enable Enables hardware parity generation and checking. When parity is enabled, the bit immediately before the stop bit is treated as the parity bit. 0 No hardware parity generation or checking. 1 Parity enabled.
0 PT	Parity Type Provided parity is enabled (PE = 1), this bit selects even or odd parity. Odd parity means the total number of 1s in the data character, including the parity bit, is odd. Even parity means the total number of 1s in the data character, including the parity bit, is even. 0 Even parity. 1 Odd parity.

59.3.4 LPUART Data Register (LPUARTx_DATA)

This register is actually two separate registers. Reads return the contents of the read-only receive data buffer and writes go to the write-only transmit data buffer. Reads and writes of this register are also involved in the automatic flag clearing mechanisms for some of the LPUART status flags.

Address: Base address + Ch offset



LPUARTx_DATA field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15 NOISY	The current received dataword contained in DATA[R9:R0] was received with noise. 0 The dataword was received without noise. 1 The data was received with noise.
14 PARITYE	The current received dataword contained in DATA[R9:R0] was received with a parity error.

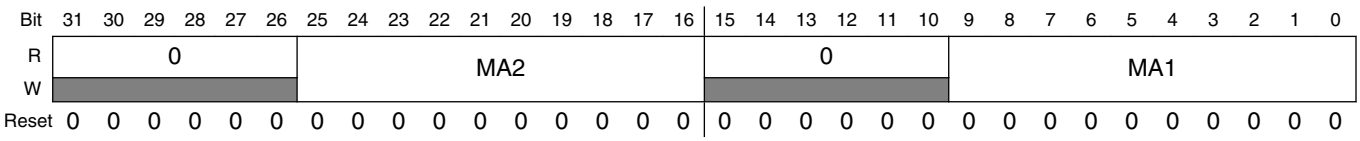
Table continues on the next page...

LPUARTx_DATA field descriptions (continued)

Field	Description
	0 The dataword was received without a parity error. 1 The dataword was received with a parity error.
13 FRETSC	Frame Error / Transmit Special Character For reads, indicates the current received dataword contained in DATA[R9:R0] was received with a frame error. For writes, indicates a break or idle character is to be transmitted instead of the contents in DATA[T9:T0]. T9 is used to indicate a break character when 0 and a idle character when 1, he contents of DATA[T8:T0] should be zero. 0 The dataword was received without a frame error on read, transmit a normal character on write. 1 The dataword was received with a frame error, transmit an idle or break character on transmit.
12 RXEMPT	Receive Buffer Empty Asserts when there is no data in the receive buffer. This field does not take into account data that is in the receive shift register. 0 Receive buffer contains valid data. 1 Receive buffer is empty, data returned on read is not valid.
11 IDLINE	Idle Line Indicates the receiver line was idle before receiving the character in DATA[9:0]. Unlike the IDLE flag, this bit can set for the first character received when the receiver is first enabled. 0 Receiver was not idle before receiving this character. 1 Receiver was idle before receiving this character.
10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9 R9T9	Read receive data buffer 9 or write transmit data buffer 9.
8 R8T8	Read receive data buffer 8 or write transmit data buffer 8.
7 R7T7	Read receive data buffer 7 or write transmit data buffer 7.
6 R6T6	Read receive data buffer 6 or write transmit data buffer 6.
5 R5T5	Read receive data buffer 5 or write transmit data buffer 5.
4 R4T4	Read receive data buffer 4 or write transmit data buffer 4.
3 R3T3	Read receive data buffer 3 or write transmit data buffer 3.
2 R2T2	Read receive data buffer 2 or write transmit data buffer 2.
1 R1T1	Read receive data buffer 1 or write transmit data buffer 1.
0 R0T0	Read receive data buffer 0 or write transmit data buffer 0.

59.3.5 LPUART Match Address Register (LPUARTx_MATCH)

Address: Base address + 10h offset



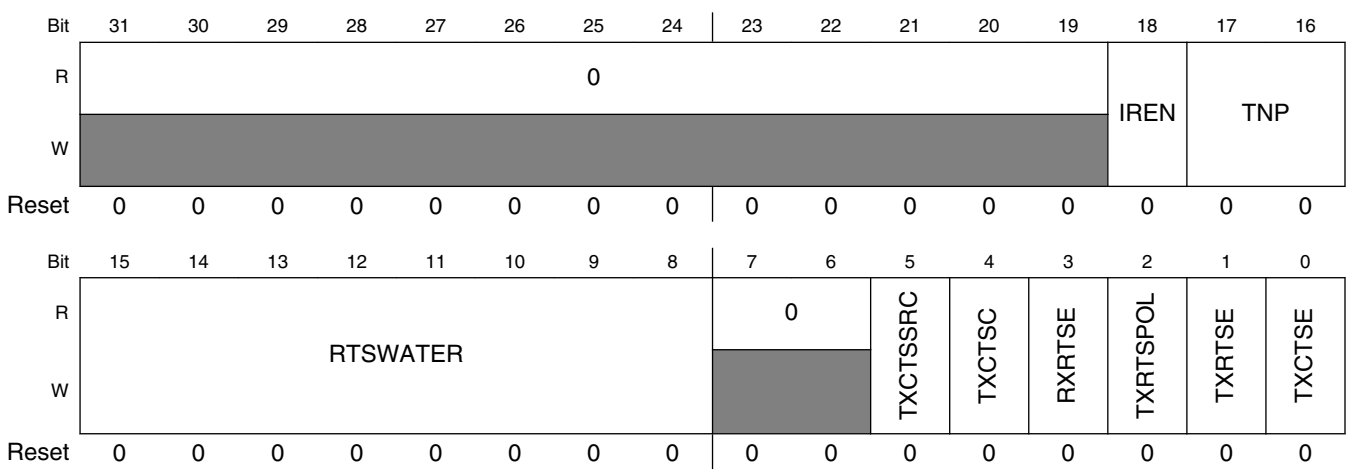
LPUARTx_MATCH field descriptions

Field	Description
31–26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25–16 MA2	Match Address 2 The MA1 and MA2 registers are compared to input data addresses when the most significant bit is set and the associated BAUD[MAEN] bit is set. If a match occurs, the following data is transferred to the data register. If a match fails, the following data is discarded. Software should only write a MA register when the associated BAUD[MAEN] bit is clear.
15–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
MA1	Match Address 1 The MA1 and MA2 registers are compared to input data addresses when the most significant bit is set and the associated BAUD[MAEN] bit is set. If a match occurs, the following data is transferred to the data register. If a match fails, the following data is discarded. Software should only write a MA register when the associated BAUD[MAEN] bit is clear.

59.3.6 LPUART Modem IrDA Register (LPUARTx_MODIR)

The MODEM register controls options for setting the modem configuration.

Address: Base address + 14h offset



LPUARTx_MODIR field descriptions

Field	Description
31–19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18 IREN	Infrared enable Enables/disables the infrared modulation/demodulation. 0 IR disabled. 1 IR enabled.
17–16 TNP	Transmitter narrow pulse Enables whether the LPUART transmits a 1/OSR, 2/OSR, 3/OSR or 4/OSR narrow pulse. 00 1/OSR. 01 2/OSR. 10 3/OSR. 11 4/OSR.
15–8 RTSWATER	Receive RTS Configuration Configures the point at which the RX RTS output negates based on the number of additional characters that can be stored in the Receive FIFO. When configured to 0, RTS negates when the the start bit is detetected for the character that will cause the FIFO to become full. 0 RTS asserts when the receiver FIFO is full or receiving a character that causes the FIFO to become full. 1 RTS asserts when the receive FIFO is less than or equal to the RXWATER configuration and negates when the receive FIFO is greater than the RXWATER configuration.
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 TXCTSSRC	Transmit CTS Source Configures the source of the CTS input. 0 CTS input is the LPUART_CTS pin. 1 CTS input is the inverted Receiver Match result.
4 TXCTSC	Transmit CTS Configuration Configures if the CTS state is checked at the start of each character or only when the transmitter is idle. 0 CTS input is sampled at the start of each character. 1 CTS input is sampled when the transmitter is idle.
3 RXRTSE	Receiver request-to-send enable Allows the RTS output to control the CTS input of the transmitting device to prevent receiver overrun. **NOTE:** Do not set both RXRTSE and TXRTSE. 0 The receiver has no effect on RTS. 1 RTS is deasserted if the receiver data register is full or a start bit has been detected that would cause the receiver data register to become full. RTS is asserted if the receiver data register is not full and has not detected a start bit that would cause the receiver data register to become full.RTS assertion is configured by the RTSWATER field

Table continues on the next page...

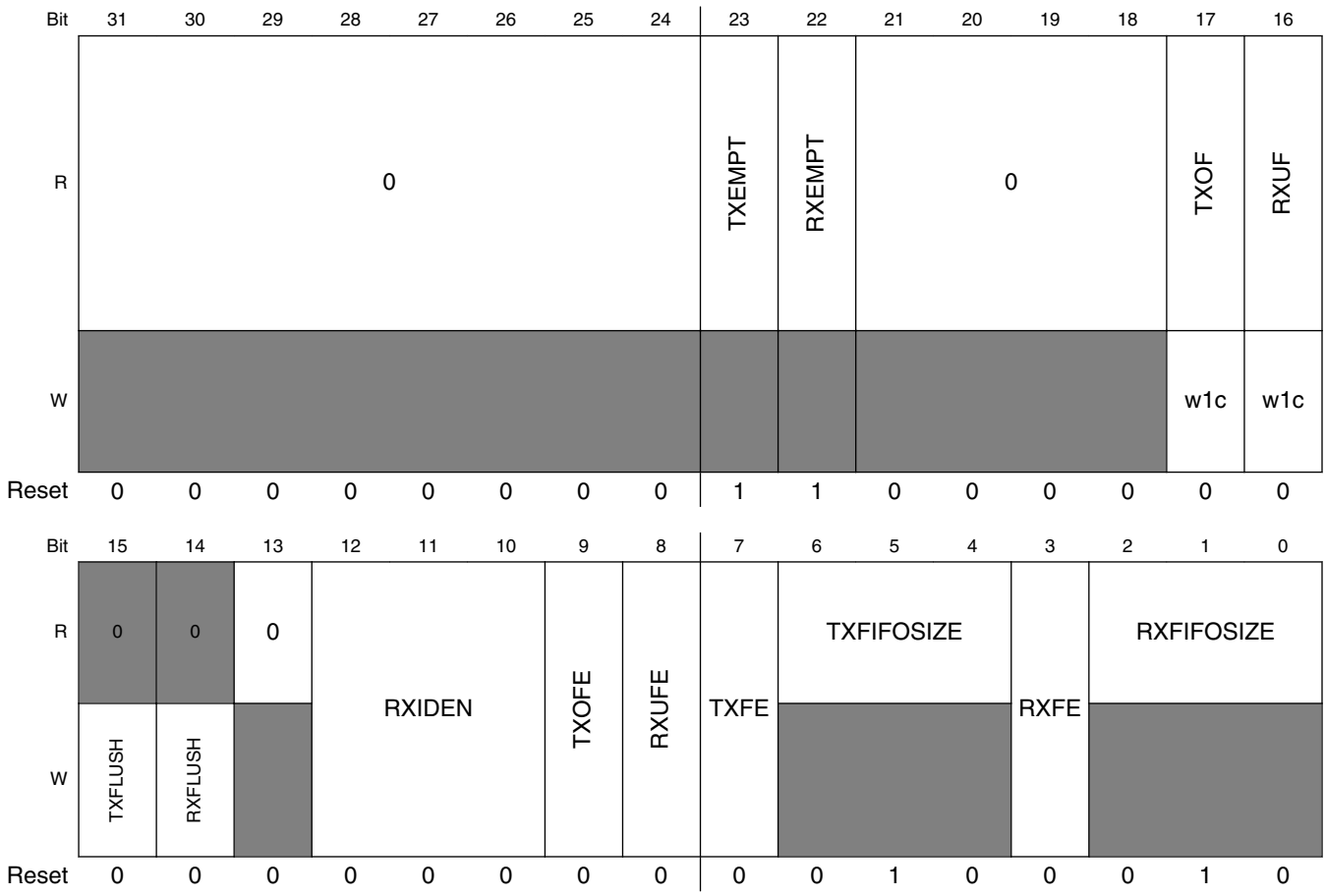
LPUARTx_MODIR field descriptions (continued)

Field	Description
2 TXRTSPOL	Transmitter request-to-send polarity Controls the polarity of the transmitter RTS. TXRTSPOL does not affect the polarity of the receiver RTS. RTS will remain negated in the active low state unless TXRTSE is set. 0 Transmitter RTS is active low. 1 Transmitter RTS is active high.
1 TXRTSE	Transmitter request-to-send enable Controls RTS before and after a transmission. 0 The transmitter has no effect on RTS. 1 When a character is placed into an empty transmitter data buffer , RTS asserts one bit time before the start bit is transmitted. RTS deasserts one bit time after all characters in the transmitter data buffer and shift register are completely sent, including the last stop bit.
0 TXCTSE	Transmitter clear-to-send enable TXCTSE controls the operation of the transmitter. TXCTSE can be set independently from the state of TXRTSE and RXRTSE. 0 CTS has no effect on the transmitter. 1 Enables clear-to-send operation. The transmitter checks the state of CTS each time it is ready to send a character. If CTS is asserted, the character is sent. If CTS is deasserted, the signal TXD remains in the mark state and transmission is delayed until CTS is asserted. Changes in CTS as a character is being sent do not affect its transmission.

59.3.7 LPUART FIFO Register (LPUARTx_FIFO)

This register provides the ability for the programmer to turn on and off FIFO functionality. It also provides the size of the FIFO that has been implemented. This register may be read at any time. This register must be written only when CTRL[RE] and CTRL[TE] are cleared/not set and when the data buffer/FIFO is empty.

Address: Base address + 18h offset



LPUARTx_FIFO field descriptions

Field	Description
31–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23 TXEMPT	Transmit Buffer/FIFO Empty Asserts when there is no data in the Transmit FIFO/buffer. This field does not take into account data that is in the transmit shift register. 0 Transmit buffer is not empty. 1 Transmit buffer is empty.

Table continues on the next page...

LPUARTx_FIFO field descriptions (continued)

Field	Description
22 RXEMPT	Receive Buffer/FIFO Empty Asserts when there is no data in the receive FIFO/Buffer. This field does not take into account data that is in the receive shift register. 0 Receive buffer is not empty. 1 Receive buffer is empty.
21–18 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
17 TXOF	Transmitter Buffer Overflow Flag Indicates that more data has been written to the transmit buffer than it can hold. This field will assert regardless of the value of TXOFE. However, an interrupt will be issued to the host only if TXOFE is set. This flag is cleared by writing a 1. 0 No transmit buffer overflow has occurred since the last time the flag was cleared. 1 At least one transmit buffer overflow has occurred since the last time the flag was cleared.
16 RXUF	Receiver Buffer Underflow Flag Indicates that more data has been read from the receive buffer than was present. This field will assert regardless of the value of RXUFE. However, an interrupt will be issued to the host only if RXUFE is set. This flag is cleared by writing a 1. 0 No receive buffer underflow has occurred since the last time the flag was cleared. 1 At least one receive buffer underflow has occurred since the last time the flag was cleared.
15 TXFLUSH	Transmit FIFO/Buffer Flush Writing to this field causes all data that is stored in the transmit FIFO/buffer to be flushed. This does not affect data that is in the transmit shift register. 0 No flush operation occurs. 1 All data in the transmit FIFO/Buffer is cleared out.
14 RXFLUSH	Receive FIFO/Buffer Flush Writing to this field causes all data that is stored in the receive FIFO/buffer to be flushed. This does not affect data that is in the receive shift register. 0 No flush operation occurs. 1 All data in the receive FIFO/buffer is cleared out.
13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12–10 RXIDEN	Receiver Idle Empty Enable When set, enables the assertion of RDRF when the receiver is idle for a number of idle characters and the FIFO is not empty. 000 Disable RDRF assertion due to partially filled FIFO when receiver is idle. 001 Enable RDRF assertion due to partially filled FIFO when receiver is idle for 1 character. 010 Enable RDRF assertion due to partially filled FIFO when receiver is idle for 2 characters. 011 Enable RDRF assertion due to partially filled FIFO when receiver is idle for 4 characters. 100 Enable RDRF assertion due to partially filled FIFO when receiver is idle for 8 characters. 101 Enable RDRF assertion due to partially filled FIFO when receiver is idle for 16 characters.

Table continues on the next page...

LPUARTx_FIFO field descriptions (continued)

Field	Description
	110 Enable RDRF assertion due to partially filled FIFO when receiver is idle for 32 characters. 111 Enable RDRF assertion due to partially filled FIFO when receiver is idle for 64 characters.
9 TXOFE	Transmit FIFO Overflow Interrupt Enable When this field is set, the TXOF flag generates an interrupt to the host. 0 TXOF flag does not generate an interrupt to the host. 1 TXOF flag generates an interrupt to the host.
8 RXUFE	Receive FIFO Underflow Interrupt Enable When this field is set, the RXUF flag generates an interrupt to the host. 0 RXUF flag does not generate an interrupt to the host. 1 RXUF flag generates an interrupt to the host.
7 TXFE	Transmit FIFO Enable When this field is set, the built in FIFO structure for the transmit buffer is enabled. The size of the FIFO structure is indicated by TXFIFOSIZE. If this field is not set, the transmit buffer operates as a FIFO of depth one dataword regardless of the value in TXFIFOSIZE. Both CTRL[TE] and CTRL[RE] must be cleared prior to changing this field. 0 Transmit FIFO is not enabled. Buffer is depth 1. (Legacy support). 1 Transmit FIFO is enabled. Buffer is depth indicated by TXFIFOSIZE.
6–4 TXFIFOSIZE	Transmit FIFO. Buffer Depth The maximum number of transmit datawords that can be stored in the transmit buffer. This field is read only. 000 Transmit FIFO/Buffer depth = 1 dataword. 001 Transmit FIFO/Buffer depth = 4 datawords. 010 Transmit FIFO/Buffer depth = 8 datawords. 011 Transmit FIFO/Buffer depth = 16 datawords. 100 Transmit FIFO/Buffer depth = 32 datawords. 101 Transmit FIFO/Buffer depth = 64 datawords. 110 Transmit FIFO/Buffer depth = 128 datawords. 111 Transmit FIFO/Buffer depth = 256 datawords
3 RXFE	Receive FIFO Enable When this field is set, the built in FIFO structure for the receive buffer is enabled. The size of the FIFO structure is indicated by the RXFIFOSIZE field. If this field is not set, the receive buffer operates as a FIFO of depth one dataword regardless of the value in RXFIFOSIZE. Both CTRL[TE] and CTRL[RE] must be cleared prior to changing this field. 0 Receive FIFO is not enabled. Buffer is depth 1. (Legacy support) 1 Receive FIFO is enabled. Buffer is depth indicted by RXFIFOSIZE.
RXFIFOSIZE	Receive FIFO. Buffer Depth The maximum number of receive datawords that can be stored in the receive buffer before an overrun occurs. This field is read only. 000 Receive FIFO/Buffer depth = 1 dataword.

Table continues on the next page...

LPUARTx_FIFO field descriptions (continued)

Field	Description
	001 Receive FIFO/Buffer depth = 4 datawords. 010 Receive FIFO/Buffer depth = 8 datawords. 011 Receive FIFO/Buffer depth = 16 datawords. 100 Receive FIFO/Buffer depth = 32 datawords. 101 Receive FIFO/Buffer depth = 64 datawords. 110 Receive FIFO/Buffer depth = 128 datawords. 111 Receive FIFO/Buffer depth = 256 datawords.

59.3.8 LPUART Watermark Register (LPUARTx_WATER)

This register provides the ability to set a programmable threshold for notification of needing additional transmit data. This register may be read at any time but must be written only when CTRL[TE] is not set.

Address: Base address + 1Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RXCOUNT								RXWATER								TXCOUNT								TXWATER							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LPUARTx_WATER field descriptions

Field	Description
31–24 RXCOUNT	Receive Counter The value in this register indicates the number of datawords that are in the receive FIFO/buffer. If a dataword is being received, that is, in the receive shift register, it is not included in the count. This value may be used in conjunction with FIFO[RXFIFOSIZE] to calculate how much room is left in the receive FIFO/buffer.
23–16 RXWATER	Receive Watermark When the number of datawords in the receive FIFO/buffer is greater than the value in this register field, an interrupt or a DMA request is generated. For proper operation, the value in RXWATER must be set to be less than the receive FIFO/buffer size as indicated by FIFO[RXFIFOSIZE] and FIFO[RXFE] and must be greater than 0.
15–8 TXCOUNT	Transmit Counter The value in this register indicates the number of datawords that are in the transmit FIFO/buffer. If a dataword is being transmitted, that is, in the transmit shift register, it is not included in the count. This value may be used in conjunction with FIFO[TXFIFOSIZE] to calculate how much room is left in the transmit FIFO/buffer.
TXWATER	Transmit Watermark When the number of datawords in the transmit FIFO/buffer is equal to or less than the value in this register field, an interrupt or a DMA request is generated. For proper operation, the value in TXWATER must be set to be less than the size of the transmit buffer/FIFO size as indicated by FIFO[TXFIFOSIZE] and FIFO[TXFE].

LPUARTx_WATER field descriptions (continued)

Field	Description

59.4 Functional description

The LPUART supports full-duplex, asynchronous, NRZ serial communication and comprises a baud rate generator, transmitter, and receiver block. The transmitter and receiver operate independently, although they use the same baud rate generator. The following describes each of the blocks of the LPUART.

59.4.1 Baud rate generation

A 13-bit modulus counter in the baud rate generator derive the baud rate for both the receiver and the transmitter. The value from 1 to 8191 written to SBR[12:0] determines the baud clock divisor for the asynchronous LPUART baud clock. The SBR bits are in the LPUART baud rate registers, BDH and BDL. The baud rate clock drives the receiver, while the transmitter is driven by the baud rate clock divided by the over sampling ratio. Depending on the over sampling ratio, the receiver has an acquisition rate of 4 to 32 samples per bit time.

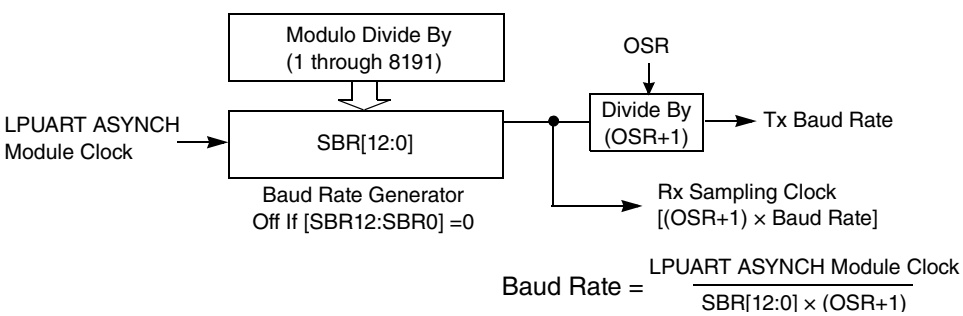


Figure 59-3. LPUART baud rate generation

Baud rate generation is subject to two sources of error:

- Integer division of the asynchronous LPUART baud clock may not give the exact target frequency.
- Synchronization with the asynchronous LPUART baud clock can cause phase shift.

59.4.2 Transmitter functional description

This section describes the overall block diagram for the LPUART transmitter, as well as specialized functions for sending break and idle characters.

The transmitter output (LPUART_TX) idle state defaults to logic high, CTRL[TXINV] is cleared following reset. The transmitter output is inverted by setting CTRL[TXINV]. The transmitter is enabled by setting the CTRL[TE] bit. This queues a preamble character that is one full character frame of the idle state. The transmitter then remains idle until data is available in the transmit data buffer. Programs store data into the transmit data buffer by writing to the LPUART data register.

The central element of the LPUART transmitter is the transmit shift register that is 10-bit to 13 bits long depending on the setting in the CTRL[M], BAUD[M10] and BAUD[SBNS] control bits. For the remainder of this section, assume CTRL[M], BAUD[M10] and BAUD[SBNS] are cleared, selecting the normal 8-bit data mode. In 8-bit data mode, the shift register holds a start bit, eight data bits, and a stop bit. When the transmit shift register is available for a new character, the value waiting in the transmit data register is transferred to the shift register, synchronized with the baud rate clock, and the transmit data register empty (STAT[TDRE]) status flag is set to indicate another character may be written to the transmit data buffer at LPUART_DATA.

If no new character is waiting in the transmit data buffer after a stop bit is shifted out the LPUART_TX pin, the transmitter sets the transmit complete flag and enters an idle mode, with LPUART_TX high, waiting for more characters to transmit.

Writing 0 to CTRL[TE] does not immediately disable the transmitter. The current transmit activity in progress must first be completed (that could include a data character, idle character or break character), although the transmitter will not start transmitting another character.

59.4.2.1 Send break and queued idle

The LPUART_CTRL[SBK] bit sends break characters originally used to gain the attention of old teletype receivers. Break characters are a full character time of logic 0, 10-bit to 12-bit times including the start and stop bits. A longer break of 13-bit times can be enabled by setting LPUART_STAT[BRK13]. Normally, a program would wait for LPUART_STAT[TDRE] to become set to indicate the last character of a message has moved to the transmit shifter, write 1, and then write 0 to the LPUART_CTRL[SBK] bit. This action queues a break character to be sent as soon as the shifter is available. If LPUART_CTRL[SBK] remains 1 when the queued break moves into the shifter,

synchronized to the baud rate clock, an additional break character is queued. If the receiving device is another Freescale Semiconductor LPUART, the break characters are received as 0s in all data bits and a framing error (LPUART_STAT[FE] = 1) occurs.

A break character can also be transmitted by writing to the LPUART_DATA register with bit 13 set and the data bits clear. This supports transmitting the break character as part of the normal data stream and also allows the DMA to transmit a break character.

When idle-line wakeup is used, a full character time of idle (logic 1) is needed between messages to wake up any sleeping receivers. Normally, a program would wait for LPUART_STAT[TDRE] to become set to indicate the last character of a message has moved to the transmit shifter, then write 0 and then write 1 to the LPUART_CTRL[TE] bit. This action queues an idle character to be sent as soon as the shifter is available. As long as the character in the shifter does not finish while LPUART_CTRL[TE] is cleared, the LPUART transmitter never actually releases control of the LPUART_TX pin.

An idle character can also be transmitted by writing to the LPUART_DATA register with bit 13 set and the data bits also set. This supports transmitting the idle character as part of the normal data stream and also allows the DMA to transmit a break character.

The length of the break character is affected by the LPUART_STAT[BRK13], LPUART_CTRL[M], LPUART_BAUD[M10] and LPUART_BAUD[SNBS] bits as shown below.

Table 59-2. Break character length

BRK13	M	M10	SBNS	Break character length
0	0	0	0	10 bit times
0	0	0	1	11 bit times
0	1	0	0	11 bit times
0	1	0	1	12 bit times
0	X	1	0	12 bit times
0	X	1	1	13 bit times
1	0	0	0	13 bit times
1	0	0	1	13 bit times
1	1	0	0	14 bit times
1	1	0	1	14 bit times
1	X	1	0	15 bit times
1	X	1	1	15 bit times

59.4.2.2 Hardware flow control

The transmitter supports hardware flow control by gating the transmission with the value of CTS. If the clear-to-send operation is enabled, the character is transmitted when CTS is asserted. If CTS is deasserted in the middle of a transmission with characters remaining in the receiver data buffer, the character in the shift register is sent and LPUART_TX remains in the mark state until CTS is reasserted.

If the clear-to-send operation is disabled, the transmitter ignores the state of CTS.

The transmitter's CTS signal can also be enabled even if the same LPUART receiver's RTS signal is disabled.

59.4.2.3 Transceiver driver enable

The transmitter can use LPUART_RTS as an enable signal for the driver of an external transceiver. See Transceiver driver enable using LPUART_RTS for details. If the request-to-send operation is enabled, when a character is placed into an empty transmitter data buffer, LPUART_RTS asserts one bit time before the start bit is transmitted. LPUART_RTS remains asserted for the whole time that the transmitter data buffer has any characters. LPUART_RTS deasserts one bit time after all characters in the transmitter data buffer and shift register are completely sent, including the last stop bit. Transmitting a break character also asserts LPUART_RTS, with the same assertion and deassertion timing as having a character in the transmitter data buffer.

The transmitter's LPUART_RTS signal asserts only when the transmitter is enabled. However, the transmitter's LPUART_RTS signal is unaffected by its LPUART_CTS signal. LPUART_RTS will remain asserted until the transfer is completed, even if the transmitter is disabled mid-way through a data transfer.

59.4.3 Receiver functional description

In this section, the receiver block diagram is a guide for the overall receiver functional description. Next, the data sampling technique used to reconstruct receiver data is described in more detail. Finally, different variations of the receiver wakeup function are explained.

The receiver input is inverted by setting LPUART_STAT[RXINV]. The receiver is enabled by setting the LPUART_CTRL[RE] bit. Character frames consist of a start bit of logic 0, eight to ten data bits (msb or lsb first), and one or two stop bits of logic 1. For

information about 9-bit or 10-bit data mode, refer to 8-bit, 9-bit and 10-bit data modes. For the remainder of this discussion, assume the LPUART is configured for normal 8-bit data mode.

After receiving the stop bit into the receive shifter, and provided the receive data register is not already full, the data character is transferred to the receive data register and the receive data register full (LPUART_STAT[RDRF]) status flag is set. If LPUART_STAT[RDRF] was already set indicating the receive data register (buffer) was already full, the overrun (OR) status flag is set and the new data is lost. Because the LPUART receiver is double-buffered, the program has one full character time after LPUART_STAT[RDRF] is set before the data in the receive data buffer must be read to avoid a receiver overrun.

When a program detects that the receive data register is full (LPUART_STAT[RDRF] = 1), it gets the data from the receive data register by reading LPUART_DATA. Refer to Interrupts and status flags for details about flag clearing.

59.4.3.1 Data sampling technique

The LPUART receiver supports a configurable oversampling rate of between 4× and 32× of the baud rate clock for sampling. The receiver starts by taking logic level samples at the oversampling rate times the baud rate to search for a falling edge on the LPUART_RX serial data input pin. A falling edge is defined as a logic 0 sample after three consecutive logic 1 samples. The oversampling baud rate clock divides the bit time into 4 to 32 segments from 1 to OSR (where OSR is the configured oversampling ratio). When a falling edge is located, three more samples are taken at (OSR/2), (OSR/2)+1, and (OSR/2)+2 to make sure this was a real start bit and not merely noise. If at least two of these three samples are 0, the receiver assumes it is synchronized to a received character. If another falling edge is detected before the receiver is considered synchronized, the receiver restarts the sampling from the first segment.

The receiver then samples each bit time, including the start and stop bits, at (OSR/2), (OSR/2)+1, and (OSR/2)+2 to determine the logic level for that bit. The logic level is interpreted to be that of the majority of the samples taken during the bit time. If any sample in any bit time, including the start and stop bits, in a character frame fails to agree with the logic level for that bit, the noise flag (LPUART_STAT[NF]) is set when the received character is transferred to the receive data buffer.

When the LPUART receiver is configured to sample on both edges of the baud rate clock, the number of segments in each received bit is effectively doubled (from 1 to OSR×2). The start and data bits are then sampled at OSR, OSR+1 and OSR+2. Sampling on both edges of the clock must be enabled for oversampling rates of 4× to 7× and is optional for higher oversampling rates.

The falling edge detection logic continuously looks for falling edges. If an edge is detected, the sample clock is resynchronized to bit times (unless resynchronization has been disabled). This improves the reliability of the receiver in the presence of noise or mismatched baud rates. It does not improve worst case analysis because some characters do not have any extra falling edges anywhere in the character frame.

In the case of a framing error, provided the received character was not a break character, the sampling logic that searches for a falling edge is filled with three logic 1 samples so that a new start bit can be detected almost immediately.

59.4.3.2 Receiver wakeup operation

Receiver wakeup and receiver address matching is a hardware mechanism that allows an LPUART receiver to ignore the characters in a message intended for a different receiver.

During receiver wakeup, all receivers evaluate the first character(s) of each message, and as soon as they determine the message is intended for a different receiver, they write logic 1 to the receiver wake up control bit (LPUART_CTRL[RWU]). When RWU bit and LPUART_S2[RWUID] bit are set, the status flags associated with the receiver, with the exception of the idle bit, IDLE, are inhibited from setting, thus eliminating the software overhead for handling the unimportant message characters. At the end of a message, or at the beginning of the next message, all receivers automatically force LPUART_CTRL[RWU] to 0 so all receivers wake up in time to look at the first character(s) of the next message.

During receiver address matching, the address matching is performed in hardware and the LPUART receiver will ignore all characters that do not meet the address match requirements.

Table 59-3. Receiver Wakeup Options

RWU	MA1 | MA2	MATCFG	WAKE:RWUID	Receiver Wakeup
0	0	X	X	Normal operation
1	0	00	00	Receiver wakeup on idle line, IDLE flag not set
1	0	00	01	Receiver wakeup on idle line, IDLE flag set

Table continues on the next page...

Table 59-3. Receiver Wakeup Options (continued)

RWU	MA1 | MA2	MATCFG	WAKE:RWUID	Receiver Wakeup
1	0	00	10	Receiver wakeup on address mark
1	1	11	X0	Receiver wakeup on data match
0	1	00	X0	Address mark address match, IDLE flag not set for discarded characters
0	1	00	X1	Address mark address match, IDLE flag set for discarded characters
0	1	01	X0	Idle line address match
0	1	10	X0	Address match on and address match off, IDLE flag not set for discarded characters
0	1	10	X1	Address match on and address match off, IDLE flag set for discarded characters

59.4.3.2.1 Idle-line wakeup

When wake is cleared, the receiver is configured for idle-line wakeup. In this mode, LPUART_CTRL[RWU] is cleared automatically when the receiver detects a full character time of the idle-line level. The LPUART_CTRL[M] and LPUART_BAUD[M10] control bit selects 8-bit to 10-bit data mode and the LPUART_BAUD[SBNS] bit selects 1-bit or 2-bit stop bit number that determines how many bit times of idle are needed to constitute a full character time, 10 to 13 bit times because of the start and stop bits.

When LPUART_CTRL[RWU] is one and LPUART_STAT[RWUID] is zero, the idle condition that wakes up the receiver does not set the LPUART_STAT[IDLE] flag. The receiver wakes up and waits for the first data character of the next message that sets the LPUART_STAT[RDRF] flag and generates an interrupt if enabled. When LPUART_STAT[RWUID] is one, any idle condition sets the LPUART_STAT[IDLE] flag and generates an interrupt if enabled, regardless of whether LPUART_CTRL[RWU] is zero or one.

The idle-line type (LPUART_CTRL[ILT]) control bit selects one of two ways to detect an idle line. When LPUART_CTRL[ILT] is cleared, the idle bit counter starts after the start bit so the stop bit and any logic 1s at the end of a character count toward the full

character time of idle. When LPUART_CTRL[ILT] is set, the idle bit counter does not start until after the stop bit time, so the idle detection is not affected by the data in the last character of the previous message.

59.4.3.2.2 Address-mark wakeup

When LPUART_CTRL[WAKE] is set, the receiver is configured for address-mark wakeup. In this mode, LPUART_CTRL[RWU] is cleared automatically when the receiver detects a logic 1 in the most significant bit of a received character.

Address-mark wakeup allows messages to contain idle characters, but requires the MSB be reserved for use in address frames. The logic 1 in the MSB of an address frame clears the LPUART_CTRL[RWU] bit before the stop bits are received and sets the LPUART_STAT[RDRF] flag. In this case, the character with the MSB set is received even though the receiver was sleeping during most of this character time.

59.4.3.2.3 Data match wakeup

When LPUART_CTRL[RWU] is set and LPUART_BAUD[MATCFG] equals 11, the receiver is configured for data match wakeup. In this mode, LPUART_CTRL[RWU] is cleared automatically when the receiver detects a character that matches MATCH[MA1] field when BAUD[MAEN1] is set, or that matches MATCH[MA2] when BAUD[MAEN2] is set.

59.4.3.2.4 Address Match operation

Address match operation is enabled when the LPUART_BAUD[MAEN1] or LPUART_BAUD[MAEN2] bit is set and LPUART_BAUD[MATCFG] is equal to 00. In this function, a character received by the LPUART_RX pin with a logic 1 in the bit position immediately preceding the stop bit is considered an address and is compared with the associated MATCH[MA1] or MATCH[MA2] field. The character is only transferred to the receive buffer, and LPUART_STAT[RDRF] is set, if the comparison matches. All subsequent characters received with a logic 0 in the bit position immediately preceding the stop bit are considered to be data associated with the address and are transferred to the receive data buffer. If no marked address match occurs then no transfer is made to the receive data buffer, and all following characters with logic zero in the bit position immediately preceding the stop bit are also discarded. If both the LPUART_BAUD[MAEN1] and LPUART_BAUD[MAEN2] bits are negated, the receiver operates normally and all data received is transferred to the receive data buffer.

Address match operation functions in the same way for both MATCH[MA1] and MATCH[MA2] fields.

- If only one of LPUART_BAUD[MAEN1] and LPUART_BAUD[MAEN2] is asserted, a marked address is compared only with the associated match register and data is transferred to the receive data buffer only on a match.
- If LPUART_BAUD[MAEN1] and LPUART_BAUD[MAEN2] are asserted, a marked address is compared with both match registers and data is transferred only on a match with either register.

59.4.3.2.5 Idle Match operation

Idle match operation is enabled when the LPUART_BAUD[MAEN1] or LPUART_BAUD[MAEN2] bit is set and LPUART_BAUD[MATCFG] is equal to 01. In this function, the first character received by the LPUART_RX pin after an idle line condition is considered an address and is compared with the associated MA1 or MA2 register. The character is only transferred to the receive buffer, and LPUART_STAT[RDRF] is set, if the comparison matches. All subsequent characters are considered to be data associated with the address and are transferred to the receive data buffer until the next idle line condition is detected. If no address match occurs then no transfer is made to the receive data buffer, and all following frames until the next idle condition are also discarded. If both the LPUART_BAUD[MAEN1] and LPUART_BAUD[MAEN2] bits are negated, the receiver operates normally and all data received is transferred to the receive data buffer.

Idle match operation functions in the same way for both MA1 and MA2 registers.

- If only one of LPUART_BAUD[MAEN1] and LPUART_BAUD[MAEN2] is asserted, the first character after an idle line is compared only with the associated match register and data is transferred to the receive data buffer only on a match.
- If LPUART_BAUD[MAEN1] and LPUART_BAUD[MAEN2] are asserted, the first character after an idle line is compared with both match registers and data is transferred only on a match with either register.

59.4.3.2.6 Match On Match Off operation

Match on, match off operation is enabled when both LPUART_BAUD[MAEN1] and LPUART_BAUD[MAEN2] are set and LPUART_BAUD[MATCFG] is equal to 10. In this function, a character received by the LPUART_RX pin that matches MATCH[MA1] is received and transferred to the receive buffer, and LPUART_STAT[RDRF] is set. All subsequent characters are considered to be data and are also transferred to the receive data buffer, until a character is received that matches MATCH[MA2] register. The character that matches MATCH[MA2] and all following characters are discarded, this

continues until another character that matches MATCH[MA1] is received. If both the LPUART_BAUD[MAEN1] and LPUART_BAUD[MAEN2] bits are negated, the receiver operates normally and all data received is transferred to the receive data buffer.

NOTE

Match on, match off operation requires both LPUART_BAUD[MAEN1] and LPUART_BAUD[MAEN2] to be asserted.

59.4.3.3 Hardware flow control

To support hardware flow control, the receiver can be programmed to automatically deassert and assert LPUART_RTS.

- LPUART_RTS remains asserted until the transfer is complete, even if the transmitter is disabled midway through a data transfer. See Transceiver driver enable using LPUART_RTS for more details.
- If the receiver request-to-send functionality is enabled, the receiver automatically deasserts LPUART_RTS if the number of characters in the receiver data register is full or a start bit is detected that will cause the receiver data register to be full.
- The receiver asserts LPUART_RTS when the number of characters in the receiver data register is not full and has not detected a start bit that will cause the receiver data register to be full. It is not affected if STAT[RDRF] is asserted.
- Even if LPUART_RTS is deasserted, the receiver continues to receive characters until the receiver data buffer is overrun.
- If the receiver request-to-send functionality is disabled, the receiver LPUART_RTS remains deasserted.

59.4.3.4 Infrared decoder

The infrared decoder converts the received character from the IrDA format to the NRZ format used by the receiver. It also has a OSR oversampling baud rate clock counter that filters noise and indicates when a 1 is received.

59.4.3.4.1 Start bit detection

When STAT[RXINV] is cleared, the first falling edge of the received character corresponds to the start bit. The infrared decoder resets its counter. At this time, the receiver also begins its start bit detection process. After the start bit is detected, the

receiver synchronizes its bit times to this start bit time. For the rest of the character reception, the infrared decoder's counter and the receiver's bit time counter count independently from each other.

59.4.3.4.2 Noise filtering

Any further rising edges detected during the first half of the infrared decoder counter are ignored by the decoder. Any pulses less than one oversampling baud clock can be undetected by it regardless of whether it is seen in the first or second half of the count.

59.4.3.4.3 Low-bit detection

During the second half of the decoder count, a rising edge is decoded as a 0, which is sent to the receiver. The decoder counter is also reset.

59.4.3.4.4 High-bit detection

At OSR oversampling baud rate clocks after the previous rising edge, if a rising edge is not seen, then the decoder sends a 1 to the receiver.

If the next bit is a 0, which arrives late, then a low-bit is detected according to Low-bit detection. The value sent to the receiver is changed from 1 to a 0. Then, if a noise pulse occurs outside the receiver's bit time sampling period, then the delay of a 0 is not recorded as noise.

59.4.4 Additional LPUART functions

The following sections describe additional LPUART functions.

59.4.4.1 8-bit, 9-bit and 10-bit data modes

The LPUART transmitter and receiver can be configured to operate in 9-bit data mode by setting the LPUART_CTRL[M] or 10-bit data mode by setting LPUART_CTRL[M10]. In 9-bit mode, there is a ninth data bit in 10-bit mode there is a tenth data bit. For the transmit data buffer, these bits are stored in LPUART_CTRL[T8] and LPUART_CTRL[T9]. For the receiver, these bits are held in LPUART_CTRL[R8] and LPUART_CTRL[R9]. They are also accessible via 16-bit or 32-bit accesses to the LPUART_DATA register.

For coherent 8-bit writes to the transmit data buffer, write to LPUART_CTRL[T8] and LPUART_CTRL[T9] before writing to LPUART_DATA[7:0]. For 16-bit and 32-bit writes to the LPUART_DATA register all 10 transmit bits are written to the transmit data buffer at the same time.

If the bit values to be transmitted as the ninth and tenth bit of a new character are the same as for the previous character, it is not necessary to write to LPUART_CTRL[T8] and LPUART_CTRL[T9] again. When data is transferred from the transmit data buffer to the transmit shifter, the value in LPUART_CTRL[T8] and LPUART_CTRL[T9] is copied at the same time data is transferred from LPUART_DATA[7:0] to the shifter.

The 9-bit data mode is typically used with parity to allow eight bits of data plus the parity in the ninth bit, or it is used with address-mark wakeup so the ninth data bit can serve as the wakeup bit. The 10-bit data mode is typically used with parity and address-mark wakeup so the ninth data bit can serve as the wakeup bit and the tenth bit as the parity bit. In custom protocols, the ninth and/or tenth bits can also serve as software-controlled markers.

59.4.4.2 Idle length

An idle character is a character where the start bit, all data bits and stop bits are in the mark postion. The CTRL[ILT] register can be configured to start detecting an idle character from the previous start bit (any data bits and stop bits count towards the idle character detection) or from the previous stop bit.

The number of idle characters that must be received before an idle line condition is detected can also be configured using the CTRL[IDLECFG] field. This field configures the number of idle characters that must be received before the STAT[IDLE] flag is set, the STAT[RAF] flag is cleared and the DATA[IDLINE] flag is set with the next received character.

Idle-line wakeup and idle match operation are also affected by the CTRL[IDLECFG] field. When address match or match on/off operation is enabled, setting the STAT[RWUID] bit will cause any discarded characters to be treated as if they were idle characters.

59.4.4.3 Loop mode

When LPUART_CTRL[LOOPS] is set, the LPUART_CTRL[RSRC] bit in the same register chooses between loop mode (LPUART_CTRL[RSRC] = 0) or single-wire mode (LPUART_CTRL[RSRC] = 1). Loop mode is sometimes used to check software,

independent of connections in the external system, to help isolate system problems. In this mode, the transmitter output is internally connected to the receiver input and the LPUART_RX pin is not used by the LPUART.

59.4.4.4 Single-wire operation

When LPUART_CTRL[LOOPS] is set, the RSRC bit in the same register chooses between loop mode (LPUART_CTRL[RSRC] = 0) or single-wire mode (LPUART_CTRL[RSRC] = 1). Single-wire mode implements a half-duplex serial connection. The receiver is internally connected to the transmitter output and to the LPUART_TX pin (the LPUART_RX pin is not used).

In single-wire mode, the LPUART_CTRL[TXDIR] bit controls the direction of serial data on the LPUART_TX pin. When LPUART_CTRL[TXDIR] is cleared, the LPUART_TX pin is an input to the receiver and the transmitter is temporarily disconnected from the LPUART_TX pin so an external device can send serial data to the receiver. When LPUART_CTRL[TXDIR] is set, the LPUART_TX pin is an output driven by the transmitter, the internal loop back connection is disabled, and as a result the receiver cannot receive characters that are sent out by the transmitter.

59.4.5 Infrared interface

The LPUART provides the capability of transmitting narrow pulses to an IR LED and receiving narrow pulses and transforming them to serial bits, which are sent to the LPUART. The IrDA physical layer specification defines a half-duplex infrared communication link for exchanging data. The full standard includes data rates up to 16 Mbits/s. This design covers data rates only between 2.4 kbits/s and 115.2 kbits/s.

The LPUART has an infrared transmit encoder and receive decoder. The LPUART transmits serial bits of data that are encoded by the infrared submodule to transmit a narrow pulse for every zero bit. No pulse is transmitted for every one bit. When receiving data, the IR pulses are detected using an IR photo diode and transformed to CMOS levels by the IR receive decoder, external from the LPUART. The narrow pulses are then stretched by the infrared receive decoder to get back to a serial bit stream to be received by the UART. The polarity of transmitted pulses and expected receive pulses can be inverted so that a direct connection can be made to external IrDA transceiver modules that use active high pulses.

The infrared submodule receives its clock sources from the LPUART. One of these two clocks are selected in the infrared submodule to generate either 1/OSR, 2/OSR, 3/OSR, or 4/OSR narrow pulses during transmission.

59.4.5.1 Infrared transmit encoder

The infrared transmit encoder converts serial bits of data from transmit shift register to the LPUART_TX signal. A narrow pulse is transmitted for a zero bit and no pulse for a one bit. The narrow pulse is sent at the start of the bit with a duration of 1/OSR, 2/OSR, 3/OSR, or 4/OSR of a bit time. A narrow low pulse is transmitted for a zero bit when LPUART_CTRL[TXINV] is cleared, while a narrow high pulse is transmitted for a zero bit when LPUART_CTRL[TXINV] is set.

59.4.5.2 Infrared receive decoder

The infrared receive block converts data from the LPUART_RX signal to the receive shift register. A narrow pulse is expected for each zero received and no pulse is expected for each one received. A narrow low pulse is expected for a zero bit when LPUART_STAT[RXINV] is cleared, while a narrow high pulse is expected for a zero bit when LPUART_STAT[RXINV] is set. This receive decoder meets the edge jitter requirement as defined by the IrDA serial infrared physical layer specification.

59.4.6 Interrupts and status flags

The LPUART transmitter has two status flags that can optionally generate hardware interrupt requests. Transmit data register empty LPUART_STAT[TDRE]) indicates when there is room in the transmit data buffer to write another transmit character to LPUART_DATA. If the transmit interrupt enable LPUART_CTRL[TIE]) bit is set, a hardware interrupt is requested when LPUART_STAT[TDRE] is set. Transmit complete (LPUART_STAT[TC]) indicates that the transmitter is finished transmitting all data, preamble, and break characters and is idle with LPUART_TX at the inactive level. This flag is often used in systems with modems to determine when it is safe to turn off the modem. If the transmit complete interrupt enable (LPUART_CTRL[TCIE]) bit is set, a hardware interrupt is requested when LPUART_STAT[TC] is set. Instead of hardware interrupts, software polling may be used to monitor the LPUART_STAT[TDRE] and LPUART_STAT[TC] status flags if the corresponding LPUART_CTRL[TIE] or LPUART_CTRL[TCIE] local interrupt masks are cleared.

When a program detects that the receive data register is full (LPUART_STAT[RDRF] = 1), it gets the data from the receive data register by reading LPUART_DATA. The LPUART_STAT[RDRF] flag is cleared by reading LPUART_DATA.

The IDLE status flag includes logic that prevents it from getting set repeatedly when the LPUART_RX line remains idle for an extended period of time. IDLE is cleared by writing 1 to the LPUART_STAT[IDLE] flag. After LPUART_STAT[IDLE] has been cleared, it cannot become set again until the receiver has received at least one new character and has set LPUART_STAT[RDRF].

If the associated error was detected in the received character that caused LPUART_STAT[RDRF] to be set, the error flags - noise flag (LPUART_STAT[NF]), framing error (LPUART_STAT[FE]), and parity error flag (LPUART_STAT[PF]) - are set at the same time as LPUART_STAT[RDRF]. These flags are not set in overrun cases.

If LPUART_STAT[RDRF] was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (LPUART_STAT[OR]) flag is set instead of the data along with any associated NF, FE, or PF condition is lost.

If the received character matches the contents of MATCH[MA1] and/or MATCH[MA2] then the LPUART_STAT[MA1F] and/or LPUART_STAT[MA2F] flags are set at the same time that LPUART_STAT[RDRF] is set.

At any time, an active edge on the LPUART_RX serial data input pin causes the LPUART_STAT[RXEDGIF] flag to set. The LPUART_STAT[RXEDGIF] flag is cleared by writing a 1 to it. This function depends on the receiver being enabled (LPUART_CTRL[RE] = 1).

Chapter 60
FlexIO

60.1 Chip-specific FlexIO information

60.1.1 FlexIO Instantiation

This section summarize the features and module configurations of FlexIO

Amongst other features, the FlexIO module in this device supports:

1. Emulation in serial/parallel communication protocols
2. Programmable logic blocks allowing the implementation of digital logic functions on-chip and configurable interaction of internal and external modules

60.1.2 FlexIO Trigger options

FlexIO has a selectable trigger input source controlled by FlexIO_TIMCTLn[TRGSEL] (4-bit field) to use for starting the counter and/or reloading the counter. The options available are shown in the following table

Table 60-1. FlexIO Trigger Options

FlexIO_TIMCTLn[TRGSEL] (4-bit field)	Selected source
0000	External trigger pin input (EXTRG_IN)
0001	CMP0 output
0010	CMP1 output
0011	Reserved
0100	PIT trigger 0
0101	PIT trigger 1
0110	PIT trigger 2

Table continues on the next page...

Table 60-1. FlexIO Trigger Options (continued)

FlexIO_TIMCTLn[TRGSEL] (4-bit field)	Selected source
0111	PIT trigger 3
1000	FTM0 trigger
1001	FTM1 trigger
1010	FTM2 trigger
1011	FTM3 trigger
1100	RTC alarm
1101	RTC seconds
1110	LPTMR trigger
1111	Reserved

60.2 Introduction

60.2.1 Overview

The FlexIO is a highly configurable module providing a wide range of functionality including:

- Emulation of a variety of serial/parallel communication protocols
- Flexible 16-bit timers with support for a variety of trigger, reset, enable and disable conditions
- Programmable logic blocks allowing the implementation of digital logic functions on-chip and configurable interaction of internal and external modules
- Programmable state machine for offloading basic system control functions from CPU

These functions are provided by the FlexIO while adhering to the following key objectives:

- Low software/CPU overhead: less overhead than software bit-banging, more overhead than dedicated peripheral IP.
- Area/Power efficient implementation: more efficient than integrating multiple peripherals for each desired protocol or adding external board-level discrete logic.

60.2.2 Features

The FlexIO module is capable of supporting a wide range of protocols including, but not limited to:

- UART
- I2C
- SPI
- I2S
- Camera IF
- Motorola 68K/Intel 8080 bus
- PWM/Waveform generation

The following key features are provided:

- Array of 32-bit shift registers with transmit, receive and data match modes
- Double buffered shifter operation for continuous data transfer
- Shifter concatenation to support large transfer sizes
- Automatic start/stop bit generation
- 1, 2, 4, 8, 16 or 32 multi-bit shift widths for parallel interface support
- Interrupt, DMA or polled transmit/receive operation
- Programmable baud rates independent of bus clock frequency, with support for asynchronous operation during stop modes
- Highly flexible 16-bit timers with support for a variety of internal or external trigger, reset, enable and disable conditions
- Programmable logic mode for integrating external digital logic functions on-chip or combining pin/shifter/timer functions to generate complex outputs
- Programmable state machine for offloading basic system control functions from CPU with support for up to 8 states, 8 outputs and 3 selectable inputs per state

60.2.3 Block Diagram

The following diagram gives a high-level overview of the configuration of FlexIO timers and shifters.

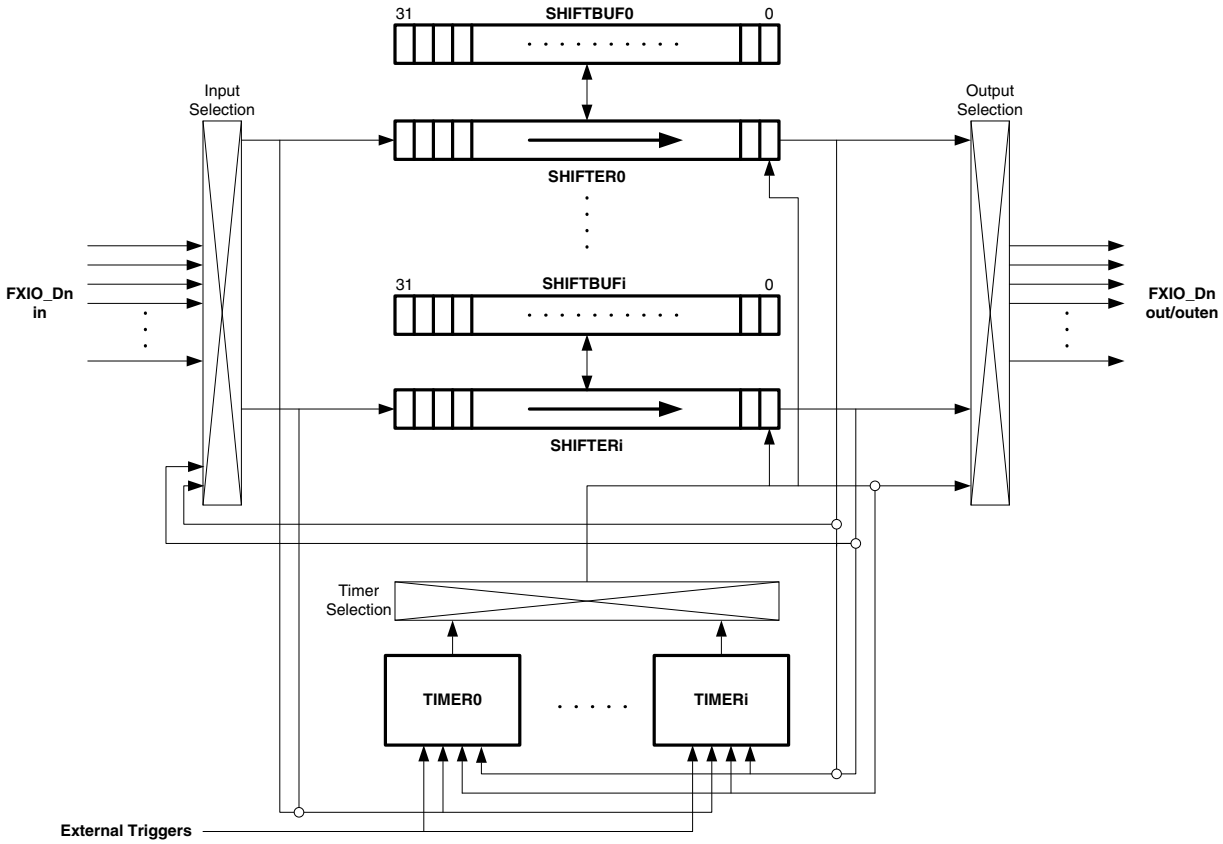


Figure 60-1. FlexIO block diagram

60.2.4 Modes of operation

The FlexIO module supports the chip modes described in the following table.

Table 60-2. Chip modes supported by the FlexIO module

Chip mode	FlexIO Operation
Run	Normal operation
Stop/Wait	Can continue operating provided the Doze Enable bit (CTRL[DOZEN]) is set and the FlexIO is using an external or internal clock source which remains operating during stop/wait modes.
Low Leakage Stop	The Doze Enable (CTRL[DOZEN]) bit is ignored and the FlexIO will wait for all Timers to complete any pending operation before acknowledging low leakage mode entry.
Debug	Can continue operating provided the Debug Enable bit (CTRL[DBGE]) is set.

60.2.5 FlexIO Signal Descriptions

Signal	Description	I/O
FXIO_Dn (n=0...31)	Bidirectional FlexIO Shifter and Timer pin inputs/outputs	I/O

60.3 Memory Map and Registers

FLEXIO memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_F000	Version ID Register (FLEXIO0_VERID)	32	R	0101_0001h	60.3.1/1966
400D_F004	Parameter Register (FLEXIO0_PARAM)	32	R	See section	60.3.2/1966
400D_F008	FlexIO Control Register (FLEXIO0_CTRL)	32	R/W	0000_0000h	60.3.3/1967
400D_F00C	Pin State Register (FLEXIO0_PIN)	32	R	0000_0000h	60.3.4/1968
400D_F010	Shifter Status Register (FLEXIO0_SHIFTSTAT)	32	w1c	0000_0000h	60.3.5/1969
400D_F014	Shifter Error Register (FLEXIO0_SHIFTERR)	32	w1c	0000_0000h	60.3.6/1969
400D_F018	Timer Status Register (FLEXIO0_TIMSTAT)	32	w1c	0000_0000h	60.3.7/1970
400D_F020	Shifter Status Interrupt Enable (FLEXIO0_SHIFTSIEN)	32	R/W	0000_0000h	60.3.8/1971
400D_F024	Shifter Error Interrupt Enable (FLEXIO0_SHIFTEIEN)	32	R/W	0000_0000h	60.3.9/1971
400D_F028	Timer Interrupt Enable Register (FLEXIO0_TIMIEN)	32	R/W	0000_0000h	60.3.10/ 1972
400D_F030	Shifter Status DMA Enable (FLEXIO0_SHIFTSDEN)	32	R/W	0000_0000h	60.3.11/ 1972
400D_F040	Shifter State Register (FLEXIO0_SHIFTSTATE)	32	R/W	0000_0000h	60.3.12/ 1973
400D_F080	Shifter Control N Register (FLEXIO0_SHIFTCTL0)	32	R/W	0000_0000h	60.3.13/ 1974
400D_F084	Shifter Control N Register (FLEXIO0_SHIFTCTL1)	32	R/W	0000_0000h	60.3.13/ 1974
400D_F088	Shifter Control N Register (FLEXIO0_SHIFTCTL2)	32	R/W	0000_0000h	60.3.13/ 1974
400D_F08C	Shifter Control N Register (FLEXIO0_SHIFTCTL3)	32	R/W	0000_0000h	60.3.13/ 1974
400D_F090	Shifter Control N Register (FLEXIO0_SHIFTCTL4)	32	R/W	0000_0000h	60.3.13/ 1974
400D_F094	Shifter Control N Register (FLEXIO0_SHIFTCTL5)	32	R/W	0000_0000h	60.3.13/ 1974
400D_F098	Shifter Control N Register (FLEXIO0_SHIFTCTL6)	32	R/W	0000_0000h	60.3.13/ 1974
400D_F09C	Shifter Control N Register (FLEXIO0_SHIFTCTL7)	32	R/W	0000_0000h	60.3.13/ 1974

Table continues on the next page...

FLEXIO memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_F100	Shifter Configuration N Register (FLEXIO0_SHIFTCFG0)	32	R/W	0000_0000h	60.3.14/ 1975
400D_F104	Shifter Configuration N Register (FLEXIO0_SHIFTCFG1)	32	R/W	0000_0000h	60.3.14/ 1975
400D_F108	Shifter Configuration N Register (FLEXIO0_SHIFTCFG2)	32	R/W	0000_0000h	60.3.14/ 1975
400D_F10C	Shifter Configuration N Register (FLEXIO0_SHIFTCFG3)	32	R/W	0000_0000h	60.3.14/ 1975
400D_F110	Shifter Configuration N Register (FLEXIO0_SHIFTCFG4)	32	R/W	0000_0000h	60.3.14/ 1975
400D_F114	Shifter Configuration N Register (FLEXIO0_SHIFTCFG5)	32	R/W	0000_0000h	60.3.14/ 1975
400D_F118	Shifter Configuration N Register (FLEXIO0_SHIFTCFG6)	32	R/W	0000_0000h	60.3.14/ 1975
400D_F11C	Shifter Configuration N Register (FLEXIO0_SHIFTCFG7)	32	R/W	0000_0000h	60.3.14/ 1975
400D_F200	Shifter Buffer N Register (FLEXIO0_SHIFTBUF0)	32	R/W	0000_0000h	60.3.15/ 1977
400D_F204	Shifter Buffer N Register (FLEXIO0_SHIFTBUF1)	32	R/W	0000_0000h	60.3.15/ 1977
400D_F208	Shifter Buffer N Register (FLEXIO0_SHIFTBUF2)	32	R/W	0000_0000h	60.3.15/ 1977
400D_F20C	Shifter Buffer N Register (FLEXIO0_SHIFTBUF3)	32	R/W	0000_0000h	60.3.15/ 1977
400D_F210	Shifter Buffer N Register (FLEXIO0_SHIFTBUF4)	32	R/W	0000_0000h	60.3.15/ 1977
400D_F214	Shifter Buffer N Register (FLEXIO0_SHIFTBUF5)	32	R/W	0000_0000h	60.3.15/ 1977
400D_F218	Shifter Buffer N Register (FLEXIO0_SHIFTBUF6)	32	R/W	0000_0000h	60.3.15/ 1977
400D_F21C	Shifter Buffer N Register (FLEXIO0_SHIFTBUF7)	32	R/W	0000_0000h	60.3.15/ 1977
400D_F280	Shifter Buffer N Bit Swapped Register (FLEXIO0_SHIFTBUFBIS0)	32	R/W	0000_0000h	60.3.16/ 1977
400D_F284	Shifter Buffer N Bit Swapped Register (FLEXIO0_SHIFTBUFBIS1)	32	R/W	0000_0000h	60.3.16/ 1977
400D_F288	Shifter Buffer N Bit Swapped Register (FLEXIO0_SHIFTBUFBIS2)	32	R/W	0000_0000h	60.3.16/ 1977
400D_F28C	Shifter Buffer N Bit Swapped Register (FLEXIO0_SHIFTBUFBIS3)	32	R/W	0000_0000h	60.3.16/ 1977
400D_F290	Shifter Buffer N Bit Swapped Register (FLEXIO0_SHIFTBUFBIS4)	32	R/W	0000_0000h	60.3.16/ 1977
400D_F294	Shifter Buffer N Bit Swapped Register (FLEXIO0_SHIFTBUFBIS5)	32	R/W	0000_0000h	60.3.16/ 1977

Table continues on the next page...

FLEXIO memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_F298	Shifter Buffer N Bit Swapped Register (FLEXIO0_SHIFTBUFBIS6)	32	R/W	0000_0000h	60.3.16/ 1977
400D_F29C	Shifter Buffer N Bit Swapped Register (FLEXIO0_SHIFTBUFBIS7)	32	R/W	0000_0000h	60.3.16/ 1977
400D_F300	Shifter Buffer N Byte Swapped Register (FLEXIO0_SHIFTBUFBYS0)	32	R/W	0000_0000h	60.3.17/ 1978
400D_F304	Shifter Buffer N Byte Swapped Register (FLEXIO0_SHIFTBUFBYS1)	32	R/W	0000_0000h	60.3.17/ 1978
400D_F308	Shifter Buffer N Byte Swapped Register (FLEXIO0_SHIFTBUFBYS2)	32	R/W	0000_0000h	60.3.17/ 1978
400D_F30C	Shifter Buffer N Byte Swapped Register (FLEXIO0_SHIFTBUFBYS3)	32	R/W	0000_0000h	60.3.17/ 1978
400D_F310	Shifter Buffer N Byte Swapped Register (FLEXIO0_SHIFTBUFBYS4)	32	R/W	0000_0000h	60.3.17/ 1978
400D_F314	Shifter Buffer N Byte Swapped Register (FLEXIO0_SHIFTBUFBYS5)	32	R/W	0000_0000h	60.3.17/ 1978
400D_F318	Shifter Buffer N Byte Swapped Register (FLEXIO0_SHIFTBUFBYS6)	32	R/W	0000_0000h	60.3.17/ 1978
400D_F31C	Shifter Buffer N Byte Swapped Register (FLEXIO0_SHIFTBUFBYS7)	32	R/W	0000_0000h	60.3.17/ 1978
400D_F380	Shifter Buffer N Bit Byte Swapped Register (FLEXIO0_SHIFTBUFBBS0)	32	R/W	0000_0000h	60.3.18/ 1978
400D_F384	Shifter Buffer N Bit Byte Swapped Register (FLEXIO0_SHIFTBUFBBS1)	32	R/W	0000_0000h	60.3.18/ 1978
400D_F388	Shifter Buffer N Bit Byte Swapped Register (FLEXIO0_SHIFTBUFBBS2)	32	R/W	0000_0000h	60.3.18/ 1978
400D_F38C	Shifter Buffer N Bit Byte Swapped Register (FLEXIO0_SHIFTBUFBBS3)	32	R/W	0000_0000h	60.3.18/ 1978
400D_F390	Shifter Buffer N Bit Byte Swapped Register (FLEXIO0_SHIFTBUFBBS4)	32	R/W	0000_0000h	60.3.18/ 1978
400D_F394	Shifter Buffer N Bit Byte Swapped Register (FLEXIO0_SHIFTBUFBBS5)	32	R/W	0000_0000h	60.3.18/ 1978
400D_F398	Shifter Buffer N Bit Byte Swapped Register (FLEXIO0_SHIFTBUFBBS6)	32	R/W	0000_0000h	60.3.18/ 1978
400D_F39C	Shifter Buffer N Bit Byte Swapped Register (FLEXIO0_SHIFTBUFBBS7)	32	R/W	0000_0000h	60.3.18/ 1978
400D_F400	Timer Control N Register (FLEXIO0_TIMCTL0)	32	R/W	0000_0000h	60.3.19/ 1979
400D_F404	Timer Control N Register (FLEXIO0_TIMCTL1)	32	R/W	0000_0000h	60.3.19/ 1979
400D_F408	Timer Control N Register (FLEXIO0_TIMCTL2)	32	R/W	0000_0000h	60.3.19/ 1979
400D_F40C	Timer Control N Register (FLEXIO0_TIMCTL3)	32	R/W	0000_0000h	60.3.19/ 1979

Table continues on the next page...

FLEXIO memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_F410	Timer Control N Register (FLEXIO0_TIMCTL4)	32	R/W	0000_0000h	60.3.19/ 1979
400D_F414	Timer Control N Register (FLEXIO0_TIMCTL5)	32	R/W	0000_0000h	60.3.19/ 1979
400D_F418	Timer Control N Register (FLEXIO0_TIMCTL6)	32	R/W	0000_0000h	60.3.19/ 1979
400D_F41C	Timer Control N Register (FLEXIO0_TIMCTL7)	32	R/W	0000_0000h	60.3.19/ 1979
400D_F480	Timer Configuration N Register (FLEXIO0_TIMCFG0)	32	R/W	0000_0000h	60.3.20/ 1981
400D_F484	Timer Configuration N Register (FLEXIO0_TIMCFG1)	32	R/W	0000_0000h	60.3.20/ 1981
400D_F488	Timer Configuration N Register (FLEXIO0_TIMCFG2)	32	R/W	0000_0000h	60.3.20/ 1981
400D_F48C	Timer Configuration N Register (FLEXIO0_TIMCFG3)	32	R/W	0000_0000h	60.3.20/ 1981
400D_F490	Timer Configuration N Register (FLEXIO0_TIMCFG4)	32	R/W	0000_0000h	60.3.20/ 1981
400D_F494	Timer Configuration N Register (FLEXIO0_TIMCFG5)	32	R/W	0000_0000h	60.3.20/ 1981
400D_F498	Timer Configuration N Register (FLEXIO0_TIMCFG6)	32	R/W	0000_0000h	60.3.20/ 1981
400D_F49C	Timer Configuration N Register (FLEXIO0_TIMCFG7)	32	R/W	0000_0000h	60.3.20/ 1981
400D_F500	Timer Compare N Register (FLEXIO0_TIMCMP0)	32	R/W	0000_0000h	60.3.21/ 1983
400D_F504	Timer Compare N Register (FLEXIO0_TIMCMP1)	32	R/W	0000_0000h	60.3.21/ 1983
400D_F508	Timer Compare N Register (FLEXIO0_TIMCMP2)	32	R/W	0000_0000h	60.3.21/ 1983
400D_F50C	Timer Compare N Register (FLEXIO0_TIMCMP3)	32	R/W	0000_0000h	60.3.21/ 1983
400D_F510	Timer Compare N Register (FLEXIO0_TIMCMP4)	32	R/W	0000_0000h	60.3.21/ 1983
400D_F514	Timer Compare N Register (FLEXIO0_TIMCMP5)	32	R/W	0000_0000h	60.3.21/ 1983
400D_F518	Timer Compare N Register (FLEXIO0_TIMCMP6)	32	R/W	0000_0000h	60.3.21/ 1983
400D_F51C	Timer Compare N Register (FLEXIO0_TIMCMP7)	32	R/W	0000_0000h	60.3.21/ 1983
400D_F680	Shifter Buffer N Nibble Byte Swapped Register (FLEXIO0_SHIFTBUFNBS0)	32	R/W	0000_0000h	60.3.22/ 1984
400D_F684	Shifter Buffer N Nibble Byte Swapped Register (FLEXIO0_SHIFTBUFNBS1)	32	R/W	0000_0000h	60.3.22/ 1984

Table continues on the next page...

FLEXIO memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400D_F688	Shifter Buffer N Nibble Byte Swapped Register (FLEXIO0_SHIFTBUFNBS2)	32	R/W	0000_0000h	60.3.22/ 1984
400D_F68C	Shifter Buffer N Nibble Byte Swapped Register (FLEXIO0_SHIFTBUFNBS3)	32	R/W	0000_0000h	60.3.22/ 1984
400D_F690	Shifter Buffer N Nibble Byte Swapped Register (FLEXIO0_SHIFTBUFNBS4)	32	R/W	0000_0000h	60.3.22/ 1984
400D_F694	Shifter Buffer N Nibble Byte Swapped Register (FLEXIO0_SHIFTBUFNBS5)	32	R/W	0000_0000h	60.3.22/ 1984
400D_F698	Shifter Buffer N Nibble Byte Swapped Register (FLEXIO0_SHIFTBUFNBS6)	32	R/W	0000_0000h	60.3.22/ 1984
400D_F69C	Shifter Buffer N Nibble Byte Swapped Register (FLEXIO0_SHIFTBUFNBS7)	32	R/W	0000_0000h	60.3.22/ 1984
400D_F700	Shifter Buffer N Half Word Swapped Register (FLEXIO0_SHIFTBUFHWS0)	32	R/W	0000_0000h	60.3.23/ 1984
400D_F704	Shifter Buffer N Half Word Swapped Register (FLEXIO0_SHIFTBUFHWS1)	32	R/W	0000_0000h	60.3.23/ 1984
400D_F708	Shifter Buffer N Half Word Swapped Register (FLEXIO0_SHIFTBUFHWS2)	32	R/W	0000_0000h	60.3.23/ 1984
400D_F70C	Shifter Buffer N Half Word Swapped Register (FLEXIO0_SHIFTBUFHWS3)	32	R/W	0000_0000h	60.3.23/ 1984
400D_F710	Shifter Buffer N Half Word Swapped Register (FLEXIO0_SHIFTBUFHWS4)	32	R/W	0000_0000h	60.3.23/ 1984
400D_F714	Shifter Buffer N Half Word Swapped Register (FLEXIO0_SHIFTBUFHWS5)	32	R/W	0000_0000h	60.3.23/ 1984
400D_F718	Shifter Buffer N Half Word Swapped Register (FLEXIO0_SHIFTBUFHWS6)	32	R/W	0000_0000h	60.3.23/ 1984
400D_F71C	Shifter Buffer N Half Word Swapped Register (FLEXIO0_SHIFTBUFHWS7)	32	R/W	0000_0000h	60.3.23/ 1984
400D_F780	Shifter Buffer N Nibble Swapped Register (FLEXIO0_SHIFTBUFNIS0)	32	R/W	0000_0000h	60.3.24/ 1985
400D_F784	Shifter Buffer N Nibble Swapped Register (FLEXIO0_SHIFTBUFNIS1)	32	R/W	0000_0000h	60.3.24/ 1985
400D_F788	Shifter Buffer N Nibble Swapped Register (FLEXIO0_SHIFTBUFNIS2)	32	R/W	0000_0000h	60.3.24/ 1985
400D_F78C	Shifter Buffer N Nibble Swapped Register (FLEXIO0_SHIFTBUFNIS3)	32	R/W	0000_0000h	60.3.24/ 1985
400D_F790	Shifter Buffer N Nibble Swapped Register (FLEXIO0_SHIFTBUFNIS4)	32	R/W	0000_0000h	60.3.24/ 1985
400D_F794	Shifter Buffer N Nibble Swapped Register (FLEXIO0_SHIFTBUFNIS5)	32	R/W	0000_0000h	60.3.24/ 1985
400D_F798	Shifter Buffer N Nibble Swapped Register (FLEXIO0_SHIFTBUFNIS6)	32	R/W	0000_0000h	60.3.24/ 1985
400D_F79C	Shifter Buffer N Nibble Swapped Register (FLEXIO0_SHIFTBUFNIS7)	32	R/W	0000_0000h	60.3.24/ 1985

60.3.1 Version ID Register (FLEXIOx_VERID)

.

Address: 400D_F000h base + 0h offset = 400D_F000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MAJOR								MINOR								FEATURE															
W																																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

FLEXIOx_VERID field descriptions

Field	Description
31–24 MAJOR	Major Version Number This read only field returns the major version number for the module specification.
23–16 MINOR	Minor Version Number This read only field returns the minor version number for the module specification.
FEATURE	Feature Specification Number This read only field returns the feature set number. 0x0000 Standard features implemented. 0x0001 Supports state, logic and parallel modes.

60.3.2 Parameter Register (FLEXIOx_PARAM)

.

Address: 400D_F000h base + 4h offset = 400D_F004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	TRIGGER								PIN								TIMER								SHIFTER							
W																																
Reset	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FLEXIOx_PARAM field descriptions

Field	Description
31–24 TRIGGER	Trigger Number Number of external triggers implemented.
23–16 PIN	Pin Number Number of Pins implemented.

Table continues on the next page...

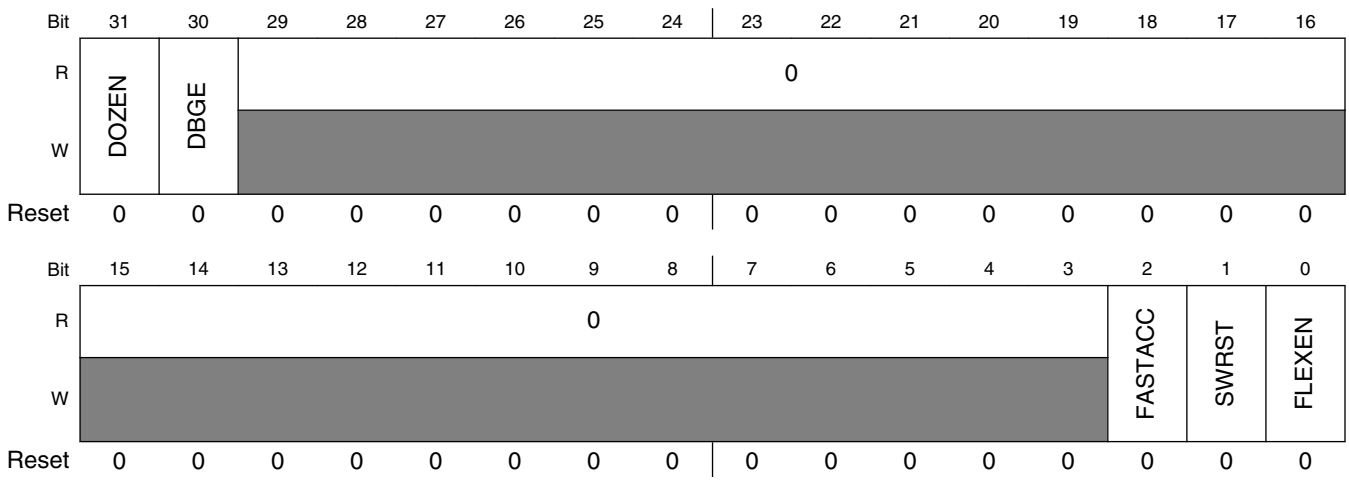
FLEXIOx_PARAM field descriptions (continued)

Field	Description
15–8 TIMER	Timer Number Number of Timers implemented.
SHIFTER	Shifter Number Number of Shifters implemented.

60.3.3 FlexIO Control Register (FLEXIOx_CTRL)

.

Address: 400D_F000h base + 8h offset = 400D_F008h



FLEXIOx_CTRL field descriptions

Field	Description
31 DOZEN	Doze Enable Disables FlexIO operation in Doze modes. This field is ignored and the FlexIO always disabled in low-leakage stop modes. 0 FlexIO enabled in Doze modes. 1 FlexIO disabled in Doze modes.
30 DBGE	Debug Enable Enables FlexIO operation in Debug mode. 0 FlexIO is disabled in debug modes. 1 FlexIO is enabled in debug modes
29–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

FLEXIOx_CTRL field descriptions (continued)

Field	Description
2 FASTACC	Fast Access Enables fast register accesses to FlexIO registers, but requires the FlexIO clock to be at least twice the frequency of the bus clock. 0 Configures for normal register accesses to FlexIO 1 Configures for fast register accesses to FlexIO
1 SWRST	Software Reset The FlexIO Control Register is not affected by the software reset, all other logic in the FlexIO is affected by the software reset and register accesses are ignored until this bit is cleared. This register bit will remain set until cleared by software, and the reset has cleared in the FlexIO clock domain. 0 Software reset is disabled 1 Software reset is enabled, all FlexIO registers except the Control Register are reset.
0 FLEXEN	FlexIO Enable 0 FlexIO module is disabled. 1 FlexIO module is enabled.

60.3.4 Pin State Register (FLEXIOx_PIN)

Address: 400D_F000h base + Ch offset = 400D_F00Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PDI																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_PIN field descriptions

Field	Description
PDI	Pin Data Input Returns the input data on each of the FlexIO pins.

60.3.5 Shifter Status Register (FLEXIOx_SHIFTSTAT)

.

Address: 400D_F000h base + 10h offset = 400D_F010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																								SSF							
W																									w1c							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_SHIFTSTAT field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
SSF	Shifter Status Flag The shifter status flag is updated when one of the following events occurs: For SMOD=Receive, the status flag is set when SHIFTBUF has been loaded with data from Shifter (SHIFTBUF is full), and the status flag is cleared when SHIFTBUF register is read. For SMOD=Transmit, the status flag is set when SHIFTBUF data has been transferred to the Shifter (SHIFTBUF is empty) or when initially configured for SMOD=Transmit, and the status flag is cleared when the SHIFTBUF register is written. For SMOD=Match Store, the status flag is set when a match has occured between SHIFTBUF and Shifter, and the status flag is cleared when the SHIFTBUF register is read. For SMOD=Match Continuous, returns the current match result between the SHIFTBUF and Shifter. For SMOD=State, the status flag for a shifter will set when it is selected by the current state pointer. For SMOD=Logic, returns the current value of the programmable logic block output. The status flag can also be cleared by writing a logic one to the flag for all modes except Match Continuous/State/Logic. 0 Status flag is clear 1 Status flag is set

60.3.6 Shifter Error Register (FLEXIOx_SHIFTERR)

.

Address: 400D_F000h base + 14h offset = 400D_F014h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																								SEF							
W																									w1c							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_SHIFTERR field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
SEF	Shifter Error Flags The shifter error flag is set when one of the following events occurs: For SMOD=Receive, indicates Shifter was ready to store new data into SHIFTBUF before the previous data was read from SHIFTBUF (SHIFTBUF Overrun), or indicates that the received start or stop bit does not match the expected value. For SMOD=Transmit, indicates Shifter was ready to load new data from SHIFTBUF before new data had been written into SHIFTBUF (SHIFTBUF Underrun). For SMOD=Match Store, indicates a match event occured before the previous match data was read from SHIFTBUF (SHIFTBUF Overrun). For SMOD=Match Continuous, the error flag is set when a match has occured between SHIFTBUF and Shifter. For SMOD=Logic, the error flag is set when the output of the programmable logic block has asserted. Can be cleared by writing logic one to the flag. For SMOD=Match Continuous, can also be cleared when the SHIFTBUF register is read. 0 Shifter Error Flag is clear 1 Shifter Error Flag is set

60.3.7 Timer Status Register (FLEXIOx_TIMSTAT)

.

Address: 400D_F000h base + 18h offset = 400D_F018h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																								TSF							
W																									w1c							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_TIMSTAT field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
TSF	Timer Status Flags The timer status flag sets depending on the timer mode, and can be cleared by writing logic one to the flag. In 8-bit counter mode, the timer status flag is set when the upper 8-bit counter equals zero and decrements, this also causes the counter to reload with the value in the compare register. In 8-bit PWM mode, the timer status flag is set when the upper 8-bit counter equals zero and decrements, this also causes the counter to reload with the value in the compare register..

Table continues on the next page...

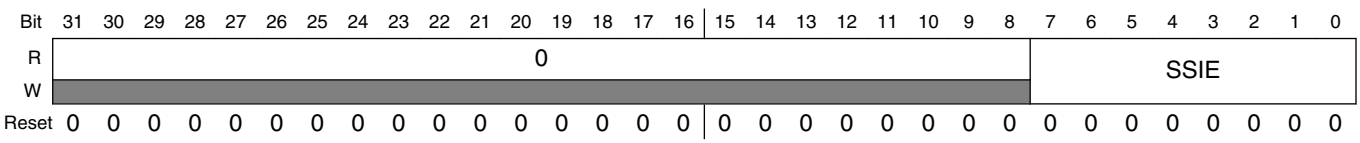
FLEXIOx_TIMSTAT field descriptions (continued)

Field	Description
	In 16-bit counter mode, the timer status flag is set when the 16-bit counter equals zero and decrements, this also causes the counter to reload with the value in the compare register.. 0 Timer Status Flag is clear 1 Timer Status Flag is set

60.3.8 Shifter Status Interrupt Enable (FLEXIOx_SHIFTSIEN)

.

Address: 400D_F000h base + 20h offset = 400D_F020h



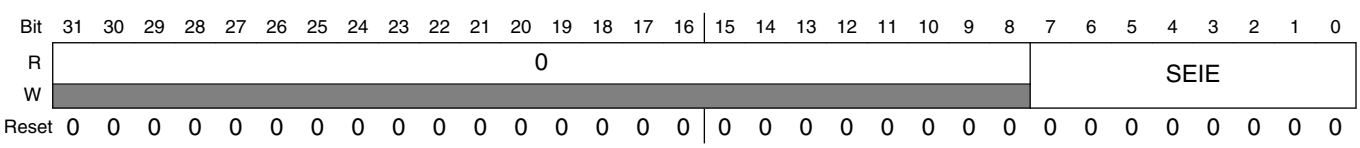
FLEXIOx_SHIFTSIEN field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
SSIE	Shifter Status Interrupt Enable Enables interrupt generation when corresponding SSF is set. 0 Shifter Status Flag interrupt disabled 1 Shifter Status Flag interrupt enabled

60.3.9 Shifter Error Interrupt Enable (FLEXIOx_SHIFTEIEN)

.

Address: 400D_F000h base + 24h offset = 400D_F024h



FLEXIOx_SHIFTEIEN field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

FLEXIOx_SHIFTEIEN field descriptions (continued)

Field	Description
SEIE	Shifter Error Interrupt Enable Enables interrupt generation when corresponding SEF is set. 0 Shifter Error Flag interrupt disabled 1 Shifter Error Flag interrupt enabled

60.3.10 Timer Interrupt Enable Register (FLEXIOx_TIMIEN)

.

Address: 400D_F000h base + 28h offset = 400D_F028h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																								TEIE							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_TIMIEN field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
TEIE	Timer Status Interrupt Enable Enables interrupt generation when corresponding TSF is set. 0 Timer Status Flag interrupt is disabled 1 Timer Status Flag interrupt is enabled

60.3.11 Shifter Status DMA Enable (FLEXIOx_SHIFTSDEN)

.

Address: 400D_F000h base + 30h offset = 400D_F030h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																								SSDE							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_SHIFTSDEN field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
SSDE	Shifter Status DMA Enable Enables DMA request generation when corresponding SSF is set. 0 Shifter Status Flag DMA request is disabled 1 Shifter Status Flag DMA request is enabled

60.3.12 Shifter State Register (FLEXIOx_SHIFTSTATE)

.

Address: 400D_F000h base + 40h offset = 400D_F040h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																													STATE		
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_SHIFTSTATE field descriptions

Field	Description
31–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
STATE	Current State Pointer The current state field maintains a pointer to keep track of the current Shifter (configured for State mode) enabled to drive outputs and compute the next state. See 'State Mode' section for more detail.

60.3.13 Shifter Control N Register (FLEXIO*x*_SHIFTCTL*n*)

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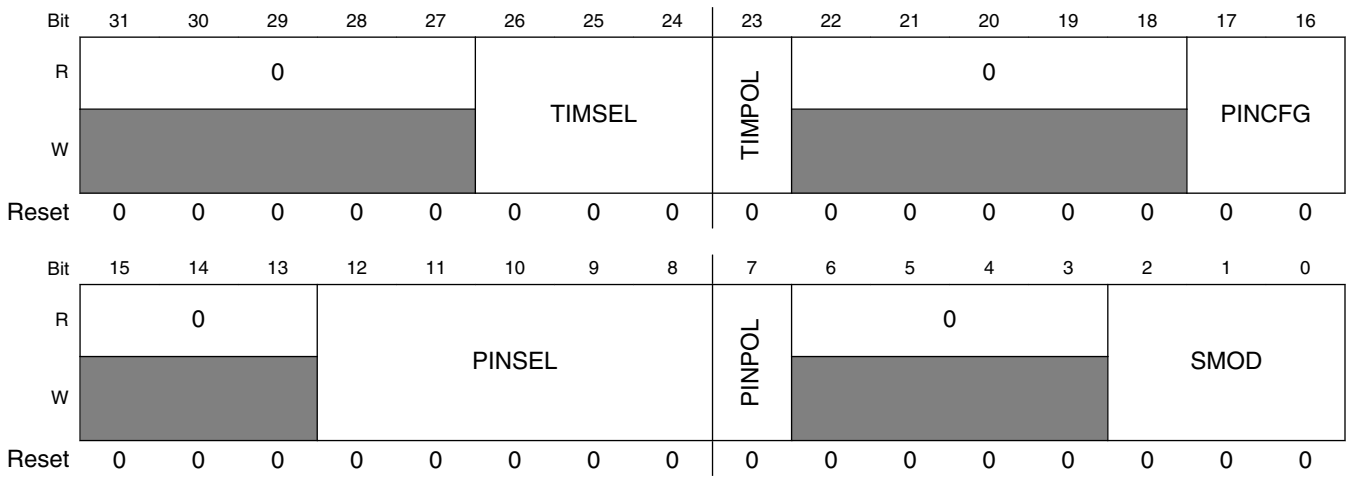
Address: 400D_F000h base + 80h offset + (4d × i), where i=0d to 7d



FLEXIO*x*_SHIFTCTL*n* field descriptions

Field	Description
31–27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26–24 TIMSEL	Timer Select Selects which Timer is used for controlling the logic/shift register and generating the Shift clock.
23 TIMPOL	Timer Polarity 0 Shift on posedge of Shift clock 1 Shift on negedge of Shift clock
22–18 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
17–16 PINCFG	Shifter Pin Configuration 00 Shifter pin output disabled 01 Shifter pin open drain or bidirectional output enable 10 Shifter pin bidirectional output data 11 Shifter pin output
15–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12–8 PINSEL	Shifter Pin Select Selects which pin is used by the Shifter input or output.
7 PINPOL	Shifter Pin Polarity 0 Pin is active high 1 Pin is active low

Table continues on the next page...

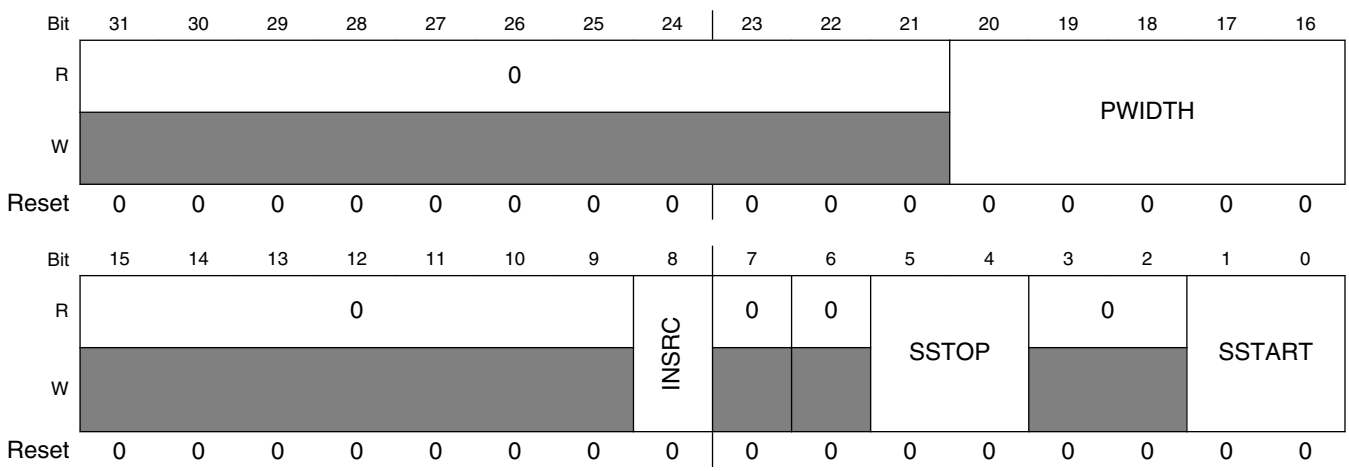
FLEXIOx_SHIFTCTL*n* field descriptions (continued)

Field	Description
6–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
SMOD	Shifter Mode Configures the mode of the Shifter. 000 Disabled. 001 Receive mode. Captures the current Shifter content into the SHIFTBUF on expiration of the Timer. 010 Transmit mode. Load SHIFTBUF contents into the Shifter on expiration of the Timer. 011 Reserved. 100 Match Store mode. Shifter data is compared to SHIFTBUF content on expiration of the Timer. 101 Match Continuous mode. Shifter data is continuously compared to SHIFTBUF contents. 110 State mode. SHIFTBUF contents are used for storing programmable state attributes. 111 Logic mode. SHIFTBUF contents are used for implementing programmable logic look up table.

60.3.14 Shifter Configuration N Register (FLEXIOx_SHIFTCFG*n*)

.

Address: 400D_F000h base + 100h offset + (4d × i), where i=0d to 7d



FLEXIOx_SHIFTCFG*n* field descriptions

Field	Description
31–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20–16 PWIDTH	Parallel Width For all Shifters, this register field configures the number of bits to be shifted on each Shift clock as follows: 1-bit shift for PWIDTH=0 4-bit shift for PWIDTH=1...3

Table continues on the next page...

FLEXIOx_SHIFTCFG*n* field descriptions (continued)

Field	Description
	8-bit shift for PWIDTH=4...7 16-bit shift for PWIDTH=8...15 32-bit shift for PWIDTH=16...31 For Shifters which support parallel transmit (SHIFTER0, SHIFTER4) or parallel receive (SHIFTER3, SHIFTER7), this register field, together with PSEL, also selects the pins to be driven or sampled on each Shift clock as follows: FXIO_D[PSEL+PWIDTH]:FXIO_D[PSEL] For SMOD=State, this field is used to disable state outputs. See 'State Mode' section for more detail.
15–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 INSRC	Input Source Selects the input source for the shifter. 0 Pin 1 Shifter N+1 Output
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5–4 SSTOP	Shifter Stop bit For SMOD=Transmit, this field allows automatic stop bit insertion if the selected timer has also enabled a stop bit. For SMOD=Receive or Match Store, this field allows automatic stop bit checking if the selected timer has also enabled a stop bit. For SMOD=State, this field is used to disable state outputs. See 'State Mode' section for more detail. For SMOD=Logic, this field is used to mask logic pin inputs. See 'Logic Mode' section for more detail. 00 Stop bit disabled for transmitter/receiver/match store 01 Reserved for transmitter/receiver/match store 10 Transmitter outputs stop bit value 0 on store, receiver/match store sets error flag if stop bit is not 0 11 Transmitter outputs stop bit value 1 on store, receiver/match store sets error flag if stop bit is not 1
3–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
SSTART	Shifter Start bit For SMOD=Transmit, this field allows automatic start bit insertion if the selected timer has also enabled a start bit. For SMOD=Receive or Match Store, this field allows automatic start bit checking if the selected timer has also enabled a start bit. For SMOD=State, this field is used to disable state outputs. See 'State Mode' section for more detail. For SMOD=Logic, this field is used to mask logic pin inputs. See 'Logic Mode' section for more detail. 00 Start bit disabled for transmitter/receiver/match store, transmitter loads data on enable 01 Start bit disabled for transmitter/receiver/match store, transmitter loads data on first shift

Table continues on the next page...

FLEXIOx_SHIFTCFG*n* field descriptions (continued)

Field	Description
	10 Transmitter outputs start bit value 0 before loading data on first shift, receiver/match store sets error flag if start bit is not 0 11 Transmitter outputs start bit value 1 before loading data on first shift, receiver/match store sets error flag if start bit is not 1

60.3.15 Shifter Buffer N Register (FLEXIOx_SHIFTBUF*n*)

.

Address: 400D_F000h base + 200h offset + (4d × i), where i=0d to 7d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	SHIFTBUF																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_SHIFTBUF*n* field descriptions

Field	Description
SHIFTBUF	Shift Buffer Shift buffer data is used for a variety of functions depending on the SMOD setting: For SMOD=Receive, Shifter data is transferred into SHIFTBUF at the expiration of Timer. For SMOD=Transmit, SHIFTBUF data is transferred into the Shifter before the Timer begins. For SMOD=Match Store/Continuous, SHIFTBUF[31:16] contains the data to be matched with the Shifter contents. The Match is checked either continuosly (Match Continous mode) or when the Timer expires (Match Store mode). SHIFTBUF[15:0] can be used to mask the match result (1=mask, 0=no mask). In Match Store mode, Shifter data [31:16] is written to SHIFTBUF[31:16] whenever a match event occurs. For SMOD=Logic, SHIFTBUF[31:0] is used to implement a 5-input, 32-bit programmable logic look-up table. See 'Logic Mode' section for more detail. For SMOD=State, SHIFTBUF[31:24] is used to drive the output value when this shifter is selected by the current state pointer and SHIFTBUF[23:0] is used to configure the value of the next state transition. See 'State Mode' section for more detail.

60.3.16 Shifter Buffer N Bit Swapped Register (FLEXIOx_SHIFTBUFBIS*n*)

.

Address: 400D_F000h base + 280h offset + (4d × i), where i=0d to 7d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	SHIFTBUFBIS																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_SHIFTBUFBISn field descriptions

Field	Description
SHIFTBUFBIS	Shift Buffer Alias to SHIFTBUF register, except reads/writes to this register are bit swapped. Reads return SHIFTBUF[0:31].

60.3.17 Shifter Buffer N Byte Swapped Register (FLEXIOx_SHIFTBUFBYSn)

.

Address: 400D_F000h base + 300h offset + (4d × i), where i=0d to 7d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	SHIFTBUFBYS																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_SHIFTBUFBYSn field descriptions

Field	Description
SHIFTBUFBYS	Shift Buffer Alias to SHIFTBUF register, except reads/writes to this register are byte swapped. Reads return { SHIFTBUF[7:0], SHIFTBUF[15:8], SHIFTBUF[23:16], SHIFTBUF[31:24] }.

60.3.18 Shifter Buffer N Bit Byte Swapped Register (FLEXIOx_SHIFTBUFBBSn)

.

Address: 400D_F000h base + 380h offset + (4d × i), where i=0d to 7d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	SHIFTBUFBBS																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

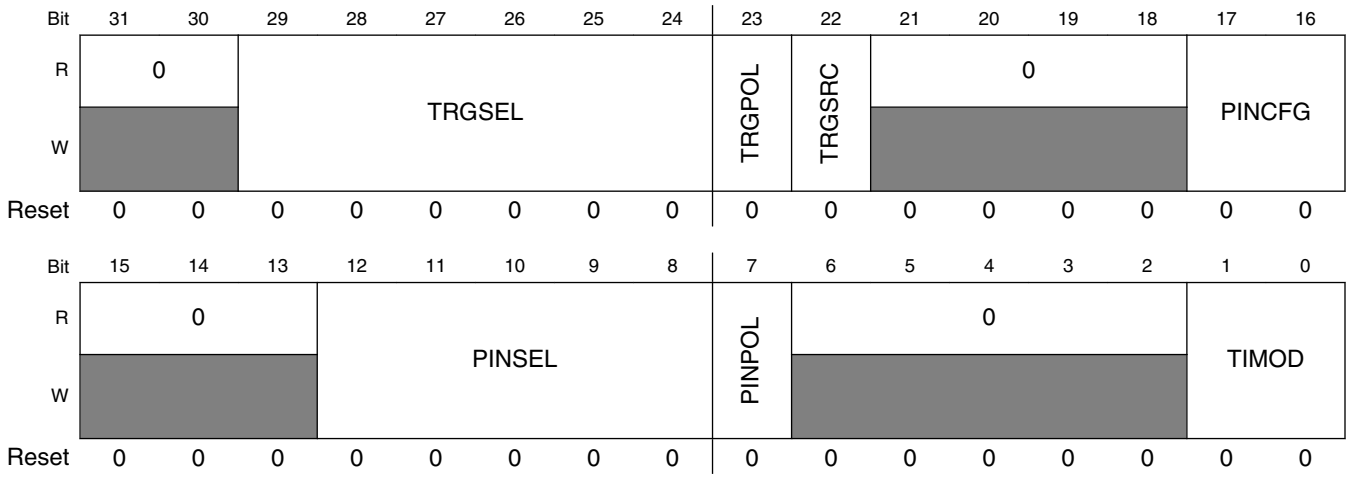
FLEXIOx_SHIFTBUFBBSn field descriptions

Field	Description
SHIFTBUFBBS	Shift Buffer Alias to SHIFTBUF register, except reads/writes to this register are bit swapped within each byte. Reads return { SHIFTBUF[24:31], SHIFTBUF[16:23], SHIFTBUF[8:15], SHIFTBUF[0:7] }.

60.3.19 Timer Control N Register (FLEXIOx_TIMCTL*n*)

.

Address: 400D_F000h base + 400h offset + (4d × i), where i=0d to 7d



FLEXIOx_TIMCTL*n* field descriptions

Field	Description
31–30 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
29–24 TRGSEL	Trigger Select The valid values for TRGSEL will depend on the FLEXIO_PARAM register. • When TRGSRC = 1, the valid values for N will depend on PIN, TIMER, SHIFTER fields in the FLEXIO_PARAM register. • When TRGSRC = 0, the valid values for N will depend on TRIGGER field in FLEXIO_PARAM register. Refer to the chip configuration section for external trigger selection. The internal trigger selection is configured as follows: {N,00} pin 2N input {N,01} shifter N status flag {N,10} pin 2N+1 input {N,11} timer N trigger output
23 TRGPOL	Trigger Polarity 0 Trigger active high 1 Trigger active low
22 TRGSRC	Trigger Source 0 External trigger selected 1 Internal trigger selected
21–18 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

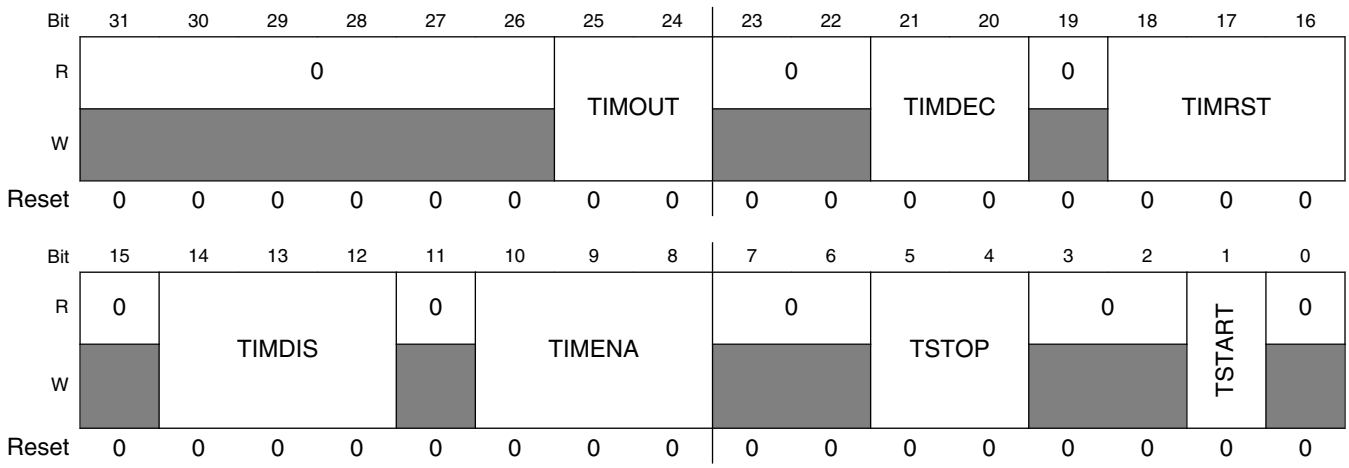
FLEXIOx_TIMCTL*n* field descriptions (continued)

Field	Description
17–16 PINCFG	Timer Pin Configuration 00 Timer pin output disabled 01 Timer pin open drain or bidirectional output enable 10 Timer pin bidirectional output data 11 Timer pin output
15–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12–8 PINSEL	Timer Pin Select Selects which pin is used by the Timer input or output.
7 PINPOL	Timer Pin Polarity 0 Pin is active high 1 Pin is active low
6–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
TIMOD	Timer Mode In 8-bit counter mode, the lower 8-bits of the counter and compare register are used to configure the baud rate of the timer shift clock and the upper 8-bits are used to configure the shifter bit count. In 8-bit PWM mode, the lower 8-bits of the counter and compare register are used to configure the high period of the timer shift clock and the upper 8-bits are used to configure the low period of the timer shift clock. The shifter bit count is configured using another timer or external signal. In 16-bit counter mode, the full 16-bits of the counter and compare register are used to configure either the baud rate of the shift clock or the shifter bit count. 00 Timer Disabled. 01 Dual 8-bit counters baud/bit mode. 10 Dual 8-bit counters PWM mode. 11 Single 16-bit counter mode.

60.3.20 Timer Configuration N Register (FLEXIOx_TIMCFG*n*)

The options to enable or disable the timer using the Timer N-1 enable or disable are reserved when N is evenly divisible by 4 (eg: Timer 0).

Address: 400D_F000h base + 480h offset + (4d × i), where i=0d to 7d



FLEXIOx_TIMCFG*n* field descriptions

Field	Description
31–26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25–24 TIMOUT	Timer Output Configures the initial state of the Timer Output and whether it is affected by the Timer reset. 00 Timer output is logic one when enabled and is not affected by timer reset 01 Timer output is logic zero when enabled and is not affected by timer reset 10 Timer output is logic one when enabled and on timer reset 11 Timer output is logic zero when enabled and on timer reset
23–22 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
21–20 TIMDEC	Timer Decrement Configures the source of the Timer decrement and the source of the Shift clock. 00 Decrement counter on FlexIO clock, Shift clock equals Timer output. 01 Decrement counter on Trigger input (both edges), Shift clock equals Timer output. 10 Decrement counter on Pin input (both edges), Shift clock equals Pin input. 11 Decrement counter on Trigger input (both edges), Shift clock equals Trigger input.
19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18–16 TIMRST	Timer Reset

Table continues on the next page...

FLEXIOx_TIMCFGn field descriptions (continued)

Field	Description
	Configures the condition that causes the timer counter (and optionally the timer output) to be reset. In 8-bit counter mode, the timer reset will only reset the lower 8-bits that configure the baud rate. In all other modes, the timer reset will reset the full 16-bits of the counter. 000 Timer never reset 001 Reserved 010 Timer reset on Timer Pin equal to Timer Output 011 Timer reset on Timer Trigger equal to Timer Output 100 Timer reset on Timer Pin rising edge 101 Reserved 110 Timer reset on Trigger rising edge 111 Timer reset on Trigger rising or falling edge
15 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
14–12 TIMDIS	Timer Disable Configures the condition that causes the Timer to be disabled and stop decrementing. 000 Timer never disabled 001 Timer disabled on Timer N-1 disable 010 Timer disabled on Timer compare 011 Timer disabled on Timer compare and Trigger Low 100 Timer disabled on Pin rising or falling edge 101 Timer disabled on Pin rising or falling edge provided Trigger is high 110 Timer disabled on Trigger falling edge 111 Reserved
11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10–8 TIMENA	Timer Enable Configures the condition that causes the Timer to be enabled and start decrementing. 000 Timer always enabled 001 Timer enabled on Timer N-1 enable 010 Timer enabled on Trigger high 011 Timer enabled on Trigger high and Pin high 100 Timer enabled on Pin rising edge 101 Timer enabled on Pin rising edge and Trigger high 110 Timer enabled on Trigger rising edge 111 Timer enabled on Trigger rising or falling edge
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5–4 TSTOP	Timer Stop Bit The stop bit can be added on a timer compare (between each word) or on a timer disable. When stop bit is enabled, configured shifters will output the contents of the stop bit when the timer is disabled. When stop bit is enabled on timer disable, the timer remains disabled until the next rising edge of the shift clock. If configured for both timer compare and timer disable, only one stop bit is inserted on timer disable. 00 Stop bit disabled

Table continues on the next page...

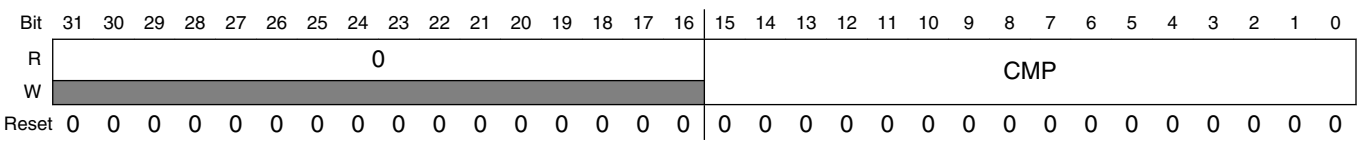
FLEXIO*x*_TIMCFG*n* field descriptions (continued)

Field	Description
	01 Stop bit is enabled on timer compare 10 Stop bit is enabled on timer disable 11 Stop bit is enabled on timer compare and timer disable
3–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 TSTART	Timer Start Bit When start bit is enabled, configured shifters will output the contents of the start bit when the timer is enabled and the timer counter will reload from the compare register on the first rising edge of the shift clock. 0 Start bit disabled 1 Start bit enabled
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

60.3.21 Timer Compare N Register (FLEXIO*x*_TIMCMP*n*)

.

Address: 400D_F000h base + 500h offset + (4d × i), where i=0d to 7d



FLEXIO*x*_TIMCMP*n* field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CMP	Timer Compare Value The timer compare value is loaded into the timer counter when the timer is first enabled, when the timer is reset and when the timer decrements down to zero. In dual 8-bit counters baud/bit mode, the lower 8-bits configures the baud rate divider equal to (CMP[7:0] + 1) * 2. The upper 8-bits configure the number of bits in each word equal to (CMP[15:8] + 1) / 2. In dual 8-bit counters PWM mode, the lower 8-bits configure the high period of the output to (CMP[7:0] + 1) and the upper 8-bits configure the low period of the output to (CMP[15:8] + 1). In 16-bit counter mode, the compare value can be used to generate the baud rate divider (if shift clock source is timer output) to equal (CMP[15:0] + 1) * 2. When the shift clock source is a pin or trigger input, the compare register is used to set the number of bits in each word equal to (CMP[15:0] + 1) / 2.

60.3.22 Shifter Buffer N Nibble Byte Swapped Register (FLEXIOx_SHIFTBUFNBS*n*)

.

Address: 400D_F000h base + 680h offset + (4d × i), where i=0d to 7d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	SHIFTBUFNBS																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_SHIFTBUFNBS*n* field descriptions

Field	Description
SHIFTBUFNBS	Shift Buffer Alias to SHIFTBUF register, except reads/writes to this register are nibble swapped within each byte. Reads return { SHIFTBUF[27:24], SHIFTBUF[31:28], SHIFTBUF[19:16], SHIFTBUF[23:20], SHIFTBUF[11:8], SHIFTBUF[15:12], SHIFTBUF[3:0], SHIFTBUF[7:4] }.

60.3.23 Shifter Buffer N Half Word Swapped Register (FLEXIOx_SHIFTBUFHWS*n*)

.

Address: 400D_F000h base + 700h offset + (4d × i), where i=0d to 7d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	SHIFTBUFHWS																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_SHIFTBUFHWS*n* field descriptions

Field	Description
SHIFTBUFHWS	Shift Buffer Alias to SHIFTBUF register, except reads/writes to this register are half word swapped. Reads return { SHIFTBUF[15:0], SHIFTBUF[31:24] }.

60.3.24 Shifter Buffer N Nibble Swapped Register (FLEXIOx_SHIFTBUFNIS*n*)

.

Address: 400D_F000h base + 780h offset + (4d × i), where i=0d to 7d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	SHIFTBUFNIS																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLEXIOx_SHIFTBUFNIS*n* field descriptions

Field	Description
SHIFTBUFNIS	Shift Buffer Alias to SHIFTBUF register, except reads/writes to this register are nibble swapped. Reads return { SHIFTBUF[3:0], SHIFTBUF[7:4], SHIFTBUF[11:8], SHIFTBUF[15:12], SHIFTBUF[19:16], SHIFTBUF[23:20], SHIFTBUF[27:24], SHIFTBUF[31:28] }.

60.4 Functional description

60.4.1 Shifter operation

Shifters are responsible for buffering and shifting data into or out of the FlexIO. The timing of shift, load and store events are controlled by the Timer assigned to the Shifter via the SHIFTCTL[TIMSEL] register. The Shifters are designed to support either DMA, interrupt or polled operation. The following block diagram provides a detailed view of the Shifter microarchitecture.

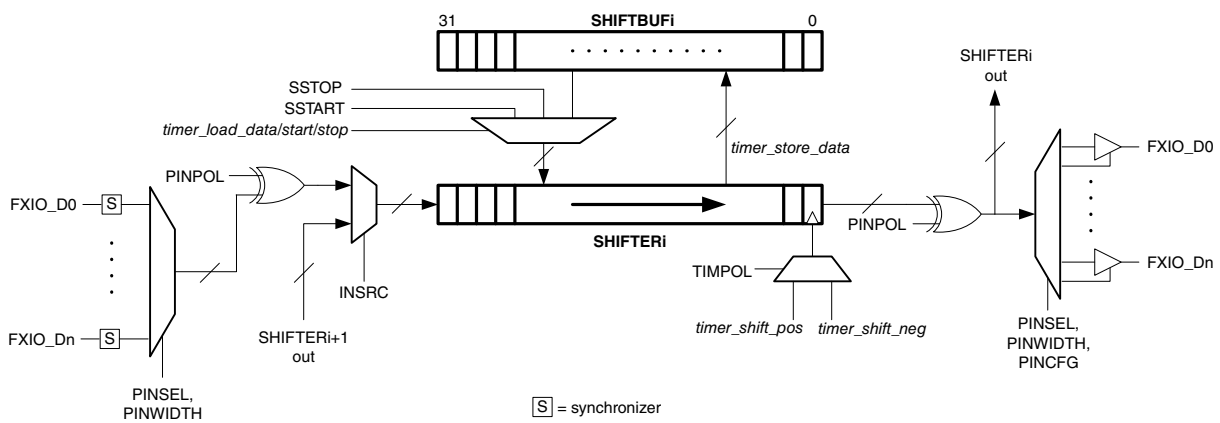


Figure 60-2. Shifter Microarchitecture

60.4.1.1 Transmit Mode

When configured for Transmit mode (SHIFTCTL[SMOD]=Transmit), the shifter will load data from the SHIFTBUF register and shift data out when a load event is signalled by the assigned Timer. An optional start/stop bit can also be automatically loaded before/after SHIFTBUF data by configuring the SHIFTCFG[SSTART], TIMCFG[TSTART] or SHIFTCFG[SSTOP], TIMCFG[TSTOP] registers in the Shifter and Timer. Note that the shifter will immediately load a stop bit when the Shifter is initially configured for Transmit mode if a stop bit is enabled.

The Shifter Status Flag (SHIFTSTAT[SSF]) and any enabled interrupts or DMA requests will set when data has been loaded from the SHIFTBUF register into the Shifter or when the Shifter is initially configured into Transmit mode. The flag will clear when new data has been written into the SHIFTBUF register.

The Shifter Error Flag (SHIFTERR[SEF]) and any enabled interrupts will set when an attempt to load data from an empty SHIFTBUF register occurs (buffer underrun). The flag can be cleared by writing it with logic 1.

60.4.1.2 Receive Mode

When configured for Receive mode (SHIFTCTL[SMOD]=Receive), the shifter will shift data in and store data into the SHIFTBUF register when a store event is signalled by the assigned Timer. Checking for a start/stop bit can be enabled before/after shifter data is sampled by configuring the SHIFTCFG[SSTART], TIMCFG[TSTART] or SHIFTCFG[SSTOP], TIMCFG[TSTOP] registers in the Shifter and Timer.

The Shifter Status Flag (SHIFTSTAT[SSF]) and any enabled interrupts or DMA requests will set when data has been stored into the SHIFTBUF register from the Shifter. The flag will clear when the data has been read from the SHIFTBUF register.

The Shifter Error Flag (SHIFTERR[SEF]) and any enabled interrupts will set when an attempt to store data into a full SHIFTBUF register occurs (buffer overrun) or when a mismatch occurs on a start/stop bit check. The flag can be cleared by writing it with logic 1.

60.4.1.3 Match Store Mode

When configured for Match Store mode (SHIFTCTL[SMOD]=Match Store), the shifter will shift data in, check for a match result and store matched data into the SHIFTBUF register when a store event is signalled by the assigned Timer. Checking for a start/stop bit can be enabled before/after shifter data is sampled by configuring the SHIFTCFG[SSTART], TIMCFG[TSTART] or SHIFTCFG[SSTOP], TIMCFG[TSTOP] registers in the Shifter and Timer. Up to 16-bits of data can be compared using SHIFTBUF[31:16] to configure the data to be matched and SHIFTBUF[15:0] to mask the match result.

The Shifter Status Flag (SHIFTSTAT[SSF]) and any enabled interrupts or DMA requests will set when a match occurs and matched data has been stored into the SHIFTBUF register from the Shifter. The flag will clear when the matched data has been read from the SHIFTBUF register.

The Shifter Error Flag (SHIFTERR[SEF]) and any enabled interrupts will set when an attempt to store matched data into a full SHIFTBUF register occurs (buffer overrun) or when a mismatch occurs on a start/stop bit check. The flag can be cleared by writing it with logic 1.

60.4.1.4 Match Continuous Mode

When configured for Match Continuous mode (SHIFTCTL[SMOD]=Match Continuous), the shifter will shift data in and continuously check for a match result whenever a shift event is signalled by the assigned Timer. Up to 16-bits of data can be compared using SHIFTBUF[31:16] to configure the data to be matched and SHIFTBUF[15:0] to mask the match result.

The Shifter Status Flag (SHIFTSTAT[SSF]) and any enabled interrupts or DMA requests will set when a match occurs. The flag will clear automatically as soon as there is no longer a match between Shifter data and SHIFTBUF register.

The Shifter Error Flag (SHIFTERR[SEF]) and any enabled interrupts will set when a match occurs. The flag will clear when there is a read from the SHIFTBUF register or it written with logic 1.

60.4.1.5 State Mode

Using State mode enables the user to implement any state machine with up to 8 states, 8 outputs and 3 selectable inputs per state. This feature allows basic control functions to be offloaded from the CPU using FlexIO hardware.

When configured for State mode (SHIFTCTL[SMOD]=State), the SHIFTBUF register is used to drive the output and compute next state values when the Shifter has been selected by the current state pointer (SHIFTSTATE[STATE]). The following diagram provides a detailed view of Shifter microarchitecture when configured for State mode.

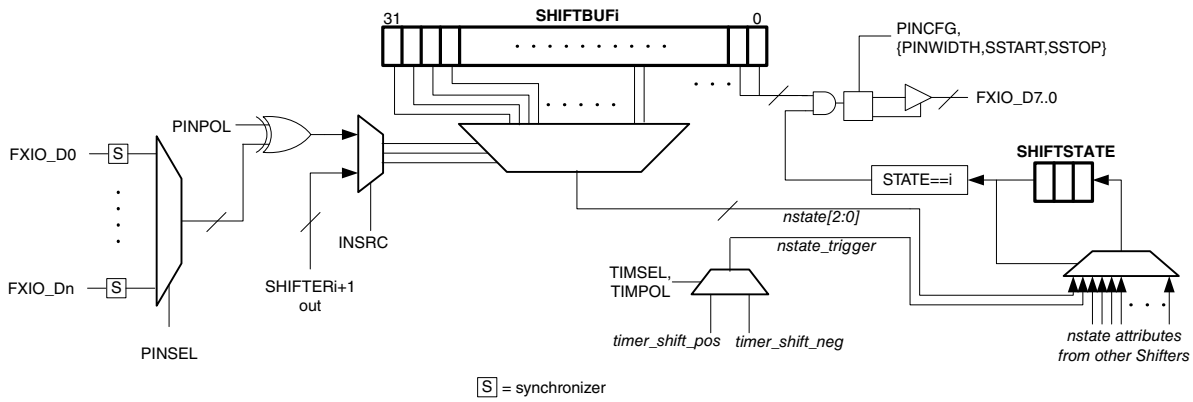


Figure 60-3. State Microarchitecture

When Shifter i has been selected by the current state pointer, output pins FXIO_D[7:0] will be driven by SHIFTBUFi[31:24] using the configuration set by SHIFTCTL[PINCFG]. When set, {PWIDTH[3:0],SSTOP[1:0],SSTART[1:0]} are respectively used to disable the output drive on pins FXIO_D[7:0] for state machine applications which require less than 8 output pins.

The next state value is computed using the 3 input pins selected by SHIFTCFG[PSEL] together with SHIFTBUFi[23:0]. Note that each state could potentially use a different set of 3 input pins. The following table details how the next state value is computed when the current state pointer is pointing to Shifter i.

Table 60-3. Next State computation for SHIFTSTATE[STATE]=i

FXIO_D[PSEL+2]	FXIO_D[PSEL+1]	FXIO_D[PSEL]	Next State Value
0	0	0	SHIFTBUFi[2:0]
0	0	1	SHIFTBUFi[5:3]
0	1	0	SHIFTBUFi[8:6]
0	1	1	SHIFTBUFi[11:9]
...	...	...	...
1	1	1	SHIFTBUFi[23:21]

Note that other shifters/timers could potentially be configured to drive the input pins of a given state, allowing the user to create complex combinations of shifters/timers as desired e.g. the output of a Shifter configured for logic mode could potentially be used to drive a state machine input.

The next state transition is triggered using the Timer output selected by SHIFTCTL[TIMSEL] with polarity controlled by SHIFTCTL[TIMPOL]. Note that each state could potentially use a different Timer to trigger each next state transition, allowing a variety of internal/external trigger sources and clocking configurations to be used (see Timer section for more detail).

The current state pointer defaults to Shifter 0 at reset, however it can be written by the user to select a different Shifter for the initial state. If the current state pointer selects a Shifter which is not configured for State mode, then outputs will not be driven and a next state transition is never triggered.

The Shifter Status Flag (SHIFTSTAT[SSF]) and any enabled interrupts or DMA requests will set whenever the Shifter has been selected by the current state pointer. The flag will clear when the current state pointer is updated to a different Shifter.

60.4.1.6 Logic Mode

Using logic mode enables the user to implement a small amount of programmable digital logic within a FlexIO Shifter. This feature allows board-level glue logic to be integrated on-chip using FlexIO hardware.

When configured for Logic mode (SHIFTCTL[SMOD]=Logic), the SHIFTBUF register is used to implement a 5-input, 32-bit programmable logic look-up table. The following diagram provides a detailed view of Shifter microarchitecture when configured for Logic mode.

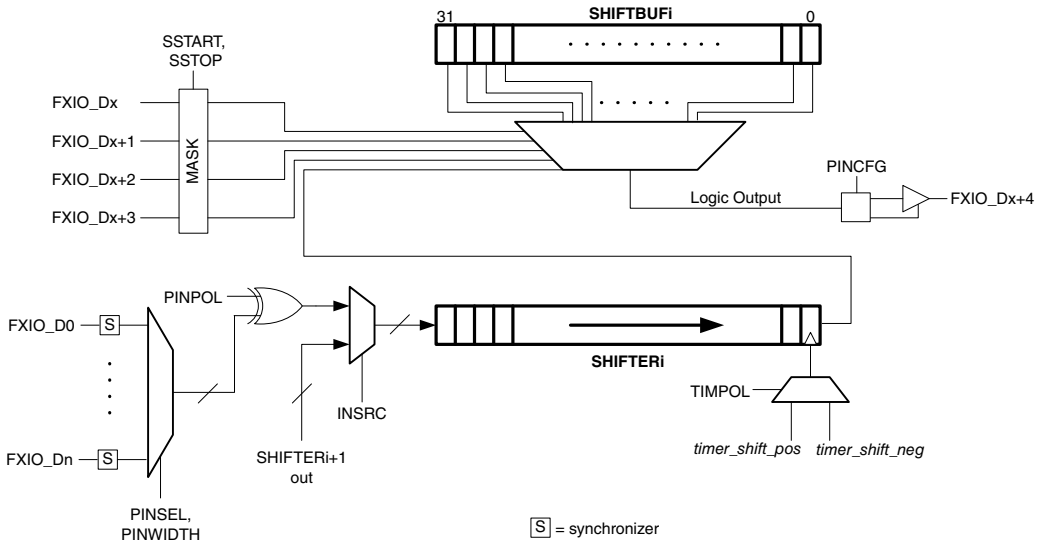


Figure 60-4. Logic Microarchitecture

The look-up table is driven using 4 pin inputs (maskable using SHIFTCFG[SSTOP] and SHFITCFG[SSTART]) plus 1 input from the internal shifter and can be configured to drive an output pin using the SHIFTCTL[PINCFG] field. Pin inputs and outputs are fixed for each logic look-up table and are not selectable. The following table lists the logic output value selected by the look-up table for Shifter 'i'.

Table 60-4. Logic Look-up table for Shifter 'i'

SHIFTERi[0]	FXIO_D[x+3][1]	FXIO_D[x+2]	FXIO_D[x+1]	FXIO_D[x]	Logic Output to FXIO_D[x+4]
0	0	0	0	0	SHIFTBUFi[0]
0	0	0	0	1	SHIFTBUFi[1]
0	0	0	1	0	SHIFTBUFi[2]
0	0	0	1	1	SHIFTBUFi[3]
...	...	...	...	...	...
1	1	1	1	1	SHIFTBUFi[31]

1. for Shifter i=0...3, x=i

   for Shifter i=4...7, x=i+4

To minimize output glitches, SHIFTCFG[SSTOP] and SHIFTCFG[SSTART] can be used to mask unused input pins. When set, {SSTOP[1:0], SSTART[1:0]} will mask FXIO_D[x+3]...FXIO_D[x] inputs respectively, so that any transitions on these pins will not cause the logic output to glitch.

Note that other shifters/timers could potentially be configured to drive the input pins of a given look-up table (without synchronization), allowing the user to concatenate look-up tables or create complex combinations of shifters/timers as desired.

SHIFTCFG[PWIDTH] will control the number of delay stages introduced by the internal shifter input (SHIFTERi[0]). For example, when configured for 1-bit shift (PWIDTH=0), the internal shifter will introduce a 32 Shift clock delay before passing its input (selected by SHIFTCTL[PSEL]) to the look-up table. When configured for 32-bit shift (PWIDTH=16...31), the internal shifter will introduce a 1 Shift clock delay to its input.

The Shifter Status Flag (SHIFTSTAT[SSF]) and any enabled interrupts or DMA requests will set whenever the output pin allocated to the logic look-up table has a value of 1 (after being synchronized to the FlexIO clock). The flag will clear when the output pin has a value of 0. This also allows the SSF flag to be used as a trigger to a Timer if desired.

The Shifter Error Flag (SHIFTERR[SEF]) and any enabled interrupts will set when the output pin allocated to the logic look-up table has a value of 1. The flag can be cleared by writing it with logic 1.

60.4.2 Timer operation

The FlexIO 16-bit timers control the loading, shifting and storing of the shift registers, the counters load the contents of the compare register and decrement down to zero on the FlexIO clock. They can perform generic timer functions such as generating a clock or select output or a PWM waveform. Timers can be configured to enable in response to a trigger, pin or shifter condition; decrement always or only on a trigger or pin edge; reset in response to a trigger or pin condition; and disable on a trigger or pin condition or on a timer compare. Timers can optionally include a start condition and/or stop condition.

Each timer operates independently, although a timer can be configured to enable or disable at the same time as the previous timer (eg: timer1 can enable or disable at the same time as timer 0) and a timer output can be used to trigger any other timer. The trigger used by each timer is configured independently and can be configured to be a timer output, shifter status flag, pin input or an external trigger input (refer to the chip configuration section for details on the external trigger connections). The trigger configuration is separate from the pin configuration, which can be configured for input, output data or output enable.

The Timer Configuration Register (TIMCFGn) should be configured before setting the Timer Mode (TIMOD). Once the TIMOD is configured for the desired mode, when the condition configured by timer enable (TIMENA) is detected then the following events occur.

- Timer counter will load the current value of the Compare Register and start decrementing as configured by TIMDEC.

- Timer output will set depending on the TIMOUT configuration.
- Transmit shifters controlled by this timer will either output their start bit value, or load the shift register from the shift buffer and output the first bit, as configured by SSTART.

The Timer will then generate the timer output and timer shift clock depending on the TIMOD and TIMDEC fields. The shifter clock is either equal to the timer output (when TIMDEC=00 or 01) or equal to the decrement clock (when TIMDEC=10 or 11). When TIMDEC is configured to decrement from a pin or trigger, the timer will decrement on both rising and falling edges.

When the Timer is configured to reset as configured in the TIMRST field then the Timer counter will load the current value of the Compare Register again, the timer output may also be affected by the reset as configured in TIMOUT.

If the Timer start bit is enabled, the timer counter will reload with the compare register on the first rising edge of the shift clock after the timer starts decrementing. If there is no falling edge on the shift clock before the first rising edge (for example, when TIMOUT=1), a shifter that is configured to shift on falling edge and load on the first shift will not load correctly.

When configured for 8-bit counter mode, whenever the lower 8-bit counter decrements to zero the timer output will toggle, the lower 8-bit counter register will reload from the compare register and the upper 8-bit counter will decrement. For 8-bit PWM mode, the lower 8-bit counter will only decrement when the output is high and the upper 8-bit counter will only decrement when the output is low. The timer output will toggle whenever either lower or upper 8-bit counter decrements to zero.

When the timer decrements to zero, a compare event occurs depending on the timer mode. For 8-bit counter or PWM modes, both halves of the counter must equal zero and the upper half must decrement for the timer compare event to occur, while in 16-bit mode the entire counter must equal zero and decrement. The timer compare event will cause the timer status flag to set, the timer counter to load the contents of the timer compare register, the timer output to toggle, any configured transmit shift registers to load and any configured receive shift registers to store .

When the is Timer is configured to add a stop bit on each compare, the following additional events will occur.

- Transmit shifters controlled by this timer will output their stop bit value (if configured by SSTOP).
- Receive shifters controlled by this timer will store the contents of the shift register in their shift buffer, as configured by SSTOP.
- On the first rising edge of the shifter clock after the compare, the timer counter will reload the current value of the Compare Register.

Transmit shifters must be configured to load on the first shift when the timer is configured to insert a stop bit on each compare.

When the condition configured by timer disable (TIMDIS) is detected, the following events occur.

- Timer counter will reload the current value of the Compare Register and start decrementing as configured by TIMDEC.
- Timer output will clear.
- Transmit shifters controlled by this timer will output their stop bit value (if configured by SSTOP).
- Receive shifters controlled by this timer will store the contents of the shift register in their shift buffer, as configured by SSTOP.

If the timer stop bit is enabled, the timer counter will continue decrementing until the next rising edge of the shift clock is detected, at which point it will finish. A timer enable condition can be detected in the same cycle as a timer disable condition (if timer stop bit is disabled), or on the first rising edge of the shift clock after the disable condition (if stop bit is enabled). Receive shift registers will stop bit enabled will store the contents of the shift register into the shift buffer and verify the state of the input data on the configured shift edge while the timer is in the stop state condition. If there is no configured edge between the timer disable and the next rising edge of the shift clock then the final store and verify do not occur.

60.4.3 Pin operation

The pin configuration for each timer and shifter can be configured to use any FlexIO pin with either polarity. Each timer and shifter can be configured as an input, output data, output enable or bidirectional output. A pin configured for output enable can be used as an open drain (with inverted polarity, since the output enable assertion would cause logic zero to be output on the pin) or to control the enable on the bidirectional output. Any timer or shifter could be configured to control the output enable for a pin where the bidirectional output data is driven by another timer or shifter.

In addition, shifters can also be configured to use multiple FlexIO pins in parallel using the SHIFTCFG[PWIDTH] field. PWIDTH is used to configure the following settings of a shifter:

1. Number of bits shifted per Shift clock.
2. Number of pins driven by the shifter per Shift clock (only on shifters supporting parallel transmit i.e. SHIFTER0, SHIFTER4).
3. Number of pins sampled by the shifter per Shift clock (only on Shifter supporting parallel receive i.e. SHIFTER3, SHIFTER7).

When configured for parallel shift, either 4, 8, 16 or 32-bits can be shifted on every Shift clock. If an adjacent shifter is selected as the input source (SHIFTCFG[INSRC]=1), the least significant 4, 8, 16 or 32-bits from the adjacent shifter will be sampled on each Shift clock.

For shifters supporting parallel receive (SHIFTER3, SHIFTER7), the shifter can be configured to sample multiple pins (SHIFTCFG[INSRC]=0), with PWIDTH and PSEL selecting the pins as follows: FXIO_D[PSEL+PWIDTH]:FXIO_D[PSEL]. Note that if PWIDTH is less than the number of bits being shifted on each Shift clock, then the most significant bits will be masked with 0 e.g. if PSEL=7 and PWIDTH=6, then SHIFTER[31:24] will sample {0,0,FXIO_D[12:7]} on each Shift clock.

For shifters supporting parallel transmit (SHIFTER0, SHIFTER4), the shifter can be configured to drive multiple pins using SHIFTCTL[PINCFG], with PWIDTH and PSEL selecting the pins as follows: FXIO_D[PSEL+PWIDTH]:FXIO_D[PSEL]. Note that if PWIDTH is less than the number of bits being shifted on each Shift clock, then the most significant pins will not be driven e.g. if PSEL=7 and PWIDTH=6, then SHIFTER[5:0] will drive only FXIO_D[12:7] on each Shift clock.

When configuring a pin as an input (this includes a timer trigger configured as a pin input), the input signal is first synchronized to the FlexIO clock before the signal is used by a timer or shifter. This introduces a small latency of between 0.5 to 1.5 FlexIO clock cycles when using an external pin input to generate an output or control a shifter. This sets the maximum setup time at 1.5 FlexIO clock cycles.

If an input is used by more than one timer or shifter then the synchronization occurs once to ensure any edge is seen on the same cycle by all timers and shifters using that input.

Note that FlexIO pins are also connected internally, configuring a FlexIO shifter or timer to output data on an unused pin will make an internal connection that allows other shifters and timer to use this pin as an input. This allows a shifter output to be used to trigger a timer or a timer output to be shifted into a shifter. This path is also synchronized to the FlexIO clock and therefore incurs a 1 cycle latency.

So when using a Pin input as a Timer Trigger, Timer Clock or Shifter Data Input, the following synchronization delays occur:

1. 0.5 – 1.5 FlexIO clock cycles for external pin
2. 1 FlexIO clock cycle for an internally driven pin

For timing considerations such as output valid time and input setup time for specific applications (SPI Master, SPI Slave, I2C Master, I2S Master, I2S Slave) please refer to the FlexIO Application Information Section.

60.5 Application Information

This section provides examples for a variety of FlexIO module applications.

60.5.1 UART Transmit

UART transmit can be supported using one Timer, one Shifter and one Pin (two Pins if supporting CTS). The start and stop bit insertion is handled automatically and multiple transfers can be supported using DMA controller. The timer status flag can be used to indicate when the stop bit of each word is transmitted.

Break and idle characters require software intervention, before transmitting a break or idle character the SSTART and SSTOP fields should be altered to transmit the required state and the data to transmit must equal 0xFF or 0x00. Supporting a second stop bit requires the stop bit to be inserted into the data stream using software (and increasing the number of bits to transmit). Note that when performing byte writes to SHIFTBUFn (or SHIFTBUFBIS for transmitting MSB first), the rest of the register remains unaltered allowing an address mark bit or additional stop bit to remain undisturbed.

FlexIO does not support automatic insertion of parity bits.

Table 60-5. UART Transmit Configuration

Register	Value	Comments
SHIFTCFGn	0x0000_0032	Configure start bit of 0 and stop bit of 1.
SHIFTCTLn	0x0003_0002	Configure transmit using Timer 0 on posedge of clock with output data on Pin 0. Can invert output data by setting PINPOL, or can support open drain by setting PINPOL=0x1 and PINCFG=0x1.
TIMCMPn	0x0000_0F01	Configure 8-bit transfer with baud rate of divide by 4 of the FlexIO clock. Set TIMCMP[15:8] = (number of bits x 2) - 1. Set TIMCMP[7:0] = (baud rate divider / 2) - 1.
TIMCFGn	0x0000_2222	Configure start bit, stop bit, enable on trigger low and disable on compare. Can support CTS by configuring TIMEN=0x3.
TIMCTLn	0x01C0_0001	Configure dual 8-bit counter using Shifter 0 status flag as inverted internal trigger source. Can support CTS by configuring PINSEL=0x1 (for Pin 1) and PINPOL=0x1.
SHIFTBUFn	Data to transmit	Transmit data can be written to SHIFTBUF[7:0] to initiate an 8-bit

Table 60-5. UART Transmit Configuration

Register	Value	Comments
		transfer, use the Shifter Status Flag to indicate when data can be written using interrupt or DMA request. Can support MSB first transfer by writing to SHIFTBUFBBS[7:0] register instead.

60.5.2 UART Receive

UART receive can be supported using one Timer, one Shifter and one Pin (two Timers and two Pins if supporting RTS). The start and stop bit verification is handled automatically and multiple transfers can be supported using the DMA controller. The timer status flag can be used to indicate when the stop bit of each word is received.

Triple voting of the received data is not supported by FlexIO, data is sampled only once in the middle of each bit. Another timer can be used to implement a glitch filter on the incoming data, another Timer can also be used to detect an idle line of programmable length. Break characters will cause the error flag to set and the shifter buffer register will return 0x00.

FlexIO does not support automatic verification of parity bits.

Table 60-6. UART Receiver Configuration

Register	Value	Comments
SHIFTCFGn	0x0000_0032	Configure start bit of 0 and stop bit of 1.
SHIFTCTLn	0x0080_0001	Configure receive using Timer 0 on negedge of clock with input data on Pin 0. Can invert input data by setting PINPOL.
TIMCMPn	0x0000_0F01	Configure 8-bit transfer with baud rate of divide by 4 of the FlexIO clock. Set TIMCMP[15:8] = (number of bits x 2) - 1. Set TIMCMP[7:0] = (baud rate divider / 2) - 1.
TIMCFGn	0x0204_2422	Configure start bit, stop bit, enable on pin posedge and disable on compare. Enable resynchronization to received data with TIMOUT=0x2 and TIMRST=0x4.
TIMCTLn	0x0000_0081	Configure dual 8-bit counter using inverted Pin 0 input.
SHIFTBUFn	Data to receive	Received data can be read from SHIFTBUFBYS[7:0], use the Shifter Status Flag to indicate when data can be

Table 60-6. UART Receiver Configuration

Register	Value	Comments
		read using interrupt or DMA request. Can support MSB first transfer by reading from SHIFTBUFBIS[7:0] register instead.

The UART Receiver with RTS configuration uses a 2nd Timer to generate the RTS output. The RTS will assert when the start bit is detected and negate when the data is read from the shifter buffer register. No start bit will be detected while the RTS is asserted, the received data is simply ignored.

Table 60-7. UART Receiver with RTS Configuration

Register	Value	Comments
SHIFTCFGn	0x0000_0032	Configure start bit of 0 and stop bit of 1.
SHIFTCTLn	0x0080_0001	Configure receive using Timer 0 on negedge of clock with input data on Pin 0. Can invert input data by setting PINPOL.
TIMCMPn	0x0000_0F01	Configure 8-bit transfer with baud rate of divide by 4 of the FlexIO clock. Set TIMCMP[15:8] = (number of bits x 2) - 1. Set TIMCMP[7:0] = (baud rate divider / 2) - 1.
TIMCFGn	0x0204_2522	Configure start bit, stop bit, enable on pin posedge with trigger low and disable on compare. Enable resynchronization to received data with TIMOUT=0x2 and TIMRST=0x4.
TIMCTLn	0x03C0_0081	Configure dual 8-bit counter using inverted Pin 0 input. Trigger is internal using inverted Pin 1 input.
TIMCMP(n+1)	0x0000_FFFF	Never compare.
TIMCFG(n+1)	0x0030_6100	Enable on Timer N enable and disable on trigger falling edge. Decrement on trigger to ensure no compare.
TIMCTL(n+1)	0x0143_0083	Configure 16-bit counter and output on Pin 1. Trigger is internal using Shifter 0 flag.
SHIFTBUFn	Data to receive	Received data can be read from SHIFTBUFBYS[7:0], use the Shifter Status Flag to indicate when data can be read using interrupt or DMA request. Can support MSB first transfer by reading from SHIFTBUFBIS[7:0] register instead.

60.5.3 SPI Master

SPI master mode can be supported using two Timers, two Shifters and four Pins. Either CPHA=0 or CPHA=1 can be supported and transfers can be supported using the DMA controller. For CPHA=1, the select can remain asserted for multiple transfers and the timer status flag can be used to indicate the end of the transfer.

The stop bit is used to guarantee a minimum of 1 clock cycle between the slave select negating and before the next transfer. Writing to the transmit buffer by either core or DMA is used to initiate each transfer.

Due to synchronization delays, the setup time for the serial input data is 1.5 FlexIO clock cycles, so the maximum baud rate is divide by 4 of the FlexIO clock frequency.

Table 60-8. SPI Master (CPHA=0) Configuration

Register	Value	Comments
SHIFTCFGn	0x0000_0000	Start and stop bit disabled.
SHIFTCTLn	0x0083_0002	Configure transmit using Timer 0 on negedge of clock with output data on Pin 0.
SHIFTCFG(n+1)	0x0000_0000	Start and stop bit disabled.
SHIFTCTL(n+1)	0x0000_0101	Configure receive using Timer 0 on posedge of clock with input data on Pin 1.
TIMCMPn	0x0000_3F01	Configure 32-bit transfer with baud rate of divide by 4 of the FlexIO clock. Set TIMCMP[15:8] = (number of bits x 2) - 1. Set TIMCMP[7:0] = (baud rate divider / 2) - 1.
TIMCFGn	0x0100_2222	Configure start bit, stop bit, enable on trigger high and disable on compare, initial clock state is logic 0. Set PINPOL to invert the output shift clock.
TIMCTLn	0x01C3_0201	Configure dual 8-bit counter using Pin 2 output (shift clock), with Shifter 0 flag as the inverted trigger.
TIMCMP(n+1)	0x0000_FFFF	Never compare.
TIMCFG(n+1)	0x0000_1100	Enable when Timer 0 is enabled and disable when Timer 0 is disabled.
TIMCTL(n+1)	0x0003_0383	Configure 16-bit counter (never compare) using inverted Pin 3 output (as slave select).
SHIFTBUFn	Data to transmit	Transmit data can be written to SHIFTBUF, use the Shifter Status Flag to indicate when data can be written using interrupt or DMA request. Can

Table continues on the next page...

Table 60-8. SPI Master (CPHA=0) Configuration (continued)

Register	Value	Comments
		support MSB first transfer by writing to SHIFTBUFBBS register instead.
SHIFTBUF(n+1)	Data to receive	Received data can be read from SHIFTBUFBYS, use the Shifter Status Flag to indicate when data can be read using interrupt or DMA request. Can support MSB first transfer by reading from SHIFTBUFBIS register instead.

Table 60-9. SPI Master (CPHA=1) Configuration

Register	Value	Comments
SHIFTCFGn	0x0000_0021	Start bit loads data on first shift.
SHIFTCTLn	0x0003_0002	Configure transmit using Timer 0 on posedge of clock with output data on Pin 0.
SHIFTCFG(n+1)	0x0000_0000	Start and stop bit disabled.
SHIFTCTL(n+1)	0x0080_0101	Configure receive using Timer 0 on negedge of clock with input data on Pin 1.
TIMCMPn	0x0000_3F01	Configure 32-bit transfer with baud rate of divide by 4 of the FlexIO clock. Set TIMCMP[15:8] = (number of bits x 2) - 1. Set TIMCMP[7:0] = (baud rate divider / 2) - 1.
TIMCFGn	0x0100_2222	Configure start bit, stop bit, enable on trigger high and disable on compare, initial clock state is logic 0. Set PINPOL to invert the output shift clock. Set TIMDIS=3 to keep slave select asserted for as long as there is data in the transmit buffer.
TIMCTLn	0x01C3_0201	Configure dual 8-bit counter using Pin 2 output (shift clock), with Shifter 0 flag as the inverted trigger.
TIMCMP(n+1)	0x0000_FFFF	Never compare.
TIMCFG(n+1)	0x0000_1100	Enable when Timer 0 is enabled and disable when Timer 0 is disabled.
TIMCTL(n+1)	0x0003_0383	Configure 16-bit counter (never compare) using inverted Pin 3 output (as slave select).
SHIFTBUFn	Data to transmit	Transmit data can be written to SHIFTBUF, use the Shifter Status Flag to indicate when data can be written using interrupt or DMA request. Can support MSB first transfer by writing to SHIFTBUFBBS register instead.

Table continues on the next page...

Table 60-9. SPI Master (CPHA=1) Configuration (continued)

Register	Value	Comments
SHIFTBUF(n+1)	Data to receive	Received data can be read from SHIFTBUFBYS, use the Shifter Status Flag to indicate when data can be read using interrupt or DMA request. Can support MSB first transfer by reading from SHIFTBUFBIS register instead.

60.5.4 SPI Slave

SPI slave mode can be supported using one Timer, two Shifters and four Pins. Either CPHA=0 or CPHA=1 can be supported and transfers can be supported using the DMA controller. For CPHA=1, the select can remain asserted for multiple transfers and the timer status flag can be used to indicate the end of the transfer.

The transmit data must be written to the transmit buffer register before the external slave select asserts, otherwise the shifter error flag will be set.

Due to synchronization delays, the output valid time for the serial output data is 2.5 FlexIO clock cycles, so the maximum baud rate is divide by 6 of the FlexIO clock frequency.

Table 60-10. SPI Slave (CPHA=0) Configuration

Register	Value	Comments
SHIFTCFGn	0x0000_0000	Start and stop bit disabled.
SHIFTCTLn	0x0083_0002	Configure transmit using Timer 0 on falling edge of shift clock with output data on Pin 0.
SHIFTCFG(n+1)	0x0000_0000	Start and stop bit disabled.
SHIFTCTL(n+1)	0x0000_0101	Configure receive using Timer 0 on rising edge of shift clock with input data on Pin 1.
TIMCMPn	0x0000_003F	Configure 32-bit transfer. Set TIMCMP[15:0] = (number of bits x 2) - 1.
TIMCFGn	0x0120_6600	Configure enable on trigger rising edge and disable on trigger falling edge, initial clock state is logic 0 and decrement on pin input.
TIMCTLn	0x06C0_0203	Configure 16-bit counter using Pin 2 input (shift clock), with Pin 3 input (slave select) as the inverted trigger.
SHIFTBUFn	Data to transmit	Transmit data can be written to SHIFTBUF, use the Shifter Status Flag to indicate when data can be written

Table continues on the next page...

Table 60-10. SPI Slave (CPHA=0) Configuration (continued)

Register	Value	Comments
		using interrupt or DMA request. Can support MSB first transfer by writing to SHIFTBUFBBS register instead.
SHIFTBUF(n+1)	Data to receive	Received data can be read from SHIFTBUFBYS, use the Shifter Status Flag to indicate when data can be read using interrupt or DMA request. Can support MSB first transfer by reading from SHIFTBUFBIS register instead.

Table 60-11. SPI Slave (CPHA=1) Configuration

Register	Value	Comments
SHIFTCFGn	0x0000_0001	Shifter configured to load on first shift and stop bit disabled.
SHIFTCTLn	0x0003_0002	Configure transmit using Timer 0 on rising edge of shift clock with output data on Pin 0.
SHIFTCFG(n+1)	0x0000_0000	Start and stop bit disabled.
SHIFTCTL(n+1)	0x0080_0101	Configure receive using Timer 0 on falling edge of shift clock with input data on Pin 1.
TIMCMPn	0x0000_003F	Configure 32-bit transfer. Set TIMCMP[15:0] = (number of bits x 2) - 1.
TIMCFGn	0x0120_6602	Configure start bit, enable on trigger rising edge, disable on trigger falling edge, initial clock state is logic 0 and decrement on pin input.
TIMCTLn	0x06C0_0203	Configure 16-bit counter using Pin 2 input (shift clock), with Pin 3 input (slave select) as the inverted trigger.
SHIFTBUFn	Data to transmit	Transmit data can be written to SHIFTBUF, use the Shifter Status Flag to indicate when data can be written using interrupt or DMA request. Can support MSB first transfer by writing to SHIFTBUFBBS register instead.
SHIFTBUF(n+1)	Data to receive	Received data can be read from SHIFTBUFBYS, use the Shifter Status Flag to indicate when data can be read using interrupt or DMA request. Can support MSB first transfer by reading from SHIFTBUFBIS register instead.

60.5.5 I2C Master

I2C master mode can be supported using two Timers, two Shifters and two Pins. One timer is used to generate the SCL output and one timer is used to control the shifters. The two shifters are used to transmit and receive for every word, when receiving the transmitter must transmit 0xFF to tristate the output. FlexIO inserts a stop bit after every word to generate/verify the ACK/NACK. FlexIO waits for the first write to the transmit data buffer before enabling SCL generation. Data transfers can be supported using the DMA controller and the shifter error flag will set on transmit underrun or receive overflow.

The first timer generates the bit clock for the entire packet (START to Repeated START/ STOP), so the compare register needs to be programmed with the total number of clock edges in the packet (minus one). The timer supports clock stretching using the reset counter when pin equal to output (although this increases both the clock high and clock low periods by at least 1 FlexIO clock cycle each). The second timer uses the SCL input pin to control the transmit/receive shift registers, this enforces an SDA data hold time by an extra 2 FlexIO clock cycles.

Both the transmit and receive shifters need to be serviced for each word in the transfer, the transmit shifter must transmit 0xFF when receiving and the receive shifter returns the data actually present on the SDA pin. The transmit shifter will load 1 additional word on the last falling edge of SCL pin, this word should be 0x00 if generating a STOP condition or 0xFF if generating a repeated START condition. During the last word of a master-receiver transfer, the transmit SSTOP bit should be set by software to generate a NACK.

The receive shift register will assert an error interrupt if a NACK is detected, but software is responsible for generating the STOP or repeated START condition. If a NACK is detected during master-transmit, the interrupt routine should immediately write the transmit shifter register with 0x00 (if generating STOP) or 0xFF (if generating repeated START). Software should then wait for the next rising edge on SCL and then disable both timers. The transmit shifter should then be disabled after waiting the setup delay for a repeated START or STOP condition.

Due to synchronization delays, the data valid time for the transmit output is 2 FlexIO clock cycles, so the maximum baud rate is divide by 6 of the FlexIO clock frequency.

The I2C master data valid is delayed 2 cycles because the clock output is passed through a synchronizer before clocking the transmit/receive shifter (to guarantee some SDA hold time). Since the SCL output is synchronous with FlexIO clock, the synchronization delay is 1 cycle and then 1 cycle to generate the output.

Table 60-12. I2C Master Configuration

Register	Value	Comments
SHIFTCFGn	0x0000_0032	Start bit enabled (logic 0) and stop bit enabled (logic 1).
SHIFTCTLn	0x0101_0082	Configure transmit using Timer 1 on rising edge of clock with inverted output enable (open drain output) on Pin 0.
SHIFTCFG(n+1)	0x0000_0020	Start bit disabled and stop bit enabled (logic 0) for ACK/NACK detection.
SHIFTCTL(n+1)	0x0180_0001	Configure receive using Timer 1 on falling edge of clock with input data on Pin 0.
TIMCMPn	0x0000_2501	Configure 2 word transfer with baud rate of divide by 4 of the FlexIO clock. Set TIMCMP[15:8] = (number of words x 18) + 1. Set TIMCMP[7:0] = (baud rate divider / 2) - 1.
TIMCFGn	0x0102_2222	Configure start bit, stop bit, enable on trigger high, disable on compare, reset if output equals pin. Initial clock state is logic 0 and is not affected by reset.
TIMCTLn	0x01C1_0101	Configure dual 8-bit counter using Pin 1 output enable (SCL open drain), with Shifter 0 flag as the inverted trigger.
TIMCMP(n+1)	0x0000_000F	Configure 8-bit transfer. Set TIMCMP[15:0] = (number of bits x 2) - 1.
TIMCFG(n+1)	0x0020_1112	Enable when Timer 0 is enabled, disable when Timer 0 is disabled, enable start bit and stop bit at end of each word, decrement on pin input.
TIMCTL(n+1)	0x01C0_0183	Configure 16-bit counter using inverted Pin 1 input (SCL).
SHIFTBUFn	Data to transmit	Transmit data can be written to SHIFTBUFBBS[7:0], use the Shifter Status Flag to indicate when data can be written using interrupt or DMA request.
SHIFTBUF(n+1)	Data to receive	Received data can be read from SHIFTBUFBIS[7:0], use the Shifter Status Flag to indicate when data can be read using interrupt or DMA request.

60.5.6 I2S Master

I2S master mode can be supported using two Timers, two Shifters and four Pins. One timer is used to generate the bit clock and control the shifters and one timer is used to generate the frame sync. FlexIO waits for the first write to the transmit data buffer before

enabling bit clock and frame sync generation. Data transfers can be supported using the DMA controller and the shifter error flag will set on transmit underrun or receive overflow.

The bit clock frequency is an even integer divide of the FlexIO clock frequency, and the initial frame sync assertion occurs at the same time as the first bit clock edge. The timer uses the start bit to ensure the frame sync is generated one clock cycle before the first output data.

Due to synchronization delays, the setup time for the receiver input is 1.5 FlexIO clock cycles, so the maximum baud rate is divide by 4 of the FlexIO clock frequency.

Table 60-13. I2S Master Configuration

Register	Value	Comments
SHIFTCFGn	0x0000_0001	Load transmit data on first shift and stop bit disabled.
SHIFTCTLn	0x0003_0002	Configure transmit using Timer 0 on rising edge of clock with output data on Pin 0.
SHIFTCFG(n+1)	0x0000_0000	Start and stop bit disabled.
SHIFTCTL(n+1)	0x0080_0101	Configure receive using Timer 0 on falling edge of clock with input data on Pin 1.
TIMCMPn	0x0000_3F01	Configure 32-bit transfer with baud rate of divide by 4 of the FlexIO clock. Set TIMCMP[15:8] = (number of bits x 2) - 1. Set TIMCMP[7:0] = (baud rate divider / 2) - 1.
TIMCFGn	0x0000_0202	Configure start bit, enable on trigger high and never disable. Initial clock state is logic 1.
TIMCTLn	0x01C3_0201	Configure dual 8-bit counter using Pin 2 output (bit clock), with Shifter 0 flag as the inverted trigger. Set PINPOL to invert the output shift clock.
TIMCMP(n+1)	0x0000_007F	Configure 32-bit transfer with baud rate of divide by 4 of the FlexIO clock. Set TIMCMP[15:0] = (number of bits x baud rate divider) - 1.
TIMCFG(n+1)	0x0000_0100	Enable when Timer 0 is enabled and never disable.
TIMCTL(n+1)	0x0003_0383	Configure 16-bit counter using inverted Pin 3 output (as frame sync).
SHIFTBUFn	Data to transmit	Transmit data can be written to SHIFTBUFBIS, use the Shifter Status Flag to indicate when data can be written using interrupt or DMA request. Can support LSB first transfer by writing to SHIFTBUF register instead.

Table continues on the next page...

Table 60-13. I2S Master Configuration (continued)

Register	Value	Comments
SHIFTBUF(n+1)	Data to receive	Received data can be read from SHIFTBUFBIS, use the Shifter Status Flag to indicate when data can be read using interrupt or DMA request. Can support LSB first transfer by reading from SHIFTBUF register instead.

60.5.7 I2S Slave

I2S slave mode can be supported using two Timers, two Shifters and four Pins (for single transmit and single receive, other combinations of transmit and receive are possible).

The transmit data must be written to the transmit buffer register before the external frame sync asserts, otherwise the shifter error flag will be set.

Due to synchronization delays, the output valid time for the serial output data is 2.5 FlexIO clock cycles, so the maximum baud rate is divide by 6 of the FlexIO clock frequency.

The output valid time of I2S slave is max 2.5 cycles because there is a maximum 1.5 cycle delay on the clock synchronization plus 1 cycle to output the data

Table 60-14. I2S Slave Configuration

Register	Value	Comments
SHIFTCFGn	0x0000_0000	Start and stop bit disabled.
SHIFTCTLn	0x0103_0002	Configure transmit using Timer 1 on rising edge of shift clock with output data on Pin 0.
SHIFTCFG(n+1)	0x0000_0000	Start and stop bit disabled.
SHIFTCTL(n+1)	0x0180_0101	Configure receive using Timer 1 on falling edge of shift clock with input data on Pin 1.
TIMCMPn	0x0000_007D	Configure two 32-bit transfers per frame. Set TIMCMP[15:0] = (number of bits x 4) - 3.
TIMCFGn	0x0030_2400	Configure enable on pin rising edge (inverted frame sync) and disable on compare, initial clock state is logic 1 and decrement on trigger input (bit clock).
TIMCTLn	0x0440_0383	Configure 16-bit counter using inverted Pin 3 input (frame sync), with Pin 2 input (bit clock) as the trigger.

Table continues on the next page...

Table 60-14. I2S Slave Configuration (continued)

Register	Value	Comments
TIMCMP(n+1)	0x0000_003F	Configure 32-bit transfers. Set TIMCMP[15:0] = (number of bits x 2) - 1.
TIMCFG(n+1)	0x0020_3500	Configure enable on pin rising edge with trigger high and disable on compare with trigger low, initial clock state is logic 0 and decrement on pin input.
TIMCTL(n+1)	0x0340_0203	Configure 16-bit counter using Pin 2 input (bit clock), with Timer 0 output as the trigger.
SHIFTBUFn	Data to transmit	Transmit data can be written to SHIFTBUFBIS, use the Shifter Status Flag to indicate when data can be written using interrupt or DMA request. Can support LSB first transfer by writing to SHIFTBUF register instead.
SHIFTBUF(n+1)	Data to receive	Received data can be read from SHIFTBUFBIS, use the Shifter Status Flag to indicate when data can be read using interrupt or DMA request. Can support LSB first transfer by reading from SHIFTBUF register instead.

60.5.8 Camera Interface

Camera Interface can be supported using one Timer, one or more Shifters and multiple Pins. Multiple transfers can be supported using DMA controller.

The example below describes FlexIO configuration for interfacing to an 8-bit CMOS sensor with PCLK, VSYNC, HREF and D[7:0] outputs. The example uses a 128-bit buffer to capture 16-pixels of image data before interrupt or DMA transfer, however a bigger or smaller buffer may be used depending on system DMA performance and FlexIO resource usage by other applications. Note that additional timers may be used to track number of pixels per row and number of rows per frame or HREF/VSYNC may be assigned as GPIO interrupts for software tracking.

Table 60-15. Camera Interface Configuration for 8-bit CMOS sensor

Register	Value	Comments
SHIFTCFGn...n+2[1]	0x0007_0100	Configure 8-bit parallel shift in from adjacent shifter.
SHIFTCFGn+3	0x0007_0000	Configure 8-bit parallel shift in from pins FXIO_D[7:0] (D[7:0]).
SHIFTCTLn...n+3	0x0080_0001	Configure receive using Timer 0 on negedge of clock.

Table continues on the next page...

Table 60-15. Camera Interface Configuration for 8-bit CMOS sensor (continued)

Register	Value	Comments
TIMCMPn	0x0000_001F	Configure 16-pixel (8 bits/pixel x 16 pixels = 128-bits) transfer. Set TIMCMP[15:0] = (number of pixels x 2) - 1.
TIMCFGn	0x0120_6600	Configure enable on trigger (HREF) rising edge and disable on trigger falling edge, initial Shift clock state is logic 0 and decrement on PCLK input.
TIMCTLn	0x12C0_0803	Configure 16-bit counter using FXIO_D[8] input (PCLK), with FXIO_D[9] input (HREF) as the inverted trigger.
SHIFTBUFn...n+3	Data to receive	Received data can be read from SHIFTBUFn...n+3, use the Shifter Status Flag to indicate when data can be read using interrupt or DMA request.

1. n=0 or 4

60.5.9 Motorola 68K/Intel 8080 Bus Interface

The Motorola 68K and Intel 8080 bus are two parallel interfaces commonly used by Smart/Asynchronous LCD controllers. In conjunction with GPIO, FlexIO is able to drive these interfaces using one Timer and one Shifter, although additional Shifters could be used to support large transfers via the DMA controller.

The configuration below provides an example of how to drive a 16-bit 68K or 8080 bus. For a 8080 bus, two GPIO are used to drive the nCS and RS pins. For a 68K bus, an additional GPIO is required to drive the RDWR pin.

Table 60-16. Motorola 68K/Intel 8080 Write Configuration

Register	Value	Comments
SHIFTCFG0...7	0x000F_0100	Configure 16-bit parallel shift in from adjacent shifter.
SHIFTCTL0	0x0003_0002	Configure transmit using Timer 0 on posedge of clock with data output to FXIO_D[15:0].
SHIFTCTL1...7	0x0000_0002	Configure transmit using Timer 0 on posedge of clock.
TIMCMP0	0x0000_0001 (1-beat) 0x0000_1F01 (16-beats)	Configure 1 or 16-beat transfer with baud rate of divide by 4 of the FlexIO clock. Set TIMCMP[15:8] = (number of beats x 2) - 1. Set TIMCMP[7:0] = (baud rate divider / 2) - 1.

Table continues on the next page...

Table 60-16. Motorola 68K/Intel 8080 Write Configuration (continued)

Register	Value	Comments
TIMCFG0	0x0000_2200	Configure enable on trigger high and disable on compare. Timer output high on enable.
TIMCTL0	0x01C3_1001 (1-beat) 0x1DC3_1001 (16-beats)	Configure dual 8-bit counter using FXIO_D[16] output (EN pin for 68K, WR pin for 8080), with Shifter 0 (1-beat) or Shifter 7 (16-beats) flag as the inverted trigger.
SHIFTBUF0...7	Data to transmit	Transmit data can be written to SHIFTBUF0 (1-beat) or SHIFTBUF0...7 (16-beats) to initiate a transfer, use the Shifter Status Flag to indicate when data can be written using interrupt or DMA request.

Table 60-17. Motorola 68K/Intel 8080 Read Configuration

Register	Value	Comments
SHIFTCFG0...6	0x000F_0100	Configure 16-bit parallel shift in from adjacent shifter.
SHIFTCFG7	0x000F_0000	Configure 16-bit parallel shift in from pin.
SHIFTCTL0...7	0x0080_0001	Configure receive using Timer 0 on negedge of clock with data input from FXIO_D[15:0].
TIMCMP0	0x0000_0001 (1-beat) 0x0000_1F01 (16-beats)	Configure 1 or 16-beat transfer with baud rate of divide by 4 of the FlexIO clock. Set TIMCMP[15:8] = (number of beats x 2) - 1. Set TIMCMP[7:0] = (baud rate divider / 2) - 1.
TIMCFG0	0x0000_2200	Configure enable on trigger high and disable on compare. Timer output high on enable.
TIMCTL0	0x01C3_1101 (Intel 8080) 0x01C3_1001 (Motorola 68K)	Configure dual 8-bit counter using either FXIO_D[16] output (EN pin for 68K) or FXIO_D[17] output (RD pin for 8080), with Shifter 0 flag as the inverted trigger.
SHIFTBUF0...7	Data received	Received data can be read from SHIFTBUF0 (1-beat) or SHIFTBUF0...7 (16-beats), use the Shifter Status Flag to indicate when data can be read using interrupt or DMA request.

In general, any operation to a 68K/8080 bus slave will begin with a register write cycle followed by one or more data read or write cycles. To accomplish this, the following program flow should be used:

1. Configure FlexIO with 1-beat write configuration
2. Configure GPIO to assert nCS, RS pins (and deassert RDWR pin for 68K)

3. Write register index data to SHIFTBUF0[15:0]
4. Configure GPIO to deassert RS pin (and assert RDWR pin for 68K data read)
5. Configure FlexIO with desired read or write configuration (e.g. 1 or 16-beats)
6. Use the Shifter Status Flag to trigger interrupt or DMA driven data transfers to/from SHIFTBUF registers
7. Configure GPIO to deassert nCS pin

60.5.10 State Machine Example

The configuration below details a hypothetical state machine example to illustrate the flexibility allowed when using Shifter state mode. In this example, FlexIO waits for the FXIO_D[2] pin to assert and then drives a complementary square wave output at a frequency of FLEXIO_CLK/131072 on the FXIO_D[1:0] pins while the comparator output is asserted (assumes comparator is connected to external trigger 15). The state diagram below shows the states and transitions implemented by this example.

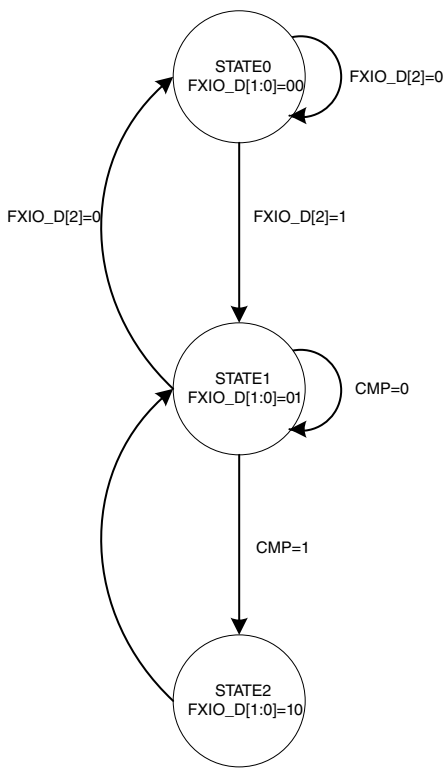


Figure 60-5. Example State Diagram

Table 60-18. State Machine Configuration

Register	Value	Comments
SHIFTCFG0...2	0x0000_0003	Enable FXIO_D[1:0] as outputs.
SHIFTCTL0	0x0080_0206	Configure for State mode using FXIO_D[4:2] as inputs to select next state and Timer0 output low to trigger next state.
SHIFTBUF0	0x0020_8208	State0: Drive FXIO_D[1:0]=00, transition to State0 if FXIO_D[2]=0, State1 if FXIO_D[2]=1.
SHIFTCTL1	0x0000_0206	Configure for State mode using FXIO_D[4:2] as inputs to select next state and Timer0 output high to trigger next state.
SHIFTBUF1	0x0140_8408	State1: Drive FXIO_D[1:0]=01, transition to State0 if FXIO_D[2]=0, State1 if CMP=0, State2 if CMP=1 (FXIO_D[3]=1)
SHIFTCTL2	0x0080_0206	Configure for State mode using FXIO_D[4:2] as inputs to select next state and Timer0 output low to trigger next state.
SHIFTBUF2	0x0224_9249	State2: Drive FXIO_D[1:0]=10, transition to State1 when Timer0 output low
TIMCMP0	0x0000_FFFF	Configure baud rate of divide by 131072 of the FlexIO clock. Set TIMCMP[7:0] = (baud rate divider / 2) - 1.
TIMCFG0	0x0000_0000	Configure timer always enabled.
TIMCTL0	0x0000_0003	Configure single 16-bit counter.
TIMCFG1	0x0010_7600	Configure timer enabled on trigger rising edge, disabled on trigger falling edge, decrement on trigger edge.
TIMCTL1	0x0F03_0303	Configure timer output enabled on FXIO_D[3], external trigger 15 (comparator output) selected.

Chapter 61
Integrated Interchip Sound (I2S) / Synchronous Audio Interface (SAI)

61.1 Chip-specific I2S/SAI information

61.1.1 Instantiation information

This device contains 1 I^2S module.

As configured on the device, module features include:

- TX data lines: 2
- RX data lines: 2
- FIFO size (words): 8
- Maximum words per frame: 32
- Maximum bit clock divider: 512

61.1.2 Features

- I2S, TDM, AC97, CODEC, DSP interfaces

- Transmit and Receive can operate asynchronously or synchronously
- Multiple SAI can be synchronized

- Asynchronous FIFO design eliminates Bit Clock / Bus Clock restrictions
- Supports operation in back-biased run mode with 1 MHz Bus Clock
- Supports operation in Stop mode from external bit clock or audio clock
- Asynchronous interrupt can generate wakeup for CPU from Stop mode
- Graceful shut-down when not configured to operate in Stop mode

- Supports 8-bit to 32-bit data word
- Bits per Word configured separately for first word in frame (AC97)

- Supports MSB or LSB first plus word alignment in FIFO is configurable
- Double-buffered word mask register can mask any word in the frame

- Configurable width and data alignment (one bit early or with first bit)
- Frame Sync Error flag and interrupt supported with external frame sync
- Word Start flag and interrupt can trigger at start of any word in frame

- Fully configurable FIFO Watermark generates Interrupt or DMA request
- Stereo 16-bit data can be packed into one 32-bit FIFO word
- Graceful restart on Frame boundary after FIFO overflow/underflow

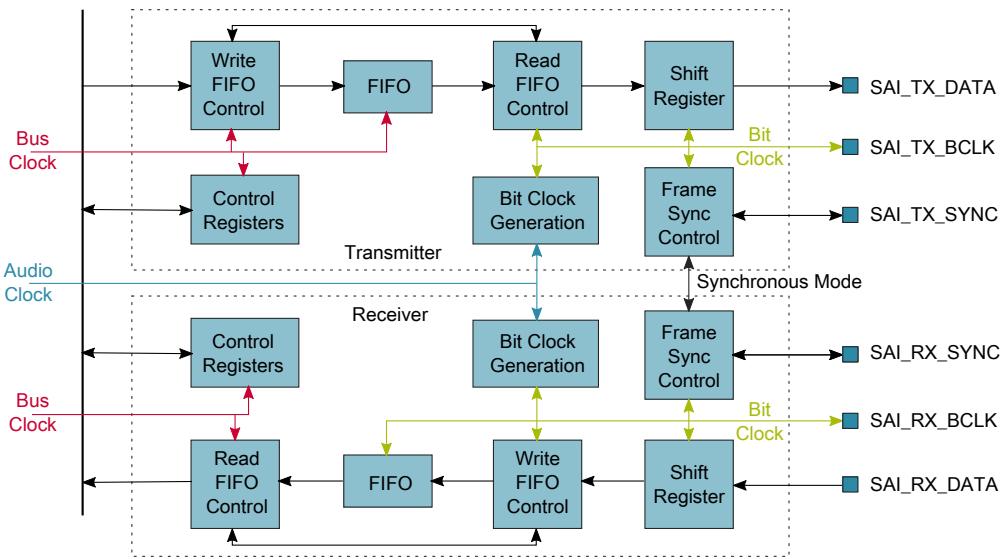


Figure 61-1. SAI Clock and Block Diagram

61.1.3 I²S/SAI clocking

61.1.3.1 Audio Master Clock

The audio master clock (MCLK) is used to generate the bit clock when the receiver or transmitter is configured for an internally generated bit clock. The audio master clock can also be output to or input from a pin. The transmitter and receiver have the same audio master clock inputs.

61.1.3.2 Bit Clock

The I^{2}S/SAI transmitter and receiver support asynchronous bit clocks (BCLKs) that can be generated internally from the audio master clock or supplied externally. The module also supports the option for synchronous operation between the receiver and transmitter product or between two separate I^{2}S/SAI peripherals.

61.1.3.3 Bus Clock

The bus clock is used by the control registers and to generate synchronous interrupts and DMA requests.

61.1.3.4 I^{2}S/SAI clock generation

Each SAI peripheral can control the input clock selection, pin direction and divide ratio of one audio master clock.

The MCLK Input Clock Select bit of the MCLK Control Register (MCR[MICS]) selects the clock input to the I^{2}S/SAI module's MCLK divider.

The following table shows the input clock selection options on this device.

Table 61-1. I2S0 MCLK input clock selection

MCR[MICS]	Clock Selection
00	System clock
01	OSC0ERCLK
10	Not supported
11	MCGPLLCLK or MCGFLLCLK

The module's MCLK Divide Register (MDR) configures the MCLK divide ratio.

The module's MCLK Output Enable bit of the MCLK Control Register (MCR[MOE]) controls the direction of the MCLK pin. The pin is the input from the pin when MOE is 0, and the pin is the output from the clock divider when MOE is 1.

The transmitter and receiver can independently select between the bus clock and the audio master clocks to generate the bit clock. Each module's Clocking Mode field of the Transmit Configuration 2 Register and Receive Configuration 2 Register (TCR2[MSEL] and RCR2[MSEL]) selects the master clock.

The following table shows the TCR2[MSEL] and RCR2[MSEL] field settings for this device.

Table 61-2. I2S0 master clock settings

TCR2[MSEL], RCR2[MSEL]	Master Clock
00	Bus Clock
01	I2S0_MCLK
10	Not supported
11	Not supported

61.1.3.5 Clock gating and I²S/SAI initialization

The clock to the I²S/SAI module can be gated using a bit in the SIM. To minimize power consumption, these bits are cleared after any reset, which disables the clock to the corresponding module. The clock enable bit should be set by software at the beginning of the module initialization routine to enable the module clock before initialization of any of the I²S/SAI registers.

61.1.4 I²S/SAI operation in low power modes

61.1.4.1 Stop and very low power modes

In Stop mode, the SAI transmitter and/or receiver can continue operating provided the appropriate Stop Enable bit is set (TCSR[STOPE] and/or RCSR[STOPE], respectively), and provided the transmitter and/or receiver is/are using an externally generated bit clock or an Audio Master Clock that remains operating in Stop mode. The SAI transmitter and/or receiver can generate an asynchronous interrupt to wake the CPU from Stop mode.

In VLPS mode, the module behaves as it does in stop mode if VLPS mode is entered from run mode. However, if VLPS mode is entered from VLPR mode, the FIFO might underflow or overflow before wakeup from stop mode due to the limits in bus bandwidth. In VLPW and VLPR modes, the module is limited by the maximum bus clock frequencies.

When operating from an internally generated bit clock or Audio Master Clock that is disabled in stop modes:

In Stop mode, if the Transmitter Stop Enable (TCSR[STOPE]) bit is clear, the transmitter is disabled after completing the current transmit frame, and, if the Receiver Stop Enable (RCSR[STOPE]) bit is clear, the receiver is disabled after completing the current receive frame. Entry into Stop mode is prevented–not acknowledged–while waiting for the transmitter and receiver to be disabled at the end of the current frame.

61.1.4.2 Low-leakage modes

When entering low-leakage modes, the Stop Enable (TCSR[STOPE] and RCSR[STOPE]) bits are ignored and the SAI is disabled after completing the current transmit and receive Frames. Entry into stop mode is prevented (not acknowledged) while waiting for the transmitter and receiver to be disabled at the end of the current frame.

61.2 Introduction

The I^2S (or I2S) module provides a synchronous audio interface (SAI) that supports full-duplex serial interfaces with frame synchronization such as I^2S, AC97, TDM, and codec/DSP interfaces.

61.2.1 Features

Note that some of the features are not supported across all SAI instances; see the chip-specific information in the first section of this chapter.

- Transmitter with independent bit clock and frame sync supporting 2 data lines
- Receiver with independent bit clock and frame sync supporting 2 data lines
- Maximum Frame Size of 32 words
- Word size of between 8-bits and 32-bits
- Word size configured separately for first word and remaining words in frame
- Asynchronous 8 × 32-bit FIFO for each transmit and receive channel
- Supports graceful restart after FIFO error
- Supports automatic restart after FIFO error without software intervention
- Supports packing of 8-bit and 16-bit data into each 32-bit FIFO word
- Supports combining multiple data channel FIFOs into single data channel FIFO

61.2.2 Block diagram

The following block diagram also shows the module clocks.

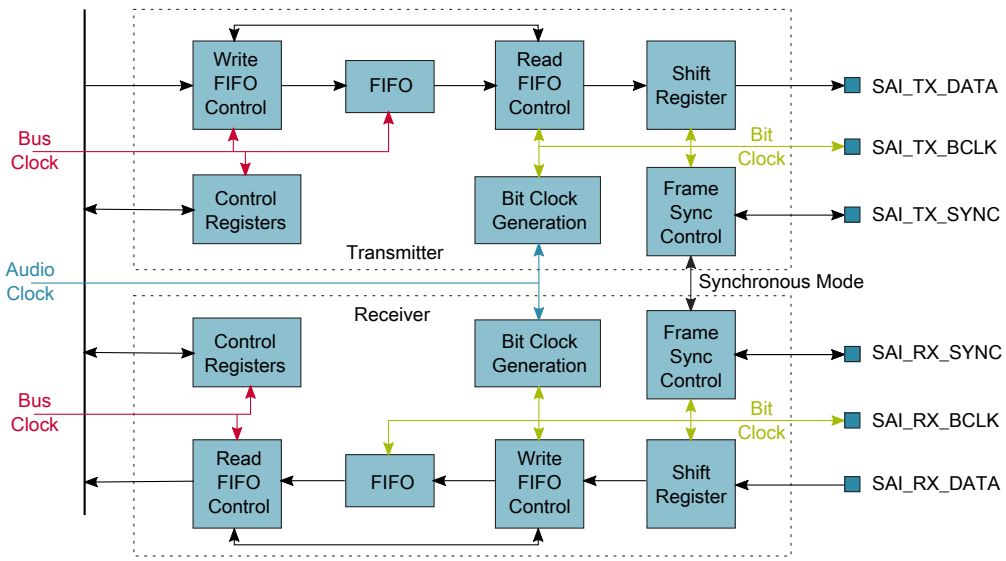


Figure 61-2. I²S/SAI block diagram

61.2.3 Modes of operation

The module operates in these power modes: Run mode, stop modes, low-leakage modes, and Debug mode.

61.2.3.1 Run mode

In Run mode, the SAI transmitter and receiver operate normally.

61.2.3.2 Stop modes

In Stop mode, the SAI transmitter and/or receiver can continue operating provided the appropriate Stop Enable bit is set (TCSR[STOPE] and/or RCSR[STOPE], respectively), and provided the transmitter and/or receiver is/are using an externally generated bit clock or an Audio Master Clock that remains operating in Stop mode. The SAI transmitter and/or receiver can generate an asynchronous interrupt to wake the CPU from Stop mode.

In Stop mode, if the Transmitter Stop Enable (TCSR[STOPE]) bit is clear, the transmitter is disabled after completing the current transmit frame, and, if the Receiver Stop Enable (RCSR[STOPE]) bit is clear, the receiver is disabled after completing the current receive frame. Entry into Stop mode is prevented–not acknowledged–while waiting for the transmitter and receiver to be disabled at the end of the current frame.

61.2.3.3 Low-leakage modes

When entering low-leakage modes, the Stop Enable (TCSR[STOPE] and RCSR[STOPE]) bits are ignored and the SAI is disabled after completing the current transmit and receive Frames. Entry into stop mode is prevented (not acknowledged) while waiting for the transmitter and receiver to be disabled at the end of the current frame.

61.2.3.4 Debug mode

In Debug mode, the SAI transmitter and/or receiver can continue operating provided the Debug Enable bit is set. When TCSR[DBGE] or RCSR[DBGE] bit is clear and Debug mode is entered, the SAI is disabled after completing the current transmit or receive frame. The transmitter and receiver bit clocks are not affected by Debug mode.

61.3 External signals

Name	Function	I/O
SAI_TX_BCLK	Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_TX_SYNC	Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_TX_DATA[1:0]	Transmit Data. The transmit data is generated synchronously by the bit clock and is tristated whenever not transmitting a word.	O
SAI_RX_BCLK	Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_RX_SYNC	Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when	I/O

Table continues on the next page...

Name	Function	I/O
	externally generated and an output generated synchronously by the bit clock when internally generated.	
SAI_RX_DATA[1:0]	Receive Data. The receive data is sampled synchronously by the bit clock.	I
SAI_MCLK	Audio Master Clock. The master clock is an input when externally generated and an output when internally generated.	I/O

61.4 Memory map and register definition

A read or write access to an address from offset 0x108 and above will result in a bus error.

I2S memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4002_F000	SAI Transmit Control Register (I2S0_TCSR)	32	R/W	0000_0000h	61.4.1/2020
4002_F004	SAI Transmit Configuration 1 Register (I2S0_TCR1)	32	R/W	0000_0000h	61.4.2/2023
4002_F008	SAI Transmit Configuration 2 Register (I2S0_TCR2)	32	R/W	0000_0000h	61.4.3/2023
4002_F00C	SAI Transmit Configuration 3 Register (I2S0_TCR3)	32	R/W	0000_0000h	61.4.4/2025
4002_F010	SAI Transmit Configuration 4 Register (I2S0_TCR4)	32	R/W	0000_0000h	61.4.5/2026
4002_F014	SAI Transmit Configuration 5 Register (I2S0_TCR5)	32	R/W	0000_0000h	61.4.6/2028
4002_F020	SAI Transmit Data Register (I2S0_TDR0)	32	W (always reads 0)	0000_0000h	61.4.7/2029
4002_F024	SAI Transmit Data Register (I2S0_TDR1)	32	W (always reads 0)	0000_0000h	61.4.7/2029
4002_F040	SAI Transmit FIFO Register (I2S0_TFR0)	32	R	0000_0000h	61.4.8/2029
4002_F044	SAI Transmit FIFO Register (I2S0_TFR1)	32	R	0000_0000h	61.4.8/2029
4002_F060	SAI Transmit Mask Register (I2S0_TMR)	32	R/W	0000_0000h	61.4.9/2030
4002_F080	SAI Receive Control Register (I2S0_RCSR)	32	R/W	0000_0000h	61.4.10/ 2031
4002_F084	SAI Receive Configuration 1 Register (I2S0_RCR1)	32	R/W	0000_0000h	61.4.11/ 2034
4002_F088	SAI Receive Configuration 2 Register (I2S0_RCR2)	32	R/W	0000_0000h	61.4.12/ 2034
4002_F08C	SAI Receive Configuration 3 Register (I2S0_RCR3)	32	R/W	0000_0000h	61.4.13/ 2036
4002_F090	SAI Receive Configuration 4 Register (I2S0_RCR4)	32	R/W	0000_0000h	61.4.14/ 2037

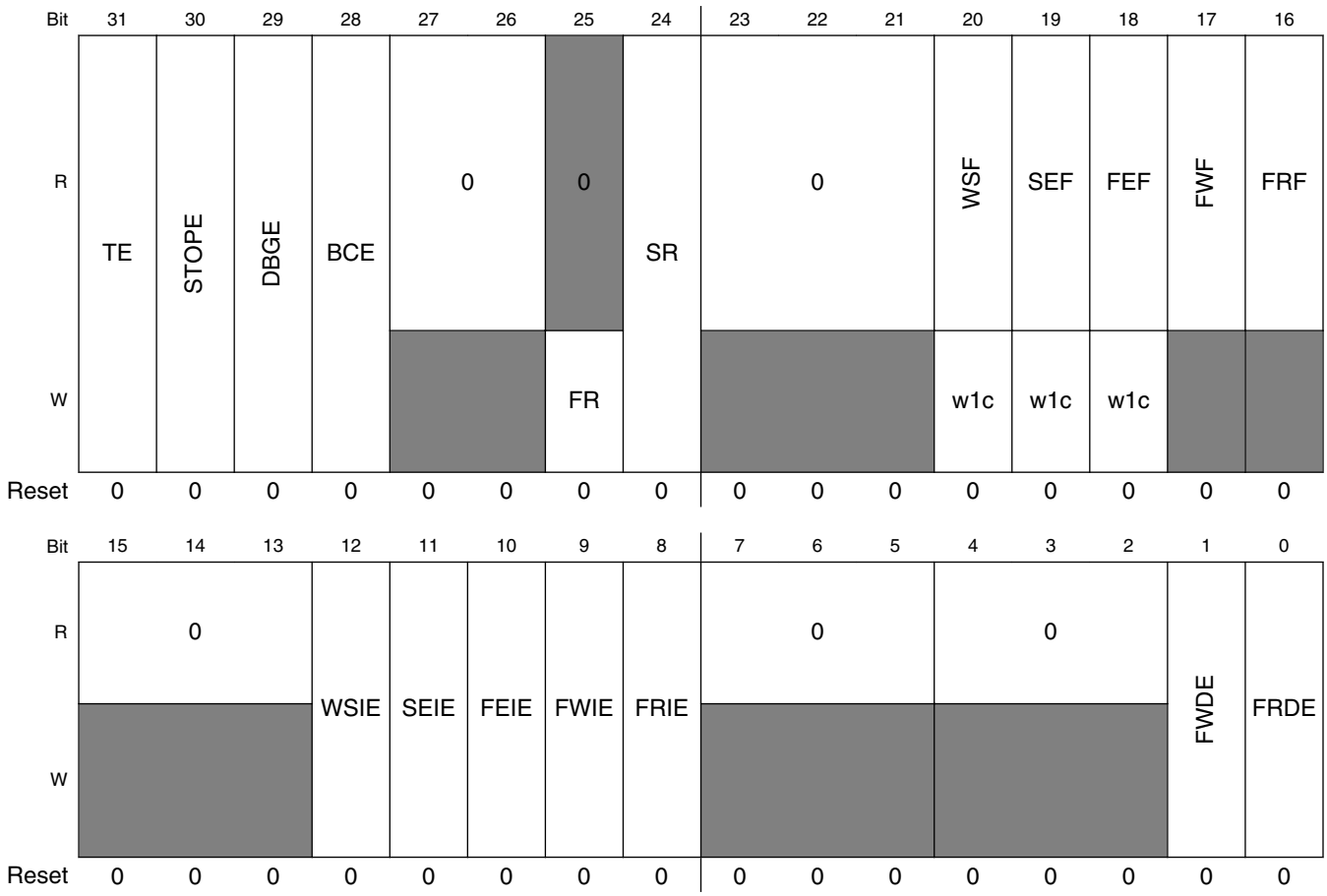
Table continues on the next page...

I2S memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4002_F094	SAI Receive Configuration 5 Register (I2S0_RCR5)	32	R/W	0000_0000h	61.4.15/ 2039
4002_F0A0	SAI Receive Data Register (I2S0_RDR0)	32	R	0000_0000h	61.4.16/ 2040
4002_F0A4	SAI Receive Data Register (I2S0_RDR1)	32	R	0000_0000h	61.4.16/ 2040
4002_F0C0	SAI Receive FIFO Register (I2S0_RFR0)	32	R	0000_0000h	61.4.17/ 2040
4002_F0C4	SAI Receive FIFO Register (I2S0_RFR1)	32	R	0000_0000h	61.4.17/ 2040
4002_F0E0	SAI Receive Mask Register (I2S0_RMR)	32	R/W	0000_0000h	61.4.18/ 2041
4002_F100	SAI MCLK Control Register (I2S0_MCR)	32	R/W	0000_0000h	61.4.19/ 2042
4002_F104	SAI MCLK Divide Register (I2S0_MDR)	32	R/W	0000_0000h	61.4.20/ 2043

61.4.1 SAI Transmit Control Register (I2Sx_TCSR)

Address: 4002_F000h base + 0h offset = 4002_F000h



I2Sx_TCSR field descriptions

Field	Description
31 TE	Transmitter Enable Enables/disables the transmitter. When software clears this field, the transmitter remains enabled, and this bit remains set, until the end of the current frame. 0 Transmitter is disabled. 1 Transmitter is enabled, or transmitter has been disabled and has not yet reached end of frame.
30 STOPE	Stop Enable Configures transmitter operation in Stop mode. This field is ignored and the transmitter is disabled in all low-leakage stop modes. 0 Transmitter disabled in Stop mode. 1 Transmitter enabled in Stop mode.
29 DBGE	Debug Enable

Table continues on the next page...

I2Sx_TCSR field descriptions (continued)

Field	Description
	Enables/disables transmitter operation in Debug mode. The transmit bit clock is not affected by debug mode. 0 Transmitter is disabled in Debug mode, after completing the current frame. 1 Transmitter is enabled in Debug mode.
28 BCE	Bit Clock Enable Enables the transmit bit clock, separately from the TE. This field is automatically set whenever TE is set. When software clears this field, the transmit bit clock remains enabled, and this bit remains set, until the end of the current frame. 0 Transmit bit clock is disabled. 1 Transmit bit clock is enabled.
27–26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25 FR	FIFO Reset Resets the FIFO pointers. Reading this field will always return zero. FIFO pointers should only be reset when the transmitter is disabled or the FIFO error flag is set. 0 No effect. 1 FIFO reset.
24 SR	Software Reset When set, resets the internal transmitter logic including the FIFO pointers. Software-visible registers are not affected, except for the status registers. 0 No effect. 1 Software reset.
23–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20 WSF	Word Start Flag Indicates that the start of the configured word has been detected. Write a logic 1 to this field to clear this flag. 0 Start of word not detected. 1 Start of word detected.
19 SEF	Sync Error Flag Indicates that an error in the externally-generated frame sync has been detected. Write a logic 1 to this field to clear this flag. 0 Sync error not detected. 1 Frame sync error detected.
18 FEF	FIFO Error Flag Indicates that an enabled transmit FIFO has underrun. Write a logic 1 to this field to clear this flag. 0 Transmit underrun not detected. 1 Transmit underrun detected.

Table continues on the next page...

I2Sx_TCSR field descriptions (continued)

Field	Description
17 FWF	FIFO Warning Flag Indicates that an enabled transmit FIFO is empty. 0 No enabled transmit FIFO is empty. 1 Enabled transmit FIFO is empty.
16 FRF	FIFO Request Flag Indicates that the number of words in an enabled transmit channel FIFO is less than or equal to the transmit FIFO watermark. 0 Transmit FIFO watermark has not been reached. 1 Transmit FIFO watermark has been reached.
15–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12 WSIE	Word Start Interrupt Enable Enables/disables word start interrupts. 0 Disables interrupt. 1 Enables interrupt.
11 SEIE	Sync Error Interrupt Enable Enables/disables sync error interrupts. 0 Disables interrupt. 1 Enables interrupt.
10 FEIE	FIFO Error Interrupt Enable Enables/disables FIFO error interrupts. 0 Disables the interrupt. 1 Enables the interrupt.
9 FWIE	FIFO Warning Interrupt Enable Enables/disables FIFO warning interrupts. 0 Disables the interrupt. 1 Enables the interrupt.
8 FRIE	FIFO Request Interrupt Enable Enables/disables FIFO request interrupts. 0 Disables the interrupt. 1 Enables the interrupt.
7–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 FWDE	FIFO Warning DMA Enable

Table continues on the next page...

I2Sx_TCSR field descriptions (continued)

Field	Description
	Enables/disables DMA requests. 0 Disables the DMA request. 1 Enables the DMA request.
0 FRDE	FIFO Request DMA Enable Enables/disables DMA requests. 0 Disables the DMA request. 1 Enables the DMA request.

61.4.2 SAI Transmit Configuration 1 Register (I2Sx_TCR1)

Address: 4002_F000h base + 4h offset = 4002_F004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																													TFW		
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

I2Sx_TCR1 field descriptions

Field	Description
31–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
TFW	Transmit FIFO Watermark Configures the watermark level for all enabled transmit channels.

61.4.3 SAI Transmit Configuration 2 Register (I2Sx_TCR2)

This register must not be altered when TCSR[TE] is set.

Address: 4002_F000h base + 8h offset = 4002_F008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	SYNC		BCS	BCI	MSEL		BCP	BCD	0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								DIV							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

I2Sx_TCR2 field descriptions

Field	Description
31–30 SYNC	Synchronous Mode Configures between asynchronous and synchronous modes of operation. When configured for a synchronous mode of operation, the receiver must be configured for asynchronous operation. 00 Asynchronous mode. 01 Synchronous with receiver. 10 Synchronous with another SAI transmitter. 11 Synchronous with another SAI receiver.
29 BCS	Bit Clock Swap This field swaps the bit clock used by the transmitter. When the transmitter is configured in asynchronous mode and this bit is set, the transmitter is clocked by the receiver bit clock (SAI_RX_BCLK). This allows the transmitter and receiver to share the same bit clock, but the transmitter continues to use the transmit frame sync (SAI_TX_SYNC). When the transmitter is configured in synchronous mode, the transmitter BCS field and receiver BCS field must be set to the same value. When both are set, the transmitter and receiver are both clocked by the transmitter bit clock (SAI_TX_BCLK) but use the receiver frame sync (SAI_RX_SYNC). 0 Use the normal bit clock source. 1 Swap the bit clock source.
28 BCI	Bit Clock Input When this field is set and using an internally generated bit clock in either synchronous or asynchronous mode, the bit clock actually used by the transmitter is delayed by the pad output delay (the transmitter is clocked by the pad input as if the clock was externally generated). This has the effect of decreasing the data input setup time, but increasing the data output valid time. The slave mode timing from the datasheet should be used for the transmitter when this bit is set. In synchronous mode, this bit allows the transmitter to use the slave mode timing from the datasheet, while the receiver uses the master mode timing. This field has no effect when configured for an externally generated bit clock . 0 No effect. 1 Internal logic is clocked as if bit clock was externally generated.
27–26 MSEL	MCLK Select Selects the audio Master Clock option used to generate an internally generated bit clock. This field has no effect when configured for an externally generated bit clock. **NOTE:** Depending on the device, some Master Clock options might not be available. See the chip-specific information for the meaning of each option. 00 Bus Clock selected. 01 Master Clock (MCLK) 1 option selected. 10 Master Clock (MCLK) 2 option selected. 11 Master Clock (MCLK) 3 option selected.
25 BCP	Bit Clock Polarity Configures the polarity of the bit clock. 0 Bit clock is active high with drive outputs on rising edge and sample inputs on falling edge. 1 Bit clock is active low with drive outputs on falling edge and sample inputs on rising edge.

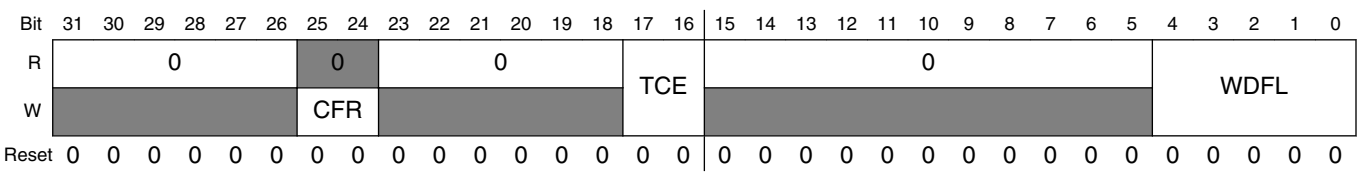
Table continues on the next page...

I2Sx_TCR2 field descriptions (continued)

Field	Description
24 BCD	Bit Clock Direction Configures the direction of the bit clock. 0 Bit clock is generated externally in Slave mode. 1 Bit clock is generated internally in Master mode.
23–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
DIV	Bit Clock Divide Divides down the audio master clock to generate the bit clock when configured for an internal bit clock. The division value is (DIV + 1) * 2.

61.4.4 SAI Transmit Configuration 3 Register (I2Sx_TCR3)

Address: 4002_F000h base + Ch offset = 4002_F00Ch



I2Sx_TCR3 field descriptions

Field	Description
31–26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25–24 CFR	Channel FIFO Reset Resets the FIFO pointers for a specific channel. Reading this field will always return zero. FIFO pointers should only be reset when a channel is disabled or the FIFO error flag is set. 0 No effect. 1 Transmit data channel N FIFO is reset.
23–18 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
17–16 TCE	Transmit Channel Enable Enables the corresponding data channel for transmit operation. A channel must be enabled before its FIFO is accessed. Changing this field will take effect immediately for generating the FIFO request and warning flags, but at the end of each frame for transmit operation. 0 Transmit data channel N is disabled. 1 Transmit data channel N is enabled.
15–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
WDFL	Word Flag Configuration

Table continues on the next page...

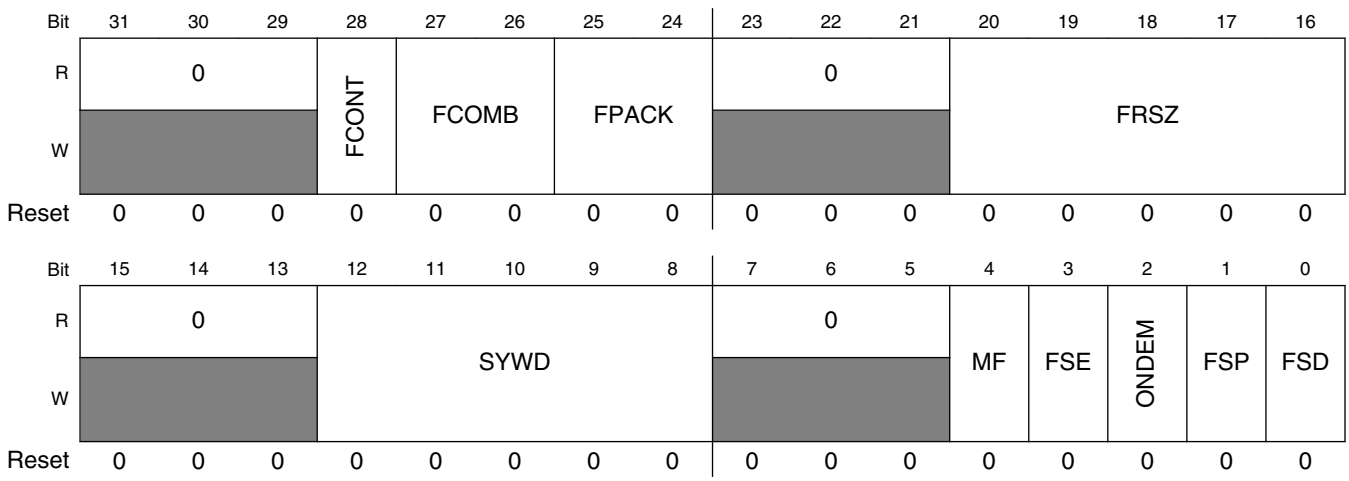
I2Sx_TCR3 field descriptions (continued)

Field	Description
	Configures which word sets the start of word flag. The value written must be one less than the word number. For example, writing 0 configures the first word in the frame. When configured to a value greater than TCR4[FRSZ], then the start of word flag is never set.

61.4.5 SAI Transmit Configuration 4 Register (I2Sx_TCR4)

This register must not be altered when TCSR[TE] is set.

Address: 4002_F000h base + 10h offset = 4002_F010h



I2Sx_TCR4 field descriptions

Field	Description
31–29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28 FCONT	FIFO Continue on Error Configures when the SAI will continue transmitting after a FIFO error has been detected. 0 On FIFO error, the SAI will continue from the start of the next frame after the FIFO error flag has been cleared. 1 On FIFO error, the SAI will continue from the same word that caused the FIFO error to set after the FIFO warning flag has been cleared.
27–26 FCOMB	FIFO Combine Mode When FIFO combine mode is enabled for FIFO writes, software writing to any FIFO data register will alternate the write among the enabled data channel FIFOs. For example, if two data channels are enabled then the first write will be performed to the first enabled data channel FIFO and the second write will be performed to the second enabled data channel FIFO. Reseting the FIFO or disabling FIFO combine mode for FIFO writes will reset the pointer back to the first enabled data channel. When FIFO combine mode is enabled for FIFO reads from the transmit shift registers, the transmit data channel output will alternate between the enabled data channel FIFOs. For example, if two data channels are enabled then the first unmasked word will be transmitted from the first enabled data channel FIFO and

Table continues on the next page...

I2Sx_TCR4 field descriptions (continued)

Field	Description
	the second unmasked word will be transmitted from the second enabled data channel FIFO. Since the first word of the frame is always transmitted from the first enabled data channel FIFO, it is recommended that the number of unmasked words per frame is evenly divisible by the number of enabled data channels. 00 FIFO combine mode disabled. 01 FIFO combine mode enabled on FIFO reads (from transmit shift registers). 10 FIFO combine mode enabled on FIFO writes (by software). 11 FIFO combine mode enabled on FIFO reads (from transmit shift registers) and writes (by software).
25–24 FPACK	FIFO Packing Mode Enables packing of 8-bit data or 16-bit data into each 32-bit FIFO word. If the word size is greater than 8-bit or 16-bit then only the first 8-bit or 16-bits are loaded from the FIFO. The first word in each frame always starts with a new 32-bit FIFO word and the first bit shifted must be configured within the first packed word. When FIFO packing is enabled, the FIFO write pointer will only increment when the full 32-bit FIFO word has been written by software. 00 FIFO packing is disabled 01 Reserved 10 8-bit FIFO packing is enabled 11 16-bit FIFO packing is enabled
23–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20–16 FRSZ	Frame size Configures the number of words in each frame. The value written must be one less than the number of words in the frame. For example, write 0 for one word per frame. The maximum supported frame size is 32 words.
15–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12–8 SYWD	Sync Width Configures the length of the frame sync in number of bit clocks. The value written must be one less than the number of bit clocks. For example, write 0 for the frame sync to assert for one bit clock only. The sync width cannot be configured longer than the first word of the frame.
7–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 MF	MSB First Configures whether the LSB or the MSB is transmitted first. 0 LSB is transmitted first. 1 MSB is transmitted first.
3 FSE	Frame Sync Early 0 Frame sync asserts with the first bit of the frame. 1 Frame sync asserts one bit before the first bit of the frame.
2 ONDEM	On Demand Mode When set, and the frame sync is generated internally, a frame sync is only generated when the FIFO warning flag is clear.

Table continues on the next page...

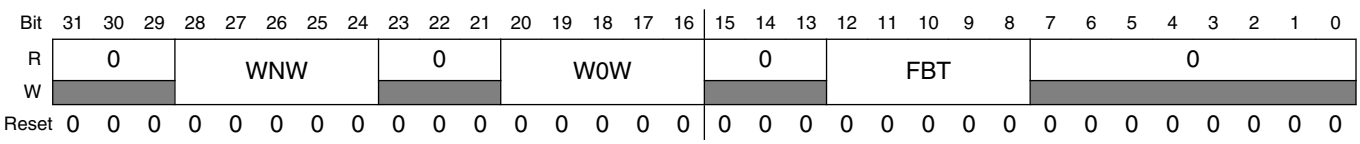
I2Sx_TCR4 field descriptions (continued)

Field	Description
	0 Internal frame sync is generated continuously. 1 Internal frame sync is generated when the FIFO warning flag is clear.
1 FSP	Frame Sync Polarity Configures the polarity of the frame sync. 0 Frame sync is active high. 1 Frame sync is active low.
0 FSD	Frame Sync Direction Configures the direction of the frame sync. 0 Frame sync is generated externally in Slave mode. 1 Frame sync is generated internally in Master mode.

61.4.6 SAI Transmit Configuration 5 Register (I2Sx_TCR5)

This register must not be altered when TCSR[TE] is set.

Address: 4002_F000h base + 14h offset = 4002_F014h



I2Sx_TCR5 field descriptions

Field	Description
31–29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28–24 WNW	Word N Width Configures the number of bits in each word, for each word except the first in the frame. The value written must be one less than the number of bits per word. Word width of less than 8 bits is not supported.
23–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20–16 W0W	Word 0 Width Configures the number of bits in the first word in each frame. The value written must be one less than the number of bits in the first word. Word width of less than 8 bits is not supported if there is only one word per frame.
15–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12–8 FBT	First Bit Shifted Configures the bit index for the first bit transmitted for each word in the frame. If configured for MSB First, the index of the next bit transmitted is one less than the current bit transmitted. If configured for LSB First,

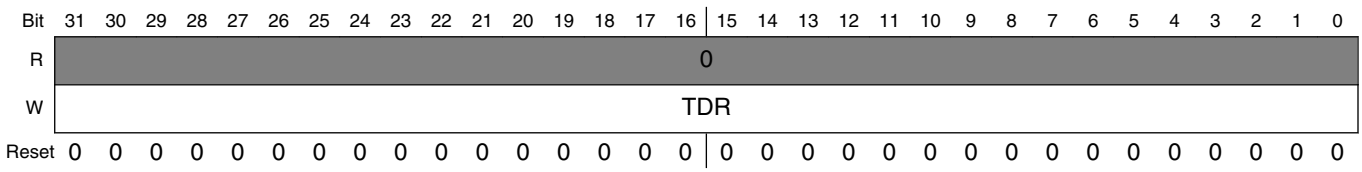
Table continues on the next page...

I2Sx_TCR5 field descriptions (continued)

Field	Description
	the index of the next bit transmitted is one more than the current bit transmitted. The value written must be greater than or equal to the word width when configured for MSB First. The value written must be less than or equal to 31-word width when configured for LSB First.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

61.4.7 SAI Transmit Data Register (I2Sx_TDR*n*)

Address: 4002_F000h base + 20h offset + (4d × i), where i=0d to 1d



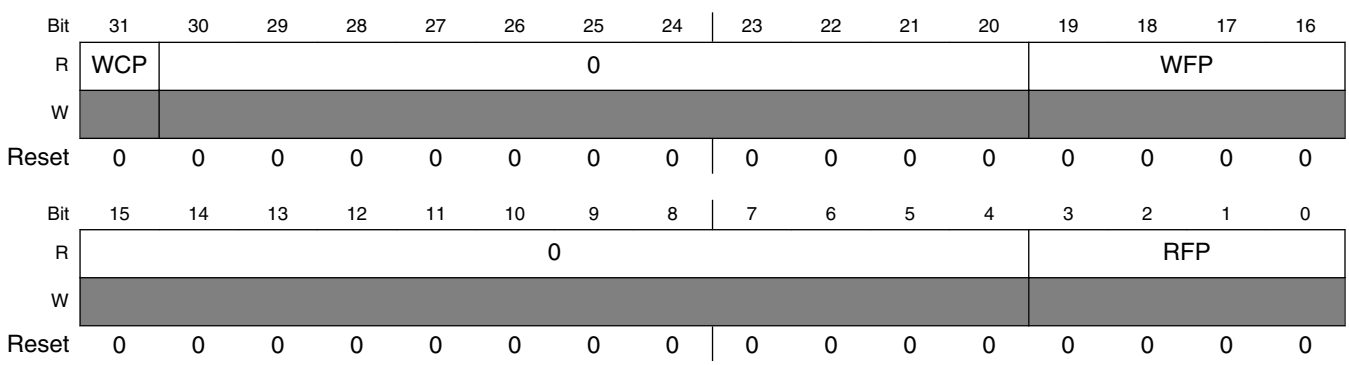
I2Sx_TDR*n* field descriptions

Field	Description
TDR	Transmit Data Register The corresponding TCR3[TCE] bit must be set before accessing the channel's transmit data register. Writes to this register when the transmit FIFO is not full will push the data written into the transmit data FIFO. Writes to this register when the transmit FIFO is full are ignored.

61.4.8 SAI Transmit FIFO Register (I2Sx_TFR*n*)

The MSB of the read and write pointers is used to distinguish between FIFO full and empty conditions. If the read and write pointers are identical, then the FIFO is empty. If the read and write pointers are identical except for the MSB, then the FIFO is full.

Address: 4002_F000h base + 40h offset + (4d × i), where i=0d to 1d



I2Sx_TFR*n* field descriptions

Field	Description
31 WCP	Write Channel Pointer When FIFO Combine mode is enabled for writes, indicates that this data channel is the next FIFO to be written. 0 No effect. 1 FIFO combine is enabled for FIFO writes and this FIFO will be written on the next FIFO write.
30–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–16 WFP	Write FIFO Pointer FIFO write pointer for transmit data channel.
15–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
RFP	Read FIFO Pointer FIFO read pointer for transmit data channel.

61.4.9 SAI Transmit Mask Register (I2Sx_TMR)

This register is double-buffered and updates:

1. When TCSR[TE] is first set
2. At the end of each frame.

This allows the masked words in each frame to change from frame to frame.

Address: 4002_F000h base + 60h offset = 4002_F060h

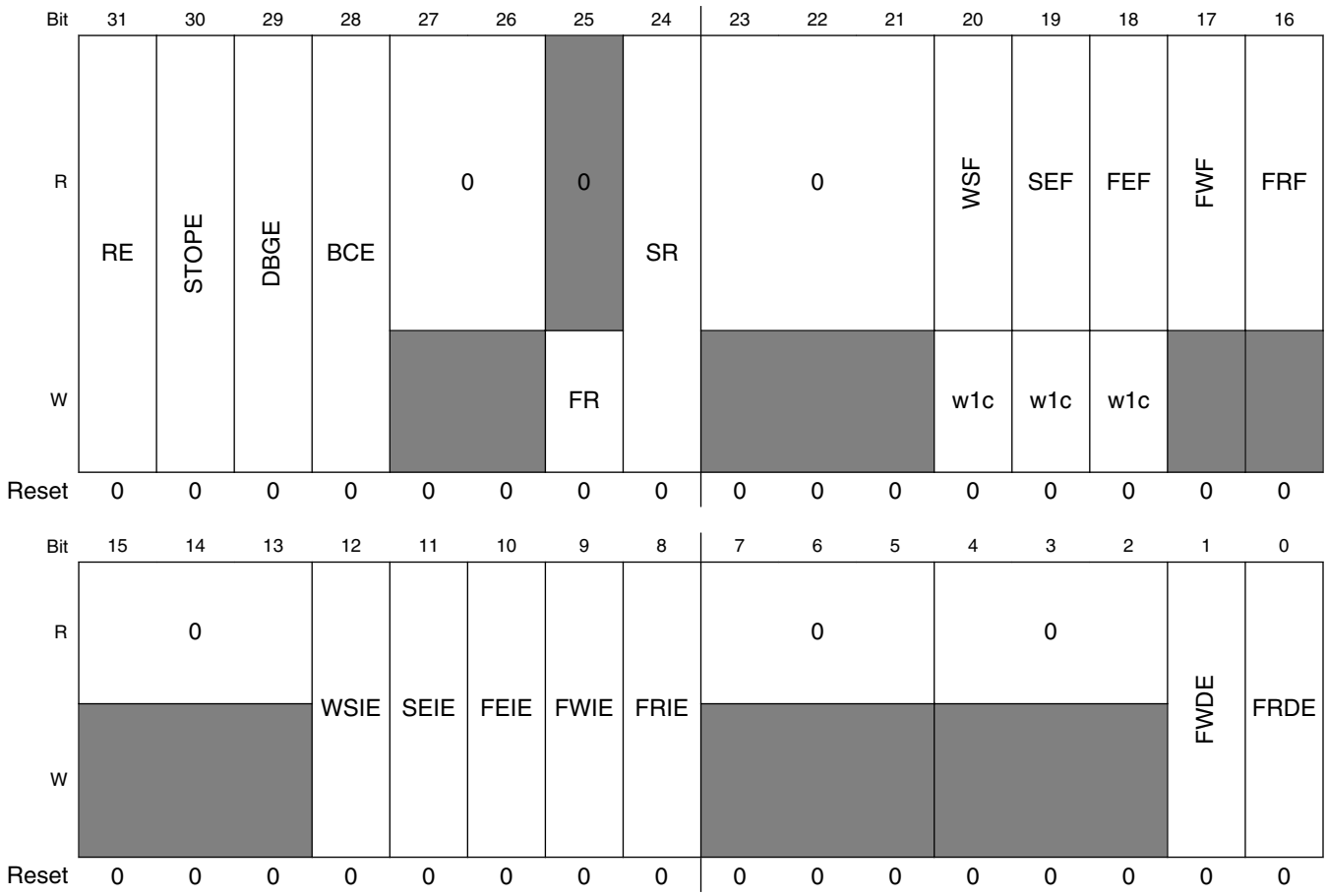
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	TWM																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

I2Sx_TMR field descriptions

Field	Description
TWM	Transmit Word Mask Configures whether the transmit word is masked (transmit data pin tristated and transmit data not read from FIFO) for the corresponding word in the frame. 0 Word N is enabled. 1 Word N is masked. The transmit data pins are tri-stated when masked.

61.4.10 SAI Receive Control Register (I2Sx_RCSR)

Address: 4002_F000h base + 80h offset = 4002_F080h



I2Sx_RCSR field descriptions

Field	Description
31 RE	Receiver Enable Enables/disables the receiver. When software clears this field, the receiver remains enabled, and this bit remains set, until the end of the current frame. 0 Receiver is disabled. 1 Receiver is enabled, or receiver has been disabled and has not yet reached end of frame.
30 STOPE	Stop Enable Configures receiver operation in Stop mode. This bit is ignored and the receiver is disabled in all low-leakage stop modes. 0 Receiver disabled in Stop mode. 1 Receiver enabled in Stop mode.
29 DBGE	Debug Enable

Table continues on the next page...

I2Sx_RCSR field descriptions (continued)

Field	Description
	Enables/disables receiver operation in Debug mode. The receive bit clock is not affected by Debug mode. 0 Receiver is disabled in Debug mode, after completing the current frame. 1 Receiver is enabled in Debug mode.
28 BCE	Bit Clock Enable Enables the receive bit clock, separately from RE. This field is automatically set whenever RE is set. When software clears this field, the receive bit clock remains enabled, and this field remains set, until the end of the current frame. 0 Receive bit clock is disabled. 1 Receive bit clock is enabled.
27–26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25 FR	FIFO Reset Resets the FIFO pointers. Reading this field will always return zero. FIFO pointers should only be reset when the receiver is disabled or the FIFO error flag is set. 0 No effect. 1 FIFO reset.
24 SR	Software Reset Resets the internal receiver logic including the FIFO pointers. Software-visible registers are not affected, except for the status registers. 0 No effect. 1 Software reset.
23–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20 WSF	Word Start Flag Indicates that the start of the configured word has been detected. Write a logic 1 to this field to clear this flag. 0 Start of word not detected. 1 Start of word detected.
19 SEF	Sync Error Flag Indicates that an error in the externally-generated frame sync has been detected. Write a logic 1 to this field to clear this flag. 0 Sync error not detected. 1 Frame sync error detected.
18 FEF	FIFO Error Flag Indicates that an enabled receive FIFO has overflowed. Write a logic 1 to this field to clear this flag. 0 Receive overflow not detected. 1 Receive overflow detected.
17 FWF	FIFO Warning Flag

Table continues on the next page...

I2Sx_RCSR field descriptions (continued)

Field	Description
	Indicates that an enabled receive FIFO is full. 0 No enabled receive FIFO is full. 1 Enabled receive FIFO is full.
16 FRF	FIFO Request Flag Indicates that the number of words in an enabled receive channel FIFO is greater than the receive FIFO watermark. 0 Receive FIFO watermark not reached. 1 Receive FIFO watermark has been reached.
15–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12 WSIE	Word Start Interrupt Enable Enables/disables word start interrupts. 0 Disables interrupt. 1 Enables interrupt.
11 SEIE	Sync Error Interrupt Enable Enables/disables sync error interrupts. 0 Disables interrupt. 1 Enables interrupt.
10 FEIE	FIFO Error Interrupt Enable Enables/disables FIFO error interrupts. 0 Disables the interrupt. 1 Enables the interrupt.
9 FWIE	FIFO Warning Interrupt Enable Enables/disables FIFO warning interrupts. 0 Disables the interrupt. 1 Enables the interrupt.
8 FRIE	FIFO Request Interrupt Enable Enables/disables FIFO request interrupts. 0 Disables the interrupt. 1 Enables the interrupt.
7–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 FWDE	FIFO Warning DMA Enable Enables/disables DMA requests.

Table continues on the next page...

I2Sx_RCSR field descriptions (continued)

Field	Description
	0 Disables the DMA request. 1 Enables the DMA request.
0 FRDE	FIFO Request DMA Enable Enables/disables DMA requests. 0 Disables the DMA request. 1 Enables the DMA request.

61.4.11 SAI Receive Configuration 1 Register (I2Sx_RCR1)

Address: 4002_F000h base + 84h offset = 4002_F084h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																													RFW		
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

I2Sx_RCR1 field descriptions

Field	Description
31–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
RFW	Receive FIFO Watermark Configures the watermark level for all enabled receiver channels.

61.4.12 SAI Receive Configuration 2 Register (I2Sx_RCR2)

This register must not be altered when RCSR[RE] is set.

Address: 4002_F000h base + 88h offset = 4002_F088h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	SYNC		BCS	BCI	MSEL		BCP	BCD	0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								DIV							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

I2Sx_RCR2 field descriptions

Field	Description
31–30 SYNC	Synchronous Mode Configures between asynchronous and synchronous modes of operation. When configured for a synchronous mode of operation, the transmitter must be configured for asynchronous operation. 00 Asynchronous mode. 01 Synchronous with transmitter. 10 Synchronous with another SAI receiver. 11 Synchronous with another SAI transmitter.
29 BCS	Bit Clock Swap This field swaps the bit clock used by the receiver. When the receiver is configured in asynchronous mode and this bit is set, the receiver is clocked by the transmitter bit clock (SAI_TX_BCLK). This allows the transmitter and receiver to share the same bit clock, but the receiver continues to use the receiver frame sync (SAI_RX_SYNC). When the receiver is configured in synchronous mode, the transmitter BCS field and receiver BCS field must be set to the same value. When both are set, the transmitter and receiver are both clocked by the receiver bit clock (SAI_RX_BCLK) but use the transmitter frame sync (SAI_TX_SYNC). 0 Use the normal bit clock source. 1 Swap the bit clock source.
28 BCI	Bit Clock Input When this field is set and using an internally generated bit clock in either synchronous or asynchronous mode, the bit clock actually used by the receiver is delayed by the pad output delay (the receiver is clocked by the pad input as if the clock was externally generated). This has the effect of decreasing the data input setup time, but increasing the data output valid time. The slave mode timing from the datasheet should be used for the receiver when this bit is set. In synchronous mode, this bit allows the receiver to use the slave mode timing from the datasheet, while the transmitter uses the master mode timing. This field has no effect when configured for an externally generated bit clock . 0 No effect. 1 Internal logic is clocked as if bit clock was externally generated.
27–26 MSEL	MCLK Select Selects the audio Master Clock option used to generate an internally generated bit clock. This field has no effect when configured for an externally generated bit clock. **NOTE:** Depending on the device, some Master Clock options might not be available. See the chip-specific information for the availability and chip-specific meaning of each option. 00 Bus Clock selected. 01 Master Clock (MCLK) 1 option selected. 10 Master Clock (MCLK) 2 option selected. 11 Master Clock (MCLK) 3 option selected.
25 BCP	Bit Clock Polarity Configures the polarity of the bit clock. 0 Bit Clock is active high with drive outputs on rising edge and sample inputs on falling edge. 1 Bit Clock is active low with drive outputs on falling edge and sample inputs on rising edge.

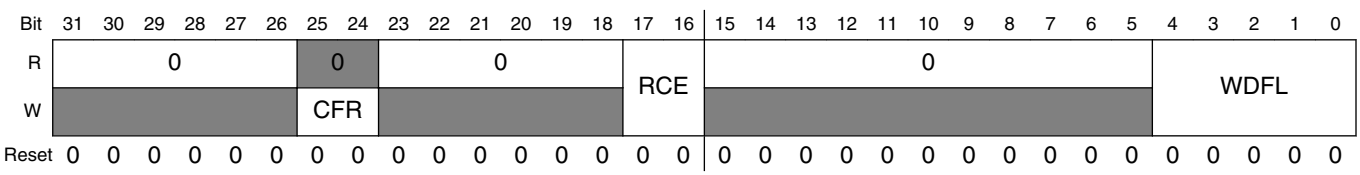
Table continues on the next page...

I2Sx_RCR2 field descriptions (continued)

Field	Description
24 BCD	Bit Clock Direction Configures the direction of the bit clock. 0 Bit clock is generated externally in Slave mode. 1 Bit clock is generated internally in Master mode.
23–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
DIV	Bit Clock Divide Divides down the audio master clock to generate the bit clock when configured for an internal bit clock. The division value is (DIV + 1) * 2.

61.4.13 SAI Receive Configuration 3 Register (I2Sx_RCR3)

Address: 4002_F000h base + 8Ch offset = 4002_F08Ch



I2Sx_RCR3 field descriptions

Field	Description
31–26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25–24 CFR	Channel FIFO Reset Resets the FIFO pointers for a specific channel. Reading this field will always return zero. FIFO pointers should only be reset when a channel is disabled or the FIFO error flag is set. 0 No effect. 1 Receive data channel N FIFO is reset.
23–18 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
17–16 RCE	Receive Channel Enable Enables the corresponding data channel for receive operation. A channel must be enabled before its FIFO is accessed. Changing this field will take effect immediately for generating the FIFO request and warning flags, but at the end of each frame for receive operation. 0 Receive data channel N is disabled. 1 Receive data channel N is enabled.
15–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
WDFL	Word Flag Configuration

Table continues on the next page...

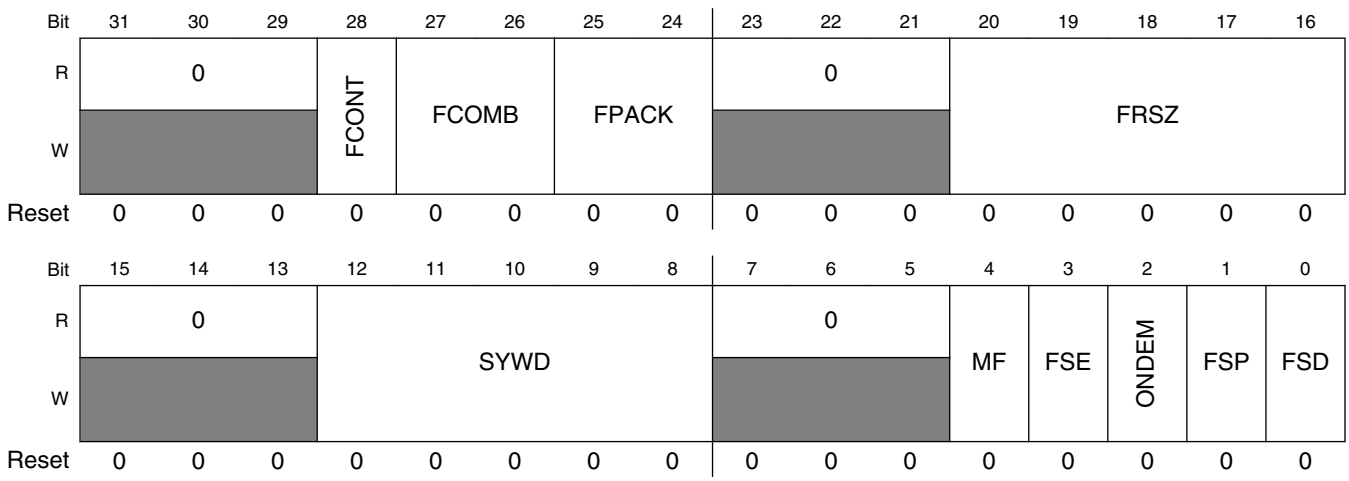
I2Sx_RCR3 field descriptions (continued)

Field	Description
	Configures which word the start of word flag is set. The value written should be one less than the word number (for example, write zero to configure for the first word in the frame). When configured to a value greater than the Frame Size field, then the start of word flag is never set.

61.4.14 SAI Receive Configuration 4 Register (I2Sx_RCR4)

This register must not be altered when RCSR[RE] is set.

Address: 4002_F000h base + 90h offset = 4002_F090h



I2Sx_RCR4 field descriptions

Field	Description
31–29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28 FCONT	FIFO Continue on Error Configures when the SAI will continue receiving after a FIFO error has been detected. 0 On FIFO error, the SAI will continue from the start of the next frame after the FIFO error flag has been cleared. 1 On FIFO error, the SAI will continue from the same word that caused the FIFO error to set after the FIFO warning flag has been cleared.
27–26 FCOMB	FIFO Combine Mode When FIFO combine mode is enabled for FIFO reads, software reading any FIFO data register will alternate the read among the enabled data channel FIFOs. For example, if two data channels are enabled then the first read will be performed to the first enabled data channel FIFO and the second read will be performed to the second enabled data channel FIFO. Reseting the FIFO or disabling FIFO combine mode for FIFO reads will reset the pointer back to the first enabled data channel. When FIFO combine mode is enabled for FIFO writes from the receive shift registers, the first enabled data channel input will alternate between the enabled data channel FIFOs. For example, if two data channels are enabled then the first unmasked received word will be stored in the first enabled data

Table continues on the next page...

I2Sx_RCR4 field descriptions (continued)

Field	Description
	channel FIFO and the second unmasked received word will be stored in the second enabled data channel FIFO. Since the first word of the frame is always stored in the first enabled data channel FIFO, it is recommended that the number of unmasked words per frame is evenly divisible by the number of enabled data channels. 00 FIFO combine mode disabled. 01 FIFO combine mode enabled on FIFO writes (from receive shift registers). 10 FIFO combine mode enabled on FIFO reads (by software). 11 FIFO combine mode enabled on FIFO writes (from receive shift registers) and reads (by software).
25–24 FPACK	FIFO Packing Mode Enables packing of 8-bit data or 16-bit data into each 32-bit FIFO word. If the word size is greater than 8-bit or 16-bit then only the first 8-bit or 16-bits are stored to the FIFO. The first word in each frame always starts with a new 32-bit FIFO word and the first bit shifted must be configured within the first packed word. When FIFO packing is enabled, the FIFO read pointer will only increment when the full 32-bit FIFO word has been read by software. 00 FIFO packing is disabled 01 Reserved. 10 8-bit FIFO packing is enabled 11 16-bit FIFO packing is enabled
23–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20–16 FRSZ	Frame Size Configures the number of words in each frame. The value written must be one less than the number of words in the frame. For example, write 0 for one word per frame. The maximum supported frame size is 32 words.
15–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12–8 SYWD	Sync Width Configures the length of the frame sync in number of bit clocks. The value written must be one less than the number of bit clocks. For example, write 0 for the frame sync to assert for one bit clock only. The sync width cannot be configured longer than the first word of the frame.
7–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 MF	MSB First Configures whether the LSB or the MSB is received first. 0 LSB is received first. 1 MSB is received first.
3 FSE	Frame Sync Early 0 Frame sync asserts with the first bit of the frame. 1 Frame sync asserts one bit before the first bit of the frame.
2 ONDEM	On Demand Mode When set, and the frame sync is generated internally, a frame sync is only generated when the FIFO warning flag is clear.

Table continues on the next page...

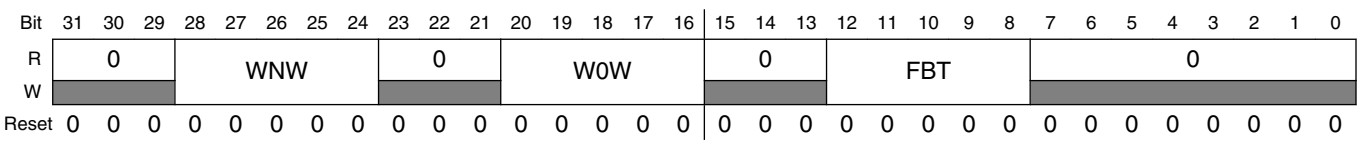
I2Sx_RCR4 field descriptions (continued)

Field	Description
	0 Internal frame sync is generated continuously. 1 Internal frame sync is generated when the FIFO warning flag is clear.
1 FSP	Frame Sync Polarity Configures the polarity of the frame sync. 0 Frame sync is active high. 1 Frame sync is active low.
0 FSD	Frame Sync Direction Configures the direction of the frame sync. 0 Frame Sync is generated externally in Slave mode. 1 Frame Sync is generated internally in Master mode.

61.4.15 SAI Receive Configuration 5 Register (I2Sx_RCR5)

This register must not be altered when RCSR[RE] is set.

Address: 4002_F000h base + 94h offset = 4002_F094h



I2Sx_RCR5 field descriptions

Field	Description
31–29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28–24 WNW	Word N Width Configures the number of bits in each word, for each word except the first in the frame. The value written must be one less than the number of bits per word. Word width of less than 8 bits is not supported.
23–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20–16 W0W	Word 0 Width Configures the number of bits in the first word in each frame. The value written must be one less than the number of bits in the first word. Word width of less than 8 bits is not supported if there is only one word per frame.
15–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12–8 FBT	First Bit Shifted Configures the bit index for the first bit received for each word in the frame. If configured for MSB First, the index of the next bit received is one less than the current bit received. If configured for LSB First, the index

Table continues on the next page...

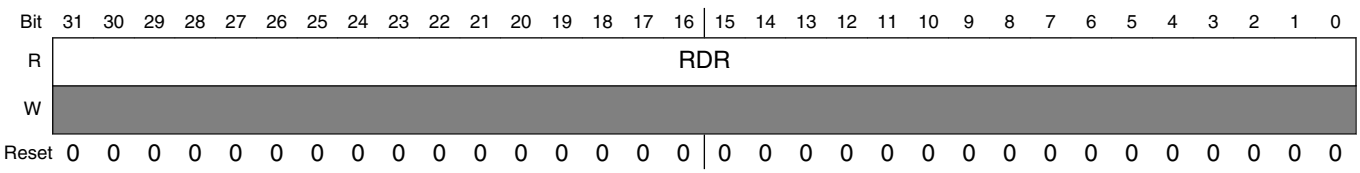
I2Sx_RCR5 field descriptions (continued)

Field	Description
	of the next bit received is one more than the current bit received. The value written must be greater than or equal to the word width when configured for MSB First. The value written must be less than or equal to 31-word width when configured for LSB First.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

61.4.16 SAI Receive Data Register (I2Sx_RDR*n*)

Reading this register introduces one additional peripheral clock wait state on each read.

Address: 4002_F000h base + A0h offset + (4d × i), where i=0d to 1d



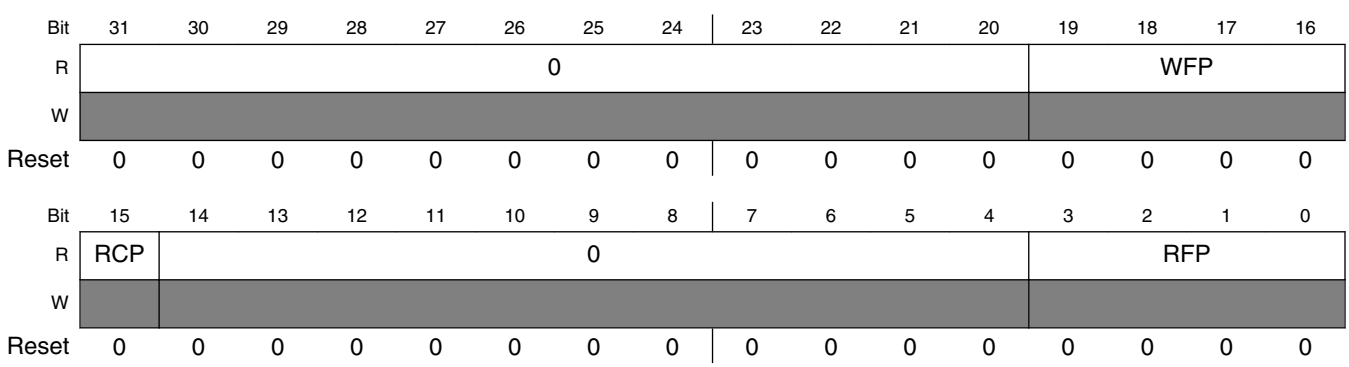
I2Sx_RDR*n* field descriptions

Field	Description
RDR	Receive Data Register The corresponding RCR3[RCE] bit must be set before accessing the channel's receive data register. Reads from this register when the receive FIFO is not empty will return the data from the top of the receive FIFO. Reads from this register when the receive FIFO is empty are ignored.

61.4.17 SAI Receive FIFO Register (I2Sx_RFR*n*)

The MSB of the read and write pointers is used to distinguish between FIFO full and empty conditions. If the read and write pointers are identical, then the FIFO is empty. If the read and write pointers are identical except for the MSB, then the FIFO is full.

Address: 4002_F000h base + C0h offset + (4d × i), where i=0d to 1d



I2Sx_RFR*n* field descriptions

Field	Description
31–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–16 WFP	Write FIFO Pointer FIFO write pointer for receive data channel.
15 RCP	Receive Channel Pointer When FIFO Combine mode is enabled for reads, indicates that this data channel is the next FIFO to be read. 0 No effect. 1 FIFO combine is enabled for FIFO reads and this FIFO will be read on the next FIFO read.
14–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
RFP	Read FIFO Pointer FIFO read pointer for receive data channel.

61.4.18 SAI Receive Mask Register (I2Sx_RMR)

This register is double-buffered and updates:

1. When RCSR[RE] is first set
2. At the end of each frame

This allows the masked words in each frame to change from frame to frame.

Address: 4002_F000h base + E0h offset = 4002_F0E0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	RWM																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

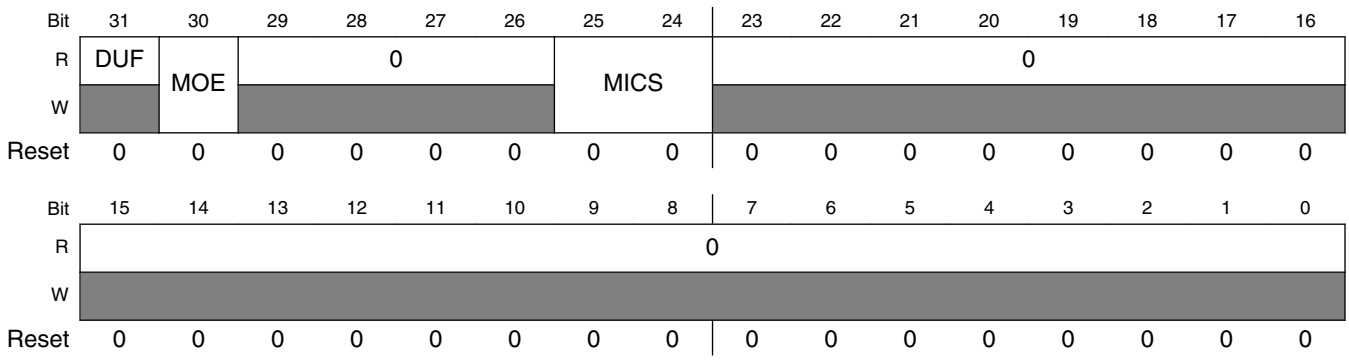
I2Sx_RMR field descriptions

Field	Description
RWM	Receive Word Mask Configures whether the receive word is masked (received data ignored and not written to receive FIFO) for the corresponding word in the frame. 0 Word N is enabled. 1 Word N is masked.

61.4.19 SAI MCLK Control Register (I2Sx_MCR)

The MCLK Control Register (MCR) controls the clock source and direction of the audio master clock.

Address: 4002_F000h base + 100h offset = 4002_F100h



I2Sx_MCR field descriptions

Field	Description
31 DUF	Divider Update Flag Provides the status of on-the-fly updates to the MCLK divider ratio. 0 MCLK divider ratio is not being updated currently. 1 MCLK divider ratio is updating on-the-fly. Further updates to the MCLK divider ratio are blocked while this flag remains set.
30 MOE	MCLK Output Enable Enables the MCLK divider and configures the MCLK signal pin as an output. When software clears this field, it remains set until the MCLK divider is fully disabled. 0 MCLK signal pin is configured as an input that bypasses the MCLK divider. 1 MCLK signal pin is configured as an output from the MCLK divider and the MCLK divider is enabled.
29–26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25–24 MICS	MCLK Input Clock Select Selects the clock input to the MCLK divider. This field cannot be changed while the MCLK divider is enabled. See the chip-specific information for the connections to these inputs. 00 MCLK divider input clock 0 is selected. 01 MCLK divider input clock 1 is selected. 10 MCLK divider input clock 2 is selected. 11 MCLK divider input clock 3 is selected.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

61.4.20 SAI MCLK Divide Register (I2Sx_MDR)

The MCLK Divide Register (MDR) configures the MCLK divide ratio. Although the MDR can be changed when the MCLK divider clock is enabled, additional writes to the MDR are blocked while MCR[DUF] is set. Writes to the MDR when the MCLK divided clock is disabled do not set MCR[DUF].

Address: 4002_F000h base + 104h offset = 4002_F104h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												FRACT				DIVIDE															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

I2Sx_MDR field descriptions

Field	Description
31–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–12 FRACT	MCLK Fraction Sets the MCLK divide ratio such that: MCLK output = MCLK input * ((FRACT + 1) / (DIVIDE + 1)). FRACT must be set equal or less than the value in the DIVIDE field. **NOTE:** When using fractional divide values, the MCLK duty cycle will not always be 50/50. See Audio master clock.
DIVIDE	MCLK Divide Sets the MCLK divide ratio such that: MCLK output = MCLK input * ((FRACT + 1) / (DIVIDE + 1)). FRACT must be set equal or less than the value in the DIVIDE field. **NOTE:** When using fractional divide values, the MCLK duty cycle will not always be 50/50. See Audio master clock.

61.5 Functional description

This section provides a complete functional description of the block.

61.5.1 SAI clocking

The SAI clocks include:

- The audio master clock
- The bit clock
- The bus clock

61.5.1.1 Audio master clock

The audio master clock is used to generate the bit clock when the receiver or transmitter is configured for an internally generated bit clock. The transmitter and receiver can independently select between the bus clock and up to three audio master clocks to generate the bit clock.

Each SAI peripheral can control the input clock selection, pin direction and divide ratio of one audio master clock. The input clock selection and pin direction cannot be altered if an SAI module using that audio master clock has been enabled. The MCLK divide ratio can be altered while an SAI is using that master clock, although the change in the divide ratio takes several cycles. MCR[DUF] can be polled to determine when the divide ratio change has completed.

The audio master clock generation and selection is chip-specific. Refer to chip-specific clocking information about how the audio master clocks are generated. A typical implementation appears in the following figure.

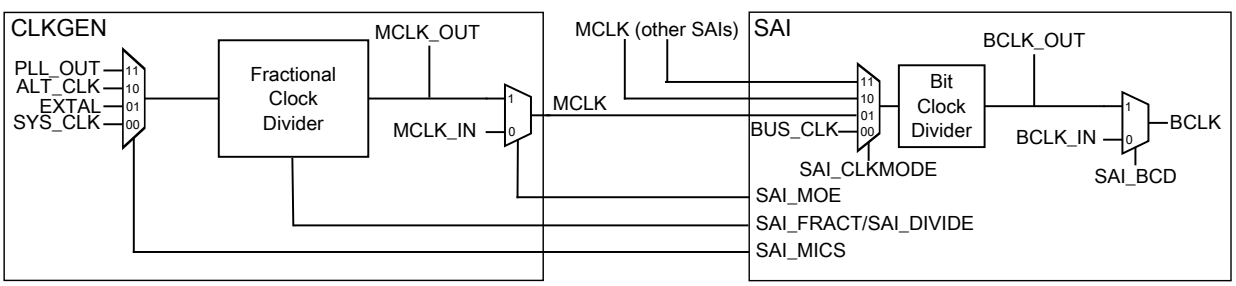


Figure 61-3. SAI master clock generation

The MCLK fractional clock divider uses both clock edges from the input clock to generate a divided down clock that will approximate the output frequency, but without creating any new clock edges. Configuring FRACT and DIVIDE to the same value will result in a divide by 1 clock, while configuring FRACT higher than DIVIDE is not supported. The duty cycle can range from 66/33 when FRACT is set to one less than DIVIDE down to 50/50 for integer divide ratios, and will approach 50/50 for large non-integer divide ratios. There is no cycle to cycle jitter or duty cycle variance when the divide ratio is an integer or half integer, otherwise the divider output will oscillate between the two divided frequencies that are the closest integer or half integer divisors of the divider input clock frequency. The maximum jitter is therefore equal to half the divider input clock period, since both edges of the input clock are used in generating the divided clock.

61.5.1.2 Bit clock

The SAI transmitter and receiver support asynchronous free-running bit clocks that can be generated internally from an audio master clock or supplied externally. There is also the option for synchronous bit clock and frame sync operation between the receiver and transmitter or between multiple SAI peripherals.

Externally generated bit clocks must be:

- Enabled before the SAI transmitter or receiver is enabled
- Disabled after the SAI transmitter or receiver is disabled and completes its current frames

If the SAI transmitter or receiver is using an externally generated bit clock in asynchronous mode and that bit clock is generated by an SAI that is disabled in stop mode, then the transmitter or receiver should be disabled by software before entering stop mode. This issue does not apply when the transmitter or receiver is in a synchronous mode because all synchronous SAIs are enabled and disabled simultaneously.

61.5.1.3 Bus clock

The bus clock is used by the control and configuration registers and to generate synchronous interrupts and DMA requests.

NOTE

Although there is no specific minimum bus clock frequency specified, the bus clock frequency must be fast enough (relative to the bit clock frequency) to ensure that the FIFOs can be serviced, without generating either a transmitter FIFO underrun or receiver FIFO overflow condition.

61.5.2 SAI resets

The SAI is asynchronously reset on system reset. The SAI has a software reset and a FIFO reset.

61.5.2.1 Software reset

The SAI transmitter includes a software reset that resets all transmitter internal logic, including the bit clock generation, status flags, and FIFO pointers. It does not reset the configuration registers. The software reset remains asserted until cleared by software.

The SAI receiver includes a software reset that resets all receiver internal logic, including the bit clock generation, status flags and FIFO pointers. It does not reset the configuration registers. The software reset remains asserted until cleared by software.

61.5.2.2 FIFO reset

The SAI transmitter includes a FIFO reset that synchronizes the FIFO write pointer to the same value as the FIFO read pointer. This empties the FIFO contents and is to be used after TCSR[FEF] is set, and before the FIFO is re-initialized and TCSR[FEF] is cleared. The FIFO reset is asserted for one cycle only.

The SAI transmitter can also reset the FIFO of individual data channels by setting the appropriate TCR3[CFR] bit. This should only be done when the corresponding TCR3[TCE] bit is clear.

The SAI receiver includes a FIFO reset that synchronizes the FIFO read pointer to the same value as the FIFO write pointer. This empties the FIFO contents and is to be used after the RCSR[FEF] is set and any remaining data has been read from the FIFO, and before the RCSR[FEF] is cleared. The FIFO reset is asserted for one cycle only.

The SAI receiver can also reset the FIFO of individual data channels by setting the appropriate RCR3[CFR] bit. This should only be done when the corresponding RCR3[RCE] bit is clear.

61.5.3 Synchronous modes

The SAI transmitter and receiver can operate synchronously to each other.

61.5.3.1 Synchronous mode

The SAI transmitter and receiver can be configured to operate with synchronous bit clock and frame sync.

If the transmitter bit clock and frame sync are to be used by both the transmitter and receiver:

- The transmitter must be configured for asynchronous operation and the receiver for synchronous operation.
- In synchronous mode, the receiver is enabled only when both the transmitter and receiver are enabled.
- It is recommended that the transmitter is the last enabled and the first disabled.

If the receiver bit clock and frame sync are to be used by both the transmitter and receiver:

- The receiver must be configured for asynchronous operation and the transmitter for synchronous operation.
- In synchronous mode, the transmitter is enabled only when both the receiver and transmitter are both enabled.
- It is recommended that the receiver is the last enabled and the first disabled.

When operating in synchronous mode, only the bit clock, frame sync, and transmitter/receiver enable are shared. The transmitter and receiver otherwise operate independently, although configuration registers must be configured consistently across both the transmitter and receiver.

61.5.4 Frame sync configuration

When enabled, the SAI continuously transmits and/or receives frames of data. Each frame consists of a fixed number of words and each word consists of a fixed number of bits. Within each frame, any given word can be masked causing the receiver to ignore that word and the transmitter to tri-state for the duration of that word.

The frame sync signal is used to indicate the start of each frame. A valid frame sync requires a rising edge (if active high) or falling edge (if active low) to be detected and the transmitter or receiver cannot be busy with a previous frame. A valid frame sync is also ignored (slave mode) or not generated (master mode) for the first four bit clock cycles after enabling the transmitter or receiver.

The transmitter and receiver frame sync can be configured independently with any of the following options:

- Externally generated or internally generated
- Active high or active low
- Assert with the first bit in frame or asserts one bit early
- Assert for a duration between 1 bit clock and the first word length
- Frame length from 1 to 32 words per frame
- Word length to support 8 to 32 bits per word

- First word length and remaining word lengths can be configured separately
- Words can be configured to transmit/receive MSB first or LSB first

These configuration options cannot be changed after the SAI transmitter or receiver is enabled.

61.5.5 Data FIFO

Each transmit and receive channel includes a FIFO of size 8 × 32-bit. The FIFO data is accessed using the SAI Transmit/Receive Data Registers.

61.5.5.1 Data alignment

Data in the FIFO can be aligned anywhere within the 32-bit wide register through the use of the First Bit Shifted configuration field, which selects the bit index (between 31 and 0) of the first bit shifted.

Examples of supported data alignment and the required First Bit Shifted configuration are illustrated in Figure 61-4 for LSB First configurations and Figure 61-5 for MSB First configurations.

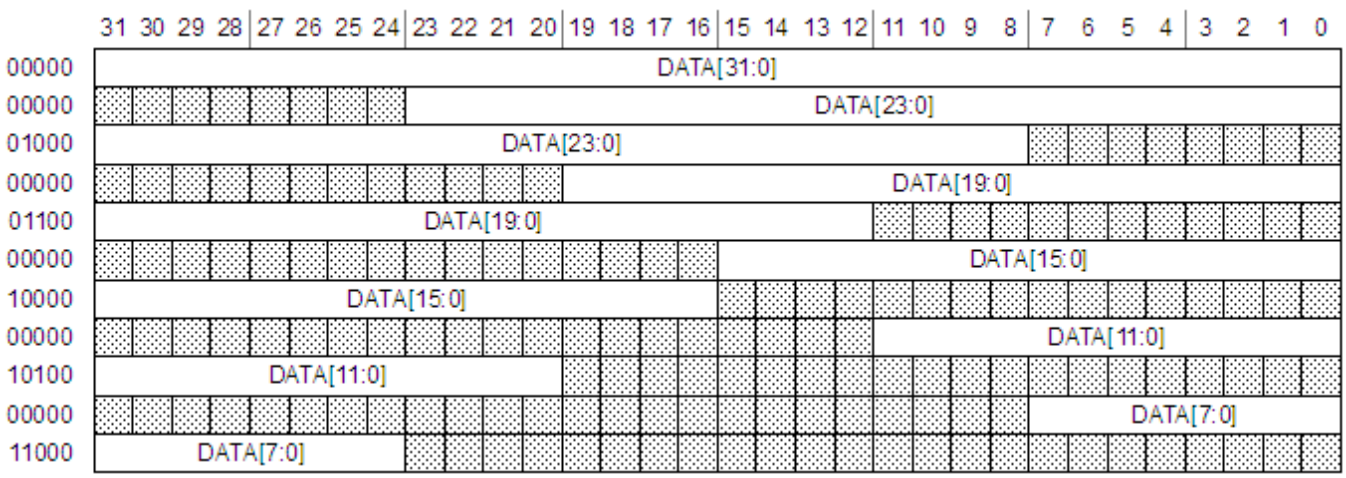


Figure 61-4. SAI first bit shifted, LSB first

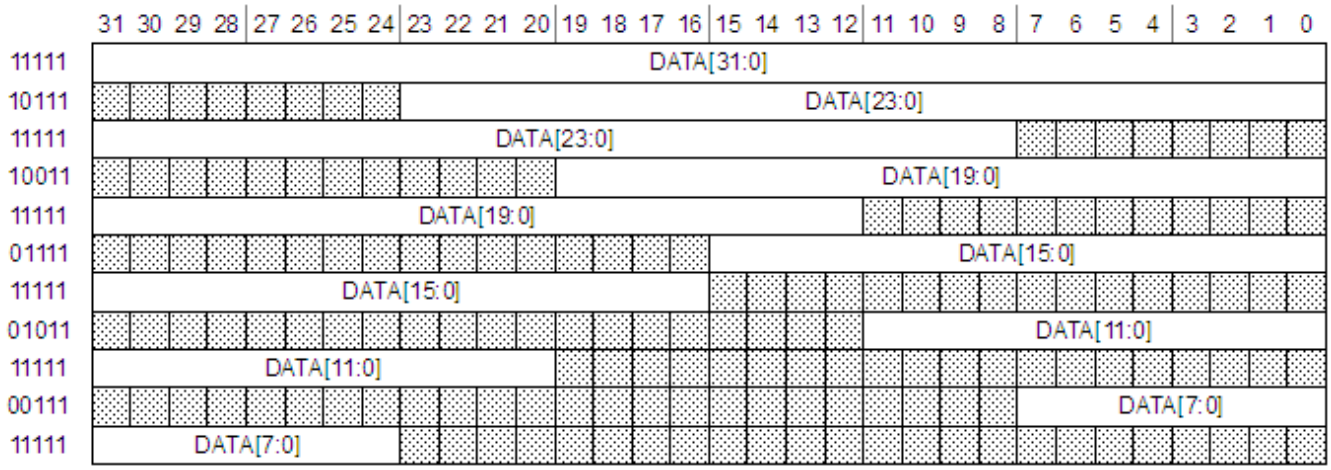


Figure 61-5. SAI first bit shifted, MSB first

61.5.5.2 FIFO pointers

When writing to a TDR, the WFP of the corresponding TFR increments after each valid write. The SAI supports 8-bit, 16-bit and 32-bit writes to the TDR and the FIFO pointer will increment after each individual write. Note that 8-bit writes should only be used when transmitting up to 8-bit data and 16-bit writes should only be used when transmitting up to 16-bit data.

Writes to a TDR are ignored if the corresponding bit of TCR3[TCE] is clear or if the FIFO is full. If the Transmit FIFO is empty, the TDR must be written at least three bit clocks before the start of the next unmasked word to avoid a FIFO underrun.

When reading an RDR, the RFP of the corresponding RFR increments after each valid read. The SAI supports 8-bit, 16-bit and 32-bit reads from the RDR and the FIFO pointer will increment after each individual read. Note that 8-bit reads should only be used when receiving up to 8-bit data and 16-bit reads should only be used when receiving up to 16-bit data.

Reads from an RDR are ignored if the corresponding bit of RCR3[RCE] is clear or if the FIFO is empty. If the Receive FIFO is full, the RDR must be read at least three bit clocks before the end of an unmasked word to avoid a FIFO overrun.

61.5.5.3 FIFO packing

FIFO packing supports storing multiple 8-bit or 16-bit data words in one 32-bit FIFO word for the transmitter and/or receiver. While this can be emulated by adjusting the number of bits per word and number of words per frame (for example, one 32-bit word

per frame versus two 16-bit words per frame), FIFO packing does not require even multiples of words per frame and fully supports word masking. When FIFO packing is enabled, the FIFO pointers only increment when the full 32-bit FIFO word has been written (transmit) or read (receive) by software, supporting scenarios where different words within each frame are loaded/stored in different areas of memory.

When 16-bit FIFO packing is enabled for transmit, the transmit shift register is loaded at the start of each frame and after every second unmasked transmit word. The first word transmitted is taken from 16-bit word at byte offset $0 (first bit is selected by TCFG5[FBT] must be configured within this 16-bit word) and the second word transmitted is taken from the 16-bit word at byte offset $2 (first bit is selected by TCSR5[FBT][3:0]). The transmitter will transmit logic zero until the start of the next word once the 16-bit word has been transmitted.

When 16-bit FIFO packing is enabled for receive, the receive shift register is stored after every second unmasked received word, and at the end of each frame if there is an odd number of unmasked received words in each frame. The first word received is stored in the 16-bit word at byte offset $0 (first bit is selected by RCFG5[FBT] and must be configured within this 16-bit word) and the second word received is stored in the 16-bit word at byte offset $2 (first bit is selected by RCSR5[FBT][3:0]). The receiver will ignore received data until the start of the next word once the 16-bit word has been received.

The 8-bit FIFO packing is similar to 16-bit packing except four words are loaded or stored into each 32-bit FIFO word. The first word is loaded/stored in byte offset $0, second word in byte offset $1, third word in byte offset $2 and fourth word in byte offset $3. The TCFG5[FBT] and/or RCFG5[FBT] must be configured within byte offset $0.

61.5.5.4 FIFO Combine

FIFO combining mode allows the separate FIFOs for multiple data channels to be used as a single FIFO for either software accesses or a single data channel or both. Note that the enabled data channels must be contiguous and data channel 0 must be enabled when FIFO Combine mode is enabled.

Combining FIFOs for software access (writing transmit FIFO registers, reading receive FIFO registers) allows a DMA controller or software to read or write multiple FIFOs without incrementing the address that is accessed. Once enabled, the first software access to a FIFO register will access the first enabled channel FIFO, while the second access to a FIFO register will access the second enabled channel FIFO. This continues until software

accesses the last enabled channel FIFO and the pointer resets back to the first enabled channel FIFO. To reset the pointer manually, software can reset the FIFOs or disable the FIFO combining on software accesses.

Combining FIFOs for transmit data channels allows one data channel to use the FIFOs of all enabled channel FIFOs, with identical data output on each enabled data channel. The transmit shift registers for all enabled data channels are loaded at the start of each frame and every N unmasked words (where N is the number of enabled data channels). The first word transmitted is loaded from the first enabled channel FIFO, while the second word transmitted is loaded from the second enabled channel FIFO, and so on until the end of the frame. Since the first word in each frame is always loaded from the first enabled data channel, it is recommended that the number of unmasked words in each frame is evenly divisible by the number of enabled data channels.

Combining FIFOs for receive data channels allows one data channel to use the FIFOs of all enabled channel FIFOs, with received data from channel 0 stored into each enabled data channel. The receive shift register for all enabled data channels are stored after every N unmasked words (where N is the number of enabled data channels). The first word received is stored to the first enabled channel FIFO, while the second word received is stored to the second enabled channel FIFO, and so on until the end of the frame. Since the first word in each frame is always stored the first enabled data channel, it is recommended that the number of unmasked words in each frame is evenly divisible by the number of enabled data channels.

Note that combining FIFOs for data channels will load or store each channel FIFO at the same time. This means that FIFO error conditions are only checked every N words (where N is the number of enabled data channels) and that the FIFO warning and request flags will assert if any of the enabled data channel meets the warning flag or request flag conditions.

61.5.6 Word mask register

The SAI transmitter and receiver each contain a word mask register, namely TMR and RMR, that can be used to mask any word in the frame. Because the word mask register is double buffered, software can update it before the end of each frame to mask a particular word in the next frame.

The TMR causes the Transmit Data pin to be tri-stated for the length of each selected word and the transmit FIFO is not read for masked words.

The RMR causes the received data for each selected word to be discarded and not written to the receive FIFO.

61.5.7 Interrupts and DMA requests

The SAI transmitter and receiver generate separate interrupts and separate DMA requests, but support the same status flags. Asynchronous versions of the transmitter and receiver interrupts are generated to wake up the CPU from stop mode.

61.5.7.1 FIFO request flag

The FIFO request flag is set based on the number of entries in the FIFO and the FIFO watermark configuration.

The transmit FIFO request flag is set when the number of entries in any of the enabled transmit FIFOs is less than or equal to the transmit FIFO watermark configuration and is cleared when the number of entries in each enabled transmit FIFO is greater than the transmit FIFO watermark configuration.

The receive FIFO request flag is set when the number of entries in any of the enabled receive FIFOs is greater than the receive FIFO watermark configuration and is cleared when the number of entries in each enabled receive FIFO is less than or equal to the receive FIFO watermark configuration.

The FIFO request flag can generate an interrupt or a DMA request.

61.5.7.2 FIFO warning flag

The FIFO warning flag is set based on the number of entries in the FIFO.

The transmit warning flag is set when the number of entries in any of the enabled transmit FIFOs is empty and is cleared when the number of entries in each enabled transmit FIFO is not empty.

The receive warning flag is set when the number of entries in any of the enabled receive FIFOs is full and is cleared when the number of entries in each enabled receive FIFO is not full.

The FIFO warning flag can generate an Interrupt or a DMA request.

61.5.7.3 FIFO error flag

The transmit FIFO error flag is set when the any of the enabled transmit FIFOs underflow. After it is set, all enabled transmit channels will transmit zero until TCSR[FEF] is cleared and the next transmit frame starts. All enabled transmit FIFOs must be reset and initialized with new data before TCSR[FEF] is cleared.

When TCR4[FCONT] is set, the FIFO will continue transmitting data following an underflow without software intervention. To ensure that data is transmitted in the correct order, the transmitter will continue from the same word number in the frame that caused the FIFO to underflow, but only after new data has been written to the transmit FIFO. Software should still clear the TCSR[FEF] flag, but without reinitializing the transmit FIFOs.

RCSR[FEF] is set when the any of the enabled receive FIFOs overflow. After it is set, all enabled receive channels discard received data until RCSR[FEF] is cleared and the next next receive frame starts. All enabled receive FIFOs should be emptied before RCSR[FEF] is cleared.

When RCR4[FCONT] is set, the FIFO will continue receiving data following an overflow without software intervention. To ensure that data is received in the correct order, the receiver will continue from the same word number in the frame that caused the FIFO to overflow, but only after data has been read from the receive FIFO. Software should still clear the RCSR[FEF] flag, but without emptying the receive FIFOs.

The FIFO error flag can generate only an interrupt.

61.5.7.4 Sync error flag

The sync error flag, TCSR[SEF] or RCSR[SEF], is set when configured for an externally generated frame sync and the external frame sync asserts when the transmitter or receiver is busy with the previous frame. The external frame sync assertion is ignored and the sync error flag is set. When the sync error flag is set, the transmitter or receiver continues checking for frame sync assertion when idle or at the end of each frame.

The sync error flag can generate an interrupt only.

61.5.7.5 Word start flag

The word start flag is set at the start of the second bit clock for the selected word, as configured by the Word Flag register field.

The word start flag can generate an interrupt only.

Chapter 62
Secured digital host controller (SDHC)

62.1 Chip-specific SDHC information

62.1.1 SDHC clocking

In addition to the system clock, the SDHC needs a clock for the base for the external card clock. There are four possible clock sources for this clock, selected by the SIM_SOPT2 register:

- Core/system clock
- MCGPLLCLK or MCGFLLCLK
- OSCERCLK
- Bypass clock from off-chip (SDHC0_CLKIN) when available

NOTE

SDHC0_CLKIN is not available on all packages. See the Pinout section for more information.

62.1.2 SD bus pullup/pulldown constraints

The SD standard requires the SD bus signals (except the SD clock) to be pulled up during data transfers. The SDHC also provides a feature of detecting card insertion/removal, by detecting voltage level changes on DAT[3] of the SD bus. To support this DAT[3] must be pulled down. To avoid a situation where the SDHC detects voltage changes due to normal data transfers on the SD bus as card insertion/removal, the interrupt relating to this event must be disabled after the card has been inserted and detected. It can be re-enabled after the card is removed.

62.2 Introduction

The chapter is intended for a module driver software developer. It describes module-level operation and programming.

62.3 Overview

62.3.1 Supported types of cards

Different types of cards supported by the SDHC are described briefly as follows:

The multimedia card (MMC) is a universal low-cost data storage and communication media that is designed to cover a wide area of applications including mobile video and gaming. Old MMC cards are based on a 7-pin serial bus with a single data pin, while the new high-speed MMC communication is based on an advanced 11-pin serial bus designed to operate in the low-voltage range.

The secure digital card (SD) is an evolution of the old MMC technology. It is specifically designed to meet the security, capacity, performance, and environment requirements inherent in newly emerging audio and video consumer electronic devices. The physical form factor, pin assignment, and data transfer protocol are forward compatible with the old MMC with some additions.

Under the SD protocol, it can be categorized into memory card, I/O card and combo card, which has both memory and I/O functions. The memory card invokes a copyright protection mechanism that complies with the security of the SDMI standard. The I/O card, which is also known as SDIO card, provides high-speed data I/O with low power consumption for mobile electronic devices. For the sake of simplicity, the figure does not show cards with reduced size or mini cards.

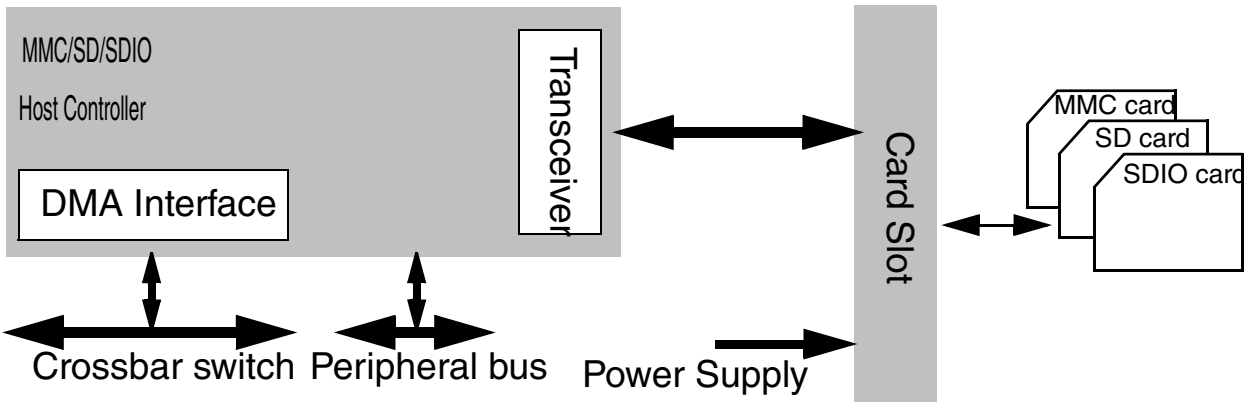


Figure 62-1. System connection of the SDHC

62.3.2 SDHC block diagram

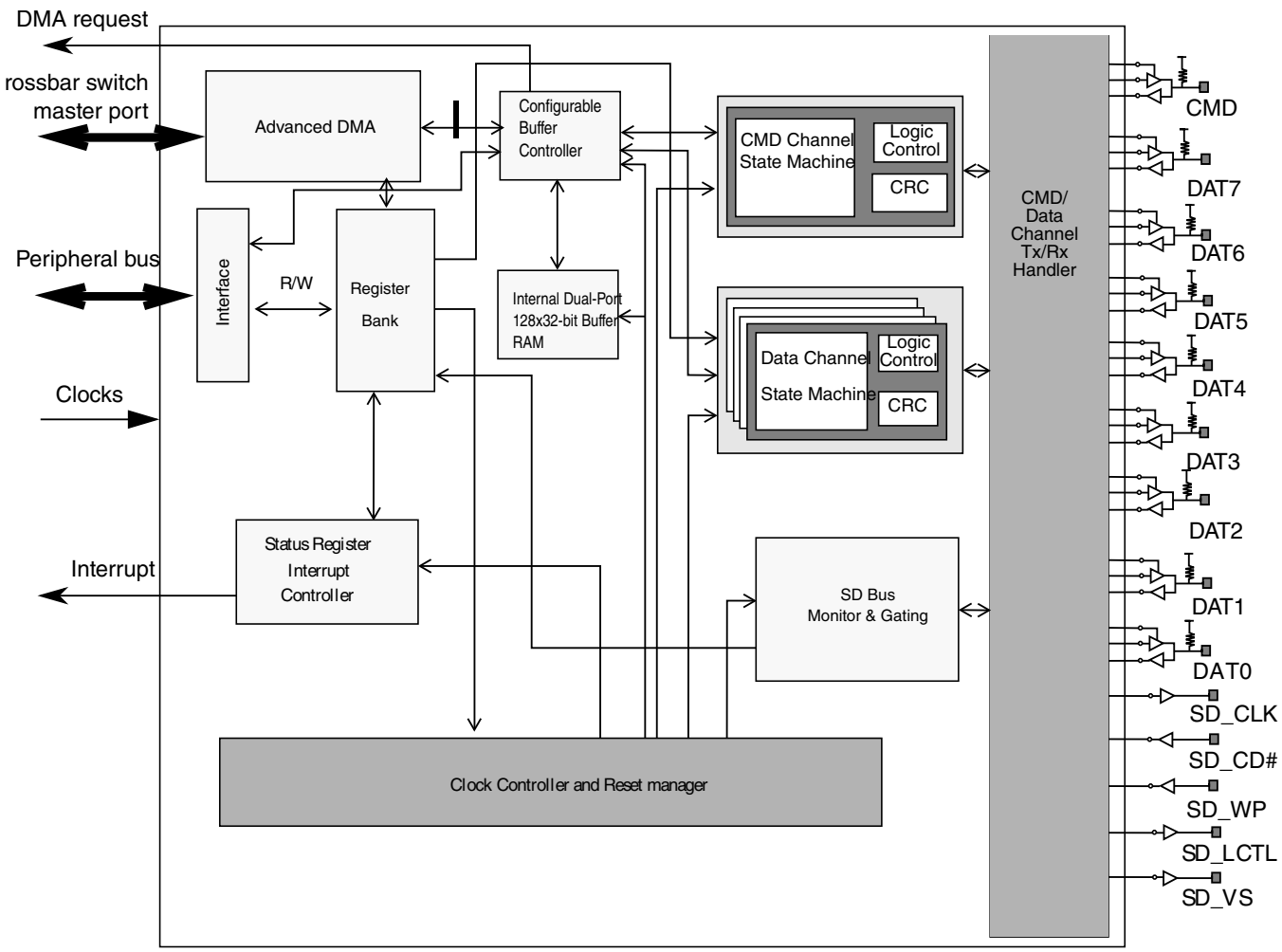


Figure 62-2. Enhanced secure digital host controller block diagram

62.3.3 Features

The features of the SDHC module include:

- Conforms to the SD Host Controller Standard Specification version 2.0 including test event register support
- Compatible with the MMC System Specification version 4.2/4.3
- Compatible with the SD Memory Card Specification version 2.0 and supports the high capacity SD memory card
- Compatible with the SDIO Card Specification version 2.0
- Designed to work with SD memory, miniSD memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Card bus clock frequency up to 52 MHz
- Supports 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit / 8-bit MMC modesdevices
  - Up to 200 Mbps of data transfer for SD/SDIO cards using 4 parallel data lines
  - Up to 416 Mbps of data transfer for MMC cards using 8 parallel data lines in Single Data Rate (SDR) mode
- Supports single block, multiblock read and write
- Supports block sizes of 1 ~ 4096 bytes
- Supports the write protection switch for write operations
- Supports both synchronous and asynchronous abort (both hardware and software CMD12)
- Supports pause during the data transfer at block gap
- Supports SDIO Read Wait and Suspend Resume operations
- Supports auto CMD12 for multiblock transfer
- Host can initiate non-data transfer command while data transfer is in progress
- Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes, also supports interrupt period
- Embodies a fully configurable 128x32-bit FIFO for read/write data

- Supports internal DMA capabilities
- Supports advanced DMA to perform linked memory access

NOTE

External SDHC DMA request is not supported.

62.3.4 Modes and operations

The SDHC can select the following modes for data transfer:

- SD 1-bit
- SD 4-bit
- MMC 1-bit
- MMC 4-bit
- MMC 8-bit
- Identification mode up to 400 kHz
- MMC Full Speed mode up to 20 MHz
- MMC High Speed mode up to 52 MHz
- SD/SDIO Full Speed mode up to 25 MHz
- SD/SDIO High Speed mode up to 50 MHz

62.4 SDHC signal descriptions

Table 62-1. SDHC signal descriptions

Signal	Description	I/O
SDHC_DCLK	Generated clock used to drive the MMC, SD, SDIO or CE-ATA cards.	O
SDHC_CMD	Send commands to and receive responses from the card.	I/O
SDHC_D0	DAT0 line or busy-state detect	I/O
SDHC_D1	8-bit mode: DAT1 line 4-bit mode: DAT1 line or interrupt detect 1-bit mode: Interrupt detect	I/O

Table continues on the next page...

Table 62-1. SDHC signal descriptions (continued)

Signal	Description	I/O
SDHC_D2	4-/8-bit mode: DAT2 line or read wait 1-bit mode: Read wait	I/O
SDHC_D3	4-/8-bit mode: DAT3 line or configured as card detection pin 1-bit mode: May be configured as card detection pin	I/O
SDHC_D4	DAT4 line in 8-bit mode Not used in other modes	I/O
SDHC_D5	DAT5 line in 8-bit mode Not used in other modes	I/O
SDHC_D6	DAT6 line in 8-bit mode Not used in other modes	I/O
SDHC_D7	DAT7 line in 8-bit mode Not used in other modes	I/O

62.5 Memory map and register definition

This section includes the module memory map and detailed descriptions of all registers.

SDHC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400B_1000	DMA System Address register (SDHC_DSADDR)	32	R/W	0000_0000h	62.5.1/2061
400B_1004	Block Attributes register (SDHC_BLKATTR)	32	R/W	0000_0000h	62.5.2/2062
400B_1008	Command Argument register (SDHC_CMDARG)	32	R/W	0000_0000h	62.5.3/2063
400B_100C	Transfer Type register (SDHC_XFERTYP)	32	R/W	0000_0000h	62.5.4/2064
400B_1010	Command Response 0 (SDHC_CMDRSP0)	32	R	0000_0000h	62.5.5/2068
400B_1014	Command Response 1 (SDHC_CMDRSP1)	32	R	0000_0000h	62.5.6/2068
400B_1018	Command Response 2 (SDHC_CMDRSP2)	32	R	0000_0000h	62.5.7/2069
400B_101C	Command Response 3 (SDHC_CMDRSP3)	32	R	0000_0000h	62.5.8/2069
400B_1020	Buffer Data Port register (SDHC_DATPORT)	32	R/W	0000_0000h	62.5.9/2070
400B_1024	Present State register (SDHC_PRSSTAT)	32	R	0000_0000h	62.5.10/ 2071
400B_1028	Protocol Control register (SDHC_PROCTL)	32	R/W	0000_0020h	62.5.11/ 2076
400B_102C	System Control register (SDHC_SYSCTL)	32	R/W	0000_8008h	62.5.12/ 2080

Table continues on the next page...

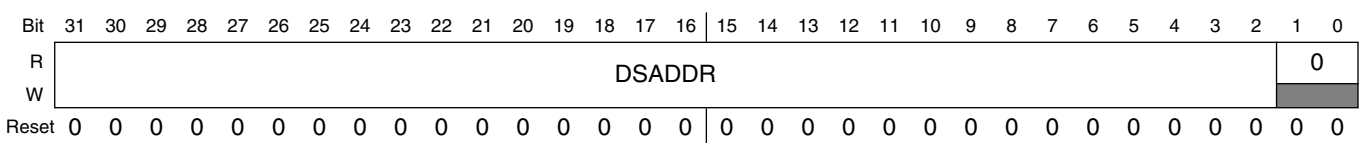
SDHC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400B_1030	Interrupt Status register (SDHC_IRQSTAT)	32	R/W	0000_0000h	62.5.13/ 2083
400B_1034	Interrupt Status Enable register (SDHC_IRQSTATEN)	32	R/W	117F_013Fh	62.5.14/ 2088
400B_1038	Interrupt Signal Enable register (SDHC_IRQSIGEN)	32	R/W	0000_0000h	62.5.15/ 2091
400B_103C	Auto CMD12 Error Status Register (SDHC_AC12ERR)	32	R	0000_0000h	62.5.16/ 2093
400B_1040	Host Controller Capabilities (SDHC_HTCAPBLT)	32	R	07F3_0000h	62.5.17/ 2097
400B_1044	Watermark Level Register (SDHC_WML)	32	R/W	0010_0010h	62.5.18/ 2099
400B_1050	Force Event register (SDHC_FEVT)	32	W (always reads 0)	0000_0000h	62.5.19/ 2099
400B_1054	ADMA Error Status register (SDHC_ADMAES)	32	R	0000_0000h	62.5.20/ 2102
400B_1058	ADMA System Addressregister (SDHC_ADSADDR)	32	R/W	0000_0000h	62.5.21/ 2104
400B_10C0	Vendor Specific register (SDHC_VENDOR)	32	R/W	0000_0001h	62.5.22/ 2105
400B_10C4	MMC Boot register (SDHC_MMCBOOT)	32	R/W	0000_0000h	62.5.23/ 2107
400B_10FC	Host Controller Version (SDHC_HOSTVER)	32	R	0000_1201h	62.5.24/ 2108

62.5.1 DMA System Address register (SDHC_DSADDR)

This register contains the physical system memory address used for DMA transfers.

Address: 400B_1000h base + 0h offset = 400B_1000h



SDHC_DSADDR field descriptions

Field	Description
31–2 DSADDR	DMA System Address Contains the 32-bit system memory address for a DMA transfer. Because the address must be word (4 bytes) align, the least 2 bits are reserved, always 0. When the SDHC stops a DMA transfer, this register points to the system address of the next contiguous data position. It can be accessed only when no transaction is executing, that is, after a transaction has stopped. Read operation during transfers may

Table continues on the next page...

SDHC_DSADDR field descriptions (continued)

Field	Description
	return an invalid value. The host driver shall initialize this register before starting a DMA transaction. After DMA has stopped, the system address of the next contiguous data position can be read from this register. This register is protected during a data transfer. When data lines are active, write to this register is ignored. The host driver shall wait, until PRSSTAT[DLA] is cleared, before writing to this register. The SDHC internal DMA does not support a virtual memory system. It supports only continuous physical memory access. And due to AHB burst limitations, if the burst must cross the 1 KB boundary, SDHC will automatically change SEQ burst type to NSEQ. Because this register supports dynamic address reflecting, when IRQSTAT[TC] bit is set, it automatically alters the value of internal address counter, so SW cannot change this register when IRQSTAT[TC] is set.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

62.5.2 Block Attributes register (SDHC_BLKATTR)

This register is used to configure the number of data blocks and the number of bytes in each block.

Address: 400B_1000h base + 4h offset = 400B_1004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BLKCNT																0			BLKSIZE											
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDHC_BLKATTR field descriptions

Field	Description
31–16 BLKCNT	Blocks Count For Current Transfer This register is enabled when XFERTYP[BCEN] is set to 1 and is valid only for multiple block transfers. For single block transfer, this register will always read as 1. The host driver shall set this register to a value between 1 and the maximum block count. The SDHC decrements the block count after each block transfer and stops when the count reaches zero. Setting the block count to 0 results in no data blocks being transferred. This register must be accessed only when no transaction is executing, that is, after transactions are stopped. During data transfer, read operations on this register may return an invalid value and write operations are ignored. When saving transfer content as a result of a suspend command, the number of blocks yet to be transferred can be determined by reading this register. The reading of this register must be applied after transfer is paused by stop at block gap operation and before sending the command marked as suspend. This is because when suspend command is sent out, SDHC will regard the current transfer as aborted and change BLKCNT back to its original value instead of keeping the dynamical indicator of remained block count. When restoring transfer content prior to issuing a resume command, the host driver shall restore the previously saved block count. **NOTE:** Although the BLKCNT field is 0 after reset, the read of reset value is 0x1. This is because when XFERTYP[MSBSEL] is 0, indicating a single block transfer, the read value of BLKCNT is always 1.

Table continues on the next page...

SDHC_BLKATTR field descriptions (continued)

Field	Description
	0000h Stop count. 0001h 1 block 0002h 2 blocks ... FFFFh 65535 blocks
15–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
BLKSIZE	Transfer Block Size Specifies the block size for block data transfers. Values ranging from 1 byte up to the maximum buffer size can be set. It can be accessed only when no transaction is executing, that is, after a transaction has stopped. Read operations during transfers may return an invalid value, and write operations will be ignored. 000h No data transfer. 001h 1 Byte 002h 2 Bytes 003h 3 Bytes 004h 4 Bytes ... 1FFh 511 Bytes 200h 512 Bytes ... 800h 2048 Bytes ... 1000h 4096 Bytes

62.5.3 Command Argument register (SDHC_CMDARG)

This register contains the SD/MMC command argument.

Address: 400B_1000h base + 8h offset = 400B_1008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	CMDARG																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDHC_CMDARG field descriptions

Field	Description
CMDARG	Command Argument The SD/MMC command argument is specified as bits 39-8 of the command format in the SD or MMC specification. This register is write protected when PRSSTAT[CDIHB0] is set.

62.5.4 Transfer Type register (SDHC_XFERTYP)

This register is used to control the operation of data transfers. The host driver shall set this register before issuing a command followed by a data transfer, or before issuing a resume command. To prevent data loss, the SDHC prevents writing to the bits that are involved in the data transfer of this register, when data transfer is active. These bits are DPSEL, MBSEL, DTDSEL, AC12EN, BCEN, and DMAEN.

The host driver shall check PRSSTAT[CDIHB] and PRSSTAT[CIHB] before writing to this register. When PRSSTAT[CDIHB] is set, any attempt to send a command with data by writing to this register is ignored; when PRSSTAT[CIHB] bit is set, any write to this register is ignored.

On sending commands with data transfer involved, it is mandatory that the block size is nonzero. Besides, block count must also be nonzero, or indicated as single block transfer (bit 5 of this register is 0 when written), or block count is disabled (bit 1 of this register is 0 when written), otherwise SDHC will ignore the sending of this command and do nothing.

If the commands with data transfer does not receive the response in 64 clock cycles, that is, response time-out, SDHC will regard the external device does not accept the command and abort the data transfer. In this scenario, the driver must issue the command again to retry the transfer. It is also possible that, for some reason, the card responds to the command but SDHC does not receive the response, and if it is internal DMA (either simple DMA or ADMA) read operation, the external system memory is over-written by the internal DMA with data sent back from the card.

The following table shows the summary of how register settings determine the type of data transfer.

Table 62-2. Transfer Type register setting for various transfer types

Multi/Single block select	Block count enable	Block count	Function
0	Don't care	Don't care	Single transfer
1	0	Don't care	Infinite transfer
1	1	Positive number	Multiple transfer
1	1	Zero	No data transfer

The following table shows the relationship between XFERTYP[CICEN] and XFERTYP[CCCEN], in regards to XFERTYP[RSPTYP] as well as the name of the response type.

Table 62-3. Relationship between parameters and the name of the response type

Response type (RSPTYP)	Index check enable (CICEN)	CRC check enable (CCCEN)	Name of response type
00	0	0	No Response
01	0	1	IR2
10	0	0	R3,R4
10	1	1	R1,R5,R6
11	1	1	R1b,R5b

NOTE

- In the SDIO specification, response type notation for R5b is not defined. R5 includes R5b in the SDIO specification. But R5b is defined in this specification to specify that the SDHC will check the busy status after receiving a response. For example, usually CMD52 is used with R5, but the I/O abort command shall be used with R5b.
- The CRC field for R3 and R4 is expected to be all 1 bits. The CRC check shall be disabled for these response types.

Address: 400B_1000h base + Ch offset = 400B_100Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0		CMDINX						CMDTYP		DPSEL	CICEN	CCCEN	0	RSPTYP	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0										MSBSEL	DTDSEL	0	AC12EN	BCEN	DMAEN
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDHC_XFERTYP field descriptions

Field	Description
31–30 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
29–24 CMDINX	Command Index These bits shall be set to the command number that is specified in bits 45-40 of the command-format in the SD Memory Card Physical Layer Specification and SDIO Card Specification.

Table continues on the next page...

SDHC_XFERTYP field descriptions (continued)

Field	Description
23–22 CMDTYP	Command Type There are three types of special commands: suspend, resume, and abort. These bits shall be set to 00b for all other commands. • Suspend command: If the suspend command succeeds, the SDHC shall assume that the card bus has been released and that it is possible to issue the next command which uses the DAT line. Because the SDHC does not monitor the content of command response, it does not know if the suspend command succeeded or not. It is the host driver's responsibility to check the status of the suspend command and send another command marked as suspend to inform the SDHC that a suspend command was successfully issued. After the end bit of command is sent, the SDHC deasserts read wait for read transactions and stops checking busy for write transactions. In 4-bit mode, the interrupt cycle starts. If the suspend command fails, the SDHC will maintain its current state, and the host driver shall restart the transfer by setting PROCTL[CREQ]. • Resume command: The host driver restarts the data transfer by restoring the registers saved before sending the suspend command and then sends the resume command. The SDHC will check for a pending busy state before starting write transfers. • Abort command: If this command is set when executing a read transfer, the SDHC will stop reads to the buffer. If this command is set when executing a write transfer, the SDHC will stop driving the DAT line. After issuing the abort command, the host driver must issue a software reset (abort transaction). 00b Normal other commands. 01b Suspend CMD52 for writing bus suspend in CCCR. 10b Resume CMD52 for writing function select in CCCR. 11b Abort CMD12, CMD52 for writing I/O abort in CCCR.
21 DPSEL	Data Present Select This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: • Commands using only the CMD line, for example: CMD52. • Commands with no data transfer, but using the busy signal on DAT[0] line, R1b or R5b, for example: CMD38. **NOTE:** In resume command, this bit shall be set, and other bits in this register shall be set the same as when the transfer was initially launched.That is to say, when this bit is set, while the DTDSEL bit is 0, writes to the register Transfer Type are ignored. 0b No data present. 1b Data present.
20 CICEN	Command Index Check Enable If this bit is set to 1, the SDHC will check the index field in the response to see if it has the same value as the command index. If it is not, it is reported as a command index error. If this bit is set to 0, the index field is not checked. 0b Disable 1b Enable
19 CCCEN	Command CRC Check Enable If this bit is set to 1, the SDHC shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The number of bits checked by the CRC field value changes according to the length of the response.

Table continues on the next page...

SDHC_XFERTYP field descriptions (continued)

Field	Description
	0b Disable 1b Enable
18 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
17–16 RSPTYP	Response Type Select 00b No response. 01b Response length 136. 10b Response length 48. 11b Response length 48, check busy after response.
15–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 MSBSEL	Multi/Single Block Select Enables multiple block DAT line data transfers. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set the block count register. 0b Single block. 1b Multiple blocks.
4 DTDSEL	Data Transfer Direction Select Defines the direction of DAT line data transfers. The bit is set to 1 by the host driver to transfer data from the SD card to the SDHC and is set to 0 for all other commands. 0b Write host to card. 1b Read card to host.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 AC12EN	Auto CMD12 Enable Multiple block transfers for memory require a CMD12 to stop the transaction. When this bit is set to 1, the SDHC will issue a CMD12 automatically when the last block transfer has completed. The host driver shall not set this bit to issue commands that do not require CMD12 to stop a multiple block data transfer. In particular, secure commands defined in File Security Specification (see reference list) do not require CMD12. In single block transfer, the SDHC will ignore this bit whether it is set or not. 0b Disable 1b Enable
1 BCEN	Block Count Enable Used to enable the Block Count register, which is only relevant for multiple block transfers. When this bit is 0, the internal counter for block is disabled, which is useful in executing an infinite transfer. 0b Disable 1b Enable
0 DMAEN	DMA Enable Enables DMA functionality. If this bit is set to 1, a DMA operation shall begin when the host driver sets the DPSEL bit of this register. Whether the simple DMA, or the advanced DMA, is active depends on PROCTL[DMAS].

Table continues on the next page...

SDHC_XFERTYP field descriptions (continued)

Field	Description
	0b Disable 1b Enable

62.5.5 Command Response 0 (SDHC_CMDRSP0)

This register is used to store part 0 of the response bits from the card.

Address: 400B_1000h base + 10h offset = 400B_1010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CMDRSP0																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDHC_CMDRSP0 field descriptions

Field	Description
CMDRSP0	Command Response 0

62.5.6 Command Response 1 (SDHC_CMDRSP1)

This register is used to store part 1 of the response bits from the card.

Address: 400B_1000h base + 14h offset = 400B_1014h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CMDRSP1																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

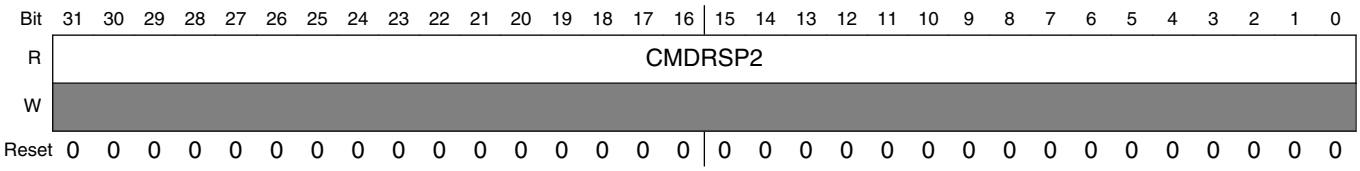
SDHC_CMDRSP1 field descriptions

Field	Description
CMDRSP1	Command Response 1

62.5.7 Command Response 2 (SDHC_CMDRSP2)

This register is used to store part 2 of the response bits from the card.

Address: 400B_1000h base + 18h offset = 400B_1018h



SDHC_CMDRSP2 field descriptions

Field	Description
CMDRSP2	Command Response 2

62.5.8 Command Response 3 (SDHC_CMDRSP3)

This register is used to store part 3 of the response bits from the card.

The following table describes the mapping of command responses from the SD bus to command response registers for each response type. In the table, R[ ] refers to a bit range within the response data as transmitted on the SD bus.

Table 62-4. Response bit definition for each response type

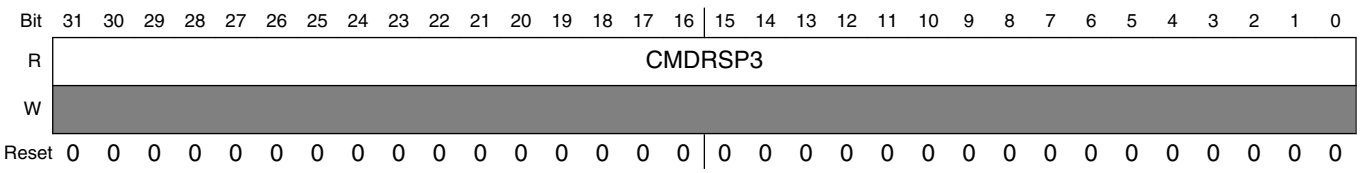
Response type	Meaning of response	Response field	Response register
R1,R1b (normal response)	Card status	R[39:8]	CMDRSP0
R1b (Auto CMD12 response)	Card status for auto CMD12	R[39:8]	CMDRSP3
R2 (CID, CSD register)	CID/CSD register [127:8]	R[127:8]	{CMDRSP3[23:0], CMDRSP2, CMDRSP1, CMDRSP0}
R3 (OCR register)	OCR register for memory	R[39:8]	CMDRSP0
R4 (OCR register)	OCR register for I/O etc.	R[39:8]	CMDRSP0
R5, R5b	SDIO response	R[39:8]	CMDRSP0
R6 (Publish RCA)	New published RCA[31:16] and card status[15:0]	R[39:9]	CMDRSP0

This table shows that most responses with a length of 48 (R[47:0]) have 32-bit of the response data (R[39:8]) stored in the CMDRSP0 register. Responses of type R1b (auto CMD12 responses) have response data bits (R[39:8]) stored in the CMDRSP3 register. Responses with length 136 (R[135:0]) have 120-bit of the response data (R[127:8]) stored in the CMDRSP0, 1, 2, and 3 registers.

To be able to read the response status efficiently, the SDHC stores only a part of the response data in the command response registers. This enables the host driver to efficiently read 32-bit of response data in one read cycle on a 32-bit bus system. Parts of the response, the index field and the CRC, are checked by the SDHC, as specified by XFERTYP[CICEN] and XFERTYP[CCCEN], and generate an error interrupt if any error is detected. The bit range for the CRC check depends on the response length. If the response length is 48, the SDHC will check R[47:1], and if the response length is 136 the SDHC will check R[119:1].

Because the SDHC may have a multiple block data transfer executing concurrently with a CMD_wo_DAT command, the SDHC stores the auto CMD12 response in the CMDRSP3 register. The CMD_wo_DAT response is stored in CMDRSP0. This allows the SDHC to avoid overwriting the Auto CMD12 response with the CMD_wo_DAT and vice versa. When the SDHC modifies part of the command response registers, as shown in the table above, it preserves the unmodified bits.

Address: 400B_1000h base + 1Ch offset = 400B_101Ch



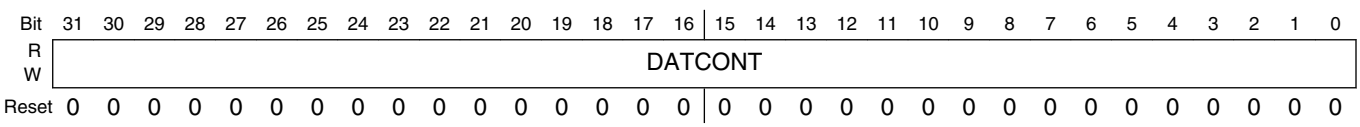
SDHC_CMDRSP3 field descriptions

Field	Description
CMDRSP3	Command Response 3

62.5.9 Buffer Data Port register (SDHC_DATPORT)

This is a 32-bit data port register used to access the internal buffer and it cannot be updated in Idle mode.

Address: 400B_1000h base + 20h offset = 400B_1020h



SDHC_DATPORT field descriptions

Field	Description
DATCONT	Data Content The Buffer Data Port register is for 32-bit data access by the CPU or the external DMA. When the internal DMA is enabled, any write to this register is ignored, and any read from this register will always yield 0s.

62.5.10 Present State register (SDHC_PRSSTAT)

The host driver can get status of the SDHC from this 32-bit read-only register.

NOTE

The host driver can issue CMD0, CMD12, CMD13 (for memory) and CMD52 (for SDIO) when the DAT lines are busy during a data transfer. These commands can be issued when Command Inhibit (CIHB) is set to zero. Other commands shall be issued when Command Inhibit (CDIHB) is set to zero. Possible changes to the SD Physical Specification may add other commands to this list in the future.

Address: 400B_1000h base + 24h offset = 400B_1024h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DLSL								CLSL	0						CINS
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				BREN	BWEN	RTA	WTA	SDOFF	PEROFF	HCKOFF	IPGOFF	SDSTB	DLA	CDIHB	CIHB
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDHC_PRSSTAT field descriptions

Field	Description
31–24 DLSL	DAT Line Signal Level Used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. The reset value is effected by the external pullup/pulldown resistors. By default, the read value of this field after reset is 8'b11110111, when DAT[3] is pulled down and the other lines are pulled up. DAT[0] Data 0 line signal level. DAT[1] Data 1 line signal level. DAT[2] Data 2 line signal level. DAT[3] Data 3 line signal level. DAT[4] Data 4 line signal level. DAT[5] Data 5 line signal level. DAT[6] Data 6 line signal level. DAT[7] Data 7 line signal level.
23 CLSL	CMD Line Signal Level Used to check the CMD line level to recover from errors, and for debugging. The reset value is effected by the external pullup/pulldown resistor, by default, the read value of this bit after reset is 1b, when the command line is pulled up.
22–17 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
16 CINS	Card Inserted Indicates whether a card has been inserted. The SDHC debounces this signal so that the host driver will not need to wait for it to stabilize. Changing from a 0 to 1 generates a card insertion interrupt in the Interrupt Status register. Changing from a 1 to 0 generates a card removal interrupt in the Interrupt Status register. A write to the force event register does not effect this bit. SYSCTL[RSTA] does not effect this bit. A software reset does not effect this bit. 0b Power on reset or no card. 1b Card inserted.
15–12 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
11 BREN	Buffer Read Enable Used for non-DMA read transfers. The SDHC may implement multiple buffers to transfer data efficiently. This read-only flag indicates that valid data exists in the host side buffer. If this bit is high, valid data greater than the watermark level exist in the buffer. This read-only flag indicates that valid data exists in the host side buffer. 0b Read disable, valid data less than the watermark level exist in the buffer. 1b Read enable, valid data greater than the watermark level exist in the buffer.
10 BWEN	Buffer Write Enable Used for non-DMA write transfers. The SDHC can implement multiple buffers to transfer data efficiently. This read-only flag indicates whether space is available for write data. If this bit is 1, valid data greater than the watermark level can be written to the buffer. This read-only flag indicates whether space is available for write data.

Table continues on the next page...

SDHC_PRSSTAT field descriptions (continued)

Field	Description
	0b Write disable, the buffer can hold valid data less than the write watermark level. 1b Write enable, the buffer can hold valid data greater than the write watermark level.
9 RTA	Read Transfer Active Used for detecting completion of a read transfer. This bit is set for either of the following conditions: • After the end bit of the read command. • When writing a 1 to PROCTL[CREQ] to restart a read transfer. A transfer complete interrupt is generated when this bit changes to 0. This bit is cleared for either of the following conditions: • When the last data block as specified by block length is transferred to the system, that is, all data are read away from SDHC internal buffer. • When all valid data blocks have been transferred from SDHC internal buffer to the system and no current block transfers are being sent as a result of the stop at block gap request being set to 1. 0b No valid data. 1b Transferring data.
8 WTA	Write Transfer Active Indicates that a write transfer is active. If this bit is 0, it means no valid write data exists in the SDHC. This bit is set in either of the following cases: • After the end bit of the write command. • When writing 1 to PROCTL[CREQ] to restart a write transfer. This bit is cleared in either of the following cases: • After getting the CRC status of the last data block as specified by the transfer count (single and multiple). • After getting the CRC status of any block where data transmission is about to be stopped by a stop at block gap request. During a write transaction, a block gap event interrupt is generated when this bit is changed to 0, as result of the stop at block gap request being set. This status is useful for the host driver in determining when to issue commands during write busy state. 0b No valid data. 1b Transferring data.
7 SDOFF	SD Clock Gated Off Internally Indicates that the SD clock is internally gated off, because of buffer over/under-run or read pause without read wait assertion, or the driver has cleared SYSCTL[SDCLKEN] to stop the SD clock. This bit is for the host driver to debug data transaction on the SD bus. 0b SD clock is active. 1b SD clock is gated off.
6 PEROFF	SDHC clock Gated Off Internally Indicates that the is internally gated off. This bit is for the host driver to debug transaction on the SD bus. When INITA bit is set, SDHC sending 80 clock cycles to the card, SDCLKEN must be 1 to enable the output card clock, otherwise the will never be gate off, so and will be always active. SDHC clockSDHC clockSDHC clockbus clock 0b SDHC clock

Table continues on the next page...

SDHC_PRSSTAT field descriptions (continued)

Field	Description
	is active. 1b SDHC clock is gated off.
5 HCKOFF	System Clock Gated Off Internally Indicates that the system clock is internally gated off. This bit is for the host driver to debug during a data transfer. 0b System clock is active. 1b System clock is gated off.
4 IPGOFF	Bus Clock Gated Off Internally Indicates that the bus clock is internally gated off. This bit is for the host driver to debug. 0b Bus clock is active. 1b Bus clock is gated off.
3 SDSTB	SD Clock Stable Indicates that the internal card clock is stable. This bit is for the host driver to poll clock status when changing the clock frequency. It is recommended to clear SYSCTL[SDCLKEN] to remove glitch on the card clock when the frequency is changing. 0b Clock is changing frequency and not stable. 1b Clock is stable.
2 DLA	Data Line Active Indicates whether one of the DAT lines on the SD bus is in use. **In the case of read transactions:** This status indicates whether a read transfer is executing on the SD bus. Changes in this value from 1 to 0, between data blocks, generates a block gap event interrupt in the Interrupt Status register. This bit will be set in either of the following cases: • After the end bit of the read command. • When writing a 1 to PROCTL[CREQ] to restart a read transfer. This bit will be cleared in either of the following cases: 1. When the end bit of the last data block is sent from the SD bus to the SDHC. 2. When the read wait state is stopped by a suspend command and the DAT2 line is released. The SDHC will wait at the next block gap by driving read wait at the start of the interrupt cycle. If the read wait signal is already driven (data buffer cannot receive data), the SDHC can wait for a current block gap by continuing to drive the read wait signal. It is necessary to support read wait to use the suspend / resume function. This bit will remain 1 during read wait. **In the case of write transactions:** This status indicates that a write transfer is executing on the SD bus. Changes in this value from 1 to 0 generate a transfer complete interrupt in the interrupt status register.

Table continues on the next page...

SDHC_PRSSTAT field descriptions (continued)

Field	Description
	This bit will be set in either of the following cases: • After the end bit of the write command. • When writing to 1 to PROCTL[CREQ] to continue a write transfer. This bit will be cleared in either of the following cases: • When the SD card releases write busy of the last data block, the SDHC will also detect if the output is not busy. If the SD card does not drive the busy signal after the CRC status is received, the SDHC shall assume the card drive "Not busy". • When the SD card releases write busy, prior to waiting for write transfer, and as a result of a stop at block gap request. **In the case of command with busy pending:** This status indicates that a busy state follows the command and the data line is in use. This bit will be cleared when the DAT0 line is released. 0b DAT line inactive. 1b DAT line active.
1 CDIHB	Command Inhibit (DAT) This status bit is generated if either the DLA or the RTA is set to 1. If this bit is 0, it indicates that the SDHC can issue the next SD/MMC Command. Commands with a busy signal belong to CDIHB, for example, R1b, R5b type. Except in the case when the command busy is finished, changing from 1 to 0 generates a transfer complete interrupt in the Interrupt Status register. **NOTE:** The SD host driver can save registers for a suspend transaction after this bit has changed from 1 to 0. 0b Can issue command which uses the DAT line. 1b Cannot issue command which uses the DAT line.
0 CIHB	Command Inhibit (CMD) If this status bit is 0, it indicates that the CMD line is not in use and the SDHC can issue a SD/MMC Command using the CMD line. This bit is set also immediately after the Transfer Type register is written. This bit is cleared when the command response is received. Even if the CDIHB bit is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a command complete interrupt in the interrupt status register. If the SDHC cannot issue the command because of a command conflict error (see command CRC error) or because of a command not issued by auto CMD12 error, this bit will remain 1 and the command complete is not set. The status of issuing an auto CMD12 does not show on this bit. 0b Can issue command using only CMD line. 1b Cannot issue command.

62.5.11 Protocol Control register (SDHC_PROCTL)

There are three cases to restart the transfer after stop at the block gap. Which case is appropriate depends on whether the SDHC issues a suspend command or the SD card accepts the suspend command:

- If the host driver does not issue a suspend command, the continue request shall be used to restart the transfer.
- If the host driver issues a suspend command and the SD card accepts it, a resume command shall be used to restart the transfer.
- If the host driver issues a suspend command and the SD card does not accept it, the continue request shall be used to restart the transfer.

Any time stop at block gap request stops the data transfer, the host driver shall wait for a transfer complete (in the interrupt status register), before attempting to restart the transfer. When restarting the data transfer by continue request, the host driver shall clear the stop at block gap request before or simultaneously.

Address: 400B_1000h base + 28h offset = 400B_1028h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0					WECRM	WECINS	WECINT	0				IABG	RWCTL	CREQ	SABGREQ
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0						DMAS		CDSS	CDTL	EMODE		D3CD	DTW		LCTL
W																
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

SDHC_PROCTL field descriptions

Field	Description
31–27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 WECRM	Wakeup Event Enable On SD Card Removal Enables a wakeup event, via IRQSTAT[CRM]. FN_WUS (Wake Up Support) in CIS does not effect this bit. When this bit is set, IRQSTAT[CRM] and the SDHC interrupt can be asserted without SD_CLK toggling. When the wakeup feature is not enabled, the SD_CLK must be active to assert IRQSTAT[CRM] and the SDHC interrupt.

Table continues on the next page...

SDHC_PROCTL field descriptions (continued)

Field	Description
	0b Disabled 1b Enabled
25 WECINS	Wakeup Event Enable On SD Card Insertion Enables a wakeup event, via IRQSTAT[CINS]. FN_WUS (Wake Up Support) in CIS does not effect this bit. When this bit is set, IRQSTATEN[CINSEN] and the SDHC interrupt can be asserted without SD_CLK toggling. When the wakeup feature is not enabled, the SD_CLK must be active to assert IRQSTATEN[CINSEN] and the SDHC interrupt. 0b Disabled 1b Enabled
24 WECINT	Wakeup Event Enable On Card Interrupt Enables a wakeup event, via IRQSTAT[CINT]. This bit can be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. When this bit is set, the card interrupt status and the SDHC interrupt can be asserted without SD_CLK toggling. When the wakeup feature is not enabled, the SD_CLK must be active to assert the card interrupt status and the SDHC interrupt. 0b Disabled 1b Enabled
23–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19 IABG	Interrupt At Block Gap Valid only in 4-bit mode, of the SDIO card, and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. Setting to 0 disables interrupt detection during a multiple block transfer. If the SDIO card can't signal an interrupt during a multiple block transfer, this bit must be set to 0 to avoid an inadvertent interrupt. When the host driver detects an SDIO card insertion, it shall set this bit according to the CCCR of the card. 0b Disabled 1b Enabled
18 RWCTL	Read Wait Control The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using the DAT[2] line. Otherwise, the SDHC has to stop the SD Clock to hold read data, which restricts commands generation. When the host driver detects an SDIO card insertion, it shall set this bit according to the CCCR of the card. If the card does not support read wait, this bit shall never be set to 1, otherwise DAT line conflicts may occur. If this bit is set to 0, stop at block gap during read operation is also supported, but the SDHC will stop the SD Clock to pause reading operation. 0b Disable read wait control, and stop SD clock at block gap when SABGREQ is set. 1b Enable read wait control, and assert read wait without stopping SD clock at block gap when SABGREQ bit is set.
17 CREQ	Continue Request Used to restart a transaction which was stopped using the PROCTL[SABGREQ]. When a suspend operation is not accepted by the card, it is also by setting this bit to restart the paused transfer. To cancel stop at the block gap, set PROCTL[SABGREQ] to 0 and set this bit to 1 to restart the transfer. The SDHC automatically clears this bit, therefore it is not necessary for the host driver to set this bit to 0. If both PROCTL[SABGREQ] and this bit are 1, the continue request is ignored.

Table continues on the next page...

SDHC_PROCTL field descriptions (continued)

Field	Description
	0b No effect. 1b Restart
16 SABGREQ	Stop At Block Gap Request Used to stop executing a transaction at the next block gap for both DMA and non-DMA transfers. Until the IRQSTATEN[TCSEN] is set to 1, indicating a transfer completion, the host driver shall leave this bit set to 1. Clearing both PROCTL[SABGREQ] and PROCTL[CREQ] does not cause the transaction to restart. Read Wait is used to stop the read transaction at the block gap. The SDHC will honor the PROCTL[SABGREQ] for write transfers, but for read transfers it requires that SDIO card support read wait. Therefore, the host driver shall not set this bit during read transfers unless the SDIO card supports read wait and has set PROCTL[RWCTL] to 1, otherwise the SDHC will stop the SD bus clock to pause the read operation during block gap. In the case of write transfers in which the host driver writes data to the data port register, the host driver shall set this bit after all block data is written. If this bit is set to 1, the host driver shall not write data to the Data Port register after a block is sent. Once this bit is set, the host driver shall not clear this bit before IRQSTATEN[TCSEN] is set, otherwise the SDHC's behavior is undefined. This bit effects PRSSTAT[RTA], PRSSTAT[WTA], and PRSSTAT[CDIHB]. 0b Transfer 1b Stop
15–10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9–8 DMAS	DMA Select This field is valid while DMA (SDMA or ADMA) is enabled and selects the DMA operation. 00 No DMA or simple DMA is selected. 01 ADMA1 is selected. 10 ADMA2 is selected. 11 Reserved
7 CDSS	Card Detect Signal Selection Selects the source for the card detection. 0b Card detection level is selected for normal purpose. 1b Card detection test level is selected for test purpose.
6 CDTL	Card Detect Test Level Enabled while the CDSS is set to 1 and it indicates card insertion. 0b Card detect test level is 0, no card inserted. 1b Card detect test level is 1, card inserted.
5–4 EMODE	Endian Mode The SDHC supports all four endian modes in data transfer. 00b Big endian mode 01b Half word big endian mode 10b Little endian mode 11b Reserved

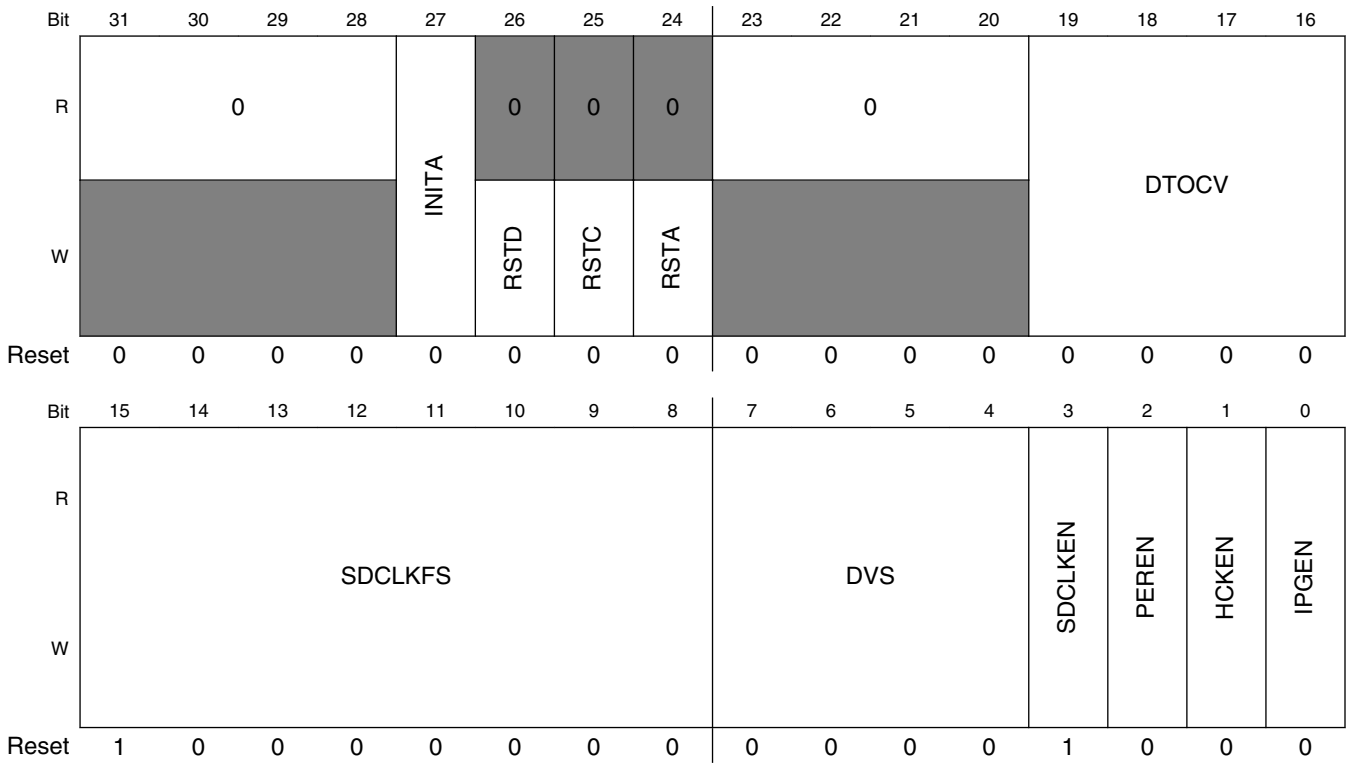
Table continues on the next page...

SDHC_PROCTL field descriptions (continued)

Field	Description
3 D3CD	DAT3 As Card Detection Pin If this bit is set, DAT3 should be pulled down to act as a card detection pin. Be cautious when using this feature, because DAT3 is also a chip-select for the SPI mode. A pulldown on this pin and CMD0 may set the card into the SPI mode, which the SDHC does not support. Note: Keep this bit set if SDIO interrupt is used. 0b DAT3 does not monitor card Insertion. 1b DAT3 as card detection pin.
2–1 DTW	Data Transfer Width Selects the data width of the SD bus for a data transfer. The host driver shall set it to match the data width of the card. Possible data transfer width is 1-bit, 4-bits or 8-bits. 00b 1-bit mode 01b 4-bit mode 10b 8-bit mode 11b Reserved
0 LCTL	LED Control This bit, fully controlled by the host driver, is used to caution the user not to remove the card while the card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all these transactions. It is not necessary to change for each transaction. When the software issues multiple SD commands, setting the bit once before the first command is sufficient: it is not necessary to reset the bit between commands. 0b LED off. 1b LED on.

62.5.12 System Control register (SDHC_SYSCTL)

Address: 400B_1000h base + 2Ch offset = 400B_102Ch



SDHC_SYSCTL field descriptions

Field	Description
31–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27 INITA	Initialization Active When this bit is set, 80 SD-clocks are sent to the card. After the 80 clocks are sent, this bit is self-cleared. This bit is very useful during the card power-up period when 74 SD-clocks are needed and the clock auto gating feature is enabled. Writing 1 to this bit when this bit is already 1 has no effect. Writing 0 to this bit at any time has no effect. When either of the PRSSTAT[CIHB] and PRSSTAT[CDIHB] bits are set, writing 1 to this bit is ignored, that is, when command line or data lines are active, write to this bit is not allowed. On the otherhand, when this bit is set, that is, during intialization active period, it is allowed to issue command, and the command bit stream will appear on the CMD pad after all 80 clock cycles are done. So when this command ends, the driver can make sure the 80 clock cycles are sent out. This is very useful when the driver needs send 80 cycles to the card and does not want to wait till this bit is self-cleared.
26 RSTD	Software Reset For DAT Line Only part of the data circuit is reset. DMA circuit is also reset. The following registers and bits are cleared by this bit: • Data Port register • Buffer Is Cleared And Initialized.Present State register • Buffer Read Enable • Buffer Write Enable • Read Transfer Active

Table continues on the next page...

SDHC_SYSCTL field descriptions (continued)

Field	Description
	• Write Transfer Active • DAT Line Active • Command Inhibit (DAT) Protocol Control register • Continue Request • Stop At Block Gap Request Interrupt Status register • Buffer Read Ready • Buffer Write Ready • DMA Interrupt • Block Gap Event • Transfer Complete 0b No reset. 1b Reset.
25 RSTC	Software Reset For CMD Line Only part of the command circuit is reset. The following registers and bits are cleared by this bit: • PRSSTAT[CIHB] • IRQSTAT[CC] 0b No reset. 1b Reset.
24 RSTA	Software Reset For ALL Effects the entire host controller except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared. During its initialization, the host driver shall set this bit to 1 to reset the SDHC. The SDHC shall reset this bit to 0 when the capabilities registers are valid and the host driver can read them. Additional use of software reset for all does not affect the value of the capabilities registers. After this bit is set, it is recommended that the host driver reset the external card and reinitialize it. 0b No reset. 1b Reset.
23–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–16 DTOCV	Data Timeout Counter Value Determines the interval by which DAT line timeouts are detected. See IRQSTAT[DTOE] for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the base clock SDCLK value by this value. The host driver can clear IRQSTATEN[DTOESEN] to prevent inadvertent time-out events. 0000b SDCLK x 2^{13} 0001b SDCLK x 2^{14} ... 1110b SDCLK x 2^{27} 1111b Reserved
15–8 SDCLKFS	SDCLK Frequency Select Used to select the frequency of the SDCLK pin. The frequency is not programmed directly. Rather this register holds the prescaler (this register) and divisor (next register) of the base clock frequency register. Setting 00h bypasses the frequency prescaler of the SD Clock. Multiple bits must not be set, or the behavior of this prescaler is undefined. The two default divider values can be calculated by the frequency of SDHC clock and the following divisor bits.

Table continues on the next page...

SDHC_SYSCTL field descriptions (continued)

Field	Description
	The frequency of SDCLK is set by the following formula: Clock frequency = (Base clock) / (prescaler x divisor) For example, if the base clock frequency is 96 MHz, and the target frequency is 25 MHz, then choosing the prescaler value of 01h and divisor value of 1h will yield 24 MHz, which is the nearest frequency less than or equal to the target. Similarly, to approach a clock value of 400 kHz, the prescaler value of 08h and divisor value of eh yields the exact clock value of 400 kHz. The reset value of this field is 80h, so if the input base clock (SDHC clock) is about 96 MHz, the default SD clock after reset is 375 kHz. According to the SD Physical Specification Version 1.1 and the SDIO Card Specification Version 1.2, the maximum SD clock frequency is 50 MHz and shall never exceed this limit. Only the following settings are allowed: 01h Base clock divided by 2. 02h Base clock divided by 4. 04h Base clock divided by 8. 08h Base clock divided by 16. 10h Base clock divided by 32. 20h Base clock divided by 64. 40h Base clock divided by 128. 80h Base clock divided by 256.
7–4 DVS	Divisor Used to provide a more exact divisor to generate the desired SD clock frequency. Note the divider can even support odd divisor without deterioration of duty cycle. The setting are as following: 0h Divisor by 1. 1h Divisor by 2. ... Eh Divisor by 15. Fh Divisor by 16.
3 SDCLKEN	SD Clock Enable The host controller shall stop SDCLK when writing this bit to 0. SDCLK frequency can be changed when this bit is 0. Then, the host controller shall maintain the same clock frequency until SDCLK is stopped (stop at SDCLK = 0). If the IRQSTAT[CINS] is cleared, this bit must be cleared by the host driver to save power.
2 PEREN	Peripheral Clock Enable If this bit is set, SDHC clock will always be active and no automatic gating is applied. Thus the SDCLK is active except for when auto gating-off during buffer danger (buffer about to over-run or under-run). When this bit is cleared, the SDHC clock will be automatically off whenever there is no transaction on the SD bus. Because this bit is only a feature enabling bit, clearing this bit does not stop SDCLK immediately. The SDHC clock will be internally gated off, if none of the following factors are met: • The cmd part is reset, or • Data part is reset, or • A soft reset, or • The cmd is about to send, or • Clock divisor is just updated, or • Continue request is just set, or • This bit is set, or • Card insertion is detected, or • Card removal is detected, or

Table continues on the next page...

SDHC_SYSCTL field descriptions (continued)

Field	Description
	• Card external interrupt is detected, or • 80 clocks for initialization phase is ongoing 0b SDHC clock will be internally gated off. 1b SDHC clock will not be automatically gated off.
1 HCKEN	System Clock Enable If this bit is set, system clock will always be active and no automatic gating is applied. When this bit is cleared, system clock will be automatically off when no data transfer is on the SD bus. 0b System clock will be internally gated off. 1b System clock will not be automatically gated off.
0 IPGEN	IPG Clock Enable If this bit is set, bus clock will always be active and no automatic gating is applied. The bus clock will be internally gated off, if none of the following factors are met: • The cmd part is reset, or • Data part is reset, or • Soft reset, or • The cmd is about to send, or • Clock divisor is just updated, or • Continue request is just set, or • This bit is set, or • Card insertion is detected, or • Card removal is detected, or • Card external interrupt is detected, or • The SDHC clock is not gated off **NOTE:** The bus clock will not be auto gated off if the SDHC clock is not gated off. So clearing only this bit has no effect unless the PEREN bit is also cleared. 0b Bus clock will be internally gated off. 1b Bus clock will not be automatically gated off.

62.5.13 Interrupt Status register (SDHC_IRQSTAT)

An interrupt is generated when the Normal Interrupt Signal Enable is enabled and at least one of the status bits is set to 1. For all bits, writing 1 to a bit clears it; writing to 0 keeps the bit unchanged. More than one status can be cleared with a single register write. For Card Interrupt, before writing 1 to clear, it is required that the card stops asserting the interrupt, meaning that when the Card Driver services the interrupt condition, otherwise the CINT bit will be asserted again.

The table below shows the relationship between the CTOE and the CC bits.

Table 62-5. SDHC status for CTOE/CC bit combinations

Command complete	Command timeout error	Meaning of the status
0	0	X
X	1	Response not received within 64 SDCLK cycles
1	0	Response received

The table below shows the relationship between the Transfer Complete and the Data Timeout Error.

Table 62-6. SDHC status for data timeout error/transfer complete bit combinations

Transfer complete	Data timeout error	Meaning of the status
0	0	X
0	1	Timeout occurred during transfer
1	X	Data transfer complete

The table below shows the relationship between the command CRC Error (CCE) and Command Timeout Error (CTOE).

Table 62-7. SDHC status for CCE/CTOE Bit Combinations

Command complete	Command timeout error	Meaning of the status
0	0	No error
0	1	Response timeout error
1	0	Response CRC error
1	1	CMD line conflict

Address: 400B_1000h base + 30h offset = 400B_1030h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0			DMAE	0			AC12E	0	DEBE	DCE	DTOE	CIE	CEBE	CCE	CTOE
W				w1c				w1c		w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0							CINT	CRM	CINS	BRR	BWR	DINT	BGE	TC	CC
W								w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDHC_IRQSTAT field descriptions

Field	Description
31–29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28 DMAE	DMA Error Occurs when an Internal DMA transfer has failed. This bit is set to 1, when some error occurs in the data transfer. This error can be caused by either Simple DMA or ADMA, depending on which DMA is in use. The value in DMA System Address register is the next fetch address where the error occurs. Because any error corrupts the whole data block, the host driver shall restart the transfer from the corrupted block boundary. The address of the block boundary can be calculated either from the current DSADDR value or from the remaining number of blocks and the block size. 0b No error. 1b Error.
27–25 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
24 AC12E	Auto CMD12 Error Occurs when detecting that one of the bits in the Auto CMD12 Error Status register has changed from 0 to 1. This bit is set to 1, not only when the errors in Auto CMD12 occur, but also when the Auto CMD12 is not executed due to the previous command error. 0b No error. 1b Error.
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 DEBE	Data End Bit Error Occurs either when detecting 0 at the end bit position of read data, which uses the DAT line, or at the end bit position of the CRC. 0b No error. 1b Error.
21 DCE	Data CRC Error Occurs when detecting a CRC error when transferring read data, which uses the DAT line, or when detecting the Write CRC status having a value other than 010. 0b No error. 1b Error.

Table continues on the next page...

SDHC_IRQSTAT field descriptions (continued)

Field	Description
20 DTOE	Data Timeout Error Occurs when detecting one of following time-out conditions. • Busy time-out for R1b,R5b type • Busy time-out after Write CRC status • Read Data time-out 0b No error. 1b Time out.
19 CIE	Command Index Error Occurs if a Command Index error occurs in the command response. 0b No error. 1b Error.
18 CEBE	Command End Bit Error Occurs when detecting that the end bit of a command response is 0. 0b No error. 1b End Bit Error generated.
17 CCE	Command CRC Error Command CRC Error is generated in two cases. • If a response is returned and the Command Timeout Error is set to 0, indicating no time-out, this bit is set when detecting a CRC error in the command response. • The SDHC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the SDHC drives the CMD line to 1, but detects 0 on the CMD line at the next SDCLK edge, then the SDHC shall abort the command (Stop driving CMD line) and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict. 0b No error. 1b CRC Error generated.
16 CTOE	Command Timeout Error Occurs only if no response is returned within 64 SDCLK cycles from the end bit of the command. If the SDHC detects a CMD line conflict, in which case a Command CRC Error shall also be set, this bit shall be set without waiting for 64 SDCLK cycles. This is because the command will be aborted by the SDHC. 0b No error. 1b Time out.
15–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 CINT	Card Interrupt This status bit is set when an interrupt signal is detected from the external card. In 1-bit mode, the SDHC will detect the Card Interrupt without the SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so the interrupt from card can only be sampled during interrupt cycle, introducing some delay between the interrupt signal from the SDIO card and the interrupt to the host system. Writing this bit to 1 can clear this bit, but as the interrupt factor from the SDIO card does not clear, this bit is set again. To clear this bit, it is required to reset the interrupt factor from the external card followed by a writing 1 to this bit.

Table continues on the next page...

SDHC_IRQSTAT field descriptions (continued)

Field	Description
	When this status has been set, and the host driver needs to service this interrupt, the Card Interrupt Signal Enable in the Interrupt Signal Enable register should be 0 to stop driving the interrupt signal to the host system. After completion of the card interrupt service (it must reset the interrupt factors in the SDIO card and the interrupt signal may not be asserted), write 1 to clear this bit, set the Card Interrupt Signal Enable to 1, and start sampling the interrupt signal again. 0b No Card Interrupt. 1b Generate Card Interrupt.
7 CRM	Card Removal This status bit is set if the Card Inserted bit in the Present State register changes from 1 to 0. When the host driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register must be confirmed. Because the card state may possibly be changed when the host driver clears this bit and the interrupt event may not be generated. When this bit is cleared, it will be set again if no card is inserted. To leave it cleared, clear the Card Removal Status Enable bit in Interrupt Status Enable register. 0b Card state unstable or inserted. 1b Card removed.
6 CINS	Card Insertion This status bit is set if the Card Inserted bit in the Present State register changes from 0 to 1. When the host driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register must be confirmed. Because the card state may possibly be changed when the host driver clears this bit and the interrupt event may not be generated. When this bit is cleared, it will be set again if a card is inserted. To leave it cleared, clear the Card Inserted Status Enable bit in Interrupt Status Enable register. 0b Card state unstable or removed. 1b Card inserted.
5 BRR	Buffer Read Ready This status bit is set if the Buffer Read Enable bit, in the Present State register, changes from 0 to 1. See the Buffer Read Enable bit in the Present State register for additional information. 0b Not ready to read buffer. 1b Ready to read buffer.
4 BWR	Buffer Write Ready This status bit is set if the Buffer Write Enable bit, in the Present State register, changes from 0 to 1. See the Buffer Write Enable bit in the Present State register for additional information. 0b Not ready to write buffer. 1b Ready to write buffer.
3 DINT	DMA Interrupt Occurs only when the internal DMA finishes the data transfer successfully. Whenever errors occur during data transfer, this bit will not be set. Instead, the DMAE bit will be set. Either Simple DMA or ADMA finishes data transferring, this bit will be set. 0b No DMA Interrupt. 1b DMA Interrupt is generated.

Table continues on the next page...

SDHC_IRQSTAT field descriptions (continued)

Field	Description
2 BGE	Block Gap Event If PROCTL[SABGREQ] is set, this bit is set when a read or write transaction is stopped at a block gap. If PROCTL[SABGREQ] is not set to 1, this bit is not set to 1. In the case of a read transaction: This bit is set at the falling edge of the DAT line active status, when the transaction is stopped at SD Bus timing. The read wait must be supported in order to use this function. In the case of write transaction: This bit is set at the falling edge of write transfer active status, after getting CRC status at SD bus timing. 0b No block gap event. 1b Transaction stopped at block gap.
1 TC	Transfer Complete This bit is set when a read or write transfer is completed. In the case of a read transaction: This bit is set at the falling edge of the read transfer active status. There are two cases in which this interrupt is generated. The first is when a data transfer is completed as specified by the data length, after the last data has been read to the host system. The second is when data has stopped at the block gap and completed the data transfer by setting PROCTL[SABGREQ], after valid data has been read to the host system. In the case of a write transaction: This bit is set at the falling edge of the DAT line active status. There are two cases in which this interrupt is generated. The first is when the last data is written to the SD card as specified by the data length and the busy signal is released. The second is when data transfers are stopped at the block gap, by setting PROCTL[SABGREQ], and the data transfers are completed,after valid data is written to the SD card and the busy signal released. 0b Transfer not complete. 1b Transfer complete.
0 CC	Command Complete This bit is set when you receive the end bit of the command response, except Auto CMD12. See PRSSTAT[CIHB]. 0b Command not complete. 1b Command complete.

62.5.14 Interrupt Status Enable register (SDHC_IRQSTATEN)

Setting the bits in this register to 1 enables the corresponding interrupt status to be set by the specified event. If any bit is cleared, the corresponding interrupt status bit is also cleared, that is, when the bit in this register is cleared, the corresponding bit in interrupt status register is always 0.

NOTE

- Depending on PROCTL[IABG] bit setting, SDHC may be programmed to sample the card interrupt signal during the interrupt period and hold its value in the flip-flop. There will be some delays on the card interrupt, asserted from the card, to the time the host system is informed.
- To detect a CMD line conflict, the host driver must set both IRQSTATEN[CTOESEN] and IRQSTATEN[CCESEN] to 1.

Address: 400B_1000h base + 34h offset = 400B_1034h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0			DMAESEN	0			AC12ESEN	0	DEBESEN	DCESEN	DTOESEN	CIESEN	CEBESEN	CCESEN	CTOESEN
W																
Reset	0	0	0	1	0	0	0	1	0	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0							CINTSEN	CRMSEN	CINSEN	BRRSEN	BWRSEN	DINTSEN	BGESEN	TCSEN	CCSEN
W																
Reset	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

SDHC_IRQSTATEN field descriptions

Field	Description
31–29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28 DMAESEN	DMA Error Status Enable 0b Masked 1b Enabled
27–25 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
24 AC12ESEN	Auto CMD12 Error Status Enable 0b Masked 1b Enabled
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 DEBESEN	Data End Bit Error Status Enable 0b Masked 1b Enabled

Table continues on the next page...

SDHC_IRQSTATEN field descriptions (continued)

Field	Description
21 DCESEN	Data CRC Error Status Enable 0b Masked 1b Enabled
20 DTOESEN	Data Timeout Error Status Enable 0b Masked 1b Enabled
19 CIESEN	Command Index Error Status Enable 0b Masked 1b Enabled
18 CEBESEN	Command End Bit Error Status Enable 0b Masked 1b Enabled
17 CCESEN	Command CRC Error Status Enable 0b Masked 1b Enabled
16 CTOESEN	Command Timeout Error Status Enable 0b Masked 1b Enabled
15–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 CINTSEN	Card Interrupt Status Enable If this bit is set to 0, the SDHC will clear the interrupt request to the system. The card interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1. The host driver must clear the this bit before servicing the card interrupt and must set this bit again after all interrupt requests from the card are cleared to prevent inadvertent interrupts. 0b Masked 1b Enabled
7 CRMSEN	Card Removal Status Enable 0b Masked 1b Enabled
6 CINSEN	Card Insertion Status Enable 0b Masked 1b Enabled
5 BRRSEN	Buffer Read Ready Status Enable 0b Masked 1b Enabled
4 BWRSEN	Buffer Write Ready Status Enable

Table continues on the next page...

SDHC_IRQSTATEN field descriptions (continued)

Field	Description
	0b Masked 1b Enabled
3 DINTSEN	DMA Interrupt Status Enable 0b Masked 1b Enabled
2 BGESEN	Block Gap Event Status Enable 0b Masked 1b Enabled
1 TCSEN	Transfer Complete Status Enable 0b Masked 1b Enabled
0 CCSEN	Command Complete Status Enable 0b Masked 1b Enabled

62.5.15 Interrupt Signal Enable register (SDHC_IRQSIGEN)

This register is used to select which interrupt status is indicated to the host system as the interrupt. All of these status bits share the same interrupt line. Setting any of these bits to 1 enables interrupt generation. The corresponding status register bit will generate an interrupt when the corresponding interrupt signal enable bit is set.

Address: 400B_1000h base + 38h offset = 400B_1038h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0			DMAEIEN	0			AC12EIEN	0	DEBEIEN	DCEIEN	DTOEIEN	CIEIEN	CEBEIEN	CCEIEN	CTOEIEN
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0							CINTIEN	CRMIEN	CINSIEN	BRRIEN	BWRIEN	DINTIEN	BGEIEN	TCIEN	CCIEN
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDHC_IRQSIGEN field descriptions

Field	Description
31–29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28 DMAEIEN	DMA Error Interrupt Enable 0b Masked 1b Enabled
27–25 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
24 AC12EIEN	Auto CMD12 Error Interrupt Enable 0b Masked 1b Enabled
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 DEBEIEN	Data End Bit Error Interrupt Enable 0b Masked 1b Enabled
21 DCEIEN	Data CRC Error Interrupt Enable 0b Masked 1b Enabled
20 DTOEIEN	Data Timeout Error Interrupt Enable 0b Masked 1b Enabled
19 CIEIEN	Command Index Error Interrupt Enable 0b Masked 1b Enabled
18 CEBEIEN	Command End Bit Error Interrupt Enable 0b Masked 1b Enabled
17 CCEIEN	Command CRC Error Interrupt Enable 0b Masked 1b Enabled
16 CTOEIEN	Command Timeout Error Interrupt Enable 0b Masked 1b Enabled
15–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 CINTIEN	Card Interrupt Enable 0b Masked 1b Enabled

Table continues on the next page...

SDHC_IRQSIGEN field descriptions (continued)

Field	Description
7 CRMIEN	Card Removal Interrupt Enable 0b Masked 1b Enabled
6 CINSIEN	Card Insertion Interrupt Enable 0b Masked 1b Enabled
5 BRRIEN	Buffer Read Ready Interrupt Enable 0b Masked 1b Enabled
4 BWRIEN	Buffer Write Ready Interrupt Enable 0b Masked 1b Enabled
3 DINTIEN	DMA Interrupt Enable 0b Masked 1b Enabled
2 BGEIEN	Block Gap Event Interrupt Enable 0b Masked 1b Enabled
1 TCIEN	Transfer Complete Interrupt Enable 0b Masked 1b Enabled
0 CCIEN	Command Complete Interrupt Enable 0b Masked 1b Enabled

62.5.16 Auto CMD12 Error Status Register (SDHC_AC12ERR)

When the AC12ESEN bit in the Status register is set, the host driver shall check this register to identify what kind of error the Auto CMD12 indicated. This register is valid only when the Auto CMD12 Error status bit is set.

The following table shows the relationship between the Auto CMGD12 CRC error and the Auto CMD12 command timeout error.

Table 62-8. Relationship between Command CRC Error and Command Timeout Error For Auto CMD12

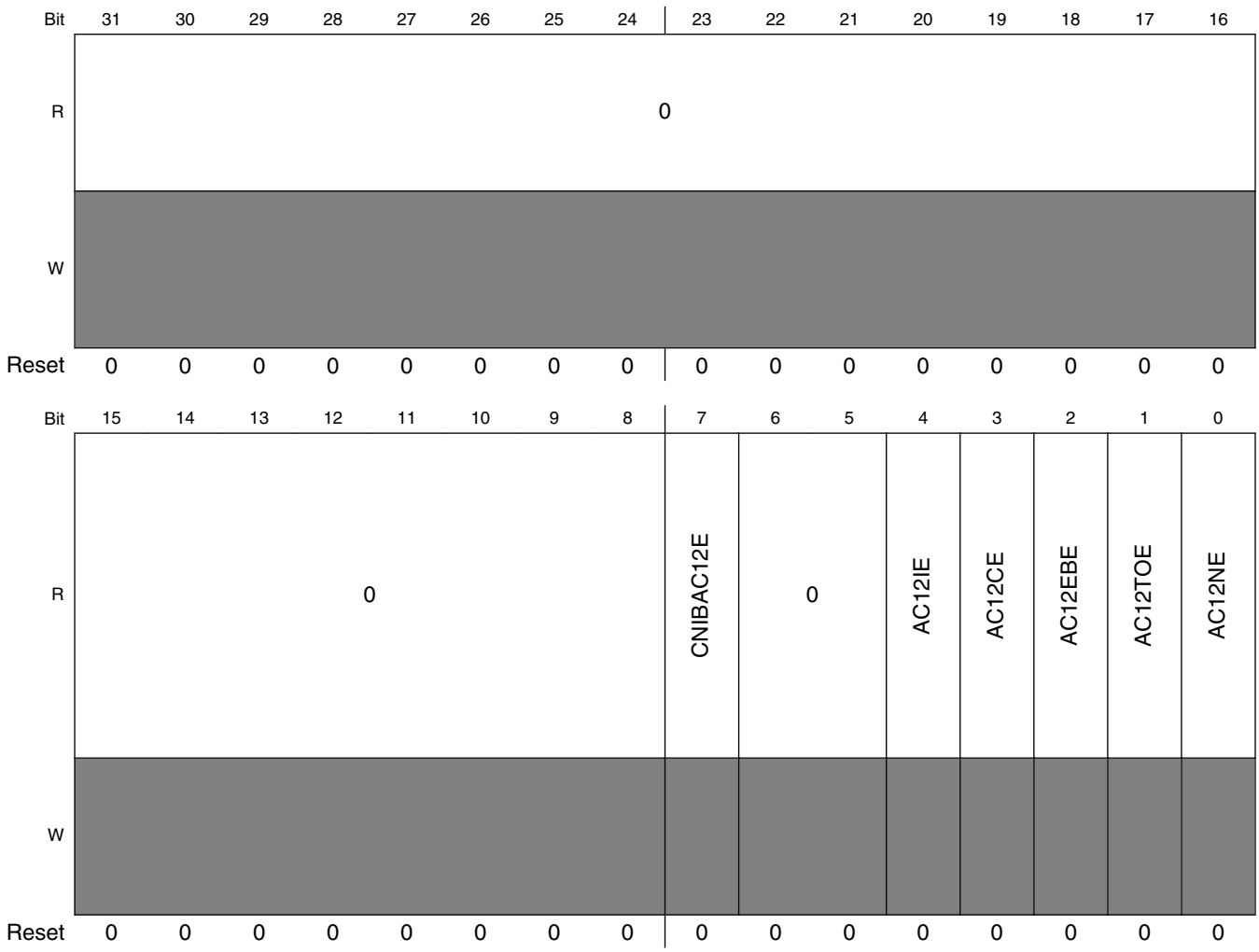
Auto CMD12 CRC error	Auto CMD12 timeout error	Type of error
0	0	No error
0	1	Response timeout error
1	0	Response CRC error
1	1	CMD line conflict

Changes in Auto CMD12 Error Status register can be classified in three scenarios:

1. When the SDHC is going to issue an Auto CMD12:
   - Set bit 0 to 1 if the Auto CMD12 can't be issued due to an error in the previous command.
   - Set bit 0 to 0 if the auto CMD12 is issued.
2. At the end bit of an auto CMD12 response:
   - Check errors corresponding to bits 1-4.
   - Set bits 1-4 corresponding to detected errors.
   - Clear bits 1-4 corresponding to detected errors.
3. Before reading the Auto CMD12 error status bit 7:
   - Set bit 7 to 1 if there is a command that can't be issued.
   - Clear bit 7 if there is no command to issue.

The timing for generating the auto CMD12 error and writing to the command register are asynchronous. After that, bit 7 shall be sampled when the driver is not writing to the command register. So it is suggested to read this register only when IRQSTAT[AC12E] is set. An Auto CMD12 error interrupt is generated when one of the error bits (0-4) is set to 1. The command not issued by auto CMD12 error does not generate an interrupt.

Address: 400B_1000h base + 3Ch offset = 400B_103Ch



SDHC_AC12ERR field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 CNIBAC12E	Command Not Issued By Auto CMD12 Error Setting this bit to 1 means CMD_wo_DAT is not executed due to an auto CMD12 error (D04-D01) in this register. 0b No error. 1b Not issued.
6–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 AC12IE	Auto CMD12 Index Error Occurs if the command index error occurs in response to a command. 0b No error. 1b Error, the CMD index in response is not CMD12.

Table continues on the next page...

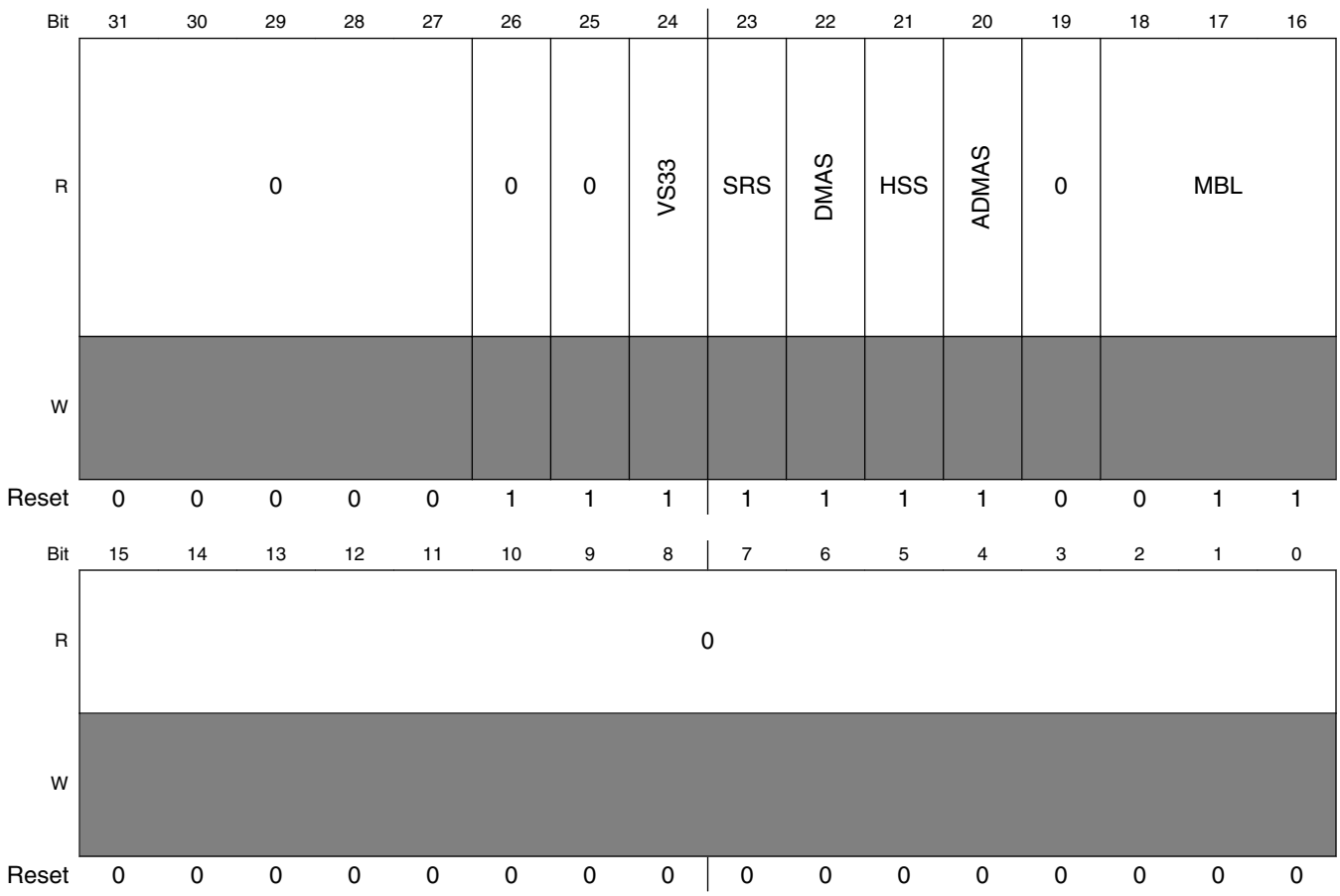
SDHC_AC12ERR field descriptions (continued)

Field	Description
3 AC12CE	Auto CMD12 CRC Error Occurs when detecting a CRC error in the command response. 0b No CRC error. 1b CRC error met in Auto CMD12 response.
2 AC12EBE	Auto CMD12 End Bit Error Occurs when detecting that the end bit of command response is 0 which must be 1. 0b No error. 1b End bit error generated.
1 AC12TOE	Auto CMD12 Timeout Error Occurs if no response is returned within 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, the other error status bits (2-4) have no meaning. 0b No error. 1b Time out.
0 AC12NE	Auto CMD12 Not Executed If memory multiple block data transfer is not started, due to a command error, this bit is not set because it is not necessary to issue an auto CMD12. Setting this bit to 1 means the SDHC cannot issue the auto CMD12 to stop a memory multiple block data transfer due to some error. If this bit is set to 1, other error status bits (1-4) have no meaning. 0b Executed. 1b Not executed.

62.5.17 Host Controller Capabilities (SDHC_HTCAPBLT)

This register provides the host driver with information specific to the SDHC implementation. The value in this register is the power-on-reset value, and does not change with a software reset. Any write to this register is ignored.

Address: 400B_1000h base + 40h offset = 400B_1040h



SDHC_HTCAPBLT field descriptions

Field	Description
31–27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
24 VS33	Voltage Support 3.3 V This bit shall depend on the host system ability.

Table continues on the next page...

SDHC_HTCAPBLT field descriptions (continued)

Field	Description
	0b 3.3 V not supported. 1b 3.3 V supported.
23 SRS	Suspend/Resume Support This bit indicates whether the SDHC supports suspend / resume functionality. If this bit is 0, the suspend and resume mechanism, as well as the read Wwait, are not supported, and the host driver shall not issue either suspend or resume commands. 0b Not supported. 1b Supported.
22 DMAS	DMA Support This bit indicates whether the SDHC is capable of using the internal DMA to transfer data between system memory and the data buffer directly. 0b DMA not supported. 1b DMA supported.
21 HSS	High Speed Support This bit indicates whether the SDHC supports high speed mode and the host system can supply a SD Clock frequency from 25 MHz to 50 MHz. 0b High speed not supported. 1b High speed supported.
20 ADMAS	ADMA Support This bit indicates whether the SDHC supports the ADMA feature. 0b Advanced DMA not supported. 1b Advanced DMA supported.
19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18–16 MBL	Max Block Length This value indicates the maximum block size that the host driver can read and write to the buffer in the SDHC. The buffer shall transfer block size without wait cycles. 000b 512 bytes 001b 1024 bytes 010b 2048 bytes 011b 4096 bytes
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

62.5.18 Watermark Level Register (SDHC_WML)

Both write and read watermark levels (FIFO threshold) are configurable. There value can range from 1 to 128 words. Both write and read burst lengths are also configurable. There value can range from 1 to 31 words.

Address: 400B_1000h base + 44h offset = 400B_1044h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0			0					WRWML								0			0					RDWML							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

SDHC_WML field descriptions

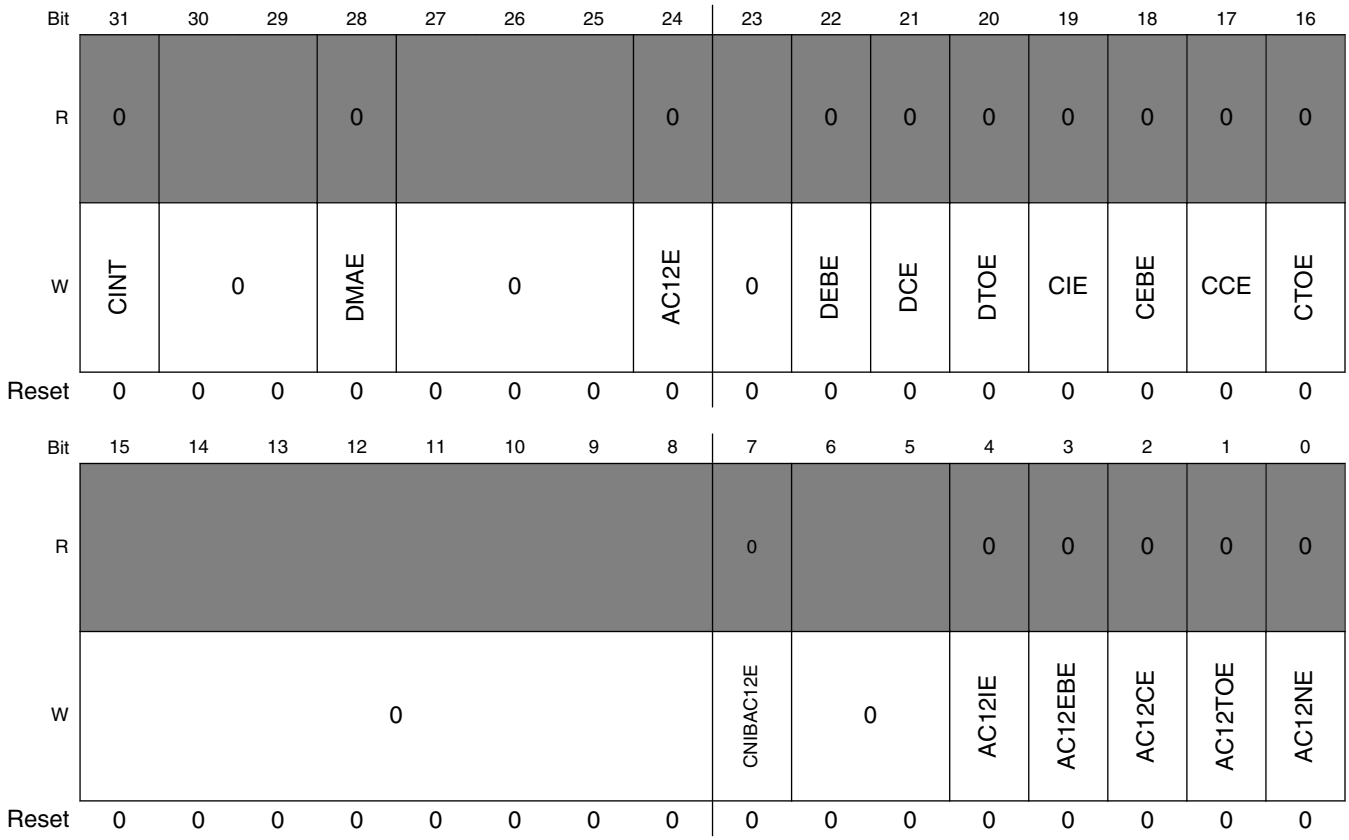
Field	Description
31–29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23–16 WRWML	Write Watermark Level The number of words used as the watermark level (FIFO threshold) in a DMA write operation. Also the number of words as a sequence of write bursts in back-to-back mode. The maximum legal value for the write watermark level is 128.
15–13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
RDWML	Read Watermark Level The number of words used as the watermark level (FIFO threshold) in a DMA read operation. Also the number of words as a sequence of read bursts in back-to-back mode. The maximum legal value for the read water mark level is 128.

62.5.19 Force Event register (SDHC_FEVT)

The Force Event (FEVT) register is not a physically implemented register. Rather, it is an address at which the Interrupt Status register can be written if the corresponding bit of the Interrupt Status Enable register is set. This register is a write only register and writing 0 to it has no effect. Writing 1 to this register actually sets the corresponding bit of Interrupt Status register. A read from this register always results in 0's. To change the corresponding status bits in the interrupt status register, make sure to set SYSCTL[IPGEN] so that bus clock is always active.

Forcing a card interrupt will generate a short pulse on the DAT[1] line, and the driver may treat this interrupt as a normal interrupt. The interrupt service routine may skip polling the card interrupt factor as the interrupt is selfcleared.

Address: 400B_1000h base + 50h offset = 400B_1050h



SDHC_FEVT field descriptions

Field	Description
31 CINT	Force Event Card Interrupt Writing 1 to this bit generates a short low-level pulse on the internal DAT[1] line, as if a self-clearing interrupt was received from the external card. If enabled, the CINT bit will be set and the interrupt service routine may treat this interrupt as a normal interrupt from the external card.
30–29 Reserved	This field is reserved.
28 DMAE	Force Event DMA Error Forces the DMAE bit of Interrupt Status Register to be set.
27–25 Reserved	This field is reserved.
24 AC12E	Force Event Auto Command 12 Error Forces IRQSTAT[AC12E] to be set.
23 Reserved	This field is reserved.

Table continues on the next page...

SDHC_FEVT field descriptions (continued)

Field	Description
22 DEBE	Force Event Data End Bit Error Forces IRQSTAT[DEBE] to be set.
21 DCE	Force Event Data CRC Error Forces IRQSTAT[DCE] to be set.
20 DTOE	Force Event Data Time Out Error Forces IRQSTAT[DTOE] to be set.
19 CIE	Force Event Command Index Error Forces IRQSTAT[CCE] to be set.
18 CEBE	Force Event Command End Bit Error Forces IRQSTAT[CEBE] to be set.
17 CCE	Force Event Command CRC Error Forces IRQSTAT[CCE] to be set.
16 CTOE	Force Event Command Time Out Error Forces IRQSTAT[CTOE] to be set.
15–8 Reserved	This field is reserved.
7 CNIBAC12E	Force Event Command Not Executed By Auto Command 12 Error Forces AC12ERR[CNIBAC12E] to be set.
6–5 Reserved	This field is reserved.
4 AC12IE	Force Event Auto Command 12 Index Error Forces AC12ERR[AC12IE] to be set.
3 AC12EBE	Force Event Auto Command 12 End Bit Error Forces AC12ERR[AC12EBE] to be set.
2 AC12CE	Force Event Auto Command 12 CRC Error Forces AC12ERR[AC12CE] to be set.
1 AC12TOE	Force Event Auto Command 12 Time Out Error Forces AC12ERR[AC12TOE] to be set.
0 AC12NE	Force Event Auto Command 12 Not Executed Forces AC12ERR[AC12NE] to be set.

62.5.20 ADMA Error Status register (SDHC_ADMAES)

When an ADMA error interrupt has occurred, the ADMA Error States field in this register holds the ADMA state and the ADMA System Address register holds the address around the error descriptor.

For recovering from this error, the host driver requires the ADMA state to identify the error descriptor address as follows:

- ST_STOP: Previous location set in the ADMA System Address register is the error descriptor address.
- ST_FDS: Current location set in the ADMA System Address register is the error descriptor address.
- ST_CADR: This state is never set because it only increments the descriptor pointer and doesn't generate an ADMA error.
- ST_TFR: Previous location set in the ADMA System Address register is the error descriptor address.

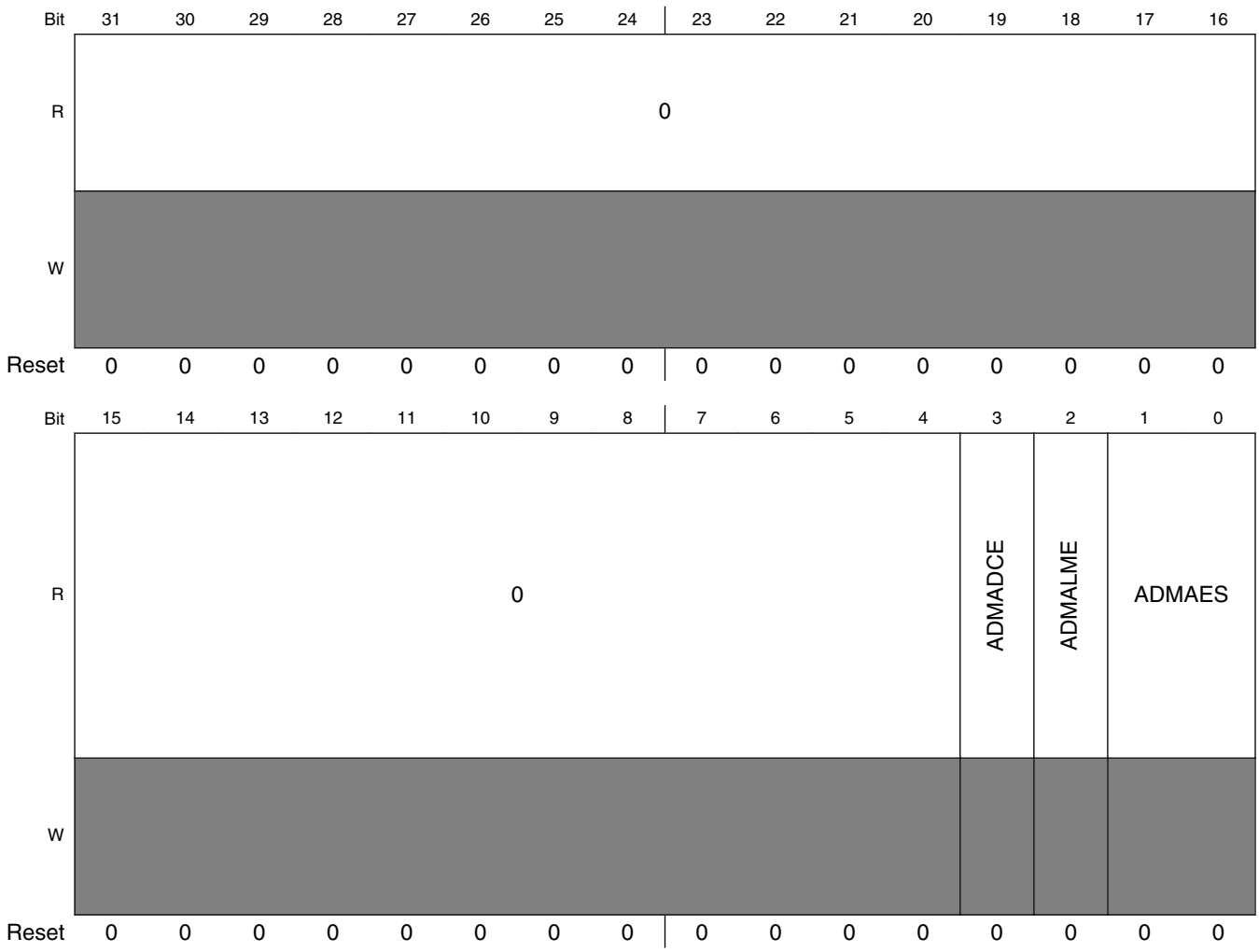
In case of a write operation, the host driver must use the ACMD22 to get the number of the written block, rather than using this information, because unwritten data may exist in the host controller.

The host controller generates the ADMA error interrupt when it detects invalid descriptor data (valid = 0) in the ST_FDS state. The host driver can distinguish this error by reading the valid bit of the error descriptor.

Table 62-9. ADMA Error State coding

D01-D00	ADMA Error State when error has occurred	Contents of ADMA System Address register
00	ST_STOP (Stop DMA)	Holds the address of the next executable descriptor command
01	ST_FDS (fetch descriptor)	Holds the valid descriptor address
10	ST_CADR (change address)	No ADMA error is generated
11	ST_TFR (Transfer Data)	Holds the address of the next executable descriptor command

Address: 400B_1000h base + 54h offset = 400B_1054h



SDHC_ADMAES field descriptions

Field	Description
31–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 ADMADCE	ADMA Descriptor Error This error occurs when an invalid descriptor is fetched by ADMA. 0b No error. 1b Error.
2 ADMALME	ADMA Length Mismatch Error This error occurs in the following 2 cases: • While the block count enable is being set, the total data length specified by the descriptor table is different from that specified by the block count and block length. • Total data length can not be divided by the block length. 0b No error. 1b Error.

Table continues on the next page...

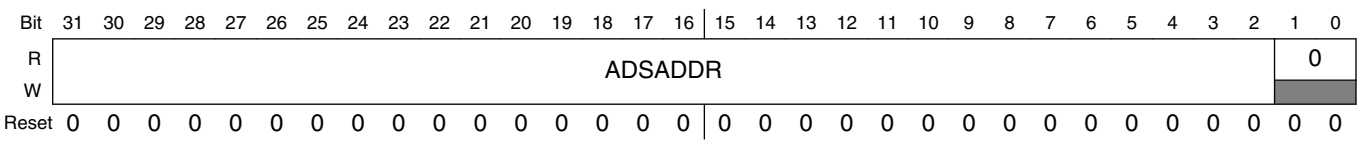
SDHC_ADMAES field descriptions (continued)

Field	Description
ADMAES	ADMA Error State (When ADMA Error Is Occurred.) Indicates the state of the ADMA when an error has occurred during an ADMA data transfer.

62.5.21 ADMA System Addressregister (SDHC_ADSADDR)

This register contains the physical system memory address used for ADMA transfers.

Address: 400B_1000h base + 58h offset = 400B_1058h



SDHC_ADSADDR field descriptions

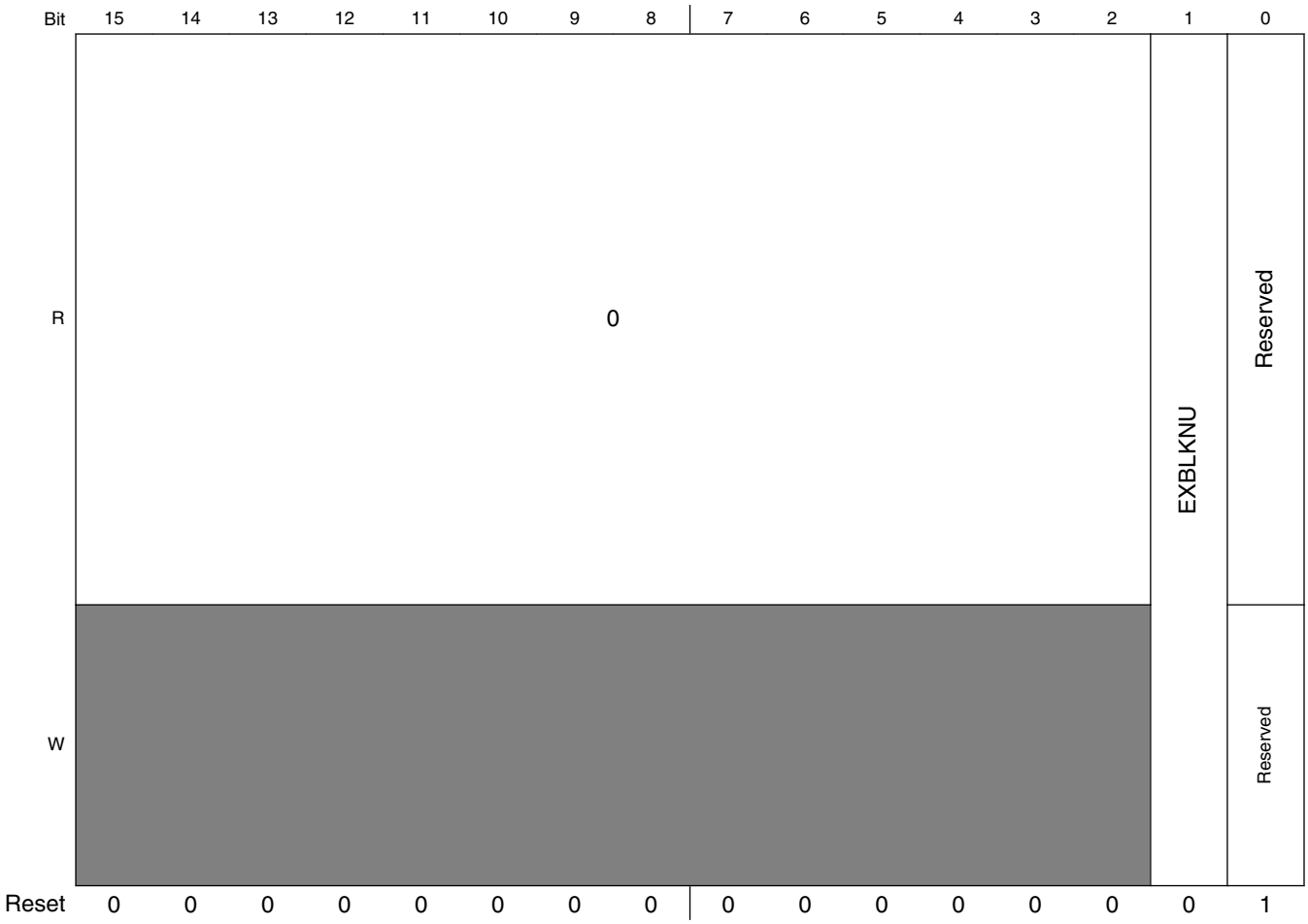
Field	Description
31–2 ADSADDR	ADMA System Address Holds the word address of the executing command in the descriptor table. At the start of ADMA, the host driver shall set the start address of the Descriptor table. The ADMA engine increments this register address whenever fetching a descriptor command. When the ADMA is stopped at the block gap, this register indicates the address of the next executable descriptor command. When the ADMA error interrupt is generated, this register shall hold the valid descriptor address depending on the ADMA state. The lower 2 bits of this register is tied to '0' so the ADMA address is always word-aligned. Because this register supports dynamic address reflecting, when TC bit is set, it automatically alters the value of internal address counter, so SW cannot change this register when TC bit is set.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

62.5.22 Vendor Specific register (SDHC_VENDOR)

This register contains the vendor-specific control/status register.

Address: 400B_1000h base + C0h offset = 400B_10C0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0				0				INTSTVAL							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



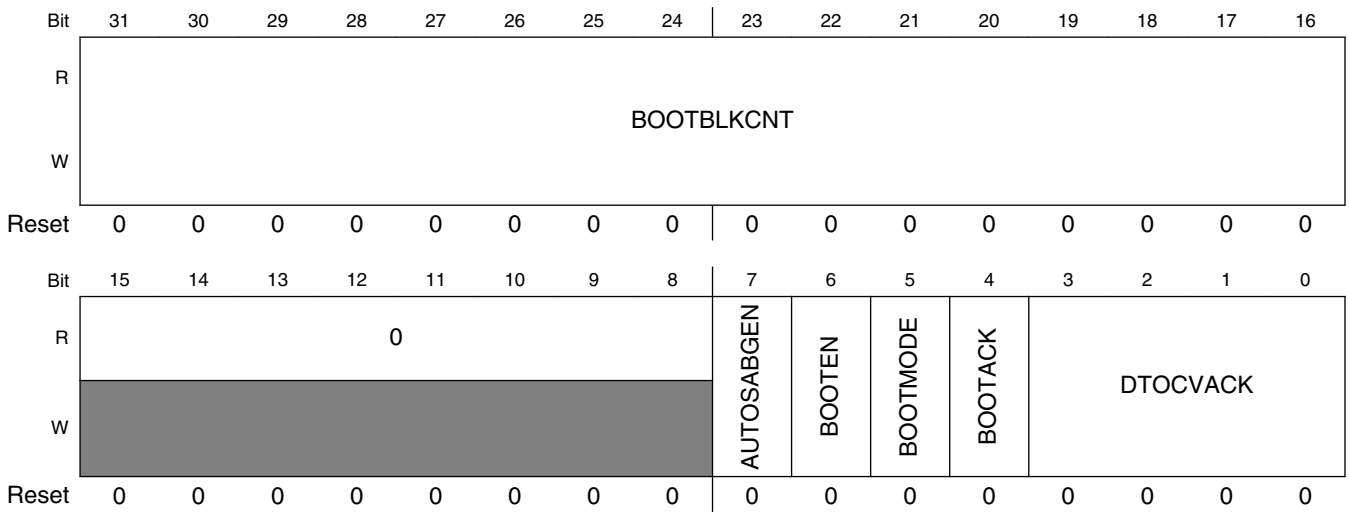
SDHC_VENDOR field descriptions

Field	Description
31–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23–16 INTSTVAL	Internal State Value Internal state value, reflecting the corresponding state value selected by **Debug Select** field. This field is read-only and write to this field does not have effect.
15–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 EXBLKNU	Exact Block Number Block Read Enable For SDIO CMD53 This bit must be set before S/W issues CMD53 multi-block read with exact block number. This bit must not be set if the CMD53 multi-block read is not exact block number. 0 None exact block read. 1 Exact block read for SDIO CMD53.
0 Reserved	This field is reserved.

62.5.23 MMC Boot register (SDHC_MMCBOOT)

This register contains the MMC fast boot control register.

Address: 400B_1000h base + C4h offset = 400B_10C4h



SDHC_MMCBOOT field descriptions

Field	Description
31–16 BOOTBLKCNT	Defines the stop at block gap value of automatic mode. When received card block cnt is equal to BOOTBLKCNT and AUTOSABGEN is 1, then stop at block gap.
15–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 AUTOSABGEN	When boot, enable auto stop at block gap function. This function will be triggered, and host will stop at block gap when received card block cnt is equal to BOOTBLKCNT.
6 BOOTEN	Boot Mode Enable 0 Fast boot disable. 1 Fast boot enable.
5 BOOTMODE	Boot Mode Select 0 Normal boot. 1 Alternative boot.
4 BOOTACK	Boot Ack Mode Select 0 No ack. 1 Ack.
DTOCVACK	Boot ACK Time Out Counter Value 0000b SDCLK x 2^8 0001b SDCLK x 2^9 0010b SDCLK x 2^10 0011b SDCLK x 2^11 0100b SDCLK x 2^12

Table continues on the next page...

SDHC_MMCBOOT field descriptions (continued)

Field	Description
	0101b SDCLK x 2^13 0110b SDCLK x 2^14 0111b SDCLK x 2^15 ... 1110b SDCLK x 2^22 1111b Reserved

62.5.24 Host Controller Version (SDHC_HOSTVER)

This register contains the vendor host controller version information. All bits are read only and will read the same as the power-reset value.

Address: 400B_1000h base + FCh offset = 400B_10FCh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																VVN								SVN							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1

SDHC_HOSTVER field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–8 VVN	Vendor Version Number These status bits are reserved for the vendor version number. The host driver shall not use this status. 00h Freescale SDHC version 1.0 10h Freescale SDHC version 2.0 11h Freescale SDHC version 2.1 12h Freescale SDHC version 2.2 All others Reserved
SVN	Specification Version Number These status bits indicate the host controller specification version. 01h SD host specification version 2.0, supports test event register and ADMA. All others Reserved

62.6 Functional description

The following sections provide a brief functional description of the major system blocks, including the data buffer, DMA crossbar switch interface, dual-port memory wrapper, data/command controller, clock & reset manager, and clock generator.

62.6.1 Data buffer

The SDHC uses one configurable data buffer, so that data can be transferred between the system bus and the SD card, with an optimized manner to maximize throughput between the two clock domains (that is, the IP peripheral clock, and the master clock). The following diagram illustrates the buffer scheme. The buffer is used as temporary storage for data being transferred between the host system and the card. The watermark levels for read and write are both configurable, and can be any number from 1 to 128 words. The burst lengths for read and write are also configurable, and can be any number from 1 to 31 words.

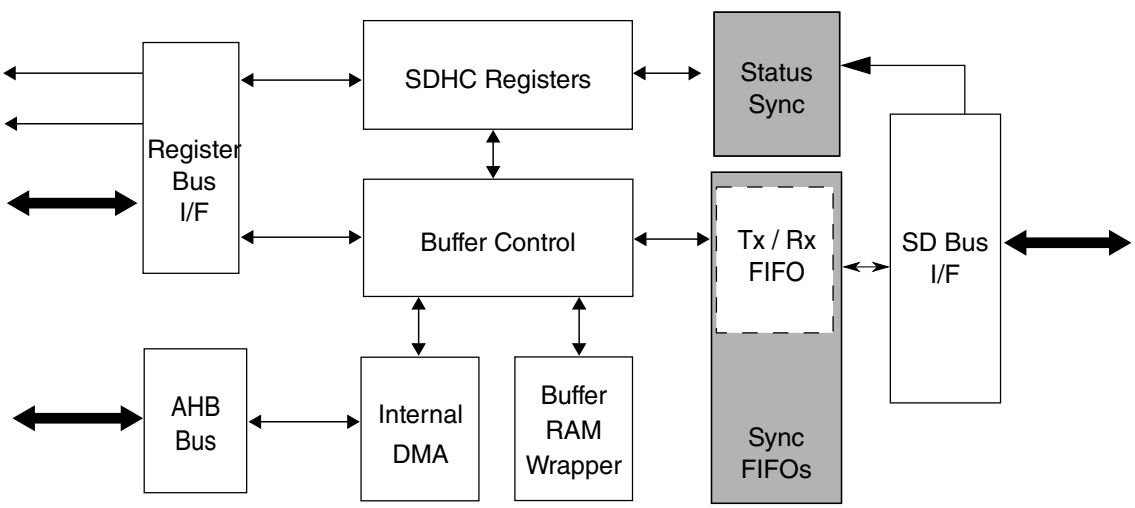


Figure 62-3. SDHC buffer scheme

There are 3 transfer modes to access the data buffer:

- CPU Polling mode:

- For a host read operation, when the number of words received in the buffer meets or exceeds the RDWML watermark value, then by polling IRQSTAT[BRR] the host driver can read the DATPORT register to fetch the amount of words set in the WML register from the buffer. The write operation is similar.

- Internal DMA mode (includes simple and advanced DMA access's):
  - The internal DMA access, either by simple or advanced DMA, is over the crossbar switch bus. For internal DMA access mode, the external DMA request will never be sent out.

For a read operation, when there are more words in the buffer than the amount set in WML, the internal DMA starts fetching data over the crossbar switch bus. Except INCR4 and INCR8, the burst type is always INCR mode and the burst length depends on the shortest of following factors:

1. Burst length configured in the burst length field of WML
2. Watermark level boundary
3. Block size boundary
4. Data boundary configured in the current descriptor if the ADMA is active
5. 1 KB address boundary

Write operation is similar.

Sequential and contiguous access is necessary to ensure the pointer address value is correct. Random or skipped access is not possible. The byte order, by reset, is little endian mode. The actually byte order is swapped inside the buffer, according to the endian mode configured by software, as illustrated in the following diagrams. For a host write operation, byte order is swapped after data is fetched from the buffer and ready to send to the SD bus. For a host read operation, byte order is swapped before the data is stored into the buffer.

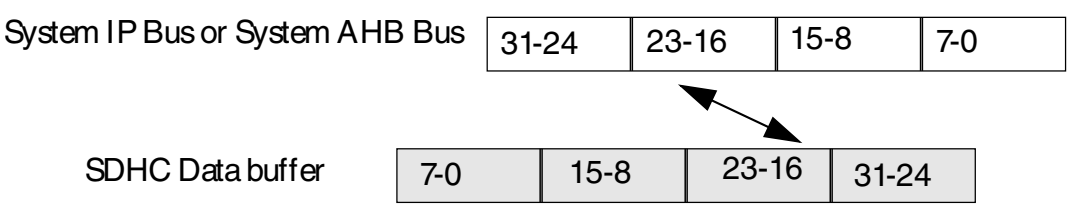


Figure 62-4. Data swap between system bus and SDHC data buffer in byte little endian mode

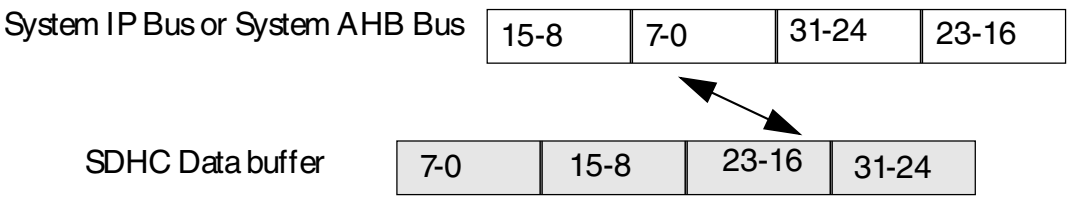


Figure 62-5. Data swap between system bus and SDHC data buffer in half word big endian mode

62.6.1.1 Write operation sequence

There are three ways to write data into the buffer when the user transfers data to the card:

1. Using external DMA through the SDHC DMA request signal.
2. Processor core polling through IRQSTAT[BWR] (interrupt or polling).
3. Using the internal DMA.

When the internal DMA is not used, that is, the XFERTYP[DMAEN] bit is not set when the command is sent, the SDHC asserts a DMA request when the amount of buffer space exceeds the value set in WML, and is ready for receiving new data. At the same time, the SDHC would set IRQSTAT[BWR]. The buffer write ready interrupt will be generated if it is enabled by software.

When internal DMA is used, the SDHC will not inform the system before all the required number of bytes are transferred if no error was encountered. When an error occurs during the data transfer, the SDHC will abort the data transfer and abandon the current block. The host driver must read the contents of the DSADDR to get the starting address of the abandoned data block. If the current data transfer is in multiblock mode, the SDHC will not automatically send CMD12, even though XFERTYP[AC12EN] is set. The host driver shall send CMD12 in this scenario and restart the write operation from that address. It is recommended that a software reset for data be applied before the transfer is restarted after error recovery.

The SDHC will not start data transmission until the number of words set in WML can be held in the buffer. If the buffer is empty and the host system does not write data in time, the SDHC will stop the SD_CLK to avoid the data buffer underrun situation.

62.6.1.2 Read operation sequence

There are three ways to read data from the buffer when the user transfers data to the card:

1. Processor core polling through IRQSTAT[BRR] (interrupt or polling)

2. Using the internal DMA

When internal DMA is not used, that is, XFERTYP[DMAEN] is not set when the command is sent, the SDHC asserts a DMA request when the amount of data exceeds the value set in WML, that is available and ready for system fetching data. At the same time, the SDHC would set IRQSTAT[BRR]. The buffer read ready interrupt will be generated if it is enabled by software.

When internal DMA is used, the SDHC will not inform the system before all the required number of bytes are transferred if no error was encountered. When an error occurs during the data transfer, the SDHC will abort the data transfer and abandon the current block. The host driver must read the content of the DMA system address register to get the starting address of the abandoned data block. If the current data transfer is in multiblock mode, the SDHC will not automatically send CMD12, even though XFERTYP[AC12EN] is set. The host driver shall send CMD12 in this scenario and restart the read operation from that address. It is recommended that a software reset for data be applied before the transfer is restarted after error recovery.

For any write transfer mode, the SDHC will not start data transmission until the number of words set in WML are in the buffer. If the buffer is full and the Host System does not read data in time, the SDHC will stop the SDHC_DCLK to avoid the data buffer overrun situation.

62.6.1.3 Data buffer and block size

The user needs to know the buffer size for the buffer operation during a data transfer to use it in the most optimized way. In the SDHC, the only data buffer can hold up to 128 words (32-bit), and the watermark levels for write and read can be configured respectively. For both read and write, the watermark level can be from 1 word to the maximum of 128 words. For both read and write, the burst length can be from 1 word to the maximum of 31 words. The host driver may configure the value according to the system situation and requirement.

During a multiblock data transfer, the block length may be set to any value between 1 and 4096 bytes inclusive, which satisfies the requirements of the external card. The only restriction is from the external card. It might not support that large of a block or it doesn't support a partial block access, which is not the integer times of 512 bytes.

For block size not times of 4, that is, not word aligned, SDHC requires stuff bytes at the end of each block, because the SDHC treats each block individually. For example, the block size is 7 bytes, there are 12 blocks to write, the system side must write 2 times for

each block, and for each block, the ending byte would be abandoned by the SDHC because it sends only 7 bytes to the card and picks data from the following system write, so there would be 24 beats of write access in total.

62.6.1.4 Dividing large data transfer

This SDIO command CMD53 definition, limits the maximum data size of data transfers according to the following formula:

Max data size = Block size x Block count

The length of a multiple block transfer needs to be in block size units. If the total data length can't be divided evenly into a multiple of the block size, then there are two ways to transfer the data which depend on the function and the card design. Option 1 is for the host driver to split the transaction. The remainder of the block size data is then transferred by using a single block command at the end. Option 2 is to add dummy data in the last block to fill the block size. For option 2, the card must manage the removal of the dummy data.

The following diagram illustrates the dividing of large data transfers. Assuming a kind of WLAN SDIO card supports block size only up to 64 bytes. Although the SDHC supports a block size of up to 4096 bytes, the SDIO can only accept a block size less than 64 bytes, so the data must be divided. See the example below.

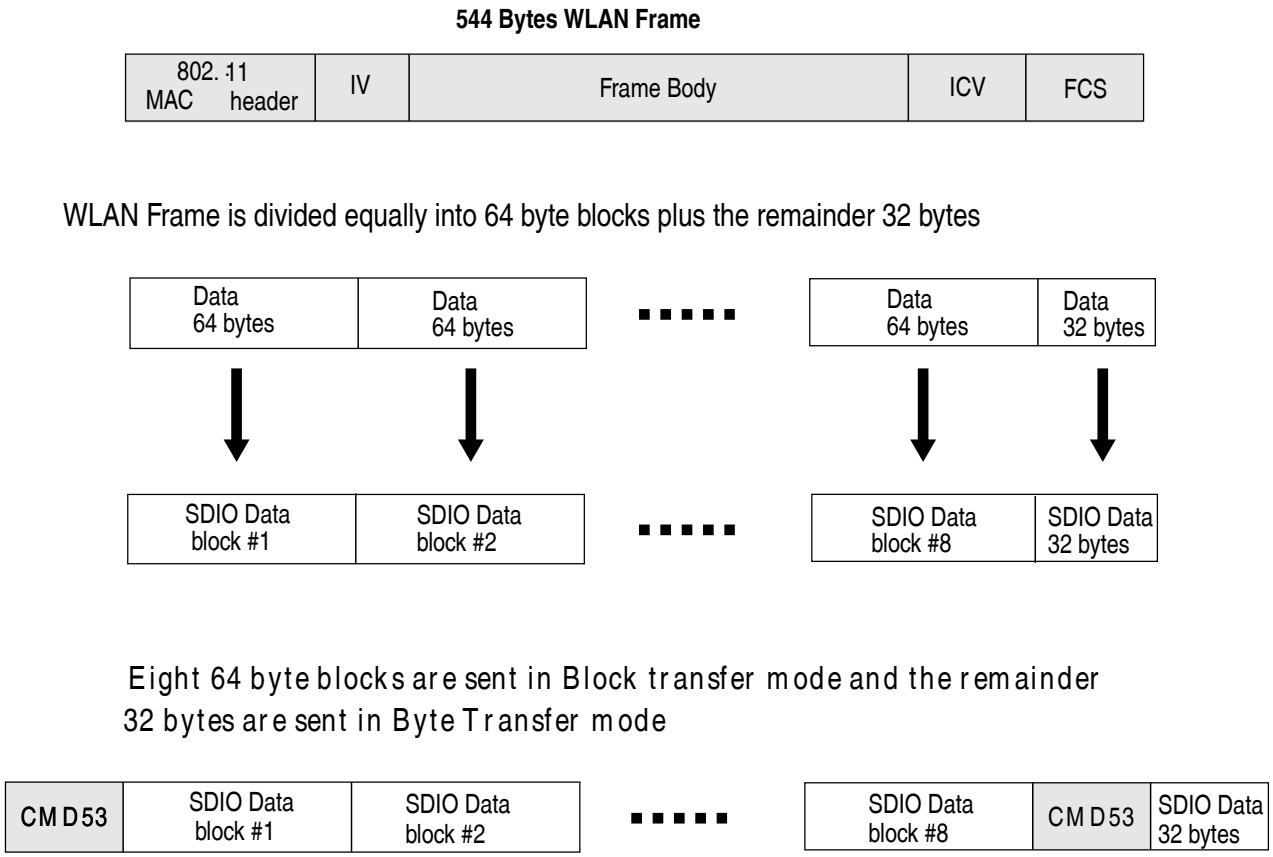


Figure 62-6. Example for dividing large data transfers

62.6.2 DMA crossbar switch interface

The internal DMA implements a DMA engine and the crossbar switch master. When the internal DMA is enabled (XFERTYP[DMAEN] is set), the interrupt status bits are set if they are enabled. To avoid setting them, clear IRQSTATEN[BWRSEN, BRRSEN]. The following diagram illustrates the DMA crossbar switch interface block.

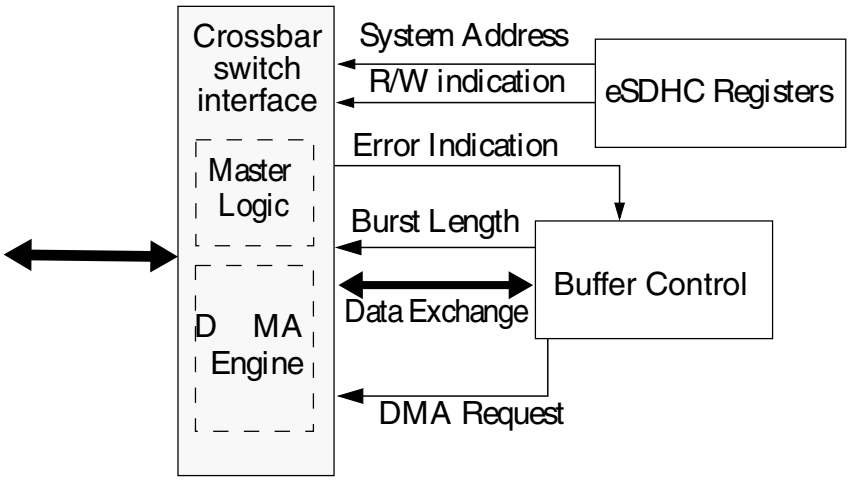


Figure 62-7. DMA crossbar switch interface block

62.6.2.1 Internal DMA request

If the watermark level requirement is met in data transfer, and the internal DMA is enabled, the data buffer block sends a DMA request to the crossbar switch interface. Meanwhile, the external DMA request signal is disabled. The delay in response from the internal DMA engine depends on the system bus loading and the priority assigned to the SDHC. The DMA engine does not respond to the request during its burst transfer, but is ready to serve as soon as the burst is over. The data buffer de-asserts the request once an access to the buffer is made. Upon access to the buffer by internal DMA, the data buffer updates its internal buffer pointer, and when the watermark level is satisfied, another DMA request is sent.

The data transfer is in the block unit, and the subsequent watermark level is always set as the remaining number of words. For instance, for a multiblock data read with each block size of 31 bytes, and the burst length set to 6 words. After the first burst transfer, if there are more than 2 words in the buffer, which might contain some data of the next block, another DMA request read is sent. This is because the remaining number of words to send for the current block is (31 - 6 * 4) / 4 = 2. The SDHC will read 2 words out of the buffer, with 7 valid bytes and 1 stuff byte.

62.6.2.2 DMA burst length

Just like a CPU polling access, the DMA burst length for the internal DMA engine can be from 1 to 16 words. The actual burst length for the DMA depends on the lesser of the configured burst length or the remaining words of the current block. Take the example in Internal DMA request again. The following burst length after 6 words are read will be 2 words, and the next burst length will be 6 words again. This is because the next block

starts, which is 31 bytes, more than 6 words. The host driver writer may take this variable burst length into account. It is also acceptable to configure the burst length as the divisor of the block size, so that each time the burst length will be the same.

62.6.2.3 Crossbar switch master interface

It is possible that the internal DMA engine could fail during the data transfer. When this error occurs, the DMA engine stops the transfer and goes to the idle state as well as the internal data buffer stops accepting incoming data. IRQSTAT[DMAE] is set to inform the driver.

After the DMAE interrupt is received, the software shall send a CMD12 to abort the current transfer and read DSADDR[DSADDR] to get the starting address of the corrupted block. After the DMA error is fixed, the software must apply a data reset and restart the transfer from this address to recover the corrupted block.

62.6.2.4 ADMA engine

In the SDHC standard, the new DMA transfer algorithm called the advanced DMA (ADMA) is defined. For simple DMA, once the page boundary is reached, a DMA interrupt will be generated and the new system address shall be programmed by the host driver. The ADMA defines the programmable descriptor table in the system memory. The host driver can calculate the system address at the page boundary and program the descriptor table before executing ADMA. It reduces the frequency of interrupts to the host system. Therefore, higher speed DMA transfers could be realized because the host MCU intervention would not be needed during long DMA-based data transfers.

There are two types of ADMA: ADMA1 and ADMA2 in host controller. ADMA1 can support data transfer of 4 KB aligned data in system memory. ADMA2 improves the restriction so that data of any location and any size can be transferred in system memory. Their formats of descriptor table are different.

ADMA can recognize all kinds of descriptors defined in the SDHC standard, and if end flag is detected in the descriptor, ADMA will stop after this descriptor is processed.

62.6.2.4.1 ADMA concept and descriptor format

For ADMA1, including the following descriptors:

- Valid/Invalid descriptor
- Nop descriptor

- Set data length descriptor
- Set data address descriptor
- Link descriptor
- Interrupt flag and end flag in descriptor

For ADMA2, including the following descriptors:

- Valid/Invalid descriptor
- Nop descriptor
- Rsv descriptor
- Set data length and address descriptor
- Link descriptor
- Interrupt flag and end flag in descriptor

ADMA2 deals with the lower 32-bit first, and then the higher 32-bit. If the Valid flag of descriptor is 0, it will ignore the high 32-bit. The address field shall be set on word aligned (lower 2-bit is always set to 0). Data length is in byte unit.

ADMA will start read/write operation after it reaches the tran state, using the data length and data address analyzed from most recent descriptor(s).

For ADMA1, the valid data length descriptor is the last set type descriptor before tran type descriptor. Every tran type will trigger a transfer, and the transfer data length is extracted from the most recent set type descriptor. If there is no set type descriptor after the previous trans descriptor, the data length will be the value for previous transfer, or 0 if no set descriptor is ever met.

For ADMA2, tran type descriptor contains both the data length and transfer data address, so only a tran type descriptor can start a data transfer.

Table 62-10. Format of the ADMA1 descriptor table

Address/page field		Address/page field		Attribute field					
31	12	11	6	5	4	3	2	1	0
Address or data length		000000		Act2	Act1	0	Int	End	Valid

Act2	Act1	Symbol	Comment	31-28	27-12
0	0	nop	No operation	Don't care	
0	1	set	Set data length	0000	Data length
1	0	tran	Transfer data	Data address	

Table continues on the next page...

Table 62-10. Format of the ADMA1 descriptor table (continued)

1	1	link	Link descriptor	Descriptor address

Valid	Valid = 1 indicates this line of descriptor is effective. If Valid = 0 generate ADMA error Interrupt and stop ADMA.
End	End = 1 indicates current descriptor is the ending one.
Int	Int = 1 generates DMA interrupt when this descriptor is processed.

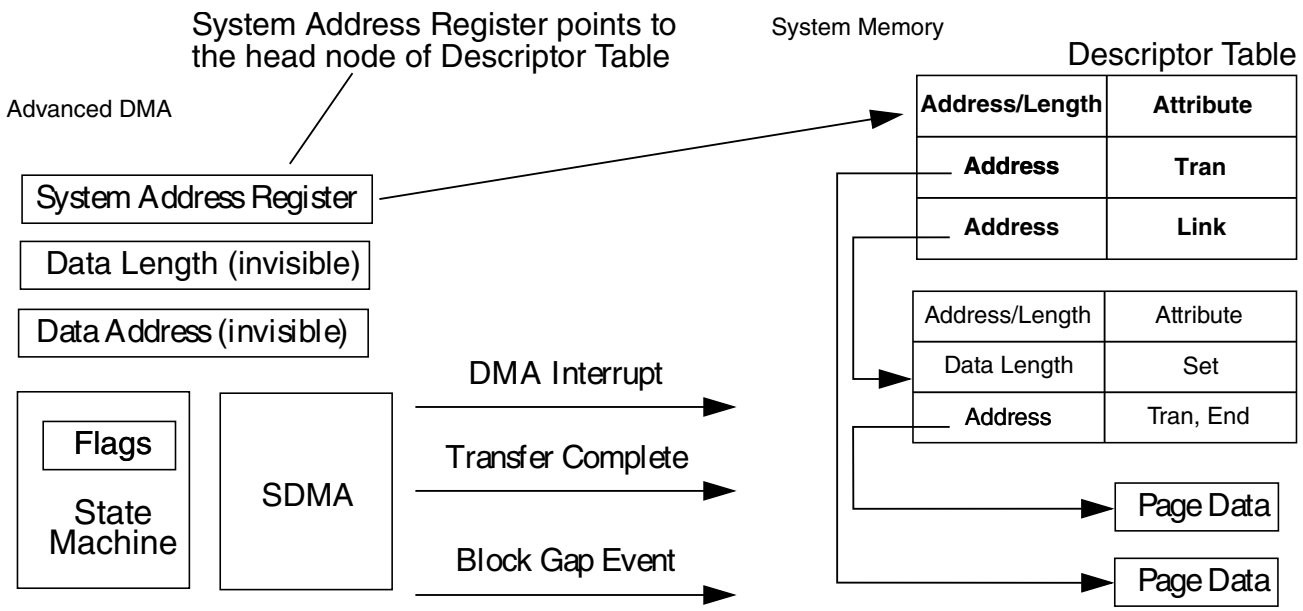


Figure 62-8. Concept and access method of ADMA1 descriptor table

Table 62-11. Format of the ADMA2 descriptor table

Address field		**Length**		**Reserved**			**Attribute field**				
63	32	31	16	15	06	05	04	03	02	01	00
32-bit address		16-bit length		0000000000		Act2	Act1	0	Int	End	Valid

Act2	**Act1**	**Symbol**	**Comment**	**Operation**
0	0	nop	No operation	Don't care
0	1	rsv	Reserved	Same as nop. Read this line and go to next one
1	0	tran	Transfer data	Transfer data with address and length set in this descriptor line
1	1	link	Link descriptor	Link to another descriptor

Valid	Valid = 1 indicates this line of descriptor is effective. If valid = 0 generate ADMA error interrupt and stop ADMA.
End	End = 1 indicates current descriptor is the ending one.
Int	Int = 1 generates DMA interrupt when this descriptor is done.

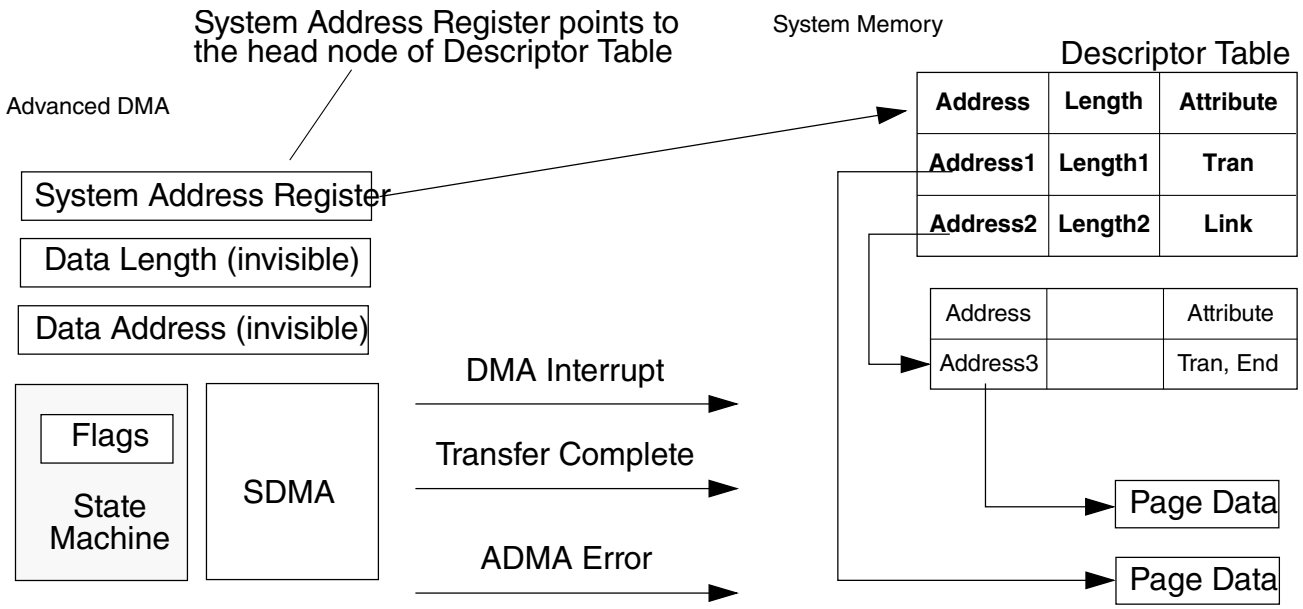


Figure 62-9. Concept and access method of ADMA2 descriptor table

62.6.2.4.2 ADMA interrupt

If the interrupt flag of descriptor is set, ADMA will generate an interrupt according to different type descriptor:

For ADMA1:

- Set type descriptor: interrupt is generated when data length is set.
- Tran type descriptor: interrupt is generated when this transfer is complete.
- Link type descriptor: interrupt is generated when new descriptor address is set.
- Nop type descriptor: interrupt is generated just after this descriptor is fetched.

For ADMA2:

- Tran type descriptor: interrupt is generated when this transfer is complete.
- Link type descriptor: interrupt is generated when new descriptor address is set.
- Nop/Rsv type descriptor: interrupt is generated just after fetch this descriptor.

62.6.2.4.3 ADMA error

The ADMA stops whenever any error is encountered. These errors include:

- Fetching descriptor error

- Transfer error
- Data length mismatch error

ADMA descriptor error will be generated when it fails to detect the valid flag in the descriptor. If ADMA descriptor error occurs, the interrupt is not generated even if the interrupt flag of this descriptor is set.

When XFERTYP[BCEN] is set, data length set in buffer must be equal to the whole data length set in descriptor nodes, otherwise data length mismatch error will be generated.

If XFERTYP[BCEN] is not set, the whole data length set in descriptor must be times of block length, otherwise, when all data set in the descriptor nodes are done not at block boundary, the data mismatch error will occur.

62.6.3 SD protocol unit

The SD protocol unit deals with all SD protocol affairs.

The SD protocol unit performs the following functions:

- Acts as the bridge between the internal buffer and the SD bus
- Sends the command data as well as its argument serially
- Stores the serial response bit stream into the corresponding registers
- Detects the bus state on the DAT[0] line
- Monitors the interrupt from the SDIO card
- Asserts the read wait signal
- Gates off the SD clock when buffer is announcing danger status
- Detects the write protect state

The SD protocol unit consists of four submodules:

- SD transceiver
- SD clock and monitor
- Command agent
- Data agent

62.6.3.1 SD transceiver

In the SD protocol unit, the transceiver is the main control module. It consists of a FSM and control module, from which the control signals for all other three modules are generated.

62.6.3.2 SD clock & monitor

This module monitors the signal level on all 8 data lines, the command lines, and directly routes the level values into the register bank. The driver can use this for debug purposes.

The module also detects the card detection (CD) line as well as the DAT[3] line. The transceiver reports the card insertion state according to the CD state, or the signal level on the DAT[3] line, when PROCTL[D3CD] is set.

The module detects the write protect (WP) line. With the information of the WP state, the register bank will ignore the command, accompanied by a write operation, when the WP switch is on.

If the internal data buffer is in danger, and the SD clock must be gated off to avoid buffer over/under-run, this module will assert the gate of the output SD clock to shut the clock off. After the buffer danger has recovered, and when the system access of the buffer catches up, the clock gate of this module will open and the SD clock will be active again.

This module also drives the SDHC_LCTL output signal when PROCTL[LCTL] is set by the driver.

62.6.3.3 Command agent

The command agent deals with the transactions on the CMD line. The following diagram illustrates the structure for the command CRC Shift Register.

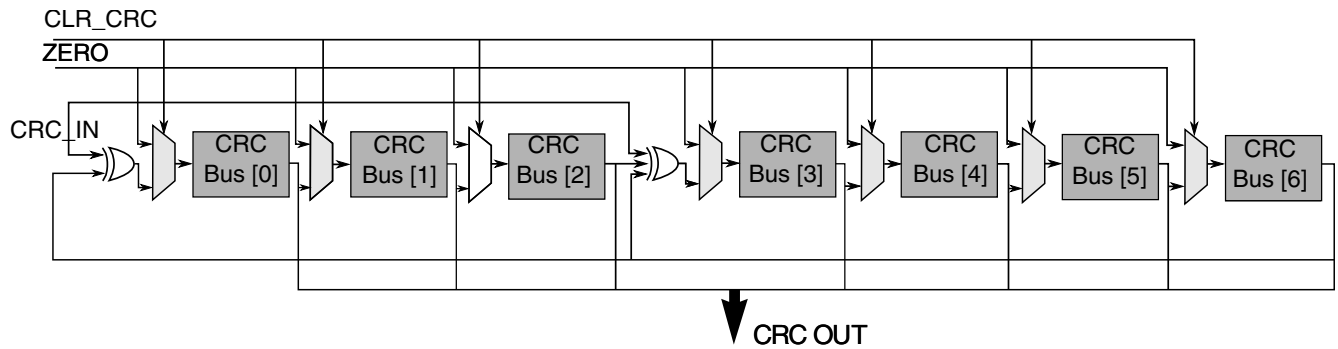


Figure 62-10. Command CRC Shift Register

The CRC polynomials for the CMD line are as follows:

```
Generator polynomial: G(x) = x^7 + x^3 + 1
M(x) = (first bit) * x^n + (second bit) * x^n-1 +...+ (last bit) * x^0
CRC[6:0] = Remainder [(M(x) * x^7) / G(x)]
```

62.6.3.4 Data agent

The data agent deals with the transactions on the eight data lines. Moreover, this module also detects the busy state on the DAT[0] line, and generates the read wait state by the request from the transceiver. The CRC polynomials for the DAT are as follows:

```
Generator polynomial: G(x) = x^16 + x^12 + x^5
 +1
M(x) = (first bit) * x^n + (second bit) * x^n-1 +...+ (last bit) * x^0
CRC[15:0] = Remainder [(M(x) * x^16) / G(x)]
```

62.6.4 Clock and reset manager

This module controls all the reset signals within the SDHC.

There are four kinds of reset signals within the SDHC:

- Hardware reset
- Software reset for all
- Software reset for the data part
- Software reset for the command part

All these signals are fed into this module and stable signals are generated inside the module to reset all other modules. The module also gates off all the inside signals.

There are three clocks inside the SDHC:

- Bus clock
- SDHC clock
- System clock

The module monitors the activities of all other modules, supplies the clocks for them, and when enabled, automatically gates off the corresponding clocks.

62.6.5 Clock generator

The clock generator generates the SDHC_CLK by peripheral source clock in two stages. The following diagram illustrates the structure of the divider. The term "base" represents the frequency of peripheral source clock.

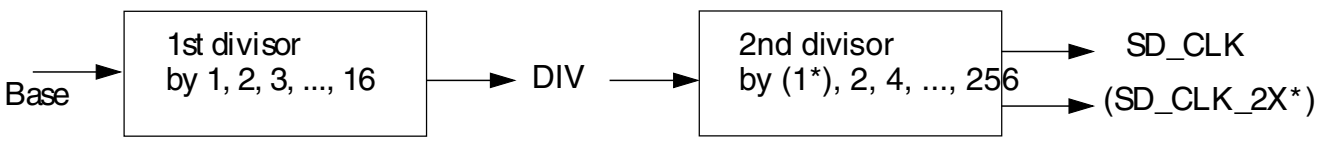


Figure 62-11. Two stages of the clock divider

The first stage outputs an intermediate clock (DIV), which can be base, base/2, base/3, ..., or base/16.

The second stage is a prescaler, and outputs the actual clock (SDHC_CLK). This clock is the driving clock for all submodules of the SD protocol unit, and the sync FIFOs to synchronize with the data rate from the internal data buffer. The frequency of the clock output from this stage, can be DIV, DIV/2, DIV/4,..., or DIV/256. Thus, the highest frequency of the SDHC_CLK is base, and the next highest is base/2, while the lowest frequency is base/4096. If the base clock is of equal duty ratio (usually true), the duty cycle of SDHC_CLK is also 50%, even when the compound divisor is an odd value.

62.6.6 SDIO card interrupt

This section discusses SDIO interrupt handling.

62.6.6.1 Interrupts in 1-bit mode

In this case, the DAT[1] pin is dedicated to providing the interrupt function. An interrupt is asserted by pulling the DAT[1] low from the SDIO card, until the interrupt service is finished to clear the interrupt.

62.6.6.2 Interrupt in 4-bit mode

Because the interrupt and data line 1 share Pin 8 in 4-bit mode, an interrupt will be sent by the card and recognized by the host only during a specific time. This is known as the interrupt period. The SDHC will only sample the level on pin 8 during the interrupt period. At all other times, the host will ignore the level on pin 8, and treat it as the data signal. The definition of the interrupt period is different for operations with single block and multiple block data transfers.

In the case of normal single data block transmissions, the interrupt period becomes active two clock cycles after the completion of a data packet. This interrupt period lasts until after the card receives the end bit of the next command that has a data block transfer associated with it.

For multiple block data transfers in 4-bit mode, there is only a limited period of time that the interrupt period can be active due to the limited period of data line availability between the multiple blocks of data. This requires a more strict definition of the interrupt period. In this case, the interrupt period is limited to two clock cycles. This begins two clocks after the end bit of the previous data block. During this 2-clock cycle interrupt period, if an interrupt is pending, the SDHC_D1 line will be held low for one clock cycle with the last clock cycle pulling SDHC_D1 high. On completion of the Interrupt Period, the card releases the SDHC_D1 line into the high Z state. The SDHC samples the SDHC_D1] during the interrupt period when PROCTL[IABG] is set.

See the SDIO Card Specification v1.10f for further information about the SDIO card interrupt.

62.6.6.3 Card interrupt handling

When IRQSIGEN[CINTIEN] is set to 0, the SDHC clears the interrupt request to the host system. The host driver must clear this bit before servicing the SDIO Interrupt and must set this bit again after all interrupt requests from the card are cleared to prevent inadvertent interrupts.

The SDIO status bit is cleared by resetting the SDIO interrupt. Writing to this bit would have no effects. In 1-bit mode, the SDHC will detect the SDIO interrupt with or without the SD clock (to support wakeup). In 4-bit mode, the interrupt signal is sampled during the interrupt period, so there are some sample delays between the interrupt signal from the SDIO card and the interrupt to the host system interrupt controller. When the SDIO status has been set, and the host driver needs to service this interrupt, so the SDIO bit in the interrupt control register of the SDIO card will be cleared. This is required to clear the

SDIO interrupt status latched in the SDHC and to stop driving the interrupt signal to the system interrupt controller. The host driver must issue a CMD52 to clear the card interrupt. After completion of the card interrupt service, the SDIO Interrupt Enable bit is set to 1, and the SDHC starts sampling the interrupt signal again.

The following diagram illustrates the SDIO card interrupt scheme and for the sequences of software and hardware events that take place during a card interrupt handling procedure.

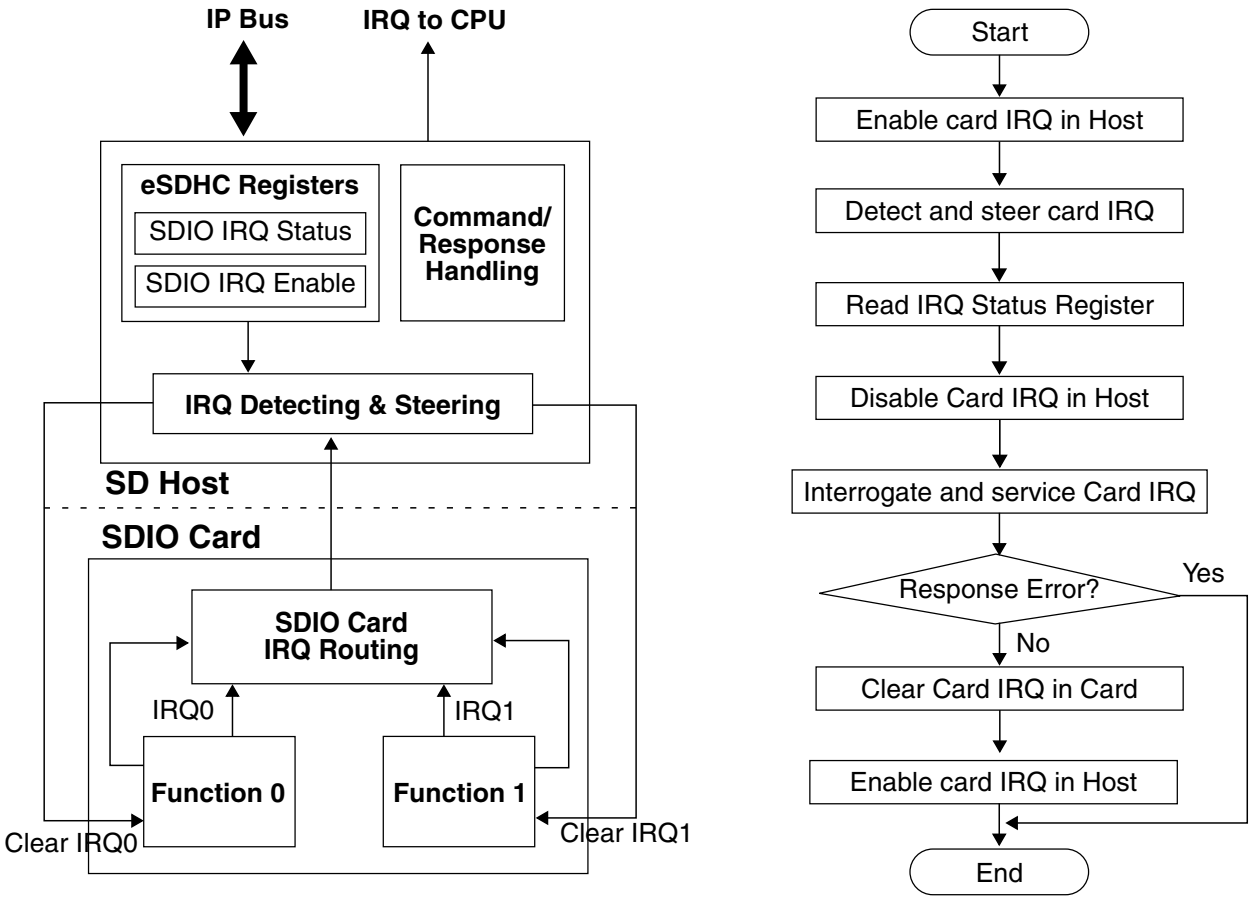


Figure 62-12. Card interrupt scheme and card interrupt detection and handling procedure

62.6.7 Card insertion and removal detection

The SDHC uses either the DAT[3] pin or the CD pin to detect card insertion or removal. When there is no card on the MMC/SD bus, the DAT[3] will be pulled to a low voltage level by default. When any card is inserted to or removed from the socket, the SDHC detects the logic value changes on the DAT[3] pin and generates an interrupt. When the DAT[3] pin is not used for card detection (for example, it is implemented in GPIO), the CD pin must be connected for card detection. Whether DAT[3] is configured for card

detection or not, the CD pin is always a reference for card detection. Whether the DAT[3] pin or the CD pin is used to detect card insertion, the SDHC will send an interrupt (if enabled) to inform the Host system that a card is inserted.

62.6.8 Power management and wakeup events

When there is no operation between the SDHC and the card through the SD bus, the user can completely disable the bus clock and the SDHC clock in the chip-level clock control module to save power. When the user needs to use the SDHC to communicate with the card, it can enable the clock and start the operation.

In some circumstances, when the clocks to the SDHC are disabled, for instance, when the system is in low-power mode, there are some events for which the user needs to enable the clock and handle the event. These events are called wakeup interrupts. The SDHC can generate these interrupt even when there are no clocks enabled.

The three interrupts which can be used as wakeup events are:

- Card removal interrupt
- Card insertion interrupt
- Interrupt from SDIO card

The SDHC offers a power management feature. By clearing the clock enabled bits in the system control register, the clocks are gated in the low position to the SDHC. For maximum power saving, the user can disable all the clocks to the SDHC when there is no operation in progress.

These three wakeup events, or wakeup interrupts, can also be used to wake up the system from low-power modes.

Note

To make the interrupt a wakeup event, when all the clocks to the SDHC are disabled or when the whole system is in low-power mode, the corresponding wakeup enabled bit needs to be set. See Protocol Control register for more information.

62.6.8.1 Setting wakeup events

For the SDHC to respond to a wakeup event, the software must set the respective wakeup enable bit before the CPU enters Sleep mode. Before the software disables the host clock, it must ensure that all of the following conditions have been met:

- No read or write transfer is active
- Data and command lines are not active
- No interrupts are pending
- Internal data buffer is empty

62.6.9 MMC fast boot

In Embedded MultiMediaCard(eMMC4.3) spec, add fast boot feature needs hardware support.

In Boot Operation mode, the master (multimediacard host) can read boot data from the slave (MMC device) by keeping CMD line low after power-on, or sending CMD0 with argument + 0xFFFFFFFA (optional for slave), before issuing CMD1.

There are two types of Fast Boot mode, boot operation, and Alternative boot operation in eMMC4.3 spec. Each type also has with acknowledge and without acknowledge modes.

Note

For the eMMC4.3 card setting, please see the eMMC4.3 specification.

62.6.9.1 Boot operation

Note

In this block guide, this fast boot is called Normal Fast Boot mode.

If the CMD line is held low for 74 clock cycles and more after power-up before the first command is issued, the slave recognizes that Boot mode is being initiated and starts preparing boot data internally.

Within 1 second after the CMD line goes low, the slave starts to send the first boot data to the master on the DAT line(s). The master must keep the CMD line low to read all of the boot data.

If boot acknowledge is enabled, the slave has to send acknowledge pattern 010 to the master within 50 ms after the CMD line goes low. If boot acknowledge is disabled, the slave will not send out acknowledge pattern '010'.

The master can terminate Boot mode with the CMD line high.

Boot operation will be terminated when all contents of the enabled boot data are sent to the master. After boot operation is executed, the slave shall be ready for CMD1 operation and the master needs to start a normal MMC initialization sequence by sending CMD1.

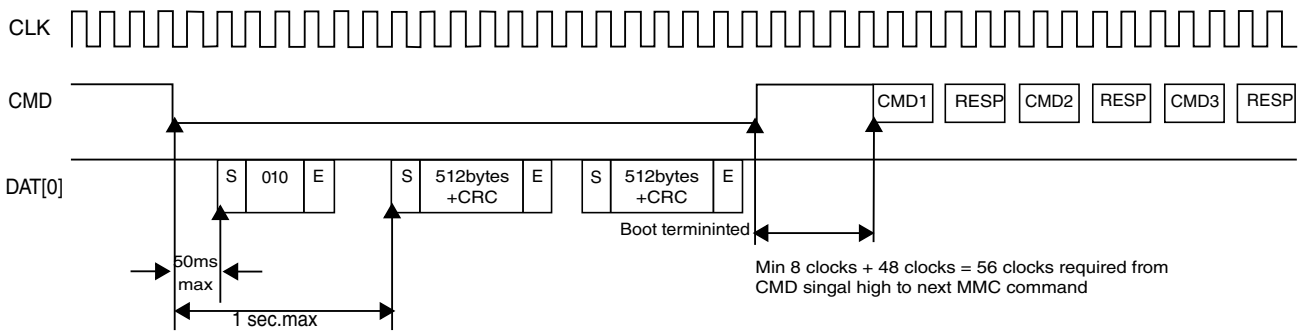


Figure 62-13. Multimediacard state diagram in Normal Boot mode

62.6.9.2 Alternative boot operation

This boot function is optional for the device. If bit 0 in the extended CSD byte[228] is set to 1, the device supports the alternative boot operation.

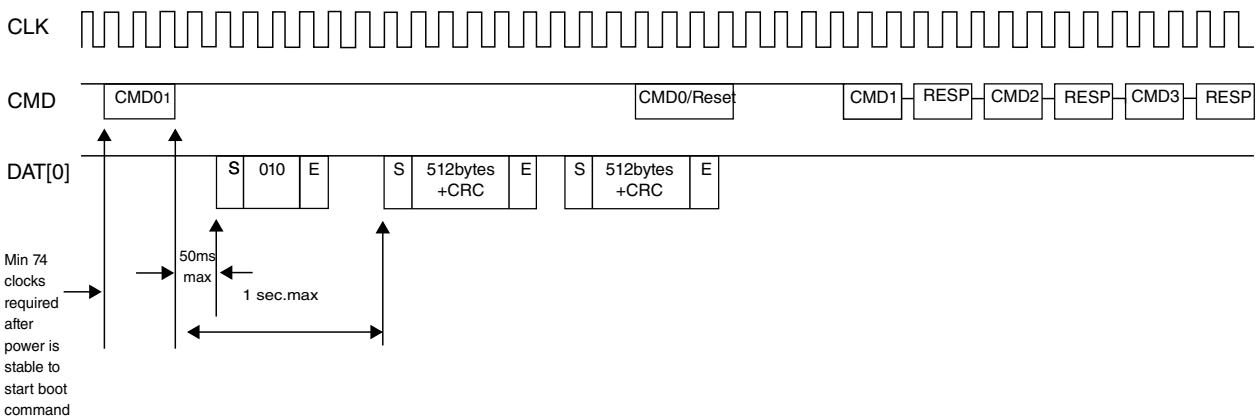
After power-up, if the host issues CMD0 with the argument of 0xFFFFFFFA after 74 clock cycles, before CMD1 is issued, or the CMD line goes low, the slave recognizes that boot mode is being initiated and starts preparing boot data internally.

Within 1 second after CMD0 with the argument of 0xFFFFFFFA is issued, the slave starts to send the first boot data to the master on the DAT line(s).

If boot acknowledge is enabled, the slave has to send the acknowledge pattern '010' to the master within 50ms after the CMD0 with the argument of 0xFFFFFFFA is received. If boot acknowledge is disabled, theslave will not send out acknowledge pattern '010'.

The master can terminate boot mode by issuing CMD0 (Reset).

Boot operation will be terminated when all contents of the enabled boot data are sent to the master. After boot operation is executed, the slave shall be ready for CMD1 operation and the master needs to start a normal MMC initialization sequence by sending CMD1.



NOTE 1. CMD0 with argument 0xFFFFFFFA

Figure 62-14. MultiMediaCard state diagram in Alternative Boot mode

62.7 Initialization/application of SDHC

All communication between system and cards are controlled by the host. The host sends commands of two types:

- Broadcast
- Addressed point-to-point

Broadcast commands are intended for all cards, such as GO_IDLE_STATE, SEND_OP_COND, ALL_SEND_CID, and so on. In Broadcast mode, all cards are in the Open-Drain mode to avoid bus contention. See Commands for MMC/SD/SDIO for the commands of bc and bcr categories.

After the broadcast command CMD3 is issued, the cards enter Standby mode. Addressed type commands are used from this point. In this mode, the CMD/DAT I/O pads will turn to Push-Pull mode, to have the driving capability for maximum frequency operation. See Commands for MMC/SD/SDIO for the commands of ac and adtc categories.

62.7.1 Command send and response receive basic operation

Assuming the data type WORD is an unsigned 32-bit integer, the following flow is a guideline for sending a command to the card(s):

```
send_command(cmd_index, cmd_arg, other requirements)
{
WORD wCmd; // 32-bit integer to make up the data to write into Transfer Type register, it is
recommended to implement in a bit-field manner
wCmd = (<cmd_index> & 0x3f) >> 24; // set the first 8 bits as '00'+<cmd_index>
set CMDTYP, DPSEL, CICEN, CCCEN, RSTTYP, DTDSEL accorind to the command index;
if (internal DMA is used) wCmd |= 0x1;
```

```
if (multi-block transfer) {
 set MSBSEL bit;
 if (finite block number) {
  set BCEN bit;
  if (auto12 command is to use) set AC12EN bit;
 }
}
write_reg(CMDARG, <cmd_arg>); // configure the command argument
write_reg(XFERTYP, wCmd); // set Transfer Type register as wCmd value to issue the command
}
wait_for_response(cmd_index)
{
while (CC bit in IRQ Status register is not set); // wait until Command Complete bit is set
read IRQ Status register and check if any error bits about Command are set
if (any error bits are set) report error;
write 1 to clear CC bit and all Command Error bits;
}
```

For the sake of simplicity, the function wait_for_response is implemented here by means of polling. For an effective and formal way, the response is usually checked after the command complete interrupt is received. By doing this, make sure the corresponding interrupt status bits are enabled.

In some scenarios, the response time-out is expected. For instance, after all cards respond to CMD3 and go to the standby state, no response to the host when CMD2 is sent. The host driver shall deal with 'fake' errors like this with caution.

62.7.2 Card Identification mode

When a card is inserted to the socket or the card was reset by the host, the host needs to validate the operation voltage range, identify the cards, request the cards to publish the relative card address (RCA) or to set the RCA for the MMC cards.

62.7.2.1 Card detect

The following diagram illustrates the detection of MMC, SD, and SDIO cards using the SDHC.

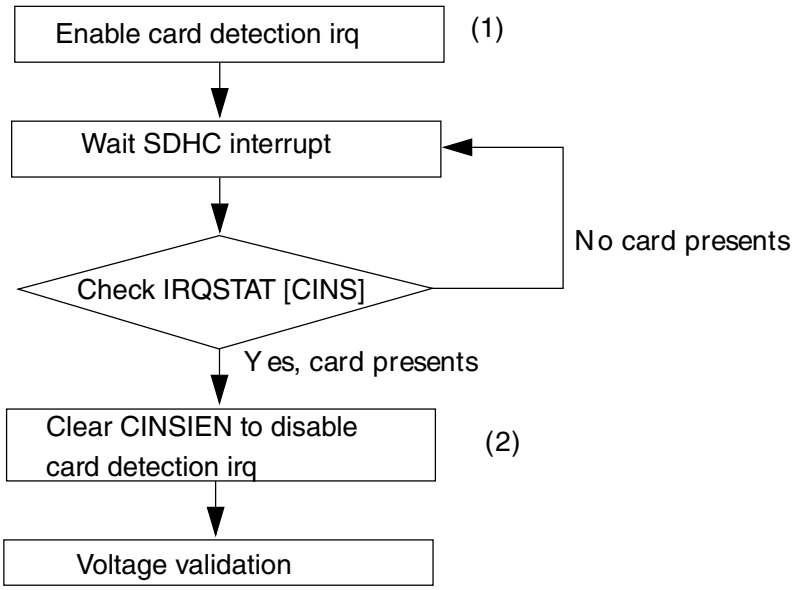


Figure 62-15. Flow diagram for card detection

Here is the card detection sequence:

- Set the CINSIEN bit to enable card detection interrupt
- When an interrupt from the SDHC is received, check IRQSTAT[CINS] in the Interrupt Status register to see whether it was caused by card insertion
- Clear the CINSIEN bit to disable the card detection interrupt and ignore all card insertion interrupts afterwards

62.7.2.2 Reset

The host consists of three types of resets:

- Hardware reset (card and host) which is driven by power on reset (POR)
- Software reset (host only) is initiated by the write operation of the SYSCTL[RSTD], SYSCTL[RSTC], or SYSCTL[RSTA] bits to reset the data part, command part, or all parts of the host controller, respectively
- Card reset (card only). The command, Go_Idle_State (CMD0), is the software reset command for all types of MMC cards, SD Memory cards. This command sets each card into the idle state regardless of the current card state. For an SD I/O Card, CMD52 is used to write an I/O reset in the CCCR. The cards are initialized with a default relative card address (RCA = 0x0000) and with a default driver stage register setting (lowest speed, highest driving current capability).

After the card is reset, the host needs to validate the voltage range of the card. The following diagram illustrates the software flow to reset both the SDHC and the card.

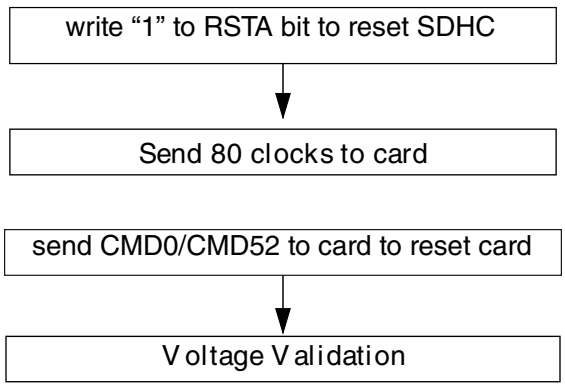


Figure 62-16. Flow chart for reset of the SDHC and SD I/O card

```
software_reset()
{
set_bit(SYSCTRL, RSTA); // software reset the Host
set DTOCV and SDCLKFS bit fields to get the SD_CLK of frequency around 400kHz
configure IO pad to set the power voltage of external card to around 3.0V
poll bits CIHB and CDIHB bits of PRSSTAT to wait both bits are cleared
set_bit(SYSCTRL, INTIA); // send 80 clock ticks for card to power up
send_command(CMD_GO_IDLE_STATE, <other parameters>); // reset the card with CMD0
or send_command(CMD_IO_RW_DIRECT, <other parameters>);
}
```

62.7.2.3 Voltage validation

All cards should be able to establish communication with the host using any operation voltage in the maximum allowed voltage range specified in the card specification. However, the supported minimum and maximum values for V_{DD} are defined in the Operation Conditions Register (OCR) and may not cover the whole range. Cards that store the CID and CSD data in the preload memory are able to communicate this information only under data transfer V_{DD} conditions. This means if the host and card have noncommon V_{DD} ranges, the card will not be able to complete the identification cycle, nor will it be able to send CSD data.

Therefore, a special command Send_Op_Cont (CMD1 for MMC), SD_Send_Op_Cont (ACMD41 for SD Memory) and IO_Send_Op_Cont (CMD5 for SD I/O) is used. The voltage validation procedure is designed to provide a mechanism to identify and reject cards which do not match the V_{DD} range(s) desired by the host. This is accomplished by the host sending the desired V_{DD} voltage window as the operand of this command. Cards that can't perform the data transfer in the specified range must discard themselves from further bus operations and go into the Inactive state. By omitting the voltage range in the command, the host can query each card and determine the common voltage range before

sending out-of-range cards into the inactive state. This query should be used if the host is able to select a common voltage range or if a notification shall be sent to the system when a nonusable card in the stack is detected.

The following steps show how to perform voltage validation when a card is inserted:

```
voltage_validation(voltage_range_arguement)
{
label the card as UNKNOWN;
send_command(IO_SEND_OP_COND, 0x0, <other parameters are omitted>); // CMD5, check SDIO
operation voltage, command argument is zero
if (RESP_TIMEOUT != wait_for_response(IO_SEND_OP_COND)) { // SDIO command is accepted
 if (0 < number of IO functions) {
  label the card as SDIO;
  IORDY = 0;
  while (!(IORDY in IO OCR response)) { // set voltage range for each IO function
   send_command(IO_SEND_OP_COND, <voltage range>, <other parameter>);
   wait_for_response(IO_SEND_OP_COND);
  } // end of while ...
 } // end of if (0 < ...
 if (memory part is present inside SDIO card) Label the card as SDCombo; // this is an
SD-Combo card
} // end of if (RESP_TIMEOUT ...
if (the card is labelled as SDIO card) return; // card type is identified and voltage range
is
set, so exit the function;
send_command(APP_CMD, 0x0, <other parameters are omitted>); // CMD55, Application specific
CMD
prefix
if (no error calling wait_for_response(APP_CMD, <...>) { // CMD55 is accepted
 send_command(SD_APP_OP_COND, <voltage range>, <...>); // ACMD41, to set voltage range
for memory part or SD card
 wait_for_response(SD_APP_OP_COND); // voltage range is set
 if (card type is UNKNOWN) label the card as SD;
 return; //
} // end of if (no error ...
else if (errors other than time-out occur) { // command/response pair is corrupted
 deal with it by program specific manner;
} // of else if (response time-out
else { // CMD55 is refuse, it must be MMC card or CE-ATA card
 if (card is already labelled as SDCombo) { // change label
  re-label the card as SDIO;
  ignore the error or report it;
  return; // card is identified as SDIO card
 } // of if (card is ...
 send_command(SEND_OP_COND, <voltage range>, <...>);
 if (RESP_TIMEOUT == wait_for_response(SEND_OP_COND)) { // CMD1 is not accepted, either
  label the card as UNKNOWN;
  return;
 } // of if (RESP_TIMEOUT ...
 if (check for CE-ATA signature succeeded) { // the card is CE-ATA
  store CE-ATA specific info from the signature;
  label the card as CE-ATA;
 } // of if (check for CE-ATA ...
 else label the card as MMC;
} // of else
}
```

62.7.2.4 Card registry

Card registry for the MMC and SD/SDIO/SD combo cards are different.

For the SD card, the identification process starts at a clock rate lower than 400 kHz and the power voltage higher than 2.7 V, as defined by the card specification. At this time, the CMD line output drives are push-pull drivers instead of open-drain. After the bus is activated, the host will request the card to send their valid operation conditions. The response to ACMD41 is the operation condition register of the card. The same command shall be send to all of the new cards in the system. Incompatible cards are put into the inactive state. The host then issues the command, All_Send_CID (CMD2), to each card to get its unique card identification (CID) number. Cards that are currently unidentified, in the ready state, send their CID number as the response. After the CID is sent by the card, the card goes into the Identification state.

The host then issues Send_Relative_Addr (CMD3), requesting the card to publish a new relative card address (RCA) that is shorter than the CID. This RCA will be used to address the card for future data transfer operations. After the RCA is received, the card changes its state to the Standby state. At this point, if the host wants the card to have an alternative RCA number, it may ask the card to publish a new number by sending another Send_Relative_Addr command to the card. The last published RCA is the actual RCA of the card.

The host repeats the identification process with CMD2 and CMD3 for each card in the system until the last CMD2 gets no response from any of the cards in system.

For MMC operation, the host starts the card identification process in Open-Drain mode with the identification clock rate lower than 400 kHz and the power voltage higher than 2.7 V. The open drain driver stages on the CMD line allow parallel card operation during card identification. After the bus is activated, the host will request the cards to send their valid operation conditions (CMD1). The response to CMD1 is the wired OR operation on the condition restrictions of all cards in the system. Incompatible cards are sent into the Inactive state.

The host then issues the broadcast command All_Send_CID (CMD2), asking all cards for their unique card identification (CID) number. All unidentified cards, the cards in ready state, simultaneously start sending their CID numbers serially, while bit-wise monitoring their outgoing bit stream. Those cards, whose outgoing CID bits do not match the corresponding bits on the command line in any one of the bit periods, stop sending their CID immediately and must wait for the next identification cycle. Because the CID is unique for each card, only one card can successfully send its full CID to the host. This card then goes into the Identification state.

Thereafter, the host issues Set_Relative_Addr (CMD3) to assign to the card a relative card address (RCA). When the RCA is received the card state changes to the standby state, and the card does not react in further identification cycles, and its output driver

switches from open-drain to push-pull. The host repeats the process, mainly CMD2 and CMD3, until the host receives a time-out condition to recognize the completion of the identification process.

For operation as MMC cards:

```
card_registry()
{
do { // decide RCA for each card until response time-out
 if(card is labelled as SDCombo or SDIO) { // for SDIO card like device
  send_command(SET_RELATIVE_ADDR, 0x00, <...>); // ask SDIO card to publish its
RCA
  retrieve RCA from response;
 } // end if (card is labelled as SDCombo ...
 else if (card is labelled as SD) { // for SD card
  send_command(ALL_SEND_CID, <...>);
  if (RESP_TIMEOUT == wait_for_response(ALL_SEND_CID)) break;
  send_command(SET_RELATIVE_ADDR, <...>);
  retrieve RCA from response;
 } // else if (card is labelled as SD ...
 else if (card is labelled as MMC or CE-ATA) { // treat CE-ATA as MMC
  send_command(ALL_SEND_CID, <...>);
  rca = 0x1; // arbitrarily set RCA, 1 here for example, this RCA is also the
relative address to access the CE-ATA card
  send_command(SET_RELATIVE_ADDR, 0x1 << 16, <...>); // send RCA at upper 16
bits
 } // end of else if (card is labelled as MMC ...
} while (response is not time-out);
}
```

62.7.3 Card access

This section discusses the various card access methods.

62.7.3.1 Block write

This section discusses the block write access methods.

62.7.3.1.1 Normal write

During a block write (CMD24 - 27, CMD60, CMD61), one or more blocks of data are transferred from the host to the card with a CRC appended to the end of each block by the host. If the CRC fails, the card shall indicate the failure on the dat line. The transferred data will be discarded and not written, and all further transmitted blocks in Multiple Block Write mode will be ignored.

If the host uses partial blocks whose accumulated length is not block aligned and block misalignment is not allowed (CSD parameter WRITE_BLK_MISALIGN is not set), the card detects the block misalignment error and aborts the programming before the beginning of the first misaligned block. The card sets the ADDRESS_ERROR error bit in

the status register, and while ignoring all further data transfer, waits in the Receive-Data-state for a stop command. The write operation is also aborted if the host tries to write over a write protected area.

For MMC and SD cards, programming of the CID and CSD registers does not require a previous block length setting. The transferred data is also CRC protected. If a part of the CSD or CID register is stored in ROM, then this unchangeable part must match the corresponding part of the receive buffer. If this match fails, then the card will report an error and not change any register contents.

For all types of cards, some may require long and unpredictable periods of time to write a block of data. After receiving a block of data and completing the CRC check, the card will begin writing and hold the DAT line low if its write buffer is full and unable to accept new data from a new WRITE_BLOCK command. The host may poll the status of the card with a SEND_STATUS command (CMD13) or other means for SDIO cards at any time, and the card will respond with its status. The responded status indicates whether the card can accept new data or whether the write process is still in progress. The host may deselect the card by issuing a CMD7 to select a different card to place the card into the Standby state and release the DAT line without interrupting the write operation. When reselecting the card, it will reactivate the busy indication by pulling DAT to low if the programming is still in progress and the write buffer is unavailable.

The software flow to write to a card incorporates the internal DMA and the write operation is a multi-block write with the Auto CMD12 enabled. For the other two methods, by means of external DMA or CPU polling status, with different transfer methods, the internal DMA parts should be removed and the alternative steps should be straightforward.

The software flow to write to a card is:

1. Check the card status, wait until the card is ready for data.
2. Set the card block length/size:
    a. For SD/MMC cards, use SET_BLOCKLEN (CMD16)
    b. For SDIO cards or the I/O portion of SDCombo cards, use IO_RW_DIRECT (CMD52) to set the I/O Block Size bit field in the CCCR register (for function 0) or FBR register (for functions 1~7)
3. Set the eSDHC block length register to be the same as the block length set for the card in Step 2.
4. Set the eSDHC number block register (NOB), nob is 5 (for instance).

5. Disable the buffer write ready interrupt, configure the DMA settings, and enable the eSDHC DMA when sending the command with data transfer. AC12EN should also be set.
6. Wait for the Transfer Complete interrupt.
7. Check the status bit to see whether a write CRC error occurred, or some another error, that occurred during the auto12 command sending and response receiving.

62.7.3.1.2 Write with pause

The write operation can be paused during the transfer. Instead of stopping the SD_CLK at any time to pause all the operations, which is also inaccessible to the host driver, the driver can set PROCTL[SABGREQ] to pause the transfer between the data blocks. As there is no time-out condition in a write operation during the data blocks, a write to all types of cards can be paused in this way, and if the DAT0 line is not required to deassert to release the busy state, no suspend command is needed.

Like the flow described in Normal write, the write with pause is shown with the same kind of write operation:

1. Check the card status, wait until card is ready for data.
2. Set the card block length/size:
   a. For SD/MMC, use SET_BLOCKLEN (CMD16)
   b. For SDIO cards or the I/O portion of SDCombo cards, use IO_RW_DIRECT(CMD52) to set the I/O Block Size bit field in the CCCR register (for function 0) or FBR register (for functions 1~7)
3. Set the SDHC block length register to be the same as the block length set for the card in Step 2.
4. Set the SDHC number block register (NOB), nob is 5 (for instance).
5. Disable the buffer write ready interrupt, configure the DMA settings, and enable the SDHC DMA when sending the command with data transfer. The XFERTYP[AC12EN] bit should also be set.
6. Set PROCTL[SABGREQ].
7. Wait for the transfer complete interrupt.
8. Clear PROCTL[SABGREQ].
9. Check the status bit to see whether a write CRC error occurred.

10. Set PROCTL[CREQ] to continue the write operation.
11. Wait for the transfer complete interrupt.
12. Check the status bit to see whether a write CRC error occurred, or some another error, that occurred during the auto12 command sending and response receiving.

The number of blocks left during the data transfer is accessible by reading the contents of the BLKATTR[BLKCNT] . As the data transfer and the setting of the PROCTL[SABGREQ] bit are concurrent, and the delay of register read and the register setting, the actual number of blocks left may not be exactly the value read earlier. The driver shall read the value of BLKATTR[BLKCNT] after the transfer is paused and the transfer complete interrupt is received.

It is also possible that the last block has begun when the stop at block gap request is sent to the buffer. In this case, the next block gap is actually the end of the transfer. These types of requests are ignored and the Driver should treat this as a non-pause transfer and deal with it as a common write operation.

When the write operation is paused, the data transfer inside the host system is not stopped, and the transfer is active until the data buffer is full. Because of this (if not needed), it is recommended to avoid using the suspend command for the SDIO card. This is because when such a command is sent, the SDHC thinks the system will switch to another function on the SDIO card, and flush the data buffer. The SDHC takes the resume command as a normal command with data transfer, and it is left for the driver to set all the relevant registers before the transfer is resumed. If there is only one block to send when the transfer is resumed, XFERTYP[MSBSEL] and XFERTYP[BCEN] are set as well as XFERTYP[AC12EN]. However, the SDHC will automatically send a CMD12 to mark the end of the multiblock transfer.

62.7.3.2 Block read

This section discusses the block read access methods.

62.7.3.2.1 Normal read

For block reads, the basic unit of data transfer is a block whose maximum size is stored in areas defined by the corresponding card specification. A CRC is appended to the end of each block, ensuring data transfer integrity. The CMD17, CMD18, CMD53, CMD60, CMD61, and so on, can initiate a block read. After completing the transfer, the card returns to the Transfer state. For multi blocks read, data blocks will be continuously transferred until a stop command is issued.

The software flow to read from a card incorporates the internal DMA and the read operation is a multi-block read with the Auto CMD12 enabled. For the other two methods (by means of external DMA or CPU polling status) with different transfer methods, the internal DMA parts should be removed and the alternative steps should be straightforward.

The software flow to read from a card is:

1. Check the card status, wait until card is ready for data.
2. Set the card block length/size:
    a. For SD/MMC, use SET_BLOCKLEN (CMD16)
    b. For SDIO cards or the I/O portion of SDCombo cards, use IO_RW_DIRECT(CMD52) to set the I/O block size bit field in the CCCR register (for function 0) or FBR register (for functions 1~7)
3. Set the SDHC block length register to be the same as the block length set for the card in Step 2.
4. Set the SDHC number block register (NOB), nob is 5 (for instance).
5. Disable the buffer read ready interrupt, configure the DMA settings and enable the SDHC DMA when sending the command with data transfer. XFERTYP[AC12EN] must also be set.
6. Wait for the transfer complete interrupt.
7. Check the status bit to see whether a read CRC error occurred, or some another error, occurred during the auto12 command sending and response receiving.

62.7.3.2.2 Read with pause

The read operation is not generally able to pause. Only the SDIO card and SDCombo card working under I/O mode supporting the read and wait feature can pause during the read operation. If the SDIO card support read wait (SRW bit in CCCR register is 1), the Driver can set the SABGREQ bit in the Protocol Control register to pause the transfer between the data blocks. Before setting the SABGREQ bit, make sure the RWCTL bit in the Protocol Control register is set, otherwise the eSDHC will not assert the Read Wait signal during the block gap and data corruption occurs. Set the RWCTL bit after the Read Wait capability of the SDIO card is recognized.

Like the flow described in Normal read, the read with pause is shown with the same kind of read operation:

1. Check the SRW bit in the CCR register on the SDIO card to confirm the card supports Read Wait.
2. Set RWCTL.
3. Check the card status and wait until the card is ready for data.
4. Set the card block length/size:
   a. For SD/MMC, use SET_BLOCKLEN (CMD16)
   b. For SDIO cards or the I/O portion of SDCombo cards, use IO_RW_DIRECT(CMD52) to set the I/O Block Size bit field in the CCCR register (for function 0) or FBR register (for functions 1~7)
5. Set the SDHC block length register to be the same as the block length set for the card in Step 2.
6. Set the SDHC number block register (NOB), nob is 5 (for instance).
7. Disable the buffer read ready interrupt, configure the DMA setting and enable the eSDHC DMA when sending the command with data transfer. AC12EN must also be set.
8. Set SABGREQ.
9. Wait for the Transfer Complete interrupt.
10. Clear SABGREQ.
11. Check the status bit to see whether read CRC error occurred.
12. Set CREQ to continue the read operation.
13. Wait for the Transfer Complete interrupt.
14. Check the status bit to see whether a read CRC error occurred, or some another error, occurred during the auto12 command sending and response receiving.

Like the write operation, it is possible to meet the ending block of the transfer when paused. In this case, the SDHC will ignore the Stop At Block Gap Request and treat it as a command read operation.

Unlike the write operation, there is no remaining data inside the buffer when the transfer is paused. All data received before the pause will be transferred to the Host System. Whether the Suspend Command is sent or not, the internal data buffer is not flushed.

If the Suspend Command is sent and the transfer is later resumed by means of a Resume Command, the SDHC takes the command as a normal one accompanied with data transfer. It is left for the Driver to set all the relevant registers before the transfer is resumed. If there is only one block to send when the transfer is resumed, the MSBSEL and BCEN bits of the Transfer Type register are set, as well as the AC12EN bit. However, the SDHC will automatically send the CMD12 to mark the end of multi-block transfer.

62.7.3.3 Suspend resume

The SDHC supports the suspend resume operations of SDIO cards, although slightly different than the suggested implementation of Suspend in the SDIO card specification.

62.7.3.3.1 Suspend

After setting the PROCTL[SABGREQ] bit, the host driver may send a suspend command to switch to another function of the SDIO card. The SDHC does not monitor the content of the response, therefore it doesn't know whether the suspend command succeeded or not. Accordingly, it doesn't deassert read wait for read pause. To solve this problem, the driver shall not mark the suspend command as a suspend, that is, setting the XFERTYP[CMDTYP] bits to 01. Instead, the driver shall send this command as if it were a normal command, and only when the command succeeds, and the BS bit is set in the response, can the driver send another command marked as suspend to inform the SDHC that the current transfer is suspended. As shown in the following sequence for suspend operation:

1. Set PROCTL[SABGREQ] to pause the current data transfer at block gap.
2. After IRQSTAT[BGE] is set, send the suspend command to suspend the active function. XFERTYP[CMDTYP] field must be 2'b00.
3. Check the BS bit of the CCCR in the response. If it is 1, repeat this step until the BS bit is cleared or abandon the suspend operation according to the Driver strategy.
4. Send another normal I/O command to the suspended function. The XFERTYP[CMDTYP] of this command must be 2'b01, so the SDHC can detect this special setting and be informed that the paused operation has successfully suspended. If the paused transfer is a read operation, the SDHC stops driving DAT2 and goes to the Idle state.
5. Save the context registers in the system memory for later use, including the DMA system address register for internal DMA operation, and the block attribute register.

6. Begin operation for another function on the SDIO card.

62.7.3.3.2 Resume

To resume the data transfer, a resume command shall be issued:

1. To resume the suspended function, restore the context register with the saved value in step 5 of the suspend operation above.
2. Send the resume command. In the transfer type register, all fields are set to the value as if this were another ordinary data transfer, instead of a transfer resume, except the CMDTYP is set to 2'b10.
3. If the resume command has responded, the data transfer will be resumed.

62.7.3.4 ADMA usage

To use the ADMA in a data transfer, the host driver must prepare the correct descriptor chain prior to sending the read/write command:

1. Create a descriptor to set the data length that the current descriptor group is about to transfer. The data length should be even numbers of the block size.
2. Create another descriptor to transfer the data from the address setting in this descriptor. The data address must be at a page boundary (4 KB address aligned).
3. If necessary, create a link descriptor containing the address of the next descriptor. The descriptor group is created in steps 1–3.
4. Repeat steps 1–3 until all descriptors are created.
5. In the last descriptor, set the end flag to 1 and make sure the total length of all descriptors match the product of the block size and block number configured in the BLKATTR register.
6. Set the DSADDR register to the address of the first descriptor and set the PROCTL[DMAS] field to 01 to select the ADMA.
7. Issue a write or read command with XFERTYP[DMAEN] set to 1.

Steps 1–5 are independent of step 6, so step 6 can finish before steps 1–5. Regarding the descriptor configuration, do not to use the link descriptor, as it requires extra system memory access.

62.7.3.5 Transfer error

This section discusses the handling of transfer errors.

62.7.3.5.1 CRC error

It is possible at the end of a block transfer that a write CRC status error or read CRC error occurs. For this type of error, the latest block received shall be discarded. This is because the integrity of the data block is not guaranteed. Discard the following data blocks and retransfer the block from the corrupted one.

For a multi-block transfer, the host driver shall issue a CMD12 to abort the current process and start the transfer by a new data command. In this scenario, even when the XFERTYP[AC12EN] and BCEND bits are set, the SDHC does not automatically send a CMD12 because the last block is not transferred. On the other hand, if it is within the last block that the CRC error occurs, an auto CMD12 will be sent by the SDHC. In this case, the driver shall re-send or re-obtain the last block with a single block transfer.

62.7.3.5.2 Internal DMA error

During the data transfer with internal simple DMA, if the DMA engine encounters some error on the system bus, the DMA operation is aborted and DMA error interrupt is sent to the host system. When acknowledged by such an interrupt, the driver shall calculate the start address of data block in which the error occurs. The start address can be calculated by either:

1. Reading the DMA system address register. The error occurs during the previous burst. Taking the block size, the previous burst length and the start address of the next burst transfer into account, it is straight forward to obtain the start address of the corrupted block.
2. Reading the BLKCNT field of the block attribute register. By the number of blocks left, the total number to transfer, the start address of transfer, and the size of each block, the start address of corrupted block can be determined. When the BCEN bit is not set, the contents of the block attribute register does not change, so this method does not work.

When a DMA error occurs, abort the current transfer by means of a CMD12 (for multi block transfer), apply a reset for data, and restart the transfer from the corrupted block to recover from the error.

62.7.3.5.3 ADMA error

There are three kinds of possible ADMA errors: transfer, invalid descriptor, and data-length mismatch. Whenever these errors occur, the DMA transfer stops and the corresponding error status bit is set. For acknowledging the status, the host driver should recover the error as shown below and retransfer from the place of interruption.

- Transfer error: May occur during data transfer or descriptor fetch. For either scenario, it is recommended to retrieve the transfer context, reset for the data part and re-transfer the block that was corrupted, or the next block if no block is corrupted.
- Invalid descriptor error: For such errors, retrieve the transfer context, reset for the data part, and recreate the descriptor chain from the invalid descriptor, and issue a new transfer. As the data to transfer now may be less than the previous setting, the data length configured in the new descriptor chain should match the new value.
- Data-length mismatch error: It is similar to recover from this error. The host driver polls relating registers to retrieve the transfer context, apply a reset for the data part, configure a new descriptor chain, and make another transfer if there is data left. Like the previous scenario of the invalid descriptor error, the data length must match the new transfer.

62.7.3.5.4 Auto CMD12 error

After the last block of the multi-block transfer is sent or received, and XFERTYP[AC12EN] is set when the data transfer is initiated by the data command, the SDHC automatically sends a CMD12 to the card to stop the transfer. When errors with this command occur, the driver can deal with the situations in the following manner:

1. Auto CMD12 response time-out: It is not certain whether the command is accepted by the card or not. The driver should clear the IRQSTAT[AC12E] bits and resend the CMD12 until it is accepted by the card.
2. Auto CMD12 response CRC error: Because the card responds to the CMD12, the card will abort the transfer. The driver may ignore the error and clear the IRQSTAT[AC12E] bit.
3. Auto CMD12 conflict error or not sent: The command is not sent, so the driver shall send a CMD12 manually.

62.7.3.6 Card interrupt

The external cards can inform the host controller by means of some special signals. For the SDIO card, it can be the low level on the DAT[1] line during some special period. The SDHC only monitors the DAT[1] line and supports the SDIO interrupt.

When the SDIO interrupt is captured by the SDHC, and the host system is informed by the SDHC asserting the SDHC interrupt line, the interrupt service from the host driver is called.

Because the interrupt factor is controlled by the external card, the interrupt from the SDIO card must be served before IRQSTAT[CINT] is cleared by written 1. See Card interrupt handling for the card interrupt handling flow.

62.7.4 Switch function

MMC cards transferring data at bus widths other than 1-bit is a new feature added to the MMC specifications. The high-speed timing mode for all card devices was also recently defined in various card specifications. To enable these new features, a switch command shall be issued by the host driver.

For SDIO cards, the high-speed mode is enabled by writing the EHS bit in the CCCR register after the SHS bit is confirmed. For SD cards, the high speed mode is queried and enabled by a CMD6, with the mnemonic symbol as SWITCH_FUNC. For MMC cards , the high-speed mode is queried by a CMD8 and enabled by a CMD6, with the mnemonic symbol as SWITCH.

The 4-bit and 8-bit bus width of the MMC is also enabled by the SWITCH command, but with a different argument.

These new functions can also be disabled by a software reset. For SDIO cards it can be done by setting the RES bit in the CCCR register. For other cards, it can be accomplished by issuing a CMD0. This method of restoring to the normal mode is not recommended because a complete identification process is needed before the card is ready for data transfer.

For the sake of simplicity, the following flowcharts do not show current capability check, which is recommended in the function switch process.

62.7.4.1 Query, enabl,e and disable SDIO high-speed mode

```
enable_sdio_high_speed_mode(void)
{
```

```
send CMD52 to query bit SHS at address 0x13;
if (SHS bit is '0') report the SDIO card does not support high speed mode and return;
send CMD52 to set bit EHS at address 0x13 and read after write to confirm EHS bit is set;
change clock divisor value or configure the system clock feeding into eSDHC to generate the
card_clk of around 50MHz;
(data transactions like normal peers)
}
disable_sdio_high_speed_mode(void)
{
send CMD52 to clear bit EHS at address 0x13 and read after write to confirm EHS bit is
cleared;
change clock divisor value or configure the system clock feeding into eSDHC to generate the
card_clk of the desired value below 25MHz;
(data transactions like normal peers)
}
```

62.7.4.2 Query, enable, and disable SD high-speed mode

```
enable_sd_high_speed_mode(void)
{
set BLKCNT field to 1 (block), set BLKSIZE field to 64 (bytes);
send CMD6, with argument 0xFFFFF1 and read 64 bytes of data accompanying the R1 response;
wait data transfer done bit is set;
check if the bit 401 of received 512 bit is set;
if (bit 401 is '0') report the SD card does not support high speed mode and return;
send CMD6, with argument 0x80FFFFF1 and read 64 bytes of data accompanying the R1 response;
check if the bit field 379~376 is 0xF;
if (the bit field is 0xF) report the function switch failed and return;
change clock divisor value or configure the system clock feeding into eSDHC to generate the
card_clk of around 50MHz;
(data transactions like normal peers)
}
disable_sd_high_speed_mode(void)
{
set BLKCNT field to 1 (block), set BLKSIZE field to 64 (bytes);
send CMD6, with argument 0x80FFFFF0 and read 64 bytes of data accompanying the R1 response;
check if the bit field 379~376 is 0xF;
if (the bit field is 0xF) report the function switch failed and return;
change clock divisor value or configure the system clock feeding into eSDHC to generate the
card_clk of the desired value below 25MHz;
(data transactions like normal peers)
}
```

62.7.4.3 Query, enable, and disable MMC high-speed mode

```
enable_mmc_high_speed_mode(void)
{
send CMD9 to get CSD value of MMC;
check if the value of SPEC_VER field is 4 or above;
if (SPEC_VER value is less than 4) report the MMC does not support high speed mode and
return;
set BLKCNT field to 1 (block), set BLKSIZE field to 512 (bytes);
send CMD8 to get EXT_CSD value of MMC;
extract the value of CARD_TYPE field to check the 'high speed mode' in this MMC is 26MHz or
52MHz;
send CMD6 with argument 0x1B90100;
send CMD13 to wait card ready (busy line released);
send CMD8 to get EXT_CSD value of MMC;
check if HS_TIMING byte (byte number 185) is 1;
if (HS_TIMING is not 1) report MMC switching to high speed mode failed and return;
change clock divisor value or configure the system clock feeding into eSDHC to generate the
```

```
card_clk of around 26MHz or 52MHz according to the CARD_TYPE;
(data transactions like normal peers)
}
disable_mmc_high_speed_mode(void)
{
send CMD6 with argument 0x2B90100;
set BLKCNT field to 1 (block), set BLKSIZE field to 512 (bytes);
send CMD8 to get EXT_CSD value of MMC;
check if HS_TIMING byte (byte number 185) is 0;
if (HS_TIMING is not 0) report the function switch failed and return;
change clock divisor value or configure the system clock feeding into eSDHC to generate the
card_clk of the desired value below 20MHz;
(data transactions like normal peers)
}
```

62.7.4.4 Set MMC bus width

```
change_mmc_bus_width(void)
{
send CMD9 to get CSD value of MMC;
check if the value of SPEC_VER field is 4 or above;
if (SPEC_VER value is less than 4) report the MMC does not support multiple bit width and
return;
send CMD6 with argument 0x3B70x00; (8-bit, x=2; 4-bit, x=1; 1-bit, x=0)
send CMD13 to wait card ready (busy line released);
(data transactions like normal peers)
}
```

62.7.5 ADMA operation

This section presents code examples for ADMA operation.

62.7.5.1 ADMA1 operation

```
Set_adma1_descriptor
{
      if (to start data transfer) {
          // Make sure the address is 4KB align.
          Set 'Set' type descriptor;
          {
              Set Act bits to 01;
              Set [31:12] bits data length (byte unit);
          }
          Set 'Tran' type descriptor;
          {
              Set Act bits to 10;
              Set [31:12] bits address (4KB align);
          }
      }
      else if (to fetch descriptor at non-continuous address) {
          Set Act bits to 11;
          Set [31:12] bits the next descriptor address (4KB align);
      }
      else { // other types of descriptor
          Set Act bits accordingly
      }
```

```
        if (this descriptor is the last one) {
            Set End bit to 1;
        }
        if (to generate interrupt for this descriptor) {
            Set Int bit to 1;
        }
        Set Valid bit to 1;
}
```

62.7.5.2 ADMA2 operation

```
Set_adma2_descriptor
{
        if (to start data transfer) {
            // Make sure the address is 32-bit boundary (lower 2-bit are always '00').
            Set higher 32-bit of descriptor for this data transfer initial address;
            Set [31:16] bits data length (byte unit);
            Set Act bits to '10';
        }
        else if (to fetch descriptor at non-continuous address) {
            Set Act bits to '11';
            // Make sure the address is 32-bit boundary (lower 2-bit are always set to '00').
            Set higher 32-bit of descriptor for the next descriptor address;
        }
        else { // other types of descriptor
            Set Act bits accordingly
        }
        if (this descriptor is the last one) {
            Set 'End' bit '1';
        }
        if (to generate interrupt for this descriptor) {
            Set 'Int' bit '1';
        }
        Set the 'Valid' bit to '1';
}
```

62.7.6 Fast boot operation

This section discusses fast boot operations.

62.7.6.1 Normal fast boot flow

1. Software needs to configure SYSCTL[INITA] to make sure 74 card clocks are finished.
2. Software needs to configure MMCBOOT[BOOTEN] to 1, MMCBOOT[BOOTMODE] to 0, and MMCBOOT[BOOTACK] to select the ack mode or not. If sending through DMA mode, software needs to configure MMCBOOT[AUTOSABGEN] to enable automatically stop at block gap feature, and MMCBOOT[DTOCVACK] to select the ack timeout value according to the sd clk frequence.

3. Software then needs to configure BLKATTR register to set block size/no.
4. Software needs to configure PROCTL[DTW].
5. Software needs to configure CMDARG to set argument if needed (no need in normal fast boot).
6. Software needs to configure XFERTYP register to start the boot process. In Normal Boot mode, XFERTYP[CMDINX], XFERTYP[CMDTYP], XFERTYP[RSPTYP], XFERTYP[CICEN], XFERTYP[CCCEN], XFERTYP[AC12EN], XFERTYP[BCEN] and XFERTYP[DMAEN] are kept default value. XFERTYP[DPSEL] bit is set to 1, XFERTYP[DTDSEL] is set to 1, XFERTYP[MSBSEL] is set to 1. Note XFERTYP[DMAEN] must be configured as 0 in polling mode. And if XFERTYP[BCEN] is configured as 1, better to configure BLKATTR[BLKSIZE] to the max value.
7. When the step 6 is configured, boot process will begin. Software needs to poll the data buffer ready status to read the data from buffer in time. If boot time-out happened (ack time out or the first data read time out), Interrupt will be triggered, and software need to configure MMCBOOT[]BOOTEN] to 0 to disable boot. Thus will make CMD high, and then after at least 56 clocks, it is ready to begin normal initialization process.
8. If no time out, software needs to decide the data read is finished and then configure MMCBOOT[]BOOTEN] to 0 to disable boot. This will make CMD line high and command completed asserted. After at least 56 clocks, it is ready to begin normal initialization process.
9. Reset the host and then can begin the normal process.

62.7.6.2 Alternative fast boot flow

1. Software needs to configure init_active bit (system control register bit 27) to make sure 74 card clocks are finished.
2. Software needs to configure MMCBOOT [BOOTEN] to 1, MMCBOOT [BOOTMODE] to 1, and MMCBOOT [BOOTACK] to select the ack mode or not. If sending through DMA mode, it also needs to configure MMCBOOT [AUTOSABGEN] to enable automatically stop at block gap feature. And needs to configure MMCBOOT [DTOCVACK] to select the ack timeout value according to the sd clk frequence.
3. Software then needs to configure BLKATTR register to set block size/no.

4. Software needs to configure PROCTL[DTW].
5. Software needs to configure CMDARG register to set argument to 0xFFFFFFFA.
6. Software needs to configure XFERTYP register to start the boot process by CMD0 with 0xFFFFFFFA argument . In alternative boot, CMDINX, CMDTYP, RSPTYP, CICEN, CCCEN, AC12EN, BCEN, and DMAEN are kept default value. DPSEL bit is set to 1, DTDSEL is set to 1, MSBSEL is set to 1. Note DMAEN should be configured as 0 in polling mode. And if BCEN is configured as 1 in Polling mode, it is better to configure blk no in Bock Attributes Register to the max value.
7. When step 6 is configured, boot process will begin. Software needs to poll the data buffer ready status to read the data from buffer in time. If boot time out (ack data time out in 50ms or data time out in 1s), host will send out the interrupt and software need to send CMD0 with reset and then configure boot enable bit to 0 to stop this process. After command completed, configure MMCBOOT[BOOTEN] to 0 to disable boot. After at least 8 clocks from command completed, card is ready for identification step.
8. If no time out, software needs to decide when to stop the boot process, and send out the CMD0 with reset and then after command completed, configure MMCBOOT[BOOTEN] to stop the process. After 8 clocks from command completed, slave(card) is ready for identification step.
9. Reset the host and then begin the normal process.

62.7.6.3 Fast boot application case in DMA mode

In the boot application case, because the image destination and the image size are contained in the beginning of the image, switching DMA parameters on the fly during MMC fast boot is required.

In fast boot, host can use ADMA2 (advanced DMA2) with two destinations.

The detail flow:

1. Software needs to configure init_active bit (system control register bit 27) to make sure 74 card clocks are finished.
2. Software needs to configure MMCBOOT[BOOTEN] to 1; and MMCBOOT[BOOTMODE] to 0 (normal fast boot), to 1(alternative boot); and MMCBOOT[BOOTACK] to select the ack mode or not. In DMA mode, configure MMCBOOT[AUTOSABGEN] to 1 for enable automatically stop at block gap feature. Also configure MMCBOOT[BOOTBLKCNT] to set the VAULE1 (value of

block count that need to trans first time), so that host will stop at block gap when card block counter is equal to this value. And it needs to configure MMCBOOT[DTOCVACK] to select the ack timeout value according to the sd clk frequence.

3. Software then needs to configure BLKATTR register to set block size/no. In DMA mode, it is better to set block number to the max value(16'hffff).
4. Software needs to configure PROCTL[DTW].
5. Software enables ADMA2 by configuring PROCTL[DMAS].
6. Software need to set at least three pairs ADMA2 descriptor in boot memory (that is, in IRAM, at least 6 words). The first pair descriptor define the start address (IRAM) and data length(512byte*VALUE1) of first part boot code. Software also need to set the second pair descriptor, the second start address (any value that is writable), data length is suggest to set 1~2 word (record as VAULE2). Note: the second couple desc also transfer useful data even at lease 1 word. Because our ADMA2 can't support 0 data_length data transfer descriptor.
7. Software needs to configure CMDARG register to set argument to 0xFFFFFFFA in alternative fast boot, and doesn't need to be set in normal fast boot.
8. Software needs to configure XFERTYP register to start the boot process . XFERTYP[CMDINX], XFERTYP[CMDTYP], XFERTYP[RSPTYP], XFERTYP[CICEN], XFERTYP[CCCEN], XFERTYP[AC12EN], XFERTYP[BCEN], and XFERTYP[DMAEN] are kept at default value. XFERTYP[DPSEL] bit is set to 1, XFERTYP[DTDSEL] is set to 1, XFERTYP[MSBSEL] is set to 1. XFERTYP[DMAEN] is configured as 1 in DMA mode. And if XFERTYP[BCEN] is configured as 1, better to configure blk no in BLKATTR register to the max value.
9. When step 8 is configured, boot process will begin, the first VAULE1 block number data has transfer. Software needs to poll IRQSTAT[TC] bit to determine first transfer is end. Also software needs to poll IRQSTAT[BGE] bit to determine if first transfer stop at block gap.
10. When IRQSTAT[TC] and IRQSTAT[BGE] bits are 1, . SW can analyzes the first code of VAULE1 block, initializes the new memory device, if required, and sets the third pair of descriptors to define the start address and length of the remaining part of boot code (VAULE3 the remain boot code block). Remember set the last descriptor with END.
11. Software needs to configure MMCBOOT register (offset 0xc4) again. Set MMCBOOT[BOOTEN] bit to 1; and MMCBOOT[BOOTMODE] bit to 0 (normal fast boot), to 1 (alternative boot); and MMCBOOT[BOOTACK] bit to select the ack

mode or not. In DMA mode, configure MMCBOOT[AUTOSABGEN] bit to 1 for enable automatically stop at block gap feature. Also configure MMCBOOT[BOOTBLKCNT] bit to set the (VAULE1+1+VAULE3), so that host will stop at block gap when card block counter is equal to this value. And need to configure MMCBOOT[DTOCVACK] bit to select the ack timeout value according to the sd clk frequence.

12. Software needs to clear IRQSTAT[TC] and IRQSTAT[BGE] bit. And software need to clear PROCTL[SABGREQ], and set PROCTL[CREQ] to 1 to resume the data transfer. Host will transfer the VALUE2 and VAULE3 data to the destination that is set by descriptor.
13. Software needs to poll IRQSTAT[BGE] bit to determine if the fast boot is over.

Note

1. When ADMA boot flow is started, for SDHC, it is like a normal ADMA read operation. So setting ADMA2 descriptor as the normal ADMA2 transfer.
2. Need a few words length memory to keep descriptor.
3. For the 1~2 words data in second descriptor setting, it is the useful data, so software need to deal the data due to the application case.

62.7.7 Commands for MMC/SD/SDIO

The following table lists the commands for the MMC/SD/SDIO cards.

See the corresponding specifications for more details about the command information.

There are four kinds of commands defined to control the Multimediacard:

- Broadcast commands (bc), no response
- Broadcast commands with response (bcr), response from all cards simultaneously
- Addressed (point-to-point) commands (ac), no data transfer on the DAT
- Addressed (point-to-point) data transfer commands (adtc)

Table 62-12. Commands for MMC/SD/SDIO cards

CMD INDEX	Type	Argument	Resp	Abbreviation	Description
CMD0	bc	[31:0] stuff bits	-	GO_IDLE_STATE	Resets all MMC and SD memory cards to idle state.
CMD1	bcr	[31:0] OCR without busy	R3	SEND_OP_COND	Asks all MMC and SD memory cards in idle state to send their operation conditions register contents in the response on the CMD line.
CMD2	bcr	[31:0] stuff bits	R2	ALL_SEND_CID	Asks all cards to send their CID numbers on the CMD line.
CMD3[1]	ac	[31:6] RCA [15:0] stuff bits	R1 R6 (SDIO)	SET/ SEND_RELATIVE_ADDR	Assigns relative address to the card.
CMD4	bc	[31:0] DSR [15:0] stuff bits	-	SET_DSR	Programs the DSR of all cards.
CMD5	bc	[31:0] OCR without busy	R4	IO_SEND_OP_COND	Asks all SDIO cards in idle state to send their operation conditions register contents in the response on the CMD line.
CMD6[2]	adtc	[31] Mode 0: Check function 1: Switch function [30:8] Reserved for function groups 6 ~ 3 (All 0 or 0xFFFF) [7:4] Function group1 for command system [3:0] Function group2 for access mode	R1	SWITCH_FUNC	Checks switch ability (mode 0) and switch card function (mode 1). Refer to "SD Physical Specification V1.1" for more details.
CMD6[3]	ac	[31:26] Set to 0 [25:24] Access [23:16] Index [15:8] Value [7:3] Set to 0 [2:0] Cmd Set	R1b	SWITCH	Switches the mode of operation of the selected card or modifies the EXT_CSD registers. Refer to "The MultiMediaCard System Specification Version 4.0 Final draft 2" for more details.
CMD7	ac	[31:6] RCA [15:0] stuff bits	R1b	SELECT/ DESELECT_CARD	Toggles a card between the stand-by and transfer states or between the programming and disconnect states. In both cases, the card is selected by its own relative address and gets deselected by any other address. Address 0 deselects all.

Table continues on the next page...

Table 62-12. Commands for MMC/SD/SDIO cards (continued)

CMD INDEX	Type	Argument	Resp	Abbreviation	Description
CMD8	adtc	[31:0] stuff bits	R1	SEND_EXT_CSD	The card sends its EXT_CSD register as a block of data, with a block size of 512 bytes.
CMD9	ac	[31:6] RCA [15:0] stuff bits	R2	SEND_CSD	Addressed card sends its card-specific data (CSD) on the CMD line.
CMD10	ac	[31:6] RCA [15:0] stuff bits	R2	SEND_CID	Addressed card sends its card-identification (CID) on the CMD line.
CMD11	adtc	[31:0] data address	R1	READ_DAT_UNTIL_STOP	Reads data stream from the card, starting at the given address, until a STOP_TRANSMISSION follows.
CMD12	ac	[31:0] stuff bits	R1b	STOP_TRANSMISSION	Forces the card to stop transmission.
CMD13	ac	[31:6] RCA [15:0] stuff bits	R1	SEND_STATUS	Addressed card sends its status register.
CMD14	Reserved				
CMD15	ac	[31:6] RCA [15:0] stuff bits	-	GO_INACTIVE_STATE	Sets the card to inactive state to protect the card stack against communication breakdowns.
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	Sets the block length (in bytes) for all following block commands (read and write). Default block length is specified in the CSD.
CMD17	adtc	[31:0] data address	R1	READ_SINGLE_BLOCK	Reads a block of the size selected by the SET_BLOCKLEN command.
CMD18	adtc	[31:0] data address	R1	READ_MULTIPLE_BLOCK	Continuously transfers data blocks from card to host until interrupted by a stop command.
CMD19	Reserved				
CMD20	adtc	[31:0] data address	R1	WRITE_DAT_UNTIL_STOP	Writes data stream from the host, starting at the given address, until a STOP_TRANSMISION follows.
CMD21-23	Reserved				
CMD24	adtc	[31:0] data address	R1	WRITE_BLOCK	Writes a block of the size selected by the SET_BLOCKLEN command.
CMD25	adtc	[31:0] data address	R1	WRITE_MULTIPLE_BLOCK	Continuously writes blocks of data until a STOP_TRANSMISSION follows.

Table continues on the next page...

Table 62-12. Commands for MMC/SD/SDIO cards (continued)

CMD INDEX	Type	Argument	Resp	Abbreviation	Description
CMD26	adtc	[31:0] stuff bits	R1	PROGRAM_CID	Programming of the card identification register. This command shall be issued only once per card. The card contains hardware to prevent this operation after the first programming. Normally this command is reserved for the manufacturer.
CMD27	adtc	[31:0] stuff bits	R1	PROGRAM_CSD	Programming of the programmable bits of the CSD.
CMD28	ac	[31:0] data address	R1b	SET_WRITE_PROT	If the card has write protection features, this command sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE).
CMD29	ac	[31:0] data address	R1b	CLR_WRITE_PROT	If the card provides write protection features, this command clears the write protection bit of the addressed group.
CMD30	adtc	[31:0] write protect data address	R1	SEND_WRITE_PROT	If the card provides write protection features, this command asks the card to send the status of the write protection bits.
CMD31	Reserved				
CMD32	ac	[31:0] data address	R1	TAG_SECTOR_START	Sets the address of the first sector of the erase group.
CMD33	ac	[31:0] data address	R1	TAG_SECTOR_END	Sets the address of the last sector in a continuous range within the selection of a single sector to be selected for erase.
CMD34	ac	[31:0] data address	R1	UNTAG_SECTOR	Removes one previously selected sector from the erase selection.
CMD35	ac	[31:0] data address	R1	TAG_ERASE_GROUP_START	Sets the address of the first erase group within a range to be selected for erase.
CMD36	ac	[31:0] data address	R1	TAG_ERASE_GROUP_END	Sets the address of the last erase group within a continuous range to be selected for erase.
CMD37	ac	[31:0] data address	R1	UNTAG_ERASE_GROUP	Removes one previously selected erase group from the erase selection.

Table continues on the next page...

Table 62-12. Commands for MMC/SD/SDIO cards (continued)

CMD INDEX	Type	Argument	Resp	Abbreviation	Description
CMD38	ac	[31:0] stuff bits	R1b	ERASE	Erase all previously selected sectors.
CMD39	ac	[31:0] RCA [15] register write flag [14:8] register address [7:0] register data	R4	FAST_IO	Used to write and read 8-bit (register) data fields. The command addresses a card, and a register, and provides the data for writing if the write flag is set. The R4 response contains data read from the address register. This command accesses application dependent registers which are not defined in the MMC standard.
CMD40	bcr	[31:0] stuff bits	R5	GO_IRQ_STATE	Sets the system into interrupt mode.
CMD41	Reserved				
CDM42	adtc	[31:0] stuff bits	R1b	LOCK_UNLOCK	Used to set/reset the password or lock/unlock the card. The size of the data block is set by the SET_BLOCK_LEN command.
CMD43~51	Reserved				
CMD52	ac	[31:0] stuff bits	R5	IO_RW_DIRECT	Access a single register within the total 128k of register space in any I/O function.
CMD53	ac	[31:0] stuff bits	R5	IO_RW_EXTENDED	Accesses a multiple I/O register with a single command. Allows the reading or writing of a large number of I/O registers.
CMD54	Reserved				
CMD55	ac	[31:16] RCA [15:0] stuff bits	R1	APP_CMD	Indicates to the card that the next command is an application specific command rather that a standard command.
CMD56	adtc	[31:1] stuff bits [0]: RD/WR	R1b	GEN_CMD	Used either to transfer a data block to the card or to get a data block from the card for general purpose / application specific commands. The size of the data block is set by the SET_BLOCK_LEN command.
CMD57~59	Reserved				
CMD60	adtc	[31] WR [30:24] stuff bits [23:16] address [15:8] stuff bits	R1b	RW_MULTIPLE_REGISTER	These registers are used to control the behavior of the device and to retrieve status information regarding the operation of the device. All

Table continues on the next page...

Table 62-12. Commands for MMC/SD/SDIO cards (continued)

CMD INDEX	Type	Argument	Resp	Abbreviation	Description
		[7:0] byte count			Status and Control registers are WORD (32-bit) in size and are WORD aligned. CMD60 shall be used to read and write these registers.
CMD61	adtc	[31] WR [30:16] stuff bits [15:0] data unit count	R1b	RW_MULTIPLE_BLOCK	The host issues a RW_MULTIPLE_BLOCK (CMD61) to begin the data transfer.
CMD62~63	Reserved				
ACMD6[4]	ac	[31:2] stuff bits [1:0] bus width	R1	SET_BUS_WIDTH	Defines the data bus width ('00'=1bit or '10'=4bit bus) to be used for data transfer. The allowed data bus widths are given in SCR register.
ACMD13[4]	adtc	[31:0] stuff bits	R1	SD_STATUS	Send the SD memory card status.
ACMD22[4]	adtc	[31:0] stuff bits	R1	SEND_NUM_WR_SECTORS	Send the number of the written sectors (without errors). Responds with 32-bit plus the CRC data block.
ACMD23[4]	ac		R1	SET_WR_BLK_ERASE_COUNT	-
ACMD41[4]	bcr	[31:0] OCR	R3	SD_APP_OP_COND	Asks the accessed card to send its operating condition register (OCR) contents in the response on the CMD line.
ACMD42[4]	ac		R1	SET_CLR_CARD_DETECT	-
ACMD51[4]	adtc	[31:0] stuff bits	R1	SEND_SCR	Reads the SD Configuration Register (SCR).

1. CMD3 differs for MMC and SD cards. For MMC cards, it is referred to as SET_RELATIVE_ADDR, with a response type of R1. For SD cards, it is referred to as SEND_RELATIVE_ADDR, with a response type of R6 (with RCA inside).
2. CMD6 differs completely between high speed MMC cards and high speed SD cards. Command SWITCH_FUNC is for high speed SD cards.
3. Command SWITCH is for high speed MMC cards . The Index field can contain any value from 0-255, but only values 0-191 are valid. If the Index value is in the 192-255 range the card does not perform any modification and the SWITCH_ERROR status bit in the EXT_CSD register is set. The Access Bits are shown in Table 2.
3. Command SWITCH is for high speed MMC cards . The Index field can contain any value from 0-255, but only values 0-191 are valid. If the Index value is in the 192-255 range the card does not perform any modification and the SWITCH_ERROR status bit in the EXT_CSD register is set. The Access Bits are shown in Table 2.
4. ACMDs shall be preceded with the APP_CMD command. (Commands listed are used for SD only, other SD commands not listed are not supported on this module).

The Access Bits for the EXT_CSD Access Modes are shown in the following table.

Table 62-13. EXT_CSD Access Modes

Bits	Access Name	Operation
00	Command Set	The command set is changed according to the Cmd Set field of the argument
01	Set Bits	The bits in the pointed byte are set, according to the 1 bits in the Value field.
10	Clear Bits	The bits in the pointed byte are cleared, according to the 1 bits in the Value field.
11	Write Byte	The Value field is written into the pointed byte.

62.8 Software restrictions

Software for the SDHC must observe the following restrictions.

62.8.1 Initialization active

The driver cannot set SYSCTL[INITA] when any of the command line or data lines is active, so the driver must ensure both PRSSTAT[CDIHB] and PRSSTAT[CIHB] bits are cleared. To auto clear SYSCTL[INITA], SYSCTL[SDCLKEN] must be 1, otherwise no clocks can go out to the card and SYSCTL[INITA] will never clear.

62.8.2 Software polling procedure

For polling read or write, when the software begins a buffer read or write, it must access exactly the number of times as the values set in the watermark level register. Moreover, if the block size is not the times of the value in watermark level register, read and write respectively, the software must access exactly the remained number of words at the end of each block.

For example, for read operation, if the WML[RDWML] is 4, indicating the watermark level is 16 bytes, block size is 40 bytes, and the block number is 2, then the access times for the burst sequence in the whole transfer process must be 4, 4, 2, 4, 4, 2.

62.8.3 Suspend operation

To suspend the data transfer, the software must inform SDHC that the suspend command is successfully accepted. To achieve this, after the suspend command is accepted by the SDIO card, software must send another normal command marked as suspend command (XFERTYP[CMDTYP] bits set as 01) to inform SDHC that the transfer is suspended.

If software needs resume the suspended transfer, it should read the value in BLKATTR[BLKCNT] to save the remained number of blocks before sending the normal command marked as suspend, otherwise on sending such suspend command, SDHC will regard the current transfer as aborted and change BLKATTR[BLKCNT] to its original value, instead of keeping the remained number of blocks.

62.8.4 Data length setting

For either ADMA (ADMA1 or ADMA2) transfer, the data in the data buffer must be word aligned, so the data length set in the descriptor must be times of 4.

62.8.5 (A)DMA address setting

To configure ADMA1/ADMA2/DMA address register, when TC[IRQSTAT] is set, the register will always update itself with the internal address value to support dynamic address synchronization, so software must ensure that TC[IRQSTAT] is cleared prior to configuring ADMA1/ADMA2/DMA address register.

62.8.6 Data port access

Data port does not support parallel access. For example, during an external DMA access, it is not allowed to write any data to the data port by CPU; or during a CPU read operation, it is also prohibited to write any data to the data port, by either CPU or external DMA. Otherwise the data would be corrupted inside the SDHC buffer.

62.8.7 Change clock frequency

SDHC does not automatically gates off the card clock when the host driver changes the clock frequency. To remove possible glitch on the card clock, clear SYSCTL[SDCLKEN] when changing clock divisor value and set SYSCTL[SDCLKEN] to 1 after PRSSTAT[SDSTB] is 1 again.

62.8.8 Multi-block read

For predefined multi-block read operation, that is, the number of blocks to read has been defined by previous CMD23 for MMC, or predefined number of blocks in CMD53 for SDIO/SDCombo, or whatever multi-block read without abort command at card side, an

abort command, either automatic or manual CMD12/CMD52, is still required by SDHC after the pre-defined number of blocks are done, to drive the internal start response timeout. Manually sending an abort command with XFERTYP[RSPTYP] both bits cleared is recommended.

Chapter 63
Touch Sensing Input (TSI)

63.1 Chip-specific TSI information

63.1.1 TSI Instantiation Information

This device includes one TSI module containing the channels as shown in the following table. In Stop, VLPS, LLS and VLLSx modes any one channel can be enabled to be the wakeup source.

TSI0 hardware trigger is from the LPTMR.

The number of TSI channels present on the device is determined by the pinout of the specific device package and is shown in the following table.

Table 63-1. Number of TSI channels

Device	TSI0 channels
MK82FN256VDC15	16
MK82FN256VLL15	16

63.1.2 TSI Interrupts

The TSI has multiple sources of interrupt requests. However, these sources are OR'd together to generate a single interrupt request. When a TSI interrupt occurs, read the TSI status register to determine the exact interrupt source.

63.2 Introduction

The touch sensing input (TSI) module provides capacitive touch sensing detection with high sensitivity and enhanced robustness.

Each TSI pin implements the capacitive measurement by a current source scan, charging and discharging the electrode, once or several times. A reference oscillator ticks the scan time and stores the result in a 16-bit register when the scan completes. Meanwhile, an interrupt request is submitted to CPU for post-processing if TSI interrupt is enabled and DMA function is not selected.The TSI module can be periodically triggered to work in low power mode with ultra-low current adder and wake CPU at the end of scan or the conversion result is out of the range specified by TSI threshold. It provides a solid capacitive measurement module to the implementation of touch keyboard, rotaries and sliders.

63.2.1 Features

TSI features includes:

- Support up to 16 external electrodes
- Automatic detection of electrode capacitance across all operational power modes
- Internal reference oscillator for high-accuracy measurement
- Configurable software or hardware scan trigger
- Fully support Freescale touch sensing software (TSS) library, see www.freescale.com/touchsensing.
- Capability to wake MCU from low power modes
- Compensate for temperature and supply voltage variations
- High sensitivity change with 16-bit resolution register
- Configurable up to 4096 scan times.
- Support DMA data transfer

For electrode design recommendations, refer to AN3863: Designing Touch Sensing Electrodes

63.2.2 Modes of operation

This module supports the following operation modes.

Table 63-2. Operating modes

Mode	Description
Stop and low power stop	TSI module is fully functional in all of the stop modes as long as TSI_GENCS[STPE] is set. The channel specified by TSI_DATA[TSICH] will be scanned upon the trigger. After scan finishes, either end-of-scan or out-of-range interrupt can be selected to bring MCU out of low power modes.
Wait	TSI module is fully functional in this mode. When a scan completes, TSI submits an interrupt request to CPU if the interrupt is enabled.
Run	TSI module is fully functional in this mode. When a scan completes, TSI submits an interrupt request to CPU if the interrupt is enabled.

63.2.3 Block diagram

The following figure is a block diagram of the TSI module.

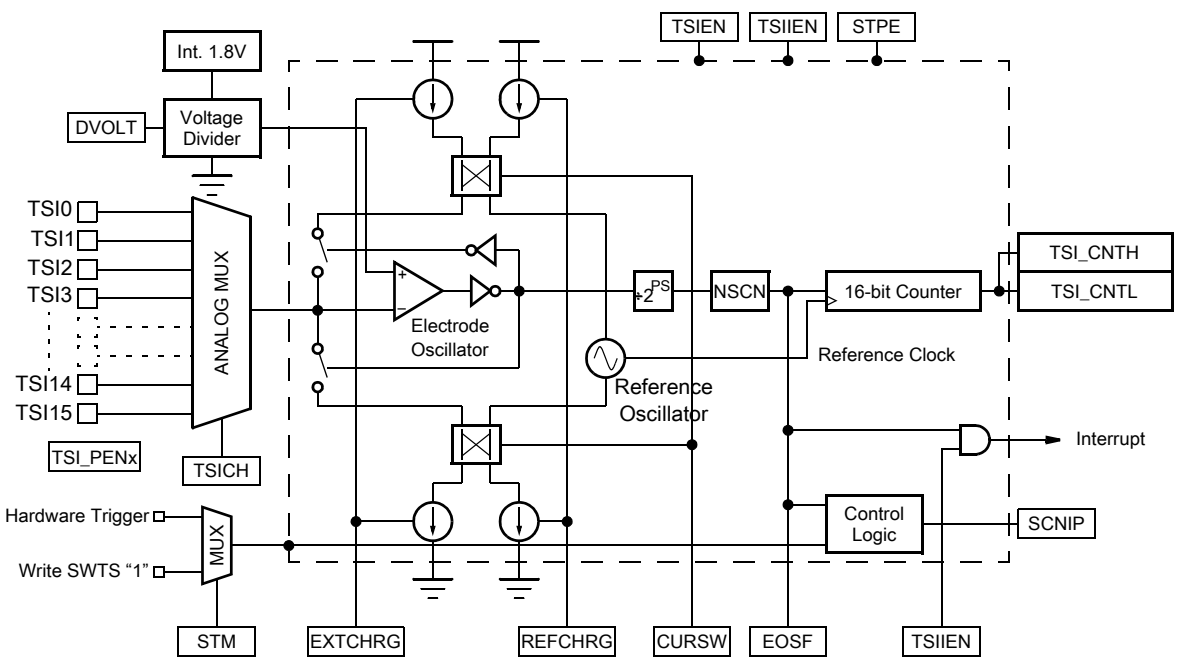


Figure 63-1. TSI module block diagram

63.3 External signal description

The TSI module contains up to 16 external pins for touch sensing. The table found here describes each of the TSI external pins.

Table 63-3. TSI signal description

Name	Port	Direction	Function	Reset state
TSI[15:0]	TSI	I/O	TSI capacitive pins. Switches driver that connects directly to the electrode pins TSI[15:0] can operate as GPIO pins.	I/O

63.3.1 TSI[15:0]

When TSI functionality is enabled , the TSI analog portion uses the corresponding channel to connect external on-board touch capacitors. The PCB connection between the pin and the touch pad must be kept as short as possible to reduce distribution capacity on board.

63.4 Register definition

This section describes the memory map and control/status registers for the TSI module.

TSI memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4004_5000	TSI General Control and Status Register (TSI0_GENCS)	32	R/W	0000_0000h	63.4.1/2164
4004_5004	TSI DATA Register (TSI0_DATA)	32	R/W	0000_0000h	63.4.2/2169
4004_5008	TSI Threshold Register (TSI0_TSHD)	32	R/W	0000_0000h	63.4.3/2170

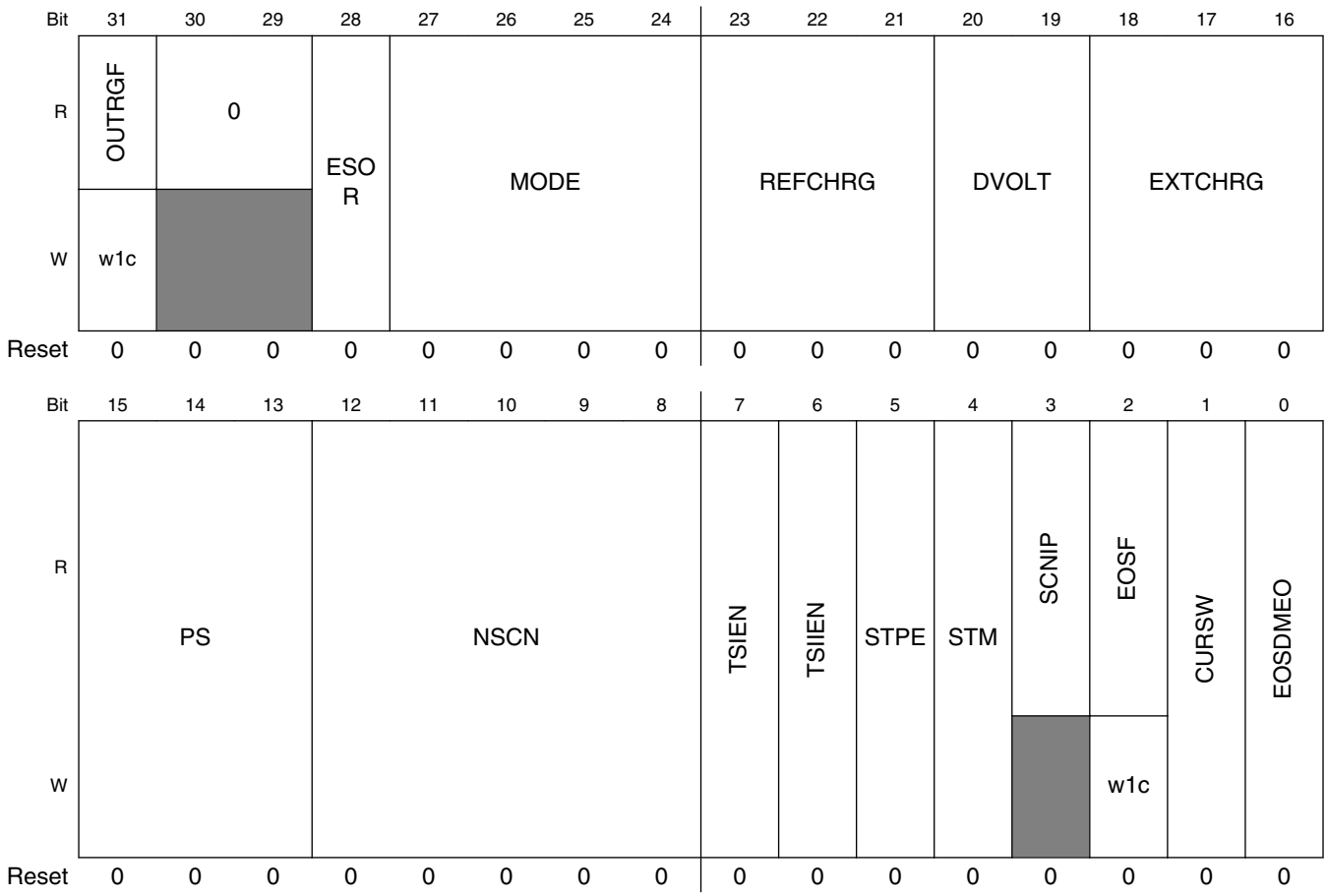
63.4.1 TSI General Control and Status Register (TSIx_GENCS)

This control register provides various control and configuration information for the TSI module.

NOTE

When TSI is working, the configuration bits (GENCS[TSIEN], GENCS[TSIIEN], and GENCS[STM]) must not be changed. The EOSF flag is kept until the software acknowledge it.

Address: 4004_5000h base + 0h offset = 4004_5000h



TSIx_GENCS field descriptions

Field	Description
31 OUTRGF	Out of Range Flag. This flag is set if the result register of the enabled electrode is out of the range defined by the TSI_THRESHOLD register. This flag is set only when TSI is configured in non-noise detection mode. It can be read once the CPU wakes. Write "1" , when this flag is set, to clear it.
30–29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28 ESOR	End-of-scan or Out-of-Range Interrupt Selection This bit is used to select out-of-range or end-of-scan event to generate an interrupt. 0 Out-of-range interrupt is allowed. 1 End-of-scan interrupt is allowed.

Table continues on the next page...

TSIx_GENCS field descriptions (continued)

Field	Description
27–24 MODE	TSI analog modes setup and status bits. Set up TSI analog modes, especially, setting MODE[3:2] to not 2'b00 will configure TSI to noise detection modes. MODE[1:0] take no effect on TSI operation mode and should always write to 2'b00 for setting up. When reading this field will return the analog status. Refer to chapter "Noise detection mode" for details. 0000 Set TSI in capacitive sensing(non-noise detection) mode. 0100 Set TSI analog to work in single threshold noise detection mode and the frequency limitation circuit is disabled. 1000 Set TSI analog to work in single threshold noise detection mode and the frequency limitation circuit is enabled to work in higher frequencies operations. 1100 Set TSI analog to work in automatic noise detection mode.
23–21 REFCHRG	REFCHRG These bits indicate the reference oscillator charge and discharge current value. 000 500 nA. 001 1 µA. 010 2 µA. 011 4 µA. 100 8 µA. 101 16 µA. 110 32 µA. 111 64 µA.
20–19 DVOLT	DVOLT These bits indicate the oscillator's voltage rails as below. 00 DV = 1.026 V; V_P = 1.328 V; V_m = 0.302 V. 01 DV = 0.592 V; V_P = 1.111 V; V_m = 0.519 V. 10 DV = 0.342 V; V_P = 0.986 V; V_m = 0.644 V. 11 DV = 0.197 V; V_P = 0.914 V; V_m = 0.716 V.
18–16 EXTCHRG	EXTCHRG These bits indicate the electrode oscillator charge and discharge current value. 000 500 nA. 001 1 µA. 010 2 µA. 011 4 µA. 100 8 µA. 101 16 µA. 110 32 µA. 111 64 µA.
15–13 PS	PS These bits indicate the prescaler of the output of electrode oscillator. 000 Electrode Oscillator Frequency divided by 1 001 Electrode Oscillator Frequency divided by 2

Table continues on the next page...

TSIx_GENCS field descriptions (continued)

Field	Description
	010 Electrode Oscillator Frequency divided by 4 011 Electrode Oscillator Frequency divided by 8 100 Electrode Oscillator Frequency divided by 16 101 Electrode Oscillator Frequency divided by 32 110 Electrode Oscillator Frequency divided by 64 111 Electrode Oscillator Frequency divided by 128
12–8 NSCN	NSCN These bits indicate the scan number for each electrode. The scan number is equal to NSCN + 1, which allows the scan time ranges from 1 to 32. By default, NSCN is configured as 0, which asserts the TSI scans once on the selected eletrode channel. 00000 Once per electrode 00001 Twice per electrode 00010 3 times per electrode 00011 4 times per electrode 00100 5 times per electrode 00101 6 times per electrode 00110 7 times per electrode 00111 8 times per electrode 01000 9 times per electrode 01001 10 times per electrode 01010 11 times per electrode 01011 12 times per electrode 01100 13 times per electrode 01101 14 times per electrode 01110 15 times per electrode 01111 16 times per electrode 10000 17 times per electrode 10001 18 times per electrode 10010 19 times per electrode 10011 20 times per electrode 10100 21 times per electrode 10101 22 times per electrode 10110 23 times per electrode 10111 24 times per electrode 11000 25 times per electrode 11001 26 times per electrode 11010 27 times per electrode 11011 28 times per electrode 11100 29 times per electrode 11101 30 times per electrode 11110 31 times per electrode 11111 32 times per electrode
7 TSIEN	Touch Sensing Input Module Enable This bit enables TSI module.

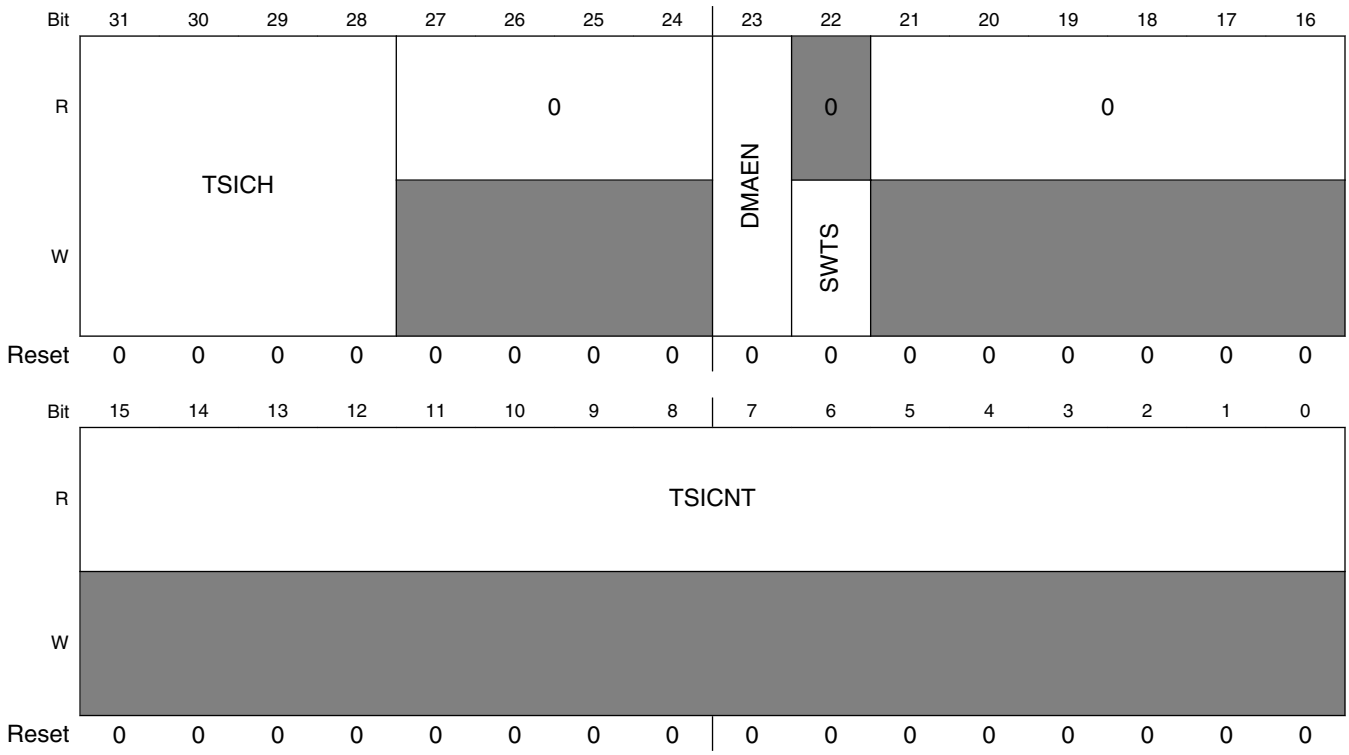
Table continues on the next page...

TSIx_GENCS field descriptions (continued)

Field	Description
	0 TSI module disabled. 1 TSI module enabled.
6 TSIIEN	Touch Sensing Input Interrupt Enable This bit enables TSI module interrupt request to CPU when the scan completes. The interrupt will wake MCU from low power mode if this interrupt is enabled. 0 TSI interrupt is disabled. 1 TSI interrupt is enabled.
5 STPE	TSI STOP Enable This bit enables TSI module function in low power modes (stop, VLPS, LLS and VLLS{3,2,1}). 0 TSI is disabled when MCU goes into low power mode. 1 Allows TSI to continue running in all low power modes.
4 STM	Scan Trigger Mode This bit specifies the trigger mode. User is allowed to change this bit when TSI is not working in progress. 0 Software trigger scan. 1 Hardware trigger scan.
3 SCNIP	Scan In Progress Status This read-only bit indicates if scan is in progress. This bit will get asserted after the analog bias circuit is stable after a trigger and it changes automatically by the TSI. 0 No scan in progress. 1 Scan in progress.
2 EOSF	End of Scan Flag This flag is set when all active electrodes are finished scanning after a scan trigger. Write "1" , when this flag is set, to clear it. 0 Scan not complete. 1 Scan complete.
1 CURSW	CURSW This bit specifies if the current sources of electrode oscillator and reference oscillator are swapped. 0 The current source pair are not swapped. 1 The current source pair are swapped.
0 EOSDMEO	End-of-Scan DMA Transfer Request Enable Only This bit makes simultaneous DMA request at End-of-Scan and Interrupt at Out-of-Range possible. EOSDMEO has precedence to ESOR when trying to set this bit and ESOR bit. When EOSDMEO = 1, End-of-Scan will generate DMA request and Out-of-Range will generate interrupt. 0 Do not enable the End-of-Scan DMA transfer request only. Depending on ESOR state, either Out-of-Range or End-of-Scan can trigger a DMA transfer request and interrupt. 1 Only the End-of-Scan event can trigger a DMA transfer request. The Out-of-Range event only and always triggers an interrupt if TSIIE is set.

63.4.2 TSI DATA Register (TSIx_DATA)

Address: 4004_5000h base + 4h offset = 4004_5004h



TSIx_DATA field descriptions

Field	Description
31–28 TSICH	TSICH These bits specify current channel to be measured. In hardware trigger mode (TSI_GENCS[STM] = 1), the scan will not start until the hardware trigger occurs. In software trigger mode (TSI_GENCS[STM] = 0), the scan starts immediately when TSI_DATA[SWTS] bit is written by 1. 0000 Channel 0. 0001 Channel 1. 0010 Channel 2. 0011 Channel 3. 0100 Channel 4. 0101 Channel 5. 0110 Channel 6. 0111 Channel 7. 1000 Channel 8. 1001 Channel 9. 1010 Channel 10. 1011 Channel 11. 1100 Channel 12. 1101 Channel 13.

Table continues on the next page...

TSIx_DATA field descriptions (continued)

Field	Description
	1110 Channel 14. 1111 Channel 15.
27–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23 DMAEN	DMA Transfer Enabled This bit is used together with the TSI interrupt enable bits(TSIIE, ESOR) to generate a DMA transfer request instead of an interrupt. 0 Interrupt is selected when the interrupt enable bit is set and the corresponding TSI events assert. 1 DMA transfer request is selected when the interrupt enable bit is set and the corresponding TSI events assert.
22 SWTS	Software Trigger Start This write-only bit is a software start trigger. When STM bit is clear, write "1" to this bit will start a scan. The electrode channel to be scanned is determinated by TSI_DATA[TSICH] bits. 0 No effect. 1 Start a scan to determine which channel is specified by TSI_DATA[TSICH].
21–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
TSICNT	TSI Conversion Counter Value These read-only bits record the accumulated scan counter value ticked by the reference oscillator.

63.4.3 TSI Threshold Register (TSIx_TSHD)

Address: 4004_5000h base + 8h offset = 4004_5008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	THRESH																THRESL															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TSIx_TSHD field descriptions

Field	Description
31–16 THRESH	TSI Wakeup Channel High-threshold This half-word specifies the high threshold of the wakeup channel.
THRESL	TSI Wakeup Channel Low-threshold This half-word specifies the low threshold of the wakeup channel.

63.5 Functional description

63.5.1 Capacitance measurement

The electrode pin capacitance measurement uses a dual oscillator approach. The frequency of the TSI electrode oscillator depends on the external electrode capacitance and the TSI module configuration. After going to a configurable prescaler, the TSI electrode oscillator signal goes to the input of the module counter. The time for the module counter to reach its module value is measured using the TSI reference oscillator. The measured electrode capacitance is directly proportional to the time.

63.5.1.1 TSI electrode oscillator

The TSI electrode oscillator circuit is illustrated in the following figure. A configurable constant current source is used to charge and discharge the external electrode capacitance. A buffer hysteresis defines the oscillator delta voltage. The delta voltage defines the margin of high and low voltage which are the reference input of the comparator in different time.

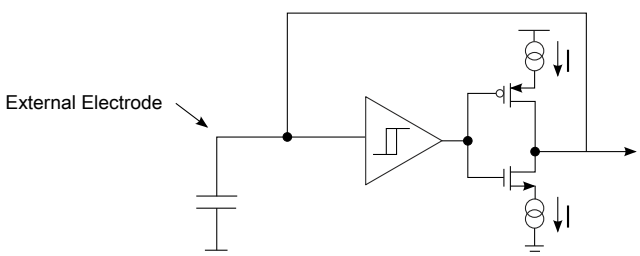


Figure 63-2. TSI electrode oscillator circuit

The current source applied to the pad capacitance is controlled by the GENCS[EXTCHRG]. The hysteresis delta voltage is defined in the module electrical specifications present in the device Data Sheet. The figure below shows the voltage amplitude waveform of the electrode capacitance charging and discharging with a programmable current.

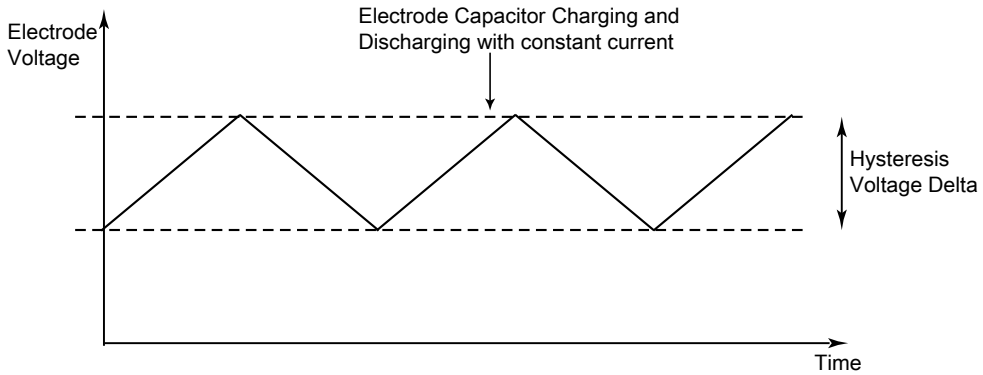


Figure 63-3. TSI electrode oscillator chart

The oscillator frequency is give by the following equation

$$F_{elec} = \frac{I}{2 * C_{elec} * \Delta V}$$

Equation 4. TSI electrode oscillator frequency

Where:

I: constant current

C_{elec}: electrode capacitance

ΔV: Hysteresis delta voltage

So by this equation, for example, an electrode with C_{elec}= 20 pF, with a current source of I = 16 µA and ΔV = 600 m V have the following oscillation frequency:

$$F_{elec} = \frac{16\ \mu A}{2 * 20pF * 600mV} = 0.67MHz$$

Equation 5. TSI electrode oscillator frequency

The current source is used to accommodate the TSI electrode oscillator frequency with different electrode capacitance sizes.

63.5.1.2 Electrode oscillator and counter module control

The TSI oscillator frequency signal goes through a prescaler defined by the GENCS[PS] and then enters in a modulus counter. GENCS[NSCN] defines the maximum count value of the modulus counter.

The pin capacitance sampling time is given by the time the module counter takes to go from 0 to its maximum value, defined by NSCN. The electrode sample time is expressed by the following equation:

$$T_{cap_samp} = \frac{PS * NSCN}{F_{elec}}$$

Using Equation 1

$$T_{cap_samp} = \frac{2 * PS * NSCN * C_{elec} * \Delta V}{I}$$

Equation 6. Electrode sampling time

Where:

PS: prescaler value

NSCN: module counter maximum value

I: constant current

C_{elec}: electrode capacitance

ΔV: Hysteresis delta voltage

By this equation we have that an electrode with C = 20 pF, with a current source of I = 16 µA and ΔV = 600 mV, PS = 2 and NSCN = 16 have the following sampling time:

$$T_{cap_samp} = \frac{2*2*16*20pF*600mV}{16\mu A} = 48\mu s$$

63.5.1.3 TSI reference oscillator

The TSI reference oscillator has the same topology of the TSI electrode oscillator. The TSI reference oscillator instead of using an external capacitor for the electrode oscillator has an internal reference capacitor.

The TSI reference oscillator has an independent programmable current source controlled by GENCS[REFCHRG].

The reference oscillator frequency is given by the following equation:

$$F_{ref_osc} = \frac{I_{ref}}{2 * C_{ref} * \Delta V}$$

Equation 7. TSI reference oscillator frequency

Where:

C_{ref}: Internal reference capacitor

I_{ref}: Reference oscillator current source

ΔV : Hysteresis delta voltage

Considering C_{ref} = 1.0 pF, I_{ref} = 12 µA and ΔV = 600 mV, follows

$$F_{ref_osc} = \frac{12\mu A}{2 * 1.0pF * 600mV} = 10.0MHz$$

63.5.2 TSI measurement result

The capacitance measurement result is defined by the number of TSI reference oscillator periods during the sample time and is stored in the TSICHnCNT register.

TSICHnCNT = T_{cap_samp} * F_{ref_osc}

Using Equation 2 and Equation 1 follows:

$$TSICHnCNT = \frac{I_{ref} * PS * NSCN}{C_{ref} * I_{elec}} * C_{elec}$$

Equation 8. Capacitance result value

In the example where F_{ref_osc} = 10.0 MHz and T_{cap_samp} = 48 µs, TSICHnCNT = 480

63.5.3 Enable TSI module

The TSI module can be fully functional in run, wait and low power modes. The TSI_GENCS[TSIEN] bit must be set to enable the TSI module in run and wait mode. When TSI_GENCS[STPE] bit is set, it allows the TSI module to work in low power mode.

63.5.4 Software and hardware trigger

The TSI module allows a software or hardware trigger to start a scan. When a software trigger is applied (TSI_GENCS[STM] bit clear), the TSI_GENCS[SWTS] bit must be written "1" to start the scan electrode channel that is identified by TSI_DATA[TSICH]. When a hardware trigger is applied (TSI_GENCS[STM] bit set), the TSI will not start scanning until the hardware trigger arrives. The hardware trigger is different depending on the MCU configuration. Generally, it could be an event that RTC overflows. See chip configuration section for details.

63.5.5 Scan times

The TSI provides multi-scan function. The number of scans is indicated by TSI_GENCS[NSCN] that allow the scan number from 1 to 32. When TSI_GENCS[NSCN] is set to 0 (only once), the single scan is engaged. The 16-bit counter accumulates all scan results until the NSCN time scan completes, and users can read TSI_DATA[TSICNT] to get this accumulation. When DMA transfer is enabled, the counter values can also be read out by DMA engine.

63.5.6 Clock setting

TSI is built with dual oscillator architecture. In normal sensing application, the reference oscillator clock is the only clock source for operations. The reference clock is used to measure the electrode oscillator by ticking a 16-bit counter. The reference oscillator frequency depends on the current source setting. Please refer to the Current source for more details.

The output of electrode oscillator has several prescalers up to 128 indicated by TSI_GENCS[PS]. This allows a flexible counter configuration for different electrode oscillator frequency.

63.5.7 Reference voltage

The TSI module offers a internal reference voltage for both electrode oscillator and reference oscillator. The internal reference voltage can work in low power modes even when the MCU regulator is partially powered down, which is ideally for low-power touch detection.

The charge and discharge difference voltage is configurable upon the setting of TSI_GENCS[DVOLT]. The following table shows the all the delta voltage configurations.

NOTE

Table 63-4. Delta voltage configuration

DVOLT	V_p (V)	V_m (V)	ΔV (V)
00	1.328	0.302	1.026
01	1.111	0.519	0.592
10	0.986	0.644	0.342
11	0.914	0.716	0.198

63.5.8 Current source

The TSI module supports eight different current source power to increment from 500 nA to 64 µA. TSI_GENCS[EXTCHRG] determines the current of electrode oscillator that charges and discharges external electrodes. The TSI_GENCS[REFCHRG] determines the current of reference oscillator on which the internal reference clock depends. The lower current source takes more time for charge and discharge, which is useful to detect high-accuracy change. The higher current source takes less time, which can be used to charge a big electrode by less power consumption.

TSI_GENCS[CURSW] allows the current source to swap, so that the reference oscillator and electrode oscillator use the opposite current sources. When TSI_GENCS[CURSW] is set and the current sources are swapped, TSI_GENCS[EXTCHRG] and TSI_GENCS[REFCHRG] still control the corresponding current sources, that is, TSI_GENCS[EXTCHRG] controls the reference oscillator current and TSI_GENCS[REFCHRG] controls the electrode oscillator current.

63.5.9 End of scan

As a scan starts, [SCNIP] bit is set to indicate scan is in progress. When the scan completes, the [EOSF] bit is set. Before clearing the [EOSF] bit, the value in TSI_DATA[TSICNT] must be read. If the TSI_GENCS[TSIIEN] and TSI_GENCS[ESOR] are set andTSI_GENCS[DMAEN]is not set, an interrupt is submitted to CPU for post-processing immediately. The interrupt is also optional to wake MCU to execute ISR if it is in low power mode. When DMA function is enabled by setting TSI_GENCS[TSIIEN] and TSI_GENCS[ESOR], as soon as scan completes, a DMA transfer request is asserted to DMA controller for data movement, generally, DMA engine will fetch TSI conversion result from TSI_DATA register,store it to other memory space and then refresh the TSI scan channel index(TSI_DATA[TSICH]) for next loop. When DMA transfer is done, TSI_GENCS[EOSF] is cleared automatically.

63.5.10 Out-of-range interrupt

If enabled, TSI will scan the electrode specified by TSI_DATA[TSICH] as soon as the trigger arrives. The TSI_GENCS[OUTRGF] flag generates a TSI interrupt request if the TSI_GENCS[TSIIE] bit is set and GENCS[ESOR] bit is cleared. With this configuration, after the end-of-electrode scan, the electrode capacitance will be converted and stored to the result register TSI_DATA[TSICNT], the out-of-range interrupt is only requested if

there is a considerable capacitance change defined by the TSI_TSHD. For instance, if in low power mode the electrode capacitance does not vary, the out-of-range interrupt does not interrupt the CPU. This interrupt will not happen in noise detection mode. It is worthy to note that when the counter value reaches 0xFFFF is treated as an extreme case the out-of-range will not happen. Also in noise detection mode, the out-of-range will not assert either.

63.5.11 Wake up MCU from low power modes

In low power modes, once enabled by TSI_GENCS[STPE] and TSI_GENCS[TSIIE], TSI can bring MCU out of its low power modes(STOP, VLPS, VLLS,etc) by either end of scan or out of range interrupt, that is, if TSI_GENCS[ESOR] is set, end of scan interrupt is selected and otherwise, out of range is selected.

63.5.12 DMA function support

Transmit by DMA is supported only when TSI_DATA[DMAEN] is set. A DMA transfer request is asserted when all the flags based on TSI_GENCS[ESOR] settings and TSI_GENCS[TSIIE] are set. Then the on-chip DMA controller detects this request and transfers data between memory space and TSI register space. After the data tranfer, DMA DONE is asserted to clear TSI_GENCS[EOSF] automatically. This function is normally used by DMA controller to get the conversion result from TSI_DATA[TSICNT] upon a end-of-scan event and then refresh the channel index(TSI_DATA[TSICH]) for next trigger.

Chapter 64
General-Purpose Input/Output (GPIO)

64.1 Chip-specific GPIO information

64.1.1 GPIO access protection

The GPIO module does not have access protection because it is not connected to a peripheral bridge slot and is not protected by the MPU.

64.1.2 Number of GPIO signals

The number of GPIO signals available on the devices covered by this document are detailed in Orderable part numbers.

Eight GPIO pins support a high drive capability - PTB0, PTB1, PTD4, PTD5, PTD6, PTD7, PTC3, and PTC4. All other GPIO support normal drive option only.

PTA4 includes a passive input filter that is enabled or disabled by PORTA_PCR4[PFE] control. This reset default is to have this function disabled.

64.2 Introduction

The general-purpose input and output (GPIO) module is accessible via the peripheral bus. The GPIO registers support 8-bit, 16-bit or 32-bit accesses.

The GPIO data direction and output data registers control the direction and output data of each pin when the pin is configured for the GPIO function. The GPIO input data register displays the logic value on each pin when the pin is configured for any digital function, provided the corresponding Port Control and Interrupt module for that pin is enabled.

Efficient bit manipulation of the general-purpose outputs is supported through the addition of set, clear, and toggle write-only registers for each port output data register.

64.2.1 Features

Features of the GPIO module include:

- Port Data Input register visible in all digital pin-multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register

NOTE

The GPIO module is clocked by system clock.

64.2.2 Modes of operation

The following table depicts different modes of operation and the behavior of the GPIO module in these modes.

Table 64-1. Modes of operation

Modes of operation	Description
Run	The GPIO module operates normally.
Wait	The GPIO module operates normally.
Stop	The GPIO module is disabled.
Debug	The GPIO module operates normally.

64.2.3 GPIO signal descriptions

Table 64-2. GPIO signal descriptions

GPIO signal descriptions	Description	I/O
PORTA31–PORTA0	General-purpose input/output	I/O
PORTB31–PORTB0	General-purpose input/output	I/O
PORTC31–PORTC0	General-purpose input/output	I/O
PORTD31–PORTD0	General-purpose input/output	I/O
PORTE31–PORTE0	General-purpose input/output	I/O

NOTE

Not all pins within each port are implemented on each device. See the chapter on signal multiplexing for the number of GPIO ports available in the device.

64.2.3.1 Detailed signal description

Table 64-3. GPIO interface-detailed signal descriptions

Signal	I/O	Description	
PORTA31–PORTA0 PORTB31–PORTB0 PORTC31–PORTC0 PORTD31–PORTD0 PORTE31–PORTE0	I/O	General-purpose input/output	
		State meaning	Asserted: The pin is logic 1. Deasserted: The pin is logic 0.
		Timing	Assertion: When output, this signal occurs on the rising-edge of the system clock. For input, it may occur at any time and input may be asserted asynchronously to the system clock. Deassertion: When output, this signal occurs on the rising-edge of the system clock. For input, it may occur at any time and input may be asserted asynchronously to the system clock.

NOTE

Not all pins within each port are implemented on each device. See the chapter on signal multiplexing for the number of GPIO ports available in the device.

64.3 Memory map and register definition

Any read or write access to the GPIO memory space that is outside the valid memory map results in a bus error.

GPIO memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400F_F000	Port Data Output Register (GPIOA_PDOR)	32	R/W	0000_0000h	64.3.1/2183
400F_F004	Port Set Output Register (GPIOA_PSOR)	32	W (always reads 0)	0000_0000h	64.3.2/2184
400F_F008	Port Clear Output Register (GPIOA_PCOR)	32	W (always reads 0)	0000_0000h	64.3.3/2184

Table continues on the next page...

GPIO memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400F_F00C	Port Toggle Output Register (GPIOA_PTOR)	32	W (always reads 0)	0000_0000h	64.3.4/2185
400F_F010	Port Data Input Register (GPIOA_PDIR)	32	R	0000_0000h	64.3.5/2185
400F_F014	Port Data Direction Register (GPIOA_PDDR)	32	R/W	0000_0000h	64.3.6/2186
400F_F040	Port Data Output Register (GPIOB_PDOR)	32	R/W	0000_0000h	64.3.1/2183
400F_F044	Port Set Output Register (GPIOB_PSOR)	32	W (always reads 0)	0000_0000h	64.3.2/2184
400F_F048	Port Clear Output Register (GPIOB_PCOR)	32	W (always reads 0)	0000_0000h	64.3.3/2184
400F_F04C	Port Toggle Output Register (GPIOB_PTOR)	32	W (always reads 0)	0000_0000h	64.3.4/2185
400F_F050	Port Data Input Register (GPIOB_PDIR)	32	R	0000_0000h	64.3.5/2185
400F_F054	Port Data Direction Register (GPIOB_PDDR)	32	R/W	0000_0000h	64.3.6/2186
400F_F080	Port Data Output Register (GPIOC_PDOR)	32	R/W	0000_0000h	64.3.1/2183
400F_F084	Port Set Output Register (GPIOC_PSOR)	32	W (always reads 0)	0000_0000h	64.3.2/2184
400F_F088	Port Clear Output Register (GPIOC_PCOR)	32	W (always reads 0)	0000_0000h	64.3.3/2184
400F_F08C	Port Toggle Output Register (GPIOC_PTOR)	32	W (always reads 0)	0000_0000h	64.3.4/2185
400F_F090	Port Data Input Register (GPIOC_PDIR)	32	R	0000_0000h	64.3.5/2185
400F_F094	Port Data Direction Register (GPIOC_PDDR)	32	R/W	0000_0000h	64.3.6/2186
400F_F0C0	Port Data Output Register (GPIOD_PDOR)	32	R/W	0000_0000h	64.3.1/2183
400F_F0C4	Port Set Output Register (GPIOD_PSOR)	32	W (always reads 0)	0000_0000h	64.3.2/2184
400F_F0C8	Port Clear Output Register (GPIOD_PCOR)	32	W (always reads 0)	0000_0000h	64.3.3/2184
400F_F0CC	Port Toggle Output Register (GPIOD_PTOR)	32	W (always reads 0)	0000_0000h	64.3.4/2185
400F_F0D0	Port Data Input Register (GPIOD_PDIR)	32	R	0000_0000h	64.3.5/2185
400F_F0D4	Port Data Direction Register (GPIOD_PDDR)	32	R/W	0000_0000h	64.3.6/2186
400F_F100	Port Data Output Register (GPIOE_PDOR)	32	R/W	0000_0000h	64.3.1/2183

Table continues on the next page...

GPIO memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400F_F104	Port Set Output Register (GPIOE_PSOR)	32	W (always reads 0)	0000_0000h	64.3.2/2184
400F_F108	Port Clear Output Register (GPIOE_PCOR)	32	W (always reads 0)	0000_0000h	64.3.3/2184
400F_F10C	Port Toggle Output Register (GPIOE_PTOR)	32	W (always reads 0)	0000_0000h	64.3.4/2185
400F_F110	Port Data Input Register (GPIOE_PDIR)	32	R	0000_0000h	64.3.5/2185
400F_F114	Port Data Direction Register (GPIOE_PDDR)	32	R/W	0000_0000h	64.3.6/2186

64.3.1 Port Data Output Register (GPIOx_PDOR)

This register configures the logic levels that are driven on each general-purpose output pins.

NOTE

Do not modify pin configuration registers associated with pins not available in your selected package. All unbonded pins not available in your package will default to DISABLE state for lowest power consumption.

Address: Base address + 0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PDO																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

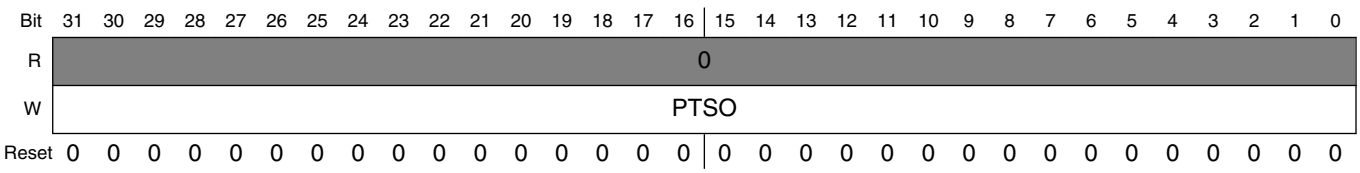
GPIOx_PDOR field descriptions

Field	Description
PDO	Port Data Output Register bits for unbonded pins return a undefined value when read. 0 Logic level 0 is driven on pin, provided pin is configured for general-purpose output. 1 Logic level 1 is driven on pin, provided pin is configured for general-purpose output.

64.3.2 Port Set Output Register (GPIOx_PSOR)

This register configures whether to set the fields of the PDOR.

Address: Base address + 4h offset



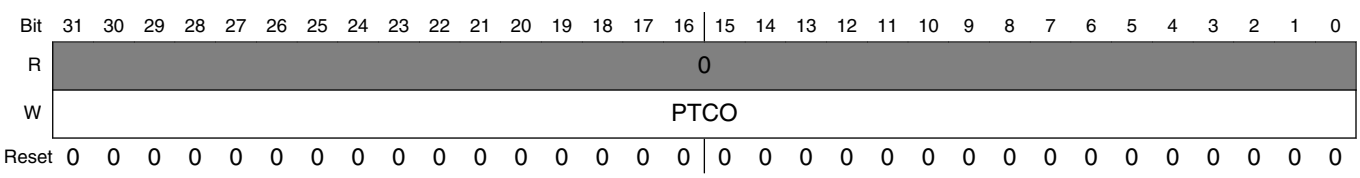
GPIOx_PSOR field descriptions

Field	Description
PTSO	Port Set Output Writing to this register will update the contents of the corresponding bit in the PDOR as follows: 0 Corresponding bit in PDORn does not change. 1 Corresponding bit in PDORn is set to logic 1.

64.3.3 Port Clear Output Register (GPIOx_PCOR)

This register configures whether to clear the fields of PDOR.

Address: Base address + 8h offset



GPIOx_PCOR field descriptions

Field	Description
PTCO	Port Clear Output Writing to this register will update the contents of the corresponding bit in the Port Data Output Register (PDOR) as follows: 0 Corresponding bit in PDORn does not change. 1 Corresponding bit in PDORn is cleared to logic 0.

64.3.4 Port Toggle Output Register (GPIOx_PTOR)

Address: Base address + Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W	PTTO																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_PTOR field descriptions

Field	Description
PTTO	Port Toggle Output Writing to this register will update the contents of the corresponding bit in the PDOR as follows: 0 Corresponding bit in PDORn does not change. 1 Corresponding bit in PDORn is set to the inverse of its existing logic state.

64.3.5 Port Data Input Register (GPIOx_PDIR)

NOTE

Do not modify pin configuration registers associated with pins not available in your selected package. All unbonded pins not available in your package will default to DISABLE state for lowest power consumption.

Address: Base address + 10h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PDI																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_PDIR field descriptions

Field	Description
PDI	Port Data Input Reads 0 at the unimplemented pins for a particular device. Pins that are not configured for a digital function read 0. If the Port Control and Interrupt module is disabled, then the corresponding bit in PDIR does not update. 0 Pin logic level is logic 0, or is not configured for use by digital function. 1 Pin logic level is logic 1.

64.3.6 Port Data Direction Register (GPIOx_PDDR)

The PDDR configures the individual port pins for input or output.

Address: Base address + 14h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PDD																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_PDDR field descriptions

Field	Description
PDD	Port Data Direction Configures individual port pins for input or output. 0 Pin is configured as general-purpose input, for the GPIO function. 1 Pin is configured as general-purpose output, for the GPIO function.

64.4 Functional description

64.4.1 General-purpose input

The logic state of each pin is available via the Port Data Input registers, provided the pin is configured for a digital function and the corresponding Port Control and Interrupt module is enabled.

The Port Data Input registers return the synchronized pin state after any enabled digital filter in the Port Control and Interrupt module. The input pin synchronizers are shared with the Port Control and Interrupt module, so that if the corresponding Port Control and Interrupt module is disabled, then synchronizers are also disabled. This reduces power consumption when a port is not required for general-purpose input functionality.

64.4.2 General-purpose output

The logic state of each pin can be controlled via the port data output registers and port data direction registers, provided the pin is configured for the GPIO function. The following table depicts the conditions for a pin to be configured as input/output.

If	Then

Table continues on the next page...

A pin is configured for the GPIO function and the corresponding port data direction register bit is clear.	The pin is configured as an input.
A pin is configured for the GPIO function and the corresponding port data direction register bit is set.	The pin is configured as an output and and the logic state of the pin is equal to the corresponding port data output register.

To facilitate efficient bit manipulation on the general-purpose outputs, pin data set, pin data clear, and pin data toggle registers exist to allow one or more outputs within one port to be set, cleared, or toggled from a single register write.

The corresponding Port Control and Interrupt module does not need to be enabled to update the state of the port data direction registers and port data output registers including the set/clear/toggle registers.

Chapter 65
JTAG Controller (JTAGC)

65.1 Introduction

The JTAGC block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format.

65.1.1 Block diagram

The following is a simplified block diagram of the JTAG Controller (JTAGC) block. Refer to the chip-specific configuration information as well as Register description for more information about the JTAGC registers.

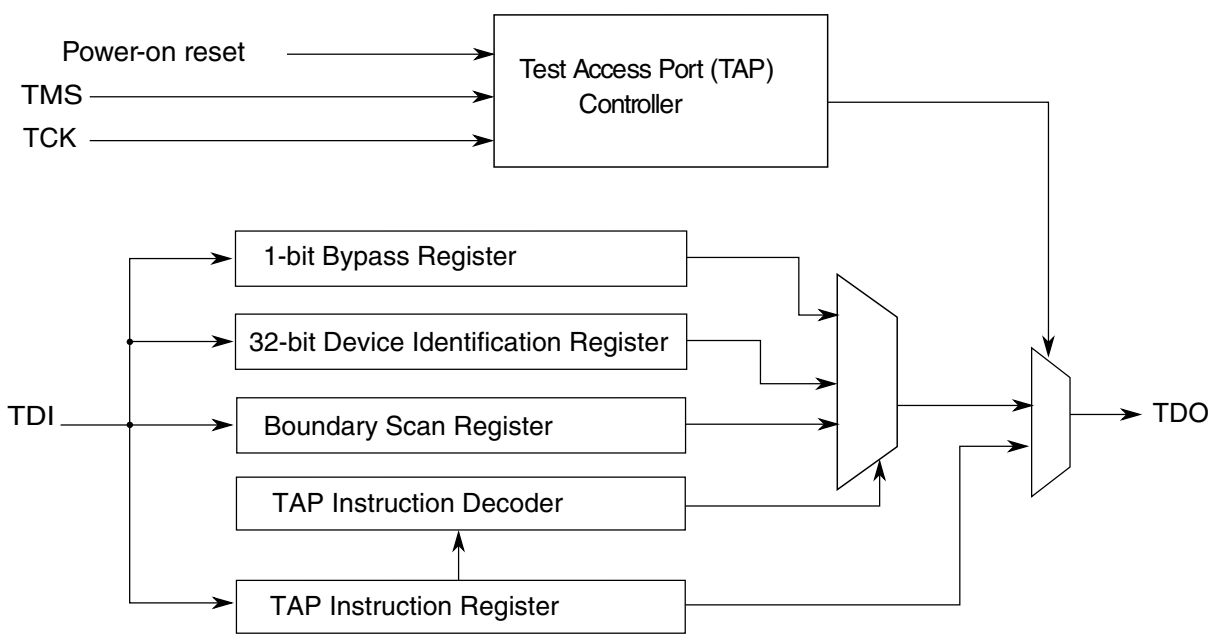


Figure 65-1. JTAG (IEEE 1149.1) block diagram

65.1.2 Features

The JTAGC block is compliant with the IEEE 1149.1-2001 standard, and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface
  - 4 pins (TDI, TMS, TCK, and TDO)
- Instruction register that supports several IEEE 1149.1-2001 defined instructions as well as several public and private device-specific instructions. Refer to Table 65-3 for a list of supported instructions.
- Bypass register, boundary scan register, and device identification register.
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

65.1.3 Modes of operation

The JTAGC block uses a power-on reset indication as its primary reset signals. Several IEEE 1149.1-2001 defined test modes are supported, as well as a bypass mode.

65.1.3.1 Reset

The JTAGC block is placed in reset when either power-on reset is asserted, or the TMS input is held high for enough consecutive rising edges of TCK to sequence the TAP controller state machine into the Test-Logic-Reset state. Holding TMS high for five consecutive rising edges of TCK guarantees entry into the Test-Logic-Reset state regardless of the current TAP controller state. Asserting power-on reset results in asynchronous entry into the reset state. While in reset, the following actions occur:

- The TAP controller is forced into the Test-Logic-Reset state, thereby disabling the test logic and allowing normal operation of the on-chip system logic to continue unhindered
- The instruction register is loaded with the IDCODE instruction

65.1.3.2 IEEE 1149.1-2001 defined test modes

The JTAGC block supports several IEEE 1149.1-2001 defined test modes. A test mode is selected by loading the appropriate instruction into the instruction register while the JTAGC is enabled. Supported test instructions include EXTEST, HIGHZ, CLAMP, SAMPLE and SAMPLE/PRELOAD. Each instruction defines the set of data register(s) that may operate and interact with the on-chip system logic while the instruction is current. Only one test data register path is enabled to shift data between TDI and TDO for each instruction.

The boundary scan register is enabled for serial access between TDI and TDO when the EXTEST, SAMPLE or SAMPLE/PRELOAD instructions are active. The single-bit bypass register shift stage is enabled for serial access between TDI and TDO when the BYPASS, HIGHZ, CLAMP or reserved instructions are active. The functionality of each test mode is explained in more detail in JTAGC block instructions.

65.1.3.3 Bypass mode

When no test operation is required, the BYPASS instruction can be loaded to place the JTAGC block into bypass mode. While in bypass mode, the single-bit bypass shift register is used to provide a minimum-length serial path to shift data between TDI and TDO.

65.2 External signal description

The JTAGC consists of a set of signals that connect to off chip development tools and allow access to test support functions. The JTAGC signals are outlined in the following table and described in the following sections.

Table 65-1. JTAG signal properties

Name	I/O	Function	Reset State	Pull
TCK	Input	Test Clock	—	Down
TDI	Input	Test Data In	—	Up
TDO	Output	Test Data Out	High Z[1]	—
TMS	Input	Test Mode Select	—	Up

1. TDO output buffer enable is negated when the JTAGC is not in the Shift-IR or Shift-DR states. A weak pull may be implemented at the TDO pad for use when JTAGC is inactive.

65.2.1 TCK—Test clock input

Test Clock Input (TCK) is an input pin used to synchronize the test logic and control register access through the TAP.

65.2.2 TDI—Test data input

Test Data Input (TDI) is an input pin that receives serial test instructions and data. TDI is sampled on the rising edge of TCK.

65.2.3 TDO—Test data output

Test Data Output (TDO) is an output pin that transmits serial output for test instructions and data. TDO is three-stateable and is actively driven only in the Shift-IR and Shift-DR states of the TAP controller state machine, which is described in TAP controller state machine.

65.2.4 TMS—Test mode select

Test Mode Select (TMS) is an input pin used to sequence the IEEE 1149.1-2001 test control state machine. TMS is sampled on the rising edge of TCK.

65.3 Register description

This section provides a detailed description of the JTAGC block registers accessible through the TAP interface, including data registers and the instruction register. Individual bit-level descriptions and reset states of each register are included. These registers are not memory-mapped and can only be accessed through the TAP.

65.3.1 Instruction register

The JTAGC block uses a 4-bit instruction register as shown in the following figure. The instruction register allows instructions to be loaded into the block to select the test to be performed or the test data register to be accessed or both. Instructions are shifted in through TDI while the TAP controller is in the Shift-IR state, and latched on the falling edge of TCK in the Update-IR state. The latched instruction value can only be changed in the Update-IR and Test-Logic-Reset TAP controller states. Synchronous entry into the

Test-Logic-Reset state results in the IDCODE instruction being loaded on the falling edge of TCK. Asynchronous entry into the Test-Logic-Reset state results in asynchronous loading of the IDCODE instruction. During the Capture-IR TAP controller state, the instruction shift register is loaded with the value 0001b , making this value the register's read value when the TAP controller is sequenced into the Shift-IR state.

	3	2	1	0
R	0	0	0	1
W	Instruction Code			
Reset:	0	0	0	1

Figure 65-2. Instruction register

65.3.2 Bypass register

The bypass register is a single-bit shift register path selected for serial data transfer between TDI and TDO when the BYPASS, CLAMP, HIGHZ or reserve instructions are active. After entry into the Capture-DR state, the single-bit shift register is set to a logic 0. Therefore, the first bit shifted out after selecting the bypass register is always a logic 0.

65.3.3 Device identification register

The device identification (JTAG ID) register, shown in the following figure, allows the revision number, part number, manufacturer, and design center responsible for the design of the part to be determined through the TAP. The device identification register is selected for serial data transfer between TDI and TDO when the IDCODE instruction is active. Entry into the Capture-DR state while the device identification register is selected loads the IDCODE into the shift register to be shifted out on TDO in the Shift-DR state. No action occurs in the Update-DR state.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Part Revision Number				Design Center						Part Identification Number					
W																
Reset	PRN				DC						PIN					

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Part Identification Number				Manufacturer Identity Code											1
W																
Reset	PIN (contd.)				MIC											1

The following table describes the device identification register functions.

Table 65-2. Device identification register field descriptions

Field	Description
PRN	Part Revision Number. Contains the revision number of the part. Value is 0x0.
DC	Design Center. Indicates the design center. Value is 0x2C.
PIN	Part Identification Number. Contains the part number of the device. On this device, the PIN mirrors bits 9-0 of the SIM_SDID register. Please see the SIM_SDID register description for more detail.
MIC	Manufacturer Identity Code. Contains the reduced Joint Electron Device Engineering Council (JEDEC) ID. Value is 0x00E.
IDCODE ID	IDCODE Register ID. Identifies this register as the device identification register and not the bypass register. Always set to 1.

65.3.4 Boundary scan register

The boundary scan register is connected between TDI and TDO when the EXTEST, SAMPLE or SAMPLE/PRELOAD instructions are active. It is used to capture input pin data, force fixed values on output pins, and select a logic value and direction for bidirectional pins. Each bit of the boundary scan register represents a separate boundary scan register cell, as described in the IEEE 1149.1-2001 standard and discussed in Boundary scan. The size of the boundary scan register and bit ordering is device-dependent and can be found in the device BSDL file.

65.4 Functional description

This section explains the JTAGC functional description.

65.4.1 JTAGC reset configuration

While in reset, the TAP controller is forced into the Test-Logic-Reset state, thus disabling the test logic and allowing normal operation of the on-chip system logic. In addition, the instruction register is loaded with the IDCODE instruction.

65.4.2 IEEE 1149.1-2001 (JTAG) Test Access Port

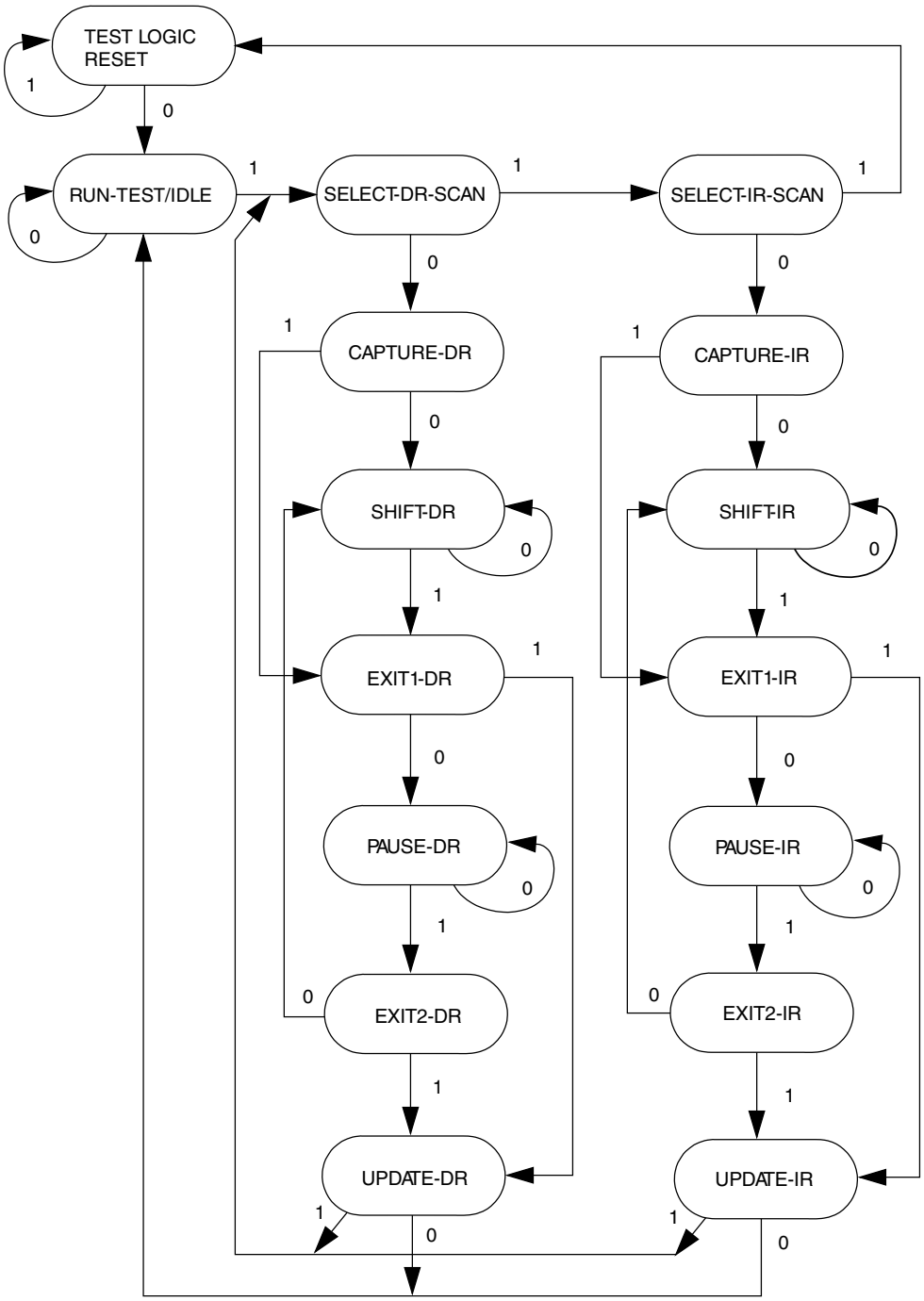
The JTAGC block uses the IEEE 1149.1-2001 TAP for accessing registers. This port can be shared with other TAP controllers on the MCU. Ownership of the port is determined by the value of the currently loaded instruction.

Data is shifted between TDI and TDO though the selected register starting with the least significant bit, as illustrated in the following figure. This applies for the instruction register, test data registers, and the bypass register.

Figure 65-3. Shifting data through a register

65.4.3 TAP controller state machine

The TAP controller is a synchronous state machine that interprets the sequence of logical values on the TMS pin. The following figure shows the machine's states. The value shown next to each state is the value of the TMS signal sampled on the rising edge of the TCK signal. As the following figure shows, holding TMS at logic 1 while clocking TCK through a sufficient number of rising edges also causes the state machine to enter the Test-Logic-Reset state.



The value shown adjacent to each state transition in this figure represents the value of TMS at the time of a rising edge of TCK.

Figure 65-4. IEEE 1149.1-2001 TAP controller finite state machine

65.4.3.1 Enabling the TAP controller

The JTAGC TAP controller is enabled by setting the JTAGC enable to a logic 1 value.

65.4.3.2 Selecting an IEEE 1149.1-2001 register

Access to the JTAGC data registers is achieved by loading the instruction register with any of the JTAGC block instructions while the JTAGC is enabled. Instructions are shifted in via the Select-IR-Scan path and loaded in the Update-IR state. At this point, all data register access is performed via the Select-DR-Scan path.

The Select-DR-Scan path is used to read or write the register data by shifting in the data (LSB first) during the Shift-DR state. When reading a register, the register value is loaded into the IEEE 1149.1-2001 shifter during the Capture-DR state. When writing a register, the value is loaded from the IEEE 1149.1-2001 shifter to the register during the Update-DR state. When reading a register, there is no requirement to shift out the entire register contents. Shifting may be terminated once the required number of bits have been acquired.

65.4.4 JTAGC block instructions

The JTAGC block implements the IEEE 1149.1-2001 defined instructions listed in the following table. This section gives an overview of each instruction; refer to the IEEE 1149.1-2001 standard for more details. All undefined opcodes are reserved.

Table 65-3. 4-bit JTAG instructions

Instruction	Code[3:0]	Instruction summary
IDCODE	0000	Selects device identification register for shift
SAMPLE/PRELOAD	0010	Selects boundary scan register for shifting, sampling, and preloading without disturbing functional operation
SAMPLE	0011	Selects boundary scan register for shifting and sampling without disturbing functional operation
EXTEST	0100	Selects boundary scan register and applies preloaded values to output pins. **NOTE:** Execution of this instruction asserts functional reset.
Factory debug reserved	0101	Intended for factory debug only
Factory debug reserved	0110	Intended for factory debug only
Factory debug reserved	0111	Intended for factory debug only
ARM JTAG-DP Reserved	1000	This instruction goes the ARM JTAG-DP controller. See the ARM JTAG-DP documentation for more information.
HIGHZ	1001	Selects bypass register and three-states all output pins. **NOTE:** Execution of this instruction asserts functional reset.
ARM JTAG-DP Reserved	1010	This instruction goes the ARM JTAG-DP controller. See the ARM JTAG-DP documentation for more information.

Table continues on the next page...

Table 65-3. 4-bit JTAG instructions (continued)

Instruction	Code[3:0]	Instruction summary
ARM JTAG-DP Reserved	1011	This instruction goes the ARM JTAG-DP controller. See the ARM JTAG-DP documentation for more information.
CLAMP	1100	Selects bypass register and applies preloaded values to output pins. **NOTE:** Execution of this instruction asserts functional reset.
ARM JTAG-DP Reserved	1110	This instruction goes the ARM JTAG-DP controller. See the ARM JTAG-DP documentation for more information.
BYPASS	1111	Selects bypass register for data operations

65.4.4.1 IDCODE instruction

IDCODE selects the 32-bit device identification register as the shift path between TDI and TDO. This instruction allows interrogation of the MCU to determine its version number and other part identification data. IDCODE is the instruction placed into the instruction register when the JTAGC block is reset.

65.4.4.2 SAMPLE/PRELOAD instruction

The SAMPLE/PRELOAD instruction has two functions:

- The SAMPLE portion of the instruction obtains a sample of the system data and control signals present at the MCU input pins and just before the boundary scan register cells at the output pins. This sampling occurs on the rising edge of TCK in the Capture-DR state when the SAMPLE/PRELOAD instruction is active. The sampled data is viewed by shifting it through the boundary scan register to the TDO output during the Shift-DR state. Both the data capture and the shift operation are transparent to system operation.
- The PRELOAD portion of the instruction initializes the boundary scan register cells before selecting the EXTEST or CLAMP instructions to perform boundary scan tests. This is achieved by shifting in initialization data to the boundary scan register during the Shift-DR state. The initialization data is transferred to the parallel outputs of the boundary scan register cells on the falling edge of TCK in the Update-DR state. The data is applied to the external output pins by the EXTEST or CLAMP instruction. System operation is not affected.

65.4.4.3 SAMPLE instruction

The SAMPLE instruction obtains a sample of the system data and control signals present at the MCU input pins and just before the boundary scan register cells at the output pins. This sampling occurs on the rising edge of TCK in the Capture-DR state when the SAMPLE instruction is active. The sampled data is viewed by shifting it through the boundary scan register to the TDO output during the Shift-DR state. There is no defined action in the Update-DR state. Both the data capture and the shift operation are transparent to system operation.

65.4.4.4 EXTEST External test instruction

EXTEST selects the boundary scan register as the shift path between TDI and TDO. It allows testing of off-chip circuitry and board-level interconnections by driving preloaded data contained in the boundary scan register onto the system output pins. Typically, the preloaded data is loaded into the boundary scan register using the SAMPLE/PRELOAD instruction before the selection of EXTEST. EXTEST asserts the internal system reset for the MCU to force a predictable internal state while performing external boundary scan operations.

65.4.4.5 HIGHZ instruction

HIGHZ selects the bypass register as the shift path between TDI and TDO. While HIGHZ is active all output drivers are placed in an inactive drive state (e.g., high impedance). HIGHZ also asserts the internal system reset for the MCU to force a predictable internal state.

65.4.4.6 CLAMP instruction

CLAMP allows the state of signals driven from MCU pins to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. CLAMP enhances test efficiency by reducing the overall shift path to a single bit (the bypass register) while conducting an EXTEST type of instruction through the boundary scan register. CLAMP also asserts the internal system reset for the MCU to force a predictable internal state.

65.4.4.7 BYPASS instruction

BYPASS selects the bypass register, creating a single-bit shift register path between TDI and TDO. BYPASS enhances test efficiency by reducing the overall shift path when no test operation of the MCU is required. This allows more rapid movement of test data to and from other components on a board that are required to perform test functions. While the BYPASS instruction is active the system logic operates normally.

65.4.5 Boundary scan

The boundary scan technique allows signals at component boundaries to be controlled and observed through the shift-register stage associated with each pad. Each stage is part of a larger boundary scan register cell, and cells for each pad are interconnected serially to form a shift-register chain around the border of the design. The boundary scan register consists of this shift-register chain, and is connected between TDI and TDO when the EXTEST, SAMPLE, or SAMPLE/PRELOAD instructions are loaded. The shift-register chain contains a serial input and serial output, as well as clock and control signals.

65.5 Initialization/Application information

The test logic is a static logic design, and TCK can be stopped in either a high or low state without loss of data. However, the system clock is not synchronized to TCK internally. Any mixed operation using both the test logic and the system functional logic requires external synchronization.

To initialize the JTAGC block and enable access to registers, the following sequence is required:

1. Place the JTAGC in reset through TAP controller state machine transitions controlled by TMS.
2. Load the appropriate instruction for the test or action to be performed.

Chapter 66
Release Notes for Revision 2

66.1 General changes throughout document

- Updated Table 8-1 Kinetis Bootloader Peripheral Pinmux to include all peripherals supported by the device.

66.2 About This Document chapter changes

- No substantial content changes

66.3 Introduction chapter changes

- No substantial content changes

66.4 Core Overview chapter changes

- No substantial content changes

66.5 Memories and Memory Interfaces changes

- No substantial content changes

66.6 Memory Map chapter changes

- Updated the note in the 'System memory map' table as follows: Debug access is available only in the aliased QuadSPI memory region. (Breakpoints are not supported in the main QuadSPI memory region.)

66.7 Clock Distribution chapter changes

- No substantial content changes

66.8 Reset and Boot chapter changes

- No substantial content changes

66.9 Kinetis ROM Bootloader changes

- No substantial content changes

66.10 Power Management chapter changes

- No substantial content changes

66.11 Security chapter changes

- No substantial content changes

66.12 Debug chapter changes

- No substantial content changes

66.13 Signal Multiplexing and Signal Descriptions chapter changes

- No substantial content changes

66.14 PORT changes

- No substantial content changes

66.15 SIM changes

- No substantial content changes

66.16 EMVSIM changes

No substantial content changes

66.17 RCM changes

- No substantial content changes

66.18 SMC changes

- No substantial content changes

66.19 PMC changes

- No substantial content changes

66.20 LLWU changes

- No substantial content changes

66.21 MCM changes

- No substantial content changes

66.22 Crossbar switch module changes

- No substantial content changes

66.23 AIPS module changes

- No substantial content changes

66.24 MPU module changes

66.24.1 MPU chip-specific changes

- No substantial content changes

66.24.2 MPU module changes

- No substantial content changes

66.25 BME configuration changes

- No substantial content changes

66.26 DMAMUX module changes

66.26.1 DMAMUX chip-specific changes

- No substantial content changes

66.26.2 DMAMUX module changes

- No substantial content changes

66.27 eDMA module changes

- No substantial content changes

66.28 EWM changes

- No substantial content changes

66.29 WDOG changes

- No substantial content changes

66.30 MCG changes

- No substantial content changes

66.31 OSC changes

- No substantial content changes

66.32 RTC Oscillator changes

- No substantial content changes

66.33 LMEM changes

- No substantial content changes

66.34 FMC changes

- No substantial content changes

66.35 FTFA changes

- No substantial content changes

66.36 SDRAM Controller changes

- No substantial content changes

66.37 QuadSPI changes

66.37.1 QuadSPI chip-specific changes

- No substantial content changes

66.37.2 QuadSPI changes

- No substantial content changes

66.38 OTFAD changes

In sections "CTR-AES128 mode basics" and "Context determination", added clarification that the OTFAD module "sees" only the *physical* address space assigned to the QuadSPI module, not the aliased area.

66.39 FlexBus changes

• No substantial content changes

66.40 CRC changes

• No substantial content changes

66.41 CAU changes

• No substantial content changes

66.42 TRNG module changes

• No substantial content changes

66.43 LTC module changes

• No substantial content changes

66.44 ADC changes

• No substantial content changes

66.45 CMP changes

- No substantial content changes

66.46 VREF changes

- No substantial content changes

66.47 DAC changes

- No substantial content changes

66.48 FTM changes

- No substantial content changes

66.49 TPM changes (showing internal content)

66.49.1 TPM chip-specific changes

- No substantial content changes

66.49.2 TPM changes

- No substantial content changes

66.50 LPTMR changes

- No substantial content changes

66.51 CMT changes

- No substantial content changes

66.52 PDB changes (showing internal content)

66.52.1 PDB chip-specific changes

- No substantial content changes

66.52.2 PDB changes

- No substantial content changes

66.53 PIT module changes

- No substantial content changes

66.54 RTC changes

- No substantial content changes

66.55 USB full speed OTG controller changes

- No substantial content changes

66.56 USBDCD changes

- No substantial content changes

66.57 USB VREG changes

- No substantial content changes

66.58 SPI module changes

- No substantial content changes

66.59 I2C changes

- No substantial content changes

66.60 LPUART changes

- No substantial content changes

66.61 FlexIO changes (showing internal content)

66.61.1 FlexIO chip-specific changes

- No substantial content changes

66.61.2 FlexIO changes

No substantial content changes

66.62 I2S/SAI changes

- No substantial content changes

66.63 SDHC changes

- No substantial content changes

66.64 Touch sense input chapter changes

- No substantial content changes

66.65 GPIO changes

- No substantial content changes

66.66 JTAGC module changes

- No substantial content changes

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