

## SKEA8P44M48SF0

### KEA8 Sub-Family Data Sheet

Supports the following:  
SKEAZN8AMTG(R) and  
SKEAZN8AMFK(R)

#### Key features

- Operating characteristics
  - Voltage range: 2.7 to 5.5 V
  - Flash write voltage range: 2.7 to 5.5 V
  - Temperature range (ambient): -40 to 125°C
- Performance
  - Up to 40 MHz ARM® Cortex-M0+ core and up to 20 MHz bus clock
  - Up to 48 MHz ARM® Cortex-M0+ core
  - Single cycle 32-bit x 32-bit multiplier
  - Single cycle I/O access port
- Memories and memory interfaces
  - Up to 8 KB flash
  - Up to 1 KB RAM
- Clocks
  - Oscillator (OSC) - supports 32.768 kHz crystal or 4 MHz to 24 MHz crystal or ceramic resonator; choice of low power or high gain oscillators
  - Internal clock source (ICS) - internal FLL with internal or external reference, 37.5 kHz pre-trimmed internal reference for 48 MHz system clock
  - Internal 1 kHz low-power oscillator (LPO)
- System peripherals
  - Power management module (PMC) with three power modes: Run, Wait, Stop
  - Low-voltage detection (LVD) with reset or interrupt, selectable trip points
  - Watchdog with independent clock source (WDOG)
  - Programmable cyclic redundancy check module (CRC)
  - Serial wire debug interface (SWD)
  - Aliased SRAM bitband region (BIT-BAND)
  - Bit manipulation engine (BME)
- Security and integrity modules
  - 80-bit unique identification (ID) number per chip
- Human-machine interface
  - Up to 22 general-purpose input/output (GPIO)
  - Two 8-bit keyboard interrupt modules (KBI)
  - External interrupt (IRQ)
- Analog modules
  - One 12-channel 12-bit SAR ADC, operation in Stop mode, optional hardware trigger (ADC)
  - Two analog comparators containing a 6-bit DAC and programmable reference input (ACMP)
- Timers
  - One 6-channel FlexTimer/PWM (FTM)
  - One 2-channel FlexTimer/PWM (FTM)
  - One 2-channel periodic interrupt timer (PIT)
  - One pulse width timer (PWT)
  - One real-time clock (RTC)
- Communication interfaces
  - One SPI module (SPI)
  - One UART module (UART)
  - One I2C module (I2C)
- Package options
  - 24-pin QFN
  - 16-pin TSSOP

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [freescale.com](http://freescale.com) and perform a part number search for the following device numbers: KEAZN8.

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q KEA A C FFF M T PP N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>S = Automotive qualified</li> <li>P = Prequalification</li> </ul>
KEA	Kinetis Auto family	<ul style="list-style-type: none"> <li>KEA</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>Z = M0+ core</li> <li>F = M4 W/ DSP &amp; FPU</li> <li>C= M4 W/ AP + FPU</li> </ul>
C	CAN availability	<ul style="list-style-type: none"> <li>N = CAN not available</li> <li>(Blank) = CAN available</li> </ul>
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>8 = 8 KB</li> </ul>

*Table continues on the next page...*

## Parameter classification

Field	Description	Values
M	Maskset revision	<ul style="list-style-type: none"><li>• A = 1<sup>st</sup> Fab version</li><li>• B = Revision after 1<sup>st</sup> version</li></ul>
T	Temperature range (°C)	<ul style="list-style-type: none"><li>• C = -40 to 85</li><li>• V = -40 to 105</li><li>• M = -40 to 125</li></ul>
PP	Package identifier	<ul style="list-style-type: none"><li>• TG = 16 TSSOP (4.5 mm x 5 mm)</li><li>• FK = 24 QFN (4 mm x 4 mm)</li></ul>
N	Packaging type	<ul style="list-style-type: none"><li>• R = Tape and reel</li><li>• (Blank) = Trays</li></ul>

## 2.4 Example

This is an example part number:

SKEAZN8AMFK

## 3 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 1. Parameter classifications**

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

## 4 Ratings

### 4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	–55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	–6000	+6000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78D, *IC Latch-up Test*.

### 4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pullup resistor associated with the pin is enabled.

**Table 2. Voltage and current operating ratings**

Symbol	Description	Min.	Max.	Unit
$V_{DD}$	Digital supply voltage	-0.3	6.0	V
$I_{DD}$	Maximum current into $V_{DD}$	—	120	mA
$V_{IN}$	Input voltage except true open drain pins	-0.3	$V_{DD} + 0.3$ <sup>1</sup>	V
	Input voltage of true open drain pins	-0.3	6	V
$I_D$	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

1. Maximum rating of  $V_{DD}$  also applies to  $V_{IN}$ .

## 5 General

### 5.1 Nonswitching electrical specifications

#### 5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

**Table 3. DC characteristics**

Symbol	C	Descriptions		Min	Typical <sup>1</sup>	Max	Unit
—	—	Operating voltage		2.7	—	5.5	V
$V_{OH}$	P	Output high voltage	All I/O pins, except PTA2 and PTA3, standard-drive strength	5 V, $I_{load} = -5$ mA	$V_{DD} - 0.8$	—	V
	C			3 V, $I_{load} = -2.5$ mA	$V_{DD} - 0.8$	—	V
	P		High current drive pins, high-drive strength <sup>2</sup>	5 V, $I_{load} = -20$ mA	$V_{DD} - 0.8$	—	V
	C			3 V, $I_{load} = -10$ mA	$V_{DD} - 0.8$	—	V
$I_{OHT}$	D	Output high current	Max total $I_{OH}$ for all ports	5 V	—	—	mA
				3 V	—	—	

Table continues on the next page...

**Table 3. DC characteristics (continued)**

Symbol	C	Descriptions			Min	Typical <sup>1</sup>	Max	Unit
$V_{OL}$	P	Output low voltage	All I/O pins, standard-drive strength	5 V, $I_{load} = 5$ mA	—	—	0.8	V
	C			3 V, $I_{load} = 2.5$ mA	—	—	0.8	V
	P		High current drive pins, high-drive strength <sup>2</sup>	5 V, $I_{load} = 20$ mA	—	—	0.8	V
	C			3 V, $I_{load} = 10$ mA	—	—	0.8	V
$I_{OLT}$	D	Output low current	Max total $I_{OL}$ for all ports	5 V	—	—	100	mA
				3 V	—	—	60	
$V_{IH}$	P	Input high voltage	All digital inputs	$4.5 \leq V_{DD} < 5.5$ V	$0.65 \times V_{DD}$	—	—	V
				$2.7 \leq V_{DD} < 4.5$ V	$0.70 \times V_{DD}$	—	—	
$V_{IL}$	P	Input low voltage	All digital inputs	$4.5 \leq V_{DD} < 5.5$ V	—	—	$0.35 \times V_{DD}$	V
				$2.7 \leq V_{DD} < 4.5$ V	—	—	$0.30 \times V_{DD}$	
$V_{hys}$	C	Input hysteresis	All digital inputs	—	$0.06 \times V_{DD}$	—	—	mV
$ I_{In} $	P	Input leakage current	Per pin (pins in high impedance input mode)	$V_{IN} = V_{DD}$ or $V_{SS}$	—	0.1	1	$\mu$ A
$ I_{INTOT} $	C	Total leakage combined for all port pins	Pins in high impedance input mode	$V_{IN} = V_{DD}$ or $V_{SS}$	—	—	2	$\mu$ A
$R_{PU}$	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	k $\Omega$
$R_{PU}^3$	P	Pullup resistors	PTA2 and PTA3 pins	—	30.0	—	60.0	k $\Omega$
$I_{IC}$	D	DC injection current <sup>4, 5, 6</sup>	Single pin limit	$V_{IN} < V_{SS}$ , $V_{IN} > V_{DD}$	-2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
$C_{In}$	C	Input capacitance, all pins		—	—	—	7	pF
$V_{RAM}$	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.

2. Only PTB5, PTC1 and PTC5 support high current output.

3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.

4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to  $V_{SS}$  and  $V_{DD}$ . PTA2 and PTA3 are true open drain I/O pins that are internally clamped to  $V_{SS}$ .

5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.

## Nonswitching electrical specifications

6. Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If the positive injection current ( $V_{IN} > V_{DD}$ ) is higher than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure that external  $V_{DD}$  load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

**Table 4. LVD and POR specification**

Symbol	C	Description		Min	Typ	Max	Unit
V <sub>POR</sub>	D	POR re-arm voltage <sup>1</sup>		1.5	1.75	2.0	V
V <sub>LVDH</sub>	C	Falling low-voltage detect threshold—high range (LVDV = 1) <sup>2</sup>		4.2	4.3	4.4	V
V <sub>LVW1H</sub>	C	Falling low-voltage warning threshold—high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V <sub>LVW2H</sub>	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V <sub>LVW3H</sub>	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V <sub>LVW4H</sub>	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V <sub>HYSH</sub>	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V <sub>LVDL</sub>	C	Falling low-voltage detect threshold—low range (LVDV = 0)		2.56	2.61	2.66	V
V <sub>LVW1L</sub>	C	Falling low-voltage warning threshold—low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V <sub>LVW2L</sub>	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V <sub>LVW3L</sub>	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V <sub>LVW4L</sub>	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V <sub>HYSDL</sub>	C	Low range low-voltage detect hysteresis		—	40	—	mV
V <sub>HYSWL</sub>	C	Low range low-voltage warning hysteresis		—	80	—	mV
V <sub>BG</sub>	P	Buffered bandgap output <sup>3</sup>		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at  $V_{DD} = 5.0$  V, Temp = 25 °C

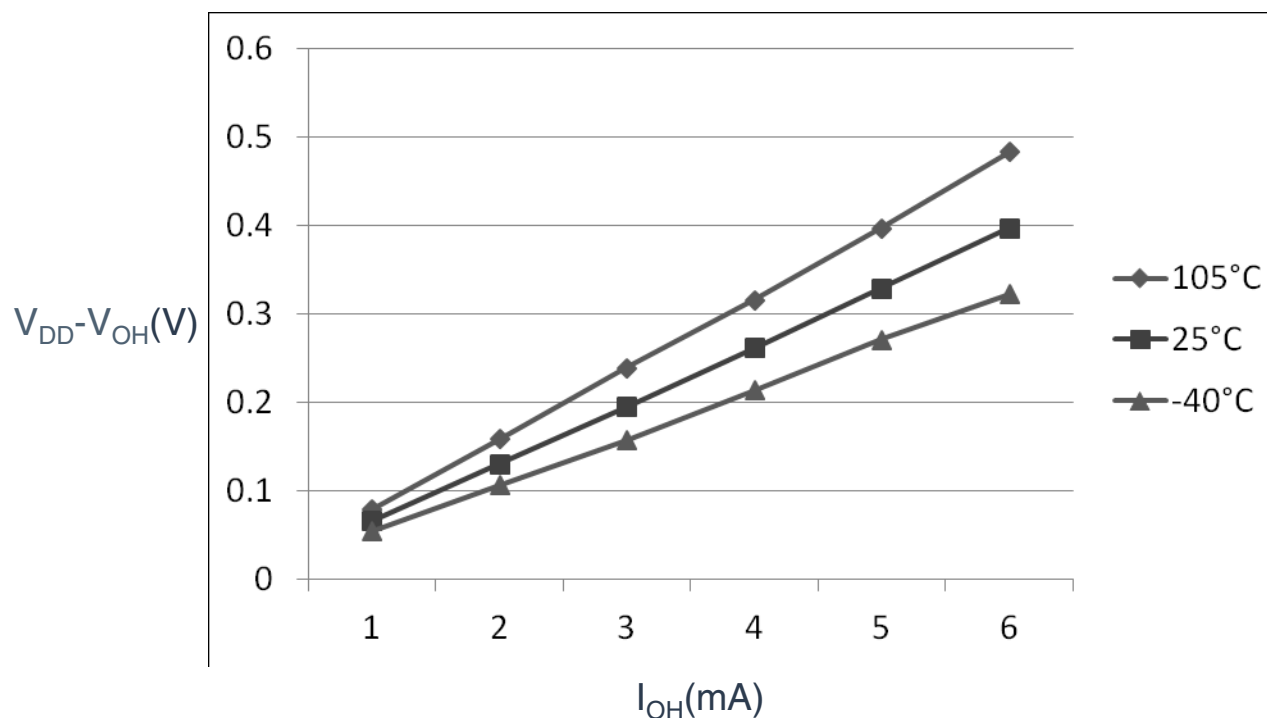


Figure 1. Typical  $V_{DD}-V_{OH}$  Vs.  $I_{OH}$  (standard drive strength) ( $V_{DD} = 5V$ )

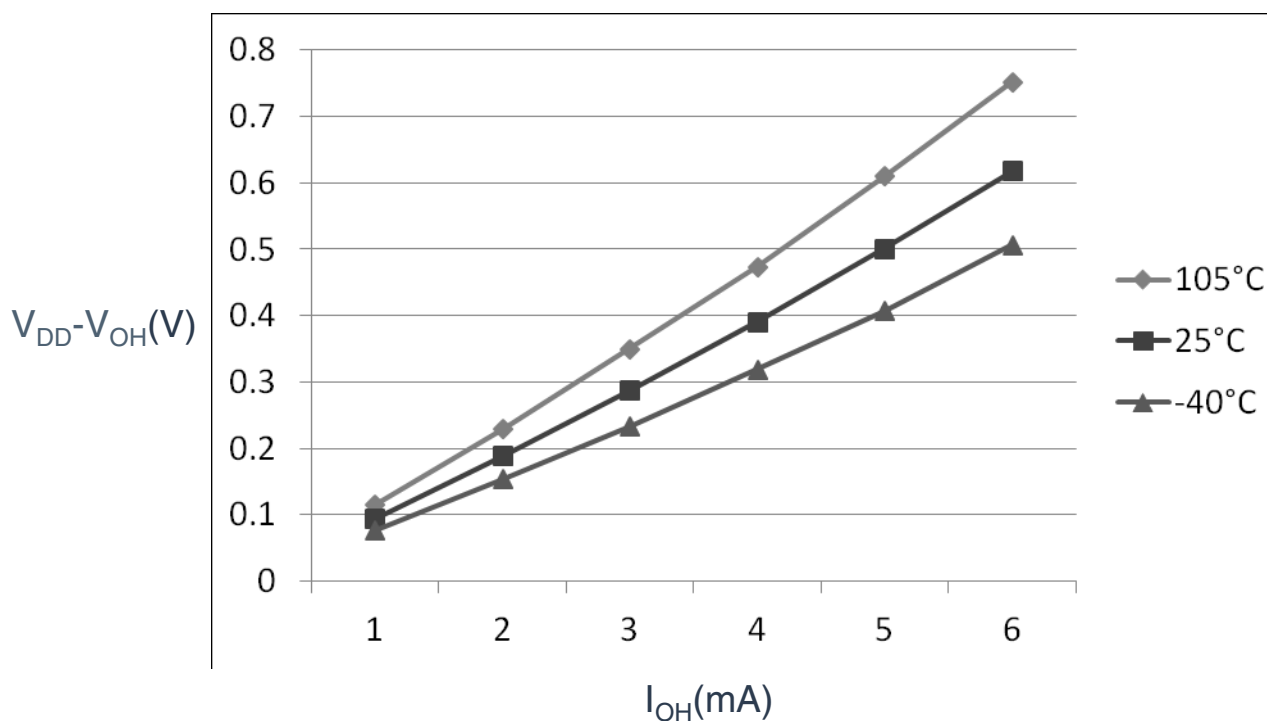


Figure 2. Typical  $V_{DD}-V_{OH}$  Vs.  $I_{OH}$  (standard drive strength) ( $V_{DD} = 3V$ )

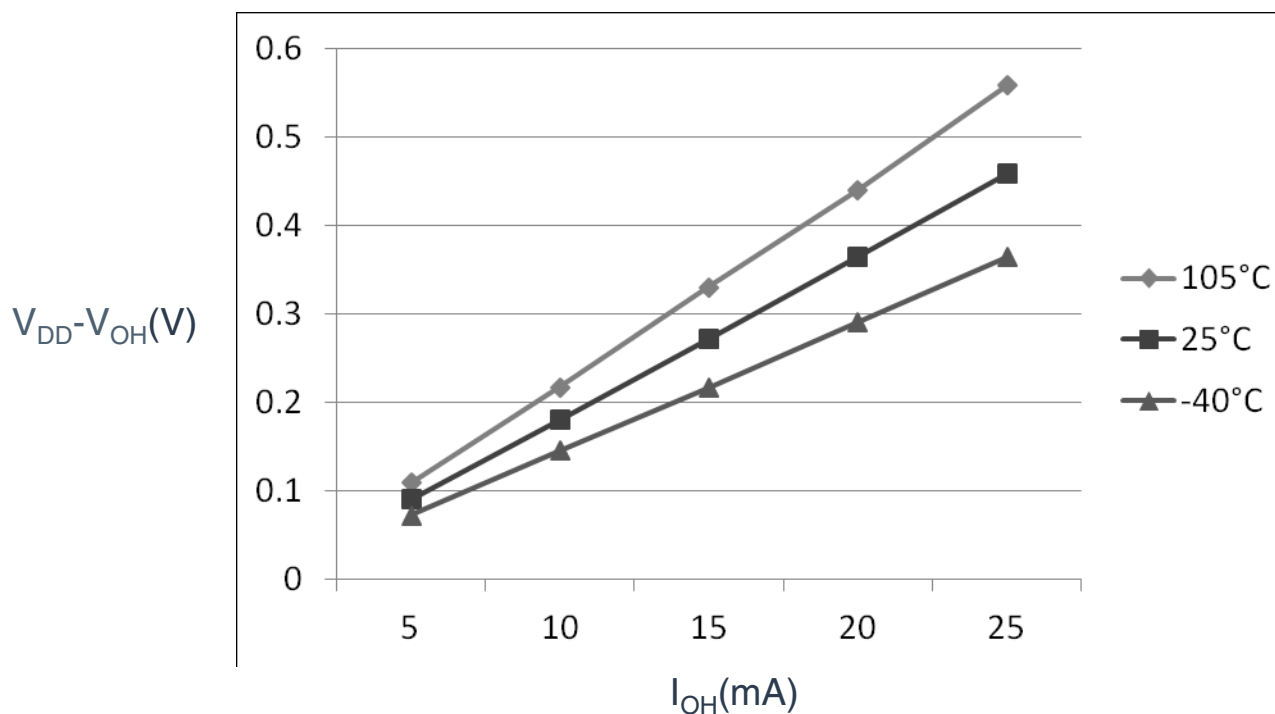


Figure 3. Typical  $V_{DD}-V_{OH}$  Vs.  $I_{OH}$  (high drive strength) ( $V_{DD} = 5\text{ V}$ )

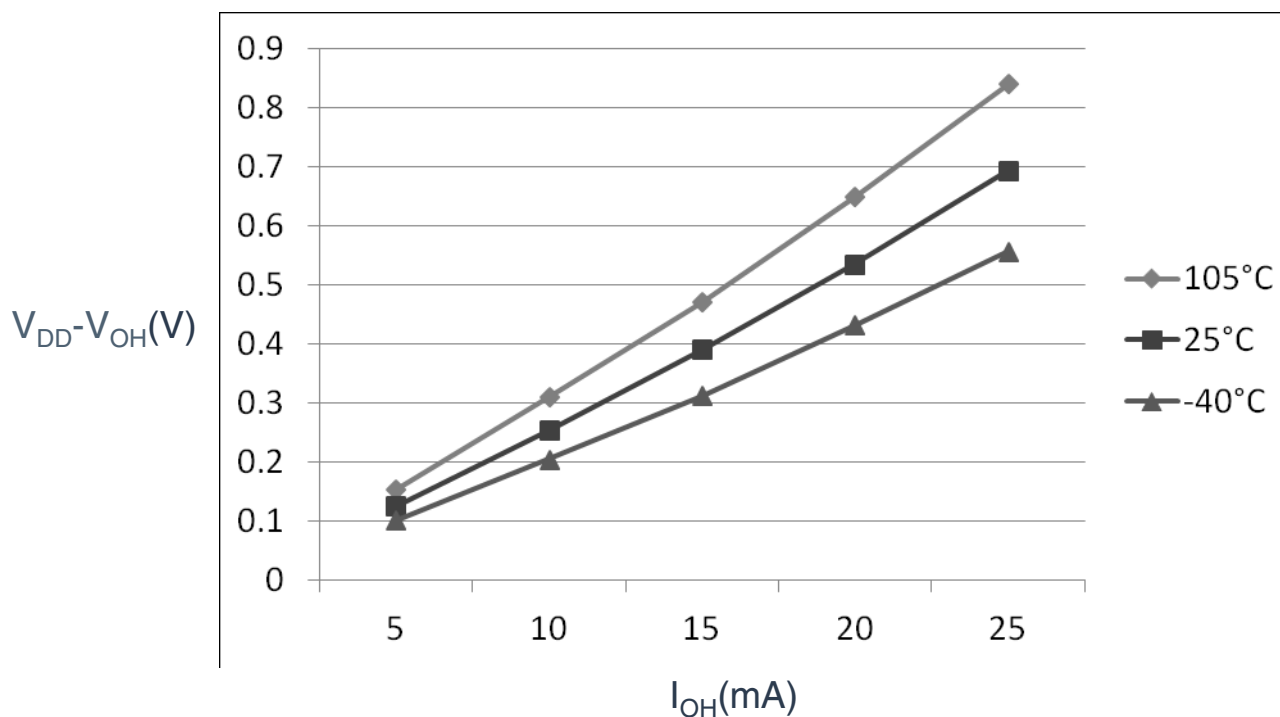


Figure 4. Typical  $V_{DD}-V_{OH}$  Vs.  $I_{OH}$  (high drive strength) ( $V_{DD} = 3\text{ V}$ )

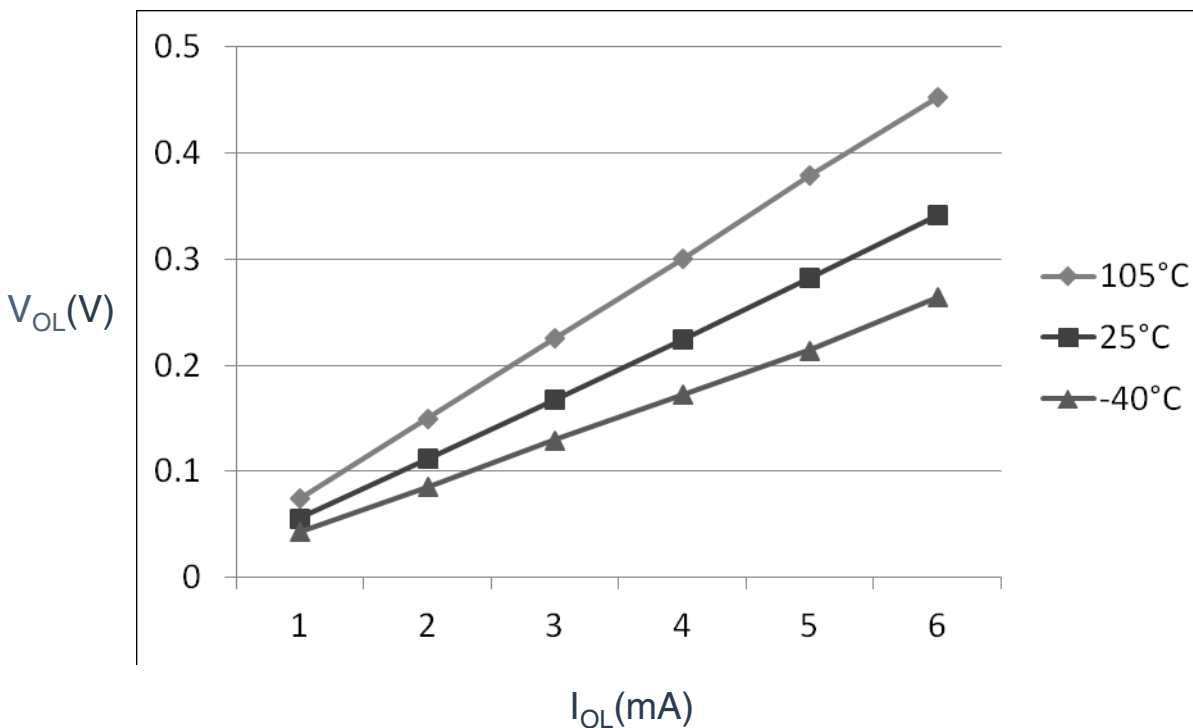


Figure 5. Typical  $V_{OL}$  Vs.  $I_{OL}$  (standard drive strength) ( $V_{DD} = 5$  V)

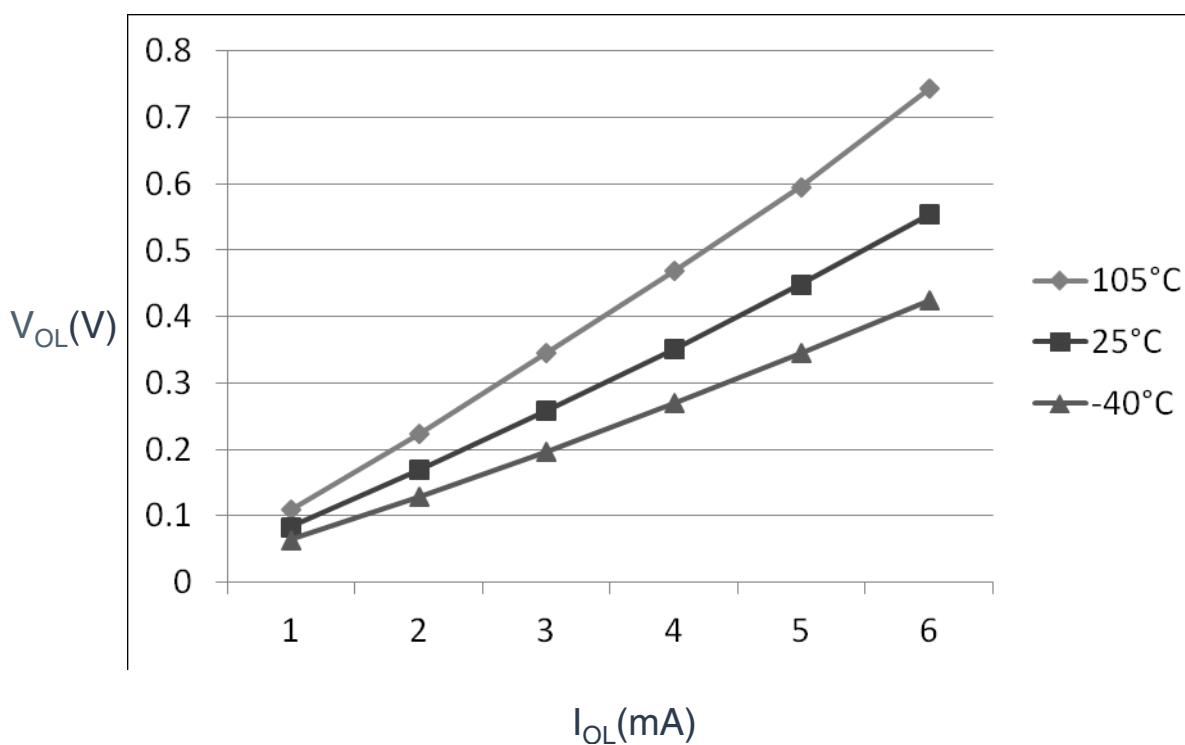


Figure 6. Typical  $V_{OL}$  Vs.  $I_{OL}$  (standard drive strength) ( $V_{DD} = 3$  V)

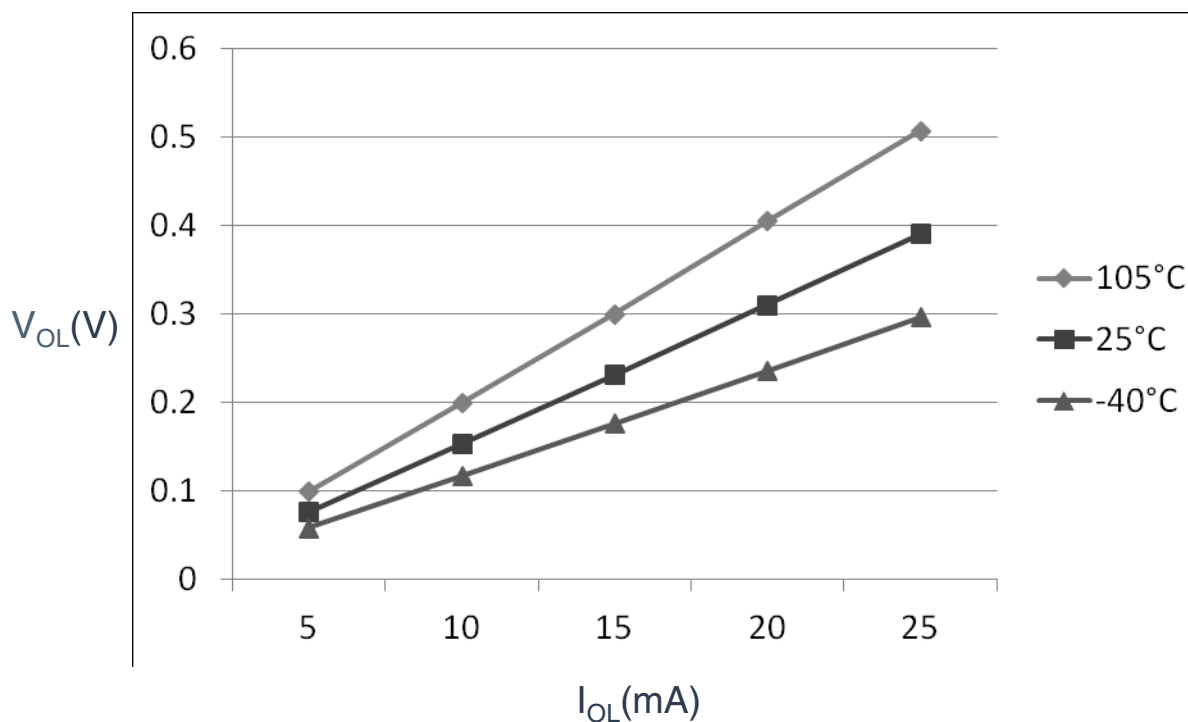


Figure 7. Typical  $V_{OL}$  Vs.  $I_{OL}$  (high drive strength) ( $V_{DD} = 5$  V)

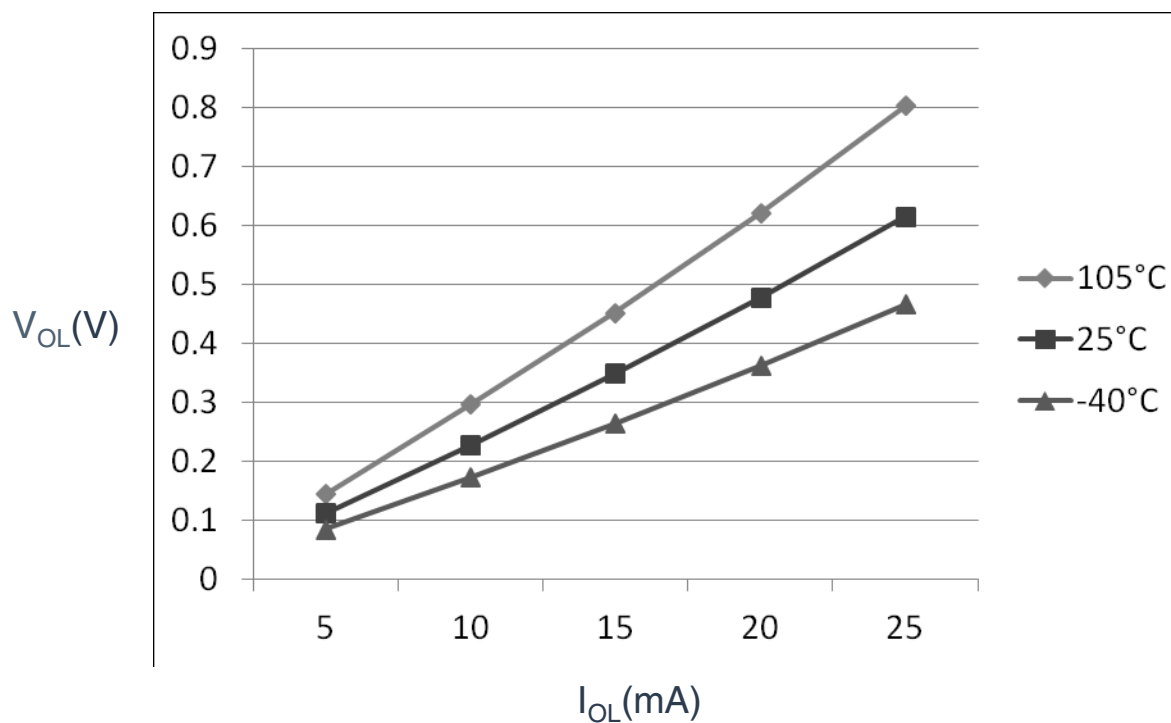


Figure 8. Typical  $V_{OL}$  Vs.  $I_{OL}$  (high drive strength) ( $V_{DD} = 3$  V)

## 5.1.2 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following Freescale applications notes, available on [freescale.com](http://freescale.com) for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

## 5.2 Switching specifications

### 5.2.1 Control timing

Table 5. Control timing

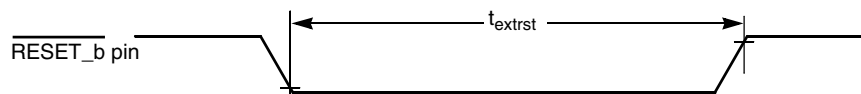
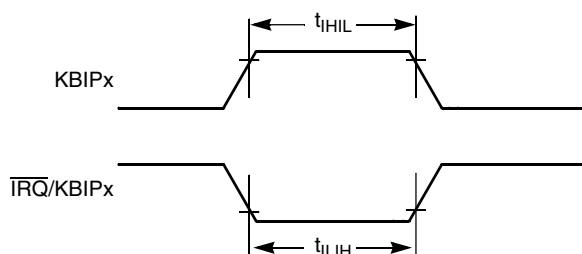
Num	C	Rating		Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	D	System and core clock		$f_{\text{Sys}}$	DC	—	48	MHz
2	P	Bus frequency ( $t_{\text{cyc}} = 1/f_{\text{Bus}}$ )		$f_{\text{Bus}}$	DC	—	24	MHz
3	P	Internal low power oscillator frequency		$f_{\text{LPO}}$	0.67	1.0	1.25	KHz
4	D	External reset pulse width <sup>2</sup>		$t_{\text{extrst}}$	$1.5 \times t_{\text{cyc}}$	—	—	ns
5	D	Reset low drive		$t_{\text{rstdrv}}$	$34 \times t_{\text{cyc}}$	—	—	ns
6	D	IRQ pulse width	Asynchronous path <sup>2</sup>	$t_{\text{LIH}}$	100	—	—	ns
	D		Synchronous path <sup>3</sup>	$t_{\text{HIL}}$	$1.5 \times t_{\text{cyc}}$	—	—	ns
7	D	Keyboard interrupt pulse width	Asynchronous path <sup>2</sup>	$t_{\text{LIH}}$	100	—	—	ns
	D		Synchronous path	$t_{\text{HIL}}$	$1.5 \times t_{\text{cyc}}$	—	—	ns
8	C	Port rise and fall time - Normal drive strength (load = 50 pF) <sup>4</sup>	—	$t_{\text{Rise}}$	—	10.2	—	ns
	C			$t_{\text{Fall}}$	—	9.5	—	ns

Table continues on the next page...

**Table 5. Control timing (continued)**

Num	C	Rating	Symbol	Min	Typical <sup>1</sup>	Max	Unit
	C	Port rise and fall time - high drive strength (load = 50 pF) <sup>4</sup>	$t_{\text{Rise}}$	—	5.4	—	ns
	C		$t_{\text{Fall}}$	—	4.6	—	ns

1. Typical values are based on characterization data at  $V_{\text{DD}} = 5.0 \text{ V}$ ,  $25^\circ\text{C}$  unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a RESET pin request.
3. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
4. Timing is shown with respect to 20%  $V_{\text{DD}}$  and 80%  $V_{\text{DD}}$  levels. Temperature range  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**Figure 9. Reset timing****Figure 10. KBIPx timing**

## 5.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter.

**Table 6. FTM input timing**

C	Function	Symbol	Min	Max	Unit
D	Timer clock frequency	$f_{\text{Timer}}$	$f_{\text{Bus}}$	$f_{\text{Sys}}$	Hz
D	External clock frequency	$f_{\text{TCLK}}$	0	$f_{\text{Timer}}/4$	Hz
D	External clock period	$t_{\text{TCLK}}$	4	—	$t_{\text{cyc}}$
D	External clock high time	$t_{\text{clkh}}$	1.5	—	$t_{\text{cyc}}$
D	External clock low time	$t_{\text{clkl}}$	1.5	—	$t_{\text{cyc}}$
D	Input capture pulse width	$t_{\text{ICPW}}$	1.5	—	$t_{\text{cyc}}$

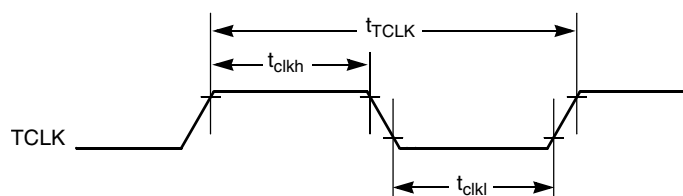


Figure 11. Timer external clock

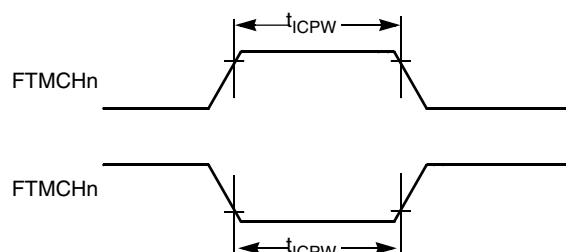


Figure 12. Timer input capture pulse

## 5.3 Thermal specifications

### 5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.

Table 7. Thermal attributes

Board type	Symbol	Description	24 QFN	16 TSSOP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	110	130	$^{\circ}\text{C/W}$	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	42	87	$^{\circ}\text{C/W}$	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	92	109	$^{\circ}\text{C/W}$	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	36	80	$^{\circ}\text{C/W}$	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	18	48	$^{\circ}\text{C/W}$	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	3.7	33	$^{\circ}\text{C/W}$	5

Table continues on the next page...

**Table 7. Thermal attributes (continued)**

Board type	Symbol	Description	24 QFN	16 TSSOP	Unit	Notes
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	10	10	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature ( $T_J$ ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

$T_A$  = Ambient temperature, °C

$\theta_{JA}$  = Package thermal resistance, junction-to-ambient, °C/W

$$P_D = P_{int} + P_{I/O}$$

$P_{int}$  =  $I_{DD} \times V_{DD}$ , Watts - chip internal power

$P_{I/O}$  = Power dissipation on input and output pins - user determined

For most applications,  $P_{I/O} \ll P_{int}$  and can be neglected. An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is:

$$P_D = K \div (T_J + 273 \text{ °C})$$

Solving the equations above for K gives:

$$K = P_D \times (T_A + 273 \text{ °C}) + \theta_{JA} \times (P_D)^2$$

where K is a constant pertaining to the particular part. K can be determined by measuring  $P_D$  (at equilibrium) for an known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving the above equations iteratively for any value of  $T_A$ .

## 6 Peripheral operating requirements and behaviors

## 6.1 Core modules

### 6.1.1 SWD electricals

Table 8. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>	0	24	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	3	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	35	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

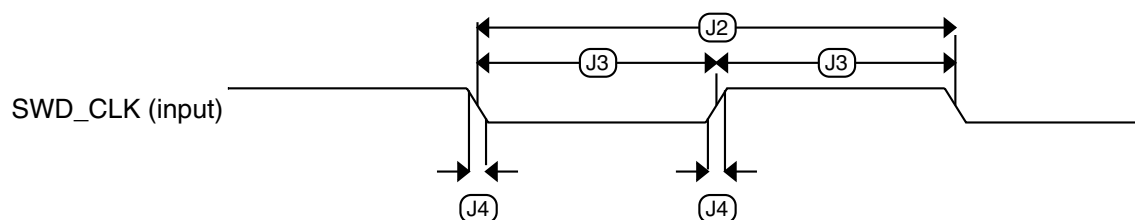


Figure 13. Serial wire clock input timing

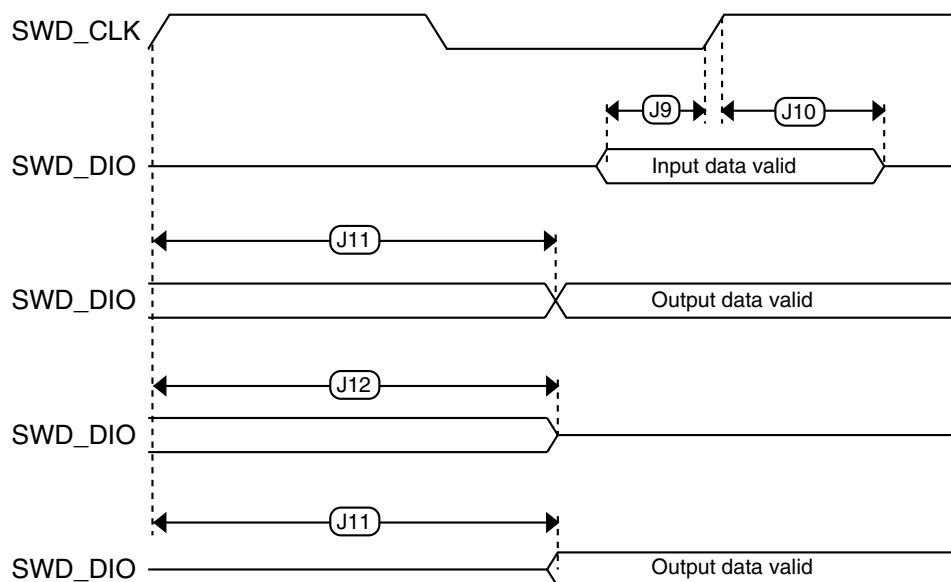


Figure 14. Serial wire data timing

## 6.2 External oscillator (OSC) and ICS characteristics

Table 9. OSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	C	Crystal or resonator frequency	Low range (RANGE = 0)	$f_{lo}$	31.25	32.768	39.0625	kHz
	C		High range (RANGE = 1)	$f_{hi}$	4	—	24	MHz
2	D	Load capacitors		C1, C2	See Note <sup>2</sup>			
3	D	Feedback resistor	Low Frequency, Low-Power Mode <sup>3</sup>	$R_F$	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode <sup>3</sup>	$R_S$	—	0	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode <sup>3</sup>	$R_S$	—	0	—	kΩ

Table continues on the next page...

**Table 9. OSC and ICS specifications (temperature range = -40 to 125 °C ambient) (continued)**

Num	C	Characteristic		Symbol	Min	Typical <sup>1</sup>	Max	Unit
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time low range = 32.768 kHz crystal; High range = 20 MHz crystal <sup>4,5</sup>	Low range, low power	$t_{CSTL}$	—	1000	—	ms
	C		Low range, high gain		—	800	—	ms
	C		High range, low power	$t_{CSTH}$	—	3	—	ms
	C		High range, high gain		—	1.5	—	ms
7	T	Internal reference start-up time		$t_{IRST}$	—	20	50	μs
8	P	Internal reference clock (IRC) frequency trim range		$f_{int\_t}$	31.25	—	39.0625	kHz
9	P	Internal reference clock frequency, factory trimmed	T = 25 °C, V <sub>DD</sub> = 5 V	$f_{int\_ft}$	—	37.5	—	kHz
10	P	DCO output frequency range	FLL reference = $f_{int\_t}$ , $f_{lo}$ , or $f_{hi}/RDIV$	$f_{dco}$	40	—	50	MHz
11	P	Factory trimmed internal oscillator accuracy	T = 25 °C, V <sub>DD</sub> = 5 V	$\Delta f_{int\_ft}$	-0.5	—	0.5	%
12	C	Deviation of IRC over temperature when trimmed at T = 25 °C, V <sub>DD</sub> = 5 V	Over temperature range from -40 °C to 105°C	$\Delta f_{int\_t}$	-1.2	—	1	%
			Over temperature range from 0 °C to 105°C	$\Delta f_{int\_t}$	-0.5	—	1	
13	C	Frequency accuracy of DCO output using factory trim value	Over temperature range from -40 °C to 105°C	$\Delta f_{dco\_ft}$	-1.7	—	1.5	%
			Over temperature range from 0 °C to 105°C	$\Delta f_{dco\_ft}$	-1	—	1.5	
14	C	FLL acquisition time <sup>4,6</sup>		$t_{Acquire}$	—	—	2	ms
15	C	Long term jitter of DCO output clock (averaged over 2 ms interval) <sup>7</sup>		$C_{Jitter}$	—	0.02	0.2	% $f_{dco}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.
3. Load capacitors (C<sub>1</sub>, C<sub>2</sub>), feedback resistor (R<sub>F</sub>) and series resistor (R<sub>S</sub>) are incorporated internally when RANGE = HGO = 0.
4. This parameter is characterized and not tested on each device.
5. Proper PC board layout procedures must be followed to achieve specifications.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{Bus}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V<sub>DD</sub> and V<sub>SS</sub> and variation in crystal oscillator frequency increase the  $C_{Jitter}$  percentage for a given interval.

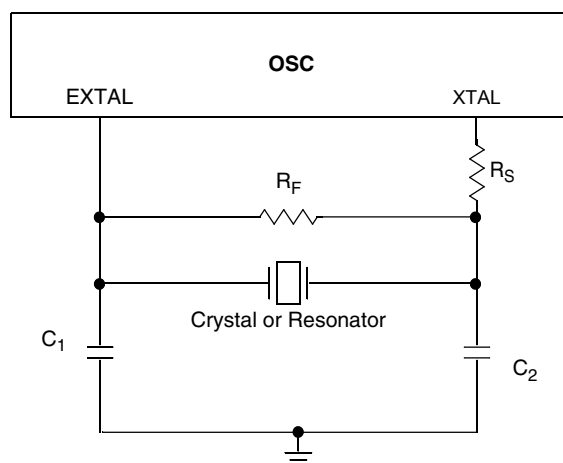


Figure 15. Typical crystal or resonator circuit

## 6.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash memories.

Table 10. Flash characteristics

C	Characteristic	Symbol	Min <sup>1</sup>	Typical <sup>2</sup>	Max <sup>3</sup>	Unit <sup>4</sup>
D	Supply voltage for program/erase –40 °C to 125 °C	$V_{\text{prog/erase}}$	2.7	—	5.5	V
D	Supply voltage for read operation	$V_{\text{Read}}$	2.7	—	5.5	V
D	NVM Bus frequency	$f_{\text{NVMBUS}}$	1	—	24	MHz
D	NVM Operating frequency	$f_{\text{NVMOP}}$	0.8	1	1.05	MHz
D	Erase Verify All Blocks	$t_{\text{VFYALL}}$	—	—	2605	$t_{\text{cyc}}$
D	Erase Verify Flash Block	$t_{\text{RD1BLK}}$	—	—	2579	$t_{\text{cyc}}$
D	Erase Verify Flash Section	$t_{\text{RD1SEC}}$	—	—	485	$t_{\text{cyc}}$
D	Read Once	$t_{\text{RDONCE}}$	—	—	464	$t_{\text{cyc}}$
D	Program Flash (2 word)	$t_{\text{PGM2}}$	0.12	0.13	0.31	ms
D	Program Flash (4 word)	$t_{\text{PGM4}}$	0.21	0.21	0.49	ms
D	Program Once	$t_{\text{PGMONCE}}$	0.20	0.21	0.21	ms
D	Erase All Blocks	$t_{\text{ERSALL}}$	95.42	100.18	100.30	ms
D	Erase Flash Block	$t_{\text{ERSBLK}}$	95.42	100.18	100.30	ms
D	Erase Flash Sector	$t_{\text{ERSPG}}$	19.10	20.05	20.09	ms
D	Unsecure Flash	$t_{\text{UNSECU}}$	95.42	100.19	100.31	ms
D	Verify Backdoor Access Key	$t_{\text{VFYKEY}}$	—	—	482	$t_{\text{cyc}}$
D	Set User Margin Level	$t_{\text{MLOADU}}$	—	—	415	$t_{\text{cyc}}$
C	FLASH Program/erase endurance $T_L$ to $T_H = -40\text{ °C to }125\text{ °C}$	$n_{\text{FLPE}}$	10 k	100 k	—	Cycles

Table continues on the next page...

**Table 10. Flash characteristics (continued)**

C	Characteristic	Symbol	Min <sup>1</sup>	Typical <sup>2</sup>	Max <sup>3</sup>	Unit <sup>4</sup>
C	Data retention at an average junction temperature of $T_{Javg} = 85^{\circ}\text{C}$ after up to 10,000 program/erase cycles	$t_{D\_ret}$	15	100	—	years

1. Minimum times are based on maximum  $f_{NVMOP}$  and maximum  $f_{NVMBUS}$
2. Typical times are based on typical  $f_{NVMOP}$  and maximum  $f_{NVMBUS}$
3. Maximum times are based on typical  $f_{NVMOP}$  and typical  $f_{NVMBUS}$  plus aging
4.  $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal  $V_{DD}$  supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

## 6.4 Analog

### 6.4.1 ADC characteristics

**Table 11. 5 V 12-bit ADC operating conditions**

Characteristic	Conditions	Symbol	Min	Typ <sup>1</sup>	Max	Unit	Comment
Supply voltage	Absolute	$V_{DDA}$	2.7	—	5.5	V	—
	Delta to $V_{DD}$ ( $V_{DD} - V_{DDA}$ )	$\Delta V_{DDA}$	-100	0	+100	mV	—
Input voltage		$V_{ADIN}$	$V_{REFL}$	—	$V_{REFH}$	V	—
Input capacitance		$C_{ADIN}$	—	4.5	5.5	pF	—
Input resistance		$R_{ADIN}$	—	3	5	k $\Omega$	—
Analog source resistance	12-bit mode	$R_{AS}$	—	—	2	k $\Omega$	External to MCU
	• $f_{ADCK} > 4 \text{ MHz}$		—	—	5		
	• $f_{ADCK} < 4 \text{ MHz}$		—	—	5		
	10-bit mode		—	—	5		
	• $f_{ADCK} > 4 \text{ MHz}$		—	—	10		
	• $f_{ADCK} < 4 \text{ MHz}$		—	—	10		
	8-bit mode		—	—	10		
	(all valid $f_{ADCK}$ )						
ADC conversion clock frequency	High speed (ADLPC=0)	$f_{ADCK}$	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume  $V_{DDA} = 5.0 \text{ V}$ ,  $\text{Temp} = 25^{\circ}\text{C}$ ,  $f_{ADCK} = 1.0 \text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.

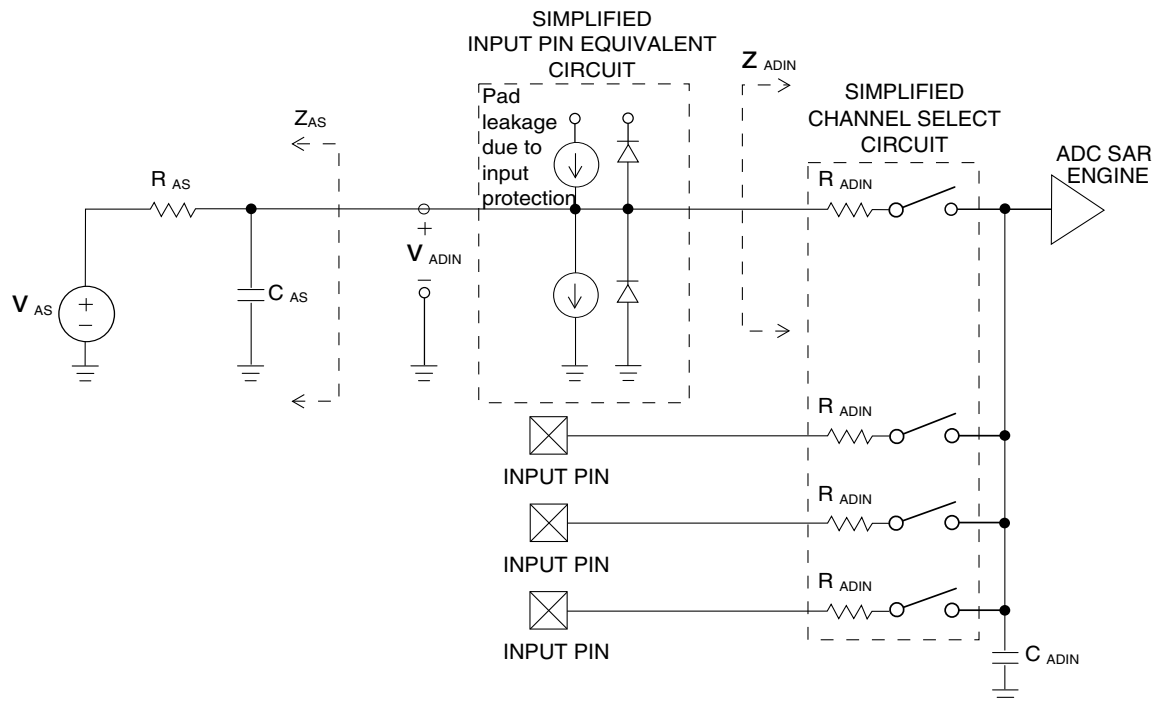


Figure 16. ADC input impedance equivalency diagram

Table 12. 12-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

Characteristic	Conditions	C	Symbol	Min	Typ <sup>1</sup>	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	$I_{DDA}$	—	133	—	$\mu A$
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	$I_{DDA}$	—	218	—	$\mu A$
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	$I_{DDA}$	—	327	—	$\mu A$
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	$I_{DDA}$	—	582	990	$\mu A$
Supply current	Stop, reset, module off	T	$I_{DDA}$	—	0.011	1	$\mu A$
ADC asynchronous clock source	High speed (ADLPC = 0)	P	$f_{ADACK}$	2	3.3	5	MHz

Table continues on the next page...

**Table 12. 12-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Characteristic	Conditions	C	Symbol	Min	Typ <sup>1</sup>	Max	Unit
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	$t_{ADC}$	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	$t_{ADS}$	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error <sup>2</sup>	12-bit mode	T	$E_{TUE}$	—	$\pm 3.0$	—	LSB <sup>3</sup>
	10-bit mode	C		—	$\pm 1.0$	$\pm 2.0$	
	8-bit mode	T		—	$\pm 0.8$	—	
Differential Non-Linearity	12-bit mode	T	DNL	—	$\pm 1.2$	—	LSB <sup>3</sup>
	10-bit mode <sup>4</sup>	C		—	$\pm 0.3$	$\pm 1.0$	
	8-bit mode <sup>4</sup>	T		—	$\pm 0.15$	—	
Integral Non-Linearity	12-bit mode	T	INL	—	$\pm 1.2$	—	LSB <sup>3</sup>
	10-bit mode	C		—	$\pm 0.3$	$\pm 1.0$	
	8-bit mode	T		—	$\pm 0.15$	—	
Zero-scale error <sup>5</sup>	12-bit mode	T	$E_{ZS}$	—	$\pm 1.2$	—	LSB <sup>3</sup>
	10-bit mode	C		—	$\pm 0.15$	$\pm 1.0$	
	8-bit mode	T		—	$\pm 0.3$	—	
Full-scale error <sup>6</sup>	12-bit mode	T	$E_{FS}$	—	$\pm 1.8$	—	LSB <sup>3</sup>
	10-bit mode	C		—	$\pm 0.7$	$\pm 1.0$	
	8-bit mode	T		—	$\pm 0.5$	—	
Quantization error	$\leq 12$ bit modes	D	$E_Q$	—	—	$\pm 0.5$	LSB <sup>3</sup>
Input leakage error <sup>7</sup>	all modes	D	$E_{IL}$	$I_{in} * R_{AS}$			mV
Temp sensor slope	-40 °C–25 °C	D	m	—	3.266	—	mV/°C
	25 °C–125 °C			—	3.638	—	
Temp sensor voltage	25 °C	D	$V_{TEMP25}$	—	1.396	—	V

1. Typical values assume  $V_{DDA} = 5.0$  V, Temp = 25 °C,  $f_{ADCK} = 2.5$  MHz under FBE mode and alternate clock source (ALTCLK) is selected as ADC clock.
2. Includes quantization
3.  $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5.  $V_{ADIN} = V_{SSA}$
6.  $V_{ADIN} = V_{DDA}$
7.  $I_{in}$  = leakage current (refer to DC characteristics)

## 6.4.2 Analog comparator (ACMP) electricals

**Table 13. Comparator electrical specifications**

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	$V_{DDA}$	2.7	—	5.5	V
T	Supply current (Operation mode)	$I_{DDA}$	—	10	20	$\mu A$
D	Analog input voltage	$V_{AIN}$	$V_{SS} - 0.3$	—	$V_{DDA}$	V
P	Analog input offset voltage	$V_{AIO}$	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	$V_H$	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	$V_H$	—	20	30	mV
T	Supply current (Off mode)	$I_{DDAOFF}$	—	60	—	nA
C	Propagation Delay	$t_D$	—	0.4	1	$\mu s$

## 6.5 Communication interfaces

### 6.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$ , unless noted, and 25 pF load on all SPI pins. All timing assumes slew rate control is disabled and high-drive strength is enabled for SPI output pins.

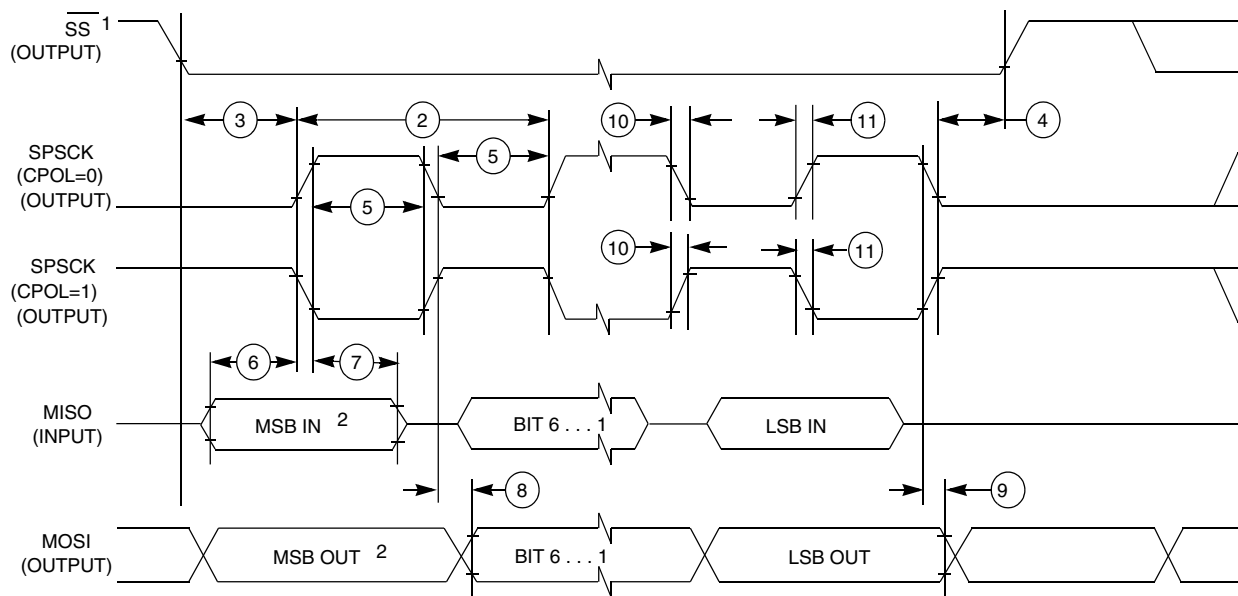
**Table 14. SPI master mode timing**

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	$f_{op}$	Frequency of operation	$f_{Bus}/2048$	$f_{Bus}/2$	Hz	$f_{Bus}$ is the bus clock
2	$t_{SPSCK}$	SPSCK period	$2 \times t_{Bus}$	$2048 \times t_{Bus}$	ns	$t_{Bus} = 1/f_{Bus}$
3	$t_{Lead}$	Enable lead time	1/2	—	$t_{SPSCK}$	—
4	$t_{Lag}$	Enable lag time	1/2	—	$t_{SPSCK}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{Bus} - 30$	$1024 \times t_{Bus}$	ns	—
6	$t_{SU}$	Data setup time (inputs)	8	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	8	—	ns	—
8	$t_v$	Data valid (after SPSCK edge)	—	25	ns	—
9	$t_{HO}$	Data hold time (outputs)	20	—	ns	—
10	$t_{RI}$	Rise time input	—	$t_{Bus} - 25$	ns	—

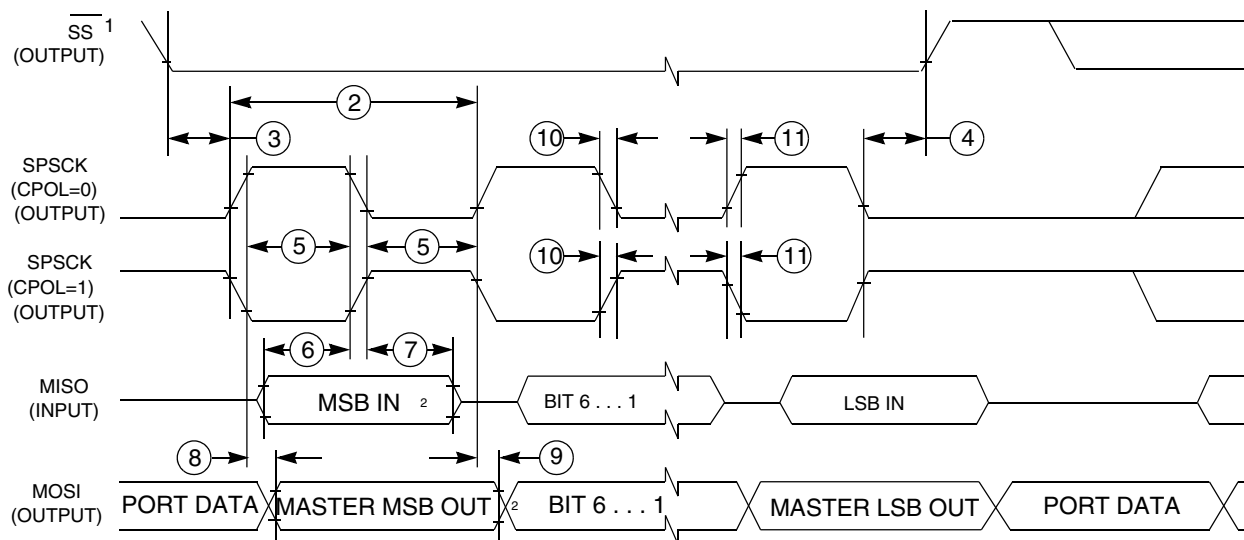
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**Table 14. SPI master mode timing (continued)**

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
	$t_{FI}$	Fall time input				
11	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

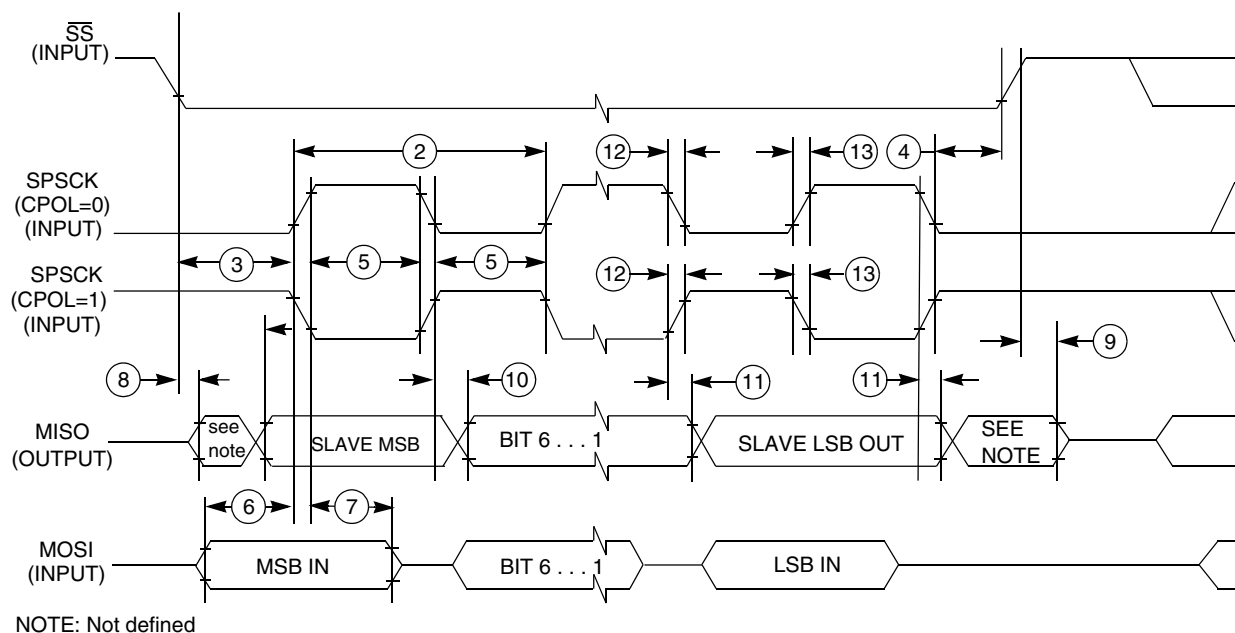
**Figure 17. SPI master mode timing (CPHA=0)**

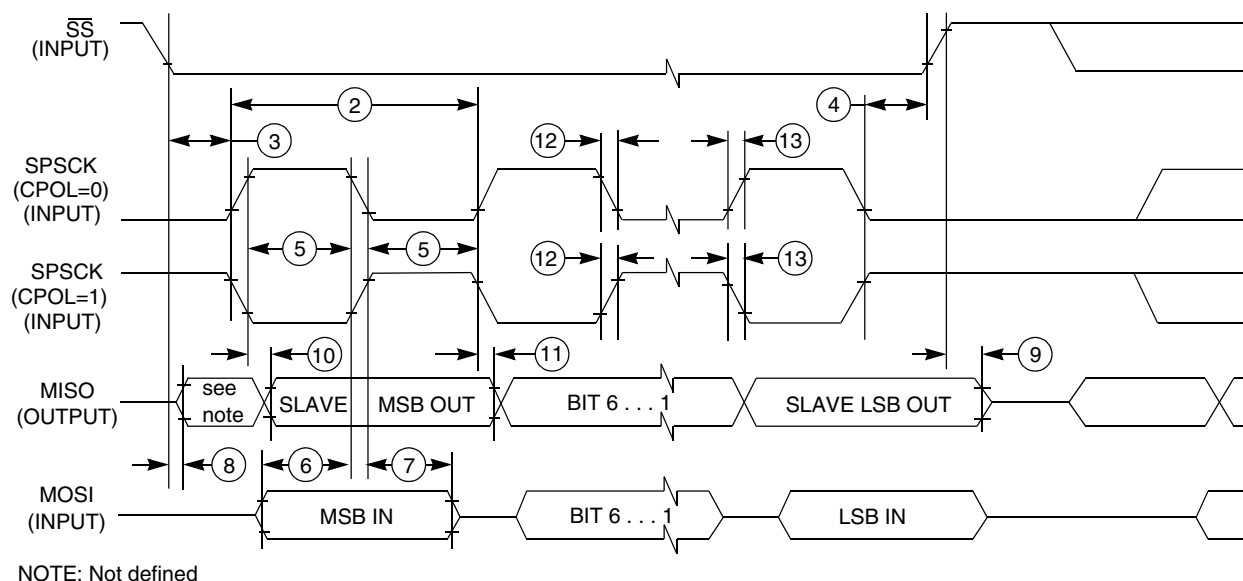
1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 18. SPI master mode timing (CPHA=1)**

**Table 15. SPI slave mode timing**

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	$f_{op}$	Frequency of operation	0	$f_{Bus}/4$	Hz	$f_{Bus}$ is the bus clock as defined in <a href="#">Control timing</a> .
2	$t_{SPSCK}$	SPSCK period	$4 \times t_{Bus}$	—	ns	$t_{Bus} = 1/f_{Bus}$
3	$t_{Lead}$	Enable lead time	1	—	$t_{Bus}$	—
4	$t_{Lag}$	Enable lag time	1	—	$t_{Bus}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{Bus} - 30$	—	ns	—
6	$t_{SU}$	Data setup time (inputs)	15	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	25	—	ns	—
8	$t_a$	Slave access time	—	$t_{Bus}$	ns	Time to data active from high-impedance state
9	$t_{dis}$	Slave MISO disable time	—	$t_{Bus}$	ns	Hold time to high-impedance state
10	$t_v$	Data valid (after SPSCK edge)	—	25	ns	—
11	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
12	$t_{RI}$	Rise time input	—	$t_{Bus} - 25$	ns	—
	$t_{FI}$	Fall time input	—	$t_{Bus} - 25$	ns	—
13	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output	—	25	ns	—

**Figure 19. SPI slave mode timing (CPHA = 0)**



**Figure 20. SPI slave mode timing (CPHA=1)**

## 7 Dimensions

### 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [freescale.com](http://freescale.com) and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
16-pin TSSOP	98ASH70247A
24-pin QFN	98ASA00474D

## 8 Pinout

### 8.1 Signal multiplexing and pin assignments

For the pin muxing details see section Signal Multiplexing and Signal Descriptions of KEA8 Reference Manual.

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