LPC5411x

32-bit ARM Cortex-M4/M0+ MCU; 192 KB SRAM; 256 KB flash, Crystal-less USB operation, DMIC subsystem, Flexcomm Interface, 32-bit counter/ timers, SCTimer/PWM, 12-bit 5.0 Msamples/sec ADC, Temperature sensor

Rev. 1.2 — 24 February 2016 Product data sheet

1. General description

The LPC5411x are ARM Cortex-M4 based microcontrollers for embedded applications. These devices include an ARM Cortex-M0+ coprocessor, up to 192 KB of on-chip SRAM, up to 256 KB on-chip flash, full-speed USB device interface with Crystal-less operation, a DMIC subsystem with PDM microphone interface and I2S, five general-purpose timers, one SCTimer/PWM, one RTC/alarm timer, one 24-bit Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), eight flexible serial communication peripherals (each of which can be a USART, SPI, or I^2C interface), and one 12-bit 5.0 Msamples/sec ADC, and a temperature sensor.

The ARM Cortex-M4 is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point unit is integrated in the core.

The ARM Cortex-M0+ coprocessor is an energy-efficient and easy-to-use 32-bit core which is code and tool-compatible with the Cortex-M4 core. The Cortex-M0+ coprocessor offers up to 100 MHz performance with a simple instruction set and reduced code size.

2. Features and benefits

- Dual processor cores: ARM Cortex-M4 and ARM Cortex-M0+. Both cores operate up to a maximum frequency of 100 MHz.
- ARM Cortex-M4 core (version r0p1):
  - ARM Cortex-M4 processor, running at a frequency of up to 100 MHz.
  - Floating Point Unit (FPU) and Memory Protection Unit (MPU).
  - ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug (SWD) with six instruction breakpoints, two literal comparators, and four watch points. Includes Serial Wire Output for enhanced debug capabilities.
  - System tick timer.

- ARM Cortex-M0+ core
  - ARM Cortex-M0+ processor, running at a frequency of up to 100 MHz (uses the same clock as Cortex-M4) with a single-cycle multiplier and a fast single-cycle I/O port.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug with four breakpoints and two watch points.
  - System tick timer.
- On-chip memory:
  - Up to 256 KB on-chip flash program memory with flash accelerator and 256 byte page erase and write.
  - Up to 192 KB total SRAM consisting of 160 KB contiguous main SRAM and an additional 32 KB SRAM on the I&D buses.
- ROM API support:
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
  - ROM-based USB drivers (HID, CDC, and MSC). Flash updates via USB is supported.
  - Supports booting from valid user code in flash, USART, SPI, and I^2C.
  - Dual image boot.
- Serial interfaces:
  - Flexcomm Interface contains eight serial peripherals. Each can be selected by software to be a USART, SPI, or I^2C interface. Two Flexcomm Interfaces also include an I^2S interface. Each Flexcomm Interface includes a FIFO that supports USART, SPI, and I^2S if supported by that Flexcomm Interface. A variety of clocking options are available to each Flexcomm Interface and include a shared fractional baud-rate generator.
  - I^2C-bus interfaces support Fast-mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Two sets of true I^2C pads also support high speed mode (3.4 Mbit/s) as a slave.
  - Crystal-less USB full-speed device interface.
- Digital peripherals:
  - DMA controller with 20 channels and 20 programmable triggers, able to access all memories and DMA-capable peripherals.
  - Up to 48 General-Purpose Input/Output (GPIO) pins. Most GPIOs have configurable pull-up/pull-down resistors, programmable open-drain mode, and input inverter.
  - GPIO registers are located on the AHB for fast access.
  - Up to eight GPIOs can be selected as pin interrupts (PINT), triggered by rising, falling or both input edges.
  - Two GPIO grouped interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
  - CRC engine.

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- Analog peripherals:
  - 12-bit ADC with 12 input channels and with multiple internal and external trigger inputs and sample rates of up to 5.0 MSamples/sec. The ADC supports two independent conversion sequences.
  - Integrated temperature sensor connected to the ADC.
- DMIC subsystem including a dual-channel PDM microphone interface, flexible decimators, 16 entry FIFOs, optional DC locking, hardware voice activity detection, and the option to stream the processed output data to I^2S.
- Timers:
  - Five 32-bit standard general purpose timers/counters, four of which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests. The fifth timer does not have external pin connections and may be used for internal timing operations.
  - One SCTimer/PWM with eight input and eight output functions (including capture and match). Inputs and outputs can be routed to or from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports ten captures/matches, ten events, and ten states.
  - 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
  - Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Windowed Watchdog Timer (WWDT).
- Clock generation:
  - 12 MHz internal Free Running Oscillator (FRO). This oscillator provides a selectable 48 MHz or 96 MHz output, and a 12 MHz output (divided down from the selected higher frequency) that can be used as a system clock. The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.
  - External clock input for clock frequencies of up to 25 MHz.
  - Watchdog oscillator (WDTOSC) with a frequency range of 200 kHz to 1.5 MHz.
  - 32.768 kHz low-power RTC oscillator.
  - System PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency external clock. May be run from the internal FRO 12 MHz output, the external clock input CLKIN, or the RTC oscillator.
  - Clock output function with divider.
  - Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.
- Power control:
  - Programmable PMU (Power Management Unit) to minimize power consumption and to match requirements at different performance levels.
  - Reduced power modes: sleep, deep-sleep, and deep power-down.
  - Wake-up from deep-sleep modes due to activity on the USART, SPI, and I2C peripherals when operating as slaves.

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- The Micro-Tick Timer running from the watchdog oscillator, and the Real-Time Clock (RTC) running from the 32.768 kHz clock, can be used to wake-up the device from any reduced power modes.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.

- Single power supply 1.62 V to 3.6 V.
- JTAG boundary scan supported.
- 128 bit unique device serial number for identification.
- Operating temperature range −40 °C to +105 °C.
- Available as WLCSP49 and LQFP64 packages.

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3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC54113J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.436 x 3.436 x 0.525 mm	-
LPC54114J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.436 x 3.436 x 0.525 mm	-
LPC54113J128BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54113J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54114J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

3.1 Ordering options

Table 2. Ordering options

Type number	Flash in KB	SRAM in KB					Cortex-M4 with FPU	Cortex-M0+	USB FS	GPIO
		SRAMX	SRAM0	SRAM1	SRAM2	Total				
LPC54113J256UK49	256	32	64	64	32	192	1	0	1	37
LPC54114J256UK49	256	32	64	64	32	192	1	1	1	37
LPC54113J128BD64	128	32	64	-	-	96	1	0	1	48
LPC54113J256BD64	256	32	64	64	32	192	1	0	1	48
LPC54114J256BD64	256	32	64	64	32	192	1	1	1	48

4. Marking

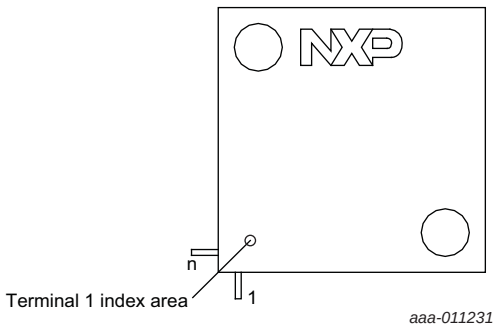

Fig 1. LQFP64 package marking

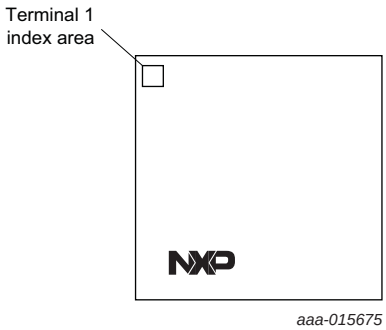

Fig 2. WLCSP49 package marking

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The LPC5411x LQFP64 package has the following top-side marking:

- First line: LPC5411xJyyy
  - x: 4 = dual core (M4, M0+)
  - x: 3 = single core (M4)
  - yyy
  - : flash size
- Second line: BD64
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - R = Chip revision.

The LPC5411x WLCSP49 package has the following top-side marking:

- First line: LPC5411x
  - x: 4 = dual core (M4, M0+)
  - x: 3 = single core (M4)
- Second line: JxxxUK49
  - xxx: flash size
- Third line: xxxxxxxx
- Fourth line: xxxyyww
  - yyww: Date code with yy = year and ww = week.
- Fifth line: xxxxx
- Sixth line: NXP x[R]x
  - R = Chip revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
‘A’	Initial device revision.

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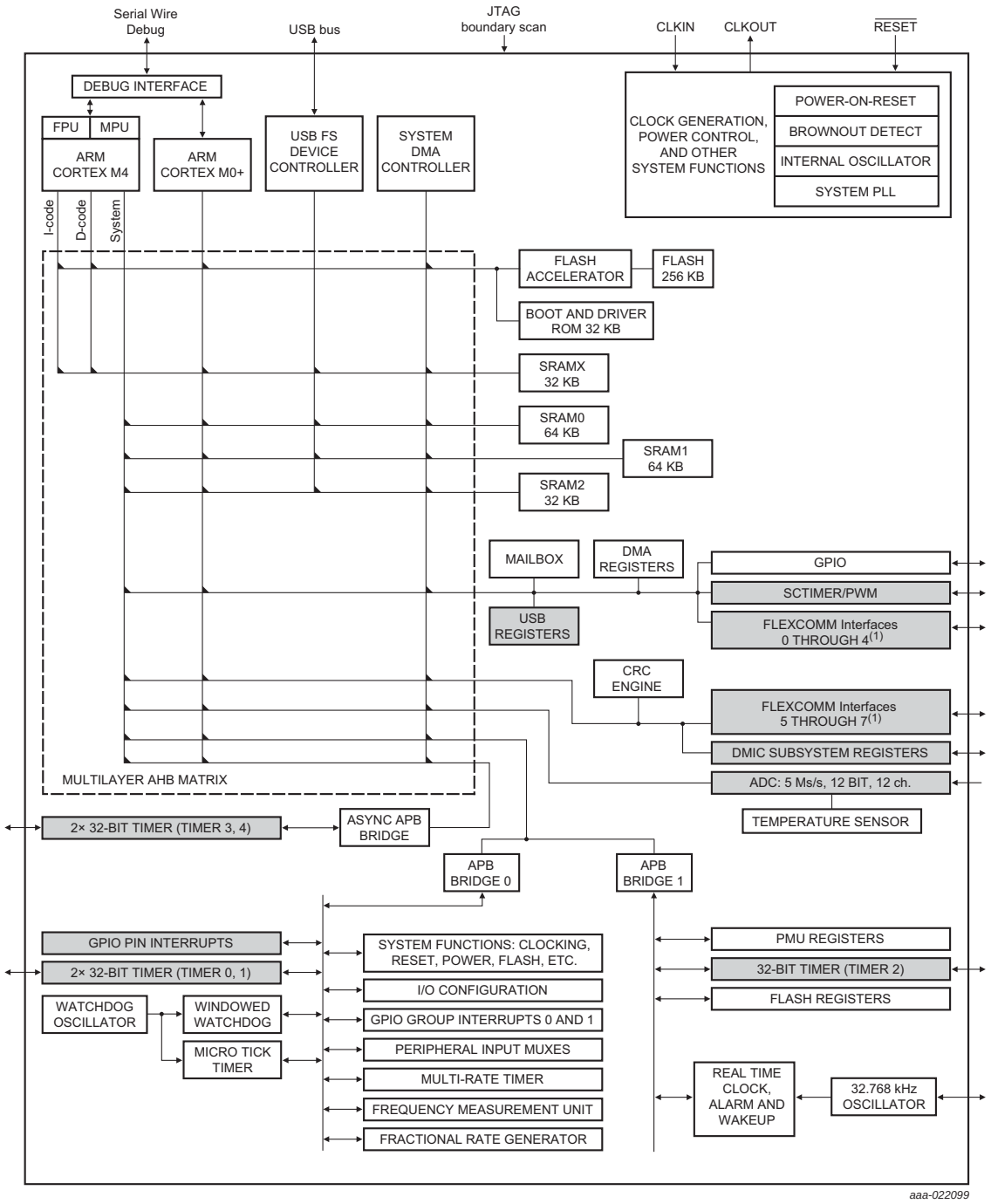
5. Block diagram



Each Flexcomm Interface includes USART, SPI, and I^{2}C functions. Flexcomm Interfaces 6 and 7 each also provide an I2S function. Grey-shaded blocks indicate peripherals that provide DMA requests or are otherwise able to trigger DMA transfers

Fig 3. LPC5411x Block diagram

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6. Pinning information

6.1 Pinning

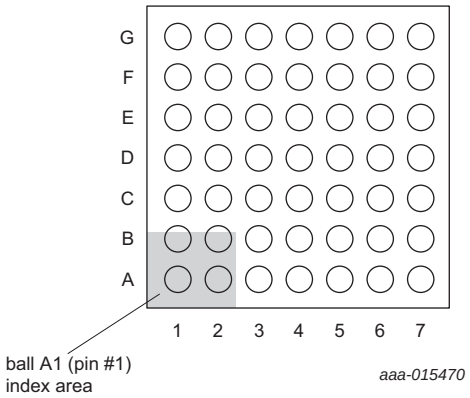

Fig 4. WLCSP49 Pin configuration

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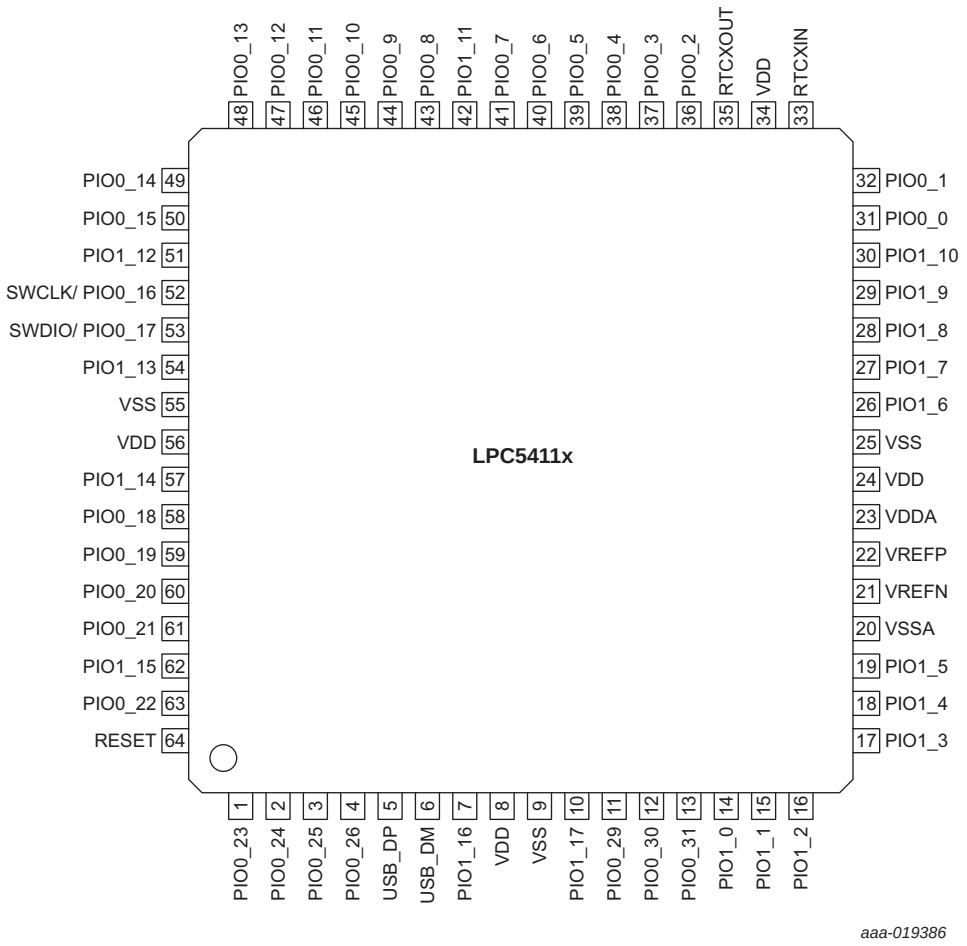

Fig 5. LQFP64 Pin configuration

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6.2 Pin description

On the LPC5411x, digital pins are grouped into two ports. Each digital pin may support up to four different digital functions and one analog function, including General Purpose I/O (GPIO).

Table 4. Pin description

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO0_0	A6	31	[2]	PU	I/O	**PIO0_0 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm Interface 0 USART RXD function.
					I/O	**FC0_RXD_SDA_MOSI —** Flexcomm Interface 0: USART RXD, I2C SDA, SPI MOSI.
					I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm Interface 3: USART CTS, I2C SDA, SPI SSEL0.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
						R — Reserved.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
PIO0_1	B6	32	[2]	PU	I/O	**PIO0_1 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm Interface 0 USART TXD function.
					I/O	**FC0_TXD_SCL_MISO —** Flexcomm Interface 0: USART TXD, I2C SCL, SPI MISO.
					I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm Interface 3: USART RTS, I2C SCL, SPI SSEL1.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
						R — Reserved.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
PIO0_2	-	36	[2]	PU	I/O	**PIO0_2 —** General-purpose digital input/output pin.
					I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm Interface 0: USART CTS, I2C SDA, SPI SSEL0.
					I/O	**FC3_SSEL3 —** Flexcomm Interface 3: SPI SSEL3.
					I	**CT32B2_CAP1 —** 32-bit CT32B2 capture input 1.
PIO0_3	-	37	[2]	PU	I/O	**PIO0_3 —** General-purpose digital input/output pin.
					I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm Interface 0: USART RTS, I2C SCL, SPI SSEL1.
					I/O	**FC2_SSEL2 —** Flexcomm Interface 2: SPI SSEL2.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
PIO0_4	C7	38	[2]	PU	I/O	**PIO0_4 —** General-purpose digital input/output pin. **Remark:** The state of this pin at Reset in conjunction with PIO0_31 and PIO1_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM10914 for more details.
					I/O	**FC0_SCK —** Flexcomm Interface 0: USART or SPI clock.
					I/O	**FC3_SSEL2 —** Flexcomm Interface 3: SPI SSEL2.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.

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Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO0_5	C6	39	[2]	PU	I/O	**PIO0_5 —** General-purpose digital input/output pin.
					I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm Interface 6: USART RXD, I2C SDA, SPI MOSI, I2S data.
					O	**SCT0_OUT6 —** SCT0 output 6. PWM output 6.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
PIO0_6	D7	40	[2]	PU	I/O	**PIO0_6 —** General-purpose digital input/output pin.
					I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm Interface 6: USART TXD, I2C SCL, SPI MISO, I2S WS.
						R — Reserved.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
						R — Reserved.
					I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
PIO0_7	D6	41	[2]	PU	I/O	**PIO0_7 —** General-purpose digital input/output pin.
					I/O	**FC6_SCK —** Flexcomm Interface 6: USART, SPI, or I2S clock.
					O	**SCT0_OUT0 —** SCT0 output 0. PWM output 0.
					O	**CT32B0_MAT2 —** 32-bit CT32B0 match output 2.
						R — Reserved.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
PIO0_8	D5	43	[2]	PU	I/O	**PIO0_8 —** General-purpose digital input/output pin.
					I/O	**FC2_RXD_SDA_MOSI —** Flexcomm Interface 2: USART RXD, I2C SDA, SPI MOSI.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
PIO0_9	E7	44	[2]	PU	I/O	**PIO0_9 —** General-purpose digital input/output pin.
					I/O	**FC2_TXD_SCL_MISO —** Flexcomm Interface 2: USART TXD, I2C SCL, SPI MISO.
					O	**SCT0_OUT2 —** SCT0 output 2. PWM output 2.
					I	**CT32B3_CAP0 —** 32-bit CT32B3 capture input 0.
						R — Reserved.
					I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm Interface 3: USART CTS, I2C SDA, SPI SSEL0.
PIO0_10	E6	45	[2]	PU	I/O	**PIO0_10 —** General-purpose digital input/output pin.
					I/O	**FC2_SCK —** Flexcomm Interface 2: USART or SPI clock.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
					O	**CT32B3_MAT0 —** 32-bit CT32B3 match output 0.
PIO0_11	E5	46	[2]	PU	I/O	**PIO0_11 —** General-purpose digital input/output pin.
					I/O	**FC3_SCK —** Flexcomm Interface 3: USART or SPI clock.
					I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm Interface 6: USART RXD, I2C SDA, SPI MOSI, I2S DATA.
					O	**CT32B2_MAT1 —** 32-bit CT32B2 match output 1.

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Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO0_12	F7	47	[2]	PU	I/O	**PIO0_12 —** General-purpose digital input/output pin.
					I/O	**FC3_RXD_SDA_MOSI —** Flexcomm Interface 3: USART RXD, I2C SDA, SPI MOSI.
					I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm Interface 6: USART TXD, I2C SCL, SPI MISO, I2S WS.
					O	**CT32B2_MAT3 —** 32-bit CT32B2 match output 3.
PIO0_13	G7	48	[2]	PU	I/O	**PIO0_13 —** General-purpose digital input/output pin.
					I/O	**FC3_TXD_SCL_MISO —** Flexcomm Interface 3: USART TXD, I2C SCL, SPI MISO.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
PIO0_14/ TCK	F6	49	[2]	PU	I/O	**PIO0_14 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock In).
					I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm Interface 3: USART CTS, I2C SDA, SPI SSEL0.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					O	**CT32B2_MAT1 —** 32-bit CT32B2 match output 1.
						R — Reserved.
					I/O	**FC1_SCK —** Flexcomm Interface 1: USART or SPI clock.
PIO0_15/ TDO	G6	50	[2]	PU	I/O	**PIO0_15 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out).
					I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm Interface 3: USART RTS, I2C SCL, SPI SSEL1.
					I/O	**SWO —** Serial wire trace output.
					O	**CT32B2_MAT2 —** 32-bit CT32B2 match output 2.
						R — Reserved.
					I/O	**FC4_SCK —** Flexcomm Interface 4: USART or SPI clock.
SWCLK/ PIO0_16	F5	52	[2]	PU	I/O	**PIO0_16 —** General-purpose digital input/output pin.
					I/O	**FC3_SSEL2 —** Flexcomm Interface 3: SPI SSEL2.
					I/O	**FC6_CTS_SDA_SSEL0 —** Flexcomm Interface 6: USART CTS, I2C SDA, SPI SSEL0.
					O	**CT32B3_MAT1 —** 32-bit CT32B3 match output 1.
						R — Reserved.
					I/O	**SWCLK —** Serial Wire Clock. JTAG Test Clock. This is the default function after booting.
						R — Reserved.

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Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
SWDIO/ PIO0_17	G5	53	[2]	PU	I/O	**PIO0_17 —** General-purpose digital input/output pin.
					I/O	**FC3_SSEL3 —** Flexcomm Interface 3: SPI SSEL3.
					I/O	**FC6_RTS_SCL_SSEL1 —** Flexcomm Interface 6: USART RTS, I2C SCL, SPI SSEL1.
					O	**CT32B3_MAT2 —** 32-bit CT32B3 match output 2.
						R — Reserved.
					I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.
PIO0_18/ $\overline{\text{TRST}}$	G4	58	[2]	PU	I/O	**PIO0_18 —** General-purpose digital input/output pin. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset).
					I/O	**FC5_TXD_SCL_MISO —** Flexcomm Interface 5: USART TXD, I2C SCL, SPI MISO.
					O	**SCT0_OUT0 —** SCT0 output 0. PWM output 0.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
PIO0_19/ TDI	G3	59	[2]	PU	I/O	**PIO0_19 —** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In).
					I/O	**FC5_SCK —** Flexcomm Interface 5: USART or SPI clock.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
PIO0_20/ TMS	F3	60	[2]	PU	I/O	**PIO0_20 —** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select).
					I/O	**FC5_RXD_SDA_MOSI —** Flexcomm Interface 5: USART RXD, I2C SDA, SPI MOSI.
					I/O	**FC0_SCK —** Flexcomm Interface 0: USART or SPI clock.
					I	**CT32B3_CAP0 —** 32-bit CT32B3 capture input 0.
PIO0_21	E3	61	[2]	PU	I/O	**PIO0_21 —** General-purpose digital input/output pin.
					O	**CLKOUT —** Clock output.
					I/O	**FC0_TXD_SCL_MISO —** Flexcomm Interface 0: USART TXD, I2C SCL, SPI MISO.
					O	**CT32B3_MAT0 —** 32-bit CT32B3 match output 0.
PIO0_22	G2	63	[2]	PU	I/O	**PIO0_22 —** General-purpose digital input/output pin.
					I	**CLKIN —** Clock input.
					I/O	**FC0_RXD_SDA_MOSI —** Flexcomm Interface 0: USART RXD, I2C SDA, SPI MOSI.
					O	**CT32B3_MAT3 —** 32-bit CT32B3 match output 3.
PIO0_23	F2	1	[3]	Z	I/O	**PIO0_23 —** General-purpose digital input/output pin.
					I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm Interface 1: USART CTS, I2C SCL, SPI SSEL1.
						R — Reserved.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
						R — Reserved.
					I	**UTICK_CAP1 —** Micro-tick timer capture input 1.

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Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO0_24	F1	2	[3]	Z	I/O	**PIO0_24 —** General-purpose digital input/output pin.
					I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm Interface 1: USART CTS, I2C SDA, SPI SSEL0.
						R — Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
						R — Reserved.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
PIO0_25	E2	3	[3]	Z	I/O	**PIO0_25 —** General-purpose digital input/output pin.
					I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm Interface 4: USART CTS, I2C SCL, SPI SSEL1.
					I/O	**FC6_CTS_SDA_SSEL0 —** Flexcomm Interface 6: USART CTS, I2C SDA, SPI SSEL0.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
						R — Reserved.
					I	**CT32B1_CAP1 —** 32-bit CT32B1 capture input 1.
PIO0_26	E1	4	[3]	Z	I/O	**PIO0_26 —** General-purpose digital input/output pin.
					I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm Interface 4: USART CTS, I2C SDA, SPI SSEL0.
						R — Reserved.
					I	**CT32B0_CAP3 —** 32-bit CT32B0 capture input 3.
PIO0_29/ ADC0_0	D3	11	[4]	PU	I/O; AI	**PIO0_29/ADC0_0 —** General-purpose digital input/output pin. ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I/O	**FC1_RXD_SDA_MOSI —** Flexcomm Interface 1: USART RXD, I2C SDA, SPI MOSI.
					O	**SCT0_OUT2 —** SCT0 output 2. PWM output 2.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
						R — Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
						R — Reserved.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
PIO0_30/ ADC0_1	C1	12	[4]	PU	I/O; AI	**PIO0_30/ADC0_1 —** General-purpose digital input/output pin. ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I/O	**FC1_TXD_SCL_MISO —** Flexcomm Interface 1: USART TXD, I2C SCL, SPI MISO.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
					O	**CT32B0_MAT2 —** 32-bit CT32B0 match output 2.
						R — Reserved.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.

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Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO0_31/ ADC0_2	C2	13	[4]	PU	I/O; AI	**PIO0_31/ADC0_2 —** General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin. **Remark:** This pin is also used to invoke ISP mode after device reset. Secondary selection of boot source for ISP mode also uses PIO0_4 and PIO1_6.
					O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
					I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm Interface 2: USART CTS, I2C SDA, SPI SSEL0.
					I	**CT32B2_CAP2 —** 32-bit CT32B2 capture input 2.
						R — Reserved.
					I	**CT32B0_CAP3 —** 32-bit CT32B0 capture input 3.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
PIO1_0/ ADC0_3	C3	14	[4]	PU	I/O; AI	**PIO1_0/ADC0_3 —** General-purpose digital input/output pin. ADC input channel 3 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I	**PDM0_DATA —** Data for PDM interface 0, digital microphone input.
					I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm Interface 2: USART RTS, I2C SCL, SPI SSEL1.
					O	**CT32B3_MAT1 —** 32-bit CT32B3 match output 1.
						R — Reserved.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
PIO1_1/ ADC0_4	B1	15	[4]	PU	I/O; AI	**PIO1_1/ADC0_4 —** General-purpose digital input/output pin. ADC input channel 4 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
						R — Reserved.
					I/O	**SWO —** Serial wire trace output.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					I/O	**FC5_SSEL2 —** Flexcomm Interface 5: SPI SSEL2.
					I/O	**FC4_TXD_SCL_MISO —** Flexcomm Interface 4: USART TXD, I2C SCL, SPI MISO.
PIO1_2/ ADC0_5	A1	16	[4]	PU	I/O; AI	**PIO1_2/ADC0_5 —** General-purpose digital input/output pin. ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
					I/O	**FC7_SSEL3 —** Flexcomm Interface 7: SPI SSEL3.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					I/O	**FC5_SSEL3 —** Flexcomm Interface 5: SPI SSEL3.
					I/O	**FC4_RXD_SDA_MOSI —** Flexcomm Interface 4: USART RXD, I2C SDA, SPI MOSI.

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Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO1_3/ ADC0_6	B2	17	[4]	PU	I/O; AI	**PIO1_3/ADC0_6 —** General-purpose digital input/output pin. ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
						R — Reserved.
					I/O	**FC7_SSEL2 —** Flexcomm Interface 7: SPI SSEL2.
					O	**SCT0_OUT6 —** SCT0 output 6. PWM output 6.
						R — Reserved.
					I/O	**FC3_SCK —** Flexcomm Interface 3: USART or SPI clock.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					O	**USB_UP_LED —** USB port 2 GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled). It is HIGH when the device is not configured or during global suspend.
PIO1_4/ ADC0_7	A2	18	[4]	PU	I/O; AI	**PIO1_4/ADC0_7 —** General-purpose digital input/output pin. ADC input channel 7 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
					I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm Interface 7: USART RTS, I2C SCL, SPI SSEL1.
					O	**SCT0_OUT7 —** SCT0 output 7. PWM output 7.
						R — Reserved.
					I/O	**FC3_TXD_SCL_MISO —** Flexcomm Interface 3: USART TXD, I2C SCL, SPI MISO.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
PIO1_5/ ADC0_8	B3	19	[4]	PU	I/O; AI	**PIO1_5/ADC0_8 —** General-purpose digital input/output pin. ADC input channel 8 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I	**PDM1_DATA —** Data for PDM interface 1, digital microphone input. Also PDM clock input in bypass mode.
					I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm Interface 7: USART CTS, I2C SDA, SPI SSEL0.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
						R — Reserved.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
						R — Reserved.
					O	**USB_FRAME —** USB start-of-frame signal derived from host signaling.

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Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO1_6/ ADC0_9	A5	26	[4]	PU	I/O; AI	**PIO1_6/ADC0_9 —** General-purpose digital input/output pin. ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin. **Remark:** This pin is also used as part of secondary selection of boot source for ISP mode after device reset, in connection with PIO0_31 and PIO0_4.
						R — Reserved.
					I/O	**FC7_SCK —** Flexcomm Interface 7: USART, SPI, or I2S clock.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
						R — Reserved.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
						R — Reserved.
					I	**USB_VBUS —** Monitors the presence of USB bus power. This signal must be HIGH for USB reset to occur.
PIO1_7/ ADC0_10	B5	27	[4]	PU	I/O; AI	**PIO1_7/ADC0_10 —** General-purpose digital input/output pin. ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
						R — Reserved.
					I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm Interface 7: USART RXD, I2C SDA, SPI MOSI, I2S DATA.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
						R — Reserved.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
PIO1_8/ ADC0_11	C5	28	[4]	PU	I/O; AI	**PIO1_8/ADC0_11 —** General-purpose digital input/output pin. ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
						R — Reserved.
					I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm Interface 7: USART TXD, I2C SCL, SPI MISO, I2S WS.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
						R — Reserved.
					I	**CT32B1_CAP3 —** 32-bit CT32B1 capture input 3.
PIO1_9	-	29	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC3_RXD_SDA_MOSI —** Flexcomm Interface 3: USART RXD, I2C SDA, SPI MOSI.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
						R — Reserved.
						R — Reserved.
					O	**USB_UP_LED —** USB port 2 GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled). It is HIGH when the device is not configured or during global suspend.

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Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO1_10	-	30	[2]	PU	I/O	**PIO1_10 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm Interface 6: USART TXD, I2C SCL, SPI MISO, I2S WS.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					I/O	**FC1_SCK —** Flexcomm Interface 1: USART or SPI clock.
						R — Reserved.
						R — Reserved.
					I	**USB_FRAME —** USB start-of-frame signal derived from host signaling.
PIO1_11	-	42	[2]	PU	I/O	**PIO1_11 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC6_RTS_SCL_SSEL1 —** Flexcomm Interface 6: USART RTS, I2C SCL, SPI SSEL1.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
					I/O	**FC4_SCK —** Flexcomm Interface 4: USART or SPI clock.
						R — Reserved.
						R — Reserved.
					I	**USB_VBUS —** Monitors the presence of USB bus power. This signal must be HIGH for USB reset to occur.
PIO1_12	-	51	[2]	PU	I/O	**PIO1_12 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC5_RXD_SDA_MOSI —** Flexcomm Interface 5: USART RXD, I2C SDA, SPI MOSI.
					O	**CT32B1_MAT0 —** 32-bit CT32B1 match output 0.
					I/O	**FC7_SCK —** Flexcomm Interface 7: USART, SPI, or I2S clock.
					I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
PIO1_13	-	54	[2]	PU	I/O	**PIO1_13 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC5_TXD_SCL_MISO —** Flexcomm Interface 5: USART TXD, I2C SCL, SPI MISO.
					O	**CT32B1_MAT1 —** 32-bit CT32B1 match output 1.
					I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm Interface 7: USART RXD, I2C SDA, SPI MOSI, I2S DATA.
PIO1_14	-	57	[2]	PU	I/O	**PIO1_14 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC2_RXD_SDA_MOSI —** Flexcomm Interface 2: USART RXD, I2C SDA, SPI MOSI.
					O	**SCT0_OUT7 —** SCT0 output 7. PWM output 7.
					I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm Interface 7: USART TXD, I2C SCL, SPI MISO, I2S WS.

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Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO1_15	-	62	[2]	PU	I/O	**PIO1_15 —** General-purpose digital input/output pin.
					O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					I	**CT32B1_CAP3 —** 32-bit CT32B1 capture input 3.
					I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm Interface 7: USART CTS, I2C SDA, SPI SSEL0.
PIO1_16	-	7	[2]	PU	I/O	**PIO1_16 —** General-purpose digital input/output pin.
					I	**PDM0_DATA —** Data for PDM interface 0, digital microphone input.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
					I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm Interface 7: USART RTS, I2C SCL, SPI SSEL1.
PIO1_17	-	10	[2]	PU	I/O	**PIO1_17 —** General-purpose digital input/output pin.
						R — Reserved.
						R — Reserved.
						R — Reserved.
					I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
					I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
USB_DP	D2	5	[6]	F	I/O	USB0 bidirectional D+ line.
USB_DM	D1	6	[6]	F	I/O	USB0 bidirectional D- line.
RESETN	G1	64	[5]	PU	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. Wakes up the part from deep power-down mode.
RTCXIN	A7	33		-	-	RTC oscillator input.
RTCXOUT	B7	35		-	-	RTC oscillator output.
VREFP	B4	22		-	-	ADC positive reference voltage.
VREFN	-	21		-	-	ADC negative reference voltage.
V_{DDA}	A4	23		-	-	Analog supply voltage.
V_{DD}	C4, F4	8, 24, 34, 56		-	-	Single 1.62 V to 3.6 V power supply powers internal digital functions and I/Os.
V_{SS}	D4, E4	9, 25, 55		-	-	Ground.
VSSA	A3	20		-	-	Analog ground.

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

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[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 30. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

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6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP	-	Tie to V_{DD}.
VREFN	-	Tie to V_{SS}.
V_{DDA}	-	Tie to V_{DD}.
V_{SSA}	-	Tie to V_{SS}.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up enabled

6.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_23 to PIO0_28 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled. Reset function disabled.			

[1] Default and programmed pin states are retained in sleep and deep-sleep modes.

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7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses, one system bus and the I-code and D-code buses. One bus is dedicated for instruction fetch (I-code), and one bus is dedicated for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

The LPC5411x uses a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M4 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

7.3 ARM Cortex-M4 integrated Floating Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

7.4 ARM Cortex-M0+ co-processor

The ARM Cortex-M0+ co-processor offers high performance and very low power consumption. This processor uses a 2-stage pipeline von Neumann architecture and a small but powerful instruction set providing high-end processing hardware. The processor includes a single-cycle multiplier, an NVIC with 32 interrupts, and a separate system tick timer.

7.5 Memory Protection Unit (MPU)

The Cortex-M4 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

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The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

7.6 Nested Vectored Interrupt Controller (NVIC) for Cortex-M4

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- 40 vectored interrupt slots.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table using Vector Table Offset Register (VTOR).
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.7 Nested Vectored Interrupt Controller (NVIC) for Cortex-M0+

The NVIC is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.7.1 Features

- Controls system exceptions and peripheral interrupts.
- 32 vectored interrupt slots.
- Four programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table using VTOR.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

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7.8 System Tick timer (SysTick)

The ARM Cortex-M4 and ARM Cortex-M0+ cores include a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the system clock or the SYSTICK clock.

7.9 On-chip static RAM

The LPC5411x supports up to192 KB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.10 On-chip flash

The LPC5411x supports up to 256 KB of on-chip flash memory.

7.11 On-chip ROM

The 32 KB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming.
- ROM-based USB drivers (HID, CDC, and MSC).Flash updates via USB is supported.
- Supports booting from valid user code in flash, USART, SPI, and I^2C.
- Dual image boot.

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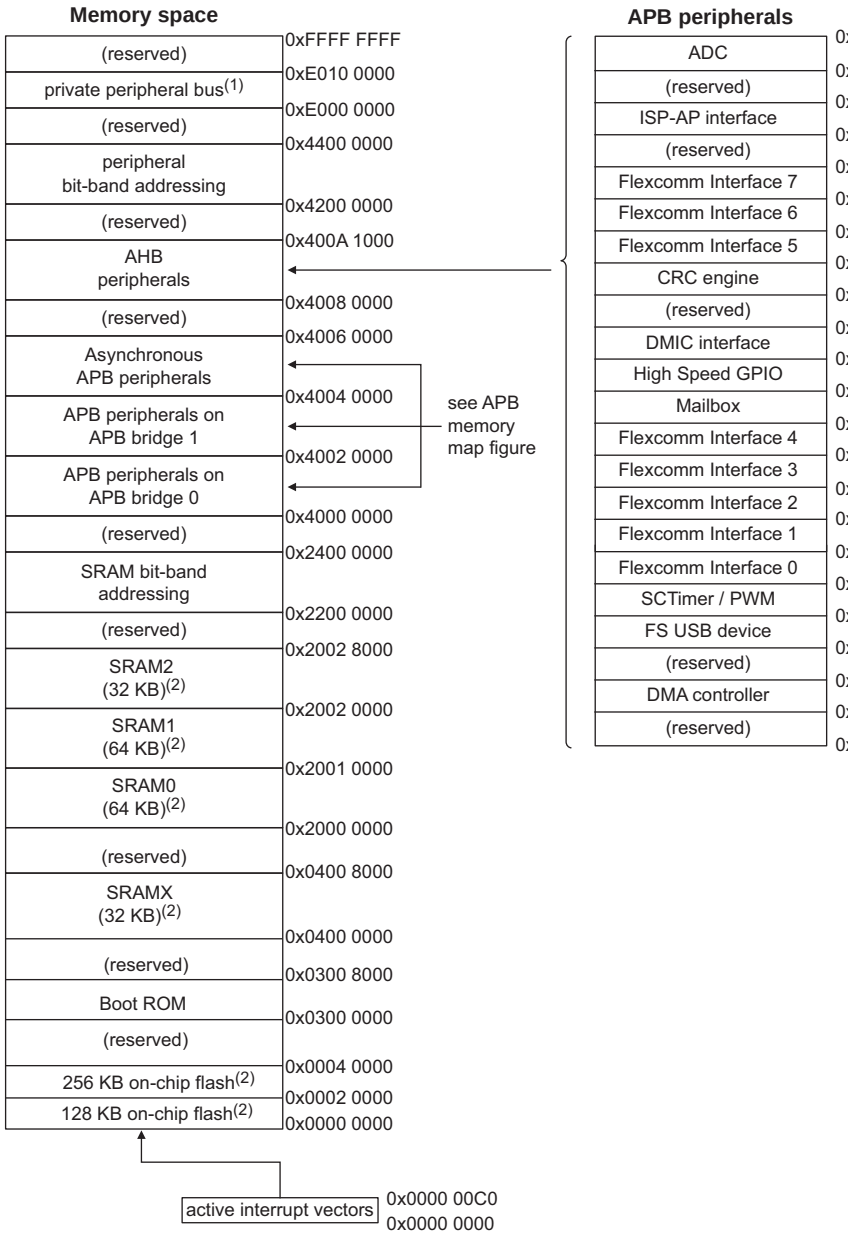
7.12 Memory mapping

The LPC5411x incorporates several distinct memory regions. The APB peripheral area is 64 KB in size and is divided to allow for up to 32 peripherals. Each peripheral is allocated 4 KB of space simplifying the address decoding.

Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset.



[1] The private peripheral bus includes CPU peripherals such as the NVIC, SysTick, and the core control registers.

[2] The total size of flash and SRAM is part dependent. See Table 1 on page 5.

Fig 6. LPC5411x Memory mapping

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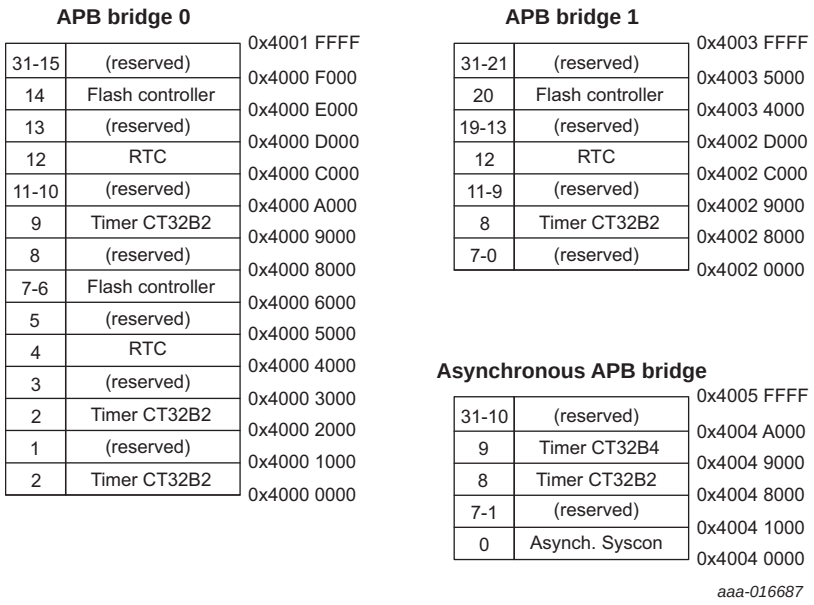

Fig 7. LPC5411x APB Memory map

7.13 Power control

The LPC5411x support a variety of power control features. In Active mode, when the chip is running, power and clocks to selected peripherals can be adjusted for power consumption. In addition, there are four special modes of processor power reduction with different peripherals running: sleep mode, deep-sleep mode, and deep power-down mode, activated by the power mode configure API.

7.13.1 Sleep mode

In sleep mode, the system clock to the CPU is stopped and execution of instructions is suspended until either a reset or an interrupt occurs. Peripheral functions, if selected to be clocked can continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

7.13.2 Deep-sleep mode

In deep-sleep mode, all peripheral clocks and all clock sources are off with the option of keeping the 32.768 kHz clock, and the WDTOSC running. In addition, all analog blocks and the flash are shut down. In deep-sleep mode, the application can keep the BOD circuit running for BOD protection.

The LPC5411x can wake up from deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer reset interrupt, BOD interrupt/reset, or an interrupt from the USART (in 32.768 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals. For wake-up from deep-sleep mode, the SPI, USART, and I2C peripherals must be configured in slave mode.

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In deep-sleep mode, the processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static. Deep-sleep mode reduces power consumption compared to deep-sleep mode at the expense of longer wake-up times.

7.13.3 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the RTC power domain and the $\overline{\text{RESET}}$ pin. The LPC5411x can wake up from deep power-down mode via the $\overline{\text{RESET}}$ pin and the RTC alarm. The ALARM1HZ flag in RTC control register generates an RTC wake-up interrupt request, which can wake up the part. During deep power-down mode, the contents of the SRAM and registers are not retained. All functional pins are tri-stated in deep power-down mode.

Table 7 shows the peripheral configuration in reduced power modes.

Table 7. Peripheral configuration in reduced power modes

Peripheral	Sleep mode	Deep power- down mode
FRO	Software configured	Off
Flash	Software configured	Off
BOD	Software configured	Off
PLL	Software configured	Off
Watchdog osc and WWDT	Software configured	Off
USART	Software configured	Off
SPI	Software configured	Off
I2C	Software configured	Off
Other digital peripherals	Software configured	Off
Analog peripherals	Software configured	Off
RTC oscillator	Software configured	Software configured

7.14 General Purpose I/O (GPIO)

The LPC5411x provides two GPIO ports with a total of 48 GPIO pins.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

See Table 4 for the default state on reset.

7.14.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.

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- Bit-level set, clear, and toggle registers allow a single instruction set, clear or toggle of any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request.
- One GPIO group interrupt can be triggered by a combination of any pin or pins.

7.15 Pin interrupt/pattern engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC. The pattern match engine can be used in conjunction with software to create complex state machines based on pin inputs. Any digital pin, independent of the function selected through the switch matrix can be configured through the SYSCON block as an input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the I/O+ bus for fast single-cycle access.

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7.15.1 Features

- Pin interrupts:
  - Up to eight pins can be selected from all GPIO pins on ports 0 and 1 as edge-sensitive or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Pin interrupts can wake up the device from sleep mode and deep-sleep mode.
- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake-up only from active and sleep modes.

7.16 AHB peripherals

7.16.1 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.16.1.1 Features

- 20 channels, 19 of which are connected to peripheral DMA requests. These come from the Flexcomm Interfaces (USART, SPI, I^2C, and I2S) and digital microphone interfaces.
- DMA operations can be triggered by on-chip or off-chip events.
- Priority is user selectable for each channel (up to eight priority levels).
- Continuous priority arbitration.
- Address cache with four entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

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7.17 Digital serial peripherals

7.17.1 USB 2.0 device controller

7.17.1.1 Features

- USB2.0 full-speed device controller.
- Supports ten physical (five logical) endpoints including one control endpoint.
- Supports Single and double-buffering.
- Supports Crystal-less operation and calibration of FRO using USB frames.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Link Power Management (LPM) supported.

7.17.2 DMIC subsystem

7.17.2.1 Features

- Pulse-Density Modulation (PDM) data input for left and/or right channels on 1 or 2 buses.
- Flexible decimation.
- 16 entry FIFO for each channel.
- DC blocking or unaltered DC bias can be selected.
- Data can be transferred using DMA from deep-sleep mode without waking up the CPU, then automatically returning to deep-sleep mode.
- Data can be streamed directly to I^2S on Flexcomm Interface 7.

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7.17.3 Flexcomm Interface serial communication

Each Flexcomm Interface provides a choice of peripheral functions, one of which the user must choose before the function can be configured and used.

7.17.3.1 Features

- USART with asynchronous operation or synchronous master or slave operation.
- SPI master or slave, with up to four slave selects.
- I^2C, including separate master, slave, and monitor functions.
- Flexcomm Interfaces 6 and 7 support I^2S function.
- Data for USART, SPI, and I^2S traffic uses the Flexcomm Interface FIFO. The I^2C function does not use the FIFO.

7.17.4 USART

7.17.4.1 Features

- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Maximum bit rates of 1.875 Mbit/s in asynchronous mode.
- Maximum data rates of 10 Mbit/s in synchronous master and slave modes for USART functions.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection.
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register.
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for FIFO receive level reached, FIFO transmit level reached, Transmit Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep mode.
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

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- Activity on the USART synchronous slave mode allows wake-up from deep-sleep mode on any enabled interrupt

7.17.5 SPI serial I/O controller

7.17.5.1 Features

- Master and slave operation.
- Maximum data rates of 50 Mbit/s in master mode for SPI functions.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software or DMA set-up.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- Four Slave Select input/outputs with selectable polarity and flexible usage.
- Activity on the SPI in slave mode allows wake-up from deep-sleep mode on any enabled interrupt.

7.17.6 I^2C-bus interface

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.17.7 Features

- Independent Master, Slave, and Monitor functions.
- Bus speeds supported:
  - Standard mode, up to 100 kbits/s.
  - Fast-mode, up to 400 kbits/s.
  - Fast-mode Plus, up to 1 Mbits/s (on specific I^2C pins).
  - High speed mode, 3.4 Mbits/s as a Slave only (on specific I^2C pins).
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C bus addresses.
- 10-bit addressing supported with software assist.
- Supports System Management Bus (SMBus).
- Separate DMA requests for Master, Slave, and Monitor functions.
- No chip clocks are required in order to receive and compare an address as a Slave, so this event can wake up the device from deep-sleep mode.

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7.17.8 I²S-bus interface

The I²S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I²S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select/frame trigger signal, providing single or dual (mono or stereo) audio data transfer as well as other configurations. In the LPC5411x, the I²S function is included in Flexcomm Interface 6 and Flexcomm Interface 7. Each of these Flexcomm Interfaces implement four I²S channel pairs.

The I²S interface within one Flexcomm Interface provides at least one channel pair that can be configured as a master or a slave. Other channel pairs, if present, always operate as slaves. All of the channel pairs within one Flexcomm Interface share one set of I²S signals, and are configured together for either transmit or receive operation, using the same mode, same data configuration and frame configuration. All such channel pairs can participate in a time division multiplexing (TDM) arrangement. For cases requiring an MCLK input and/or output, this is handled outside of the I²S block in the system level clocking scheme.

7.17.8.1 Features

- A Flexcomm Interface may implement one or more I²S channel pairs, the first of which could be a master or a slave, and the rest of which would be slaves. All channel pairs are configured together for either transmit or receive and other shared attributes. The number of channel pairs is defined for each Flexcomm Interface, and may be from 0 to 4.
- Configurable data size for all channels within one Flexcomm Interface, from 4 bits to 32 bits. Each channel pair can also be configured independently to act as a single channel (mono as opposed to stereo operation).
- All channel pairs within one Flexcomm Interface share a single bit clock (SCK) and word select/frame trigger (WS), and data line (SDA).
- Data for all I²S traffic within one Flexcomm Interface uses the Flexcomm Interface FIFO. The FIFO depth is 8 entries.
- Left justified and right justified data modes.
- DMA support using FIFO level triggering.
- TDM (Time Division Multiplexing) with a several stereo slots and/or mono slots is supported. Each channel pair can act as any data slot. Multiple channel pairs can participate as different slots on one TDM data line.
- The bit clock and WS can be selectively inverted.
- Sampling frequencies supported depends on the specific device configuration and applications constraints (e.g. system clock frequency, PLL availability, etc.) but generally supports standard audio data rates.

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7.18 Standard counter/timers (CT32B0 to 4)

The LPC5411x includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.18.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to four 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs per timer corresponding to match registers with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.
- PWM mode using up to three match channels for PWM output.

7.18.2 SCTimer/PWM subsystem

The SCTimer/PWM is a flexible timer module capable of creating complex PWM waveforms and performing other advanced timing and control operations with minimal or no CPU intervention.

The SCTimer/PWM can operate as a single 32-bit counter or as two independent, 16-bit counters in uni-directional or bi-directional mode. It supports a selection of match registers against which the count value can be compared, and capture registers where the current count value can be recorded when some pre-defined condition is detected.

The SCTimer/PWM module supports multiple separate events that can be defined by the user based on some combination of parameters including a match on one of the match registers, and/or a transition on one of the SCTimer/PWM inputs or outputs, the direction of count, and other factors.

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Every action that the SCTimer/PWM block can perform occurs in direct response to one of these user-defined events without any software overhead. Any event can be enabled to:

- Start, stop, or halt the counter.
- Limit the counter which means to clear the counter in unidirectional mode or change its direction in bi-directional mode.
- Set, clear, or toggle any SCTimer/PWM output.
- Force a capture of the count value into any capture registers.
- Generate an interrupt of DMA request.

7.18.2.1 Features

- The SCTimer/PWM Supports:
  - Eight inputs.
  - Eight outputs.
  - Ten match/capture registers.
  - Ten events.
  - Ten states.
- Counter/timer features:
  - Each SCTimer/PWM is configurable as two 16-bit counters or one 32-bit counter.
  - Counters clocked by system clock or selected input.
  - Configurable number of match and capture registers. Up to five match and capture registers total.
  - Ten events.
  - Ten states.
  - Upon match and/or an input or output transition create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs; change the state.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.

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- PWM features:
  - Counters can be used in conjunction with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to eight single-edge or four dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as an rising or falling edge or level, a combination of match and/or input/output condition.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.

7.18.3 Windowed WatchDog Timer (WWDT)

The purpose of the Watchdog Timer is to reset or interrupt the microcontroller within a programmable time if it enters an erroneous state. When enabled, a watchdog reset is generated if the user program fails to feed (reload) the Watchdog within a predetermined amount of time.

7.18.3.1 Features

- Internally resets chip if not reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Programmable 24-bit timer with internal fixed pre-scaler.
- Selectable time period from 1,024 watchdog clocks ($T_{WDCLK} \times 256 \times 4$) to over 67 million watchdog clocks ($T_{WDCLK} \times 2^{24} \times 4$) in increments of four watchdog clocks.
- “Safe” watchdog operation. Once enabled, requires a hardware reset or a Watchdog reset to be disabled.
- Incorrect feed sequence causes immediate watchdog event if enabled.
- The watchdog reload value can optionally be protected such that it can only be changed after the “warning interrupt” time is reached.
- Flag to indicate Watchdog reset.

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- The Watchdog clock (WDCLK) source is a selectable frequency in the range of 200 kHz to 1.5 MHz. The accuracy of this clock is limited to +/- 40% over temperature, voltage, and silicon processing variations.
- The Watchdog timer can be configured to run in deep-sleep mode.
- Debug mode.

7.18.4 RTC timer

The RTC block has two timers: main RTC timer, and high-resolution/wake-up timer. The main RTC timer is a 32-bit timer that uses a 1 Hz clock and is intended to run continuously as a real-time clock. When the timer value reaches a match value, an interrupt is raised. The alarm interrupt can also wake up the part from any low power mode, if enabled.

The high-resolution or wake-up timer is a 16-bit timer that uses a 1 kHz clock and operates as a one-shot down timer. When the timer is loaded, it starts counting down to 0 at which point an interrupt is raised. The interrupt can be used to wake-up the part from any low power modes. This timer is intended to be used for timed wake-up from deep-sleep or deep power-down modes. The high-resolution wake-up timer can be disabled to conserve power if not used.

The RTC timer uses the 32.768 kHz clock input to create a 1 Hz or 1 kHz clock.

7.18.4.1 Features

- The RTC oscillator has the following clock outputs:
  - 32.768 kHz clock, selectable for system clock and CLKOUT pin.
  - 1 Hz clock for RTC timing.
  - 1 kHz clock for high-resolution RTC timing.
- 32-bit, 1 Hz RTC counter and associated match register for alarm generation.
- Separate 16-bit high-resolution/wake-up timer clocked at 1 kHz for 1 ms resolution with a more that one minute maximum time-out period.
- RTC alarm and high-resolution/wake-up timer time-out each generate independent interrupt requests. Either time-out can wake up the part from any of the low power modes, including deep power-down.

7.18.5 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

7.18.5.1 Features

- 24-bit interrupt timer.
- Four channels independently counting down from individually set values.
- Repeat interrupt, one-shot interrupt, and one-shot bus stall modes.

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7.18.6 Micro-tick timer (UTICK)

The ultra-low power Micro-tick Timer, running from the Watchdog oscillator, can be used to wake up the device from low power modes.

7.18.6.1 Features

- Ultra simple timer.
- Write once to start.
- Interrupt or software polling.
- Four capture registers that can be triggered by external pin transitions.

7.19 12-bit Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12-bit and fast conversion rates of up to 5.0 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCTimer/PWM, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCTimer/PWM inputs for tight timing control between the ADC and the SCTimer/PWM.

7.19.1 Features

- 12-bit successive approximation analog to digital converter.
- Input multiplexing up to 12 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Measurement range V_{REFN} to V_{REFP} (not to exceed V_{DDA} voltage level).
- 12-bit conversion rate of 5.0 MHz. Options for reduced resolution at higher conversion rates.
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.
- A temperature sensor is connected as an alternative input for ADC channel 0.

7.20 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a Complement To Absolute Temperature (V_{CTAT}) voltage. The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

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For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

7.21 System control

7.21.1 Clock sources

The LPC5411x supports two external and three internal clock sources:

- The Free Running Oscillator (FRO).
- Watchdog oscillator (WDTOSC).
- External clock source from the digital I/O pin CLKIN.
- External RTC 32.768 kHz clock.
- Output of the system PLL.

7.21.1.1 FRO

The internal FRO can be used as a CPU clock or a clock source to the system PLL. On power-up, or any chip reset, the LPC5411x uses an internal 12 MHz FRO as the clock source. Software may later switch to one of the available clock sources. A selectable 48 MHz or 96 MHz FRO is also available as a clock source.

The 48 MHz FRO can be used as a clock source to the USB.

The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.

7.21.1.2 Watchdog oscillator (WDTOSC)

The watchdog oscillator is a low-power internal oscillator. The WDTOSC can be used to provide a clock to the WWDT and to the entire chip. The watchdog oscillator has a selectable frequency in the range of 200 kHz to 1.5 MHz.

7.21.1.3 Clock input

An external square-wave clock source (up to 25 MHz) can be supplied on the digital I/O pin CLKIN.

7.21.1.4 RTC Oscillator

An external RTC (32.768 kHz) can be used to create the main clock when the PLL input or output is selected as the clock source to the main clock.

7.21.1.5 System PLL

The system PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency external clock. The system PLL can run from the internal FRO 12 MHz output, the external clock input CLKIN, or the RTC oscillator.

The system PLL accepts an input clock frequency in the range of 32 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO) The PLL can be enabled or disabled by software.

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7.21.2 Clock Generation

The system control block facilitates the clock generation. Many clocking variations are possible. Figure 8 gives an overview of the potential clock options.

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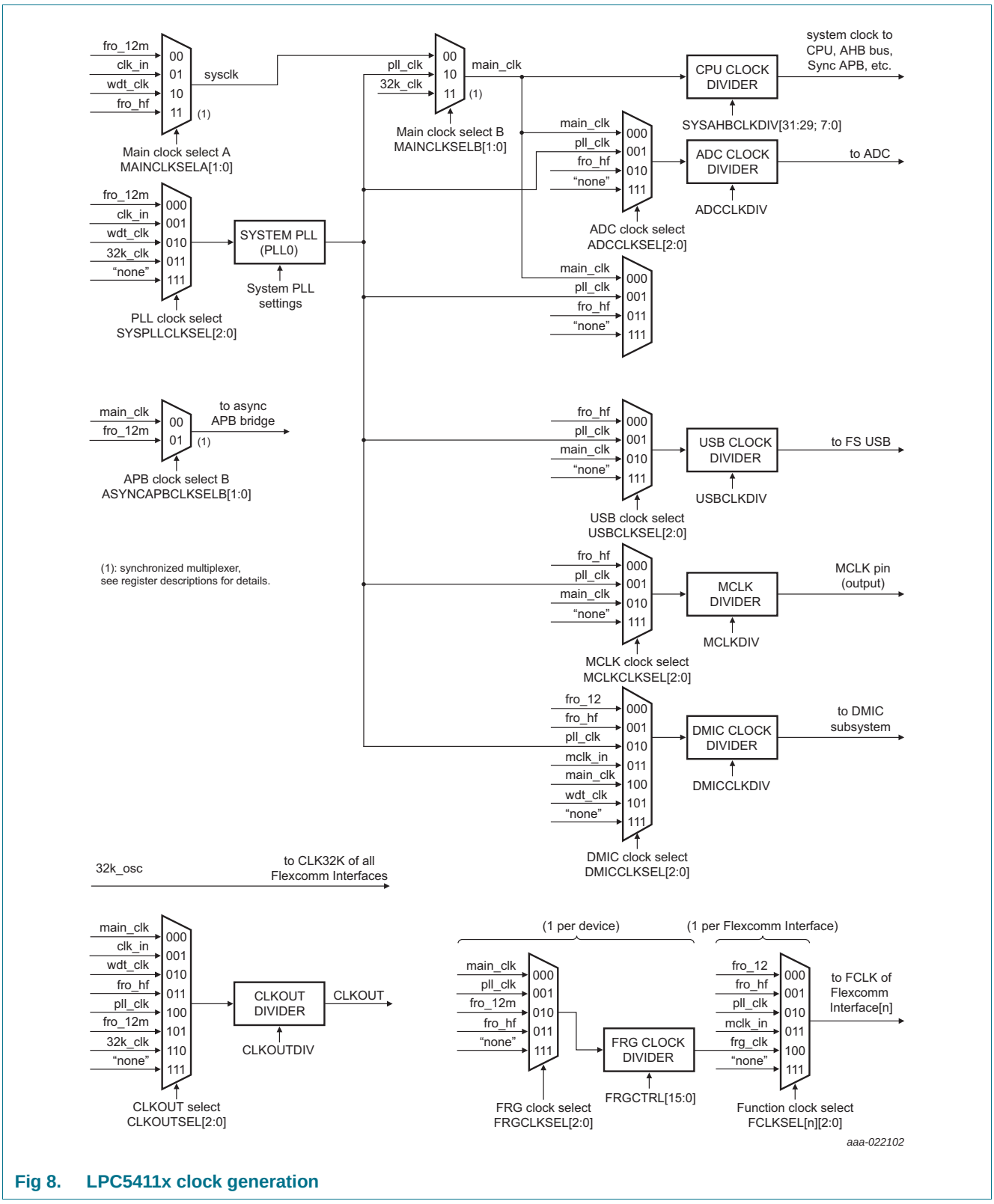

Fig 8. LPC5411x clock generation

Table 8 describes signals on the clocking diagram.

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Table 8. Clocking diagram signal name descriptions

Name	Description
32k_clk	The 32 kHz output of the RTC oscillator. The 32 kHz clock must be enabled in the RTCOSCCTRL register.
clk_in	This is the internal clock that comes from the main CLK_IN pin function. That function must be connected to the pin by selecting it in the IOCON block.
frg_clk	The output of the Fractional Rate Generator.
fro_12m	The 12 MHz output of the currently selected on-chip FRO oscillator.
fro_hf	The currently selected FRO high speed output. This may be either 96 MHz or 48 MHz.
main_clk	The main clock used by the CPU and AHB bus, and potentially many others.
mclk_in	The MCLK input function, when it is connected to a pin by selecting it in the IOCON block.
pll_clk	The output of the PLL.
wdt_clk	The output of the watchdog oscillator, which has a selectable target frequency. It must also be enabled in the PDRINCFG0 register.
“none”	A tied-off source that should be selected to save power when the output of the related multiplexer is not used.

7.21.3 Brownout detection

The LPC5411x includes a monitor for the voltage level on the V_{DD} pin. If this voltage falls below a fixed level, the BOD sets a flag that can be polled or cause an interrupt. In addition, a separate threshold levels can be selected to cause chip reset and interrupt.

7.21.4 Safety

The LPC5411x includes a Windowed WatchDog Timer (WWDT), which can be enabled by software after reset. Once enabled, the WWDT remains locked and cannot be modified in any way until a reset occurs.

7.22 Code security (Code Read Protection - CRP)

This feature of the LPC5411x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry can be invoked by pulling a pin on the LPC5411x LOW on reset. This pin is called the ISP entry pin.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. CRP3 fully disables any access to the chip via SWD and ISP. It is up to the user’s application to provide (if needed) flash update mechanism using IAP calls or a call to reinvoke ISP command to enable a flash update via USART.

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4. In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled (No_ISP mode). For details, see the LPC5411x user manual.

CAUTION	
⚠	If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.23 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M4 and ARM Cortex-M0+. Serial wire debug and trace functions are supported. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points. In addition, JTAG boundary scan mode is provided.

The ARM SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

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8. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)	on pin V_{DD}	[2]	–0.5	+4.6	V
V_{DDA}	analog supply voltage	on pin V_{DDA}		–0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP	-	–0.5	+4.6	V
V_I	input voltage	only valid when the V_{DD} > 1.8 V; 5 V tolerant I/O pins	[6][7]	–0.5	+5.0	V
V_I	input voltage	on I2C open-drain pins	[5]	–0.5	+5.0	V
		USB_DM, USB_DP pins		–0.5	+5.0	V
V_{IA}	analog input voltage	on digital pins configured for an analog function	[8][9]	–0.5	V_{DD}	V
I_{DD}	total supply current	per supply pin	[3]	-	60	mA
I_{SS}	total ground current	per ground pin	[3]	-	60	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; T_j < 125 °C		-	100	mA
$V_{i(rtcx)}$	32.768 kHz oscillator input voltage		[2]	–0.5	+4.6	V
T_{stg}	storage temperature		[10]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[4]		4000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 19.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 19) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] Applies to all 5 V tolerant I/O pins except true open-drain pins.

[7] Including the voltage on outputs in 3-state mode.

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[8] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 10. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
LQFP64 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	58 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	81 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		18 ± 15 %	°C/W
WLCSP49 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	41 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		0.3 ± 15 %	°C/W

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10. Static characteristics

10.1 General operating conditions

Table 11. General operating conditions

T_{amb} = –40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	100	MHz
V_{DD}	supply voltage (core and external rail)			1.62	-	3.6	V
V_{DDA}	analog supply voltage			1.62	-	3.6	V
V_{refp}	ADC positive reference voltage	$V_{DDA} \geq 2$ V		2.0	-	V_{DDA}	V
		$V_{DDA} < 2$ V		V_{DDA}	-	V_{DDA}	V
RTC oscillator pins							
$V_{i(rtcx)}$	32.768 kHz oscillator input voltage	on pin RTCXIN		–0.5	-	+3.6	V
$V_{o(rtcx)}$	32.768 kHz oscillator output voltage	on pin RTCXOUT		–0.5	-	+3.6	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

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10.2 CoreMark data

Table 12. CoreMark score

T_{amb} = 25 °C, V_{DD} = 3.3V

Parameter	Conditions		Typ	Unit
ARM Cortex-M4 in active mode; ARM Cortex-M0+ in sleep mode				
CoreMark score	CoreMark code executed from SRAMX; CCLK = 12 MHz	[1][2][3][5][6]	2.6	(Iterations/s) / MHz
	CCLK = 48 MHz	[1][2][3][5][6]	2.6	(Iterations/s) / MHz
	CCLK = 96 MHz	[1][2][3][5][6]	2.6	(Iterations/s) / MHz
CoreMark score	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[1][2][3][4][6]	2.6	(Iterations/s) / MHz
	CCLK = 48 MHz; 3 system clock flash access time.	[1][2][3][4][6]	2.4	(Iterations/s) / MHz
	CCLK = 96 MHz; 5 system clock flash access time.	[1][2][3][4][6]	2.1	(Iterations/s) / MHz
ARM Cortex-M0+ in active mode; ARM Cortex-M4 in sleep mode				
CoreMark score	CoreMark code executed from SRAMX; CCLK = 12 MHz	[1][2][3][5][6]	2.0	(Iterations/s) / MHz
	CCLK = 48 MHz	[1][2][3][5][6]	2.0	(Iterations/s) / MHz
	CCLK = 96 MHz	[1][2][3][5][6]	2.0	(Iterations/s) / MHz
CoreMark score	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[1][2][3][4][6]	2.0	(Iterations/s) / MHz
	CCLK = 48 MHz; 3 system clock flash access time.	[1][2][3][4][6]	1.9	(Iterations/s) / MHz
	CCLK = 96 MHz; 5 system clock flash access time.	[1][2][3][4][6]	1.7	(Iterations/s) / MHz

[1] Clock source FRO. PLL disabled.

[2] Characterized through bench measurements using typical samples.

[3] Compiler settings: Keil µVision v.5.17., optimization level 3, optimized for time ON.

[4] See the FLASHCFG register in the LPC5411x User Manual for system clock flash access time settings.

[5] Flash is powered down

[6] SRAM1 and SRAM2 powered down. SRAM0 and SRAMX powered.

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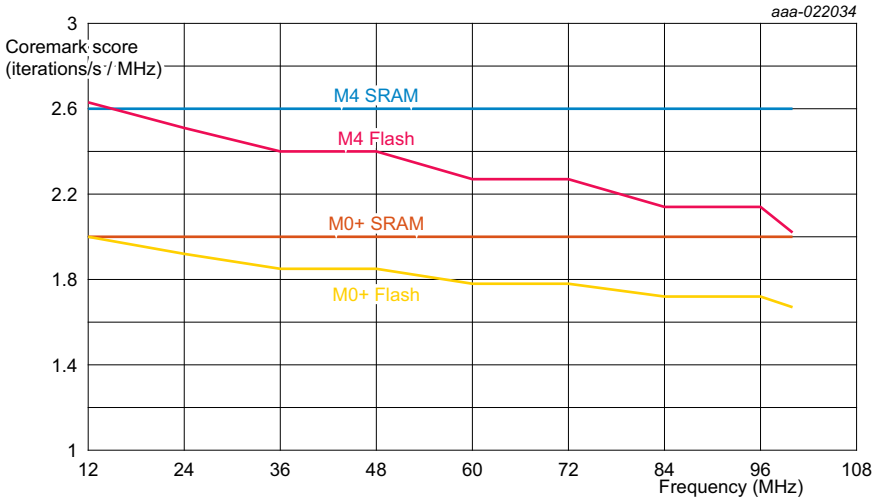

Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; See the FLASHCFG register in the LPC5411x, UM10914 User Manual for system clock flash access time settings. Measured with Keil uVision 5.17. Optimization level 3, optimized for time ON.

12 MHz, 48 MHz, and 96 MHz: FRO enabled; PLL disabled.

24 MHz, 36 MHz, 60 MHz, 72 MHz, 84 MHz, and 100 MHz: FRO enabled; PLL enabled.

Fig 9. Typical CoreMark score

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10.3 Power consumption

Power measurements in active, sleep, and deep-sleep modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.
- All peripherals disabled.

Table 13. Static characteristics: Power consumption in active mode

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M0+ in active mode; ARM Cortex-M4 in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAMX; flash powered down:					
		CCLK = 12 MHz	[2][3][4][6][7]	-	1.1	-	mA
		CCLK = 48 MHz	[2][3][4][6][7]	-	3.0	-	mA
		CCLK = 96 MHz	[2][3][4][6]	-	7.1	-	mA
I_{DD}	supply current	CoreMark code executed from flash;					
		CCLK = 12 MHz; 1 system clock flash access time.	[2][3][4][5][7]	-	1.3	-	mA
		CCLK = 48 MHz; 3 system clock flash access time.	[2][3][4][5][7]	-	3.6	-	mA
		CCLK = 96 MHz; 7 system clock flash access time.	[2][3][4][5]	-	8.0	-	mA
ARM Cortex-M4 in active mode; ARM Cortex-M0+ in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAMX; flash powered down:					
		CCLK = 12 MHz	[2][3][4][6][7]	-	1.3	-	mA
		CCLK = 48 MHz	[2][3][4][6][7]	-	3.9	-	mA
		CCLK = 96 MHz	[2][3][4][6]	-	9.3	-	mA
I_{DD}	supply current	CoreMark code executed from flash;					
		CCLK = 12 MHz; 1 system clock flash access time.	[2][3][4][5][7]	-	1.5	-	mA
		CCLK = 48 MHz; 3 system clock flash access time.	[2][3][4][5][7]	-	4.6	-	mA
		CCLK = 96 MHz; 7 system clock flash access time.	[2][3][4][5]	-	9.9	-	mA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), 3.3V.

[2] Clock source FRO. PLL disabled.

[3] Characterized through bench measurements using typical samples.

[4] Compiler settings: Keil µVision 5.17., optimization level 0, optimized for time off.

[5] Prefetch disabled in FLASHCFG register. SRAM0 powered. SRAM1, SRAM2, and SRAMX powered down. All peripheral clocks disabled.

[6] Flash is powered down; SRAM0 and SRAMX are powered; SRAM1 and SRAM2 are powered down. All peripheral clocks disabled.

[7] Characterized using low power regulation mode.

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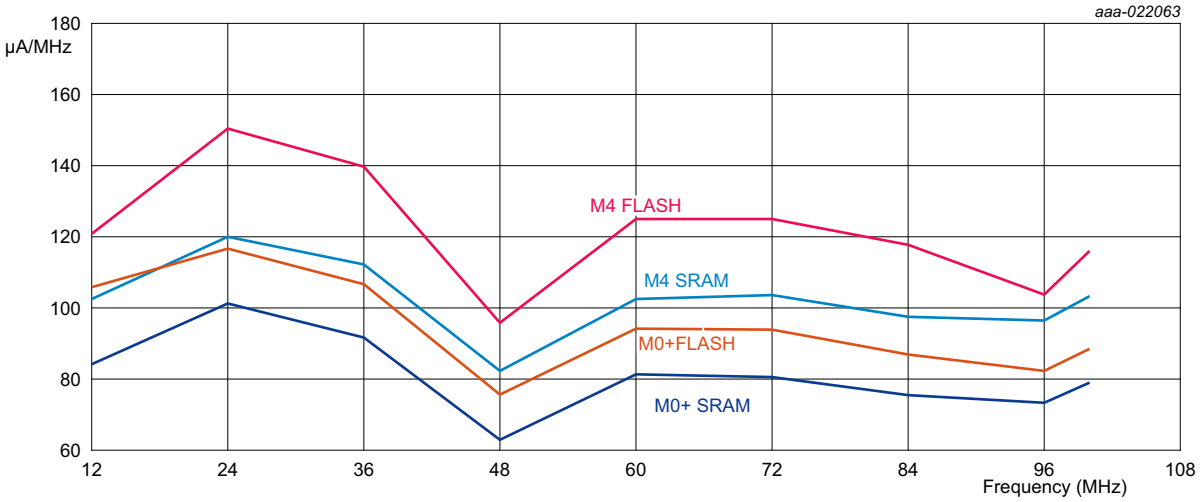

Conditions: VDD = 3.3 V; Tamb = 25 °C; active mode; all peripherals disabled; BOD disabled; Prefetch disabled in FLASHCFG register. See the FLASHCFG register in the LPC5411x, UM10914 User Manual for system clock flash access time settings. SRAM0 and SRAMX powered. SRAM1 and SRAM2 powered down. Measured with Keil uVision 5.17. Optimization level 0, optimized for time OFF.

12 MHz, 48 MHz, and 96 MHz: FRO enabled; PLL disabled.

24 MHz, 36 MHz, 60 MHz, 72 MHz, 84 MHz, and 100 MHz: FRO enabled; PLL enabled.

Fig 10. CoreMark power consumption: typical µA/MHz for M4 and M0+ cores

Table 14. Static characteristics: Power consumption in sleep mode

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M4 in sleep mode; ARM Cortex-M0+ in sleep mode							
I_{DD}	supply current	CCLK = 12 MHz	[2][3]	-	900	-	µA
		CCLK = 48 MHz	[2][3]	-	1.6	-	mA
		CCLK = 96 MHz	[2][3]	-	3.0	-	mA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), 3.3V.

[2] Characterized through bench measurements using typical samples.

[3] Clock source FRO. PLL disabled. All SRAM powered. Compiler settings: Keil µVision 5.17., optimization level 0, optimized for time off.

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Table 15. Static characteristics: Power consumption in deep-sleep and deep power-down modes

T_{amb} = −40 °C to +105 °C, 1.62 V ≤ V_{DD} ≤ 2.0 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1][2]	Max	Unit
I_{DD}	supply current	Deep-sleep mode. Flash is powered down.				
		SRAM0 (64 KB) powered.	-	7	-	μA
		SRAM0 (64 KB), SRAM1 (64 KB) powered.	-	10	-	μA
		SRAM0 (64 KB), SRAM1 (64 KB), SRAM2 (32 KB) powered.	-	11	-	μA
		SRAM0 (64 KB), SRAM1 (64 KB), SRAM2 (32 KB), SRAMX (32 KB) powered.	-	13	-	μA
		Deep power-down mode; RTC oscillator input grounded (RTC oscillator disabled). T_{amb} = 25 °C	-	300	-	nA
		T_{amb} = 105 °C	-	7	-	μA
		RTC oscillator running with external crystal.	-	390	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples. V_{DD} = 1.8V.

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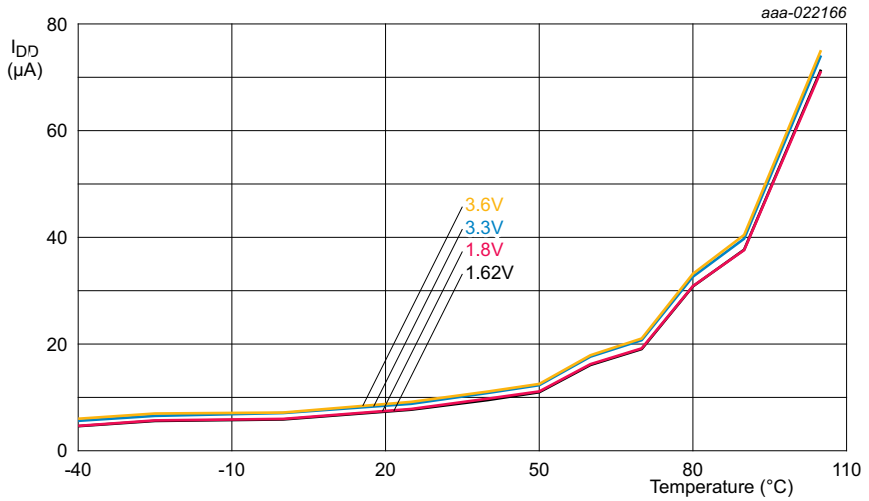
Table 16. Static characteristics: Power consumption in deep-sleep and deep power-down modes
T_{amb} = −40 °C to +105 °C, 2.7 V ≤ V_{DD} ≤ 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1][2]	Max	Unit
I_{DD}	supply current	Deep-sleep mode. Flash is powered down.				
		SRAM0 (64 KB) powered.	-	12	-	μA
		SRAM0 (64 KB), SRAM1 (64 KB) powered.	-	15	-	μA
		SRAM0 (64 KB), SRAM1 (64 KB), SRAM2 (32 KB) powered.	-	16	-	μA
		SRAM0 (64 KB), SRAM1 (64 KB), SRAM2 (32 KB), SRAMX(32 KB) powered.	-	18	-	μA
		Deep power-down mode; RTC oscillator input grounded (RTC oscillator disabled). T_{amb} = 25 °C	-	320	-	nA
		T_{amb} = 105 °C	-	9	-	μA
		RTC oscillator running with external crystal.	-	450	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples. V_{DD} = 3.3 V.



Conditions: all SRAMs disabled except SRAM0 (64 KB).

Fig 11. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

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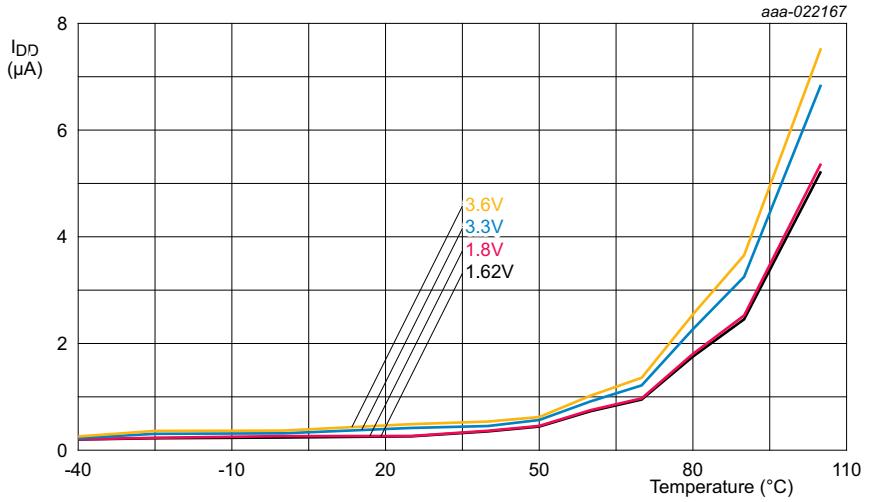

Conditions: RTC disabled (RTC oscillator input grounded)

Fig 12. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

Table 17. Typical peripheral power consumption[1][2][3]

V_{DD} = 3.3 V; T_{amb} = 25 °C

Peripheral	I_{DD} in uA
FRO (12 MHz, 48 MHz, 96 MHz)	100.0
WDT OSC	2.0
Flash	200.0
BOD	2.0

[1] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using PDRUNCFG0/1 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[2] The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, and 96 MHz.

[3] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

Table 18. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
AHB peripheral		**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 48 MHz**	**CPU: 96MHz, sync APB bus: 96 MHz**
USB		2.14	2.09	2.09
Temperature sensor		0.02	0.01	0.01
DMIC		0.17	0.17	0.17
GPIO0	[1]	0.69	0.65	0.66
GPIO1	[1]	0.56	0.56	0.56
DMA		0.34	0.43	0.43
CRC		0.50	0.54	0.54
MAILBOX		0.19	0.12	0.12

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Table 18. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
ADC0		1.65	1.67	1.67
SCTimer/PWM		4.10	4.05	4.04
Flexcomm Interface 0 (USART, SPI, I^2C)		1.1	1.2	1.2
Flexcomm Interface1 (USART, SPI, I^2C)		1.2	1.2	1.2
Flexcomm Interface 2 (USART, SPI, I^2C)		1.2	1.2	1.2
Flexcomm Interface 3 (USART, SPI, I^2C)		1.1	1.1	1.1
Flexcomm Interface 4 (USART, SPI, I^2C)		1.2	1.2	1.2
Flexcomm Interface 5 (USART, SPI, I^2C)		1.3	1.3	1.3
Flexcomm Interface 6 (USART, SPI, I^2C, I^2S)		1.3	1.3	1.3
Flexcomm Interface 7 (USART, SPI, I^2C, I^2S)		1.3	1.3	1.4
Sync APB peripheral		**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 48 MHz**	**CPU: 96MHz, sync APB bus: 96 MHz**
INPUTMUX	[1]	0.87	0.93	0.93
IOCON	[1]	5.04	5.12	5.12
PINT		1.28	1.26	1.26
GINT		1.20	1.17	1.17
WWDT		0.28	0.32	0.32
RTC		0.73	0.65	0.66
MRT		0.26	0.34	0.34
UTICK		0.13	0.16	0.16
Timer0		0.52	0.50	0.50
Timer1		0.39	0.46	0.47
Timer2		0.48	0.52	0.52
Fractional Rate Generator		0.46	0.44	0.44
Async APB peripheral		**CPU: 12 MHz, Async APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 12 MHz**	**CPU: 96MHz, Async APB bus: 12 MHz[2]**
Timer3		0.36	0.36	0.36
Timer4		0.37	0.38	0.38

[1] Turn off the peripheral when the configuration is done.

[2] For optimal system power consumption, use fixed low frequency Async APB bus when the CPU is at a higher frequency.

[3] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1, and PDRUNCFG0 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[4] The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, and 96 MHz.

[5] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

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10.4 Pin characteristics

Table 19. Static characteristics: pin characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
RESET pin							
V_{IH}	HIGH-level input voltage			0.8 × V_{DD}	-	5.0	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage		[12]	0.05 × V_{DD}	-	-	V
Standard I/O pins							
Input characteristics							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled.		-	3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; V_{DD} = 3.6 V; for RESETN pin.			3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	3.0	180	nA
V_I	input voltage	pin configured to provide a digital function;	[3]				
		V_{DD} > 1.8 V		0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_{IH}	HIGH-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		1.5	-	5.0	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		2.0	-	5.0	V
V_{IL}	LOW-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		−0.5	-	+0.4	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		−0.5	-	+0.8	V
V_{hys}	hysteresis voltage		[12]	0.1 × V_{DD}	-	-	V
Output characteristics							
V_O	output voltage	output active		0	-	V_{DD}	V
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/pull-down resistors disabled		-	3	180	nA
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA; 1.62 V ≤ V_{DD} < 2.7 V		V_{DD} − 0.4	-	-	V
		I_{OH} = −6 mA; 2.7 V ≤ V_{DD} ≤ 3.6 V		V_{DD} − 0.4			
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 1.62 V ≤ V_{DD} < 2.7 V		-	-	0.4	V
		I_{OL} = 6 mA; 2.7 V ≤ V_{DD} ≤3.6 V		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 1.62 V ≤ V_{DD} < 2.7 V		4.0	-	-	mA
		V_{OH} = V_{DD} − 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; 1.62 V ≤ V_{DD} < 2.7 V		4.0	-	-	mA
		V_{OL} = 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	1.62 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	35	mA
	drive HIGH; connected to ground;	2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	87	mA

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Table 19. Static characteristics: pin characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OLS}	LOW-level short-circuit output current	1.62 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	30	mA
	drive LOW; connected to V_{DD}	2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	77	mA
Weak input pull-up/pull-down characteristics							
I_{pd}	pull-down current	V_I = V_{DD}		25		80	μA
		V_I = 5 V	[2]	80		100	μA
I_{pu}	pull-up current	V_I = 0 V		−25		−80	μA
		V_{DD} < V_I < 5 V	[2][7]	6		30	μA
Open-drain I²C pins							
V_{IH}	HIGH-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		0.7 × V_{DD}	-	-	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		0.7 × V_{DD}	-	-	V
V_{IL}	LOW-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		0	-	0.3 × V_{DD}	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		0	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage			0.1 × V_{DD}	-	-	V
I_{LI}	input leakage current	V_I = V_{DD}	[5]	-	2.5	3.5	μA
		V_I = 5 V		-	5.5	10	μA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; pin configured for standard mode or fast mode		4.0	-	-	mA
		V_{OL} = 0.4V; pin configured for Fast-mode Plus		20	-	-	mA
USB_DM and USB_DP pins							
V_I	input voltage			0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
Z_{out}	output impedance			33.0	-	44	Ω
V_{OH}	HIGH-level output voltage			2.8	-	-	V
V_{OL}	LOW-level output voltage			-	-	0.3	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.3 V	[9][10]	38	-	74	mA
		V_{OH} = V_{DD} − 0.3 V	[10][11]	6.0		9.0	mA
I_{OL}	LOW-level output current	V_{OL} = 0.3 V	[9][10]	38	-	74	mA
		V_{OL} = 0.3 V	[10][11]	6.0		9.0	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; pad connected to ground	[10]	-	-	100	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; pad connected to ground	[10]	-	-	100	mA

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Table 19. Static characteristics: pin characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Pin capacitance							
C_{io}	input/output capacitance	I^2C-bus pins	[8]	-	-	6.0	pF
		pins with digital functions only	[6]	-	-	2.0	pF
		Pins with digital and analog functions	[6]	-	-	7.0	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltage.

[2] Based on characterization. Not tested in production.

[3] With respect to ground.

[4] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[5] To V_{SS}.

[6] The values specified are simulated and absolute values, including package/bondwire capacitance.

[7] The weak pull-up resistor is connected to the V_{DD} rail and pulls up the I/O pin to the V_{DD} level.

[8] The value specified is a simulated value, excluding package/bondwire capacitance.

[9] Without 33 Ω ± 2 % series external resistor.

[10] The parameter values specified are simulated and absolute values.

[11] With 33 Ω ± 2 % series external resistor.

[12] Guaranteed by design, not tested in production.

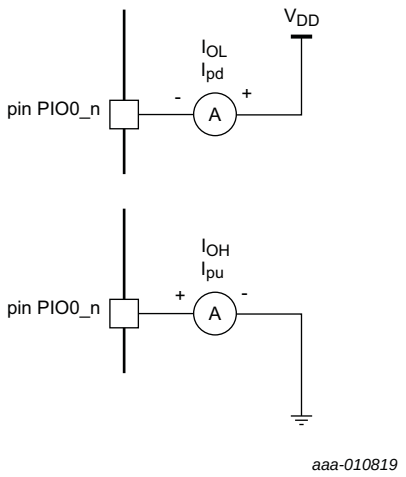

Fig 13. Pin input/output current measurement

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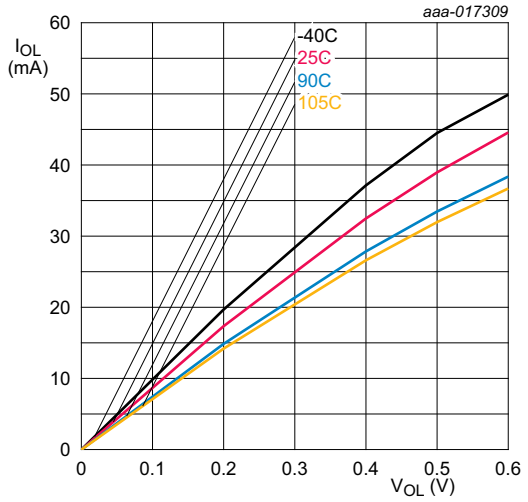
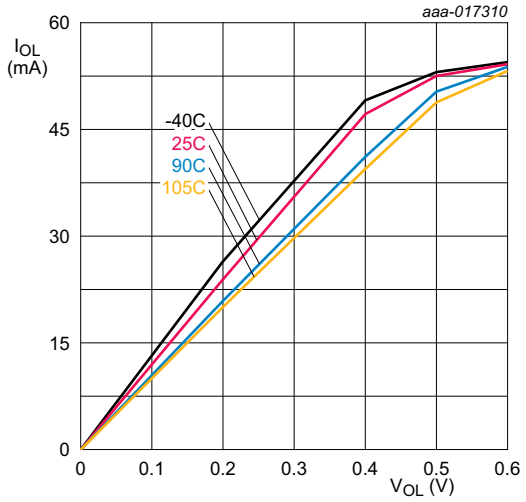
10.4.1 Electrical pin characteristics

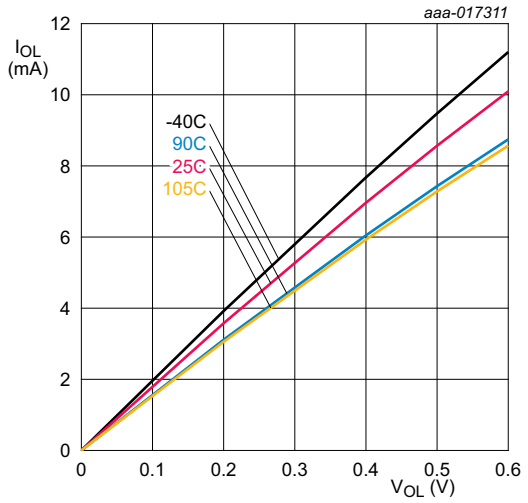


Conditions: V_{DD} = 1.8 V; on pins PIO0_23 to PIO0_26.

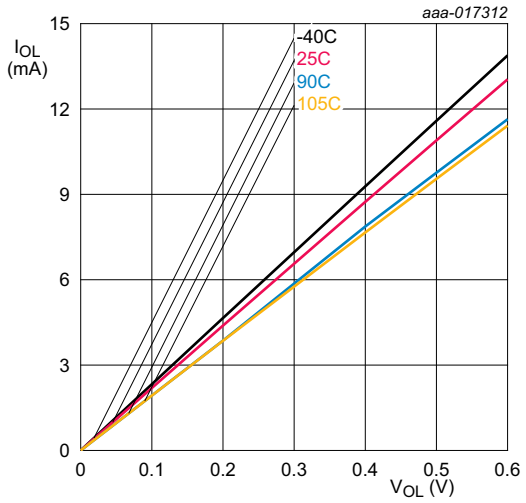


Conditions: V_{DD} = 3.3 V; on pins PIO0_23 to PIO0_26.

Fig 14. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 15. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

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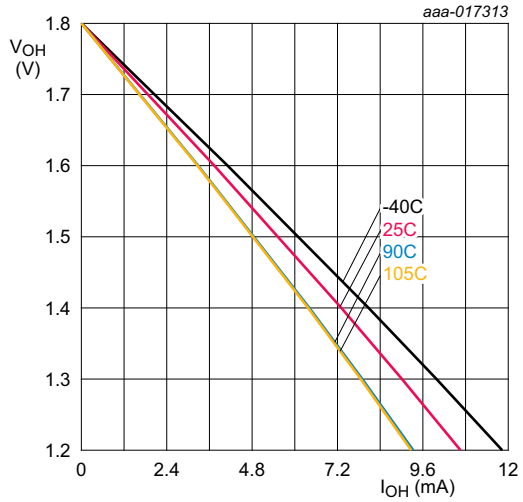
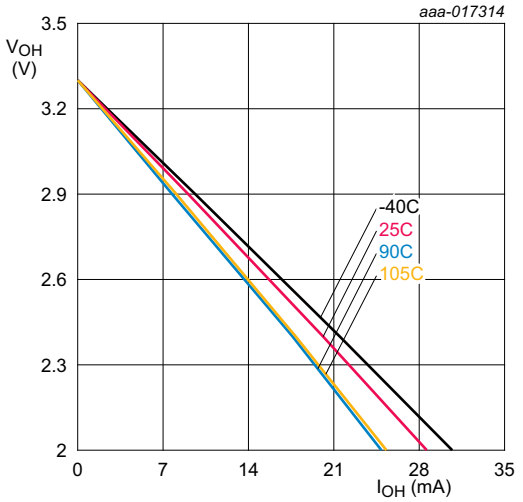
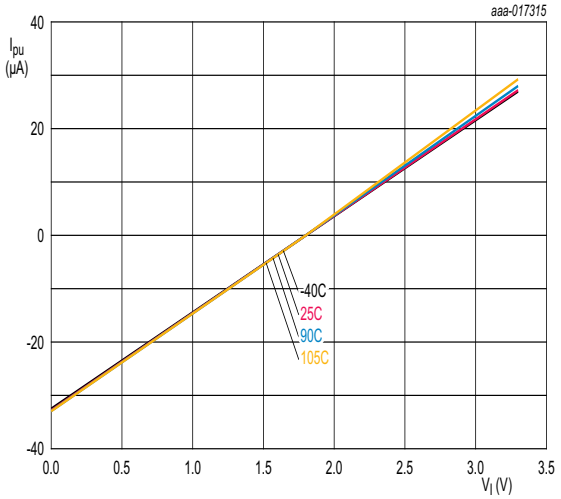


Conditions: V_{DD} = 1.8 V; on standard port pins.

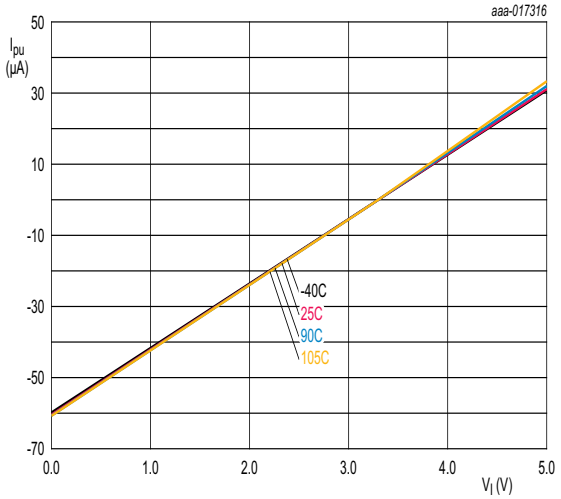


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 16. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 1.8 V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 17. Typical pull-up current I_{PU} versus input voltage V_I

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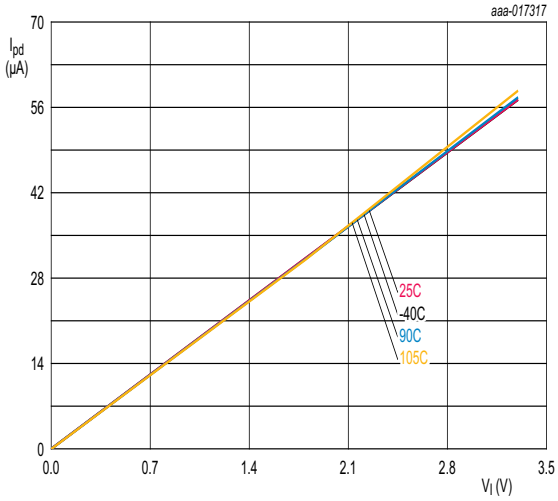
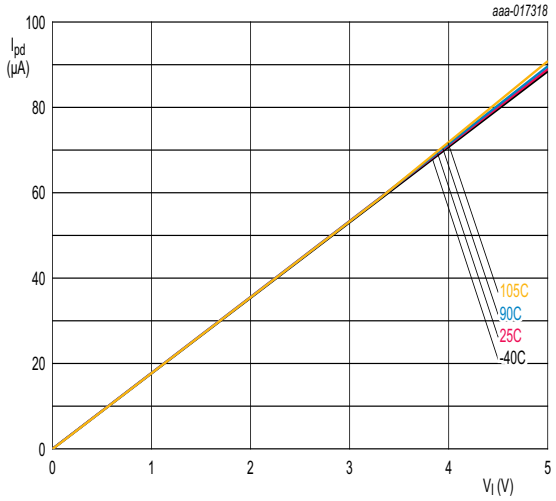


Conditions: V_{DD} = 1.8V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 18. Typical pull-down current I_{PD} versus input voltage V_I

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11. Dynamic characteristics

11.1 Power-up ramp conditions

Table 20. Power-up characteristics

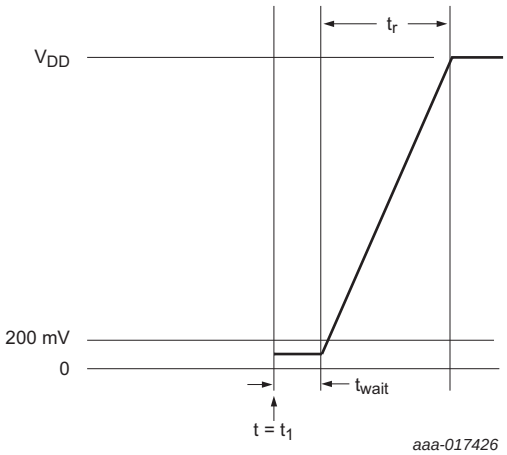
T_{amb} = −40 °C to +105 °C unless otherwise specified; 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	at t = t_1: 0 < V_I ≤ 200 mV	[1][3]	0	-	500	ms
t_{wait}	wait time		[1][2]	12	-	-	µs
V_I	input voltage	at t = t_1 on pin V_{DD}	[3]	0	-	500	mV

[1] See Figure 19.

[2] Based on simulation. The wait time specifies the time the power supply must be at levels below 200 mV before ramping up.

[3] Based on characterization, not tested in production.



Condition: 0 < V_I ≤ 200 mV at start of power-up (t = t_1)

Fig 19. Power-up ramp

11.2 Flash memory

Table 21. Flash characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
N_{endu}	endurance	sector erase/program	[2]	10000	-	-	cycles
		page erase/program; page in large sector		1000	-	-	cycles
		page erase/program; page in small sector		10000	-	-	cycles

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Table 21. Flash characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	page, sector, or multiple consecutive sectors		-	100	-	ms
t_{prog}	programming time		[3]	-	1	-	ms

[1] Typical ratings are not guaranteed.

[2] Number of erase/program cycles.

[3] Programming times are given for writing 512 bytes from RAM to the flash. Data must be written to the flash in blocks of 512 bytes.

11.3 I/O pins

Table 22. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +85 °C unless otherwise specified; 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1 (fast mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.0	-	2.5	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		1.6	-	3.8	ns
t_f	fall time	pin configured as output; SLEW = 1 (fast mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		0.9	-	2.5	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		1.7	-	4.1	ns
t_r	rise time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.9	-	4.3	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		2.9	-	7.8	ns
t_f	fall time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.9	-	4.0	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		2.7	-	6.7	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data.

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the IOCON block the SLEW bit. See the *LPC5411x UM10914* user manual.

[4] C_L = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

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11.4 Wake-up process

Table 23. Dynamic characteristic: Typical wake-up times from low power modes
V_{DD} = 3.3 V;T_{amb} = 25 °C; using FRO as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from Sleep mode	[2][3]	-	2.0	-	µs
		from Deep-sleep mode to code executing in flash	[2][5]	-	19	-	µs
		to code executing in SRAM	[2][5]	-	19	-	µs
		from deep power-down mode; RTC disabled; using $\overline{\text{RESET}}$ pin.	[4][5]	-	1.2	-	ms

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[3] FRO enabled, all peripherals off. PLL disabled.

[4] RTC disabled. Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the $\overline{\text{RESET}}$ pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

[5] FRO disabled.

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11.5 PLL

Table 24. PLL lock times and current

T_{amb} = −40 °C to +105 °C. V_{DD} = 1.62 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL configuration: input frequency 12 MHz; output frequency 75 MHz							
$t_{lock(PLL)}$	PLL lock time	PLL set-up procedure followed	[2]	-	-	400	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	550	µA
PLL configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL)}$	PLL lock time	PLL set-up procedure followed	[2]	-	-	400	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	750	µA
PLL0 configuration: input frequency 32.768 kHz; output frequency 75 MHz							
$t_{lock(PLL)}$	PLL lock time	-	[1]	-	-	6250	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	450	µA
PLL0 configuration: input frequency 32.768 kHz; output frequency 100 MHz							
$t_{lock(PLL)}$	PLL lock time	-	[1]	-	-	6250	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	560	µA

[1] Data based on characterization results, not tested in production.

[2] PLL set-up requires high-speed start-up and transition to normal mode. Lock times are only valid when high-speed start-up settings are applied followed by normal mode settings. The procedure for setting up the PLL is described in the LPC5411x user manual.

[3] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

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Table 25. Dynamic characteristics of the PLL[1]
T_{amb} = −40 °C to +105 °C. V_{DD} = 1.62 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
f_{ref}	reference frequency	input frequency at PFD (clkref)		32.768 kHz	-	25 MHz	-
$f_{ref-jitter}$	input jitter for reference frequency	-	[2]	-	-	10% of period frequency	-
Clock output							
f_o	output frequency	for PLL clkout output	[3]	1.2	-	150	MHz
d_o	output duty cycle	for PLL clkout output		46	-	54	%
f_{CCO}	CCO frequency	-		-	-	150	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion	-	[4]	1	2	4	ns
Dynamic parameters at f_{out} = f_{CCO} = 100 MHz; standard bandwidth settings							
$J_{rms-interval}$	RMS interval jitter	f_{ref} = 10 MHz	[5][6]	-	15	30	ps
$J_{pp-period}$	peak-to-peak, period jitter	f_{ref} = 10 MHz	[5][6]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Output jitter depends on the frequency of input jitter and is equal to or less than the input jitter.

[3] Excluding under- and overshoot which may occur when the PLL is not in lock.

[4] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[5] Actual jitter dependent on amplitude and spectrum of substrate noise.

[6] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.6 FRO

Table 26. Dynamic characteristic: FRO
T_{amb} = −40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Min[2]	Typ[1]	Max[2]	Unit
$f_{osc(FRO)}$	FRO clock frequency	11.88	12	12.12	MHz
$f_{osc(FRO)}$	FRO clock frequency	47.52	48	48.48	MHz
$f_{osc(FRO)}$	FRO clock frequency	95.04	96	96.96	MHz

[1] Tested in production.The values listed are at room temperature (25 °C).

[2] Data based on characterization results, not tested in production.

11.7 RTC oscillator

See Section 13.4 for connecting the RTC oscillator to an external clock source.

Table 27. Dynamic characteristic: RTC oscillator
T_{amb} = −40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V[1]

Symbol	Parameter	Min	Typ	Max	Unit
f_i	input frequency	-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

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11.8 Watchdog oscillator

Table 28. Dynamic characteristics: Watchdog oscillator
T_{amb} = −40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal watchdog oscillator frequency	[2]	200	-	1500	kHz
D_{clkout}	clkout duty cycle		48	-	52	%
J_{PP-CC}	peak-peak period jitter	[3][4]	-	1	20	ns
t_{start}	start-up time	[4]	-	4	-	µs

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] Actual jitter dependent on amplitude and spectrum of substrate noise.

[4] Guaranteed by design. Not tested in production samples.

11.9 I²C-bus

Table 29. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] Guaranteed by design. Not tested in production.

[2] Parameters are valid over operating temperature range unless otherwise specified. See the I²C-bus specification *UM10204* for details.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

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[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

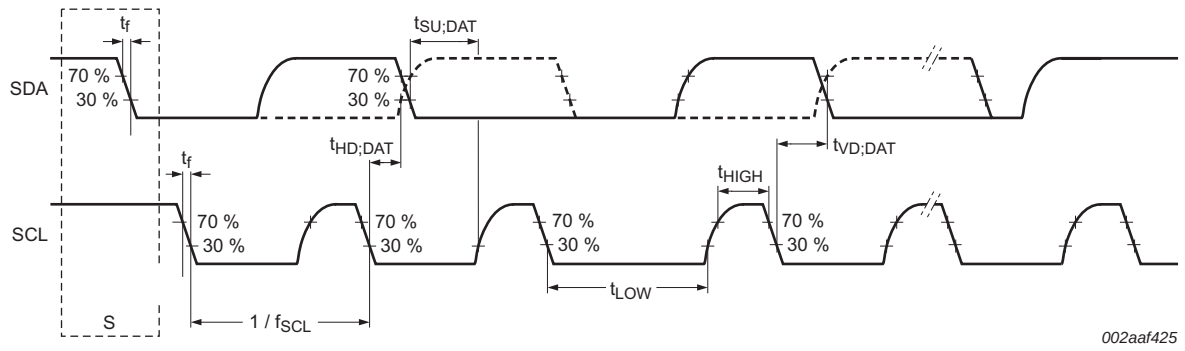

Fig 20. I²C-bus pins clock timing

11.10 I²S-bus interface

Table 30. Dynamic characteristics: I²S-bus interface pins [1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, EHS set to 0 for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
common to input and output							
t_r	rise time	CCLK = 1 MHz to 12 MHz		-	4	-	ns
		CCLK = 48 MHz to 60 MHz		-	4	-	ns
		CCLK = 96 MHz		-	4	-	ns
t_f	fall time	CCLK = 1 MHz to 12 MHz		-	4	-	ns
		CCLK = 48 MHz to 60 MHz		-	4	-	ns
		CCLK = 96 MHz		-	4	-	ns
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK					
		CCLK = 1 MHz to 12 MHz		20	-	-	ns
		CCLK = 48 MHz to 60 MHz		20	-	-	ns
		CCLK = 96 MHz		20	-	-	ns

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Table 30. Dynamic characteristics: I²S-bus interface pins [1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, EHS set to 0 for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK					
		CCLK = 1 MHz to 12 MHz		20	-	-	ns
		CCLK = 48 MHz to 60 MHz		20	-	-	ns
		CCLK = 96 MHz		20	-	-	ns
output; 1.62 V ≤ V_{DD} ≤ 2.0 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK = 1 MHz to 12 MHz		-	36	-	ns
		CCLK = 48 MHz to 60 MHz		-	32	-	ns
		CCLK = 96 MHz		-	30	-	ns
		on pin I2Sx_TX_WS					
		CCLK = 1 MHz to 12 MHz		-	38	-	ns
		CCLK = 48 MHz to 60 MHz		-	30	-	ns
		CCLK = 96 MHz		-	28	-	ns
input; 1.62 V ≤ V_{DD} ≤ 2.0 V							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK = 1 MHz to 12 MHz		-	−3	-	ns
		CCLK = 48 MHz to 60 MHz		-	−2	-	ns
		CCLK = 96 MHz		-	−1.5	-	ns
		on pin I2Sx_RX_WS					
		CCLK = 1 MHz to 12 MHz		-	0	-	ns
		CCLK = 48 MHz to 60 MHz		-	−1	-	ns
		CCLK = 96 MHz		-	−1	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK = 1 MHz to 12 MHz		-	3.1	-	ns
		CCLK = 48 MHz to 60 MHz		-	3	-	ns
		CCLK = 96 MHz		-	2.8	-	ns
		on pin I2Sx_RX_WS					
		CCLK = 1 MHz to 12 MHz		-	3.2	-	ns
		CCLK = 48 MHz to 60 MHz		-	2.8	-	ns
		CCLK = 96 MHz		-	2.4	-	ns
output; 2.7 V ≤ V_{DD} ≤ 3.6 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK = 1 MHz to 12 MHz		-	28	-	ns
		CCLK = 48 MHz to 60 MHz		-	23	-	ns
		CCLK = 96 MHz		-	20	-	ns
		on pin I2Sx_TX_WS					
		CCLK = 1 MHz to 12 MHz		-	20	-	ns
		CCLK = 48 MHz to 60 MHz		-	12	-	ns
		CCLK = 96 MHz		-	9	-	ns

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Table 30. Dynamic characteristics: I²S-bus interface pins [1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, EHS set to 0 for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
input; 2.7 V ≤ V_{DD} ≤ 3.6 V							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK = 1 MHz to 12 MHz		-	−3	-	ns
		CCLK = 48 MHz to 60 MHz		-	−1.7	-	ns
		CCLK = 96 MHz		-	−1.4	-	ns
		on pin I2Sx_RX_WS					
		CCLK = 1 MHz to 12 MHz		-	2	-	ns
		CCLK = 48 MHz to 60 MHz		-	1.3	-	ns
		CCLK = 96 MHz		-	1.1	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK = 1 MHz to 12 MHz		-	1.2	-	ns
		CCLK = 48 MHz to 60 MHz		-	1	-	ns
		CCLK = 96 MHz		-	0.8	-	ns
		on pin I2Sx_RX_WS					
		CCLK = 1 MHz to 12 MHz		-	3	-	ns
		CCLK = 48 MHz to 60 MHz		-	1.6	-	ns
		CCLK = 96 MHz		-	1.2	-	ns

[1] Based on characterization; not tested in production.

[2] Clock to the I²S-bus interface BASE_APB1_CLK = 100 MHz; peripheral clock to the I²S-bus interface PCLK = BASE_APB1_CLK / 4. I²S clock cycle time $T_{cy(clk)}$ = 40.69 ns, corresponds to the SCK signal in the *I²S-bus specification*.

[3] Typical ratings are not guaranteed.

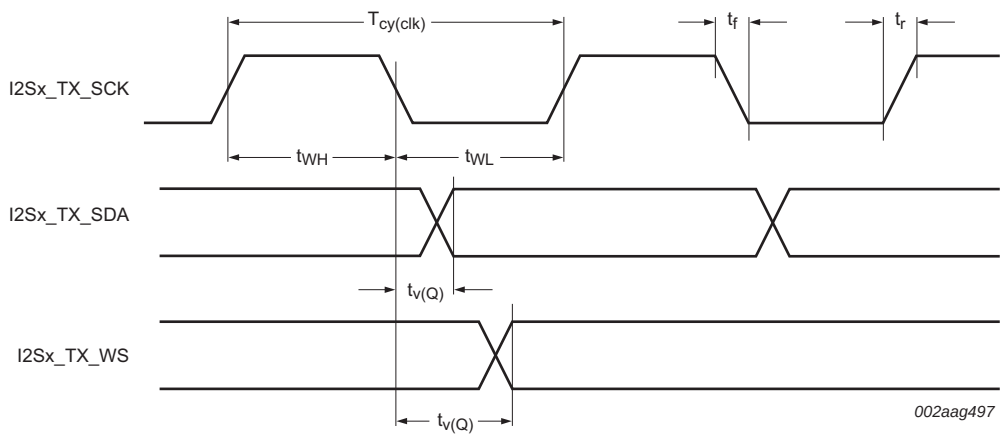

Fig 21. I²S-bus timing (transmit)

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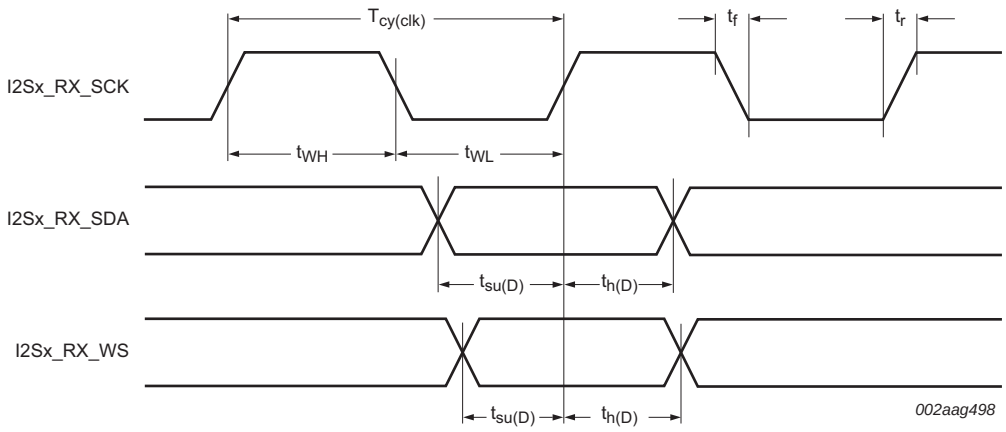

Fig 22. I²S-bus timing (receive)

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11.11 SPI interfaces

Table 31. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, EHS set to 0 for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
SPI master 1.62 V ≤ V_{DD} ≤ 2.0 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz	-	−7	-	ns
		CCLK = 48 MHz to 60 MHz	-	−6	-	ns
		CCLK = 96 MHz	-	−5	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz	-	6	-	ns
		CCLK = 48 MHz to 60 MHz	-	7	-	ns
		CCLK = 96 MHz	-	8	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	-	2	-	ns
		CCLK = 48 MHz to 60 MHz	-	2	-	ns
		CCLK = 96 MHz	-	1	-	ns
SPI slave 1.62 V ≤ V_{DD} ≤ 2.0 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz	-	−1	-	ns
		CCLK = 48 MHz to 60 MHz	-	−2	-	ns
		CCLK = 96 MHz	-	−3	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz	-	1	-	ns
		CCLK = 48 MHz to 60 MHz	-	2	-	ns
		CCLK = 96 MHz	-	3	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	-	45	-	ns
		CCLK = 48 MHz to 60 MHz	-	35	-	ns
		CCLK = 96 MHz	-	32	-	ns
SPI master 2.7 V ≤ V_{DD} ≤ 3.6 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz	-	5	-	ns
		CCLK = 48 MHz to 60 MHz	-	4	-	ns
		CCLK = 96 MHz	-	4	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz	-	3	-	ns
		CCLK = 48 MHz to 60 MHz	-	4	-	ns
		CCLK = 96 MHz	-	4	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	-	2	-	ns
		CCLK = 48 MHz to 60 MHz	-	2	-	ns
		CCLK = 96 MHz	-	1	-	ns

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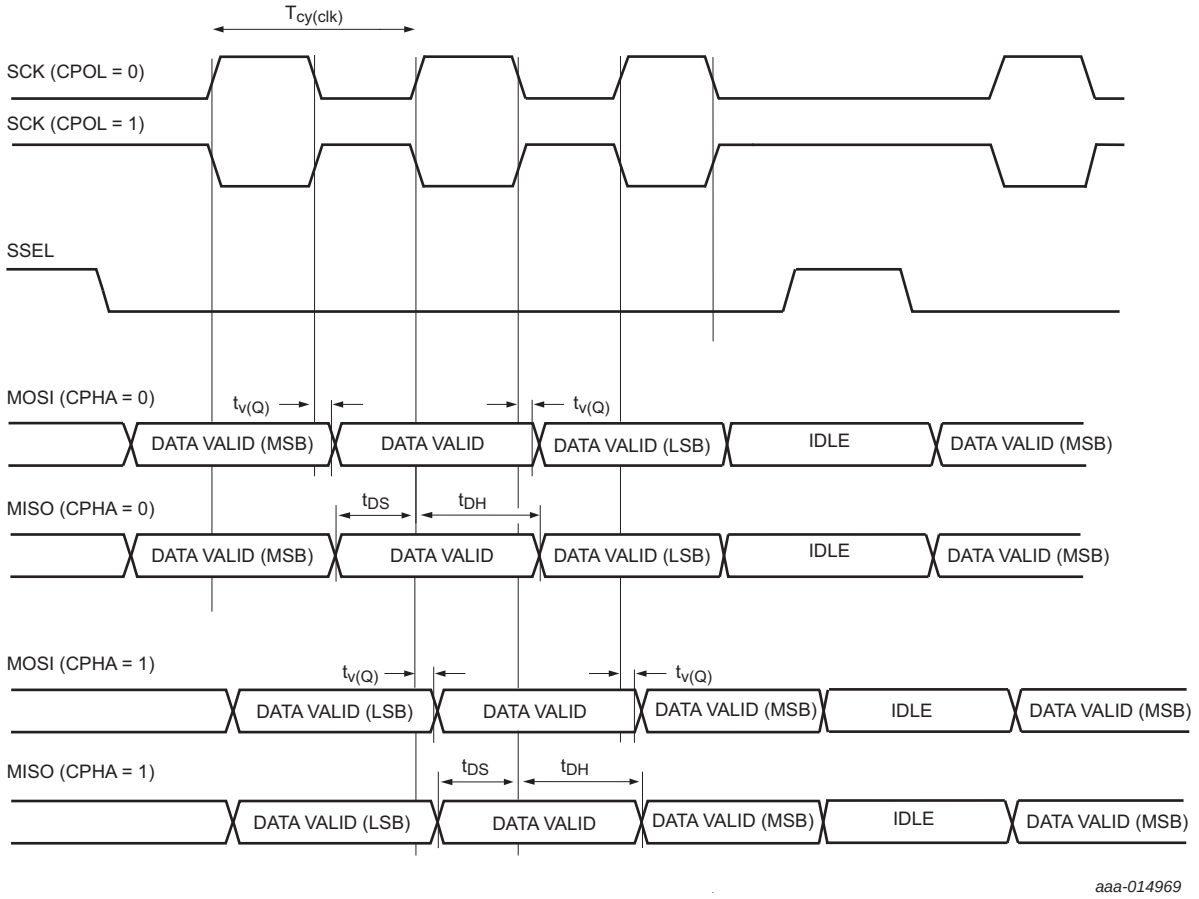
Table 31. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, EHS set to 0 for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
SPI slave 2.7 V ≤ V_{DD} ≤ 3.6 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz	-	−6	-	ns
		CCLK = 48 MHz to 60 MHz	-	−7	-	ns
		CCLK = 96 MHz	-	−8	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz	-	6	-	ns
		CCLK = 48 MHz to 60 MHz	-	7	-	ns
		CCLK = 96 MHz	-	8	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	-	32	-	ns
		CCLK = 48 MHz to 60 MHz	-	24	-	ns
		CCLK = 96 MHz	-	22	-	ns

[1] Based on characterization; not tested in production.

[2] Typical ratings are not guaranteed.



$T_{cy(clk)}$ = CCLK/DIVVAL with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the LPC5411x *User manual*.

Fig 23. SPI master timing

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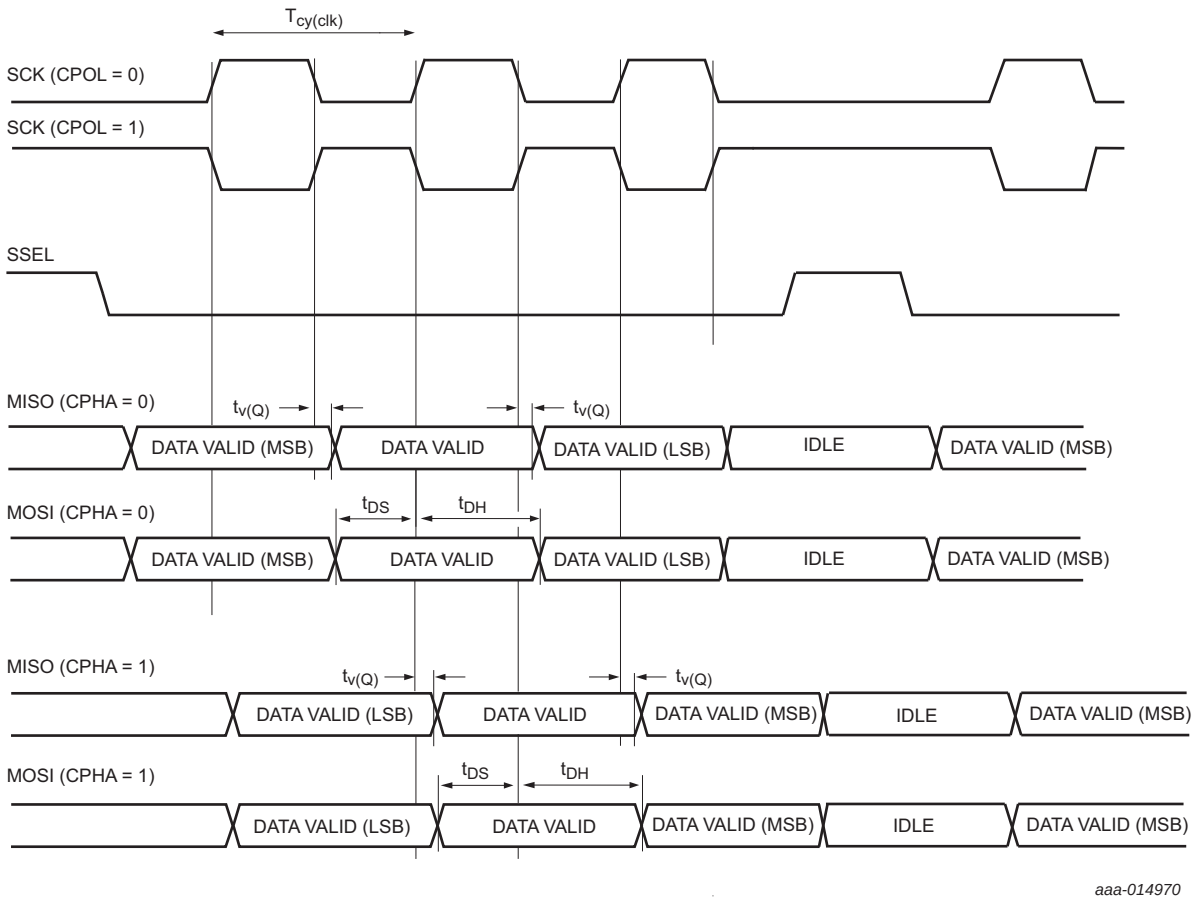

Fig 24. SPI slave timing

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11.12 USART interface

In master and slave synchronous modes, the maximum supported bit rate is 10.0 Mbit/sec.The actual bit rate depends on the delays introduced by the external trace, the external device, and capacitive loading.

Table 32. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, EHS set to 0 for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
USART master (in synchronous mode) 1.62 V ≤ V_{DD} ≤ 2.0 V						
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	-	35	-	ns
		CCLK = 48 MHz to 60 MHz	-	30	-	ns
		CCLK = 96 MHz	-	28	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	-	−35	-	ns
		CCLK = 48 MHz to 60 MHz	-	−30	-	ns
		CCLK = 96 MHz	-	−28	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	-	7	-	ns
		CCLK = 48 MHz to 60 MHz	-	5	-	ns
		CCLK = 96 MHz	-	4	-	ns
USART slave (in synchronous mode) 1.62 V ≤ V_{DD} ≤ 2.0 V						
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	-	−2	-	ns
		CCLK = 48 MHz to 60 MHz	-	−3	-	ns
		CCLK = 96 MHz	-	−3	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	-	3	-	ns
		CCLK = 48 MHz to 60 MHz	-	2	-	ns
		CCLK = 96 MHz	-	2	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	-	40	-	ns
		CCLK = 48 MHz to 60 MHz	-	35	-	ns
		CCLK = 96 MHz	-	32	-	ns
USART master (in synchronous mode) 2.7 V ≤ V_{DD} ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	-	25	-	ns
		CCLK = 48 MHz to 60 MHz	-	20	-	ns
		CCLK = 96 MHz	-	18	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	-	−25	-	ns
		CCLK = 48 MHz to 60 MHz	-	−20	-	ns
		CCLK = 96 MHz	-	−18	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	-	8	-	ns
		CCLK = 48 MHz to 60 MHz	-	6	-	ns
		CCLK = 96 MHz	-	5	-	ns

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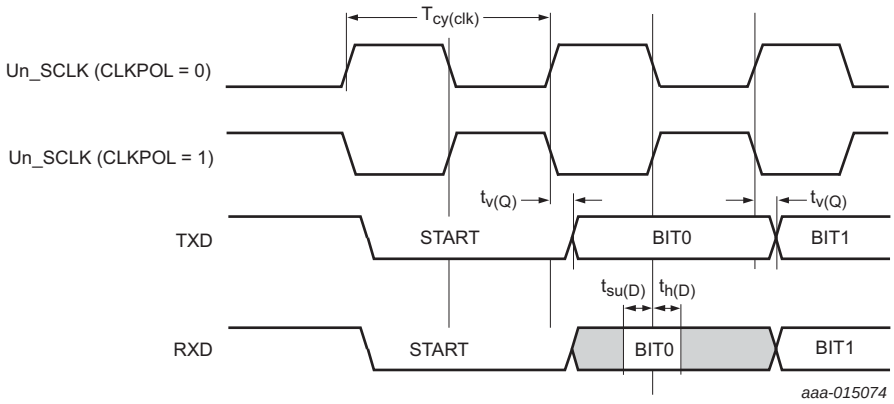
Table 32. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, EHS set to 0 for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
USART slave (in synchronous mode) 2.7 V ≤ V_{DD} ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	-	2	-	ns
		CCLK = 48 MHz to 60 MHz	-	2	-	ns
		CCLK = 96 MHz	-	1	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	-	2	-	ns
		CCLK = 48 MHz to 60 MHz	-	1	-	ns
		CCLK = 96 MHz	-	1	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	-	30	-	ns
		CCLK = 48 MHz to 60 MHz	-	24	-	ns
		CCLK = 96 MHz	-	22	-	ns

[1] Based on characterization; not tested in production.

[2] Typical ratings are not guaranteed.



In master mode, $T_{cy(clk)}$ = U_PCLK/BRGVAL. See the LPC5411x *User manual*.

Fig 25. USART timing

11.13 SCTimer/PWM output timing

Table 33. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V C_L = 30 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at 10 % and 90 % of the signal level; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	-	-	2.7	ns

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11.14 DMIC subsystem

Table 34. Dynamic characteristics

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, EHS set to 0 for all pins; Bypass bit = 0; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz	-	23	-	ns
		CCLK = 48 MHz to 60 MHz	-	13	-	ns
		CCLK = 96 MHz	-	9	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz	-	0	-	ns
		CCLK = 48 MHz to 60 MHz	-	0	-	ns
		CCLK = 96 MHz	-	0	-	ns

[1] Based on simulated values and for 2.7 V to 3.6 V.

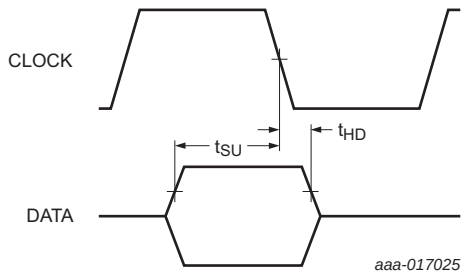

Fig 26. DMIC timing diagram

11.15 USB interface characteristics

Table 35. Dynamic characteristics: USB pins (Full-Speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		4.0	-	20	ns
t_f	fall time	10 % to 90 %		4.0	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		90	-	111.11	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 27		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 27		−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 27	[1]	40	-		ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 27	[1]	82	-	-	ns

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[1] Characterized but not implemented as production test. Guaranteed by design.

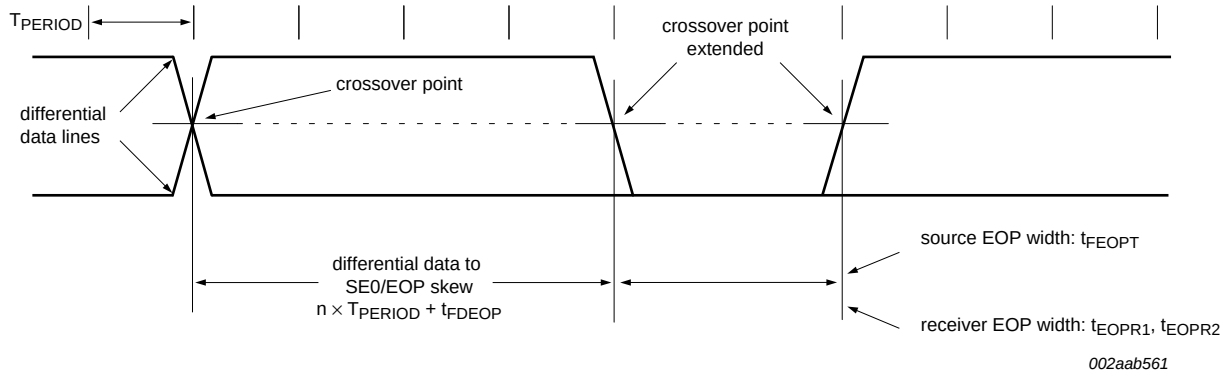

Fig 27. Differential data-to-EOP transition skew and EOP width

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12. Analog characteristics

12.1 BOD

Table 36. BOD static characteristics

T_{amb} = 25 °C; based on characterization; not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.97	-	V
		de-assertion	-	2.11	-	V
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	2.36	-	V
		de-assertion	-	2.51	-	V
		reset level 1				
		assertion	-	1.77	-	V
		de-assertion	-	1.92	-	V
V_{th}	threshold voltage	interrupt level 2				
		assertion	-	2.66	-	V
		de-assertion	-	2.80	-	V
		reset level 2				
		assertion	-	1.92	-	V
		de-assertion	-	2.06	-	V
V_{th}	threshold voltage	interrupt level 3				
		assertion	-	2.95	-	V
		de-assertion	-	3.09	-	V
		reset level 3				
		assertion	-	2.21	-	V
		de-assertion	-	2.36	-	V

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12.2 12-bit ADC characteristics

Table 37. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V; V_{SSA} = VREFN = GND. ADC calibrated at T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
V_{IA}	analog input voltage		[3]	0	-	V_{DDA}	V
C_{ia}	analog input capacitance		[4]	-	5	-	pF
$f_{clk(ADC)}$	ADC clock frequency				-	80	MHz
f_s	sampling frequency			-	-	5.0	Msamples/s
E_D	differential linearity error	1.62 V ≤ V_{DDA} ≤ 3.6 V 1.62 V ≤ VREFP ≤ 3.6 V $f_{clk(ADC)}$ = ≤ 72 MHz	[1][5]	-	±3.0	-	LSB
		2.0 V ≤ V_{DDA} ≤ 3.6 V 2.0 V ≤ VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	±3.0	-	LSB
		V_{DDA} = VREFP = 1.62 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	±7.1	-	LSB
$E_{L(adj)}$	integral non-linearity	1.62 V ≤ V_{DDA} ≤ 3.6 V 1.62 V ≤ VREFP ≤ 3.6 V $f_{clk(ADC)}$ ≤ 72 MHz	[1][6]	-	±5.0	-	LSB
		2.0 V ≤ V_{DDA} ≤ 3.6 V 2.0 V ≤ VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	±4.0	-	LSB
		V_{DDA} = VREFP = 1.62 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	±9.0	-	LSB
E_O	offset error	calibration enabled	[1][7]	-	±1.2	-	mV
$V_{err(FS)}$	full-scale error voltage	1.62 V ≤ V_{DDA} ≤ 2.0 V 1.62 V ≤ VREFP ≤ 2.0 V	[1][8]	-	±3.5		LSB
		2.0 V ≤ V_{DDA} ≤ 3.6 V 2.0 V ≤ VREFP ≤ 3.6 V		-	±2.0		LSB
Z_i	input impedance	f_s = 5.0 Msamples/s	[9][10]	17.0	-	-	kΩ

[1] Based on characterization; not tested in production.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] The input resistance of ADC channels 6 to 11 is higher than ADC channels 0 to 5.

[4] C_{ia} represents the external capacitance on the analog input channel for sampling speeds of 5.0 Msamples/s. No parasitic capacitances included.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 28.

[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 28.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 28.

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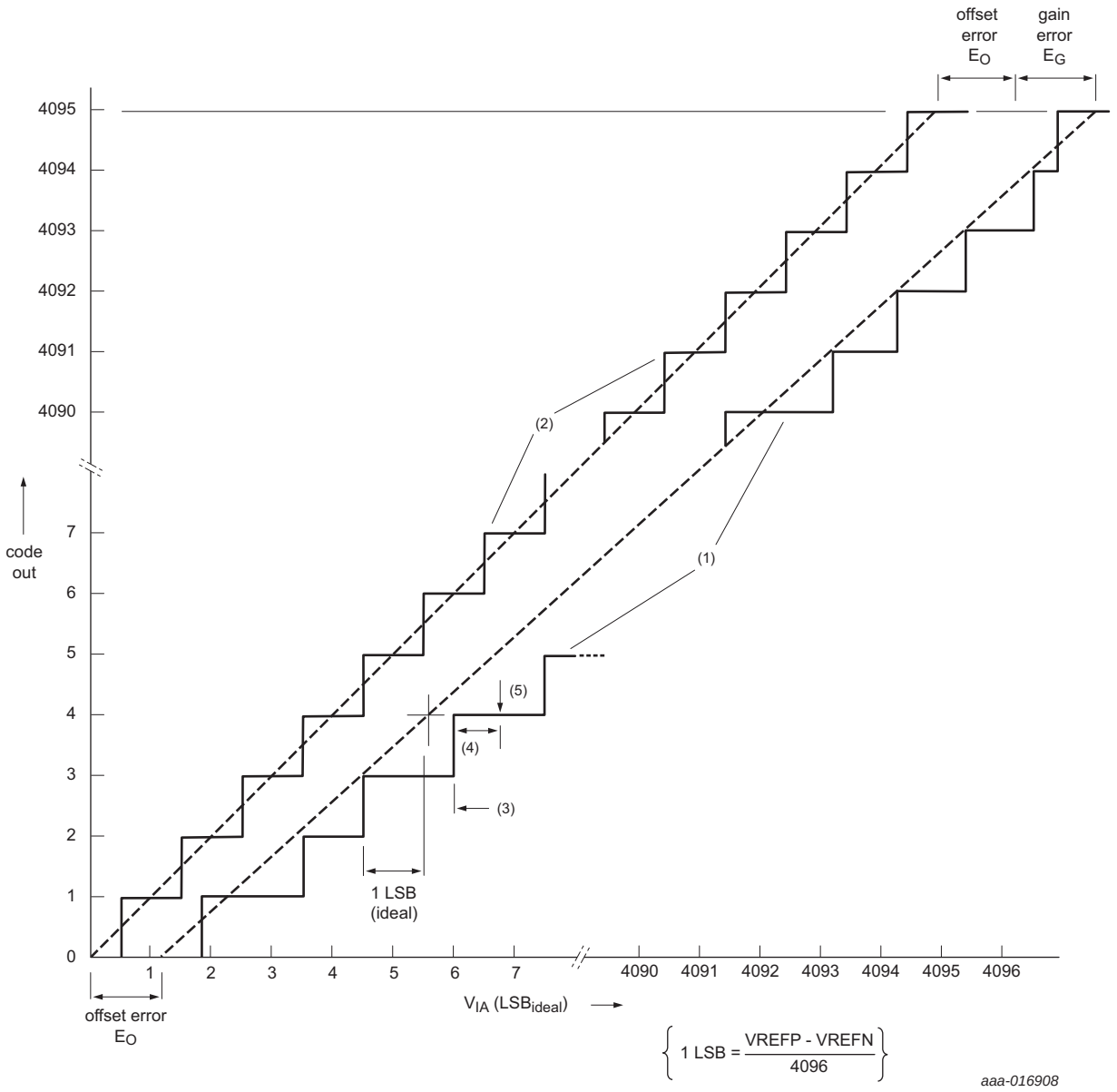
[8] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 28.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 5.0 Msamples/s and analog input capacitance C_{ia} = 5 pF.

[10] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 19 for C_{io}. See Figure 29.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 28. 12-bit ADC characteristics

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Table 38. ADC sampling times[1]

T_{amb} = -40 °C to 85 °C; 1.62 V ≤ V_{DDA} ≤ 3.6 V; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		23	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		26	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		31	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		47	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		75	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	15	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		18	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		20	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		24	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		38	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		62	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	12	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		13	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		15	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		19	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		30	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		48	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	9	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		10	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		11	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		13	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		22	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		36	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	43	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		46	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		50	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		56	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		74	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		105	-	-	ns

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Table 38. ADC sampling times[1] *...continued*

T_{amb} = -40 °C to 85 °C; 1.62 V ≤ V_{DDA} ≤ 3.6 V; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	35	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		38	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		40	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		46	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		61	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		86	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	27	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		29	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		32	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		36	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		48	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		69	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		22	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		23	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		26	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		36	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		51	-	-	ns

[1] Characterized through simulation. Not tested in production.

[2] The ADC default sampling time is 2.5 ADC clock cycles. To match a given analog source output impedance, the sampling time can be extended by adding up to seven ADC clock cycles for a maximum sampling time of 9.5 ADC clock cycles. See the TSAMP bits in the ADC CTRL register.

[3] Z_o = analog source output impedance.

12.2.1 ADC input impedance

Figure 29 shows the ADC input impedance. In this figure:

- ADCx represents slow ADC input channels 6 to 11.
- ADCy represents fast ADC input channels 0 to 5.
- R_1 and R_{sw} are the switch-on resistance on the ADC input channel.
- If fast channels (ADC inputs 0 to 5) are selected, the ADC input signal goes through R_{sw} to the sampling capacitor (C_{ia}).
- If slow channels (ADC inputs 6 to 11) are selected, the ADC input signal goes through R_1 + R_{sw} to the sampling capacitor (C_{ia}).
- Typical values, R_1 = 487 Ω, R_{sw} = 278 Ω
- See Table 19 for C_{io}.
- See Table 37 for C_{ia}.

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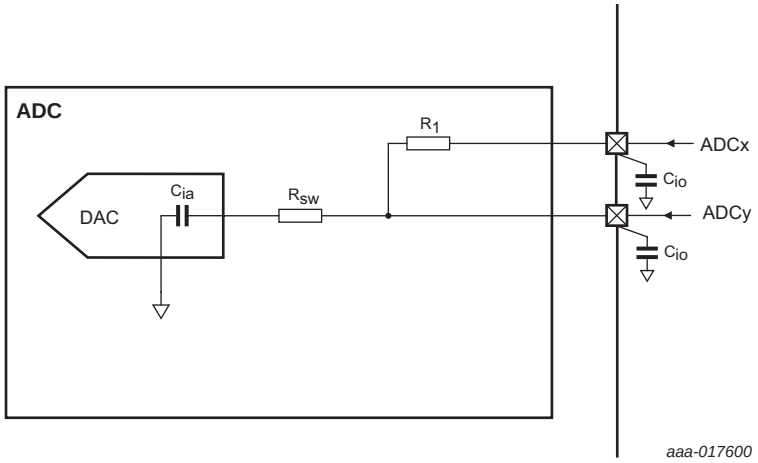

Fig 29. ADC input impedance

12.2.2 Temperature sensor

Table 39. Temperature sensor Linear-Least-Square (LLS) fit parameters
$V_{DD} = V_{DDA}$ = 1.62 V to 3.6 V

Fit parameter	Range		Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C	[1]	-	-2.0	-	mV/°C
LLS intercept at 0 °C	T_{amb} = −40 °C to +105 °C	[1]	-	590.0	-	mV
Value at 30 °C		[2]	521.0	-	540.0	mV

[1] Measured over typical samples.

[2] Measured for samples over process corners.

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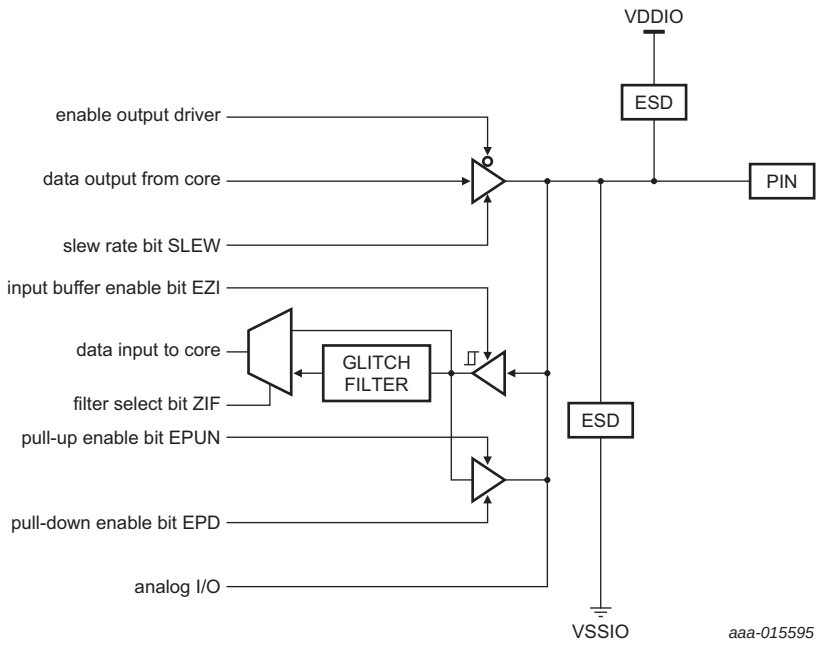
13. Application information

13.1 Standard I/O pin configuration

Figure 30 shows the possible pin modes for standard I/O pins:

- Digital output driver: enabled/disabled.
- Digital input: Pull-up enabled/disabled.
- Digital input: Pull-down enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Z mode; High impedance (no cross-bar currents for floating inputs).

The default configuration for standard I/O pins is Z mode. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.



The glitch filter rejects pulses of typical 12 ns width.

Fig 30. Standard I/O and $\overline{\text{RESET}}$ pin configuration

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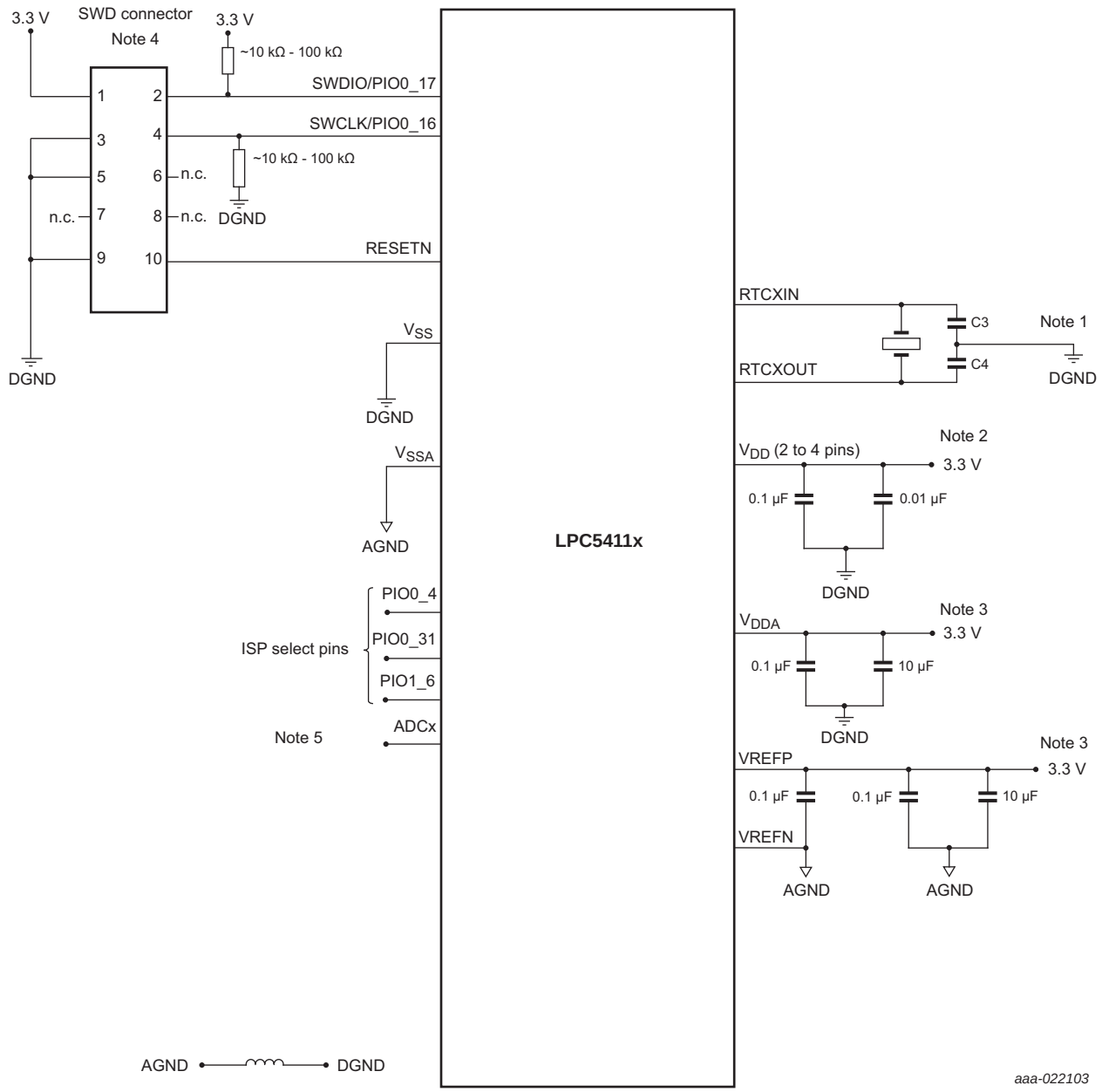
13.2 Connecting power, clocks, and debug functions



(1) See Section 13.4 “RTC oscillator” for the values of C3 and C4.

(2) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the ARM 10-pin interface for SWD.

(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 1.

Fig 31. Power, clock, and debug connections

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13.3 I/O power consumption

I/O pins can contribute to the overall static and dynamic power consumption of the part.

If pins are configured as digital inputs with the pull-up resistor enabled, a static current can flow depending on the voltage level at the pin. This current can be obtained using the parameters I_{pu} and I_{pd} given in Table 19.

If pins are configured as digital outputs, the static current is obtained from parameters IOH and IOL shown in Table 19, and any external load connected to the pin.

When an I/O pin switches in an application, it contributes to the dynamic power consumption because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 19 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

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13.4 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on RTCXIN and RTCXOUT. See Figure 32.

An external clock can be connected to RTCX1 if RTCX2 is left open. The recommended amplitude of the clock signal is $V_{i(RMS)}$ = 100 mV to 200 mV (<450 mV) with a coupling capacitance of 5 pF to 10 pF.

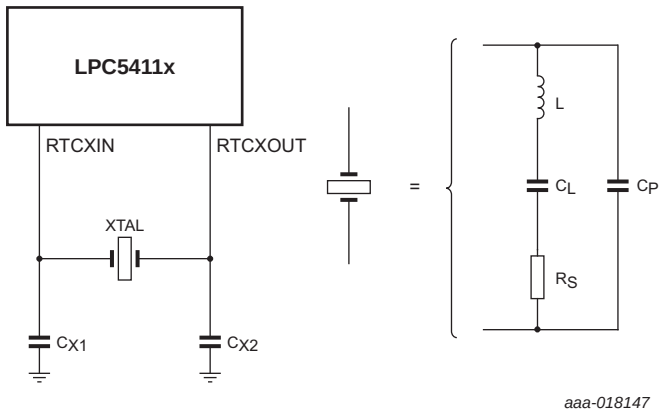

Fig 32. RTC oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the RTCXIN and RTCXOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, output the RTC Clock to one of the GPIOs and optimize the values of external load capacitors for minimum frequency deviation.

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13.4.1 RTC Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

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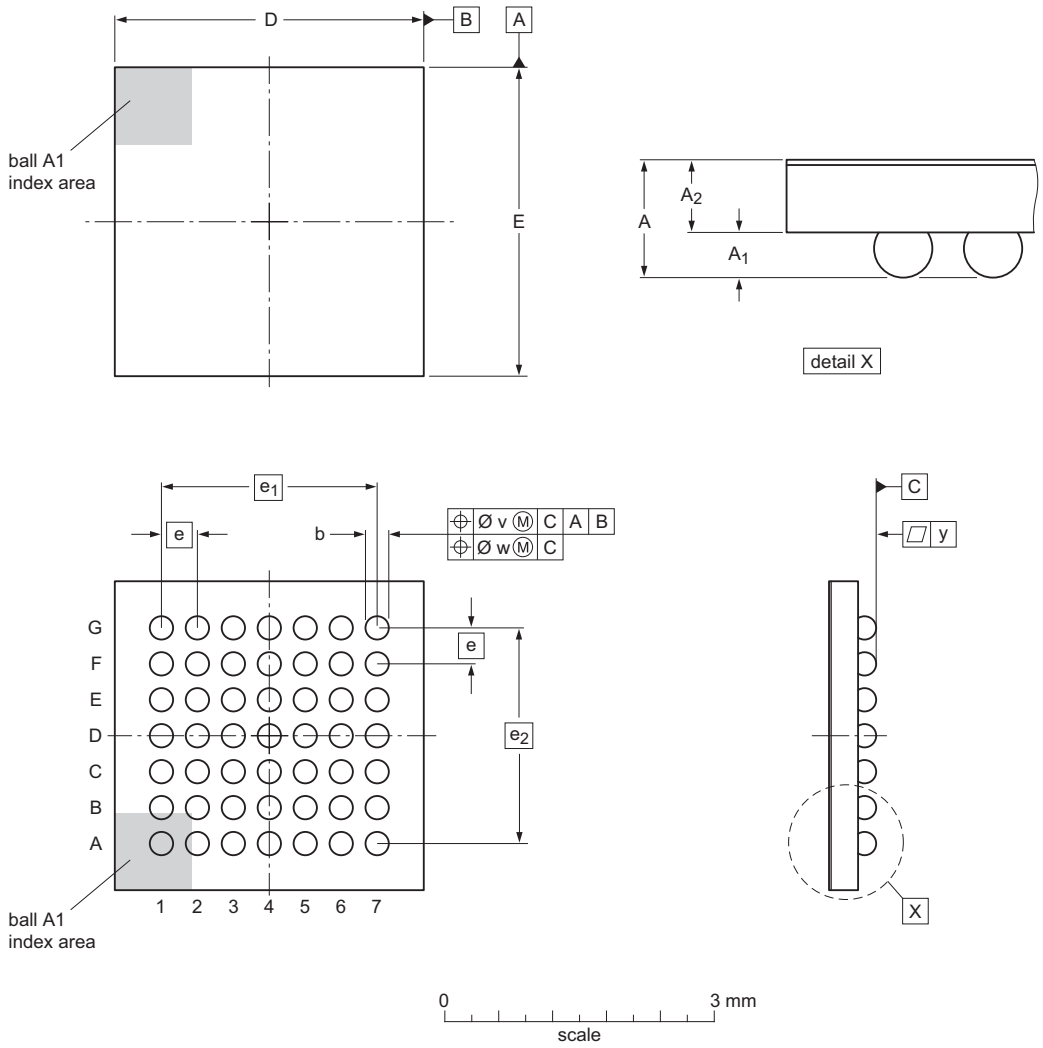
14. Package outline

WLCSP49: wafer level chip-scale package; 49 bumps; 3.44 x 3.44 x 0.525 mm (Backside coating included) **SOT1444-5**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.565	0.23	0.350	0.29	3.47	3.47						
	nom	0.525	0.20	0.325	0.26	3.44	3.44	0.4	2.4	2.4	0.05	0.015	0.03
	min	0.485	0.17	0.300	0.23	3.41	3.41						

Note
Backside coating 25 µm

sot1444-5_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1444-5		- - -				~~15-01-30~~ 16-01-20

Fig 33. WLCSP49 Package outline

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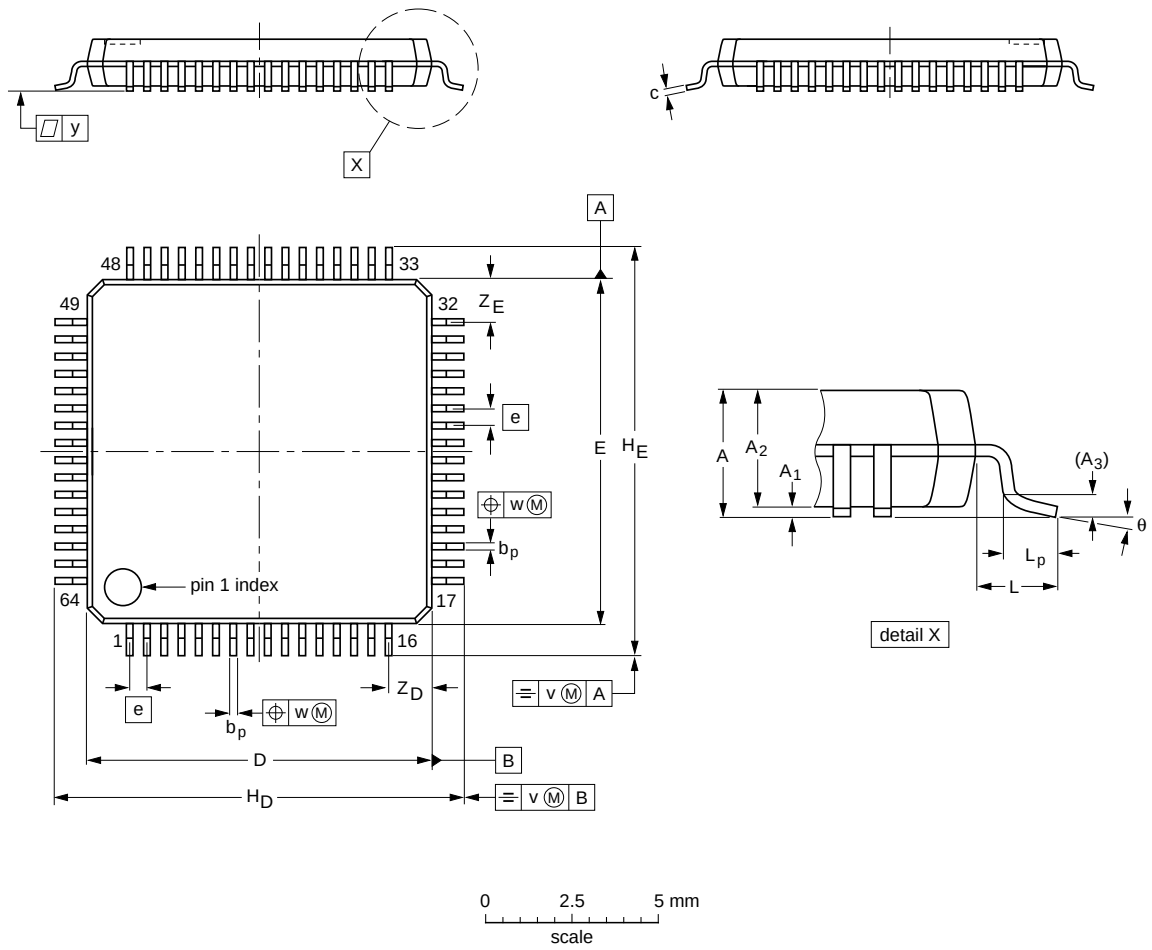
LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 34. LQFP64 Package outline

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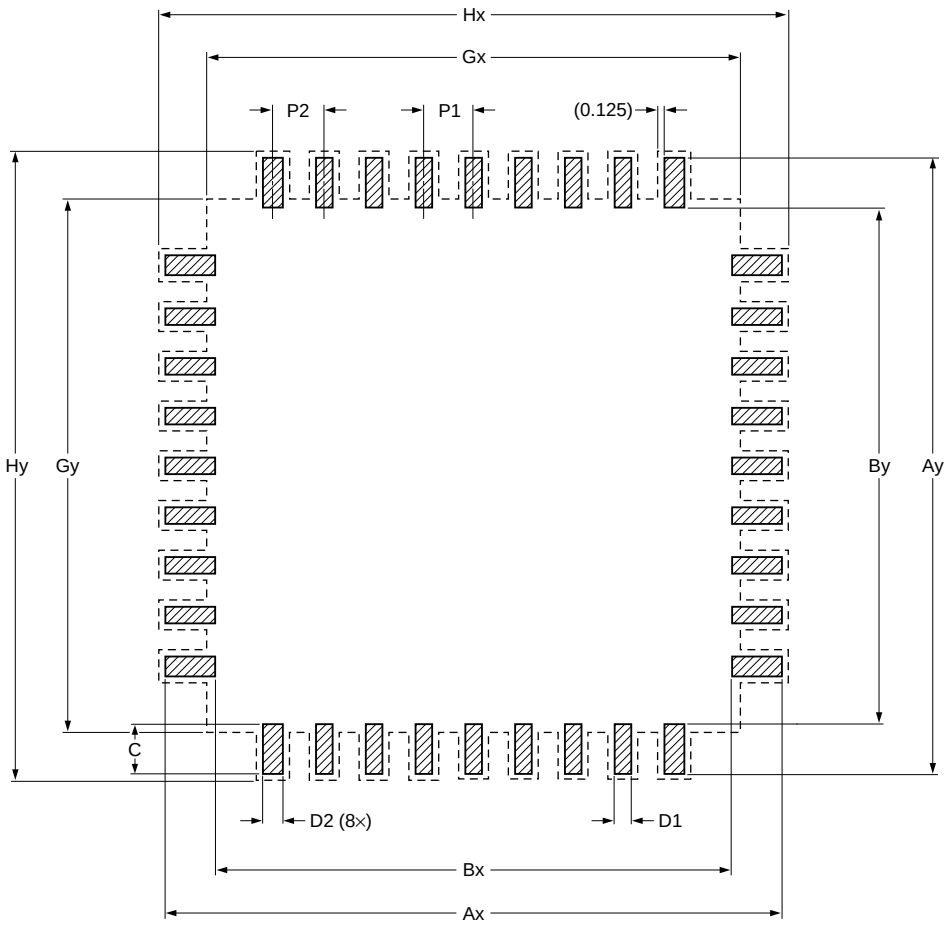
15. Soldering

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 35. LQFP64 Soldering footprint

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16. Abbreviations

Table 40. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
CDC	Communication Device Class
DMA	Direct Memory Access
FRO oscillator	Internal Free-Running Oscillator, tuned to the factory specified frequency
GPIO	General Purpose Input/Output
FRO	Free Running Oscillator
HID	Human Interface Device
LSB	Least Significant Bit
MCU	MicroController Unit
MSC	Mass Storage Device
PDM	Pulse Density Modulation
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
USART	Universal Asynchronous Receiver/Transmitter

17. References

[1] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

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18. Revision history

Table 41. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC5411x v.1.2	20160224	Product data sheet	-	LPC5411x v.1.1
Modifications:	• Updated Table 34 “Dynamic characteristics” on page 76: V_{DD} = 1.62 V to 3.6 V and table note is: Based on simulated values and for 2.7 V to 3.6 V. • Added Figure 11 “Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}” on page 52 and Figure 12 “Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}” on page 53.			
LPC5411x v.1.1	20160222	Product data sheet	-	LPC5411x v.1
Modifications:	• Fixed graphic numbers. • Updated Table 2 “Ordering options” on page 5. • Updated the list item in Section 2 “Features and benefits”: ROM-based USB drivers (HID, CDC, and MSC). • Updated Figure 6 “LPC5411x Memory mapping” on page 25 to include 128 KB on-chip flash and a note: The total size of flash and SRAM is part dependent. • Added Section 7.21.1.4 “RTC Oscillator” on page 39. • Updated figure note of Figure 9 “Typical CoreMark score” on page 48 to include “all peripherals disabled.” • Added table description: *T_{amb} = –40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V* to Table 14 “Static characteristics: Power consumption in sleep mode” on page 50. • Moved Figure 10 “CoreMark power consumption: typical mA/MHz for M4 and M0+ cores” after Table 14 “Static characteristics: Power consumption in sleep mode” on page 50. • Updated table notes to Table 17 “Typical peripheral power consumption[1][2][3]” on page 53. • Added Table 18 “Typical AHB/APB peripheral power consumption [3][4][5]” on page 53. • Removed table note: The values specified are simulated and absolute values, including package/bondwire capacitance from “Weak input pull-up/pull-down characteristics” heading of Table 19 “Static characteristics: pin characteristics” on page 55. • Renamed PLL0 to PLL. See Table 24 “PLL lock times and current” on page 64. • Added table description: *T_{amb} = –40 °C to +105 °C. V_{DD} = 1.62 V to 3.6 V to* Table 25 “Dynamic characteristics of the PLL[1]” on page 65. • Changed the symbol in Table 26 “Dynamic characteristic: FRO” on page 65 to $f_{osc(FRO)}$. • Added table note: Typical ratings are not guaranteed to Table 30 “Dynamic characteristics: I^2S-bus interface pins [1]” on page 67, Table 31 “SPI dynamic characteristics[1]” on page 71, and Table 32 “USART dynamic characteristics[1]” on page 74. • Updated footnote to: data based on characterization results, not tested in production. See Table 26 “Dynamic characteristic: FRO” on page 65. • Changed the order of the conditions for E_D and $E_{L(adj)}$ in Table 37 “12-bit ADC static characteristics” on page 79.			
LPC5411x v.1	20160216	Product data sheet	-	-

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19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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