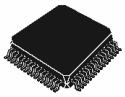
STM32F333Kx STM32F333Cx STM32F333Rx

ARM Cortex™-M4F 32b MCU+FPU, up to 64KB Flash+16KB SRAM, 2 ADCs, 3 DAC chan., 3 comp.,1 PGA, 10-channel high-resolution timer

Data brief

Features

- Core: ARM 32-bit Cortex®-M4F CPU (72 MHz max), single-cycle multiplication and HW division, and DSP instruction with FPU
- Memories
  - Up to 64 KB of Flash memory
  - Up to 12 KB of SRAM with HW parity check
  - 4 KB of SRAM on instruction bus with HW parity check (CCM)
- CRC calculation unit
- Reset and supply management
  - V_{DD}, V_{DDA} voltage range: 2.0 to 3.6 V
  - Power-on/Power-down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - Low power modes: Sleep, Stop, Standby
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x 16 PLL option
  - Internal 40 kHz oscillator
- Up to 52 fast I/O ports, all mappable on external interrupt vectors, several 5 V-tolerant
- 7-channel DMA controller
- Up to 2×ADC 0.20 µS (up to 22 channels) with selectable resolution of 12/10/8/6 bits, 0 to 3.6 V conversion range, separate analog supply from 2.0 to 3.6 V
- Temperature sensor
- 3x12-bit DAC channels
- 3 ultra-fast rail-to-rail analog comparators
- One operational amplifiers that can be used in PGA mode, all terminal accessible
- Up to 18 capacitive sensing channels supporting touchkeys, linear and rotary touchsensors



LQFP32 (7 × 7 mm)
LQFP48 (7 × 7 mm)
LQFP64 (10 × 10 mm)

- Up to 12 timers
  - High-resolution timer with 5x16-bit counters, 217ps resolution, 10 PWM outputs, 5 fault inputs, 10 external event inputs, 1 synchro. input, 1 synchro. output
  - 1x16-bit 6-channel advanced-control timer, with up to 6 PWM channels, deadtime generation and emergency stop
  - 1 x 32-bit timer and 1 x 16-bit timer with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 1x16-bit timer with 2 IC/OCs, 1 OCN/PWM, deadtime generation, emergency stop
  - 2x16-bit timers with IC/OC/OCN/PWM, deadtime generation and emergency stop
  - 2 watchdog timers (independent, window)
  - 1 SysTick timer: 24-bit downcounter
  - 2x16-bit basic timers to drive the DAC
- Calendar RTC with alarm, periodic wakeup from Stop/Standby
- Communication interfaces
  - CAN interface (2.0B Active)
  - One I^2C with 20 mA current sink to support Fast mode plus, SMBus/PMBus
  - Up to 3 USARTs, one with ISO 7816 interface, LIN, IrDA, modem control
  - One SPI
- Debug mode: serial wire debug (SWD), JTAG
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F333Kx	STM32F333K4/K6/K8
STM32F333Cx	STM32F333C4/C6/C8
STM32F333Rx	STM32F333R4/R6/R8

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1 Description

The STM32F333xx family is based on the high-performance ARM® Cortex™-M4 32-bit RISC core operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU). The family incorporates high-speed embedded memories (up to 64 Kbytes of Flash memory, up to 16 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The devices offer up to two fast 12-bit ADCs (5 Msps), up to three ultra-fast comparators, an operational amplifier, three DAC channels, a low-power RTC, one high-resolution timer, one general-purpose 32-bit timer, one timer dedicated to motor control, and four general-purpose 16-bit timers. They also feature standard and advanced communication interfaces:

- One I^2C
- One SPI
- Up to three USARTs
- One CAN

The STM32F333xx family operates in the –40 to +85 °C and –40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

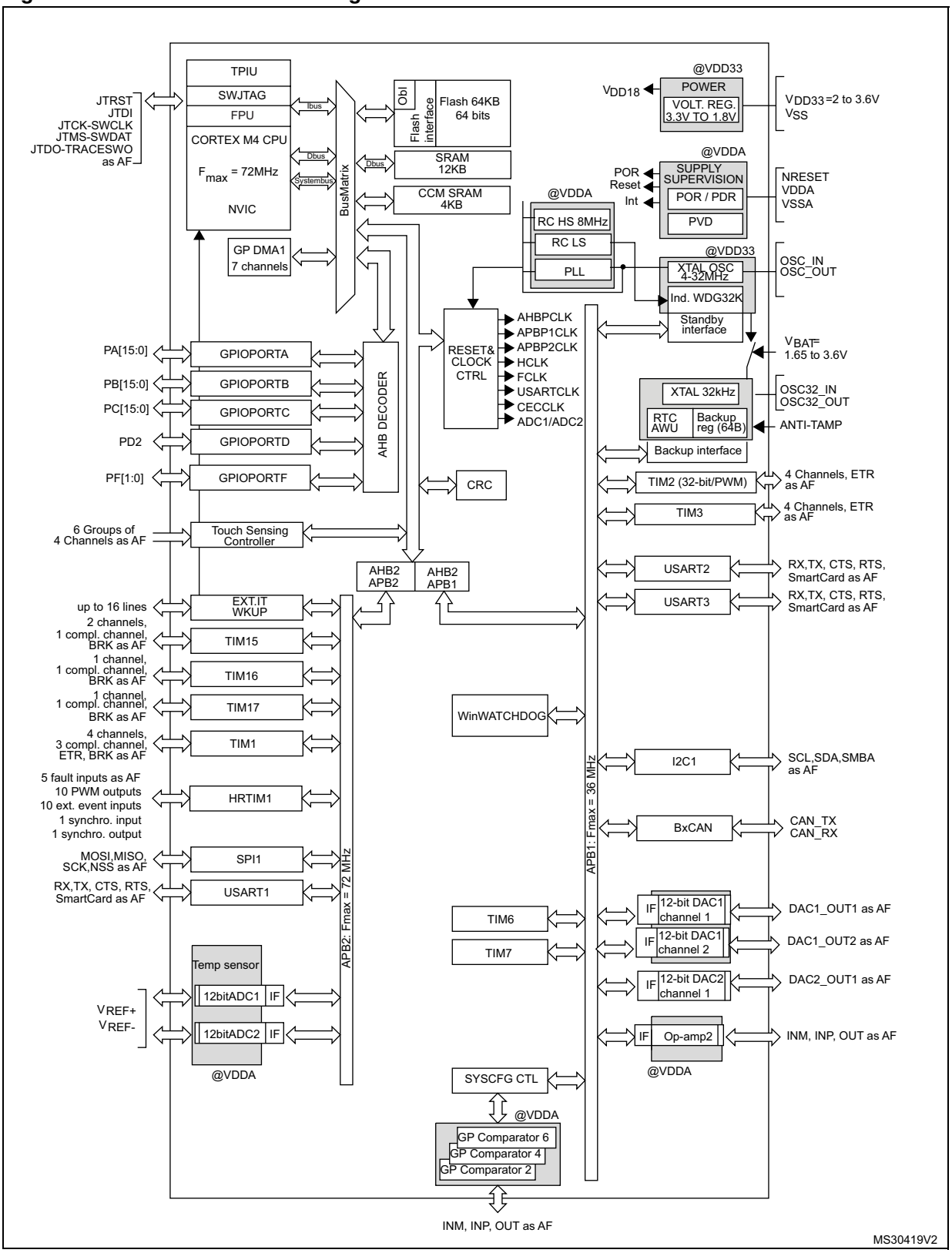
The STM32F333xx family offers devices in 32, 48 and 64-pin packages.

The set of included peripherals changes with the device chosen.

Table 2. STM32F333xx family device features and peripheral counts

Peripheral		STM32F333Kx			STM32F333Cx			STM32F333Rx		
Flash (Kbytes)		16	32	64	16	32	64	16	32	64
SRAM on data bus (Kbytes)		8	10	12	8	10	12	8	10	12
Core coupled memory SRAM on instruction bus (CCM SRAM) (Kbytes)		4								
Timers	High-resolution timer	1 (16 bits/ 10 channels)								
	Advanced control	1 (16-bit)								
	General purpose	4 (16-bit) 1 (32 bit)								
	Basic	2 (16-bit)								
	SysTick timer	1								
	Watchdog timers (independent, window)	2								
Comm. interfaces	SPI	1								
	I^2C	1								
	USART	2			3					
	CAN	1								
GPIOs	Normal I/Os (TC, TTa)	9			20			26		
	5-Volt tolerant I/Os (FT,FTf)	15			17			25		
DMA channels		7								
12-bit ADCs Number of channels		2 9			2 15			2 22		
12-bit DAC channels		3								
Ultra-fast analog comparator		2			3					
Operational amplifiers		1								
CPU frequency		72 MHz								
Operating voltage		2.0 to 3.6 V								
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C								
Packages		LQFP32			LQFP48			LQFP64		

Figure 1. STM32F333xx block diagram



1. AF: alternate function on I/O pins.

2 Functional overview

2.1 ARM® Cortex™-M4F core with embedded Flash and SRAM

The ARM Cortex-M4F processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4F 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F333xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagrams of the STM32F333xx family devices.

2.2 Memories

2.3 Embedded Flash memory

All STM32F333xx devices feature up to 64 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

2.4 Embedded SRAM

The STM32F333xx devices feature up to 16 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states, allowing the CPU to achieve 90 Dhrystone Mips at 72 MHz (when running code from CCM, core coupled memory).

The SRAM is organized as follows:

- 4 Kbytes of SRAM with parity check mapped on the instruction bus (core coupled memory or CCM) and used to execute critical routines or to access data
- 12 Kbytes of SRAM with parity check mapped on the data bus.

2.5 Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1, USART2, or I2C1.

2.6 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

2.7 Power management

2.7.1 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, DACs, comparators operational amplifiers, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the DACs and operational amplifiers are used). The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{BAT} = 1.6 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

2.7.2 Power supply supervisor

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated

when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

2.7.4 Low-power modes

The STM32F333xx supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm, COMPx, I2C or USARTx.

- Standby mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.8 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

2.9 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.10 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 7 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, high-resolution timer, DAC and ADC.

2.11 Interrupts and events

2.11.1 Nested vectored interrupt controller (NVIC)

The STM32F333xx devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

2.11.2 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of 27 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 51 GPIOs can be connected to the 16 external interrupt lines.

2.12 Fast analog-to-digital converter (ADC)

Two 5 MSPS fast analog-to-digital converters, with selectable resolution between 12 and 6 bit, are embedded in the STM32F333xx family devices. The ADCs have up to 22 external channels. Some of the external channels are shared between ADC1and 2, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADCs also have internal channels: temperature sensor connected to ADC1 channel 16, $V_{BAT}/2$ connected to ADC1 channel 17, voltage reference V_{REFINT} connected both to ADC1 and ADC2 channel 18, and VOPAMP2 connected to ADC2 channel 17.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single-shunt phase current reading techniques.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) and the high-resolution timer (HRTIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.12.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

2.12.2 Internal voltage reference (VREFINT)

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and Comparators. VREFINT is internally connected to the ADC_IN18 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

2.12.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN17. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

2.12.4 OPAMP2 reference voltage (VOPAMP2)

OPAMP2 reference voltage can be measured using ADC2 internal channel 17.

2.13 Digital-to-analog converter (DAC)

One 12-bit buffered DAC channel (DAC1_OUT1) and two 12-bit unbuffered DAC channels (DAC1_OUT2 and DAC2_OUT1) can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Three DAC output channels
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

2.14 Operational amplifier

The STM32F333xx embeds an operational amplifier with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8 MHz GBP
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to 2, 4, 8 or 16.

2.15 Ultra-fast comparators (COMP)

The STM32F333xx devices embed three ultra-fast rail-to-rail comparators which offer the features below:

- Programmable internal or external reference voltage
- Programmable hysteresis
- Selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers.

2.16 Timers and watchdogs

The STM32F333xx includes advanced control timer, 5 general-purpose timers, basic timer, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 3. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare Channels	Complementary outputs
High-resolution timer	HRTIM1	16-bit	Up	/1 /2 /4 x2 x4 x8 x16 x32	Yes	10	Yes
Advanced control	TIM1	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

2.16.1 High-resolution timer (HRTIM1)

The high-resolution timer (HRTIM1) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 6 timers, 1 master and 5 slaves, totaling 10 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 5 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

HRTIM1 timer is made of a digital kernel clocked at 144 MHz followed by delay lines. Delay lines with closed loop control guarantee a 217ps resolution whatever the voltage, temperature or chip-to-chip manufacturing process deviation. The high-resolution is available on the 10 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user defined timings and external events such as analog or digital feedbacks signals.

HRTIM1 timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, burst mode controller, push-pull and resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

In debug mode, the HRTIM1 counters can be frozen and the PWM outputs enter safe state.

2.16.2 Advanced timer (TIM1)

The advanced-control timer can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 2.16.3* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

2.16.3 General-purpose timers (TIM2, TIM3, TIM15, TIM16, TIM17)

There are up to three synchronizable general-purpose timers embedded in the STM32F333xx (see *Table 3* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2 and TIM3

  They are full-featured general-purpose timers:

  – TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 has 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  These three timers general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

2.16.4 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

2.16.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

2.16.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.16.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.17 Real-time clock (RTC) and backup registers

The RTC and the 5 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the VBAT pin. The backup registers are sixteen 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synbchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

2.18 Communication interfaces

2.18.1 Inter-integrated circuit interface (I^2C)

The devices feature an I^2C bus interface which can operate in multimaster and slave mode. It can support standard (up to 100 KHz), fast (up to 400 KHz) and fast mode + (up to 1 MHz) modes.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). It also includes programmable analog and digital noise filters.

Table 4. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Disabled when Wakeup from Stop mode is enabled

In addition, it provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. It also has a clock domain independent from the CPU clock, allowing the I2Cx (x=1,2) to wake up the MCU from Stop mode on address match.

The I2C interface can be served by the DMA controller.

2.18.2 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F333xx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9Mbits/s.

USART1 provides hardware management of the CTS and RTS signals. It supports IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and has LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

2.18.3 Serial peripheral interface (SPI)

An SPI interface allows to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

2.18.4 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames

with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

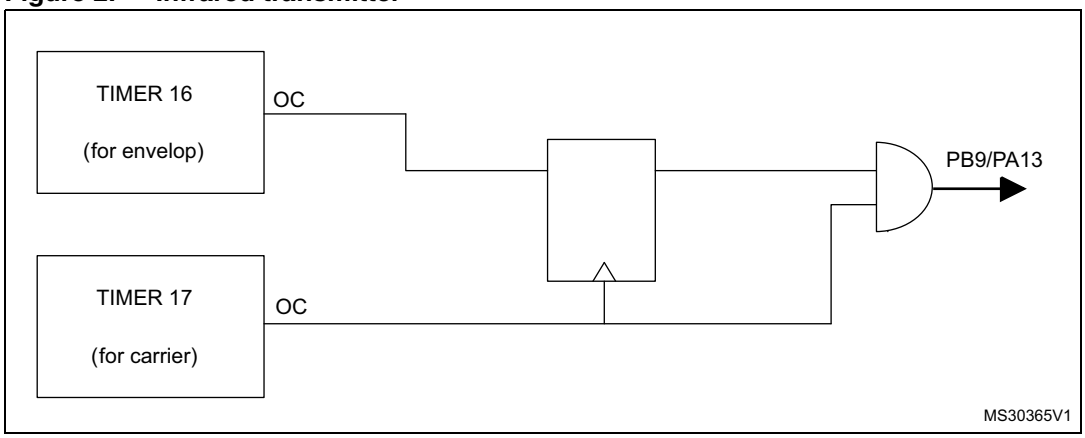
2.19 Infrared transmitter

The STM32F333xx devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 2. Infrared transmitter



2.20 Touch sensing controller (TSC)

The STM32F333xx devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/Os group.

Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 5. Capacitive sensing GPIOs available on STM32F333xx devices

Group	Capacitive sensing group name	Pin name	Group	Capacitive sensing group name	Pin name
1	TSC_G1_IO1	PA0	4	TSC_G4_IO1	PA9
	TSC_G1_IO2	PA1		TSC_G4_IO2	PA10
	TSC_G1_IO3	PA2		TSC_G4_IO3	PA13
	TSC_G1_IO4	PA3		TSC_G4_IO4	PA14
2	TSC_G2_IO1	PA4	5	TSC_G5_IO1	PB3
	TSC_G2_IO2	PA5		TSC_G5_IO2	PB4
	TSC_G2_IO3	PA6		TSC_G5_IO3	PB6
	TSC_G2_IO4	PA7		TSC_G5_IO4	PB7
3	TSC_G3_IO1	PC5	6	TSC_G6_IO1	PB11
	TSC_G3_IO2	PB0		TSC_G6_IO2	PB12
	TSC_G3_IO3	PB1		TSC_G6_IO3	PB13
	TSC_G3_IO4	PB2		TSC_G6_IO4	PB14

2.21 Development support

2.21.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinouts and pin description

Figure 3. LQFP32 pinout

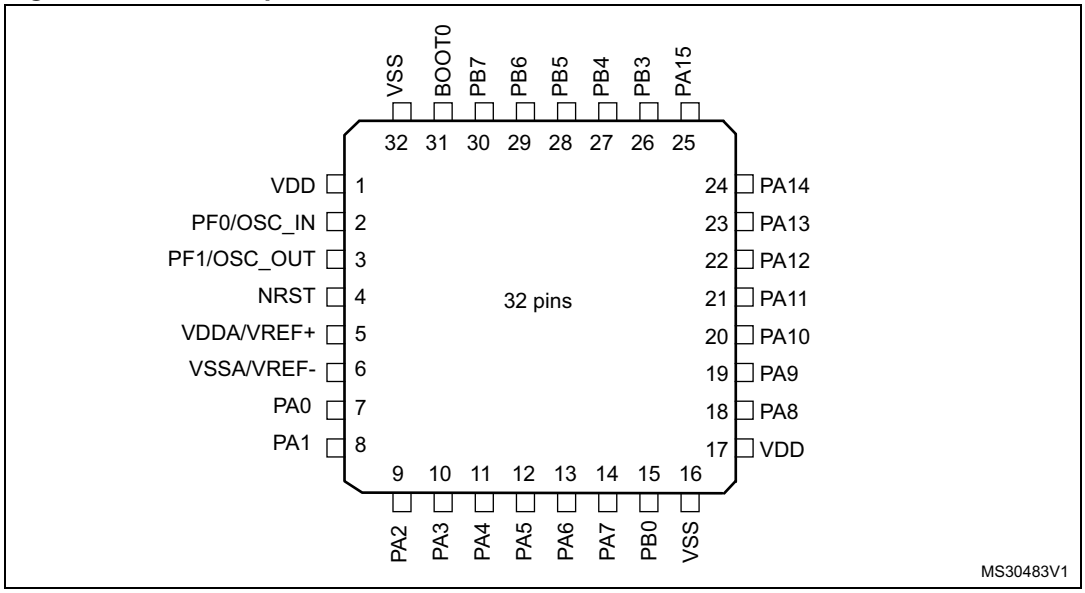


Figure 4. LQFP48 pinout

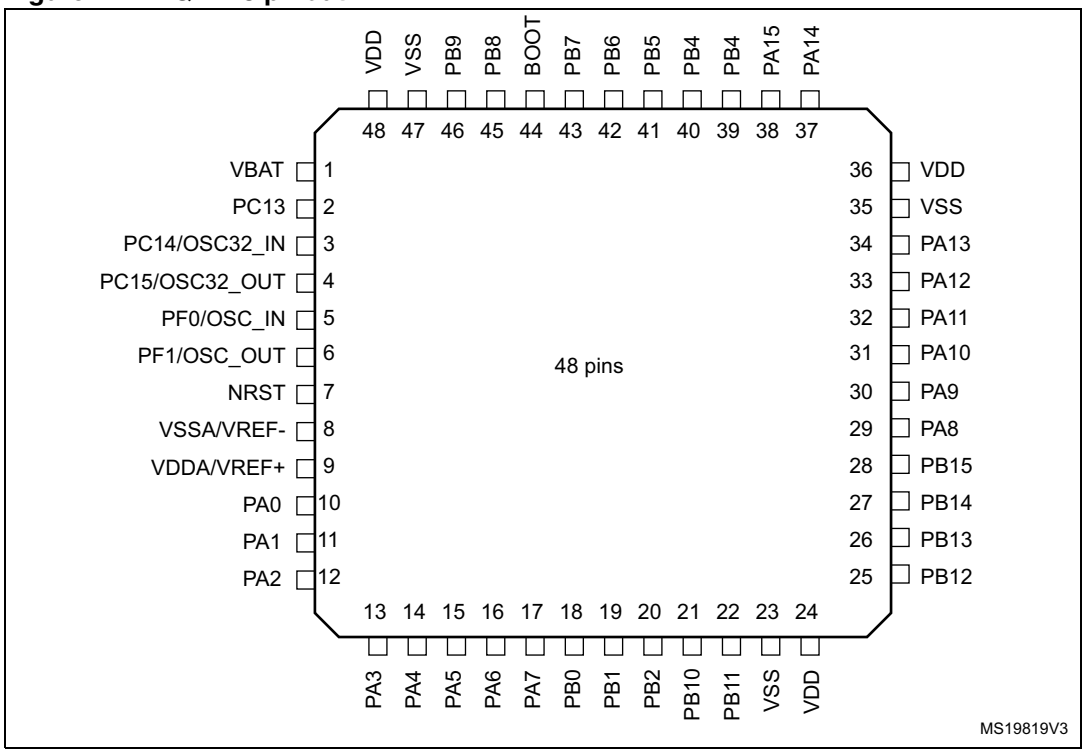


Figure 5. LQFP64 pinout

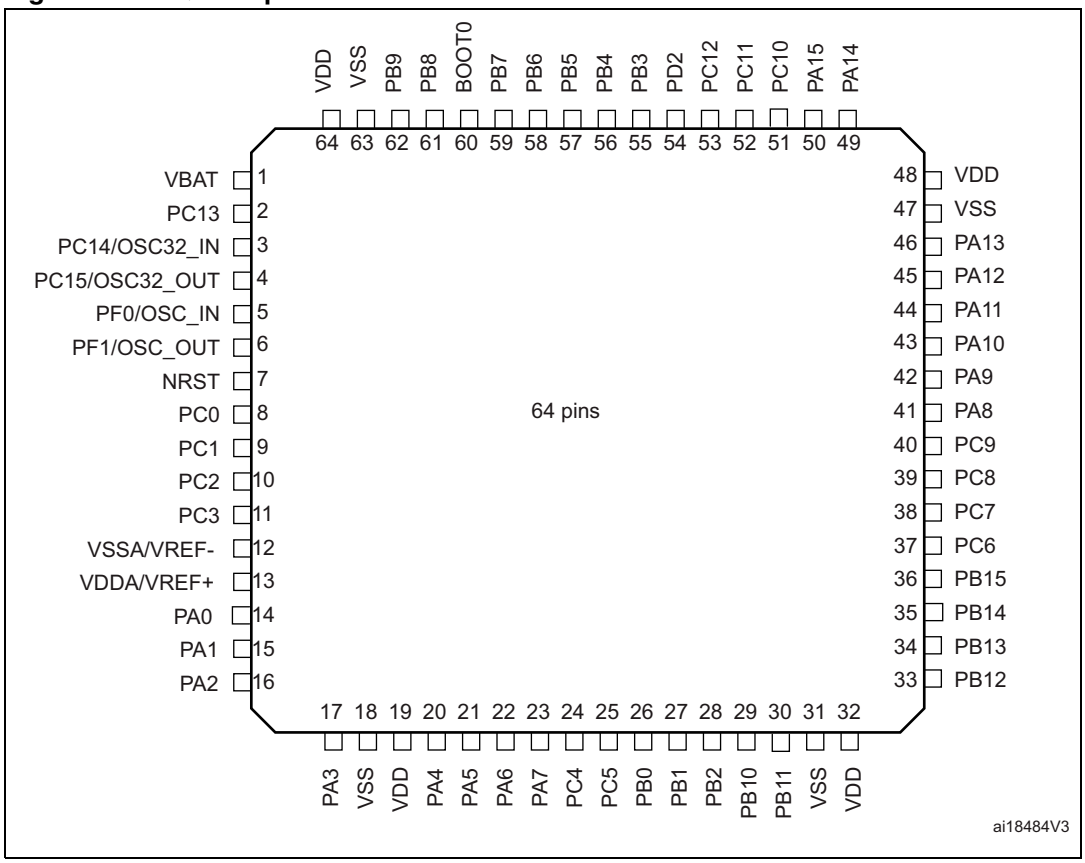


Table 6. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 7. STM32F333xx pin definitions

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP 64	LQFP 48	LQFP 32					Alternate functions	Additional functions
1	1	-	V_{BAT}	S			Backup power supply	
2	2	-	PC13	I/O	TC		TIM1_CH1N	WKUP2,RTC_TAMPER1, RTC_TS,RTC_OUT
3	3	-	PC14/OSC32_IN	I/O	TC			OSC32_IN
4	4	-	PC15/OSC32_OUT	I/O	TC			OSC32_OUT
5	5	2	PF0/OSC_IN	I/O	FT		TIM1_CH3N	OSC_IN
6	6	3	PF1/OSC_OUT	I/O	FT			OSC_OUT
7	7	4	NRST	I/O	RST		Device reset input / internal reset output (active low)	
8	-	-	PC0	I/O	TTa		TIM1_CH1	ADC12_IN6
9	-	-	PC1	I/O	TTa		TIM1_CH2	ADC12_IN7
10	-	-	PC2	I/O	TTa		TIM1_CH3	ADC12_IN8
11	-	-	PC3	I/O	TTa		TIM1_BKIN2, TIM1_CH4	ADC12_IN9

Table 7. STM32F333xx pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP 64	LQFP 48	LQFP 32					Alternate functions	Additional functions
12	8	6	V_{SSA}/V_{REF-}	S				
13	9	5	V_{DDA}/V_{REF+}	S				
14	10	7	PA0	I/O	TTa		USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1	ADC1_IN1, RTC_ TAMP2, WKUP1
15	11	8	PA1	I/O	TTa		USART2_RTS, TIM2_CH2, TSC_G1_IO2, TIM15_CH1N	ADC1_IN2
16	12	9	PA2	I/O	TTa		USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3, COMP2_OUT	ADC1_IN3, COMP2_INM
17	13	10	PA3	I/O	TTa		USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4,	ADC1_IN4
18	-	-	VSS	S				
19	-	-	V_{DD}	S				
20	14	11	PA4	I/O	TTa		SPI1_NSS USART2_CK, TSC_G2_IO1 TIM3_CH2	DAC1_OUT1, ADC2_IN1, COMP2_INM4, COMP4_INM4, COMP6_INM4
21	15	12	PA5	I/O	TTa		SPI1_SCK, TIM2_CH1_ETR, TSC_G2_IO2	DAC1_OUT2, ADC2_IN2, OPAMP2_VINM
22	16	13	PA6	I/O	TTa		SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, TSC_G2_IO3	DAC2_OUT1, ADC2_IN3, AOP2_OUT
23	17	14	PA7	I/O	TTa		SPI1_MOSI, TIM3_CH2, TIM17_CH1, TIM1_CH1N, TSC_G2_IO4	ADC2_IN4, COMP2_INP, OPAMP2_VINP
24	-	-	PC4	I/O	TTa		USART1_TX, TIM1_ETR	ADC2_IN5

Table 7. STM32F333xx pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP 64	LQFP 48	LQFP 32					Alternate functions	Additional functions
25	-	-	PC5	I/O	TTa		USART1_RX, TSC_G3_IO1, TIM15_BKIN	ADC2_IN11, OPAMP2_VINM
26	18	15	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, TSC_G3_IO2	ADC1_IN11, COMP4_INP, OPAMP2_VINP
27	19	-	PB1	I/O	TTa		HRTIM1_SCOUT, TIM3_CH4, TIM1_CH3N, COMP4_OUT, TSC_G3_IO3	ADC1_IN12
28	20	-	PB2	I/O	TTa		HRTIM1_SCIN, TSC_G3_IO4	ADC2_IN12, COMP4_INM
29	21	-	PB10	I/O	TTa		HRTIM1_FLT3, USART3_TX, TIM2_CH3, TSC_SYNC	
30	22	-	PB11	I/O	TTa		HRTIM1_FLT4, USART3_RX, TIM2_CH4, TSC_G6_IO1	COMP6_INP
31	23	16	V_{SS}	S			Digital ground	
32	24	17	V_{DD}	S			Digital power supply	
33	25	-	PB12	I/O	TTa		HRTIM1_CHC1, USART3_CK, TIM1_BKIN, TSC_G6_IO2	ADC2_IN13
34	26	-	PB13	I/O	TTa		HRTIM1_CHC2, USART3_CTS, TIM1_CH1N, TSC_G6_IO3	ADC1_IN13
35	27	-	PB14	I/O	TTa		HRTIM1_CHD1, USART3_RTS, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	ADC2_IN14, OPAMP2_VINP
36	28	-	PB15	I/O	TTa		HRTIM1_CHD2, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	ADC2_IN15, COMP6_INM, RTC_REFIN

Table 7. STM32F333xx pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP 64	LQFP 48	LQFP 32					Alternate functions	Additional functions
37	-	-	PC6	I/O	FT		HRTIM1_EEV10, TIM3_CH1, COMP6_OUT	
38	-	-	PC7	I/O	FT		HRTIM1_FLT5, TIM3_CH2	
39	-	-	PC8	I/O	FT		HRTIM1_CHE1, TIM3_CH3	
40	-	-	PC9	I/O	FT		HRTIM1_CHE2, TIM3_CH4	
41	29	18	PA8	I/O	FT		HRTIM1_CHA1, USART1_CK, TIM1_CH1, MCO	
42	30	19	PA9	I/O	FTf		HRTIM1_CHA2, USART1_TX, TIM1_CH2, TIM2_CH3, TIM15_BKIN TSC_G4_IO1	
43	31	20	PA10	I/O	FTf		HRTIM1_CHB1, USART1_RX, TIM1_CH3, TIM2_CH4, TIM17_BKIN, TSC_G4_IO2, COMP6_OUT	
44	32	21	PA11	I/O	FTf		HRTIM1_CHB2, USART1_CTS, CAN_RX, TIM1_CH1N, TIM1_CH4, TIM1_BKIN2	
45	33	22	PA12	I/O	FT		HRTIM1_FLT1, USART1_RTS, CAN_TX, TIM1_CH2N, TIM1_ETR, TIM16_CH1, COMP2_OUT	
46	34	23	PA13	I/O	FT		USART3_CTS, TIM16_CH1N, TSC_G4_IO3, IR_OUT, JTMS-SWDAT	

Table 7. STM32F333xx pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP 64	LQFP 48	LQFP 32					Alternate functions	Additional functions
47	35	-	V_{SS}	S				
48	36	-	V_{DD}	S				
49	37	24	PA14	I/O	FTf		I2C1_SDA, USART2_TX, TIM1_BKIN, TSC_G4_IO4, JTCK-SWCLK	
50	38	25	PA15	I/O	FTf		HRTIM1_FLT2, I2C1_SCL, SPI1_NSS, USART2_RX, TIM1_BKIN, TIM2_CH1_ETR, JTDI	
51	-	-	PC10	I/O	FT		USART3_TX	
52	-	-	PC11	I/O	FT		HRTIM1_EEV2, USART3_RX	
53	-	-	PC12	I/O	FT		HRTIM1_EEV1, USART3_CK	
54	-	-	PD2	I/O	FT		TIM3_ETR	
55	39	26	PB3	I/O	FT		HRTIM1_EEV9, HRTIM1_SCOUT SPI1_SCK, USART2_TX, TIM2_CH2, TIM3_ETR, TSC_G5_IO1, JTDO-TRACESWO	
56	40	27	PB4	I/O	FT		HRTIM1_EEV7, SPI1_MISO, USART2_RX, TIM3_CH1, TIM16_CH1, TIM17_BKIN, TSC_G5_IO2, NJTRST	
57	41	28	PB5	I/O	FT		HRTIM1_EEV6, SPI1_MOSI, I2C1_SMBA, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM17_CH1	

Table 7. STM32F333xx pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP 64	LQFP 48	LQFP 32					Alternate functions	Additional functions
58	42	29	PB6	I/O	FTf		HRTIM1_SCIN, HRTIM1_EEV4, I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_IO3	
59	43	30	PB7	I/O	FTf		HRTIM1_EEV3, I2C1_SDA, USART1_RX, TIM3_CH4, TIM17_CH1N, TSC_G5_IO4	
60	44	31	BOOT0	I	B			
61	45	-	PB8	I/O	FTf		HRTIM1_EEV8, I2C1_SCL, CAN_RX, USART3_RX, TIM16_CH1, TIM1_BKIN, TSC_SYNC	
62	46	-	PB9	I/O	FTf		HRTIM1_EEV5, I2C1_SDA, CAN_TX, USART3_TX, TIM17_CH1, IR_OUT, COMP2_OUT	
63	47	32	V_{SS}	S				
64	48	-	V_{DD}	S				

Table 8. Alternate functions

AF n°	Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
7	PA0		TIM2_ CH1_ ETR		TSC_G1 _IO1				USART2 _CTS								EVEN TOUT
5	PA1		TIM2_ CH2		TSC_G1 _IO2				USART2 _RTS		TIM15_ CH1N						EVEN TOUT
6	PA2		TIM2_ CH3		TSC_G1 _IO3				USART2 _TX	COMP2 _OUT	TIM15_ CH1						EVEN TOUT
5	PA3		TIM2_ CH4		TSC_G1 _IO4				USART2 _RX		TIM15_ CH2						EVEN TOUT
6	PA4			TIM3_ CH2	TSC_G2 _IO1		SPI1_ NSS		USART2 _CK								EVEN TOUT
4	PA5		TIM2_ CH1_ ETR		TSC_G2 _IO2		SPI1_ SCK										EVEN TOUT
8	PA6		TIM16_ CH1	TIM3_ CH1	TSC_G2 _IO3		SPI1_ MISO	TIM1_ BKIN									EVEN TOUT
8	PA7		TIM17_ CH1	TIM3_ CH2	TSC_G2 _IO4		SPI1_ MOSI	TIM1_ CH1N									EVEN TOUT
8	PA8	MCO						TIM1_ CH1	USART1 _CK						HRTIM1 _CHA1		EVEN TOUT
9	PA9				TSC_G4 _IO1			TIM1_ CH2	USART1 _TX		TIM15_ BKIN	TIM2_ CH3			HRTIM1 _CHA2		EVEN TOUT
9	PA10		TIM17_ BKIN		TSC_G4 _IO2			TIM1_ CH3	USART1 _RX	COMP6 _OUT		TIM2_ CH4			HRTIM1 _CHB1		EVEN TOUT
9	PA11							TIM1_ CH1N	USART1 _CTS		CAN_RX		TIM1_ CH4	TIM1_ BKIN2	HRTIM1 _CHB2		EVEN TOUT
9	PA12		TIM16_ CH1					TIM1_ CH2N	USART1 _RTS	COMP2 _OUT	CAN_TX		TIM1_ ETR		HRTIM1 _FLT1		EVEN TOUT

Table 8. Alternate functions (continued)

AF n°	Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
7	PA13	JTMS-SWDAT	TIM16_CH1N		TSC_G4_IO3		IR-OUT		USART3_CTS								EVENTOUT
7	PA14	JTCK-SWCLK			TSC_G4_IO4	I2C1_SDA		TIM1_BKIN	USART2_TX								EVENTOUT
9	PA15	JTDI	TIM2_CH1_ETR			I2C1_SCL	SPI1_NSS		USART2_RX		TIM1_BKIN				HRTIM1_FLT2		EVENTOUT
5	PB0			TIM3_CH3	TSC_G3_IO2			TIM1_CH2N									EVENTOUT
6	PB1			TIM3_CH4	TSC_G3_IO3			TIM1_CH3N		COMP4_OUT					HRTIM1_SCOUT		EVENTOUT
2	PB2				TSC_G3_IO4										HRTIM1_SCIN		EVENTOUT
10	PB3	JTDO-TRACESWO	TIM2_CH2		TSC_G5_IO1		SPI1_SCK		USART2_TX			TIM3_ETR		HRTIM1_SCOUT	HRTIM1_EEV9		EVENTOUT
10	PB4	NJTRST	TIM16_CH1	TIM3_CH1	TSC_G5_IO2		SPI1_MISO		USART2_RX			TIM17_BKIN			HRTIM1_EEV7		EVENTOUT
9	PB5		TIM16_BKIN	TIM3_CH2		I2C1_SMBA	SPI1_MOSI		USART2_CK			TIM17_CH1			HRTIM1_EEV6		EVENTOUT
9	PB6		TIM16_CH1N		TSC_G5_IO3	I2C1_SCL			USART1_TX					HRTIM1_SCIN	HRTIM1_EEV4		EVENTOUT
8	PB7		TIM17_CH1N		TSC_G5_IO4	I2C1_SDA			USART1_RX			TIM3_CH4			HRTIM1_EEV3		EVENTOUT
10	PB8		TIM16_CH1		TSC_SYNCH	I2C1_SCL			USART3_RX		CAN_RX			TIM1_BKIN	HRTIM1_EEV8		EVENTOUT
9	PB9		TIM17_CH1			I2C1_SDA		IR-OUT	USART3_TX	COMP2_OUT	CAN_TX				HRTIM1_EEV5		EVENTOUT
4	PB10		TIM2_CH3		TSC_SYNCH				USART3_TX						HRTIM1_FLT3		EVENTOUT

Table 8. Alternate functions (continued)

AF n°	Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
4	PB11		TIM2_ CH4		TSC_G6 _IO1				USART3 _RX						HRTIM1 _FLT4		EVEN TOUT
6	PB12				TSC_G6 _IO2			TIM1_ BKIN	USART3 _CK						HRTIM1 _CHC1		EVEN TOUT
5	PB13				TSC_G6 _IO3			TIM1_ CH1N	USART3 _CTS						HRTIM1 _CHC2		EVEN TOUT
6	PB14		TIM15_ CH1		TSC_G6 _IO4			TIM1_ CH2N	USART3 _RTS						HRTIM1 _CHD1		EVEN TOUT
5	PB15		TIM15_ CH2	TIM15_ CH1N		TIM1_ CH3N									HRTIM1 _CHD2		EVEN TOUT
1	PC0		EVENT OUT	TIM1_ CH1													
1	PC1		EVENT OUT	TIM1_ CH2													
2	PC2		EVENT OUT	TIM1_ CH3													
2	PC3		EVENT OUT	TIM1_ CH4				TIM1_ BKIN2									
2	PC4		EVENT OUT	TIM1_ ETR					USART1 _TX								
3	PC5		EVENT OUT	TIM1_ BKIN	TSC_G3 _IO1				USART1 _RX								
5	PC6		EVENT OUT	TIM3_ CH1	HRTIM1 _EEV10				COMP6_ OUT								
5	PC7		EVENT OUT	TIM3_ CH2	HRTIM1 _FLT5												
4	PC8		EVENT OUT	TIM3_ CH3	HRTIM1 _CHE1												

Table 8. Alternate functions (continued)

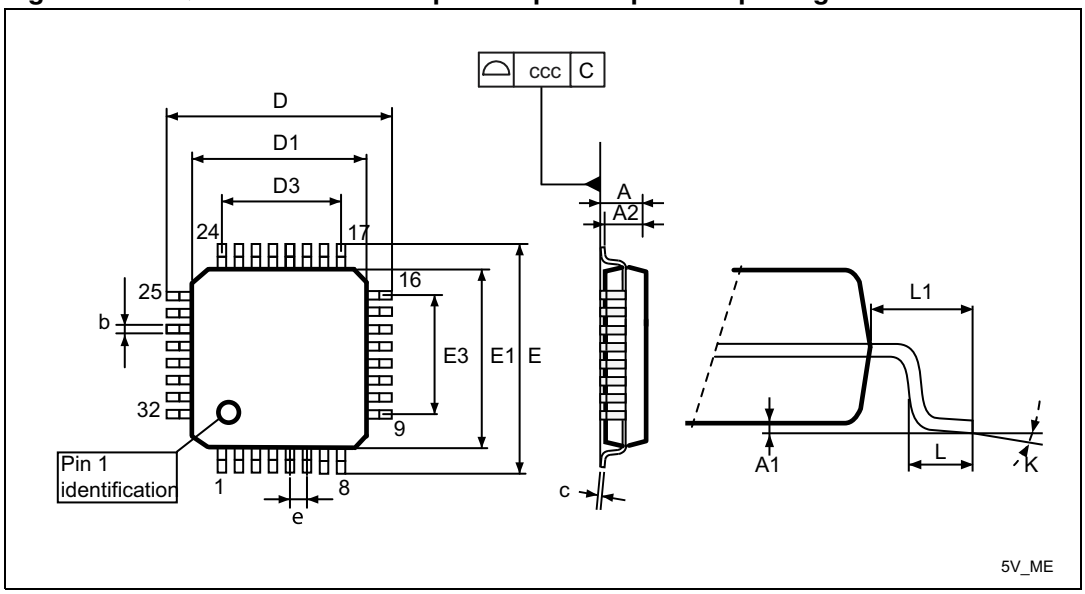
AF n°	Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
5	PC9		EVENT OUT	TIM3_ CH4	HRTIM1 _CHE2												
5	PC10		EVENT OUT						USART3 _TX								
5	PC11		EVENT OUT		HRTIM1 _EEV2				USART3 _RX								
5	PC12		EVENT OUT		HRTIM1 _EEV1				USART3 _CK								
1	PC13					TIM1_ CH1N											
0	PC14																
0	PC15																
4	PD2		EVENT OUT	TIM3_ ETR													
2	PF0							TIM1_ CH3N									
1	PF1																

4 Package characteristics

4.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 6. LQFP32 - 7 x 7mm 32-pin low-profile quad flat package outline



1. Drawing is not to scale.

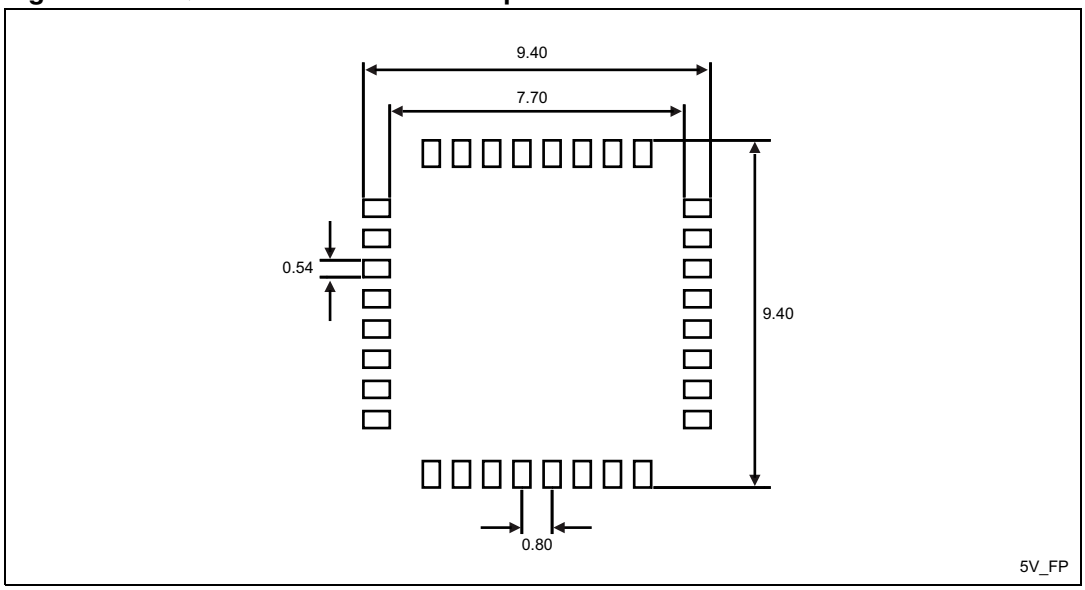
Table 9. LQFP32 7 x 7mm 32-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.600			0.2205	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.600			0.2205	
e		0.800			0.0315	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc			0.100			0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

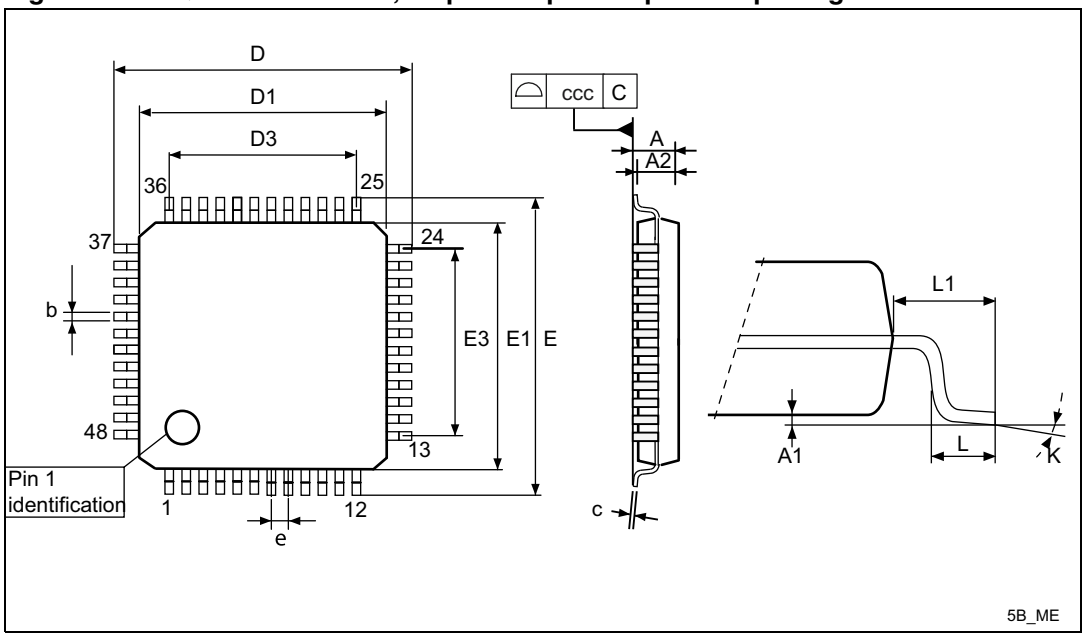
1.

Figure 7. LQFP32 recommended footprint



1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Figure 8. LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package outline



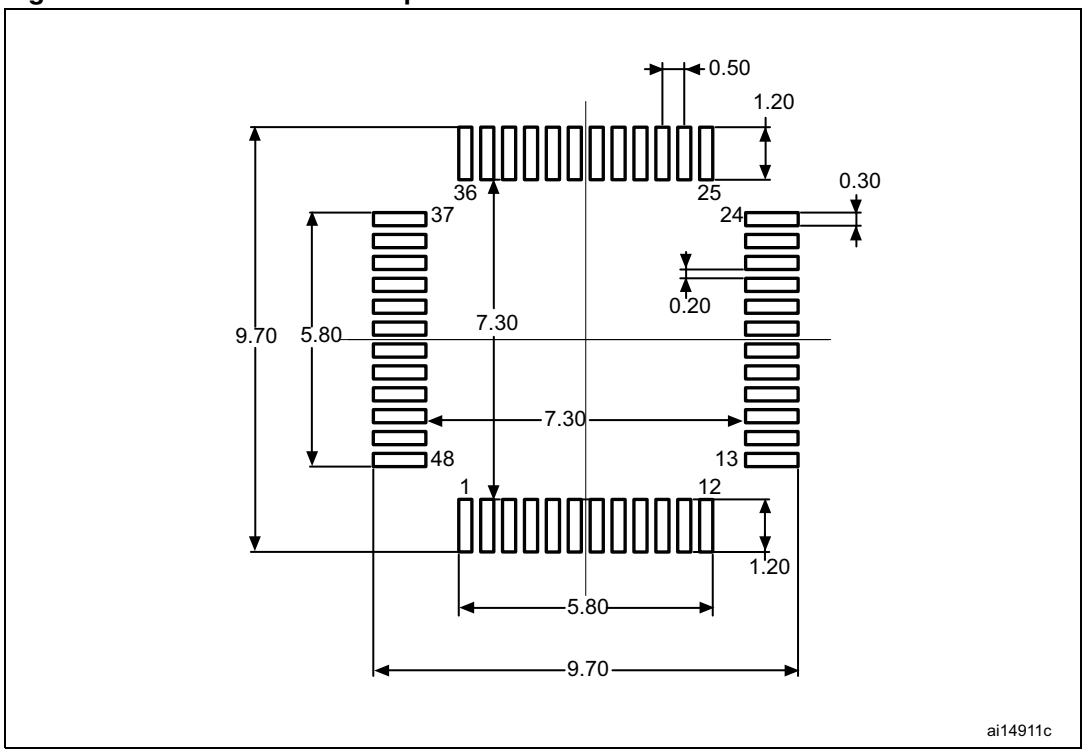
1. Drawing is not to scale.

Table 10. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.500			0.2165	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc			0.080			0.0031

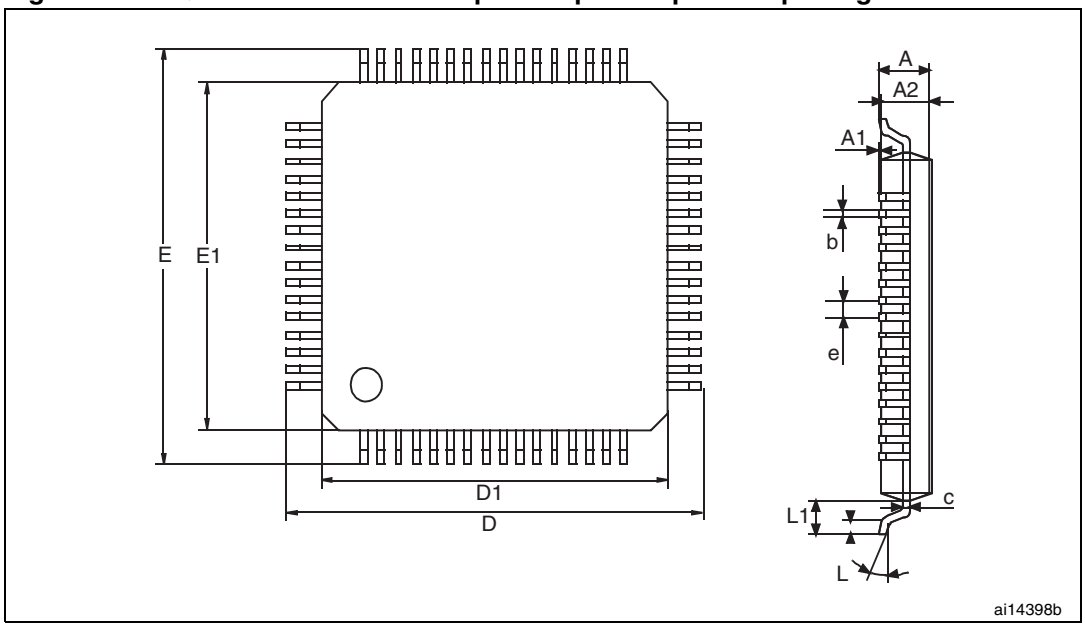
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 9. Recommended footprint



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Figure 10. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



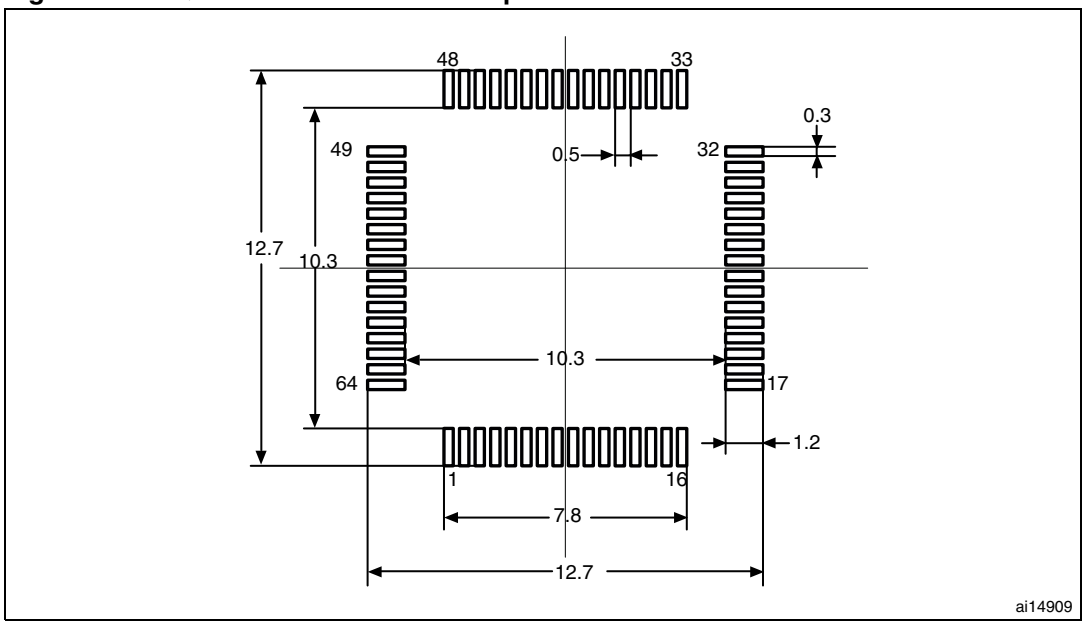
1. Drawing is not to scale.

Table 11. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D		12.000			0.4724	
D1		10.000			0.3937	
E		12.000			0.4724	
E1		10.000			0.3937	
e		0.500			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
N	Number of pins					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 11. LQFP64 recommended footprint



1. Drawing is not to scale.
2. Dimensions are in millimeters.

4.2 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max x } \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 12. Package thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP32 - 7 × 7 mm / 0.8 mm pitch	TBD	°C/W
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	TBD	
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm / 0.5 mm pitch	TBD	

1. TBD stands for “to be defined”.

4.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

4.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 13: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F333xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 12* T_{Jmax} is calculated as follows:

– For LQFP64, TBD °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 13: Ordering information scheme*).

5 Part numbering

Table 13. Ordering information scheme

Example: STM32 F 333 R 8 T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

333 = STM32F333xx

Pin count

K = 32 pins
C = 48 pins
R = 64 pins

Flash memory size

4 = 16 Kbytes of Flash memory (medium density)
6 = 32 Kbytes of Flash memory (medium density)
8 = 64 Kbytes of Flash memory (high density)

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts
TR = tape and reel

6 Revision history

Table 14. Document revision history

Date	Revision	Changes
26-Apr -2012	0.1	Initial draft
29-Oct-2012	0.2	Added LQFP32 package as well as STM32F333Kx part numbers. *Features*: reorganized all features, updated core, DAC, and high-resolution timer descriptions. Updated *Table 2: STM32F333xx family device features and peripheral counts*. Updated *Figure 1: STM32F333xx block diagram*. Added *Section 2.11.2: Extended interrupt/event controller (EXTI)* and *Section 2.12.2: Internal voltage reference (VREFINT)*, *Section 2.12.4: OPAMP2 reference voltage (VOPAMP2)*, and *Section 2.19: Infrared transmitter*. Updated *Section 2.20: Touch sensing controller (TSC)*. Updated *Figure 4: LQFP48 pinout*, *Figure 5: LQFP64 pinout*, *Table 7: STM32F333xx pin definitions* and *Table 8: Alternate functions*.

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