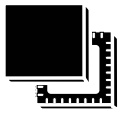
STM32L062K8

Ultra-low-power 32-bit MCU ARM-based Cortex-M0+, 64 KB Flash, 8 KB SRAM, 2 KB EEPROM, USB, ADC, DAC, AES

Datasheet - preliminary data

Features

- Ultra-low-power platform
  - 1.65 V to 3.6 V power supply
  - -40 to 105/125 °C temperature range
  - 0.27 µA Standby mode (2 wakeup pins)
  - 0.4 µA Stop mode (16 wakeup lines)
  - 0.8 µA Stop mode + RTC + 8 KB RAM retention
  - 139 µA/MHz Run mode at 32 MHz
  - 3.5 µs wakeup time (from RAM)
  - 5 µs wakeup time (from Flash)
- Core: ARM® 32-bit Cortex®-M0+ with MPU
  - From 32 kHz up to 32 MHz max.
  - 26 DMIPS peak (Dhrystone 2.1)
- Reset and supply management
  - Ultra-safe, low-power BOR (brownout reset) with 5 selectable thresholds
  - Ultralow power POR/PDR
  - Programmable voltage detector (PVD)
- Clock sources
  - 1 to 24 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - High speed internal 16 MHz factory-trimmed RC (+/- 1%)
  - Internal low-power 37 kHz RC
  - Internal multispeed low-power 65 kHz to 4.2 MHz RC
  - Internal self calibration of 48 MHz RC for USB
  - PLL for CPU clock
- Pre-programmed bootloader
  - USART, SPI supported
- Development support
  - Serial wire debug supported
- Up to 51 fast I/Os (45 I/Os 5V tolerant)
- Memories
  - 64 KB Flash with ECC
  - 8 KB RAM
  - 2 KB of data EEPROM with ECC
  - 20-byte backup register
  - Sector protection against R/W operation



UFQFPN32 5x5 mm

- Rich Analog peripherals (down to 1.8 V)
  - 12-bit ADC 1.14 Msps up to 16 channels
  - 12-bit 1 channel DAC with output buffers
  - 2x ultra-low-power comparators (window mode and wake up capability)
- Up to 24 capacitive sensing channels supporting touchkey, linear and rotary touch sensors
- 7-channel DMA controller, supporting ADC, SPI, I2C, USART, DAC, Timers, AES
- 8x peripherals communication interface
- 1x USB 2.0 crystal-less, battery charging detection and LPM
- 2x USART (ISO 7816, IrDA), 1x UART (low power)
- 2x SPI 16 Mbits/s
- 2x I2C (SMBus/PMBus)
- 9x timers: 1x 16-bit with up to 4 channels, 2x 16-bit with up to 2 channels, 1x 16-bit ultra-low-power timer, 1x SysTick, 1x RTC, 1x 16-bit basic for DAC, and 2x watchdogs (independent/window)
- CRC calculation unit, 96-bit unique ID
- True RNG and firewall protection
- Hardware Encryption Engine AES 128-bit
- All packages are ECOPACK®2

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1 Introduction

The ultra-low-power STM32L062K8 includes devices in a 32-pin package. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L062K8 microcontroller suitable for a wide range of applications:

- Medical and hand-held equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors, Video intercom
- Utility metering

This STM32L062K8 datasheet should be read in conjunction with the STM32L0x2xx reference manual (RM0376).

For information on the ARM® Cortex®-M0+ core please refer to the Cortex®-M0+ Technical Reference Manual, available from the www.arm.com website.

Figure 1 shows the general block diagram of the device family.

2 Description

The ultra-low-power STM32L062K8 incorporates the connectivity power of the universal serial bus (USB 2.0 crystal-less) with the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, a memory protection unit (MPU), high-speed embedded memories (64 Kbytes of Flash program memory, 2 Kbytes of data EEPROM and 8 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L062K8 device provides high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L062K8 device offers several analog features, one 12-bit ADC, one DAC, two ultra-low-power comparators, AES, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers and one basic timer, one RTC and one SysTick which can be used as timebases. It also features two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L062K8 device embeds standard and advanced communication interfaces: up to two I2Cs, two SPIs, two I2S, three USARTs and a crystal-less USB. The devices offer up to 24 capacitive sensing channels to simply add touch sensing functionality to any application.

It also includes a real-time clock and a set of backup registers that remain powered in Standby mode.

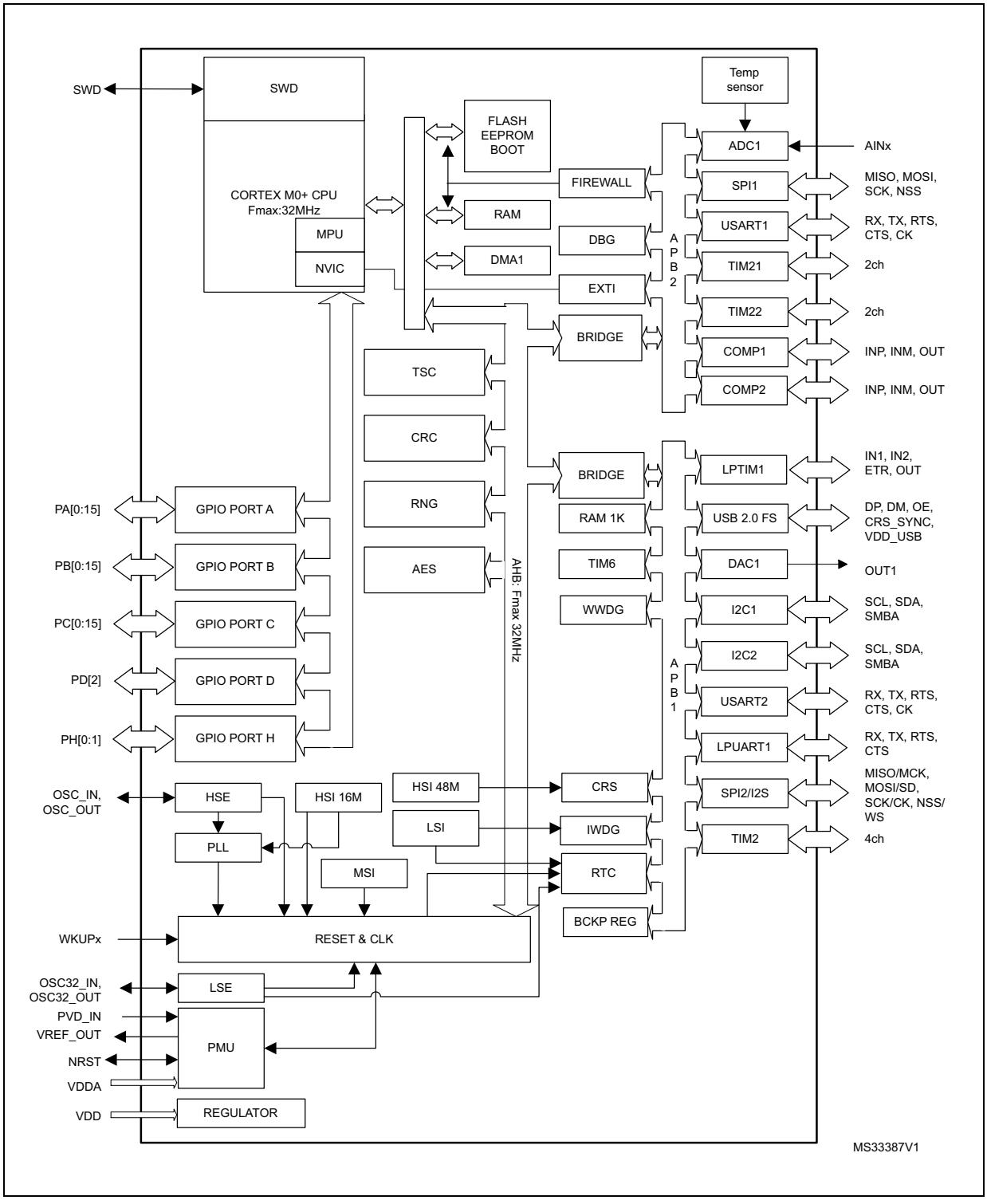
The ultra-low-power STM32L062K8 device operates from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. It is available in the -40 to +105 °C temperature range, extended to 125 °C in low-power dissipation state. A comprehensive set of power-saving modes allows the design of low-power applications.

2.1 Device overview

Table 1. Ultra-low-power STM32L062K8 device features and peripheral counts

Peripheral		STM32L062K8	
Flash (Kbytes)		64	
Data EEPROM (Kbytes)		2	
RAM (Kbytes)		8	
AES		1	
Timers	General-purpose	3	
	Basic	1	
	LPTIMER	1	
RTC/SYSTICK/IWDG/WWDG		1/1/1/1	
Communication interfaces	SPI/(I2S)	2/(1)	
	I^2C	2	
	USART	2	
	LPUART	1	
	USB/(USB_VDD)	1/(1)	
GPIOs		37	51
Clocks: HSE/LSE/HSI/MSI/LSI		0/1/1/1/1	
12-bit synchronized ADC Number of channels		1 10	1 16
12-bit DAC Number of channels		1 1	
Comparators		2	
Capacitive sensing channels		17	24
Max. CPU frequency		32 MHz	
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option	
Operating temperatures		Ambient temperature: –40 to +105 °C Junction temperature: –40 to +125 °C	
Packages		UFQFPN32	

Figure 1. STM32L062K8 block diagram



2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from proprietary 8-bit core to up ARM® Cortex®-M3, including ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 Ultra-low-power series are the best solution for applications such as gaz/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power Run mode, operational amplifiers, AES 128-bit, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L062K8 supports dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

  This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

- **Stop mode with RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event

(if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USB/USART/I2C/LPUART/LPTIMER wakeup events.

- **Stop mode without RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB/USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

  The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 2. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	Dynamic voltage scaling range	I/O operation	USB
V_{DD} = 1.65 to 1.71 V	Not functional	Range 2 or range 3	Degraded speed performance	Not functional
V_{DD} = 1.71 to 1.8 V(1)	Not functional	Range 1, range 2 or range 3	Degraded speed performance	Functional(2)

Table 2. Functionalities depending on the operating power supply range (continued)

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	Dynamic voltage scaling range	I/O operation	USB
V_{DD} = 1.8 to 2.0 V(1)	Conversion time up to 1.14 Msps	Range1, range 2 or range 3	Degraded speed performance	Functional(2)
V_{DD} = 2.0 to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation	Functional(2)
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation	Functional(2)

1. CPU frequency changes from initial to final must respect "fcpu initial <4*fcpu final". It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.
2. To be USB compliant from the I/O voltage standpoint, the minimum V_{DD_USB} is 3.0 V.

Table 3. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

Table 4. Functionalities depending on the working mode (from Run/active down to standby)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	--	Y	--	--		--	
Flash memory	Y	Y	Y	N	--		--	
RAM	Y	Y	Y	Y	Y		--	
Backup registers	Y	Y	Y	Y	Y		Y	
EEPROM	Y	--	Y	Y	Y		--	
Brown-out rest (BOR)	Y	Y	Y	Y	Y	Y	Y	
DMA	Y	Y	Y	Y	--		--	
Programmable Voltage Detector (PVD)	Y	Y	Y	Y	Y	Y	Y	
Power On Reset (POR)	Y	Y	Y	Y	Y	Y	Y	
Power Down Rest (PDR)	Y	Y	Y	Y	Y		Y	
High Speed Internal (HSI)	Y	Y	--	--	--		--	
High Speed External (HSE)	Y	Y	--	--	--		--	
Low Speed Internal (LSI)	Y	Y	Y	Y	Y		--	
Low Speed External (LSE)	Y	Y	Y	Y	Y		--	
Multi-Speed Internal (MSI)	Y	Y	Y	Y	--		--	

Table 4. Functionalities depending on the working mode (from Run/active down to standby) (continued)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
Inter-Connect Controller	Y	Y	Y	Y	--		--	
RTC	Y	Y	Y	Y	Y	Y	Y	
RTC Tamper	Y	Y	Y	Y	Y	Y	Y	Y
Auto WakeUp (AWU)	Y	Y	Y	Y	Y	Y	Y	Y
USB	Y	Y	--	--	--	Y	--	
USART	Y	Y	Y	Y	Y	Y	--	
LPUART	Y	Y	Y	Y	Y	Y	-	
SPI	Y	Y	Y	Y			--	
I2C	Y	Y	Y	Y		Y	--	
ADC	Y	Y	--	--	--		--	
DAC	Y	Y	Y	Y	Y		--	
Temperature sensor	Y	Y	Y	Y	Y		--	
Comparators	Y	Y	Y	Y	Y	Y	--	
16-bit and 32-bit Timers	Y	Y	Y	Y	--		--	
LPTIMER	Y	Y	Y	Y	Y	Y		
IWDG	Y	Y	Y	Y	Y	Y	Y	Y
WWDG	Y	Y	Y	Y	--		--	
Touch sensing controller (TSC)	Y	Y	--	--	--		--	
SysTick Timer	Y	Y	Y	Y			--	
GPIOs	Y	Y	Y	Y	Y	Y		2 pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs	3.5 µs		50 µs	
Consumption V_{DD}=1.8 to 3.6 V (Typ)	Down to 140 µA/MHz (from Flash)	Down to 37 µA/MHz (from Flash)	Down to 8 µA	Down to 4.5 µA	0.4 µA (No RTC) V_{DD}=1.8 V		0.28 µA (No RTC) V_{DD}=1.8 V	
					0.8 µA (with RTC) V_{DD}=1.8 V		0.65 µA (with RTC) V_{DD}=1.8 V	
					0.4 µA (No RTC) V_{DD}=3.0 V		0.29 µA (No RTC) V_{DD}=3.0 V	
					1 µA (with RTC) V_{DD}=3.0 V		0.85 µA (with RTC) V_{DD}=3.0 V	

3.2 ARM® Cortex®-M0+ core with MPU

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L062K8 are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L062K8 embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{DD_USB} = 1.65 to 3.6V: external power supply for USB transceiver, USB_DM (PA11) and USB_DP (PA12). To guarantee a correct voltage level for USB communication V_{DD_USB} must be above 3.0V. If USB is not used this pin must be tied to V_{DD}.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the VDD min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.3.4 Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using USART1(PA9, PA10), USART2(PA2, PA3), SPI1(PA4, PA5, PA6, PA7) or SPI2(PB12, PB13, PB14, PB15). See STM32™ microcontroller system memory boot mode AN2606 for details.

3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**

  To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**

  Clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management**

  To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**

  Three different clock sources can be used to drive the master clock SYSCLK:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz).

When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.

- **Auxiliary clock source**

  Two ultra-low-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC clock source**

  The LSI, LSE or HSE sources can be chosen to clock the RTC , whatever the system clock.
- **USB clock source**

  A 48 MHz clock trimmed through the USB SOF supplies the USB interface.
- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS)**

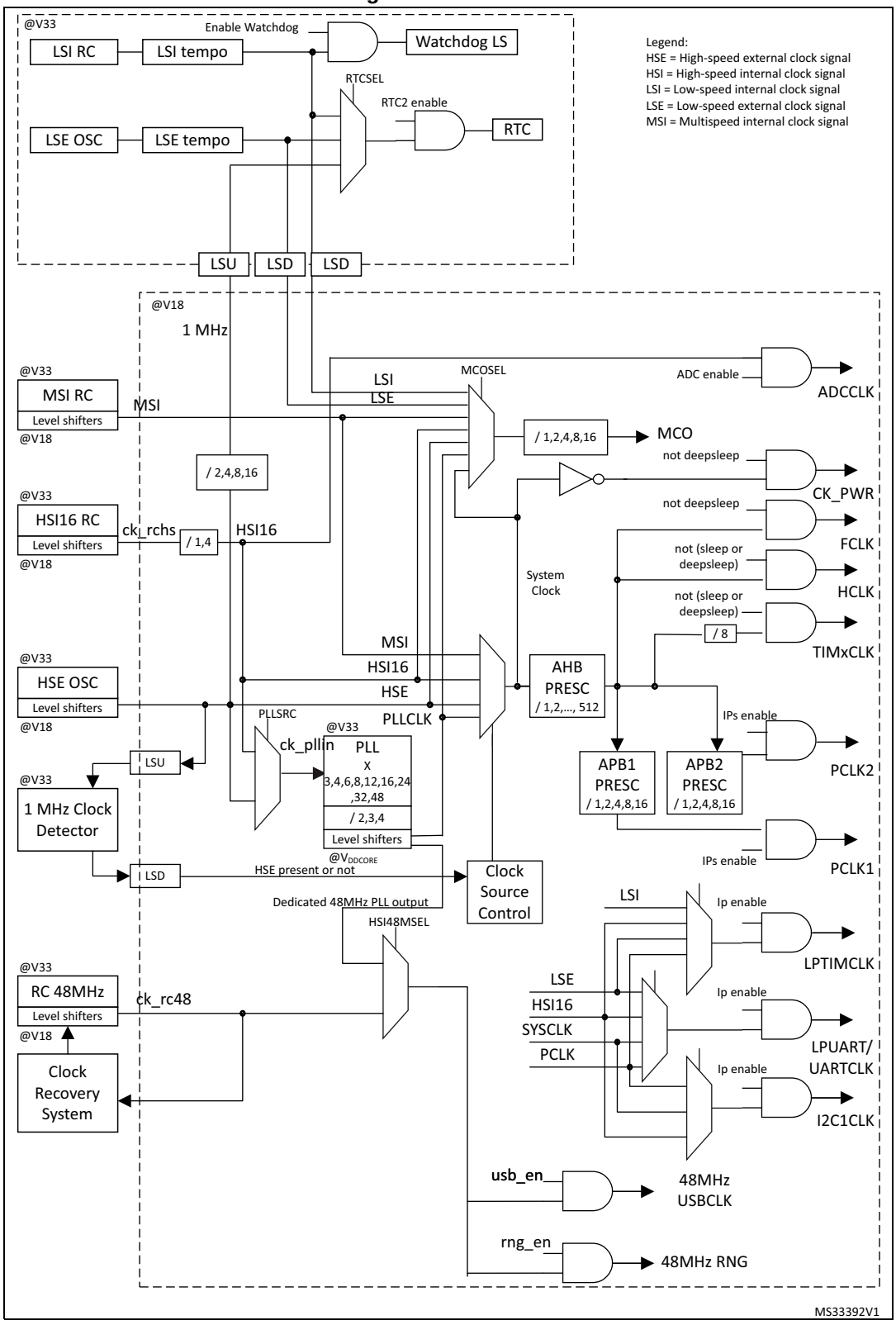
  This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

  Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

Figure 2. Clock tree



1. For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 24 MHz or 32 MHz.

3.5 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

3.6 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 28 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 51 GPIOs can be connected to the 16 configurable interrupt/event lines. The 12 other lines are connected to PVD, RTC, USB, USARTs, LPUART, LPTIMER or comparator events.

3.7 Memories

The STM32L062K8 device has the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 32 or 64 Kbytes of embedded Flash program memory
  - 2 Kbytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0**: no protection
- **Level 1**: memory readout protected.

  The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: AES, SPI, I^2C, USART, LPUART, general-purpose timers, DAC, and ADC.

3.9 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L062K8 devices. It has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference). It performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 µA at 10 kSPS, ~200 µA at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

3.10 Temperature sensor

The temperature sensor (T_{SENSE}) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 5. Temperature sensor calibration values

Calibration value name	Description	Memory address
TSENSE_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TSENSE_CAL2	TS ADC raw data acquired at temperature of 130 °C V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

3.10.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value . The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 6. Internal voltage reference measured values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C V_{DDA} = 3 V	0x1FF8 0078 - 0x1FF8 0079

3.11 Digital-to-analog converter (DAC)

One 12-bit buffered DAC can be used to convert digital signal into analog voltage signal output. An optional amplifier can be used to reduce the output signal impedance.

This digital Interface supports the following features:

- One data holding register
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- DMA capability (including the underrun interrupt)
- External triggers for conversion

Four DAC trigger inputs are used in the STM32L062K8. The DAC channel is triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Ultra-low-power comparators and reference voltage

The STM32L062K8 embeds two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
  - DAC output
  - External I/O pins
  - Internal reference voltage (V_{REFINT})
  - submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.13 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM21, TIM22 and LPTIM timer input captures. It also controls the routing of internal analog signals to the USB internal oscillator, ADC, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

3.14 Touch sensing controller (TSC)

The STM32L062K8 provides a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (such as glass, plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 7. Capacitive sensing GPIOs available on STM32L062K8 devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PC0
	TSC_G3_IO2	PB0		TSC_G7_IO2	PC1
	TSC_G3_IO3	PB1		TSC_G7_IO3	PC2
	TSC_G3_IO4	PB2		TSC_G7_IO4	PC3
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PC6
	TSC_G4_IO2	PA10		TSC_G8_IO2	PC7
	TSC_G4_IO3	PA11		TSC_G8_IO3	PC8
	TSC_G4_IO4	PA12		TSC_G8_IO4	PC9

3.15 AES

The AES Hardware Accelerator can be used to encrypt and decrypt data using the AES algorithm (compatible with FIPS PUB 197, 2001 Nov 26).

- Key scheduler
- Key derivation for decryption
- 128-bit data block processed
- 128-bit key length
- 213 clock cycles to encrypt/decrypt one 128-bit block
- Electronic codebook (ECB), cypher block chaining (CBC), and counter mode (CTR) supported by hardware.

The AES can be served by the DMA controller.

3.16 Timers and watchdogs

The ultra-low-power STM32L062K8 device includes three general-purpose timers, one low-power timer (LPTM), one basic timer, two watchdog timers and the SysTick timer.

Table 8 compares the features of the general-purpose and basic timers.

Table 8. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.16.1 General-purpose timers (TIM2, TIM21 and TIM22)

There are three synchronizable general-purpose timers embedded in the STM32L062K8 device (see *Table 8* for differences).

TIM2

TIM2 is based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2 general-purpose timers can work together or with the TIM21 and TIM22 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2 have independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together and be synchronized with the TIM2, full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.16.2 Low-power Timer (LPTIM)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one shot mode
- Selectable software / hardware input trigger
- Selectable clock source
  - Internal clock source: LSE, LSI, HSI or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.16.3 Basic timer (TIM6)

This timer can be used as a generic 16-bit timebase. It is mainly used for DAC trigger generation.

3.16.4 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches ‘0’.

3.16.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.16.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.17 Communication interfaces

3.17.1 I²C bus

Up to two I²C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 9. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to *Table 10* for the differences between I2C1 and I2C2.

Table 10. STM32L062K8 I²C implementation

I2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X(2)
Independent clock	X	-

Table 10. STM32L062K8 I²C implementation (continued)

I2C features(1)	I2C1	I2C2
SMBus	X	-
Wakeup from STOP	X	-

1. X = supported.
2. See for the list of I/Os that feature Fast Mode Plus capability

3.17.2 Universal synchronous/asynchronous receiver transmitter (USART)

The two USART interfaces (USART1 and USART2) are able to communicate at speeds of up to 4 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. The support also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode.

All USART interfaces can be served by the DMA controller.

Refer to *Table 11* for the supported modes and features of USART1 and USART2.

Table 11. USART implementation

USART modes/features(1)	USART1 and USART2
Hardware flow control for modem	X
Continuous communication using DMA	X
Multiprocessor communication	X
Synchronous mode	X
Smartcard mode	X
Single-wire half-duplex communication	X
IrDA SIR ENDEC block	X
LIN mode	X
Dual clock domain and wakeup from Stop mode	X
Receiver timeout interrupt	X
Modbus communication	X
Auto baud rate detection (4 modes)	X
Driver Enable	X

1. X = supported.

3.17.3 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode. The Wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Or any received data frame
- Or a specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.17.4 Serial peripheral interface (SPI)/Inter-integrated sound (I2S)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

One standard I2S interfaces (multiplexed with SPI2) is available. It can operate in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When the I2S interfaces is configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The SPIs can be served by the DMA controller.

Refer to *Table 12* for the differences between SPI1 and SPI2.

Table 12. SPI/I2S implementation

SPI features(1)	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I2S mode	-	X
TI mode	X	X

1. X = supported.

3.17.5 Universal serial bus (USB)

The STM32L062K8 embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming

mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

3.18 Clock recovery system (CRS)

The STM32L062K8 embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.19 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

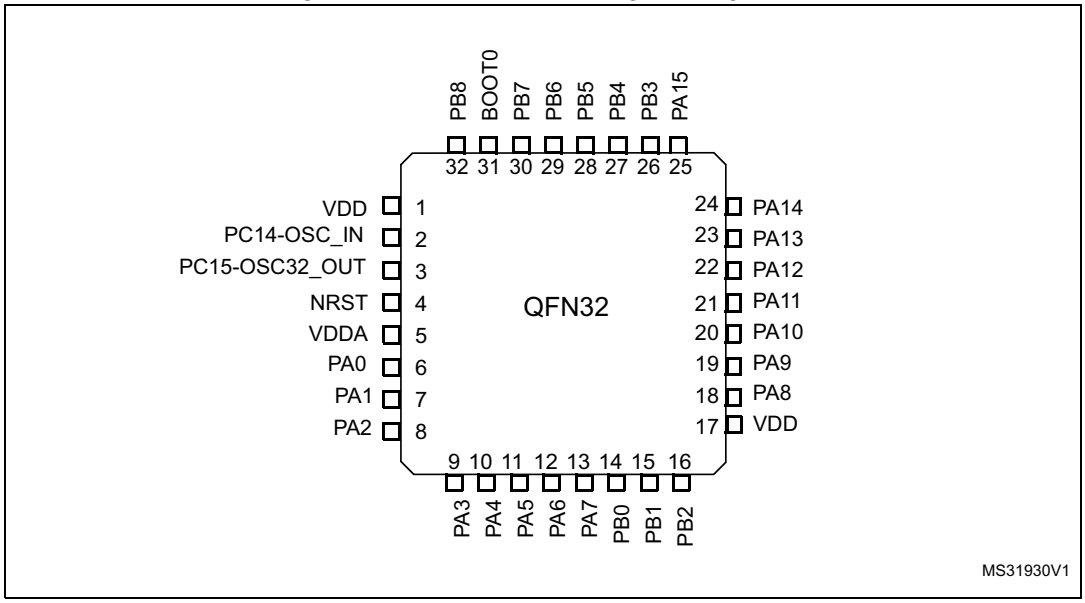
Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.20 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pin descriptions

Figure 3. STM32L062K8 UFQFPN32 pinout



1. The above figure shows the package top view.

Table 13. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 14. STM32L062K8 pin definitions

Pin Number	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32						
2	PC14-OSC32_IN	I/O	TC			OSC32_IN
3	PC15-OSC32_OUT	I/O	TC			OSC32_OUT
4	NRST	I/O				
5	VDDA	S				
6	PA0	I/O	TC		TIM2_CH1, TSC_G1_IO1, USART2_CTS, TIM2_ETR, COMP1_OUT	COMP1_INM6, ADC_IN0, RTC_TAMP2/WKUP1
7	PA1	I/O	FT		EVENTOUT, TIM2_CH2, TSC_G1_IO2, USART2_RTS, TIM21_ETR	COMP1_INP, ADC_IN1
8	PA2	I/O	FT		TIM21_CH1, TIM2_CH3, TSC_G1_IO3, USART2_TX, COMP2_OUT	COMP2_INM6, ADC_IN2
9	PA3	I/O	FT		TIM21_CH2, TIM2_CH4, TSC_G1_IO4, USART2_RX	COMP2_INP, ADC_IN3
10	PA4	I/O	TC	(1)	SPI1_NSS, TSC_G2_IO1, USART2_CK, TIM22_ETR	COMP1_INM4, COMP2_INM4, ADC_IN4, DAC_OUT
11	PA5	I/O	TC		SPI1_SCK, TIM2_ETR, TSC_G2_IO2, TIM2_CH1	COMP1_INM5, COMP2_INM5, ADC_IN5

Table 14. STM32L062K8 pin definitions (continued)

Pin Number	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32						
12	PA6	I/O	FT		SPI1_MISO, TSC_G2_IO3, USART3_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6
13	PA7	I/O	FT		SPI1_MOSI, TSC_G2_IO4, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
14	PB0	I/O	FT		EVENTOUT, TSC_G3_IO2	ADC_IN8, VREF_OUT
15	PB1	I/O	FT		TSC_G3_IO3, USART3_RTS	ADC_IN9, VREF_OUT
16	PB2	I/O	FT		LPTIM1_OUT, TSC_G3_IO4	
17	VDD	S				
18	PA8	I/O	FT		MCO, USB_CRS_SYNC, EVENTOUT, USART1_CK	
19	PA9	I/O	FT		MCO, TSC_G4_IO1, USART1_TX	
20	PA10	I/O	FT		TSC_G4_IO2, USART1_RX	
21	PA11	I/O	FT		SPI1_MISO, EVENTOUT, TSC_G4_IO3, USART1_CTS, COMP1_OUT	USB_DM
22	PA12	I/O	FT		SPI1_MOSI, EVENTOUT, TSC_G4_IO4, USART1_RTS, COMP2_OUT	USB_DP

Table 14. STM32L062K8 pin definitions (continued)

Pin Number	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32						
23	PA13	I/O	FT		SWDIO, USB_OE	
24	PA14	I/O	FT		SWCLK, USART2_TX	
25	PA15	I/O	FT		SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1	
26	PB3	I/O	FT		SPI1_SCK, TIM2_CH2, TSC_G5I_O1, EVENTOUT	COMP2_INN
27	PB4	I/O	FT		SPI1_MISO, EVENTOUT, TSC_G5_IO2, TIM22_CH1	COMP2_INP
28	PB5	I/O	FT		SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM22_CH2	COMP2_INP
29	PB6	I/O	FTf		USART1_TX, I2C1_SCL, LPTIM1_ETR, TSC_G5_IO3	COMP2_INP
30	PB7	I/O	FTf		USART1_RX, I2C1_SDA, LPTIM1_IN2, TSC_G5_IO4	COMP2_INP, PVD_IN
31	BOOT0	I				
32	PB8	I/O	FTf		TSC_SYNC, I2C1_SCL	
-	VSS	S				
1	VDD	S				

1. PA4 offers a reduced touch sensing sensitivity. It is thus recommended to use it as sampling capacitor I/O.

Table 15. Alternate functions for port A

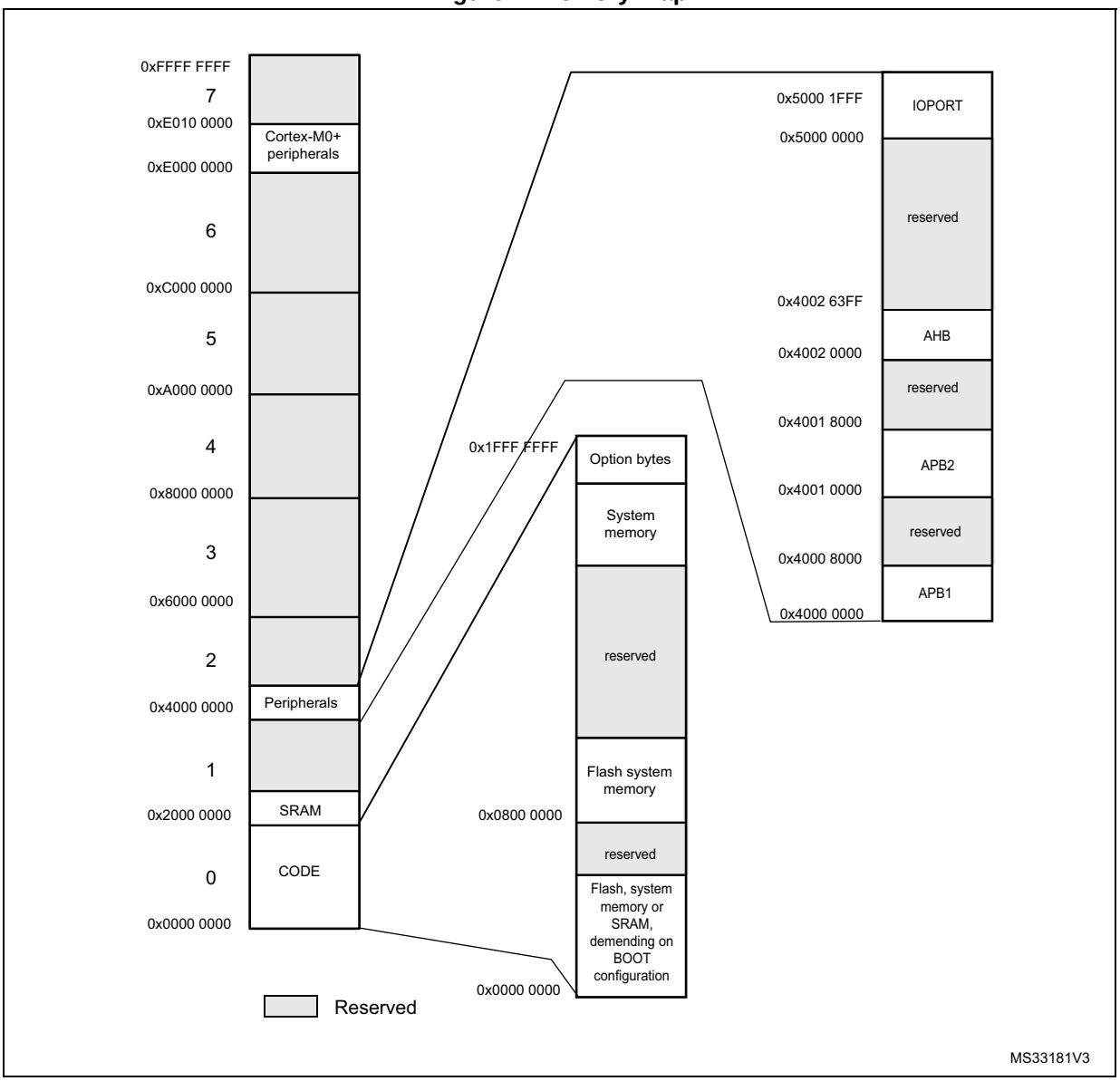
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/3/ USB/LPTIM/ TSC/TIM2/21/22 /EVENOUT/ SYS_AF	SPI1/SPI2/I2S2/ I2C1/TIM2/21	SPI2/I2S2/ USART3/USB/ LPTIM/TIM2/ EVENOUT/ SYS_AF	I2C1/TSC/ EVENOUT	I2C1/USART1/2 /3/TIM22/ EVENOUT	SPI2/I2S2/I2C2/ TIM2/21/22	I2C2/TIM21/ EVENOUT	COMP1/2
Port A	PA0			TIM2_CH1	TSC_G1_IO1	USART2_CTS	TIM2_ETR		COMP1_OUT
	PA1	EVENTOUT		TIM2_CH2	TSC_G1_IO2	USART2_RTS	TIM21_ETR		
	PA2	TIM21_CH1		TIM2_CH3	TSC_G1_IO3	USART2_TX			COMP2_OUT
	PA3	TIM21_CH2		TIM2_CH4	TSC_G1_IO4	USART2_RX			
	PA4	SPI1_NSS			TSC_G2_IO1	USART2_CK	TIM22_ETR		
	PA5	SPI1_SCK		TIM2_ETR	TSC_G2_IO2		TIM2_CH1		
	PA6	SPI1_MISO			TSC_G2_IO3	USART3_CTS	TIM22_CH1	EVENTOUT	COMP1_OUT
	PA7	SPI1_MOSI			TSC_G2_IO4		TIM22_CH2	EVENTOUT	COMP2_OUT
	PA8	MCO		USB_CRS_ SYNC	EVENTOUT	USART1_CK			
	PA9	MCO			TSC_G4_IO1	USART1_TX			
	PA10				TSC_G4_IO2	USART1_RX			
	PA11	SPI1_MISO		EVENTOUT	TSC_G4_IO3	USART1_CTS			COMP1_OUT
	PA12	SPI1_MOSI		EVENTOUT	TSC_G4_IO4	USART1_RTS			COMP2_OUT
	PA13	SWDIO		USB_OE					
	PA14	SWCLK				USART2_TX			
	PA15	SPI1_NSS		TIM2_ETR	EVENTOUT	USART2_RX	TIM2_CH1		

Table 16. Alternate functions for port B

Port		AF0	AF1	AF2	AF3	AF4
		SPI1/SPI2/I2S2 /USART1/2/3/ USB/LPTIM/ TSC/TIM2/21/22/ EVENOUT/SYS_AF	SPI1/SPI2/I2S2 /I2C1/TIM2/21	SPI2/I2S2/ USART3/USB/ LPTIM/TIM2/ EVENOUT/ SYS_AF	I2C1/TSC/ EVENOUT	I2C1/USART1/2/3/ TIM22/EVENOUT
Port B	PB0	EVENTOUT			TSC_G3_IO2	
	PB1				TSC_G3_IO3	USART3_RTS
	PB2			LPTIM1_OUT	TSC_G3_IO4	
	PB3	SPI1_SCK		TIM2_CH2	TSC_G5I_O1	EVENTOUT
	PB4	SPI1_MISO		EVENTOUT	TSC_G5_IO2	TIM22_CH1
	PB5	SPI1_MOSI		LPTIM1_IN1	I2C1_SMBA	TIM22_CH2
	PB6	USART1_TX		LPTIM1_ETR	TSC_G5_IO3	
	PB7	USART1_RX		LPTIM1_IN2	TSC_G5_IO4	
	PB8				TSC_SYNC	I2C1_SCL

5 Memory mapping

Figure 4. Memory map



6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 5*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 6*.

Figure 5. Pin loading conditions

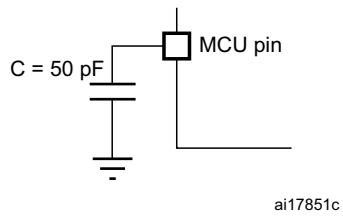
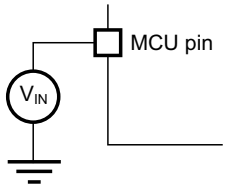
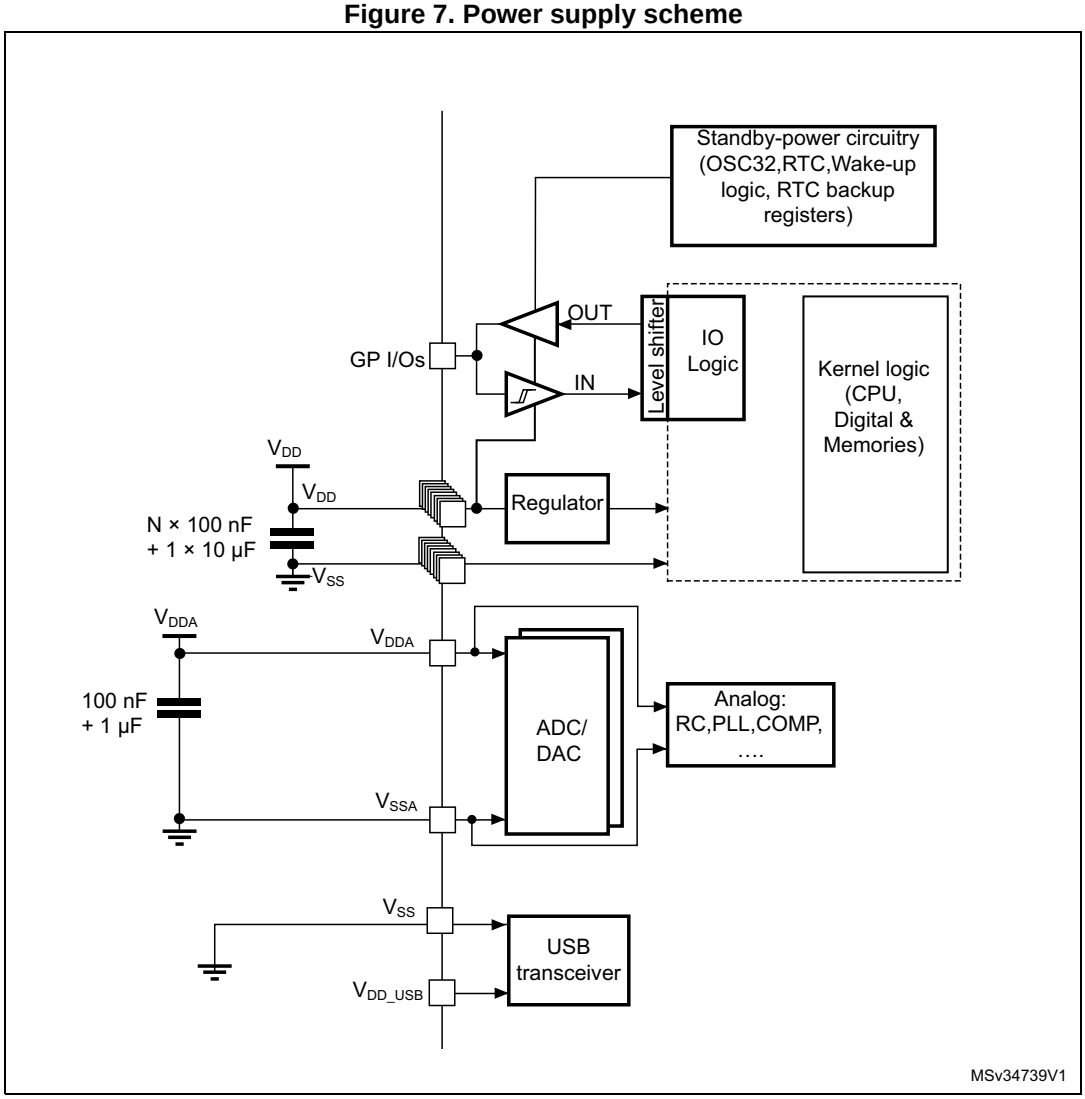


Figure 6. Pin input voltage



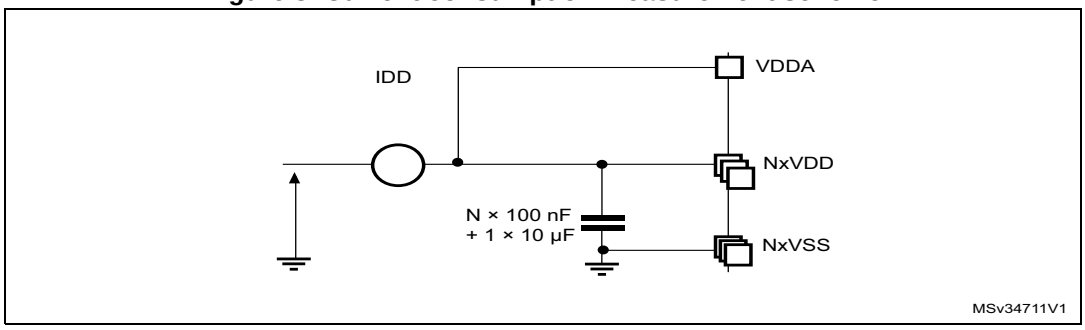
6.1.6 Power supply scheme

Figure 7. Power supply scheme



6.1.7 Current consumption measurement

Figure 8. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 17: Voltage characteristics*, *Table 18: Current characteristics*, and *Table 19: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 17. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five-volt tolerant pin	V_{SS} – 0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS} – 0.3	4.0	
$\lvert\Delta V_{DD}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert\Delta V_{SS}\rvert$	Variations between all different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 18* for maximum allowed injected current values.

Table 18. Current characteristics

Symbol	Ratings	Max.	Unit
$I_{VDD(\Sigma)}$	Total current into sum of all V_{DD} power lines (source)(1)	100	mA
$I_{VSS(\Sigma)}$(2)	Total current out of sum of all V_{SS} ground lines (sink)(1)	100	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	70	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	-70	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	- 25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	60	
	Total output current sourced by sum of all IOs and control pins(2)	-60	
$I_{INJ(PIN)}$ (3)	Injected current on five-volt tolerant I/O(4)	-5/+0	
	Injected current on any other pin (5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.15*.

4. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 17* for maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 17: Voltage characteristics* for the maximum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 19. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 20. General operating conditions(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32	
f_{PCLK2}	Internal APB2 clock frequency	-	0	32	
V_{DD}	Standard operating voltage	BOR detector disabled	1.65	3.6	V
		BOR detector enabled, at power on	1.8	3.6	
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA}(2)	Analog operating voltage (ADC and DAC not used)	Must be the same voltage as V_{DD}(3)	1.65	3.6	V
	Analog operating voltage (ADC or DAC used)		1.8	3.6	
V_{IN}	Input voltage on FT pins(4)	2.0 V ≤ V_{DD} ≤ 3.6 V	-0.3	5.55	V
		1.65 V ≤ V_{DD} ≤ 2.0 V	-0.3	5.25	
	Input voltage on BOOT0 pin	-	0	5.5	
	Input voltage on any other pin	-	-0.3	V_{DD}+0.3	
P_D	Power dissipation at T_A = 85 °C (range 6) or T_A =105 °C (rage 7) (5)	UFQFPN32	-	351	mW

Table 20. General operating conditions(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Temperature range	Maximum power dissipation (range 6)	–40	85	°C
		Maximum power dissipation (range 7)	–40	105	
		Low-power dissipation (range 7) (6)	–40	125	
T_J	Junction temperature range (range 6)	-40 °C ≤ T_A ≤ 85 °	–40	105	
	Junction temperature range (range 7)	-40 °C ≤ T_A ≤ 105 °C	–40	125	

1. TBD stands for “to be defined”.
2. When the ADC is used, refer to *Table 54: ADC characteristics*.
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and normal operation.
4. To sustain a voltage higher than V_{DD}+0.3V, the internal pull-up/pull-down resistors must be disabled.
5. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 70: Thermal characteristics on page 100*).
6. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_J max (see *Table 70: Thermal characteristics on page 100*).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 20*.

Table 21. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	

Table 21. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.6	V
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization, not tested in production.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in *Table 23* are based on characterization results, unless otherwise specified.

Table 22. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C V_{DDA}= 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 23. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$(1)	Internal reference voltage	– 40 °C < T_J < +105 °C	1.202	1.224	1.242	V
I_{REFINT}	Internal reference current consumption	-	-	1.4	2.3	µA
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REF} value(2)	Including uncertainties due to ADC and V_{DDA}values	-	-	±5	mV
T_{Coeff}(3)	Temperature coefficient	–40 °C < T_J < +105 °C	-	20	50	ppm/°C
		0 °C < T_J < +50 °C	-	-	20	
A_{Coeff}(3)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(3)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(3)(4)	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}(3)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(3)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(3)	VREF_OUT output current(5)	-	-	-	1	µA
C_{VREF_OUT}(3)	VREF_OUT output load	-	-	-	50	pF
I_{LPBUF}(3)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(3)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(3)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(3)	3/4 reference voltage	-	74	75	76	

1. Tested in production.
2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.

3. Guaranteed by design, not tested in production.
4. Shortest sampling time can be determined in the application by multiple iterations.
5. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 8: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 33: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

The parameters given in *Table 41*, *Table 20* and *Table 21* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Table 24. Current consumption in Run mode, code with data processing running from Flash(1)(2)

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(3)	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(4)	Range 3, V_{CORE}=1.2 V	1 MHz	165	TBD	µA
				2 MHz	300	TBD	
				4 MHz	580	-	
			Range 3, V_{CORE}=1.2 V, CoreMark(5)	4 MHz	585	-	
			Range 3, V_{CORE}=1.2 V, Fibonacci(5)		505	-	
			Range 3, V_{CORE}=1.2 V, while(1)(5)		360	-	
			Range 3, V_{CORE}=1.2 V, running while(1), 1WS, prefetch OFF(5)		TBD	TBD	
			Range 2, V_{CORE}=1.5 V	4 MHz	0.685	TBD	mA
				8 MHz	1.35	TBD	
				16 MHz	2.6	TBD	
			Range 1, V_{CORE}=1.8 V	8 MHz	1.6	TBD	
				16 MHz	3.1	TBD	
				32 MHz	6	8.4	
			Range 1, V_{CORE}=1.8 V, CoreMark(5)	32 MHz	6.1	-	
			Range 1, V_{CORE}=1.8 V, Fibonacci(5)		5.65	-	
			Range 1, V_{CORE}=1.8 V, while(1)(5)		5.1	-	
			Range 1, V_{CORE}=1.8 V, while(1)(5), prefetch OFF		4.45	-	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V	16 MHz	2.55	TBD	
			Range 1, V_{CORE}=1.8 V	32 MHz	6.15	8.5	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V	65 kHz	36.5	TBD	µA
		MSI clock, 524 kHz		524 kHz	100	TBD	
		MSI clock, 4.2 MHz		4.2 MHz	245	TBD	

1. TBD stands for “to be defined”.
2. CoreMark, Fibonacci and while(1) conditions are given for current consumption estimates compared to Dhrystone.
3. Based on characterization, not tested in production, unless otherwise specified.
4. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).
5. CoreMark, Fibonacci and while(1) conditions are given for current consumption estimate vs. Dhrystone

The following current consumption curves will be provided in next revision of this datasheet:

- I_{DD} vs V_{DD}, at T_A= -40 °C/25 °C/85 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS
- I_{DD} vs V_{DD}, at T_A= -40 °C/25 °C/85 °C, Run mode, code running from Flash memory, Range 2, HSI 1WS

Table 25. Current consumption in Run mode, code with data processing running from RAM(1)

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(2)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(3)	Range 3, V_{CORE}=1.2 V	1 MHz	TBD	TBD	µA
				2 MHz	TBD	TBD	
				4 MHz	TBD	TBD	
			Range 3, V_{CORE}=1.2 V, CoreMark	4 MHz	TBD	-	
			Range 3, V_{CORE}=1.2 V, Fibonacci		445	-	
			Range 3, V_{CORE}=1.2 V, while(1)		405	-	
			Range 2, V_{CORE}=1.5 V	4 MHz	TBD	TBD	mA
				8 MHz	TBD	TBD	
				16 MHz	TBD	TBD	
			Range 1, V_{CORE}=1.8 V	8 MHz	TBD	TBD	
				16 MHz	TBD	TBD	
				32 MHz	TBD	6.8	
			Range 1, V_{CORE}=1.8 V, CoreMark	32 MHz	TBD	-	
			Range 1, V_{CORE}=1.8 V, Fibonacci		5.10	-	
			Range 1, V_{CORE}=1.8 V, while(1)		3.95	-	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V	16 MHz	TBD	TBD	
			Range 1, V_{CORE}=1.8 V	32 MHz	TBD	6.9	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V	65 kHz	TBD	TBD	µA
		MSI clock, 524 kHz		524 kHz	TBD	TBD	
		MSI clock, 4.2 MHz		4.2 MHz	TBD	TBD	

1. TBD stands for “to be defined”.
2. Based on characterization, not tested in production, unless otherwise specified.
3. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 26. Current consumption in Sleep mode(1)

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(2)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(3)	Range 3, V_{CORE}=1.2 V	1 MHz	49.4	TBD	µA
				2 MHz	78.5	TBD	
				4 MHz	140	TBD	
			Range 2, V_{CORE}=1.5 V	4 MHz	160	TBD	
				8 MHz	295	TBD	
				16 MHz	570	TBD	
			Range 1, V_{CORE}=1.8 V	8 MHz	380	TBD	
				16 MHz	710	TBD	
				32 MHz	1600	TBD	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V	16 MHz	645	TBD	
			Range 1, V_{CORE}=1.8 V	32 MHz	1700	TBD	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V	65 kHz	18	TBD	
		MSI clock, 524 kHz		524 kHz	32.5	TBD	
		MSI clock, 4.2 MHz		4.2 MHz	145	TBD	
	Supply current in Sleep mode, Flash ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(3)	Range 3, V_{CORE}=1.2 V	1 MHz	59.5	TBD	
				2 MHz	89	TBD	
				4 MHz	150	TBD	
			Range 2, V_{CORE}=1.5 V	4 MHz	170	TBD	
				8 MHz	310	TBD	
				16 MHz	580	TBD	
			Range 1, V_{CORE}=1.8 V	8 MHz	380	TBD	
				16 MHz	710	TBD	
				32 MHz	1600	TBD	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V	16 MHz	660	TBD	
			Range 1, V_{CORE}=1.8 V	32 MHz	1700	TBD	
	Supply current in Sleep mode, code executed from Flash	MSI clock, 65 kHz	Range 3, V_{CORE}=1.2V	65 kHz	29	TBD	
		MSI clock, 524 kHz		524 kHz	43	TBD	
		MSI clock, 4.2 MHz		4.2 MHz	160	TBD	

1. TBD stands for “to be defined”.
2. Based on characterization, not tested in production, unless otherwise specified.
3. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)

Table 27. Current consumption in Low-power Run mode(1)

Symbol	Parameter	Conditions			Typ	Max(2)	Unit
I_{DD} (LP Run)	Supply current in Low-power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	8.55	TBD	µA
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A =-40 °C to 25 °C	12.5	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	23	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	22	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	27.5	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	39.5	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
I_{DD} max (LP Run)	Max allowed current in Low-power run mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	TBD	

1. TBD stands for “to be defined”.
2. Based on characterization, not tested in production, unless otherwise specified.

The following current consumption curve will be provided in next revision of this datasheet:

- I_{DD} vs V_{DD}, at T_A= -40 °C/25 °C/55 °C/ 85 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS

Table 28. Current consumption in Low-power Sleep mode(1)

Symbol	Parameter	Conditions			Typ	Max(2)	Unit
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz Flash OFF	T_A = -40 °C to 25 °C	4.65	TBD	µA
			MSI clock, 65 kHz f_{HCLK} = 32 kHz Flash ON	T_A = -40 °C to 25 °C	17	TBD	
				T_A = 85 °C	19	TBD	
				T_A = 105 °C	TBD	TBD	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz, Flash ON	T_A = -40 °C to 25 °C	17	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz, Flash ON	T_A = -40 °C to 25 °C	19.5	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
I_{DD} max (LP Sleep)	Max allowed current in Low-power sleep mode	V_{DD} from 1.65 V to 3.6 V	-	-	TBD	TBD	

1. TBD stands for “to be defined”.
2. Based on characterization, not tested in production, unless otherwise specified.

Table 29. Typical and maximum current consumptions in Stop mode(1)

Symbol	Parameter	Conditions			Typ	Max(2)	Unit
I_{DD} (Stop with RTC)	Supply current in Stop mode with RTC enabled	RTC clocked by LSI, regulator in LP mode, HSI, LSE and HSE OFF (no independent watchdog)		T_A = -40°C to 25°C V_{DD} = 1.8 V	1.1	TBD	µA
				T_A = -40°C to 25°C	1.35	TBD	
				T_A = 55°C	TBD	TBD	
				T_A= 85°C	TBD	TBD	
				T_A = 105°C	TBD	TBD	

Table 29. Typical and maximum current consumptions in Stop mode(1) (continued)

Symbol	Parameter	Conditions			Typ	Max(2)	Unit
I_{DD} (Stop with RTC)	Supply current in Stop mode with RTC enabled	RTC clocked by LSE external quartz (32.768kHz), regulator in LP mode, HSI/HSE OFF (no independent watchdog(3)(4)		T_A = -40°C to 25°C V_{DD} = 1.8V	0.82	-	µA
				T_A = -40°C to 25°C V_{DD} = 3.0V	1	-	
				T_A = -40°C to 25°C V_{DD} = 3.6V	1.15	-	
				T_A = 55°C	TBD	-	
				T_A = 85°C	TBD	-	
				T_A = 105°C	TBD	-	
				T_A = 125°C	TBD	-	
			LSE high drive	T_A = -40°C to 25°C	1.4	-	
				T_A = 55°C	TBD	-	
				T_A= 85°C	TBD	-	
				T_A = 105°C	TBD	-	

Table 29. Typical and maximum current consumptions in Stop mode(1) (continued)

Symbol	Parameter	Conditions		Typ	Max(2)	Unit
I_{DD} (Stop)	Supply current in Stop mode (RTC disabled)	Reg in LP mode, LSE/HSI/HSE OFF, independent watchdog with LSI enabled	T_A = -40°C to 25°C	TBD	TBD	µA
				TBD	TBD	
				TBD	TBD	
				TBD	TBD	
		LPTIM1 enabled, regulator in LP mode, HSI/HSE/LSE/LSI OFF (no independent watchdog), 0 Hz external clock on LPTIM1_IN1	T_A = -40°C to 25°C	0.415	TBD	
		LPTIM1 enabled, regulator in LP mode, HSI/HSE/LSE/LSI OFF (no independent watchdog), 100 Hz external clock on LPTIM1_IN1		0.42	TBD	
		LPTIM1 enabled, regulator in LP mode, HSI/HSE/LSE/LSI OFF (no independent watchdog), 100 KHz external clock on LPTIM1_IN1		1.2	TBD	
		LPTIM1 enabled. regulator in LP mode, HSI/HSE/LSE/LSI OFF (no independent watchdog), 1 MHz external clock on LPTIM1_IN1		5.6	TBD	
		LPUART1 enabled and clocked by LSE external quartz at 32,768 kHz, regulator in LP mode, HSI/HSE/LSI OFF (no independent watchdog), LSE Low drive		0.785	TBD	
		LPUART1 enabled and clocked by LSE external quartz at 32,768 kHz, regulator in LP mode, HSI, HSE, and LSI OFF (no independent watchdog), LSE High drive		TBD	TBD	
		LPUART1 enabled and clocked by LSE(5) 32,768 kHz, regulator in LP mode, HSI/HSE/LSI OFF (no independent watchdog)		TBD	TBD	
		LPTIM1 and LPUART1 enabled and clocked by LSE(5), LSE bypass, regulator in LP mode, HSI/HSE/LSI OFF (no independent watchdog)		TBD	TBD	
		Regulator in Low power mode, LSI/LSE/HSI/HSE OFF (no independent watchdog)	T_A = -40°C to 25°C	0.415	TBD	
			T_A = 55°C	TBD	TBD	
			T_A= 85°C	TBD	TBD	
			T_A = 105°C	TBD	TBD(6)	
			T_A = 125°C	-	28	

Table 29. Typical and maximum current consumptions in Stop mode(1) (continued)

Symbol	Parameter	Conditions		Typ	Max(2)	Unit
I_{DD} (Stop)	Supply current in Stop mode (LPTIM1 enabled)	Regulator in Low power mode, HSI/HSE OFF, LSE Bypass and independent watchdog with LSI enabled	T_A = -40°C to 25°C	TBD	TBD	µA
			T_A = 55°C	TBD	TBD	
			T_A= 85°C	TBD	TBD	
			T_A = 105°C	TBD	TBD	
		Regulator in Low power mode, LSI/HSI/HSE OFF, LSE Bypass (no independent watchdog)	T_A = -40°C to 25°C	TBD	TBD	
			T_A = 55°C	TBD	TBD	
			T_A= 85°C	TBD	TBD	
			T_A = 105°C	TBD	TBD	
	Supply current in Stop mode (LPUART1 enabled)	Regulator in Low power mode, HSI/HSE OFF, LSE Bypass and independent watchdog with LSI enabled	T_A = -40°C to 25°C	TBD	TBD	
			T_A = 55°C	TBD	TBD	
			T_A= 85°C	TBD	TBD	
			T_A = 105°C	TBD	TBD	
		Regulator in Low power mode, LSI/HSI/HSE OFF, LSE Bypass (no independent watchdog)	T_A = -40°C to 25°C	TBD	TBD	
			T_A = 55°C	TBD	TBD	
			T_A= 85°C	TBD	TBD	
			T_A = 105°C	TBD	TBD	
I_{DD} (WU from Stop)	Supply current during wakeup from Stop mode	MSI = 4.2 MHz	T_A = -40°C to 25°C	TBD	-	mA
		MSI = 1.05 MHz		TBD	-	
		MSI = 65 kHz(7)		TBD	-	
		HSI16 = 16 MHz		TBD	-	
		HSI16/4 = 4 MHz		TBD	-	

1. TBD stands for “to be defined”.
2. Based on characterization, not tested in production, unless otherwise specified.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. LSE Low drive unless otherwise specified.
5. Oscillator bypassed (LSEBYP = 1 in RCC_CSR register).
6. Tested in production.
7. When MSI = 64 kHz, the RMS current is measured over the first 15 µs following the wakeup event. For the remaining part of the wakeup period, the current corresponds the Run mode current.

The following current consumption curve will be provided in next revision of this datasheet:

- I_{DD} vs V_{DD}, at T_A= -40 °C/25 °C/55 °C/ 85 °C, Stop mode with RTC enabled, all clocks OFF
- I_{DD} vs V_{DD}, at T_A= -40 °C/25 °C/55 °C/ 85 °C, Stop mode with RTC disabled, all clocks OFF

Table 30. Typical and maximum current consumptions in Standby mode(1)

Symbol	Parameter	Conditions		Typ	Max(2)	Unit
I_{DD} (Standby with RTC)	Supply current in Standby mode with RTC enabled	RTC clocked by LSI (no independent watchdog)	T_A = -40 °C to 25 °C, V_{DD} = 1.8 V	0.93	TBD	µA
			T_A = -40 °C to 25 °C	1.2	TBD	
			T_A = 55 °C	TBD	TBD	
			T_A= 85 °C	TBD	TBD	
			T_A = 105 °C	TBD	TBD	
			T_A = 125 °C	TBD	TBD	
		RTC clocked by LSI (with independent watchdog)	T_A = -40 °C to 25 °C, V_{DD} = 1.8 V	TBD	TBD	
			T_A = -40 °C to 25 °C	TBD	TBD	
			T_A = 55 °C	TBD	TBD	
			T_A= 85 °C	TBD	TBD	
			T_A = 105 °C	TBD	TBD	
			T_A = 125 °C	TBD	TBD	
		RTC clocked by LSE (no independent watchdog), oscillator bypassed (3)	T_A = -40 °C to 25 °C	TBD	TBD	
			T_A = -40 °C to 25 °C, V_{DD} = 1.8 V	TBD	TBD	
		RTC clocked by LSE 32.768 KHz external quartz (no independent watchdog), LSE low drive(3)	T_A = -40 °C to 25 °C, V_{DD} = 1.8 V	0.655	TBD	
			T_A = -40 °C to 25 °C	0.845	TBD	
			T_A = 55 °C	TBD	TBD	
			T_A= 85 °C	TBD	TBD	
			T_A = 105 °C	TBD	TBD	
			T_A = 125 °C	TBD	TBD	
		RTC clocked by LSE 32.768 KHz external quartz (no independent watchdog), LSE high drive(3)	T_A = -40 °C to 25 °C, V_{DD} = 1.8 V	1	-	
			T_A = -40 °C to 25 °C	1.2	-	
			T_A = 55 °C	TBD	-	
			T_A= 85 °C	TBD	-	
			T_A = 105 °C	TBD	-	
			T_A = 125 °C	TBD	-	
I_{DD} (Standby)	Supply current in Standby mode (RTC disabled)	Independent watchdog and LSI enabled	T_A = -40 °C to 25 °C	TBD	TBD	
			T_A = 55 °C	TBD	TBD	
			T_A= 85 °C	TBD	TBD	
			T_A = 105 °C	TBD	TBD	

Table 30. Typical and maximum current consumptions in Standby mode(1) (continued)

Symbol	Parameter	Conditions		Typ	Max(2)	Unit
I_{DD} (Standby)	Supply current in Standby mode (RTC disabled)	Independent watchdog and LSI OFF	T_A = -40 °C to 25 °C	0.29	TBD	µA
			T_A = 55 °C	TBD	TBD	
			T_A = 85 °C	TBD	TBD	
			T_A = 105 °C	TBD	TBD	
			T_A = 125 °C	TBD	9	
I_{DD} (WU from Standby)	Supply current during wakeup time from Standby mode	-	T_A = -40 °C to 25 °C	TBD	-	mA

1. TBD stands for “to be defined”.
2. Based on characterization, not tested in production, unless otherwise specified
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

Table 31. Peripheral current consumption(1)(2)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB1	WWDG	TBD	TBD	TBD	TBD	µA/MHz (f_{HCLK})
	SPI2	TBD	TBD	TBD	TBD	
	LPUART	TBD	TBD	TBD	TBD	
	I2C1	TBD	TBD	TBD	TBD	
	I2C2	TBD	TBD	TBD	TBD	
	USB	TBD	TBD	TBD	TBD	
	DAC1	TBD	TBD	TBD	TBD	
	USART2	TBD	TBD	TBD	TBD	

Table 31. Peripheral current consumption(1)(2) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB2	COMP1	TBD	TBD	TBD	TBD	µA/MHz (f_{HCLK})
	COMP2	TBD	TBD	TBD	TBD	
	ADC1(3)	TBD	TBD	TBD	TBD	
	SPI1	TBD	TBD	TBD	TBD	
	USART1	TBD	TBD	TBD	TBD	
	TIM2	TBD	TBD	TBD	TBD	
	TIM21	TBD	TBD	TBD	TBD	
	TIM22	TBD	TBD	TBD	TBD	
	TIM6	TBD	TBD	TBD	TBD	
Cortex-M0+ core I/O port	GPIOA	TBD	TBD	TBD	TBD	µA/MHz (f_{HCLK})
	GPIOB	TBD	TBD	TBD	TBD	
	GPIOC	TBD	TBD	TBD	TBD	
	GPIOD	TBD	TBD	TBD	TBD	
	GPIOH	TBD	TBD	TBD	TBD	
AHB	CRC	TBD	TBD	TBD	TBD	µA/MHz (f_{HCLK})
	FLASH	TBD	TBD	TBD	TBD	
	DMA1	TBD	TBD	TBD	TBD	
All enabled		TBD	TBD	TBD	TBD	
SYSCFG & RI		TBD	TBD	TBD	TBD	µA/MHz (f_{HCLK})
PWR		TBD	TBD	TBD	TBD	
$I_{DD\ (RTC)}$		TBD				µA
$I_{DD\ (ADC)}$(4)		TBD				
$I_{DD\ (DAC)}$(5)		TBD				
$I_{DD\ (COMP1)}$		TBD				
$I_{DD\ (COMP2)}$	Slow mode	TBD				
	Fast mode	TBD				
$I_{DD\ (PVD\ /\ BOR)}$(6)		TBD				
$I_{DD\ (IWDG)}$		TBD				

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.

2. TBD stands for “to be defined”.
3. HSI oscillator is OFF for this measure.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion (HSI consumption not included).
5. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of $V_{DD}/2$. DAC is in buffered mode, output is left floating.
6. Including supply current of internal reference voltage.

6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Table 32. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	TBD	-	µs
$t_{WUSLEEP\_LP}$	Wakeup from Low-power sleep mode, f_{HCLK} = 262 kHz	f_{HCLK} = 262 kHz Flash enabled	TBD	-	
		f_{HCLK} = 262 kHz Flash switched OFF	TBD	-	
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz	TBD	-	
		$f_{HCLK} = f_{HSI}$ = 16 MHz	TBD	-	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	TBD	-	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 1 and 2	TBD	TBD	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 3	TBD	TBD	
		$f_{HCLK} = f_{MSI}$ = 2.1 MHz	TBD	TBD	
		$f_{HCLK} = f_{MSI}$ = 1.05 MHz	TBD	TBD	
		$f_{HCLK} = f_{MSI}$ = 524 kHz	TBD	TBD	
		$f_{HCLK} = f_{MSI}$ = 262 kHz	TBD	TBD	
		$f_{HCLK} = f_{MSI}$ = 131 kHz	TBD	TBD	
		f_{HCLK} = MSI = 65 kHz	TBD	TBD	
		$f_{HCLK} = f_{HSI}$ = 16 MHz	TBD	-	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	TBD	-	
	Wakeup from Stop mode, regulator in low-power mode, code running from RAM	$f_{HCLK} = f_{HSI}$ = 16 MHz	TBD	TBD	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	TBD	TBD	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz	TBD	TBD	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	f_{HCLK} = MSI = 2.1 MHz	TBD	TBD	
	Wakeup from Standby mode FWU bit = 0	f_{HCLK} = MSI = 2.1 MHz	TBD	TBD	ms

1. Based on characterization, not tested in production, unless otherwise specified

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

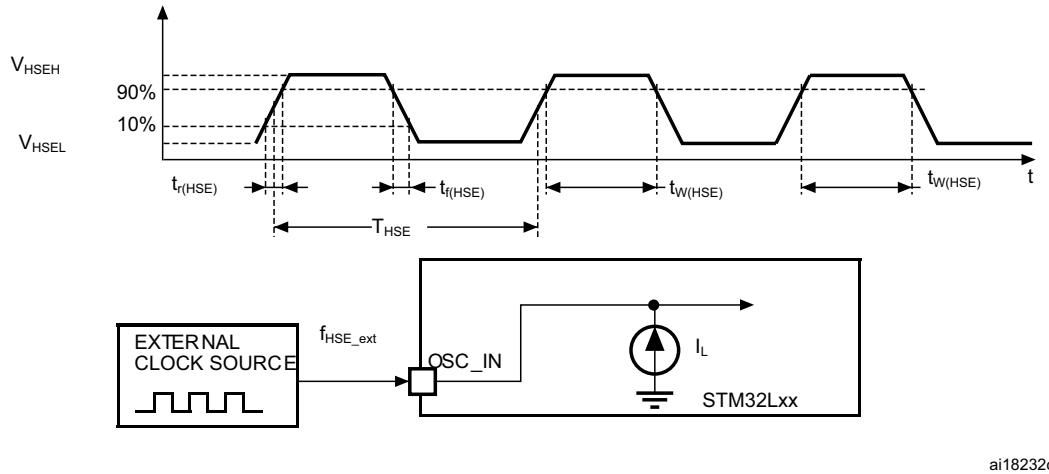
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.12*. However, the recommended clock input waveform is shown in *Figure 9*.

Table 33. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance		-	2.6	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 9. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

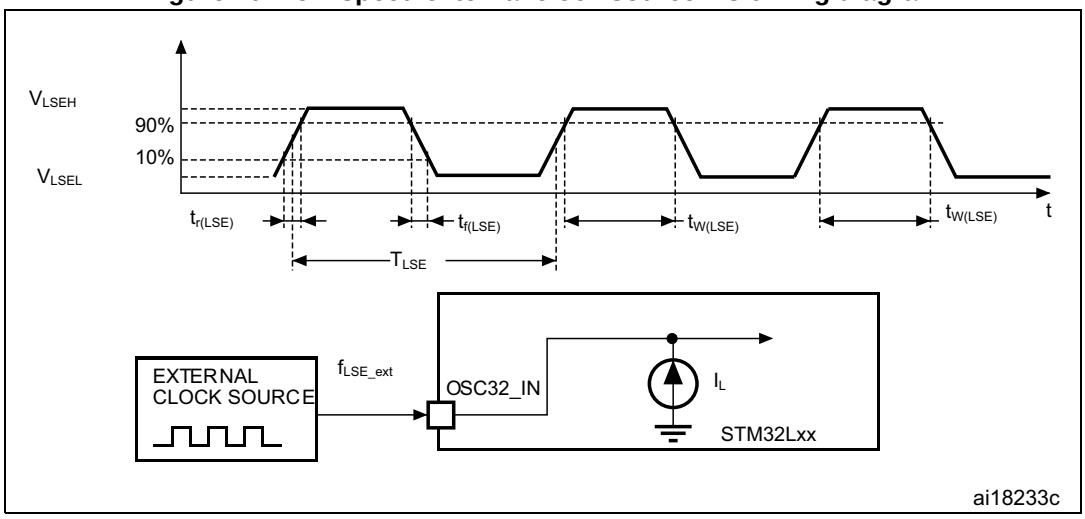
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 20*.

Table 34. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production

Figure 10. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 35*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization

time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

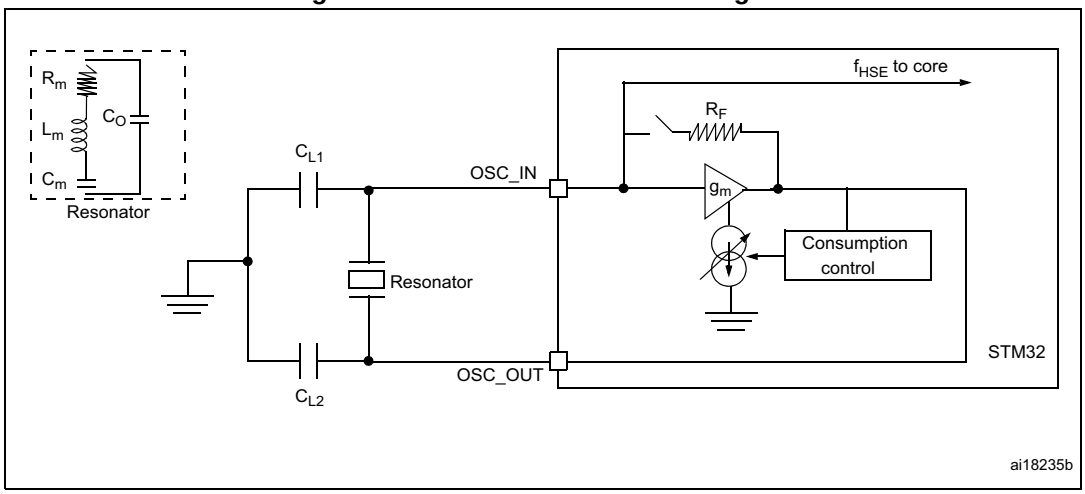
Table 35. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		24	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	20	-	pF
I_{HSE}	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA /V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization results, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 11*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 11. HSE oscillator circuit diagram



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 36*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 36. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

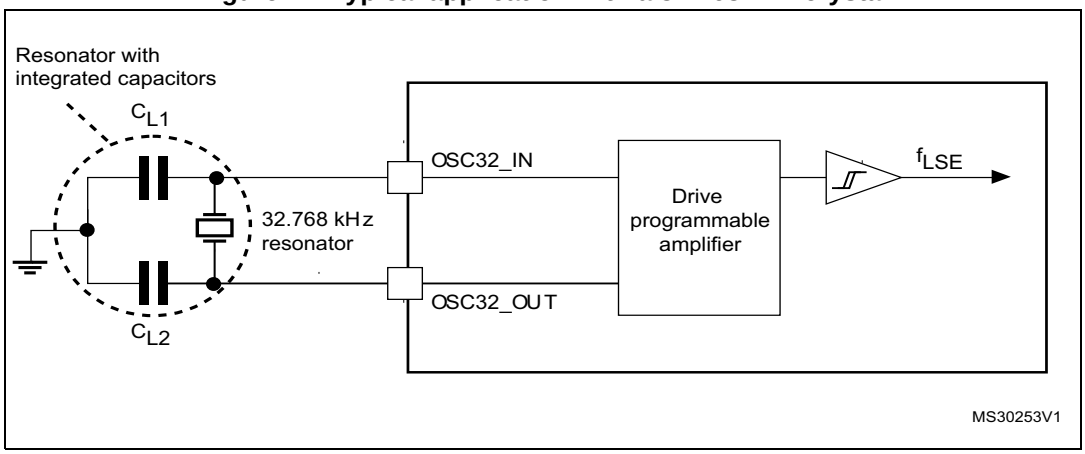
Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]= 01 medium low driving capability	-	-	1	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	8	-	-	
		LSEDRV[1:0] = 10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.

2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 12. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.7 Internal clock source characteristics

The parameters given in *Table 37* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

High-speed internal 16 MHz (HSI16) RC oscillator

Table 37. 16 MHz HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI16 user-trimmed resolution	Trimming code is not a multiple of 16	-	± 0.4	0.7	%
		Trimming code is a multiple of 16	-	-	± 1.5	%
ACC_{HSI16} (2)	Accuracy of the factory-calibrated HSI16 oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1(3)	-	1(3)	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = -40 to 105 °C	-4	-	3	%
$t_{SU(HSI16)}^{(2)}$	HSI16 oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI16)}^{(2)}$	HSI16 oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Based on characterization, not tested in production.
3. Tested in production.

High-speed internal 48 MHz (HSI48) RC oscillator

Table 38. HSI48 oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	Frequency		-	48	-	MHz
TRIM	HSI48 user-trimming step		0.09(3)	0.14	0.2(3)	%
$DuCy_{(HSI48)}$	Duty cycle		45(3)	-	55(3)	%
ACC_{HSI48}	Accuracy of the HSI48 oscillator (factory calibrated)	T_A = –40 to 105 °C	TBD	-	TBD	%
		T_A = –10 to 85 °C	TBD	-	TBD	%
		T_A = 0 to 70 °C	TBD	-	TBD	%
		T_A = 25 °C	TBD	-	TBD	%
$t_{su(HSI48)}$	HSI48 oscillator startup time		-	-	TBD	µs
$I_{DDA(HSI48)}$	HSI48 oscillator power consumption		-	TBD	TBD	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. TBD stands for “to be defined”.
3. Guaranteed by design, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 39. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(1)	LSI frequency	26	38	56	kHz
D_{LSI}(2)	LSI oscillator frequency drift 0°C ≤ T_A ≤ 85°C	-10	-	4	%
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	400	510	nA

1. Tested in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design, not tested in production.

Multi-speed internal (MSI) RC oscillator

Table 40. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤ T_A ≤ 85 °C	-	±3	-	%
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤ V_{DD} ≤ 3.6 V, T_A = 25 °C	-	-	2.5	%/V
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	

Table 40. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	
$t_{STAB(MSI)}$(2)	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Based on characterization, not tested in production.

6.3.8 PLL characteristics

The parameters given in *Table 41* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Table 41. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	2	-	24	MHz
	PLL input clock duty cycle	45	-	55	%
f_{PLL_OUT}	PLL output clock	2	-	32	MHz
t_{LOCK}	Worst case PLL lock time PLL input = 2 MHz PLL VCO = 96 MHz	-	TBD	TBD	µs
Jitter	Cycle-to-cycle jitter	-		±600	ps
I_{DDA}(PLL)	Current consumption on V_{DDA}	-	220	450	µA
I_{DD}(PLL)	Current consumption on V_{DD}	-	120	150	

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

6.3.9 Memory characteristics

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

RAM memory

Table 42. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode(1)	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 43. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming time for word or half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during the whole programming / erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	TBD	TBD	µA
	Maximum current (peak) during the whole programming / erase operation		-	TBD	TBD	mA

1. Guaranteed by design, not tested in production.

Table 44. Flash memory and data EEPROM endurance and retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{CYC}(2)	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	-	-	kcycles
	Cycling (erase / write) EEPROM data memory		100	-	-	
t_{RET}(2)	Data retention (program memory) after 10 kcycles at T_A = 85 °C	T_{RET} = +85 °C	30	-	-	years
	Data retention (EEPROM data memory) after 100 kcycles at T_A = 85 °C		30	-	-	
	Data retention (program memory) after 10 kcycles at T_A = 105 °C	T_{RET} = +105 °C	10	-	-	
	Data retention (EEPROM data memory) after 100 kcycles at T_A = 105 °C		10	-	-	

1. Based on characterization not tested in production.
2. Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 45*. They are based on the EMS levels and classes defined in application note AN1709.

Table 45. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 46. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. frequency range			Unit
				4 MHz voltage range 3	16 MHz voltage range 2	32 MHz voltage range 1	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	3	-6	-5	dBµV
			30 to 130 MHz	18	4	-7	
			130 MHz to 1GHz	15	5	-7	
			SAE EMI Level	2.5	2	1	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 47. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1.	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 48. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the *Table 49*.

Table 49. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PA1 or PA4 with induced leakage current on the other pin of the group less that -10 µA	-5	NA	
	Injected current on PA4 or PA7 with induced leakage current on the other pin of the group less that -10 µA	-5	NA	
	Injected current on PA5 or PB0 with induced leakage current on the other pin of the group less that -10 µA	-5	NA	
	Injected current on all 5 V tolerant (FT) pins	-5 (1)	NA	
	Injected current on any other pin	-5 (1)	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 20*. All I/Os are CMOS and TTL compliant.

Table 50. I/O static characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage for all I/Os except for BOOT0	V_{DD}=3.3 V, T_A=25 °C	-	-	$0.3V_{DD}$(2)	V
	Input low level voltage for BOOT0		-	-	$0.14V_{DD}$	
V_{IH}	Input high level voltage for all I/Os except for BOOT0		$0.7\ V_{DD}$(2)	-	-	
	Input high level voltage for BOOT0			-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis for FT and NRST I/Os (3)	1.6 V<V_{DD}<3.6 V	-	10% V_{DD}(4)	-	
	I/O Schmitt trigger voltage hysteresis for TC I/Os(3)		-	10% V_{DD}(4)	-	
	I/O Schmitt trigger voltage hysteresis for BOOT0(3)		-	10	-	mV
I_{lkg}	Input leakage current (5)	$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches	-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with USB	-	-	250	
		$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os	-	-	±50	
		FT I/O $V_{DD} \le V_{IN} \le 5$ V	-	-	±10	µA
R_{PU}	Weak pull-up equivalent resistor(6)(2)	$V_{IN} = V_{SS}$	30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor(6)	$V_{IN} = V_{DD}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. TBD stands for “to de defined’.
2. Tested in production
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
4. With a minimum of 200 mV. Based on characterization, not tested in production.
5. The max. value may be exceeded if negative current is injected on adjacent pins.
6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA with the non-standard V_{OL}/V_{OH} specifications given in *Table 51*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 18*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 18*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*. All I/Os are CMOS and TTL compliant.

Table 51. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)(2)	Output low level voltage for an I/O pin	I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)(2)	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
V_{OL} (3)(4)	Output low level voltage for an I/O pin	I_{IO} =+ 4 mA 1.65 V < V_{DD} < 2.7 V	-	0.45	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-0.45	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-1.3	-	
V_{OLFM+} (4)	Output low level voltage for an FTf I/O pin in Fm+ mode	TBD	-	TBD	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 18* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. Tested in production.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 18* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 13* and *Table 52*, respectively.

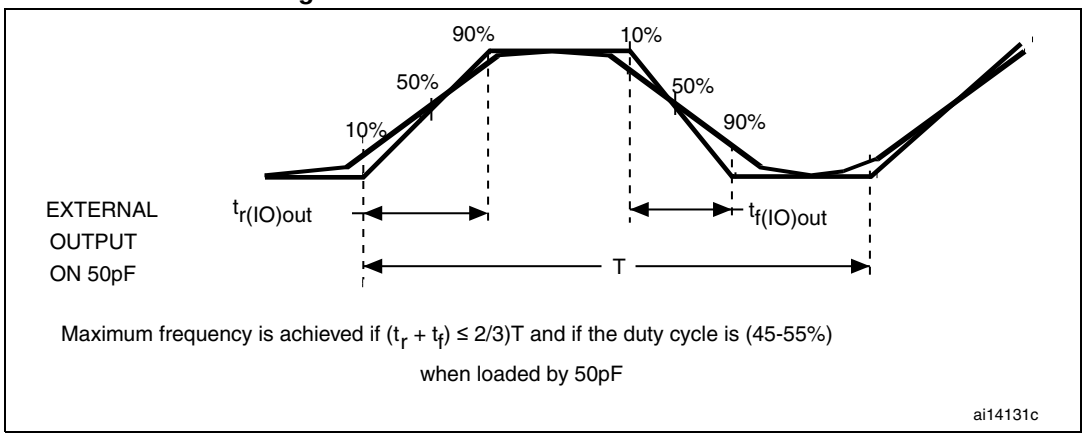
Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Table 52. I/O AC characteristics(1)

OSPEEDRx [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max(2)	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	400	kHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	400	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	625	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	625	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	2	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	1	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	125	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	250	
10	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	10	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	2	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	25	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	125	
11	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	8	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	30	
Fm+ configuration (4)	$f_{max(IO)out}$	Maximum frequency(3)	CL = 50 pF	-	TBD	MHz
	$t_{f(IO)out}$	Output fall time		-	TBD	ns
	$t_{r(IO)out}$	Output rise time		-	TBD	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	8	-	

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the line reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design. Not tested in production.
3. The maximum frequency is defined in *Figure 13*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the line reference manual for a detailed description of Fm+ I/O configuration.

Figure 13. I/O AC characteristics definition



6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 53*)

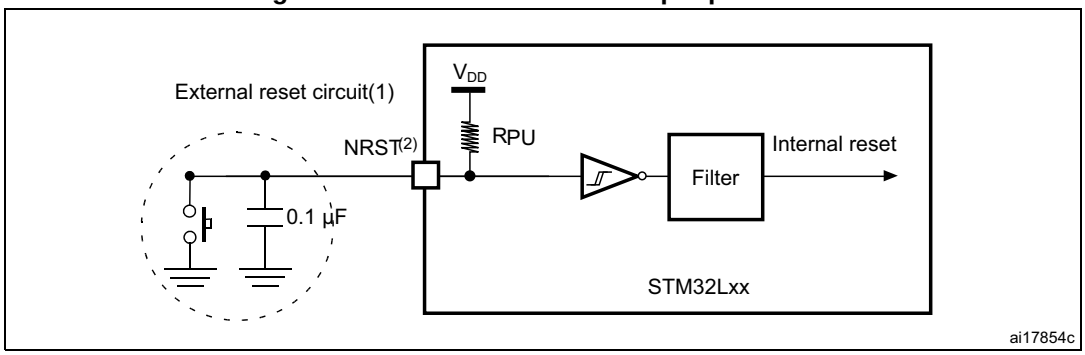
Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Table 53. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$(1)	NRST output low level voltage	I_{OL} = 2 mA 2.7 V < V_{DD} < 3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA 1.65 V < V_{DD} < 2.7 V	-	-		
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis	-	-	10%V_{DD}(2)	-	mV
R_{PU}	Weak pull-up equivalent resistor(3)	V_{IN} = V_{SS}	30	45	60	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	-	350	-	-	ns

1. Guaranteed by design, not tested in production.
2. 200 mV minimum value
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

Figure 14. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 53*. Otherwise the reset will not be taken into account by the device.

6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 54* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 20: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 54. ADC characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON		2.4	-	3.6	V
$I_{DDA\ (ADC)}$	Current consumption of the ADC(2)	1.14 Msps	-	TBD	-	mA
		10 ksps	-	TBD	-	
f_{ADC}	ADC clock frequency		0.6	-	16	MHz
f_S(3)	Sampling rate		0.05	-	1.14	MHz
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 16 MHz	-	-	941	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0	-	V_{DDA}	V
R_{AIN}(3)	External input impedance	See *Equation 1* and *Table 55* for details	-	-	50	kΩ
R_{ADC}(3)	Sampling switch resistance		-	-	1	kΩ
C_{ADC}(3)	Internal sample and hold capacitor		-	-	8	pF
t_{CAL}(3)	Calibration time	f_{ADC} = 16 MHz	5.2			µs
			83			$1/f_{ADC}$

Table 54. ADC characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$W_{LATENCY}$	ADC_DR register write latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr}(3)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2 = 16$ MHz	0.172			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4 = 8$ MHz	0.172			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI16} = 16$ MHz	TBD	-	TBD	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
t_S(3)	Sampling time	$f_{ADC} = 16$ MHz	0.093	-	15	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(3)	Power-up time		0	0	1	µs
t_{CONV}(3)	Total conversion time (including sampling time)	$f_{ADC} = 16$ MHz	1		15.75	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. TBD stands for “to be defined’.
2. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} should be taken into account.
3. Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 55. R_{AIN} max for f_{ADC} = 14 MHz

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)(1)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

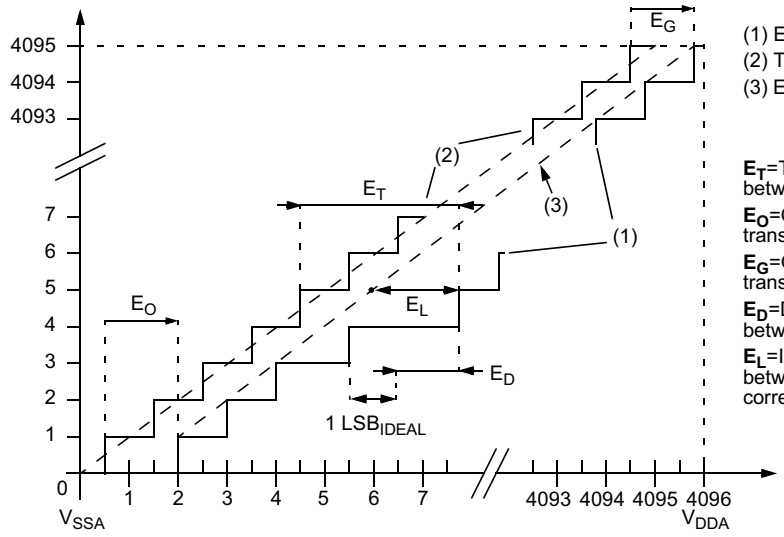
1. Guaranteed by design, not tested in production.

Table 56. ADC accuracy(1)(2)(3)(4)

Symbol	Parameter	Test conditions	Typ	Max(5)	Unit
ET	Total unadjusted error	f_{PCLK} = 32 MHz, f_{ADC} = 6 MHz, R_{AIN} < 10 kΩ V_{DDA} = 3.3 V T_A = 25 °C	±1.3	TBD	LSB
EO	Offset error		±0.4	TBD	
EG	Gain error		±0.4	TBD	
ED	Differential linearity error		±1	TBD	
EL	Integral linearity error		±1.6	TBD	
ET	Total unadjusted error	f_{PCLK} = 32 MHz, f_{ADC} = 6 MHz, R_{AIN} < 10 kΩ V_{DDA} = 1.8 to 3.6 V T_A = –40 to 105 °C	±2.9	TBD	LSB
EO	Offset error		±1.2	TBD	
EG	Gain error		±1.7	TBD	
ED	Differential linearity error		±1	TBD	
EL	Integral linearity error		±1.6	TBD	
ET	Total unadjusted error	f_{PCLK} = 32 MHz, f_{ADC} = 6 MHz, R_{AIN} < 10 kΩ V_{DDA} = 1.8 to 3.6 V T_A = 25 °C	±2.5	TBD	LSB
EO	Offset error		±0.9	TBD	
EG	Gain error		±1.2	TBD	
ED	Differential linearity error		±1	TBD	
EL	Integral linearity error		±1.6	TBD	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.12* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. TBD stands for “to be defined’.
5. Data based on characterization results, not tested in production.

Figure 15. ADC accuracy characteristics



(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T=Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.

E_O=Offset Error: deviation between the first actual transition and the first ideal one.

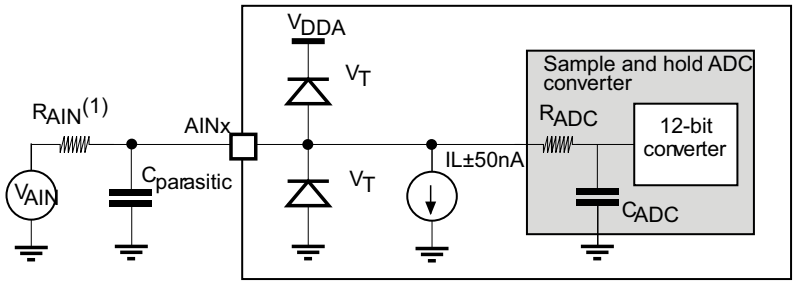
E_G=Gain Error: deviation between the last ideal transition and the last actual one.

E_D=Differential Linearity Error: maximum deviation between actual steps and the ideal one.

E_L=Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

MS19880V1

Figure 16. Typical connection diagram using the ADC



MSv34712V1

1. Refer to *Table 54: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.16 DAC electrical specifications

Data guaranteed by design, not tested in production, unless otherwise specified.

Table 57. DAC characteristics

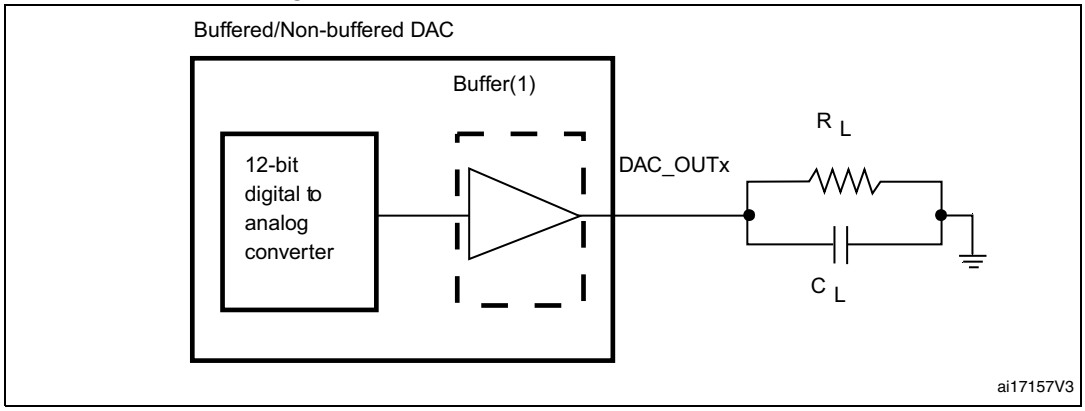
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage		1.8	-	3.6	V
I_{DDA}(1)	Current consumption on V_{DDA} supply V_{DDA} = 3.3 V	No load, middle code (0x800)	-	340	540	µA
		No load, worst code (0xF1C)	-	540	870	
R_L(1)	Resistive load	DAC output buffer ON	5	-	-	kΩ
C_L(1)	Capacitive load		-	-	50	pF
R_O	Output impedance	DAC output buffer OFF	6	8	10	kΩ
DNL(1)	Differential non linearity(2)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer ON	-	1.5	3	LSB
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer OFF	-	1.5	3	
INL(1)	Integral non linearity(3)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer ON	-	2	4	
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer OFF	-	2	4	
Offset(1)	Offset error at code 0x800 (4)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer ON	-	±10	±25	
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer OFF	-	±5	±8	
Offset1(1)	Offset error at code 0x001(5)	No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer OFF	-	±1.5	±5	
dOffset/dT(1)	Offset error temperature coefficient (code 0x800)	V_{DDA} = 3.3V T_A = 0 to 50 °C DAC output buffer OFF	-20	-10	0	µV/°C
		V_{DDA} = 3.3V T_A = 0 to 50 °C DAC output buffer ON	0	20	50	
Gain(1)	Gain error(6)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer ON	-	+0.1 / -0.2%	+0.2 / -0.5%	%
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer OFF	-	+0 / -0.2%	+0 / -0.4%	
dGain/dT(1)	Gain error temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C DAC output buffer OFF	-10	-2	0	µV/°C
		V_{DDA} = 3.3V T_A = 0 to 50 °C DAC output buffer ON	-40	-8	0	

Table 57. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TUE(1)	Total unadjusted error	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer ON	-	12	30	LSB
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer OFF	-	8	12	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	-	-	1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)(7)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	-	9	15	µs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	-	-60	-35	dB

1. Connected between DAC_OUT and V_{SSA}.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x800) and the ideal value = /2.
5. Difference between the value measured at Code (0x001) and the ideal value.
6. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is ON.
7. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Figure 17. 12-bit buffered/non-buffered DAC



6.3.17 Temperature sensor characteristics

Table 58. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

Table 59. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{130}	Voltage at 130°C ±5°C(2)	654	670	686	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(4)(3)	ADC sampling time when reading the temperature	10	-	-	

1. Guaranteed by characterization, not tested in production.
2. Measured at V_{DD} = 3 V ±10 mV. V130 ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design, not tested in production.
4. Shortest sampling time can be determined in the application by multiple iterations.

6.3.18 Comparators

Table 60. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV

Table 60. Comparator 1 characteristics (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

1. Based on characterization, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

Table 61. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay(2) in fast mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	1.2	4	
V_{offset}	Comparator offset error		-	±4	±20	mV
dThreshold/dt	Threshold voltage temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C V- =V_{REFINT}, 3/4 V_{REFINT}, 1/2 V_{REFINT}, 1/4 V_{REFINT}.	-	15	30	ppm /°C
I_{COMP2}	Current consumption(3)	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

1. Based on characterization, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

6.3.19 Timer characteristics

TIM timer characteristics

The parameters given in the *Table 62* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 62. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-		16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM6, TIM21, and TIM22 timers.

6.3.20 Communications interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I^2C timing requirements are guaranteed by design when the I^2C peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

All I^2C SDA and SCL I/Os embed an analog filter (see *Table 63* for the analog filter characteristics).

Table 63. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 20*.

Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 64. SPI characteristics(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	16	MHz
		Slave mode receiver			16	
		Slave mode Transmitter 1.65 V<V_{DD}<3.6 V	-	-	TBD (4)	
		Slave mode Transmitter 2.7 V<V_{DD}<3.6 V	-	-	16(4)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	TBD	-	-	
$t_{su(SI)}$		Slave mode	TBD	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	TBD	-	-	
$t_{h(SI)}$		Slave mode	TBD	-	-	
$t_{a(SO}$	Data output access time	Slave mode	TBD	-	TBD	
$t_{dis(SO}$	Data output disable time	Slave mode	TBD	-	TBD	
$t_{v(SO)}$	Data output valid time	Slave mode 1.65 V<V_{DD}<3.6 V	-	29	TBD	
		Slave mode 2.7 V<V_{DD}<3.6 V	-	22	TBD	
$t_{v(MO)}$		Master mode	-	10	TBD	
$t_{h(SO)}$	Data output hold time	Slave mode	TBD	-	-	
$t_{h(MO)}$		Master mode	TBD	-	-	

1. The characteristics above are given for voltage range 1.
2. Based on characterization, not tested in production.
3. TBD stands for “to be defined”.
4. The maximum SPL clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 18. SPI timing diagram - slave mode and CPHA = 0

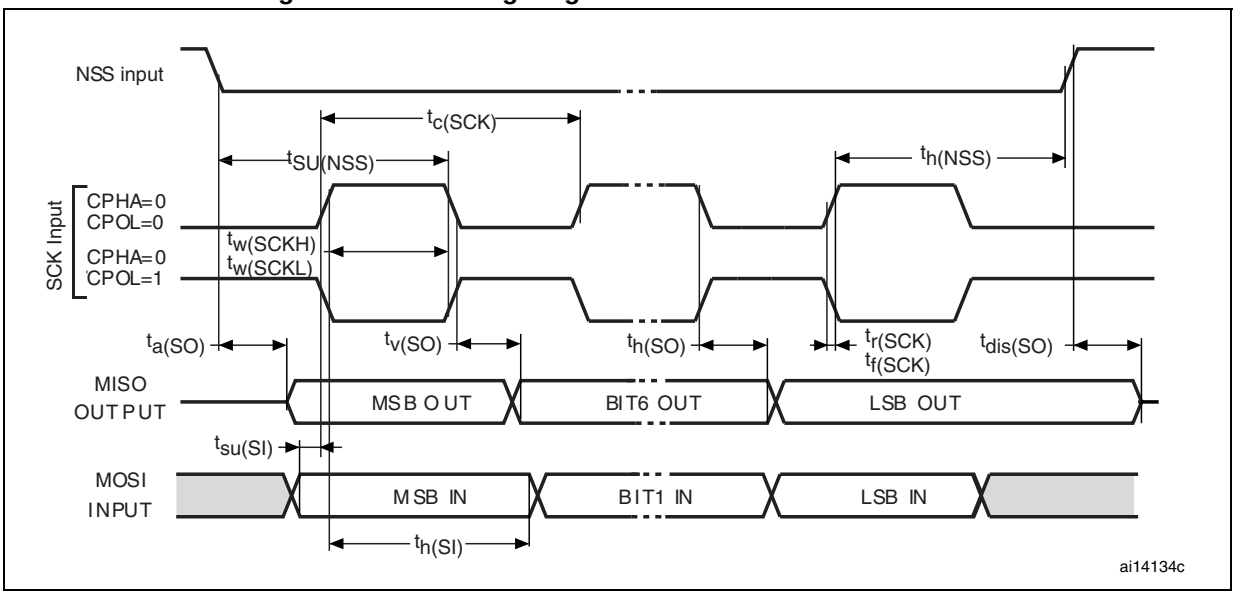
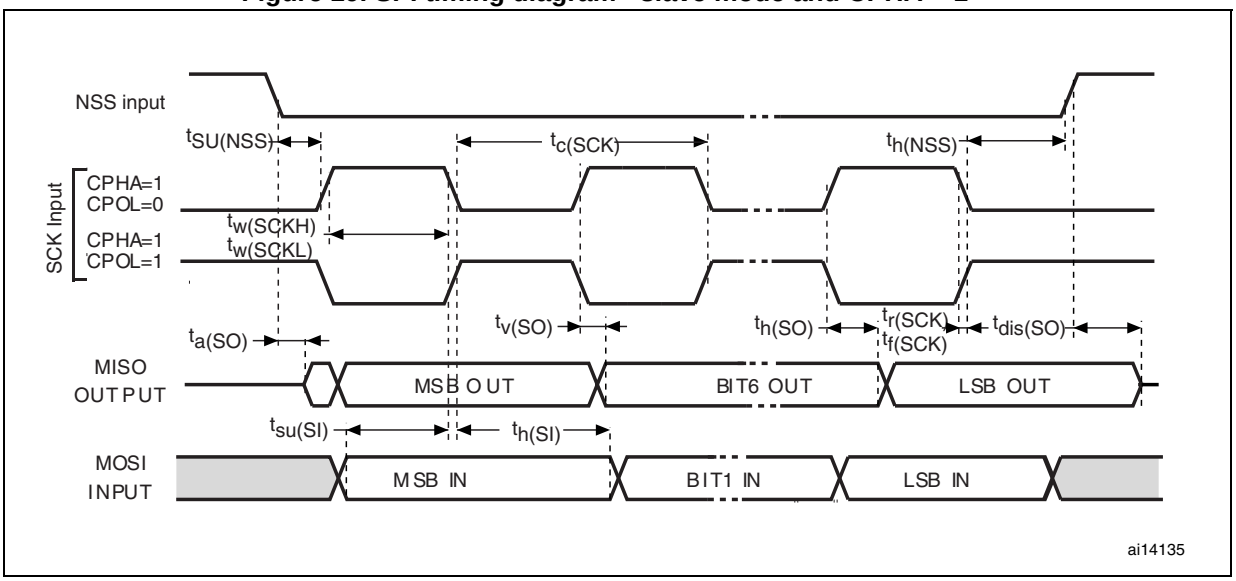
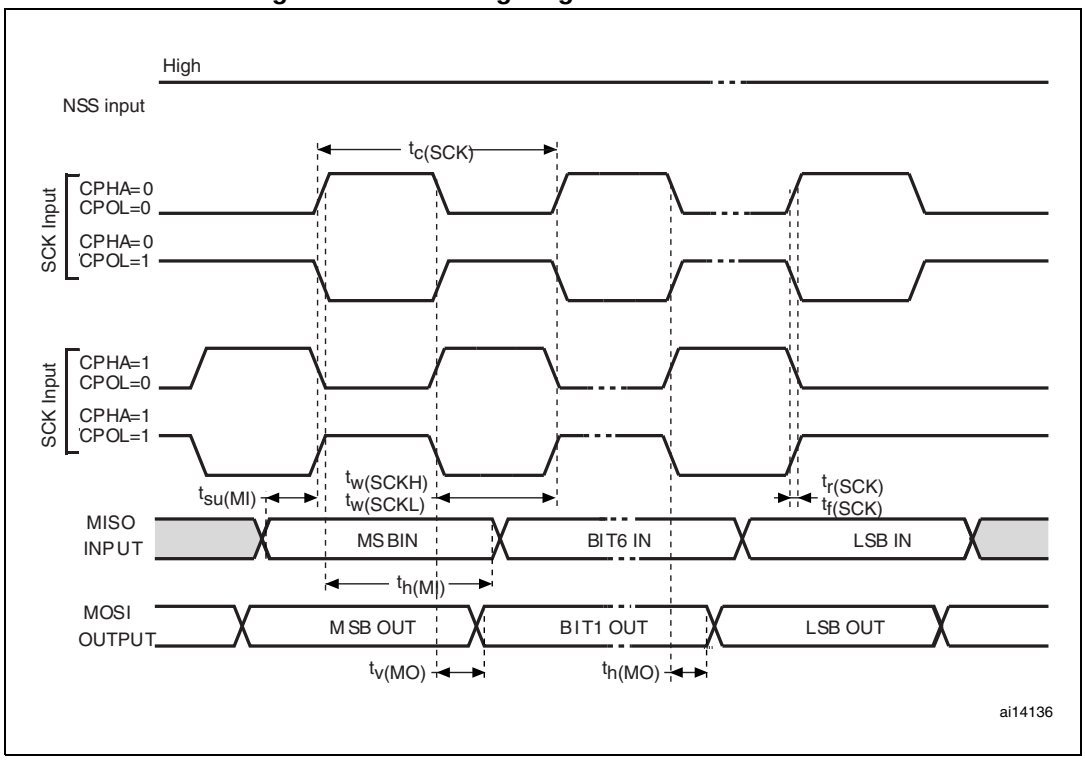


Figure 19. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 20. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

I2S characteristics

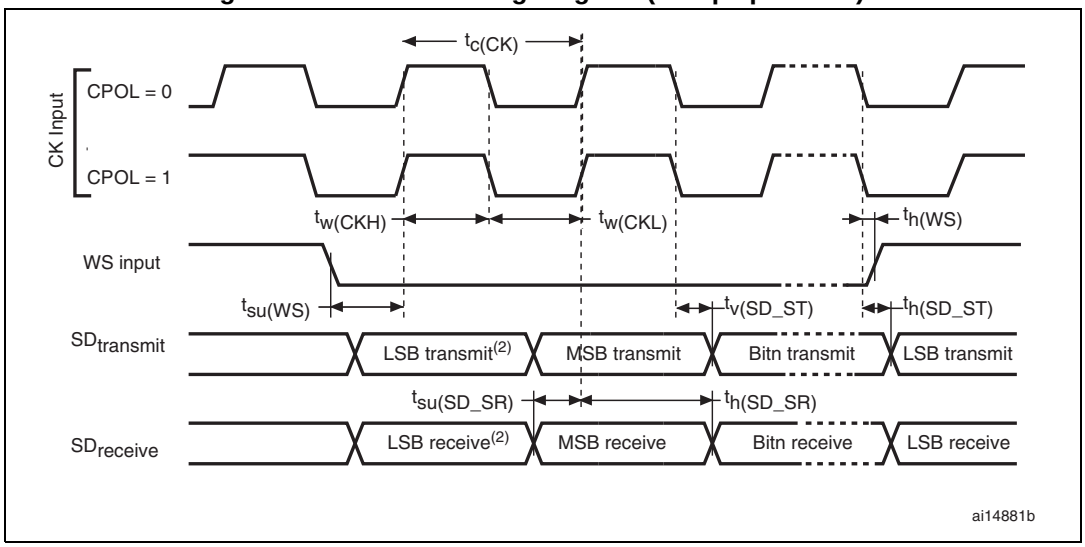
Table 65. I2S characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256xFs (3)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	TBD	ns
$t_{h(WS)}$	WS hold time	Master mode	TBD	-	
$t_{su(WS)}$	WS setup time	Slave mode	TBD	-	
$t_{h(WS)}$	WS hold time	Slave mode	TBD	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	TBD	-	
$t_{su(SD\_SR)}$		Slave receiver	TBD	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	TBD	-	
$t_{h(SD\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	TBD	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	TBD	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	TBD	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	TBD	-	

1. Based on characterization, not tested in production.
2. TBD stands for “to be defined”.
3. The maximum for 256xFs is 8 MHz

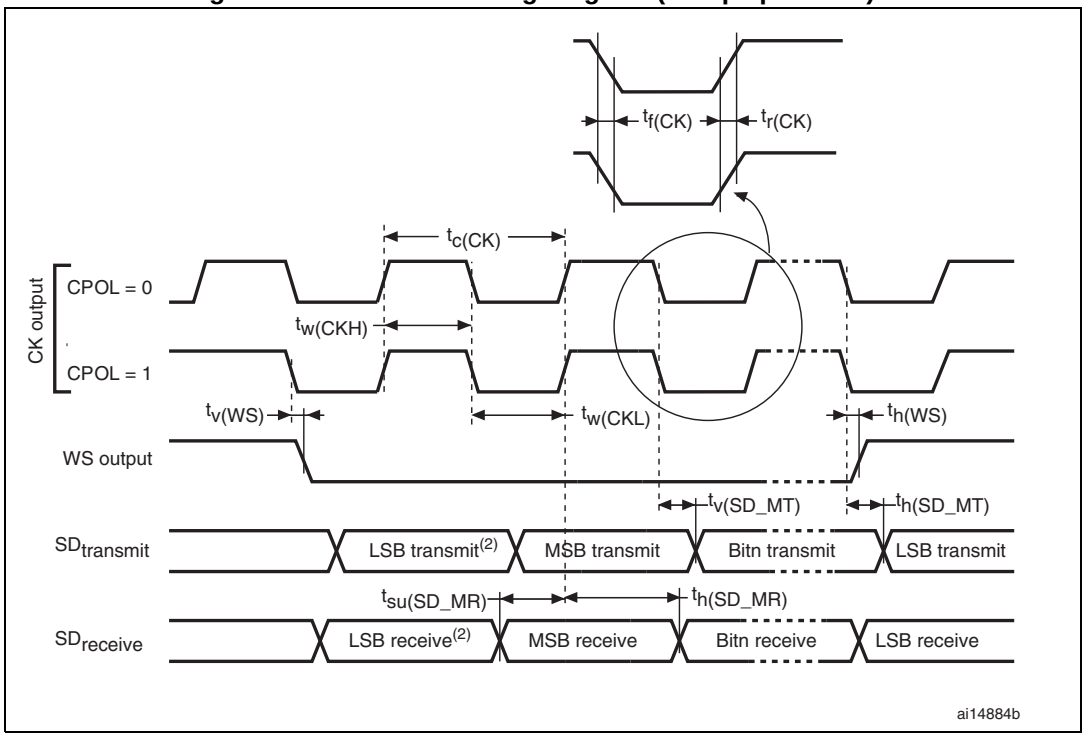
*Note: Refer to the I2S section of the product reference manual for more details about the sampling frequency (Fs), f_{MCK}, f_{CK} and D_{CK} values. These values reflect only the digital peripheral behavior, source clock precision might slightly change them. DCK depends mainly on the ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.*

Figure 21. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 22. I²S master timing diagram (Philips protocol)(1)



1. Based on characterization, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 66. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 67. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage	-	3.0	3.6	V
V_{DI}(2)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(2)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(2)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}(3)	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	0.3	V
V_{OH}(3)	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. Guaranteed by characterization, not tested in production.
3. Tested in production.
4. R_L is the load connected on the USB drivers.

Figure 23. USB timings: definition of data signal rise and fall time

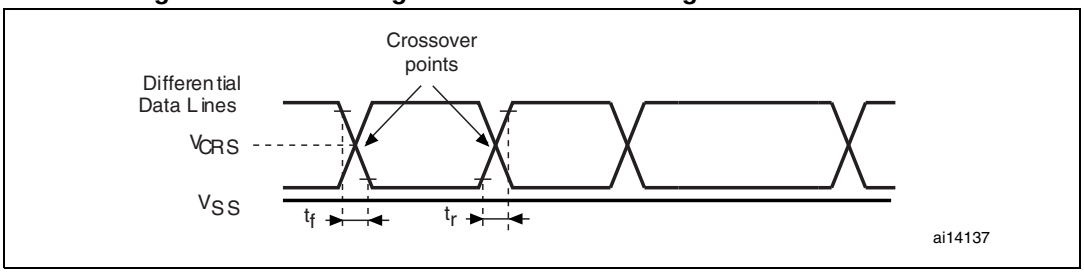


Table 68. USB: full speed electrical characteristics

Driver characteristics[1]					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time[2]	C_L = 50 pF	4	20	ns
t_f	Fall Time[2]	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

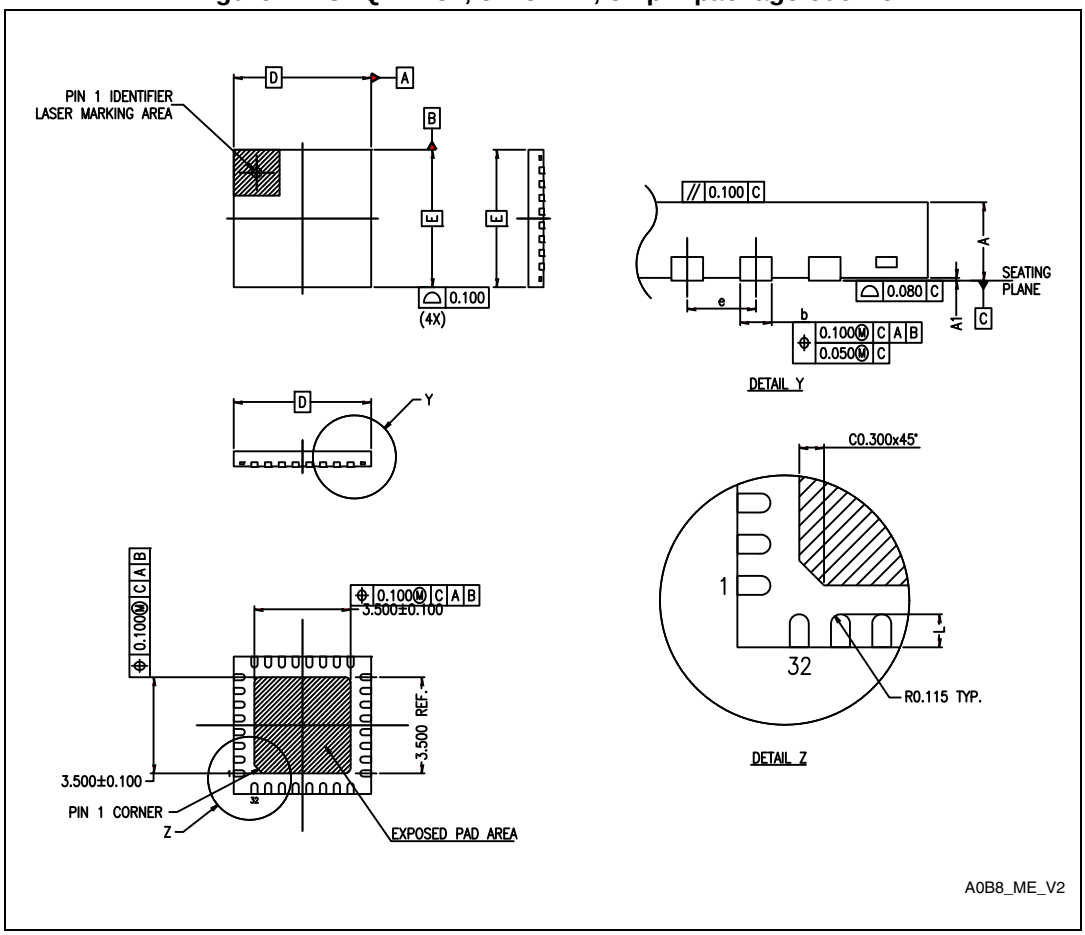
7 Package characteristics

7.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at http://www.st.com.* ECOPACK® is an ST trademark.

7.1.1 UFQFPN32 5 x 5 mm package

Figure 24. UFQFPN32, 5 x 5 mm, 32-pin package outline



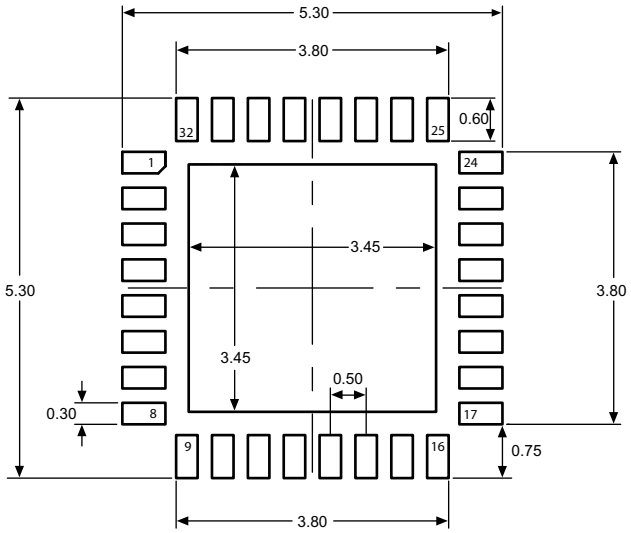
1. Drawing is not to scale.

Table 69. UFQFPN32, 5 x 5 mm, 32-pin package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.200	-	-	0.0079	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D2	3.200	3.450	3.700	0.1260	0.1358	0.1457
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E2	3.200	3.450	3.700	0.1260	0.1358	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

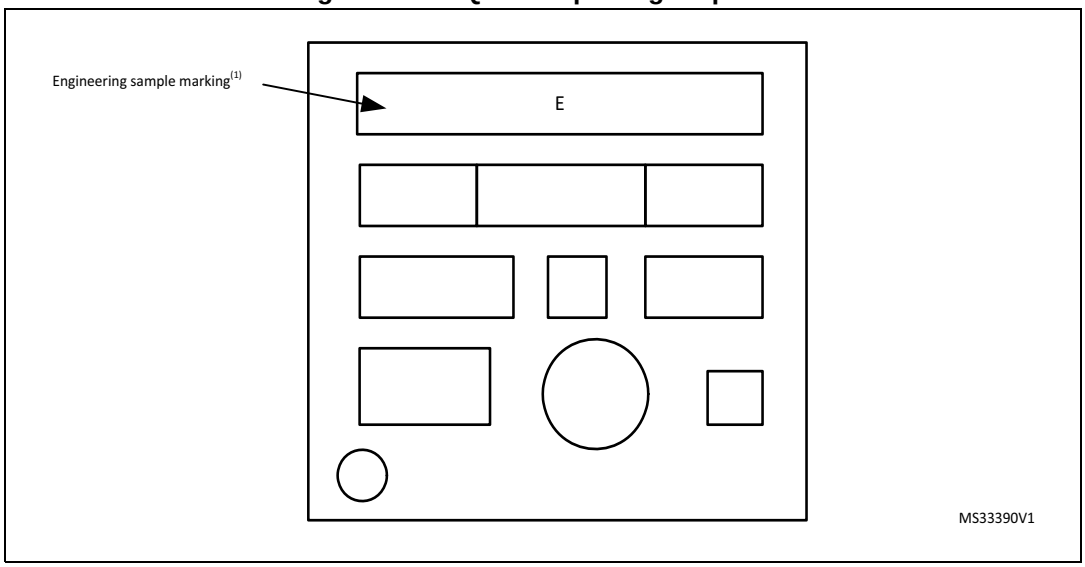
Figure 25. UFQFPN32 recommended footprint



1. Dimensions are expressed in millimeters.

Marking of engineering samples

Figure 26. UFQFPN32 package top view



1. Samples marked "E" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

7.2 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 70. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFQFPN32 - 5 x 5 mm / 0.5 mm pitch	38	°C/W

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

8 Ordering information

Table 71. STM32L062K8 ordering information scheme

Example: STM32 L 062 K 8 T 6 D xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

062 = USB + AES

Pin count

K = 32 pins

Flash memory size

8 = 64 Kbytes

Package

U = UFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled

D = V_{DD} range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

9 Revision history

Table 72. Document revision history

Date	Revision	Changes
27-Feb-2014	1	Initial release.

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