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Revisions

Rev	Description	Date	Approved
A	Initial Release	12/17/2015	
A1	Update C12 capacitor	5/27/2016	
A2	For production board	6/22/2016	
A3	Update R63 resistor	7/13/2016	

TWR-KE18F

Microcontroller Solutions Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: ____ IU: X PUBI: ____

Designer: Ben Wang	Drawing Title: TWR-KE18F		
Drawn by: Ben Wang	Page Title: TABLE OF CONTENTS		
Approved: Mario Guardado	Size: C	Document Number: SCH-29160 PDF: SPF-29160	Rev: A3
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1. Unless Otherwise Specified:
   All resistors are in ohms
   All capacitors are in uF
   All voltages are DC

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

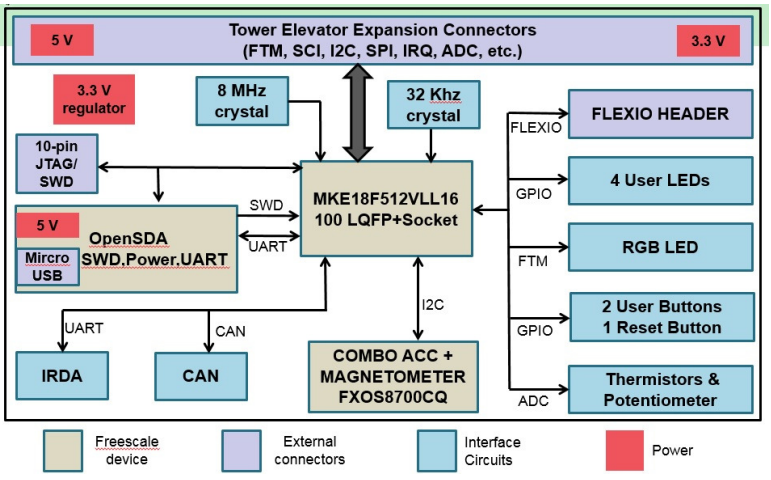
4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Power & Ground Nets

NET	VOLTAGE	DESCRIPTION
P5V_TRG_SDA	5V	Output of USB power switch controlled by the VTRG_EN signal from the OpenSDA and the ELE_PS_SENSE signal from the TWR elevator connectors. Goes to regulator input select header.
USB0_VBUS	5V	USB power from primary elevator Pin A57.
SDA_VOUT33	3.3V	Output of OpenSDA's K20 internal regulator to power OpenSDA's circurity
P5V_ELEV	5V	Power to the elevator boards.
P3V3_REG	3.3V	Output of 3.3V regulator or from the Elevator connectors. May also be supplied externally by connecting to the board voltage select header at pin 3.
V_BRD	3.3-5V	Output of 3.3V or 5V regulators as selected by the board voltage select header. May also be supplied externally by connecting to the board voltage select header at pin 3.
VREG_IN	5V	Power into the on board voltage regulators.
MCU_PWR	3.3-5V	MCU digital power. Filtered from V_BRD
MCU_VDD	3.3-5V	MCU digital power input after current measurement jumper
VDDA	3.3-5V	VDDA power for MCU and analog circuits. Filtered from MCU_PWR.
VREFH	3.3V-5V	Upper reference voltage for ADC on the MCU. Filtered from VDDA.
VREFL	0V	Lower reference voltage for ADC on the MCU. Filtered from VSSA.
VSSA	0V	VSSA power for MCU and analog circuits. Filtered from GND.
GND	0V	Digital and Analog Ground.

Block Diagram



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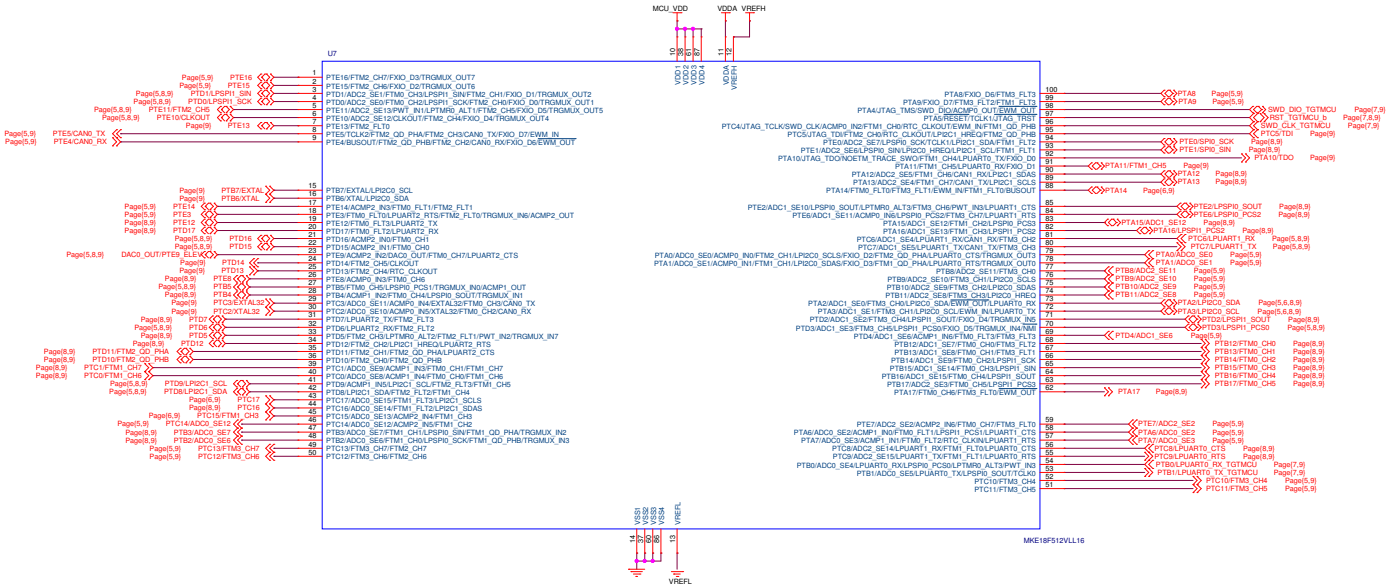

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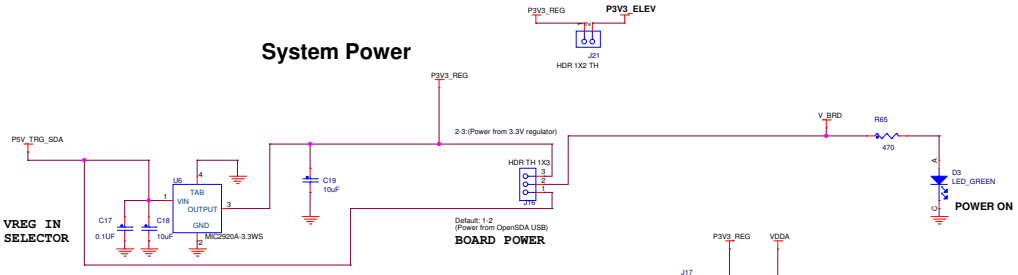
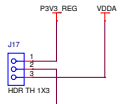
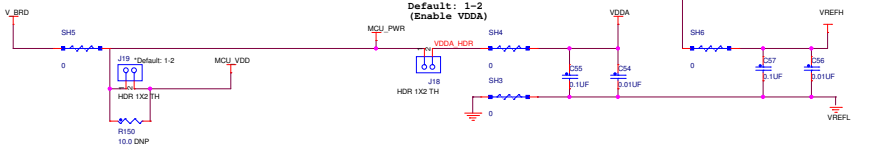
System Power





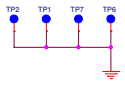
PWR_MCU



For dynamic current measurements

CAD NOTE:
Place this circuitry near the processor

GND LOOP TEST LOOPS



CAD NOTE:
Place ground test loops
in the four corners
away from sensitive signals
that might short
with scope probe alligator clips

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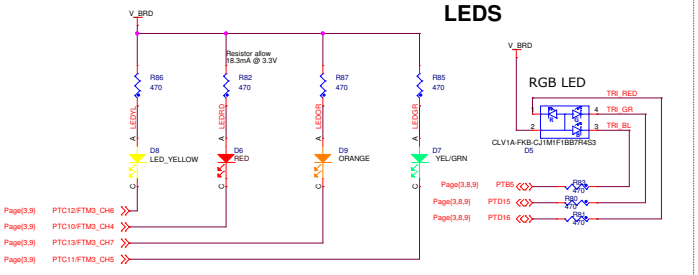
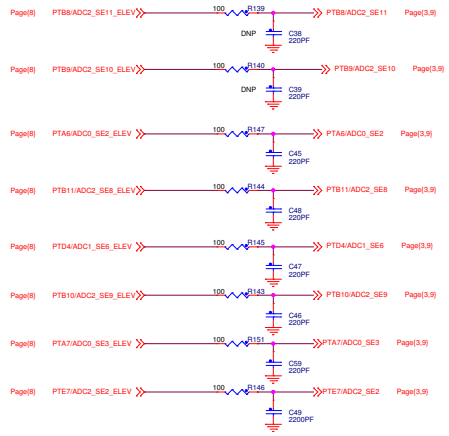
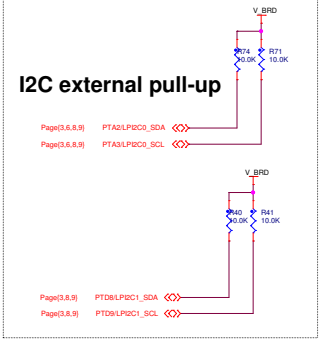
LEDS



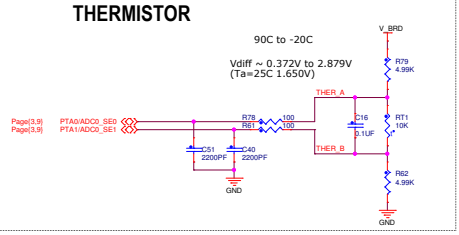
Motor control filters



I2C external pull-up

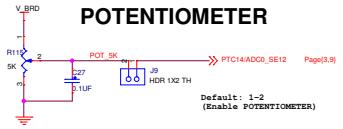


THERMISTOR

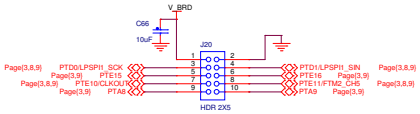


DAC0 output filter

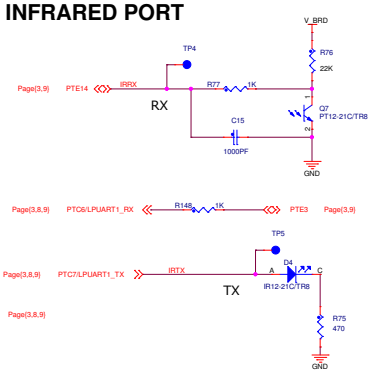
POTENTIOMETER



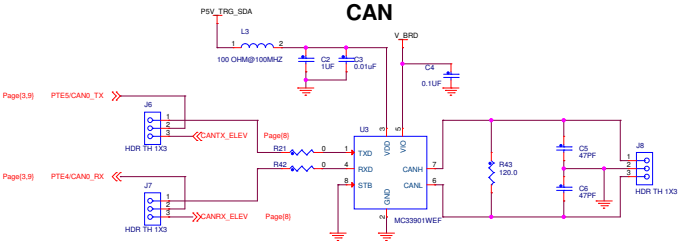
FLEXIO HEADER



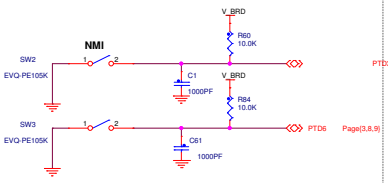
INFRARED PORT



CAN



PUSH BUTTONS



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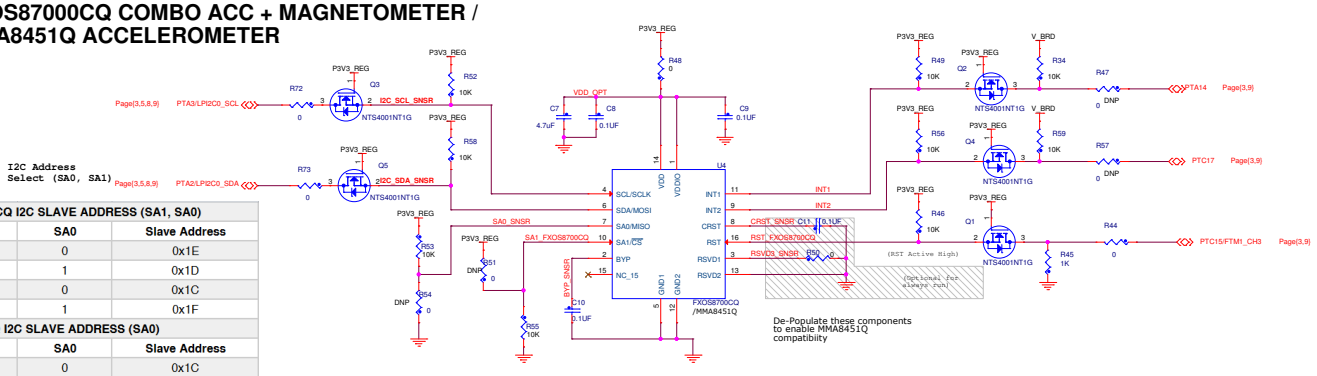
FXOS87000CQ COMBO ACC + MAGNETOMETER / MMA8451Q ACCELEROMETER



FXOS8700CQ I2C SLAVE ADDRESS (SA1, SA0)		
SA1	**SA0**	**Slave Address**
0	0	0x1E
0	1	0x1D
1	0	0x1C
1	1	0x1F
MMA8451Q I2C SLAVE ADDRESS (SA0)		
-	**SA0**	**Slave Address**
-	0	0x1C
-	1	0x1D

NXP

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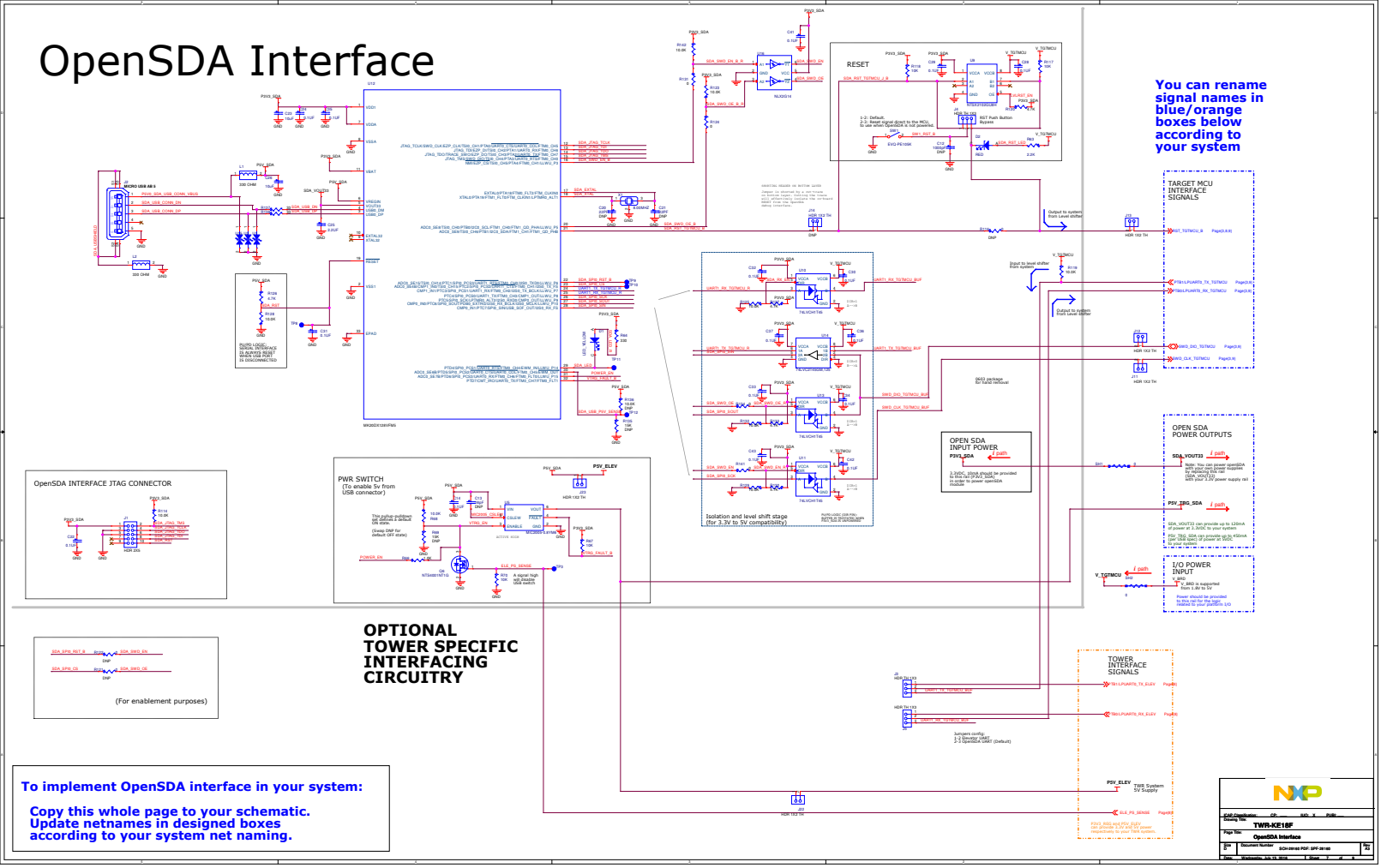
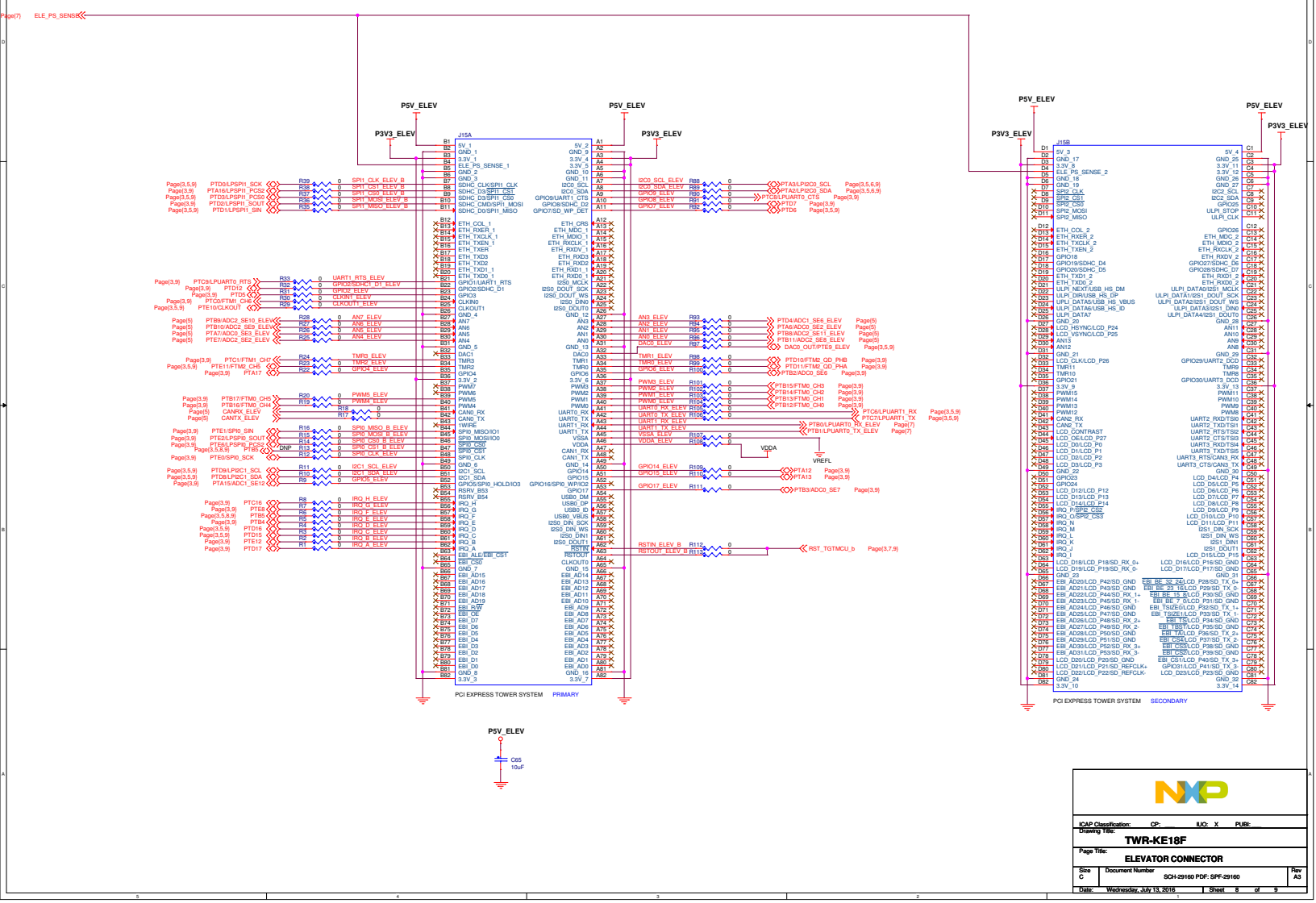
OpenSDA Interface



ELEVATOR CONNECTOR



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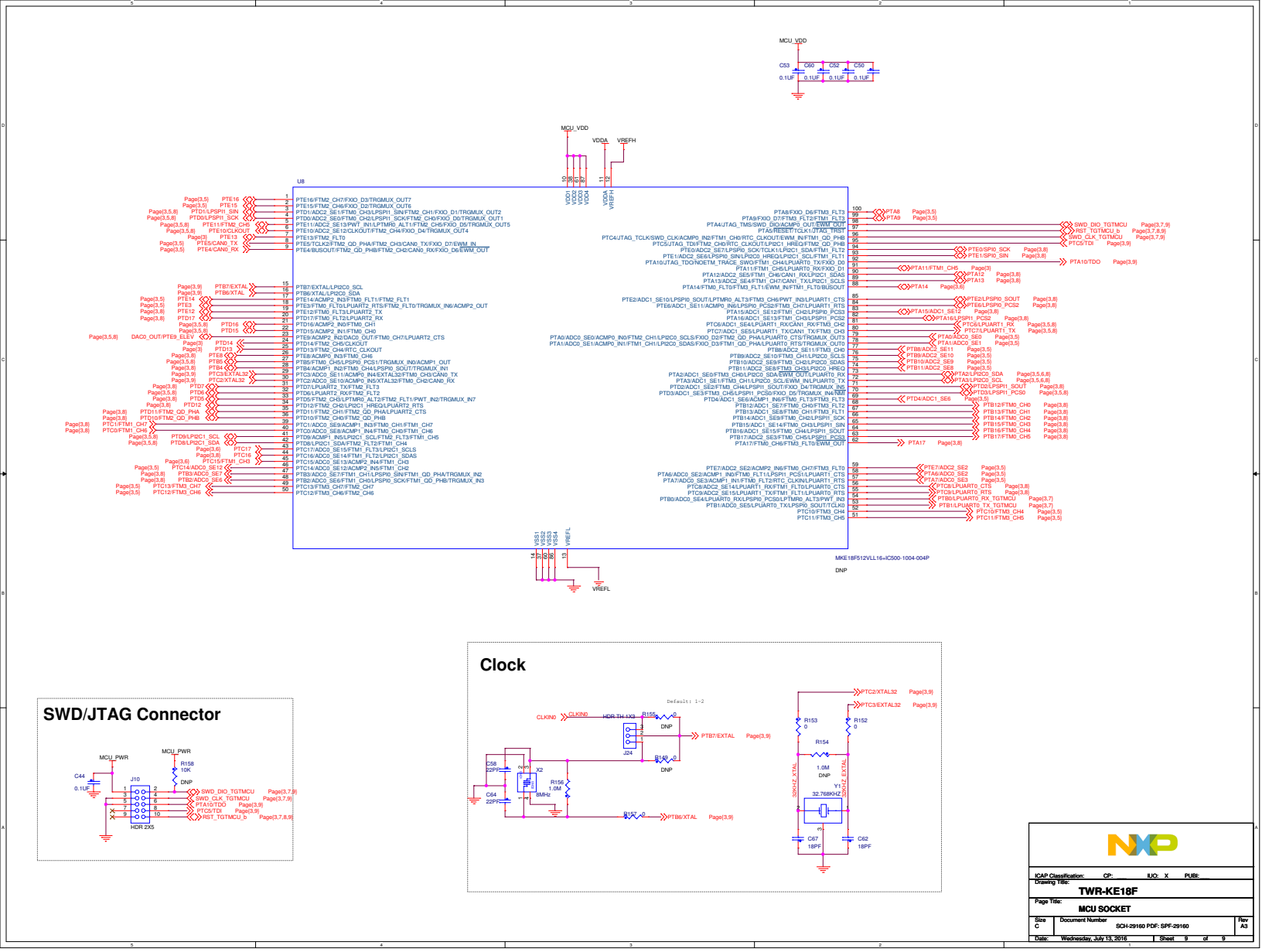

SWD/JTAG Connector

Clock

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