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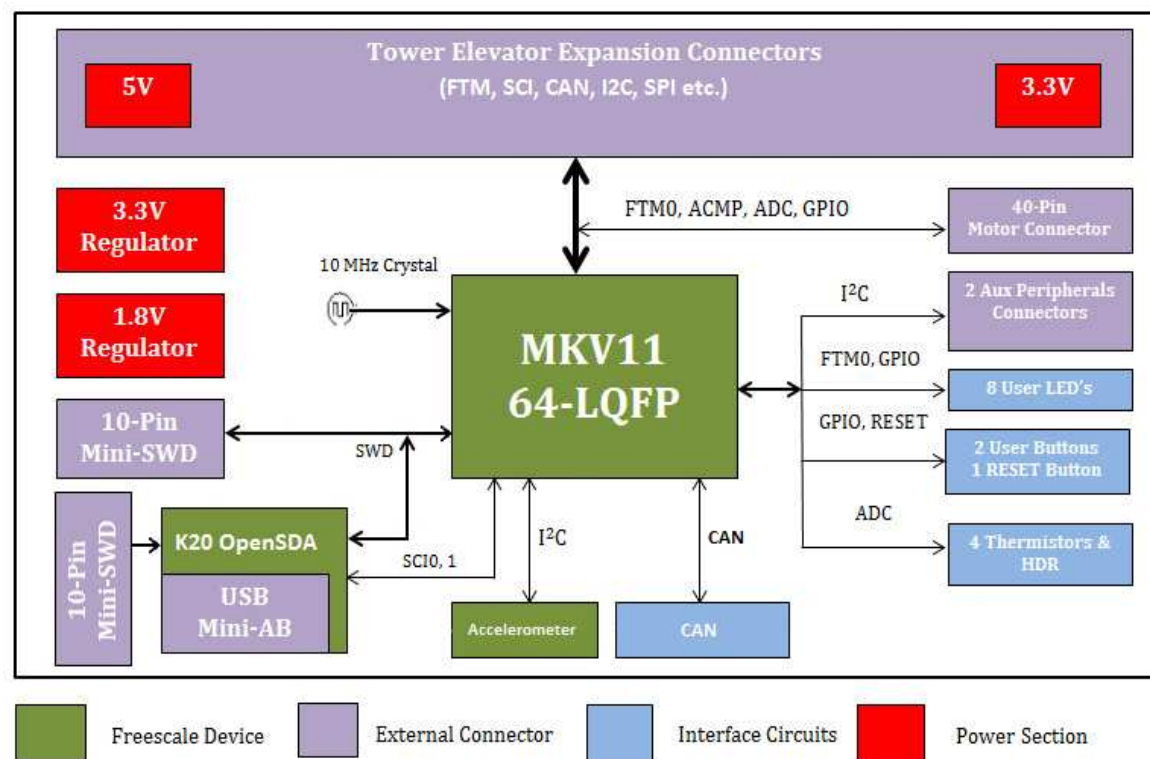
Revisions

Rev	Description	Date	Approved
X1	Initial	26-Nov-2014	Pavel
X2	Review Feedback updated	04-Dec-2014	Pavel
X3	USB Mini-B changed to USB Micro-AB. J21, J22 changed to TH component. Motor Connector (J15) footprint changed from "con2x20_2p54_hle_be" to "con2x20_2p54_hle_be_nsp"	08-Dec-2014	Pavel
X4	VBAT in U7 is changed to NC	11-Dec-2014	Pavel
X5	Accelerometer "MMA84151Q" into Accelerometer & Magnetometer "FXOS8700CQ"	16-Dec-2014	Pavel
A	A085 Release	20-Dec-2014	Pavel
B	A085 Release; with Open SDA Power Changes	05-Jan-2015	Pavel
B1	A085 Release	13-Jan-2015	Pavel
C	New Open SDA, CAN interface and some other improvements	10-Apr-2015	M. Hr. P. Su.

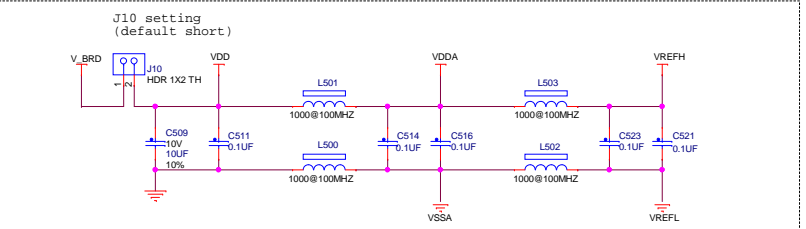
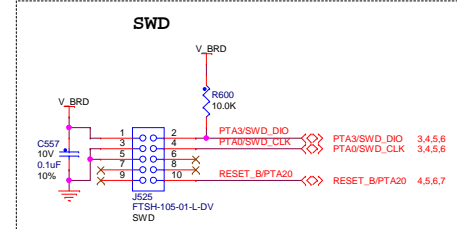
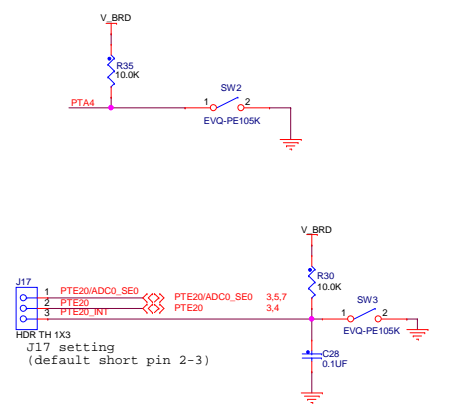
TWR-KV11Z75M

		Microcontroller Product Group 6501 William Cannon Drive West Austin, TX 78735-6508	
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Designer: Mankandan M		Drawing Title: TWR-KV11Z75M	
Drawn by: Mankandan M		Page Title: Table of Contents, Revisions	
Approved: Pavel Sustak Martin Hroczek	Size: C	Document Number: SCH-28647 PDF: SPF-28647	Rev: C
Date: Thursday, June 11, 2015		Sheet 1 of 8	

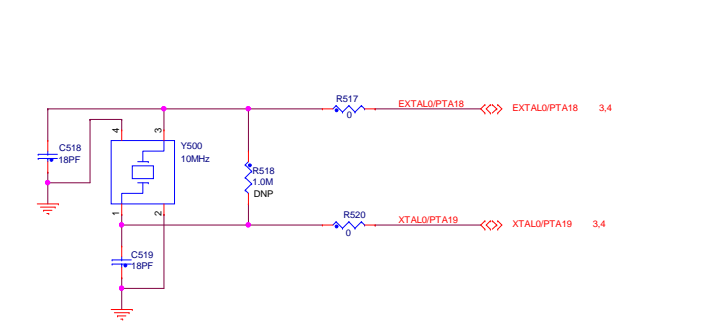
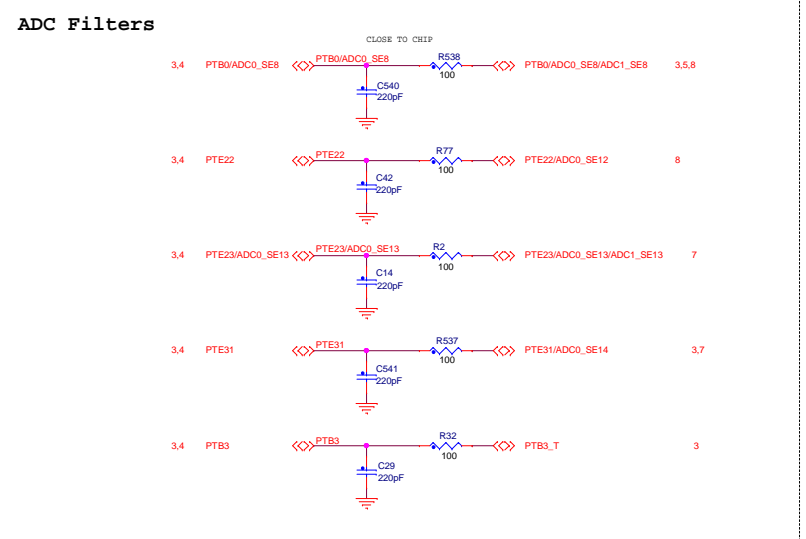
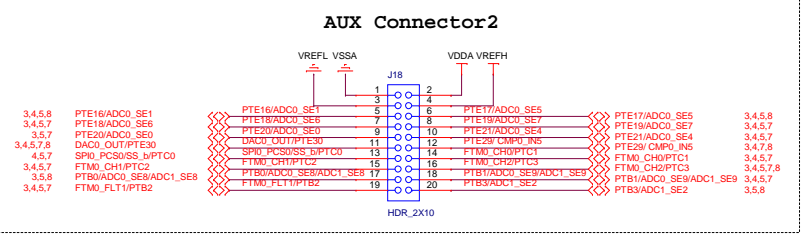
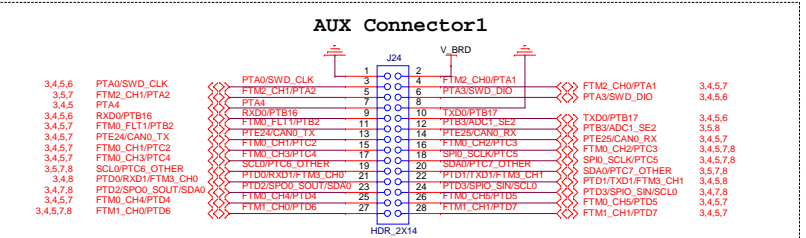
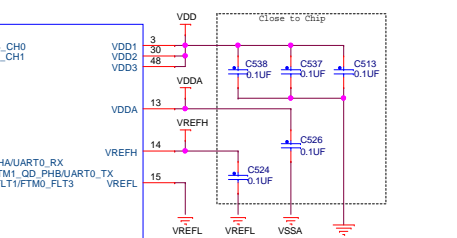
Block Diagram



MKV11Z128VLH7 Controller



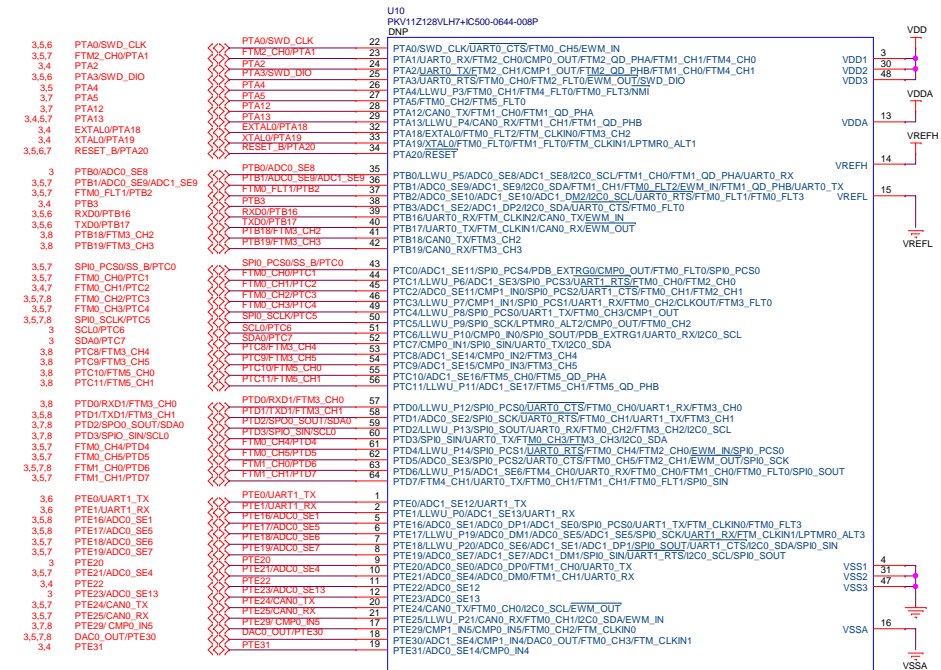
Pin	Signal	Pin	Signal	Pin	Signal
3.4,5.6	PTA0/SWD_CLK	22	PTA0/SWD_CLK/UART0_CTS/FTM0_CH5/EWM_IN	3	VDD1
3.4,5.7	FTM2_CH0/PTA1	23	PTA1/UART0_RX/FTM2_CH0/CMPO_OUT/FTM2_QD_PHA/FTM1_CH1/FTM4_CH0	30	VDD2
3.4,5.6	PTA3/SWD_DIO	24	PTA2	48	VDD3
3.4,5	PTA4	25	PTA3/UART0_RTS/FTM0_CH0/FTM2_FLT0/EWM_OUT/SWD_DIO	13	VDDA
4.7	PTA5	26	PTA4/LLWU_P3/FTM0_CH1/FTM4_FLT0/FTM3_NMI	14	VREFH
4.7	PTA12	27	PTA5/FTM0_CH2/FTM5_FLT0	15	VREFL
3.4,5.7	PTA13	28	PTA12/CAN0_TX/FTM1_CH0/FTM1_QD_PHA	16	VREFL
3.4	EXTAL0/PTA18	29	PTA13/LLWU_P4/CAN0_RX/FTM1_CH1/FTM1_QD_PHB	17	VSSA
3.4	XTAL0/PTA19	32	PTA18/EXTAL0/FTM0_FLT2/FTM_CLKIN0/FTM5_CH2	18	VSSA
4.5,6,7	RESET_B/PTA20	33	PTA19/XTAL0/FTM0_FLT0/FTM1_FLT0/FTM_CLKIN1/LPTMR0_ALT1	19	VSSA
3.4	PTB0/ADC0_SE8	34	PTA20/RESET	20	VSSA
3.4,5.7	PTB1/ADC0_SE9/ADC1_SE9	35	PTB0/LLWU_P5/ADC0_SE8/ADC1_SE8/ADC2_SCL/FTM1_CH0/FTM1_QD_PHA/UART0_RX	21	VSSA
3.4,5.7	FTM0_FLT1/PTB2	36	PTB1/ADC0_SE9/ADC1_SE9/ADC2_SDA/FTM1_CH1/FTM0_FLT2/EWM_IN/FTM1_QD_PHB/UART0_TX	22	VSSA
3.4	PTB3	37	PTB2/ADC0_SE10/ADC1_SE10/ADC1_DM2/ADC2_SCL/UART0_RTS/FTM0_FLT1/FTM0_FLT3	23	VSSA
3.4,5.6	RXD0/PTB16	38	PTB3	24	VSSA
3.4,5.6	TXD0/PTB17	39	PTB3/ADC1_SE2/ADC1_DP2/ADC2_SDA/UART0_CTS/FTM0_FLT0	25	VSSA
4.8	PTB18/FTM3_CH2	40	PTB16/UART0_RX/FTM_CLKIN2/CAN0_TX/EWM_IN	26	VSSA
4.8	PTB19/FTM3_CH3	41	PTB17/UART0_TX/FTM_CLKIN1/CAN0_RX/EWM_OUT	27	VSSA
4.8	PTB19/CAN0_RX/FTM3_CH3	42	PTB18/CAN0_TX/FTM3_CH2	28	VSSA
4.5,7	SP0_PCS0/SS_B/PTC0	43	PTB19/CAN0_RX/FTM3_CH3	29	VSSA
3.4,5.7	FTM0_CH0/PTC1	44	PTC0/ADC1_SE11/SP0_PCS4/PDB_EXTRG0/CMPO_OUT/FTM0_FLT0/SP0_PCS0	30	VSSA
3.4,5.7	FTM0_CH1/PTC2	45	PTC1/LLWU_P6/ADC1_SE3/SP0_PCS3/UART1_RTS/FTM0_CH0/FTM2_CH0	31	VSSA
3.4,5.7,8	FTM0_CH2/PTC3	46	PTC2/ADC0_SE11/CMPI_IN0/SP0_PCS2/UART1_CTS/FTM0_CH1/FTM2_CH1	32	VSSA
3.4,5.7	FTM0_CH3/PTC4	47	PTC3/LLWU_P7/CMPI_IN1/SP0_PCS1/UART1_RX/FTM0_CH2/CLKOUT/FTM3_FLT0	33	VSSA
3.4,5.7,8	SP0_SCLK/PTC5	48	PTC4/LLWU_P8/SP0_PCS0/UART1_TX/FTM0_CH3/CMPI_OUT	34	VSSA
3.4	SCL0/PTC6	49	PTC5/LLWU_P9/CMPI_IN0/SP0_SOUT/PDB_EXTRG1/UART0_RX/ADC0_SCL	35	VSSA
3.4	SDA0/PTC7	50	PTC6/LLWU_P10/CMPI_IN0/SP0_SOUT/PDB_EXTRG1/UART0_RX/ADC0_SCL	36	VSSA
4.8	PTC8/FTM3_CH4	51	PTC7/CMPI_IN1/SP0_SIN/UART0_TX/ADC0_SDA	37	VSSA
4.8	PTC9/FTM3_CH5	52	PTC8/ADC1_SE14/CMPI_IN2/FTM3_CH4	38	VSSA
4.8	PTC10/FTM3_CH0	53	PTC9/ADC1_SE15/CMPI_IN3/FTM3_CH5	39	VSSA
4.8	PTC11/FTM3_CH1	54	PTC10/ADC1_SE16/FTM5_CH0/FTM5_QD_PHA	40	VSSA
3.4,8	PTD0/RXD1/FTM3_CH0	55	PTC11/LLWU_P11/ADC1_SE17/FTM5_CH1/FTM5_QD_PHB	41	VSSA
3.4,5.8	PTD1/TXD1/FTM3_CH1	56	PTD0/LLWU_P12/SP0_PCS0/UART0_CTS/FTM0_CH0/UART1_RX/FTM3_CH0	42	VSSA
3.4,7,8	PTD2/SPO_SOUT/SDA0	57	PTD1/ADC0_SE2/SP0_SCLK/UART0_RTS/FTM0_CH1/UART1_TX/FTM3_CH1	43	VSSA
3.4,7,8	PTD3/SPO_SIN/SCLO	58	PTD2/LLWU_P13/SP0_SOUT/UART0_RX/FTM0_CH2/FTM3_CH2/ADC0_SCL	44	VSSA
3.4,7,8	FTM0_CH4/PTD4	59	PTD3/SP0_SIN/UART0_TX/FTM0_CH3/FTM3_CH3/ADC0_SDA	45	VSSA
3.4,5.7	FTM0_CH5/PTD5	60	PTD4/LLWU_P14/SP0_PCS1/UART0_RTS/FTM0_CH4/FTM2_CH0/EWM_IN/SP0_PCS0	46	VSSA
3.4,5.7,8	FTM1_CH0/PTD6	61	PTD5/ADC0_SE3/SP0_PCS2/UART0_CTS/FTM0_CH5/FTM2_CH1/EWM_OUT/SP0_SOUT	47	VSSA
3.4,5.7	FTM1_CH1/PTD7	62	PTD6/LLWU_P15/ADC1_SE6/FTM4_CH0/UART0_RX/FTM0_CH0/FTM1_CH0/FTM0_FLT0/SP0_SOUT	48	VSSA
4.6	PTE0/UART1_TX	63	PTD7/FTM0_CH1/UART0_TX/FTM0_CH1/FTM1_CH1/FTM0_FLT1/SP0_SIN	49	VSSA
4.6	PTE1/UART1_RX	64	PTE0/UART1_TX	50	VSSA
3.4,5.8	PTE16/ADC0_SE1	1	PTE1/UART1_RX	51	VSSA
3.4,5.8	PTE17/ADC0_SE5	2	PTE16/ADC0_SE1/ADC1_SE1/UART1_RX	52	VSSA
3.4,5.7	PTE18/ADC0_SE6	3	PTE17/LLWU_P16/ADC0_DP1/ADC1_SE0/SP0_PCS0/UART1_TX/FTM_CLKIN0/FTM0_FLT3	53	VSSA
3.4,5.7	PTE19/ADC0_SE7	4	PTE18/LLWU_P17/ADC0_DM1/ADC1_SE5/ADC1_SE5/UART1_RX/FTM_CLKIN1/LPTMR0_ALT3	54	VSSA
3.4	PTE20	5	PTE19/LLWU_P18/ADC0_SE8/ADC1_SE1/ADC1_DP1/SP0_SOUT/UART1_CTS/ADC0_SDA/SP0_SIN	55	VSSA
3.4,5.7	PTE21/ADC0_SE4	6	PTE19/ADC0_SE7/ADC1_SE7/ADC1_DM1/SP0_SIN/UART1_RTS/ADC0_SCL/SP0_SOUT	56	VSSA
3.4	PTE22	7	PTE20/ADC0_SE4	57	VSSA
3.4	PTE23/ADC0_SE13	8	PTE21/ADC0_SE4	58	VSSA
3.4,5.7	PTE24/CAN0_TX	9	PTE22/ADC0_SE12	59	VSSA
3.4,5.7	PTE25/CAN0_RX	10	PTE23/ADC0_SE13	60	VSSA
3.4,7,8	PTE26/CMPO_IN5	11	PTE24/CAN0_TX	61	VSSA
3.4,5.7,8	DAC0_OUT/PTF30	12	PTE25/LLWU_P21/CAN0_RX/FTM0_CH1/ADC0_SDA/EWM_IN	62	VSSA
3.4	PTF31	13	PTE26/CMPI_IN5/CMPI_IN5/FTM0_CH0/FTM_CLKIN0	63	VSSA
		14	PTE30/ADC1_SE4/CMPI_IN4/DAC0_OUT/FTM0_CH3/FTM_CLKIN1	64	VSSA
		15	PTE31/ADC0_SE14/CMPO_IN4	65	VSSA



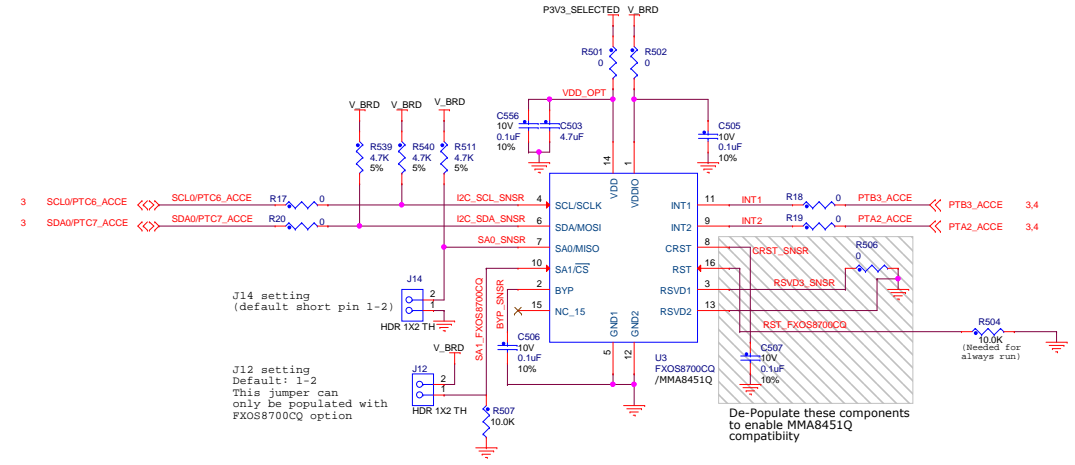
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MMA8451Q ACCELEROMETER / FXOS8700CQ COMBO ACC + MAGNETOMETER



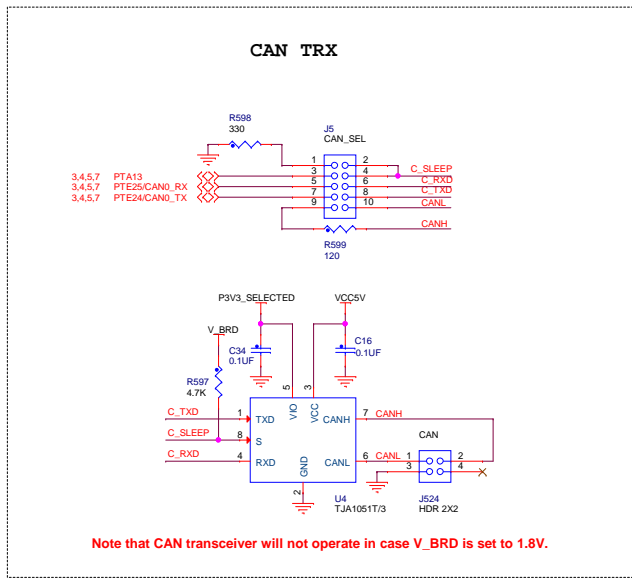
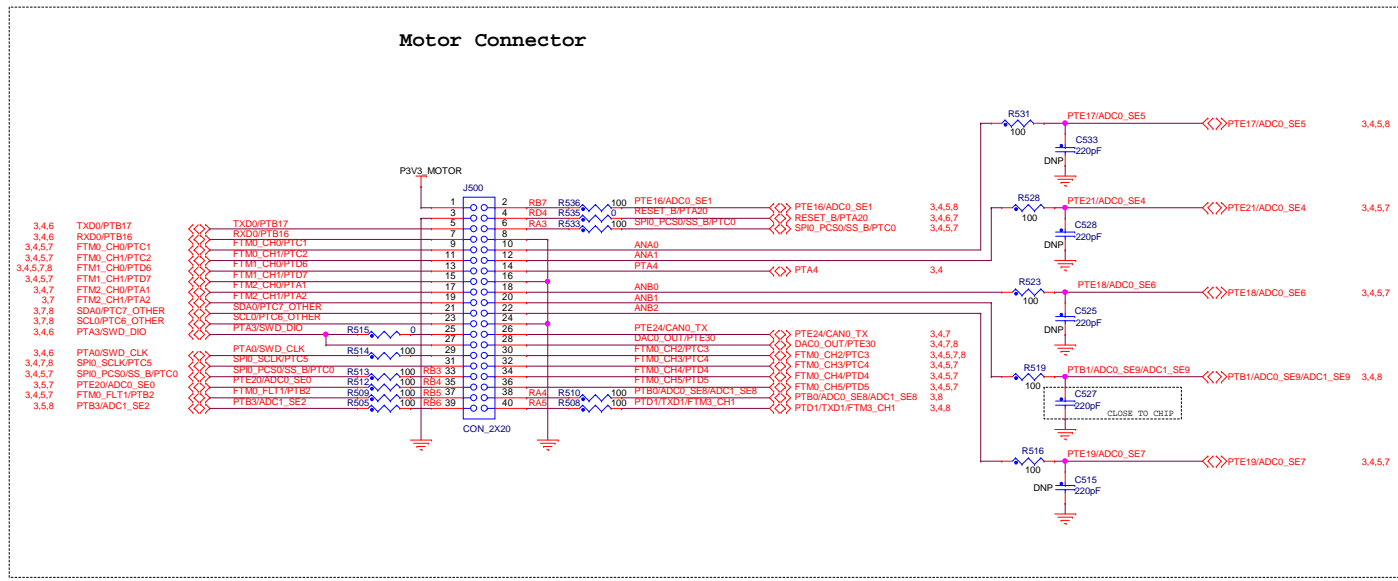
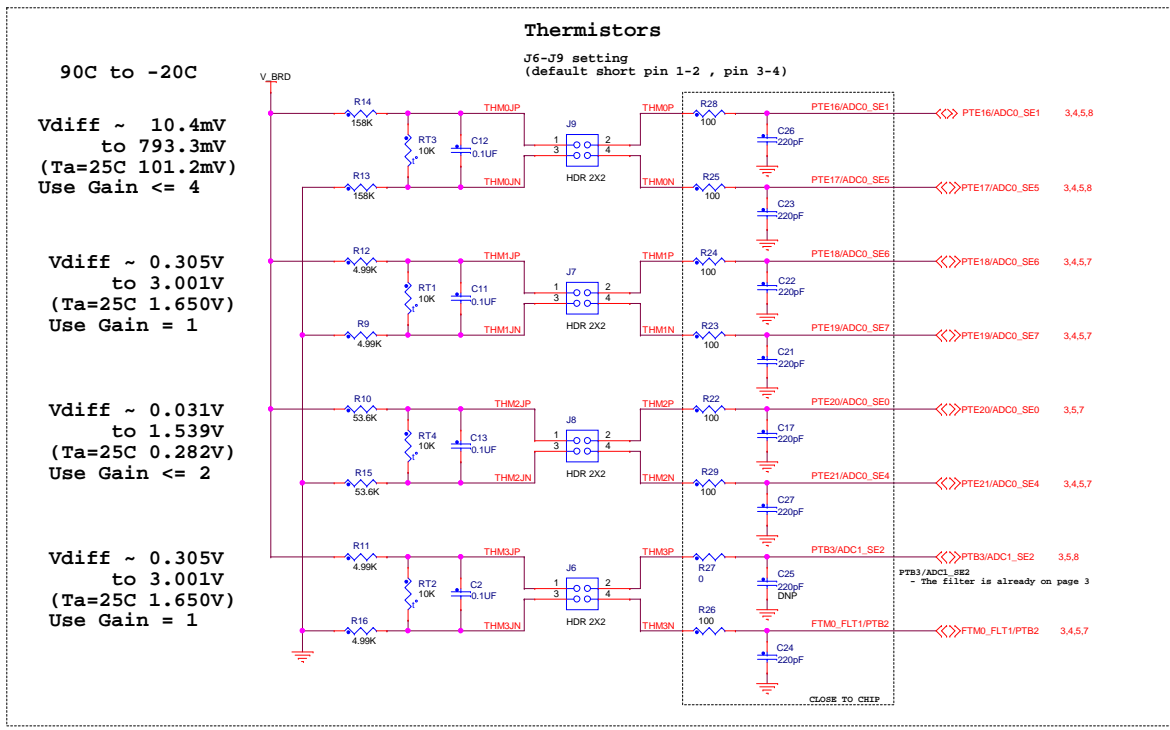
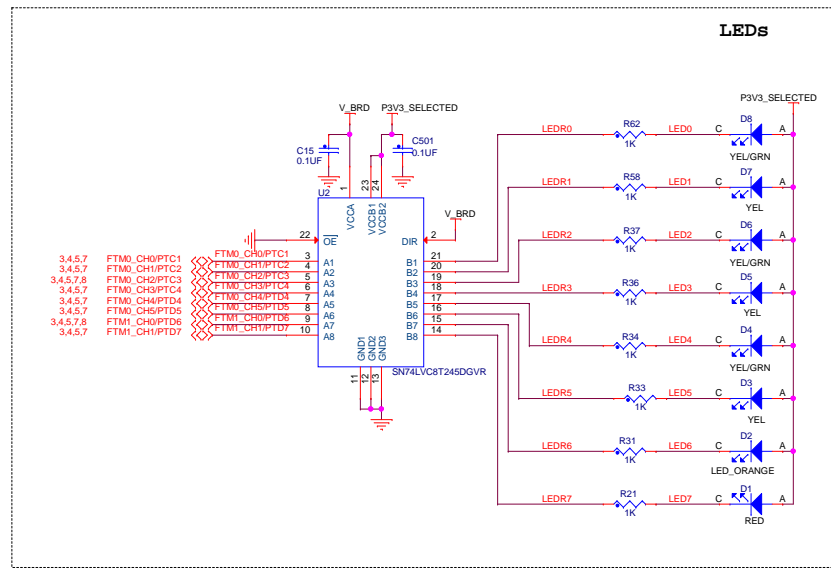
I2C address is 0x1C using default configuration SA0->0, SA1->1

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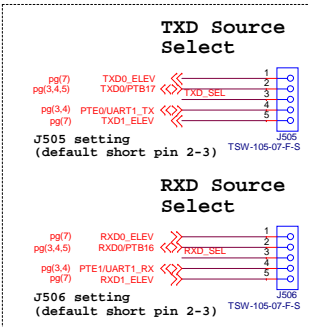
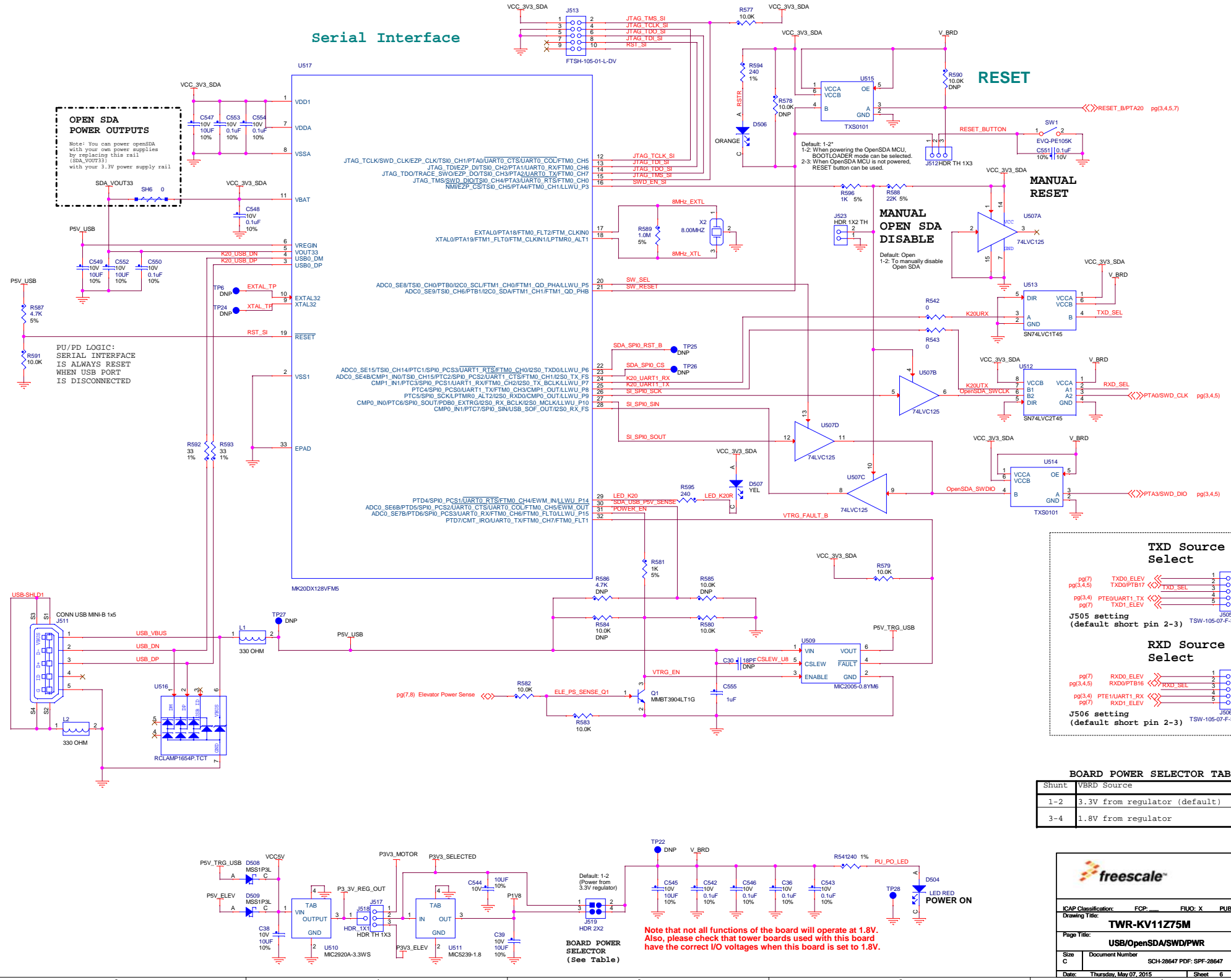
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Serial Interface

OPEN SDA POWER OUTPUTS

Note: You can power opensDA with your own power supplies by replacing this rail (SDA_VOUT33) with your 3.3V power supply rail



BOARD POWER SELECTOR TABLE

Shunt	VBRD Source
1-2	3.3V from regulator (default)
3-4	1.8V from regulator

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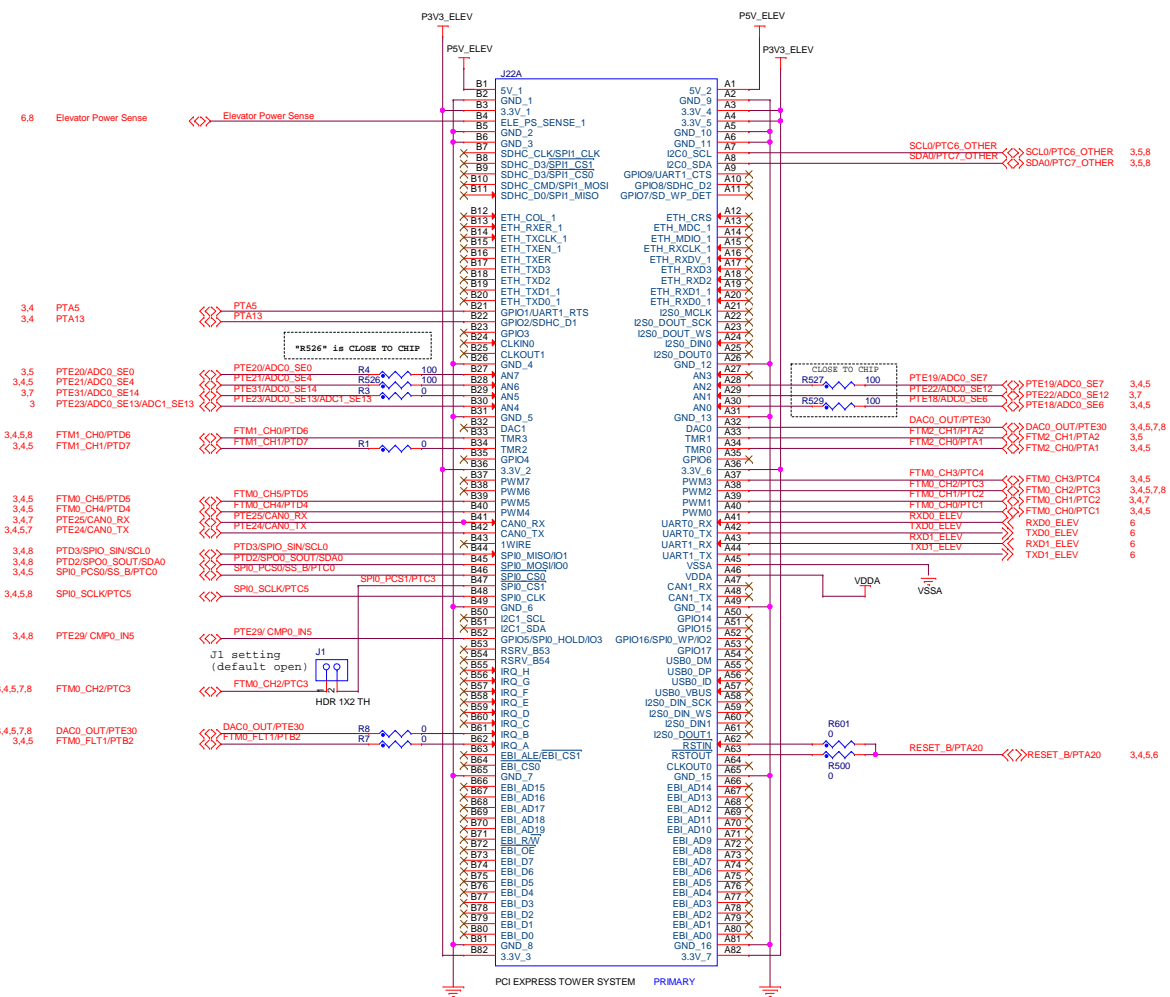
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Note that not all functions of the board will operate at 1.8V. Also, please check that tower boards used with this board have the correct I/O voltages when this board is set to 1.8V.



6.8 Elevator Power Sense

3.4 PTA5
3.4 PTA13

3.5 PTE20/ADC0_SE0
3.4.5 PTE21/ADC0_SE4
3.7 PTE31/ADC0_SE14
3 PTE23/ADC0_SE13/ADC1_SE13

3.4.5.8 FTM1_CH0/PTD6
3.4.5 FTM1_CH1/PTD7

3.4.5 FTM0_CH5/PTD5
3.4.5 FTM0_CH4/PTD4
3.4.7 PTE25/CAN0_RX
3.4.5.7 PTE24/CAN0_TX

3.4.8 PTD3/SPI0_SIN/SCL0
3.4.8 PTD2/SPI0_SOUT/SDA0
3.4.5 SPI0_PC0/SS_B/PTC0

3.4.5.8 SPI0_SCLK/PTC5

3.4.8 PTE29/CMP0_IN5

3.4.5.7.8 FTM0_CH2/PTC3

3.4.5.7.8 DAC0_OUT/PTC30
3.4.5 FTM0_FLT1/PTB2

SCL0/PTC6_OTHER
SDA0/PTC7_OTHER

PTE19/ADC0_SE7
PTE22/ADC0_SE12
PTE18/ADC0_SE6

DAC0_OUT/PTC30
FTM2_CH1/PTA2
FTM2_CH0/PTA1

FTM0_CH3/PTC4
FTM0_CH2/PTC3
FTM0_CH1/PTC2
FTM0_CH0/PTC1

RXDD0_ELEV
TXDD0_ELEV
RXDD1_ELEV
TXDD1_ELEV

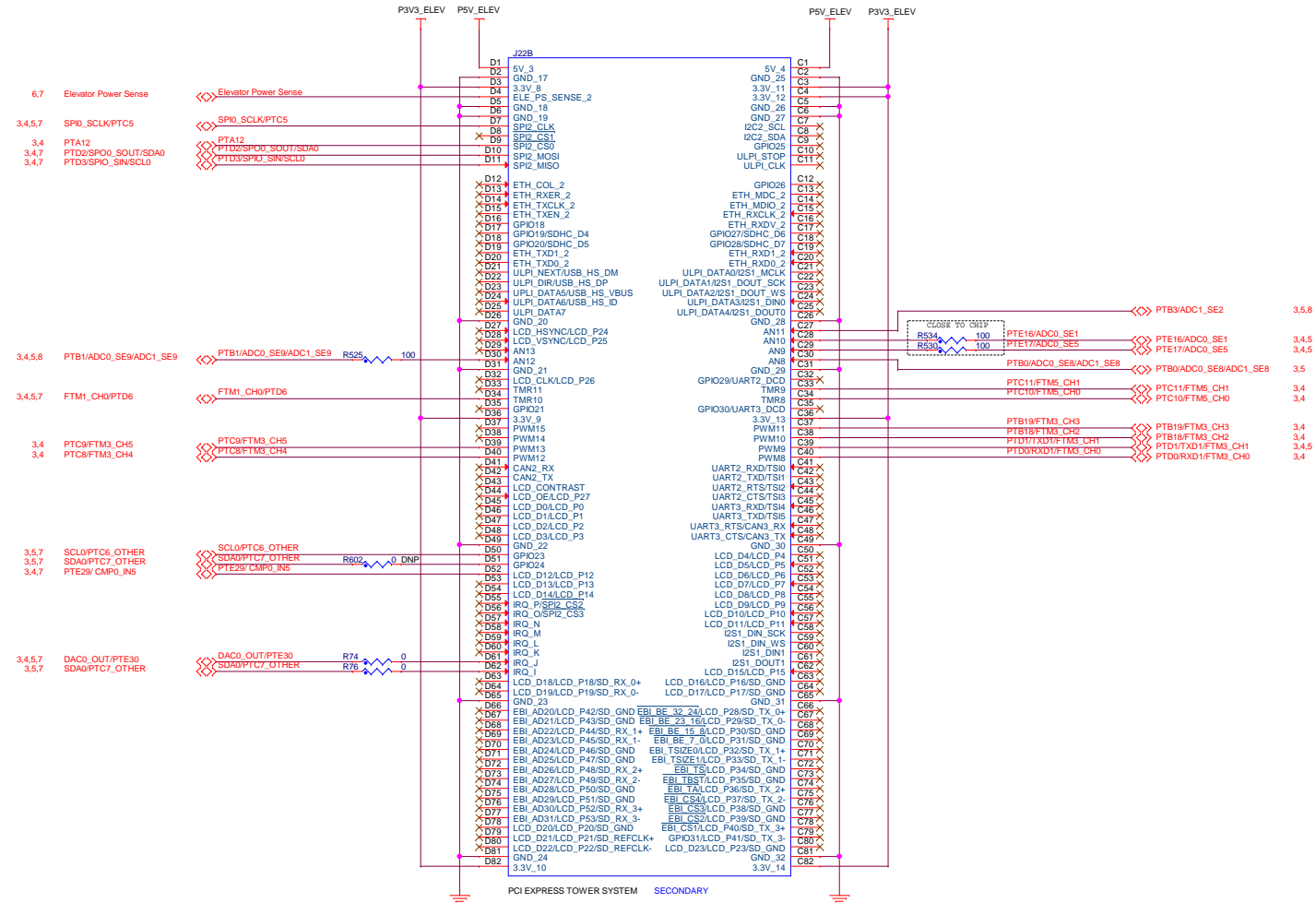
RESET_B/PTA20

RESET_B/PTA20

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