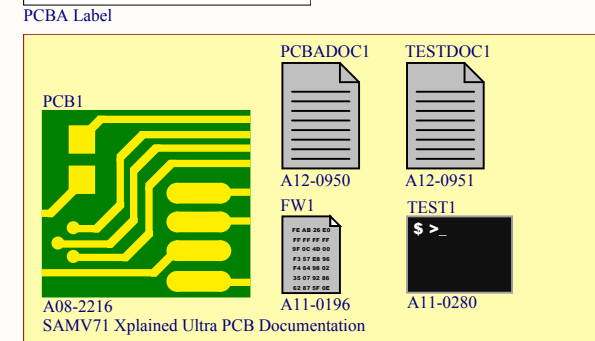
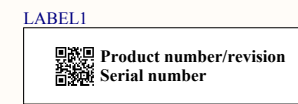
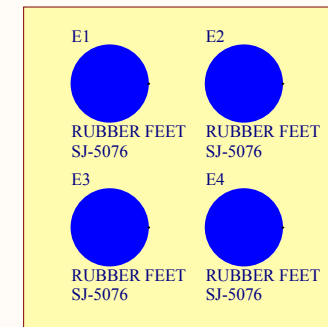
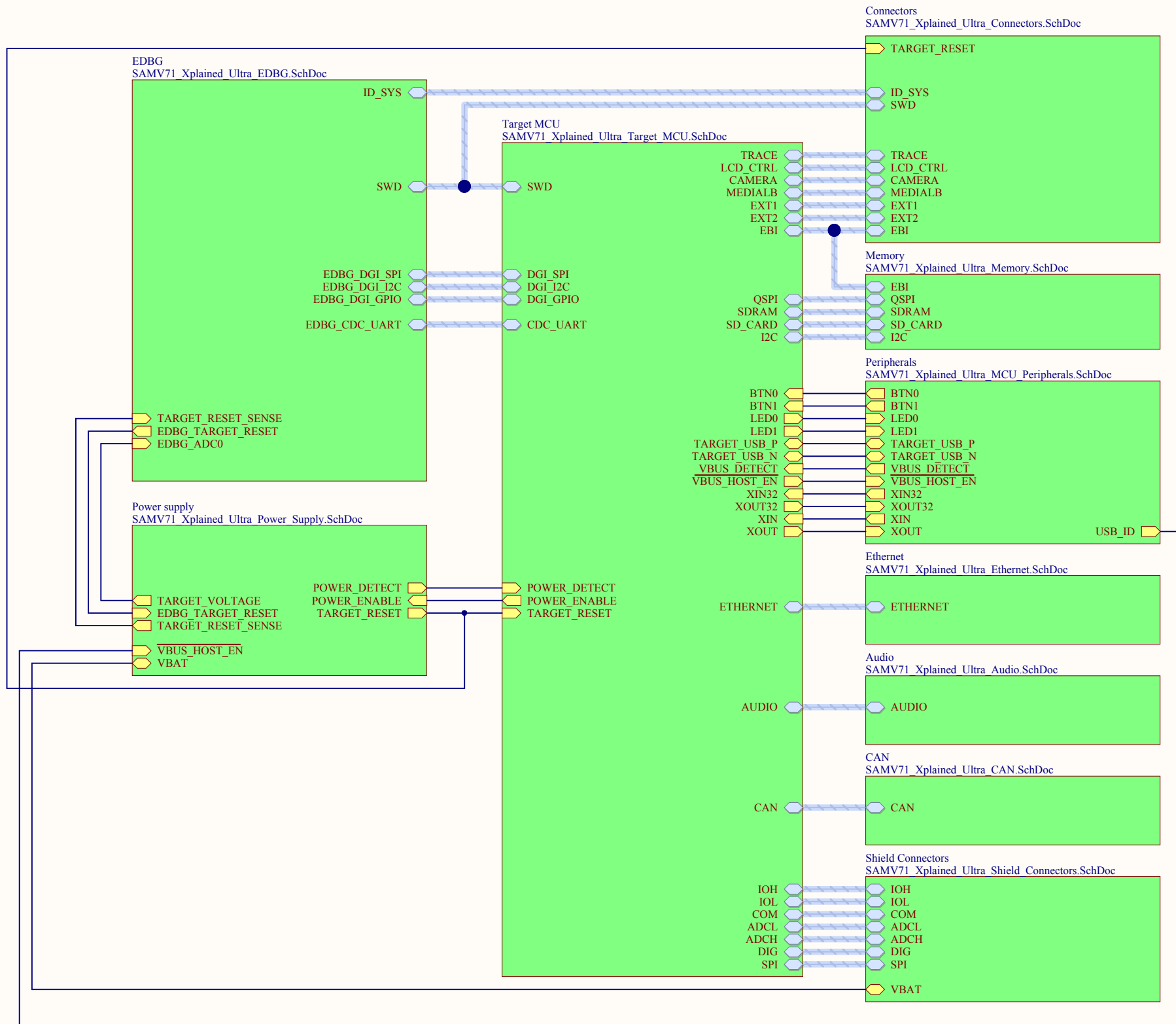

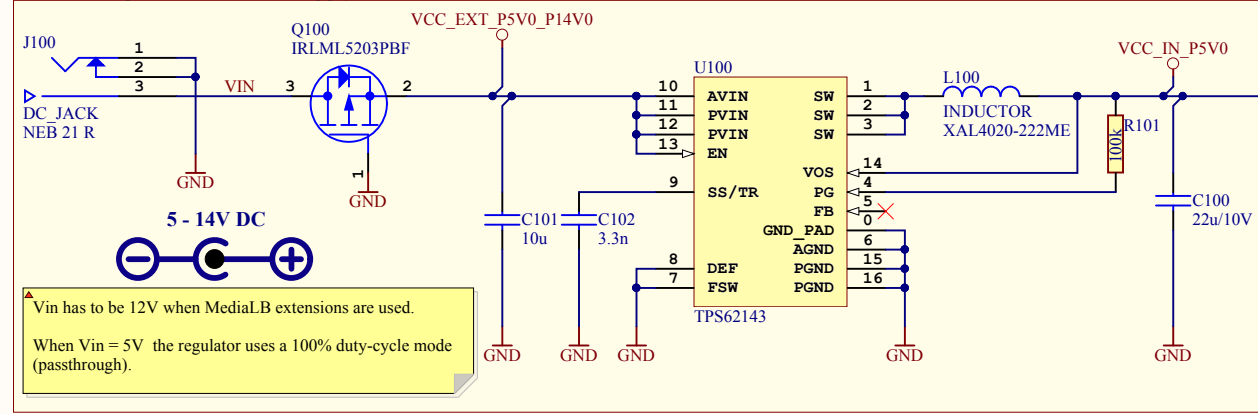


# SAM V71 Xplained ULTRA



ATMEL Norway	*		 Enabling Unlimited Possibilities
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	16.03.2015	15:01:48	PAGE: 1 of 13
Document number:	A09-2407		Revision: 3
TITLE: Top Level Schematics			
SAMV71_Xplained_Ultra_TopLevel.SchDoc			

### 5V to 14V input, 5V out Power Supply

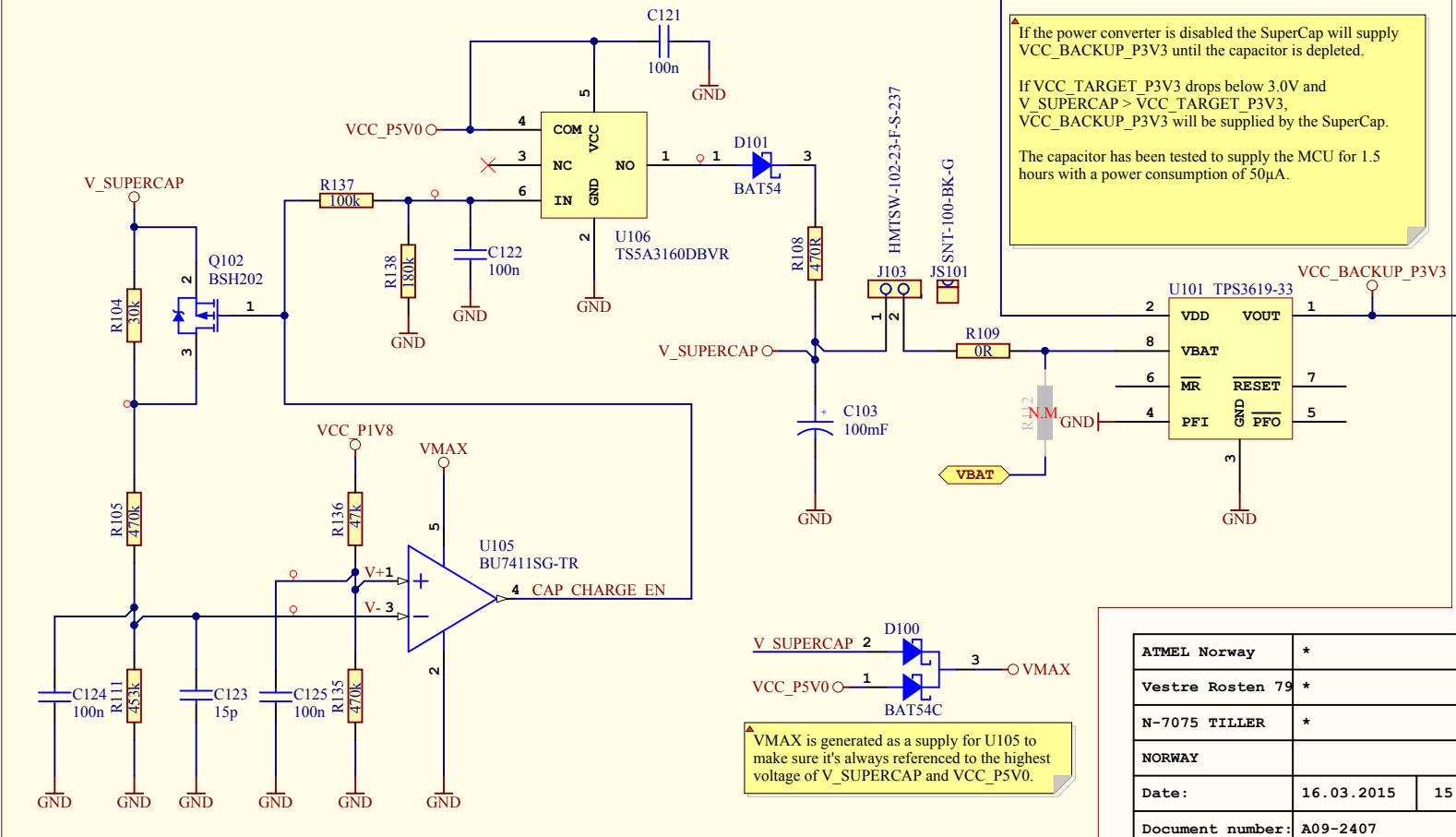


Vin has to be 12V when MediaLB extensions are used.  
When Vin = 5V the regulator uses a 100% duty-cycle mode (passthrough).

**Power inputs to SAM V71 Xplained Ultra:**  
**VCC\_EXT\_P5V0\_P14V0:** 2.1mm power jack with positive center. This voltage is used to generate VCC\_EXT\_P5V0, the regulator supports 5V to 17V input voltage. If MediaLB is not used the input voltage can be 17V.  
**VCC\_EXT\_P5V0:** This power input can be used to power the whole board and it has a higher priority as the USB power inputs. Connect a power supply if a target MCU with USB host is present and VCC\_EXT\_P5V0\_P17V0 is not used. 4.3V to 5.5V is possible but for USB host operation and in case on-board devices use this voltage it should be 5V +2%.  
**VCC\_EDBG\_USB\_P5V0:** EDBG USB power input. This supply is used when VCC\_EXT\_P5V0 is not present.  
**VCC\_TARGET\_USB\_P5V0:** Target MCU USB power input. It is used to power the whole board when no other 5V power supply is present.  
**Other voltages:**  
**VCC\_P5V0:** This supply is connected to either VCC\_EXT\_P5V0, VCC\_EDBG\_USB\_P5V0 or VCC\_TARGET\_USB\_P5V0, based on the availability and priority of these supplies.  
**VCC\_P3V3:** Regulated 3.3V from VCC\_P5V0  
**VCC\_P2V0:** Regulated 2.0V from VCC\_P5V0  
**VCC\_P1V8:** Regulated 1.8V from VCC\_P5V0  
**VCC\_P1V2:** Regulated 1.2V from VCC\_P5V0  
**VCC\_TARGET\_P3V3:** Target supply voltage (target MCU, peripherals, connectors and SuperCap charge)  
**VCC\_BACKUP\_P3V3:** Powers target MCU, can be supplied from either VCC\_TARGET\_P3V3 or V\_SUPERCAP.  
**V\_SUPERCAP:** The SuperCap is charged to 3.52V from VCC\_P5V0 when that voltage is present. V\_SUPERCAP is used to supply target MCU when the voltage regulator for VCC\_P3V3 is turned off, intended for sleep mode and currents below 100µA.

U105 compares V\_SUPERCAP to a known reference, when V\_SUPERCAP is low Q101 and Q102 will open causing V\_SUPERCAP to charge to:  
 $V_{cap} (max) = (U105\_V- * (R111 + R105)) / R111 = 3.52V$   
 At Vcap (max) Q101 and Q102 will close and R104 is no longer short circuited by Q102.  
 Vcap is now given by the following formula:  
 $V_{cap} = (U105\_V- * (R111 + R105 + R104)) / R111 = 3.40V$   
 Q102 and R104 implements a charge hysteresis to prevent oscillation when the capacitor is fully charged.

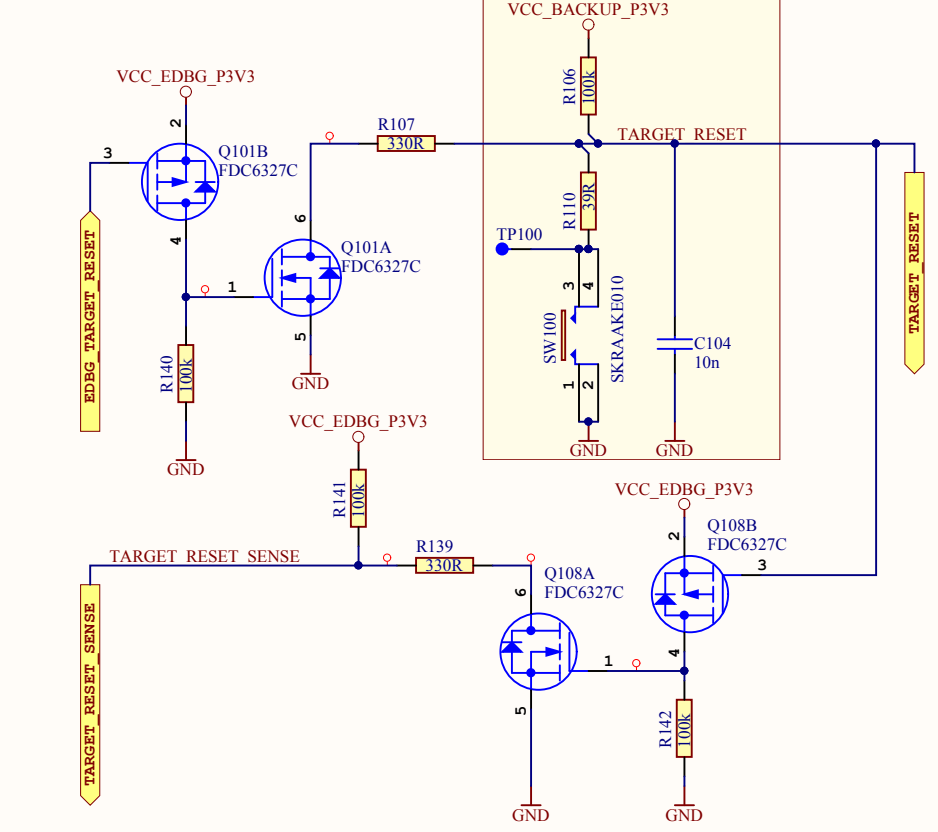
### Electric Double-Layer Capacitor (Supercap) for backup voltage



If the power converter is disabled the SuperCap will supply VCC\_BACKUP\_P3V3 until the capacitor is depleted.  
 If VCC\_TARGET\_P3V3 drops below 3.0V and V\_SUPERCAP > VCC\_TARGET\_P3V3, VCC\_BACKUP\_P3V3 will be supplied by the SuperCap.  
 The capacitor has been tested to supply the MCU for 1.5 hours with a power consumption of 50µA.

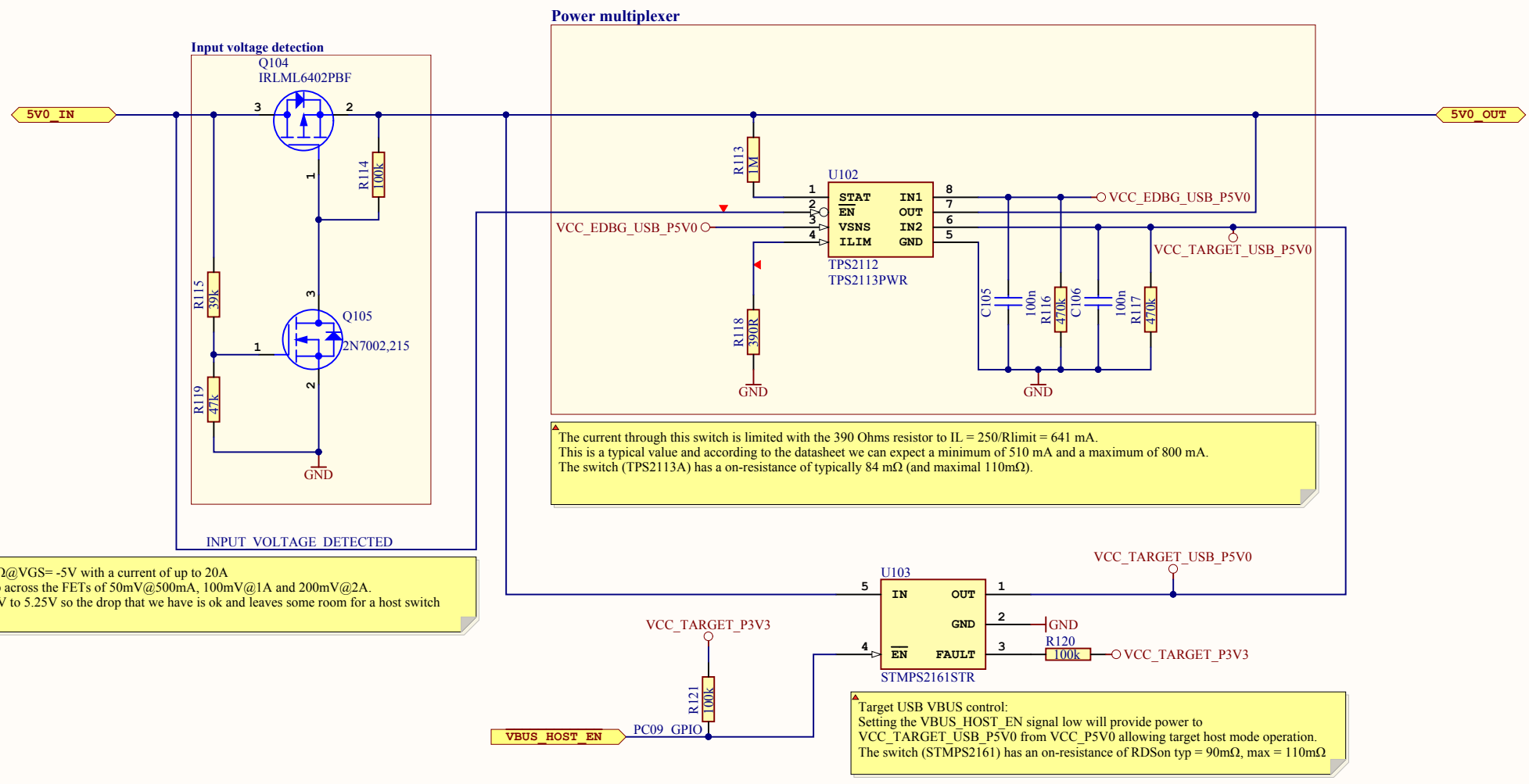
VMAX is generated as a supply for U105 to make sure it's always referenced to the highest voltage of V\_SUPERCAP and VCC\_P5V0.

### RESET button with current limit and noise filter



For current measurements of the target MCU remove this jumper and connect a measurement instrument.


ATMEL Norway	*			
Vestre Rosten 79	*			
N-7075 TILLER	*			
NORWAY				
Date:	16.03.2015	15:01:48	PAGE: 2 of 13	
Document number:	A09-2407		Revision	3
TITLE: Power supply				
SAMV71_Xplained_Ultra_Power_Supply_SchDoc				

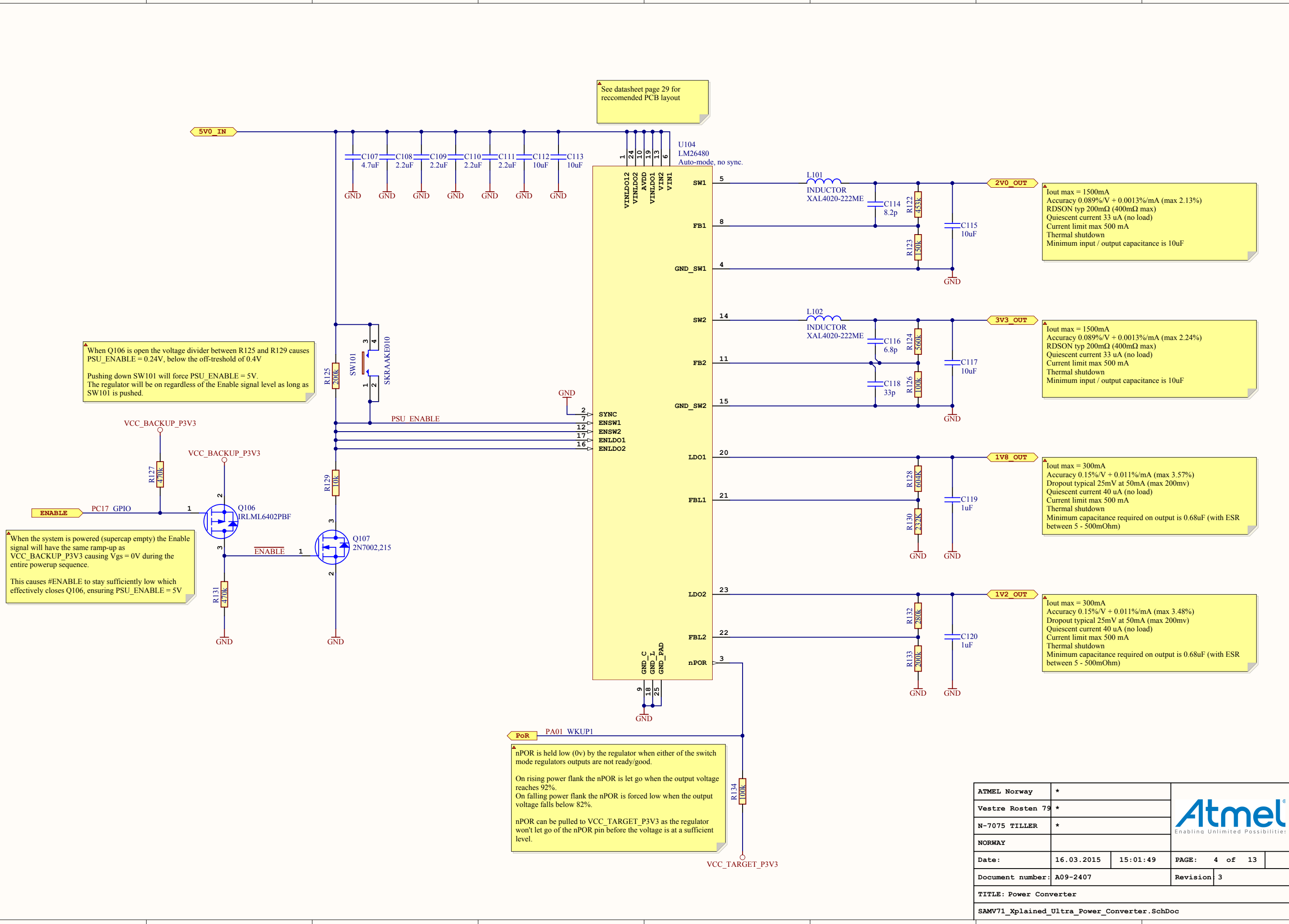


Each FET in the power path has a  $R_{DSon}$  of  $<50m\Omega$  @  $V_{GS} = -5V$  with a current of up to 20A. That means we can expect a maximum voltage drop across the FETs of  $50mV$  @  $500mA$ ,  $100mV$  @  $1A$  and  $200mV$  @  $2A$ . For USB host mode we need a voltage between 4.4V to 5.25V so the drop that we have is ok and leaves some room for a host switch on-resistance.

The current through this switch is limited with the 390 Ohms resistor to  $I_L = 250/R_{limit} = 641$  mA. This is a typical value and according to the datasheet we can expect a minimum of 510 mA and a maximum of 800 mA. The switch (TPS2113A) has a on-resistance of typically 84 mΩ (and maximal 110mΩ).

Target USB VBUS control:  
Setting the VBUS\_HOST\_EN signal low will provide power to VCC\_TARGET\_USB\_P5V0 from VCC\_P5V0 allowing target host mode operation. The switch (STMP2161) has an on-resistance of  $R_{DSon}$  typ = 90mΩ, max = 110mΩ

ATMEL Norway	*	 Enabling Unlimited Possibilities	
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	16.03.2015	15:01:48	PAGE: 3 of 13
Document number:	A09-2407		Revision 3
TITLE: Power Multiplexer			
SAMV71_Xplained_Ultra_Power_Multiplexer.SchDoc			



See datasheet page 29 for recommended PCB layout

When Q106 is open the voltage divider between R125 and R129 causes PSU\_ENABLE = 0.24V, below the off-threshold of 0.4V  
 Pushing down SW101 will force PSU\_ENABLE = 5V.  
 The regulator will be on regardless of the Enable signal level as long as SW101 is pushed.

When the system is powered (supercap empty) the Enable signal will have the same ramp-up as VCC\_BACKUP\_P3V3 causing Vgs = 0V during the entire powerup sequence.  
 This causes #ENABLE to stay sufficiently low which effectively closes Q106, ensuring PSU\_ENABLE = 5V

nPOR is held low (0v) by the regulator when either of the switch mode regulators outputs are not ready/good.  
 On rising power flank the nPOR is let go when the output voltage reaches 92%.  
 On falling power flank the nPOR is forced low when the output voltage falls below 82%.  
 nPOR can be pulled to VCC\_TARGET\_P3V3 as the regulator won't let go of the nPOR pin before the voltage is at a sufficient level.

Iout max = 1500mA  
 Accuracy 0.089%/V + 0.0013%/mA (max 2.13%)  
 RDS(on) typ 200mΩ (400mΩ max)  
 Quiescent current 33 uA (no load)  
 Current limit max 500 mA  
 Thermal shutdown  
 Minimum input / output capacitance is 10uF

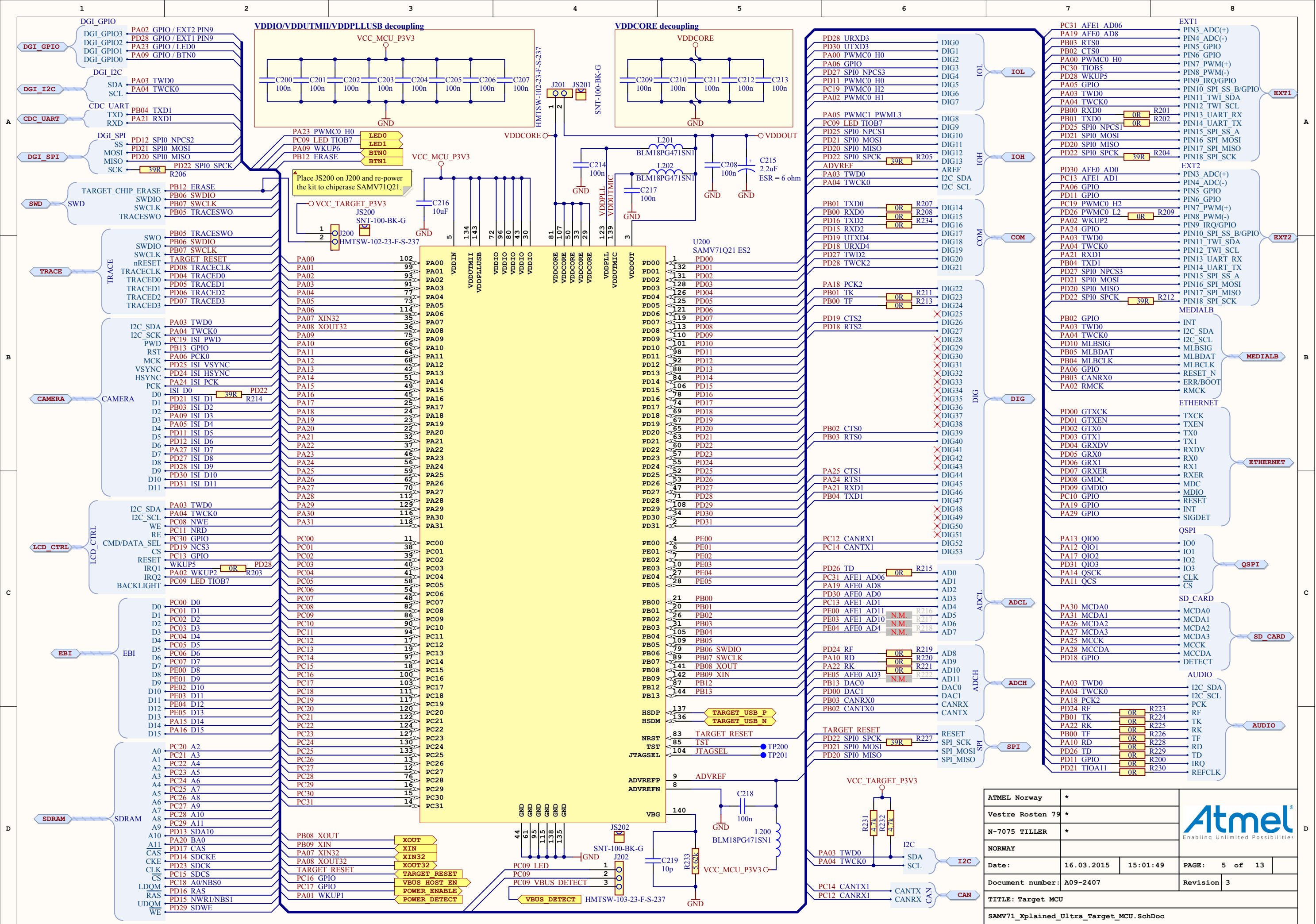
Iout max = 1500mA  
 Accuracy 0.089%/V + 0.0013%/mA (max 2.24%)  
 RDS(on) typ 200mΩ (400mΩ max)  
 Quiescent current 33 uA (no load)  
 Current limit max 500 mA  
 Thermal shutdown  
 Minimum input / output capacitance is 10uF

Iout max = 300mA  
 Accuracy 0.15%/V + 0.011%/mA (max 3.57%)  
 Dropout typical 25mV at 50mA (max 200mv)  
 Quiescent current 40 uA (no load)  
 Current limit max 500 mA  
 Thermal shutdown  
 Minimum capacitance required on output is 0.68uF (with ESR between 5 - 500mOhm)

Iout max = 300mA  
 Accuracy 0.15%/V + 0.011%/mA (max 3.48%)  
 Dropout typical 25mV at 50mA (max 200mv)  
 Quiescent current 40 uA (no load)  
 Current limit max 500 mA  
 Thermal shutdown  
 Minimum capacitance required on output is 0.68uF (with ESR between 5 - 500mOhm)

ATMEL Norway	*			 Enabling Unlimited Possibilities
Vestre Rosten 79	*			
N-7075 TILLER	*			
NORWAY				
Date:	16.03.2015	15:01:49	PAGE:	4 of 13
Document number:	A09-2407		Revision:	3
TITLE: Power Converter				
SAMV71_Xplained_Ultra_Power_Converter.SchDoc				

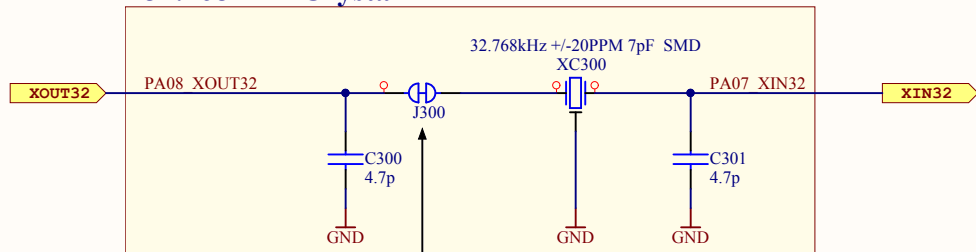




ATMEL Norway	*			
Vestre Rosten 79	*			
N-7075 TILLER	*			
NORWAY				
Date:	16.03.2015	15:01:49	PAGE: 5 of 13	
Document number:	A09-2407		Revision: 3	
TITLE: Target MCU				
SAMV71_Xplained_Ultra_Target_MCU.SchDoc				



### 32.768 kHz Crystal



These straps with SMD pads can be used to place a resistor in the XOUT signal in order to measure the oscillator allowance. By default these straps are closed and nothing is mounted on the pads.

Crystal datasheet:  
 Ccrystal = 7pF  
 max ESR = 60kOhm  
 Accuracy +20ppm

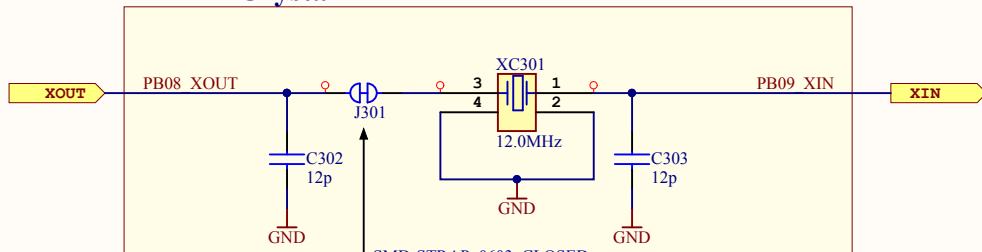
SAM V71 datasheet:  
 Cpara = 0.5pF (Typical)  
 max ESR = 100kOhm  
 PCB capacitance: Cpcb = 1pF (estimated)

Estimated load  
 $C = 2 (C_{crystal} - C_{para} - C_{pcb})$   
 $C = 2 (7pF - 0.5pF - 1pF)$   
 $C = 11pF$

Selected in design  
 $C = 10pF$

Verification showed: 4.7pF  
 Accuracy: 5.2 ppm  
 Startup time: 400 ms to reach full swing with a 9.5pF probe connected to the crystal.  
 Safety factor: Above 5.5

### 12 MHz Crystal



These straps with SMD pads can be used to place a resistor in the XOUT signal in order to measure the oscillator allowance. By default these straps are closed and nothing is mounted on the pads.

Crystal datasheet:  
 Ccrystal = 20pF  
 max ESR = 80 Ohm  
 Accuracy +20ppm

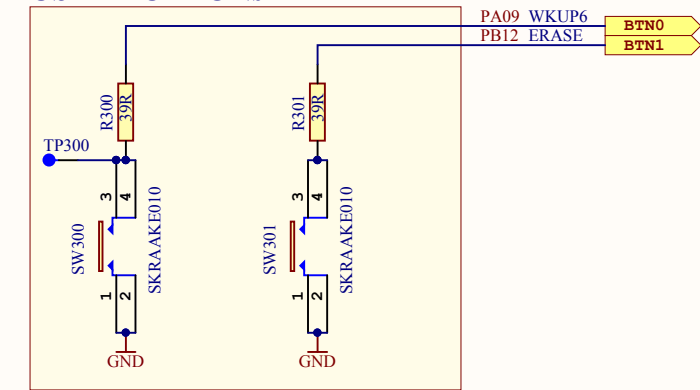
SAM V71 datasheet:  
 CL = 9.0pF (typical)  
 Maximum load 17.5pF  
 Maximum ESR = 100 Ohm  
 Estimated Cpcb = 1pF

$C = 2 (C_{crystal} - CL - C_{pcb})$   
 $C = 2 (20pF - 9pF - 1pF)$   
 $C = 20pF$

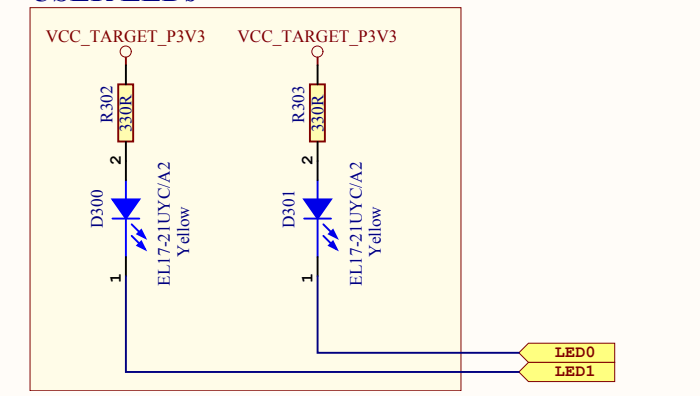
Selected in design  
 $C = 18pF$

Verification showed: 12.0pF  
 Accuracy 5 ppm  
 Startup: full swing after 850 μs (first clock after 451 μs)  
 Safety factor: Above 5.5

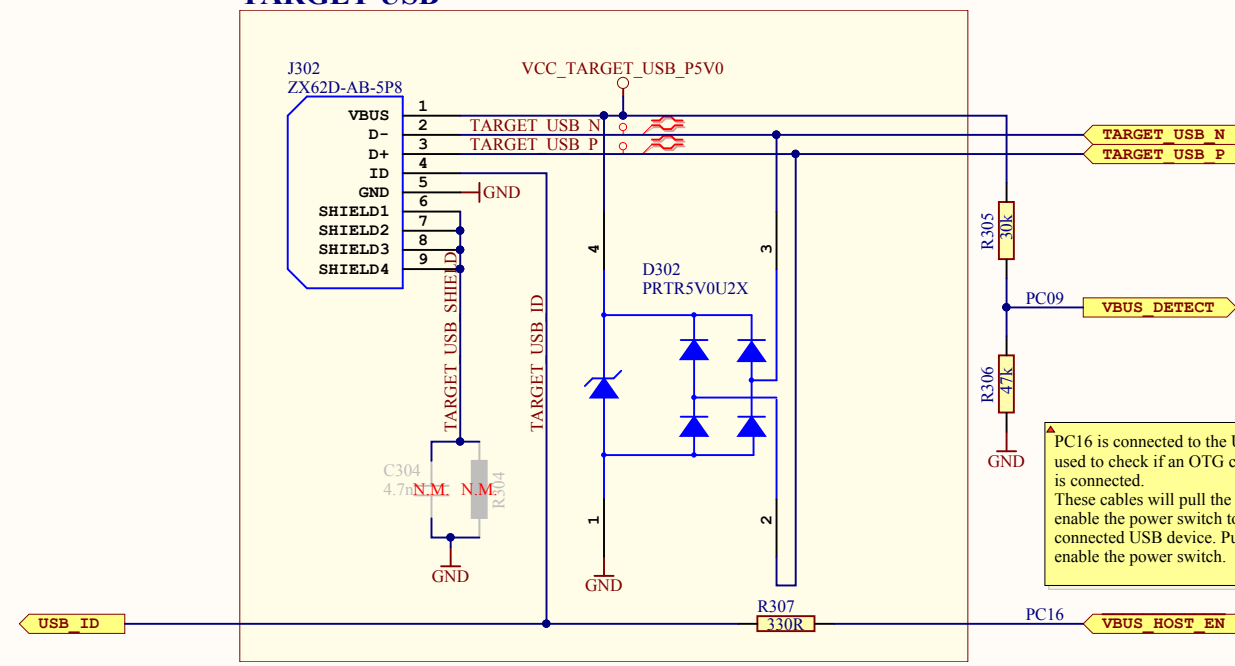
### USER BUTTONS



### USER LEDs



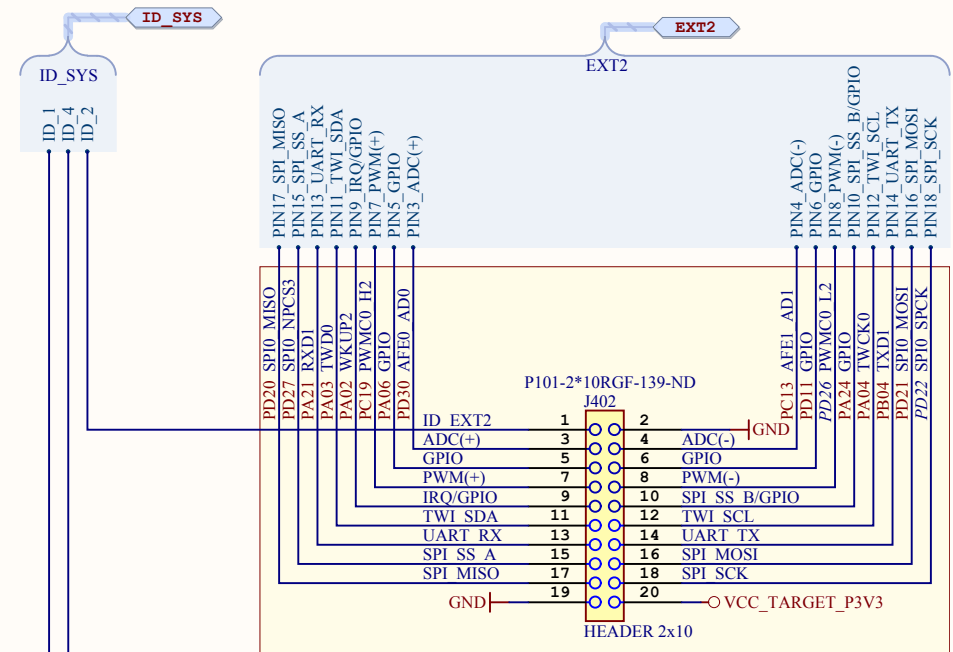
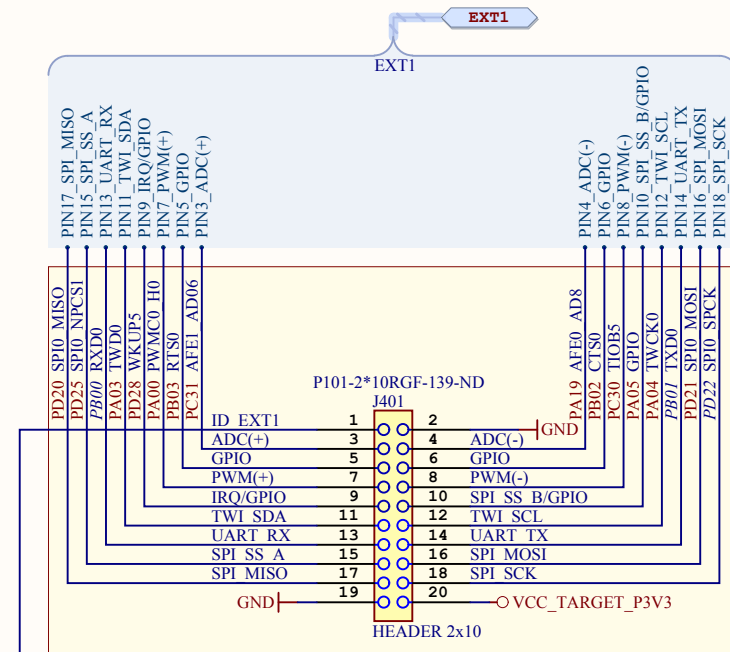
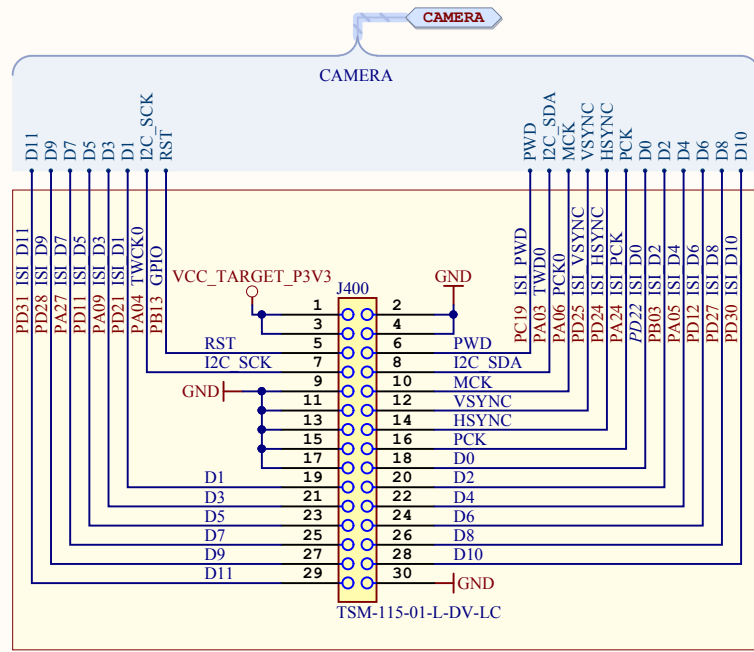
### TARGET USB



PD10 can be used to check if there is a voltage present at VCC\_TARGET\_USB\_P5V0.  
 $V_{max} 3.20V$   
 $V_{min} 2.69V$   
 Note: PD10 is connected through a jumper on J202

PC16 is connected to the USB\_ID signal and can be used to check if an OTG cable or a host mode cable is connected. These cables will pull the USB\_ID signal low and enable the power switch to the connected USB device. Pulling PC16 low will also enable the power switch.

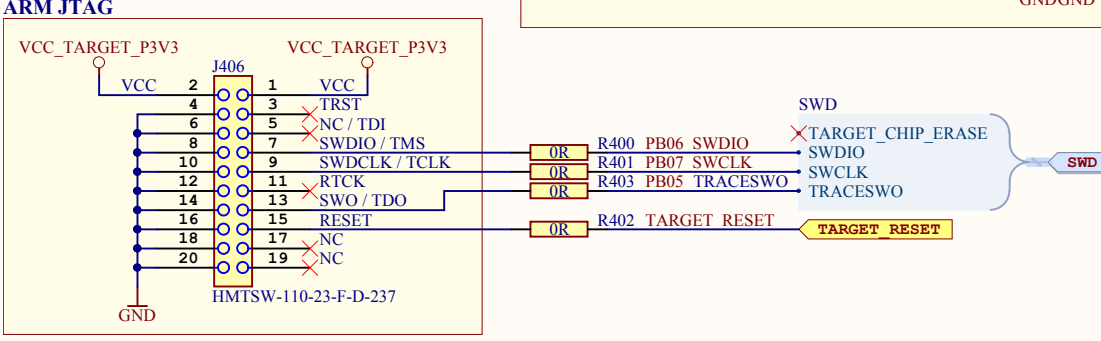
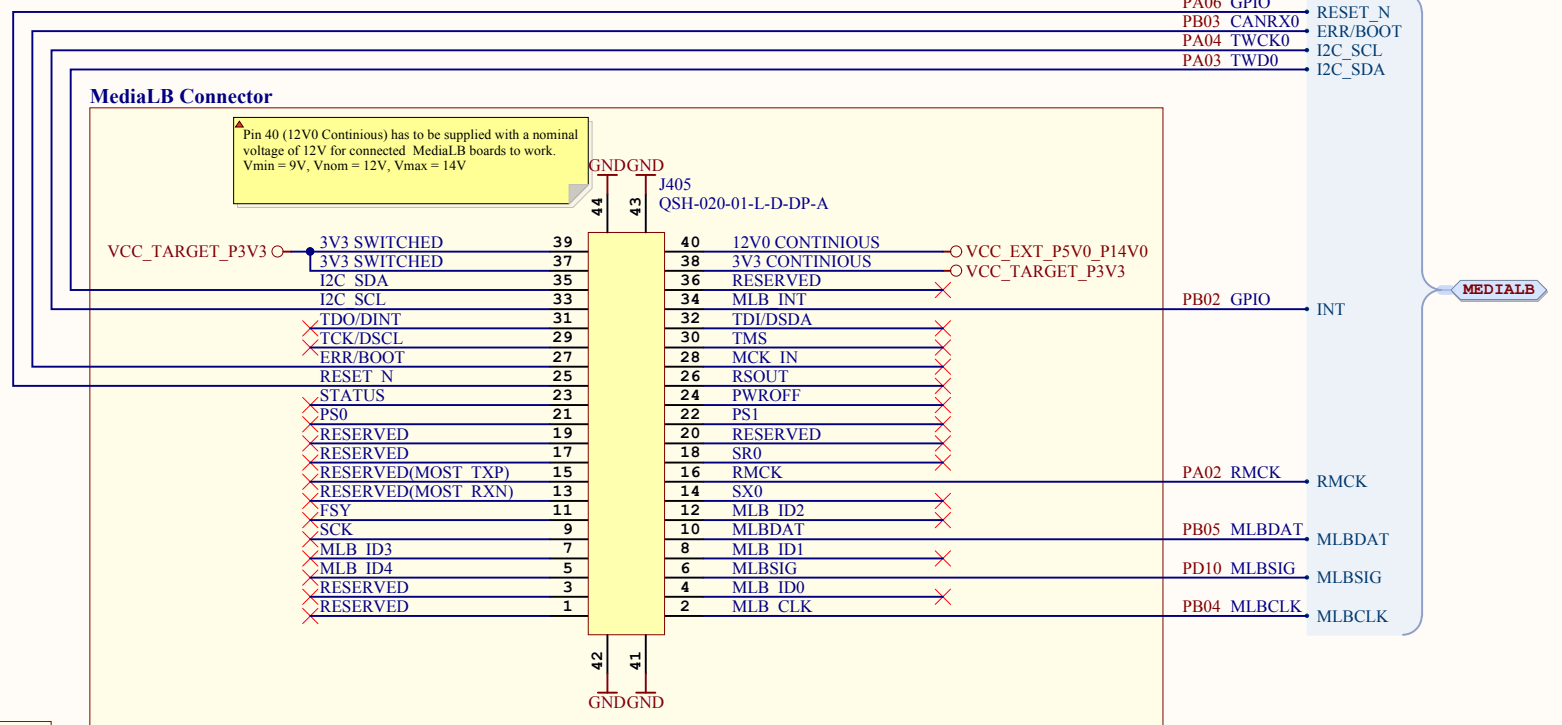
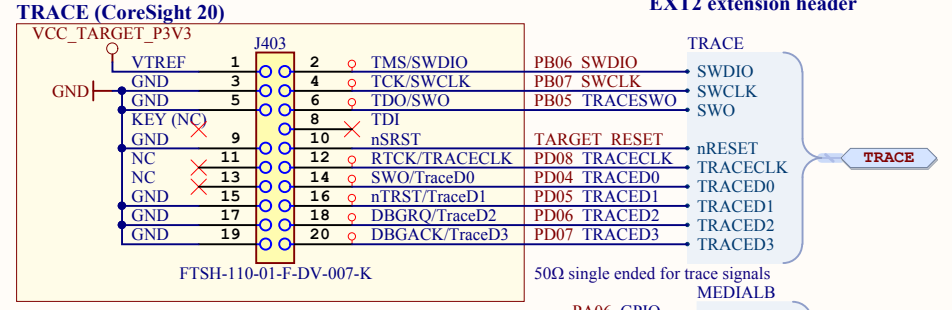
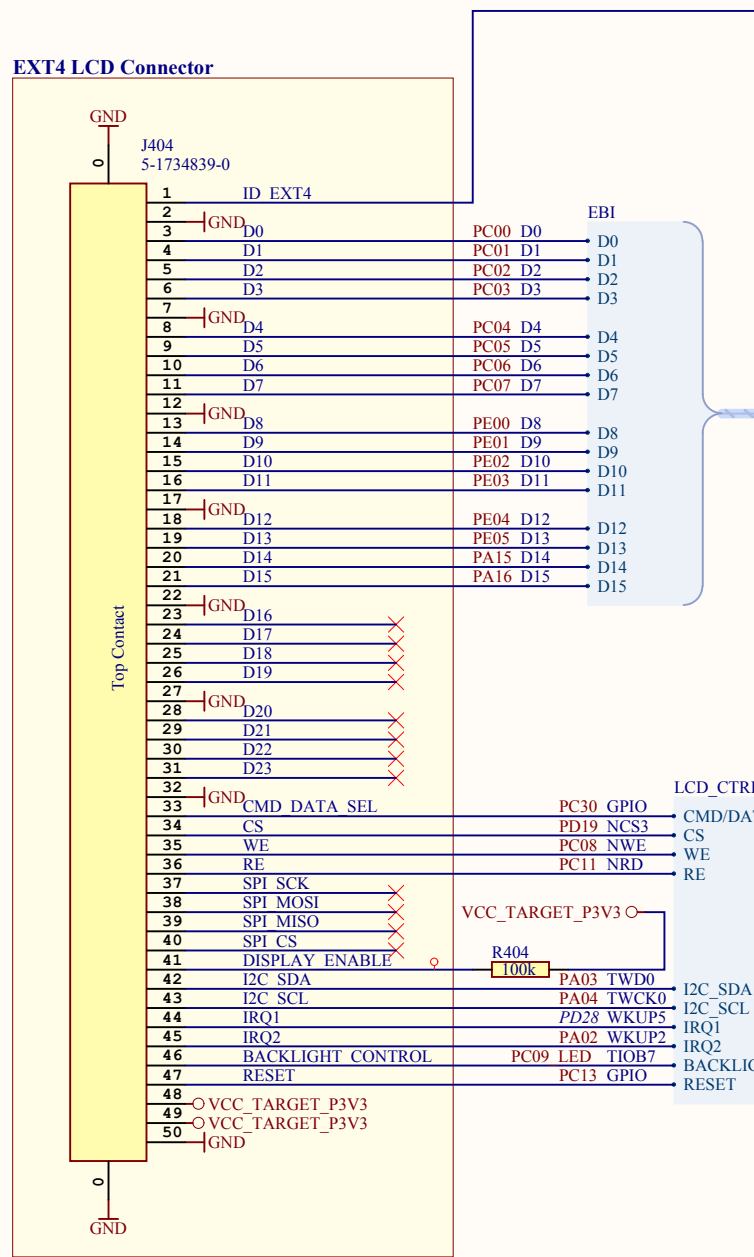
ATMEL Norway	*			
Vestre Rosten 79	*			
N-7075 TILLER	*			
NORWAY				
Date:	16.03.2015	15:01:49	PAGE: 6 of 13	
Document number:	A09-2407		Revision	3
TITLE: Target MCU Peripherals				
SAMV71_Xplained_Ultra_MCU_Peripherals.SchDoc				



Camera Interface Connector

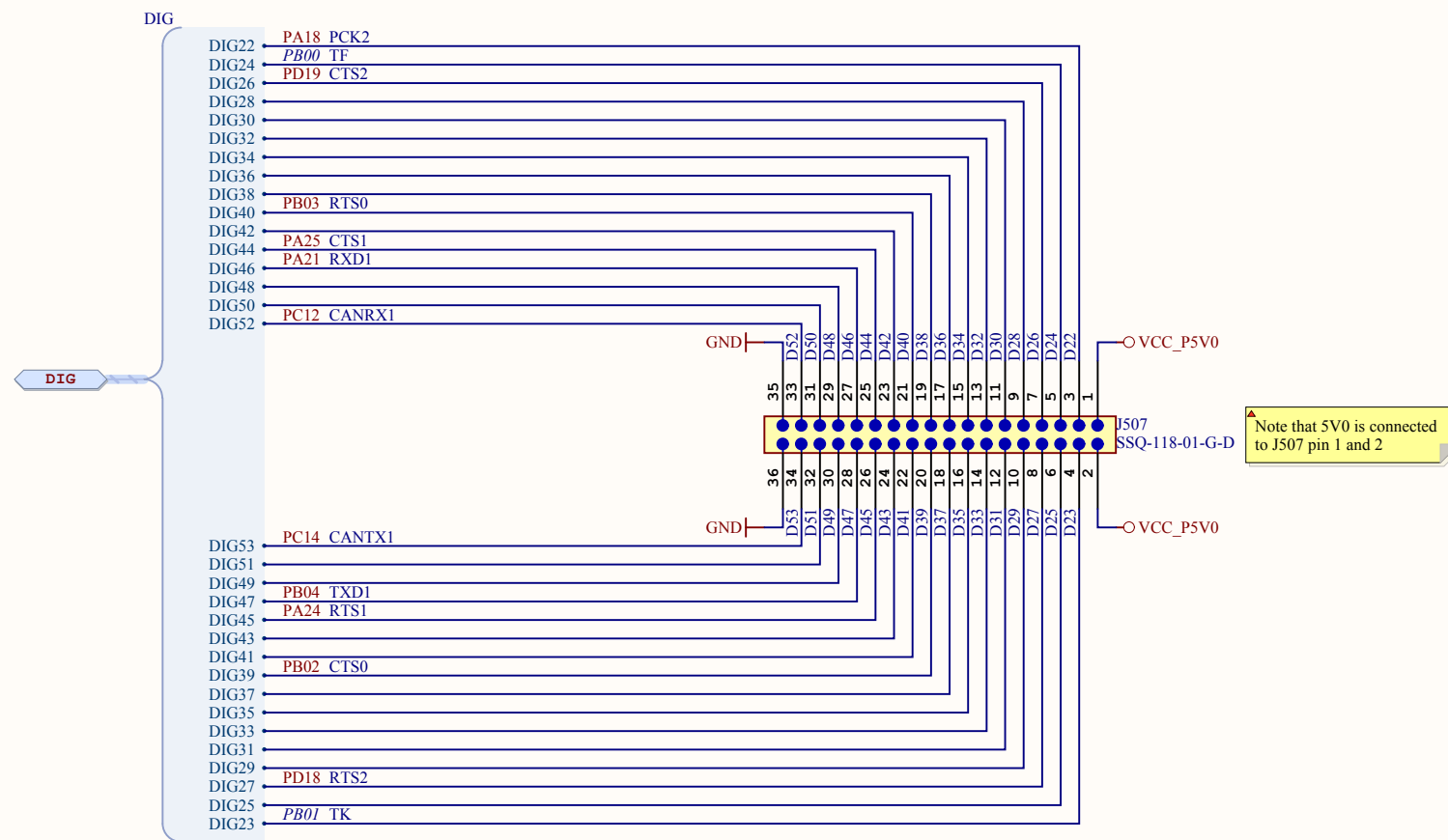
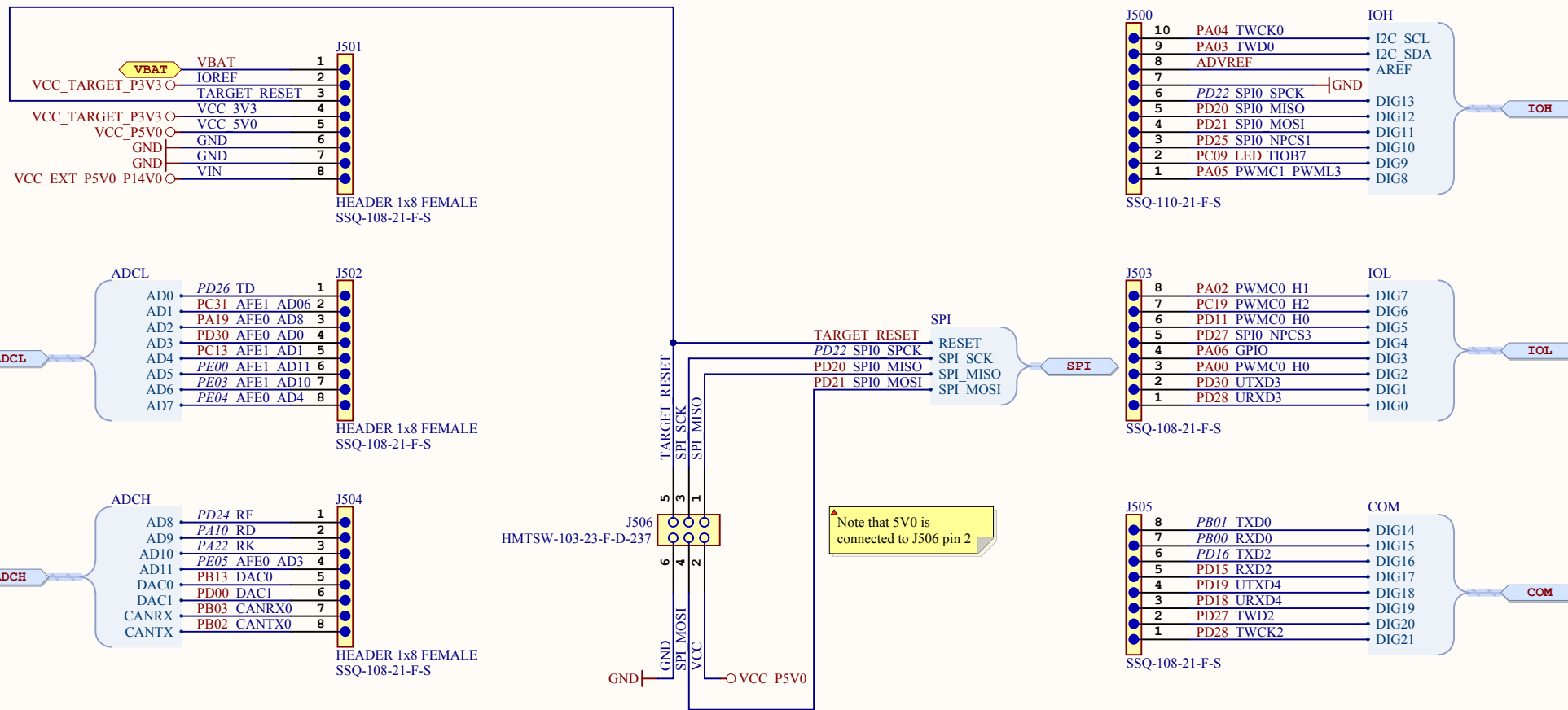
EXT1 extension header


EXT2 extension header



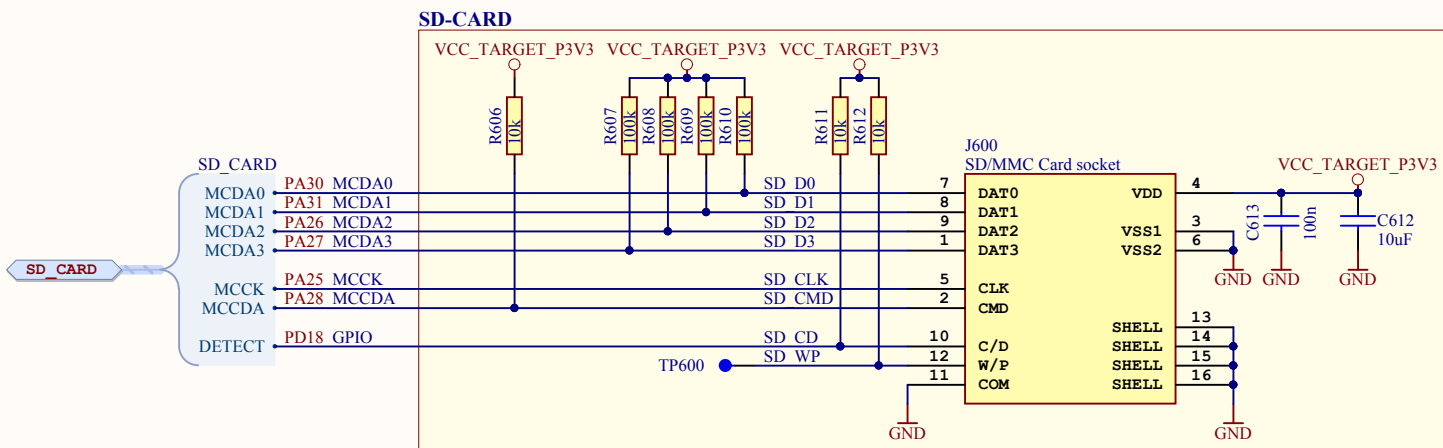
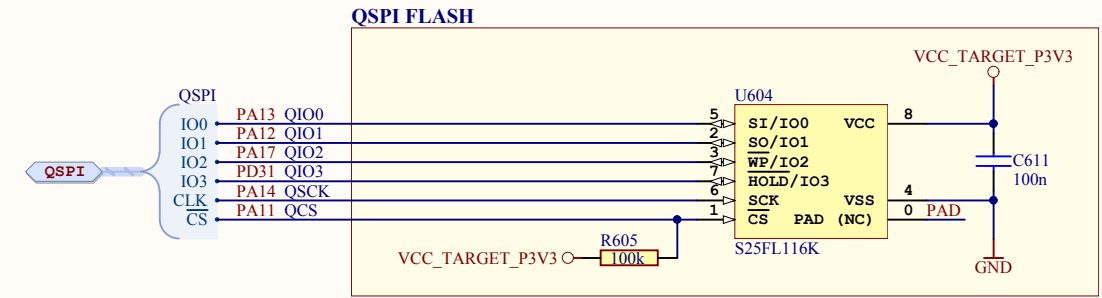
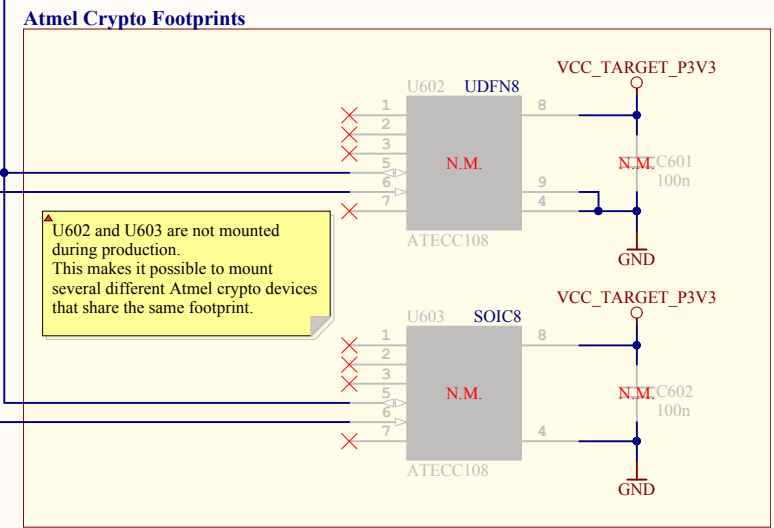
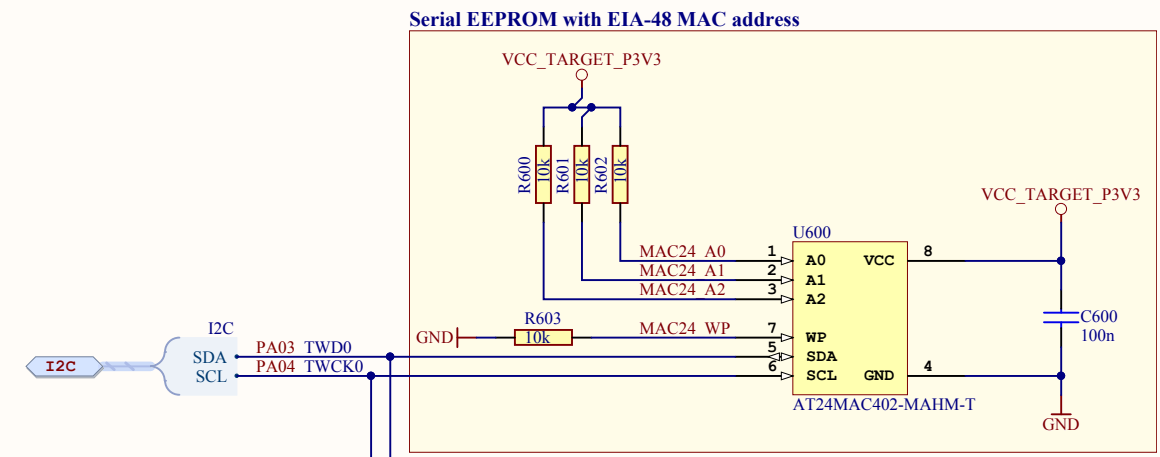
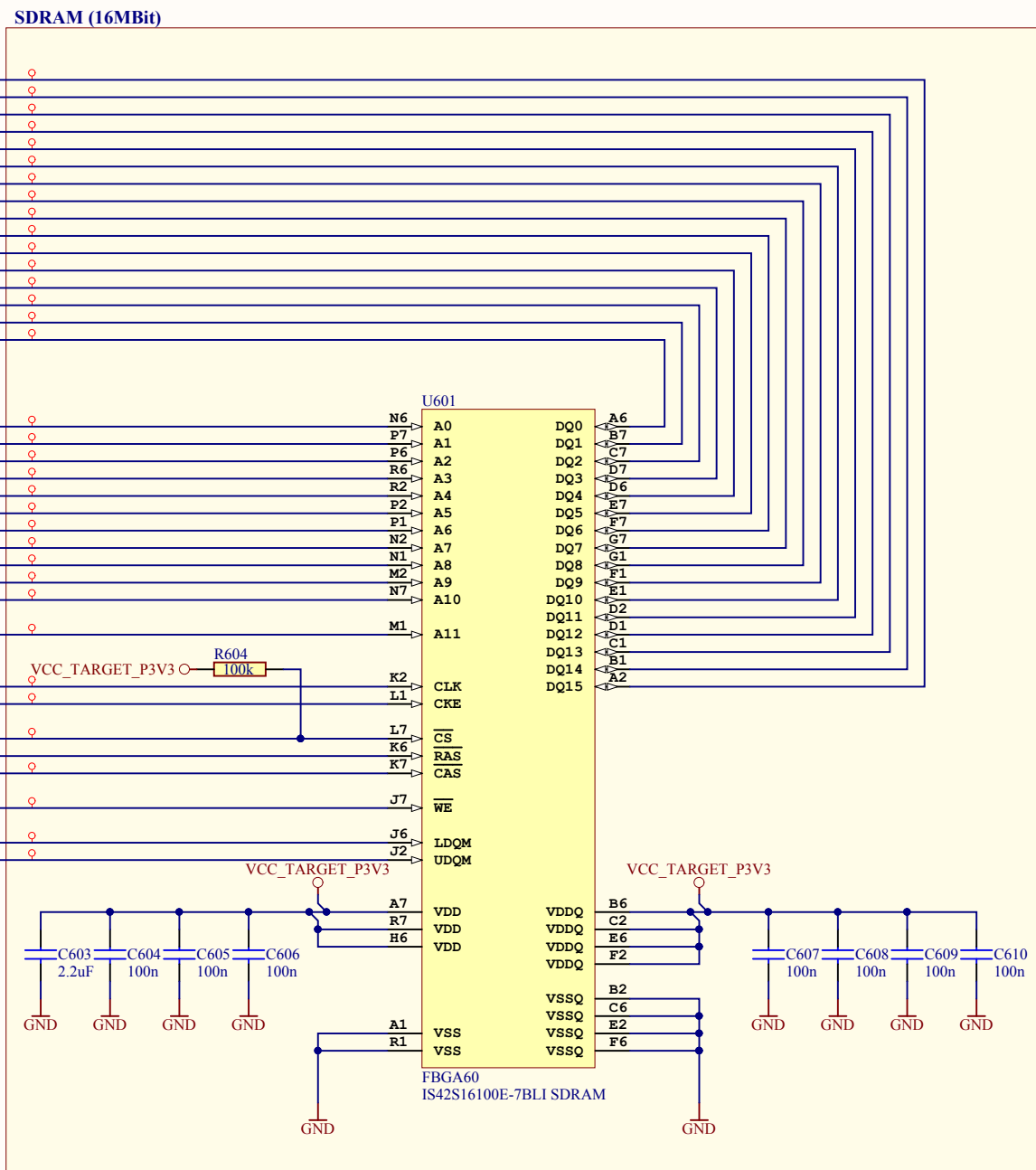
ATMEL Norway	*		
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	16.03.2015	15:01:49	PAGE: 7 of 13
Document number:	A09-2407		Revision 3
TITLE: Extension connectors			
SAMV71_Xplained_Ultra_Connectors.SchDoc			





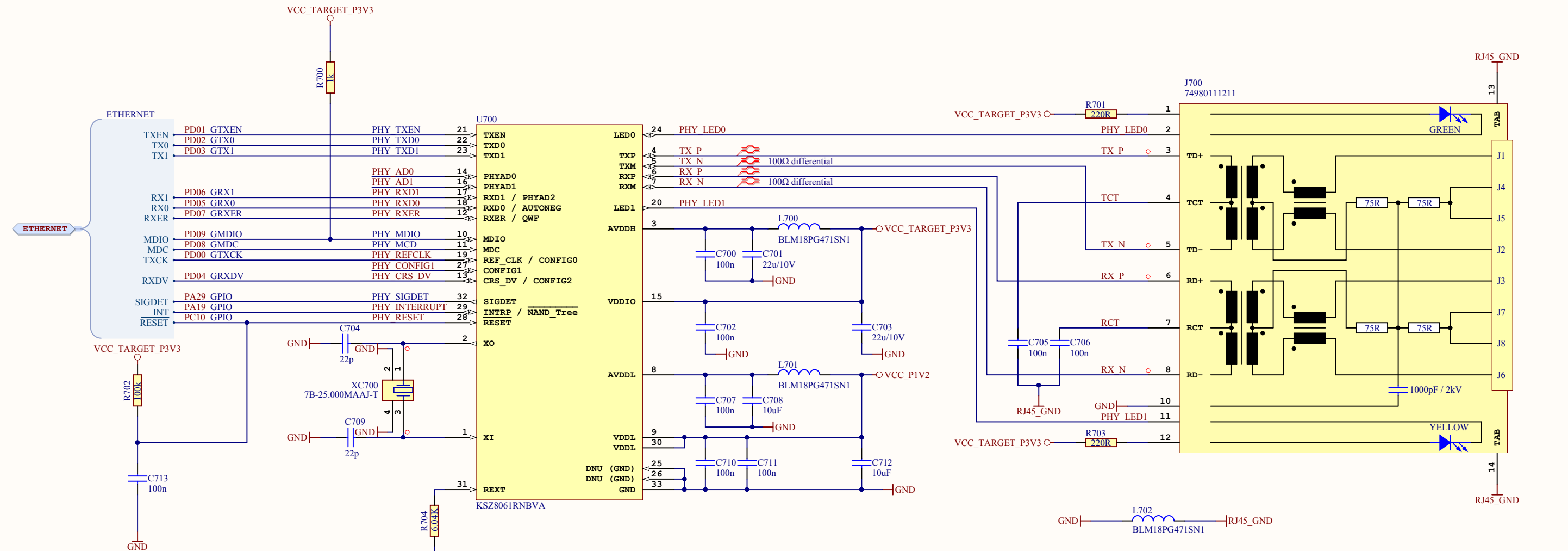
ATMEL Norway	*		
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	16.03.2015	15:01:50	PAGE: 8 of 13
Document number:	A09-2407		Revision: 3
TITLE: Shield Connectors			
SAMV71_Xplained_Ultra_Shield_Connectors.SchDoc			





C/D is connected to COM when a card is placed into the socket.  
W/P is connected to COM when the write protect slider is in protect position.

ATMEL Norway	*			
Vestre Rosten 79	*			
N-7075 TILLER	*			
NORWAY				
Date:	16.03.2015	15:01:50	PAGE: 9 of 13	
Document number:	A09-2407		Revision	3
TITLE: Memory				
SAM71_Xplained_Ultra_Memory.SchDoc				



When the KSZ8061RNBVA is released from reset the configuration values on the pins are latched into the PHY's registers.

PHYAD[2:0] is used to set the PHY's address:  
 001 (default on board)  
 010  
 ....  
 110  
 111

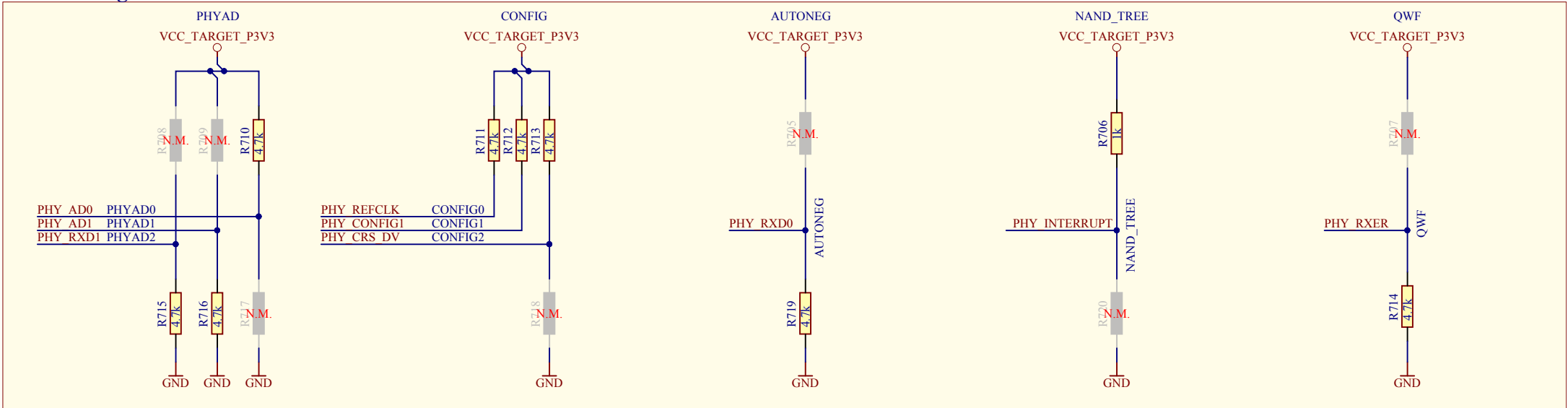
CONFIG[2:0] is used to select operation mode.  
 001 = RMII normal, MDI/MDI-X disabled  
 101 = RMII back to back  
 111 = RMII normal MDI/MDI-X enabled  
 Not configurable on board as back to back


AUTONEG is used to select if auto negotiation of link speed should be enabled.  
 1 = disable Auto-Negotiation  
 0 = enable Auto-Negotiation (default on board)

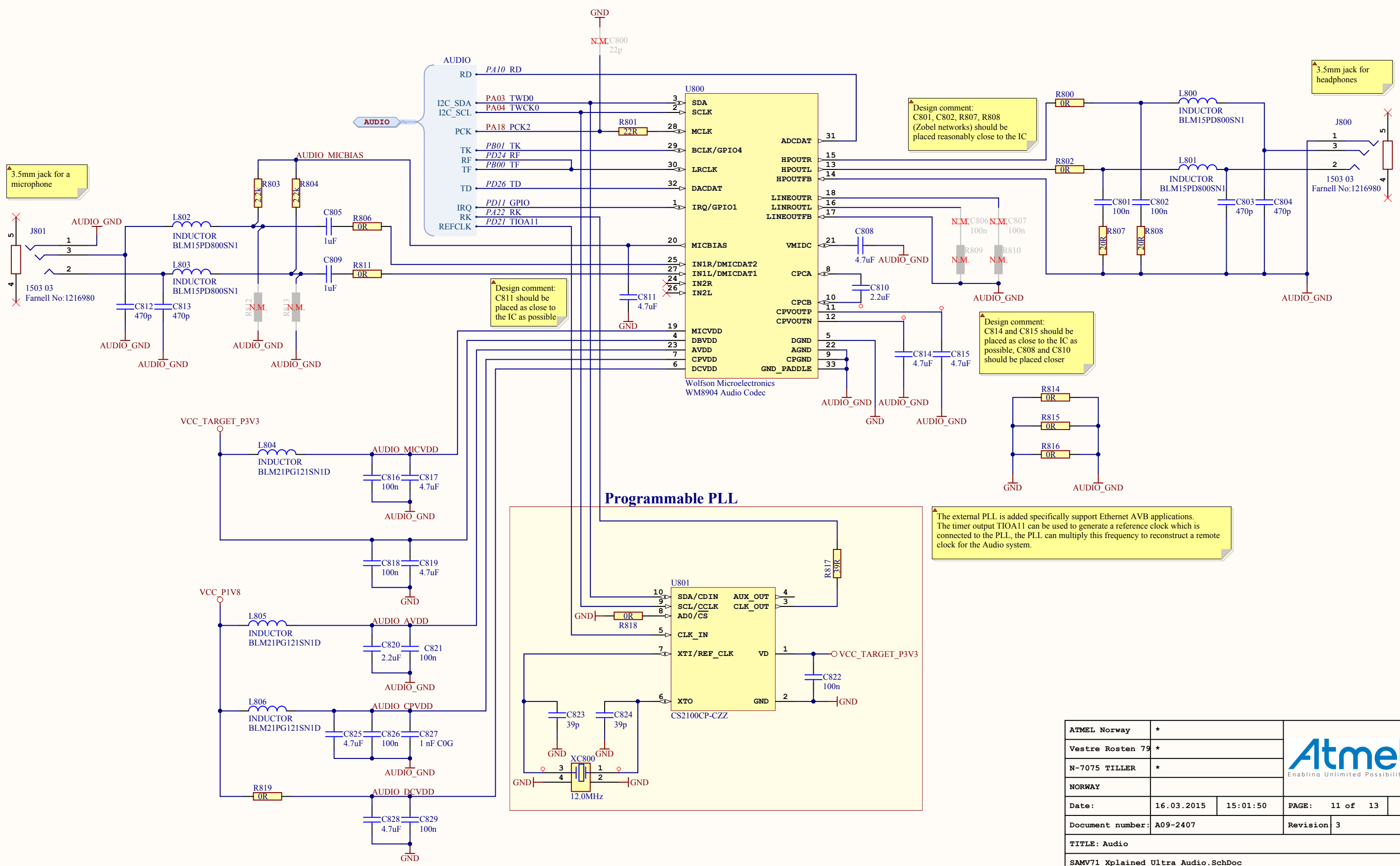
NAND\_TREE enables a test mode for all pins connected to the SAM71Q21.  
 1 = Disable NAND\_TREE (default on board)  
 0 = Enable NAND\_TREE

QWF is used to enable/disable Quiet-WIRE Filtering  
 1 = Disable Quiet-WIRE Filtering  
 0 = Enable Quiet-WIRE Filtering (default on board)

**PHY Configuration**



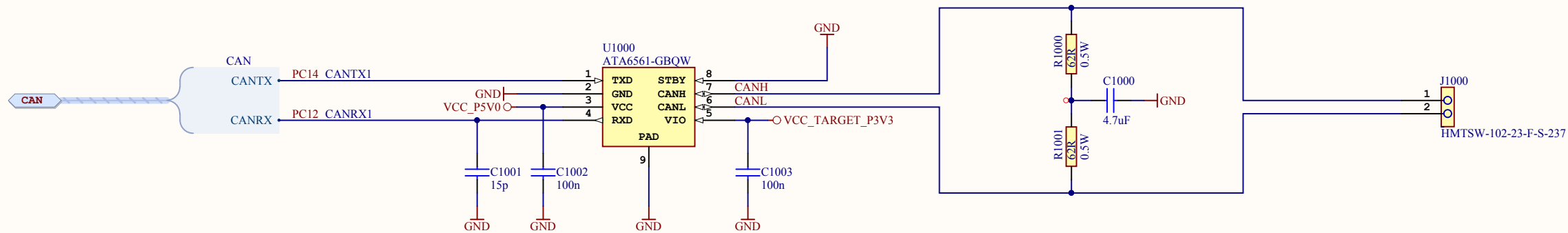
ATMEL Norway	*		
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	16.03.2015	15:01:50	PAGE: 10 of 13
Document number:	A09-2407		Revision: 3
TITLE: Ethernet			
SAM71_Xplained_Ultra_Ethernet.SchDoc			




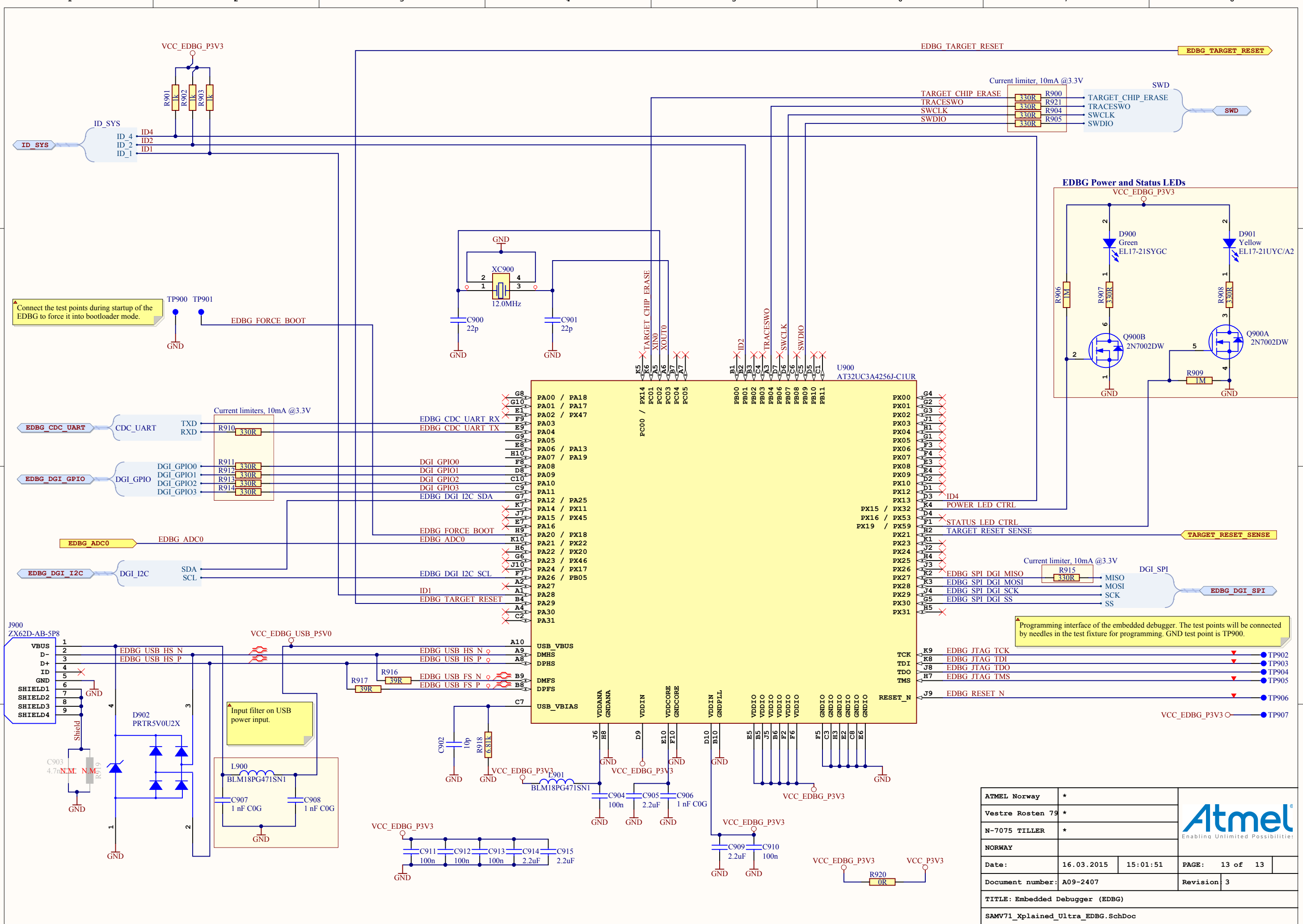
ATMEL Norway	*		
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	16.03.2015	15:01:50	PAGE: 11 of 13
Document number:	A09-2407		Revision: 3
TITLE: Audio			
SAMV71_Xplained_Ultra_Audio.SchDoc			







ATMEL Norway	*	 Enabling Unlimited Possibilities	
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	16.03.2015	15:01:51	PAGE: 12 of 13
Document number:	A09-2407		Revision 3
TITLE: CAN			
SAMV71_Xplained_Ultra_CAN_SchDoc			



Connect the test points during startup of the EDBG to force it into bootloader mode.

Current limiters, 10mA @3.3V

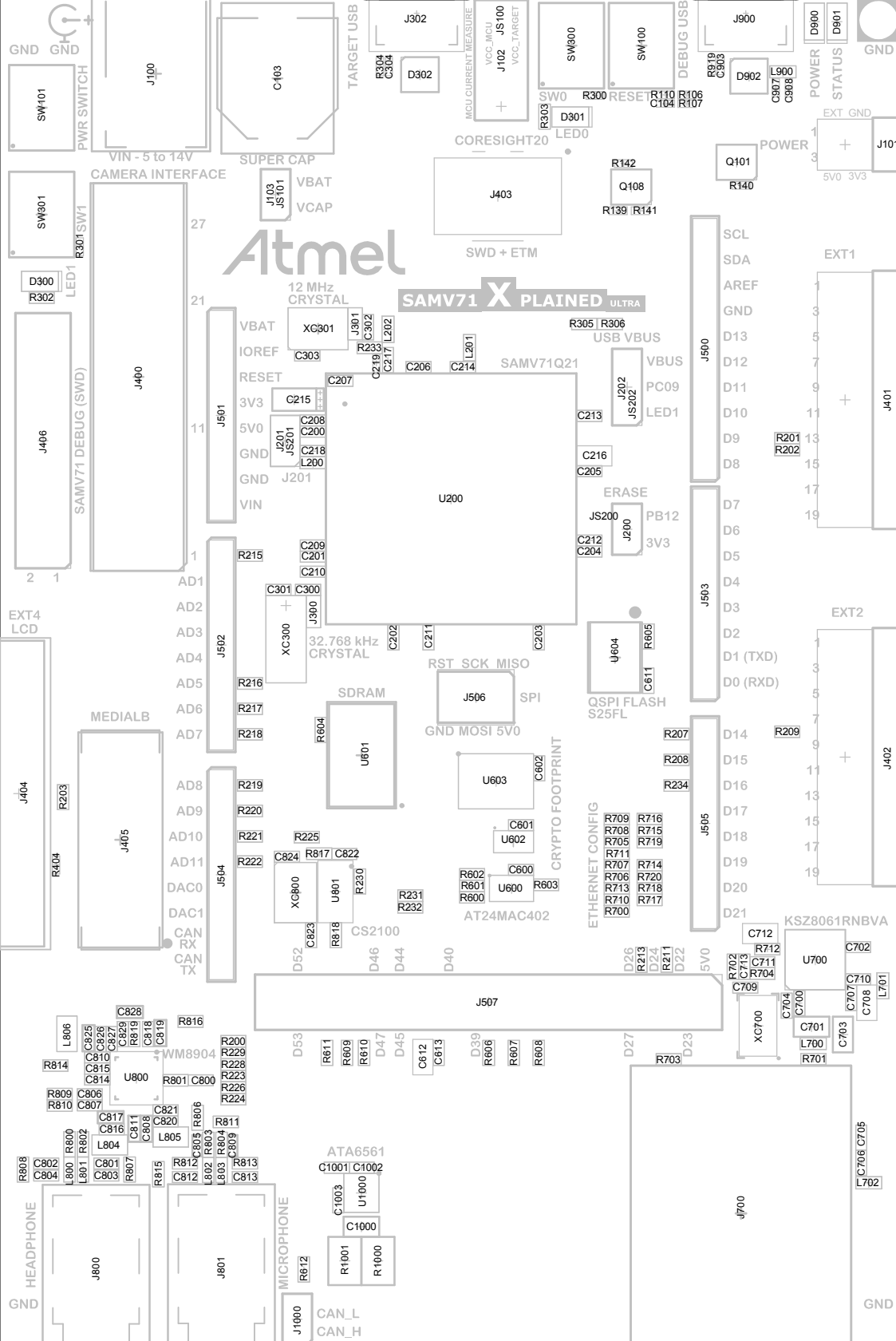
Current limiter, 10mA @3.3V

Current limiter, 10mA @3.3V

Input filter on USB power input.

Programming interface of the embedded debugger. The test points will be connected by needles in the test fixture for programming. GND test point is TP900.

ATMEL Norway	*			
Vestre Rosten 79	*			
N-7075 TILLER	*			
NORWAY				
Date:	16.03.2015	15:01:51	PAGE:	13 of 13
Document number:	A09-2407		Revision:	3
TITLE: Embedded Debugger (EDBG)				
SAMV71_Xplained_Ultra_EDBG.SchDoc				



# Atmel SAM71X PLAINED ULTRA

**Atmel SAM71X PLAINED ULTRA**

VIN - 5 to 14V

PWR SWITCH SW401

GND

J100

C163

TARGET USB J302

R304 C304

D302

MCU CURRENT MEASURE J102 JS100

VCC\_MCU

SW800

SW100

DEBUG USB J900

R919 C903

D902

L900 C907 C908

POWER D900

STATUS D901

GND

EXT GND

1 3

POWER

5V0 3V3

J101

CAMERA INTERFACE

SW301

R301/SW1

D300

R302

LED1

J400

11 27

21

12 MHz CRYSTAL XC301

J901

C302

C303

VBAT

IOREF

RESET

3V3

C215

C208

C200

C218

L200

J201

J406

J501

11

J400

SAM71X DEB (SWD)

R301/SW1

2 1

21

11

AD1

AD2

AD3

AD4

AD5

AD6

AD7

AD8

AD9

AD10

AD11

DAC0

DAC1

CAN RX

CAN TX

EXT4 LCD

J404

R203

R205

R215

R216

R217

R218

R219

R220

R221

R222

J502

J504

J501

C209

C201

C210

C300

C301

J300

XC300

32.768 kHz CRYSTAL

C202

C211

C203

J506

J503

J505

J401

EXT1

1 3 5 7 9 11 13 15 17 19

SCL

SDA

AREF

GND

D13

D12

D11

D10

D9

D8

D7

D6

D5

D4

D3

D2

D1 (TXD)

D0 (RXD)

EXT2

J402

1 3 5 7 9 11 13 15 17 19

SDRAM U601

R604

R600

R601

R600

R602

R601

R600

U600

C602

U603

U604

R605

C611

QSPI FLASH S25FL

CRYPTO FOOTPRINT

AT24MAC402 U600

C600

C601

U602

R709

R708

R705

R711

R707

R714

R706

R720

R713

R718

R710

R717

R716

R715

R719

R711

R714

R718

R720

R717

R700

ETHERNET CONFIG

J405

R203

R204

R205

R206

R207

R208

R234

R209

J405

J402

1 3 5 7 9 11 13 15 17 19

MEDIA L B

J405

R203

R204

R205

R206

R207

R208

R234

R209

J405

J402

1 3 5 7 9 11 13 15 17 19

CS2100

D52

D46

D44

D40

D45

D47

D43

D42

D26

R213

D24

R211

D22

5V0

D27

D23

J507

D53

R611

R609

R610

D47

D45

C812

C813

D39

R606

R607

R608

U700

C712

R712

C713

C711

R704

C707

C704

C706

C705

C701

L700

R701

C703

C707

C710

C708

L701

C702

C706

C705

L702

KSZ8061RNBVA

J700

R703

D23

HEADPHONE

J800

R808

C802

C804

L800

R801

R802

C801

C803

R807

R815

R816

R809

C806

R810

C807

C817

C816

L804

C811

C810

C819

C828

C825

C826

C827

C829

R819

R818

C818

C819

WM8904

R200

R229

R228

R223

R226

R224

R801

C800

R803

R804

C809

R811

R812

C803

R804

C809

R813

C813

ATA6561

C1001

C1002

C1003

U1000

R1000

R1000

MICROPHONE

J801

R812

C812

L805

C820

C821

C820

R811

R812

C803

R804

C809

R813

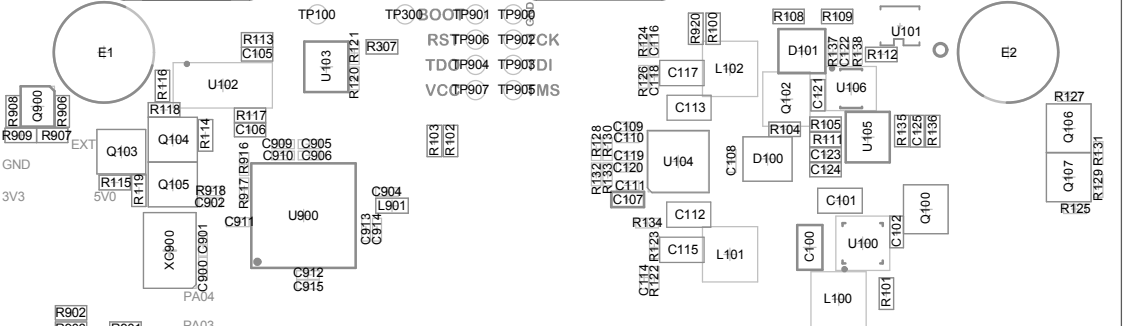
C813

J1000

CAN\_L

CAN\_H

GND



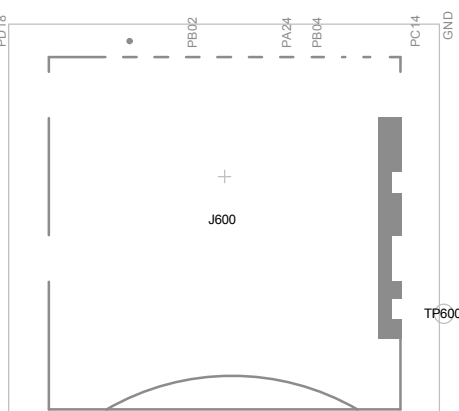
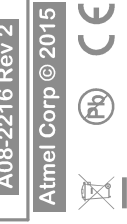
GND	ID	ADVREF
PA19	PC31	GND
PB02	PB03	NC
PC30	PA00	PD20
PA05	PD28	PD21
PA04	PA03	PD25
PB01	PB00	PC09
PD21	PD25	PA05
PD22	PD20	
VCC	GND	PA02
		PC19
		PD11
		PD27
		PA06
GND	ID	PA00
PC13	PD30	PD30
PD11	PA06	PD28
PD26	PC19	
PA24	PA02	PB01
PA04	PA03	PB00
PB04	PA21	PD16
PD21	PD27	PD15
PD22	PD20	PD19
3V3	GND	PD18
		PD27
		PD28

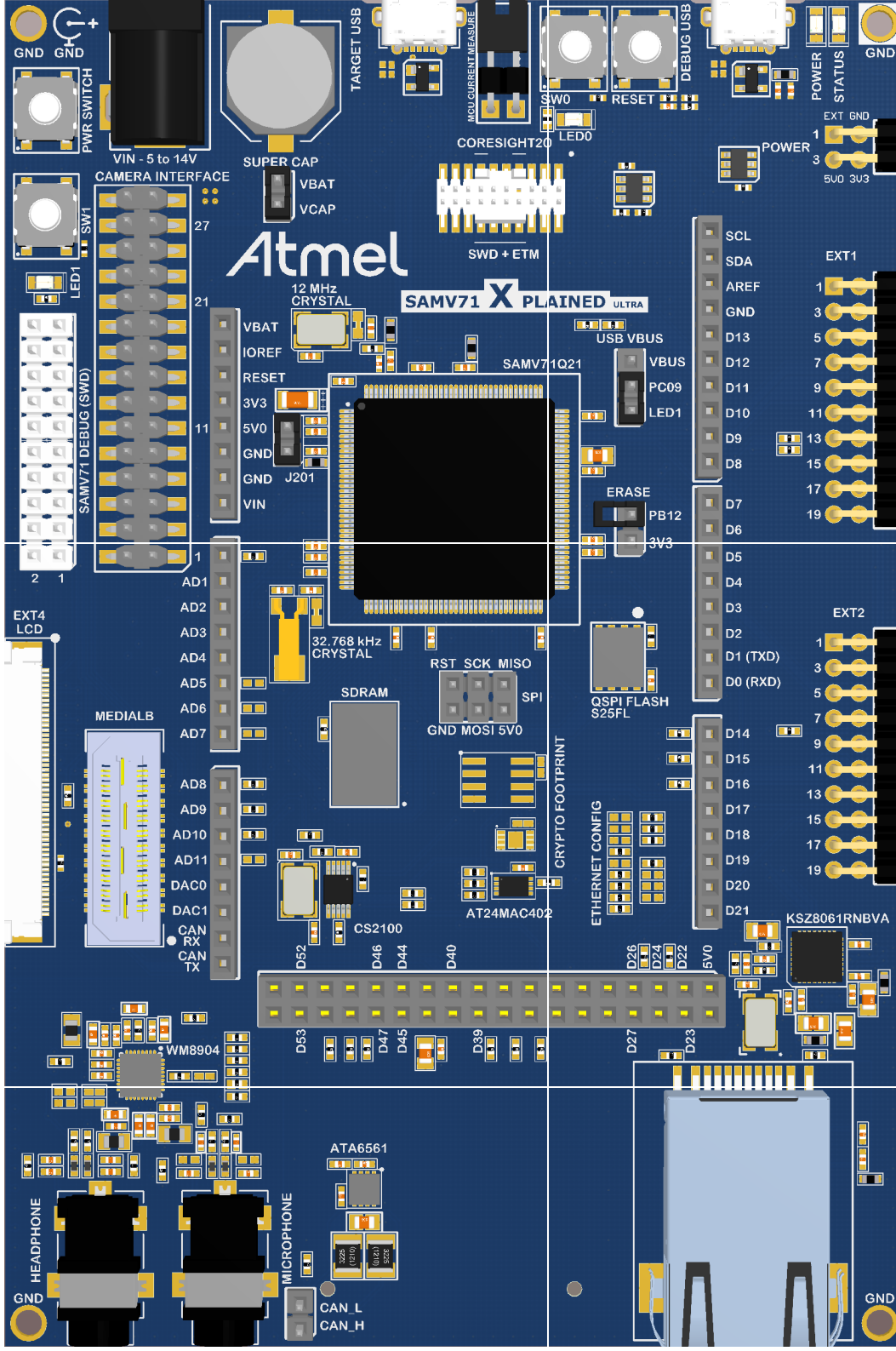
R914	R913	R912	R911	R905	R904	R903	R902	R901	R900
TP201									
TP200									

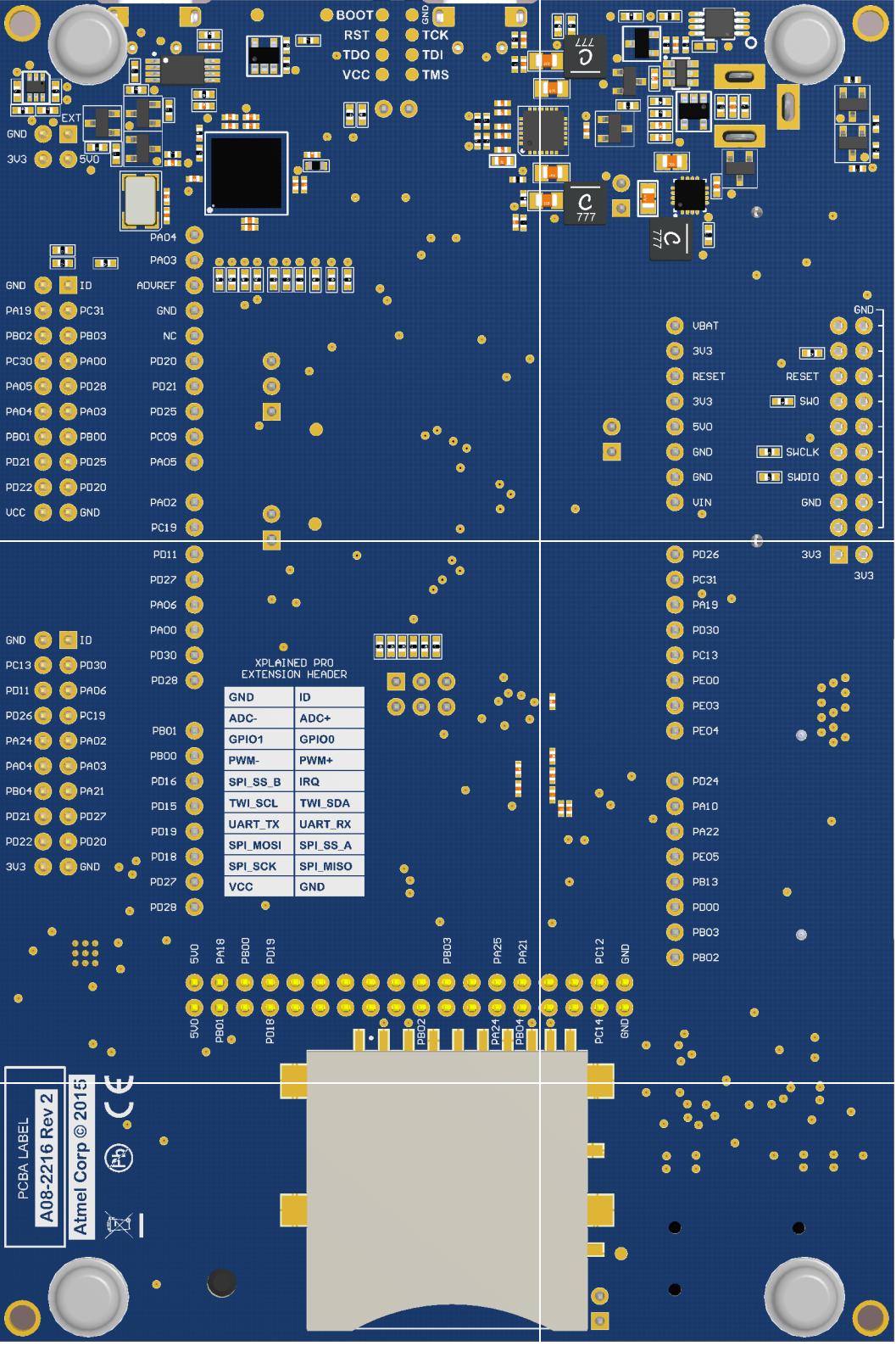
R204	R212	R227	R228	R229	R230	R231	R234
VBAT	3V3	RESET	RESET	3V3	SWO	5V0	SWCLK
GND	SWDIO	SWCLK	SWCLK	GND	SWDIO	GND	SWDIO
VIN	GND	GND	GND	VIN	GND	GND	GND
PD26	3V3	3V3	3V3	PD26	3V3	3V3	3V3
PC31	PC31	PC31	PC31	PC31	PC31	PC31	PC31
PA19	PA19	PA19	PA19	PA19	PA19	PA19	PA19
PD30	PD30	PD30	PD30	PD30	PD30	PD30	PD30
PC13	PC13	PC13	PC13	PC13	PC13	PC13	PC13
PE00	PE00	PE00	PE00	PE00	PE00	PE00	PE00
PE03	PE03	PE03	PE03	PE03	PE03	PE03	PE03
PE04	PE04	PE04	PE04	PE04	PE04	PE04	PE04
PD24	PD24	PD24	PD24	PD24	PD24	PD24	PD24
PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10
PA22	PA22	PA22	PA22	PA22	PA22	PA22	PA22
PE05	PE05	PE05	PE05	PE05	PE05	PE05	PE05
PB13	PB13	PB13	PB13	PB13	PB13	PB13	PB13
PD00	PD00	PD00	PD00	PD00	PD00	PD00	PD00
PB03	PB03	PB03	PB03	PB03	PB03	PB03	PB03
PB02	PB02	PB02	PB02	PB02	PB02	PB02	PB02

XPLAINED PRO  
EXTENSION HEADER

GND	ID
ADC-	ADC+
GPIO1	GPIO0
PWM-	PWM+
SPI_SS_B	IRQ
TWI_SCL	TWI_SDA
UART_TX	UART_RX
SPI_MOSI	SPI_SS_A
SPI_SCK	SPI_MISO
VCC	GND







- BOOT
- RST
- TDO
- VCC
- TCK
- TDI
- TMS

- GND
- 3V3
- 5V0
- PA04
- PA03
- ID
- ADUREF
- PA19
- PB02
- PC30
- PA05
- PAD4
- PB01
- PD21
- PD22
- UCC
- GND
- PA02
- PC19

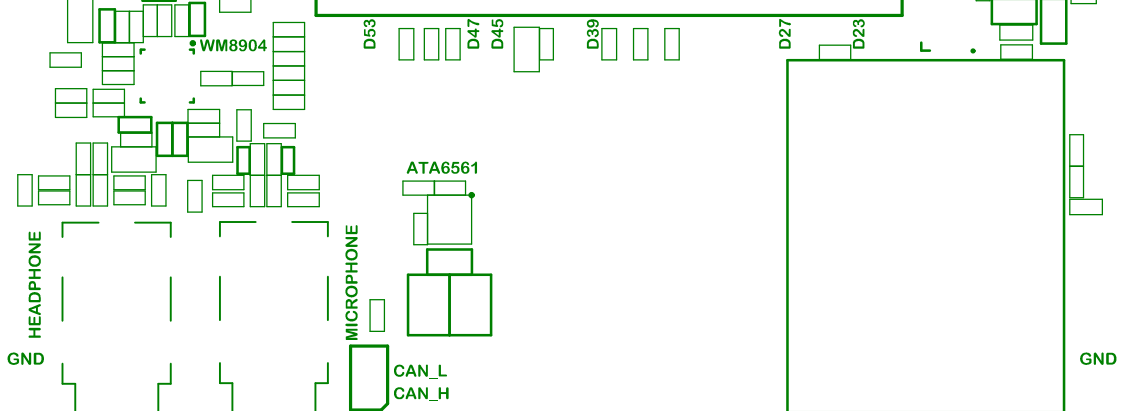
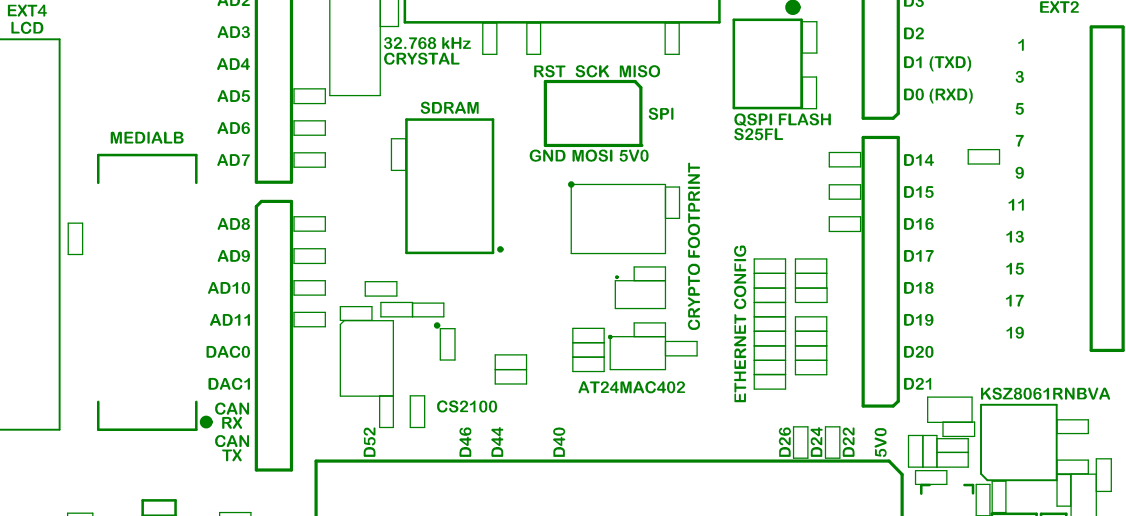
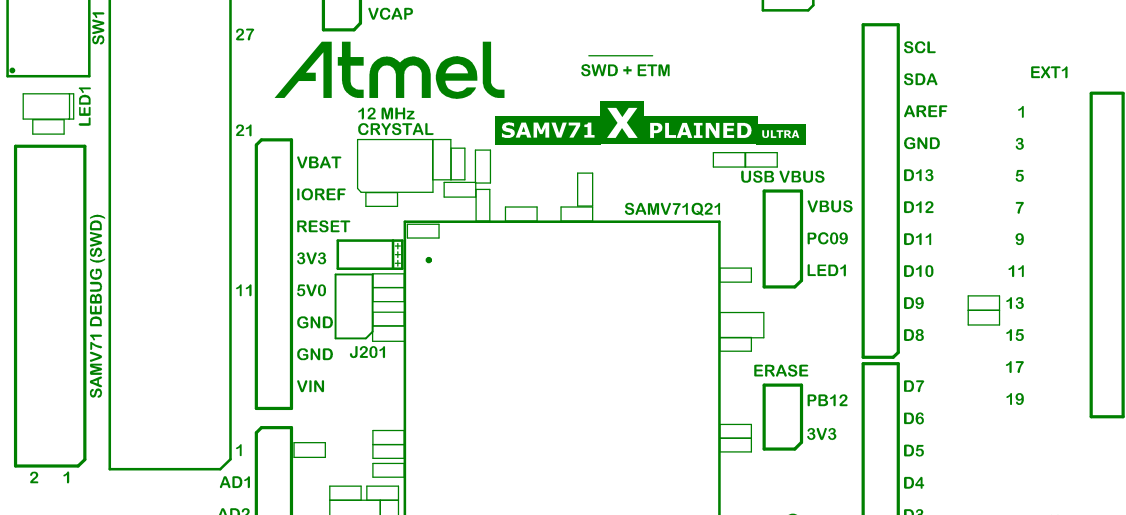
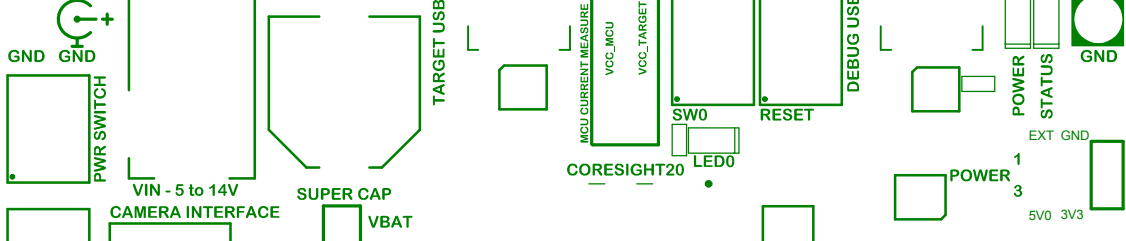
- GND
- UBAT
- 3V3
- RESET
- 3V3
- 5V0
- GND
- GND
- UIN
- GND
- SW0
- SWCLK
- SWDIO
- GND

- GND
- PC13
- PD11
- PD26
- PA24
- PA04
- PB04
- PD21
- PD22
- 3V3
- GND
- PD28
- PD18
- PD27
- PD29
- 5V0
- PA18
- PB00
- PD16
- PB01
- PD02
- PA24
- PB04
- PC14
- GND

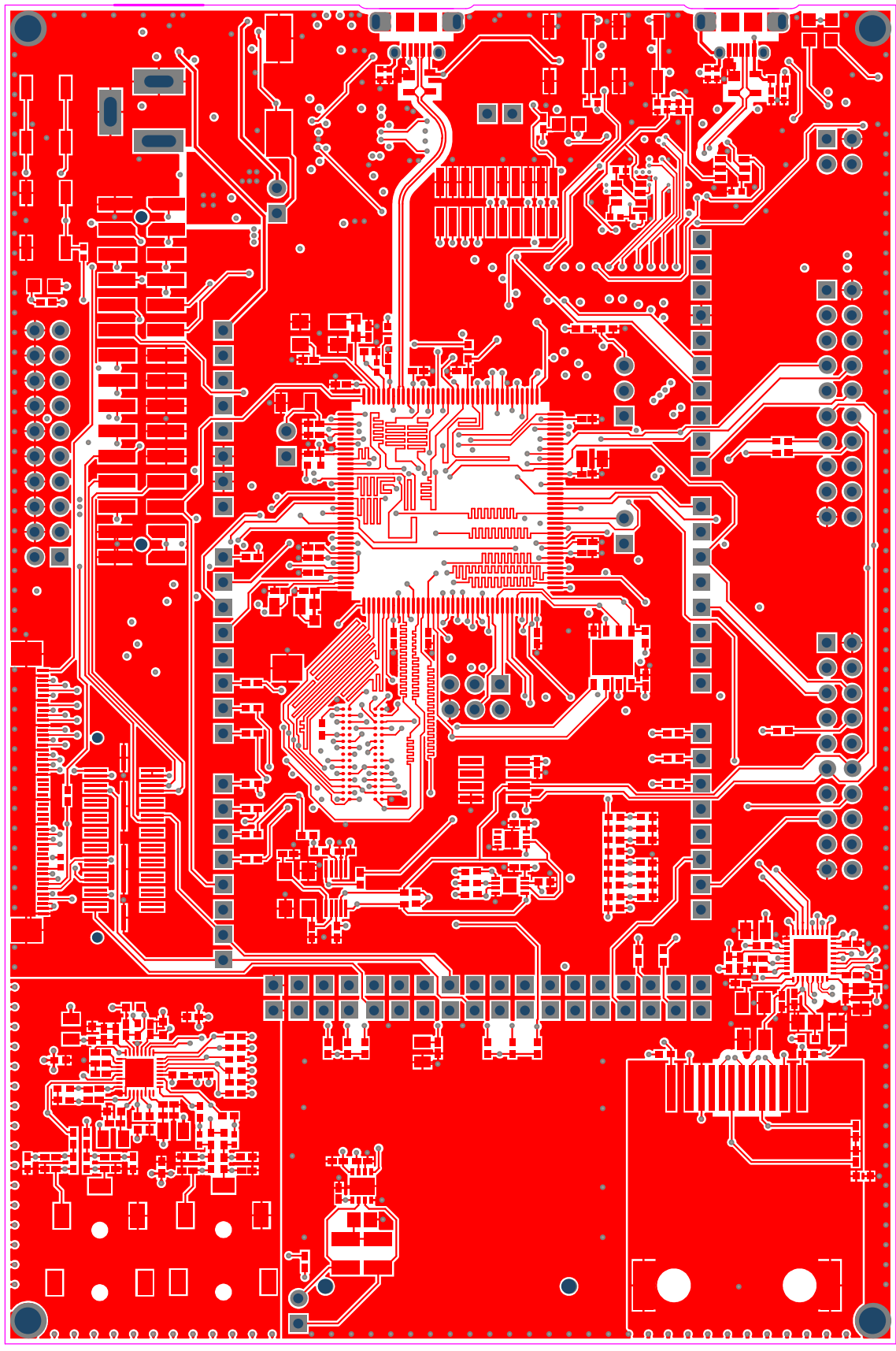
XPLAINED PRO  
EXTENSION HEADER

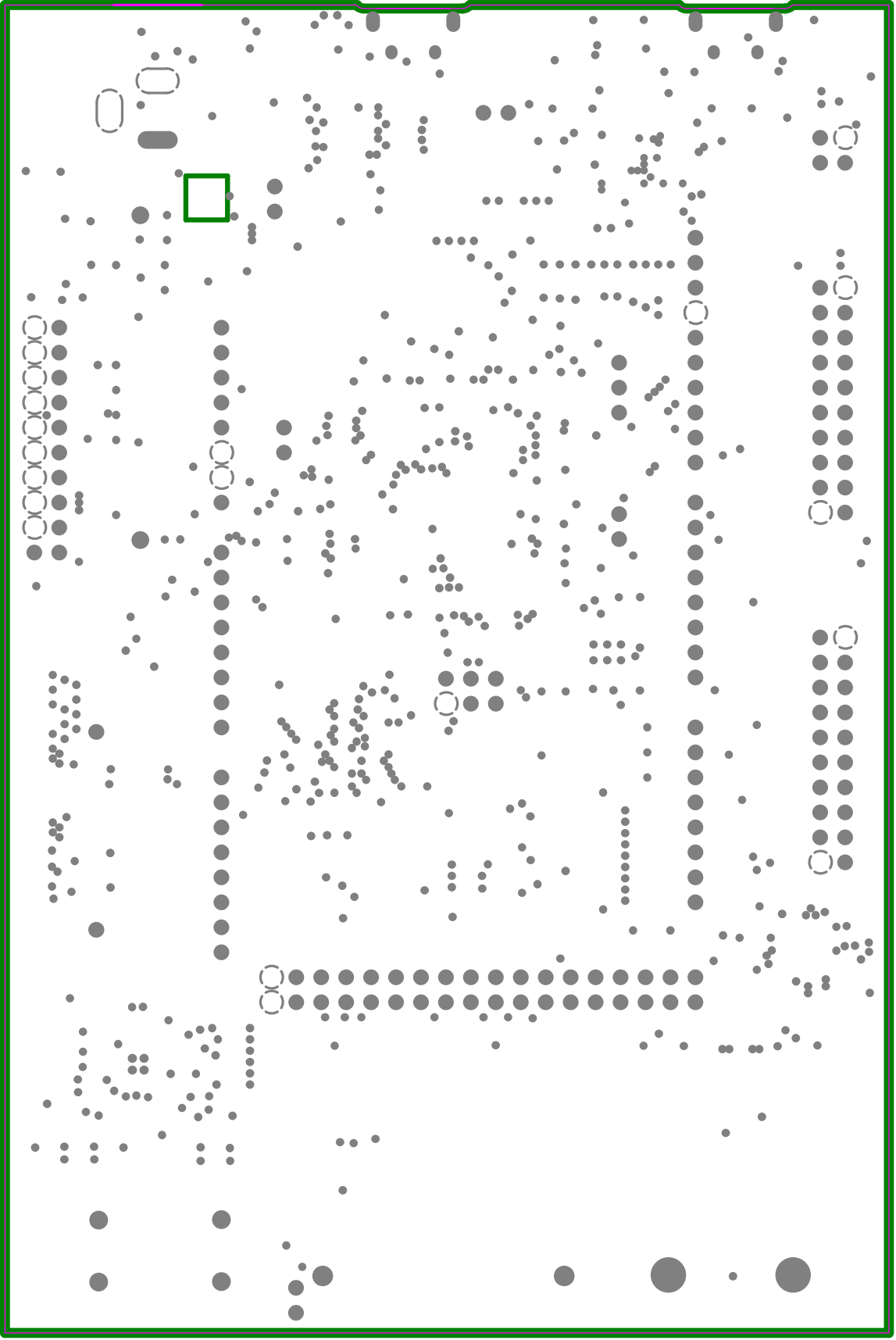
GND	ID
ADC-	ADC+
GPIO1	GPIO0
PWM-	PWM+
SPI_SS_B	IRQ
TWI_SCL	TWI_SDA
UART_TX	UART_RX
SPI_MOSI	SPI_SS_A
SPI_SCK	SPI_MISO
VCC	GND

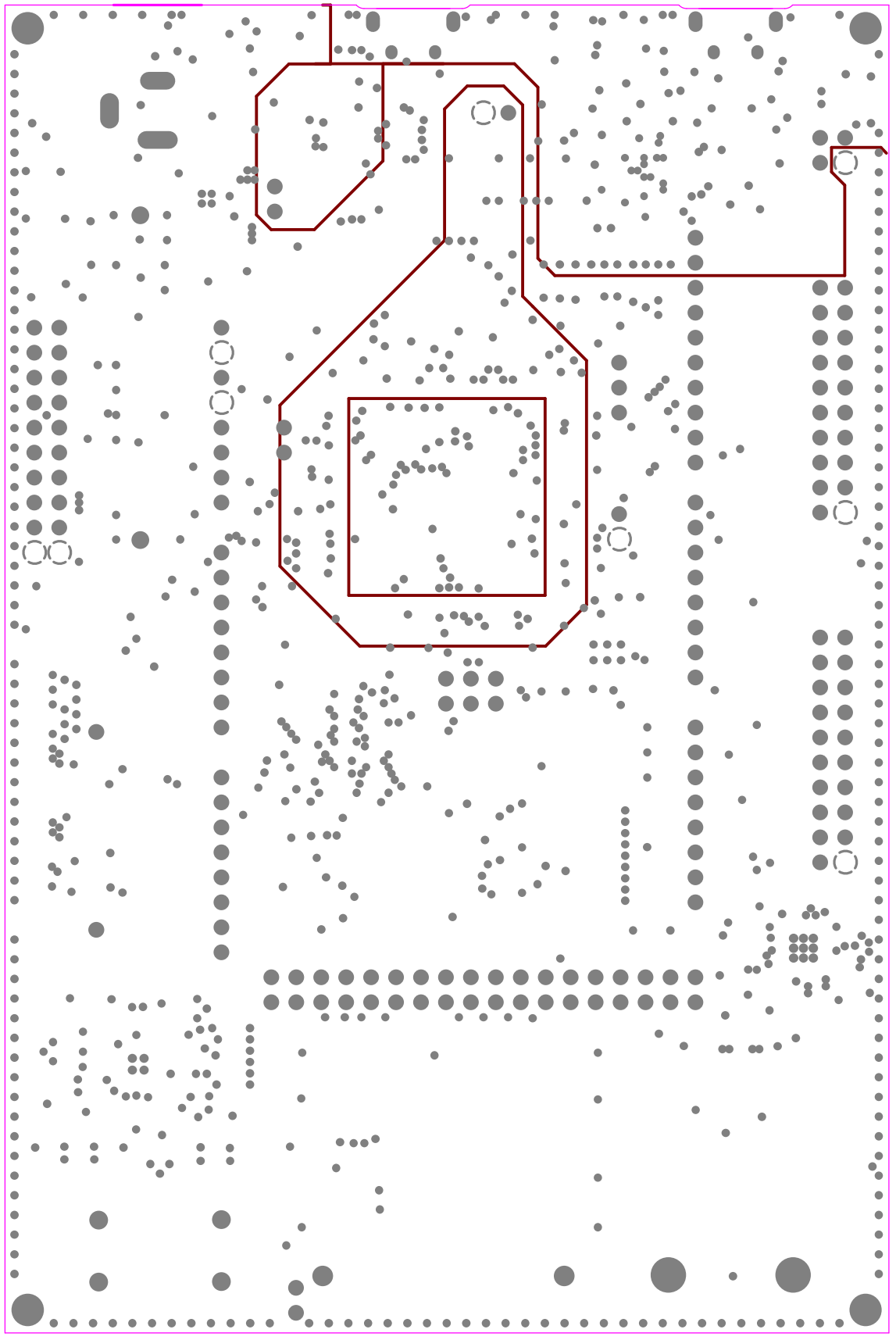
- PD26
- 3V3
- PC31
- 3V3
- PA19
- PD30
- PC13
- PE00
- PE03
- PE04
- PD24
- PA10
- PA22
- PE05
- PB13
- PD00
- PB03
- PB02

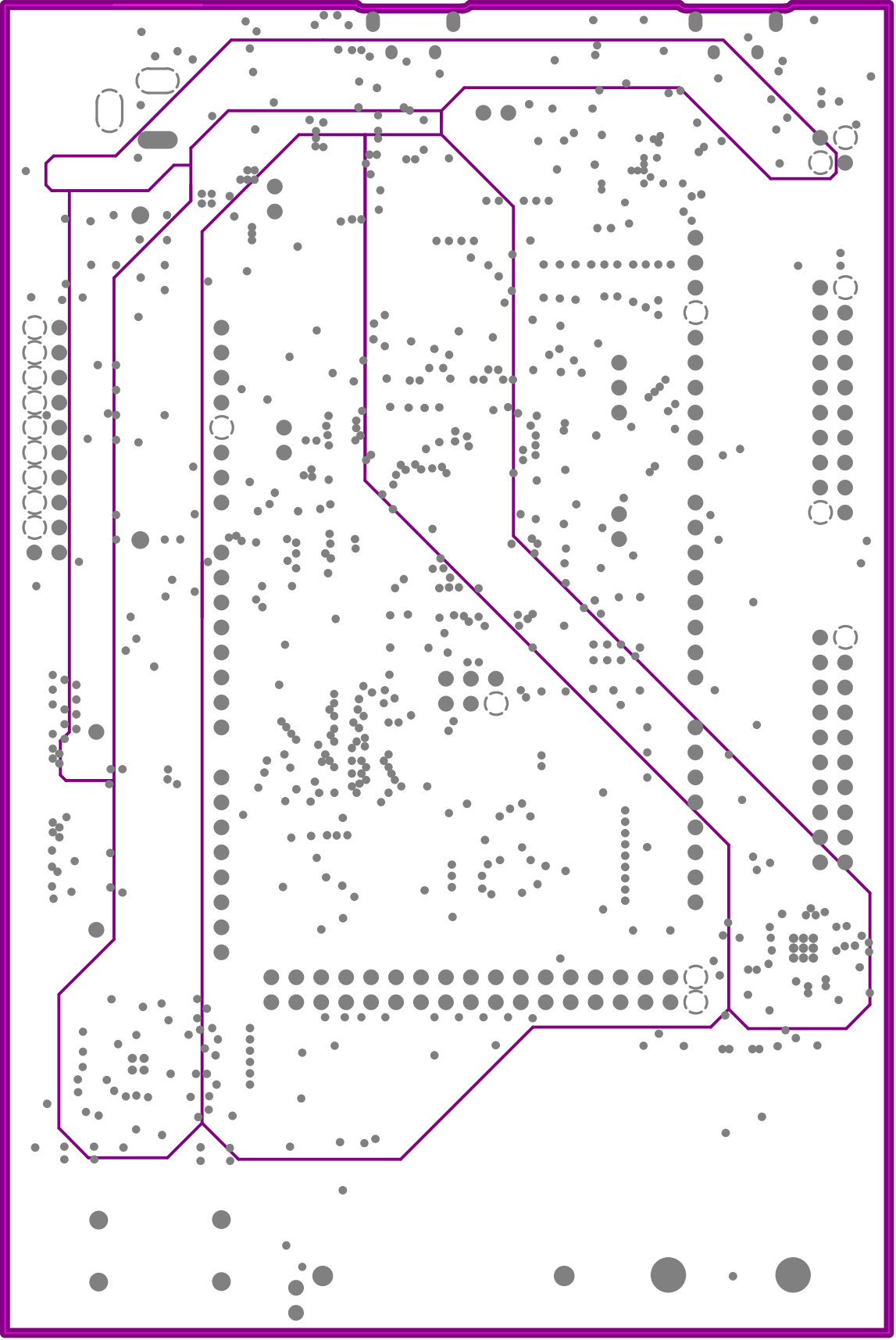


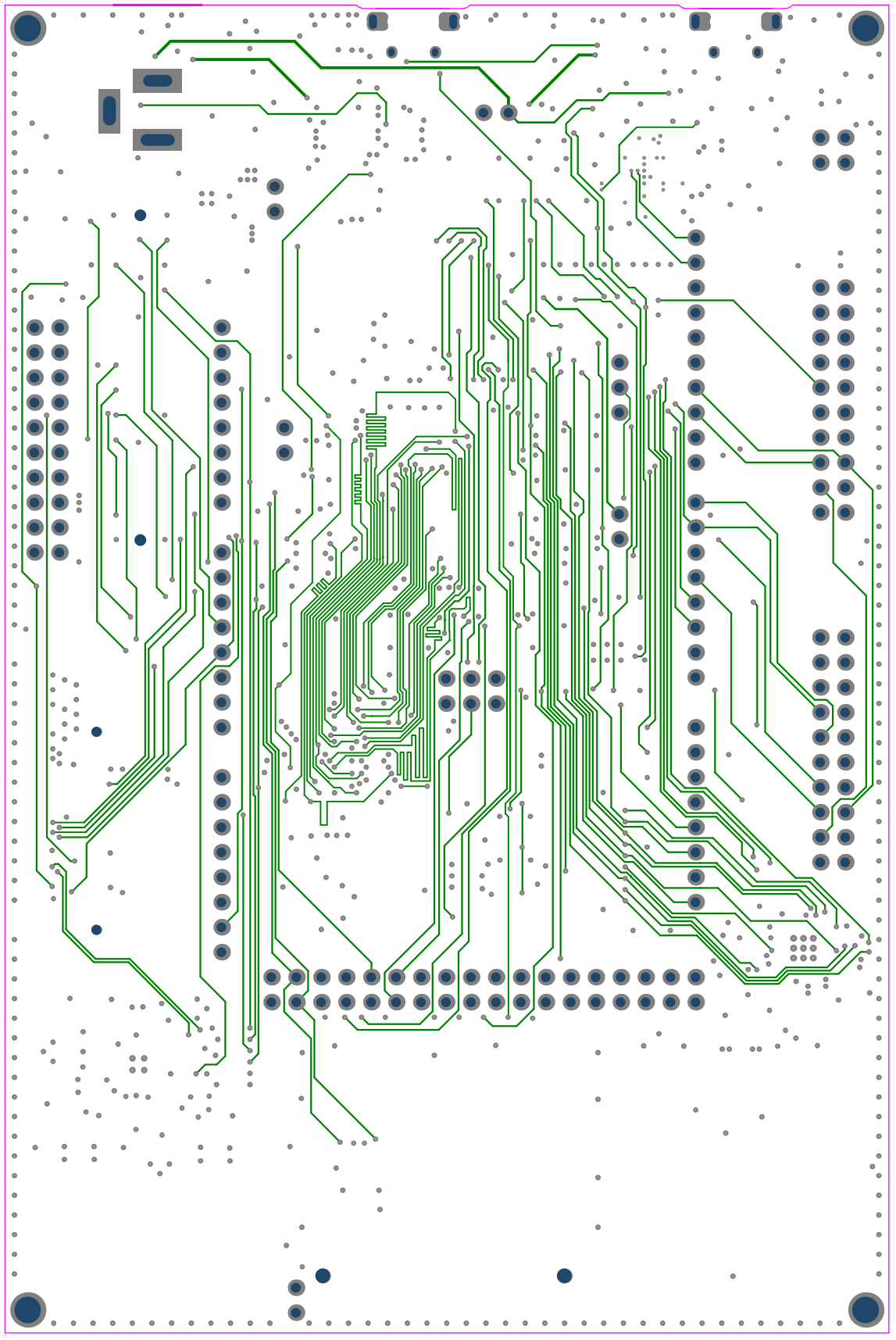


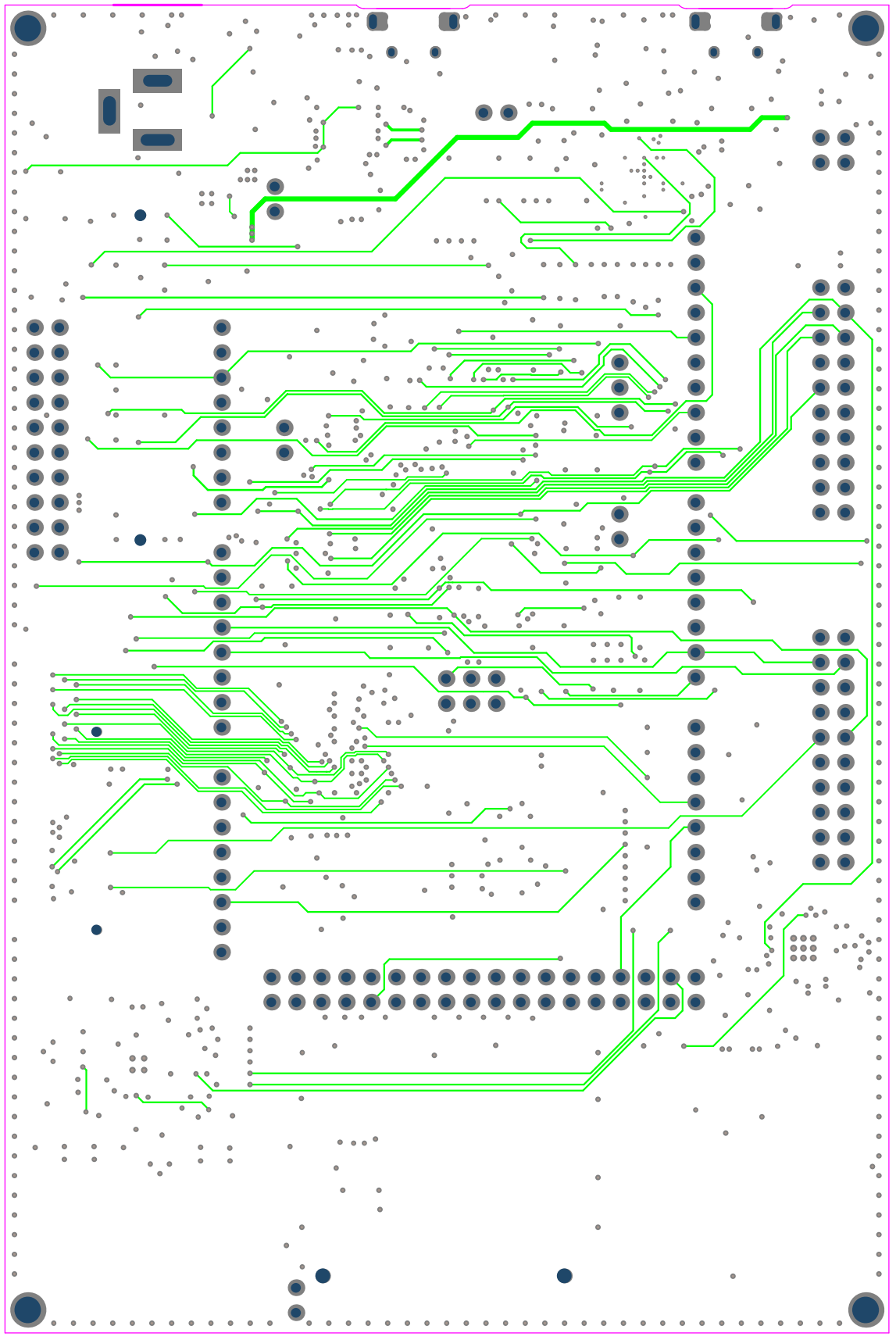


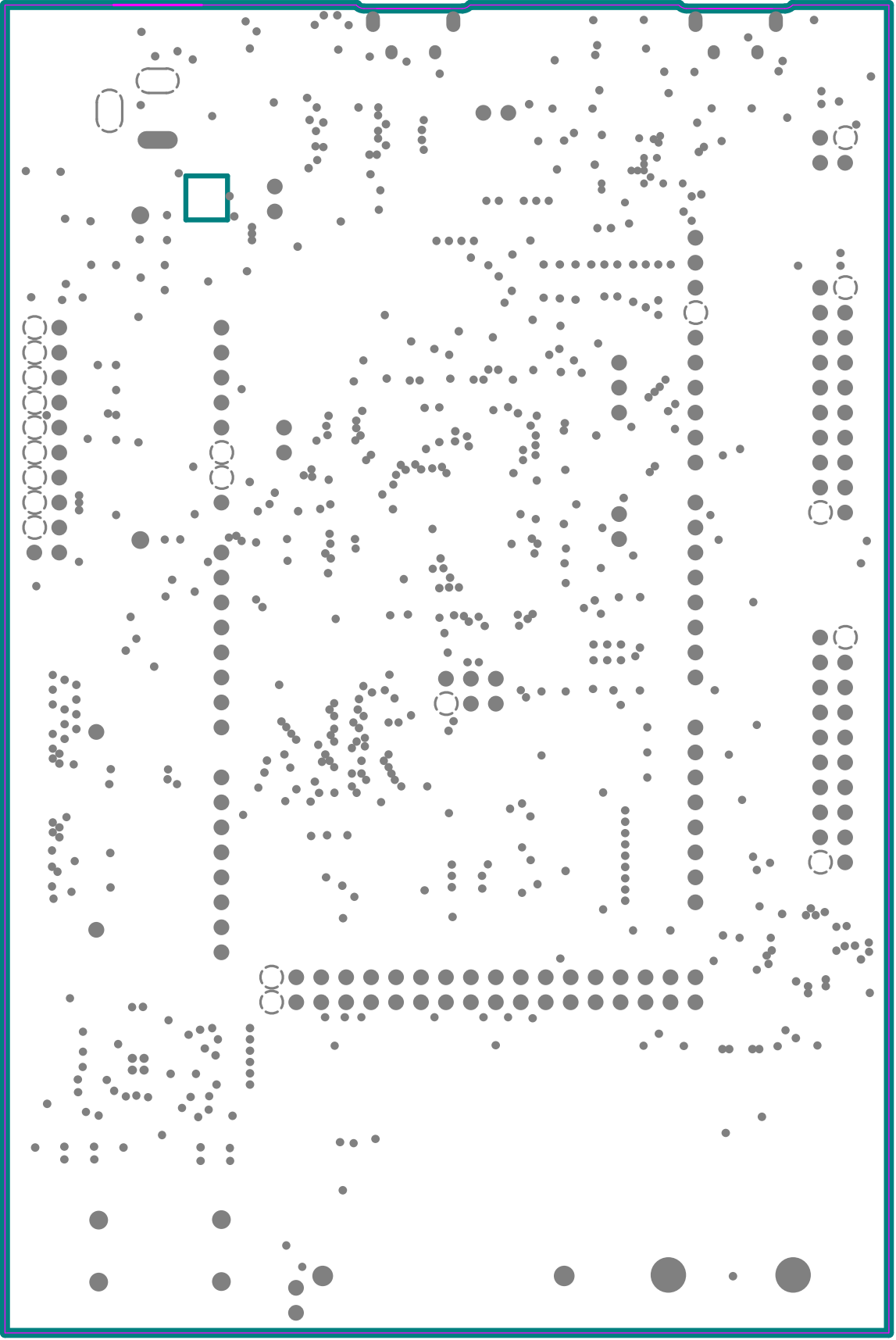




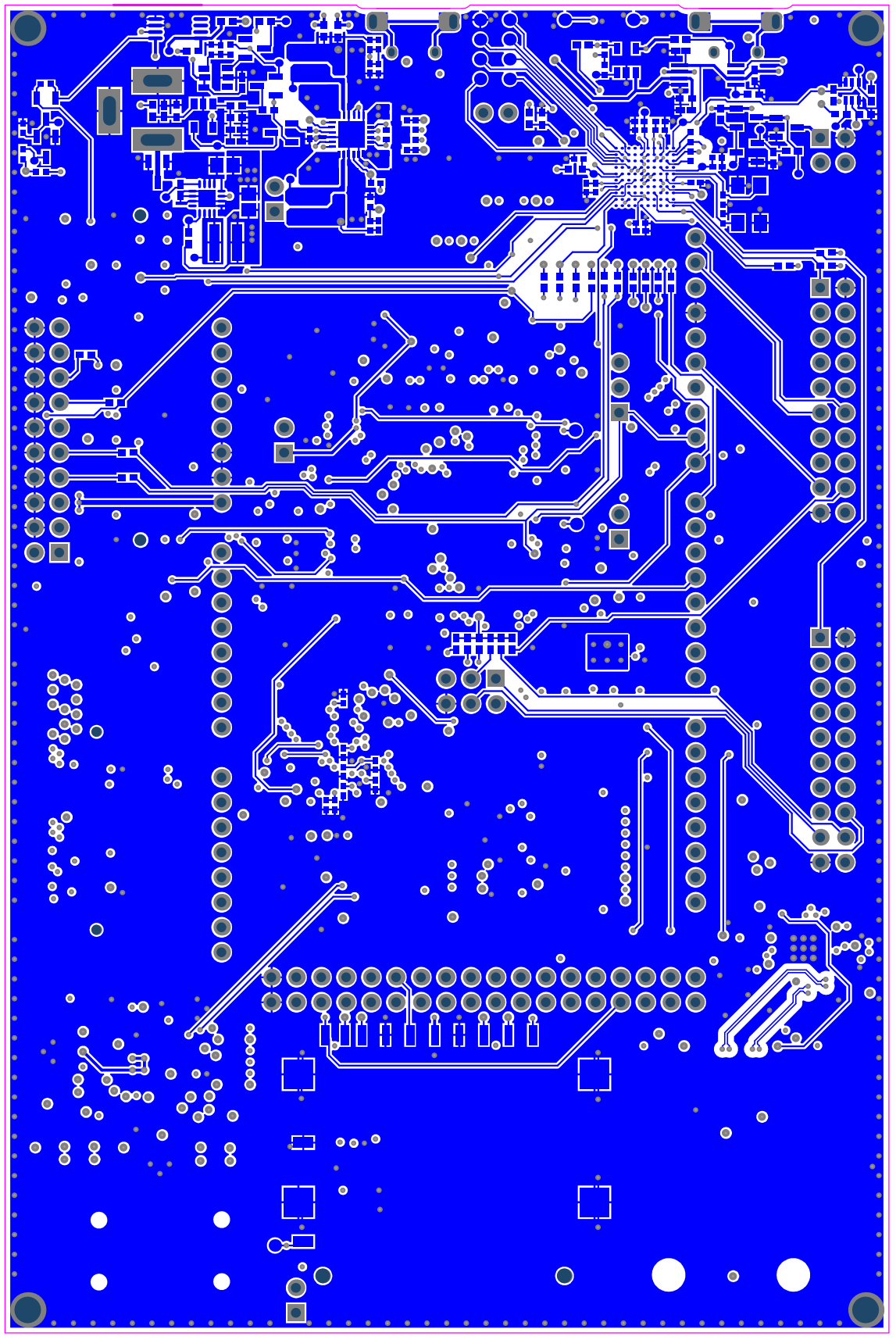


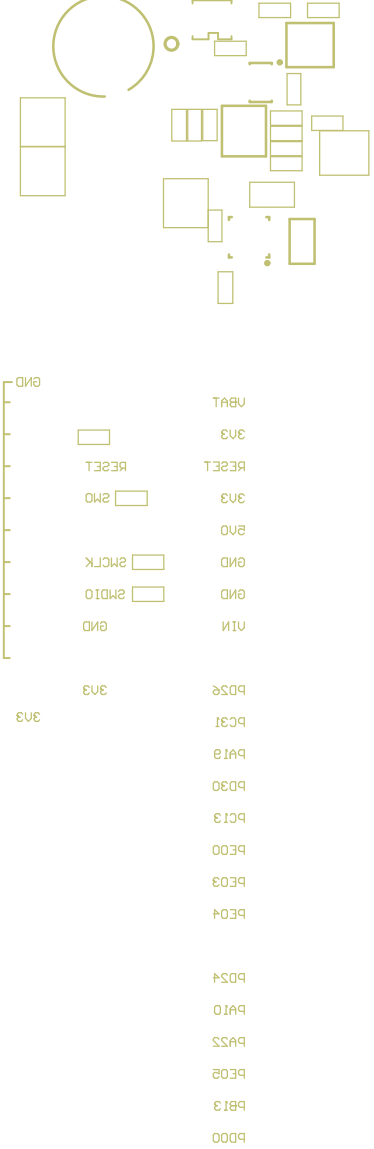
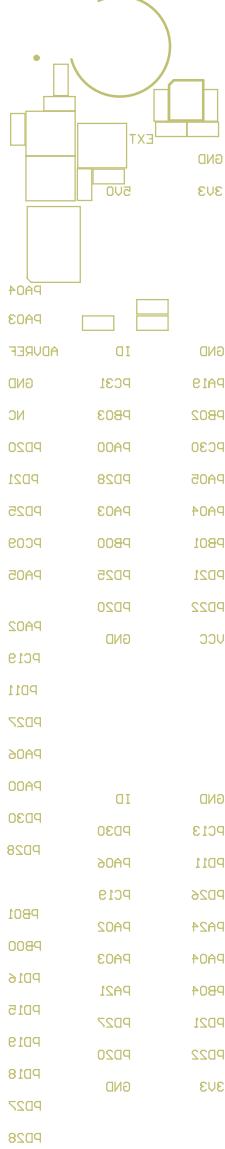




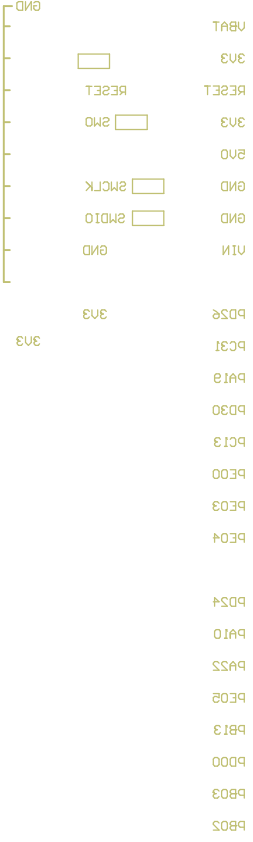








EXTENSION HEADER	EXPLAINED PRO
GND	ID
VCC	GND
SP1_MISO	SP1_MISO
SP1_MOSI	SP1_MOSI
UART_RX	UART_RX
UART_TX	UART_TX
TWI_SCL	TWI_SDA
SP1_SS_B	IRQ
PWM+	PWM+
GPIO1	GPIO1
ADC-	ADC+
GND	ID



TMS

TDI

RST

BOOT

# Component list

Top Level Schematics

Source Data From:

SAMV71\_Xplained\_Ultra\_PjPCB

Project:

SAMV71\_Xplained\_Ultra\_PjPCB

Variant:

Default\_assembly

Report Date: 16.03.2015  
Print Date: 16.03.2015

15.02.29  
14.55.47



RefDes	Designator	Quantity	Value	Manufacturer	MPN	Description
Filled	C100, C101, C103	3	22uF/10V	tk	C2012XSR1A200M220	Ceramic capacitor: SMD0805_XSR_10V_A020%
Filled	C1000	1	4.7uF	Murata	GRM21BR1047KA1L	Ceramic capacitor: SMD0805_XSR_20V_+10%
Filled	C101	1	15u	Murata	GRM21BR1010K7A7L	Ceramic capacitor: SMD0805_XSR_25V_+10%
Filled	C102	3	100nF			Ceramic capacitor: SMD0402_XTR_50V_+10%
Filled	C103	1	100nF			Electro Double Layer (Super) capacitor: 100uF_SMD_10.5mm diameter_C20E1SR
Filled	C104	1	10n			Ceramic capacitor: SMD0402_XTR_25V_+10%
Filled	C108, C109, C101, C104, C108, C200, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C200, C211, C213, C214, C215, C216, C217, C218, C200, C211, C213, C214, C215, C216, C217, C218, C200, C211, C213, C214, C215, C216, C217, C218, C200, C211, C213, C214, C215, C216, C217, C218, C200, C211, C213, C214, C215, C216, C217, C218	43	100n	Samt	CD4022T046K4R4CTU	Ceramic capacitor: SMD0402_XTR_10V_+10%
Filled	C107, C098, C811, C817, C819, C098, C099	7	4.7uF	tk	C108XSR1A47K	Ceramic capacitor: SMD0805_XSR_10V_10% (d631036)
Filled	C108, C109, C110, C111, C093, C094, C095, C096, C097, C098, C099, C100	9	2.2uF		CD4022C25MPCRA	Ceramic capacitor: SMD0402_XTR_6.3V_+20%
Filled	C112, C113, C115, C117, C122	5	10uF	Murata	GRM21BR1A106KE1L	Ceramic capacitor: SMD0805_XSR_10V_10% (d419441)
Filled	C114	1	82p			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C118	1	35p			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C119, C140	2	1uF	AVX	9402ZV08KATZA	Ceramic capacitor: SMD0402_XTR_50V_+10%
Filled	C123, C085, C096, C097, C098, C099, C100	6	100n	Samt	CD4022T046K4R4CTU	Ceramic capacitor: SMD0402_XTR_10V_+10%
Filled	C123, C101	2	15u			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C125	1	2.2uF	Samt	T4644ZD910A1	Capacitor: FeedBack: 10V_2.2uF_10%_ESR_4.5mm
Filled	C126, C108, C102	3	10uF	Murata	GRM21BR1A106KE1L	Ceramic capacitor: SMD0805_XSR_10V_10% (d419441)
Filled	C129, C102	2	15u			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C300, C101	2	4.7uF			Ceramic capacitor: SMD0402_NFP_50V_+10% (d4328F)
Filled	C302, C303	2	15u			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C126, C108, C102	3	10uF	Murata	GRM21BR1A106KE1L	Ceramic capacitor: SMD0805_XSR_10V_10% (d419441)
Filled	C129, C102	2	15u			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C300, C101	2	4.7uF			Ceramic capacitor: SMD0402_NFP_50V_+10% (d4328F)
Filled	C126, C108, C102	3	10uF	Murata	GRM21BR1A106KE1L	Ceramic capacitor: SMD0805_XSR_10V_10% (d419441)
Filled	C129, C102	2	15u			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C125, C101	2	2.2uF	AVX	CD4022T046K4R4CTU	Ceramic capacitor: SMD0402_XTR_10V_+10%
Filled	C126, C108, C102	3	10uF	Murata	GRM21BR1A106KE1L	Ceramic capacitor: SMD0805_XSR_10V_10% (d419441)
Filled	C129, C102	2	15u			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C125, C101	2	2.2uF	AVX	CD4022T046K4R4CTU	Ceramic capacitor: SMD0402_XTR_10V_+10%
Filled	C126, C108, C102	3	10uF	Murata	GRM21BR1A106KE1L	Ceramic capacitor: SMD0805_XSR_10V_10% (d419441)
Filled	C129, C102	2	15u			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C125, C101	2	2.2uF	AVX	CD4022T046K4R4CTU	Ceramic capacitor: SMD0402_XTR_10V_+10%
Filled	C126, C108, C102	3	10uF	Murata	GRM21BR1A106KE1L	Ceramic capacitor: SMD0805_XSR_10V_10% (d419441)
Filled	C129, C102	2	15u			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C125, C101	2	2.2uF	AVX	CD4022T046K4R4CTU	Ceramic capacitor: SMD0402_XTR_10V_+10%
Filled	C126, C108, C102	3	10uF	Murata	GRM21BR1A106KE1L	Ceramic capacitor: SMD0805_XSR_10V_10% (d419441)
Filled	C129, C102	2	15u			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C125, C101	2	2.2uF	AVX	CD4022T046K4R4CTU	Ceramic capacitor: SMD0402_XTR_10V_+10%
Filled	C126, C108, C102	3	10uF	Murata	GRM21BR1A106KE1L	Ceramic capacitor: SMD0805_XSR_10V_10% (d419441)
Filled	C129, C102	2	15u			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C125, C101	2	2.2uF	AVX	CD4022T046K4R4CTU	Ceramic capacitor: SMD0402_XTR_10V_+10%
Filled	C126, C108, C102	3	10uF	Murata	GRM21BR1A106KE1L	Ceramic capacitor: SMD0805_XSR_10V_10% (d419441)
Filled	C129, C102	2	15u			Ceramic capacitor: SMD0402_NFP_50V_+5%
Filled	C125, C101	2	2.2uF	AVX	CD4022T046K4R4CTU	Ceramic capacitor: SMD0402_XTR_10V_+10%

Approved

Notes