UM1855
User manual

Evaluation board with STM32L476ZGT6 MCU

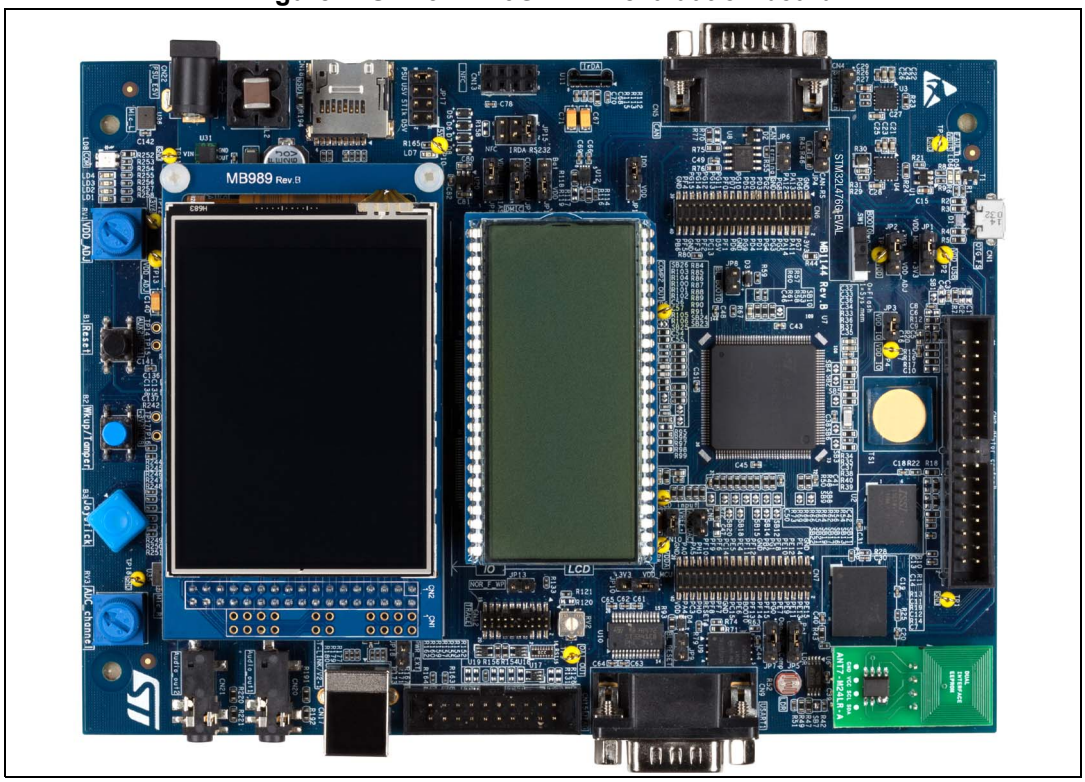
Introduction

The STM32L476G-EVAL evaluation board is designed as complete demonstration and development platform for STMicroelectronics ARM® Cortex®-M4-core-based STM32L476ZGT6 microcontroller with three I²C buses, three SPI and six USART ports, CAN port, SWPMI, two SAI ports, 12-bit ADC, 12-bit DAC, LCD driver, internal 128-Kbyte SRAM and 1-Mbyte Flash memory, Quad-SPI port, touch sensing capability, USB OTG FS port, LCD controller, flexible memory controller (FMC), JTAG debug port. STM32L476G-EVAL, shown in *Figure 1*(1), can be used as reference design for user application development, although it is not considered as final application.

A full range of hardware features on the board helps users evaluate all on-board peripherals such as USB, USART, digital microphones, ADC and DAC, dot-matrix TFT LCD, LCD glass module, IrDA, LDR, SRAM, NOR Flash memory device, Quad-SPI Flash memory device, microSD card, sigma-delta modulators, smartcard with SWP, CAN transceiver, EEPROM, RF-EEPROM. Extension headers allow connecting daughterboards or wrapping boards.

ST-LINK/V2-1 in-circuit debugger and flashing facility is integrated on the mainboard.

Figure 1. STM32L476G-EVAL evaluation board



1. Picture not contractual.

Contents

List of tables

List of figures

1 Overview

1.1 Features

- STM32L476ZGT6 microcontroller with 1-Mbyte Flash memory and 128-Kbyte RAM
- four power supply options: power jack, ST-LINK/V2-1 USB connector, USB OTG FS connector, daughterboard
- microcontroller supply voltage: 3.3 V or range from 1.71 V to 3.6 V
- two MEMS digital microphones
- two stereo audio headphones jack outputs with independent audio content
- slot for microSD card supporting SD, SDHC, SDXC
- 4-Gbyte microSD card bundled
- 16-Mbit (1M x 16 bit) SRAM device
- 128-Mbit (8M x 16 bit) NOR Flash memory device
- 256-Mbit Quad-SPI Flash memory device with double transfer rate (DTR) support
- RF-EEPROM with I²C bus
- EEPROM supporting 1 MHz I²C-bus communication speed
- RS-232 port configurable for communication or MCU flashing
- IrDA transceiver
- USB OTG FS Micro-AB port
- CAN 2.0A/B-compliant port
- joystick with four-way controller and selector
- reset and wake-up / tamper buttons
- touch-sensing button
- light-dependent resistor (LDR)
- potentiometer
- coin battery cell for power backup
- LCD glass module daughterboard (MB979) with 40x8-segment LCD driven directly by STM32L476ZGT6
- 2.8-inch 320x240 dot-matrix color TFT LCD panel with resistive touchscreen
- smartcard connector and SWP support
- NFC transceiver connector
- connector for ADC input and DAC output
- power-metering demonstration with dual-channel sigma-delta modulator
- PT100 thermal sensor with dual-channel sigma-delta modulator
- MCU current consumption measurement circuit
- access to comparator and operational amplifier of STM32L476ZGT6
- extension connector for motor control module
- JTAG/SWD, ETM trace debug support, user interface through USB virtual COM port, embedded ST-LINK/V2-1 debug and flashing facility
- extension connector for daughterboard

1.2 Demonstration software

Demonstration software is preloaded in the STM32L476ZGT6 Flash memory, for easy demonstration of the device peripherals in stand-alone mode. For more information and to download the latest available version, refer to the STM32L476G-EVAL demonstration software available on *www.st.com*.

1.3 Order code

To order the evaluation board based on the STM32L476ZGT6 MCU, use the order code STM32L476G-EVAL.

1.4 Unpacking recommendations

Before the first use, make sure that, no damage occurred to the board during shipment and no socketed components are loosen in their sockets or fallen into the plastic bag.

In particular, pay attention to the following components:

1. quartz crystal (X2 position)
2. microSD card in its CN18 receptacle
3. RF-EEPROM board (ANT7-M24LR-A) in its CN3 connector

For product information related with STM32L476ZGT6 microcontroller, visit *www.st.com*.

2 Hardware layout and configuration

The STM32L476G-EVAL evaluation board is designed around STM32L476ZGT6 target microcontroller in LQFP 144-pin package. *Figure 2* illustrates STM32L476ZGT6 connections with peripheral components. *Figure 3* shows the location of main components on the evaluation board.

Figure 2. STM32L476G-EVAL hardware block diagram

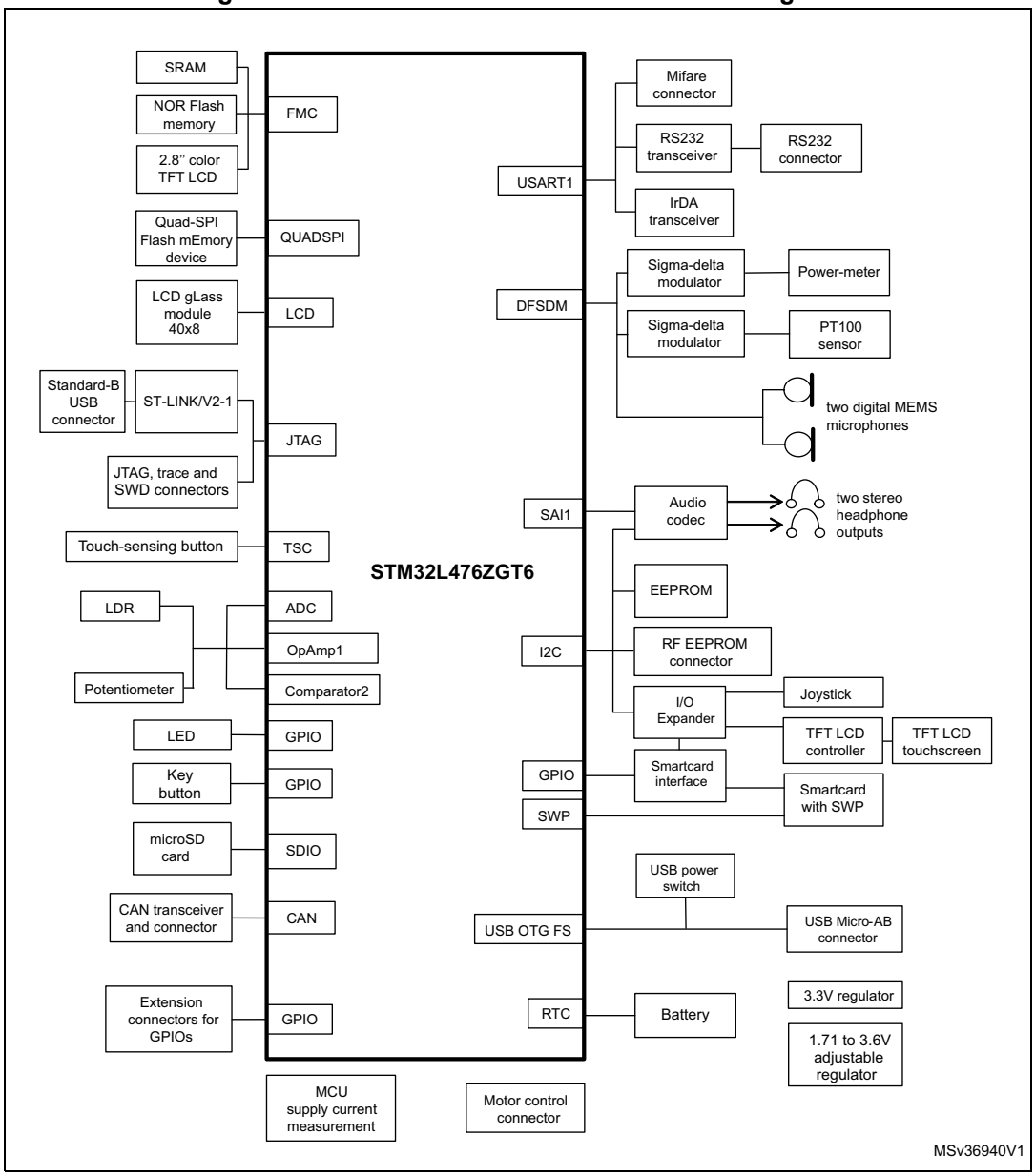
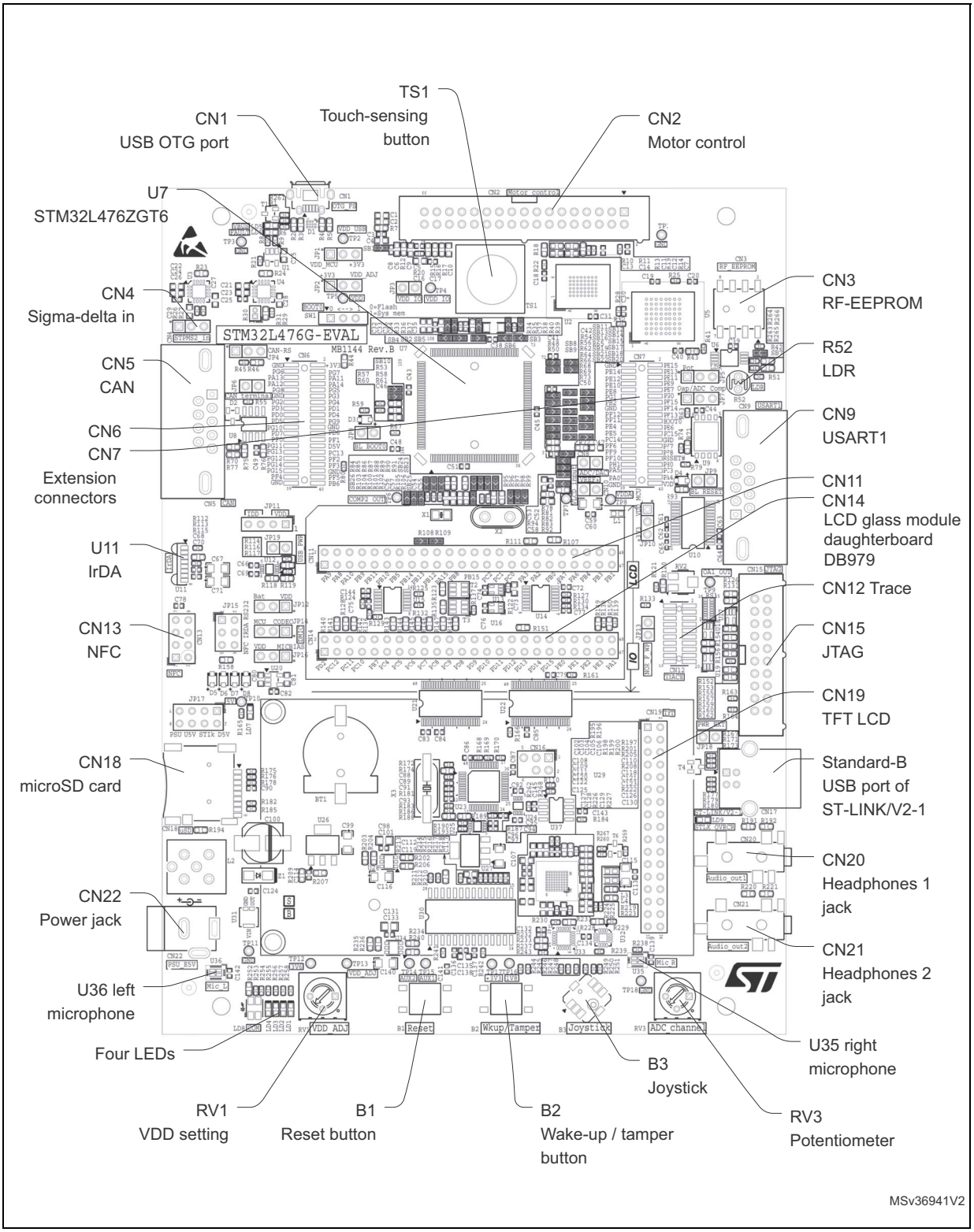


Figure 3. STM32L476G-EVAL main component layout



2.1 ST-LINK/V2-1

ST-LINK/V2-1 facility for debug and flashing of STM32L476ZGT6, is integrated on the STM32L476G-EVAL evaluation board.

Compared to ST-LINK/V2 stand-alone tool available from STMicroelectronics, ST-LINK/V2-1 offers new features and drops some others.

New features:

- USB software re-enumeration
- Virtual COM port interface on USB
- Mass storage interface on USB
- USB power management request for more than 100mA power on USB

Features dropped:

- SWIM interface

The USB connector CN17 can be used to power STM32L476G-EVAL regardless of ST-LINK/V2-1 facility use for debugging or for flashing STM32L476ZGT6. This holds also when ST-LINK/V2 stand-alone tool is connected to CN12 or CN15 connector and used for debugging or flashing STM32L476ZGT6. *Section 2.3* provides more detail on powering STM32L476G-EVAL.

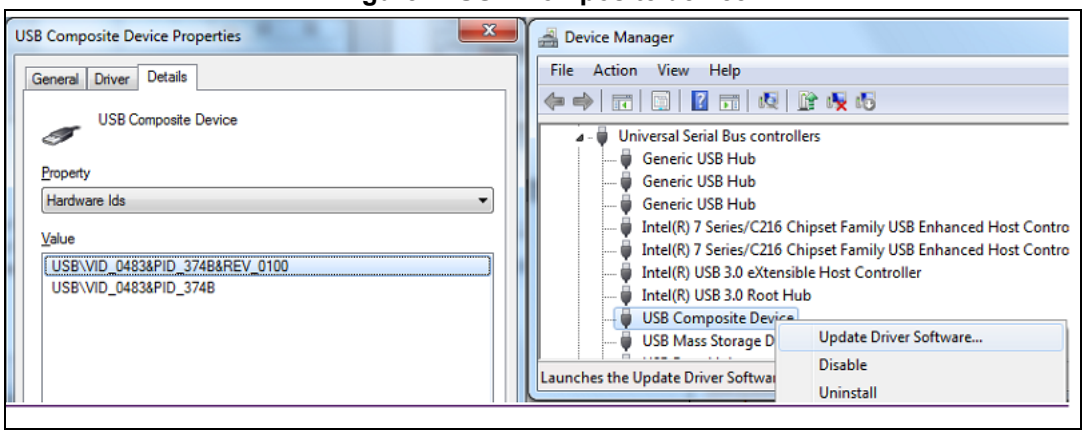
For full detail on both versions of the debug and flashing tool, the stand-alone ST-LINK/V2 and the embedded ST-LINK/V2-1, refer to *www.st.com*.

2.1.1 Drivers

Before connecting STM32L476G-EVAL to a Windows 7, Windows 8 or Windows XP PC via USB, a driver for ST-LINK/V2-1 must be installed. It can be downloaded from *www.st.com*.

In case the STM32L476G-EVAL evaluation board is connected to the PC before installing the driver, the Windows device manager may report some USB devices found on STM32L476G-EVAL as “Unknown”. To recover from this situation, after installing the dedicated driver downloaded from *www.st.com*, the association of “Unknown” USB devices found on STM32L476G-EVAL to this dedicated driver must be updated in the device manager manually. It is recommended to proceed using USB Composite Device line, as shown in *Figure 4*.

Figure 4. USB Composite device



2.1.2 ST-LINK/V2-1 firmware upgrade

For its own operation, ST-LINK/V2-1 employs a dedicated MCU with Flash memory. Its firmware determines ST-LINK/V2-1 functionality and performance. The firmware may evolve during the life span of STM32L476G-EVAL to include new functionality, fix bugs or support new target microcontroller families. It is therefore recommended to keep ST-LINK/V2-1 firmware up to date. The latest version is available from *www.st.com*.

2.2 ETM Trace

The connector CN12 can output trace signals used for debug. By default, the evaluation board is configured such that, STM32L476ZGT6 signals PE2 through PE5 are not connected to trace outputs Trace_D0, Trace_D1, Trace_D2, Trace_D3 and Trace_CK of CN12. They are used for other functions.

Table 1 shows the setting of configuration elements to shunt PE2, PE3, PE4 and PE5 MCU ports to CN12 connector, to use them as debug trace signals.

Table 1. Setting of configuration elements for trace connector CN12

Element	Setting	Use of PE2, PE3, PE4, PE5 terminals of STM32L476ZGT6
R103 SB26	R103 in SB26 open	**Default setting**. PE2 connected to LCDSEG38 and memory address line A23.
	R103 out SB26 closed	PE2 connected to TRACE_CK on CN12. A23 pulled down.
R104	R104 in	**Default setting**. PE3 connected to LCDSEG39 and memory address line A19.
	R104 out	PE3 connected to TRACE_D0 on CN12. A19 pulled down.
R84 SB40	R84 in SB40 open	**Default setting**. PE4 connected to memory address line A20.
	R84 out SB40 closed	PE4 connected to TRACE_D1 on CN12. A20 pulled down.
R85 SB38	R85 in SB38 open	**Default setting**. PE5 connected to memory address line A21.
	R85 out SB38 closed	PE5 connected to TRACE_D2 on CN12. A21 pulled down.
R86 SB39	R86 in SB39 open	**Default setting**. PE6 is used for address bit A22.
	R86 out SB39 closed	PE6 connected to TRACE_D3 on CN12. A22 pulled down.

Warning: Enabling the CN12 trace outputs through hardware modifications described in *Table 1* results in reducing the memory address bus width to 19 address lines and so the addressable space to 512 Kwords of 16 bits. As a consequence, the on-board SRAM and NOR Flash memory usable capacity is reduced to 8 Mbits.

2.3 Power supply

STM32L476G-EVAL evaluation board is designed to be powered from 5 V DC power source. It incorporates a precise polymer Zener diode (Poly-Zen) protecting the board from damage due to wrong power supply. One of the following four 5V DC power inputs can be used, upon an appropriate board configuration:

- Power jack CN22, marked PSU_E5V on the board. A jumper must be placed in PSU location of JP17. The positive pole is on the center pin as illustrated in *Figure 5*.
- Standard-B USB receptacle CN17 of ST-LINK/V2-1, offering enumeration feature described in *Section 2.3.1*.
- Micro-AB USB receptacle CN1 of USB OTG interface, marked OTG_FS on the board. Up to 500mA can be supplied to the board in this way.
- Pin 28 of CN6 extension connector for custom daughterboards, marked D5V on the board.

No external power supply is provided with the board.

LD7 red LED turns on when the voltage on the power line marked as +5V is present. All supply lines required for the operation of the components on STM32L476G-EVAL are derived from that +5V line.

Table 2 describes the settings of all jumpers related with powering STM32L476G-EVAL and extension board. VDD_MCU is STM32L476ZGT6 digital supply voltage line. It can be connected to either fixed 3.3 V or to an adjustable voltage regulator controlled with RV1 potentiometer and producing a range of voltages between 1.71 V and 3.6 V.

2.3.1 Supplying the board through ST-LINK/V2-1 USB port

To power STM32L476G-EVAL in this way, the USB host (a PC) gets connected with the STM32L476G-EVAL board's Standard-B USB receptacle, via a USB cable. This event starts the USB enumeration procedure. In its initial phase, the host's USB port current supply capability is limited to 100 mA. It is enough because only ST-LINK/V2-1 part of STM32L476G-EVAL draws power at that time. If the jumper header JP18 is open, the U37 ST890 power switch is set to OFF position, which isolates the remainder of STM32L476G-EVAL from the power source. In the next phase of the enumeration procedure, the host PC informs the ST-LINK/V2-1 facility of its capability to supply up to 300 mA of current. If the answer is positive, the ST-LINK/V2-1 sets the U37 ST890 switch to ON position to supply power to the remainder of the STM32L476G-EVAL board. If the PC USB port is not capable of supplying up to 300 mA of current, the CN22 power jack can be used to supply the board.

The ST890 power switch protects the host's USB port against current demand exceeding 600 mA, should a short-circuit occur on the board. In such an event, the LD9 LED lights on.

The STM32L476G-EVAL board can also be supplied from a USB power source not supporting enumeration, such as a USB charger. In this particular case, the JP18 header must be fitted with a jumper as shown in *Table 2*. ST-LINK/V2-1 turns the ST890 power switch ON regardless of enumeration procedure result and passes the power unconditionally to the board.

The LD7 red LED turns on whenever the whole board is powered.

2.3.2 Using ST-LINK/2-1 along with powering through CN22 power jack

It can happen that the board requires more than 300 mA of supply current. It cannot be supplied from host PC connected to ST-LINK/2-1 USB port for debugging or flashing STM32L476ZGT6. In such a case, the board can be supplied through CN22 (marked PSU _E5V on the board).

To do this, it is important to power the board **before** connecting it with the host PC, which requires the following sequence to be respected:

1. set the jumper in JP15 header in PSU position
2. connect the external 5 V power source to CN22
3. check the red LED LD7 is turned on
4. connect host PC to USB connector CN17

In case the board demands more than 300 mA and the host PC is connected via USB before the board is powered from CN22, there is a risk of the following events to occur, in the order of severity:

1. The host PC is capable of supplying 300 mA (the enumeration succeeds) but it does not incorporate any over-current protection on its USB port. It is damaged due to over-current.
2. The host PC is capable of supplying 300 mA (the enumeration succeeds) and it has a built-in over-current protection on its USB port, limiting or shutting down the power out of its USB port when the excessive current demand from STM32L476G-EVAL is detected. This causes an operating failure to STM32L476G-EVAL.
3. The host PC is not capable of supplying 300 mA (the enumeration fails) so ST-LINK/V2-1 does not supply the remainder of STM32L476G-EVAL from its USB port VBUS line.

Figure 5. CN22 power jack polarity

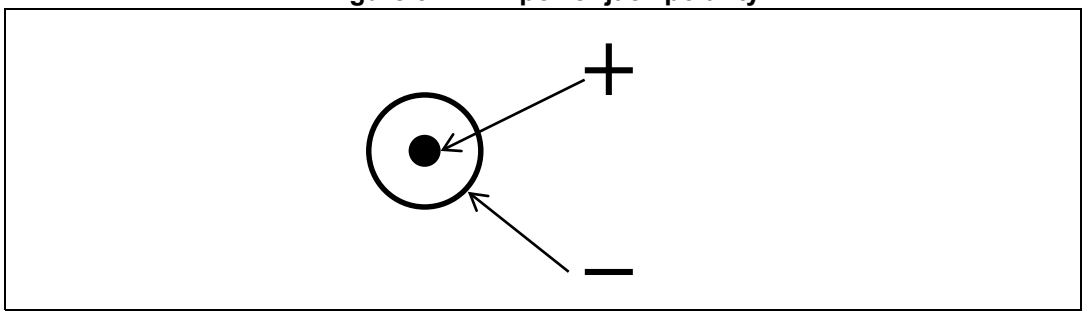


Table 2. Power-supply-related jumper settings

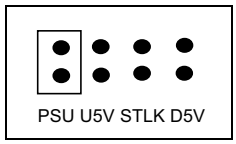
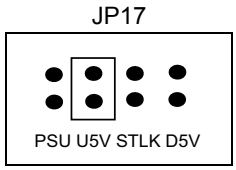
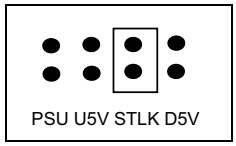
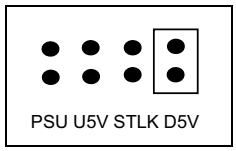
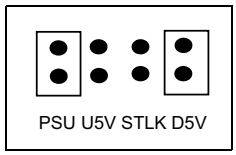
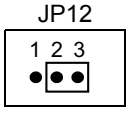
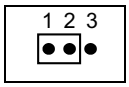
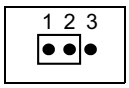
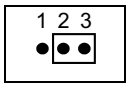
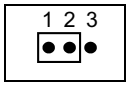
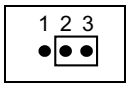
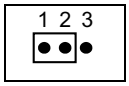
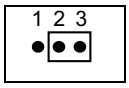
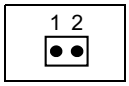
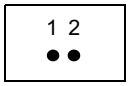
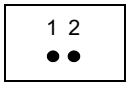
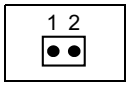
Jumper array	Jumper setting	Configuration
JP17 Power source selector	JP17 	STM32L476G-EVAL is supplied through **CN22 power jack** (marked PSU_E5V). CN6 extension connector does not pass the 5 V of STM32L476G-EVAL to daughterboard.
	JP17 	STM32L476G-EVAL is supplied through **CN1 Micro-AB USB connector**. CN6 extension connector does not pass the 5 V of STM32L476G-EVAL to daughterboard.
	JP17 	**Default setting**. STM32L476G-EVAL is supplied through **CN17 Standard-B USB connector**. CN6 extension connector does not pass the 5 V of STM32L476G-EVAL to daughterboard. Check JP18 setting in *Table 2*.
	JP17 	STM32L476G-EVAL is supplied through pin 28 of CN6 extension connector.
	JP17 	STM32L476G-EVAL is supplied through **CN22 power jack** (marked PSU_E5V). CN6 extension connector passes the 5 V of STM32L476G-EVAL to daughterboard. Make sure to disconnect from the daughterboard any power supply that could generate conflict with the power supply on CN22 power jack.
JP12 V_{bat} connection	JP12 	V_{bat} is connected to battery.
	JP12 	**Default setting**. V_{bat} is connected to V_{DD}.

Table 2. Power-supply-related jumper settings (continued)

Jumper array	Jumper setting	Configuration
JP2 VDD_MCU connection	JP2 	**Default setting**. VDD_MCU (VDD terminals of STM32L476ZGT6) is connected to fixed +3.3 V.
	JP2 	VDD_MCU is connected to voltage in the range from +1.71 V to +3.6 V, adjustable with potentiometer RV1.
JP10 VDDA connection	JP10 	**Default setting**. VDDA terminal of STM32L476ZGT6 is connected with VDD_MCU.
	JP10 	VDDA terminal of STM32L476ZGT6 is connected to +3.3 V.
JP1 VDD_USB connection	JP1 	**Default setting**. VDD_USB (VDDUSB terminal of STM32L476ZGT6) is connected with VDD_MCU.
	JP1 	VDD_USB is connected to +3.3V.
JP3 VDD_IO connection	JP3 	**Default setting**. VDD_IO (VDDIO2 terminals of STM32L476ZGT6) is connected with VDD_MCU
	JP3 	VDD_IO is open.
JP18 Powering through USB of ST-LINK/V2-1	JP18 	**Default setting**. Standard-B USB connector CN17 of ST-LINK/V2-1 can supply power to the STM32L476G-EVAL board remainder, depending on host PC USB port's powering capability declared in the enumeration.
	JP18 	Standard-B USB connector CN17 of ST-LINK/V2-1 supplies power to the STM32L476G-EVAL board remainder. Setting for powering the board through CN17 using USB charger.

2.4 Clock references

Two clock references are available on STM32L476G-EVAL for the STM32L476ZGT6 target microcontroller:

- 32.768 kHz crystal X1, for embedded RTC
- 8 MHz crystal X2, for main clock generator

The main clock can also be generated using an internal RC oscillator. The X2 crystal is in a socket. It can be removed when the internal RC oscillator is used.

Table 3. X1-crystal-related solder bridge settings

Solder bridge	Setting	Description
SB41	Open	**Default setting**. PC14-OSC32_IN terminal is not routed to extension connector CN7. X1 is used as clock reference.
	Closed	PC14-OSC32_IN is routed to extension connector CN7. R87 must be removed, for X1 quartz circuit not to disturb clock reference or source on daughterboard.
SB33	Open	**Default setting**. PC15-OSC32_OUT terminal is not routed to extension connector CN7. X1 is used as clock reference.
	Closed	PC15-OSC32_OUT is routed to extension connector CN7. R88 must be removed, for X1 quartz circuit not to disturb clock reference on daughterboard.

Table 4. X2-crystal-related solder bridge settings

Solder bridge	Setting	Configuration
SB24	Open	**Default setting**. PH0-OSC_IN terminal is not routed to extension connector CN7. X2 is used as clock reference.
	Closed	PH0-OSC_IN is routed to extension connector CN7. X2 and C54 must be removed, in order not to disturb clock reference or source on daughterboard.
SB23	Open	**Default setting**. PH1-OSC_OUT terminal is not routed to extension connector CN7. X2 is used as clock reference.
	Closed	PH1-OSC_OUT is routed to extension connector CN7. R95 must be removed, in order not to disturb clock reference or source on daughterboard.

2.5 Reset sources

Reset signal of the STM32L476G-EVAL board is active low.

Sources of reset are:

- reset button B1
- JTAG/SWD connector CN15 and ETM trace connector CN12 (reset from debug tools)
- through extension connector CN7, pin 32 (reset from daughterboard)
- ST-LINK/V2-1
- RS-232 connector CN9, terminal 8 (CTS signal), if JP9 is closed (open by default)

2.6 Boot

2.6.1 Boot options

After reset, the STM32L476ZGT6 MCU can boot from the following embedded memory locations:

- main (user, non-protected) Flash memory
- system (protected) Flash memory
- RAM, for debugging

The microcontroller is configured to one of the listed boot options by setting the STM32L476ZGT6 port BOOT0 level by the switch SW1 and by setting nBOOT1 bit of FLASH_OPTR option bytes register, as shown in *Table 5*. Depending on JP8, BOOT0 level can be forced high and, SW1 action overruled, by DSR line of RS-232 connector CN9, as shown in *Table 6*. This can be used to force the execution of bootloader and start user Flash memory flashing process (ISP) from RS-232 interface.

The option bytes of STM32L476ZGT6 and their modification procedure are described in the reference manual RM0351. The application note AN2606 details the bootloader mechanism and configurations.

Table 5. Boot selection switch

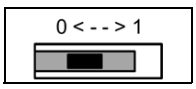
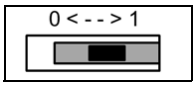
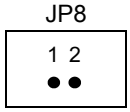
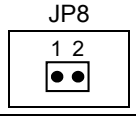
Switch	Setting	Description
SW1		**Default setting**. BOOT0 line is tied low. STM32L476ZGT6 boots from user Flash memory.
		BOOT0 line is tied high. STM32L476ZGT6 boots from system Flash memory (nBOOT1 bit of FLASH_OPTR register is set high) or from RAM (nBOOT1 is set low).

Table 6. Bootloader-related jumper setting

Jumper	Setting	Description
JP8		**Default setting**. BOOT0 level only depends on SW1 switch position
		BOOT0 can be forced high with terminal 6 of CN9 connector (RS-232 DSR line). This configuration is used to allow the device connected via RS-232 to initiate STM32L476ZGT6 flashing process.

2.6.2 Bootloader limitations

Boot from system Flash memory results in executing **bootloader** code stored in the system Flash memory protected against write and erase. This allows in-system programming (ISP), that is, flashing the MCU user Flash memory. It also allows writing data into RAM. The data come in via one of communication interfaces such as USART, SPI, I²C bus, USB or CAN.

Bootloader version can be identified by reading Bootloader ID at the address 0x1FFF6FFE.

The STM32L476ZGT6 part soldered on the STM32L476G-EVAL main board is marked with a date code corresponding to its date of manufacture. STM32L476ZGT6 parts with the date code prior or equal to week 22 of 2015 are fitted with **bootloader V 9.0** affected by the limitations to be worked around, as described hereunder. Parts with the date code starting week 23 of 2015 contain bootloader V9.2 in which the limitations no longer exist.

To locate the visual date code information on the STM32L476ZGT6 package, refer to its datasheet (DS10198) available on *www.st.com*, section Package Information. Date code related portion of the package marking takes Y WW format, where Y is the last digit of the year and WW is the week. For example, a part manufactured in week 23 of 2015 bares the date code 5 23.

Bootloader ID of the bootloader V 9.0 is 0x90.

The following limitations exist in the bootloader V 9.0:

1. **RAM data get corrupted when written via USART/SPI/I2C/USB interface**

Description:

Data write operation into RAM space via USART, SPI, I²C bus or USB results in wrong or no data written.

Workaround:

To correct the issue of wrong write into RAM, download STSW-STM32158 bootloader V 9.0 patch package from *www.st.com* and load "Bootloader V9.0 SRAM patch" to the MCU, following the information in readme.txt file available in the package.

2. **User Flash memory data get corrupted when written via CAN interface**

Description:

Data write operation into user Flash memory space via CAN interface results in wrong or no data written.

Workaround:

To correct the issue of wrong write into Flash memory, download STSW-STM32158 bootloader V 0.9 patch package from *www.st.com* and load "Bootloader V9.0 CAN patch" to the MCU, following the information in readme.txt file available in the package.

2.7 Audio

A codec connected to SAI interface of STM32L476ZGT6 supports TDM feature of the SAI port. TDM feature offers to STM32L476ZGT6 the capability to stream two independent stereo audio channels to two separate stereo analog audio outputs, simultaneously.

There are two digital microphones on board of STM32L476G-EVAL.

2.7.1 Digital microphones

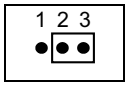
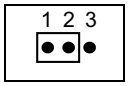
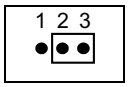
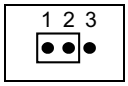
U35 and U36 on board of STM32L476G-EVAL are MP34DT01TR MEMS digital omni-directional microphones providing PDM (pulse density modulation) outputs. To share the same data line, their outputs are interlaced. The combined data output of the microphones is directly routed to STM32L476ZGT6 terminals, thanks to the integrated input digital filters. The microphones are supplied with programmable clock generated directly by STM32L476ZGT6.

As an option, the microphones can be connected to U29, Wolfson audio codec device, WM8994. In that configuration, U29 also supplies the PDM clock to the microphones.

Regardless of where the microphones are routed to, STM32L476ZGT6 or WM8994, they can be power-supplied from either VDD or MICBIAS1 output of the WM8994 codec device.

Table 7 shows settings of all jumpers associated with the digital microphones on the board.

Table 7. Digital microphone-related jumper settings

Jumper	Setting	Configuration
JP14	JP14 	**Default setting**. PDM clock for digital microphones comes from STM32L476ZGT6
	JP14 	PDM clock for digital microphones comes from WM8994 codec.
JP16	JP16 	**Default setting**. Power supply of digital microphones is VDD.
	JP16 	Power supply of digital microphones is generated by WM8994 codec.

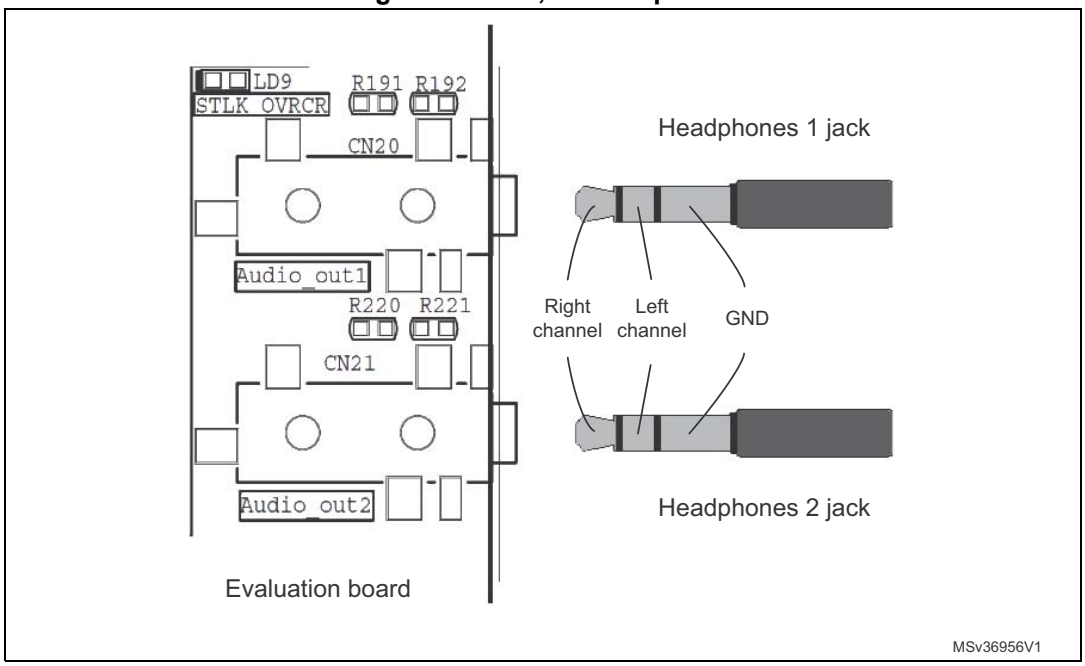
2.7.2 Headphones outputs

The STM32L476G-EVAL evaluation board can drive two sets of stereo headphones. Identical or different stereo audio content can be played back in each set of headphones. The STM32L476ZGT6 sends up to two independent stereo audio channels, via its SAI1 TDM port, to the WM8994 codec device. The codec device converts the digital audio stream to stereo analog signals. It then boosts them for direct drive of headphones connecting to 3.5 mm stereo jack receptacles on the board, CN20 for Audio-output1 and CN21 for Audio_output2. *Figure 6* shows a top view of the CN20 and CN21 headphones jack receptacles.

The CN21 jack takes its signal from the WM8994 codec device's output intended for driving an amplifier for loudspeakers. A hardware adaptation is incorporated on the board to make it compatible with a direct headphone drive. The adaptation consists of coupling capacitors blocking the DC component of the signal, attenuator and anti-pop resistors. The WM8994 codec device's loudspeaker output must be configured by software in linear mode called "class AB" and not in switching mode called "class D".

The I²C-bus address of WM8994 is 0b0011010.

Figure 6. CN20, CN21 top view



2.7.3 Limitations in using audio features

Due to the share of some terminals of STM32L476ZGT6 by multiple peripherals, the following limitations apply in using the audio features:

- If the SAI1_SDA is used as part of SAI1 port, it cannot be used as FMC_NWAIT signal for NOR Flash memory device. However, FMC_NWAIT is not necessary for operating the NOR Flash memory device. More details on FMC_NWAIT are available in *Section 2.22: NOR Flash memory device*.
- If the SAI1 port of STM32L476ZGT6 is used for streaming audio to the WM8994 codec IC, STM32L476ZGT6 cannot control the motor.
- If the digital microphones are attached to STM32L476ZGT6, the LCD glass module cannot be driven.

2.8 USB OTG FS port

The STM32L476G-EVAL board supports USB OTG full-speed (FS) communication.The USB OTG connector CN1 is of Micro-AB type.

2.8.1 STM32L476G-EVAL used as USB device

When a “USB host” connection to the CN1 Micro-AB USB connector of STM32L476G-EVAL is detected, the STM32L476G-EVAL board starts behaving as “USB device”. Depending on the powering capability of the USB host, the board can take power from VBUS terminal of CN1. In the board schematic diagrams, the corresponding power voltage line is called U5V. *Section 2.3* provides information on how to set associated jumpers for this powering option. The JP19 jumper must be left open to prevent STM32L476G-EVAL from sourcing 5 V to VBUS terminal, which would cause conflict with the 5 V sourced by the USB host. This may

happen if the PC6 GPIO is controlled by the software of STM32L476ZGT6 such that, it enables the output of U1 power switch.

2.8.2 STM32L476G-EVAL used as USB host

When a “USB device” connection to the CN1 Micro-AB USB connector is detected, the STM32L476G-EVAL board starts behaving as “USB host”. It sources 5 V on the VBUS terminal of CN1 Micro-AB USB connector to power the USB device. For this to happen, the STM32L476ZGT6 MCU sets the U1 power switch STMPS2151STR to ON state. The LD5 green LED marked VBUS indicates that the peripheral is supplied from the board. The LD6 red LED marked FAULT lights up if over-current is detected. The JP19 jumper must be closed to allow the PC6 GPIO to control the U1 power switch.
In any other STM32L476G-EVAL powering option, the JP19 jumper should be open, to avoid accidental damage caused to an external USB host.

2.8.3 Configuration elements related with USB OTG FS port

The following STM32L476ZGT6 terminals related with USB OTG FS port control are shared by other resources of the STM32L476G-EVAL board:

- PB12, used as USB over-current input (USBOTG_OVRCR signal); it is shared with SWP, touch sensing, LCD glass module and motor control resources
- PB13, used as USB power ready input (USBOTG_PRDY signal); it is shared with NFC, touch sensing and LCD glass module resources
- PC6, used as USB power switch control (USBOTG_PPWR signal); it is shared with touch sensing, LCD glass module and motor control

Configuration elements related with the USB OTG FS port, such as jumpers, solder bridges and zero-ohm resistors, shunt the shared ports toward different resources or determine the operating mode of the USB OTG FS port. By default, they are set such as to enable the USB OTG FS port operation where STM32L476G-EVAL plays USB device role and can be connected to a USB host. *Table 8* gives an overview of all configuration elements related with the USB OTG FS port. The LCD glass module daughterboard should be connected in I/O position.

USBOTG_OVRCR and USBOTG_PRDY signals, requiring the PB12 and PB13 ports of STM32L476ZGT6, are only exploited when STM32L476G-EVAL acts as USB host. That is why, the USB host function of STM32L476G-EVAL is exclusive with alternate functions also requiring PB12 and PB13 ports of STM32L476ZGT6 - NFC, touch sensing, motor control, SWP.

The PB12 and PB13 ports of STM32L476ZGT6 are not required for the USB OTG FS port operating as USB device.

Table 8. Configuration elements related with USB OTG FS port

Element	Setting	Description
JP19	Open	USB OTG FS port can be connected with a USB **host** and get power from it. If connected with USB device, STM32L476G-EVAL cannot supply power to it.
	Closed	**Default setting.** USB OTG FS port can be connected with a USB device and supply power to it. It must not be connected with USB host.

Table 8. Configuration elements related with USB OTG FS port (continued)

Element	Setting	Description
R36	In	**Default setting** PC6 is shunted to control the U1 power switch, transiting through the LCD glass module daughterboard connector. LCD glass module daughterboard should be in I/O position, with SB2 and SB27 open.
	Out	PC6 is disconnected from the LCD glass module daughterboard connector. It can be shunted to one of alternate resources, either touch sensing (SB2 closed) or motor control (SB27 closed).
R39	In	**Default setting**. PB12 receives USBOTG_OVRCR signal from U1 power switch, transiting through the LCD glass module daughterboard connector. SB3 should be open, R109 in, no smartcard in CN23 slot.
	Out	PB12 is disconnected from the LCD glass module daughterboard connector. It can be shunted to one of alternate resources, either touch sensing or motor control (SB3 closed).
R38	In	**Default setting**. PB13 receives USBOTG_PRDY signal from CN1 connector, transiting through the LCD glass module daughterboard connector. SB6 should be open and no daughterboard inserted in CN13 NFC connector.
	Out	PB13 s disconnected from the LCD glass module daughterboard connector. It can be shunted to touch sensing (SB6 closed).

2.8.4 Limitations in using USB OTG FS port

- The USB OTG FS port operation as USB host is exclusive with NFC, SWP, LCD glass module, touch sensing, motor control
- The USB OTG FS port operation as USB device is exclusive with LCD glass module, touch sensing, motor control

2.8.5 Operating voltage

The USB-related operating supply voltage of STM32L476ZGT6 (VDD_USB line) must be within the range from 3.0 V to 3.6 V.

2.9 RS-232 and IrDA ports

The STM32L476G-EVAL board offers one RS-232 communication port and one IrDA port.

2.9.1 RS-232 port

The RS-232 communication port uses the DE-9M 9-pole connector CN9. RX, TX, RTS and CTS signals of USART1 port of STM32L476ZGT6 are routed to CN9. Bootloader_RESET_3V3 and Bootloader_BOOT0_3V3 signals can also be routed to CN9, for ISP (in-system programming) support. To route Bootloader_RESET_3V3 to CN9, the R93 resistor must be removed and the JP9 jumper closed (open by default). To route Bootloader_BOOT0_3V3 to CN9, the JP8 jumper must be closed.

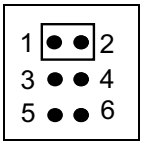
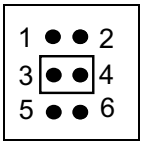
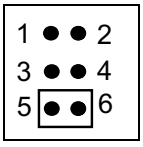
For configuration elements related with the RS-232 port operation, refer to *Table 6* and *Table 9*.

Section 2.10 brings information on using the LPUART port of STM32L476ZGT6 for RS-232, instead of its USART1 port.

2.9.2 IrDA port

The IrDA communication port uses an IrDA transceiver (U11). *Table 9* shows the configuration elements related with the IrDA port operation

Table 9. Settings of configuration elements for RS-232 and IrDA ports

Element	Setting	Description
JP15	JP15 	**Default setting.** RS-232 selected: PB7 port of STM32L476ZGT6 receives signal originating from RXD terminal of CN9.
	JP15 	IrDA selected: PB7 port of STM32L476ZGT6 is connected with RxD terminal of the IrDA transceiver U11.
	JP15 	NFC selected: PB7 port of STM32L476ZGT6 receives NFC_IRQOUT signal from NFC peripheral. *Section 2.28* provides more detail on the NFC peripheral.
R93, R118, R116	In	Required for IrDA operation
R158, R119	Out	Required for IrDA operation

2.9.3 Limitations

The operation of RS-232 and IrDA ports is mutually exclusive. The operation of either port is also mutually exclusive with the NFC peripheral operation.

2.9.4 Operating voltage

The RS-232- and IrDA-related operating supply voltage of STM32L476ZGT6 (VDD line) must be within the range from 1.71 V to 3.6 V.

2.10 LPUART port

On top of USART1 port for serial communication, the STM32L476ZGT6 offers LPUART, a low-power UART port.

In the default configuration of STM32L476G-EVAL, the RX and TX terminals of the LPUART port are routed to the USB virtual COM port of ST-LINK/V2-1 and, the RX and TX terminals of USART1 port to the RS-232 connector CN9.

For specific purposes, the TX and RX of the LPUART port of STM32L476ZGT6 can be routed to the RS-232 connector CN9 instead. As RTS and CTS terminals of CN9 keep routed to USART1 port, they may block the LPUART communication flow. To avoid this, set the USART1 hardware flow control off.

The default settings of LPUART are: 115200b/s, 8bits, no parity, 1 stop bit, no flow control.

Table 10. Hardware settings for LPUART

LPUART port use	R188	R189	R158	R119	R118	JP15 1-2
Default setting USB virtual COM port of ST-LINK/V2-1	In	In	Out	Out	don't care	don't care
RS-232 (RX and TX)	Out	Out	In	In	Out	Closed

2.11 microSD card

The CN18 slot for microSD card is routed to STM32L476ZGT6's SDIO port, accepting SD (up to 2 Gbytes), SDHC (up to 32 Gbytes) and SDXC (up to 2 Tbytes) cards. One 4-Gbyte microSD card is delivered as part of STM32L476G-EVAL. The card insertion switch is routed to the PA8 GPIO port.

Table 11. Terminals of CN18 microSD slot

Terminal	Terminal name (MCU port)	Terminal	Terminal name (MCU port)
1	SDIO_D2 (PC10)	6	Vss/GND
2	SDIO_D3 (PC11)	7	SDIO_D0 (PC8)
3	SDIO_CMD (PD2)	8	SDIO_D1 (PC9)
4	VDD	9	GND
5	SDIO_CLK (PC12)	10	MicroSDcard_detect (PA8)

For microSD card operation, the LCD glass module daughterboard must be plugged into CN11 and CN14 in I/O-bridge position, as explained in *Section 2.15*.

2.11.1 Limitations

Due to the share of SDIO port and PA8 terminals, the following limitations apply:

- The microSD card cannot be operated simultaneously with LCD glass module or with motor control.
- The microSD card insertion cannot be detected when the PA8 is used as microcontroller clock output (MCO), one of alternate functions of PA8.

2.11.2 Operating voltage

The supply voltage for STM32L476G-EVAL microSD card operation must be within the range from 2.7 V to 3.6 V.

2.12 Motor control

The CN2 connector is designed to receive a motor control (MC) module. *Table 12* shows the assignment of CN2 and STM32L476ZGT6 terminals.

Table 12 also lists the modifications to be made on the board versus its by-default configuration. See *Section 2.12.1* for further details.

Table 12. Motor control terminal and function assignment

Motor control connector CN2		STM32L476ZGT6 microcontroller			
Terminal	**Terminal name**	**Port name**	**Function**	**Alternate function**	**Board modifications for enabling motor control**
1	Emergency Stop	PC9	TIM8_BKIN2	-	Close SB29 Remove MB979 daughterboard
2	GND	-	GND	-	-
3	PWM_1H	PC6	TIM8_CH1	-	Close SB27 Open SB2 Remove MB979 daughterboard
4	GND	-	GND	-	-
5	PWM_1L	PA7	TIM8_CH1N	-	Close SB19 Open SB18 Remove R66
6	GND	-	GND	-	-
7	PWM_2H	PC7	TIM8_CH2	-	Close SB30 Open SB4 Remove R33
8	GND	-	GND	-	-
9	PWM_2L	PB0	TIM8_CH2N	-	Close SB15 Open SB14 Remove R62
10	GND	-	GND	-	-
11	PWM_3H	PC8	TIM8_CH3	-	Close SB28 Remove MB979 daughterboard
12	GND	-	GND	-	-
13	PWM_3L	PB1	TIM8_CH3N	-	Close SB13 Open SB12
14	Bus Voltage	PC5	ADC12_IN	-	Close SB16 Remove MB979 daughterboard
15	PhaseA current+	PC0	ADC123_IN	-	Close SB34 Remove MB979 daughterboard
16	PhaseA current-	-	GND	-	-
17	PhaseB current+	PC1	ADC123_IN	-	Close SB36

Table 12. Motor control terminal and function assignment (continued)

Motor control connector CN2		STM32L476ZGT6 microcontroller			
Terminal	Terminal name	Port name	Function	Alternate function	Board modifications for enabling motor control
18	PhaseB current-	-	GND	-	-
19	PhaseC current+	PC2	ADC123_IN	-	Close SB42 Remove MB979 daughterboard
20	PhaseC current-	-	GND	-	-
21	ICL Shutout	PG6	GPIO	-	Close SB5 Remove R35
22	GND	-	GND	-	-
23	Dissipative Brake	PB2	GPIO	-	Close SB11 Remove R54
24	PFC ind. curr.	PC4	ADC12_IN	-	Close SB17 Remove MB979 daughterboard
25	+5V	-	+5V	-	-
26	Heatsink Temp.	PA3	ADC12_IN	-	Close SB22 Remove MB979 daughterboard
27	PFC Sync	PF9	TIM15_CH1	-	Close SB25 Remove R90
28	+3.3V	-	+3.3V	-	-
29	PFC PWM	PF10	TIM15_CH2	-	Close SB37 Remove R91
30	PFC Shutdown	PB12	TIM15_BKIN	-	Close SB3 Remove MB979 daughterboard
31	Encoder A	PA0	TIM2_CH1	ADC12_IN	Close SB35 Remove R83
32	PFC Vac	PA6	ADC12_IN	-	Close SB20 Open SB21 Remove MB979 daughterboard
33	Encoder B	PA1	TIM2_CH2	ADC12_IN	Close SB32 Remove MB979 daughterboard
34	Encoder Index	PA2	TIM2_CH3	ADC12_IN	Close SB31 Remove MB979 daughterboard

2.12.1 Board modifications to enable motor control

Figure 7 (top side) and *Figure 8* (bottom side) illustrate the board modifications listed in *Table 12*, required for the operation of motor control. Red color denotes a component to remove. Green color denotes a component to be fitted.

Figure 7. PCB top-side rework for motor control

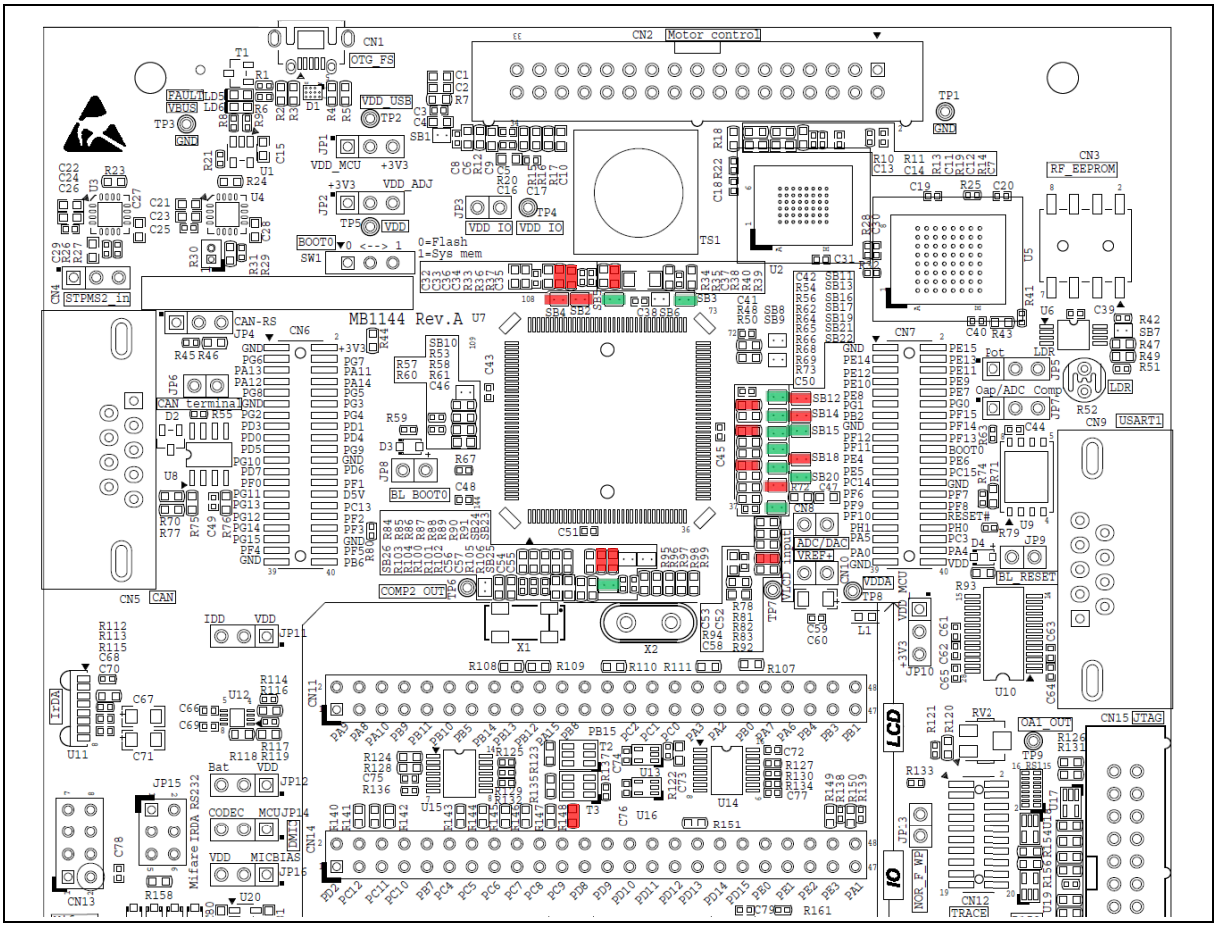
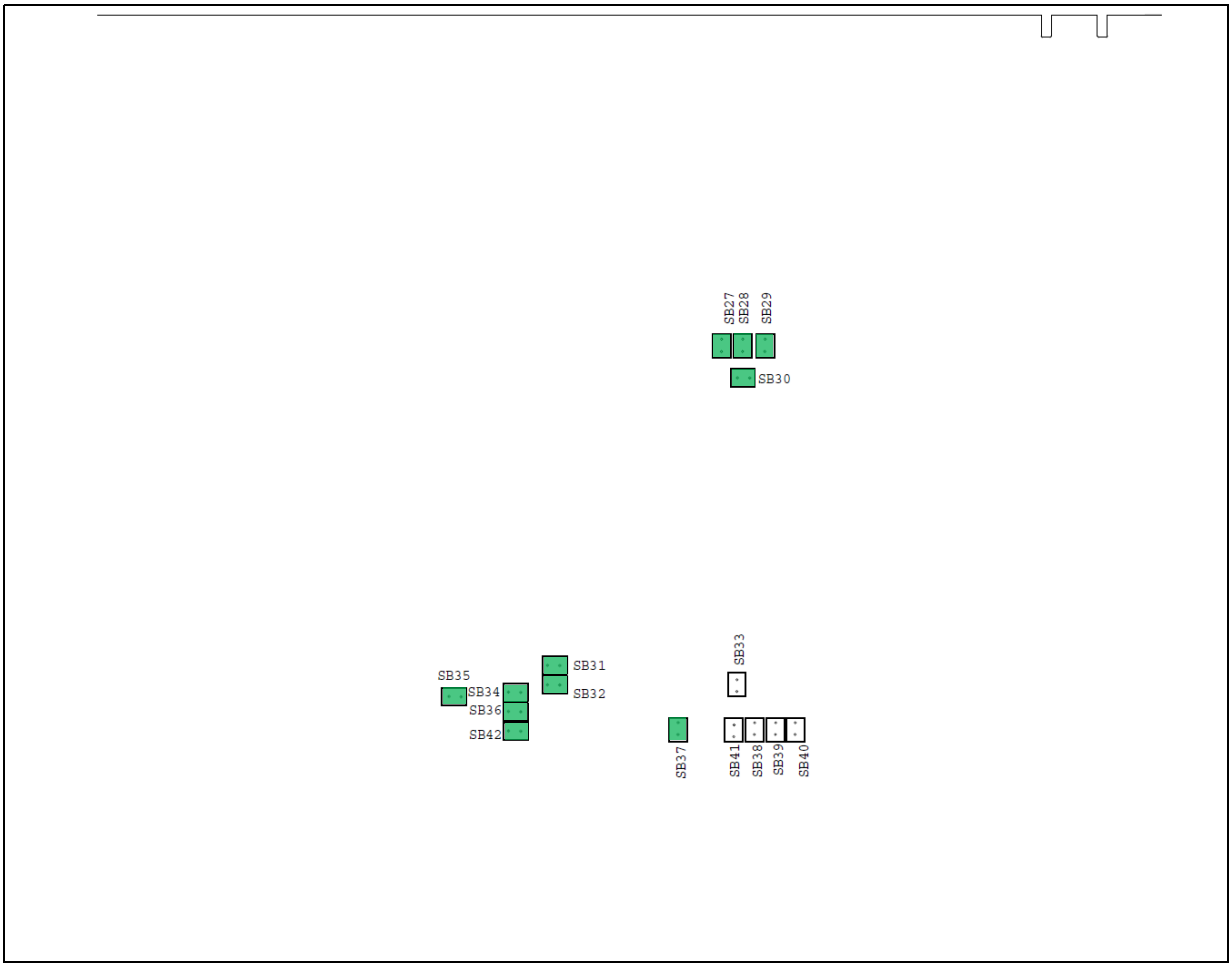


Figure 8. PCB underside rework for motor control



2.12.2 Limitations

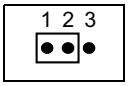
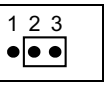
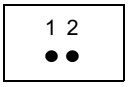
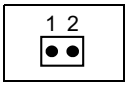
Motor control operation is exclusive with LCD glass module, Quad-SPI Flash memory device, audio codec, potentiometer, LDR, smartcard, LED1 drive and the use of sigma-delta modulators.

2.13 CAN

The STM32L476G-EVAL board supports one CAN2.0A/B channel compliant with CAN specification. The CN5 9-pole male connector of DE-9M type is available as CAN interface. A 3.3 V CAN transceiver is fitted between the CN5 connector and the CAN controller port of STM32L476ZGT6.

The JP4 jumper allows selecting one of high-speed, standby and slope control modes of the CAN transceiver. The JP6 jumper can fit a CAN termination resistor in.

Table 13. CAN related jumpers

Jumper	Setting	Configuration
JP4	JP4 1 2 3 	**Default setting** CAN transceiver operates in high-speed mode
	JP4 1 2 3 	CAN transceiver is in standby mode
JP6	JP6 1 2 	No termination resistor on CAN physical link
	JP6 1 2 	**Default setting** Termination resistor fitted on CAN physical link

2.13.1 Limitations

CAN operation is exclusive with LCD glass module operation.

2.13.2 Operating voltage

The supply voltage for STM32L476G-EVAL CAN operation must be within the range from 3.0 V to 3.6 V.

2.14 Extension connectors CN6 and CN7

The CN6 and CN7 headers complement the LCD glass module daughterboard connector, to give access to all GPIOs of the STM32L476ZGT6 microcontroller. In addition to GPIOs, the following signals and power supply lines are also routed on CN6 or CN7:

- GND
- +3V3
- DSV
- RESET#
- VDD
- Clock terminals PC14-OSC32_IN, PC15-OSC32_OUT, PH0-OSC_IN, PH1-OSC_OUT

Each header has two rows of 20 pins, with 1.27 mm pitch and 2.54 mm row spacing. For extension modules, SAMTEC RSM-120-02-L-D-xxx and SMS-120-x-x-D can be recommended as SMD and through-hole receptacles, respectively (**x** is a wild card).

2.15 LCD glass module daughterboard

The MB979 daughterboard delivered in the STM32L476G-EVAL package bears a segmented LCD glass module. The daughterboard inserts into CN11 and CN14 extension headers of the main board, each having two rows of pins. The corresponding female

connectors on the daughterboard have three rows of holes each. One raw is routed to segments of the LCD. The other two rows are interconnected and form a series of jumpers.

The way of inserting the LCD glass module daughterboard into CN11 and CN14 headers determines two functions of LCD glass module daughterboard. In its display function, STM32L476ZGT6 terminals are routed to LCD segments. In its I/O-bridge function, they are not. Instead, they transit from one row of CN11 pins to the other and from one row of CN14 pins to the other, thanks to interconnections fitted by the LCD glass module daughterboard.

Figure 9 shows how the LCD glass module daughterboard must be positioned for display function. This position is designated in the document as **display position**.

Figure 10 shows how the LCD glass module daughterboard must be positioned for I/O-bridge function. This position is designated in the document as **I/O-bridge position**.

The arrow indicates the side of the CN11 and CN14 headers where the extra row of holes of each female counterpart on the LCD glass module daughterboard has to protrude.

When the LCD glass module daughterboard is not plugged in, CN11 and CN14 give access to ports of the target microcontroller. *Figure 36* shows the related schematic diagram.

Table 14 shows the default settings of board configuration elements linked with CN11 and CN14 extension connectors and LCD glass module daughterboard.

Figure 9. LCD glass module daughterboard in display position

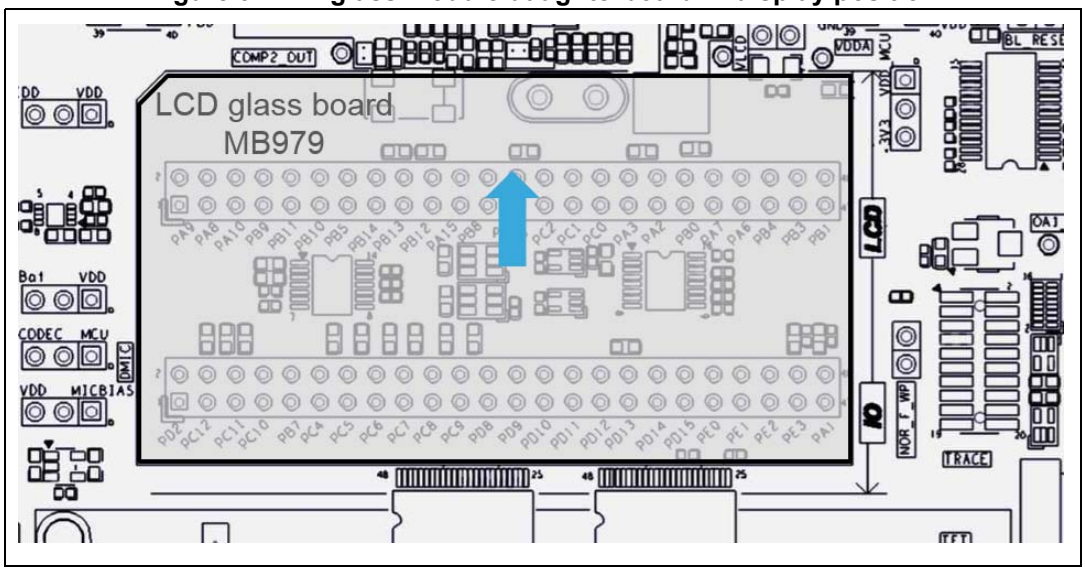


Figure 10. LCD glass module daughterboard in I/O-bridge position

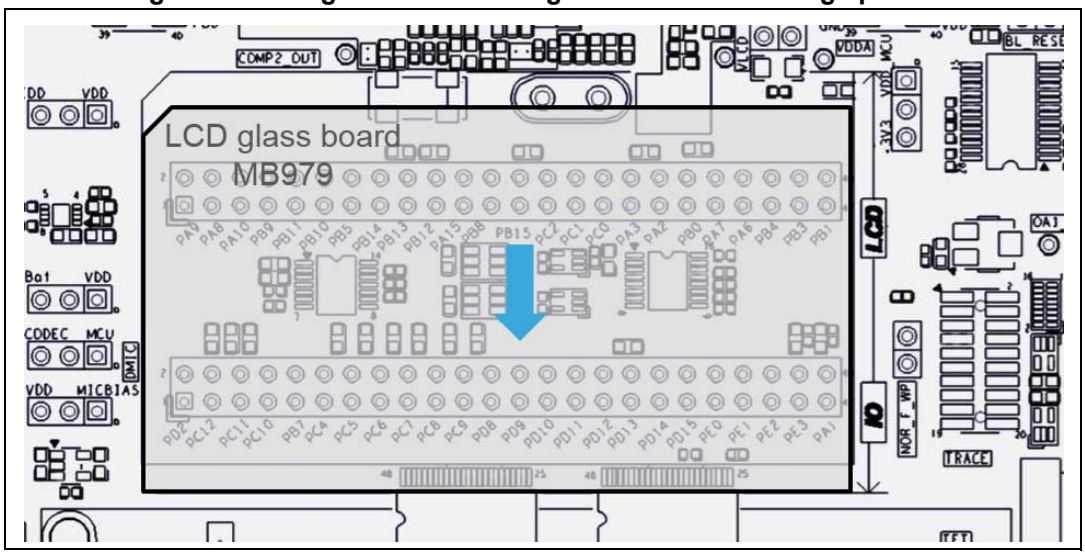


Table 14. LCD-daughterboard-related configuration elements

LCD segment	Element	Setting to enable LCD glass module	Description
SEG0	R82	In	PA1 routed to LCDSEG0
	SB32	Open	PA1 not routed to motor control
SEG1	R81	In	PA2 routed to LCDSEG1
	SB31	Open	PA2 not routed to motor control
SEG2	R78	In	PA3 routed to LCDSEG2
	SB22	Open	PA3 not routed to motor control
SEG3	R68	In	PA6 routed to LCDSEG3
	SB21	Open	PA6 not routed to Quad-SPI Flash memory device
	SB20	Open	PA6 not routed to motor control
SEG4	R66	In	PA7 routed to LCDSEG4
	SB18	Open	PA7 not routed to Quad-SPI Flash memory device
	SB19	Open	PA7 not routed to motor control
SEG5	R62	In	PB0 routed to LCDSEG5
	SB14	Open	PB0 not routed to Quad-SPI Flash memory device
	SB15	Open	PB0 not routed to motor control
SEG6	R56	In	PB1 routed to LCDSEG6
	SB12	Open	PB1 not routed to Quad-SPI Flash memory device
	SB13	Open	PB1 not routed to motor control
SEG10	R50	In	PB10 routed to LCDSEG10
	SB9	Open	PB10 not routed to Quad-SPI Flash memory device

Table 14. LCD-daughterboard-related configuration elements (continued)

LCD segment	Element	Setting to enable LCD glass module	Description
SEG11	R48	In	PB11 routed to LCDSEG11
	SB8	Open	PB11 not routed to Quad-SPI Flash memory device
SEG12	R39	In	PB12 routed to LCDSEG12
	SB3	Open	PB12 not routed to Quad-SPI Flash memory device
SEG13	R38	In	PB13 routed to LCDSEG13
	SB6	Open	PB13 not routed to Touch sensing
SEG18	R97	In	PC0 routed to LCDSEG18
	SB34	Open	PC0 not routed to motor control
SEG19	R98	In	PC1 routed to LCDSEG19
	SB36	Open	PC1 not routed to motor control
SEG20	R99	In	PC2 routed to LCDSEG20
	SB42	Open	PC2 not routed to motor control
SEG22	R65	In	PC4 routed to LCDSEG22
	SB17	Open	PC4 not routed to motor control
SEG23	R64	In	PC5 routed to LCDSEG23
	SB16	Open	PC5 not routed to motor control
SEG24	R36	In	PC6 routed to LCDSEG24
	SB2	Open	PC6 not routed to Touch sensing
	SB27	Open	PC6 not routed to for motor control
SEG25	R33	In	PC7 routed to LCDSEG25
	SB4	Open	PC7 not routed to Touch sensing
	SB30	Open	PC7 not routed to for motor control
SEG26	SB28	Open	PC8 not routed to motor control
SEG27	SB29	Open	PC9 not routed to motor control
SEG38	R103	In	PE2 routed to LCDSEG38
	SB26	Open	PE2 not routed to Trace
SEG39	R104	In	PE3 routed to LCDSEG39

The custom LCD glass module used on MB979 daughterboard is XHO5002B. To optimize the number of driving signals, the display elements are connected to eight common planes called COMx (LCDCOMx in the schematic digrams), where “x” can be substituted with figures from “0” to “7”. The other pole of each display element is called segment, SEGy (LCDSEGy in the schematic diagrams), where “y” can be substituted with figures from “0” to “39”. Each combination of COMx and SEGy addresses one display element. *Table 15*, *Table 16*, *Table 17* and *Table 22* show the LCD element mapping. COMx are ordered in rows, SEGy in columns. The table cells then display the display element names

corresponding to each COMx and SEGy combination. Names in quoting marks denote elements forming textual symbols, for example “µA” or “+”. *Figure 11* shows the physical location and shape of each segment on the LCD glass module.

Table 15. LCD glass element mapping - segments 0 to 9

	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9
COM0	O1	5D	Q4	O4	6D	Q5	ST	7D	Q6	S5
COM1	O2	5K	5L	O3	6K	6L	“nA”	7K	7L	S6
COM2	13b	12b	11b	16b	15b	14b	19b	18b	17b	1b
COM3	13a	12a	11a	16a	15a	14a	19a	18a	17a	1a
COM4	5I	5A	5G	6I	6A	6G	7I	7A	7G	1I
COM5	5B	5H	5F	6B	6H	6F	7B	7H	7F	1B
COM6	5C	5M	P4	6C	6M	P5	7C	7M	P6	1C
COM7	5J	5N	5E	6J	6N	6E	7J	7N	7E	1J

Table 16. LCD glass element mapping - segments 10 to 19

	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19
COM0	1D	“-”	C1	2D	Q1	C4	3D	Q2	“µA”	4D
COM1	1K	1L	C2	2K	2L	C3	3K	3L	“mA”	4K
COM2	S4	S2	4b	3b	2b	7b	6b	5b	10b	9b
COM3	S3	S1	4a	3a	2a	7a	6a	5a	10a	9a
COM4	1A	1G	2I	2A	2G	3I	3A	3G	4I	4A
COM5	1H	1F	2B	2H	2F	3B	3H	3F	4B	4H
COM6	1M	“+”	2C	2M	P1	3C	3M	P2	4C	4M
COM7	1N	1E	2J	2N	2E	3J	3N	3E	4J	4N

Table 17. LCD glass element mapping - segments 20 to 29

	SEG20	SEG21	SEG22	SEG23	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29
COM0	Q3	1e	2e	3e	4e	5e	6e	7e	8e	9e
COM1	4L	1f	2f	3f	4f	5f	6f	7f	8f	9f
COM2	8b	1c	2c	3c	4c	5c	6c	7c	8c	9c
COM3	8a	1d	2d	3d	4d	5d	6d	7d	8d	9d
COM4	4G	1j	2j	3j	4j	5j	6j	7j	8j	9j
COM5	4F	1i	2i	3i	4i	5i	6i	7i	8i	9i
COM6	P3	1h	2h	3h	4h	5h	6h	7h	8h	9h
COM7	4E	1g	2g	3g	4g	5g	6g	7g	8g	9g

Table 18. LCD glass element mapping - segments 30 to 39

	SEG30	SEG31	SEG32	SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39
COM0	10e	11e	12e	13e	14e	15e	16e	17e	18e	19e
COM1	10f	11f	12f	13f	14f	15f	16f	17f	18f	19f
COM2	10c	11c	12c	13c	14c	15c	16c	17c	18c	19c
COM3	10d	11d	12d	13d	14d	15d	16d	17d	18d	19d
COM4	10j	11j	12j	13j	14j	15j	16j	17j	18j	19j
COM5	10i	11i	12i	13i	14i	15i	16i	17i	18i	19i
COM6	10h	11h	12h	13h	14h	15h	16h	17h	18h	19h
COM7	10g	11g	12g	13g	14g	15g	16g	17g	18g	19g

2.15.1 Limitations

LCD glass module operation is exclusive with all other features of the board.

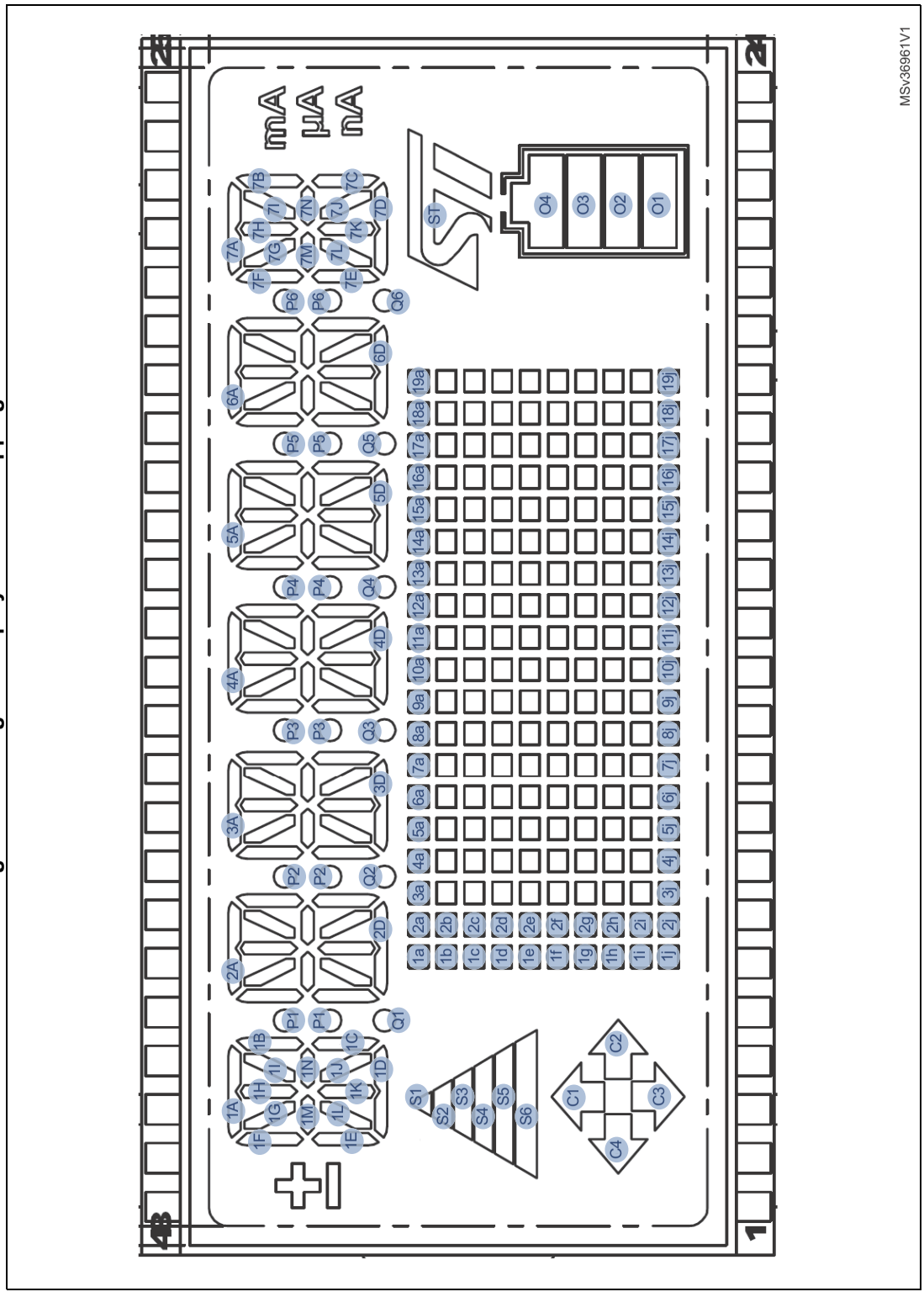


Figure 11. LCD glass display element mapping

2.16 TFT LCD panel

STM32L476G-EVAL is delivered with MB989P, a daughterboard plugged into the CN19 extension connector. It bears a TFT 2.8-inch color LCD panel with resistive touchscreen and an on-board controller. *Section 2.18* provides further information.

Thanks to level shifters on all signal lines, the TFT LCD panel can operate with the entire operating voltage range of STM32L476G-EVAL.

The TFT LCD panel is attached to the 16-bit data bus and accessed with FMC. The base address is 0x6800 0000, corresponding to NOR/SRAM3 bank1. The panel is selected with LCD_NE3 chip select signal generated by PG10 port of the STM32L476ZGT6. Address lines A0 and A1 determine the panel resources addressed, as depicted in *Table 19*.

Table 20 gives the CN19 extension connector terminal assignment.

Table 19. Access to TFT LCD resources with FMC address lines A0 and A1

Address	A1	A0	Usage
0x6800_0000	0	0	Read register
0x6800_0002	0	1	Read Graphic RAM (GRAM)
0x6800_0004	1	0	Write register
0x6800_0006	1	1	Write graphic RAM (GRAM)

Table 20. Assignment of CN19 connector terminals of TFT LCD panel

CN19 terminal	Terminal name	MCU port	CN19 terminal	Terminal name	MCU port
1	CSN	PG10	2	RS	PF0
3	WRN	PD5	4	RDN	PD4
5	RSTN	RESET#	6	D0	PD14
7	D1	PD15	8	D2	PD0
9	D3	PD1	10	D4	PE7
11	D5	PE8	12	D6	PE9
13	D7	PE10	14	D8	PE11
15	D9	PE12	16	D10	PE13
17	D11	PE14	18	D12	PE15
19	D13	PD8	20	D14	PD9
21	D15	PD10	22	BL_GND	-
23	BL_CONTROL	-	24	+3V3	-
25	+3V3	-	26	26	-
27	GND	-	28	BL_VDD	-
29	SDO	-	30	SDI	-
31	XL	I/O expander_X-	32	XR	I/O expander_X+
33	YD	I/O expander_Y-	34	YU	I/O expander_Y+

2.17 User LEDs

Four general-purpose color LEDs (LD1, LD2, LD3, LD4) are available as light indicators. Each LED is in light-emitting state with low level of the corresponding control port. They are controlled either by the STM32L476ZGT6 or by the I/O expander IC U32, named IOExpander1 in the schematic diagram. *Table 21* gives the assignment of control ports to the LED indicators.

Table 21. Port assignment for control of LED indicators

User LED	Control port	Control device
LED1 (Green)	PB2	STM32L476ZGT6
LED2 (Orange)	GPIO0	IOExpander1
LED3 (Red)	PC1	STM32L476ZGT6
LED4 (Blue)	GPIO2	IOExpander1

2.18 Physical input devices

The STM32L476G-EVAL board provides a number of input devices for physical human control. These are:

- four-way joystick controller with select key (B3)
- wake-up/ tamper button (B2)
- reset button (B1)
- resistive touchscreen of the TFT LCD panel
- 10 kΩ potentiometer (RV3)
- light-dependent resistor, LDR (R52)

Table 22 shows the assignment of ports routed to the physical input devices. They are either ports of the STM32L476ZGT6 or of one of the two I/O expander ICs on the board, named, in the schematic diagrams, IOExpander1 and IOExpander2.

Table 22. Port assignment for control of physical input devices

Input device	Control port	Control device
Joystick SEL	GPIO0	IOExpander2
Joystick DOWN	GPIO1	IOExpander2
Joystick LEFT	GPIO2	IOExpander2
Joystick RIGHT	GPIO3	IOExpander2
Joystick UP	GPIO4	IOExpander2
Wake-up/ tamper B2	PC13	STM32L476ZGT6
Reset B1	NRST	STM32L476ZGT6
Resistive touch screen X+	X+	IOExpander1
Resistive touch screen X-	X-	IOExpander1
Resistive touch screen Y+	Y+	IOExpander1

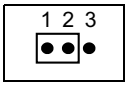
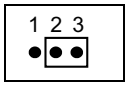
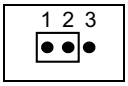
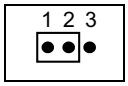
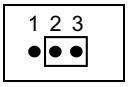
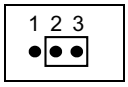
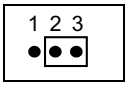
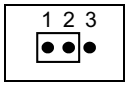
Table 22. Port assignment for control of physical input devices (continued)

Input device	Control port	Control device
Resistive touch screen Y-	Y-	IOExpander1
Potentiometer	PB4 or PA0	STM32L476ZGT6
LDR	PA0 or PB4	STM32L476ZGT6

The potentiometer and the light-dependent resistor can be routed, mutually exclusively, to either PB4 or to PA0 port of STM32L476ZGT6. *Table 23* depicts the setting of associated configuration jumpers.

As illustrated in the schematic diagram in *Figure 46*, the PB4 port is routed, in the STM32L476ZGT6, to the non-inverting input of comparator Comp2. The PA0 is routed to non-inverting input of operational amplifier OpAmp1. However, depending on register settings, it can also be routed to ADC1 or to ADC2.

Table 23. Setting of jumpers related with potentiometer and LDR

Jumper	Setting		Routing
JP5 **JP7**	JP5 	JP7 	Potentiometer is routed to pin PB4 of STM32L476ZGT6.
JP5 **JP7**	JP5 	JP7 	**Default setting.** Potentiometer is routed to pin PA0 of STM32L476ZGT6.
JP5 **JP7**	JP5 	JP7 	LDR is routed to pin PB4 of STM32L476ZGT6.
JP5 **JP7**	JP5 	JP7 	LDR is routed to pin PA0 of STM32L476ZGT6.

2.18.1 Limitations

The potentiometer and the light-dependent resistor are mutually exclusive.

2.19 Operational amplifier and comparator

2.19.1 Operational amplifier

STM32L476ZGT6 provides two on-board operational amplifiers, one of which, OpAmp1, is made accessible on STM32L476G-EVAL. OpAmp1 has its inputs and its output routed to I/O ports PA0, PA1 and PA3, respectively. The non-inverting input PA0 is accessible on the terminal 1 of the JP7 jumper header. On top of the possibility of routing either of the

potentiometer or LDR to PA0, en external source can also be connected to it, using the terminal 1 of JP7.

The PA3 output of the operational amplifier can be accessed on test point TP9. Refer to the schematic diagram in *Figure 46*.

The gain of OpAmp1 is determined by the ratio of the variable resistor RV2 and the resistor R121, as shown in the following equation:

$$Gain = 1 + (RV2) \div (R121)$$

With the RV2 ranging from 0 to 10 kΩ and R121 being 1 kΩ, the gain can vary from 1 to 11.

The R63 resistor in series with PA0 is beneficial for reducing the output offset.

2.19.2 Comparator

STM32L476ZGT6 provides two on-board comparators, one of which, Comp2, is made accessible on STM32L476G-EVAL. Comp2 has its non-inverting input and its output routed to I/O ports PB4 and PB5, respectively. The input is accessible on the terminal 3 of the JP7 jumper header. On top of the possibility of routing either of the potentiometer or LDR to PB4, en external source can also be connected to it, using the terminal 3 of JP7.

The PB5 output of the comparator can be accessed on test point TP6. Refer to the schematic diagram in *Figure 46*.

2.20 Analog input, output, VREF

STM32L476ZGT6 provides on-board analog-to-digital converter, ADC and, digital-to-analog converter, DAC. The port PA4 can be configured to operate either as ADC input or as DAC output. PA4 is routed to the two-way header CN8 allowing to fetch signals to or from PA4 or to ground it by fitting a jumper into CN8.

Parameters of the ADC input low-pass filter formed with R72 and C47 can be modified by replacing these components according to application requirements. Similarly, parameters of the DAC output low-pass filter formed with R73 and C47 can be modified by replacing these components according to application requirements.

The VREF+ terminal of STM32L476ZGT6 is used as reference voltage for both ADC and DAC. By default, it is routed to VDDA through a jumper fitted into the two-way header CN10. The jumper can be removed and an external voltage applied to the terminal 1 of CN10, for specific purposes.

2.21 SRAM device

IS61WV102416BLL, a 16-Mbit static RAM (SRAM), 1 M x16 bit, is fitted on the STM32L476G-EVAL main board, in U2 position. The STM32L476G-EVAL main board as well as the addressing capabilities of FMC allow hosting SRAM devices up to 64 Mbytes. This is the reason why the schematic diagram in *Figure 41* mentions several SRAM devices.

The SRAM device is attached to the 16-bit data bus and accessed with FMC. The base address is 0x6000 0000, corresponding to NOR/SRAM1 bank1. The SRAM device is

selected with FMC_NE1 chip select. FMC_NBL0 and FMC_NBL1 signals allow selecting 8-bit and 16-bit data word operating modes.

By removal of R18, a zero-ohm resistor, the SRAM is deselected and the STM32L476ZGT6 ports PD7, PE0 and PE1 corresponding to FMC_NE1, FMC_NBL0 and FMC_NBL1 signals, respectively, can be used for other application purposes.

Table 24. SRAM chip select configuration

Resistor	Fitting	Configuration
R18	In	**Default setting.** SRAM chip select is controlled with FMC_NE1
	Out	SRAM is deselected. FMC_NE1 is freed for other application purposes.

2.21.1 Limitations

The SRAM addressable space is limited if some or all of A19, A20, A21, A22 and A23 FMC address lines are shunted to the CN12 connector for debug trace purposes. In such a case, the disconnected addressing inputs of the SRAM device are pulled down by resistors. *Section 2.2* provides information on the associated configuration elements.

2.21.2 Operating voltage

The SRAM device operating voltage is in the range from 2.4 V to 3.6 V.

2.22 NOR Flash memory device

M29W128GL70ZA6E, a 128-Mbit NOR Flash memory, 8 M x16 bit, is fitted on the STM32L476G-EVAL main board, in U5 position. The STM32L476G-EVAL main board as well as the addressing capabilities of FMC allow hosting M29W256GL70ZA6E, a 256-Mbit NOR Flash memory device. This is the reason why the schematic diagram in *Figure 41* mentions both devices.

The NOR Flash memory device is attached to the 16-bit data bus and accessed with FMC. The base address is 0x6400 0000, corresponding to NOR/SRAM2 bank1. The NOR Flash memory device is selected with FMC_NE2 chip select signal. 16-bit data word operation mode is selected by a pull-up resistor connected to BYTE terminal of NOR Flash memory. The jumper JP13 is dedicated for write protect configuration.

By default, the FMC_NWAIT signal is not routed to RB port of the NOR Flash memory device, and, to know its ready status, its status register is polled by the demo software fitted in STM32L476G-EVAL. This can be modified with configuration elements, as shown in *Table 25*.

Table 25. NOR Flash memory-related configuration elements

Element	Setting	Configuration
JP13	JP13 1 2 ● ●	**Default setting.** NOR Flash memory write is enabled.
	JP13 1 2 ● ●	NOR Flash memory write is inhibited. Write protect is activated.
R53 SB10	R53 In SB10 open	**Default setting.** PD6 port of STM32L476ZGT6 is used for SAI1_SDA signal and routed to audio codec. NOR Flash memory device's status register can be accessed.
	R53 Out SB10 closed	PD6 port of STM32L476ZGT6 is used for FMC_NWAIT signal and routed to NOR Flash memory device's RB port. NOR Flash memory device's status register cannot be accessed.

2.22.1 Limitations

- FMC_NWAIT and SAI1_SDA signals are mutually exclusive.
- The NOR Flash memory device's addressable space is limited if some or all of A19, A20, A21, A22 and A23 FMC address lines are shunted to the CN12 connector for debug trace purposes. In such a case, the disconnected addressing inputs of the NOR Flash memory device are pulled down by resistors. *Section 2.2* provides information on the associated configuration elements.

2.22.2 Operating voltage

NOR Flash memory operating voltage must be in the range from 1.65 V to 3.6 V.

2.23 EEPROM

M24128-DFDW6TP, a 128-Kbit I²C-bus EEPROM device, is fitted on the main board of STM32L476G-EVAL, in U6 position. it is accessed with I²C-bus lines I2C2_SCL and I2C2_SDA of STM32L476ZGT6. It supports all I²C-bus modes with speeds up to 1 MHz. The base I²C-bus address is 0xA0. Write-protecting the EEPROM is possible through opening the SB7 solder bridge. By default, SB7 is closed and writing into the EEPROM enabled.

2.23.1 Operating voltage

The M24128-DFDW6TP EEPROM device's operating voltage must be in the range from 1.7 V to 3.6 V

2.24 RF-EEPROM

RF-EEPROM daughterboard, ANT7-M24LR-A, can be connected to CN3 connector of the STM32L476G-EVAL board. STM32L476ZGT6 can access the RF-EEPROM in two ways,

wired through I²C bus or wireless using 13.56 MHz RF band reserved for RFID and NFC equipment. For wireless access, CR95HF reader daughterboard plugged in the CN13 connector can be used, for example.

I²C address of RF-EEPROM device is 0xA6.

2.25 Quad-SPI Flash memory device

N25Q256A13EF840E, a 256-Mbit Quad-SPI Flash memory device, is fitted on the STM32L476G-EVAL main board, in U9 position. It allows evaluating STM32L476ZGT6 Quad-SPI Flash memory device interface.

N25Q256A13EF840E can operate in single transfer rate (STR) and double transfer rate (DTR) modes.

By default, the Quad-SPI Flash memory device is not accessible. *Table 26* shows the configuration elements and their settings allowing to access the Quad-SPI Flash memory device. The LCD glass module daughterboard MB979 takes active part in the configuration. It must be removed from the main board (denoted as “MB979 out”), to operate the Quad-SPI Flash memory device. *Section 2.12: Motor control* provides additional information.

Table 26. Configuration elements related with Quad-SPI device

Element	Setting	Configuration
SB12 SB13 MB979	SB12 open SB13 open	**Default setting.** QSPI_D0 data line is not available at Quad-SPI Flash memory device: PB1 port of STM32L476ZGT6 is only routed to CN11 connector for the MB979 daughterboard.
	SB12 closed SB13 open MB979 out	QSPI_D0 data line is available at Quad-SPI Flash memory device: PB1 port of STM32L476ZGT6 is routed to DQ0 port of Quad-SPI Flash memory device.
SB14 SB15 MB979	SB14 open SB15 open	**Default setting.** QSPI_D1 data line is not available at Quad-SPI Flash memory device: PB0 port of STM32L476ZGT6 is only routed to CN11 connector for the MB979 daughterboard.
	SB14 closed SB15 open MB979 out	QSPI_D1 data line is available at Quad-SPI Flash memory device: PB0 port of STM32L476ZGT6 is routed to DQ1 port of Quad-SPI Flash memory device.
SB18 SB19 MB979	SB18 open SB19 open	**Default setting.** QSPI_D2 data line is not available at Quad-SPI Flash memory device: PA7 port of STM32L476ZGT6 is only routed to CN11 connector for the MB979 daughterboard.
	SB18 closed SB19 open MB979 out	QSPI_D2 data line is available at Quad-SPI Flash memory device: PA7 port of STM32L476ZGT6 is routed to DQ2 port of Quad-SPI Flash memory device.

Table 26. Configuration elements related with Quad-SPI device (continued)

Element	Setting	Configuration
SB21 SB20 MB979	SB21 open SB20 open	**Default setting.** QSPI_D3 data line is not available at Quad-SPI Flash memory device: PA6 port of STM32L476ZGT6 is only routed to CN11 connector for the MB979 daughterboard.
	SB21 closed SB20 open MB979 out	QSPI_D3 data line is available at Quad-SPI Flash memory device: PA6 port of STM32L476ZGT6 is routed to DQ3 port of Quad-SPI Flash memory device.
SB9 MB979	SB9 open	**Default setting.** QSPI_CLK clock line is not available at Quad-SPI Flash memory device: PB10 port of STM32L476ZGT6 is only routed to CN11 connector for the MB979 daughterboard.
	SB9 closed MB979 out	QSPI_CLK clock line is available at Quad-SPI Flash memory device: PB10 port of STM32L476ZGT6 is routed to C port of Quad-SPI Flash memory device.
SB8 MB979	SB8 open	**Default setting.** QSPI_CS line is not available at Quad-SPI Flash memory device: PB11 port of STM32L476ZGT6 is only routed to CN11 connector for the MB979 daughterboard.
	SB8 closed MB979 out	QSPI_CS line is available at Quad-SPI Flash memory device: PB11 port of STM32L476ZGT6 is routed to S# port of Quad-SPI Flash memory device.

2.25.1 Limitations

Quad-SPI operation is exclusive with LCD glass module and with motor control.

2.25.2 Operating voltage

Voltage of Quad-SPI Flash memory device N25Q256A13EF840E is in the range of 2.7 V to 3.6 V.

2.26 Touch-sensing button

The STM32L476G-EVAL evaluation board supports a touch sensing button based on either RC charging or on charge-transfer technique. The latter is enabled, by default.

The touch sensing button is connected to PB12 port of STM32L476ZGT6 and the related charge capacitor is connected to PB13.

An active shield is designed in the layer two of the main PCB, under the button footprint. It allows reducing disturbances from other circuits to prevent from false touch detections.

The active shield is connected to PC6 port of STM32L476ZGT6 through the resistor R37.The related charge capacitor is connected to PC7.

Table 27 shows the configuration elements related with the touch sensing function. Some of them serve to enable or disable its operation. However, most of them serve to optimize the touch sensing performance, by isolating copper tracks to avoid disturbances due to their antenna effect.

Table 27. Touch-sensing-related configuration elements

Element	Setting	Configuration
R39	In	**Default setting.** PB12 port is routed to CN11 connector for LCD glass module daughterboard. This setting is not good for robustness of touch sensing.
	Out	PB12 port is cut from CN11. This setting is good for robustness of touch sensing.
SB3	Open	**Default setting.** PB12 is not routed to motor control. This setting is good for robustness of touch sensing.
	Closed	PB12 is routed to motor control. This setting is not good for robustness of touch sensing.
R38	In	**Default setting.** PB13 port is routed to CN11 connector for LCD glass module daughterboard. This setting is not good for robustness of touch sensing.
	Out	PB13 port is cut from CN11. This setting is good for robustness of touch sensing.
SB6	Open	**Default setting.** PB13 is not routed to sampling capacitor. Touch sensing cannot operate.
	Closed	PB13 is routed to sampling capacitor. Touch sensing can operate.
R36	In	**Default setting.** PC6 port is routed to CN14 connector for LCD glass module daughterboard. This setting is not good for robustness of touch sensing.
	Out	PC6 port is cut from CN14. This setting is good for robustness of touch sensing.
SB2	Open	**Default setting.** PC6 is not routed to active shield under the touch-sensing button. This setting is not good for robustness of touch sensing.
	Closed	PC6 is routed to active shield under the touch-sensing button. This setting is good for robustness of touch sensing.
SB27	Open	**Default setting.** PC6 port of STM32L476ZGT6 is not routed to motor control. This setting is good for robustness of touch sensing.
	Closed	PC6 is routed to motor control. This setting is not good for robustness of touch sensing.
R33	In	**Default setting.** PC7 port is routed to CN14 connector for LCD glass module daughterboard. This setting is not good for robustness of touch sensing.
	Out	PC7 port is cut from CN14. This setting is good for robustness of touch sensing.
SB4	Open	**Default setting.** PC7 port of STM32L476ZGT6 is not routed to sampling capacitor of the active shield under the touch-sensing button. This setting is not good for robustness of touch sensing.
	Closed	PC7 is routed to sampling capacitor of the active shield under the touch-sensing button. This setting is good for robustness of touch sensing.

Table 27. Touch-sensing-related configuration elements (continued)

Element	Setting	Configuration
SB30	Open	**Default setting.** PC7 port of STM32L476ZGT6 is not routed to motor control. This setting is good for robustness of touch sensing.
	Closed	PC7 is routed to motor control. This setting is not good for robustness of touch sensing.

2.26.1 Limitations

Touch sensing button is exclusive with LCD glass module, thermal sensor PT100 via sigma-delta conversion, USB OTG FS port operating as USB host, SWP and NFC.

2.27 Smartcard, SWP

ST8024CDR, an interface device for 3 V and 5 V asynchronous smartcards, is fitted on the STM32L476G-EVAL main board, in U30 position. ST8024CDR performs all supply protection and control functions of the smartcard.

ST8024CDR is controlled, on its turn, by STM32L476ZGT6, directly through its ports or indirectly through ports of the U33 I/O expander device (IOExpander2), as shown in *Table 28*.

The SWIO port of the smartcard for single-wire protocol (SWP) communication is managed directly by PB12 port of STM32L476ZGT6.

Table 28. Assignment of ports for ST8024CDR control

ST8024CDR port	Function	Control port
5V/3V	Smartcard power supply selection pin.	IOexpander2 GPIO7
I/OUC	Data I/O line	STM32L476ZGT6 PC4
XTAL1	Quartz crystal or external clock input	STM32L476ZGT6 PB0
OFF	Card presence detect	IOexpander2 GPIO8
RSTIN	Card reset command input	IOexpander2 GPIO5
CMDVCC	Activation sequence start command input (active low)	IOexpander2 GPIO6

Table 29 provides information on configuration elements related with smartcard operation. Refer to *Table 8*, *Table 12*,*Table 26* and*Table 27* for complementary information. Bridging of CN11 and CN14 rows of I/Os can be done by means of the MB979 daughterboard plugged into CN11 and CN14 in I/O-bridge position, as explained in *Section 2.15*.

Table 29. Configuration elements related with smartcard and SWP

Element	Setting	Configuration
R39 SB3 R109 CN11	R109 in R39 in SB3 open CN11 I/O-bridged	**Default setting.** Smartcard SWP cannot be handled: PB12 is routed to USB OTG FS port as USBOTG_OVRCR line, on top of being routed to SWIO port of smartcard Configuration dedicated for USB OTG FS operation.
	R109 out R39 in SB3 open CN11 I/O-bridged	Smartcard SWP can be handled: PB12 is routed to SWIO port of smartcard. It is disconnected from any other resource that could affect the SWP operation Configuration dedicated for smartcard SWP operation
	R39 out SB3 closed	Smartcard SWP cannot be handled: PB12 is routed to motor control as MC_PFC_Shutdown Configuration dedicated for motor control operation
	R39 out SB3 open	Smartcard SWP cannot be handled: PB12 is only routed to touch-sensing button and it is disconnected from any other resource. Configuration dedicated for touch-sensing button operation.
R62 SB14 SB15	R62 in SB14 open SB15 open CN11 I/O-bridged	**Default setting.** Smartcard controller U30 is supplied with clock: PB0 port is routed to XTAL1 of U30, as SmartCard_CLK line and it is not routed to other resources. Configuration dedicated for smartcard operation.
	R62 out SB14 closed SB15 open	Smartcard controller U30 is not supplied with clock: PB0 is routed to Quad-SPI Flash memory device as QSPI_D1 and it is not routed to other resources. Configuration dedicated for Quad-SPI Flash memory device operation.
	R62 out SB14 open SB15 closed	Smartcard controller U30 is not supplied with clock: PB0 is routed to motor control as MC_PWM_2L line and it is not routed to other resources. Configuration dedicated for motor control operation.
R65 SB17 CN14	R65 in SB17 open CN14 I/O-bridged	**Default setting.** Smartcard controller gets SmartCard_IO line: PC4 port of MCU is routed to IOUC port of U30, as SmartCard_IO line and it is not routed to other resources. Configuration dedicated for smartcard operation.
	R65 out SB17 closed	Smartcard controller does not get SmartCard_IO line: PC4 port of MCU is routed to motor control as MC0PFC0IndCur line and it is not routed to other resources. Configuration dedicated for motor control operation.

2.27.1 Limitations

The following limitations apply for the smartcard operation:

- Smartcard operation is mutually exclusive with LCD glass module, Quad-SPI Flash memory device and motor control operation.
- SWP operation is mutually exclusive with LCD glass module, touch-sensing button, motor control and USB OTG FS port operation, if the last operates as USB host. SWP can operate concurrently with USB OTG FS port acting as USB device.

2.27.2 Operating voltage

Smartcard operating ranging from V_{DD} = 2.7 V to V_{DD} = 3.6 V. However, the SWP only operates with the supply voltage of 3.3 V.

2.28 Near-field communication (NFC)

The STM32L476G-EVAL board can host an NFC transceiver board plugged in CN13 extension connector.

Figure 12 illustrates the way of attaching an NFC board.

Figure 12. NFC board plugged into STM32L476G-EVAL board

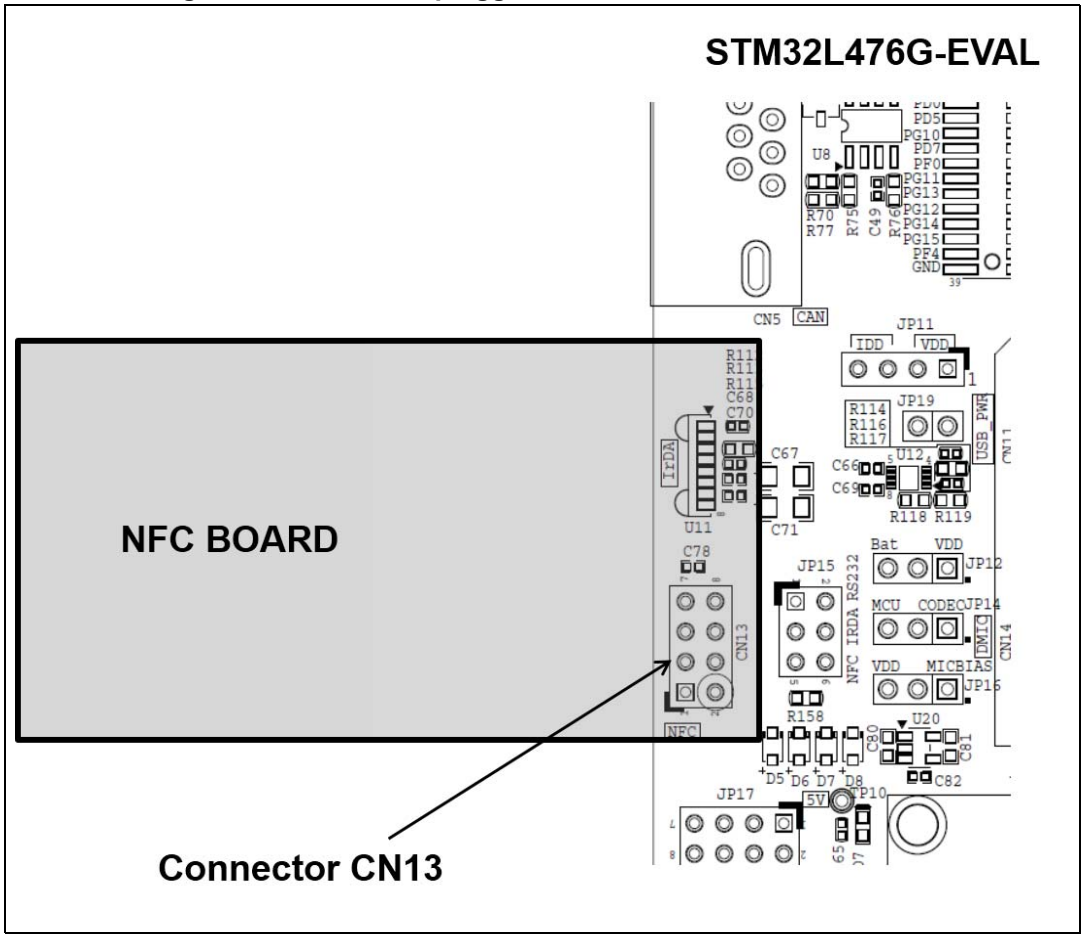


Table 30 shows the assignment of signals to CN13 connector.

The serial communication with the module plugged in CN13 can either use SPI communication protocol (default) or UART communication protocol.

Table 30. CN13 NFC connector terminal assignment

CN13 terminal	NFC line name	MCU port	Function
1	NFC_IRQOUTN or UART_TX	PB7	Interrupt output for NFC device Connected to STM32L476ZGT6 UART RX
2	NFC_IRQINN or UART_RX	PB6	Interrupt input for NFC device Connected to STM32L476ZGT6 UART TX
3	NFC_NSS	PF11	SPI slave select
4	NFC_MISO	PB14	SPI data, slave output
5	NFC_MOSI	PB15	SPI data, slave input
6	NFC_SCK	PB13	SPI serial clock
7	+3V3	-	Main power supply/power supply for RF drivers
8	GND	-	Ground

2.29 Dual-channel sigma-delta modulators STPMS2L

2.29.1 STPMS2L presentation

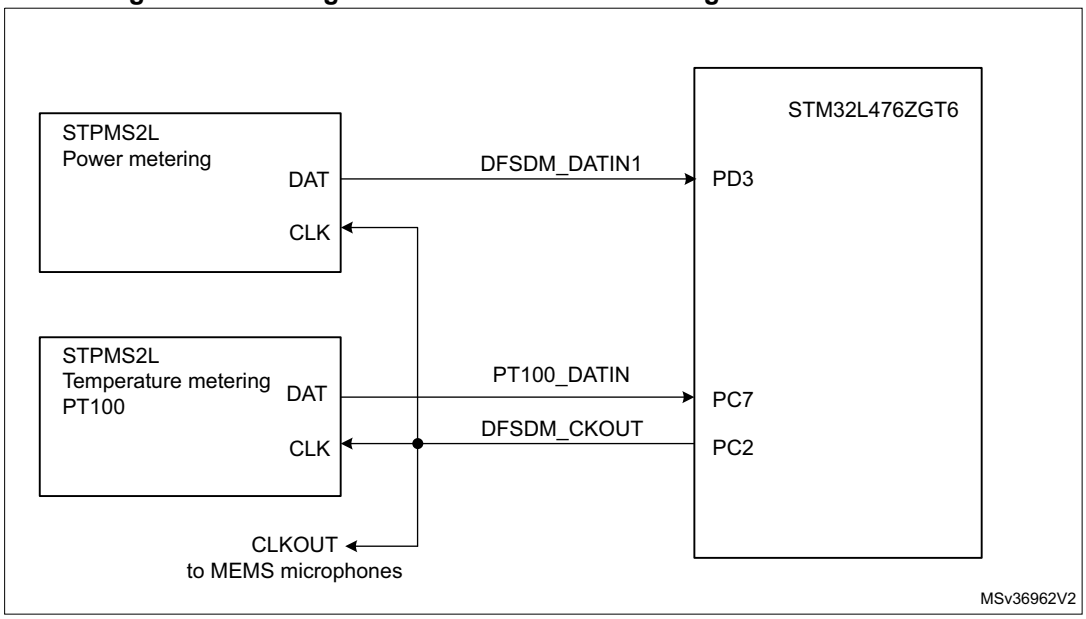
With its DFSDM interface, the STM32L476ZGT6 microcontroller can directly interact with sigma-delta modulator devices, such as STPMS2L.

STPMS2L comprises two analog measuring channels based on second-order sigma-delta modulators. Typically, it can be used in power metering where both voltage and current need to be known. One channel measures the voltage, the other channel measures the current.

DAT port outputs converted measurement data on the DFSDM_DATIN1 line, received by the STM32L476ZGT6 DFSDM controller. The data from STPMS2L are synchronized with DFSDM_CKOUT clock generated by the STM32L476ZGT6 DFSDM controller and received on CLK terminal of STPMS2L.

There are two STPMS2L devices on STM32L476G-EVAL, sharing the DFSDM clock. One is wired such as to support a power-metering demonstrator. The other allows measuring temperature using the PT100 sensor.

Figure 13. Routing of STPMS2L dual-channel sigma-delta modulators



2.29.2 STPMS2L settings

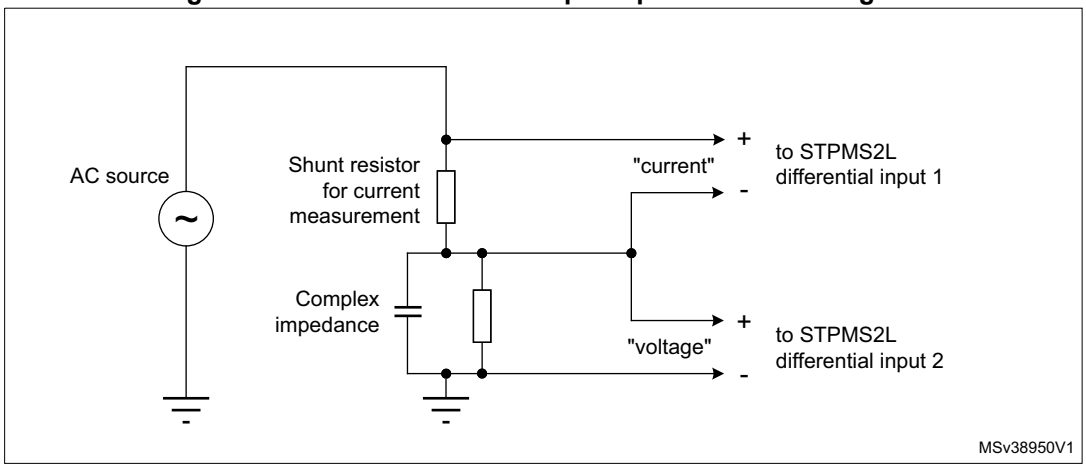
STPMS2L operating parameters are set through its configuration terminals MS0, MS1, MS2 and MS3. On STM32L476G-EVAL, both devices are configured as follows:

- voltage channel range: differential voltage +/- 300mV
- current channel range: differential voltage +/- 300mV
- internal voltage reference is used
- input bandwidth: 0 to 1 kHz
- temperature compensation: flattest +30ppm/°C
- DAT output: voltage and current samples multiplexed
- DATn output: not used
- HW mode selected for settings

2.29.3 STPMS2L power metering

STPMS2L in U3 position simulates low-voltage AC power metering, with capacitive load impedance, to give different phase to voltage and current.

Figure 14. Power measurement principle schematic diagram



A low-voltage AC generator is to be applied by the user as shown in *Figure 14*. The shunt resistor is connected in series with the load to provide current measurement points to one of STPMS2L input channels. The voltage measurement points for the other input channel are taken across the load. *Figure 15* shows an extract of the corresponding schematic diagram.

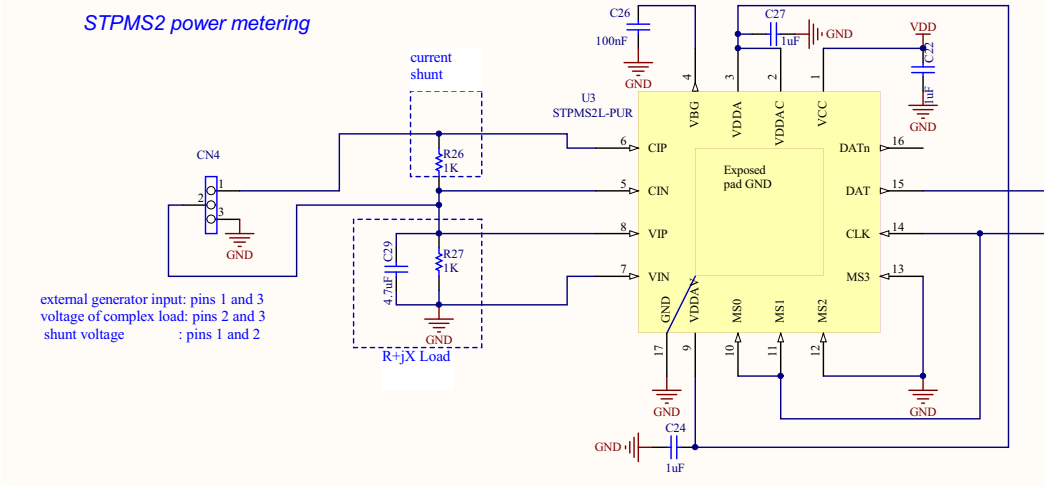
Warning: do not connect AC mains!

Test example:

The output of a low-voltage AC generator is connected to CN4, terminals 1 and 3. The amplitude is set between 200 mV and 300 mV and the frequency adjustable between 10 Hz and 100 Hz.

With 34 Hz frequency and the load formed of R27 of 1 kΩ in parallel with C29 of 4.7 µF, the voltage and current phases are theoretically 45 degrees apart.

Figure 15. STPMS2L power metering schematic diagram



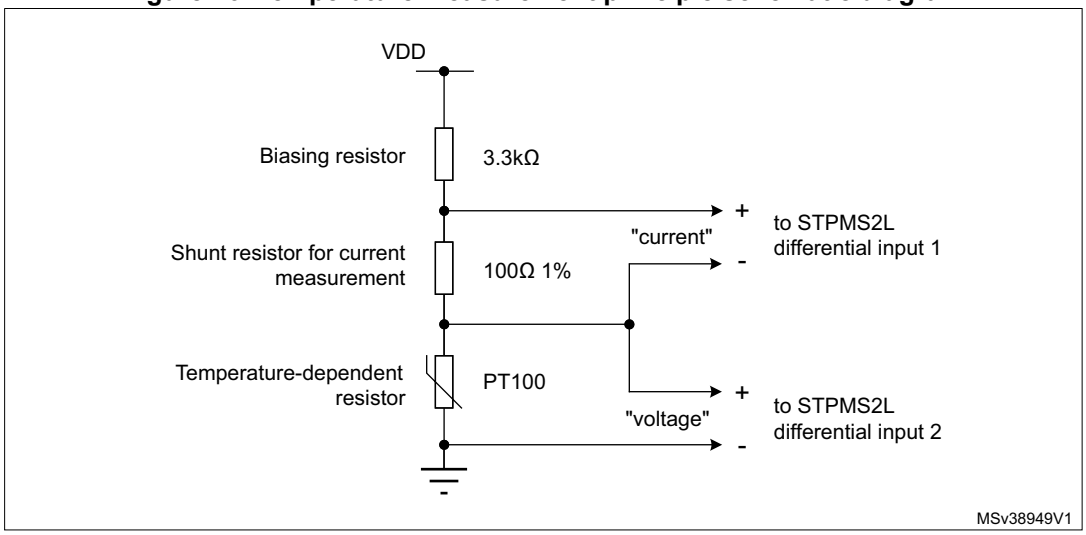
2.29.4 STPMS2L for PT100 measurement

PT100 is a resistor with temperature-dependent resistance.

Usually, one of two methods is used for measuring temperature with a temperature-dependent resistor. In the first method, a known current is driven through the measuring resistor. The temperature is represented by the voltage measured across the resistor. In the second method, a known voltage is applied on the resistor and the current flowing through is measured, representing the temperature. In these methods, either an accurate current source or an accurate voltage source is required.

With the dual-input measurement with STPMS2L in U4 position, no such accurate current or voltage sources are required. Instead, a precision shunt resistor is required. One channel of the STPMS2L measures the voltage across the precise shunt resistor, representing the current flowing through PT100. The other channel measures the voltage across PT100.

Figure 16. Temperature measurement principle schematic diagram



With voltage across and current through the PT100 resistor, the STM32L476ZGT6 microcontroller computes resistance PT100.

For temperatures lower than +100°C, the temperature is given by the following equation, where PT100 is resistance of the PT100 resitor and T is temperature in degrees centigrade:

$$T = (PT100 - 100) / (0.385)$$

2.29.5 Limitations

Operating voltage must be in the range from 3.2 V to 3.6 V.

2.30 STM32L476ZGT6 current consumption measurement

STM32L476ZGT6 has a built-in circuit allowing to measure its own current consumption (IDD) in Run and Low-power modes, except for Shutdown mode.

It is strongly recommended that, the MCU supply voltage (VDD_MCU line) does not exceed 3.3 V. This is because there are components on STM32L476G-EVAL supplied from 3.3 V

that communicate with the MCU through I/O ports. Voltage exceeding 3.3 V on the MCU output port may inject current into 3.3 V-supplied peripheral I/Os and false the MCU current consumption measurement.

2.30.1 IDD measurement principle - analog part

The analog part is based on measuring voltage drop across a shunt resistor, amplified with a differential amplifier. The STM32L476ZGT6 microcontroller supply current is shunted, by jumper settings, to flow through the measurement 1 Ω resistor R135: JP11 terminals 1 and 2 are to be open, terminals 3 and 4 closed. When the transistor T2 is in conductive state, the MCU supply current is proportional to the voltage across R135. When T2 is in high-impedance state, the MCU supply current is proportional to the voltage across the series of R135 and R123. The former state is used for measuring the current consumption in dynamic run mode, the latter in low-power mode.

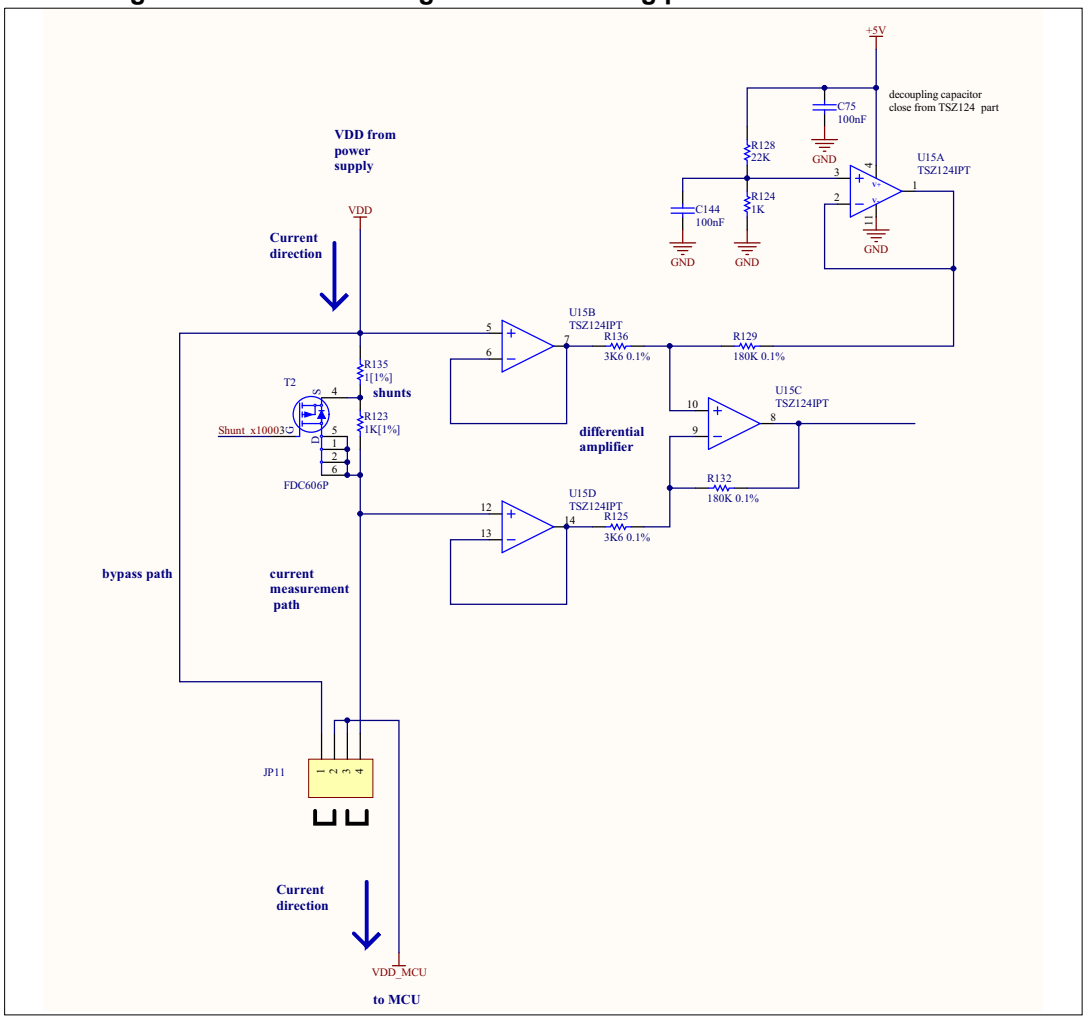
The differential amplifier uses three stages U15B, U15C, U15D of quadruple operational amplifier device U15, TSZ124. The gain is set to 50, so every 1 mA of supply current is represented by additional 50 mV at the U15C output, terminal 8 of U15.

The resistance formed with the series of R135 and R123, when T2 is in high-impedance state, is of 1001 Ω. It makes the voltage on terminal 8 of U15 increase by approximately 50 mV for every µA of MCU power consumption. The full-scale range, with VDD at 1.8 V is about 30 µA.

Even with precision resistors R136, R125, R129, R132 to set the gain of the differential amplifier, the output voltage may theoretically become negative. To avoid the need of negative power supply, a positive offset of about 220 mV is created at the output, at zero current consumption of the MCU. This offset does not need to be precise. Any dispersion is compensated through a calibration procedure detailed in *Section 2.30.4*.

For allowing the IDD measurement, the jumper in the JP11 header must be placed such as to short its terminals 3 and 4.

Figure 17. Schematic diagram of the analog part of IDD measurement

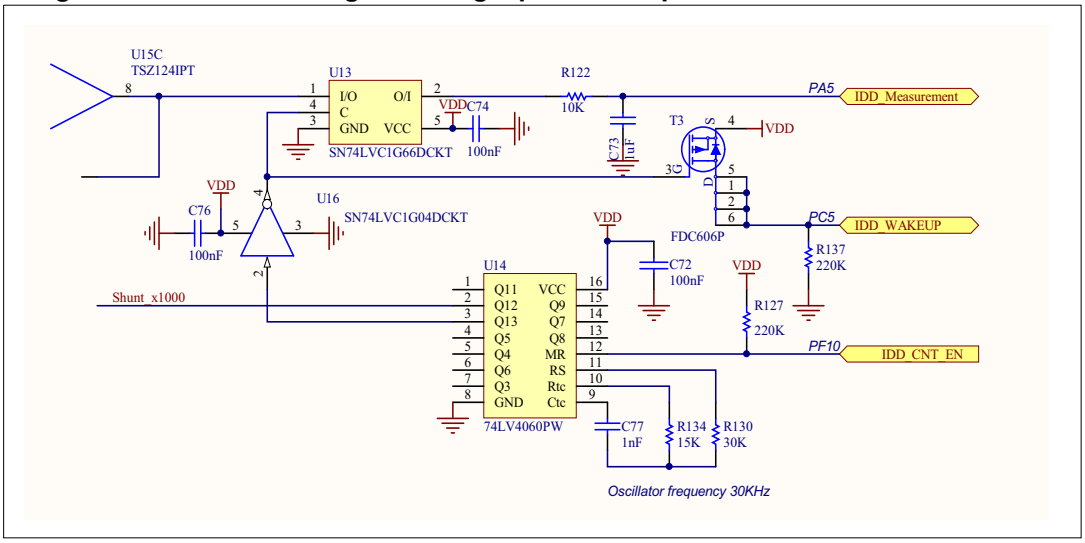


2.30.2 Low-power-mode IDD measurement principle - logic part

The target microcontroller can only carry out actions for measuring a voltage when in dynamic run mode. This is the reason why, voltage representing the current consumed by the microcontroller when in low-power mode needs to be held by a sample-and-hold circuit, for being exploited by the microcontroller at a later time, when back in dynamic run mode. The sample-and-hold (S&H) circuit is built with U13 switch, R122 resistor and C73 sampling capacitor.

The measurement of low-power-mode current consumption is started and end by the microcontroller in its dynamic run mode. As, between the start and end event, the microcontroller must transit through one of its low-power modes, an extra logic is required to time and control events during this state. It consists of U14 counter, U16 inverter and the transistor T3. *Figure 18* shows the corresponding schematic diagram.

Figure 18. Schematic diagram of logic part of low-power-mode IDD measurement



The measurement process consists of 3 phases:

Phase 1 - start and transiting to low-power mode

While in dynamic run mode, the MCU sets IDD_CNT_EN signal on its PF10 port low, starting the measurement process. This makes the counters in U14 start counting the clock pulses generated with an own RC oscillator. At about 150 ms from the start, the Q12 output of U14 goes high, terminating the phase 1. After starting the measurement process, the MCU transits to low-power mode. The duration of the phase 1 of about 150ms allows the MCU enough time for transiting into low-power mode.

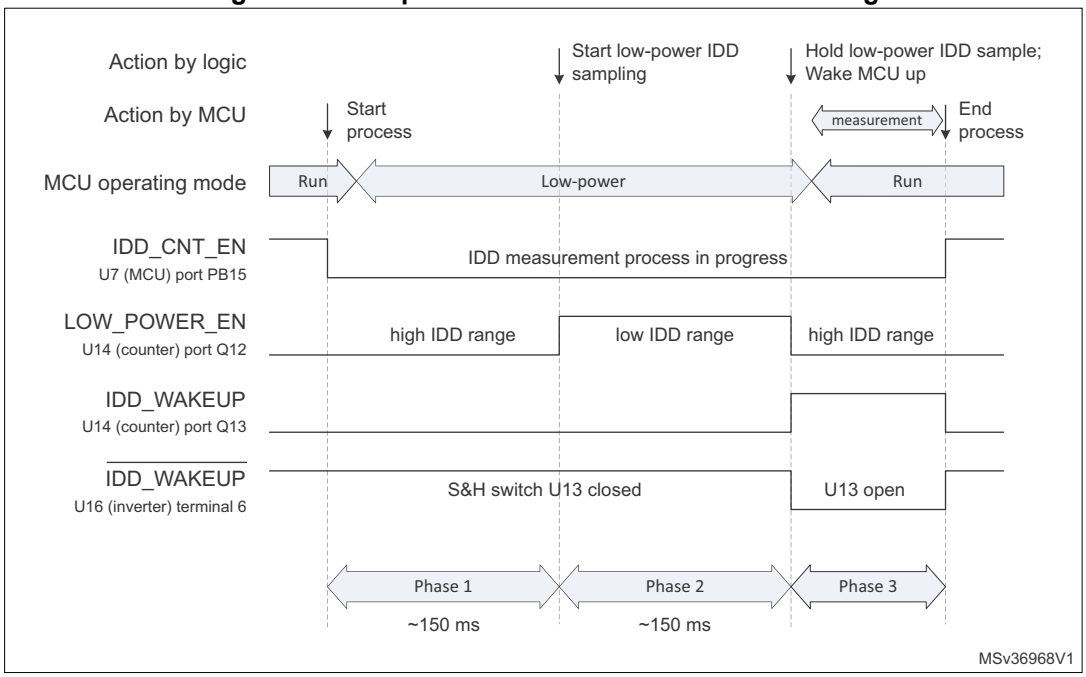
Phase 2 - sampling

The MCU is now in low-power mode. The phase 2 starts with the Q12 port of U14 going high, 150 ms after the MCU, at that time in dynamic run mode, started the low-power-mode consumption current measurement process. The transistor T2 goes in high-impedance mode, which results in setting the analog part in high sensitivity state, needed for measuring very low currents. The Q13 port of U14 keeps the path between ports I/O and O/I of U13 conductive. The sampling capacitor C73 is charged through the resistor R122 to the voltage at the output of the differential analog amplifier, representing the current consumed by the MCU in low-power mode. The duration of the phase 2 is about 150 ms. This time is needed to allow the voltage on the sampling capacitor C73 to stabilize.

Phase 3 - exiting low-power mode, measurement and end

The MCU is in low-power mode. The voltage across C73 capacitor is now stabilized so it represents the current consumed by the MCU in low-power mode. The phase 3 starts with setting the U13 path between ports O/I and I/O to non-conductive state, for the voltage across C73 to hold. The same event causes the IDD_WAKEUP signal for the MCU to change state, to signal to the MCU that the voltage on C73 is now ready for being measured. The MCU transits from low-power mode to dynamic run mode. The voltage on C73 representing the current the MCU consumed when it was in low-power mode, is now measured by the MCU, using the ADC port PA5, and stored. The Q12 port transits to low state at the same time as the Q13 goes high. As a consequence, the analog part of the IDD measurement circuit is back to low-sensitivity mode adapted for measuring the microcontroller supply current in its dynamic run mode. The phase 3 and the whole measurement process ends with the microcontroller setting the IDD_CNT_EN signal back high. *Figure 19* illustrates the timing of the low-power-mode current consumption measurement process.

Figure 19. Low power mode IDD measurement timing



2.30.3 IDD measurement in dynamic run mode

In dynamic run mode, the IDD_CNT_EN remains high. The T2 is in conductive state, setting the shunt resistor to 1 Ω. The U13 path from port 1 to 2 is permanently conductive and the voltage on the capacitor C73 follows the MCU current consumption. R122 allows filtering fast changes.

2.30.4 Calibration procedure

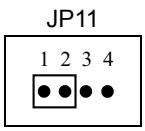
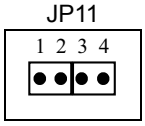
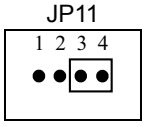
For the measurement to be precise, it is mandatory to perform a calibration before the measurement. The calibration allows subtracting, from the voltage measured across C73, the offset at the differential amplifier output, described in *Section 2.30.1*.

The calibration procedure consists in measuring the offset voltage when the current through the shunt resistor is zero. The current consumption values measured by the microcontroller are then compensated for offset, by subtracting the now-known offset number from the measured number. Setting the current through the shunt resistor to zero is reached through appropriate setting jumpers in the JP11 jumper header.

Calibration procedure and current measurement compensation steps:

- On JP11, short terminals 1,2 and open terminals 3,4. The current through the shunt resistor is now zero.
- Run low-power-mode IDD measurement as described in *Section 2.30.2*. The value V_{offset} measured corresponds to offset of the differential amplifier.
- On JP11, add a second jumper, to short terminals 3 and 4, then remove the jumper from terminals 1,2 of JP11. The MCU supply has not been interrupted and the supply current now passes through the shunt resistor.
- Run low-power-mode IDD measurement as described in *Section 2.30.2*. The value $V_{measured}$ obtained corresponds to the sum of MCU supply current and the differential amplifier's offset V_{offset}.
- The software computes a V_{out} number representing the MCU supply current as **$V_{out} = V_{measured} - V_{offset}$**

Table 31. JP11 jumper settings during IDD measurement with calibration

Jumper	Setting	Description
JP11		Configuration used to measure V_{offset}. JP11 in VDD position STM32L476ZGT6 supply current does not flow through shunt resistor.
		Configuration to transit from direct to shunted supply to STM32L476ZGT6, without ever interrupting the MCU supply.
		**Default setting.** Configuration used to measure the MCU supply current. JP11 in IDD position STM32L476ZGT6 supply current flows through shunt resistor.

3 Connectors

3.1 RS-232 D-sub male connector CN9

Figure 20. RS-232 D-sub (DE-9M) 9-pole connector (front view)

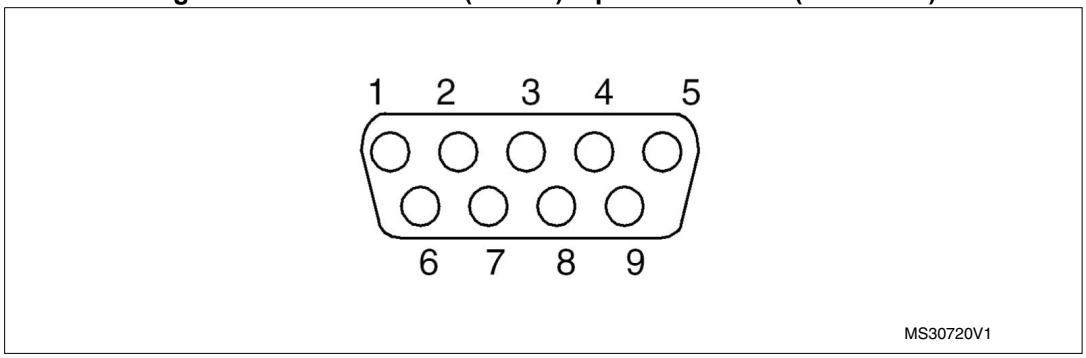


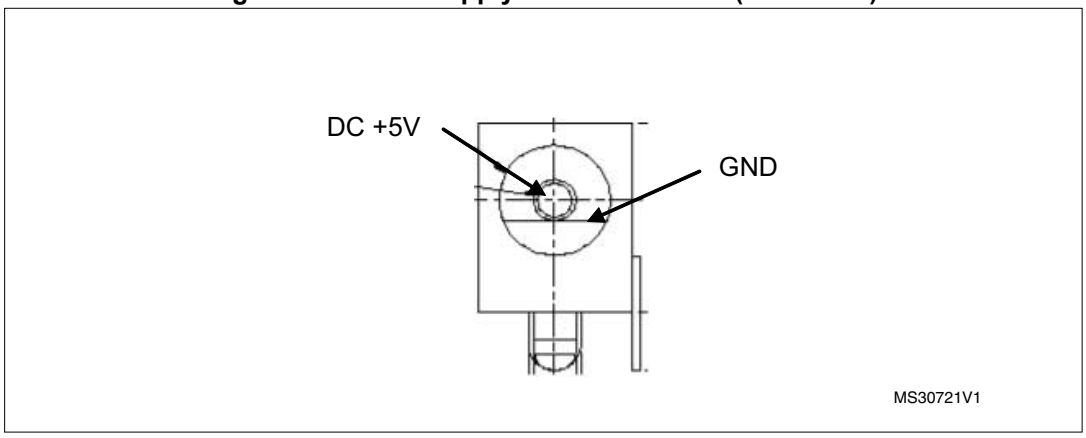
Table 32. RS-232 D-sub (DE-9M) connector CN9 with HW flow control and ISP support

Terminal	Terminal name	Terminal	Description
1	NC	6	Bootloader_BOOT0
2	RS232_RX (PB7)	7	NC
3	RS232_TX (PG12)	8	Bootloader_RESET
4	NC	9	NC
5	GND	-	-

3.2 Power connector CN22

The STM32L476G-EVAL board can be powered from a DC-5V external power supply via the CN22 jack illustrated in *Figure 21*. The central pin of CN22 must be positive.

Figure 21. Power supply connector CN22 (front view)



3.3 LCD daughterboard connectors CN11 and CN14

Two 48-pin male headers CN11 and CN14 are used to connect to LCD glass module daughterboard MB979. The type of connectors, their mutual orientation, distance and terminal assignment are kept for a number of ST MCU evaluation boards. This standardization allows developing daughterboards that can be used in multiple evaluation kits. The width between CN11 pin1 and CN14 pin1 is 700 mils (17.78 mm).

STM32L476ZGT6 ports routed to these two connectors can be accessed on odd CN11 and CN14 pins (the row of pin 1), when no daughterboard is plugged in.

Daughterboards plugging into CN11 and CN14 must keep the even terminals of CN11 and CN14 open.

Table 33 shows the signal assignment to terminals.

Table 33. CN11 and CN14 daughterboard connectors

CN11		CN14	
Odd pin	**MCU port**	**Odd pin**	**MCU port**
1	PA9	1	PD2
3	PA8	3	PC12
5	PA10	5	PC11
7	PB9	7	PC10
9	PB11	9	PC3
11	PB10	11	PC4
13	PB5	13	PC5
15	PB14	15	PC6
17	PB13	17	PC7
19	PB12	19	PC8
21	PA15	21	PC9
23	PB8	23	PD8
25	PB15	25	PD9
27	PC2	27	PD10
29	PC1	29	PD11
31	PC0	31	PD12
33	PA3	33	PD13
35	PA2	35	PD14
37	PB0	37	PD15
39	PA7	39	PE0
41	PA6	41	PE1
43	PB4	43	PE2

Table 33. CN11 and CN14 daughterboard connectors (continued)

CN11		CN14	
Odd pin	MCU port	Odd pin	MCU port
45	PB3	45	PE3
47	PB1	47	PA1

3.4 Extension connectors CN6 and CN7

Table 34. Daughterboard extension connector CN6

Pin	Description	Alternative Functions	How to disconnect Alternative functions to use on the extension connector
1	GND	-	-
3	PG6	CODEC_INT, MC_ICL_Shutout	Remove R35, Open SB5
5	PA13	TMS/SWDIO	Don’t use Trace connector CN12 and JTAG connector CN15
7	PA12	USBOTG_DP	Remove R4
9	PG8	LPUART_RX_3V3	Remove R158, R188
11	GND	-	-
13	PG2	A12	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5
15	PD3	DFSDM_DATIN1	Remove R23
17	PD0	D2	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5
19	PD5	FMC_NWE	Can not be disconnected from SRAM and Flash memory, but is an input for SRAM and Flash memory
21	PG10	LCD_NE3	Can not be disconnected from TFT LCD level shifters U21 and U22, but is an input for TFT LCD.
23	PD7	FMC_NE1	Remove R18
25	PF0	A0	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5
27	PG11	USART1_CTS_3V3	Remove R93
29	PG13	I2C_SDA	Remove R58
31	PG12	USART1_RTS	Remove R116
33	PG14	I2C_SCL	Remove R61
35	PG15	IOExpander_INT	Remove R228
37	PF4	A4	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5

Table 34. Daughterboard extension connector CN6 (continued)

Pin	Description	Alternative Functions	How to disconnect Alternative functions to use on the extension connector
39	GND	-	-
2	+3V3	-	-
4	PG7	LPUART_TX	Remove R119, R189
6	PA11	USBOTG_DM	Remove R3
8	PA14	TCK/SWCLK	Don't use Trace connector CN12 and JTAG connector CN15
10	PG5	A15	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5
12	PG3	A13	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5
14	PG4	A14	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5
16	PD1	D3	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5
18	PD4	FMC_NOE	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5
20	PG9	FMC_NE2	Remove R43
22	GND	-	-
24	PD6	SAI1_SDA, FMC_NWAIT	Remove R53, open SB10
26	PF1	A1	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5
28	D5V	-	-
30	PC13	Wake-up	Remove R244
32	PF2	A2	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5
34	PF3	A3	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5
36	GND	-	-
38	PF5	A5	Remove R18 to deselect SRAM U2 Remove R43 to deselect Flash memory U5
40	PB6	USART1_TX	Remove R118

Table 35. Daughterboard extension connector CN7

Pin	Description	Alternative Functions	How to disconnect Alternative functions to use on the extension connector
1	GND	-	-
3	PE14	D11	-

Table 35. Daughterboard extension connector CN7 (continued)

Pin	Description	Alternative Functions	How to disconnect Alternative functions to use on the extension connector
5	PE12	D9	-
7	PE10	D7	-
9	PE8	D5	-
11	PG1	A11	-
13	PB2	LED1, MC_DissipativeBrake	Remove R54, SB11
15	GND	-	-
17	PF12	A6	-
19	PF11	NFC_NSS	Don’t connect the NFC daughterboard to connector CN13
21	PE4	A20, TRACE_D1	Remove R84, SB40
23	PE5	A21, TRACE_D2	Remove R85, SB38
25	PC14	OSC32_IN	Remove R87, Close SB41
27	PF6	SAI1_SDB	Remove R105
29	PF9	SAI1_FSB, MC_PFC_sync	Remove R90, SB25
31	PF10	IDD_CNT_EN, MC_PFC_PWM	Remove R91, SB37
33	PH1	OSC_OUT	Remove R95, close SB23
35	PA5	IDD_Measurement	Remove R69
37	PA0	OpAmp1_INP, MC_EncA	Remove R83, SB35
39	GND	-	-
2	PE15	D12	-
4	PE13	D10	-
6	PE11	D8	-
8	PE9	D6	-
10	PE7	D4	-
12	PG0	A10	-
14	PF15	A9	-
16	PF14	A8	-
18	PF13	A7	-
20	BOOT0	BootLoader from UART	Remove JP8
22	PE6	A21, TRACE_D3	Remove R86, SB39
24	PC15	OSC32_OUT	Remove R88, close SB33

Table 35. Daughterboard extension connector CN7 (continued)

Pin	Description	Alternative Functions	How to disconnect Alternative functions to use on the extension connector
26	GND	-	-
28	PF7	SAI1_MCKB	Remove R106
30	PF8	SAI1_SCKB	Remove R89
32	RESET#	-	-
34	PH0	OSCIN	Remove crystal X2, C54, close SB24
36	PC3	VLCD	Remove R94
38	PA4	ADC_DAC	Remove R73
40	VDD	-	-

3.5 ST-LINK/V2-1 programming connector CN16

The connector CN16 is used only for embedded ST-LINK/V2-1 programming, during board manufacture. It is not populated by default and not for use by the end user.

3.6 ST-LINK/V2-1 Standard-B USB connector CN17

The USB connector CN17 is used to connect the on-board ST-LINK/V2-1 facility to PC for flashing and debugging software.

Figure 22. USB type B connector CN17 (front view)

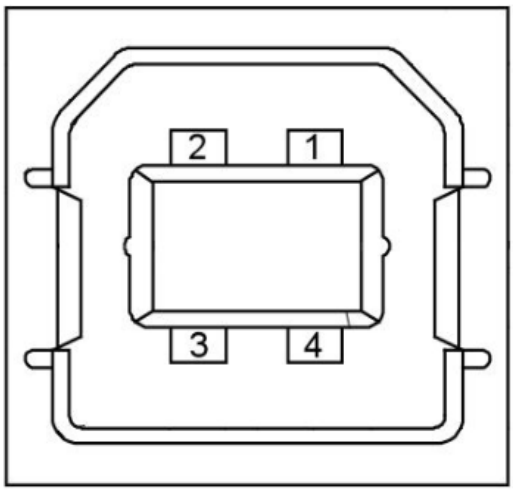


Table 36. USB Standard-B connector CN17

Terminal	Description	Terminal	Description
1	VBUS(power)	4	GND
2	DM	5,6	Shield
3	DP	-	-

3.7 JTAG connector CN15

Figure 23. JTAG debugging connector CN15 (top view)

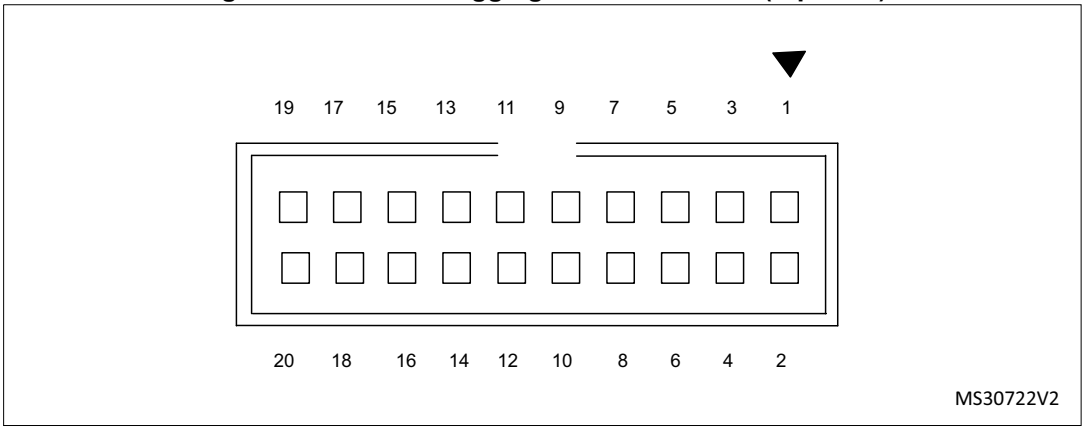


Table 37. JATG debugging connector CN15

Terminal	Function / MCU port	Terminal	Function / MCU port
1	VDD power	2	VDD power
3	PB4	4	GND
5	PA15	6	GND
7	PA13	8	GND
9	PA14	10	GND
11	RTCK	12	GND
13	PB3	14	GND
15	RESET#	16	GND
17	DBGRQ	18	GND
19	DBGACK	20	GND

3.8 ETM trace debugging connector CN12

Figure 24. Trace debugging connector CN12 (top view)

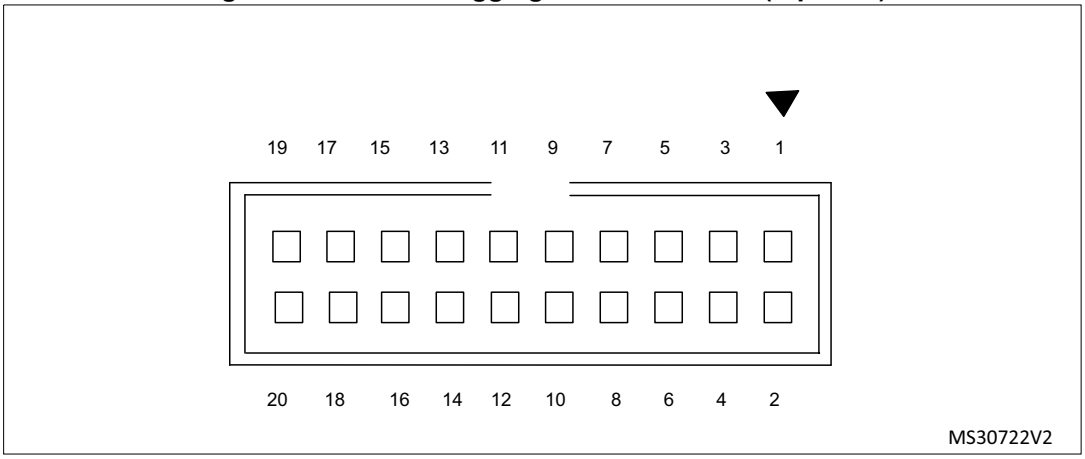


Table 38. Trace debugging connector CN12

Terminal	Function / MCU port	Terminal	Function / MCU port
1	VDD power	2	TMS/PA13
3	GND	4	TCK/PA14
5	GND	6	TDO/PB3
7	KEY	8	TDI/PA15
9	GND	10	RESET#
11	GND	12	TraceCLK/PE2
13	GND	14	TraceD0/PE3 or SWO/PB3
15	GND	16	TraceD1/PE4 or nTRST/PB4
17	GND	18	TraceD2/PE5
19	GND	20	TraceD3/PE6

3.9 microSD card connector CN18

Figure 25. microSD card connector CN18

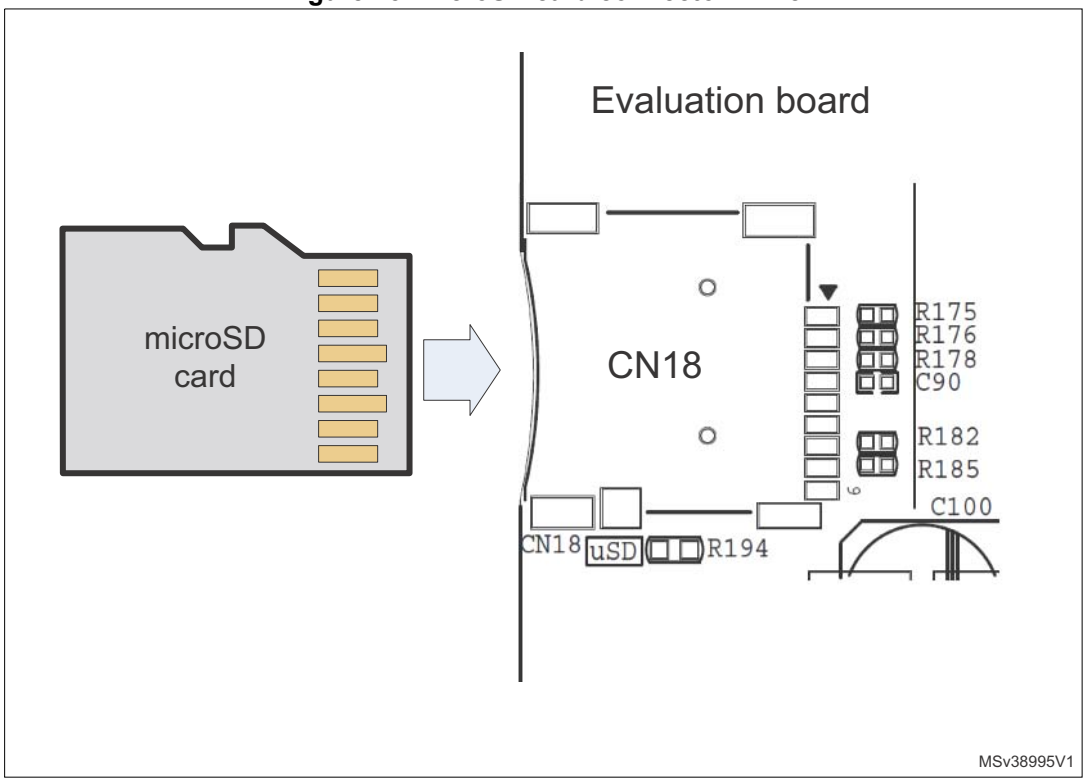


Table 39. microSD card connector CN18

Terminal	Terminal name (MCU port)	Terminal	Terminal name (MCU port)
1	SDIO_D2 (PC10)	6	Vss/GND
2	SDIO_D3 (PC11)	7	SDIO_D0 (PC8)
3	SDIO_CMD (PD2)	8	SDIO_D1 (PC9)
4	VDD	9	GND
5	SDIO_CLK (PC12)	10	MicroSDcard_detect (PA8)

3.10 ADC/DAC connector CN8

Figure 26. Analog input-output connector CN8 (top view)

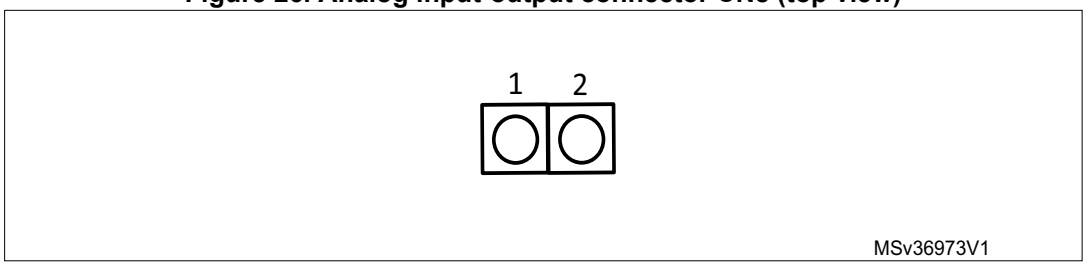


Table 40. Analog input-output connector CN8

Terminal	Function / MCU port	Terminal	Function / MCU port
1	GND	2	analog input-output PA4

3.11 RF-EEPROM daughterboard connector CN3

Figure 27. RF EEPROM daughterboard connector CN3 (front view)

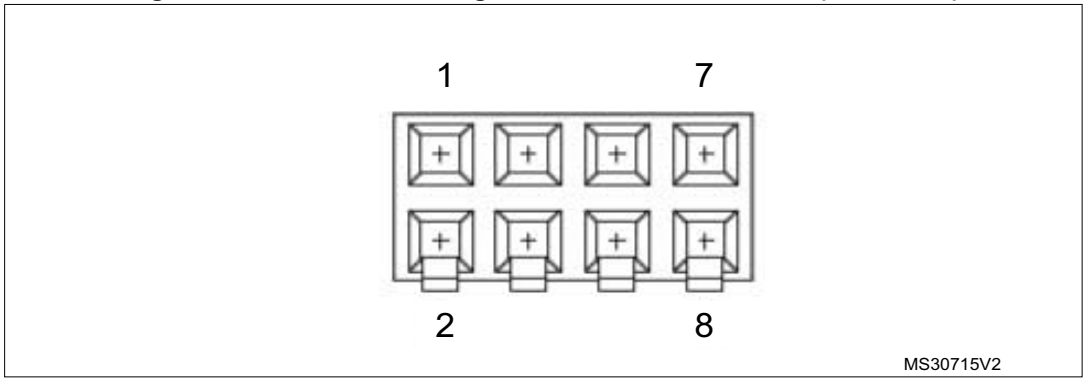


Table 41. RF-EEPROM daughterboard connector CN3

Terminal	Terminal name (MCU port)	Terminal	Terminal name (MCU port)
1	I2C_SDA (PG13)	5	+3V3
2	NC	6	NC
3	I2C_SCL (PG14)	7	GND
4	EXT_RESET(PC6)	8	+5 V

3.12 Motor control connector CN2

Figure 28. Motor control connector CN2 (top view)

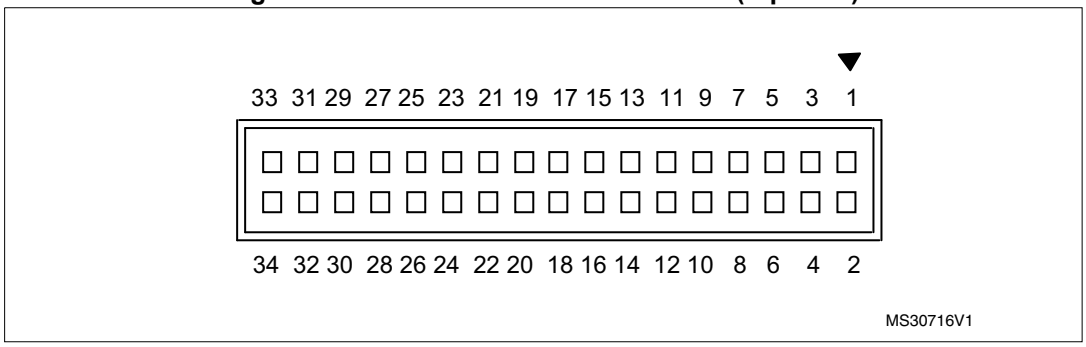
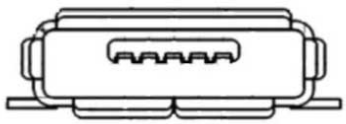


Table 42. Motor control connector CN2

CN2 terminal	Description	MCU port	CN2 terminal	MCU port	Description
1	Emergency STOP	PC9	2	-	GND
3	PWM_1H	PC6	4	-	GND
5	PWM_1L	PA7	6	-	GND
7	PWM_2H	PC7	8	-	GND
9	PWM_2L	PB0	10	-	GND
11	PWM_3H	PC8	12	-	GND
13	PWM_3L	PB1	14	PC5	BUS VOLTAGE
15	CURRENT A	PC0	16	-	GND
17	CURRENT B	PC1	18	-	GND
19	CURRENT C	PC2	20	-	GND
21	ICL Shutout	PG6	22	-	GND
23	DISSIPATIVE BRAKE	PB2	24	PC4	PCD Ind Current
25	+5V power	-	26	PA3	Heat sink temperature
27	PFC SYNC	PF9	28	-	3.3 V power
29	PFC PWM	PF10	30	PB12	PFC Shut Down
31	Encoder A	PA0	32	PA6	PFC Vac
33	Encoder B	PA1	34	PA2	Encoder Index

3.13 USB OTG FS Micro-AB connector CN1

Figure 29. USB OTG FS Micro-AB connector CN1 (front view)



MS36975V1

Table 43. USB OTG FS Micro-AB connector CN1

Terminal	Terminal name (MCU port)	Terminal	Terminal name (MCU port)
1	VBUS (PA9 & PB13)	4	ID (PA10)
2	D- (PA11)	5	GND
3	D+ (PA12)	-	-

3.14 CAN D-sub male connector CN5

Figure 30. CAN D-sub (DE-9M) 9-pole male connector CN5 (front view)

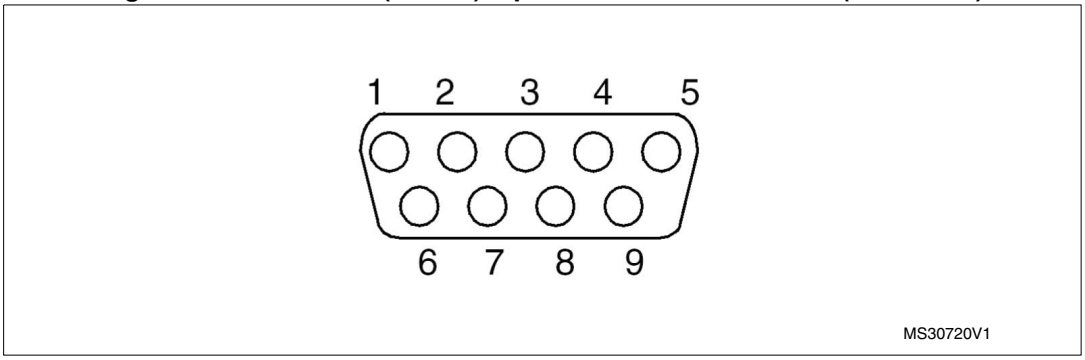


Table 44. CAN D-sub (DE-9M) 9-pins male connector CN5

Terminal	Terminal name	Terminal	Terminal name
1,4,8,9	NC	7	CANH
2	CANL	3,5,6	GND

3.15 NFC connector CN13

Figure 31. NFC female connector CN13 (top view)

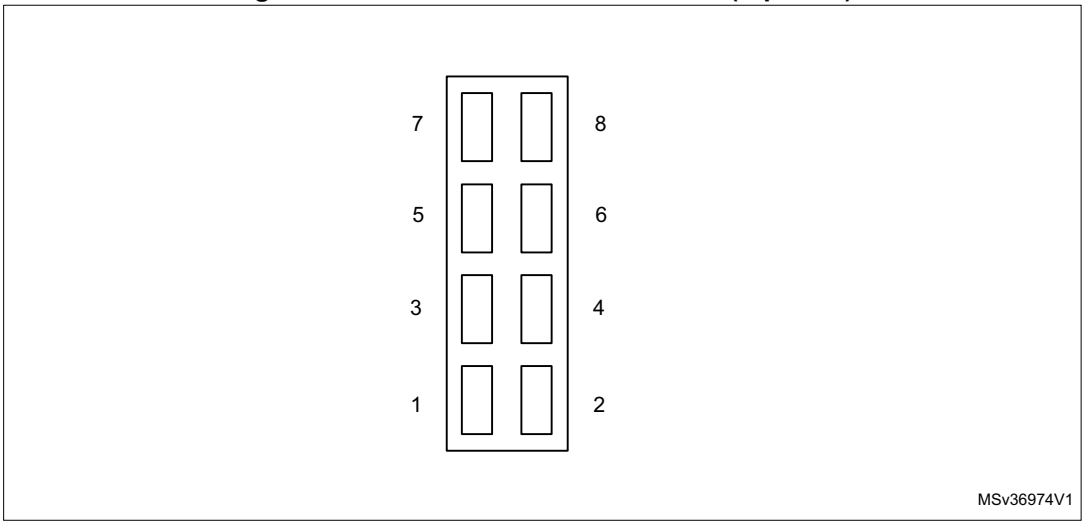


Table 45. NFC CN13 terminal assignment

CN13 terminal	NFC signal	MCU port	Description
1	NFC_IRQOUTN or UART_TX	PB7	Interrupt output for NFC Connected to STM32L476ZGT6 UART RX
2	NFC_IRQINN or UART_RX	PB6	Interrupt input for CR95HF Connected to STM32L476ZGT6 UART TX

Table 45. NFC CN13 terminal assignment (continued)

CN13 terminal	NFC signal	MCU port	Description
3	NFC_NSS	PF11	SPI slave select
4	NFC_MISO	PB14	SPI data, slave output
5	NFC_MOSI	PB15	SPI data, slave input
6	NFC_SCK	PB13	SPI serial clock
7	+3V3	PB6	Main power supply/power supply for RF drivers
8	GND	PB7	Ground

Appendix A Schematic diagrams

Figure 32. STM32L476G-EVAL top schematic diagram

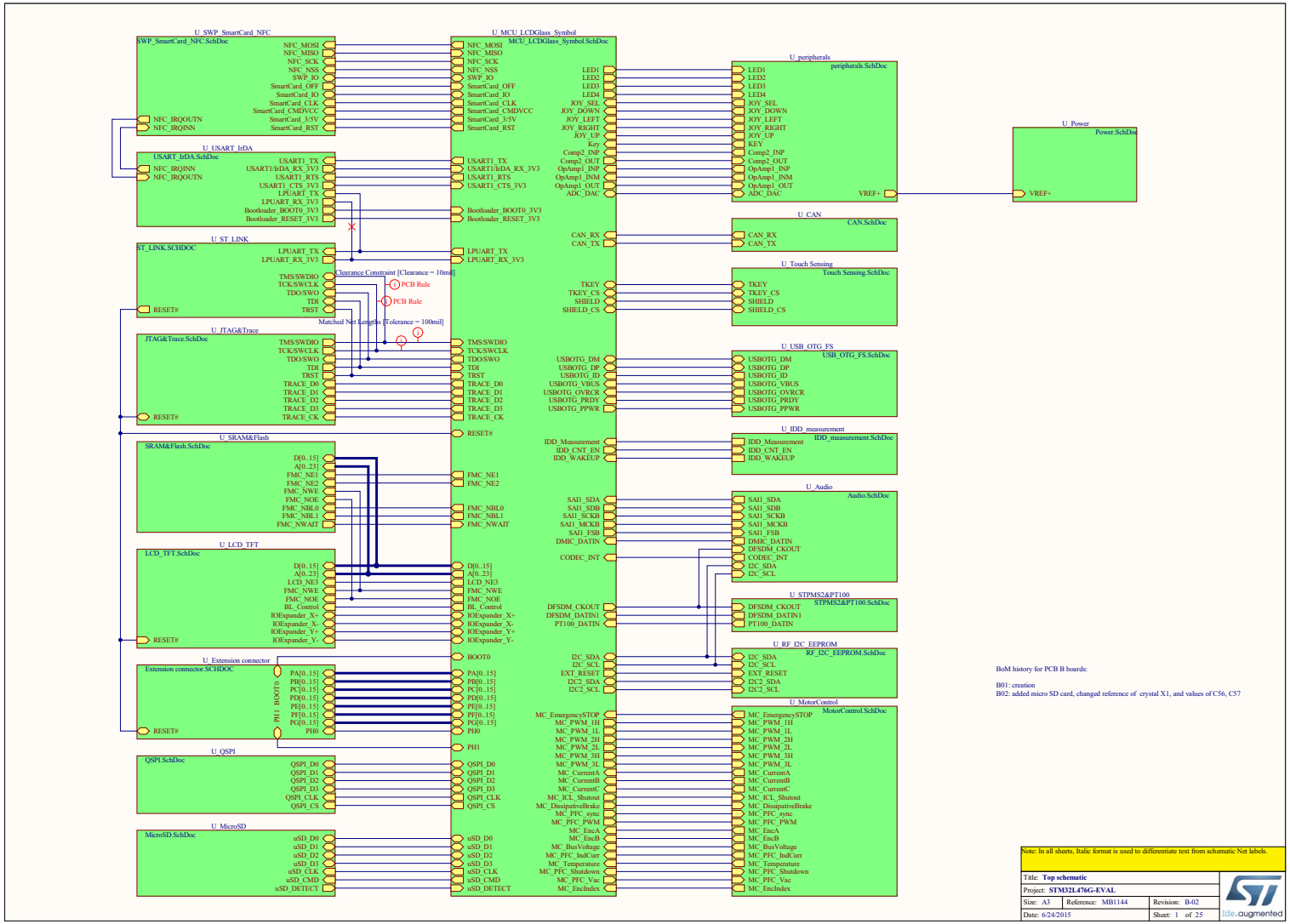


Figure 33. MCU, LCD daughterboard and I/O expander interfaces - schematic diagram

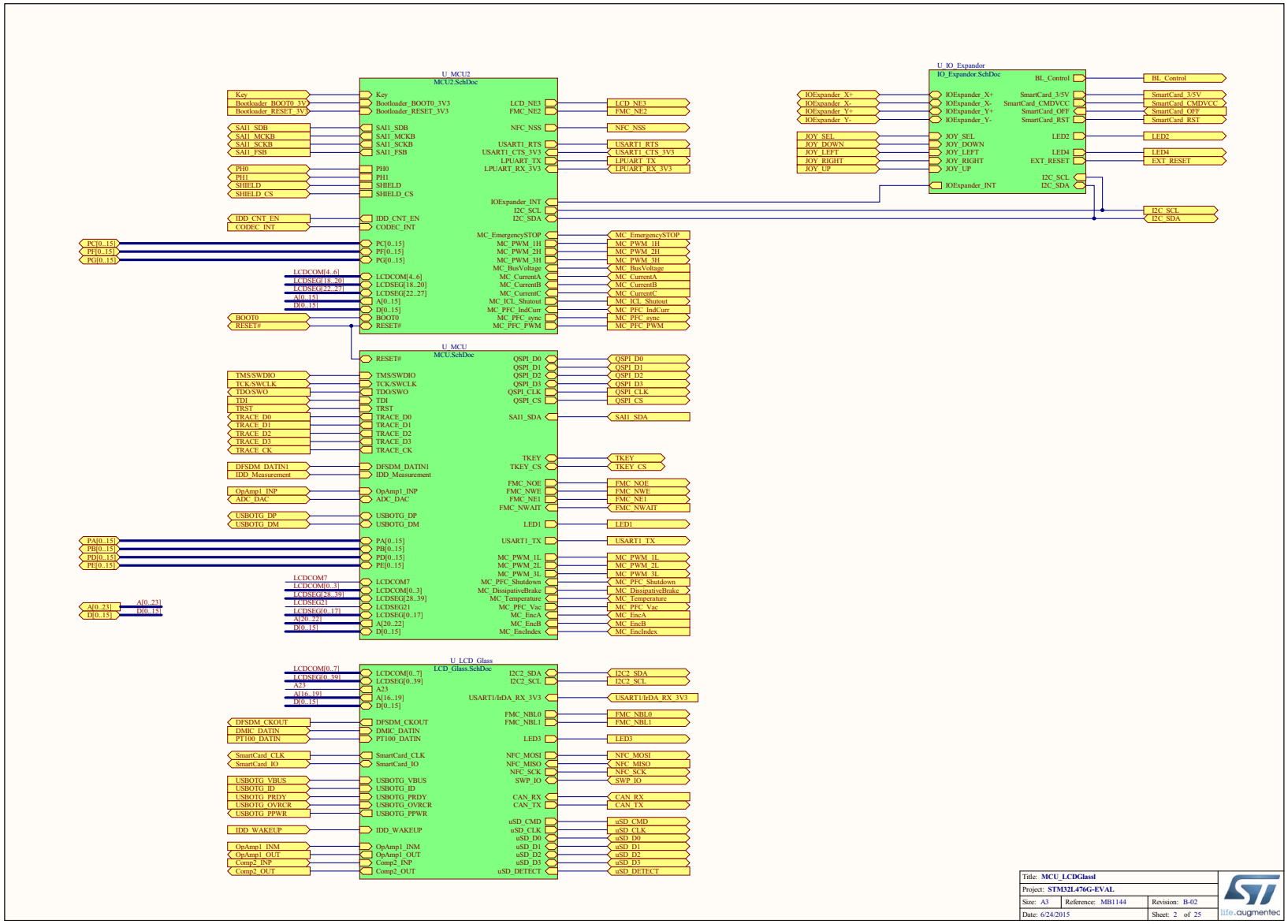


Figure 34. STM32L476G-EVAL MCU part 1 - schematic diagram

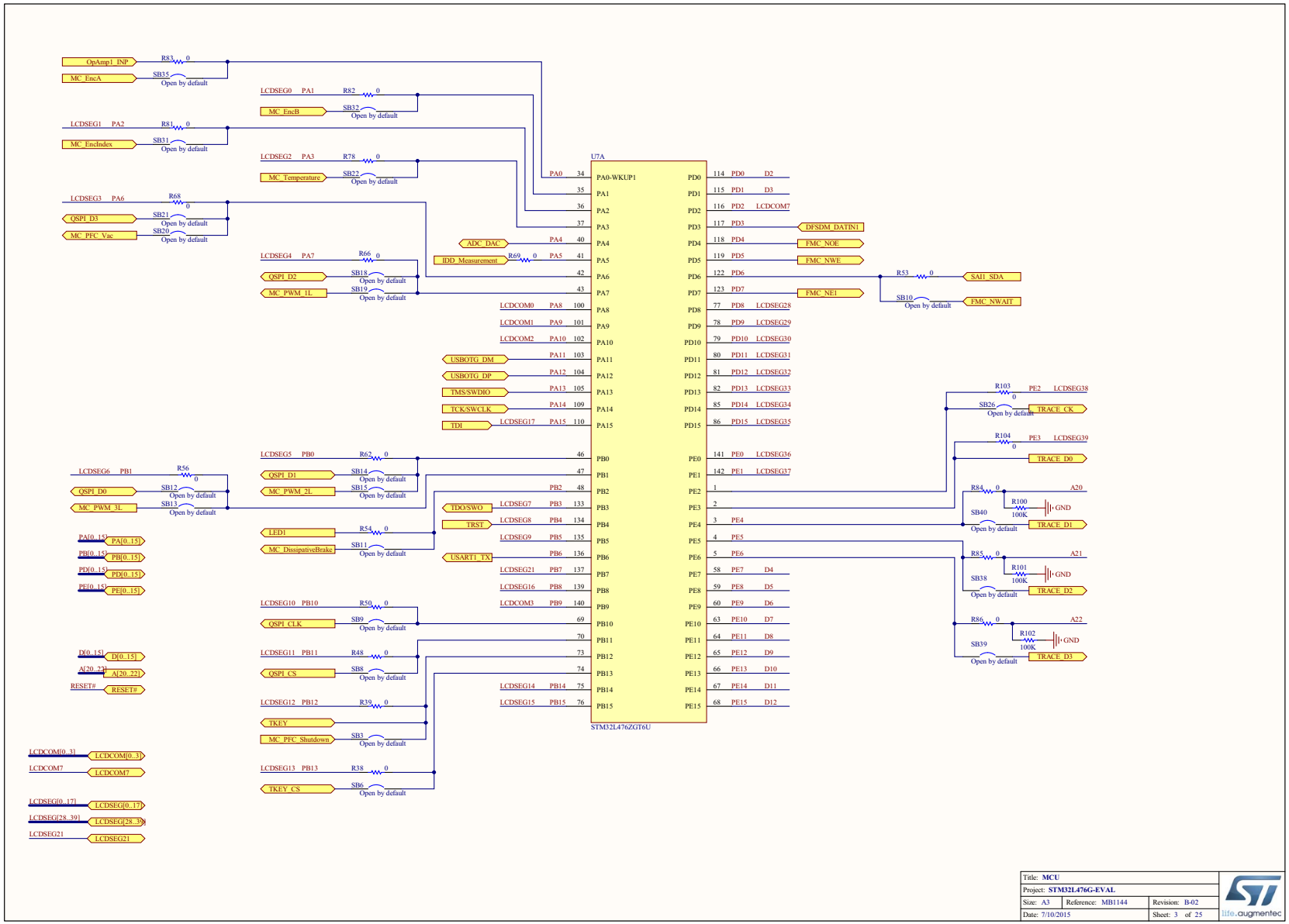


Figure 35. STM32L476G-EVAL MCU part 2 - schematic diagram

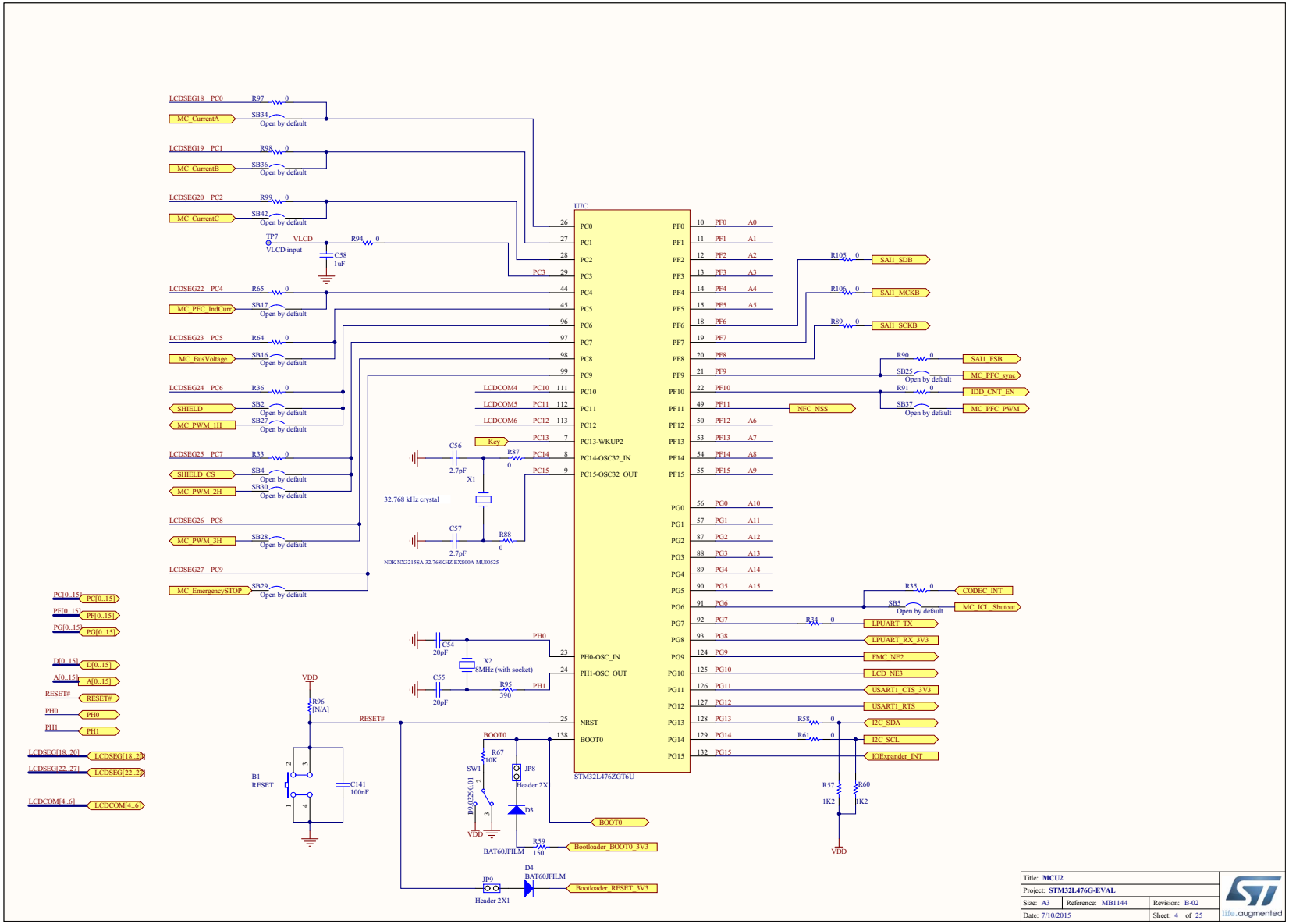


Figure 36. LCD glass module daughterboard connectors - schematic diagram

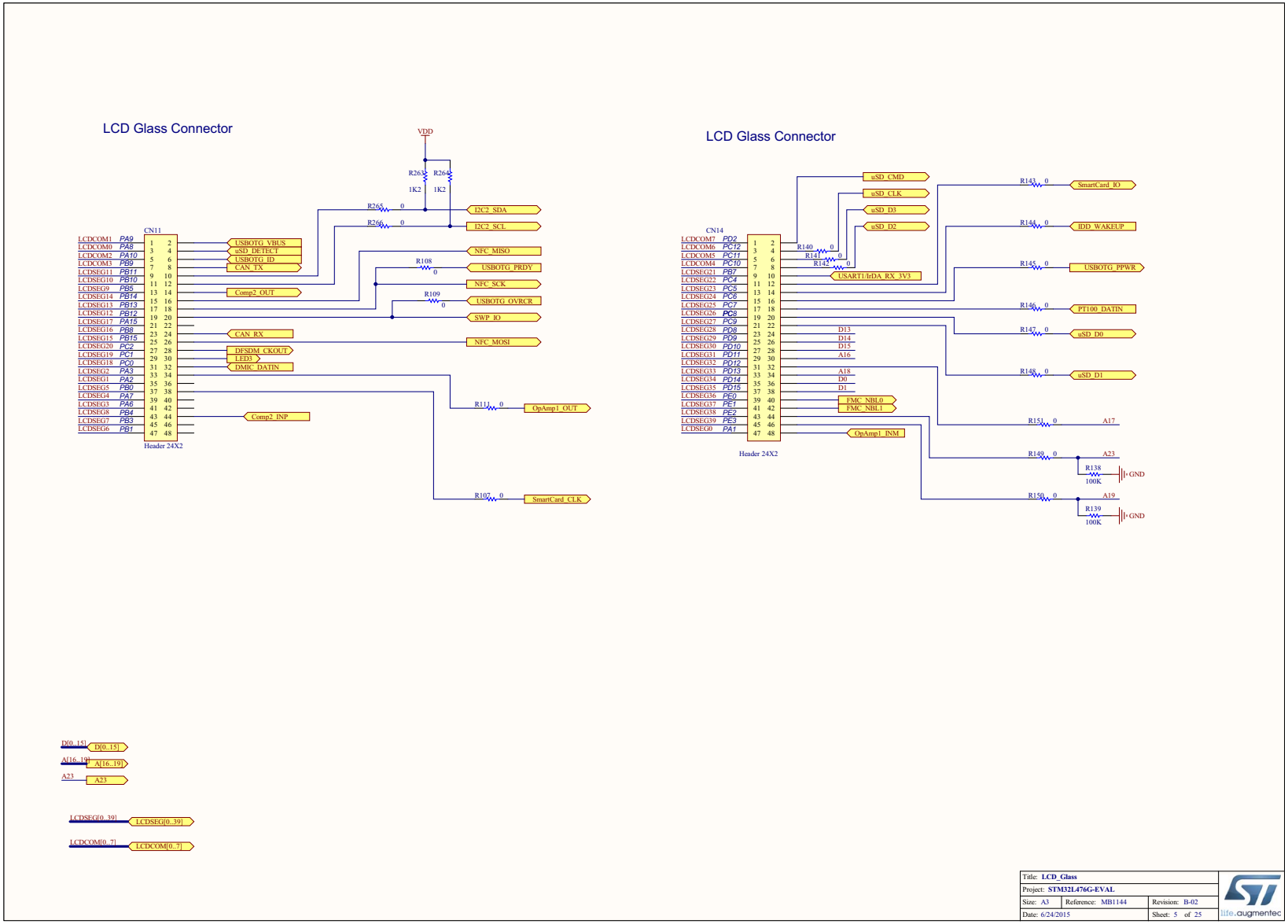


Figure 37. I/O expander schematic diagram

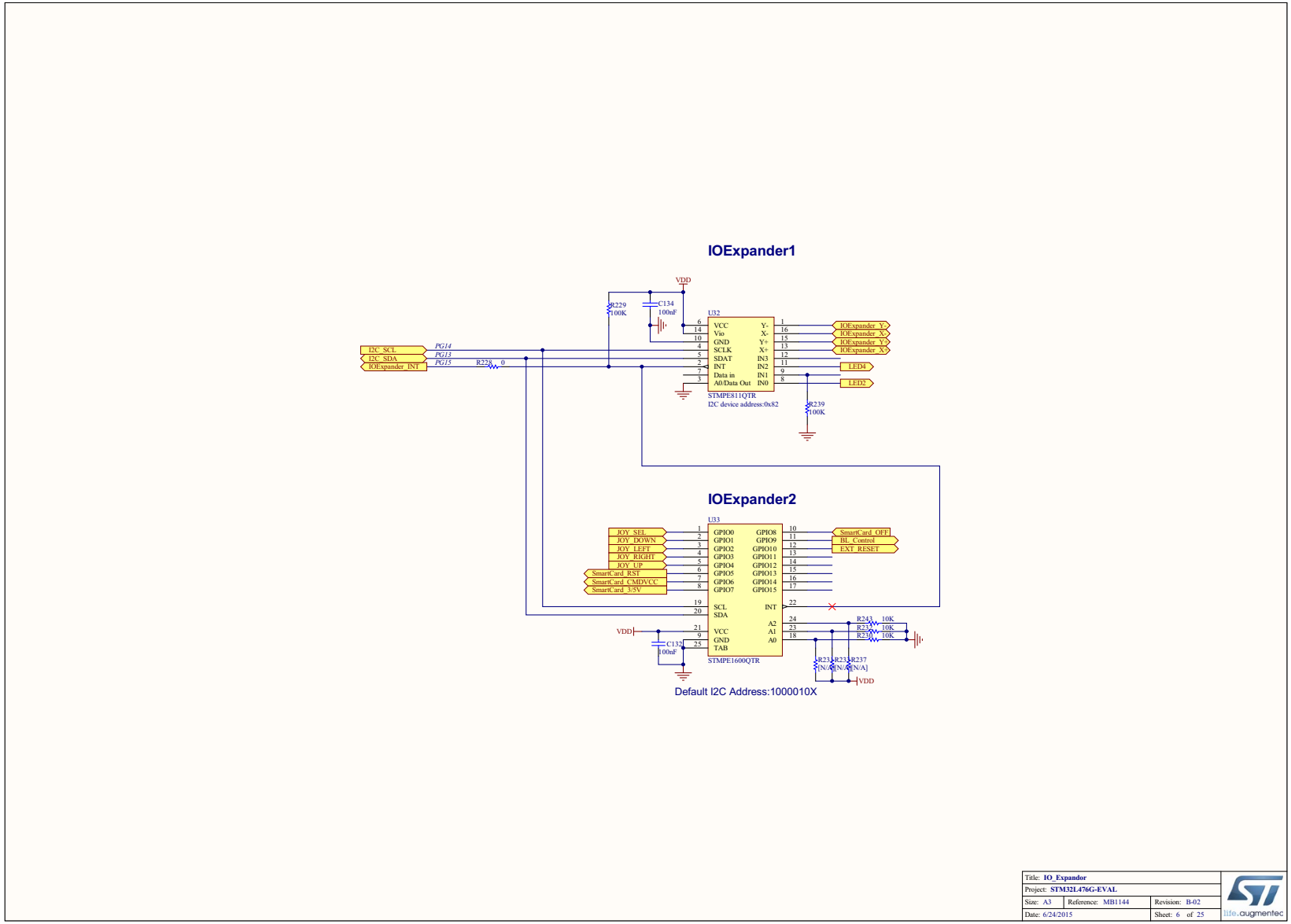


Figure 38. Power supply schematic diagram

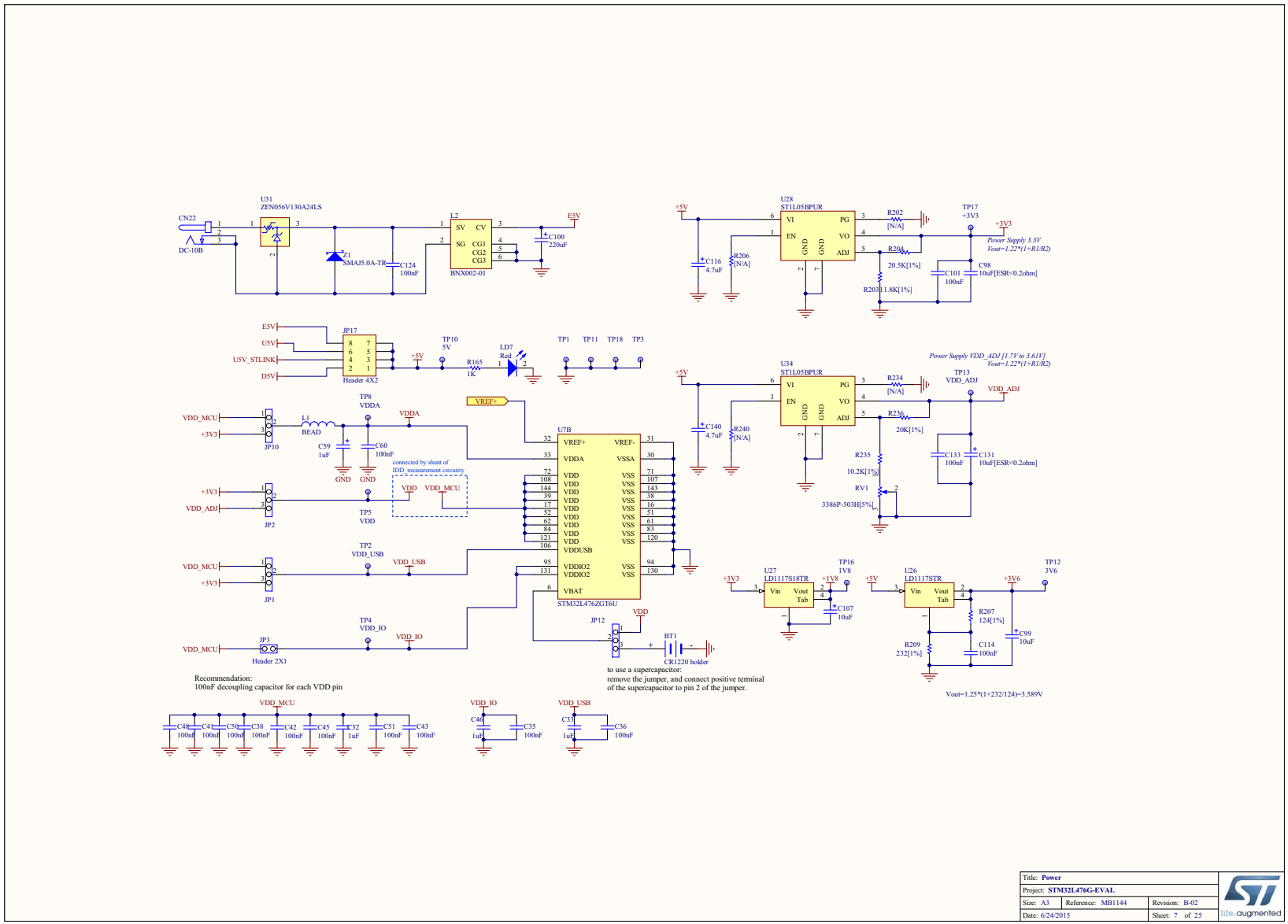


Figure 39. Smartcard, SWP and NFC - schematic diagram

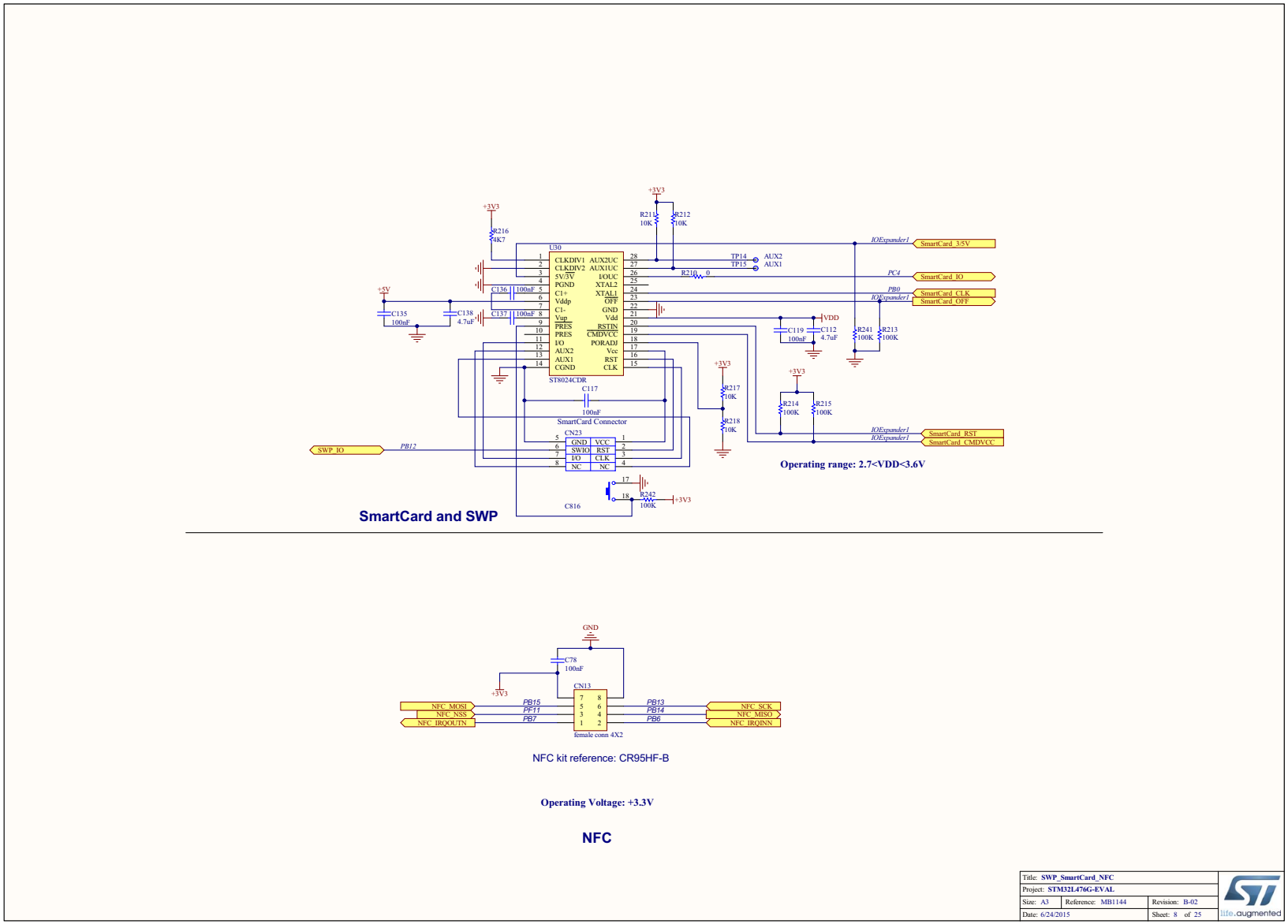


Figure 40. USART and IrDA - schematic diagram

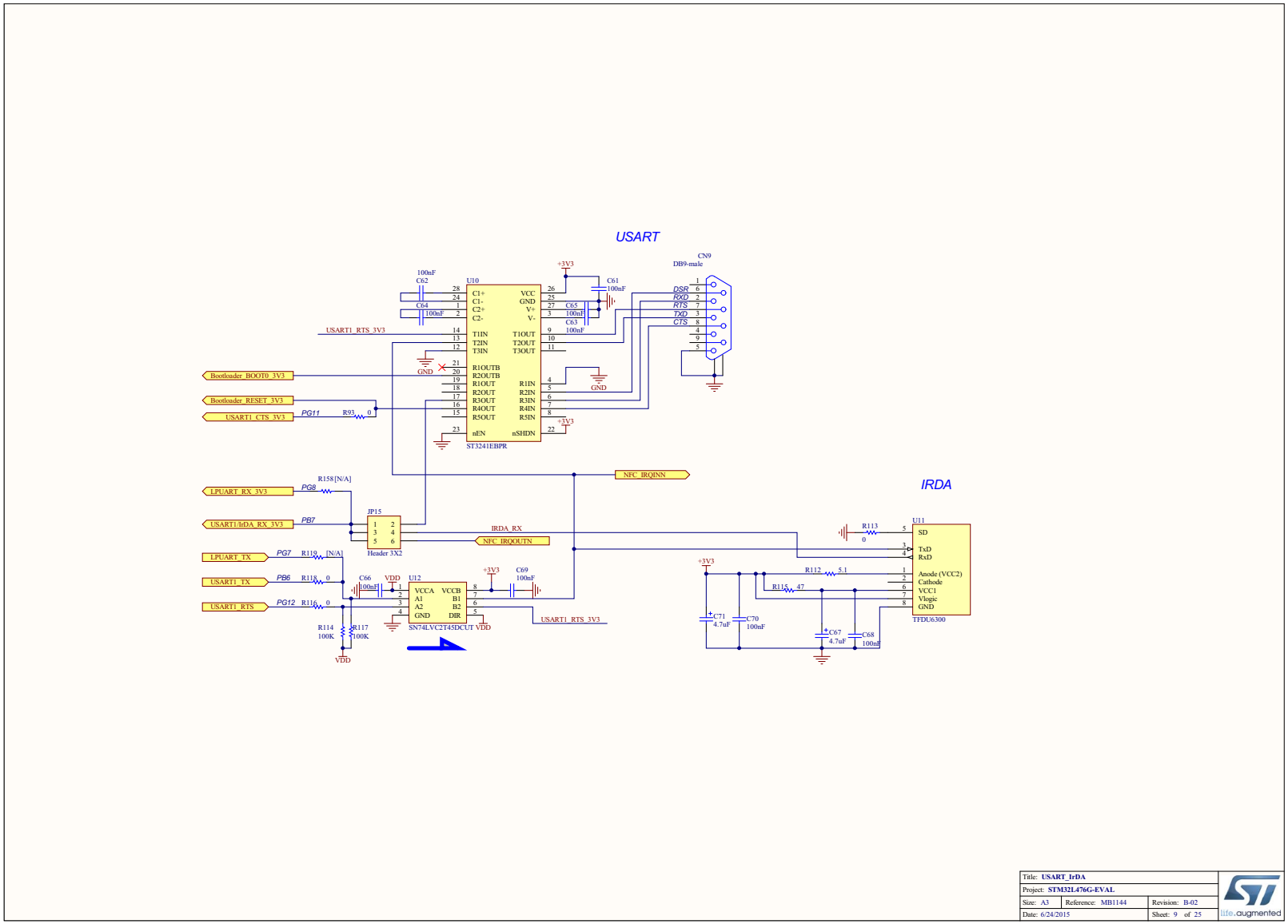


Figure 41. SRAM and NOR Flash memory devices - schematic diagram

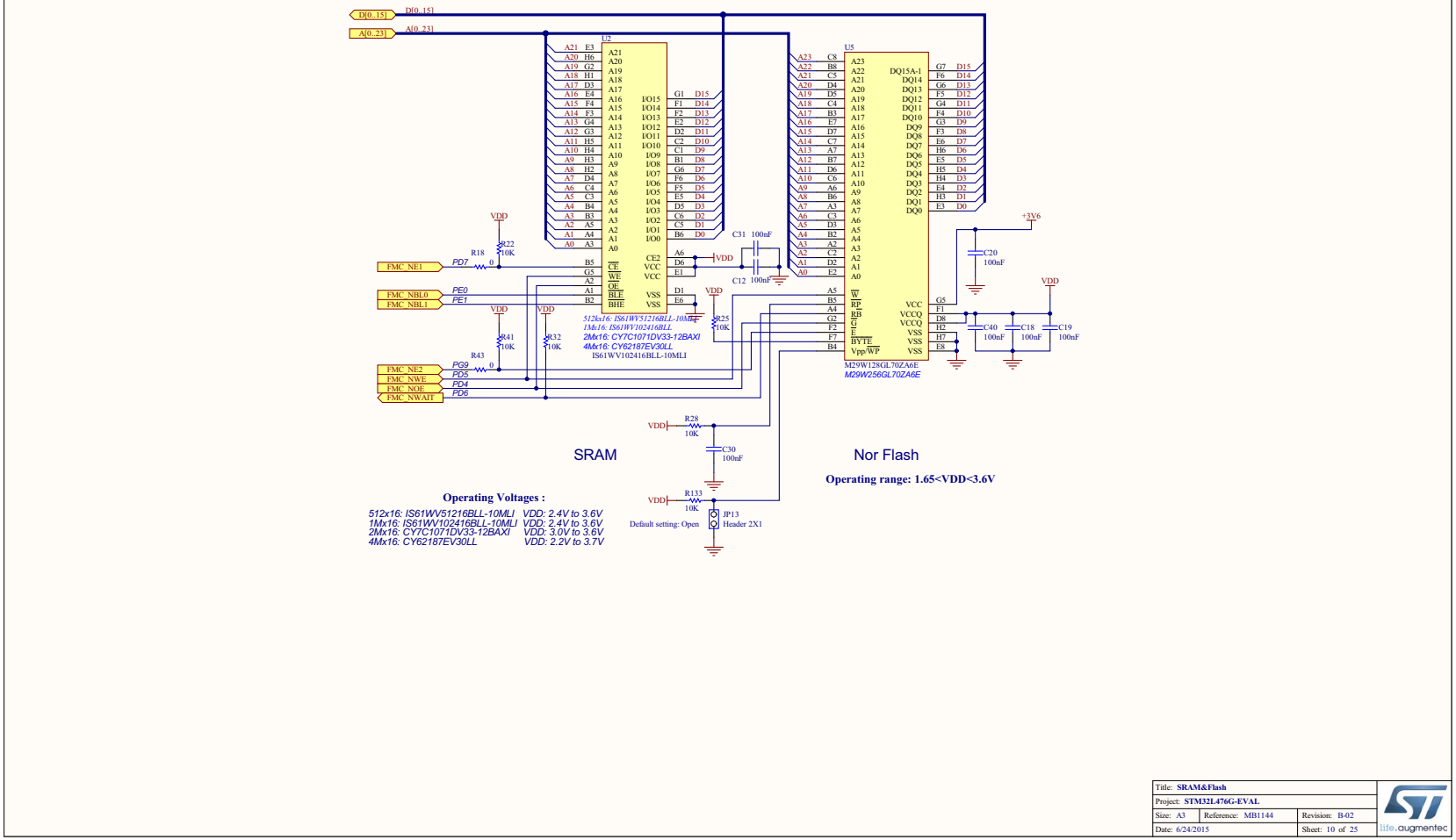


Figure 42. TFT LCD schematic diagram

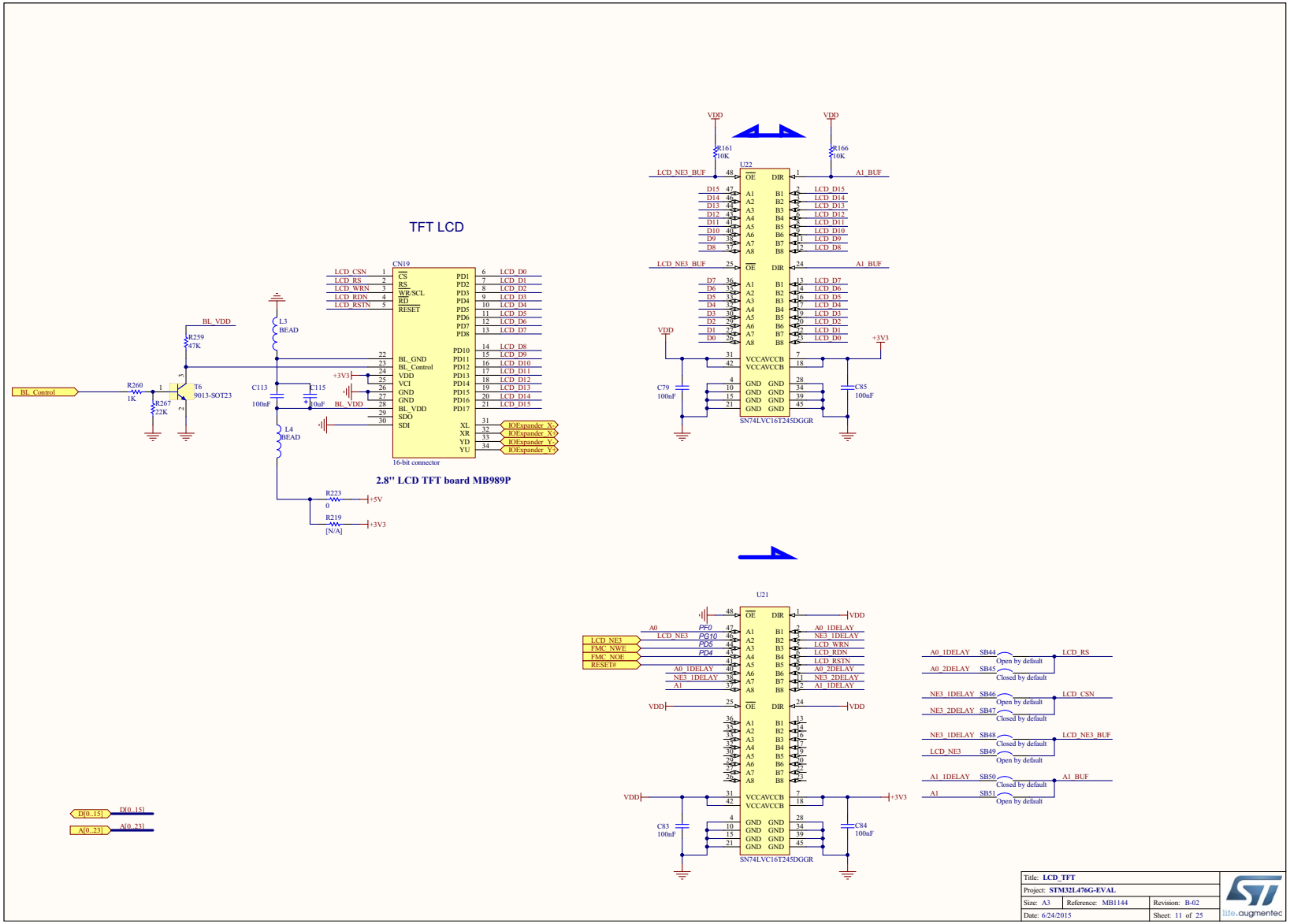


Figure 43. Extension connector schematic diagram

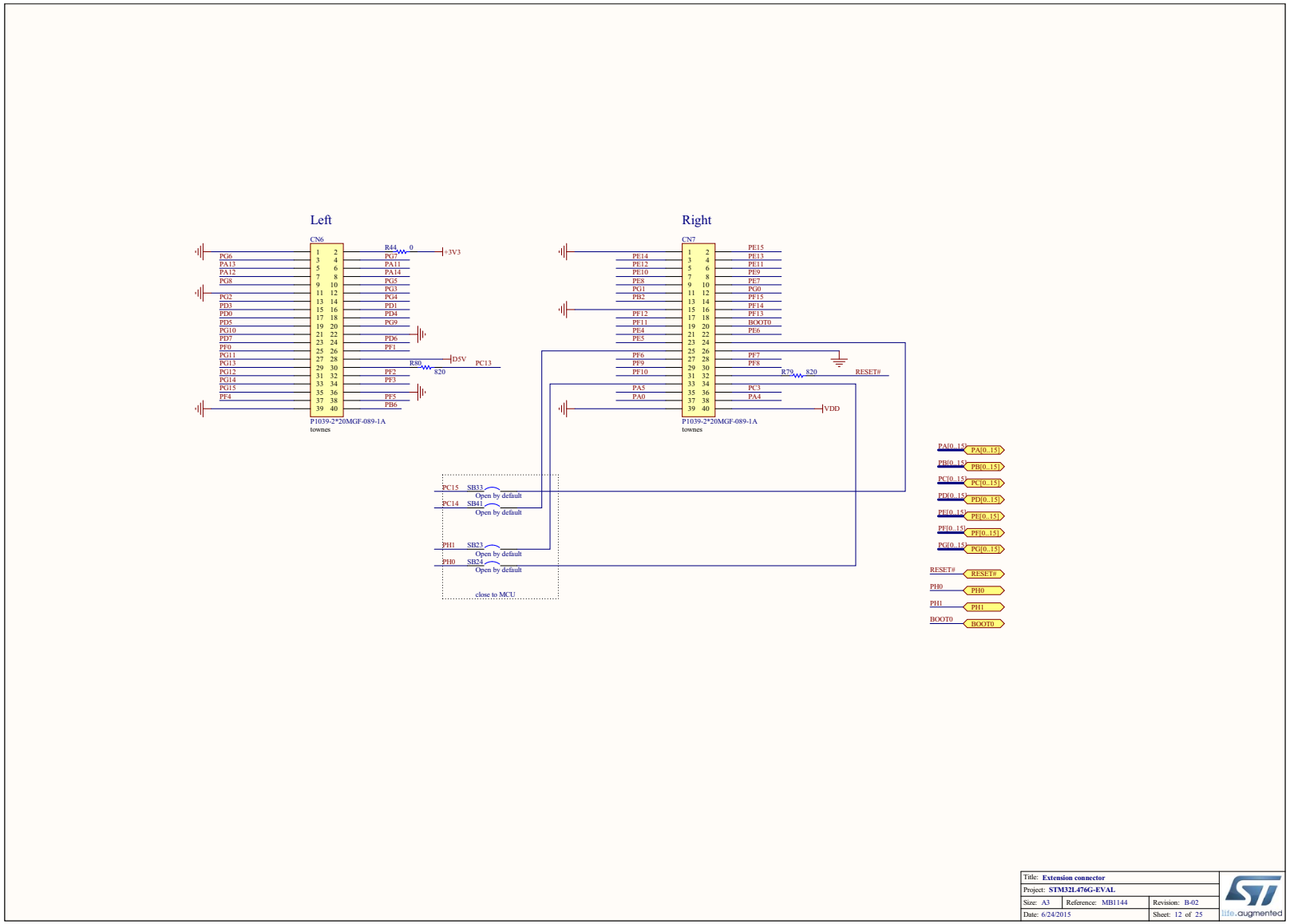


Figure 44. Quad-SPI Flash memory device schematic diagram

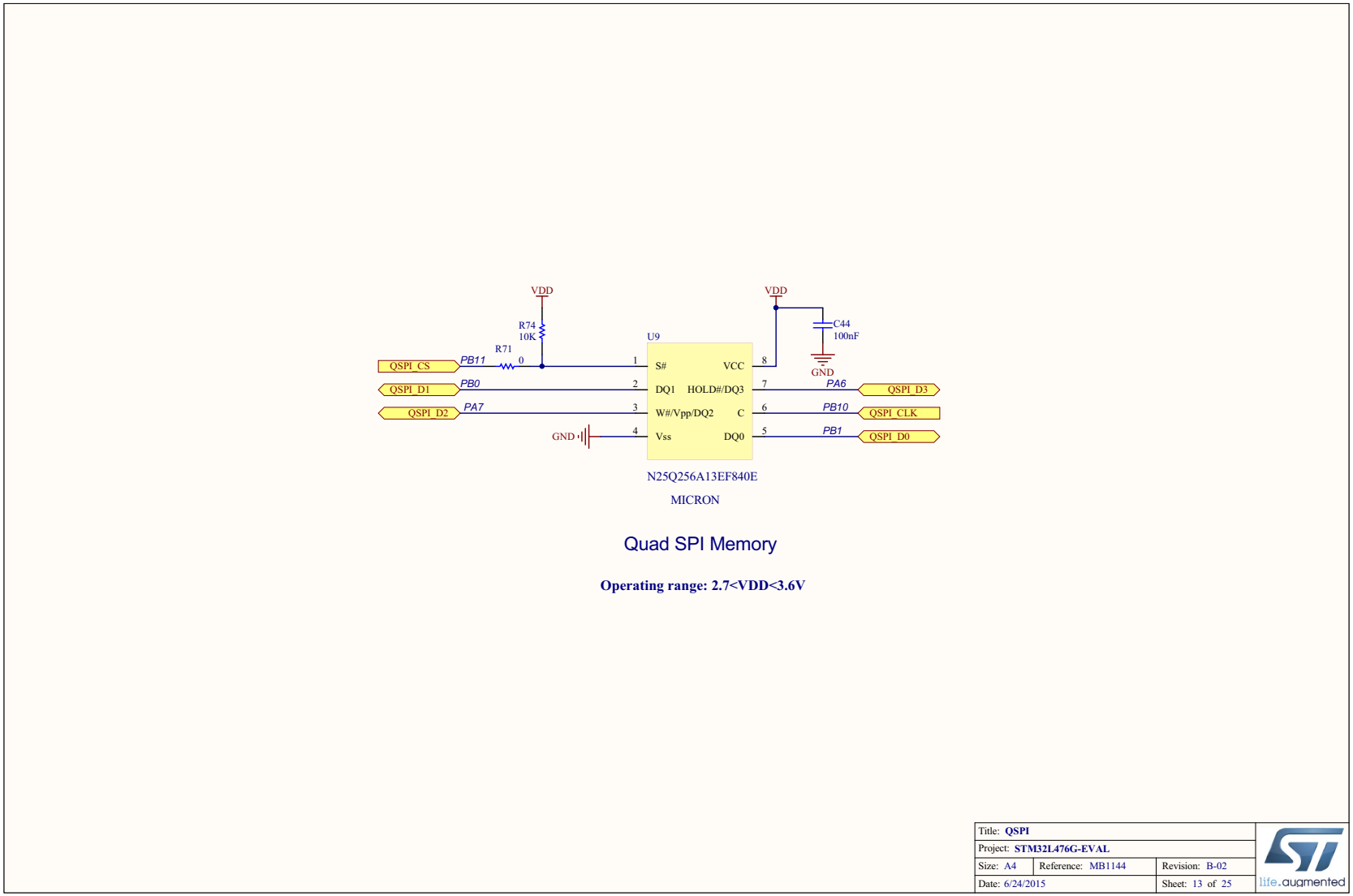


Figure 45. microSD card schematic diagram

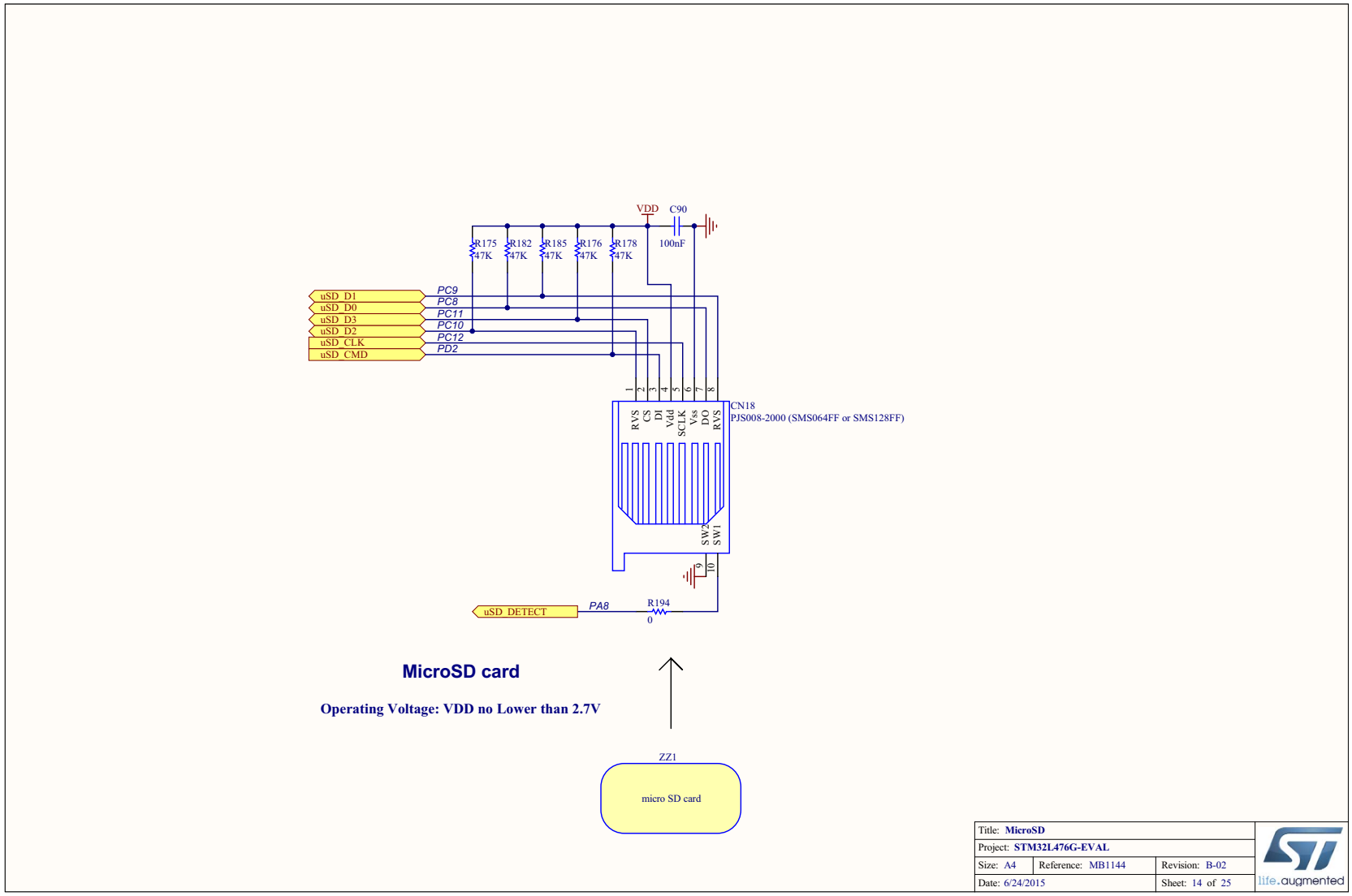


Figure 46. Physical control peripherals - schematic diagram

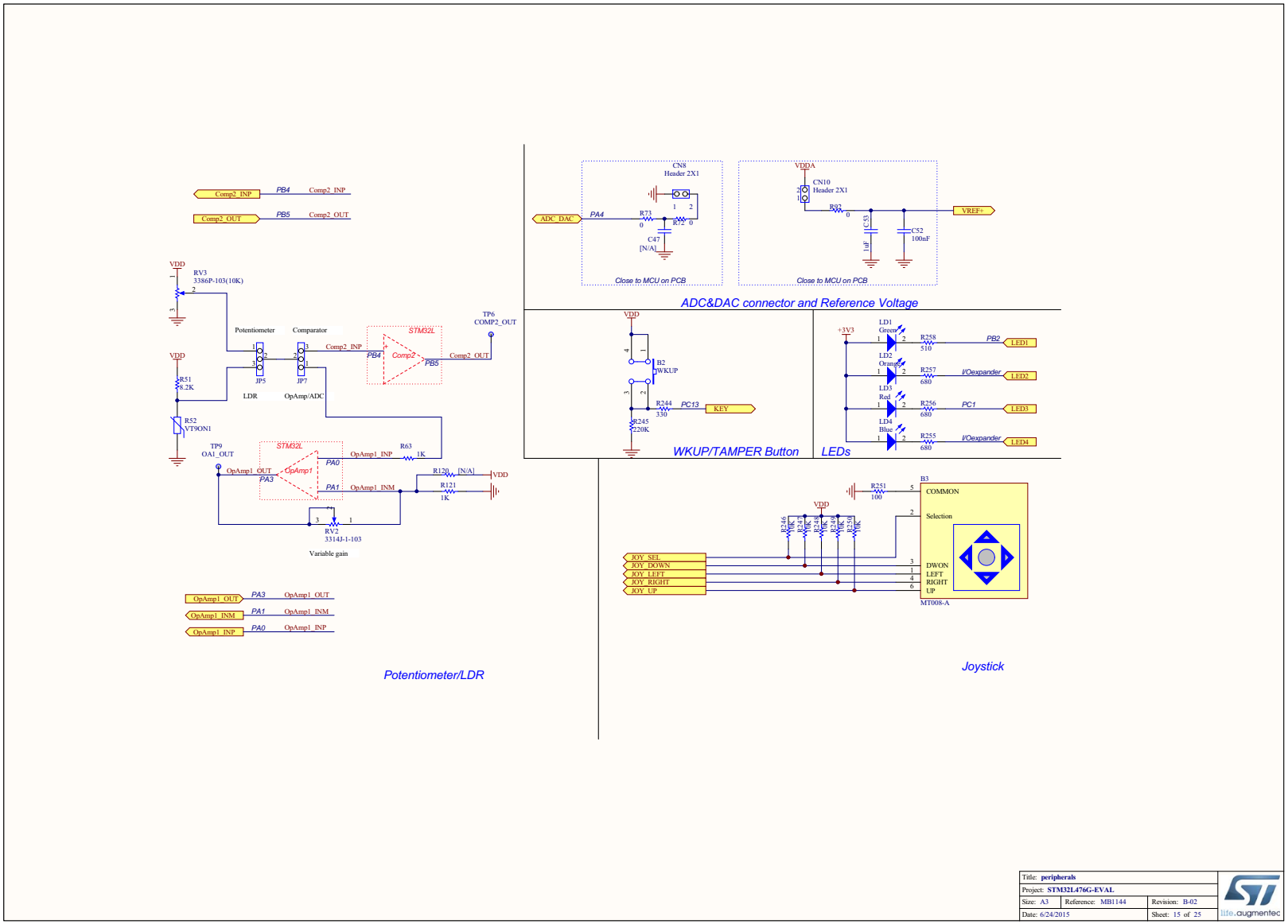


Figure 47. CAN transceiver schematic diagram

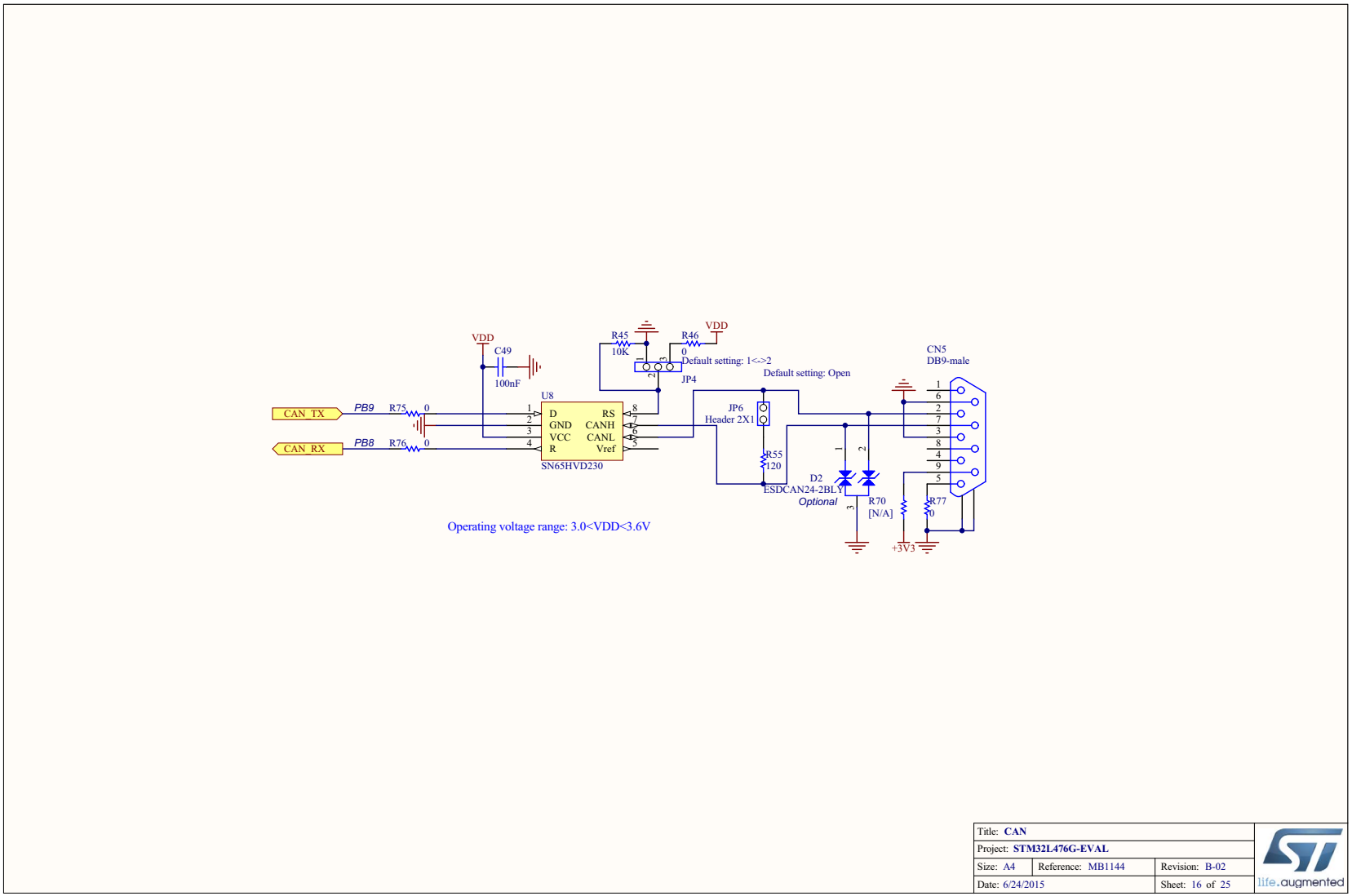


Figure 48. Touch-sensing device schematic diagram

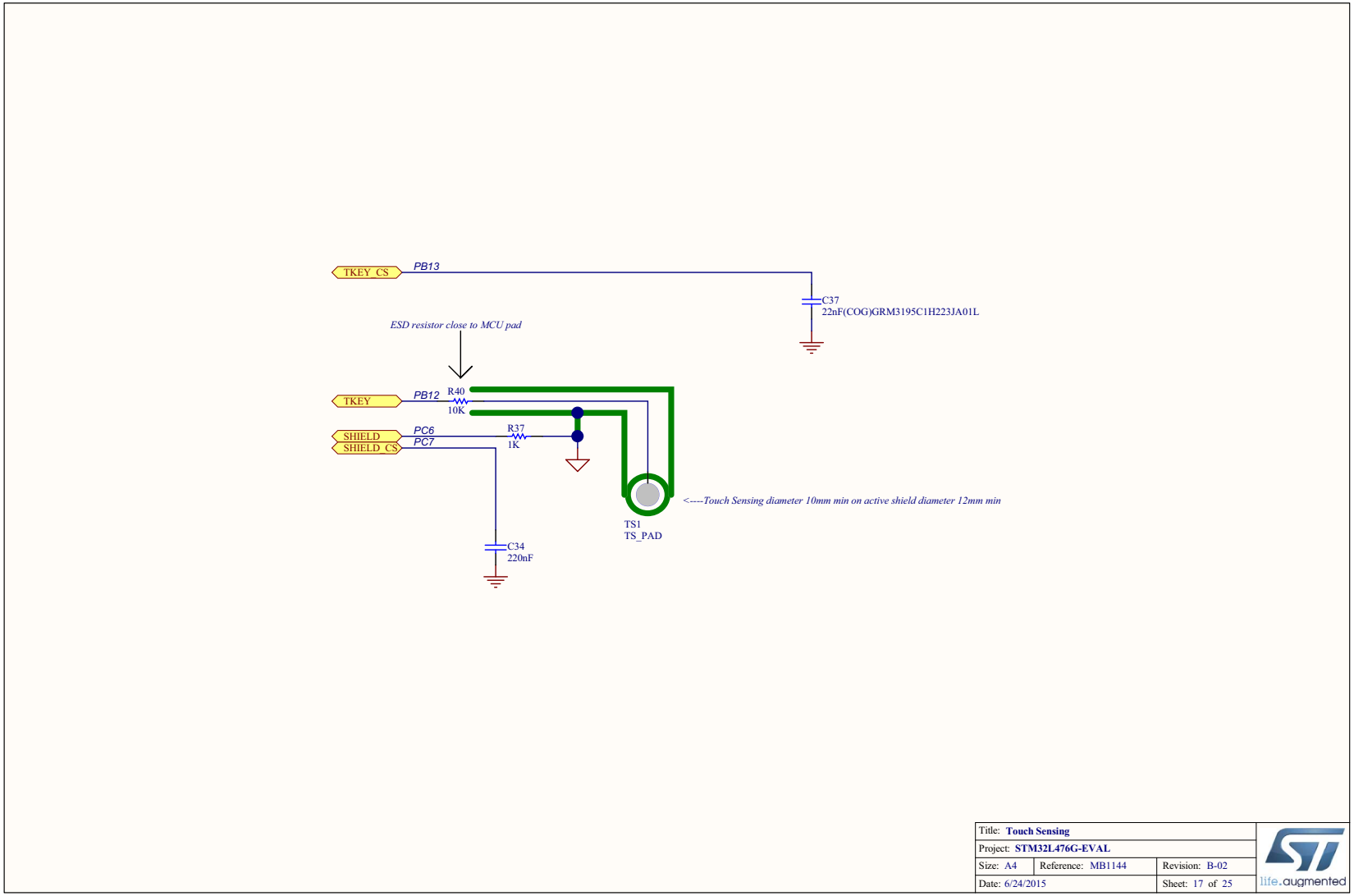


Figure 49. USB_OTG_FS port schematic diagram

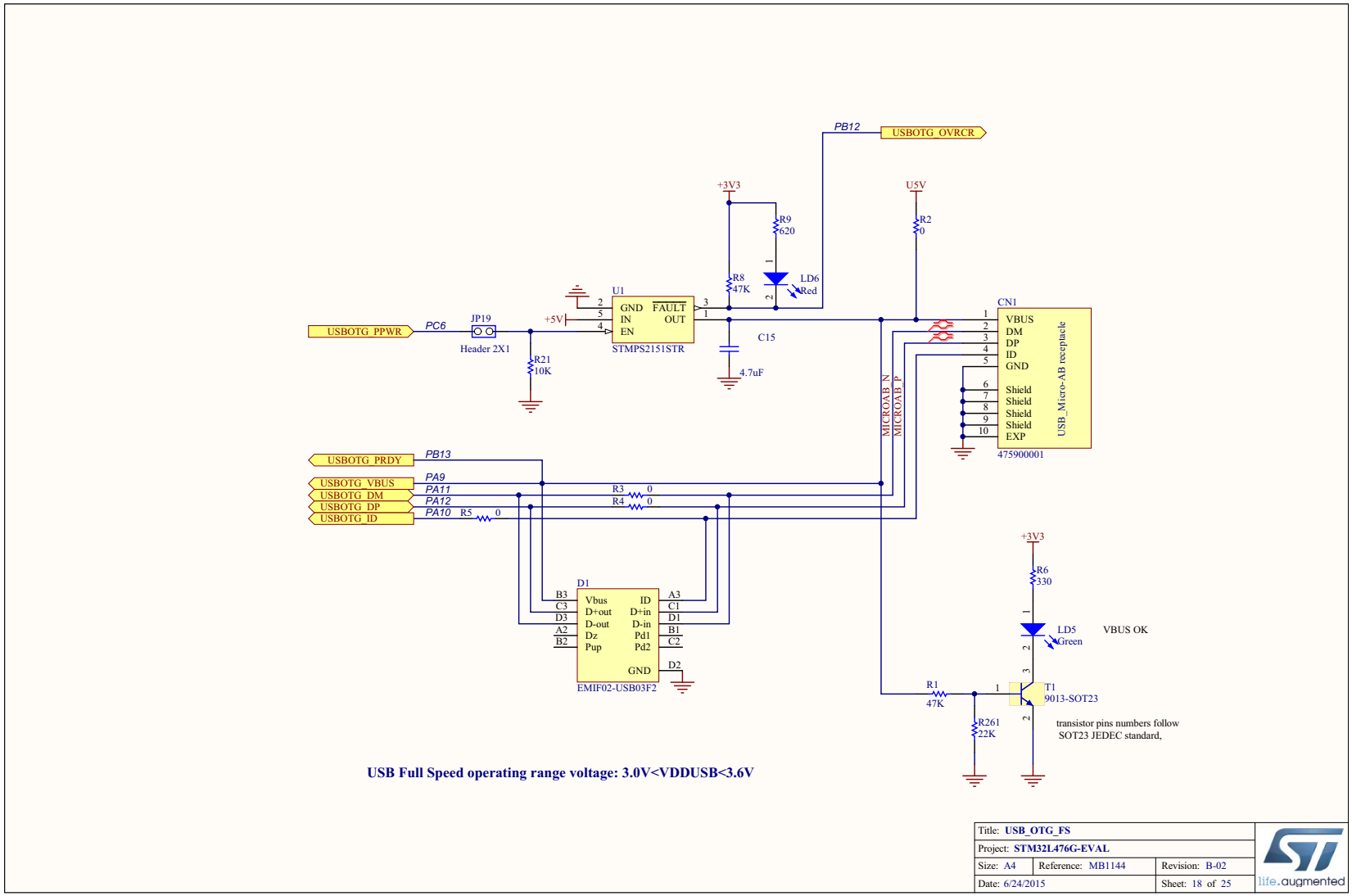


Figure 50. IDD measurement schematic diagram

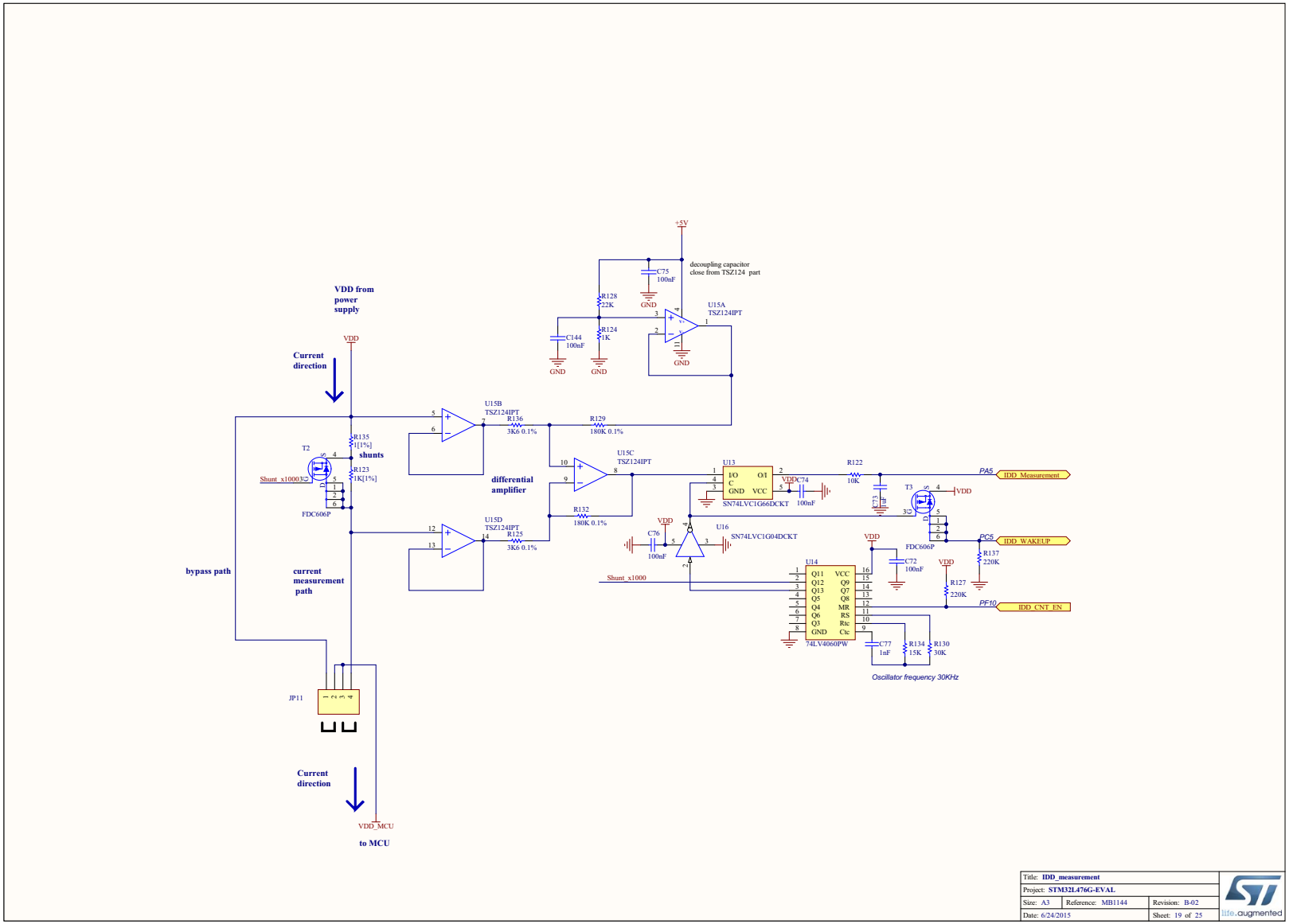


Figure 51. Audio codec device schematic diagram

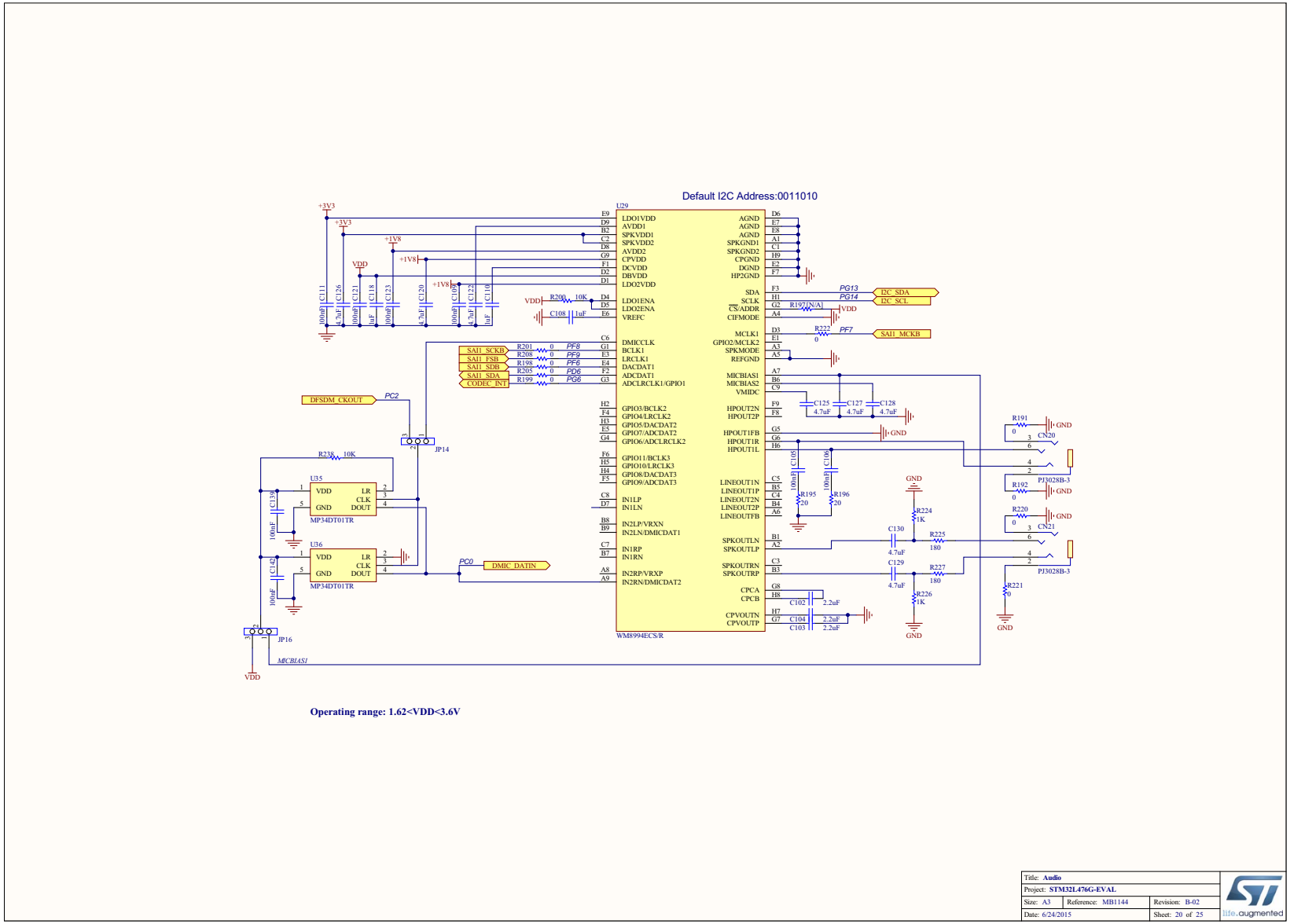


Figure 52. STPMS2L and PT100 schematic diagram

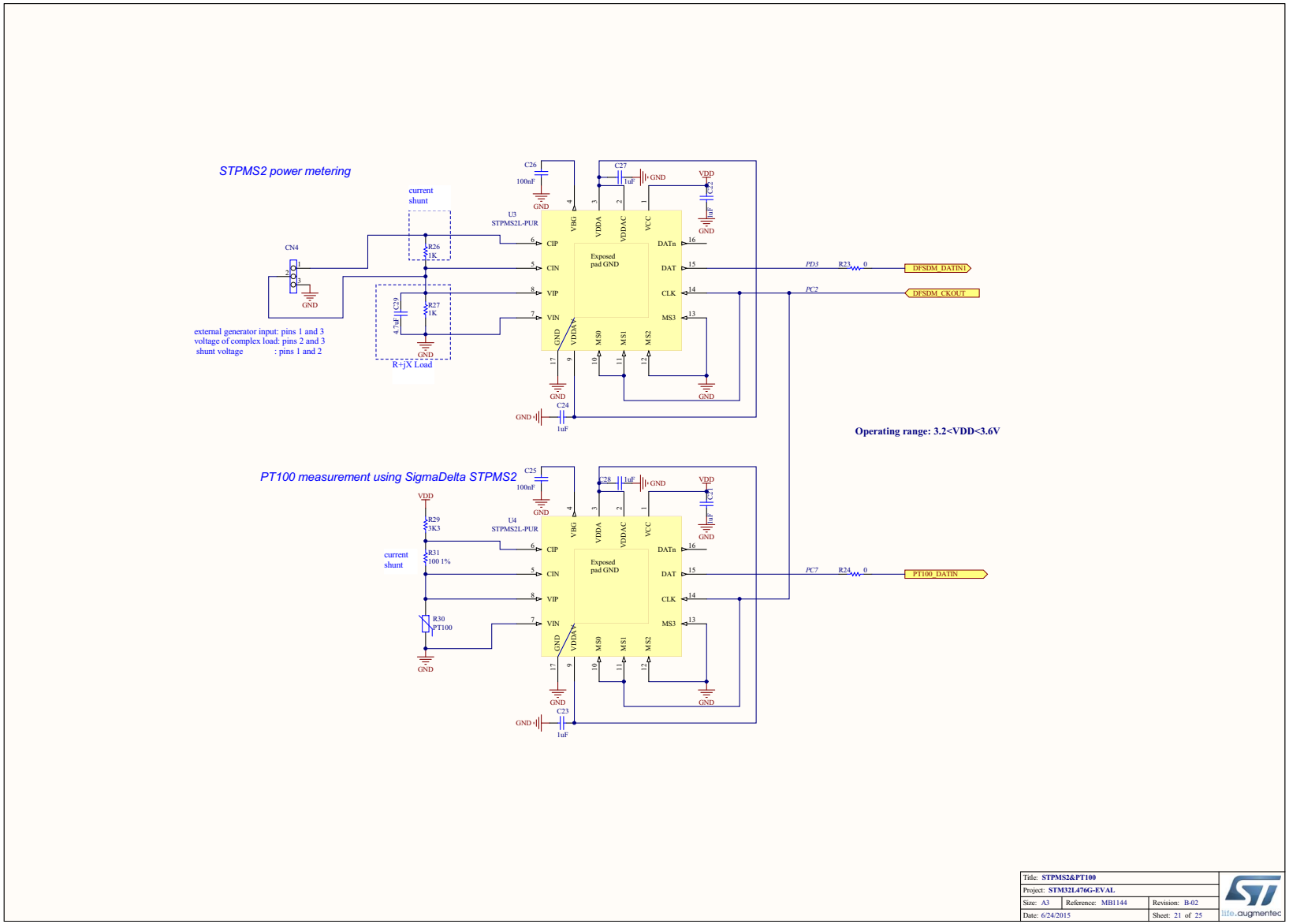


Figure 53. RF-EEPROM and EEPROM schematic diagram

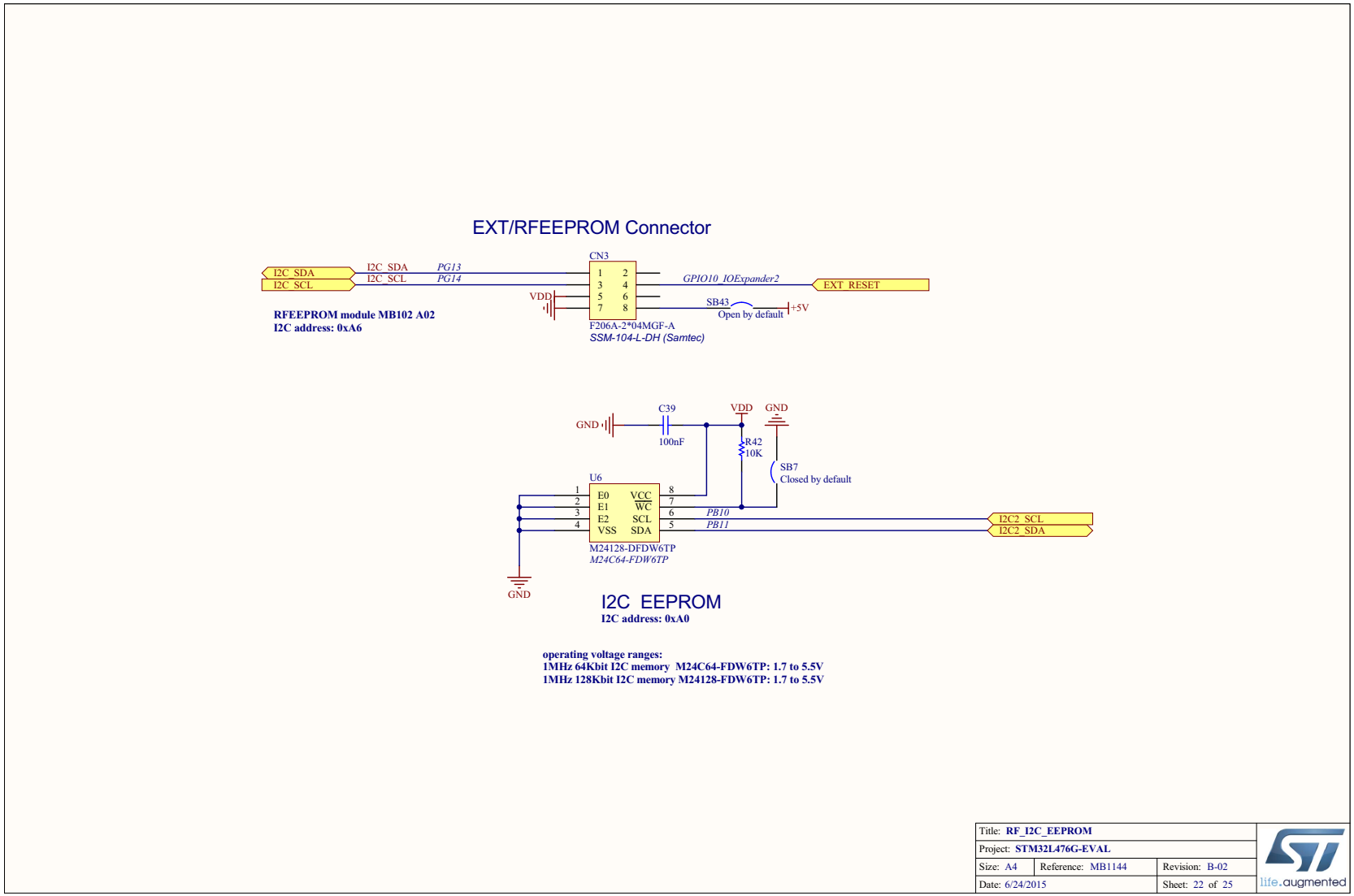


Figure 54. Motor control connector schematic diagram

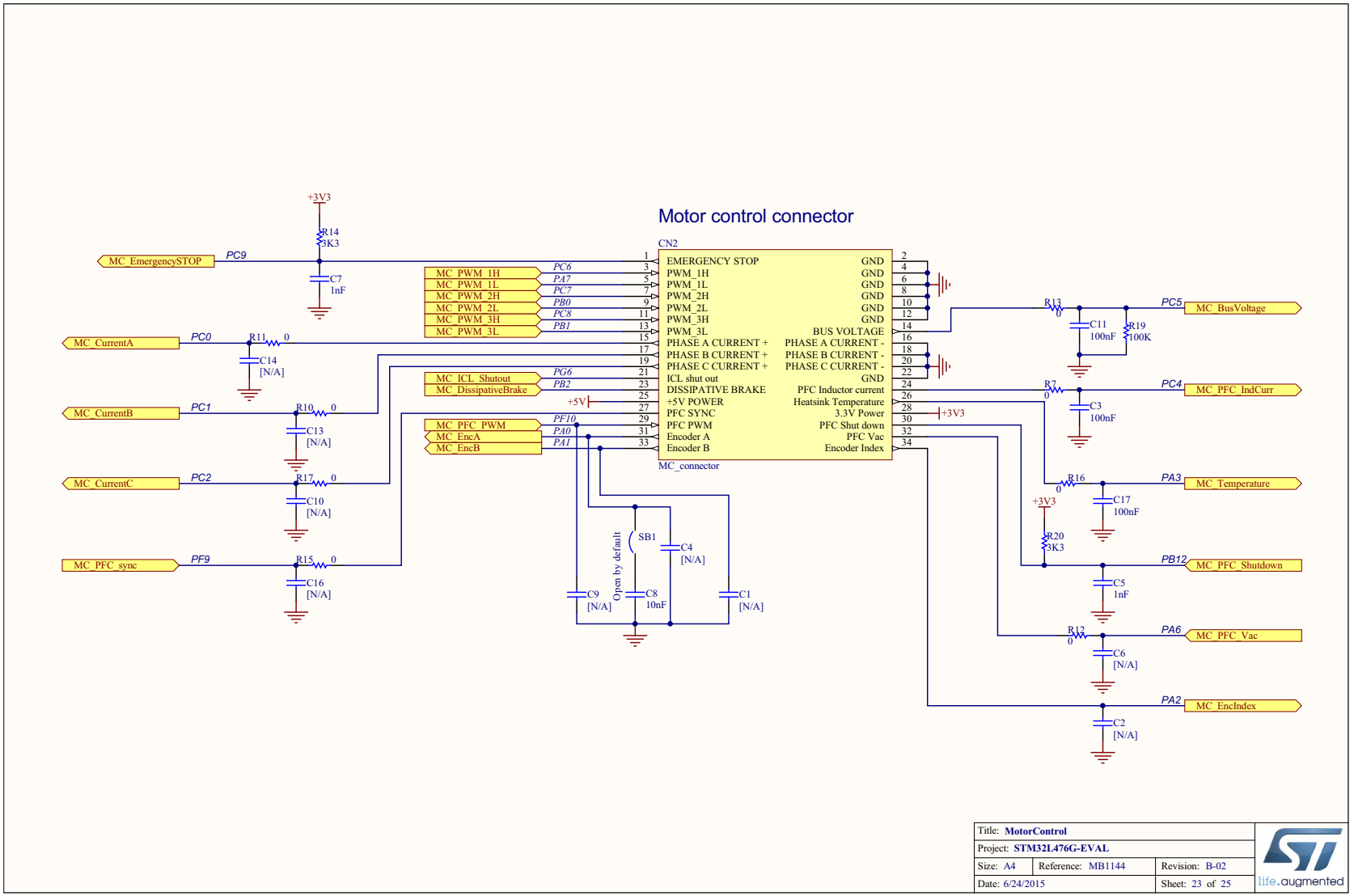


Figure 55. JTAG and trace debug connectors - schematic diagram

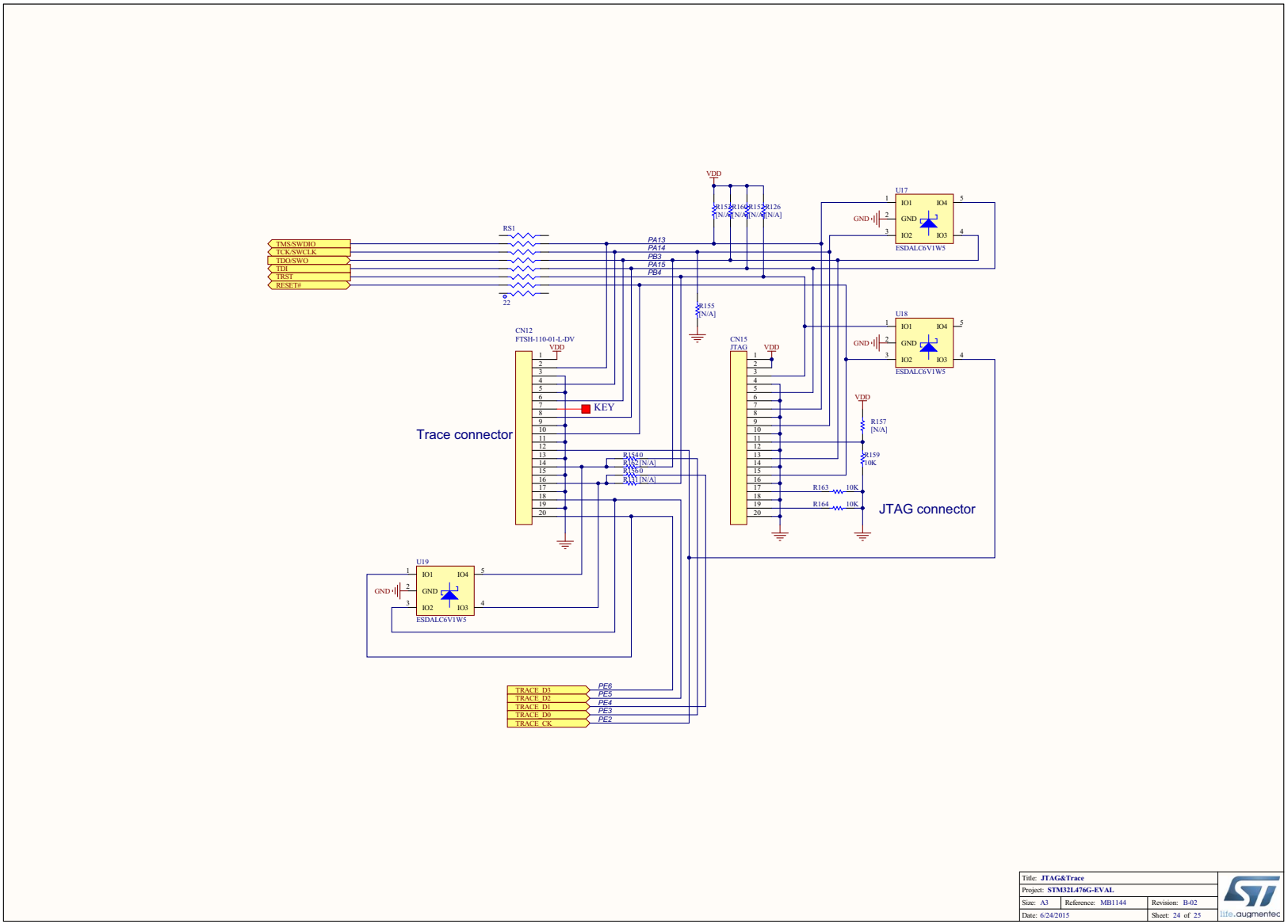
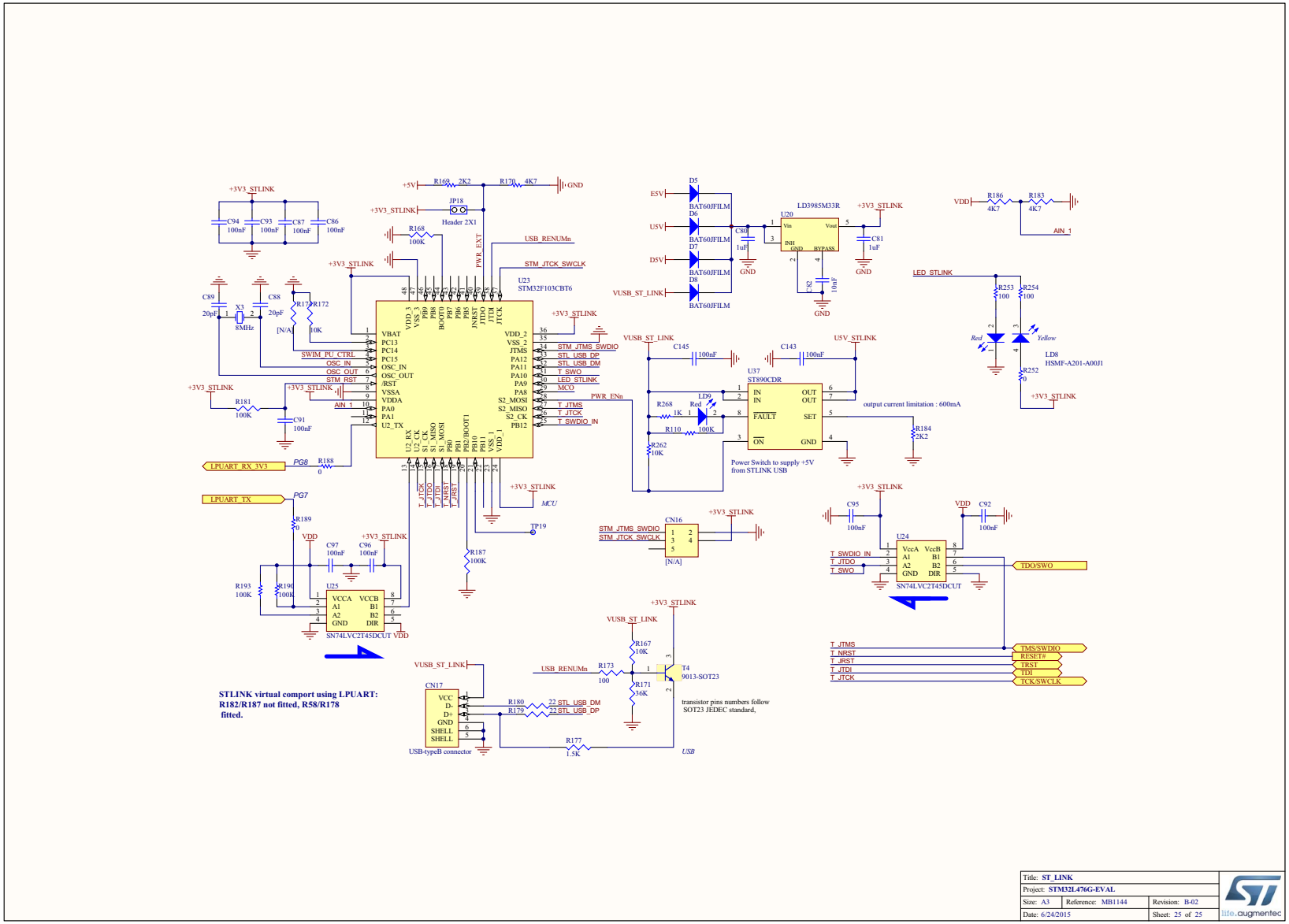


Figure 56. ST-LINK/V2-1 schematic diagram



Appendix B Federal Communications Commission (FCC) and Industry Canada (IC) Compliance Statements

B.1 FCC Compliance Statement

B.1.1 Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

B.1.2 Part 15.105

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference's by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

B.1.3 Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

B.2 IC Compliance Statement

B.2.1 Compliance Statement

Industry Canada ICES-003 Compliance Label: *CAN ICES-3 (B)/NMB-3(B)*

B.2.2 Déclaration de conformité

Étiquette de conformité à la NMB-003 d'Industrie Canada : *CAN ICES-3 (B)/NMB-3(B)*

4 Revision History

Table 46. Document Revision History

Date	Version	Revision Details
22-Jul-2015	1	Initial Version
29-Jul-2015	2	Added *Section 2.6.2: Bootloader limitations*. Classification change from ST Restricted to Public.
09-Sep-2015	3	*Figure 3*: swap of FAULT and VBUS prints in the upper-left corner of the board. *Section 2.8.3*: swap of LD5 and LD6. *Appendix B*: modified *Section B.1.3* and *Section B.2* text. *Table 13*: JP6 default setting modified. *Section 2.5* and *Section 2.9.1*: JP9 by-default setting added. *Table 31*: JP11 default setting modified and position information added. *Table 8*: JP19 default setting modified. *Table 42*: CN2 instead of CN1 *Section 3.2*: CN2 corrected in CN22 Multiple language or typographical corrections.