## Table of Contents



## Revisions

| Rev | Description | Date | Approved |
|---|---|---|---|
| X1 | Initial | 30 Dec 11 | Anthony H. |
| A | Release | 21 Mar 12 | Anthony H. |
| B | Release | 24 May 12 | Anthony H. |
| C | Release | 29 June 12 | Anthony H. |
| E | Release | 22 Aug 12 | Anthony H. |
| F | Release | 18 Oct 12 | Anthony H. |
| G | Release | 19 Dec 12 | Anthony H. |
| G1 | Release | 11 July 13 | Naoum G. |
| G2 | Update | 24 July 13 | Naoum G. |
| G3 | Release | 26 July 13 | Naoum G. |
| G4 | Update | 08 Nov 13 | Naoum G. |
| G5 | Update | 21 Nov 13 | Jiri K. |
| G6 | Update | 22 Nov 13 | Jiri K. |
| G7 | Update | 24 Dec 13 | Guillermo Ron |
| H | Release | 23 Jan 14 | Guillermo Ron |

# TWR-VF65GS10

# VYBRID TOWER SYSTEM MODULE


Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598




ICAP Classification: FCP: FIUO: X PUBI:

| | |
|---|---|
| Designer: B04178, B07446, B23443 & B42818 | Drawing Title: TWR-VF65GS10 |
| Drawn by: Jun Q. | Page Title: Table of Contents & Revisions |
| Approved: Naoum G. & Jiri K. | Size C / Document Number SCH-27442 PDF: SPF-27442 / Rev H |
| | Date: Thursday, January 23, 2014 / Sheet 1 of 11 |

# Global Power & Ground Nets

| NET | VOLTAGE | DESCRIPTION |
|---|---|---|
| Pxx_ELEV | xx | Input/output power from/to Elevators. |
| P5V_USB | 5V | Input power. Filtered from USB connector. Input to USB power switch. |
| P5V_SW | 5V | Output of USB power switch, enabled by input of USB power supply. |
| P5V | 5V | Source from either P5V_ELEV, or USB0_VBUS, or USB_VBUS, or external source. |
| P3V3 | 3.3V | Output of high-power Switch-Mode regulator. |
| VCC_3V3_K20 | 3.3V | Output of low-power Linear regulator, power supply for K20 (Kinetis). |
| VCC_3V3_MCU | 3.3V | MCU digital power. Comes from P3V3. |
| VCC_2V5 | 2.5V | DDR3 2.5V pre-drive supply. |
| VCC_1V5 | 1.5V | DDR3 1.5V main IO supply. |
| VCC_1V2 | 1.2V | MCU core power. Output of regulator based on on-chip controller and external ballast transistor. |
| GND | 0V | Main Ground |

# Main Revision Modifications:

1. 100mil headers replaced with smaller 2mm ones.
2. 5V and 3.3V power partition changed.
3. Quad SPI and USB data switches deleted (bypassed).
4. Vybrid ballast transistor powered from 1.5V, not 3.3V.
5. 1.5V generated by Swith-Mode, not Linear regulator.
6. Optional "Virtual VF3xx" configuration created.
7. Optional VADCSE[0:3] and LVDS0 connections provided.
8. Vybrid USB ports made compliant with USB spec.
9. Vybrid Power-On-Reset active timeout made longer to guarantee proper SD card initialization.
10. Initial current comsumption of OpenSDA USB port lowered to make compliant with USB spec (by splitting RESET_B net).
11. Removing U1 and powering K20 (Kinetis) by its internal regualtor output 3.3V (which is regulated from elevator P5V or USB switch P5V_SW).
12. Optional Ethernet MII interface added (DNP-ed 0-Ohm resistors).
13. DDR3: external termination deleted, Vref circuit simplified.
14. Series 0-Ohm resistors added into I2C0, I2C1, and I2C2 lines to Elevator for flexibility.
15. Filtering (series ferrite beads) added into x_AFE and x_ADC power rails for better performance.
16. New button SW4 added to test low power use cases.

1. Unless Otherwise Specified:
   All resistors are in ohms
   All capacitors are in uF
   All voltages are DC
   All polarized capacitors are aluminum electrolytic.

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

*6. Specific PCB LAYOUT notes are detailed in ITALICS.*

7. Special component funtion notes are detailed in Narrow Arial.

8. Jumper setting notes are detailed in Courier New.

9. Version modifications are detailed in Arial.

freescale semiconductor

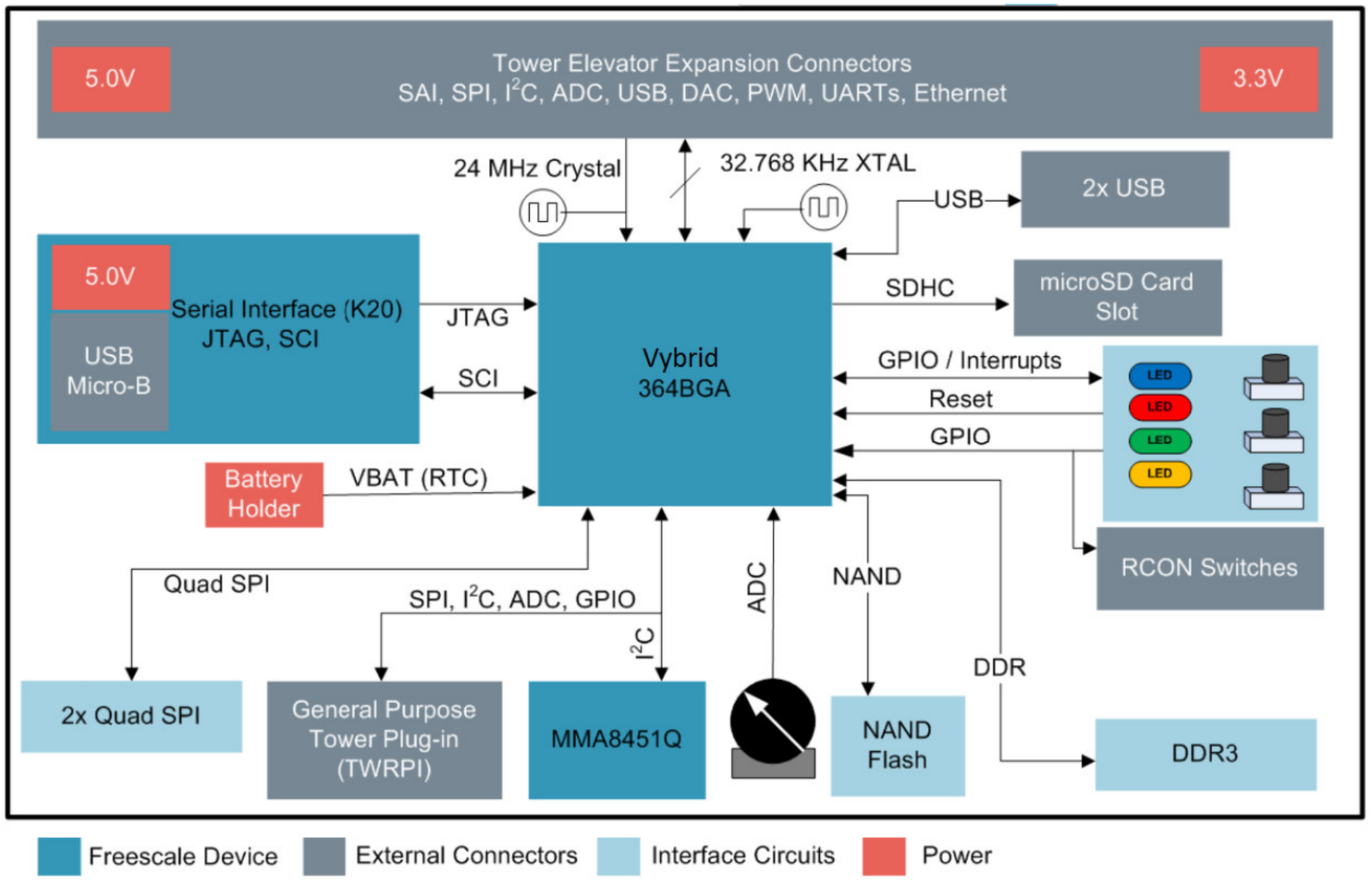
ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title:
**TWR-VF65GS10**

Page Title:
**02-Notes & Rev Modifications**

| Size | Document Number | Rev |
|---|---|---|
| C | SCH-27442 PDF: SPF-27442 | H |
| Date: Thursday, January 23, 2014 | Sheet 2 of 11 | |

# Block Diagram




freescale semiconductor

ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **TWR-VF65GS10**

Page Title: **Block Diagram**

| Size | Document Number | Rev |
|---|---|---|
| C | SCH-27442 PDF: SPF-27442 | H |

Date: Thursday, January 23, 2014 Sheet 3 of 11

U7B

6,7,8,9 PTA[6..31]

| | | |
|---|---|---|
| PTA6 | RMII_CLKIN | N5 |
| PTA7 | SDHC1_CD | V15 |
| PTA8 | JTCLK | K4 |
| PTA9 | JTDI | K2 |
| PTA10 | JTDO | K1 |
| PTA11 | JTMS | L1 |
| PTA12 | TRACECK | L3 |
| PTA16 | TRACE[D0] | Y5 |
| PTA17 | TRACE[D1] | Y6 |
| PTA18 | TRACE[D2] | V6 |
| PTA19 | TRACE[D3] | U6 |
| PTA20 | TRACE[D4]* | B18 |
| PTA21 | SAI2_RX_BCLK/TRACE[D5]* | D18 |
| PTA22 | SAI2_RX_DATA/TRACE[D6]* | E17 |
| PTA23 | SAI2_RX_SYNC/TRACE[D7]* | C17 |
| PTA24 | SDHC1_CLK/TRACE[D8]* | R16 |
| PTA25 | SDHC1_CMD/TRACE[D9]* | R17 |
| PTA26 | SDHC1_DAT0/TRACE[D10]* | R19 |
| PTA27 | SDHC1_DAT1/TRACE[D11]* | R20 |
| PTA28 | SDHC1_DAT2/TRACE[D12]*/ENET1_1588_TMR0* | P20 |
| PTA29 | SDHC1_DAT3/TRACE[D13]*/ENET1_1588_TMR1* | P18 |
| PTA30 | TRACE[D14]*/ENET1_1588_TMR2* | P17 |
| PTA31 | TRACE[D15]*/ENET1_1588_TMR3* | P16 |

PTA6/RMII_CLKOUT/RMII_CLKIN
PTA7
PTA8/JTCLK/SWCLK
PTA9/JTDI/RMII_CLKOUT/RMII_CLKIN/WDOG
PTA10/JTDO/EXT_AUDIO_MCLK/ENET_TS_CLKIN
PTA11/JTMS/SWDIO
PTA12/TRACECK/EXT_AUDIO_MCLK

PTA16/TRACED0/USB0_VBUS_EN/ADC1SE0/SAI2_TX_BCLK
PTA17/TRACED1/USB0_VBUS_OC/ADC1SE1/USB0_SOF_PULSE
PTA18/TRACED2/ADC0SE0/FTM1_QD_PHA/SAI2_TX_DATA
PTA19/TRACED3/ADC0SE1/FTM1_QD_PHB/SAI2_TX_SYNC
PTA20/TRACED4/SCI3_TX
PTA21/TRACED5/SAI2_RX_BCLK/SCI3_RX
PTA22/TRACED6/SAI2_RX_DATA
PTA23/TRACED7/SAI2_RX_SYNC
PTA24/TRACED8/USB1_VBUS_EN/SDHC1_CLK/WDOG
PTA25/TRACED9/USB1_VBUS_OC/SDHC1_CMD
PTA26/TRACED10/SAI3_TX_BCLK/SDHC1_DAT0
PTA27/TRACED11/SAI3_RX_BCLK/SDHC1_DAT1
PTA28/TRACED12/SAI3_RX_DATA/ENET1_1588_TMR0/SCI4_TX/SDHC1_DAT2
PTA29/TRACED13/SAI3_TX_DATA/ENET1_1588_TMR1/SCI4_RX/SDHC1_DAT3
PTA30/TRACED14/SAI3_RX_SYNC/ENET1_1588_TMR2/SCI4_RTS/SCI3_TX
PTA31/TRACED15/SAI3_TX_SYNC/ENET1_1588_TMR3/SCI4_CTS/SCI3_RX

7,8,9,10 PTB[0..28]

| | | |
|---|---|---|
| PTB0 | FTM0CH0 | T6 |
| PTB1 | FTM0CH1/RCON30** | T7 |
| PTB2 | FTM0CH2/RCON31** | V7 |
| PTB3 | FTM0CH3 | W7 |
| PTB4 | SCI1_TX | Y7 |
| PTB5 | SCI1_RX | Y8 |
| PTB6 | SCI2_TX/FTM0CH6 | W8 |
| PTB7 | SCI2_RX/FTM0CH7 | D13 |
| PTB8 | FTM1CH0 | J16 |
| PTB9 | FTM1CH1 | J19 |
| PTB10 | ENET_TS_CLKIN/CKO1* | B15 |
| PTB11 | CKO2* | D14 |
| PTB12 | | E13 |
| PTB13 | TRACECTL | D15 |
| PTB14 | I2C0_SCL | B14 |
| PTB15 | I2C0_SDA | A14 |
| PTB16 | CAN1_RX*/I2C1_SCL* | C14 |
| PTB17 | CAN1_TX*/I2C1_SDA* | A15 |
| PTB18 | DSPI0_PCS1/EXT_AUDIO_MCLK | B12 |
| PTB19 | DSPI0_PCS0 | C13 |
| PTB20 | DSPI0_SIN | A13 |
| PTB21 | DSPI0_SOUT | E12 |
| PTB22 | DSPI0_SCK | D12 |
| PTB23 | SAI0_TX_BCLK/RCON18** | A19 |
| PTB24 | NF_WE_b/RCON19** | A18 |
| PTB25 | NF_CE0_b/RCON20** | B17 |
| PTB26 | SAI0_TX_DATA/RCON21** | A17 |
| PTB27 | NF_RE_b/RCON22** | U8 |
| PTB28 | SAI0_TX_SYNC/RCON23** | A16 |

TP12 CKO1* PTB10
TP14 CKO2* PTB11

PTB0/FTM0CH0/ADC0SE2/TRACECTL/SAI2_RX_BCLK
PTB1/FTM0CH1/ADC0SE3/RCON30/SAI2_RX_DATA
PTB2/FTM0CH2/ADC1SE2/RCON31/SAI2_RX_SYNC
PTB3/FTM0CH3/ADC1SE3/EXTRIG
PTB4/FTM0CH4/SCI1_TX/ADC0SE4
PTB5/FTM0CH5/SCI1_RX/ADC1SE4
PTB6/FTM0CH6/SCI1_RTS/SCI2_TX
PTB7/FTM0CH7/SCI1_CTS/SCI2_RX
PTB8/FTM1CH0/FTM1_QD_PHA
PTB9/FTM1CH1/FTM1_QD_PHB
PTB10/SCI0_TX/CKO1/ENET_TS_CLKIN
PTB11/SCI0_RX/CKO2
PTB12/SCI0_RTS/DSPI0_PCS5
PTB13/SCI0_CTS/DSPI0_PCS4/TRACECTL
PTB14/CAN0_RX/I2C0_SCL
PTB15/CAN0_TX/I2C0_SDA
PTB16/CAN1_RX/I2C1_SCL
PTB17/CAN1_TX/I2C1_SDA
PTB18/DSPI0_PCS1/EXT_AUDIO_MCLK
PTB19/DSPI0_PCS0
PTB20/DSPI0_SIN
PTB21/DSPI0_SOUT
PTB22/DSPI0_SCK
PTB23/SAI0_TX_BCLK/SCI1_TX/RCON18
PTB24/SAI0_RX_BCLK/SCI1_RX/RCON19/NF_WE
PTB25/SAI0_RX_DATA/SCI1_RTS/RCON20/NF_CE0
PTB26/SAI0_TX_DATA/SCI1_CTS/RCON21/NF_CE1
PTB27/SAI0_RX_SYNC/RCON22/NF_RE
PTB28/SAI0_TX_SYNC/RCON23

7,8,9,10,11 PTC[0..31]

| | | |
|---|---|---|
| PTC0 | RMII0_MDC | L4 |
| PTC1 | RMII0_MDIO | L5 |
| PTC2 | RMII0_CRS_DV | M5 |
| PTC3 | RMII0_RXD[1] | M3 |
| PTC4 | RMII0_RXD[0] | L2 |
| PTC5 | RMII0_RXER | M1 |
| PTC6 | RMII0_TXD[1] | N1 |
| PTC7 | RMII0_TXD[0] | N2 |
| PTC8 | RMII0_TXEN | N4 |
| PTC9 | RMII1_MDC/ESAI_SCKT | T15 |
| PTC10 | RMII1_MDIO/ESAI_FST | U15 |
| PTC11 | RMII1_CRS_DV/ESAI_SDO0 | P4 |
| PTC12 | RMII1_RXD[1]/ESAI_SDO1 | P3 |
| PTC13 | RMII1_RXD[0] | P1 |
| PTC14 | RMII1_RXER | R1 |
| PTC15 | RMII1_TXD[1]/ESAI_SDI0 | P2 |
| PTC16 | RMII1_TXD[0]/ESAI_SDI1 | R3 |
| PTC17 | RMII1_TXEN | R4 |
| PTC26 | NF_RB_b/RCON24** | D16 |
| PTC27 | NF_ALE/RCON25** | E16 |
| PTC28 | NF_CLE/RCON26** | E15 |
| PTC29 | RCON27** | C16 |
| PTC30 | ADC0SE5/RCON28** | T6 |
| PTC31 | ADC1SE5/RCON29** | W5 |

PTC0/RMII0_MDC/FTM1CH0/DSPI0_PCS3/ESAI_SCKT/RCON18
PTC1/RMII0_MDIO/FTM1CH1/DSPI0_PCS2/ESAI_FST/RCON19
PTC2/RMII0_CRS_DV/SCI1_TX/ESAI_SDO0/RCON20
PTC3/RMII0_RXD1/SCI1_RX/ESAI_SDO1
PTC4/RMII0_RXD0/SCI1_RTS/DSPI1_PCS1/ESAI_SDO2
PTC5/RMII0_RXER/SCI1_CTS/DSPI1_PCS0/ESAI_SDO3
PTC6/RMII0_TXD1/DSPI1_SIN/ESAI_SDI0
PTC7/RMII0_TXD0/DSPI1_SOUT/ESAI_SDI1
PTC8/RMII0_TXEN/DSPI1_SCK
PTC9/RMII1_MDC/ESAI_SCKT
PTC10/RMII1_MDIO/ESAI_FST
PTC11/RMII1_CRS_DV/ESAI_SDO0
PTC12/RMII1_RXD1/ESAI_SDO1/SAI2_TX_BCLK
PTC13/RMII1_RXD0/ESAI_SDO2/SAI2_RX_BCLK
PTC14/RMII1_RXER/ESAI_SDO3/SCI5_TX/SAI2_RX_DATA/ADC0SE6
PTC15/RMII1_TXD1/ESAI_SDI0/SCI5_RX/SAI2_TX_DATA/ADC0SE7
PTC16/RMII1_TXD0/ESAI_SDI1/SCI5_RTS/SAI2_RX_SYNC/ADC1SE6
PTC17/RMII1_TXEN/SCI5_CTS/SAI2_TX_SYNC/USB1_SOF_PULSE/ADC1SE7

PTC26/SAI1_TX_BCLK/DSPI0_PCS5/RCON24/NF_RB
PTC27/SAI1_RX_BCLK/DSPI0_PCS4/RCON25/NF_ALE
PTC28/SAI1_RX_DATA/DSPI0_PCS3/RCON26/NF_CLE
PTC29/SAI1_TX_DATA/DSPI0_PCS2/RCON27
PTC30/SAI1_RX_SYNC/DSPI1_PCS2/RCON28/ADC0SE5
PTC31/SAI1_TX_SYNC/RCON29/ADC1SE5

EXTAL_MAIN Y13 EXTAL
XTAL_MAIN W13 XTAL
EXTAL32_RTC Y12 EXTAL32
XTAL32_RTC W12 XTAL32

J7 1X2 MTMM-102-07-G-S-236 Default: 1-2 (loopback)
TP6 TP4
TAMPER0 T14 EXT_TAMPER0
TAMPER1 U14 EXT_TAMPER1
TAMPER2 T13 EXT_TAMPER2/EXT_WM0_TAMPER_IN
TAMPER3 U13 EXT_TAMPER3/EXT_WM0_TAMPER_OUT
TAMPER4 U12 EXT_TAMPER4/EXT_WM1_TAMPER_IN
TAMPER5 U10 EXT_TAMPER5/EXT_WM1_TAMPER_OUT
R39 0
R137 10.0K R138 10.0K R139 0.0K R140 10.0K R141 10.0K R142 0.0K
GND

T1 Ext_POR
GND

6,7,8,9 RESET_B T4 RESET/RESET_OUT

MVF61NS151CMK50
(PVF61NS151CMK50)

PTD0/QSPI0_A_SCK/SCI2_TX/SPDIF_EXTCLK
PTD1/QSPI0_A_CS0/SCI2_RX/SPDIF_IN1
PTD2/QSPI0_A_DATA3/SCI2_RTS/DSPI1_PCS3/SPDIF_OUT1
PTD3/QSPI0_A_DATA2/SCI2_CTS/DSPI1_PCS2/SPDIF_PLOCK
PTD4/QSPI0_A_DATA1/DSPI1_PCS1/SPDIF_SRCLK
PTD5/QSPI0_A_DATA0/DSPI1_PCS0
PTD6/QSPI0_A_DQS/DSPI1_SIN
PTD7/QSPI0_B_SCK/DSPI1_SOUT
PTD8/QSPI0_B_CS0/DSPI1_SCK
PTD9/QSPI0_B_DATA3/DSPI3_PCS1/SAI1_TX_SYNC
PTD10/QSPI0_B_DATA2/DSPI3_PCS0
PTD11/QSPI0_B_DATA1/DSPI3_SIN
PTD12/QSPI0_B_DATA0/DSPI3_SOUT
PTD13/QSPI0_B_DQS/DSPI3_SCK

PTD16/NF_IO0/ESAI_HCKT
PTD17/NF_IO1/ESAI_HCKR
PTD18/NF_IO2/ESAI_FSR/FTM2_QD_PHB
PTD19/NF_IO3/ESAI_SCKR/FTM2_QD_PHA
PTD20/NF_IO4/ENET0_1588_TMR3/SDHC0_DAT7/SCI2_CTS
PTD21/NF_IO5/ENET0_1588_TMR2/SDHC0_DAT6/SCI2_RTS
PTD22/NF_IO6/FTM2CH1/ENET0_1588_TMR1/SDHC0_DAT5/SCI2_RX
PTD23/NF_IO7/FTM2CH0/ENET0_1588_TMR0/SDHC0_DAT4/SCI2_TX
PTD24/NF_IO8/FTM3CH7
PTD25/NF_IO9/FTM3CH6
PTD26/NF_IO10/FTM3CH5/SDHC1_WP
PTD27/NF_IO11/FTM3CH4/DSPI2_SCK
PTD28/NF_IO12/FTM3CH3/DSPI2_SOUT
PTD29/NF_IO13/FTM3CH2/DSPI2_SIN
PTD30/NF_IO14/FTM3CH1/DSPI2_PCS0
PTD31/NF_IO15/FTM3CH0/DSPI2_PCS1

PTE0/DCU0_HSYNC/DCU0_TCON1/BOOTMOD1
PTE1/DCU0_VSYNC/DCU0_TCON2/BOOTMOD0
PTE2/DCU0_PCLK
PTE3/DCU0_TAG/DCU0_TCON0/ADC0SE5
PTE4/DCU0_DE/DCU0_TCON3
PTE5/DCU0_R0
PTE6/DCU0_R1
PTE7/DCU0_R2/RCON0
PTE8/DCU0_R3/RCON1
PTE9/DCU0_R4/RCON2
PTE10/DCU0_R5/RCON3
PTE11/DCU0_R6/RCON4
PTE12/DCU0_R7/DSPI1_PCS3/RCON5/LPT_ALT0
PTE13/DCU0_G0
PTE14/DCU0_G1
PTE15/DCU0_G2/RCON6
PTE16/DCU0_G3/RCON7
PTE17/DCU0_G4/RCON8
PTE18/DCU0_G5/RCON9
PTE19/DCU0_G6/RCON10
PTE20/DCU0_G7/RCON11/EWM_in
PTE21/DCU0_B0
PTE22/DCU0_B1
PTE23/DCU0_B2/RCON12
PTE24/DCU0_B3/RCON13
PTE25/DCU0_B4/RCON14
PTE26/DCU0_B5/RCON15
PTE27/DCU0_B6/RCON16
PTE28/DCU0_B7/RCON17/EWM_out

USB0_VBUS_DETECT Y11
USB0_DM T9
USB0_DP T10
USB0_GND V10
GND
USB1_VBUS_DETECT U9
USB1_DM V9
USB1_DP W9
USB1_GND Y9
GND

ADC0SE8 Y2
ADC0SE9 W2
ADC1SE8 W3
ADC1SE9 Y3

VADCSE0 Y4 R156 10.0K
VADCSE1 U4 R157 10.0K
VADCSE2 W4 R159 10.0K
VADCSE3 V5 R158 10.0K
GND

DACO0 U1
DACO1 U2

LVDS0P W14 TPV1
LVDS0N Y14 TPV2

C73 18PF 50V 0402_CC
C70 18PF 50V 0402_CC

Layout Note:
Place capacitors as close to MCU as possible.

TEST T3
GND

PTD[0..31] 7,8,10,11

| | | |
|---|---|---|
| Y17 | QSPI0_A_SCK | PTD0 |
| Y18 | QSPI0_A_CS0_B | PTD1 |
| V18 | QSPI0_A_DATA[3] | PTD2 |
| Y19 | QSPI0_A_DATA[2] | PTD3 |
| W19 | QSPI0_A_DATA[1] | PTD4 |
| W20 | QSPI0_A_DATA[0] | PTD5 |
| V20 | QSPI0_A_DQS | PTD6 |
| V19 | QSPI0_B_SCK | PTD7 |
| U17 | QSPI0_B_CS0_B | PTD8 |
| U18 | QSPI0_B_DATA[3] | PTD9 |
| U20 | QSPI0_B_DATA[2] | PTD10 |
| T20 | QSPI0_B_DATA[1] | PTD11 |
| T19 | QSPI0_B_DATA[0] | PTD12 |
| T18 | QSPI0_B_DQS | PTD13 |
| D20 | NF_IO[0] | PTD16 |
| E20 | NF_IO[1] | PTD17 |
| E18 | NF_IO[2] | PTD18 |
| F16 | NF_IO[3] | PTD19 |
| F17 | NF_IO[4]/ENET0_1588_TMR3* | PTD20 |
| F19 | NF_IO[5]/ENET0_1588_TMR2* | PTD21 |
| F20 | NF_IO[6]/ENET0_1588_TMR1* | PTD22 |
| G20 | NF_IO[7]/ENET0_1588_TMR0* | PTD23 |
| G19 | NF_IO[8] | PTD24 |
| G18 | NF_IO[9] | PTD25 |
| G16 | NF_IO[10] | PTD26 |
| H16 | NF_IO[11] | PTD27 |
| H17 | NF_IO[12] | PTD28 |
| H18 | NF_IO[13] | PTD29 |
| H20 | NF_IO[14] | PTD30 |
| J20 | NF_IO[15] | PTD31 |

PTE[0..28] 7,8

| | | |
|---|---|---|
| N16 | DCU0_HSYNC/DCU0_TCON1/BOOTMOD[1]** | PTE0 |
| N18 | DCU0_VSYNC/DCU0_TCON2/BOOTMOD[0]** | PTE1 |
| N19 | DCU0_PCLK | PTE2 |
| Y15 | DCU0_TAG/DCU0_TCON0 | PTE3 |
| N20 | DCU0_DE/DCU0_TCON3 | PTE4 |
| T16 | DCU0_R0 | PTE5 |
| W16 | DCU0_R1 | PTE6 |
| M20 | DCU0_R2 | PTE7 |
| M19 | DCU0_R3 | PTE8 |
| M17 | DCU0_R4 | PTE9 |
| M16 | DCU0_R5 | PTE10 |
| L16 | DCU0_R6 | PTE11 |
| L17 | DCU0_R7 | PTE12 |
| Y16 | DCU0_G0 | PTE13 |
| W15 | DCU0_G1 | PTE14 |
| L18 | DCU0_G2 | PTE15 |
| L20 | DCU0_G3 | PTE16 |
| K20 | DCU0_G4 | PTE17 |
| K19 | DCU0_G5 | PTE18 |
| K18 | DCU0_G6 | PTE19 |
| A12 | DCU0_G7 | PTE20 |
| V16 | DCU0_B0 | PTE21 |
| W17 | DCU0_B1 | PTE22 |
| J17 | DCU0_B2 | PTE23 |
| D19 | DCU0_B3 | PTE24 |
| C19 | DCU0_B4 | PTE25 |
| C20 | DCU0_B5 | PTE26 |
| B20 | DCU0_B6 | PTE27 |
| K16 | DCU0_B7 | PTE28 |

Y2 32.768KHz
EXTAL32_RTC — C7 18PF 50V — GND
XTAL32_RTC — C6 18PF 50V — GND

Layout Note:
Place 32.768KHz clock curcuit adjacent to MCU.

Y1 24MHZ
XTAL_MAIN — R151 2.2M RC0402_25 — C8 12PF 50V CC0402_25 — GND
EXTAL_MAIN — C9 12PF 50V CC0402_25 — GND

Layout Note:
Place 24MHZ clock curcuit adjacent to MCU.

Revision Modification Note:

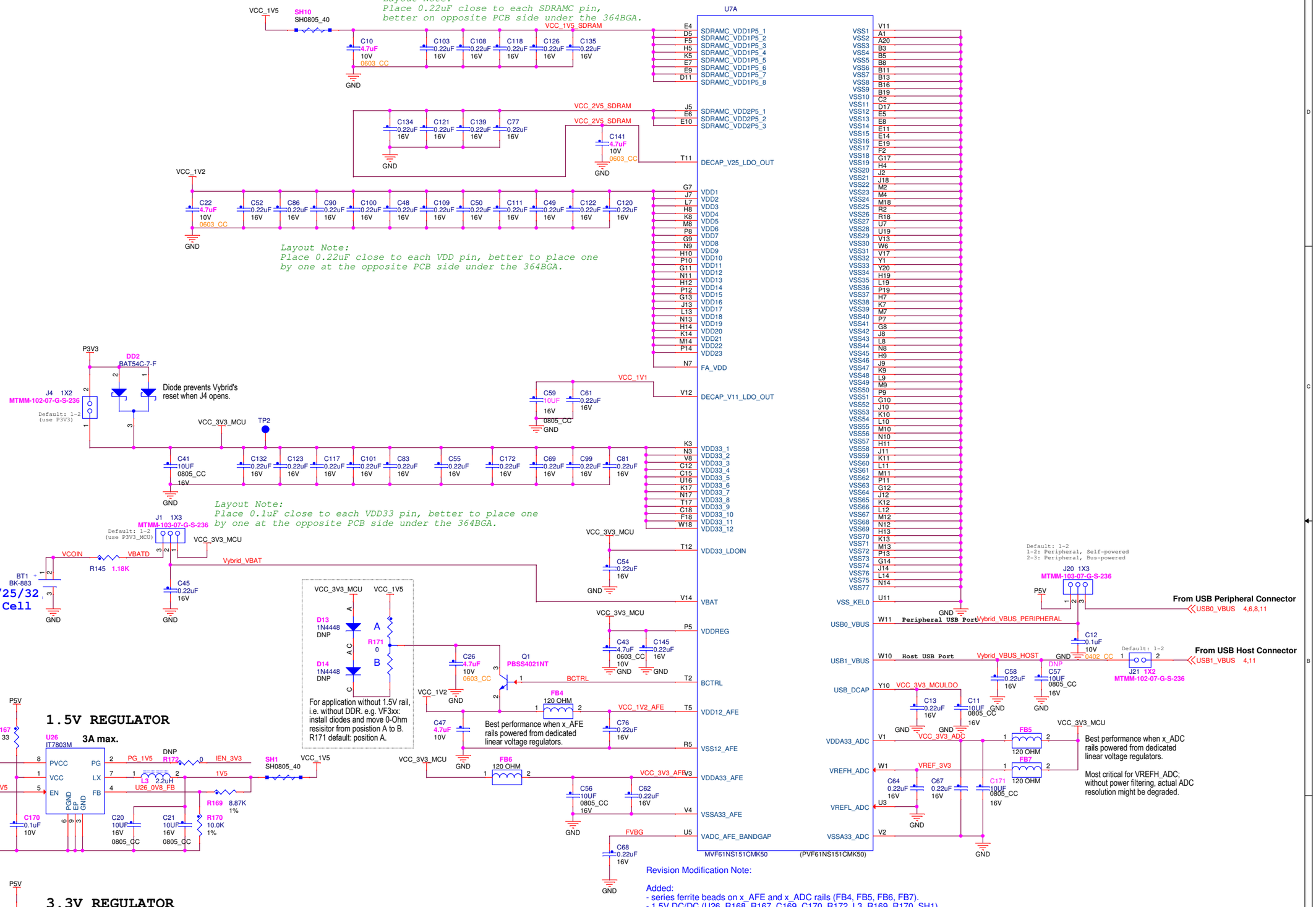
Added:
- R156...R158,
- TP17, and TP18,
- TPVs.

Deleted: R149, R150.

Changed:
- C6, C7, C8, C9, and R151 footprint changed from 0603 to 0402.
- C70 and C73 changed from 47pF to 18pF. (for BOM consolidation).
- 0402 capacitors (close to MCU) footprint from CC0402_25 to 0402_CC.

freescale semiconductor

ICAP Classification: FCP:___ FIUO: X PUBI:___
Drawing Title: **TWR-VF65GS10**
Page Title: **Vybrid Misc Pin**
Size C | Document Number SCH-27442 PDF: SPF-27442 | Rev H
Date: Thursday, January 23, 2014 | Sheet 4 of 11


Layout Note:
Place 0.22uF close to each SDRAMC pin,
better on opposite PCB side under the 364BGA.
VCC_1V5
SH10
SH0805_40
VCC_1V5_SDRAM
C10 4.7uF 10V 0603_CC
C103 C108 C118 C126 C135 0.22uF 16V
GND
U7A
E4 D5 F5 H5 K5 E7 E9 D11
SDRAMC_VDD1P5_1
SDRAMC_VDD1P5_2
SDRAMC_VDD1P5_3
SDRAMC_VDD1P5_4
SDRAMC_VDD1P5_5
SDRAMC_VDD1P5_6
SDRAMC_VDD1P5_7
SDRAMC_VDD1P5_8
VCC_2V5_SDRAM
C134 C121 C139 C77 0.22uF 16V
C141 4.7uF 10V 0603_CC
J5 E6 E10
SDRAMC_VDD2P5_1
SDRAMC_VDD2P5_2
SDRAMC_VDD2P5_3
T11
DECAP_V25_LDO_OUT
VCC_1V2
C22 4.7uF 10V 0603_CC
C52 C86 C90 C100 C48 C109 C50 C111 C49 C122 C120 0.22uF 16V
G7 J7 L7 H8 K8 M8 P8 G9 N9 H10 P10 G11 N11 H12 P12 G13 J13 L13 N13 H14 K14 M14 P14
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18 VDD19 VDD20 VDD21 VDD22 VDD23
N7
FA_VDD
Layout Note:
Place 0.22uF close to each VDD pin, better to place one
by one at the opposite PCB side under the 364BGA.
VCC_1V1
C59 10UF 16V 0805_CC
C61 0.22uF 16V
V12
DECAP_V11_LDO_OUT
P3V3
DD2
BAT54C-7-F
Diode prevents Vybrid's reset when J4 opens.
J4 1X2
MTMM-102-07-G-S-236
Default: 1-2 (use P3V3)
VCC_3V3_MCU
TP2
C41 10UF 0805_CC 16V
C132 C123 C117 C101 C83 C55 C172 C69 C99 C81 0.22uF 16V
K3 N3 V8 C12 C15 U16 K17 N17 T17 C18 F18 W18
VDD33_1 VDD33_2 VDD33_3 VDD33_4 VDD33_5 VDD33_6 VDD33_7 VDD33_8 VDD33_9 VDD33_10 VDD33_11 VDD33_12
Layout Note:
Place 0.1uF close to each VDD33 pin, better to place one
by one at the opposite PCB side under the 364BGA.
J1 1X3
MTMM-103-07-G-S-236
Default: 1-2 (use P3V3_MCU)
VCOIN
VBATD
R145 1.18K
BT1 BK-883
2016/25/32 Coin Cell
C45 0.22uF 16V
Vybrid_VBAT
VCC_3V3_MCU
C54 0.22uF 16V
T12
VDD33_LDOIN
V14
VBAT
P5
VDDREG
C43 4.7uF 0603_CC 10V
C145 0.22uF 16V
T2
BCTRL
D13 1N4448 DNP
D14 1N4448 DNP
R171 0
For application without 1.5V rail, i.e. without DDR. e.g. VF3xx: install diodes and move 0-Ohm resistor from posistion A to B. R171 default: position A.
C26 4.7uF 10V 0603_CC
Q1 PBSS4021NT
BCTRL
VCC_1V2
C47 4.7uF 10V
FB4 120 OHM
VCC_1V2_AFE
T5
VDD12_AFE
C76 0.22uF 16V
Best performance when x_AFE rails powered from dedicated linear voltage regulators.
R5
VSS12_AFE
FB6 120 OHM
VCC_3V3_AFE
V3
VDDA33_AFE
C56 10UF 0805_CC 16V
C62 0.22uF 16V
V4
VSSA33_AFE
FVBG
U5
VADC_AFE_BANDGAP
C68 0.22uF 16V
MVF61NS151CMK50
(PVF61NS151CMK50)
VSS1 A1 A20 B3 B5 B8 B11 B13 B16 B19 C2 D17 E5 E8 E11 E14 E19 F2 G17 H4 J2 J18 M2 M4 M18 R2 R18 U7 U19 V13 W6 V17 Y1 Y20 H19 L19 P19 H7 K7 M7 P7 G8 J8 L8 N8 H9 J9 K9 L9 M9 P9 G10 J10 K10 L10 M10 N10 H11 J11 K11 L11 M11 P11 G12 J12 K12 L12 M12 N12 H13 K13 M13 P13 G14 J14 L14 N14
VSS_KEL0
U11
GND
USB0_VBUS
W11
Peripheral USB Port
Vybrid_VBUS_PERIPHERAL
USB1_VBUS
W10
Host USB Port
Vybrid_VBUS_HOST
USB_DCAP
Y10
VCC_3V3_MCULDO
C13 0.22uF 16V
C11 10UF 0805_CC 16V
C58 0.22uF 16V
C57 10UF 0805_CC 16V
DNP
VDDA33_ADC
V1
VCC_3V3_ADC
FB5 120 OHM
VREFH_ADC
W1
VREF_3V3
FB7 120 OHM
C64 0.22uF 16V
C67 0.22uF 16V
C171 10UF 0805_CC 16V
U3
VREFL_ADC
VSSA33_ADC
V2
Best performance when x_ADC rails powered from dedicated linear voltage regulators.
Most critical for VREFH_ADC; without power filtering, actual ADC resolution might be degraded.
Default: 1-2
1-2: Peripheral, Self-powered
2-3: Peripheral, Bus-powered
J20 1X3
MTMM-103-07-G-S-236
P5V
From USB Peripheral Connector
USB0_VBUS 4,6,8,11
C12 0.1uF 10V
0402_CC
J21 1X2
MTMM-102-07-G-S-236
From USB Host Connector
USB1_VBUS 4,11
1.5V REGULATOR
3A max.
U26 IT7803M
R168 10.0K
R167 33
PVCC VCC EN PGND AGND GND PG LX FB
PG_1V5
IEN_3V3
IEN_1V5
L3 2.2uH
U26_0V8_FB
R172 0
DNP
SH1
SH0805_40
1V5
R169 8.87K 1%
R170 10.0K 1%
C15 10UF 16V 0805_CC
C169 0.1uF 10V
C170 0.1uF 10V
C20 10UF 16V 0805_CC
C21 10UF 16V 0805_CC
3.3V REGULATOR
3A max.
U11 IT7803M
R133 1.18K
R125 33
L2 2.2uH
U11_0V8_FB
3V3
SH2
SH0805_40
R127 30.9K 1%
R71 240
D9_3V3_ON
R128 10.0K 1%
C154 10UF 16V 0805_CC
C155 0.1uF 10V
C146 0.1uF 10V
C158 10UF 16V 0805_CC
C159 10UF 16V 0805_CC
D9 YEL/GRN
POWER ON
BCTRL pin protection: prevents applying 3.3V to Vybrid prior to 1.5V to Q1 collector.
BCTRL pin protection: prevents applying 3.3V to Vybrid prior to providing 1.5V for Q1.
D2 DNP
MBRA210LT3G
Q4 IRLML6401
R173 10.0K
ELE_PS_SENSE 6,8
P3V3_ELEV
Default: 1-2 (P3V3_ELEV)
J18 1X2
MTMM-102-07-G-S-236
Revision Modification Note:
Added:
- series ferrite beads on x_AFE and x_ADC rails (FB4, FB5, FB6, FB7).
- 1.5V DC/DC (U26, R168, R167, C169, C170, R172, L3, R169, R170, SH1).
- others (DD2, D13, D14, J9, DD4, R171, D2, Q4, R173).
Deleted: DDR termination U5, R98,..., U2.
DNP-ed: C57, C60, C63, C65, C66, and C110.
Changed:
- J20 from 1x4 to 1x3,
- C47 from 10uF to 4.7uF (as per Datasheet),
- R145 from 1.8K to 1.18K,
- R133 from 10K to 1.18K,
- Q1 from NJD2873T4 to PBSS4021NT,
- All 10uF 16V are 0805
- All 100mil headers to 2mm ones,
- J21 from 1x4 to 1x2,
- 0402 capacitors (close to MCU) footprint from CC0402_25 to 0402_CC, and change to be 0.22uF
- 0603 capacitors (close to MCU) footprint from CC0603_OV to 0603_CC. and change to be 4.7uF
freescale semiconductor
ICAP Classification: FCP:___ FIUO: X PUBI:___
Drawing Title:
TWR-VF65GS10
Page Title:
Power Distribution
Size C
Document Number SCH-27442 PDF: SPF-27442
Rev H
Date: Thursday, January 23, 2014
Sheet 5 of 11

# Serial Interface

## Reset

U13

PK20DX128VFM5

VCC_3V3_K20

P5V

P5V_SW

P5V_USB

P3V3

GND

DD1 BAT54C-7-F

C5 10UF 16V 0805_CC

TPV9

K20_VBAT

R70 0 DNP

C40 1uF 10V

C1 1uF 10V

C2 0.1uF 10V

K20_USB_DN

K20_USB_DP

R26 4.7K

RST_SI_B

R28 10.0K

Serial interface reset when USB port disconnected.

R89 33

R90 33

R160 10.0K

JTAG_TMS_SI

JTAG_TCLK_SI

JTAG_TDO_SI

JTAG_TDI_SI

RST_SI_B

FTSH-105-01-L-DV

JTAG_TCLK/SWD_CLK/EZP_CLK/TSI0_CH1/PTA0/UART0_CTS/UART0_COL/FTM0_CH5

JTAG_TDI/EZP_DI/TSI0_CH2/PTA1/UART0_RX/FTM0_CH6

JTAG_TDO/TRACE_SWO/EZP_DO/TSI0_CH3/PTA2/UART0_TX/FTM0_CH7

JTAG_TMS/SWD_DIO/TSI0_CH4/PTA3/UART0_RTS/FTM0_CH0

NMI/EZP_CS/TSI0_CH5/PTA4/FTM0_CH1/LLWU_P3

SWD_EN_SI_B

8MHz_EXTL

8MHz_XTL

X1 8.00MHZ

R88 1.0M

EXTAL0/PTA18/FTM0_FLT2/FTM_CLKIN0

XTAL0/PTA19/FTM1_FLT0/FTM_CLKIN1/LPTMR0_ALT1

ADC0_SE8/TSI0_CH0/PTB0/I2C0_SCL/FTM1_CH0/FTM1_QD_PHA/LLWU_P5

ADC0_SE9/TSI0_CH6/PTB1/I2C0_SDA/FTM1_CH1/FTM1_QD_PHB

SW_SEL_B

RESET_K20_B

R99 10.0K DNP

ADC0_SE15/TSI0_CH14/PTC1/SPI0_PCS3/UART1_RTS/FTM0_CH0/I2S0_TXD0/LLWU_P6

ADC0_SE4B/CMP1_IN0/TSI0_CH15/PTC2/SPI0_PCS2/UART1_CTS/FTM0_CH1/I2S0_TX_FS

CMP1_IN1/PTC3/SPI0_PCS1/UART1_RX/FTM0_CH2/I2S0_TX_BCLK/LLWU_P7

PTC4/SPI0_PCS0/UART1_TX/FTM0_CH3/CMP1_OUT/LLWU_P8

PTC5/SPI0_SCK/LPTMR0_ALT2/I2S0_RXD0/CMP0_OUT/LLWU_P9

CMP0_IN0/PTC6/SPI0_SOUT/PDB0_EXTRG/I2S0_RX_BCLK/I2S0_MCLK/LLWU_P10

CMP0_IN1/PTC7/SPI0_SIN/USB_SOF_OUT/I2S0_RX_FS

SI_SPI0_CS

K20_UART1_RX

K20_UART1_TX

SI_SPI0_SCK

SI_SPI0_SOUT

SI_SPI0_SIN

PTD4/SPI0_PCS1/UART0_RTS/FTM0_CH4/EWM_IN/LLWU_P14

ADC0_SE6B/PTD5/SPI0_PCS2/UART0_CTS/UART0_COL/FTM0_CH5/EWM_OUT

ADC0_SE7B/PTD6/SPI0_PCS3/UART0_RX/FTM0_CH6/FTM0_FLT0/LLWU_P15

PTD7/CMT_IRO/UART0_TX/FTM0_CH7/FTM0_FLT1

D5 YEL

R31 1.18K

R35 10.0K

R34 10.0K

R38 10.0K

R42 1.18K

Q2 NTS4001NT1G sc70_3

C161 0.1uF 10V

U3 MIC2506YM

IN CTLA OUTA OUTB CTLB GND FLGA FLGB

ELE_PS_SENSE

From USB Peripheral Connector

USB0_VBUS

J19 1X3 MTMM-103-07-G-S-236

Default: 1-2 (OpenSDA)

+5V

TP17 DNP

P5V

Default: 1-2 (P5V_ELEV)

P5V_ELEV

J25 1X2 MTMM-102-07-G-S-236

TZ1 SMCJ5.0A

C163 0.1uF 10V

GND1

GND2

R161 10.0K DNP

R25 10.0K

R152 10.0K

U14A MC74HC125ADTG

U14B MC74HC125ADTG

U14C MC74HC125ADTG

U14D MC74HC125ADTG

SH3

SH4

SH0805_40

OpenSDA_UART_RX 9

OpenSDA_UART_TX 9

PTA[6..31] 4,7,8,9

SWCLK

SWDIO

R189 0

R190 0

PTA8

PTA11

Reset

Q3 NTS4001NT1G sc70_3

SW3 PB switch

MANUAL RESET

R162 DNP

C165 0.1uF 10V DNP

U25 MCP130T-300I/TT

VDD VSS RST

C3 0.1uF 10V

R36 1.18K

R37 4.7K DNP

RSTR

D7 ORANGE RESET

{2.85V to 3.0V Threshold}
{150 to 400 ms delay}
{RST - Open Drain with Built-In 5K pull-Up}

RESET_B 4,7,8,9

## OpenSDA Debug Interface

### Peripheral (OTG, Micro-B)

USB-SHLD1

SHELL1 SHELL2 SHELL3 SHELL4

VBUS D- D+ ID GND

J3 1050170001

USB_VBUS

USB_DN

USB_DP

R33 100

C4 1000pF 50V

U21 RCLAMP1654P.TCT

DN DP USB_ID VBUS GND

FB3 120 OHM IND_0402

P5V_USB

TP1 DNP

C160 1uF 10V

Revision Modification Note:

Added: DD1, Q3, U25, D13, TZ1, R160, TP16, J19, J28, U25 (to improve SD boot).

Deleted: U16, U17, C18, C97, U1, C39.

DNP-ed:
- R99,
- R37 (and changed from 10K to 4.7K).
- R161, R162, C165

Changed:
- R31 and R36 from 240 to 1.18K (to optimize D7 brightness),
- Ferrite beads from 330/0805 to 120/0402,
- Q2 from MMBT3904 to NTS4001NT1G,
- R42 from 10K to 1.18K.

freescale semiconductor

ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **TWR-VF65GS10**

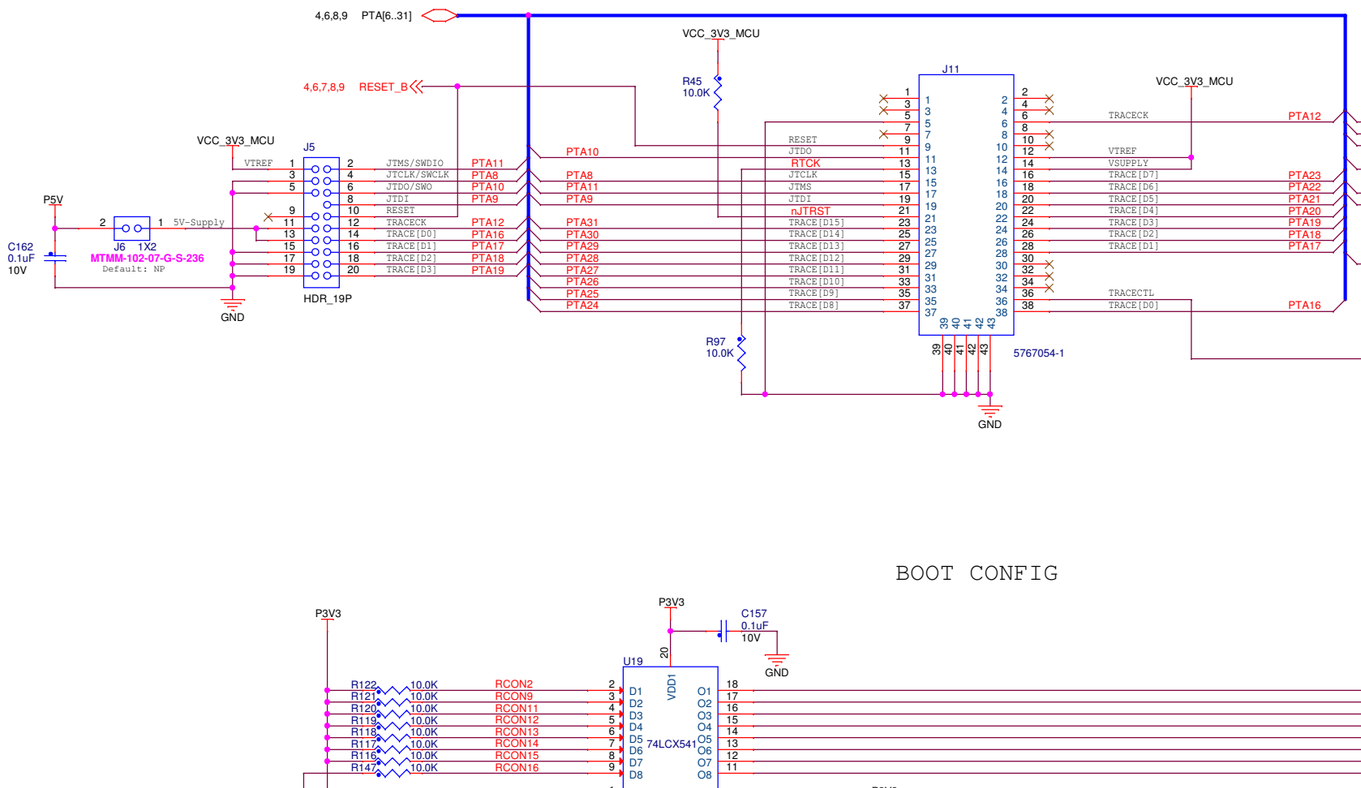
Page Title: **Serial Interface**

| Size | Document Number | Rev |
|---|---|---|
| C | SCH-27442 PDF: SPF-27442 | H |

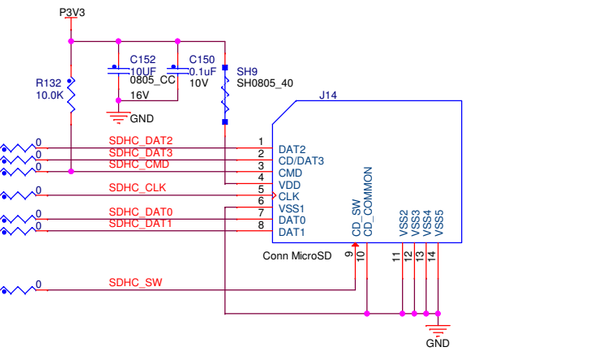
Date: Thursday, January 23, 2014 Sheet 6 of 11

## JTAG+TRACE 38pin MICTOR ETMv3

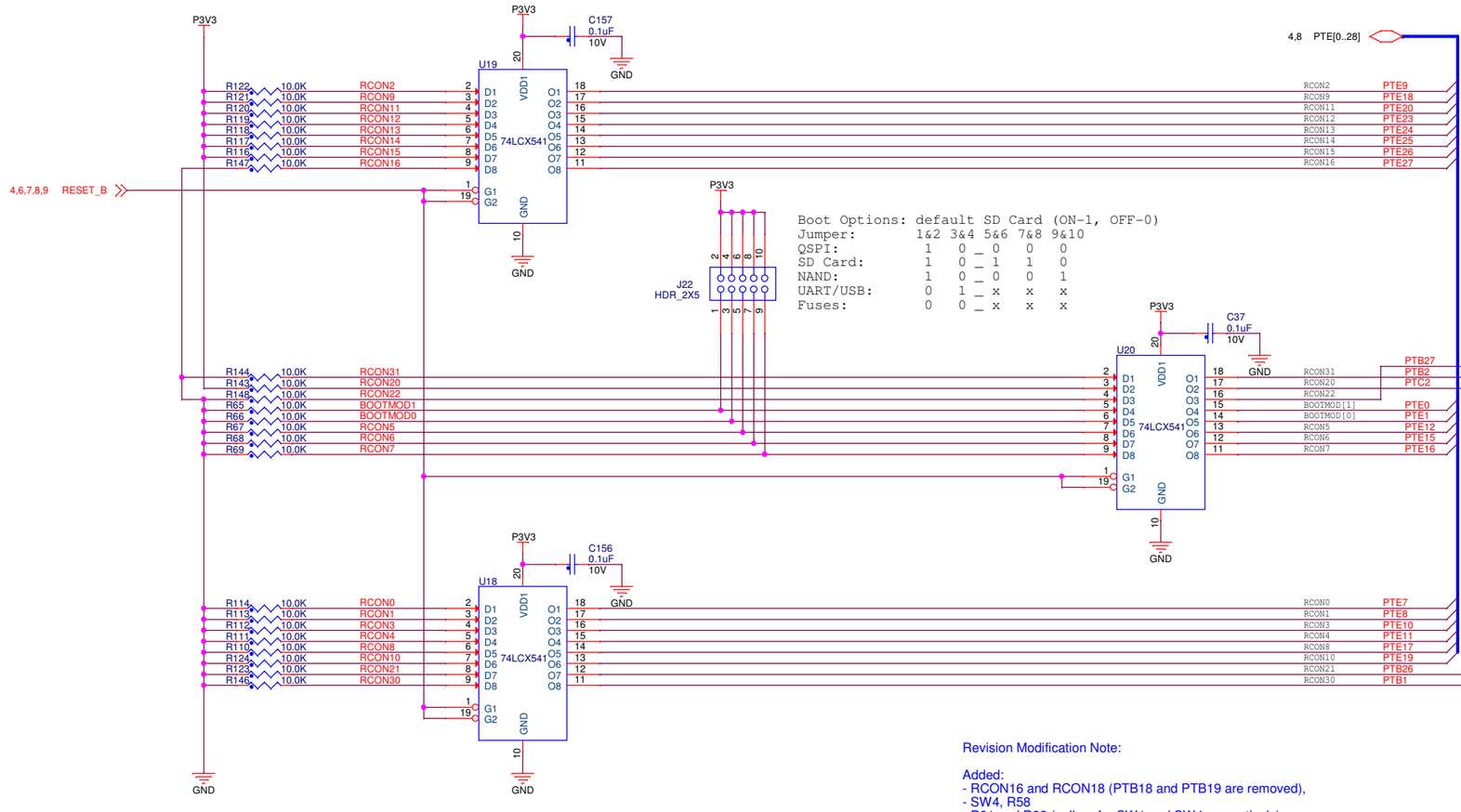
*Layout Note:*
*Place 38-pin connector in corner on top side, oriented so that ribbon cable comes out of tower board.*



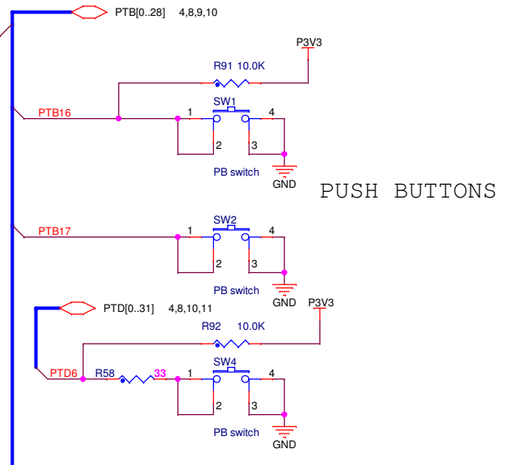

## MICRO SD INTERFACE



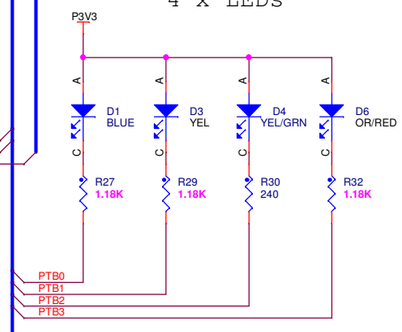

## BOOT CONFIG




## PUSH BUTTONS




## 4 x LEDs




Revision Modification Note:

Added:
- RCON16 and RCON18 (PTB18 and PTB19 are removed),
- SW4, R58
- R91 and R92 (pull-up for SW1 and SW4 respectively)

Deleted: R70.

Changed:
- R29 and R32 from 1K to 1.18K to optimize D3 brightness,
- R27 from 240 to 1.18K to optimize D1 brightness,
- J22 from larger 2x6 with 2mm pitch to smaller 2x5 with 2mm pitch (USB0_SEL function deleted).

freescale semiconductor

ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **TWR-VF65GS10**

Page Title: **Peripherals**

| Size | Document Number | Rev |
|---|---|---|
| C | SCH-27442 PDF: SPF-27442 | H |

Date: Thursday, January 23, 2014 Sheet 7 of 11

Optional MII0 interface:

PTA6 ? MII0_TXCLK to J17A ?B14 (also used as RMII_CLKIN)
PTA21 ?MII0_RXCLK to J17A ?A15 (also used as AI2_RX_BCLK)
PTD17 ?MII0_TXERR to J17A ?B16
PTD18 ?MII0_TX2 to J17A ?B18
PTD19 ?MII0_TX3 to J17A ?B17
PTD20 ?MII0_COL to J17A ?B12
PTD21 ?MII0_CRS to J17A ?A12
PTD22 ?MII0_RX2 to J17A ?A18
PTD23 ?MII0_RX3 to J17A ?A17

PTDx signals also used by NAND => no simultaneous use of NAND and MII0.

PTD17 R175 0 DNP MII0_TXERR
PTD18 R176 0 DNP MII0_TX2
PTD19 R177 0 DNP MII0_TX3
PTD20 R178 0 DNP MII0_COL
PTD21 R179 0 DNP MII0_CRS
PTD22 R180 0 DNP MII0_RX2
PTD23 R181 0 DNP MII0_RX3

4,7,10,11 PTD[0..31]
4,7,9,10,11 PTC[0..31]
4,7,9,10 PTB[0..28]

P5V_ELEV
P3V3_ELEV

J17A

| | | | | | |
|---|---|---|---|---|---|
| B1 | 5V_1 | | A1 | 5V_2 | |
| B2 | GND_1 | | A2 | GND_9 | |
| B3 | 3.3V_1 | | A3 | 3.3V_4 | |
| B4 | ELE_PS_SENSE_1 | 5,6,8 ELE_PS_SENSE | A4 | 3.3V_5 | |
| B5 | GND_2 | | A5 | GND_10 | |
| B6 | GND_3 | | A6 | GND_11 | |
| B7 | SDHC_CLK/SPI1_CLK | | A7 | I2C0_SCL | I2C0_SCL R183 0 PTB14 |
| B8 | SDHC_D3/SPI1_CS1 | | A8 | I2C0_SDA | I2C0_SDA R185 0 PTB15 |
| B9 | SDHC_D3/SPI1_CS0 | | A9 | GPIO9/UART1_CTS | EGPIO9 R85 0 PTB12 |
| B10 | SDHC_CMD/SPI1_MOSI | | A10 | GPIO8/SDHC_D2 | EGPIO8 R86 0 PTB9 |
| B11 | SDHC_D0/SPI1_MISO | | A11 | GPIO7/SD_WP_DET | EGPIO7 R87 0 PTB28 |
| B12 | ETH_COL_1 | MII0_COL | A12 | MII0_CRS | |
| B13 | ETH_RXER_1 | PTC5 RMII0_RXER MII0_TXCLK | A13 | RMII0_MDC | PTC0 PTC14 |
| B14 | ETH_TXCLK_1 | | A14 | RMII0_MDIO | PTC1 |
| B15 | ETH_TXEN_1 | PTC8 RMII0_TXEN MII0_TXERR | A15 | MII0_RXCLK | PTC17 |
| B16 | ETH_TXER | MII0_TX3 | A16 | RMII0_CRS_DV | PTC2 |
| B17 | ETH_TXD3 | MII0_TX2 | A17 | MII0_RX3 | |
| B18 | ETH_TXD2 | | A18 | MII0_RX2 | |
| B19 | ETH_TXD1_1 | PTC6 RMII0_TXD[1] | A19 | RMII0_RXD[1] | PTC3 PTC15 |
| B20 | ETH_TXD0_1 | PTC7 RMII0_TXD[0] | A20 | RMII0_RXD[0] | PTC4 PTC16 |
| B21 | GPIO1/UART1_RTS | PTB10 0 R24 EGPIO1 | A21 | EXT_AUDIO_MCLK | |
| B22 | GPIO2/SDHC_D1 | PTB23 0 R23 EGPIO2 | A22 | SAI2_TX_BCLK | R191 33 PTA16 |
| B23 | GPIO3 | PTB26 0 R22 EGPIO3 | A23 | SAI2_TX_SYNC | R192 33 |
| B24 | CLKIN0 | CLK_IN0 | A24 | SAI2_RX_DATA | R193 33 |
| B25 | CLKOUT1 | | A25 | SAI2_TX_DATA | R194 33 |
| B26 | GND_4 | | A26 | | |
| B27 | AN7 | | A27 | | |
| B28 | AN6 | PTC30 0 R20 ADC0SE5 | A28 | | ADC0SE8 4,9 |
| B29 | AN5 | PTC31 0 R19 ADC1SE5 | A29 | | ADC0SE9 4,9 |
| B30 | AN4 | | A30 | | ADC1SE8 4,9 |
| B31 | GND_5 | 4 DACO1 | A31 | | ADC1SE9 4,9 |
| B32 | DAC1 | | A32 | GND_13 | DACO0 4 |
| B33 | TMR3 | PTA31 R18 33 ENET_1588_TMR3 | A33 | DAC0 | ENET_1588_TMR1 R78 33 PTA29 |
| B34 | TMR2 | PTA30 R17 33 ENET_1588_TMR2 | A34 | TMR1 | ENET_1588_TMR0 R79 33 PTA28 |
| B35 | GPIO4 | | A35 | TMR0 | EGPIO6 R80 0 PTB18 |
| B36 | 3.3V_2 | PTB6 R16 0 | A36 | GPIO6 | |
| B37 | PWM7 | PTB9 R15 0 DNP FTM1CH1 | A37 | 3.3V_6 | FTM0CH3 PTB3 |
| B38 | PWM6 | PTB8 R14 0 DNP FTM1CH0 | A38 | PWM3 | FTM0CH2 PTB2 |
| B39 | PWM5 | PTB7 R13 0 FTM0CH7 | A39 | PWM2 | FTM0CH1 PTB1 |
| B40 | PWM4 | PTB6 R12 0 FTM0CH6 | A40 | PWM1 | FTM0CH0 PTB0 |
| B41 | CAN0_RX | PTB16 R11 0 DNP CAN1_RX | A41 | PWM0 | R81 0 DNP SCI1_RX PTB5 |
| B42 | CAN0_TX | PTB17 R10 0 DNP CAN1_TX | A42 | UART0_RX | R82 0 DNP SCI1_TX PTB4 |
| B43 | 1WIRE | | A43 | UART0_TX | |
| B44 | SPI0_MISO/IO1 | PTB20 R9 0 DSPI0_SIN_0 | A44 | UART1_RX | ELEV_UART1_RX 9 |
| B45 | SPI0_MOSI/IO0 | PTB21 R8 0 DSPI0_SOUT_0 | A45 | UART1_TX | ELEV_UART1_TX 9 |
| B46 | SPI0_CS0 | PTB19 R7 0 DSPI0_PCS0_0 | A46 | VSSA | |
| B47 | SPI0_CS1 | | A47 | VDDA | |
| B48 | SPI0_CLK | PTB22 R6 0 DSPI0_SCK_0 | A48 | CAN1_RX | CAN0_RX R83 0 DNP PTB14 |
| B49 | GND_6 | | A49 | CAN1_TX | CAN0_TX R84 0 DNP PTB15 |
| B50 | I2C1_SCL | PTB14 R187 0 I2C0_SCL | A50 | GND_14 | FB13 DNP 1 2 120 OHM P3V3_ELEV |
| B51 | I2C1_SDA | PTB15 R188 0 I2C0_SDA | A51 | GPIO14 | FB14 DNP GND 1 2 120 OHM |
| B52 | GPIO5/SPI0_HOLD/IO3 | PTA20 R5 33 EGPIO5 | A52 | GPIO15 | |
| B53 | RSRV_B53 | | A53 | GPIO16/SPI0_WP/IO2 | |
| B54 | RSRV_B54 | | A54 | GPIO17 | |
| B55 | IRQ_H | PTB7 R4 0 EIRQ3 | A55 | USB0_DM | ELEV_USB0_DN 11 |
| B56 | IRQ_G | | A56 | USB0_DP | ELEV_USB0_DP 11 |
| B57 | IRQ_F | PTA31 R3 33 EIRQ2 | A57 | USB0_ID | |
| B58 | IRQ_E | | A58 | USB0_VBUS | USB0_VBUS 4,5,6,11 |
| B59 | IRQ_D | PTA30 R2 33 EIRQ1 | A59 | I2S0_DIN_SCK | SAI2_RX_BCLK |
| B60 | IRQ_C | | A60 | I2S0_DIN_WS | SAI2_TX_SYNC R195 33 PTA23 PTA30 |
| B61 | IRQ_B | PTB12 R1 0 EIRQ0 | A61 | I2S0_DIN1 | PTA18 PTA31 |
| B62 | IRQ_A | | A62 | I2S0_DOUT1 | |
| B63 | EBI_ALE/EBI_CS1 | | A63 | RSTIN | RESET_B 4,6,7,9 |
| B64 | EBI_CS0 | | A64 | RSTOUT | PTE3 |
| B65 | GND_7 | | A65 | CLKOUT0 | |
| B66 | EBI_AD15 | | A66 | GND_15 | |
| B67 | EBI_AD16 | | A67 | EBI_AD14 | |
| B68 | EBI_AD17 | | A68 | EBI_AD13 | |
| B69 | EBI_AD18 | | A69 | EBI_AD12 | |
| B70 | EBI_AD19 | | A70 | EBI_AD11 | |
| B71 | EBI_R/W | | A71 | EBI_AD10 | |
| B72 | EBI_OE | | A72 | EBI_AD9 | |
| B73 | EBI_D7 | | A73 | EBI_AD8 | |
| B74 | EBI_D6 | | A74 | EBI_AD7 | |
| B75 | EBI_D5 | | A75 | EBI_AD6 | |
| B76 | EBI_D4 | | A76 | EBI_AD5 | |
| B77 | EBI_D3 | | A77 | EBI_AD4 | |
| B78 | EBI_D2 | | A78 | EBI_AD3 | |
| B79 | EBI_D1 | | A79 | EBI_AD2 | |
| B80 | EBI_D0 | | A80 | EBI_AD1 | |
| B81 | GND_8 | | A81 | EBI_AD0 | |
| B82 | 3.3V_3 | | A82 | GND_16 | |
| | | | | 3.3V_7 | |

PCI EXPRESS TOWER SYSTEM PRIMARY

GND GND

4,6,7,9 PTA[6..31]

RMII_CLKIN
A
R21 0
B
PTA6
MII0_TXCLK

Use (R21) to switch between RMII CLK and MII TXCLK.
R21 default: Position A

To use CAN1, populate R10 and R11. SW1 and SW2 push buttons (Sheet 7) cannot be used in this case.

A
R182 0
B
R56 33 PTA21
MII0_RXCLK

Use (R182) to switch between SAI RX BCLK and MII RXCLK.
R182 default: Position A

P3V3_ELEV

J17B

| | | | | | |
|---|---|---|---|---|---|
| D1 | 5V_3 | | C1 | 5V_4 | |
| D2 | GND_17 | | C2 | GND_25 | |
| D3 | 3.3V_8 | | C3 | 3.3V_11 | |
| D4 | ELE_PS_SENSE_2 | 5,6,8 ELE_PS_SENSE | C4 | 3.3V_12 | |
| D5 | GND_18 | | C5 | GND_26 | |
| D6 | GND_19 | | C6 | GND_27 | |
| D7 | SPI2_CLK | PTB22 R61 0 DSPI0_SCK_1 | C7 | I2C2_SCL | I2C0_SCL R184 0 PTB14 |
| D8 | SPI2_CS1 | | C8 | I2C2_SDA | I2C0_SDA R186 0 PTB15 |
| D9 | SPI2_CS0 | PTB19 R62 0 DSPI0_PCS0_1 | C9 | GPIO25 | |
| D10 | SPI2_MOSI | PTB21 R63 0 DSPI0_SOUT_1 | C10 | ULPI_STOP | |
| D11 | SPI2_MISO | PTB20 R64 0 DSPI0_SIN_1 | C11 | ULPI_CLK | |
| D12 | ETH_COL_2 | PTB8 | C12 | GPIO26 | |
| D13 | ETH_RXER_2 | RMII1_RXER | C13 | ETH_MDC_2 | RMII1_MDC PTC9 |
| D14 | ETH_TXCLK_2 | | C14 | ETH_MDIO_2 | RMII1_MDIO PTC10 |
| D15 | ETH_TXEN_2 | RMII1_TXEN | C15 | ETH_RXCLK_2 | |
| D16 | ETH_RXDV_2 | | C16 | ETH_RXDV_2 | RMII1_CRS_DV PTC11 |
| D17 | GPIO18 | | C17 | GPIO27/SDHC_D6 | |
| D18 | GPIO19/SDHC_D4 | | C18 | GPIO28/SDHC_D7 | |
| D19 | GPIO20/SDHC_D5 | | C19 | ETH_RXD1_2 | RMII1_RXD[1] PTC12 |
| D20 | ETH_TXD1_2 | RMII1_TXD[1] | C20 | ETH_RXD0_2 | RMII1_RXD[0] PTC13 |
| D21 | ETH_TXD0_2 | RMII1_TXD[0] | C21 | ULPI_DATA0/I2S1_MCLK | |
| D22 | ULPI_NEXT/USB_HS_DM | | C22 | ULPI_DATA1/I2S1_DOUT_SCK | |
| D23 | ULPI_DIR/USB_HS_DP | | C23 | ULPI_DATA2/I2S1_DOUT_WS | |
| D24 | ULPI_DATA5/USB_HS_VBUS | | C24 | ULPI_DATA3/I2S1_DIN0 | |
| D25 | ULPI_DATA6/USB_HS_ID | | C25 | ULPI_DATA4/I2S1_DOUT0 | |
| D26 | ULPI_DATA7 | | C26 | | |
| D27 | GND_20 | | C27 | GND_28 | |
| D28 | LCD_HSYNC/LCD_P24 | PTE0 DCU0_HSYNC | C28 | AN11 | |
| D29 | LCD_VSYNC/LCD_P25 | PTE1 DCU0_VSYNC | C29 | AN10 | |
| D30 | AN13 | | C30 | AN9 | |
| D31 | AN12 | | C31 | AN8 | |
| D32 | GND_21 | PTE2 DCU0_PCLK | C32 | GND_29 | |
| D33 | LCD_CLK/LCD_P26 | | C33 | GPIO29/UART2_DCD | |
| D34 | TMR11 | | C34 | TMR9 | |
| D35 | TMR10 | | C35 | TMR8 | |
| D36 | GPIO21 | | C36 | GPIO30/UART3_DCD | |
| D37 | 3.3V_9 | | C37 | 3.3V_13 | |
| D38 | PWM15 | | C38 | PWM11 | |
| D39 | PWM14 | | C39 | PWM10 | |
| D40 | PWM13 | | C40 | PWM9 | |
| D41 | PWM12 | | C41 | PWM8 | |
| D42 | CAN2_RX | | C42 | UART2_RXD/TSI0 | |
| D43 | CAN2_TX | | C43 | UART2_TXD/TSI1 | |
| D44 | LCD_CONTRAST | LCD_ENABLE | C44 | UART2_RTS/TSI2 | |
| D45 | LCD_OE/LCD_P27 | PTE4 DCU0_DE | C45 | UART2_CTS/TSI3 | |
| D46 | LCD_D0/LCD_P0 | PTE21 DCU0_B0 | C46 | UART3_RXD/TSI4 | |
| D47 | LCD_D1/LCD_P1 | PTE22 DCU0_B1 | C47 | UART3_TXD/TSI5 | |
| D48 | LCD_D2/LCD_P2 | PTE23 DCU0_B2 | C48 | UART3_RTS/CAN3_RX | |
| D49 | LCD_D3/LCD_P3 | PTE24 DCU0_B3 | C49 | UART3_CTS/CAN3_TX | |
| D50 | GND_22 | | C50 | GND_30 | DCU0_B4 PTE25 |
| D51 | GPIO23 | | C51 | LCD_D4/LCD_P4 | DCU0_B5 PTE26 |
| D52 | GPIO24 | | C52 | LCD_D5/LCD_P5 | DCU0_B6 PTE27 |
| D53 | LCD_D12/LCD_P12 | PTE17 DCU0_G4 | C53 | LCD_D6/LCD_P6 | DCU0_B7 PTE28 |
| D54 | LCD_D13/LCD_P13 | PTE18 DCU0_G5 | C54 | LCD_D7/LCD_P7 | DCU0_G0 PTE13 |
| D55 | LCD_D14/LCD_P14 | PTE19 DCU0_G6 | C55 | LCD_D8/LCD_P8 | DCU0_G1 PTE14 |
| D56 | IRQ_P/SPI2_CS2 | R72 0 EIRQ7 | C56 | LCD_D9/LCD_P9 | DCU0_G2 PTE15 |
| D57 | IRQ_O/SPI2_CS3 | R73 0 EIRQ6 | C57 | LCD_D10/LCD_P10 | DCU0_G3 PTE16 |
| D58 | IRQ_N | | C58 | LCD_D11/LCD_P11 | |
| D59 | IRQ_M | R74 33 EIRQ5 | C59 | I2S1_DIN_SCK | |
| D60 | IRQ_L | | C60 | I2S1_DIN_WS | |
| D61 | IRQ_K | R75 33 EIRQ4 | C61 | I2S1_DIN1 | |
| D62 | IRQ_J | | C62 | I2S1_DOUT1 | DCU0_G7 PTE20 |
| D63 | IRQ_I | PTE7 DCU0_R2 | C63 | LCD_D15/LCD_P15 | DCU0_R0 PTE5 |
| D64 | LCD_D18/LCD_P18/SD_RX_0+ | PTE8 DCU0_R3 | C64 | LCD_D16/LCD_P16/SD_GND | DCU0_R1 PTE6 |
| D65 | LCD_D19/LCD_P19/SD_RX_0- | | C65 | LCD_D17/LCD_P17/SD_GND | |
| D66 | GND_23 | | C66 | GND_31 | |
| D67 | EBI_AD20/LCD_P42/SD_GND | | C67 | EBI_BE_32_24/LCD_P28/SD_TX_0+ | |
| D68 | EBI_AD21/LCD_P43/SD_GND | | C68 | EBI_BE_23_16/LCD_P29/SD_TX_0- | |
| D69 | EBI_AD22/LCD_P44/SD_RX_1+ | | C69 | EBI_BE_15_8/LCD_P30/SD_GND | |
| D70 | EBI_AD23/LCD_P45/SD_RX_1- | | C70 | EBI_BE_7_0/LCD_P31/SD_GND | |
| D71 | EBI_AD24/LCD_P46/SD_GND | | C71 | EBI_TSIZE0/LCD_P32/SD_TX_1+ | |
| D72 | EBI_AD25/LCD_P47/SD_GND | | C72 | EBI_TSIZE1/LCD_P33/SD_TX_1- | |
| D73 | EBI_AD26/LCD_P48/SD_RX_2+ | | C73 | EBI_TS/LCD_P34/SD_GND | |
| D74 | EBI_AD27/LCD_P49/SD_RX_2- | | C74 | EBI_TBST/LCD_P35/SD_GND | |
| D75 | EBI_AD28/LCD_P50/SD_GND | | C75 | EBI_TA/LCD_P36/SD_TX_2+ | |
| D76 | EBI_AD29/LCD_P51/SD_GND | | C76 | EBI_CS4/LCD_P37/SD_TX_2- | |
| D77 | EBI_AD30/LCD_P52/SD_RX_3+ | | C77 | EBI_CS3/LCD_P38/SD_GND | |
| D78 | EBI_AD31/LCD_P53/SD_RX_3- | | C78 | EBI_CS2/LCD_P39/SD_GND | |
| D79 | LCD_D20/LCD_P20/SD_GND | | C79 | EBI_CS1/LCD_P40/SD_TX_3+ | |
| D80 | LCD_D21/LCD_P21/SD_REFCLK+ | PTE9 DCU0_R4 | C80 | GPIO31/LCD_P41/SD_TX_3- | DCU0_R7 PTE12 |
| D81 | LCD_D22/LCD_P22/SD_REFCLK- | PTE10 DCU0_R5 | C81 | LCD_D23/LCD_P23/SD_GND | |
| D82 | GND_24 | PTE11 DCU0_R6 | C82 | GND_32 | |
| | 3.3V_10 | | | 3.3V_14 | |

PCI EXPRESS TOWER SYSTEM SECONDARY

GND GND

PTE[0..28] 4,7

Revision Modification Note:

Added:
- Series 0-Ohm resistors into I2C0, I2C1, and I2C2 lines to Elevator for flexibility.
- DNP-ed series 0-Ohm resistors for optional MII0 interface (R175-R181).
- R182 3-pad, R56, R191, R192, R193, R194.

Changed:
- R21 made 3-pad,
- R2, R3, R17, R18, R74, and R75 from 0R to 33R
  (to improve signal integrity on PTA30 and PTA31 lines bearing TRACE signals).

freescale semiconductor

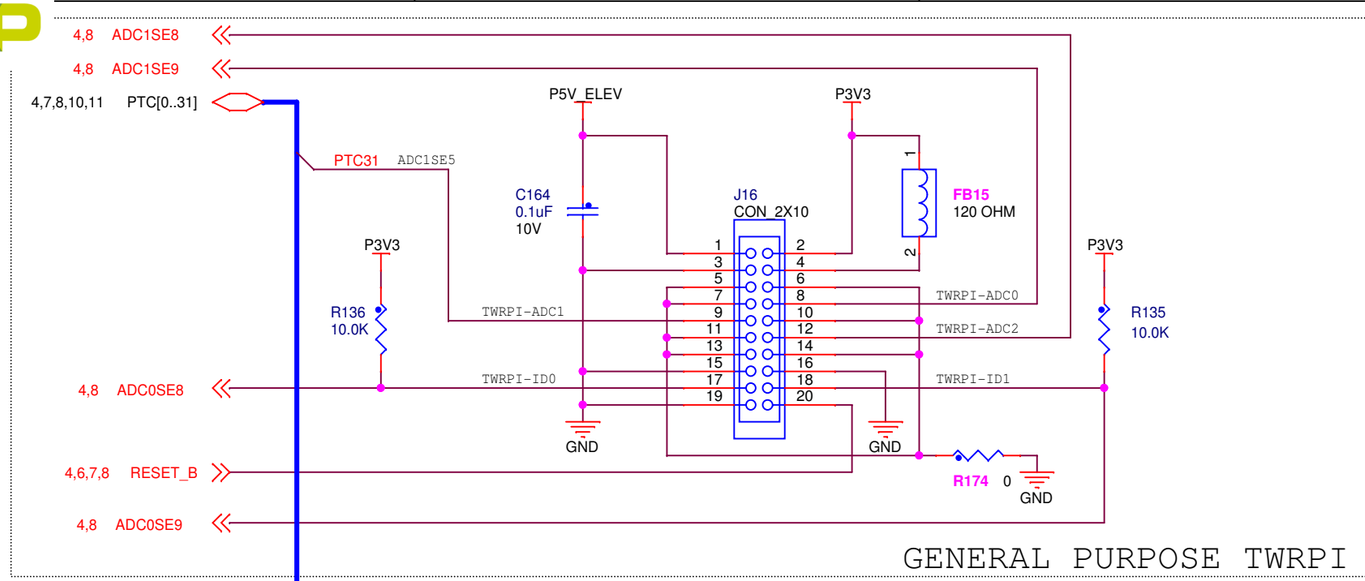
ICAP Classification: FCP:___ FIUO: X PUBI: ___

Drawing Title:
**TWR-VF65GS10**

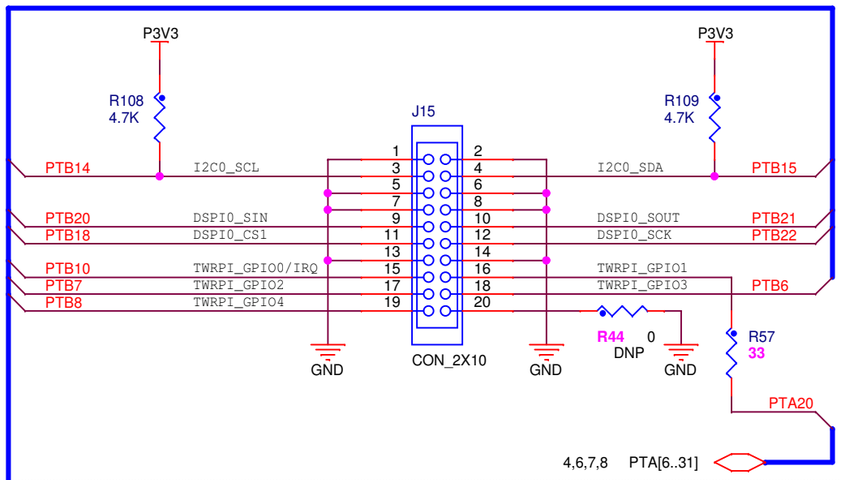
Page Title:
**Elevator Connector**

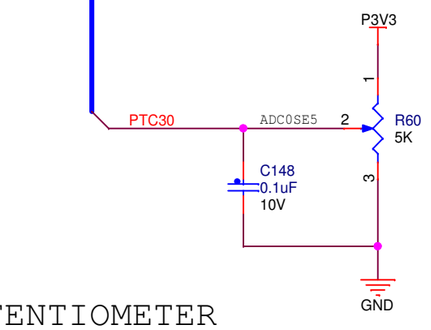
| Size | Document Number | Rev |
|---|---|---|
| C | SCH-27442 PDF: SPF-27442 | H |

Date: Thursday, January 23, 2014 Sheet 8 of 11




GENERAL PURPOSE TWRPI



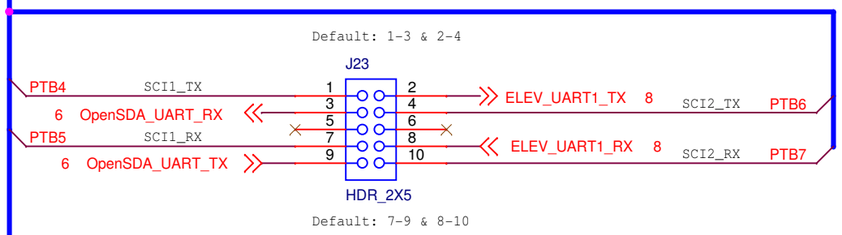

POTENTIOMETER

Default:

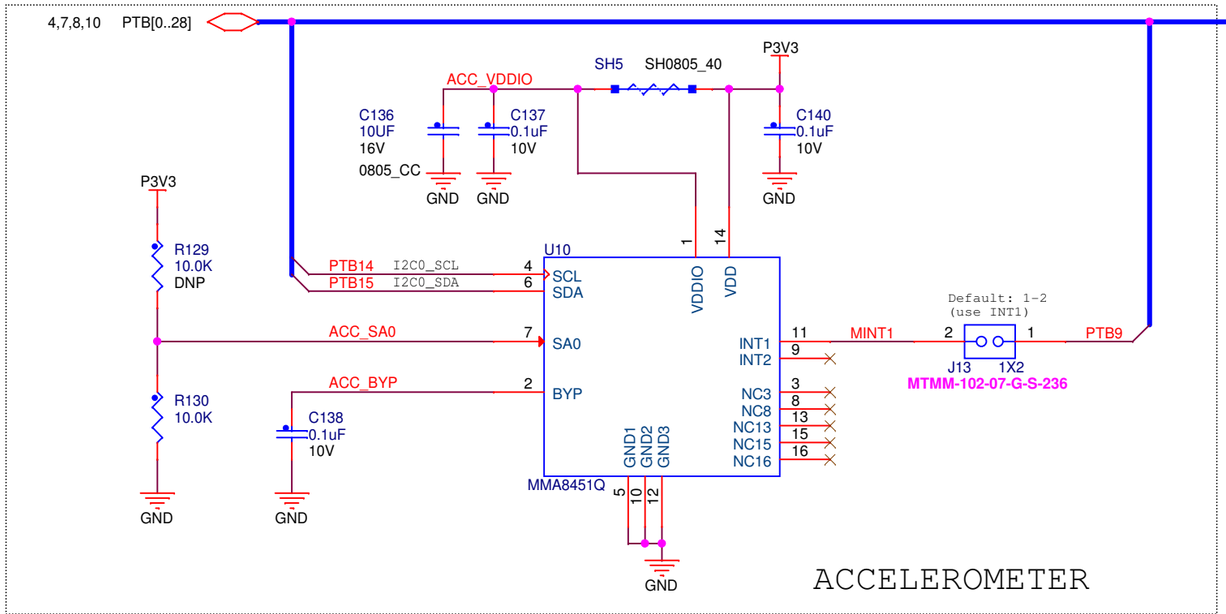
J23 (1-3 & 2-4) and (7-9 & 8-10)
Vybrid SCI1 to OpenSDA (K20)
Vybrid SCI2 to Elev UART1 (TWR-SER)

Alternative 1:
J23 (1-2 & 3-4) and (7-8 & 9-10)
Vybrid SCI1 to Elev UART1 (TWR-SER)
Vybrid SCI2 to OpenSDA (K20)

Alternative 2:
J23 (2-4) and (8-10)
Vybrid SCI1 to Elev UART0 (populate R81 and R82)
Vybrid SCI2 to Elev UART1 (TWR-SER)




SERIAL PORTS SELECTION




ACCELEROMETER

Revision Modification Note:

Added: FB15, R174, R44 (DNP-ed), R57.

Changed: J23 (2x2) + J24 (2x2) replaced with J23 (2x5 2mm pitch) (BOM consolidation)

freescale semiconductor

ICAP Classification: FCP:___ FIUO: X PUBI:___

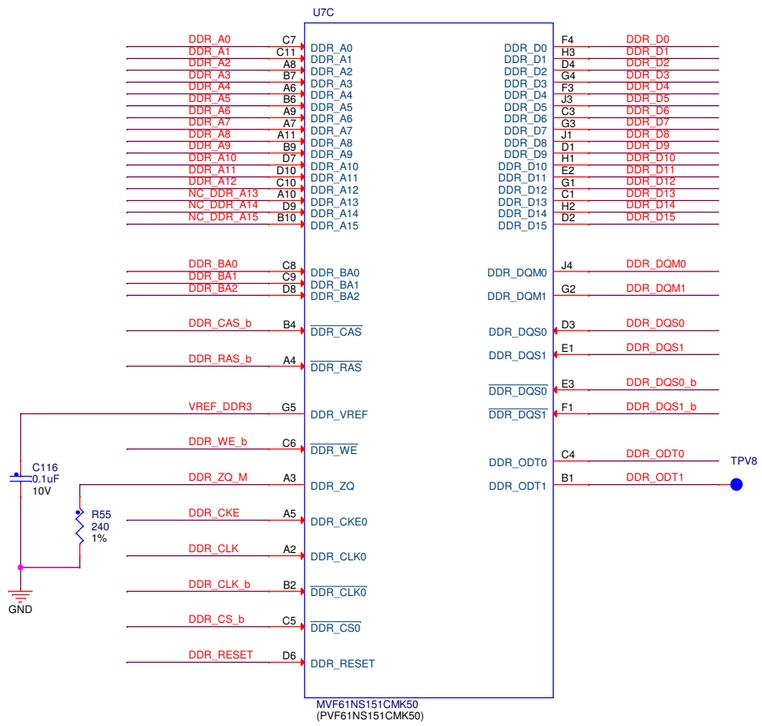
Drawing Title:
**TWR-VF65GS10**

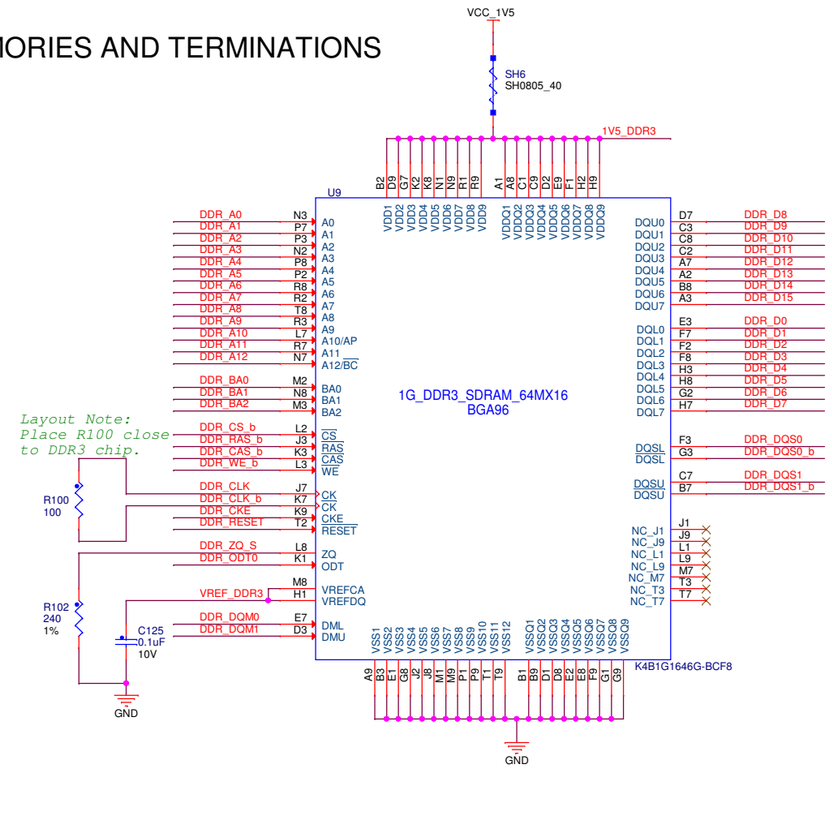
Page Title:
**TWRPI & POT & ACC & SS**

| Size | Document Number | Rev |
|---|---|---|
| B | SCH-27442 PDF: SPF-27442 | H |

Date: Thursday, January 23, 2014 Sheet 9 of 11

# DDR3 MEMORIES AND TERMINATIONS

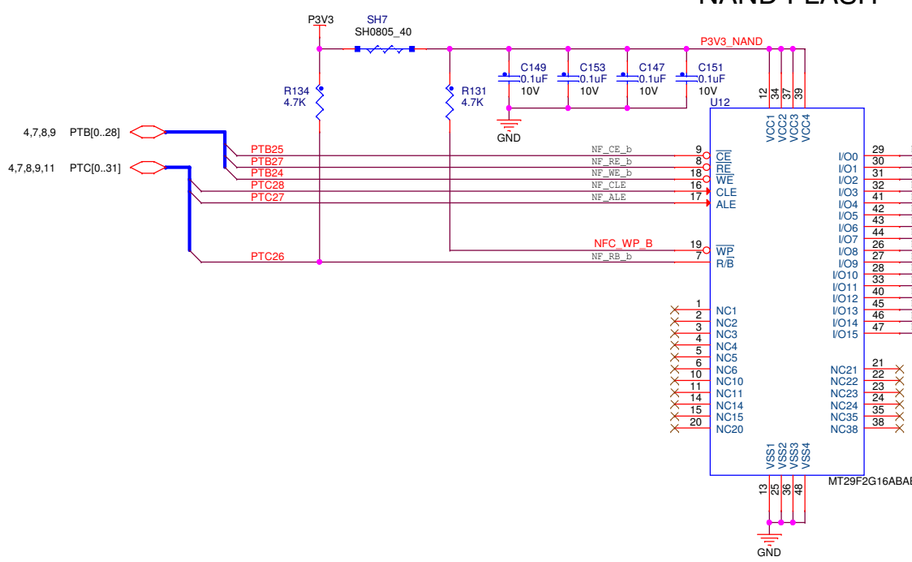


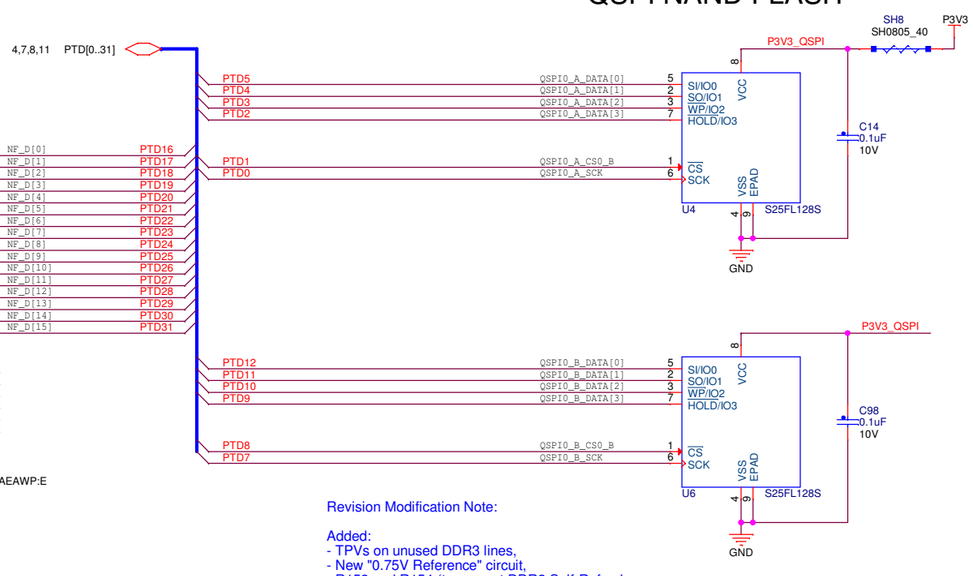




## NAND FLASH




## QSPI NAND FLASH




Revision Modification Note:

Added:
- TPVs on unused DDR3 lines,
- New "0.75V Reference" circuit,
- R153 and R154 (to support DDR3 Self-Refresh mode when Vybrid in LPStop modes).

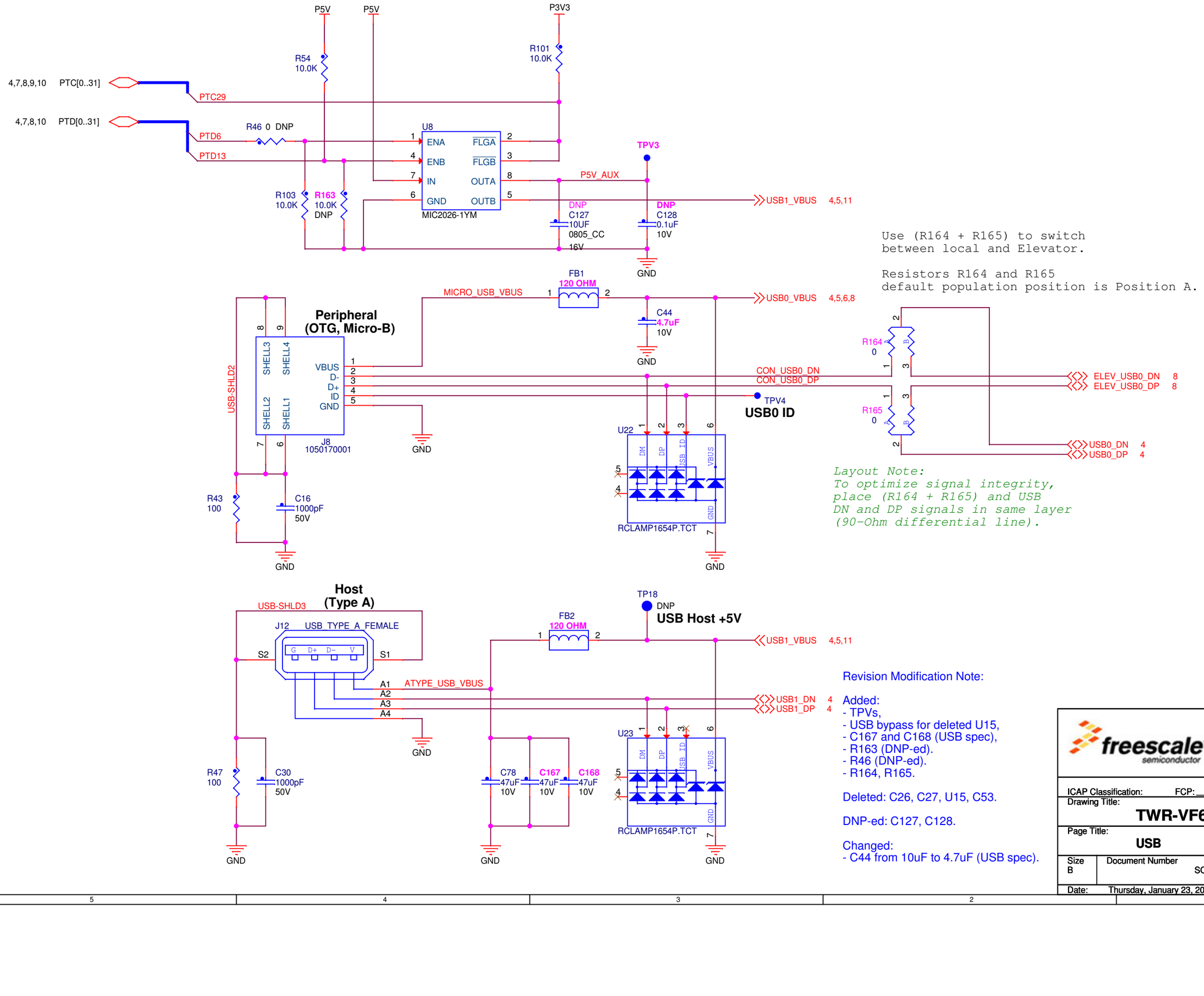
Deleted: DDR3 termination.

DNP-ed: R107.

Changed:
- C51 from 47uF to 10uF (BOM consolidation).

freescale semiconductor

| | | |
|---|---|---|
| ICAP Classification: | FCP: ___ FIUO: X PUBI: ___ | |
| Drawing Title: | **TWR-VF65GS10** | |
| Page Title: | **DDR3 & NAND Flash** | |
| Size: C | Document Number: SCH-27442 PDF: SPF-27442 | Rev: H |
| Date: Thursday, January 23, 2014 | Sheet 10 of 11 | |


P5V
P5V
P3V3
R54
10.0K
R101
10.0K
4,7,8,9,10 PTC[0..31]
PTC29
4,7,8,10 PTD[0..31]
PTD6
PTD13
R46 0 DNP
U8
ENA
ENB
IN
GND
FLGA
FLGB
OUTA
OUTB
MIC2026-1YM
TPV3
P5V_AUX
R103
10.0K
R163
10.0K
DNP
DNP
C127
10UF
0805_CC
16V
DNP
C128
0.1uF
10V
GND
USB1_VBUS 4,5,11
FB1
120 OHM
MICRO_USB_VBUS
USB0_VBUS 4,5,6,8
C44
4.7uF
10V
GND
Peripheral
(OTG, Micro-B)
USB-SHLD2
SHELL3
SHELL4
SHELL2
SHELL1
VBUS
D-
D+
ID
GND
J8
1050170001
GND
CON_USB0_DN
CON_USB0_DP
TPV4
USB0 ID
U22
DM
DP
USB_ID
VBUS
GND
RCLAMP1654P.TCT
GND
R164
0
R165
0
ELEV_USB0_DN 8
ELEV_USB0_DP 8
USB0_DN 4
USB0_DP 4
R43
100
C16
1000pF
50V
GND
Use (R164 + R165) to switch
between local and Elevator.
Resistors R164 and R165
default population position is Position A.
Layout Note:
To optimize signal integrity,
place (R164 + R165) and USB
DN and DP signals in same layer
(90-Ohm differential line).
Host
(Type A)
USB-SHLD3
J12 USB_TYPE_A_FEMALE
G D+ D- V
S1
S2
A1
A2
A3
A4
ATYPE_USB_VBUS
GND
TP18
DNP
USB Host +5V
FB2
120 OHM
USB1_VBUS 4,5,11
USB1_DN 4
USB1_DP 4
U23
DM
DP
USB_ID
VBUS
GND
RCLAMP1654P.TCT
GND
R47
100
C30
1000pF
50V
GND
C78
47uF
10V
C167
47uF
10V
C168
47uF
10V
GND
Revision Modification Note:
Added:
- TPVs,
- USB bypass for deleted U15,
- C167 and C168 (USB spec),
- R163 (DNP-ed).
- R46 (DNP-ed).
- R164, R165.
Deleted: C26, C27, U15, C53.
DNP-ed: C127, C128.
Changed:
- C44 from 10uF to 4.7uF (USB spec).
freescale semiconductor
ICAP Classification: FCP:___ FIUO: X PUBI:___
Drawing Title:
TWR-VF65GS10
Page Title:
USB
Size B
Document Number
SCH-27442 PDF: SPF-27442
Rev H
Date: Thursday, January 23, 2014
Sheet 11 of 11