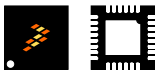
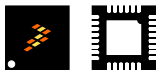
MKW36A/35A Data Sheet

An ultra low power, highly integrated Bluetooth® Low Energy wireless microcontroller

MKW36A512VHT4
MKW36A512VFP4
MKW35A512VFP4



48 LQFN
7x7 mm Pitch 0.5 mm



40 "Wettable" QFN
6x6 mm Pitch 0.5 mm

Multi-Standard Radio

- 2.4 GHz Bluetooth Low Energy version 5.0 compliant supporting up to 8 simultaneous hardware connections
- Generic FSK modulation
  - Data Rate: 250, 500 and 1000 kbps
  - Modulations: GFSK BT = 0.3, 0.5, and 0.7; FSK/MSK
  - Modulation Index: 0.32, 0.5, 0.7, and 1.0
- Typical Receiver Sensitivity (BLE 1 Mbps) = -95 dBm
- Typical Receiver Sensitivity (250 kbps GFSK-BT=0.5, h=0.5) = -99 dBm
- Programmable Transmitter Output Power: -30 dBm to +3.5 dBm
- Low external component counts for low cost application
- On-chip balun with single ended bidirectional RF port

MCU and Memories

- 256 KB program flash memory plus 256 KB FlexNVM on KW36A
- 8 KB FlexRAM supporting EEPROM emulation on KW36A
- 512 KB program flash memory on KW35A
- Up to 48 MHz ARM® Cortex-M0+ core
- On-chip 64 KB SRAM

Low Power Consumption

- Transceiver current (DC-DC buck mode, 3.6 V supply)
  - Typical Rx Current: 6.3 mA
  - Typical Tx current: 5.7 mA (0 dBm output)
- Low Power Mode (VLLS0) Current: 258 nA

System peripherals

- Nine MCU low-power modes to provide power optimization based on application requirements
- DC-DC Converter supporting Buck and Bypass operating modes
- Direct memory access (DMA) Controller
- Computer operating properly (COP) watchdog
- Serial wire debug (SWD) Interface and Micro Trace buffer
- Bit Manipulation Engine (BME)

Analog Modules

- 16-bit Analog-to-Digital Converter (ADC)
- 6-bit High Speed Analog Comparator (CMP)
- 1.2 V voltage reference (VREF)

Timers

- 16-bit low-power timer (LPTMR)
- 3 Timer/PWM Modules(TPM): One 4 channel TPM and two 2 channel TPMs
- Programmable Interrupt Timer (PIT)
- Real-Time Clock (RTC)

Communication interfaces

- 2 serial peripheral interface (SPI) modules
- 2 inter-integrated circuit (I2C) modules
- Low Power UART (LPUART) module with LIN support (2x LPUART on KW36A)
- Carrier Modulator Timer (CMT)
- FlexCAN module (with CAN FD support up to 3.2 Mbps baudrate) on KW36A

Preliminary

Clocks

- 26 and 32 MHz supported for BLE and Generic FSK modes
- 32.768 kHz Crystal Oscillator

Operating Characteristics

- Voltage range: 1.71 V to 3.6 V
- Ambient temperature range: –40 to 105 °C
- AEC Q100 Grade 2 Automotive Qualification

Human-machine interface

- General-purpose input/output

Security

- AES-128 Hardware Accelerator (AESA)
- True Random Number Generator (TRNG)
- Advanced flash security on Program Flash
- 80-bit unique identification number per chip
- 40-bit unique media access control (MAC) sub-address
- LE Secure Connections

Orderable parts details

Device	Qualification	CAN FD	2nd UART with LIN	FlexRAM	Package
MKW36A512VHT4	Auto	Y	Y	Y	7X7 mm 48-pin LQFN
MKW36A512VFP4	Auto	Y	Y	Y	6X6 mm 40-pin "Wettable" QFN
MKW35A512VFP4	Auto	N	N	N	6X6 mm 40-pin "Wettable" QFN

Related Resources

Type	Description
Product Selector	The Product Selector lets you find the right Kinetis part for your design.
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.
Package drawing	Package dimensions are provided in package drawings.

Table of Contents

1 Introduction

The KW36A/35A wireless microcontrollers (MCU), which includes the KW36A and KW35A families of devices, are highly integrated single-chip devices that enable Bluetooth Low Energy (BLE) and Generic FSK connectivity for automotive and industrial embedded systems. To meet the stringent requirements of automotive applications, the KW36A/35A is fully AEC Q100 Grade 2 Automotive Qualified. The target applications center on wirelessly bridging the embedded world with mobile devices to enhance the human interface experience, share embedded data between devices and the cloud and enable wireless firmware updates. Leading the automotive applications is the Digital Key, where a smartphone can be used by the owner as an alternative to the key FOB for unlocking and personalizing the driving experience. For a car sharing experience, the owner can provide selective, temporary authorization for access to the car allowing the authorized person to unlock, start and operate the car using their mobile device using BLE.

The KW36A/35A Wireless MCU integrates an Arm® Cortex-M0+ CPU with up to 512 KB flash and 64 KB SRAM and a 2.4 GHz radio that supports BLE 5.0 and Generic FSK modulations. The BLE radio supports up to 8 simultaneous connections in any master/slave combination. The Medical Body Area Network (MBAN) frequencies from 2.36 to 2.4 GHz are also supported enabling wearable or implantable wireless medical devices.

The KW36A includes an integrated FlexCAN module enabling seamless integration into a cars in-vehicle or industrial CAN communication network. The FlexCAN module can support CAN's flexible data-rate (CAN FD) protocol for increased bandwidth and lower latency required by many automotive applications.

The KW36A/35A devices can be used as a "BlackBox" modem in order to add BLE or Generic FSK connectivity to an existing host MCU or MPU (microprocessor), or may be used as a standalone smart wireless sensor with embedded application where no host controller is required.

The RF circuit of the KW36A/35A is optimized to require very few external components, achieving the smallest RF footprint possible on a printed circuit board. Extremely long battery life is achieved through the efficiency of code execution in the Cortex-M0+ CPU core and the multiple low power operating modes of the KW36A/35A. For power critical applications, an integrated DC-DC converter enables operation from a single coin cell or Li-ion battery with a significant reduction of peak receive and transmit current consumption.

2 Feature Descriptions

This section provides a simplified block diagram and highlights the KW36A/35A features.

2.1 Block Diagram

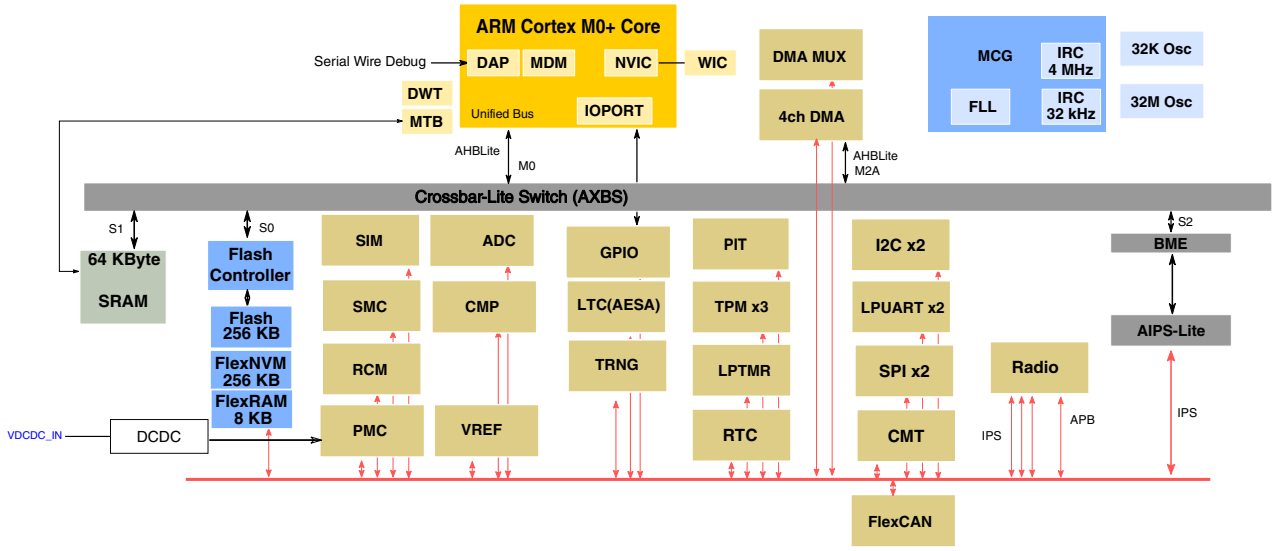


Figure 1. KW36 Detailed Block Diagram

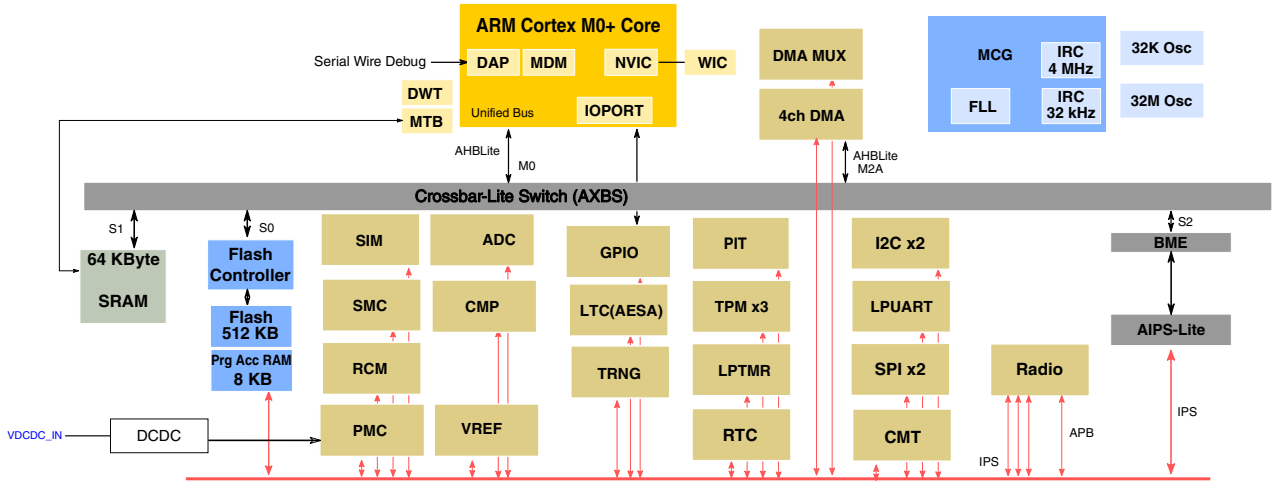


Figure 2. KW35 Detailed Block Diagram

2.2 Radio features

Operating frequencies:

- 2.4 GHz ISM band (2400-2483.5 MHz)
- Medical Body Area Network (MBAN) 2360-2400 MHz

Supported standards:

- Bluetooth Low Energy Version 5 compliant radio
- Generic FSK modulation supporting data rates up to 1 Mbps
- Support for up to 8 simultaneous BLE hardware connections in any master, slave combination
- Bluetooth Low Energy(BLE) Application Profiles

Receiver performance:

- Receive sensitivity of up to -95 dBm for BLE
- Receive sensitivity of up to -99 dBm for a 250 kbps GFSK mode with a modulation index of 0.5. Receive sensitivity in Generic FSK modes depends on mode selection and data rate.

Other features:

- Programmable transmit output power from -30 dBm to +3.5 dBm
- Integrated on-chip balun
- Single ended bidirectional RF port shared by transmit and receive
- Low external component count
- Supports transceiver range extension using external PA and/or LNA
- 26 MHz and 32 MHz crystals supported for BLE and Generic FSK modes
- Bluetooth Low Energy version 5 Link Layer hardware with 1 Mbps PHY support
- Hardware acceleration for Generic FSK packet processing
- Generic FSK modulation at 250, 500 and 1000 kbps
- Supports 8 simultaneous BLE connections in any master/slave combination
- Enhanced BLE automatic deep sleep modes (DSM) supporting Slave Latency
- Up to 26 devices supported by whitelist in hardware
- Up to 8 private resolvable addresses supported in hardware
- Supports DMA capture of IQ data with sampling rate of up to 2 MHz, when using a 32 MHz crystal

2.3 Microcontroller features

ARM Cortex-M0+ CPU

- Up to 48 MHz CPU
- As compared to Cortex-M0, the Cortex-M0+ uses an optimized 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Supports up to 32 interrupt request sources
- Binary compatible instruction set architecture with the Cortex-M0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial Wire Debug (SWD) reduces the number of pins required for debugging
- Micro Trace Buffer (MTB) provides lightweight program trace capabilities using system RAM as the destination memory

Nested Vectored Interrupt Controller (NVIC)

- 32 vectored interrupts, 4 programmable priority levels
- Includes a single non-maskable interrupt

Wake-up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low power modes
- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to very-deep-sleep
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a non-masked interrupt is detected

Debug Controller

- Two-wire Serial Wire Debug (SWD) interface
- Hardware breakpoint unit for 2 code addresses
- Hardware watchpoint unit for 2 data items
- Micro Trace Buffer for program tracing

On-Chip Memory

- Up to 512 KB Flash
  - KW36A contains 256 KB program flash with ECC and 256 KB FlexNVM.
  - KW35A contains 512 KB program flash with ECC.

    - Flash implemented as two equal blocks each of 256 KB block. Code can execute or read from one block while the other block is being erased or programmed on KW35A only.
    - Firmware distribution protection. Program flash can be marked execute-only on a per-sector (8 KB) basis to prevent firmware contents from being read by third parties.
- 64 KB SRAM
- KW36A contains 8 KB FlexRAM.
- KW35A contains 8 KB program acceleration RAM.
- Security circuitry to prevent unauthorized access to RAM and flash contents through the debugger

2.4 System features

Power Management Control Unit (PMC)

- Programmable power saving modes
- Available wake-up from power saving modes via internal and external sources
- Integrated Power-on Reset (POR)
- Integrated Low Voltage Detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Individual peripheral clocks can be gated off to reduce current consumption
- Internal Buffered bandgap reference voltage
- Factory programmed trim for bandgap and LVD
- 1 kHz Low Power Oscillator (LPO)

DC-DC Converters

- Internal switched mode power supply supporting Buck and Bypass operating modes
- Buck operation supports external voltage sources of 2.1 V to 3.6 V
- When DC-DC is not used, the device supports an external voltage range of 1.5 V to 3.6 V (1.5 - 3.6 V on VDD_RF1, VDD_RF2, VDD_XTAL and VDD_1P5OUT_PMCIN pins. 1.71 - 3.6 V on VDD_0, VDD_1 and VDDA pins)
- An external inductor is required to support the Buck mode
- The DC-DC Converter VDD_1P8OUT current drive for external devices (MCU in RUN mode, Radio is enabled, other peripherals are disabled)
    - Up to 44 mA in buck mode with VDD_1P8OUT = 1.8 V
    - Up to 31.4 mA in buck mode with VDD_1P8OUT = 3.0 V

Direct Memory Access (DMA) Controller

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses and transfer size
- Support for enhanced addressing modes
- 4-channel implementation that performs complex data transfers with minimal intervention from a host processor
- Internal data buffer, used as temporary storage to support 16- and 32-byte transfers
- Connections to the crossbar switch for bus mastering the data movement
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
- 32-byte TCD stored in local memory for each channel
- An inner data transfer loop defined by a minor byte transfer count
- An outer data transfer loop defined by a major iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests, one per channel
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- One interrupt per channel, optionally asserted at completion of major iteration count
- Optional error terminations per channel and logically summed together to form one error interrupt to the interrupt controller
- Optional support for scatter/gather DMA processing
- Support for complex data structures

DMA Channel Multiplexer (DMA MUX)

- 4 independently selectable DMA channel routers
- 2 periodic trigger sources available
- Each channel router can be assigned to 1 of the peripheral DMA sources

COP Watchdog Module

- Independent clock source input (independent from CPU/bus clock)
- Choice between two clock sources
  - LPO oscillator
  - Bus clock

System Clocks

- Both 26 MHz and 32 MHz crystal reference oscillator supported for BLE and Generic FSK modes
- MCU can derive its clock either from the crystal reference oscillator or the frequency locked loop (FLL)[1]
- 32.768 kHz crystal reference oscillator used to maintain precise Bluetooth Low Energy timing in low power modes
- Multipurpose Clock Generator (MCG)
- Internal reference clocks — Can be used as a clock source for other on-chip peripherals
  - On-chip RC oscillator range of 31.25 kHz to 39.0625 kHz with 2% accuracy across full temperature range
  - On-chip 4MHz oscillator with 5% accuracy across full temperature range
- Frequency-locked loop (FLL) controlled by internal or external reference
  - 20 MHz to 48 MHz FLL output

Unique Identifiers

- 80-bit Unique ID represents a unique identifier for each chip
- 40-bit unique Media Access Control (MAC) address, which can be used to build a unique 48-bit Bluetooth Low Energy MAC address

2.5 Peripheral features

16-bit Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with 16-bit resolution
- Output formatted in differential-ended 16-, 13-, 11-, and 9-bit mode
- Output formatted in single-ended 16-, 12-, 10-, and 8-bit mode
- Single or continuous conversion
- Configurable sample time and conversion speed / power
- Conversion rates in 16-bit mode with no averaging up to ~500Ksamples/sec
- Input clock selection
- Operation in low power modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for less-than, or greater than, or equal to programmable value
- Temperature sensor

1. Clock options can have restrictions based on the chosen SoC configuration.

- Battery voltage measurement
- Hardware average function
- Selectable voltage reverence
- Self-calibration mode

High-Speed Analog Comparator (CMP)

- 6-bit DAC programmable reference generator output
- Up to eight selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Two performance modes:
  - Shorter propagation delay at the expense of higher power
  - Low power, with longer propagation delay
- Operational in all MCU power modes except VLLS0 mode

Voltage Reference(VREF1)

- Programmable trim register with 0.5 mV steps, automatically loaded with factory trimmed value upon reset
- Programmable buffer mode selection:
  - Off
  - Bandgap enabled/standby (output buffer disabled)
  - High power buffer mode (output buffer enabled)
- 1.2 V output at room temperature
- VREF_OUT output signal

Low Power Timer (LPTMR)

- One channel
- Operation as timer or pulse counter
- Selectable clock for prescaler/glitch filter
  - 1 kHz internal LPO
  - External low power crystal oscillator
  - Internal reference clock
- Configurable glitch filter or prescaler
- Interrupt generated on timer compare
- Hardware trigger generated on timer compare
- Functional in all power modes

Timer/PWM (TPM)

- TPM0: 4 channels, TPM1 and TPM2: 2 channels each
- Selectable source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Generation of hardware triggers
- TPM1 and TPM2: Quadrature decoder with input filters
- Global time base mode shares single time base across multiple TPM instances

Programmable Interrupt Timer (PIT)

- Up to 2 interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by bus clock frequency

Real-Time Clock (RTC)

- 32-bit seconds counter with 32-bit alarm
  - Can be invalidated on detection of tamper detect
- 16-bit prescaler with compensation
- Register write protection
  - Hard Lock requires MCU POR to enable write access
  - Soft lock requires POR or software reset to enable write/read access
- Capable of waking up the system from low power modes

Inter-Integrated Circuit (I^2C)

- Two channels
- Compatible with I2C bus standard and SMBus Specification Version 2 features
- Up to 400 kHz operation
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low power mode

LPUART

- One channel (2 channels on KW36A)
- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Programmable 1 or 2 stop bits
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Address match feature in receiver to reduce address mark wakeup ISR overhead
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking
- Configurable oversampling ratio to support from 1/4 to 1/32 bit-time noise detection
- Operation in low power modes
- Hardware Flow Control RTS\CTS
- Functional in Stop/VLPS modes
- Break detect supporting LIN

Serial Peripheral Interface (SPI)

- Two independent SPI channels
- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Support for both transmit and receive by DMA

Carrier Modulator Timer (CMT)

- Four modes of operation
  - Time; with independent control of high and low times

    - Baseband
    - Frequency shift key (FSK)
    - Direct software control of CMT_IRO signal
- Extended space operation in time, baseband, and FSK modes
- Selectable input clock divider
- Interrupt on end of cycle
- Ability to disable CMT_IRO signal and use as timer interrupt

General Purpose Input/Output (GPIO)

- Hysteresis and configurable pull up device on all input pins
- Independent pin value register to read logic level on digital pin
- All GPIO pins can generate IRQ and wakeup events
- Configurable drive strength on some output pins
- GPIO can be configured to function as a interrupt driven keyboard scanning matrix
    - In the 48-pin package there are a total of 25 digital pins
    - In the 40-pin package there are a total of 18 digital pins

FlexCAN (for KW36A only)

- Full implementation of the CAN with Flexible Data Rate (CAN FD) protocol specification and CAN protocol specification, Version 2.0 B
- Flexible Message Buffers (MBs); there are total 32 MBs of 8 bytes data length each, configurable as Rx or Tx, all supporting standard and extended messages
- Programmable clock source to the CAN Protocol Interface, either peripheral clock or oscillator clock
- Capability to select priority between mailboxes and Rx FIFO during matching process
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 individual masking capability

2.6 Security Features

Advanced Encryption Standard Accelerator(AES-128 Accelerator)

The advanced encryption standard accelerator (AESA) module is a standalone hardware coprocessor capable of accelerating the 128-bit advanced encryption standard (AES) cryptographic algorithms.

The AESA engine supports the following cryptographic features.

LTC includes the following features:

- Cryptographic authentication
  - Message authentication codes (MAC)
    - Cipher-based MAC (AES-CMAC)
    - Extended cipher block chaining message authentication code (AES-XCBC-MAC)
  - Auto padding
  - Integrity Check Value(ICV) checking
- Authenticated encryption algorithms
  - Counter with CBC-MAC (AES-CCM)
  - Galois counter mode (AES-GCM)
- Symmetric key block ciphers
  - AES (128-bit keys)
  - Cipher modes:
    - AES-128 modes
      - Electronic codebook (ECB)
      - Cipher block chaining (CBC)
      - Counter (CTR)
    - DES modes
      - Electronic codebook (ECB)
      - Cipher block chaining (CBC)
      - Cipher feedback (CFB)
      - Output Feedback (OFB)
- Secure scan

True Random Number Generator (TRNG)

True Random Number Generator (TRNG) is a hardware accelerator module that constitutes a high-quality entropy source.

- TRNG generates a 512-bit (4x 128-bit) entropy as needed by an entropy-consuming module, such as a deterministic random number generator.
- TRNG output can be read and used by a deterministic pseudo-random number generator (PRNG) implemented in software.
- TRNG-PRNG combination achieves NIST compliant true randomness and cryptographic-strength random numbers using the TRNG output as the entropy source.
- A fully FIPS 180 compliant solution can be realized using the TRNG together with a FIPS compliant deterministic random number generator and the SoC-level security.

Flash Memory Protection

The on-chip flash memory controller enables the following useful features:

- Program flash protection scheme prevents accidental program or erase of stored data.
- Program flash access control scheme prevents unauthorized access to selected code segments.
- Automated, built-in, program and erase algorithms with verify.
- Read access to one program flash block is possible while programming or erasing data in the other program flash block.

3 Transceiver Description

- Direct Conversion Receiver (Zero IF)
- Constant Envelope Transmitter
- 2.36 GHz to 2.483 GHz PLL Range
- Low Transmit and Receive Current Consumption
- Low BOM

3.1 Key Specifications

KW36A/35A meets or exceeds all Bluetooth Low Energy version 5 performance specifications. The key specification for the KW36A/35A are:

Frequency Band:

- ISM Band: 2400 to 2483.5MHz
- MBAN Band: 2360 to 2400MHz

Bluetooth Low Energy version 5 modulation scheme:

- Symbol rate: 1000 kbps
- Modulation: GFSK
- Receiver sensitivity: -95 dBm, typical
- Programmable transmitter output power: -30 dBm to +3.5 dBm

Generic FSK modulation scheme:

- Symbol rate: 250, 500 and 1000 kbps

- Modulation(s): GFSK (modulation index = 0.32, 0.5, 0.7 and 1.0, BT =0.3, 0.5, and 0.7), FSK and MSK
- Receiver Sensitivity: Mode and data rate dependent. -99 dBm typical for GFSK (r=250 kbps, BT = 0.5, h = 0.5)

3.2 Channel Map Frequency Plans

3.2.1 Channel Plan for Bluetooth Low Energy

This section describes the frequency plan / channels associated with 2.4GHz ISM and MBAN bands for Bluetooth Low Energy.

2.4 GHz ISM Channel numbering:

- Fc=2402 + k * 2 MHz, k=0,.....,39.

MBAN Channel numbering:

- Fc=2360 + k in MHz, for k=0,.....,39

where k is the channel number.

Table 1. 2.4 GHz ISM and MBAN frequency plan and channel designations

2.4 GHz ISM[1]		MBAN[2]		2.4GHz ISM + MBAN	
Channel	Freq (MHz)	Channel	Freq (MHz)	Channel	Freq (MHz)
0	2402	0	2360	28	2390
1	2404	1	2361	29	2391
2	2406	2	2362	30	2392
3	2408	3	2363	31	2393
4	2410	4	2364	32	2394
5	2412	5	2365	33	2395
6	2414	6	2366	34	2396
7	2416	7	2367	35	2397
8	2418	8	2368	36	2398
9	2420	9	2369	0	2402
10	2422	10	2370	1	2404
11	2424	11	2371	2	2406
12	2426	12	2372	3	2408

Table continues on the next page...

Table 1. 2.4 GHz ISM and MBAN frequency plan and channel designations (continued)

2.4 GHz ISM[1]		MBAN[2]		2.4GHz ISM + MBAN	
Channel	Freq (MHz)	Channel	Freq (MHz)	Channel	Freq (MHz)
13	2428	13	2373	4	2410
14	2430	14	2374	5	2412
15	2432	15	2375	6	2414
16	2434	16	2376	7	2416
17	2436	17	2377	8	2418
18	2438	18	2378	9	2420
19	2440	19	2379	10	2422
20	2442	20	2380	11	2424
21	2444	21	2381	12	2426
22	2446	22	2382	13	2428
23	2448	23	2383	14	2430
24	2450	24	2384	15	2432
25	2452	25	2385	16	2434
26	2454	26	2386	17	2436
27	2456	27	2387	18	2438
28	2458	28	2388	19	2440
29	2460	29	2389	20	2442
30	2462	30	2390	21	2444
31	2464	31	2391	22	2446
32	2466	32	2392	23	2448
33	2468	33	2393	24	2450
34	2470	34	2394	25	2452
35	2472	35	2395	26	2454
36	2474	36	2396	27	2456
37	2476	37	2397	37	2476
38	2478	38	2398	38	2478
39	2480	39	2399	39	2480

1. ISM frequency of operation spans from 2400.0 MHz to 2483.5 MHz
2. Per FCC guideline rules, Bluetooth Low Energy single mode operation is allowed in these channels.

3.2.2 Other Channel Plans

The RF synthesizer can be configured to use any channel frequency between 2.36 and 2.487 GHz.

3.3 Transceiver Functions

Receive

The receiver architecture is Zero IF (ZIF) where the received signal after passing through RF front end is down-converted to a baseband signal. The signal is filtered and amplified before it is fed to analog-to-digital converter. The digital signal is then decimated to a baseband clock frequency before it is digitally processed, demodulated and passed on to packet processing/link-layer processing.

Transmit

The transmitter transmits GFSK/FSK modulation having power and channel selection adjustment per user application. After the channel of operation is determined, coarse and fine tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission.

4 Transceiver Electrical Characteristics

4.1 Radio operating conditions

Table 2. Radio operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Input Frequency	f_{in}	2.360	—	2.480	GHz
Ambient Temperature Range	T_A	-40	25	105	°C
Logic Input Voltage Low	V_{IL}	0	—	30% VDD_{INT} [1]	V
Logic Input Voltage High	V_{IH}	70% VDD_{INT}	—	VDD_{INT}	V
SPI Clock Rate	f_{SPI}	—	—	12.0	MHz
Maximum RF Input Power	P_{max}	—	—	10	dBm
Crystal Reference Oscillator Frequency [2]	f_{ref}	26 MHz or 32 MHz			

1. VDD_{INT} is the internal LDO regulated voltage supplying various circuit blocks, VDD_{INT}=1.2 V
2. The recommended crystal accuracy is ±40 ppm including initial accuracy, mechanical, temperature and aging factors.

4.2 Receiver Feature Summary

Table 3. Top Level Receiver Specifications (TA=25°C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current power down on VDD_RFx supplies	I_{pdn}	—	200	1000	nA
Supply current Rx On with DC-DC converter enable (Buck; V_{DCDC_IN} = 3.6 V) [2]	I_{Rxon}	—	6.3	—	mA
Supply current Rx On with DC-DC converter disabled (Bypass) [2]	I_{Rxon}	—	17.2	—	mA
Input RF Frequency	f_{in}	2.360	—	2.4835	GHz
GFSK Rx Sensitivity(250 kbps GFSK-BT=0.5, h=0.5)	$SENS_{GFSK}$	—	-99	—	dBm
BLE Rx Sensitivity [3]	$SENS_{BLE}$	—	-95	—	dBm
Noise Figure for maximum gain mode @ typical sensitivity	NF_{HG}	—	7.5	—	dB
Receiver Signal Strength Indicator Range[4]	$RSSI_{Range}$	-100	—	5[5]	dBm
Receiver Signal Strength Indicator Resolution	$RSSI_{Res}$	—	1	—	dB
Typical RSSI variation over frequency		-2	—	2	dB
Typical RSSI variation over temperature		-2	—	2	dB
Narrowband RSSI accuracy[6]	$RSSI_{Acc}$	-3	—	3	dB
BLE Co-channel Interference (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz).			-7		dB
Adjacent/Alternate Channel Performance[7]					
BLE Adjacent +/- 1 MHz Interference offset (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz.)	$SEL_{BLE,\ 1\ MHz}$	—	2	—	dB
BLE Adjacent +/- 2 MHz Interference offset (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz.)	$SEL_{BLE,\ 2\ MHz}$	—	43	—	dB
BLE Alternate +/-3 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.)	$SEL_{BLE,\ 3\ MHz}$	—	50	—	dB
BLE Alternate ≥ +/-4 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.)	$SEL_{BLE,\ 4+\ MHz}$	—	50	—	dB
Intermodulation Performance					
BLE Intermodulation with continuous wave interferer at ± 3MHz and modulated interferer is at ± 6MHz (Wanted signal at -67 dBm , BER<0.1%.)		—	-23	—	dBm
BLE Intermodulation with continuous wave interferer at ±5MHz and modulated interferer is at ±10MHz (Wanted signal at -67 dBm , BER<0.1%.)		—	-24	—	dBm
Blocking Performance					

Table continues on the next page...

Table 3. Top Level Receiver Specifications (TA=25°C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
BLE Out of band blocking from 30 MHz to 1000 MHz and 4000 MHz to 5000 MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)[8]	—	-2	—	—	dBm
BLE Out of band blocking from 1000 MHz to 2000 MHz and 3000 MHz to 4000MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)	—	-8.4	—	—	dBm
BLE Out of band blocking from 2001 MHz to 2339MHz and 2484 MHz to 2999 MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)[9]	—	-17	—	—	dBm
BLE Out of band blocking from 5000 MHz to 12750 MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)[9]	—	—	10	—	dBm
Spurious Emission < 1.6 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc|< 1.6 MHz	—	—	-54	—	dBc
Spurious Emission > 2.5 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc|> 2.5 MHz[10]	—	—	-70	—	dBc

1. All the RX parameters are measured at the KW36A/35A RF pins.
2. Transceiver power consumption.
3. Measured at 0.1% BER using 37 byte long packets in maximum gain mode and nominal conditions.
4. Narrow-band RSSI mode.
5. With RSSI_CTRL_0.RSSI_ADJ field calibrated to account for antenna to RF input losses.
6. With one point calibration over frequency and temperature.
7. BLE adjacent and alternate selectivity performance is measured with modulated interference signals.
8. Exceptions allowed for carrier frequency sub harmonics.
9. Exceptions allowed for carrier frequency harmonics.
10. Exceptions allowed for twice the reference clock frequency(fref) multiples.

Table 4. Receiver Specifications with Generic FSK Modulations

				Adjacent/Alternate Channel Selectivity (dB)[1]					
Modulation Type	Data Rate (kbps)	Channel BW (kHz)	Typical Sensitivity (dBm)	Desired signal level (dBm)	Interferer at -/+1* channel BW offset	Interferer at -/+ 2* channel BW offset	Interferer at -/+ 3* channel BW offset	Interferer at -/+ 4* channel BW offset	Co-channel
GFSK BT = 0.5, h=0.5	1000	2000	-95	-67	43	50	55	50	-7
	500	1000	-97	-85	40	50	55	55	-7
	250	500	-99	-85	30	40	50	50	-7
GFSK, BT = 0.5, h=0.3	1000	1000	-89	-67	10	38	42	47	-10
	500	800	-92	-85	22	31	37	42	-10

Table continues on the next page...

Table 4. Receiver Specifications with Generic FSK Modulations (continued)

				Adjacent/Alternate Channel Selectivity (dB)[1]					
Modulation Type	Data Rate (kbps)	Channel BW (kHz)	Typical Sensitivity (dBm)	Desired signal level (dBm)	Interferer at -/+1* channel BW offset	Interferer at -/+ 2* channel BW offset	Interferer at -/+ 3* channel BW offset	Interferer at -/+ 4* channel BW offset	Co-channel
	250	500	-93	-85	20	25	30	34	-13
GFSK, BT = 0.5, h=0.7	1000	2000	-97	-85	45	50	57	60	-7
	500	1000	-98	-85	40	50	55	55	-7
	250	600	-99	-85	30	40	50	50	-7
GMSK BT=0.3	1000	1600	-91	-85	40	46	53	55	-8
	500	800	-93	-85	35	46	50	53	-7
	250	500	-95	-85	30	40	40	50	-7
GMSK, BT = 0.7	1000	2000	-96	-85	44	53	57	60	-7
	500	1000	-97	-85	40	50	55	55	-7
	250	600	-99	-85	30	40	50	50	-7
Generic MSK	1000	3000	-96	-85	43	53	60	63	-7
	500	1600	-97	-85	43	50	60	60	-8
	250	800	-99	-85	35	45	55	55	-7
GFSK BT=0.5, h=1	1000	3000	-96	-85	45	55	55	59	-8
	500	1400	-97	-85	40	45	50	50	-8
	250	800	-98	-85	35	45	45	50	-8

1. Selectivity measured with an unmodulated blocker except for GFSK BT=0.5, h=0.5 1mbps and GFSK BT=0.5, h=0.32 1mbps. The desired signal is set at -85 dBm.

4.3 Transmit and PLL Feature Summary

- Supports constant envelope modulation of 2.4 GHz ISM and 2.36 GHz MBAN frequency bands
- Fast PLL Lock time: < 25 µs
- Reference Frequency:
  - 26 MHz and 32 MHz crystals supported for BLE and Generic FSK modes

Table 5. Top level Transmitter Specifications (TA=25°C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current power down on VDD_RFx supplies	I_{pdn}	—	200	—	nA

Table continues on the next page...

Table 5. Top level Transmitter Specifications (TA=25°C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current Tx On with P_{RF} = 0dBm and DC-DC converter enabled (Buck; VDD_{DCDC_in} = 3.6 V) [2]	I_{Txone}	—	5.7	—	mA
Supply current Tx On with P_{RF} = 0 dBm and DC-DC converter disabled (Bypass) [2]	I_{Txond}	—	16	—	mA
Output Frequency	f_{in}	2.360	—	2.4835	GHz
Maximum RF Output power [3]	$P_{RF,max}$	—	+3.5	—	dBm
Minimum RF Output power [3]	$P_{RF,min}$	—	-30	—	dBm
RF Output power control range	P_{RFCR}	—	34	—	dB
BLE TX Output Spectrum 20dB BW	$TXBW_{BLE}$	1.0		—	MHz
BLE average frequency deviation using a 00001111 modulation sequence	$\Delta f1_{avg,BLE}$		250		kHz
BLE average frequency deviation using a 01010101 modulation sequence	$\Delta f2_{avg,BLE}$		220		kHz
BLE RMS FSK Error	$FSK_{err,BLE}$		3%		
BLE Maximum Deviation of the Center Frequency[4]	$F_{cdev,BLE}$	—	±3	—	kHz
BLE Adjacent Channel Transmit Power at 2MHz offset[5]	$P_{RF2MHz,BLE}$	—	—	-55	dBm
BLE Adjacent Channel Transmit Power at >= 3MHz offset[5]	$P_{RF3MHz,BLE}$	—	—	-59	dBm
BLE Frequency Hopping Support			YES		
2nd Harmonic of Transmit Carrier Frequency (P_{out} = $P_{RF,max}$), [6]	TXH2	—	-46	—	dBm/MHz
3rd Harmonic of Transmit Carrier Frequency (P_{out} = $P_{RF,max}$)[6]	TXH3	—	-58	—	dBm/MHz

1. All the TX parameters are measured at test hardware SMA connector.
2. Transceiver power consumption.
3. Measured at the KW36A/35A RF pins.
4. Maximum drift of carrier frequency of the PLL during a BLE packet with a nominal 32MHz reference crystal.
5. Measured at P_{out} = 5dBm and recommended TX match.
6. Harmonic levels based on recommended 2 component match. Transmit harmonic levels depend on the quality of matching components. Additional harmonic margin using a 3rd matching component (1x shunt capacitor) is possible.

Transmit PA driver output as a function of the PA_POWER[5:0] field when measured at the IC pins is as follows:

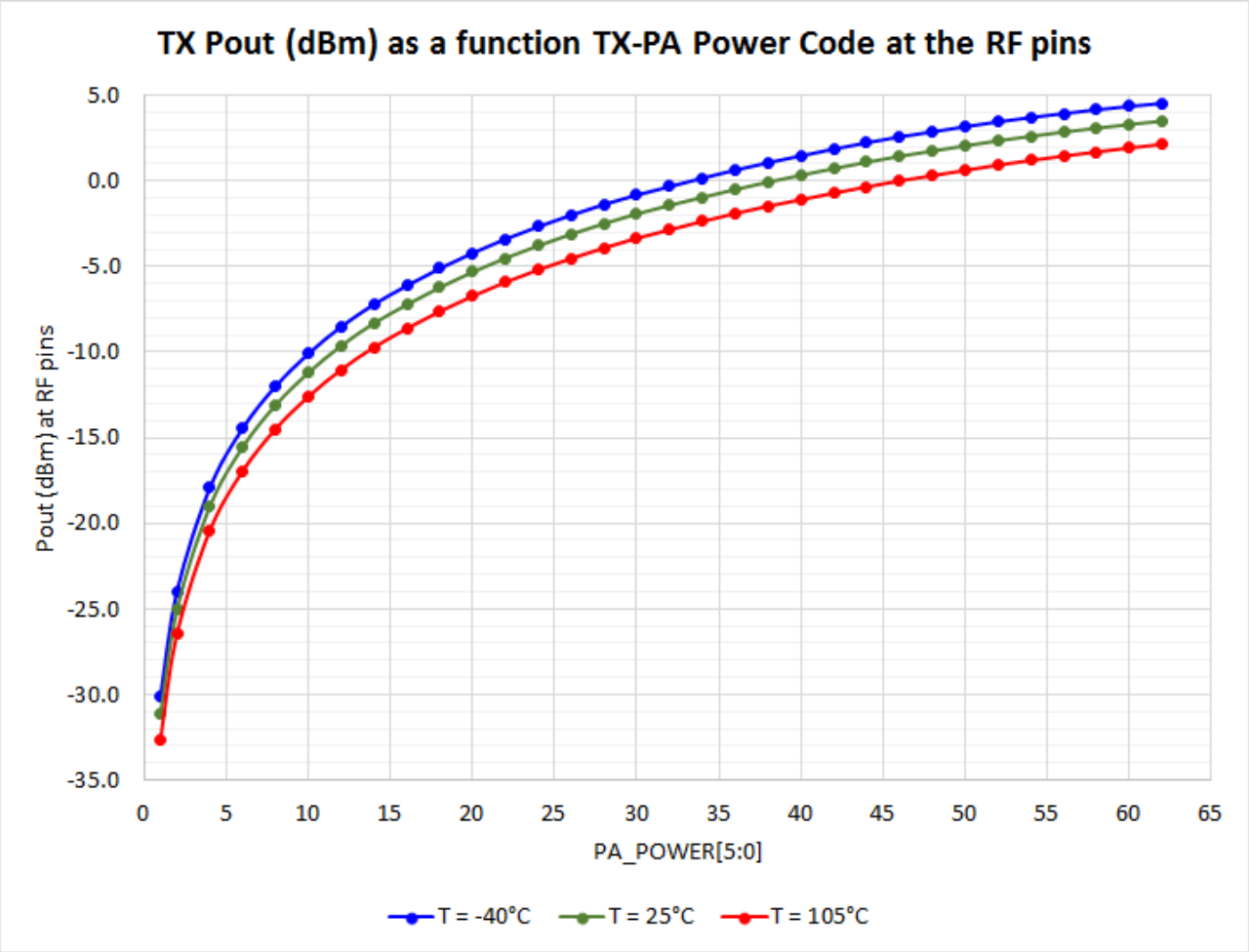


Table 6. Transmit Output Power as a function of PA_POWER[5:0]

	TX Pout (dBm)		
PA_POWER[5:0]	T = -40 °C	T = 25 °C	T = 105 °C
1	-30.1	-31.1	-32.6
2	-24.0	-25.0	-26.4
4	-17.9	-19.0	-20.4
6	-14.5	-15.6	-17.0
8	-12.0	-13.1	-14.5
10	-10.1	-11.2	-12.6
12	-8.5	-9.6	-11.0
14	-7.2	-8.3	-9.7
16	-6.1	-7.2	-8.6

Table continues on the next page...

Table 6. Transmit Output Power as a function of PA_POWER[5:0] (continued)

	TX Pout (dBm)		
PA_POWER[5:0]	T = -40 °C	T = 25 °C	T = 105 °C
18	-5.1	-6.2	-7.6
20	-4.2	-5.3	-6.7
22	-3.4	-4.5	-5.9
24	-2.7	-3.8	-5.2
26	-2.0	-3.1	-4.5
28	-1.4	-2.5	-3.9
30	-0.8	-1.9	-3.3
32	-0.3	-1.4	-2.8
34	0.2	-1.0	-2.4
36	0.6	-0.5	-1.9
38	1.1	-0.1	-1.5
40	1.5	0.3	-1.1
42	1.9	0.7	-0.7
44	2.2	1.1	-0.3
46	2.6	1.4	0.0
48	2.9	1.8	0.3
50	3.2	2.1	0.6
52	3.5	2.4	0.9
54	3.7	2.6	1.2
56	3.9	2.9	1.5
58	4.2	3.1	1.7
60	4.4	3.3	1.9
62	4.5	3.5	2.1

5 System and Power Management

5.1 Power Management

The KW36A/35A includes internal power management features that can be used to control the power usage. The power management of the KW36A/35A includes power management controller (PMC) and a DC-DC converter which can operate in a buck or bypass configuration. The PMC is designed such that the RF radio will remain in

state-retention while the core is in various stop modes. It can make sure the device can stay in low current consumption mode while the RF radio can wakeup quick enough for communication.

5.1.1 DC-DC Converter

The features of the DC-DC converter include the following:

- Single inductor, multiple outputs.
- Buck mode (pin selectable; CFG=VDCDC_IN).
- Continuous or pulsed operation (hardware/software configurable).
- Power switch input to allow external control of power up, and to select DCDC bypass mode in which all the SoC power supplies (see Table 3) are externally provided.
- Output signal to indicate power stable. Purpose is for the rest of the chip to be used as a POR.
- Scaled battery output voltage suitable for SAR ADC utilization.
- Internal oscillator for support when the reference oscillator is not present.
- VDD_1P8OUT is capable of supplying the external device a maximum of 20.9 mA (VDD_1P8OUT = 3.0 V, VDCDC_IN = 3.0 V), with MCU in RUN mode, peripherals are disabled.

5.2 Modes of Operation

The ARM Cortex-M0+ core in the KW36A/35A has three primary modes of operation: Run, Wait, and Stop modes. For each run mode, there is a corresponding wait and stop mode. Wait modes are similar to ARM sleep modes. Stop modes are similar to ARM deep sleep modes. The very low power run (VLPR) operation mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The WFI instruction invokes both wait and stop modes. The primary modes are augmented in a number of ways to provide lower power based on application needs.

5.2.1 Power modes

The power management controller (PMC) provides multiple power options to allow the user to optimize power consumption for the level of functionality needed.

Depending on the stop requirements of the user application, a variety of stop modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. The following table compares the various power modes available.

For each run mode there is a corresponding wait and stop mode. Wait modes are similar to ARM sleep modes. Stop modes (VLPS, STOP) are similar to ARM sleep deep mode. The very low power run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The three primary modes of operation are run, wait and stop. The WFI instruction invokes either wait or stop depending on the SLEEPDEEP bit in Cortex-M0+ System Control Register. The primary modes are augmented in a number of ways to provide lower power based on application needs.

Table 7. Power modes (At 25 deg C)

Power mode	Description	CPU recovery method	Radio
Normal Run (all peripherals clock off)	Allows maximum performance of chip.	—	Radio can be active
Normal Wait - via WFI	Allows peripherals to function, while allowing CPU to go to sleep reducing power.	Interrupt	
Normal Stop - via WFI	Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection.	Interrupt	
PStop2 (Partial Stop 2)	Core and system clocks are gated. Bus clock remains active. Masters and slaves clocked by bus clock remain in Run or VLPRun mode. The clock generators in MCG and the on-chip regulator in the PMC also remain in Run or VLPRun mode.	Interrupt	
PStop1 (Partial Stop 1)	Core, system clocks and bus clock are gated. All bus masters and slaves enter Stop mode. The clock generators in MCG and the on-chip regulator in the PMC also remain in Run or VLPRun mode.	Interrupt	
VLPR (Very Low Power Run) (all peripherals off)	Reduced frequency (1MHz) Flash access mode, regulator in low power mode, LVD off. Internal oscillator can provide low power 4 MHz source for core. (Values @2MHz core/ 1MHz bus and flash, module off, execution from flash). Biasing is disabled when DC-DC is configured for continuous mode in VLPR/W	—	Radio operation is possible only when DC-DC is configured for continuous mode.[1] However, there may be insufficient MIPS with a 4MHz MCU to support much in the way of radio operation.
VLPW (Very Low Power Wait) - via WFI (all peripherals off)	Similar to VLPR, with CPU in sleep to further reduce power. (Values @4MHz core/ 1MHz bus, module off)	Interrupt	

Table continues on the next page...

Table 7. Power modes (At 25 deg C) (continued)

Power mode	Description	CPU recovery method	Radio
	Biasing is disabled when DC-DC is configured for continuous mode in VLPR/W		
VLPS (Very Low Power Stop) via WFI	Places MCU in static state with LVD operation off. Lowest power mode with ADC and all pin interrupts functional. LPTMR, RTC, CMP can be operational. Biasing is disabled when DC-DC is configured for continuous mode in VLPS.	Interrupt	
LLS3 (Low Leakage Stop)	State retention power mode. LLWU, LPTMR, RTC, CMP can be operational. All of the radio Sea of Gates(SOG) logic is in state retention.	Wakeup Interrupt	Radio SOG is in state retention in LLSx. The BLE/ Generic FSK DSM[2] logic can be active using the 32 kHz clock
LLS2 (Low Leakage Stop)	State retention power mode. LLWU, LPTMR, RTC, CMP can be operational. 16 KB or 32 KB of programmable RAM can be powered on. All of the radio SOG logic is in state retention.	Wakeup Interrupt	
VLLS3 (Very Low Leakage Stop3)	Full SRAM retention. LLWU, LPTMR, RTC, CMP can be operational. All of the radio SOG logic is in state retention.	Wakeup Reset	Radio SOG is in state retention in VLLS3/2. The BLE/Generic FSK DSM logic can be active using the 32 kHz clock.
VLLS2 (Very Low Leakage Stop2)	Partial SRAM retention. 16 KB or 32 KB of programmable RAM can be powered on. LLWU, LPTMR, RTC, CMP can be operational. All of the radio SOG logic is in state retention.	Wakeup Reset	
VLLS1 (Very Low Leakage Stop1) with RTC + 32 kHz OSC	All SRAM powered off. The 32-byte system register file remains powered for customer-critical data. LLWU, LPTMR, RTC, CMP can be operational. Radio logic is power gated.	Wakeup Reset	Radio operation not supported. The Radio SOG is power-gated in VLLS1. Radio state is lost at VLLS1 and lower power states.
VLLS1 (Very Low Leakage Stop1) with LPTMR + LPO	All SRAM powered off. The 32-byte system register file remains powered for customer-critical data. LLWU, LPTMR, RTC, CMP can be operational.	Wakeup Reset	
VLLS0 (Very Low Leakage Stop0) with Brown-out Detection	VLLS0 is not supported with DC-DC The 32-byte system register file remains powered for customer-critical data. Disable all analog modules in PMC and retains I/O state and DGO state. LPO disabled, POR brown-out detection enabled, Pin interrupt only. Radio logic is power gated.	Wakeup Reset	Radio operation not supported. The Radio digital is power-gated in VLLS0.
VLLS0 (Very Low Leakage Stop0) without Brown-out Detection	VLLS0 is not supported with DC-DC buck configuration but is supported with bypass configuration The 32-byte system register file remains powered for customer-critical data. Disable all analog modules in PMC and retains I/O state and DGO state. LPO disabled, POR brown-out detection disabled, Pin interrupt only. Radio logic is power gated.	Wakeup Reset	

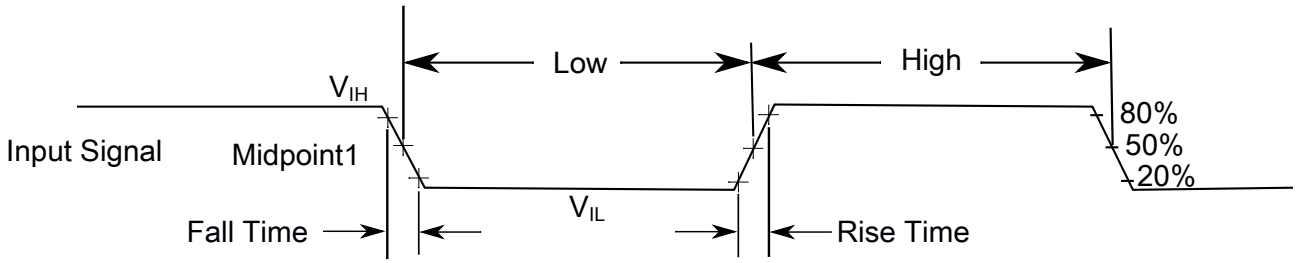
1. Biasing is disabled, but the Flash is in a low power mode for VLPx, so this configuration can realize some power savings over use of Run/Wait/Stop.

2. DSM refers to Radio's deep sleep mode. DSM does not refer to the ARM sleep deep mode.

6 KW36A/35A Electrical Characteristics

6.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 3. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Slew rate disabled
- Normal drive strength

6.2 Nonswitching electrical specifications

6.2.1 Voltage and current operating requirements

Table 8. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	

Table continues on the next page...

Table 8. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|.
2. Open drain outputs must be pulled to V_{DD}.

6.2.2 LVD and POR operating requirements

Table 9. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	

Table continues on the next page...

Table 9. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

6.2.3 Voltage and current operating behaviors

Table 10. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad (except RESET_b)				1, 2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -2.5 mA	V_{DD} – 0.5	—	V	
V_{OH}	Output high voltage — High drive pad (except RESET_b)				1, 2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	—	0.5	V	
V_{OL}	Output low voltage — High drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	500	nA	3

Table continues on the next page...

Table 10. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	3
I_{IN}	Input leakage current (total all pins) for full temperature range	—	5	µA	3
R_{PU}	Internal pullup resistors	20	50	kΩ	4

1. PTB0-1 and PTC0-3, PTC6, PTC7, PTC17, PTC18 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull-up device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at V_{DD} = 3.6 V.
4. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{SS}.

6.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLSx→RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Table 11. Power mode transition operating behaviors

Symbol	Description	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	300	µs	1
	• VLLS0 → RUN	169.0	µs	
	• VLLS1 → RUN	168.9	µs	
	• VLLS2 → RUN	97.3	µs	
	• VLLS3 → RUN	97.3	µs	
	• LLS → RUN	6.3	µs	

Table continues on the next page...

Table 11. Power mode transition operating behaviors (continued)

Symbol	Description	Max.	Unit	Notes
	• VLPS → RUN	6.2	µs	
	• STOP → RUN	6.2	µs	

1. Normal boot (FTFA_FOPT[LPBOOT]=11). When the DC-DC converter is in bypass mode, TPOR will not meet the 300µs spec when 1) VDD_1P5 < 1.6V at 25°C and 125°C. 2) 1.5V ≤ VDD_1P5 ≤ 1.8V. For the bypass mode special case where VDD_1P5 = VDD_1P8, TPOR did not meet the 300µs maximum spec when the supply slew rate <=100V/s.

6.2.5 Power consumption operating behaviors

Table 12. Power consumption operating behaviors - Bypass Mode

Symbol	Description	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	See note	mA	1
$I_{DD\_RUNCO\_CM}$	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus disabled, LPTMR running using LPO clock at 1kHz, CoreMark benchmark code executing from flash at 3.0 V	6.80	8.41	mA	2, 3
I_{DD_RUNCO}	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V	4.05	4.98	mA	3, 4
I_{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V	5.00	6.01	mA	3, 4
I_{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V				3, 4, 5
	at 25 °C	6.48	6.70	mA	
	at 70 °C	6.77	6.96	mA	
	at 105 °C	7.13	7.90	mA	
I_{DD_WAIT}	Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V	3.07	4.31	mA	4
I_{DD_WAIT}	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V	2.29	3.15	mA	4
I_{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 3.0 V	2.32	3.11	mA	4
$I_{DD\_VLPRCO\_CM}$	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, LPTMR running using LPO clock at 1 kHz	766.9	1538	µA	6

Table continues on the next page...

Table 12. Power consumption operating behaviors - Bypass Mode (continued)

Symbol	Description	Typ.	Max.	Unit	Notes
	reference clock, CoreMark benchmark code executing from flash at 3.0 V				
I_{DD_VLPRCO}	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V	158.45	377	µA	7
I_{DD_VLPR}	Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V	185.26	410	µA	7
I_{DD_VLPR}	Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V	240.96	805.3	µA	5, 7
I_{DD_VLPW}	Very-low-power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V	133.95	552.8	µA	7
I_{DD_STOP}	Stop mode current at 3.0 V				8
	at 25 °C	204.98	261.5	µA	
	at 70 °C	291.89	740	µA	
	at 105 °C	599.46	1410	µA	
I_{DD_VLPS}	Very-low-power stop mode current at Bypass mode(3.0 V),				
	at 25 °C	6.4	18	µA	
	at 70 °C	30.64	76.6	µA	
	at 105 °C	157	328	µA	
I_{DD_LLS3}	Low-leakage stop mode 3 current at Bypass mode(3.0 V),				8
	at 25 °C	2.57	3.70	µA	
	at 70 °C	11.76	22.37	µA	
	at 105 °C	50.92	90.46	µA	
I_{DD_LLS2}	Low-leakage stop mode 2 current at Bypass mode(3.0 V),				8
	at 25 °C	2.35	2.95	µA	
	at 70 °C	9.74	19.15	µA	
	at 105 °C	42.34	71.79	µA	
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current at Bypass mode(3.0 V),				
	at 25 °C	2.13	3.3	µA	
	at 70 °C	10.78	22.97	µA	
	at 105 °C	46.70	83.54	µA	
I_{DD_VLLS2}	Very-low-leakage stop mode 2 current at Bypass mode(3.0 V),				8

Table continues on the next page...

Table 12. Power consumption operating behaviors - Bypass Mode (continued)

Symbol	Description	Typ.	Max.	Unit	Notes
	at 25 °C	1.84	2.40	µA	
	at 70 °C	7.88	15.19	µA	
	at 105 °C	34.76	57.85	µA	
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current at Bypass mode(3.0 V),				8
	at 25°C	851.45	1027.8	nA	
	at 70°C	3.57	6.28	µA	
	at 105°C	17.62	23.06	µA	
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V				
	at 25 °C	433.00	702.6	nA	
	at 70 °C	3.15	5.99	µA	
	at 105 °C	17.2	22.6	µA	
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V				8, 9
	at 25 °C	258.12	516.43	nA	
	at 70 °C	2.97	5.81	µA	
	at 105 °C	16.9	22.4	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for FEI mode. CoreMark benchmark compiled using IAR 7.70 with optimization level high, optimized for balanced.
3. Radio is off.
4. MCG configured for FEI mode.
5. Incremental current consumption from peripheral activity is not included.
6. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 7.70 with optimization level high, optimized for balanced.
7. MCG configured for BLPI mode.
8. Supported through the connectivity software in its pre-defined Deep Sleep Modes.
9. No brownout.

Table 13. Power consumption operating behaviors - Buck Mode

Symbol	Description	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	See note	mA	1
I_{DD_RUNCO}	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V	3.51	—	mA	2, 3
I_{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V	4.00	—	mA	2, 3

Table continues on the next page...

Table 13. Power consumption operating behaviors - Buck Mode (continued)

Symbol	Description	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V				2, 3, 4
	at 25 °C	5.81	—	mA	
	at 85 °C	6.03	—	mA	
	at 105 °C	6.36	—	mA	
I_{DD_WAIT}	Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V	2.97	—	mA	2
I_{DD_WAIT}	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V	2.51	—	mA	2
I_{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 3.0 V	2.33	—	mA	2
I_{DD_VLPRCO}	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V	101.75	—	µA	5
I_{DD_VLPR}	Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V	132.17	—	µA	5
I_{DD_VLPR}	Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V	167.65	—	µA	4, 5
I_{DD_VLPW}	Very-low-power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V	105.72	—	µA	5
I_{DD_STOP}	Stop mode current at 3.0 V				
	at 25 °C	1.43	2.32	mA	
	at 70 °C	1.56	4.35	mA	
	at 105 °C	1.99	4.68	mA	
I_{DD_VLPS}	Very-low-power stop mode current at Buck mode(3.0 V),				
	at 25 °C	4.18	14.98	µA	
	at 70 °C	44.30	110	µA	
	at 105 °C	218.64	446	µA	
I_{DD_LLS3}	Low-leakage stop mode 3 current at Buck mode(3.0 V),				
	at 25 °C	2.64	4.89	µA	
	at 70 °C	15.27	25.51	µA	
	at 105 °C	81.93	104.35	µA	

Table continues on the next page...

Table 13. Power consumption operating behaviors - Buck Mode (continued)

Symbol	Description	Typ.	Max.	Unit	Notes
I_{DD_LLS2}	Low-leakage stop mode 2 current at Buck mode(3.0 V),				
	at 25 °C	2.46	3.80	µA	
	at 70 °C	10.14	21.14	µA	
	at 105 °C	63.49	80.21	µA	
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current at Buck mode(3.0 V),				
	at 25 °C	2.03	3.28	µA	
	at 70 °C	12.44	23.8	µA	
	at 105 °C	62.23	83.9	µA	
I_{DD_VLLS2}	Very-low-leakage stop mode 2 current at Buck mode(3.0 V),				
	at 25 °C	1.79	2.43	µA	
	at 70 °C	8.87	16.7	µA	
	at 105 °C	49.39	62.94	µA	
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current at Buck mode(3.0 V),				
	at 25 °C	0.830	1.07	µA	
	at 70 °C	4.95	10.67	µA	
	at 105 °C	27.51	36.14	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for FEI mode.
3. Radio is off.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode.

Table 14. Low power mode peripheral adders — typical value (Bypass Mode)

Symbol	Description	Temperature (°C)					Unit
		-40	25	50	70	85	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	46	46	47	47	47	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	88	91	90	89	88	µA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the RTC bits. Measured by entering all modes with the crystal enabled.						
	VLLS1	1.4	1.3	1.6	2.4	4.1	

Table continues on the next page...

Table 14. Low power mode peripheral adders — typical value (Bypass Mode) (continued)

Symbol	Description	Temperature (°C)					Unit
		-40	25	50	70	85	
	VLLS2	1.6	1.5	1.9	4.2	7.7	µA
	VLLS3	2.7	1.9	2.9	7.7	15	
	LLS2	1.8	1.4	1.7	4.1	8	
	LLS3	2.6	1.7	2.8	7.6	15.2	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	19	20	21	21	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	1.4	1.3	1.6	2.4	4.3	µA
I_{LPUART}	LPUART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.						
	MCGIRCLK (4 MHz internal reference clock)	53	54	54	54	54	µA
I_{LPTMR}	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.	30	30	30	85	100	nA
I_{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.						
	MCGIRCLK (4 MHz internal reference clock)	58	59	59	59	59	µA
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	76	82	85	87	87	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by	331	327	327	327	328	µA

Table 14. Low power mode peripheral adders — typical value (Bypass Mode)

Symbol	Description	Temperature (°C)					Unit
		-40	25	50	70	85	
	placing the device in STOP or VLPS mode. ADC is configured for low-power mode using the internal clock and continuous conversions.						

6.2.6 Diagram: Typical IDD_RUN operating behavior

The following data was measured from previous devices with same MCU core (ARM® Cortex-M0+) under these conditions:

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

NOTE

The results in the following graphs are obtained using the device in Bypass mode.

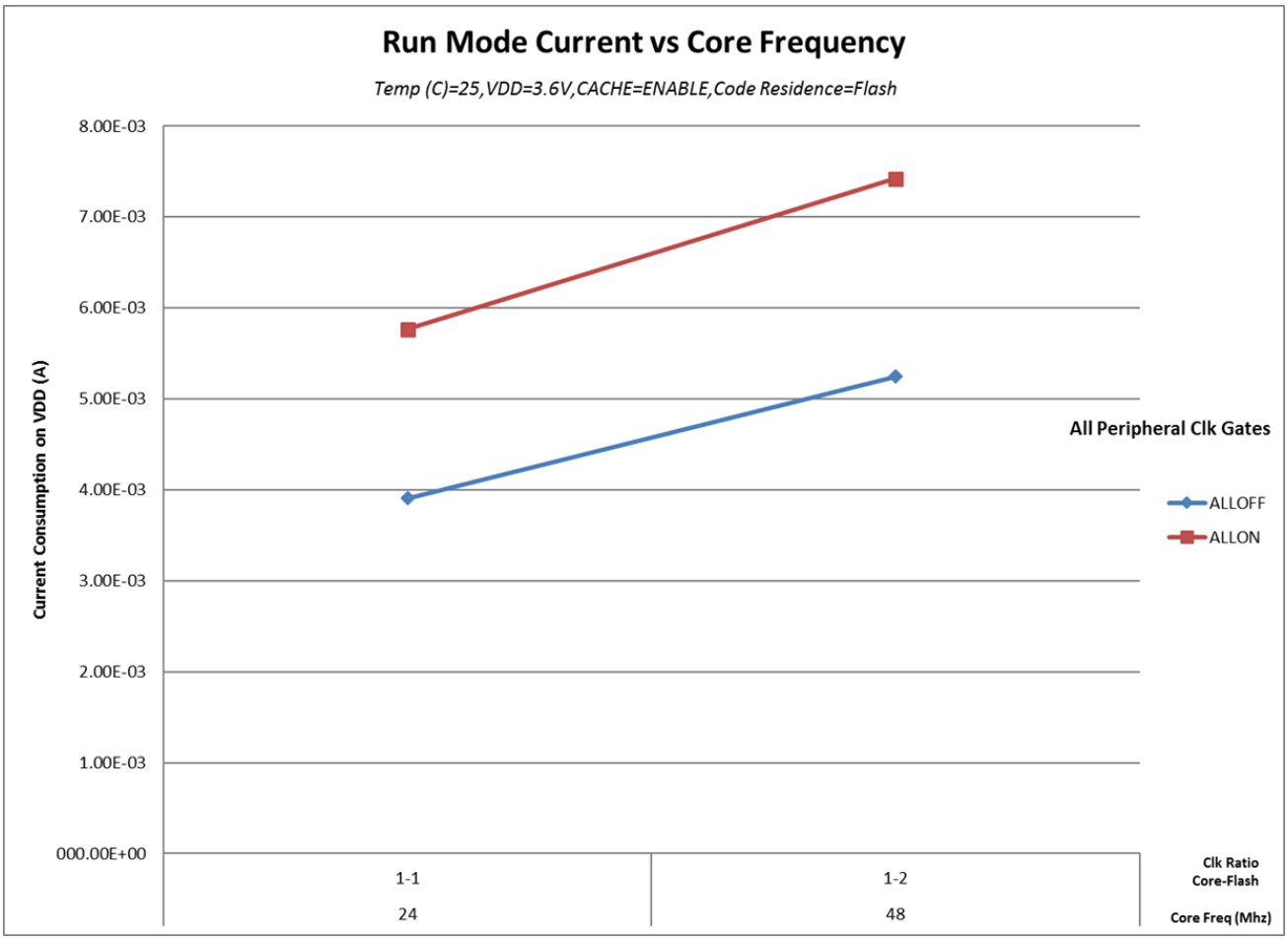


Figure 4. Run mode supply current vs. core frequency

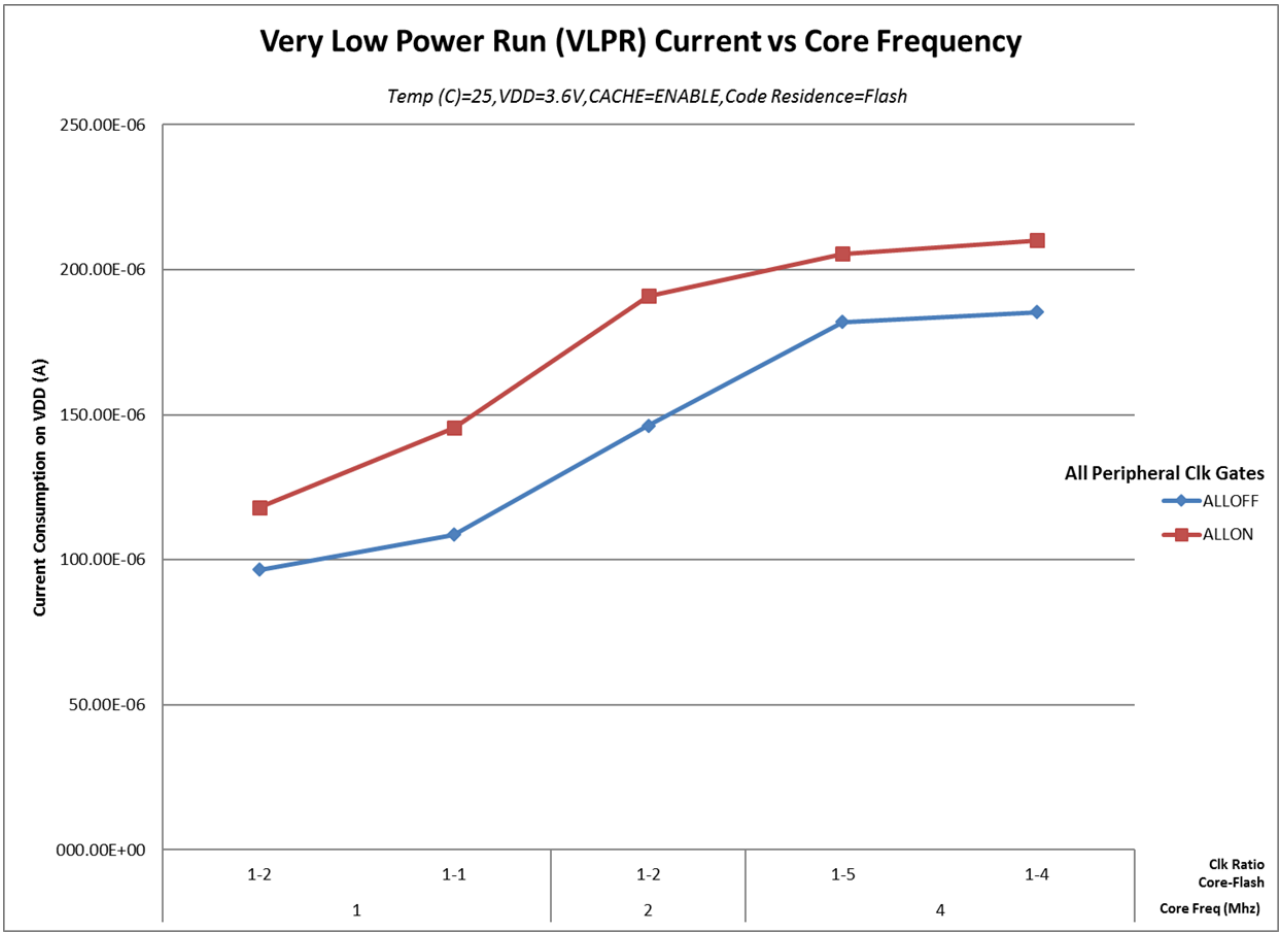


Figure 5. VLPR mode current vs. core frequency

6.2.7 SoC Power Consumption

Full KW36A/35A system-on-chip (SoC) power consumption is a function of the many configurations possible for the MCU platform and its peripherals including the 2.4 GHz radio and the DC-DC converter. A few measured SoC configurations are as follows:

Table 15. SoC Power Consumption

MCU State	Flash State	Radio State	DCDC State	Typical Average IC current	Unit
STOP	Doze	Rx	Buck (V_{DCDC_IN}=3.6 V)	8.5	mA
STOP	Doze	Tx (at 0 dBm)	Buck (V_{DCDC_IN}=3.6 V)	7.8	mA
STOP	Doze	Tx (at +3.5 dBm)	Buck (V_{DCDC_IN}=3.6 V)	9.2	mA

Table continues on the next page...

Table 15. SoC Power Consumption (continued)

MCU State	Flash State	Radio State	DCDC State	Typical Average IC current	Unit
RUN	Enabled	Rx	Buck (V_{DCDC_IN}=3.6 V)	10.4	mA
RUN	Enabled	Tx (at 0 dBm)	Buck (V_{DCDC_IN}=3.6 V)	9.9	mA
RUN	Enabled	Tx (at +3.5 dBm)	Buck (V_{DCDC_IN}=3.6 V)	11.7	mA
STOP	Doze	Rx	Disabled/Bypass	17.3	mA
STOP	Doze	Tx (at 0 dBm)	Disabled/Bypass	15.9	mA
STOP	Doze	Tx (at +3.5 dBm)	Disabled/Bypass	18.3	mA
RUN	Enabled	Rx	Disabled/Bypass	21.5	mA
RUN	Enabled	Tx (at 0 dBm)	Disabled/Bypass	19.9	mA
RUN	Enabled	Tx (at +3.5 dBm)	Disabled/Bypass	22.4	mA

6.2.8 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com
2. Perform a keyword search for “EMC design.”

6.2.9 Capacitance attributes

Table 16. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

6.3 Switching electrical specifications

6.3.1 Device clock specifications

Table 17. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	24	MHz
f_{FLASH}	Flash clock	—	24	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes[1]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock[2]	—	24	MHz
f_{ERCLK}	External reference clock	—	16	MHz
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
f_{TPM}	TPM asynchronous clock	—	8	MHz
$f_{LPUART0}$	LPUART0 asynchronous clock	—	12	MHz

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

6.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, CAN (for KW36A only), CMT and I^2C signals.

Table 18. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
NMI_b pin interrupt pulse width (analog filter enabled) — Asynchronous path	200	—	ns	3
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	20	—	ns	3
External RESET_b input pulse width (digital glitch filter disabled)	100	—	ns	
Port rise and fall time(high drive strength) • Slew enabled	— —	25 16	ns ns	4, 5

Table continues on the next page...

Table 18. General switching specifications (continued)

Description	Min.	Max.	Unit	Notes
• 1.71 ≤ VDD ≤ 2.7 V • 2.7 ≤ VDD ≤ 3.6 V • Slew disabled • 1.71 ≤ VDD ≤ 2.7 V • 2.7 ≤ VDD ≤ 3.6 V	— —	8 6	ns ns	
Port rise and fall time(low drive strength) • Slew enabled • 1.71 ≤ VDD ≤ 2.7 V • 2.7 ≤ VDD ≤ 3.6 V • Slew disabled • 1.71 ≤ VDD ≤ 2.7 V • 2.7 ≤ VDD ≤ 3.6 V	 — — —	 24 16 10 6	 ns ns ns ns	6, 7

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry in run modes.
2. The greater of synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized.
4. PTB0, PTB1, PTC0, PTC1, PTC2, PTC3, PTC6, PTC7, PTC17, PTC18.
5. 75 pF load.
6. Ports A, B, and C.
7. 25 pF load.

6.4 Thermal specifications

6.4.1 Thermal operating requirements

Table 19. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

6.4.2 Thermal attributes

Table 20. Thermal attributes

Board type	Symbol	Description	48-pin LQFN	40-pin "Wettable" QFN	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	48.3	19.2	°C/W	1, 2
—	Ψ_{JT}	Thermal characterization parameter, junction to package top (natural convection)	0.5	0.1	°C/W	1, 3

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board construction.
2. Determined according to JEDEC Standard JESD51-2.
3. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

The thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top of the package case using the following equation:

$T_J = T_T + \Psi_{JT}$ x chip power dissipation

where T_T is the thermocouple temperature at the top of the package.

6.5 Peripheral operating requirements and behaviors

6.5.1 Core modules

6.5.1.1 SWD electricals

Table 21. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns

Table continues on the next page...

Table 21. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

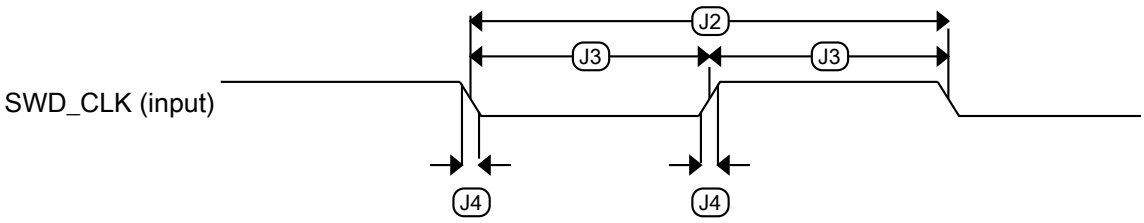


Figure 6. Serial wire clock input timing

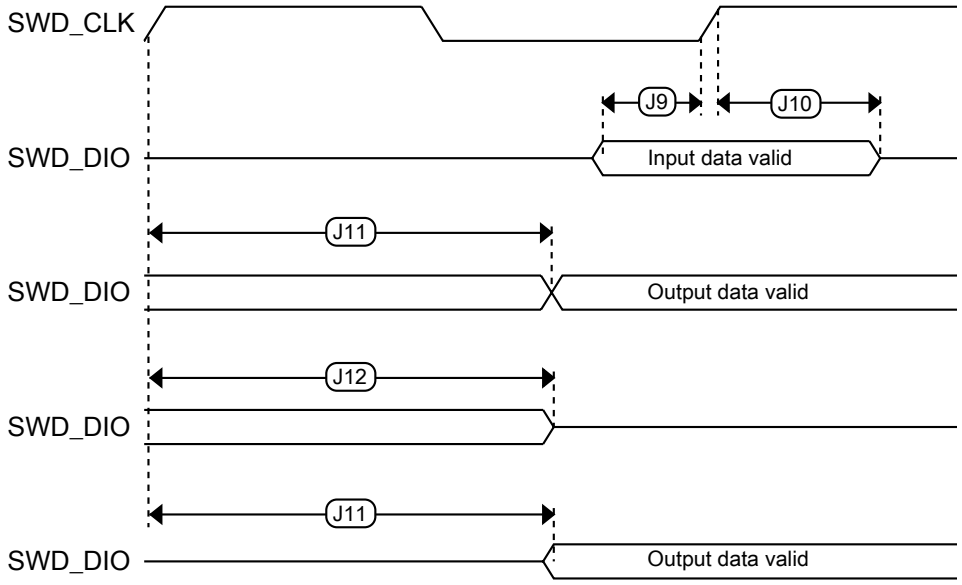


Figure 7. Serial wire data timing

6.5.2 System modules

There are no specifications necessary for the device's system modules.

6.5.3 Clock modules

6.5.3.1 MCG specifications

Table 22. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTRIM] and C4[SCFTRIM]		—	± 0.3	± 0.6	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	± 3	$\%f_{dco}$	1, 2
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C		—	± 0.4	± 1.5	$\%f_{dco}$	1, 2
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C		—	4	—	MHz	
Δf_{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V_{DD} and 25 °C		—	+1/-2	± 3	$\%f_{intf\_ft}$	2
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS = 00) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01) 1280 × f_{fll_ref}	40	41.94	48	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS = 00) 732 × f_{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS = 01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz		—	180	—	ps	7
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	8

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, f_{ints_ft}.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.5.3.2 Reference Oscillator Specification

The KW36A/35A has been designed to meet targeted standard specifications for frequency error over the life of the part, which includes the temperature, mechanical and aging excursions.

The table below shows the recommended crystal specifications. Note that these are recommendations only and deviation may be allowed. However, deviations may result in degraded RF performance or possibly a failure to meet RF protocol certification standards. Designers should do due diligence to ensure that the crystal(s) they use will meet the requirements of their application.

Table 23. Recommended Crystal Specification

Symbol	Description	Comment	32M			26M			Unit
			Min	Typ	Max	Min	Typ	Max	
	Operating Temperature		-40		105	-40		105	℃
Faging	Frequency accuracy over aging	1st year	-5		5	-5		5	ppm - 1st yr
iFacc	Initial Frequency accuracy	with respect to XO	-10		10	-10		10	ppm
Fstab	Frequency stability	across temperature, mechanical , load and voltage changes	-10		10	-10		10	ppm
CL	Values of CL supported(Integrated on die and programmable)		7	10	13	7	10	13	pF
Co	Shunt parasitic capacitance		0.469	0.67	0.871	0.42	0.6	0.78	pF

Table continues on the next page...

Table 23. Recommended Crystal Specification (continued)

Symbol	Description	Comment	32M			26M			Unit
			Min	Typ	Max	Min	Typ	Max	
Cm1	Motional capacitance Cm1		1.435	2.05	2.665	1.435	2.05	2.665	fF
Lm1	Motional inductance Lm1		8.47	12.1	15.73	12.81	18.3	23.79	mH
TS	Trim Sensitivity (TS) for the supported [Co,CL] values		6.30	9.00	11.70	6.39	9.12	11.86	ppm/pF
T_{OSC}	Oscillator Startup Time		—	500	—	—	500	—	µs
Rm1	ESR: Maximum value of Rm1			25	60		35	60	Ohms
	Maximum crystal drive level limit				200			200	µW

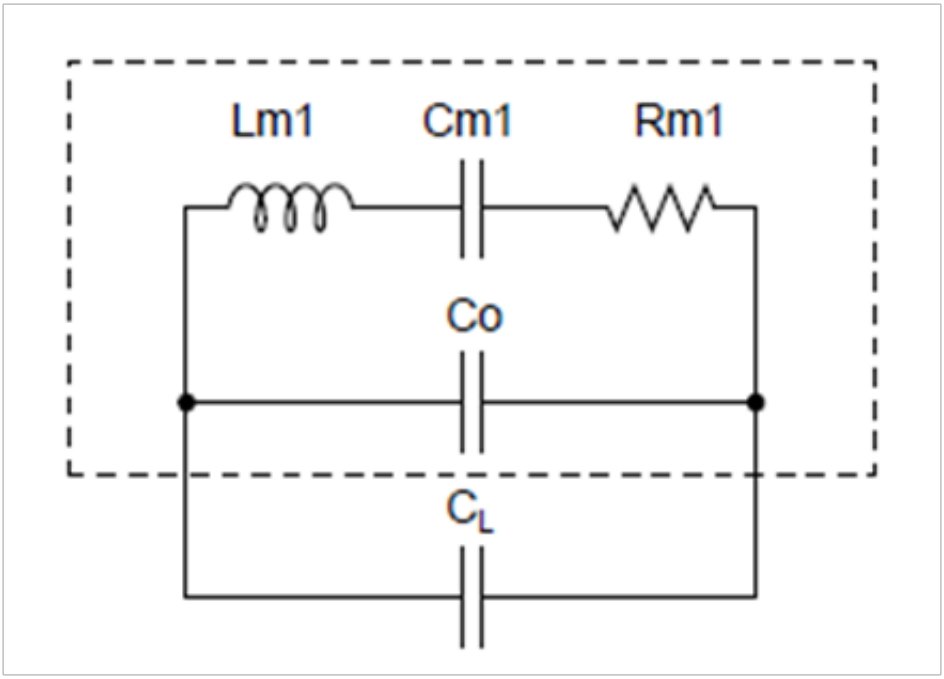


Figure 8. Crystal Electrical Model

6.5.3.3 32 kHz Oscillator Frequency Specifications

Table 24. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.678	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{DD}	mV	2, 3

1. Proper PC board layout procedures must be followed to acheive specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{DD}.

6.5.4 Memories and memory interfaces

6.5.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

6.5.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 25. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk256k}$	Erase Flash Block high-voltage time for 256 KB	—	208	1808	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.5.4.1.2 Flash timing specifications — commands

Table 26. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					

Table continues on the next page...

Table 26. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk256k}$	• 256 KB program/data flash	—	—	1.8	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (2 KB flash)	—	—	75	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	µs	1
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
$t_{ersblk256k}$	Erase Flash Block execution time • 256 KB program/data flash		220	1850	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec2k}$	Program Section execution time (2 KB flash)	—	10	—	ms	
$t_{rd1allx}$ $t_{rd1alln}$	Read 1s All Blocks execution time • FlexNVM devices • Program flash only devices	— —	— —	3.4 3.4	ms ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	450	3700	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	450	3700	ms	2
$t_{swapx01}$ $t_{swapx02}$ $t_{swapx04}$ $t_{swapx08}$ $t_{swapx10}$	Swap Control execution time • control code 0x01 • control code 0x02 • control code 0x04 • control code 0x08 • control code 0x10	 — — — — —	 200 90 90 — 90	 — 150 150 30 150	 µs µs µs µs µs	
$t_{pgmpart32k}$ $t_{pgmpart256k}$	Program Partition for EEPROM execution time • 32 KB EEPROM backup • 256 KB EEPROM backup	 — —	 230 240	 — —	 ms ms	
$t_{setramff}$ $t_{setram32k}$ $t_{setram256k}$	Set FlexRAM Function execution time: • Control Code 0xFF • 32 KB EEPROM backup • 256 KB EEPROM backup	 — — —	 112 0.8 4.5	 — 1.2 5.5	 µs ms ms	
$t_{eewr8b32k}$ $t_{eewr8b256k}$	Byte-write to FlexRAM execution time: • 32 KB EEPROM backup • 256 KB EEPROM backup	 — —	 385 1000	 1700 3250	 µs µs	
$t_{eewr16b32k}$	16-bit write to FlexRAM execution time:	—	385	1700	µs	

Table continues on the next page...

Table 26. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{eewr16b256k}$	• 32 KB EEPROM backup • 256 KB EEPROM backup	—	1000	3250	µs	
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	1500	µs	
	32-bit write to FlexRAM execution time:					
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	630	2000	µs	
$t_{eewr32b256k}$	• 256 KB EEPROM backup	—	1900	3500	µs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

6.5.4.1.3 Flash high voltage current behaviors

Table 27. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.5.4.1.4 Reliability specifications

Table 28. NVM reliability specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
Program and Data Flash						
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	—	—	years	
$n_{nvmcycp}$	Cycling endurance	1 K	—	—	cycles	1
FlexRAM as Emulated EEPROM						
$t_{nvmretee}$	Data retention	5	—	—	years	
$n_{nvmwree16}$	Write endurance					2
$n_{nvmwree256}$	• EEPROM backup to FlexRAM ratio = 16	100 K	—	—	writes	
	• EEPROM backup to FlexRAM ratio = 256	1.6 M	—	—	writes	

1. Program and erase supported across standard temperature specs.
2. EEPROM write endurance specified for 16-bit and/or 32-bit writes to FlexRAM and is supported across standard temperature specs. Greater EEPROM write endurance achieved with larger ratios of EEPROM backup to FlexRAM used.

6.5.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFE to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application.

6.5.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.5.6 Analog

6.5.6.1 ADC electrical specifications

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications. The following specification is defined with the DC-DC converter operating in Bypass mode.

6.5.6.1.1 16-bit ADC operating conditions

Table 29. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	3
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VSSA VSSA	— —	31/32 × VREFH VREFH	V	

Table continues on the next page...

Table 29. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	4
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	5
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	5
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	kS/s	6
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	kS/s	6

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated VREFH and VREFL pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SSA}.
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
5. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
6. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

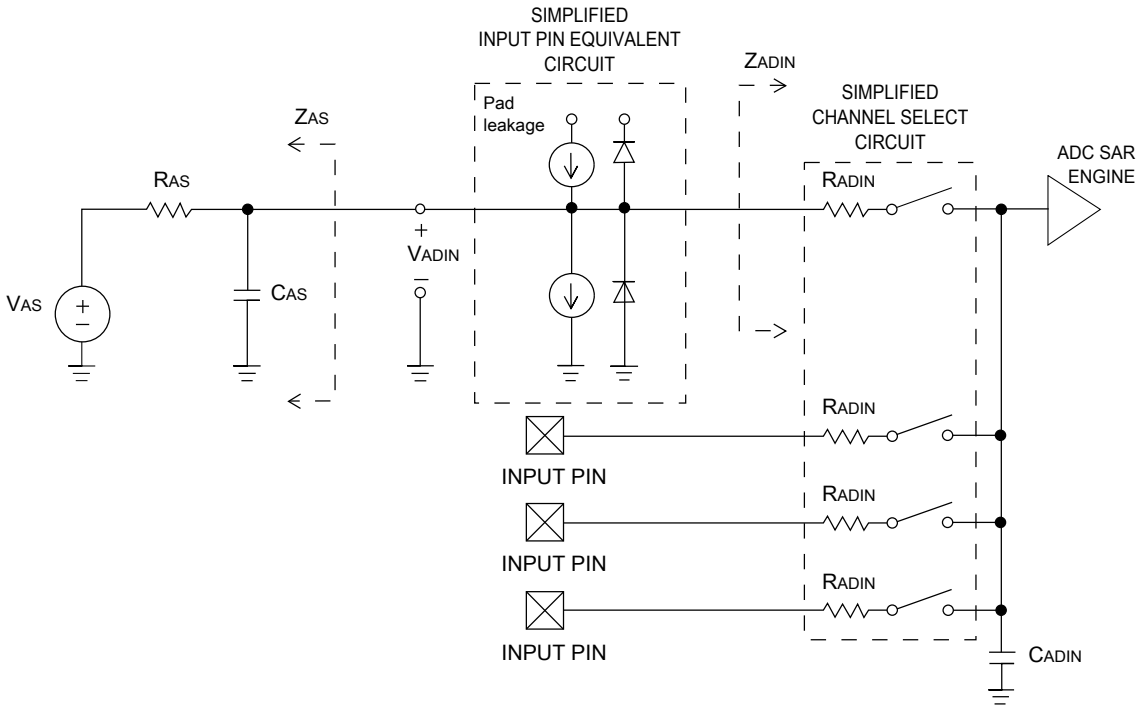


Figure 9. ADC input impedance equivalency diagram

6.5.6.1.2 16-bit ADC electrical characteristics

Table 30. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC=1, ADHSC=0 • ADLPC=1, ADHSC=1 • ADLPC=0, ADHSC=0 • ADLPC=0, ADHSC=1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz	t_{ADACK} = $1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit mode; Buck Mode[6] • 12-bit mode; Bypass Mode	— —	±0.7 ±0.5	–1.1 to +1.9 –1.1 to +1.9	LSB[4]	5

Table continues on the next page...

Table 30. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
INL	Integral non-linearity	• 12-bit mode; Buck Mode[6] • 12-bit mode; Bypass Mode	— —	±1.0 ±0.6	–2.7 to +1.9 –2.7 to +1.9	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode; Buck Mode[6] • Avg = 32 • Avg = 4 16-bit single-ended mode; Buck Mode[6] • Avg = 32 • Avg = 4 16-bit differential mode; Bypass Mode • Avg = 32 • Avg = 4 16-bit single-ended mode; Bypass Mode • Avg = 32 • Avg = 4	 12 11.25 11 9.5 12.5 11.25 11 10	 12.75 11.75 11.5 10.5 13 12 11.75 10.5	 — — — — — — — —	bits	7
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode; Buck Mode[6] • Avg = 32 16-bit single-ended mode; Buck Mode[6] • Avg = 32 16-bit differential mode; Bypass Mode • Avg = 32 16-bit single-ended mode; Bypass Mode • Avg = 32	 — — — —	 -90 -88 -89 -87	 — — — —	dB	8

Table continues on the next page...

Table 30. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
SFDR	Spurious free dynamic range distortion	16-bit differential mode; Buck Mode[6] • Avg = 32	85	89	—	dB	8
		16-bit single-ended mode; Buck Mode[6] • Avg = 32	85	87	—		
		16-bit differential mode; Bypass Mode • Avg = 32	87	94	—		
		16-bit single-ended mode; Bypass Mode • Avg = 32	85	88	—		
E_{IL}	Input leakage error		I_{In} × R_{AS}			mV	I_{In} = leakage current (see Voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.67	1.74	1.81	mV/° C	9
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}.
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = (V_{REFH} - V_{REFL})/2^N.
5. ADC conversion clock < 16 MHz, maximum hardware averaging (AVGE = %1, AVGS = %11).
6. VREFH = Output of Voltage Reference(VREF).
7. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
8. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
9. ADC conversion clock < 3 MHz.

6.5.6.2 Voltage reference electrical specifications

Table 31. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	-40 to 105		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 32. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25°C	1.190	1.1950	1.2	V	1
V_{out}	Voltage reference output with user trim at nominal V_{DDA} and temperature=25°C	1.1945	1.1950	1.1955	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift (V_{max} -V_{min} across the full temperature range)	—	—	20	mV	1
I_{bg}	Bandgap only current	—	—	80	µA	
I_{lp}	Low-power buffer current	—	—	360	uA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	µV	1, 2
T_{stup}	Buffer startup time	—	—	100	µs	
$T_{chop\_osc\_stup}$	Internal bandgap start-up delay with chop oscillator enabled	—	—	35	ms	
V_{vdrift}	Voltage drift (V_{max} -V_{min} across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 33. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	70	°C	

Table 34. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{tdrift}	Temperature drift (V_{max} -V_{min} across the limited temperature range)	—	15	mV	

6.5.6.3 CMP and 6-bit DAC electrical specifications

Table 35. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

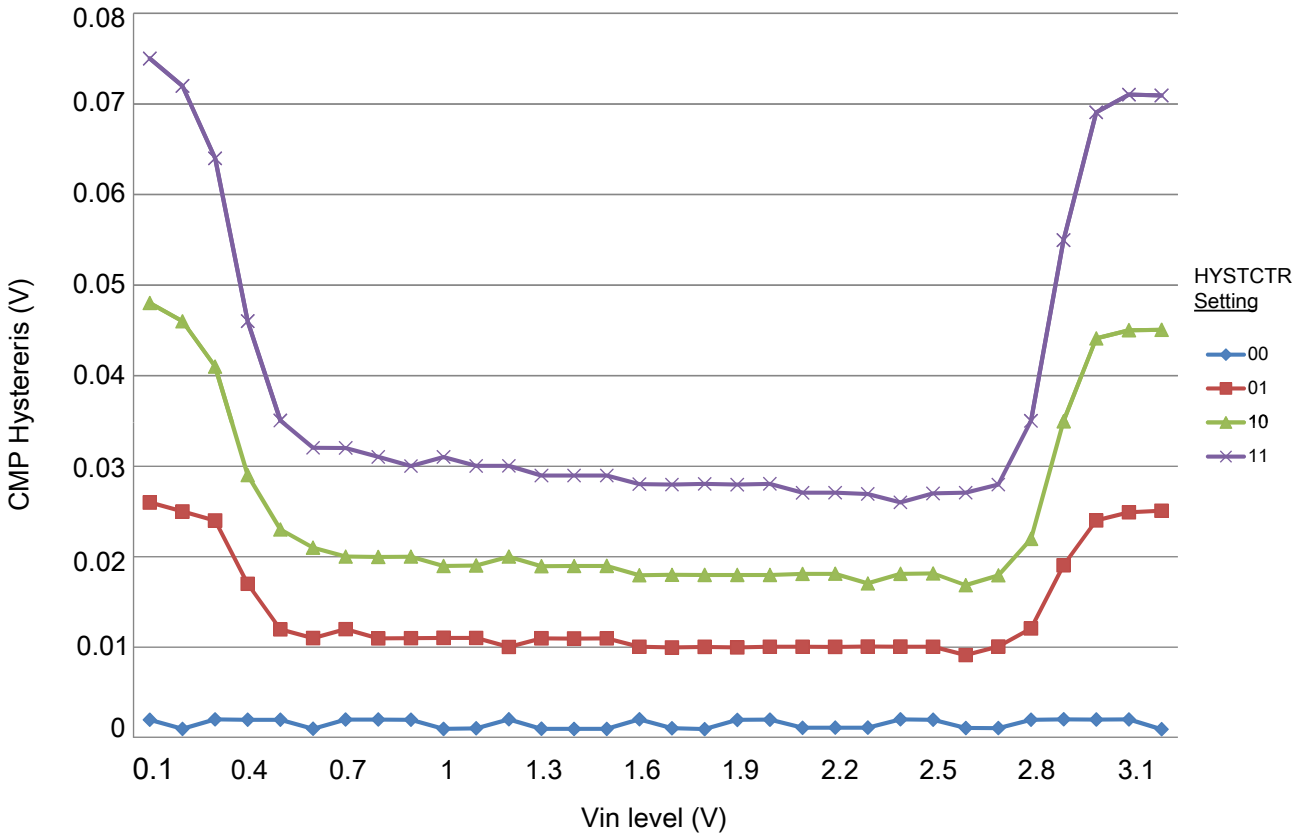


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

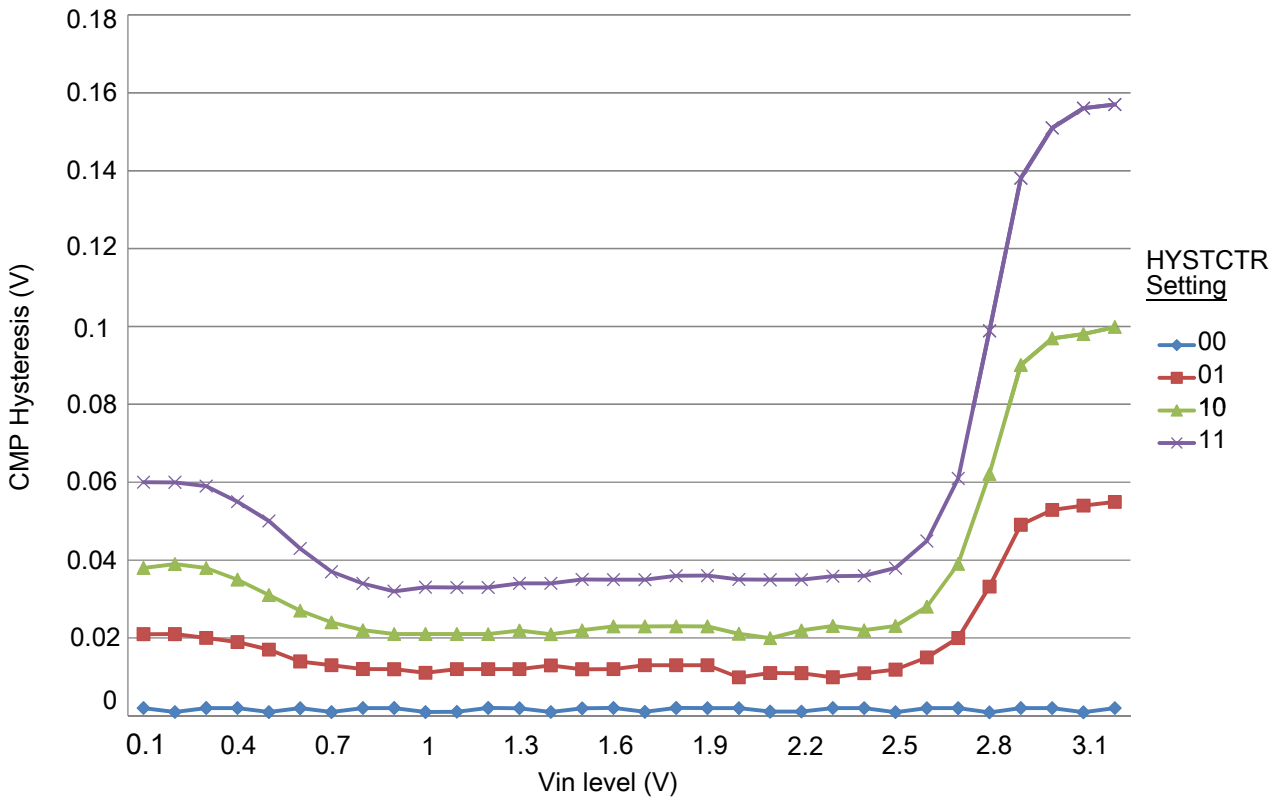


Figure 11. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.5.7 Timers

See General switching specifications.

6.5.8 Communication interfaces

6.5.8.1 CAN switching specifications

See General switching specifications.

6.5.8.2 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. See the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 36. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	12	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PCSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

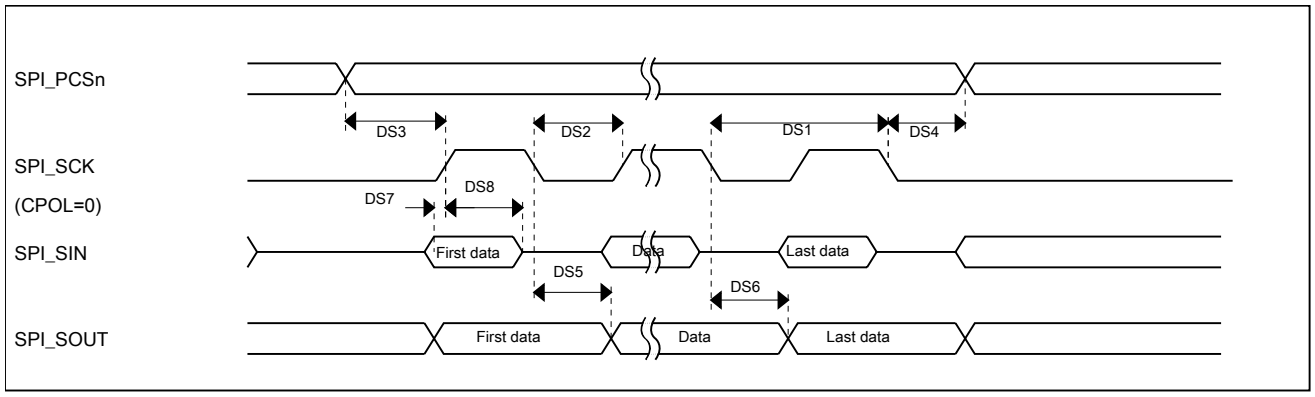


Figure 12. DSPI classic SPI timing — master mode

Table 37. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		6	MHz

Table continues on the next page...

Table 37. Slave mode DSPI timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	21.4	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

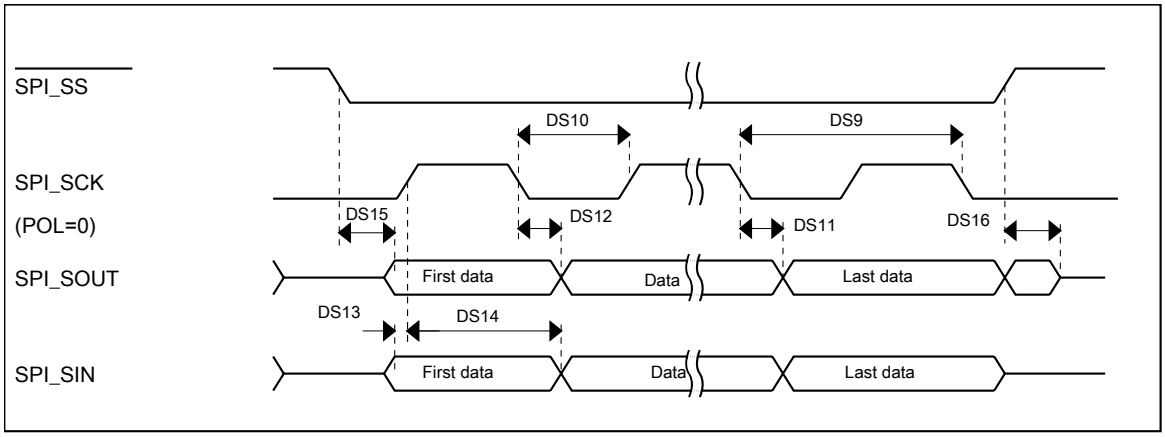


Figure 13. DSPI classic SPI timing — slave mode

6.5.8.3 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. See the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 38. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	

Table continues on the next page...

Table 38. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-1.2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	23.3	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PCSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

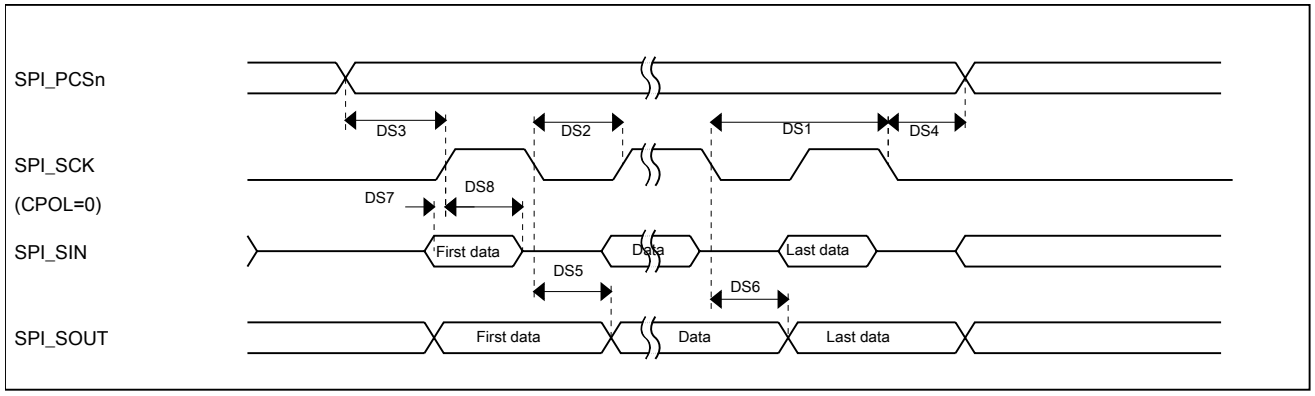


Figure 14. DSPI classic SPI timing — master mode

Table 39. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	29.1	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	25	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	25	ns

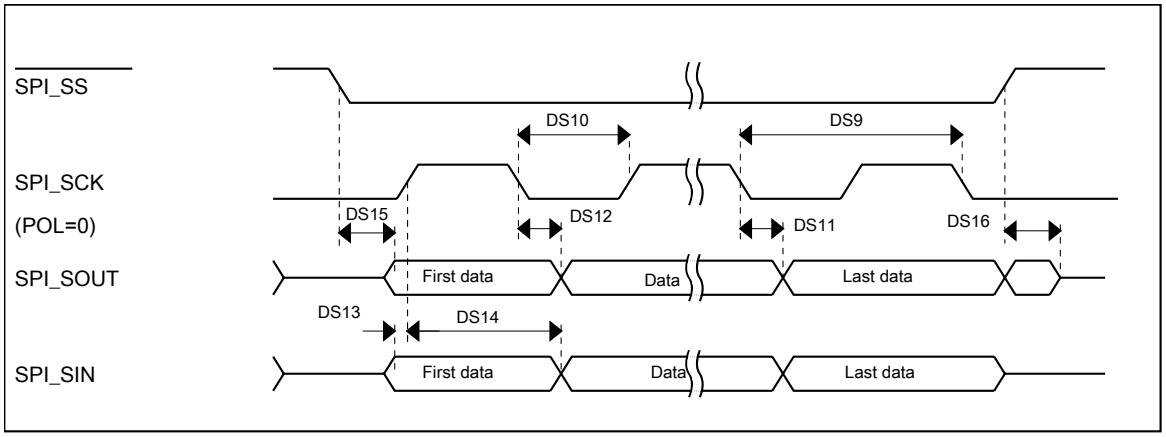


Figure 15. DSPI classic SPI timing — slave mode

6.5.8.4 Inter-Integrated Circuit Interface (I^2C) timing

Table 40. I^2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF.
4. Set-up time in slave-transmitter mode is 1 IP Bus clock period, if the TX FIFO is empty.
5. A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax}

+ $t_{SU;\ DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.

6. C_b = total capacitance of the one bus line in pF.

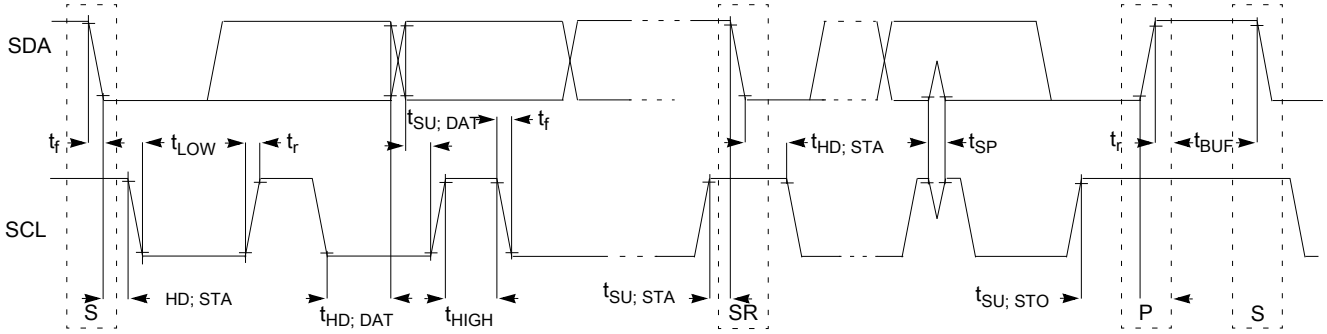


Figure 16. Timing definition for fast and standard mode devices on the I^2C bus

6.5.8.5 LPUART

See General switching specifications.

6.5.9 Human-machine interfaces (HMI)

6.5.9.1 GPIO

The maximum input voltage on PTC0/1/2/3 is VDD+0.3V. For rest of the GPIO specification, see General switching specifications.

6.6 DC-DC Converter Operating Requirements

Table 41. DC-DC Converter operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Bypass Mode Supply Voltage (RF and Analog)	VDD_{RF1}, VDD_{RF2}, VDD_{RF3}	1.425	—	3.6	Vdc
Bypass Mode Supply Voltage (Digital)	VDD_X, V_{DCDC_IN}, VDD_A	1.71	—	3.6	Vdc
Buck Mode Supply Voltage [1, 2]	V_{DCDC_IN}	2.1	—	3.6	Vdc
DCDC Inductor					
Value		—	10	—	µH
ESR		—	<0.2	<0.5	Ohms

1. In Buck mode, DC-DC converter needs 2.1 V minimum to start, the supply can drop to 1.8V after DC-DC converter settles.

2. In Buck mode, DC-DC converter will generate 1.8V at VDD_1P8OUT and 1.5V at VDD_1P5OUT_PMCIN pins. VDD_1P8OUT should supply to VDD_1, VDD_2 and VDD_A. VDD_1P5OUT_PMCIN should supply to VDD_RF_1 and VDD_RF_2. VDD_{XTAL} can be either supplied by 1.5V or 1.8V.

Table 42. DC-DC Converter Specifications

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
DC-DC Converter Output Power	Total power output of 1p8V and 1p5V	Pdcdc_out	—	—	125[1]	mW
Switching Frequency[2]		DCDC_FREQ	—	2	—	MHz
Half FET Threshold		I_half_FET	—	5	—	mA
Double FET Threshold		I_double_FET	—	40	—	mA
Buck Mode						
DC-DC Conversion Efficiency		DCDC_EFF_buck	—	90%	—	—
1.8V Output Voltage		VDD_1P8_buck	1.71	—	min(VDCDC_IN_buck, 3.5)[3, 4]	Vdc
1.8V Output Current[5, 6]	VDD_1P8 = 1.8V, VDC_1P5 = 1.5V	IDD_1P8_buck1	—	—	45	mA
	VDD_1P8 = 3.0V, VDC_1P5 = 1.5V	IDD_1P8_buck2	—	—	27	mA
1.5V Output Voltage		VDD_1P5_buck	—	1.5[7]	2.0	Vdc
1.5V Output Current[5, 8]		IDD_1P5_buck	—	—	30	mA
DCDC Transition Operating Behavior	LSS➔Run	t_DCDCbuck_LSS➔RUN	—	50	—	µs
DCDC Turn on Time		T_{DCDC_ON}	—	2.2[9]	—	ms
DCDC Settling Time for increasing voltage		$T_{DCDC\_SETTLE\_buck}$	—	3.11	—	ms/V
DCDC Settling Time for decreasing voltage	C = capacitance attached to the DCDC V1P8 output rail. V1 = the initial output voltage of the DCDC V2 = the final output voltage of the DCDC I2 = the load on the DCDC output expressed in Amperes.	$T_{DCDC\_SETTLE\_buck}$	—	(C*(V1-V2)/I2	—	s

1. This is the steady state DC output power. Excessive transient current load from external device will cause 1p8V and 1P5 output voltage unregulated temporary.
2. This is the frequency that will be observed at LN and LP pins.
3. The voltage output level can be controlled by programming DCDC_VDD1P8CTRL_TRG field in DCDC_REG3.
4. In Buck mode, the maximum VDD_1P8 output is the minimum of either VDCDC_IN_BUCK minus 50 mV or 3V. For example, if VDCDC_IN = 2.1 V, maximum VDD_1P8 is 2.05 V. If VDCDC_IN = 3.6 V, maximum VDD_1P8 is 3.5 V.

5. The output current specification in buck mode represents the maximum current the DC-DC converter can deliver. The KW36A/35A radio and MCU blocks current consumption is not excluded. Note that the maximum output power of the DC-DC converter is 125mW. The available supply current for external device depends on the energy consumed by the internal peripherals in KW36A/35A.
6. When using DC-DC in low power mode (pulsed mode), current load must be less than 1mA.
7. User needs to program DCDC_VDD1P5CTRL_TRG_BUCK field in DCDC_REG3 register to ensure that a worst case minimum of 1.425V is available as VDD_1P5_buck for radio operation. VDD_1P5 must not be programmed higher than VDD_1P8.
8. 1.5V is intended to supply power to KW36A/35A. It is not designed to supply power to an external device.
9. Turn on time is measured from the application of power (to DCDC_IN) till the DCDC_REG0[DCDC_STS_DC_OK] bit is set. Code execution may begin before the DCDC_REG0[DCDC_STS_DC_OK] bit is set. The full device specification is not guaranteed until the bit sets.

6.7 Ratings

6.7.1 Thermal handling ratings

Table 43. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.7.2 Moisture handling ratings

Table 44. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.7.3 ESD handling ratings

Table 45. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1

Table continues on the next page...

Table 45. ESD handling ratings (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

6.7.4 Voltage and current operating ratings

Table 46. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{IO_DCDC}	IO pins in the DCDC voltage domain (DCDC_CFG and PSWITCH)	GND	VDCDC	V

7 Pin Diagrams and Pin Assignments

7.1 KW36A Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

40 "Wettable" QFN	48 LQFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
—	4	PTA16	DISABLED		PTA16/ LLWU_P4	SPI1_ SOUT	LPUART1_ RTS_b		TPM0_CH0				

40 "Wettable" QFN	48 LQFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
—	5	PTA17	DISABLED		PTA17/ LLWU_P5	SPI1_SIN	LPUART1_ RX	CAN0_TX	TPM_ CLKIN1				
—	6	PTA18	DISABLED		PTA18/ LLWU_P6	SPI1_SCK	LPUART1_ TX	CAN0_RX	TPM2_CH0				
—	7	PTA19	DISABLED	ADC0_SE5	PTA19/ LLWU_P7	SPI1_PCS0	LPUART1_ CTS_b		TPM2_CH1				
—	24	ADC0_DP0	ADC0_ DP0/ CMP0_IN0	ADC0_ DP0/ CMP0_IN0									
—	25	ADC0_DM0	ADC0_ DM0/ CMP0_IN1	ADC0_ DM0/ CMP0_IN1									
—	41	PTC5	DISABLED		PTC5/ LLWU_P13/ RF_NOT_ ALLOWED		LPTMR0_ ALT2	LPUART0_ RTS_b	TPM1_CH1		BSM_CLK		
—	42	PTC6	DISABLED		PTC6/ LLWU_P14/ RF_ RFOSC_ EN		I2C1_SCL	LPUART0_ RX	TPM2_CH0		BSM_ FRAME		
—	43	PTC7	DISABLED		PTC7/ LLWU_P15	SPI0_PCS2	I2C1_SDA	LPUART0_ TX	TPM2_CH1		BSM_DATA		
1	48	PTC19	DISABLED		PTC19/ LLWU_P3/ RF_ EARLY_ WARNING	SPI0_PCS0	I2C0_SCL	LPUART0_ CTS_b	BSM_CLK			LPUART1_ CTS_b	
2	1	PTA0	SWD_DIO		PTA0	SPI0_PCS1			TPM1_CH0		SWD_DIO		
3	2	PTA1	SWD_CLK		PTA1	SPI1_PCS0			TPM1_CH1		SWD_CLK		
4	3	PTA2	RESET_b		PTA2				TPM0_CH3		RESET_b		
5	8	PSWITCH	PSWITCH	PSWITCH									
6	9	DCDC_ CFG	DCDC_ CFG	DCDC_ CFG									
7	10	VDCDC_IN	VDCDC_IN	VDCDC_IN									
8	11	DCDC_LP	DCDC_LP	DCDC_LP									
9	13	DCDC_ GND	DCDC_ GND	DCDC_ GND									
10	12	DCDC_LN	DCDC_LN	DCDC_LN									
11	14	VDD_ 1P8OUT	VDD_ 1P8OUT	VDD_ 1P8OUT									
12	—	DCDC_LN	DCDC_LN	DCDC_LN									
13	15	VDD_ 1P5OUT_ PMCIN	VDD_ 1P5OUT_ PMCIN	VDD_ 1P5OUT_ PMCIN									

40 "Wettable" QFN	48 LQFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
14	16	PTB0	DISABLED		PTB0/ LLWU_P8/ RF_ RFOSC_ EN		I2C0_SCL	CMP0_ OUT	TPM0_CH1		CLKOUT	CAN0_TX	
15	17	PTB1	DISABLED	ADC0_SE1/ CMP0_IN5	PTB1/ RF_ PRIORITY	DTM_RX	I2C0_SDA	LPTMR0_ ALT1	TPM0_CH2		CMT_IRO	CAN0_RX	
16	18	PTB2	DISABLED	ADC0_SE3/ CMP0_IN3	PTB2/ RF_NOT_ ALLOWED		DTM_TX		TPM1_CH0				
17	19	PTB3	DISABLED	ADC0_SE2/ CMP0_IN4	PTB3/ ERCLK32K	LPUART1_ RTS_b		CLKOUT	TPM1_CH1		RTC_ CLKOUT		
18	20	VDD_0	VDD_0	VDD_0									
19	21	PTB16	EXTAL32K	EXTAL32K	PTB16	LPUART1_ RX	I2C1_SCL		TPM2_CH0				
20	22	PTB17	XTAL32K	XTAL32K	PTB17	LPUART1_ TX	I2C1_SDA		TPM2_CH1		BSM_CLK		
21	23	PTB18	NMI_b	ADC0_SE4/ CMP0_IN2	PTB18	LPUART1_ CTS_b	I2C1_SCL	TPM_ CLKIN0	TPM0_CH0		NMI_b		
22	26	VREFL/ VSSA	VREFL/ VSSA	VREFL/ VSSA									
23	27	VREFH/ VREF_OUT	VREFH/ VREF_OUT	VREFH/ VREF_OUT									
24	28	VDDA	VDDA	VDDA									
25	29	XTAL_OUT	XTAL_OUT	XTAL_OUT									
26	30	EXTAL	EXTAL	EXTAL									
27	31	XTAL	XTAL	XTAL									
28	32	VDD_RF3	VDD_RF3	VDD_RF3									
29	33	ANT	ANT	ANT									
30	34	GANT	GANT	GANT									
31	35	VDD_RF2	VDD_RF2	VDD_RF2									
32	36	VDD_RF1	VDD_RF1	VDD_RF1									
33	37	PTC1	DISABLED		PTC1/ RF_ EARLY_ WARNING		I2C0_SDA	LPUART0_ RTS_b	TPM0_CH2			SPI1_SCK	BSM_CLK
34	38	PTC2	DISABLED		PTC2/ LLWU_P10	TX_ SWITCH	I2C1_SCL	LPUART0_ RX	CMT_IRO		DTM_RX	SPI1_ SOUT	BSM_ FRAME
35	39	PTC3	DISABLED		PTC3/ LLWU_P11	RX_ SWITCH	I2C1_SDA	LPUART0_ TX	TPM0_CH1		DTM_TX	SPI1_SIN	CAN0_TX
36	40	PTC4	DISABLED		PTC4/ LLWU_P12/ BLE_RF_ ACTIVE		EXTRG_IN	LPUART0_ CTS_b	TPM1_CH0		BSM_DATA	SPI1_PCS0	CAN0_RX

40 "Wettable" QFN	48 LQFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
37	44	VDD_1	VDD_1	VDD_1									
38	45	PTC16	DISABLED		PTC16/ LLWU_P0/ RF_ STATUS	SPI0_SCK	I2C0_SDA	LPUART0_ RTS_b	TPM0_CH3			LPUART1_ RTS_b	
39	46	PTC17	DISABLED		PTC17/ LLWU_P1/ RF_EXT_ OSC_EN	SPI0_ SOUT	I2C1_SCL	LPUART0_ RX	BSM_ FRAME		DTM_RX	LPUART1_ RX	
40	47	PTC18	DISABLED		PTC18/ LLWU_P2	SPI0_SIN	I2C1_SDA	LPUART0_ TX	BSM_DATA		DTM_TX	LPUART1_ TX	
41	49-64	Ground	NA										

7.2 KW36A Pinouts

KW36A device pinouts are shown in the figures below.

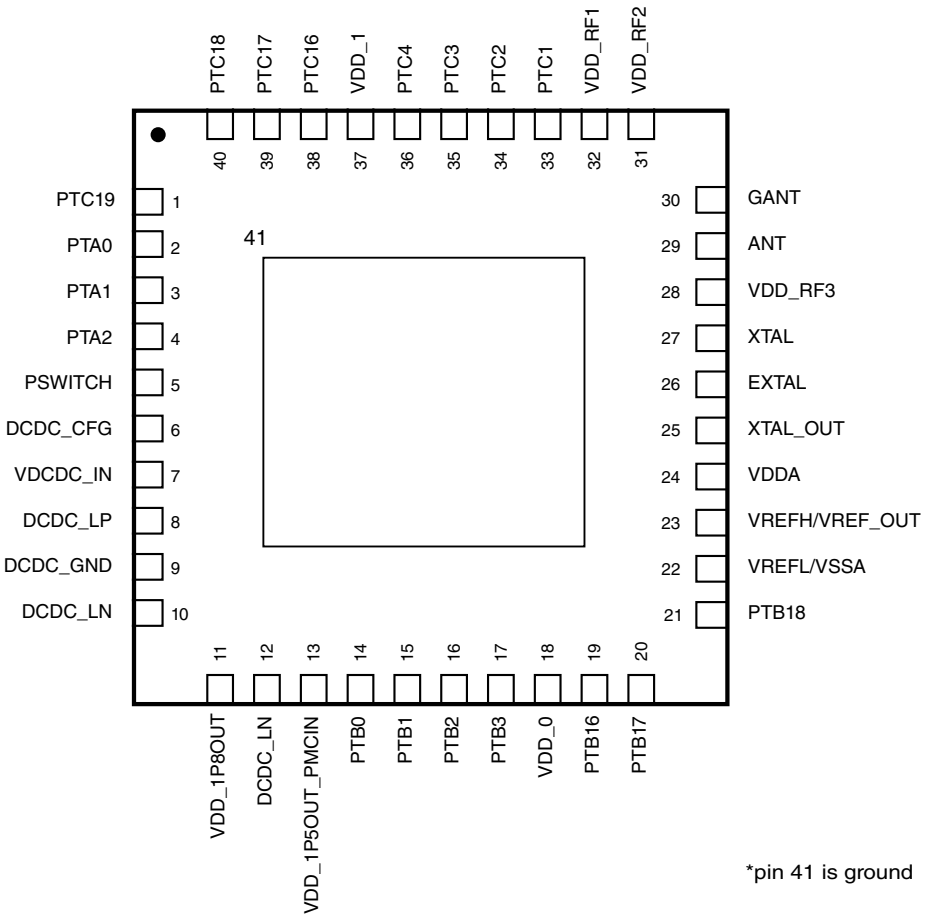


Figure 17. 40-pin "Wettable" QFN pinout diagram

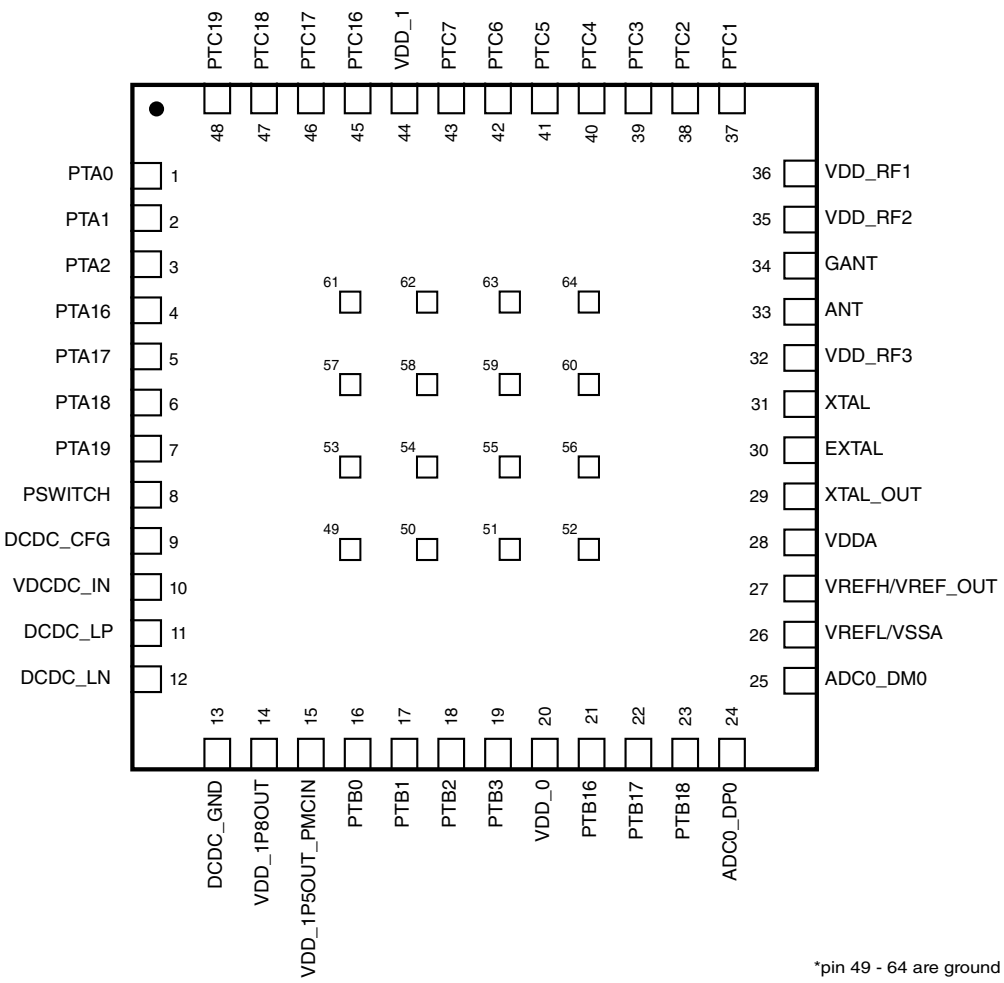


Figure 18. 48-pin LQFN pinout diagram

7.3 KW35A Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

40 "Wettable" QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
1	PTC19	DISABLED		PTC19/ LLWU_P3/	SPI0_PCS0	I2C0_SCL	LPUART0_ CTS_b	BSM_CLK				

40 "Wettable" QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
				RF_EARLY_WARNING								
2	PTA0	SWD_DIO		PTA0	SPI0_PCS1			TPM1_CH0		SWD_DIO		
3	PTA1	SWD_CLK		PTA1	SPI1_PCS0			TPM1_CH1		SWD_CLK		
4	PTA2	RESET_b		PTA2				TPM0_CH3		RESET_b		
5	PSWITCH	PSWITCH	PSWITCH									
6	DCDC_CFG	DCDC_CFG	DCDC_CFG									
7	VDCDC_IN	VDCDC_IN	VDCDC_IN									
8	DCDC_LP	DCDC_LP	DCDC_LP									
9	DCDC_GND	DCDC_GND	DCDC_GND									
10	DCDC_LN	DCDC_LN	DCDC_LN									
11	VDD_1P8OUT	VDD_1P8OUT	VDD_1P8OUT									
12	DCDC_LN	DCDC_LN	DCDC_LN									
13	VDD_1P5OUT_PMCIN	VDD_1P5OUT_PMCIN	VDD_1P5OUT_PMCIN									
14	PTB0	DISABLED		PTB0/LLWU_P8/RF_RFOSC_EN		I2C0_SCL	CMP0_OUT	TPM0_CH1		CLKOUT		
15	PTB1	DISABLED	ADC0_SE1/CMP0_IN5	PTB1/RF_PRIORITY	DTM_RX	I2C0_SDA	LPTMR0_ALT1	TPM0_CH2		CMT_IRO		
16	PTB2	DISABLED	ADC0_SE3/CMP0_IN3	PTB2/RF_NOT_ALLOWED		DTM_TX		TPM1_CH0				
17	PTB3	DISABLED	ADC0_SE2/CMP0_IN4	PTB3/ERCLK32K			CLKOUT	TPM1_CH1		RTC_CLKOUT		
18	VDD_0	VDD_0	VDD_0									
19	PTB16	EXTAL32K	EXTAL32K	PTB16		I2C1_SCL		TPM2_CH0				
20	PTB17	XTAL32K	XTAL32K	PTB17		I2C1_SDA		TPM2_CH1		BSM_CLK		
21	PTB18	NMI_b	ADC0_SE4/CMP0_IN2	PTB18		I2C1_SCL	TPM_CLKIN0	TPM0_CH0		NMI_b		
22	VREFL/VSSA	VREFL/VSSA	VREFL/VSSA									
23	VREFH/VREF_OUT	VREFH/VREF_OUT	VREFH/VREF_OUT									
24	VDDA	VDDA	VDDA									
25	XTAL_OUT	XTAL_OUT	XTAL_OUT									
26	EXTAL	EXTAL	EXTAL									
27	XTAL	XTAL	XTAL									
28	VDD_RF3	VDD_RF3	VDD_RF3									

40 "Wettable" QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
29	ANT	ANT	ANT									
30	GANT	GANT	GANT									
31	VDD_RF2	VDD_RF2	VDD_RF2									
32	VDD_RF1	VDD_RF1	VDD_RF1									
33	PTC1	DISABLED		PTC1/ RF_EARLY_ WARNING		I2C0_SDA	LPUART0_ RTS_b	TPM0_CH2			SPI1_SCK	BSM_CLK
34	PTC2	DISABLED		PTC2/ LLWU_P10	TX_SWITCH	I2C1_SCL	LPUART0_ RX	CMT_IRO		DTM_RX	SPI1_SOUT	BSM_ FRAME
35	PTC3	DISABLED		PTC3/ LLWU_P11	RX_ SWITCH	I2C1_SDA	LPUART0_ TX	TPM0_CH1		DTM_TX	SPI1_SIN	
36	PTC4	DISABLED		PTC4/ LLWU_P12/ BLE_RF_ ACTIVE		EXTRG_IN	LPUART0_ CTS_b	TPM1_CH0		BSM_DATA	SPI1_PCS0	
37	VDD_1	VDD_1	VDD_1									
38	PTC16	DISABLED		PTC16/ LLWU_P0/ RF_STATUS	SPI0_SCK	I2C0_SDA	LPUART0_ RTS_b	TPM0_CH3				
39	PTC17	DISABLED		PTC17/ LLWU_P1/ RF_EXT_ OSC_EN	SPI0_SOUT	I2C1_SCL	LPUART0_ RX	BSM_ FRAME		DTM_RX		
40	PTC18	DISABLED		PTC18/ LLWU_P2	SPI0_SIN	I2C1_SDA	LPUART0_ TX	BSM_DATA		DTM_TX		
41	Ground	NA										

7.4 KW35A Pinouts

KW35A device pinouts are shown in the figures below.

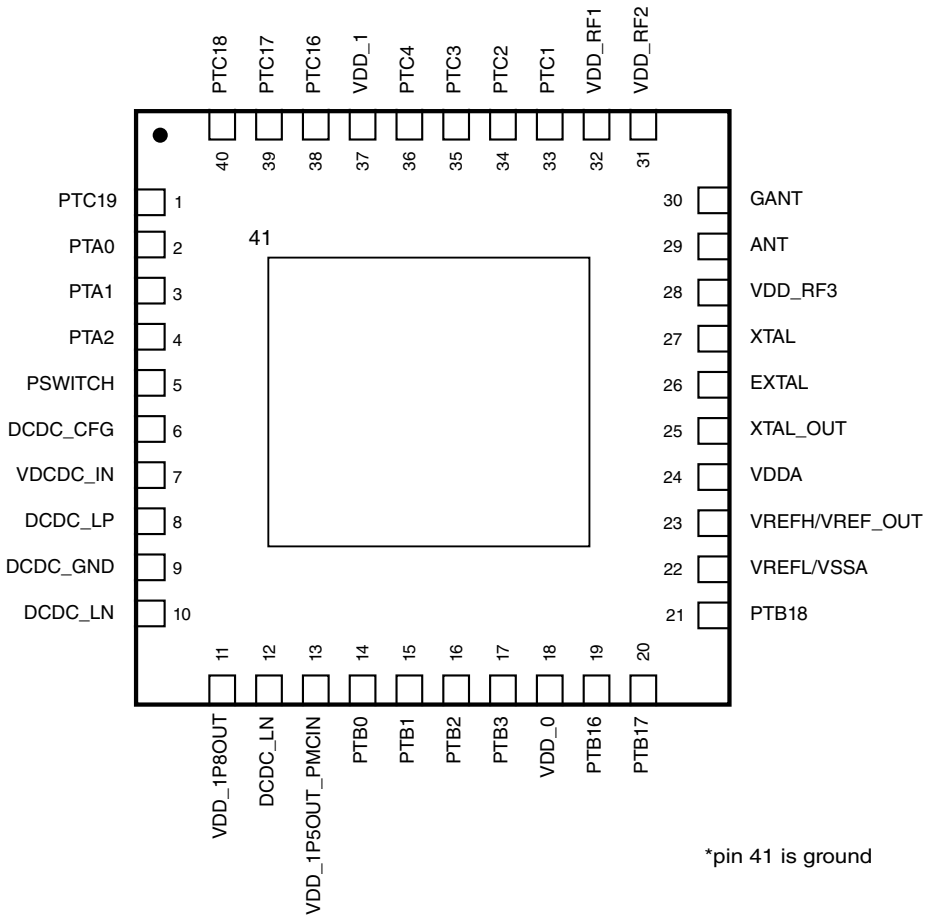


Figure 19. 40-pin "Wettable" QFN pinout diagram

7.5 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

7.5.1 Core Modules

This section contains tables describing the core module signal descriptions.

Table 47. SWD Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
SWD_DIO	SWD_DIO	Serial Wire Debug Data Input/Output[1]	I/O
SWD_CLK	SWD_CLK	Serial Wire Clock[2]	I

1. Pulled up internally by default
2. Pulled down internally by default

7.5.2 Radio Modules

This section contains tables describing the radio signals.

Table 48. Radio Module Signal Descriptions

Module Signal Name	Pin Direction	Pin Name	Pin Description
ANT	O	ANT	Antenna
BLE_RF_ACTIVE	O	BLE_RF_ACTIVE	An output which is asserted prior to any Radio event and remains asserted for the duration of the event.
BSM_CLK	O	BSM_CLK	Bit Streaming Mode (BSM) clock signal. 1 MHz bit rate clock. BSM_DATA and BSM_FRAME are synchronized to BSM_CLK. External device should capture BSM_FRAME and BSM_DATA on rising edge of BSM_CLK.
BSM_DATA	O	BSM_DATA	Serial BLE packet bit stream, LSB-first. Valid on rising edge of BSM_CLK.
BSM_FRAME	O	BSM_FRAME	Framing signal to indicate the start of reception. Active high.
DTM_RX	I	DTM_RX	Direct Test Mode Receive
DTM_TX	O	DTM_TX	Direct Test Mode Transmit
GANT	I	GANT	Antenna ground
RF_STATUS	O	RF_STATUS	An output which indicates when the Radio is in an RX or TX event; software can also control this signal directly.
RF_PRIORITY	O	RF_PRIORITY	An output which indicates to the external WiFi device that the Radio event is a high priority and it needs access to the 2.4GHz antenna.
RF_EARLY_WARNING	O	RF_EARLY_WARNING	BLE LL generated signal which can be used to wake an external sensor to make a measurement before a BLE event.
RF_NOT_ALLOWED	I	RF_NOT_ALLOWED	External signal which causes the internal Radio to cease radio activity.

Table continues on the next page...

Table 48. Radio Module Signal Descriptions (continued)

Module Signal Name	Pin Direction	Pin Name	Pin Description
RF_TX_CONF	I	RF_TX_CONF	Signal from an external Radio which indicates the availability of the 2.4GHz antenna to the internal Radio. **NOTE:** This is a GPIO, not a dedicated PIN.
RX_SWITCH	O	TX_SWITCH	Front End Module receive mode signal.
TX_SWITCH	O	TX_SWITCH	Front End Module transmit mode signal.

Table 49. Radio Module Miscellaneous Pin Descriptions

Pin Name	Pad Direction	Pin Name	Pin Description
RF_INT_OSC_EN	I	RF_RFOSC_EN	External request to turn on the Radio's internal RF oscillator.
RF_EXT_OSC_EN	O	RF_EXT_OSC_EN	Internal request to turn on an External oscillator for use by the internal Radio. The request can also be from the SoC if it is using the RF oscillator as its clock.

7.5.3 System Modules

This section contains tables describing the system signals.

Table 50. System Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
NMI_b	—	Non-maskable interrupt	I
RESET_b	—	Reset bidirectional signal	I/O
VDD_[1:0]	VDD	Power supply	I
Ground	VSS	Ground	I
VDD_RF[3:1]	VDD_RF	Radio power supply	I
VDCDC_IN	VDCDC_IN	VDCDC_IN	I
VDD_1P8OUT	VDD_1P8	DCDC 1.8 V Regulated Output / Input in bypass	I/O
VDD_1P5OUT_PMCIN	VDD_1P5/VDD_PMC	DCDC 1.5 V Regulated Output / PMC Input in bypass	I/O
PSWITCH	PSWITCH	DCDC enable switch	I
DCDC_CFG	DCDC_CFG	DCDC switch mode select	I
DCDC_LP	DCDC_LP	DCDC inductor input positive	I/O
DCDC_LN	DCDC_LN	DCDC inductor input negative	I/O
DCDC_GND	DCDC_GND	DCDC ground	I

Table 51. LLWU Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
LLWU_P[15:0]	LLWU_P[15:0]	Wakeup inputs	I

7.5.4 Clock Modules

This section contains tables for Clock signal descriptions.

Table 52. Clock Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
EXTAL	EXTAL	26 MHz/32 MHz External clock/Oscillator input	I
XTAL	XTAL	26 MHz/32 MHz Oscillator input	I
XTAL_OUT	XTAL_OUT	26 MHz/32 MHz Clock output	O
XTAL_OUT_EN	XTAL_OUT_ENABLE	26 MHz/32 MHz Clock output enable for XTAL_OUT	I
EXTAL32K	EXTAL32K	32 kHz External clock/ Oscillator input	I
XTAL32K	XTAL32K	32 kHz Oscillator input	I
CLKOUT	CLKOUT	Internal clocks monitor	O

7.5.5 Analog Modules

This section contains tables for Analog signal descriptions.

Table 53. ADC0 Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
ADC0_DM0	DADM0	ADC Channel 0 Differential Input Negative	I
ADC0_DP0	DADP0	ADC Channel 0 Differential Input Positive	I
ADC0_SE[5:1]	AD[5:1]	ADC Channel 0 Single-ended Input n	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VDDA	V_{DDA}	Analog Power Supply	I
VSSA	V_{SSA}	Analog Ground	I

Table 54. CMP0 Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
CMP0_IN[5:0]	IN[5:0]	Analog voltage inputs	I
CMP0_OUT	CMP0	Comparator output	O

Table 55. VREF Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
VREF_OUT	VREF_OUT	Internally generated voltage reference output	O

7.5.6 Timer Modules

This section contains tables describing timer module signals.

Table 56. TPM0 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock	I
TPM0_CH[3:0]	TPM_CH[3:0]	TPM channel	I/O

Table 57. TPM1 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock	I
TPM1_CH[1:0]	TPM_CH[1:0]	TPM channel	I/O

Table 58. TPM2 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock	I
TPM2_CH[1:0]	TPM_CH[1:0]	TPM channel	I/O

Table 59. LPTMR0 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
LPTMR0_ALT[2:1]	LPTMR0_ALT[2:1]	Pulse counter input pin	I

Table 60. RTC Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
RTC_CLKOUT	RTC_CLKOUT	1 Hz square-wave output	O

7.5.7 Communication Interfaces

This section contains tables for the signal descriptions for the communication modules.

Table 61. SPI0 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
SPI0_PCS0	PCS0/SS	Chip Select/Slave Select	I/O
SPI0_PCS[2:1]	PCS[2:1]	Chip Select	O
SPI0_SCK	SCK	Serial Clock	I/O
SPI0_SIN	SIN	Data In	I
SPI0_SOUT	SOUT	Data Out	O

Table 62. SPI1 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
SPI1_PCS0	SPI1_PCS0	Chip Select/Slave Select	I/O
SPI1_SCK	SCK	Serial Clock	I/O
SPI1_SIN	SIN	Data In	I
SPI1_SOUT	SOUT	Data Out	O

Table 63. I2C0 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
I2C0_SCL	SCL	I2C serial clock line	I/O
I2C0_SDA	SDA	I2C serial data line	I/O

Table 64. I2C1 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
I2C1_SCL	SCL	I2C serial clock line	I/O
I2C1_SDA	SDA	I2C serial data line	I/O

Table 65. CAN0 Signal Descriptions (KW36 only)

SoC Signal Name	Module Signal Name	Description	I/O
CAN0_RX	CAN RX	CAN Receive Pin	I
CAN0_TX	CAN TX	CAN Transmit Pin	O

Table 66. LPUART0 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
LPUART0_CTS_b	LPUART CTS	Clear To Send	I
LPUART0_RTS_b	LPUART RTS	Request To Send	O
LPUART0_RX	LPUART RxD	Receive Data	I
LPUART0_TX	LPUART TxD	Transmit Data[1]	I/O

1. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data

Table 67. LPUART1 Module Signal Descriptions (KW36 only)

SoC Signal Name	Module Signal Name	Description	I/O
LPUART1_CTS_b	LPUART CTS	Clear To Send	I
LPUART1_RTS_b	LPUART RTS	Request To Send	O
LPUART1_RX	LPUART RxD	Receive Data	I
LPUART1_TX	LPUART TxD	Transmit Data[1]	I/O

1. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data

7.5.8 Human-Machine Interfaces(HMI)

This section contains tables describing the HMI signals.

Table 68. GPIO Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
PTA[19:16][2:0]	PORTA19-16, 2-0	General Purpose Input/ Output	I/O
PTB[18:16][3:0]	PORTB18-16, 3-0	General Purpose Input/ Output	I/O
PTC[19:16][7:1]	PORTC19-16, 7-1	General Purpose Input/ Output	I/O

8 Package Information

8.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **nxp.com** and perform a keyword search for the drawing's document number:

Table 69. Packaging Dimensions

If you want the drawing for this package	Then use this document number
40-pin "Wettable" QFN (6x6)	98ASA01025D
48-pin LQFN (7x7)	98ASA00694D

9 Part identification

9.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

9.2 Format

Part numbers for this device have the following format:

Q KW## A FFF R T PP CC N

9.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 70. Part number fields descriptions

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KW##	Kinetis Wireless family	• KW35 • KW36
A	Key attribute	• A = Automotive Qualification
FFF	Program flash memory size	• 512 = 512 KB
R	Silicon revision	• A = AEC Q100 Grade 2 Automotive Qualified
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• HT = 48 LQFN (7 mm x 7 mm) • FP = 40 "Wettable" QFN (6 mm x 6 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
N	Packaging type	• (Blank) = Tray • R = Tape and reel

9.4 Example

This is an example part number:

MKW36A512VHT4

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Document Number MKW36A512
Revision 5, 07/2018

Preliminary