

S32SDK User Manual

S32K1xx RTM 4.0.2

Generated by Doxygen 1.8.10

Fri Jun 11 2021 08:16:50

Contents

1	S32 SDK	1
2	Components	2
3	PAL vs PD usage	4
4	Supported Platforms	4
5	Installation	4
6	Build Tools	5
7	IDE Support	6
8	Configuration	6
9	Acronyms and Abbreviations	7
10	MISRA Compliance	7
11	Development guidelines	7
12	Error detection and reporting	8
13	Notes - Please read	9
14	Examples and Demos	40
14.1	Introduction	40
14.2	Usage	41
14.2.1	How to build	41
14.2.2	How to debug	41
14.2.3	Using terminal emulator	42
14.3	Demo Applications	44
14.3.1	Hello World	45
14.3.2	Hello World - IAR Embedded Workbench	46
14.3.3	Hello World - Makefile	47
14.3.4	lwIP TCP/IP stack	48
14.3.5	FlexCAN Encrypted	50
14.3.6	CSEC BOOT PROTECTION	52
14.3.7	FreeMASTER	55
14.3.8	FreeRTOS	57
14.3.9	ADC Low Power	59
14.3.10	AMMCLib	61
14.3.11	LIN MASTER	64

14.3.12 LIN SLAVE	66
14.3.13 Structural Core Self Test Example	68
14.4 Driver Examples	70
14.4.1 Analog Driver Examples	70
14.4.2 ADC Hardware Trigger	71
14.4.3 ADC PAL example	72
14.4.4 ADC Software Trigger	75
14.4.5 CMP DAC	76
14.4.6 Communication Driver Examples	79
14.4.7 FLEXIO SPI	80
14.4.8 ENET Loopback	82
14.4.9 PHY TJA1101	83
14.4.10 LPUART Echo	85
14.4.11 UART PAL ECHO	87
14.4.12 CAN PAL	88
14.4.13 LPSPI Transfer	90
14.4.14 LPSPI DMA	92
14.4.15 SPI PAL	94
14.4.16 SAI Transfer	96
14.4.17 I2C PAL	97
14.4.18 I2S PAL MASTER	99
14.4.19 I2S PAL SLAVE	100
14.4.20 FLEXIO I2C	102
14.4.21 FLEXIO I2S MASTER	104
14.4.22 FLEXIO I2S SLAVE	106
14.4.23 FLEXIO UART	108
14.4.24 LPI2C MASTER	109
14.4.25 LPI2C SLAVE	111
14.4.26 LIN MASTER BAREMETAL	113
14.4.27 LIN SLAVE BAREMETAL	115
14.4.28 System Driver Examples	117
14.4.29 Trigger MUX Control	117
14.4.30 CRC Checksum	119
14.4.31 CSEc key configuration	121
14.4.32 EDMA transfer	123
14.4.33 EWM Interrupt	124
14.4.34 FLASH Partitioning	126
14.4.35 MPU Memory Protect Unit	128
14.4.36 MPU PAL Memory Protection	130
14.4.37 Power Mode Switch.	132

14.4.38 WDOG Interrupt	135
14.4.39 EIM INJECTION	136
14.4.40 ERM REPORT	138
14.4.41 WDG PAL Interrupt	139
14.4.42 External Flash over QuadSPI	141
14.4.43 SECURITY PAL	142
14.4.44 Timer Driver Examples	144
14.4.45 FTM Combined PWM	145
14.4.46 FTM Periodic Interrupt	146
14.4.47 FTM PWM	148
14.4.48 FTM Signal Measurement	150
14.4.49 IC PAL	152
14.4.50 LPTMR Periodic Interrupt	155
14.4.51 LPTMR Pulse Counter	157
14.4.52 PDB Periodic Interrupt	158
14.4.53 RTC Alarm	160
14.4.54 TIMING PAL	162
14.4.55 PWM PAL	163
14.4.56 OC PAL	165
14.4.57 LPIT Periodic Interrupt	166
15 Module Index	167
15.1 Modules	167
16 Data Structure Index	172
16.1 Data Structures	172
17 Module Documentation	178
17.1 00. Library internals	178
17.1.1 Detailed Description	178
17.1.2 Internals	178
17.1.3 Data Structure Documentation	181
17.1.4 Enumeration Type Documentation	186
17.1.5 Function Documentation	187
17.1.6 Variable Documentation	188
17.2 01. CAN & CAN partial networking configuration	189
17.2.1 Detailed Description	189
17.2.2 Introduction	189
17.2.3 Data Structure Documentation	190
17.2.4 Typedef Documentation	193
17.2.5 Enumeration Type Documentation	194

17.2.6	Function Documentation	195
17.3	01. Mode handling	198
17.3.1	Detailed Description	198
17.3.2	Introduction	198
17.3.3	Enumeration Type Documentation	198
17.3.4	Function Documentation	199
17.4	01. Primary control	200
17.4.1	Detailed Description	200
17.5	01. Regulator configuration	201
17.5.1	Detailed Description	201
17.5.2	Introduction	201
17.5.3	Data Structure Documentation	201
17.5.4	Enumeration Type Documentation	202
17.5.5	Function Documentation	203
17.6	02. Battery monitor configuration	204
17.6.1	Detailed Description	204
17.6.2	Introduction	204
17.6.3	Data Structure Documentation	204
17.6.4	Typedef Documentation	206
17.6.5	Enumeration Type Documentation	206
17.6.6	Function Documentation	207
17.7	02. LIN configuration	208
17.7.1	Detailed Description	208
17.7.2	Introduction	208
17.7.3	Data Structure Documentation	208
17.7.4	Enumeration Type Documentation	209
17.7.5	Function Documentation	210
17.8	02. Supply control	212
17.8.1	Detailed Description	212
17.9	02. Watchdog	213
17.9.1	Detailed Description	213
17.9.2	Introduction	213
17.9.3	Data Structure Documentation	214
17.9.4	Enumeration Type Documentation	214
17.9.5	Function Documentation	215
17.10	03. Fail-safe configuration	217
17.10.1	Detailed Description	217
17.10.2	Introduction	217
17.10.3	Data Structure Documentation	218
17.10.4	Typedef Documentation	219

17.10.5 Enumeration Type Documentation	219
17.10.6 Function Documentation	220
17.1103. SMPS configuration	221
17.11.1 Detailed Description	221
17.11.2 Introduction	221
17.11.3 Data Structure Documentation	221
17.11.4 Typedef Documentation	222
17.11.5 Enumeration Type Documentation	222
17.11.6 Function Documentation	223
17.1203. Transceiver control	224
17.12.1 Detailed Description	224
17.1304. HVIO bank 0 & 1 control	225
17.13.1 Detailed Description	225
17.13.2 Introduction	225
17.13.3 Data Structure Documentation	226
17.13.4 Typedef Documentation	228
17.13.5 Enumeration Type Documentation	228
17.13.6 Function Documentation	229
17.1404. Lock control	232
17.14.1 Detailed Description	232
17.14.2 Introduction	232
17.14.3 Data Structure Documentation	232
17.14.4 Typedef Documentation	234
17.14.5 Function Documentation	234
17.1505. Timer control	235
17.15.1 Detailed Description	235
17.15.2 Introduction	235
17.15.3 Data Structure Documentation	235
17.15.4 Typedef Documentation	236
17.15.5 Enumeration Type Documentation	236
17.15.6 Function Documentation	237
17.1606. Interrupts	239
17.16.1 Detailed Description	239
17.16.2 Introduction	239
17.16.3 Function Documentation	239
17.1707. MTPNV and ID	243
17.17.1 Detailed Description	243
17.17.2 Introduction	243
17.17.3 Data Structure Documentation	246
17.17.4 Function Documentation	248

17.18ADC Driver	250
17.18.1 Detailed Description	250
17.18.2 Data Structure Documentation	255
17.18.3 Enumeration Type Documentation	258
17.18.4 Function Documentation	262
17.19Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL)	268
17.19.1 Detailed Description	268
17.19.2 Data Structure Documentation	273
17.19.3 Typedef Documentation	276
17.19.4 Enumeration Type Documentation	276
17.19.5 Function Documentation	276
17.20Automotive Math and Motor Control Library	281
17.21Backward Compatibility Symbols for S32K148	282
17.22Bank N fail interrupt enable configuration options (0x38/0x48)	283
17.22.1 Detailed Description	283
17.22.2 Macro Definition Documentation	284
17.23Bank N wake-up interrupt enable configuration options (0x37/0x47)	286
17.23.1 Detailed Description	286
17.23.2 Macro Definition Documentation	287
17.24CRC Driver	289
17.24.1 Detailed Description	289
17.24.2 Data Structure Documentation	289
17.24.3 Enumeration Type Documentation	290
17.24.4 Function Documentation	290
17.25CSEc Driver	294
17.25.1 Detailed Description	294
17.25.2 Data Structure Documentation	299
17.25.3 Macro Definition Documentation	301
17.25.4 Typedef Documentation	302
17.25.5 Enumeration Type Documentation	302
17.25.6 Function Documentation	304
17.26Clock	315
17.26.1 Detailed Description	315
17.26.2 Function Documentation	315
17.27Clock Manager	316
17.27.1 Detailed Description	316
17.28Clock Manager Driver	317
17.28.1 Detailed Description	317
17.28.2 Data Structure Documentation	323
17.28.3 Macro Definition Documentation	341

17.28.4 Typedef Documentation	342
17.28.5 Enumeration Type Documentation	342
17.28.6 Function Documentation	349
17.28.7 Variable Documentation	354
17.29 Common Core API	355
17.29.1 Detailed Description	355
17.29.2 Macro Definition Documentation	355
17.30 Common Transport Layer API	357
17.30.1 Detailed Description	357
17.30.2 Macro Definition Documentation	357
17.30.3 Function Documentation	360
17.31 Comparator (CMP)	361
17.31.1 Detailed Description	361
17.32 Comparator Driver	365
17.32.1 Detailed Description	365
17.32.2 Data Structure Documentation	367
17.32.3 Macro Definition Documentation	371
17.32.4 Typedef Documentation	371
17.32.5 Enumeration Type Documentation	371
17.32.6 Function Documentation	374
17.33 Controller Area Network - Peripheral Abstraction Layer (CAN PAL)	381
17.33.1 Detailed Description	381
17.33.2 Data Structure Documentation	386
17.33.3 Enumeration Type Documentation	390
17.33.4 Function Documentation	391
17.34 Controller Area Network with Flexible Data Rate (FlexCAN)	398
17.34.1 Detailed Description	398
17.35 Cooked API	400
17.35.1 Detailed Description	400
17.35.2 Function Documentation	400
17.36 Cryptographic Services Engine (CSEc)	402
17.36.1 Detailed Description	402
17.37 Cyclic Redundancy Check (CRC)	403
17.37.1 Detailed Description	403
17.38 Diagnostic services	405
17.38.1 Detailed Description	405
17.38.2 Function Documentation	406
17.39 Driver and cluster management	409
17.39.1 Detailed Description	409
17.39.2 Function Documentation	409

17.40EDMA Driver	410
17.40.1 Detailed Description	410
17.40.2 Data Structure Documentation	415
17.40.3 Macro Definition Documentation	422
17.40.4 Typedef Documentation	422
17.40.5 Enumeration Type Documentation	422
17.40.6 Function Documentation	425
17.41EIM Driver	435
17.41.1 Detailed Description	435
17.41.2 Data Structure Documentation	437
17.41.3 Macro Definition Documentation	437
17.41.4 Function Documentation	438
17.42ENET Driver	440
17.42.1 Detailed Description	440
17.42.2 Data Structure Documentation	446
17.42.3 Macro Definition Documentation	451
17.42.4 Typedef Documentation	453
17.42.5 Enumeration Type Documentation	453
17.42.6 Function Documentation	456
17.43ERM Driver	463
17.43.1 Detailed Description	463
17.43.2 ERM Driver Initialization	463
17.43.3 ERM Driver Operation	463
17.43.4 Data Structure Documentation	465
17.43.5 Enumeration Type Documentation	466
17.43.6 Function Documentation	466
17.44EWM Driver	468
17.44.1 Detailed Description	468
17.44.2 Data Structure Documentation	470
17.44.3 Enumeration Type Documentation	471
17.44.4 Function Documentation	471
17.45Enhanced Direct Memory Access (eDMA)	473
17.45.1 Detailed Description	473
17.46Error Injection Module (EIM)	474
17.46.1 Detailed Description	474
17.47Error Reporting Module (ERM)	476
17.47.1 Detailed Description	476
17.48Ethernet MAC (ENET)	478
17.48.1 Detailed Description	478
17.49Ethernet Transceiver (PHY)	481

17.49.1 Detailed Description	481
17.50 External Watchdog Monitor (EWM)	482
17.50.1 Detailed Description	482
17.51 Flash Memory (Flash)	483
17.51.1 Detailed Description	483
17.51.2 Data Structure Documentation	486
17.51.3 Macro Definition Documentation	487
17.51.4 Typedef Documentation	491
17.51.5 Enumeration Type Documentation	491
17.51.6 Function Documentation	491
17.51.7 Variable Documentation	500
17.52 Flash Memory (Flash)	503
17.52.1 Detailed Description	503
17.53 FlexCAN Driver	506
17.53.1 Detailed Description	506
17.53.2 Data Structure Documentation	512
17.53.3 Typedef Documentation	517
17.53.4 Enumeration Type Documentation	517
17.53.5 Function Documentation	520
17.54 FlexIO Common Driver	528
17.54.1 Detailed Description	528
17.54.2 Enumeration Type Documentation	528
17.54.3 Function Documentation	528
17.55 FlexIO I2C Driver	531
17.55.1 Detailed Description	531
17.55.2 Data Structure Documentation	534
17.55.3 Function Documentation	535
17.56 FlexIO I2S Driver	540
17.56.1 Detailed Description	540
17.56.2 Data Structure Documentation	543
17.56.3 Typedef Documentation	546
17.56.4 Function Documentation	546
17.57 FlexIO SPI Driver	558
17.57.1 Detailed Description	558
17.57.2 Data Structure Documentation	561
17.57.3 Typedef Documentation	564
17.57.4 Enumeration Type Documentation	565
17.57.5 Function Documentation	565
17.58 FlexIO UART Driver	572
17.58.1 Detailed Description	572

17.58.2 Data Structure Documentation	574
17.58.3 Enumeration Type Documentation	576
17.58.4 Function Documentation	576
17.59 FlexTimer (FTM)	581
17.59.1 Detailed Description	581
17.59.2 Data Structure Documentation	587
17.59.3 Macro Definition Documentation	591
17.59.4 Enumeration Type Documentation	594
17.59.5 Function Documentation	596
17.59.6 Variable Documentation	618
17.60 FlexTimer Input Capture Driver (FTM_IC)	619
17.60.1 Detailed Description	619
17.60.2 Data Structure Documentation	621
17.60.3 Enumeration Type Documentation	623
17.60.4 Function Documentation	624
17.61 FlexTimer Module Counter Driver (FTM_MC)	627
17.61.1 Detailed Description	627
17.61.2 Data Structure Documentation	628
17.61.3 Function Documentation	629
17.62 FlexTimer Output Compare Driver (FTM_OC)	631
17.62.1 Detailed Description	631
17.62.2 Data Structure Documentation	633
17.62.3 Enumeration Type Documentation	634
17.62.4 Function Documentation	634
17.63 FlexTimer Pulse Width Modulation Driver (FTM_PWM)	637
17.63.1 Detailed Description	637
17.63.2 Data Structure Documentation	644
17.63.3 Macro Definition Documentation	649
17.63.4 Enumeration Type Documentation	649
17.63.5 Function Documentation	650
17.64 FlexTimer Quadrature Decoder Driver (FTM_QD)	654
17.64.1 Detailed Description	654
17.64.2 Data Structure Documentation	656
17.64.3 Enumeration Type Documentation	657
17.64.4 Function Documentation	658
17.65 Flexible I/O (FlexIO)	660
17.65.1 Detailed Description	660
17.66 FreeRTOS	661
17.67 Generic PHY	662
17.67.1 Detailed Description	662

17.67.2 Macro Definition Documentation	663
17.67.3 Function Documentation	665
17.67.4 Variable Documentation	666
17.68HVIO high-side configuration options (0x71)	668
17.68.1 Detailed Description	668
17.68.2 Macro Definition Documentation	669
17.69HVIO low-side configuration options (0x72)	671
17.69.1 Detailed Description	671
17.69.2 Macro Definition Documentation	672
17.70I2S - Peripheral Abstraction Layer (I2S PAL)	674
17.70.1 Detailed Description	674
17.70.2 Data Structure Documentation	676
17.70.3 Enumeration Type Documentation	678
17.70.4 Function Documentation	678
17.71 Initialization	682
17.71.1 Detailed Description	682
17.71.2 Function Documentation	682
17.72Input Capture - Peripheral Abstraction Layer (IC PAL)	683
17.72.1 Detailed Description	683
17.72.2 Data Structure Documentation	687
17.72.3 Enumeration Type Documentation	689
17.72.4 Function Documentation	689
17.73Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL)	692
17.73.1 Detailed Description	692
17.73.2 Data Structure Documentation	696
17.73.3 Enumeration Type Documentation	699
17.73.4 Function Documentation	699
17.74Interface management	707
17.74.1 Detailed Description	707
17.74.2 Function Documentation	707
17.75Interrupt Manager (Interrupt)	709
17.75.1 Detailed Description	709
17.75.2 Typedef Documentation	710
17.75.3 Function Documentation	710
17.76Interrupt vector numbers for S32K148	714
17.77J2602 Specific API	715
17.78J2602 Transport Layer specific API	716
17.78.1 Detailed Description	716
17.79LIN 2.1 Specific API	717
17.79.1 Detailed Description	717

17.79.2 Function Documentation	717
17.80 LIN Core API	719
17.80.1 Detailed Description	719
17.81 LIN Driver	720
17.81.1 Detailed Description	720
17.81.2 LIN Driver Overview	720
17.81.3 LIN Driver Device structures	720
17.81.4 LIN Driver Initialization	721
17.81.5 LIN Data Transfers	722
17.81.6 Autobaud feature	722
17.81.7 Data Structure Documentation	725
17.81.8 Macro Definition Documentation	729
17.81.9 Typedef Documentation	729
17.81.10 Enumeration Type Documentation	729
17.81.11 Function Documentation	730
17.81.12 Variable Documentation	738
17.82 LIN Stack	739
17.82.1 Detailed Description	739
17.83 I2C Driver	742
17.83.1 Detailed Description	742
17.83.2 Data Structure Documentation	745
17.83.3 Enumeration Type Documentation	748
17.83.4 Function Documentation	748
17.84 I2T Driver	758
17.84.1 Detailed Description	758
17.84.2 Data Structure Documentation	762
17.84.3 Macro Definition Documentation	763
17.84.4 Enumeration Type Documentation	764
17.84.5 Function Documentation	764
17.85 I2SPI Driver	773
17.85.1 Detailed Description	773
17.85.2 Data Structure Documentation	775
17.85.3 Enumeration Type Documentation	781
17.85.4 Function Documentation	782
17.85.5 Variable Documentation	790
17.86 I2TMR Driver	791
17.86.1 Detailed Description	791
17.86.2 Data Structure Documentation	794
17.86.3 Enumeration Type Documentation	795
17.86.4 Function Documentation	797

17.87LPUART Driver	801
17.87.1 Detailed Description	801
17.87.2 Data Structure Documentation	804
17.87.3 Enumeration Type Documentation	808
17.87.4 Function Documentation	808
17.88Local Interconnect Network (LIN)	816
17.88.1 Detailed Description	816
17.89Low Power Inter-Integrated Circuit (LPI2C)	817
17.89.1 Detailed Description	817
17.90Low Power Interrupt Timer (LPIT)	818
17.90.1 Detailed Description	818
17.91Low Power Serial Peripheral Interface (LPSPI)	819
17.91.1 Detailed Description	819
17.92Low Power Timer (LPTMR)	822
17.92.1 Detailed Description	822
17.93Low Power Universal Asynchronous Receiver-Transmitter (LPUART)	823
17.93.1 Detailed Description	823
17.94Low level API	824
17.94.1 Detailed Description	824
17.94.2 Data Structure Documentation	827
17.94.3 Macro Definition Documentation	843
17.94.4 Typedef Documentation	845
17.94.5 Enumeration Type Documentation	845
17.94.6 Function Documentation	850
17.94.7 Variable Documentation	854
17.95MPU Driver	856
17.95.1 Detailed Description	856
17.95.2 Data Structure Documentation	861
17.95.3 Enumeration Type Documentation	863
17.95.4 Function Documentation	867
17.96MPU PAL	870
17.96.1 Detailed Description	870
17.96.2 Data Structure Documentation	873
17.96.3 Typedef Documentation	875
17.96.4 Enumeration Type Documentation	877
17.96.5 Function Documentation	878
17.97MX25L6433F Serial Flash Driver	881
17.97.1 Detailed Description	881
17.97.2 Data Structure Documentation	885
17.97.3 Enumeration Type Documentation	886

17.97.4 Function Documentation	886
17.98 Memory Protection Unit (MPU)	893
17.98.1 Detailed Description	893
17.99 Memory Protection Unit Peripheral Abstraction Layer (MPU PAL)	895
17.99.1 Detailed Description	895
17.100 Node configuration	900
17.100.1 Detailed Description	900
17.100.2 Function Documentation	900
17.101 Node configuration	905
17.101.1 Detailed Description	905
17.101.2 Function Documentation	905
17.102 Node identification	907
17.102.1 Detailed Description	907
17.102.2 Function Documentation	907
17.103 Notification	908
17.104 OS Interface (OSIF)	909
17.104.1 Detailed Description	909
17.104.2 Macro Definition Documentation	911
17.104.3 Function Documentation	911
17.105 Output Compare - Peripheral Abstraction Layer (OC PAL)	918
17.105.1 Detailed Description	918
17.105.2 Data Structure Documentation	921
17.105.3 Enumeration Type Documentation	923
17.105.4 Function Documentation	924
17.106 I2C Driver	929
17.106.1 Detailed Description	929
17.106.2 Data Structure Documentation	933
17.106.3 Enumeration Type Documentation	934
17.106.4 Function Documentation	935
17.107 PHY Framework	941
17.107.1 Detailed Description	941
17.107.2 Data Structure Documentation	945
17.107.3 Enumeration Type Documentation	950
17.107.4 Function Documentation	951
17.107.5 Variable Documentation	957
17.108 I2S Driver	958
17.108.1 Detailed Description	958
17.108.2 Data Structure Documentation	958
17.108.3 Typedef Documentation	959
17.108.4 Enumeration Type Documentation	959

17.108.5Function Documentation	960
17.109Peripheral access layer for S32K148	963
17.110Pins Driver (PINS)	964
17.110.1Detailed Description	964
17.111Power Manager	966
17.111.1Detailed Description	966
17.111.2Data Structure Documentation	967
17.111.3Typedef Documentation	969
17.111.4Enumeration Type Documentation	970
17.111.5Function Documentation	971
17.111.6Variable Documentation	975
17.112Power Manager Driver	976
17.113Power_s32k1xx	978
17.113.1Detailed Description	978
17.113.2Data Structure Documentation	979
17.113.3Enumeration Type Documentation	980
17.113.4Function Documentation	982
17.114Programmable Delay Block (PDB)	984
17.114.1Detailed Description	984
17.115Pulse-width modulation - Peripheral Abstraction Layer (PWM PAL)	985
17.115.1Detailed Description	985
17.115.2Data Structure Documentation	988
17.115.3Enumeration Type Documentation	990
17.115.4Function Documentation	990
17.116Quad Serial Peripheral Interface (QuadSPI)	994
17.116.1Detailed Description	994
17.117QuadSPI Driver	995
17.117.1Detailed Description	995
17.117.2Macro Definition Documentation	997
17.117.3Typedef Documentation	997
17.117.4Enumeration Type Documentation	997
17.117.5Variable Documentation	998
17.118RTC Driver	999
17.118.1Detailed Description	999
17.118.2Data Structure Documentation	1001
17.118.3Macro Definition Documentation	1005
17.118.4Enumeration Type Documentation	1006
17.118.5Function Documentation	1007
17.119Raw API	1014
17.119.1Detailed Description	1014

17.119.2	Function Documentation	1014
17.120	Real Time Clock Driver (RTC)	1016
17.120.1	Detailed Description	1016
17.120.2	Register address map	1020
17.121.1	Detailed Description	1020
17.121.2	Macro Definition Documentation	1024
17.122	S32K148 SoC Header file	1033
17.122.1	Detailed Description	1033
17.123	S32K148 System Files	1034
17.124	SAI Driver	1035
17.124.1	Detailed Description	1035
17.124.2	Data Structure Documentation	1038
17.124.3	Macro Definition Documentation	1041
17.124.4	typedef Documentation	1041
17.124.5	Enumeration Type Documentation	1042
17.124.6	Function Documentation	1043
17.125	SBC FS45 Driver	1048
17.125.1	Detailed Description	1048
17.125.2	Data Structure Documentation	1051
17.125.3	Enumeration Type Documentation	1063
17.125.4	Function Documentation	1066
17.126	SBC configuration control options (0x74)	1076
17.126.1	Detailed Description	1076
17.126.2	Macro Definition Documentation	1077
17.127	Schedule management	1079
17.127.1	Detailed Description	1079
17.127.2	Function Documentation	1079
17.128	Security PAL	1080
17.128.1	Detailed Description	1080
17.128.2	Data Structure Documentation	1082
17.128.3	Enumeration Type Documentation	1082
17.128.4	Function Documentation	1084
17.129	Security Peripheral Abstraction Layer - SECURITY PAL	1098
17.129.1	Detailed Description	1098
17.130	Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL)	1101
17.130.1	Detailed Description	1101
17.130.2	Data Structure Documentation	1104
17.130.3	Enumeration Type Documentation	1107
17.130.4	Function Documentation	1108
17.131	Signal interaction	1113

17.13	SoC Header file (SoC Header)	1114
17.132	Detailed Description	1114
17.133	SoC Support	1115
17.133	Detailed Description	1115
17.134	Start-up control configuration options (0x73)	1117
17.134	Detailed Description	1117
17.134	Macro Definition Documentation	1118
17.135	Structural Core Self Test	1120
17.136	Supply interrupt enable configuration options (0x1C)	1122
17.136	Detailed Description	1122
17.136	Macro Definition Documentation	1123
17.137	Synchronous Audio Interface (SAI)	1125
17.137	Detailed Description	1125
17.138	System Basis Chip Driver (SBC) - FS45xx Family	1126
17.138	Detailed Description	1126
17.139	System Basis Chip Driver (SBC) - UJA116xA Family	1129
17.139	Detailed Description	1129
17.140	System Basis Chip library (SBC) - UJA113x Family	1134
17.140	Detailed Description	1134
17.140	Introduction	1134
17.141	System interrupt enable configuration options (0x04)	1135
17.141	Detailed Description	1135
17.141	Macro Definition Documentation	1135
17.142	UJA110x PHY	1136
17.142	Detailed Description	1136
17.142	Data Structure Documentation	1138
17.142	Macro Definition Documentation	1140
17.142	Enumeration Type Documentation	1144
17.142	Function Documentation	1144
17.142	Variable Documentation	1146
17.143	TRGMUX Driver	1147
17.143	Detailed Description	1147
17.143	Data Structure Documentation	1148
17.143	Typedef Documentation	1149
17.143	Function Documentation	1150
17.144	Timing - Peripheral Abstraction Layer (TIMING PAL)	1154
17.144	Detailed Description	1154
17.144	Data Structure Documentation	1158
17.144	Enumeration Type Documentation	1161
17.144	Function Documentation	1161

17.145	Transceiver interrupt enable configuration options (0x23)	1165
17.145.1	Detailed Description	1165
17.145.2	Macro Definition Documentation	1166
17.146	Transport layer API	1167
17.146.1	Detailed Description	1167
17.147	UJA116xA SBC Driver	1168
17.147.1	Detailed Description	1168
17.147.2	Data Structure Documentation	1175
17.147.3	Macro Definition Documentation	1191
17.147.4	Typedef Documentation	1191
17.147.5	Enumeration Type Documentation	1192
17.148	Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL)	1209
17.148.1	Detailed Description	1209
17.148.2	Data Structure Documentation	1214
17.148.3	Enumeration Type Documentation	1215
17.148.4	Function Documentation	1216
17.149	User provided call-outs	1222
17.149.1	Detailed Description	1222
17.149.2	Function Documentation	1222
17.150	WDG PAL	1223
17.150.1	Detailed Description	1223
17.150.2	Data Structure Documentation	1224
17.150.3	Enumeration Type Documentation	1225
17.150.4	Function Documentation	1226
17.151	WDOG Driver	1230
17.151.1	Detailed Description	1230
17.151.2	Data Structure Documentation	1233
17.151.3	Enumeration Type Documentation	1234
17.151.4	Function Documentation	1235
17.152	Watchdog Peripheral Abstraction Layer (WDG PAL)	1239
17.152.1	Detailed Description	1239
17.153	Watchdog timer (WDOG)	1242
17.153.1	Detailed Description	1242
18	Data Structure Documentation	1243
18.1	__blake2b_param Struct Reference	1243
18.1.1	Detailed Description	1243
18.1.2	Field Documentation	1243
18.2	__blake2bp_state Struct Reference	1244
18.2.1	Detailed Description	1244

18.2.2	Field Documentation	1244
18.3	__blake2s_param Struct Reference	1244
18.3.1	Detailed Description	1245
18.3.2	Field Documentation	1245
18.4	__blake2sp_state Struct Reference	1246
18.4.1	Detailed Description	1246
18.4.2	Field Documentation	1246
18.5	adc_callback_info_t Struct Reference	1246
18.5.1	Detailed Description	1246
18.5.2	Field Documentation	1247
18.6	adc_instance_t Struct Reference	1247
18.6.1	Detailed Description	1247
18.6.2	Field Documentation	1247
18.7	Aes Struct Reference	1247
18.7.1	Detailed Description	1248
18.7.2	Field Documentation	1248
18.8	Arc4 Struct Reference	1248
18.8.1	Detailed Description	1248
18.8.2	Field Documentation	1249
18.9	Arrays Struct Reference	1249
18.9.1	Detailed Description	1249
18.9.2	Field Documentation	1249
18.10	Base_entry Struct Reference	1250
18.10.1	Detailed Description	1251
18.10.2	Field Documentation	1251
18.11	Buffers Struct Reference	1251
18.11.1	Detailed Description	1252
18.11.2	Field Documentation	1252
18.12	bufferStatic Struct Reference	1253
18.12.1	Detailed Description	1254
18.12.2	Field Documentation	1254
18.13	BuildMsgArgs Struct Reference	1254
18.13.1	Detailed Description	1254
18.13.2	Field Documentation	1255
18.14	callback_functions Struct Reference	1255
18.14.1	Detailed Description	1255
18.14.2	Field Documentation	1255
18.15	can_instance_t Struct Reference	1256
18.15.1	Detailed Description	1256
18.15.2	Field Documentation	1256

18.16CertSignCtx Struct Reference	1256
18.16.1 Detailed Description	1257
18.16.2 Field Documentation	1257
18.17Ciphers Struct Reference	1257
18.17.1 Detailed Description	1257
18.17.2 Field Documentation	1258
18.18CipherSpecs Struct Reference	1258
18.18.1 Detailed Description	1258
18.18.2 Field Documentation	1258
18.19ClientRow Struct Reference	1259
18.19.1 Detailed Description	1259
18.19.2 Field Documentation	1260
18.20ClientSession Struct Reference	1260
18.20.1 Detailed Description	1260
18.20.2 Field Documentation	1260
18.21CRL_Entry Struct Reference	1260
18.21.1 Detailed Description	1261
18.21.2 Field Documentation	1261
18.22CRL_Monitor Struct Reference	1262
18.22.1 Detailed Description	1262
18.22.2 Field Documentation	1262
18.23DckeArgs Struct Reference	1262
18.23.1 Detailed Description	1263
18.23.2 Field Documentation	1263
18.24DcvArgs Struct Reference	1263
18.24.1 Detailed Description	1263
18.24.2 Field Documentation	1263
18.25DecodedCert Struct Reference	1264
18.25.1 Detailed Description	1265
18.25.2 Field Documentation	1265
18.26DecodedName Struct Reference	1269
18.26.1 Detailed Description	1270
18.26.2 Field Documentation	1270
18.27DerBuffer Struct Reference	1272
18.27.1 Detailed Description	1272
18.27.2 Field Documentation	1272
18.28Des Struct Reference	1272
18.28.1 Detailed Description	1272
18.28.2 Field Documentation	1273
18.29Des3 Struct Reference	1273

18.29.1 Detailed Description	1273
18.29.2 Field Documentation	1273
18.30DhKey Struct Reference	1274
18.30.1 Detailed Description	1274
18.30.2 Field Documentation	1274
18.31DhParams Struct Reference	1274
18.31.1 Detailed Description	1274
18.31.2 Field Documentation	1274
18.32DNS_entry Struct Reference	1275
18.32.1 Detailed Description	1275
18.32.2 Field Documentation	1275
18.33drv_config_t Struct Reference	1275
18.33.1 Detailed Description	1275
18.33.2 Field Documentation	1276
18.34DsaKey Struct Reference	1276
18.34.1 Detailed Description	1276
18.34.2 Field Documentation	1276
18.35DskeArgs Struct Reference	1277
18.35.1 Detailed Description	1277
18.35.2 Field Documentation	1277
18.36DtIsFrag Struct Reference	1278
18.36.1 Detailed Description	1278
18.36.2 Field Documentation	1278
18.37DtIsHandShakeHeader Struct Reference	1278
18.37.1 Detailed Description	1278
18.37.2 Field Documentation	1279
18.38DtIsMsg Struct Reference	1279
18.38.1 Detailed Description	1279
18.38.2 Field Documentation	1279
18.39DtIsRecordLayerHeader Struct Reference	1280
18.39.1 Detailed Description	1280
18.39.2 Field Documentation	1280
18.40EncryptedInfo Struct Reference	1281
18.40.1 Detailed Description	1281
18.40.2 Field Documentation	1281
18.41fp_int Struct Reference	1282
18.41.1 Detailed Description	1282
18.41.2 Field Documentation	1282
18.42fs45_tx_data_t Struct Reference	1282
18.42.1 Detailed Description	1282

18.42.2 Field Documentation	1283
18.43func_args Struct Reference	1283
18.43.1 Detailed Description	1283
18.43.2 Field Documentation	1283
18.44HandShakeHeader Struct Reference	1284
18.44.1 Detailed Description	1284
18.44.2 Field Documentation	1284
18.45handShakeInfo_st Struct Reference	1284
18.45.1 Detailed Description	1284
18.45.2 Field Documentation	1285
18.46Hash Union Reference	1285
18.46.1 Detailed Description	1285
18.46.2 Field Documentation	1285
18.47Hashes Struct Reference	1286
18.47.1 Detailed Description	1286
18.47.2 Field Documentation	1286
18.48HC128 Struct Reference	1286
18.48.1 Detailed Description	1286
18.48.2 Field Documentation	1286
18.49Hmac Struct Reference	1287
18.49.1 Detailed Description	1287
18.49.2 Field Documentation	1287
18.50HS_Hashes Struct Reference	1288
18.50.1 Detailed Description	1288
18.50.2 Field Documentation	1288
18.51i2c_instance_t Struct Reference	1289
18.51.1 Detailed Description	1289
18.51.2 Field Documentation	1289
18.52i2s_instance_t Struct Reference	1289
18.52.1 Detailed Description	1289
18.52.2 Field Documentation	1290
18.53ic_instance_t Struct Reference	1290
18.53.1 Detailed Description	1290
18.53.2 Field Documentation	1290
18.54Keys Struct Reference	1290
18.54.1 Detailed Description	1291
18.54.2 Field Documentation	1291
18.55lin_product_id_t Struct Reference	1292
18.55.1 Detailed Description	1292
18.55.2 Field Documentation	1292

18.56Md4 Struct Reference	1293
18.56.1 Detailed Description	1293
18.56.2 Field Documentation	1293
18.57Md5 Struct Reference	1293
18.57.1 Detailed Description	1294
18.57.2 Field Documentation	1294
18.58mp_int Struct Reference	1294
18.58.1 Detailed Description	1294
18.58.2 Field Documentation	1295
18.59mpu_instance_t Struct Reference	1295
18.59.1 Detailed Description	1295
18.59.2 Field Documentation	1295
18.60MsgsReceived Struct Reference	1296
18.60.1 Detailed Description	1296
18.60.2 Field Documentation	1296
18.61oc_instance_t Struct Reference	1297
18.61.1 Detailed Description	1298
18.61.2 Field Documentation	1298
18.62oc_pal_state_t Struct Reference	1298
18.62.1 Detailed Description	1298
18.63OcspEntry Struct Reference	1298
18.63.1 Detailed Description	1299
18.63.2 Field Documentation	1299
18.64Options Struct Reference	1299
18.64.1 Detailed Description	1300
18.64.2 Field Documentation	1300
18.65OS_Seed Struct Reference	1305
18.65.1 Detailed Description	1305
18.65.2 Field Documentation	1305
18.66packetInfo_st Struct Reference	1305
18.66.1 Detailed Description	1305
18.66.2 Field Documentation	1305
18.67phy_basicStatus_t Struct Reference	1306
18.67.1 Detailed Description	1306
18.67.2 Field Documentation	1306
18.68ProcPeerCertArgs Struct Reference	1307
18.68.1 Detailed Description	1307
18.68.2 Field Documentation	1307
18.69ProtocolVersion Struct Reference	1308
18.69.1 Detailed Description	1308

18.69.2 Field Documentation	1308
18.70pwm_instance_t Struct Reference	1309
18.70.1 Detailed Description	1309
18.70.2 Field Documentation	1309
18.71qspi_ahb_config_t Struct Reference	1309
18.71.1 Detailed Description	1310
18.71.2 Field Documentation	1310
18.72qspi_state_t Struct Reference	1310
18.72.1 Detailed Description	1310
18.73qspi_user_config_t Struct Reference	1311
18.73.1 Detailed Description	1311
18.73.2 Field Documentation	1311
18.74Rabbit Struct Reference	1313
18.74.1 Detailed Description	1314
18.74.2 Field Documentation	1314
18.75RabbitCtx Struct Reference	1314
18.75.1 Detailed Description	1314
18.75.2 Field Documentation	1314
18.76ReadDirCtx Struct Reference	1314
18.76.1 Detailed Description	1315
18.76.2 Field Documentation	1315
18.77RecordLayerHeader Struct Reference	1315
18.77.1 Detailed Description	1315
18.77.2 Field Documentation	1315
18.78RsaKey Struct Reference	1316
18.78.1 Detailed Description	1316
18.78.2 Field Documentation	1316
18.79SckeArgs Struct Reference	1317
18.79.1 Detailed Description	1318
18.79.2 Field Documentation	1318
18.80ScvArgs Struct Reference	1318
18.80.1 Detailed Description	1318
18.80.2 Field Documentation	1319
18.81SessionRow Struct Reference	1319
18.81.1 Detailed Description	1320
18.81.2 Field Documentation	1320
18.82Sha Struct Reference	1320
18.82.1 Detailed Description	1320
18.82.2 Field Documentation	1320
18.83Sha256 Struct Reference	1321

18.83.1 Detailed Description	1321
18.83.2 Field Documentation	1321
18.84SignatureCtx Struct Reference	1322
18.84.1 Detailed Description	1322
18.84.2 Field Documentation	1322
18.85Signer Struct Reference	1323
18.85.1 Detailed Description	1323
18.85.2 Field Documentation	1323
18.86smtp_send_request Struct Reference	1324
18.86.1 Detailed Description	1325
18.86.2 Field Documentation	1325
18.87spi_instance_t Struct Reference	1325
18.87.1 Detailed Description	1326
18.87.2 Field Documentation	1326
18.88SskeArgs Struct Reference	1326
18.88.1 Detailed Description	1326
18.88.2 Field Documentation	1326
18.89Suites Struct Reference	1327
18.89.1 Detailed Description	1327
18.89.2 Field Documentation	1327
18.90t_atcert Struct Reference	1328
18.90.1 Detailed Description	1328
18.90.2 Field Documentation	1328
18.91tcp_ready Struct Reference	1329
18.91.1 Detailed Description	1329
18.91.2 Field Documentation	1329
18.92timeoutInfo_st Struct Reference	1329
18.92.1 Detailed Description	1330
18.92.2 Field Documentation	1330
18.93timer_chan_state_t Struct Reference	1330
18.93.1 Detailed Description	1330
18.94timing_instance_t Struct Reference	1330
18.94.1 Detailed Description	1331
18.94.2 Field Documentation	1331
18.95uart_instance_t Struct Reference	1331
18.95.1 Detailed Description	1331
18.95.2 Field Documentation	1331
18.96WC_DerCertList Struct Reference	1332
18.96.1 Detailed Description	1332
18.96.2 Field Documentation	1332

18.97wc_HashAlg Union Reference	1332
18.97.1 Detailed Description	1332
18.97.2 Field Documentation	1332
18.98WC_RNG Struct Reference	1333
18.98.1 Detailed Description	1333
18.98.2 Field Documentation	1333
18.99wdg_instance_t Struct Reference	1333
18.99.1 Detailed Description	1334
18.99.2 Field Documentation	1334
18.100WOLF_EVENT Struct Reference	1334
18.100.1 Detailed Description	1334
18.100.2 Field Documentation	1334
18.101WOLF_EVENT_QUEUE Struct Reference	1335
18.101.1 Detailed Description	1335
18.101.2 Field Documentation	1335
18.102WOLFSSL Struct Reference	1336
18.102.1 Detailed Description	1337
18.102.2 Field Documentation	1337
18.103WOLFSSL_ALERT Struct Reference	1340
18.103.1 Detailed Description	1340
18.103.2 Field Documentation	1340
18.104WOLFSSL_ALERT_HISTORY Struct Reference	1340
18.104.1 Detailed Description	1340
18.104.2 Field Documentation	1340
18.105WOLFSSL_ASN1_BIT_STRING Struct Reference	1341
18.105.1 Detailed Description	1341
18.105.2 Field Documentation	1341
18.106WOLFSSL_ASN1_INTEGER Struct Reference	1341
18.106.1 Detailed Description	1341
18.106.2 Field Documentation	1341
18.107WOLFSSL_ASN1_OBJECT Struct Reference	1342
18.107.1 Detailed Description	1342
18.107.2 Field Documentation	1342
18.108WOLFSSL_ASN1_STRING Struct Reference	1342
18.108.1 Detailed Description	1343
18.108.2 Field Documentation	1343
18.109WOLFSSL_ASN1_TIME Struct Reference	1343
18.109.1 Detailed Description	1343
18.109.2 Field Documentation	1343
18.110WOLFSSL_BIGNUM Struct Reference	1343

18.110.	Detailed Description	1344
18.110.	Field Documentation	1344
18.11	WOLFSSL_BIO Struct Reference	1344
18.111.	Detailed Description	1344
18.111.	Field Documentation	1344
18.11	WOLFSSL_BIO_METHOD Struct Reference	1346
18.112.	Detailed Description	1346
18.112.	Field Documentation	1346
18.11	WOLFSSL_BUFFER_INFO Struct Reference	1346
18.113.	Detailed Description	1346
18.113.	Field Documentation	1346
18.11	WOLFSSL_CERT_MANAGER Struct Reference	1346
18.114.	Detailed Description	1347
18.114.	Field Documentation	1347
18.11	WOLFSSL_Cipher Union Reference	1348
18.115.	Detailed Description	1349
18.115.	Field Documentation	1349
18.11	WOLFSSL_CIPHER Struct Reference	1349
18.116.	Detailed Description	1349
18.116.	Field Documentation	1349
18.11	WOLFSSL_COMP_METHOD Struct Reference	1349
18.117.	Detailed Description	1350
18.117.	Field Documentation	1350
18.11	WOLFSSL_CRL Struct Reference	1350
18.118.	Detailed Description	1350
18.118.	Field Documentation	1350
18.11	WOLFSSL_CTX Struct Reference	1351
18.119.	Detailed Description	1352
18.119.	Field Documentation	1352
18.12	WOLFSSL_DH Struct Reference	1355
18.120.	Detailed Description	1355
18.120.	Field Documentation	1355
18.12	WOLFSSL_DSA Struct Reference	1356
18.121.	Detailed Description	1356
18.121.	Field Documentation	1356
18.12	WOLFSSL_DTLS_CTX Struct Reference	1357
18.122.	Detailed Description	1357
18.122.	Field Documentation	1357
18.12	WOLFSSL_DTLS_PEERSEQ Struct Reference	1357
18.123.	Detailed Description	1358

18.123.2	Field Documentation	1358
18.124	WOLFSSL_EC_GROUP Struct Reference	1358
18.124.1	Detailed Description	1358
18.124.2	Field Documentation	1359
18.125	WOLFSSL_EC_KEY Struct Reference	1359
18.125.1	Detailed Description	1359
18.125.2	Field Documentation	1359
18.126	WOLFSSL_EC_POINT Struct Reference	1360
18.126.1	Detailed Description	1360
18.126.2	Field Documentation	1360
18.127	WOLFSSL_ECDSA_SIG Struct Reference	1361
18.127.1	Detailed Description	1361
18.127.2	Field Documentation	1361
18.128	WOLFSSL_EVP_CIPHER_CTX Struct Reference	1361
18.128.1	Detailed Description	1361
18.128.2	Field Documentation	1361
18.129	WOLFSSL_EVP_MD_CTX Struct Reference	1362
18.129.1	Detailed Description	1362
18.129.2	Field Documentation	1362
18.130	WOLFSSL_EVP_PKEY Struct Reference	1363
18.130.1	Detailed Description	1363
18.130.2	Field Documentation	1363
18.131	WOLFSSL_Hasher Union Reference	1363
18.131.1	Detailed Description	1364
18.131.2	Field Documentation	1364
18.132	WOLFSSL_HMAC_CTX Struct Reference	1364
18.132.1	Detailed Description	1364
18.132.2	Field Documentation	1364
18.133	WOLFSSL_MD4_CTX Struct Reference	1365
18.133.1	Detailed Description	1365
18.133.2	Field Documentation	1365
18.134	WOLFSSL_MD5_CTX Struct Reference	1365
18.134.1	Detailed Description	1365
18.134.2	Field Documentation	1365
18.135	WOLFSSL_METHOD Struct Reference	1365
18.135.1	Detailed Description	1366
18.135.2	Field Documentation	1366
18.136	WOLFSSL_OCSP Struct Reference	1366
18.136.1	Detailed Description	1366
18.136.2	Field Documentation	1366

18.137	WOLFSSL_RIPEND_CTX Struct Reference	1367
18.137.1	Detailed Description	1367
18.137.2	Field Documentation	1367
18.138	WOLFSSL_RSA Struct Reference	1367
18.138.1	Detailed Description	1367
18.138.2	Field Documentation	1367
18.139	WOLFSSL_SESSION Struct Reference	1368
18.139.1	Detailed Description	1369
18.139.2	Field Documentation	1369
18.140	WOLFSSL_SHA256_CTX Struct Reference	1370
18.140.1	Detailed Description	1370
18.140.2	Field Documentation	1370
18.141	WOLFSSL_SHA_CTX Struct Reference	1370
18.141.1	Detailed Description	1370
18.141.2	Field Documentation	1370
18.142	WOLFSSL_SOCKADDR Struct Reference	1370
18.142.1	Detailed Description	1371
18.142.2	Field Documentation	1371
18.143	WOLFSSL_STACK Struct Reference	1371
18.143.1	Detailed Description	1371
18.143.2	Field Documentation	1371
18.144	wolfssl_TI_Hash Struct Reference	1372
18.144.1	Detailed Description	1372
18.144.2	Field Documentation	1372
18.145	WOLFSSL_X509 Struct Reference	1373
18.145.1	Detailed Description	1373
18.145.2	Field Documentation	1373
18.146	WOLFSSL_X509_CHAIN Struct Reference	1375
18.146.1	Detailed Description	1375
18.146.2	Field Documentation	1375
18.147	WOLFSSL_X509_LOOKUP Struct Reference	1375
18.147.1	Detailed Description	1375
18.147.2	Field Documentation	1375
18.148	WOLFSSL_X509_LOOKUP_METHOD Struct Reference	1375
18.148.1	Detailed Description	1376
18.148.2	Field Documentation	1376
18.149	WOLFSSL_X509_NAME Struct Reference	1376
18.149.1	Detailed Description	1376
18.149.2	Field Documentation	1376
18.150	WOLFSSL_X509_OBJECT Struct Reference	1377

18.150.1 Detailed Description	1377
18.150.2 Field Documentation	1377
18.151 WOLFSSL_X509_REVOKED Struct Reference	1377
18.151.1 Detailed Description	1377
18.151.2 Field Documentation	1377
18.152 WOLFSSL_X509_STORE Struct Reference	1378
18.152.1 Detailed Description	1378
18.152.2 Field Documentation	1378
18.153 WOLFSSL_X509_STORE_CTX Struct Reference	1378
18.153.1 Detailed Description	1379
18.153.2 Field Documentation	1379
18.154 509_buffer Struct Reference	1379
18.154.1 Detailed Description	1380
18.154.2 Field Documentation	1380
Index	1381

1 S32 SDK

Introduction

This topic provides an introduction to the S32 software development kit (S32 SDK), including intended audience, purpose and scope, and detailed sections on technical considerations.



Intended Audience

S32 SDK documentation is written for software developers and system engineers who have a technical background, and a working knowledge of embedded programming. The audience for the S32 SDK are users of S32 Processors.

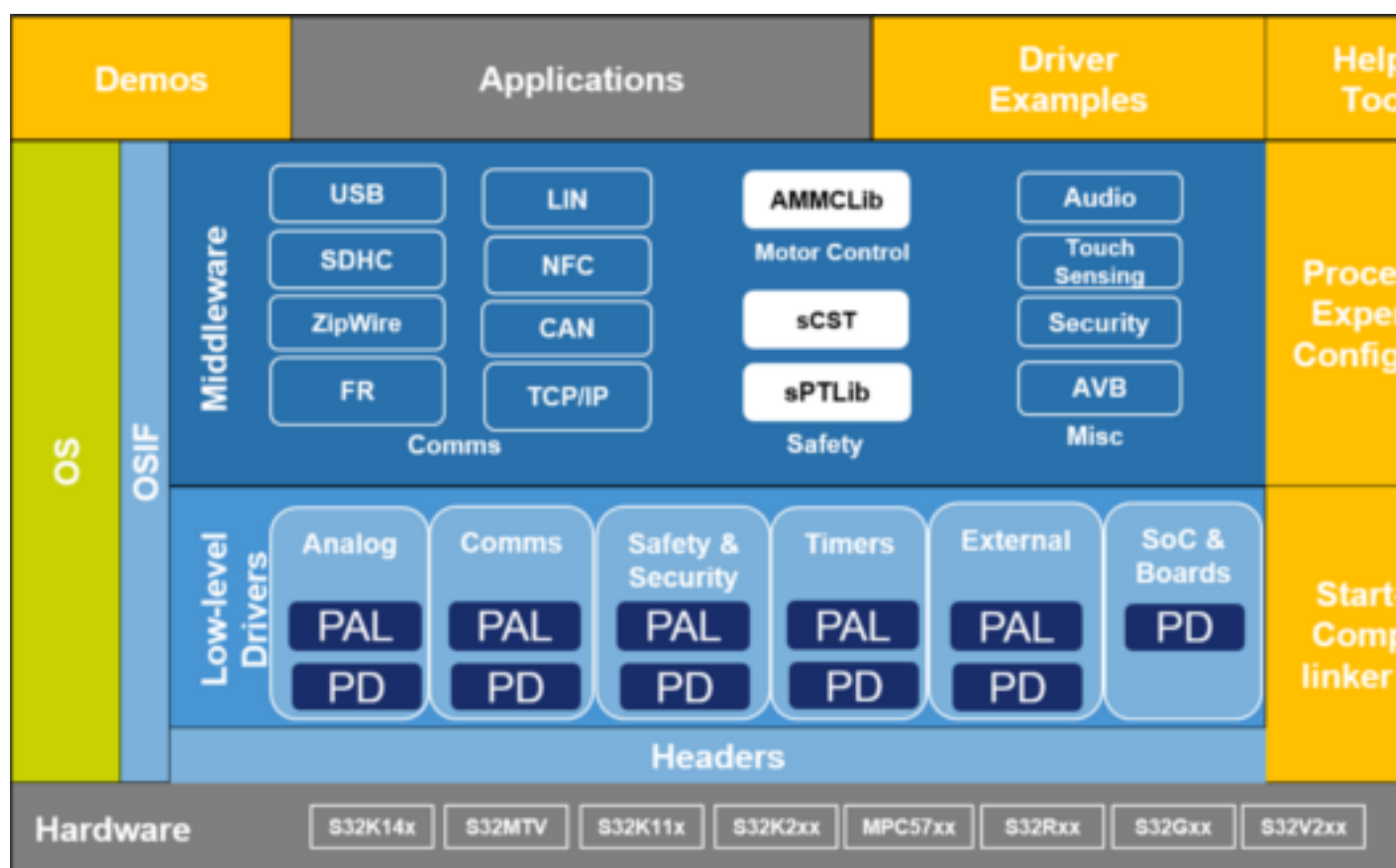
Purpose and Scope

The S32 SDK is an embedded oriented development kit. It allows users to

1. Evaluate and explore the features of the S32 processors; experience how they are supported by working "out of the box" on NXP development boards.
2. Develop embedded solutions; the NXP SDK is thoroughly tested from development to production.

S32 SDK Architecture Overview

The S32 SDK is an extensive suite of robust hardware interface and hardware abstraction layers, peripheral drivers, RTOS, stacks, and middleware designed to simplify and accelerate application development on NXP S32 SOC. The addition of Processor Expert technology for software and board configuration provides unmatched ease of use and flexibility. Included in the S32 SDK is full source code under a permissive open-source license for all hardware abstraction and peripheral driver software. See the Release Notes for details. The S32 SDK consists of the following runtime software components written in C:



2 Components

Header file

The S32 SDK contains a device-specific header files which provide direct access to the peripheral registers. Each supported device in S32 SDK has an overall System-on-Chip (SoC) memory-mapped header file. This header file contains the memory map and register base address for each peripheral and the IRQ vector table with associated vector numbers.

Feature Header File

The PAL is designed to be reusable regardless of the peripheral configuration differences from one SOC device to another. An overall Peripheral Feature Header File is provided for device to define the feature or configuration differences for each SOC sub-family device.

Peripheral Abstraction Layer

The PAL provides unified interfaces for families of peripherals, allowing for cross-platform compatibility of application code. The main goal is to provide an application programming interface that is independent of the underlying peripheral implementation.

The PAL supports all instances of each peripheral from a certain family instantiated on the SOC by using a simple integer parameter for the peripheral instance number.

The PAL instances should be configured bearing in mind possible limitations of the underlying peripherals - some features may not be supported on some hardware modules. It is the user's responsibility to correctly handle hardware resources, especially when porting the application to a different platform.

The PAL drivers can be found in the platform/pal directory.

Peripheral Drivers

The Peripheral Drivers are high-level drivers that implement high-level logic transactions based on an internal register access abstraction layer, other Peripheral Drivers, and/or System Services. For example, the UART register access abstraction layer mainly focuses on byte-level basic functional primitives, while the UART Peripheral Driver operates on an interrupt-driven level using data buffers to transfer a stream of bytes. In general, if a driver, that is mainly based on one peripheral, interfaces with functions beyond the register access abstraction layer and/or requires interrupt servicing, the driver is considered a high-level Peripheral Driver.

The Peripheral Drivers support all instances of each peripheral instantiated on the SOC by using a simple integer parameter for the peripheral instance number. The user of the Peripheral Driver does not need to know the peripheral memory-mapped base address.

The Peripheral Drivers operate on a high-level logic that requires data storage for internal operation context handling. However, the Peripheral Drivers do not allocate this memory space. Rather, the user passes in the memory for the driver internal operation through the driver initialization function.

The Peripheral Drivers are designed to handle the entire functionality for a targeted use-case. An application should be able to use only the Peripheral Driver to accomplish its purpose.

The Peripheral Drivers can be found in the platform/drivers directory.

System Services

The System Services contain a set of software entities that can be used by the Peripheral Drivers. They may be used with PAL Drivers to build the Peripheral Drivers or they can be used by an application directly. The following sections describe each of the System Services software entities. These System Services are in the platform/drivers directory.

Interrupt Manager

The Interrupt Manager provides functions to enable and disable individual interrupts within the Nested Vector Interrupt Controller (NVIC). It also provides functions to enable and disable the ARM core global interrupt (via the CPSIE and CPSID instructions) for bare-metal critical section implementation. In addition to providing functions for interrupt enabling and disabling, the Interrupt Manager provides Interrupt Service Routine (ISR) registration that allows the application software to register or replace the interrupt handler for a specified IRQ vector. The drivers do not set interrupt priorities. The interrupt priority scheme is entirely determined by the specific application logic and its setting is handled by the user application. The user application manages the interrupt priorities.

Clock Manager

The Clock Manager provides centralized clock-related functions for the entire system. It can dynamically set the system clock and perform clock gating/un-gating for specific peripherals. The Clock Manager also maintains knowledge of the clock sources required for each peripheral and provides functions to obtain the clock frequency for each supported clock used by the peripheral. The Clock Manager provides a notification framework which the software components, such as drivers, uses to register callback functions and execute the predefined code flow during the clock mode transition.

Power Manager

The Power Manager provides centralized power-related functions for the entire system. It dynamically sets the system power mode. The Power Manager provides a notification framework which the software components, such as drivers, uses to register callback functions and execute the predefined code flow during the power mode transition.

Examples

The examples provided show how to build user applications using the S32 SDK. The examples can be found in the top-level example directory. For details please see `Examples_and_Demos`.

3 PAL vs PD usage

PAL - Peripheral Abstraction layer

- Interface abstraction for a family of peripherals (E.g. LPUART + LINFlexD_UART + eSCI + FlexIO_UART + etc.)
- Single layer per SDK
- Same generic API on multiple platforms

PD - Peripheral Drivers

- IP dedicated low-level drivers
- Designed for efficiency and IP features set coverage

When to use the Peripheral Abstraction Layer (PAL)?

- Whenever an application needs a simplified, generic interface that abstracts as much as possible the underlying silicon features.
- Whenever developing portable higher level generic code that is meant to run on different NXP platforms. This may include anything from low level console utility libraries to communication stacks like TCP/IP.

When to use Peripheral Drivers?

- Whenever developing for high efficiency (code size, execution speed, etc.) or planning to use specific peripheral features.

4 Supported Platforms

Supported board and SoC versions can be found in the Release Notes. (`SDK\ReleaseNotes.pdf`)

5 Installation

Prerequisites

SDK can be used in two ways: bundled in S32 Design Studio and standalone.

S32 SDK is delivered bundled in the S32 Design Studio. In this case it's already configured and ready to use.

S32 SDK is also delivered through a standalone installer. Using the standalone installer is recommended when using a compiler which is not supported in S32 Design Studio or when the graphical interface is not required. In this case the installer can configure an existing S32 Design Studio to use the configuration files delivered in the installer.

If the integration with the S32 Design Studio is not needed the path to S32 Design Studio can be left empty – and in this case only the S32 SDK will be installed and configured.

Steps

1. Start the installer S32_SDK_<ReleaseSpecific>.exe
2. Set the destination folder for the SDK, give optional location of S32DS and install. Example of S32DS path: C:\NXP\S32ARMv1.3
3. Start using the SDK by creating a new project or importing a project

Background

The installer does the following things in background:

- Puts the SDK in the selected destination directory.
- Appends to S32SDK_PATH the path of the SDK.
 - Note: Please make sure you uninstall previous SDK so that this variable will be empty.
- Copies necessary files into S32 Design Studio installation location.
- Overwrites existing SDK from S32 Design Studio with the version from destination directory

Uninstaller

When the SDK is installed using the standalone the installer, the user can use "uninst.exe" from the root of the destination to uninstall the SDK.

Note: If you want to reinstall the SDK please use a clean copy of S32DS. When you uninstall this does not delete the copied files (ex: Config_01.pez), so a clean copy is needed.

6 Build Tools

Introduction

S32 SDK supports and is tested with multiple compiler toolchains.

Note

The toolchain list, versions and their options specific for the platform and release can be found in the Release Notes. (SDK\ReleaseNotes.pdf)

Toolchain versions and options can be found in the Release Notes. (SDK\ReleaseNotes.pdf)

Compiler warnings disabled for S32 SDK

For *Wind River DIAB Compiler* the following warnings are not checked at S32 SDK build time:

- **#1824: *explicit cast discards volatile qualifier***
Motivation: this warning has been deactivated because of false positive occurrences reported for Wind River DIAB Compiler 5.9.4.8 under tickets TCDIAB-13994, TCDIAB-14098.
- **#5387: *explicit conversion of a 64-bit integral type to a smaller integral type (potential portability problem)***
Motivation: this warning has been disabled because it is reported for conversions required by the internal SDK algorithms. Intermediary results requiring high precision are stored as `uint64_t` variables and converted into `uint32_t` variables. Checks have been put in place to ensure that the cast is only done if the value to be converted fits on 32 bits.
- **#5388: *conversion from pointer to same-sized integral type (potential portability problem)***
Motivation: for S32 SDK conversions between `uint32_t` and memory addresses are made assuming that pointers are stored on 32bits.

Makefiles

Multiple makefile projects are provided in the 'examples' folder, for all supported compilers. These projects can be modified by adding application code, or the makefiles can be reused in different projects, after reconfiguring the paths/variables. Please note that these projects require the designated compiler to be already installed on the host; also, the makefile path to compiler executable must be updated before running make utility.

S32 Design Studio

S32 Design Studio is delivered with platform specific gcc cross compiler included ("`{S32_Design_Studio_install_path}\Cross_Tools`"). Eclipse plugins for gcc are already installed in S32 Design Studio IDE, so new projects for this toolchain can be created and built directly from the IDE. To add S32 SDK source files to a clean S32 Design Studio project, eclipse "linked resources" feature can be used: project properties->New->Folder->Advanced->'Link to alternate location' (e.g. "`{S32_SDK_PATH}`"). For S32 Design Studio project with Processor Expert support, please import a project from "`{S32_SDK_PATH}` Name".

7 IDE Support

S32 Design Studio

- S32 Design Studio is delivered with Processor Expert support included. Please see [Configuration](#) chapter.
- To configure the S32 SDK path of the project, eclipse "S32 SDK Specific" feature can be used: patch project properties->Processor Expert->S32 SDK Specific->SDK path
- Processor Expert repositories and paths can be configured as it follows: Window -> Preferences -> Processor Expert -> Repositories and Paths.
- S32 Design Studio projects can be imported from S32 SDK package. Please see [Examples_and_Demos](#) chapter.

IAR Embedded Workbench

- NOT applicable to platforms which do not support IAR compiler. Please see Release Notes.
- There is no configuration support for S32 SDK in IAR.
- IAR Embedded Workbench projects can be imported from S32 SDK package. Please see [Examples_and_Demos](#) chapter.

8 Configuration

Processor Expert software allows generation of configuration structures for peripheral drivers from S32 SDK. With the help of Eclipse based graphical interface where you can configure your driver and generate corresponding configuration structure. This tool doesn't generate source code for S32 family, it only generates configurations data structures.

Processor Expert generates configuration header files that are included by application source code. The configuration data structures from these files are defined in S32 SDK. All these header files are generated by this tool in \${ProjName}/Generated_Code directory.

Peripheral drivers are not stored directly in the project directory, these drivers are stored in S32 SDK repository. Shared peripheral drivers repository is advantageous when more projects should share the same version of peripheral drivers. In this case, peripheral drivers are not physically placed in the project directory but each project is virtually linked with shared, common repository from S32 SDK. This way the management of the projects' drivers can be done in one place and any changes made in the shared repository is automatically distributed across all of the linked projects, for example in case of bug fixing or library update and also backup or archiving of the peripheral drivers versions is very simple.

9 Acronyms and Abbreviations

Acronym	Description
CPSIE, CPSID	Change Processor State Interrupt Enable / Disable
EAR	Early Access Release
EVB	Evaluation board
PAL	Peripheral Abstraction Layer
IRQ	Interrupt Request
ISR	Interrupt Service Routine
LLWU	Low Leakage Wakeup Unit
NVIC	Nested Vector Interrupt Controller
RTOS	Real Time Operating System
S32DS	S32 Design Studio
SDK	Software Development Kit
SOC	System-on-Chip
UART	Universal Asynchronous Receiver / Transmitter

10 MISRA Compliance

This section describes how the S32 SDK project addresses MISRA Compliance.

The S32 SDK SW components which are implemented to be compliant with MISRA C 2012 are:

- all drivers & PALs
- generated driver code (including Cpu.c & .h)
- main.c (generated via graphical configurator)

Violations of MISRA C 2012 guidelines which remain not fixed, shall be documented as deviations at file level.

Other SW components included in the S32 SDK package which are not subject to MISRA C 2012 compliance:

- demo_apps & driver examples
- FreeRTOS

11 Development guidelines

Set of guidelines to improve the usability of the S32 SDK.

Some usual guidelines on SDK programming model:

1. Driver state structures should be declared as global or static variables as they are used in the whole time when the driver is used.
2. Driver state structures content should not be used or modified by the application code.
3. Peripheral drivers, PALs and Middleware code are not handling clock and pins initialization. Configuration of the clock and pins driver has to be done by the application. To make sure these are properly initialized before other modules are used, please call the corresponding initialization:

```
/* Initialize and configure clocks */
CLOCK_SYS_Init(g_clockManConfigsArr, CLOCK_MANAGER_CONFIG_CNT,
               g_clockManCallbacksArr, CLOCK_MANAGER_CALLBACK_CNT);
CLOCK_SYS_UpdateConfiguration(0U,
                              CLOCK_MANAGER_POLICY_AGREEMENT);

/* Initialize pins */
PINS_DRV_Init(NUM_OF_CONFIGURED_PINS, g_pin_mux_InitConfigArr);
```

Note

The configuration structure names used in this example are the default names generated by Processor Expert components for clock and pins. Applications not using Processor Expert might have different names for these structures.

4. The recommended approach at development time is to add DEV_ERROR_DETECT symbol to the compiler defines. This will enable DEV_ASSERT mechanism which can catch application code errors in the early development stage.
5. High care should be taken to have a backup option when debug pins are routed to other functionalities.

12 Error detection and reporting

S32 SDK drivers can use a mechanism to validate data coming from upper software layers (application code) by performing a number of checks on input parameters' range or other invariants that can be statically checked (not dependent on runtime conditions). A failed validation is indicative of a software bug in application code, therefore it is important to use this mechanism during development.

The validation is performed by using DEV_ASSERT macro. A default implementation of this macro is provided in this file. However, application developers can provide their own implementation in a custom file. This requires defining the CUSTOM_DEVASSERT symbol with the specific file name in the project configuration (for example: -DCUSTOM_DEVASSERT="custom_devassert.h")

The default implementation accommodates two behaviors, based on DEV_ERROR_DETECT symbol:

- When DEV_ERROR_DETECT symbol is defined in the project configuration (for example: -DDEV_ERROR_DETECT), the validation performed by the DEV_ASSERT macro is enabled, and a failed validation triggers a software breakpoint and further execution is prevented (application spins in an infinite loop) This configuration is recommended for development environments, as it prevents further execution and allows investigating potential problems from the point of error detection.
- When DEV_ERROR_DETECT symbol is not defined, the DEV_ASSERT macro is implemented as no-op, therefore disabling all validations. This configuration can be used to eliminate the overhead of development-time checks.

It is the application developer's responsibility to decide the error detection strategy for production code: one can opt to disable development-time checking altogether (by not defining DEV_ERROR_DETECT symbol), or one can opt to keep the checks in place and implement a recovery mechanism in case of a failed validation, by defining CUSTOM_DEVASSERT to point to the file containing the custom implementation.

13 Notes - Please read

Note 1

```

1 wolfSSL as of 3.6.6 no longer enables SSLv3 by default. wolfSSL also no
2 longer supports static key cipher suites with PSK, RSA, or ECDH. This means
3 if you plan to use TLS cipher suites you must enable DH (DH is on by default),
4 or enable ECC (ECC is on by default on 64bit systems), or you must enable static
5 key cipher suites with
6     WOLFSSL_STATIC_DH
7     WOLFSSL_STATIC_RSA
8     or
9     WOLFSSL_STATIC_PSK
10
11 though static key cipher suites are deprecated and will be removed from future
12 versions of TLS. They also lower your security by removing PFS. Since current
13 NTRU suites available do not use ephemeral keys, WOLFSSL_STATIC_RSA needs to be
14 used in order to build with NTRU suites.
15
16
17 When compiling ssl.c, wolfSSL will now issue a compiler error if no cipher suites
18 are available. You can remove this error by defining WOLFSSL_ALLOW_NO_SUITES
19 in the event that you desire that, i.e., you're not using TLS cipher suites.

```

Note 2

```

1 wolfSSL takes a different approach to certificate verification than OpenSSL
2 does. The default policy for the client is to verify the server, this means
3 that if you don't load CAs to verify the server you'll get a connect error,
4 no signer error to confirm failure (-188). If you want to mimic OpenSSL
5 behavior of having SSL_connect succeed even if verifying the server fails and
6 reducing security you can do this by calling:
7
8 wolfSSL_CTX_set_verify(ctx, SSL_VERIFY_NONE, 0);
9
10 before calling wolfSSL_new(); Though it's not recommended.

```

wolfSSL (Formerly CyaSSL) Release 3.12.0 (8/04/2017)

Release 3.12.0 of wolfSSL has bug fixes and new features including:

- TLS 1.3 with Nginx! TLS 1.3 with ARMv8! TLS 1.3 with Async Crypto! (`--enable-tls13`)
- TLS 1.3 0RTT feature added
- Added port for using Intel SGX with Linux
- Update and fix PIC32MZ port
- Additional unit testing for MD5, SHA, SHA224, SHA256, SHA384, SHA512, RipeMd, HMAC, 3DES, IDEA, ChaCha20, ChaCha20Poly1305 AEAD, Camellia, [Rabbit](#), ARC4, AES, RSA, Hc128
- AVX and AVX2 assembly for improved ChaCha20 performance
- Intel QAT fixes for when using `--disable-fastmath`
- Update how DTLS handles decryption and MAC failures
- Update DTLS session export version number for `--enable-sessionexport` feature
- Add additional input argument sanity checks to ARMv8 assembly port
- Fix for making PKCS12 dynamic types match
- Fixes for potential memory leaks when using `--enable-fast-rsa`
- Fix for when using custom ECC curves and add BRAINPOOLP256R1 test
- Update TI-RTOS port for dependency on new wolfSSL source files
- DTLS multicast feature added, `--enable-mcast`

- Fix for Async crypto with GCC 7.1 and HMAC when not using Intel QuickAssist
- Improvements and enhancements to Intel QuickAssist support
- Added Xilinx port
- Added SHA3 Keccak feature, `--enable-sha3`
- Expand wolfSSL Python wrapper to now include a client side implementation
- Adjust example servers to not treat a peer closed error as a hard error
- Added more sanity checks to `fp_read_unsigned_bin` function
- Add SHA224 and AES key wrap to ARMv8 port
- Update MQX classics and mmCAU ports
- Fix for potential buffer over read with `wolfSSL_CertPemToDer`
- Add PKCS7/CMS decode support for KARI with `IssuerAndSerialNumber`
- Fix ThreadX/NetX warning
- Fixes for OCSP and CRL non blocking sockets and for incomplete cert chain with OCSP
- Added RSA PSS sign and verify
- Fix for STM32F4 AES-GCM
- Added enable all feature (`--enable-all`)
- Added trackmemory feature (`--enable-trackmemory`)
- Fixes for AES key wrap and PKCS7 on Windows VS
- Added benchmark block size argument
- Support use of staticmemory with PKCS7
- Fix for Blake2b build with GCC 5.4
- Fixes for compiling wolfSSL with GCC version 7, most dealing with switch statement fall through warnings.
- Added warning when compiling without hardened math operations

Note: There is a known issue with using ChaCha20 AVX assembly on versions of GCC earlier than 5.2. This is encountered with using the wolfSSL enable options `--enable-intelasm` and `--enable-chacha`. To avoid this issue ChaCha20 can be enabled with `--enable-chacha=noasm`. If using `--enable-intelasm` and also using `--enable-sha224` or `--enable-sha256` there is a known issue with trying to use `-fsanitize=address`.

This release of wolfSSL fixes 1 low level security vulnerability.

Low level fix for a potential DoS attack on a wolfSSL client. Previously a client would accept many warning alert messages without a limit. This fix puts a limit to the number of warning alert messages received and if this limit is reached a fatal error `ALERT_COUNT_E` is returned. The max number of warning alerts by default is set to 5 and can be adjusted with the macro `WOLFSSL_ALERT_COUNT_MAX`. Thanks for the report from Tarun Yadav and Koustav Sadhukhan from Defence Research and Development Organization, INDIA.

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/wolfSSL/Docs.html>

wolfSSL (Formerly CyaSSL) Release 3.11.1 (5/11/2017)

Release 3.11.1 of wolfSSL is a TLS 1.3 BETA release, which includes:

- TLS 1.3 client and server support for TLS 1.3 with Draft 18 support

This is strictly a BETA release, and designed for testing and user feedback. Please send any comments, testing results, or feedback to wolfSSL at support@wolfssl.com.

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/wolfSSL/Docs.html>

wolfSSL (Formerly CyaSSL) Release 3.11.0 (5/04/2017)

Release 3.11.0 of wolfSSL has bug fixes and new features including:

- Code updates for warnings reported by Coverity scans
- Testing and warning fixes for FreeBSD on PowerPC
- Updates and refactoring done to ASN1 parsing functions
- Change max PSK identity buffer to account for an identity length of 128 characters
- Update Arduino script to handle recent files and additions
- Added support for PKCS#7 Signed Data with ECDSA
- Fix for interoperability with ChaCha20-Poly1305 suites using older draft versions
- DTLS update to allow multiple handshake messages in one DTLS record. Thanks to Eric Samsel over at Welch Allyn for reporting this bug.
- Intel QuickAssist asynchronous support (PR #715 - https://www.wolfssl.com/wolfSSL/Blog/Entries/2017/1/18_wolfSSL_Asynchronous_Intel_QuickAssist_Support.html)
- Added support for HAproxy load balancer
- Added option to allow SHA1 with TLS 1.2 for IIS compatibility (WOLFSSL_ALLOW_TLS_SHA1)
- Added Curve25519 51-bit Implementation, increasing performance on systems that have 128 bit types
- Fix to not send session ID on server side if session cache is off unless we're echoing session ID as part of session tickets
- Fixes for ensuring all default ciphers are setup correctly (see PR #830)
- Added NXP Hexiwear example in `IDE/HEXIWEAR`.
- Added `wolfSSL_write_dup()` to create write only `WOLFSSL` object for concurrent access
- Fixes for TLS elliptic curve selection on private key import.
- Fixes for RNG with Intel `rdrand` and `rdseed` speedups.
- Improved performance with Intel `rdrand` to use full 64-bit output
- Added new `--enable-intelrand` option to indicate use of `RDRAND` preference for RNG source
- Removed RNG ARC4 support
- Added ECC helpers to get size and id from curve name.
- Added ECC Cofactor DH (ECC-CDH) support

- Added ECC private key only import / export functions.
- Added PKCS8 create function
- Improvements to TLS layer CTX handling for switching keys / certs.
- Added check for duplicate certificate policy OID in certificates.
- Normal math speed-up to not allocate on `mp_int` and defer until `mp_grow`
- Reduce heap usage with fast math when not using `ALT_ECC_SIZE`
- Fixes for building CRL with Windows
- Added support for inline CRL lookup when `HAVE_CRL_IO` is defined
- Added port for tenAsys INtime RTOS
- Improvements to uTKernel port (`WOLFSSL_uTKERNEL2`)
- Updated WPA Supplicant support
- Added support for Nginx
- Update stunnel port for version 5.40
- Fixes for STM32 hardware crypto acceleration
- Extended test code coverage in bundled `test.c`
- Added a sanity check for minimum authentication tag size with AES-GCM. Thanks to Yueh-Hsun Lin and Peng Li at KNOX Security at Samsung Research America for suggesting this.
- Added a sanity check that subject key identifier is marked as non-critical and a check that no policy OIDS appear more than once in the cert policies extension. Thanks to the report from Professor Zhenhua Duan, Professor Cong Tian, and Ph.D candidate Chu Chen from Institute of Computing Theory and Technology (ICTT) of Xidian University, China. Profs. Zhenhua Duan and Cong Tian are supervisors of Ph.D candidate Chu Chen.

This release of wolfSSL fixes 5 low and 1 medium level security vulnerability.

3 Low level fixes reported by Yueh-Hsun Lin and Peng Li from KNOX Security, Samsung Research America.

- Fix for out of bounds memory access in `wc_DhParamsLoad()` when `GetLength()` returns a zero. Before this fix there is a case where wolfSSL would read out of bounds memory in the function `wc_DhParamsLoad`.
- Fix for DH key accepted by `wc_DhAgree` when the key was malformed.
- Fix for a double free case when adding CA cert into `X509_store`.

Low level fix for memory management with static memory feature enabled. By default static memory is disabled. Thanks to GitHub user `hajjihraf` for reporting this.

Low level fix for out of bounds write in the function `wolfSSL_X509_NAME_get_text_by_NID`. This function is not used by TLS or crypto operations but could result in a buffer out of bounds write by one if called explicitly in an application. Discovered by Aleksandar Nikolic of Cisco Talos. <http://talosintelligence.com/vulnerability-reports/>

Medium level fix for check on certificate signature. There is a case in release versions 3.9.10, 3.10.0 and 3.10.2 where a corrupted signature on a peer certificate would not be properly flagged. Thanks to Wens Lo, James Tsai, Kenny Chang, and Oscar Yang at Castles Technology.

See `INSTALL` file for build instructions. More info can be found on-line at <http://wolfssl.com/wolfSSL/Docs.html>

wolfSSL (Formerly CyaSSL) Release 3.10.2 (2/10/2017)

Release 3.10.2 of wolfSSL has bug fixes and new features including:

- Poly1305 Windows macros fix. Thanks to GitHub user Jay Satiro
- Compatibility layer expanded with multiple functions added
- Improve fp_copy performance with ALT_ECC_SIZE
- OCSP updates and improvements
- Fixes for IAR EWARM 8 compiler warnings
- Reduce stack usage with ECC_CACHE_CURVE disabled
- Added ECC export raw for public and private key
- Fix for NO_ASN_TIME build
- Supported curves extensions now populated by default
- Add DTLS build without big integer math
- Fix for static memory feature with wc_ecc_verify_hash_ex and not SHAMIR
- Added PSK interoperability testing to script bundled with wolfSSL
- Fix for Python wrapper random number generation. Compiler optimizations with Python could place the random number in same buffer location each time. Thanks to GitHub user Erik Bray (embray)
- Fix for tests on unaligned memory with static memory feature
- Add macro WOLFSSL_NO_OCSP_OPTIONAL_CERTS to skip optional OCSP certificates
- Sanity checks on NULL arguments added to wolfSSL_set_fd and wolfSSL_DTLS_SetCookieSecret
- mp_jacobi stack use reduced, thanks to Szabi Tolnai for providing a solution to reduce stack usage

This release of wolfSSL fixes 2 low and 1 medium level security vulnerability.

Low level fix of buffer overflow for when loading in a malformed temporary DH file. Thanks to Yueh-Hsun Lin and Peng Li from KNOX Security, Samsung Research America for the report.

Medium level fix for processing of OCSP response. If using OCSP without hard faults enforced and no alternate revocation checks like OCSP stapling then it is recommended to update.

Low level fix for potential cache attack on RSA operations. If using wolfSSL RSA on a server that other users can have access to monitor the cache, then it is recommended to update wolfSSL. Thanks to Andreas Zankl, Johann Heyszl and Georg Sigl at Fraunhofer AISEC for the initial report.

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/wolfSSL/Docs.html>

wolfSSL (Formerly CyaSSL) Release 3.10.0 (12/21/2016)

Release 3.10.0 of wolfSSL has bug fixes and new features including:

- Added support for SHA224
- Added scrypt feature
- Build for Intel SGX use, added in directory IDE/WIN-SGX
- Fix for ChaCha20-Poly1305 ECDSA certificate type request

- Enhance PKCS#7 with ECC enveloped data and AES key wrap support
- Added support for RIOT OS
- Add support for parsing PKCS#12 files
- ECC performance increased with custom curves
- ARMv8 expanded to AArch32 and performance increased
- Added ANSI-X9.63-KDF support
- Port to STM32 F2/F4 CubeMX
- Port to Atmel ATECC508A board
- Removed fPIE by default when wolfSSL library is compiled
- Update to Python wrapper, dropping DES and adding wc_RSASetRNG
- Added support for NXP K82 hardware acceleration
- Added SCR client and server verify check
- Added a disable rng option with autoconf
- Added more tests vectors to [test.c](#) with AES-CTR
- Updated DTLS session export version number
- Updated DTLS for 64 bit sequence numbers
- Fix for memory management with TI and WOLFSSL_SMALL_STACK
- Hardening RSA CRT to be constant time
- Fix uninitialized warning with IAR compiler
- Fix for C# wrapper example IO hang on unexpected connection termination

This release of wolfSSL fixes a low level security vulnerability. The vulnerability reported was a potential cache attack on RSA operations. If using wolfSSL RSA on a server that other users can have access to monitor the cache, then it is recommended to update wolfSSL. Thanks to Andreas Zankl, Johann Heyszl and Georg Sigl at Fraunhofer AISEC for the report. More information will be available on our site:

<https://wolfssl.com/wolfSSL/security/vulnerabilities.php>

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/wolfSSL/Docs.html>

wolfSSL (Formerly CyaSSL) Release 3.9.10 (9/23/2016)

Release 3.9.10 of wolfSSL has bug fixes and new features including:

- Default configure option changes:
 1. DES3 disabled by default
 2. ECC Supported Curves Extension enabled by default
 3. New option Extended Master Secret enabled by default
- Added checking CA certificate path length, and new test certs
- Fix to DSA pre padding and sanity check on R/S values
- Added CTX level RNG for single-threaded builds

- Intel RDSEED enhancements
- ARMv8 hardware acceleration support for AES-CBC/CTR/GCM, SHA-256
- Arduino support updates
- Added the Extended Master Secret TLS extension
 1. Enabled by default in configure options, API to disable
 2. Added support for Extended Master Secret to sniffer
- OCSP fix with issuer key hash, lookup refactor
- Added support for Frosted OS
- Added support for DTLS over SCTP
- Added support for static memory with wolfCrypt
- Fix to ECC Custom Curve support
- Support for asynchronous wolfCrypt RSA and TLS client
- Added distribution build configure option
- Update the test certificates

This release of wolfSSL fixes medium level security vulnerabilities. Fixes for potential AES, RSA, and ECC side channel leaks is included that a local user monitoring the same CPU core cache could exploit. VM users, hyper-threading users, and users where potential attackers have access to the CPU cache will need to update if they utilize AES, RSA private keys, or ECC private keys. Thanks to Gorka Irazoqui Apecechea and Xiaofei Guo from Intel Corporation for the report. More information will be available on our site:

<https://wolfssl.com/wolfSSL/security/vulnerabilities.php>

See INSTALL file for build instructions. More info can be found on-line at <https://wolfssl.com/wolfSSL/Docs.html>

wolfSSL (Formerly CyaSSL) Release 3.9.8 (7/29/2016)

Release 3.9.8 of wolfSSL has bug fixes and new features including:

- Add support for custom ECC curves.
- Add cipher suite ECDHE-ECDSA-AES128-CCM.
- Add compkey enable option. This option is for compressed ECC keys.
- Add in the option to use [test.h](#) without gettimeofday function using the macro WOLFSSL_USER_CURRTIME.
- Add RSA blinding for private key operations. Enable option of harden which is on by default. This negates timing attacks.
- Add ECC and TLS support for all SECP, Koblitz and Brainpool curves.
- Add helper functions for static memory option to allow getting optimum buffer sizes.
- Update DTLS behavior on bad MAC. DTLS silently drops packets with bad MACs now.
- Update fp_isprime function from libtom enhancement/cleanup repository.
- Update sanity checks on inputs and return values for AES-CMAC.
- Update wolfSSL for use with MYSQL v5.6.30.
- Update LPCXpresso eclipse project to not include [misc.c](#) when not needed.

- Fix retransmit of last DTLS flight with timeout notification. The last flight is no longer retransmitted on timeout.
- Fixes to some code in math sections for compressed ECC keys. This includes edge cases for buffer size on allocation and adjustments for compressed curves build. The code and full list can be found on github with pull request #456.
- Fix function argument mismatch for build with secure renegotiation.
- X.509 bug fixes for reading in malformed certificates, reported by researchers at Columbia University
- Fix GCC version 6 warning about hard tabs in poly1305.c. This was a warning produced by GCC 6 trying to determine the intent of code.
- Fixes for static memory option. Including avoid potential race conditions with counters, decrement handshake counter correctly.
- Fix anonymous cipher with Diffie Hellman on the server side. Was an issue of a possible buffer corruption. For information and code see pull request #481.
- One high level security fix that requires an update for use with static RSA cipher suites was submitted. This fix was the addition of RSA blinding for private RSA operations. We recommend servers who allow static RSA cipher suites to also generate new private RSA keys. Static RSA cipher suites are turned off by default.

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/wolfSSL/Docs.html>

wolfSSL (Formerly CyaSSL) Release 3.9.6 (6/14/2016)

Release 3.9.6 of wolfSSL has bug fixes and new features including:

- Add staticmemory feature
- Add public wc_GetTime API with base64encode feature
- Add AES CMAC algorithm
- Add DTLS sessionexport feature
- Add python wolfCrypt wrapper
- Add ECC encrypt/decrypt benchmarks
- Add dynamic session tickets
- Add eccshamir option
- Add Whitewood netRandom support –with-wnr
- Add embOS port
- Add minimum key size checks for RSA and ECC
- Add STARTTLS support to examples
- Add uTasker port
- Add asynchronous crypto and wolf event support
- Add compile check for [misc.c](#) with inline
- Add RNG benchmark
- Add reduction to stack usage with hash-based RNG
- Update STM32F2_CRYPTOPORT with additional algorithms supported
- Update MDK5 projects

- Update AES-NI
- Fix for STM32 with STM32F2_HASH defined
- Fix for building with MinGw
- Fix ECC math bugs with ALT_ECC_SIZE and key sizes over 256 bit (1)
- Fix certificate buffers github issue #422
- Fix decrypt max size with RSA OAEP
- Fix DTLS sanity check with DTLS timeout notification
- Fix free of WOLFSSL_METHOD on failure to create CTX
- Fix memory leak in failure case with wc_RsaFunction (2)
- No high level security fixes that requires an update though we always recommend updating to the latest
- (1) Code changes for ECC fix can be found at pull requests #411, #416, and #428
- (2) Builds using RSA with using normal math and not RSA_LOW_MEM should update

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/wolfSSL/Docs.html>

wolfSSL (Formerly CyaSSL) Release 3.9.0 (03/18/2016)

Release 3.9.0 of wolfSSL has bug fixes and new features including:

- Add new leantls configuration
- Add RSA OAEP padding at wolfCrypt level
- Add Arduino port and example client
- Add fixed point DH operation
- Add CUSTOM_RAND_GENRATE_SEED_OS and CUSTOM_RAND_GENERATE_BLOCK
- Add ECDHE-PSK cipher suites
- Add PSK ChaCha20-Poly1305 cipher suites
- Add option for fail on no peer cert except PSK suites
- Add port for Nordic nRF51
- Add additional ECC NIST test vectors for 256, 384 and 521
- Add more granular ECC, Ed25519/Curve25519 and AES configs
- Update to ChaCha20-Poly1305
- Update support for Freescale KSDK 1.3.0
- Update DER buffer handling code, refactoring and reducing memory
- Fix to AESNI 192 bit key expansion
- Fix to C# wrapper character encoding
- Fix sequence number issue with DTLS epoch 0 messages
- Fix RNGA with K64 build
- Fix ASN.1 X509 V3 certificate policy extension parsing

- Fix potential free of uninitialized RSA key in [asn.c](#)
- Fix potential underflow when using ECC build with FP_ECC
- Fixes for warnings in Visual Studio 2015 build
- No high level security fixes that requires an update though we always recommend updating to the latest
- FP_ECC is off by default, users with it enabled should update for the zero sized hash fix

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/yaSSL/Docs.html>

wolfSSL (Formerly CyaSSL) Release 3.8.0 (12/30/2015)

Release 3.8.0 of wolfSSL has bug fixes and new features including:

- Example client/server with VxWorks
- AESNI use with AES-GCM
- Stunnel compatibility enhancements
- Single shot hash and signature/verify API added
- Update cavium nitrox port
- LPCXpresso IDE support added
- C# wrapper to support wolfSSL use by a C# program
- (BETA version)OCSP stapling added
- Update OpenSSH compatibility
- Improve DTLS handshake when retransmitting finished message
- fix idea_mult() for 16 and 32bit systems
- fix LowResTimer on Microchip ports
- No high level security fixes that requires an update though we always recommend updating to the latest

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/yaSSL/Docs.html>

wolfSSL (Formerly CyaSSL) Release 3.7.0 (10/26/2015)

Release 3.7.0 of wolfSSL has bug fixes and new features including:

- ALPN extension support added for HTTP2 connections with `--enable-alpn`
- Change of example/client/client max fragment flag `-L -> -F`
- Throughput benchmarking, added scripts/benchmark.test
- Sniffer API `ssl_FreeDecodeBuffer` added
- Addition of `AES_GCM` to Sniffer
- Sniffer change to handle unlimited decrypt buffer size
- New option for the sniffer where it will try to pick up decoding after a sequence number acknowledgement fault. Also includes some additional stats.
- JNI API setter and getter function for jobject added

- User RSA crypto plugin abstraction. An example placed in wolfcrypt/user-crypto
- fix to asn configuration bug
- AES-GCM/CCM fixes.
- Port for Rowley added
- Rowley Crossworks bare metal examples added
- MDK5-ARM project update
- FreeRTOS support updates.
- VXWorks support updates.
- Added the IDEA cipher and support in wolfSSL.
- Update wolfSSL website CA.
- CFLAGS is usable when configuring source.
- No high level security fixes that requires an update though we always recommend updating to the latest

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/yaSSL/Docs.html>
#wolfSSL (Formerly CyaSSL) Release 3.6.8 (09/17/2015)

Release 3.6.8 of wolfSSL fixes two high severity vulnerabilities.

It also includes bug fixes and new features including:

- Two High level security fixes, all users SHOULD update. a) If using wolfSSL for DTLS on the server side of a publicly accessible machine you MUST update. b) If using wolfSSL for TLS on the server side with private RSA keys allowing ephemeral key exchange without low memory optimizations you MUST update and regenerate the private RSA keys.

Please see <https://www.wolfssl.com/wolfSSL/Blog/Blog.html> for more details

- No filesystem build fixes for various configurations
- Certificate generation now supports several extensions including KeyUsage, SKID, AKID, and Certificate Policies
- CRLs can be loaded from buffers as well as files now
- SHA-512 Certificate Signing generation
- Fixes for sniffer reassembly processing

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/yaSSL/Docs.html>
#wolfSSL (Formerly CyaSSL) Release 3.6.6 (08/20/2015)

Release 3.6.6 of wolfSSL has bug fixes and new features including:

- OpenSSH compatibility with `--enable-openssh`
- stunnel compatibility with `--enable-stunnel`
- lighttpd compatibility with `--enable-lighty`
- SSLv3 is now disabled by default, can be enabled with `--enable-ssl3`

- Ephemeral key cipher suites only are now supported by default To enable static ECDH cipher suites define WOLFSSL_STATIC_DH To enable static RSA cipher suites define WOLFSSL_STATIC_RSA To enable static PSK cipher suites define WOLFSSL_STATIC_PSK
- Added QSH (quantum-safe handshake) extension with `--enable-ntru`
- SRP is now part of wolfCrypt, enable with `--enable-srp`
- Certificate handshake messages can now be sent fragmented if the record size is smaller than the total message size, no user action required.
- DTLS duplicate message fixes
- Visual Studio project files now support DLL and static builds for 32/64bit.
- Support for new Freescale I/O
- FreeRTOS FIPS support
- No high level security fixes that requires an update though we always recommend updating to the latest

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/yaSSL/Docs.html>
 #wolfSSL (Formerly CyaSSL) Release 3.6.0 (06/19/2015)

Release 3.6.0 of wolfSSL has bug fixes and new features including:

- Max Strength build that only allows TLSv1.2, AEAD ciphers, and PFS (Perfect Forward Secrecy). With `--enable-maxstrength`
- Server side session ticket support, the example server and echoserver use the example callback `myTicketEncCb()`, see `wolfSSL_CTX_set_TicketEncCb()`
- FIPS version submitted for iOS.
- TI Crypto Hardware Acceleration
- DTLS fragmentation fixes
- ECC key check validation with `wc_ecc_check_key()`
- 32bit code options to reduce memory for Curve25519 and Ed25519
- wolfSSL JNI build switch with `--enable-jni`
- PicoTCP support improvements
- DH min ephemeral key size enforcement with `wolfSSL_CTX_SetMinDhKey_Sz()`
- KEEP_PEER_CERT and AltNames can now be used together
- ChaCha20 big endian fix
- SHA-512 signature algorithm support for key exchange and verify messages
- ECC make key crash fix on RNG failure, ECC users must update.
- Improvements to usage of time code.
- Improvements to VS solution files.
- GNU Binutils 2.24 ld has problems with some debug builds, to fix an ld error add `-fdebug-types-section` to `C_EXTRA_FLAGS`
- No high level security fixes that requires an update though we always recommend updating to the latest (except note 14, ecc RNG failure)

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/yaSSL/Docs.html>
 #wolfSSL (Formerly CyaSSL) Release 3.4.8 (04/06/2015)

Release 3.4.8 of wolfSSL has bug fixes and new features including:

- FIPS version submitted for iOS.
- Max Strength build that only allows TLSv1.2, AEAD ciphers, and PFS.
- Improvements to usage of time code.
- Improvements to VS solution files.

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/yaSSL/Docs.html>

#wolfSSL (Formerly CyaSSL) Release 3.4.6 (03/30/2015)

Release 3.4.6 of wolfSSL has bug fixes and new features including:

- Intel Assembly Speedups using instructions rdrand, rdseed, aesni, avx1/2, rorx, mulx, adox, adcx . They can be enabled with `--enable-intelasm`. These speedup the use of RNG, SHA2, and public key algorithms.
- Ed25519 support at the crypto level. Turn on with `--enable-ed25519`. Examples in `wolcrypt/test/test.c` `ed25519_test()`.
- Post Handshake Memory reductions. wolfSSL can now hold less than 1,000 bytes of memory per secure connection including cipher state.
- wolfSSL API and wolfCrypt API fixes, you can still include the `cyassl` and `ctaocrypt` headers which will enable the compatibility APIs for the foreseeable future
- INSTALL file to help direct users to build instructions for their environment
- For ECC users with the normal math library a fix that prevents a crash when verify signature fails. Users of 3.4.0 with ECC and the normal math library must update
- RC4 is now disabled by default in autoconf mode
- AES-GCM and ChaCha20/Poly1305 are now enabled by default to make AEAD ciphers available without a switch
- External ChaCha-Poly AEAD API, thanks to Andrew Burks for the contribution
- DHE-PSK cipher suites can now be built without ASN or Cert support
- Fix some NO MD5 build issues with optional features
- Freescale CodeWarrior project updates
- ECC curves can be individually turned on/off at build time.
- Sniffer handles Cert Status message and other minor fixes
- SetMinVersion() at the wolfSSL Context level instead of just SSL session level to allow minimum protocol version allowed at runtime
- RNG failure resource cleanup fix
- No high level security fixes that requires an update though we always recommend updating to the latest (except note 6 use case of ecc/normal math)

See INSTALL file for build instructions. More info can be found on-line at <http://wolfssl.com/yaSSL/Docs.html>

#wolfSSL (Formerly CyaSSL) Release 3.4.0 (02/23/2015)

Release 3.4.0 wolfSSL has bug fixes and new features including:

- wolfSSL API and wolfCrypt API, you can still include the cyassl and ctacrypt headers which will enable the compatibility APIs for the foreseeable future
- Example use of the wolfCrypt API can be found in wolfcrypt/test/test.c
- Example use of the wolfSSL API can be found in examples/client/client.c
- Curve25519 now supported at the wolfCrypt level, wolfSSL layer coming soon
- Improvements in the build configuration under AIX
- Microchip Pic32 MZ updates
- TIRTOS updates
- PowerPC updates
- Xcode project update
- Bidirectional shutdown examples in client/server with -w (wait for full shutdown) option
- Cycle counts on benchmarks for x86_64, more coming soon
- ALT_ECC_SIZE for reducing ecc heap use with fastmath when also using large RSA keys
- Various compile warnings
- Scan-build warning fixes
- Changed a memcpy to memmove in the sniffer (if using sniffer please update)
- No high level security fixes that requires an update though we always recommend updating to the latest

CyaSSL Release 3.3.0 (12/05/2014)

- Countermeasures for Handshake message duplicates, CHANGE CIPHER without FINISHED, and fast forward attempts. Thanks to Karthikeyan Bhargavan from the Prosecco team at INRIA Paris-Rocquencourt for the report.
- FIPS version submitted
- Removes SSLv2 Client Hello processing, can be enabled with OLD_HELLO_ALLOWED
- User can set minimum downgrade version with CyaSSL_SetMinVersion()
- Small stack improvements at TLS/SSL layer
- TLS Master Secret generation and Key Expansion are now exposed
- Adds client side Secure Renegotiation, * not recommended *
- Client side session ticket support, not fully tested with Secure Renegotiation
- Allows up to 4096bit DHE at TLS Key Exchange layer
- Handles non standard SessionID sizes in Hello Messages
- PicoTCP Support
- Sniffer now supports SNI Virtual Hosts
- Sniffer now handles non HTTPS protocols using STARTTLS
- Sniffer can now parse records with multiple messages
- TI-RTOS updates

- Fix for ColdFire optimized fp_digit read only in explicit 32bit case
- ADH Cipher Suite ADH-AES128-SHA for EAP-FAST

The CyaSSL manual is available at: <http://www.wolfssl.com/documentation/CyaSSL-↵Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 3.2.0 (09/10/2014)

Release 3.2.0 CyaSSL has bug fixes and new features including:

- ChaCha20 and Poly1305 crypto and suites
- Small stack improvements for OCSP, CRL, TLS, DTLS
- NTRU Encrypt and Decrypt benchmarks
- Updated Visual Studio project files
- Updated Keil MDK5 project files
- Fix for DTLS sequence numbers with GCM/CCM
- Updated HashDRBG with more secure struct declaration
- TI-RTOS support and example Code Composer Studio project files
- Ability to get enabled cipher suites, CyaSSL_get_ciphers()
- AES-GCM/CCM/Direct support for Freescale mmCAU and CAU
- Sniffer improvement checking for decrypt key setup
- Support for raw ECC key import
- Ability to convert ecc_key to DER, EccKeyToDer()
- Security fix for RSA Padding check vulnerability reported by Intel Security Advanced Threat Research team

The CyaSSL manual is available at: <http://www.wolfssl.com/documentation/CyaSSL-↵Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 3.1.0 (07/14/2014)

Release 3.1.0 CyaSSL has bug fixes and new features including:

- Fix for older versions of icc without 128-bit type
- Intel ASM syntax for AES-NI
- Updated NTRU support, keygen benchmark
- FIPS check for minimum required HMAC key length
- Small stack (--enable-smallstack) improvements for PKCS#7, ASN
- TLS extension support for DTLS
- Default I/O callbacks external to user
- Updated example client with bad clock test
- Ability to set optional ECC context info
- Ability to enable/disable DH separate from opensslextra

- Additional test key/cert buffers for CA and server
- Updated example certificates

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 3.0.2 (05/30/2014)

Release 3.0.2 CyaSSL has bug fixes and new features including:

- Added the following cipher suites:
 - TLS_PSK_WITH_AES_128_GCM_SHA256
 - TLS_PSK_WITH_AES_256_GCM_SHA384
 - TLS_PSK_WITH_AES_256_CBC_SHA384
 - TLS_PSK_WITH_NULL_SHA384
 - TLS_DHE_PSK_WITH_AES_128_GCM_SHA256
 - TLS_DHE_PSK_WITH_AES_256_GCM_SHA384
 - TLS_DHE_PSK_WITH_AES_128_CBC_SHA256
 - TLS_DHE_PSK_WITH_AES_256_CBC_SHA384
 - TLS_DHE_PSK_WITH_NULL_SHA256
 - TLS_DHE_PSK_WITH_NULL_SHA384
 - TLS_DHE_PSK_WITH_AES_128_CCM
 - TLS_DHE_PSK_WITH_AES_256_CCM
- Added AES-NI support for Microsoft Visual Studio builds.
- Changed small stack build to be disabled by default.
- Updated the [Hash](#) DRBG and provided a configure option to enable.

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 3.0.0 (04/29/2014)

Release 3.0.0 CyaSSL has bug fixes and new features including:

- FIPS release candidate
- X.509 improvements that address items reported by Suman Jana with security researchers at UT Austin and UC Davis
- Small stack size improvements, `--enable-smallstack`. Offloads large local variables to the heap. (Note this is not complete.)
- Updated AES-CCM-8 cipher suites to use approved suite numbers.

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.9.4 (04/09/2014)

Release 2.9.4 CyaSSL has bug fixes and new features including:

- Security fixes that address items reported by Ivan Fratric of the Google Security Team
- X.509 Unknown critical extensions treated as errors, report by Suman Jana with security researchers at UT Austin and UC Davis
- Sniffer fixes for corrupted packet length and Jumbo frames
- ARM thumb mode assembly fixes
- Xcode 5.1 support including new clang
- PIC32 MZ hardware support
- CyaSSL Object has enough room to read the Record Header now w/o allocs
- FIPS wrappers for AES, 3DES, SHA1, SHA256, SHA384, HMAC, and RSA.
- A sample I/O pool is demonstrated with `–enable-iopool` to overtake memory handling and reduce memory fragmentation on I/O large sizes

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.9.0 (02/07/2014)

Release 2.9.0 CyaSSL has bug fixes and new features including:

- Freescale Kinetis RNGB support
- Freescale Kinetis mmCAU support
- TLS Hello extensions
 - ECC
 - Secure Renegotiation (null)
 - Truncated HMAC
- SCEP support
 - PKCS #7 Enveloped data and signed data
 - PKCS #10 Certificate Signing Request generation
- DTLS sliding window
- OCSP Improvements
 - API change to integrate into Certificate Manager
 - IPv4/IPv6 agnostic
 - example client/server support for OCSP
 - OCSP nonces are optional
- GMAC hashing
- Windows build additions
- Windows CYGWIN build fixes
- Updated test certificates

- Microchip MPLAB Harmony support
- Update autoconf scripts
- Additional X.509 inspection functions
- ECC encrypt/decrypt primitives
- ECC Certificate generation

The Freescale Kinetis K53 RNGB documentation can be found in Chapter 33 of the K53 Sub-Family Reference Manual: http://cache.freescale.com/files/32bit/doc/ref_manual/K53P144M100SF2RM.pdf

Freescale Kinetis K60 mmCAU (AES, DES, 3DES, MD5, SHA, SHA256) documentation can be found in the "ColdFire/ColdFire+ CAU and Kinetis mmCAU Software Library User Guide": http://cache.freescale.com/files/32bit/doc/user_guide/CAUAPIUG.pdf

CyaSSL Release 2.8.0 (8/30/2013)

Release 2.8.0 CyaSSL has bug fixes and new features including:

- AES-GCM and AES-CCM use AES-NI
- NetX default IO callback handlers
- IPv6 fixes for DTLS Hello Cookies
- The ability to unload Certs/Keys after the handshake, CyaSSL_UnloadCertsKeys()
- SEP certificate extensions
- Callback getters for easier resource freeing
- External CYASSL_MAX_ERROR_SZ for correct error buffer sizing
- MacEncrypt and DecryptVerify Callbacks for User Atomic Record Layer Processing
- Public Key Callbacks for ECC and RSA
- Client now sends blank cert upon request if doesn't have one with TLS <= 1.2

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.7.0 (6/17/2013)

Release 2.7.0 CyaSSL has bug fixes and new features including:

- SNI support for client and server
- KEIL MDK-ARM projects
- Wildcard check to domain name match, and Subject altnames are checked too
- Better error messages for certificate verification errors
- Ability to discard session during handshake verify
- More consistent error returns across all APIs
- Ability to unload CAs at the CTX or CertManager level
- Authority subject id support for Certificate matching

- Persistent session cache functionality
- Persistent CA cache functionality
- Client session table lookups to push serverID table to library level
- Camellia support to sniffer
- User controllable settings for DTLS timeout values
- Sniffer fixes for caching long lived sessions
- DTLS reliability enhancements for the handshake
- Better ThreadX support

When compiling with Mingw, libtool may give the following warning due to path conversion errors:

```
1 libtool: link: Could not determine host file name corresponding to **
2 libtool: link: Continuing, but uninstalled executables may not work.
```

If so, examples and testsuite will have problems when run, showing an error while loading shared libraries. To resolve, please run "make install".

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.6.0 (04/15/2013)

Release 2.6.0 CyaSSL has bug fixes and new features including:

- DTLS 1.2 support including AEAD ciphers
- SHA-3 finalist Blake2 support, it's fast and uses little resources
- SHA-384 cipher suites including ECC ones
- HMAC now supports SHA-512
- Track memory use for example client/server with -t option
- Better IPv6 examples with --enable-ipv6, before if ipv6 examples/tests were turned on, localhost only was used. Now link-local (with scope ids) and ipv6 hosts can be used as well.
- Xcode v4.6 project for iOS v6.1 update
- [settings.h](#) is now checked in all *.c files for true one file setting detection
- Better alignment at SSL layer for hardware crypto alignment needs
 - Note, SSL itself isn't friendly to alignment with 5 byte TLS headers and 13 bytes DTLS headers, but every effort is now made to align with the CYASSL_GENERAL_ALIGNMENT flag which sets desired alignment requirement
- NO_64BIT flag to turn off 64bit data type accumulators in public key code
 - Note, some systems are faster with 32bit accumulators
- --enable-stacksize for example client/server stack use
 - Note, modern desktop Operating Systems may add bytes to each stack frame
- Updated compression/decompression with direct crypto access
- All ./configure options are now lowercase only for consistency

- ./configure builds default to fastmath option
 - Note, if on ia32 and building in shared mode this may produce a problem with a missing register being available because of PIC, there are at least 6 solutions to this: 1) `--disable-fastmath`, don't use fastmath 2) `--disable-shared`, don't build a shared library 3) `C_EXTRA_FLAGS=-DTFM_NO_ASM`, turn off assembly use 4) use clang, it just seems to work 5) play around with no PIC options to force all registers being open, e.g., `--without-pic` 6) if static lib is still a problem try removing fPIE
- Many new ./configure switches for option enable/disable for example
 - rsa
 - dh
 - dsa
 - md5
 - sha
 - arc4
 - null (allow NULL ciphers)
 - oldtls (only use TLS 1.2)
 - asn (no certs or public keys allowed)
- ./configure generates cyassl/options.h which allows a header the user can include in their app to make sure the same options are set at the app and CyaSSL level.
- autoconf no longer needs serial-tests which lowers version requirements of automake to 1.11 and autoconf to 2.63

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.5.0 (02/04/2013)

Release 2.5.0 CyaSSL has bug fixes and new features including:

- Fix for TLS CBC padding timing attack identified by Nadhem Alfaridan and Kenny Paterson: <http://www.isg.rhul.ac.uk/tls/>
- Microchip PIC32 (MIPS16, MIPS32) support
- Microchip MPLAB X example projects for PIC32 Ethernet Starter Kit
- Updated CTaoCrypt benchmark app for embedded systems
- 1024-bit test certs/keys and cert/key buffers
- AES-CCM-8 crypto and cipher suites
- Camellia crypto and cipher suites
- Bumped minimum autoconf version to 2.65, automake version to 1.12
- Addition of OCSP callbacks
- STM32F2 support with hardware crypto and RNG
- Cavium NITROX support

CTaoCrypt now has support for the Microchip PIC32 and has been tested with the Microchip PIC32 Ethernet Starter Kit, the XC32 compiler and MPLAB X IDE in both MIPS16 and MIPS32 instruction set modes. See the README located under the <cyassl_root>/mplabx directory for more details.

To add Cavium NITROX support do:

```
./configure --with-cavium=/home/user/cavium/software
```

pointing to your licensed cavium/software directory. Since Cavium doesn't build a library we pull in the cavium_↵common.o file which gives a libtool warning about the portability of this. Also, if you're using the github source tree you'll need to remove the -Wredundant-decls warning from the generated Makefile because the cavium headers don't conform to this warning. Currently CyaSSL supports Cavium RNG, AES, 3DES, RC4, HMAC, and RS↵A directly at the crypto layer. Support at the SSL level is partial and currently just does AES, 3DES, and RC4. RSA and HMAC are slower until the Cavium calls can be utilized in non blocking mode. The example client turns on cavium support as does the crypto test and benchmark. Please see the HAVE_CAVIUM define.

CyaSSL is able to use the STM32F2 hardware-based cryptography and random number generator through the STM32F2 Standard Peripheral Library. For necessary defines, see the CYASSL_STM32F2 define in [settings.↵h](#). Documentation for the STM32F2 Standard Peripheral Library can be found in the following document↵: http://www.st.com/internet/com/TECHNICAL_RESOURCES/TECHNICAL_LITERATURE/USER_MANUAL/DM00023896.pdf

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.↵pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.4.6 (12/20/2012)

Release 2.4.6 CyaSSL has bug fixes and a few new features including:

- ECC into main version
- Lean PSK build (reduced code size, RAM usage, and stack usage)
- FreeBSD CRL monitor support
- CyaSSL_peek()
- CyaSSL_send() and CyaSSL_recv() for I/O flag setting
- CodeWarrior Support
- MQX Support
- Freescale Kinetis support including Hardware RNG
- autoconf builds use jobserver
- cyassl-config
- Sniffer memory reductions

Thanks to Brian Aker for the improved autoconf system, make rpm, cyassl-config, warning system, and general good ideas for improving CyaSSL!

The Freescale Kinetis K70 RNGA documentation can be found in Chapter 37 of the K70 Sub-Family Reference Manual: http://cache.freescale.com/files/microcontrollers/doc/ref_manual/K70↵P256M150SF3RM.pdf

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.↵pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.4.0 (10/10/2012)

Release 2.4.0 CyaSSL has bug fixes and a few new features including:

- DTLS reliability
- Reduced memory usage after handshake
- Updated build process

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.3.0 (8/10/2012)

Release 2.3.0 CyaSSL has bug fixes and a few new features including:

- AES-GCM crypto and cipher suites
- make test cipher suite checks
- Subject AltName processing
- Command line support for client/server examples
- Sniffer SessionTicket support
- SHA-384 cipher suites
- Verify cipher suite validity when user overrides
- CRL dir monitoring
- DTLS Cookie support, reliability coming soon

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.2.0 (5/18/2012)

Release 2.2.0 CyaSSL has bug fixes and a few new features including:

- Initial CRL support (`--enable-crl`)
- Initial OCSP support (`--enable-ocsp`)
- Add static ECDH suites
- SHA-384 support
- ECC client certificate support
- Add medium session cache size (1055 sessions)
- Updated unit tests
- Protection against mutex reinitialization

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.0.8 (2/24/2012)

Release 2.0.8 CyaSSL has bug fixes and a few new features including:

- A fix for malicious certificates pointed out by Remi Gacogne (thanks) resulting in NULL pointer use.
- Respond to renegotiation attempt with no_renegotiation alert
- Add basic path support for load_verify_locations()
- Add set Temp EC-DHE key size
- Extra checks on rsa test when porting into

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.0.6 (1/27/2012)

Release 2.0.6 CyaSSL has bug fixes and a few new features including:

- Fixes for CA basis constraint check
- CTX reference counting
- Initial unit test additions
- Lean and Mean Windows fix
- ECC benchmarking
- SSMTTP build support
- Ability to group handshake messages with set_group_messages(ctx/ssl)
- CA cache addition callback
- Export Base64_Encode for general use

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.0.2 (12/05/2011)

Release 2.0.2 CyaSSL has bug fixes and a few new features including:

- CTaoCrypt Runtime library detection settings when directly using the crypto library
- Default certificate generation now uses SHAwRSA and adds SHA256wRSA generation
- All test certificates now use 2048bit and SHA-1 for better modern browser support
- Direct AES block access and AES-CTR (counter) mode
- Microchip pic32 support

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.0.0rc3 (9/28/2011)

Release 2.0.0rc3 for CyaSSL has bug fixes and a few new features including:

- updated autoconf support
- better make install and uninstall (uses system directories)
- make test / make check
- CyaSSL headers now in <cyassl/*.h>
- CTaocrypt headers now in <cyassl/ctaocrypt/*.h>
- OpenSSL compatibility headers now in <cyassl/openssl/*.h>
- examples and tests all run from home directory so can use certs in ./certs (see note 1)

So previous applications that used the OpenSSL compatibility header <openssl/ssl.h> now need to include <cyassl/openssl/ssl.h> instead, no other changes are required.

Special Thanks to Brian Aker for his autoconf, install, and header patches.

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.0.0rc2 (6/6/2011)

Release 2.0.0rc2 for CyaSSL has bug fixes and a few new features including:

- bug fixes (Alerts, DTLS with DHE)
- FreeRTOS support
- lwIP support
- Wshadow warnings removed
- asn public header
- CTaoCrypt public headers now all have ctc_ prefix (the manual is still being updated to reflect this change)
- and more.

This is the 2nd and perhaps final release candidate for version 2. Please send any comments or questions to support@yassl.com.

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 2.0.0rc1 (5/2/2011)

Release 2.0.0rc1 for CyaSSL has many new features including:

- bug fixes
- SHA-256 cipher suites
- Root Certificate Verification (instead of needing all certs in the chain)
- PKCS #8 private key encryption (supports PKCS #5 v1-v2 and PKCS #12)
- Serial number retrieval for x509

- PBKDF2 and PKCS #12 PBKDF
- UID parsing for x509
- SHA-256 certificate signatures
- Client and server can send chains (SSL_CTX_use_certificate_chain_file)
- CA loading can now parse multiple certificates per file
- Dynamic memory runtime hooks
- Runtime hooks for logging
- EDH on server side
- More informative error codes
- More informative logging messages
- Version downgrade more robust (use SSL_v23*)
- Shared build only by default through ./configure
- Compiler visibility is now used, internal functions not polluting namespace
- Single Makefile, no recursion, for faster and simpler building
- Turn on all warnings possible build option, warning fixes
- and more.

Because of all the new features and the multiple OS, compiler, feature-set options that CyaSSL allows, there may be some configuration fixes needed. Please send any comments or questions to support@yassl.com.

The CyaSSL manual is available at: <http://www.yassl.com/documentation/CyaSSL-Manual.pdf>. For build instructions and comments about the new features please check the manual.

CyaSSL Release 1.9.0 (3/2/2011)

Release 1.9.0 for CyaSSL adds bug fixes, improved TLSv1.2 through testing and better hash/sig algo ids, `--enable-webServer` for the yaSSL embedded web server, improper AES key setup detection, user cert verify callback improvements, and more.

The CyaSSL manual offering is included in the doc/ directory. For build instructions and comments about the new features please check the manual.

Please send any comments or questions to support@yassl.com.

CyaSSL Release 1.8.0 (12/23/2010)

Release 1.8.0 for CyaSSL adds bug fixes, x509 v3 CA signed certificate generation, a C standard library abstraction layer, lower memory use, increased portability through the `os_settings.h` file, and the ability to use NTRU cipher suites when used in conjunction with an NTRU license and library.

The initial CyaSSL manual offering is included in the doc/ directory. For build instructions and comments about the new features please check the manual.

Please send any comments or questions to support@yassl.com.

Happy Holidays.

CyaSSL Release 1.6.5 (9/9/2010)

Release 1.6.5 for CyaSSL adds bug fixes and x509 v3 self signed certificate generation.

For general build instructions see doc/Building_CyaSSL.pdf.

To enable certificate generation support add this option to ./configure ./configure --enable-certgen

An example is included in ctacrypt/test/test.c and documentation is provided in doc/CyaSSL_Extensions_↵
Reference.pdf item 11.

CyaSSL Release 1.6.0 (8/27/2010)

Release 1.6.0 for CyaSSL adds bug fixes, RIPEMD-160, SHA-512, and RSA key generation.

For general build instructions see doc/Building_CyaSSL.pdf.

To add RIPEMD-160 support add this option to ./configure ./configure --enable-ripemd

To add SHA-512 support add this option to ./configure ./configure --enable-sha512

To add RSA key generation support add this option to ./configure ./configure --enable-keygen

Please see ctacrypt/test/test.c for examples and usage.

For Windows, RIPEMD-160 and SHA-512 are enabled by default but key generation is off by default. To turn key generation on add the define CYASSL_KEY_GEN to CyaSSL.

CyaSSL Release 1.5.6 (7/28/2010)

Release 1.5.6 for CyaSSL adds bug fixes, compatibility for our JSSE provider, and a fix for GCC builds on some systems.

For general build instructions see doc/Building_CyaSSL.pdf.

To add AES-NI support add this option to ./configure ./configure --enable-aesni

You'll need GCC 4.4.3 or later to make use of the assembly.

CyaSSL Release 1.5.4 (7/7/2010)

Release 1.5.4 for CyaSSL adds bug fixes, support for AES-NI, SHA1 speed improvements from loop unrolling, and support for the Mongoose Web Server.

For general build instructions see doc/Building_CyaSSL.pdf.

To add AES-NI support add this option to ./configure ./configure --enable-aesni

You'll need GCC 4.4.3 or later to make use of the assembly.

CyaSSL Release 1.5.0 (5/11/2010)

Release 1.5.0 for CyaSSL adds bug fixes, GoAhead WebServer support, sniffer support, and initial swig interface support.

For general build instructions see doc/Building_CyaSSL.pdf.

To add support for GoAhead WebServer either --enable-opensslExtra or if you don't want all the features of opensslExtra you can just define GOAHEAD_WS instead. GOAHEAD_WS can be added to ./configure with CFL↵
AGS=-DGOAHEAD_WS or you can define it yourself.

To look at the sniffer support please see the sniffertest app in sslSniffer/sslSnifferTest. Build with --enable-sniffer on *nix or use the vcproj files on windows. You'll need to have pcap installed on *nix and WinPcap on windows.

A swig interface file is now located in the swig directory for using Python, Java, Perl, and others with CyaSSL. This is initial support and experimental, please send questions or comments to support@yassl.com.

When doing load testing with CyaSSL, on the echoserver example say, the client machine may run out of tcp ephemeral ports, they will end up in the TIME_WAIT queue, and can't be reused by default. There are generally two ways to fix this.

1. Reduce the length sockets remain on the TIME_WAIT queue OR
2. Allow items on the TIME_WAIT queue to be reused.

To reduce the TIME_WAIT length in OS X to 3 seconds (3000 milliseconds)

```
sudo sysctl -w net.inet.tcp.msl=3000
```

In Linux

```
sudo sysctl -w net.ipv4.tcp_tw_reuse=1
```

allows reuse of sockets in TIME_WAIT

```
sudo sysctl -w net.ipv4.tcp_tw_recycle=1
```

works but seems to remove sockets from TIME_WAIT entirely?

```
sudo sysctl -w net.ipv4.tcp_fin_timeout=1
```

doesn't control TIME_WAIT, it controls FIN_WAIT(2) contrary to some posts

CyaSSL Release 1.4.0 (2/18/2010)

Release 1.3.0 for CyaSSL adds bug fixes, better multi TLS/SSL version support through SSLv23_server_method(), and improved documentation in the doc/ folder.

For general build instructions doc/Building_CyaSSL.pdf.

CyaSSL Release 1.3.0 (1/21/2010)

Release 1.3.0 for CyaSSL adds bug fixes, a potential security problem fix, better porting support, removal of assert()s, and a complete THREADX port.

For general build instructions see rc1 below.

CyaSSL Release 1.2.0 (11/2/2009)

Release 1.2.0 for CyaSSL adds bug fixes and session negotiation if first use is read or write.

For general build instructions see rc1 below.

CyaSSL Release 1.1.0 (9/2/2009)

Release 1.1.0 for CyaSSL adds bug fixes, a check against malicious session cache use, support for lighttpd, and TLS 1.2.

To get TLS 1.2 support please use the client and server functions:

```
SSL_METHOD *TLSv1_2_server_method(void);
SSL_METHOD *TLSv1_2_client_method(void);
```

CyaSSL was tested against lighttpd 1.4.23. To build CyaSSL for use with lighttpd use the following commands from the CyaSSL install dir <CyaSSLDIR>:

```
1 ./configure --disable-shared --enable-opensslExtra --enable-fastmath --without-zlib
2
3 make
4 make openssl-links
```

Then to build lighttpd with CyaSSL use the following commands from the lighttpd install dir:

```
1 ./configure --with-openssl --with-openssl-includes=<CyaSSLDDir>/include --with-openssl-libs=<CyaSSLDDir>/lib
    LDFLAGS=-lm
2
3 make
```

On some systems you may get a linker error about a duplicate symbol for MD5_Init or other MD5 calls. This seems to be caused by the lighttpd src file md5.c, which defines MD5_Init(), and is included in liblightcomp_la-md5.o. When liblightcomp is linked with the SSL_LIBs the linker may complain about the duplicate symbol. This can be fixed by editing the lighttpd src file md5.c and adding this line to the beginning of the file:

```
#if 0
```

and this line to the end of the file

```
#endif
```

Then from the lighttpd src dir do a:

```
1 make clean
2 make
```

If you get link errors about undefined symbols more than likely the actual OpenSSL libraries are found by the linker before the CyaSSL openssl-links that point to the CyaSSL library, causing the linker confusion. This can be fixed by editing the Makefile in the lighttpd src directory and changing the line:

```
SSL_LIB = -lssl -lcrypto
```

to

```
SSL_LIB = -lcyassl
```

Then from the lighttpd src dir do a:

```
1 make clean
2 make
```

This should remove any confusion the linker may be having with missing symbols.

For any questions or concerns please contact support@yassl.com.

For general build instructions see rc1 below.

CyaSSL Release 1.0.6 (8/03/2009)

Release 1.0.6 for CyaSSL adds bug fixes, an improved session cache, and faster math with a huge code option.

The session cache now defaults to a client mode, also good for embedded servers. For servers not under heavy load (less than 200 new sessions per minute), define BIG_SESSION_CACHE. If the server will be under heavy load, define HUGE_SESSION_CACHE.

There is now a fasthugemath option for configure. This enables fastmath plus even faster math by greatly increasing the code size of the math library. Use the benchmark utility to compare public key operations.

For general build instructions see rc1 below.

CyaSSL Release 1.0.3 (5/10/2009)

Release 1.0.3 for CyaSSL adds bug fixes and add increased support for OpenSSL compatibility when building other applications.

Release 1.0.3 includes an alpha release of DTLS for both client and servers. This is only for testing purposes at this time. Rebroadcast and reordering aren't fully implemented at this time but will be for the next release.

For general build instructions see rc1 below.

CyaSSL Release 1.0.2 (4/3/2009)

Release 1.0.2 for CyaSSL adds bug fixes for a couple I/O issues. Some systems will send a SIGPIPE on socket `recv()` at any time and this should be handled by the application by turning off SIGPIPE through `setsockopt()` or returning from the handler.

Release 1.0.2 includes an alpha release of DTLS for both client and servers. This is only for testing purposes at this time. Rebroadcast and reordering aren't fully implemented at this time but will be for the next release.

For general build instructions see rc1 below.

CyaSSL Release Candidate 3 rc3-1.0.0 (2/25/2009)

Release Candidate 3 for CyaSSL 1.0.0 adds bug fixes and adds a project file for iPhone development with Xcode. `cyassl-iphone.xcodeproj` is located in the root directory. This release also includes a fix for supporting other implementations that bundle multiple messages at the record layer, this was lost when cyassl i/o was re-implemented but is now fixed.

For general build instructions see rc1 below.

CyaSSL Release Candidate 2 rc2-1.0.0 (1/21/2009)

Release Candidate 2 for CyaSSL 1.0.0 adds bug fixes and adds two new stream ciphers along with their respective cipher suites. CyaSSL adds support for HC-128 and RABBIT stream ciphers. The new suites are:

```
1 TLS_RSA_WITH_HC_128_SHA
2 TLS_RSA_WITH_RABBIT_SHA
```

And the corresponding cipher names are

```
1 HC128-SHA
2 RABBIT-SHA
```

CyaSSL also adds support for building with devkitPro for PPC by changing the library proper to use libogc. The examples haven't been changed yet but if there's interest they can be. Here's an example `./configure` to build CyaSSL for devkitPro:

```
1 ./configure --disable-shared CC=/pathTo/devkitpro/devkitPPC/bin/powerpc-gekko-gcc --host=ppc --without-zlib
   --enable-singleThreaded RANLIB=/pathTo/devkitpro/devkitPPC/bin/powerpc-gekko-ranlib CFLAGS="-DDEVKITPRO
   -DGEKKO"
```

For linking purposes you'll need

```
LDFLAGS="-g -mrvl -mcpu=750 -meabi -mhard-float -Wl,-Map,$(notdir $@).map"
```

For general build instructions see rc1 below.

CyaSSL Release Candidate 1 rc1-1.0.0 (12/17/2008)

Release Candidate 1 for CyaSSL 1.0.0 contains major internal changes. Several areas have optimization improvements, less dynamic memory use, and the I/O strategy has been refactored to allow alternate I/O handling or Library use. Many thanks to Thierry Fournier for providing these ideas and most of the work.

Because of these changes, this release is only a candidate since some problems are probably inevitable on some platform with some I/O use. Please report any problems and we'll try to resolve them as soon as possible. You can contact us at support@yassl.com or todd@yassl.com.

Using TomsFastMath by passing `--enable-fastmath` to `./configure` now uses assembly on some platforms. This is new so please report any problems as every compiler, mode, OS combination hasn't been tested. On ia32 all of the registers need to be available so be sure to pass these options to CFLAGS:

```
CFLAGS="-O3 -fomit-frame-pointer"
```

OS X will also need `-mdynamic-no-pic` added to CFLAGS

Also if you're building in shared mode for ia32 you'll need to pass options to LDFLAGS as well on OS X:

```
LDFLAGS=-Wl,-read_only_relocs,warning
```

This gives warnings for some symbols but seems to work.

To build on Linux, Solaris, *BSD, Mac OS X, or Cygwin:

```
./configure
make
```

from the `./testsuite/` directory run `./testsuite`

To make a debug build:

```
./configure --enable-debug --disable-shared
make
```

To build on Win32

Choose (Re)Build All from the project workspace

Run the testsuite program

CyaSSL version 0.9.9 (7/25/2008)

This release of CyaSSL adds bug fixes, Pre-Shared [Keys](#), over-rideable memory handling, and optionally TomsFastMath. Thanks to Moisés Guimarães for the work on TomsFastMath.

To optionally use TomsFastMath pass `--enable-fastmath` to `./configure` Or define `USE_FAST_MATH` in each project from CyaSSL for MSVC.

Please use the benchmark routine before and after to see the performance difference, on some platforms the gains will be little but RSA encryption always seems to be faster. On x86-64 machines with GCC the normal math library may outperform the fast one when using `CFLAGS=-m64` because TomsFastMath can't yet use `-m64` because of GCCs inability to do 128bit division.

```
*** UPDATE GCC 4.2.1 can now do 128bit division ***
```

See notes below (0.2.0) for complete build instructions.

CyaSSL version 0.9.8 (5/7/2008)

This release of CyaSSL adds bug fixes, client side Diffie-Hellman, and better socket handling.

See notes below (0.2.0) for complete build instructions.

CyaSSL version 0.9.6 (1/31/2008)

This release of CyaSSL adds bug fixes, increased session management, and a fix for gnutls.

See notes below (0.2.0) for complete build instructions.

CyaSSL version 0.9.0 (10/15/2007)

This release of CyaSSL adds bug fixes, MSVC 2005 support, GCC 4.2 support, IPV6 support and test, and new test certificates.

See notes below (0.2.0) for complete build instructions.

CyaSSL version 0.8.0 (1/10/2007)

This release of CyaSSL adds increased socket support, for non-blocking writes, connects, and interrupted system calls.

See notes below (0.2.0) for complete build instructions.

CyaSSL version 0.6.3 (10/30/2006)

This release of CyaSSL adds debug logging to stderr to aid in the debugging of CyaSSL on systems that may not provide the best support.

If CyaSSL is built with debugging support then you need to call `CyaSSL_Debugging_ON()` to turn logging on.

On Unix use `./configure --enable-debug`

On Windows define `DEBUG_CYASSL` when building CyaSSL

To turn logging back off call `CyaSSL_Debugging_OFF()`

See notes below (0.2.0) for complete build instructions.

CyaSSL version 0.6.2 (10/29/2006)

This release of CyaSSL adds TLS 1.1.

Note that CyaSSL has certificate verification on by default, unlike OpenSSL. To emulate OpenSSL behavior, you must call `SSL_CTX_set_verify()` with `SSL_VERIFY_NONE`. In order to have full security you should never do this, provide CyaSSL with the proper certificates to eliminate impostors and call `CyaSSL_check_domain_name()` to prevent man in the middle attacks.

See notes below (0.2.0) for build instructions.

CyaSSL version 0.6.0 (10/25/2006)

This release of CyaSSL adds more SSL functions, better autoconf, nonblocking I/O for accept, connect, and read. There is now an `--enable-small` configure option that turns off TLS, AES, DES3, HMAC, and `ERROR_STRINGS`, see `configure.in` for the defines. Note that TLS requires HMAC and AES requires TLS.

See notes below (0.2.0) for build instructions.

CyaSSL version 0.5.5 (09/27/2006)

This mini release of CyaSSL adds better input processing through buffered input and big message support. Added `SSL_pending()` and some sanity checks on user settings.

See notes below (0.2.0) for build instructions.

CyaSSL version 0.5.0 (03/27/2006)

This release of CyaSSL adds AES support and minor bug fixes.

See notes below (0.2.0) for build instructions.

CyaSSL version 0.4.0 (03/15/2006)

This release of CyaSSL adds TLSv1 client/server support and libtool.

See notes below for build instructions.

CyaSSL version 0.3.0 (02/26/2006)

This release of CyaSSL adds SSLv3 server support and session resumption.

See notes below for build instructions.

CyaSSL version 0.2.0 (02/19/2006)

This is the first release of CyaSSL and its crypt brother, CTaoCrypt. CyaSSL is written in ANSI C with the idea of a small code size, footprint, and memory usage in mind. CTaoCrypt can be as small as 32K, and the current client version of CyaSSL can be as small as 12K.

The first release of CTaoCrypt supports MD5, SHA-1, 3DES, ARC4, Big Integer Support, RSA, ASN parsing, and basic x509 (en/de)coding.

The first release of CyaSSL supports normal client RSA mode SSLv3 connections with support for SHA-1 and MD5 digests. [Ciphers](#) include 3DES and RC4.

To build on Linux, Solaris, *BSD, Mac OS X, or Cygwin:

```
./configure  
make
```

from the ./testsuite/ directory run ./testsuite

to make a debug build:

```
./configure --enable-debug --disable-shared  
make
```

To build on Win32

Choose (Re)Build All from the project workspace

Run the testsuite program

*** The next release of CyaSSL will support a server and more OpenSSL compatibility functions.

Please send questions or comments to todd@wolfssl.com

14 Examples and Demos

Applications that show the user how to initialize the peripherals for the basic use cases

14.1 Introduction

S32 SDK examples structure:

- [Demo Applications](#) (SDK/examples/<CPU>/demo_apps), are demo applications for various IDEs and compilers. Also this examples are using more advanced use-cases - FreeRTOS integration, LIN Stack, FlexCAN usage and Clock Setup.
- [Driver Examples](#) (SDK/examples/<CPU>/driver_examples), are simple applications which exemplify a basic use-case for a specific driver.

14.2 Usage

14.2.1 How to build

For makefile project

There are makefile projects in all compilers supported. In order to used them:

- **Make** utility (eg. GNU Make)
- **Toolchain** (eg. GCC Toolchain)
- **Make sure the make and compiler are in Path (for Microsoft Windows : System -> Environmental Variables)**
- From command line execute the makefile: **make all**

The makefiles generate binary files for both RAM and FLASH configurations.

For IAR Embedded Workbench

From IAR Workbench for ARM use File > Open > Workspace and browse to the desired project. After the project was opened you can see the files in "Workspace Files". Finally, the project can be executed from Project > Download and Debug. Make sure that the debug probe you are using is selected and configured in Project options > Debugger > Driver.

For S32 Design Studio

From S32 Design Studio (See Release notes for the S32 Design Studio version), go to File -> New -> New Project from Example and select the example you wish to import. This will copy the example project into workspace. Next steps:

- Examples will run without an active configuration, however if any changes are required, a configuration needs to be generated. Use Open S32 Configuration button, make the desired changes (if any) then click on the "Update Code" button.
- Use Project > Build to build the project
- Use Project > Debug and launch your preferred debug configuration

14.2.2 How to debug

This section explains how to upload and debug the binary files generated after build. This assumes that you have a debug probe(see release notes for supported debug probes) and a debug software installed on the machine.

Generic steps:

1. Launch the debug software
2. Load the binary file into the MCU
3. Execute the application

Loading with Segger JLink:

- Download and install the latest drivers and GDB server, named *Software and documentation pack*, from their [site](#)
- Download your favorite GDB client (eg. arm-none-eabi-gdb)
- Browse to JLink installation folder and launch **JLinkGDBServer**
- Select the appropriate part from the device list and click on **OK**
- Open the GDB client and connect to the configured port - by default localhost:2331
- Upload the file and execute (see GDB client user manual for details regarding the commands used)

The following table is a small list of commands used in GNU ARM GDB with JLinkGDBServer to connect and run the application:

Command	Description
target remote:PortNumber	Connect to the remote target at a specified port. Please replace PortNumber with the port configured in the GDB server.
monitor reset	Reset the target MCU
monitor halt	Halt the target MCU
file ApplicationName.elf	Load the file and symbols. Please change ApplicationName with your application name
load	Download the executable to the target MCU
continue	Begin executing the application

Loading with PEmicro OpenSDA/MultiLink:

- Download and install the latest drivers and GDB server, named *P&E GDB Server for Kinetis with Windows GUI*, from their [site](#)
- Download your favorite GDB client (eg. arm-none-eabi-gdb)
- Browse to PEmicro GDB Server installation folder and launch **P&E GDB Server for Kinetis**
- Select the appropriate part from the device list and click on **Connect**
- Open the GDB client and connect to the configured port - by default localhost:7224
- Upload the file and execute (see GDB client user manual for details regarding the commands used)

The following table is a small list of commands used in GNU ARM GDB with PEmicro GDB server to connect and run the application:

Command	Description
target remote:PortNumber	Connect to the remote target at a specified port. Please replace PortNumber with the port configured in the GDB server.
monitor reset	Reset the target MCU
file ApplicationName.elf	Load the file and symbols. Please change ApplicationName with your application name
load	Download the executable to the target MCU
continue	Begin executing the application

14.2.3 Using terminal emulator

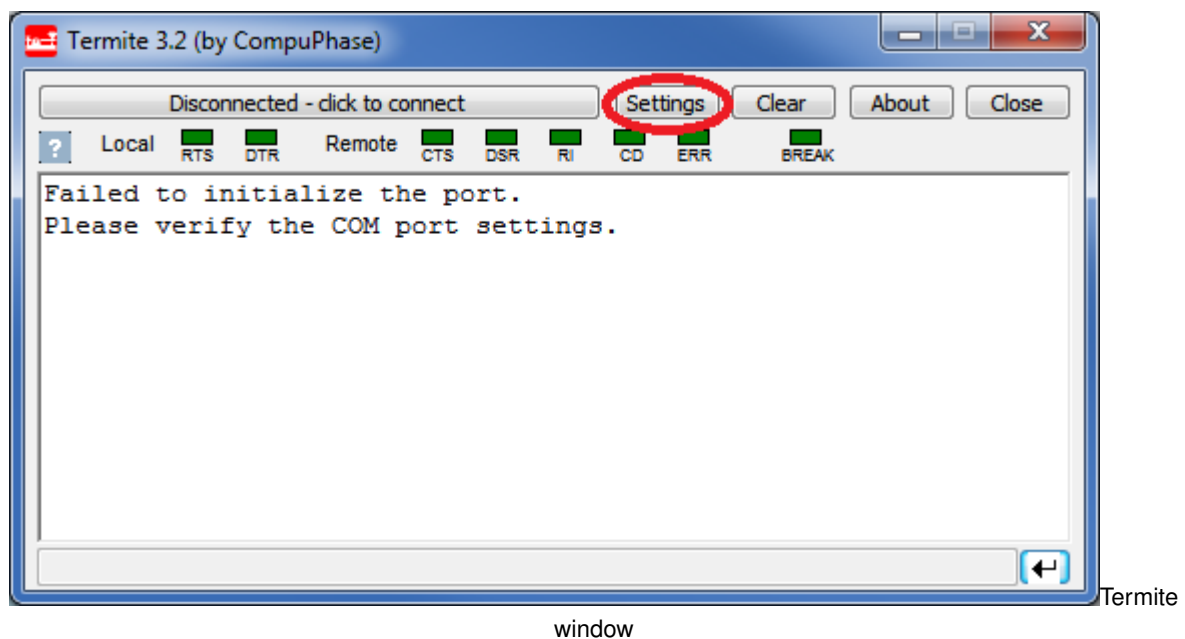
To run the examples that use LPUART to help you visualize data you must download a terminal emulator (eg. Putty, Termit, TeraTerm) and configure it.

Unless otherwise noted the standard communication parameters are:

- 115200 baud
- One stop bit
- No parity
- No flow control

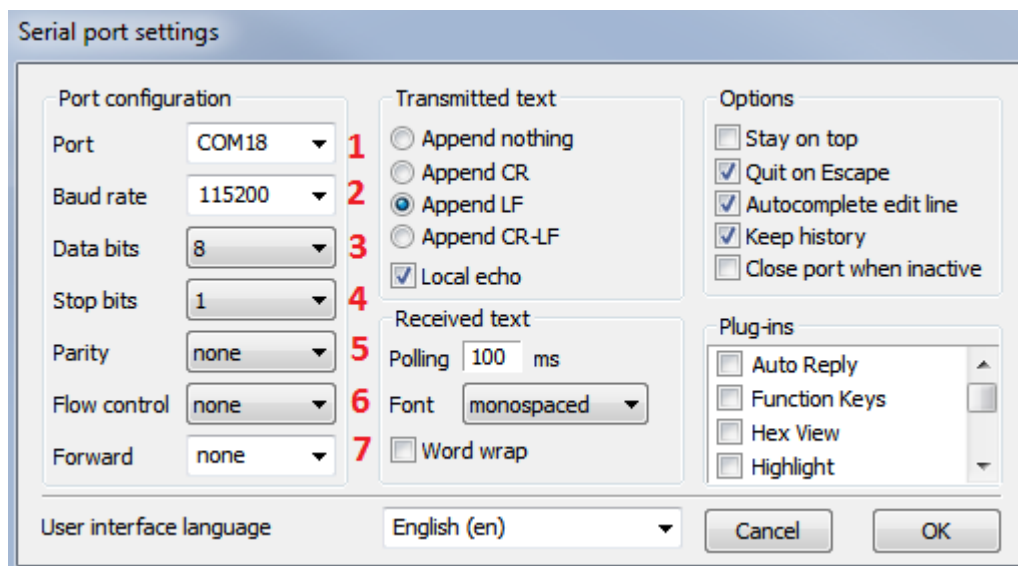
Example configuration for Terminate using OpenSDA

- 1) Download Terminate from their [site](#)
- 2) Run the installer. Wait for the installation to be completed
- 3) Go to **Start -> All Programs -> Terminate** and launch the program. The window from Fig.1 will appear ...



- 4) Click on **Settings**
- 5) As seen in Fig.2, configure the following communication parameters:

- **Port(1)** : COMx - where x must be replaced with the COM port number
- **Baud Rate(2)** : 115200
- **Data Bits(3)** : 8
- **Stop Bits(4)** : 1
- **Parity(5)** : None
- **Flow Control(6)** : None
- **Forward(7)** : None



Settings window

6) Click **OK**. Now the terminal should be configured

Note

For further help consult the terminal's documentation

14.3 Demo Applications

Applications that show more advanced use cases

Available demo applications:

Click on one of the project to see the corresponding documentation

- [Hello World](#)
- [Hello World - IAR Embedded Workbench](#)
- [Hello World - Makefile](#)
- [lwIP TCP/IP stack](#)
- [FlexCAN Encrypted](#)
- [CSEC BOOT PROTECTION](#)
- [FreeMASTER](#)
- [FreeRTOS](#)
- [ADC Low Power](#)

- [AMMCLib](#)
- [LIN MASTER](#)
- [LIN SLAVE](#)
- [Structural Core Self Test Example](#)
- [trcv_tja115x_transfer_s32k148_group](#)

14.3.1 Hello World

Basic application that presents the project scenarios for S32 SDK

Application description

The purpose of this demo is to provide the user with an out-of-the box example application for S32K148 platform, using S32 SDK. The demo uses hardware abstraction layer primitives for PCC and PORT modules in order to toggle two LEDs alternatively.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- Debug probe (JLink, PEmicro, OpenSDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **hello_world_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace. Wait for the S32 Configuration to be initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has a blue chip symbol on the top of the toolbar). In the S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
hello_world_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
hello_world_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
hello_world_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEmicro debuggers
hello_world_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEmicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.3.2 Hello World - IAR Embedded Workbench

Basic application that presents the project scenarios for S32 SDK and integration with IAR Embedded Workbench IDE

Application description

The purpose of this demo is to provide the user with an out-of-the box example application for S32K148 platform, using S32 SDK. The demo uses Clock Manager and Pins Driver to toggle two LEDs alternately.

Note

For information about how to run IAR projects please refer to [Usage](#)
The default debug probe is "Simulator". Prior to running the project on the board, the desired debug probe has to be configured in Project [Options](#) -> Debugger.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
RED_LED (PTD15)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTD16)	RGB_GREEN - wired on the board	J12.16 - J11.30

14.3.3 Hello World - Makefile

Basic application that presents the project scenarios for S32 SDK using makefiles for various compilers

Application description

The purpose of this demo is to provide the user with an out-of-the box example application for S32K148 platform, using S32 SDK. The demo uses Pins and Clock driver to initialize the MCU and to toggle two LEDs alternatively.

There are five projects delivered with this package:

- Makefile project (GCC compiler)
- Makefile project (GHS compiler)
- Makefile project (IAR compiler)
- Makefile project (DCC compiler)
- Makefile project (ARM compiler)

Note

For information about how to run the makefile please refer to [Usage](#)

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- Debug probe (JLink, PEmicro, OpenSDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
LED1 (PTD15/PTC0)	RGB_RED - wired on the board	J12.17 - J11.31
LED2 (PTD16/PTC1)	RGB_GREEN - wired on the board	J12.16 - J11.30

14.3.4 lwIP TCP/IP stack

Basic application that presents the lwIP usage with S32 SDK

Application description

The purpose of this demo is to provide the user with an out-of-the box example application for S32K148 platform, using S32 SDK. The demo uses lwIP stack and supports more scenarios, which can be enabled or disabled by modifying the settings from the Applications tab of the tcpip component.

Basic functionality can be checked by pinging the board from the host PC: ping 192.168.0.200

Please note that a prior setting of the IP on your PC might be needed. On Windows, this can be done from:

Control Panel > Network and Internet > Network and Sharing Center > Change adapter settings > Network adapter that connects to the board

Select **Internet Protocol Version 4** and click **Properties**; select **Use the following IP address** and configure the IP address and subnet mask. Configuration example: IP - 192.168.0.10, subnet mask - 255.255.255.0.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 EVB
- 1 TJA1100 daughter card
- 1 Power Adapter 12V
- 1 Personal Computer

- 1 Jlink Lite Debugger/ PEmicro Debugger (optional, users can use Open SDA)
- 1 BroadR-Reach Media Converter (if the transceiver on the board is a BroadR-Reach PHY)

The board should be powered by 12V power supply. Jumper settings on the board for 12V power supply as following: J18:1-2, J7:2-3, J8:1-2

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176 Rev C

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **lwip_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the tool-bar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lwip_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
lwip_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
lwip_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
lwip_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

5. Expected results after running the tests:

After executing "ping 192.168.0.200" cmd, ping should be successfully executed. The command windows will display something similar like this : Pinging 192.168.0.200 with 32 bytes of data: Reply from 192.168.0.200↵

```
: bytes=32 time<1ms TTL=128 Reply from 192.168.0.200: bytes=32 time<1ms TTL=128 Reply from 192.168.0.200: bytes=32 time<1ms TTL=128 Reply from 192.168.0.200: bytes=32 time<1ms TTL=128 Ping statistics for 192.168.0.200: Packets: Sent = 4, Received = 4, Lost = 0 (0% loss), Approximate round trip times in milli-seconds: Minimum = 0ms, Maximum = 0ms, Average = 0ms
```

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.3.5 FlexCAN Encrypted

Demo application showing the FlexCAN functionalities

Note

If running the encrypted communication: The encryption uses the first non-volatile user key, which needs to be configured by running the **CSEc Key Configuration** in the driver examples folder.

Encrypted communication works only for CSEc enabled parts. SIM_SDID indicates whether CSEc is available on your device.

If one of the user keys was loaded using the CSEc Key Configuration, any further full erase of the Flash requires a Challenge-Authentication process. This can be done by running the CSEc Key Configuration example again and setting the ERASE_ALL_KEYS macro to 1.

Application description

The purpose of this demo application is to show you the usage of the FlexCAN module configured to use Flexible Data Rate and the CSEc module from the S32K142 CPU using the S32 SDK API.

- In the first part, the application will setup the board clocks, pins and other system functions such as SBC if the board uses this module as a CAN transceiver.
- Then it will configure the FlexCAN module features such as FD, Bittime and Message buffers
- The application will wait for frames to be received on the configured message buffer or for an event raised by pressing one of the two buttons which will trigger a frame send to the recipient.
- Pressing SW4 button of board 1 shall trigger a CAN transfer that results in toggling the RED led on board 2.
- Pressing SW3 button of board 1 shall trigger a CAN transfer that results in toggling the GREEN led on board 2.
- Pressing both SW4 and SW3 buttons shall enable the encrypted communication. This event is signaled by the BLUE led being ON.
- The frames are sent in plain text by default.
- This demo application requires two boards, one configured as master and the other one configured as slave (see MASTER/SLAVE defines in application code).

Prerequisites

To run the example you will need to have the following items:

- 2 S32K148 board
- 1 Power Adapter 12V
- 3 Dupont female to female cable
- 1 Personal Computer
- 1 PEmicro Debugger / 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K142-MB
CAN HIGH (*)	CAN HIGH - J11.1	CAN HIGH - J60.2
CAN LOW (*)	CAN LOW - J11.2	CAN LOW - J60.3
GND (GND)	GND - J11.4	GND - J6
BUTTON 1 (PTC13)	SW4 - wired on the board	BTN2 - wired on the board
BUTTON 2 (PTC12)	SW3 - wired on the board	BTN3 - wired on the board
RED_LED (PTE21)	RGB_RED - wired on the board	LED3 - wired on the board
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	LED2 - wired on the board
BLUE_LED (PTE23)	RGB_BLUE - wired on the board	LED1 - wired on the board

(*) Those lines must be modulated using a transceiver, if it is not specified the boards already include the CAN transceiver. The CAN transceiver should be in Forced Normal Mode operation (default mode). To reset the CAN transceiver to default mode connect the SBC transceiver in next configuration with the board S32K148EVB-Q176 power off : • pin RSTN from SBC is held LOW • CANH(J11.1) is pulled up to VBAT(J11.3) • CANL(J11.2) is pulled down to GND(J11.4) Power on the board with external supply 12V (J9)

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **flexcan_encrypted_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32CT configuration

First go to **Project Explorer** View in S32 DS and select the current project(**flexcan_encrypted_s32k148**). Then go to **Project** and click on **Generate Processor Expert Code**

Wait for the code generation to be completed before continuing to the next step.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
flexcan_encrypted_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

flexcan_encrypted_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
flexcan_encrypted_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger J-Link debuggers
flexcan_encrypted_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger J-Link debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.3.6 CSEC BOOT PROTECTION

Basic application that presents the boot protection functionality of the CSEc module

Note

This example works only for CSEc enabled parts. SIM_SDID indicates whether CSEc is available on your device.

The first time when running the example on the board, or after a key erase, this example should be ran from RAM.

After the user key was loaded using this example, any further full erase of the Flash requires a Challenge-Authentication process. This can be done by setting the FLASH_MODIFY macro to 1.

After partitioning Flash for CSEc operation, using the JLink Flash configuration of any other project will not work anymore. Workaround:

- Run csec_boot_protection example with FLASH_MODIFY 1, using PEMicro Flash debug configuration

Application description

The purpose of this demo application is to show the user how to use the boot protection feature of the Cryptographic Services Engine module from the S32K148 MCU with the S32 SDK API.

The implementation demonstrates the following:

- the enablement of the CSEc module, by showing how the Flash should be partitioned (using the Flash driver);
- configuring the MASTER_ECU key;
- configuring the first user key, using the MASTER_ECU key as an authorization with boot protection enabled;
- configuring and enabling secure boot;
- availability of the user key after a secure boot when the flash was modified or not.
Erasing all the configured keys (including the MASTER_ECU key) and disabling the secure boot can be done by changing the value of the FLASH_MODIFY macro to 1. This will place the part back into factory status (the partition command will need to be run again).
Here is a table describing the outcome based on the value of FLASH_MODIFY and if the FLASH_TARGET is defined:

FLASH_MODIFY	FLASH_TARGET	Result
0	UNDEFINED	Write initial code to flash
1	UNDEFINED	Write modified code to flash
0	DEFINED	Write keys and enable secure boot
1	DEFINED	Erase keys and partition flash

Application usage

1. The first step is to run the application from RAM having the FLASH_MODIFY macro set to 1 in order to partition the flash. After this step, comment the #define INIT_PHASE line
2. Load the test program to it by setting the FLASH_MODIFY to 0 and running the application from FLASH.
3. Run the application from RAM with the FLASH_MODIFY macro set to 0 in order to load the keys necessary for secure boot and the test key with boot protection enabled.
4. Run the application from FLASH with the FLASH_MODIFY macro set to 0 in order to test secure boot. The secure boot process and the encryption using the test key should be successful.
5. Run the application from FLASH with the FLASH_MODIFY macro set to 1 this time in order to modify the flash. This will result in the secure boot to fail and the test key will be unavailable so the encryption operation will be unsuccessful.
6. Run the application from FLASH with the FLASH_MODIFY macro set to 0 in order to successfully secure boot. The test key is available again and the encryption operation is successful.
7. Set the FLASH_MODIFY macro to 1 and run the application from RAM in order to erase the keys and flash.

Note

If the FLASH_MODIFY is set to 1 at step 2 then the secure boots after the step 3 will be successful only if the FLASH_MODIFY macro is set to 1 and unsuccessful if it is set to 0.
If an assert fails at step 3, start over at step 1, uncommenting the #define INIT_PHASE line and setting FLASH_MODIFY to 1.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 PEmicro/Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From** and select **csec_boot_protection_↔s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
csec_boot_protection_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
csec_boot_protection_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
csec_boot_protection_s32k148_debug_ram_↔pemicro	Debug the RAM configuration using PEmicro debuggers
csec_boot_protection_s32k148_debug_flash_↔pemicro	Debug the FLASH configuration using PEmicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.3.7 FreeMASTER

Example application showing FreeMASTER Serial Communication usage

Application description

The purpose of this demo application is to show you how to use the FreeMASTER serial communication using S32K148 on OpenSDA with this SDK.

This demo uses the FreeMASTER Run-Time Debugging Tool to visualise ADC conversions and allows the user to monitor the ADC sampling rate for different ADC configurations (ADC sampling time and resolution can be controlled through FreeMASTER Application Commands).

The ADC is configured to perform continuous conversions and generate an interrupt after each conversion. The LPTMR is configured to generate a periodic interrupt at 10 ms which reads the number of ADC conversions.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V
- 1 Dupont male to male cable
- 1 Personal Computer
- Debug probe (JLink, PEmicro, OpenSDA)
- FreeMASTER host application

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
LPUART1 TX (PTC7)	UART_TX - wired on the board	J11.26 - J20.2
LPUART1 RX (PTC6)	UART_RX - wired on the board	J11.25 - J20.5
ADC0 Input 12 (PTC14)	POT - wired on the board	J21.1 - J11.18

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **freemaster_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace. Wait for the S32 Configuration to be initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has a blue chip symbol on the top of the toolbar). In the S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
freemaster_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
freemaster_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
freemaster_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
freemaster_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Open the FreeMASTER project (**freemaster_s32k148.pmp**) and set the communication parameters:

- Go to **Project** -> **Options** -> **Comm**, choose **Direct RS232** and set the COM port and speed 9600.
- Go to **Project** -> **Options** -> **MAP Files** and make sure the *.elf file of your project's current Debug Configuration is selected and set file format to ELF/DWARF.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

FreeMASTER host application can be downloaded from NXP's website. FreeMASTER Serial Communication is included into the project (V2.0).

14.3.8 FreeRTOS

Demo application showing the integration of FreeRTOS and S32 SDK

Application description

The purpose of this demo application is to show you how to use the FreeRTOS with the S32 SDK for the S32K148 MCU.

This project defines a very simple demo that creates two tasks, one queue, and one timer. It also demonstrates how Cortex-M4 interrupts can interact with FreeRTOS tasks/timers.

This simple demo project runs 'stand alone' (without the rest of the tower system) on the Freedom Board or Validation Board, which is populated with a S32K148 Cortex-M4 microcontroller.

The idle hook function: The idle hook function demonstrates how to query the amount of FreeRTOS heap space that is remaining (see vApplicationIdleHook() defined in this file).

The main() Function: main() creates one software timer, one queue, and two tasks. It then starts the scheduler.

The Queue Send Task: The queue send task is implemented by the `prvQueueSendTask()` function in this file. `prvQueueSendTask()` sits in a loop that causes it to repeatedly block for 200 milliseconds, before sending the value 100 to the queue that was created within `main()`. Once the value is sent, the task loops back around to block for another 200 milliseconds.

The Queue Receive Task: The queue receive task is implemented by the `prvQueueReceiveTask()` function in this file. `prvQueueReceiveTask()` sits in a loop that causes it to repeatedly attempt to read data from the queue that was created within `main()`. When data is received, the task checks the value of the data, and if the value equals the expected 100, toggles the green LED. The 'block time' parameter passed to the queue receive function specifies that the task should be held in the Blocked state indefinitely to wait for data to be available on the queue. The queue receive task will only leave the Blocked state when the queue send task writes to the queue. As the queue send task writes to the queue every 200 milliseconds, the queue receive task leaves the Blocked state every 200 milliseconds, and therefore toggles the green LED every 200 milliseconds.

The LED Software Timer and the Button Interrupt: The user button BTN1 is configured to generate an interrupt each time it is pressed. The interrupt service routine switches the red LED on, and resets the LED software timer. The LED timer has a 5000 millisecond (5 second) period, and uses a callback function that is defined to just turn the LED off again. Therefore, pressing the user button will turn the LED on, and the LED will remain on until a full five seconds pass without the button being pressed.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 2 Dupont male to male cable
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30
BTN (PTC13)	BTN1 - wired on the board	BTN3 - wired on the board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **freertos_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration to be initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code"

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
freertos_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
freertos_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
freertos_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEmicro debuggers
freertos_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEmicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.3.9 ADC Low Power

Demonstrates ADC trigger scheme using TRGMUX and LPIT, switches the power mode to stop and sends data using LPUART and DMA

Application description

The purpose of this demo application is to show you the usage of a subset of the peripherals found on the S32K148 SoC.

- The application uses LPIT to trigger ADC conversions every 100ms via TRGMUX with the CPU in sleep mode. The ADC is using Hardware Compare feature to validate an conversion only if the value is greater than half of the reference voltage, in this case **VDD/2**. This way the CPU is woken up from sleep mode only if the condition is met.
- When the conversion is complete the data is transformed into a bar graph and it is sent via LPUART using DMA memory to peripheral transfer to the host PC. This way, the CPU can be put into a low power mode to reduce the energy used.

How the example works:

- Connect to the serial port using settings found in Notes section

- The user should receive an information text on the terminal emulator
- The user must press "A" or "a" for the example to run
- The potentiometer must be rotated in order to generate valid ADC conversions
- Once a valid conversion is done then a bargraph will be printed on the terminal emulator

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
LPUART1 TX (PTC7)	UART_TX - wired on the board	J11.26 - J20.2
LPUART1 RX (PTC6)	UART_RX - wired on the board	J11.25 - J20.5
ADC0 Input 28 (PTC28)	POT - wired on the board	J21.1 - J11.18

Make sure the following jumpers are set:

Jumper Name	S32K148EVB-Q176
J5	Set jumper on position 2-3

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **adc_low_power_↔s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
adc_low_power_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
adc_low_power_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
adc_low_power_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
adc_low_power_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

For this example it is necessary to open a terminal emulator and configure it with:

- 115200 baud
- One stop bit
- No parity
- No flow control

14.3.10 AMMCLib

Provides an example of integration of AMMCLib and S32 SDK

Application description

The purpose of this demo application is to show you how to integrate the S32 SDK with AMMCLib.

The application starts by sending a welcome message to the terminal with instructions regarding how to select between the two parts:

1. The first part:

- The board sends a welcome message to the console with the supported operations and how to return to the menu.
- It uses LPUART to communicate with the user and get the simple mathematical expressions.
- The received expression is then interpreted and the result is calculated using mathematical functions from AMMCLib and then sent back to the terminal as a floating point with a precision of 4.

2. The second part:

- The board sends a welcome message to the console with further instructions and how to return to the menu.
- It uses LPTMR to generate samples of a sinusoidal signal, once every 1 ms, using trigonometric functions from the AMMCLib.
The sinusoidal signal can be seen using the FreeMASTER host application.
Calculated signal samples are then scaled to be in the range of the FTM PWM duty cycle and are used to change the intensity of the RGB leds.
The frequency of each sine can be controlled with the command `set_RGB_frequency()` from FreeMASTER project. The frequency sent is in mHz and the default value is 0,25Hz.
- Also, it implements an exponential moving average filter using the Potentiometer on ADC channel 12 as input.
The output of the filter can be seen using the FreeMASTER host application.
The filter's smoothing factor (λ) can be controlled using the command `set_FilterMA_lambda()` from FreeMASTER project.

Note

For more detailed information on the AMMCLib's functions please consult the available documentation.

Prerequisites

To run the example, you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from USB)
- 1 Personal Computer
- Debug probe (JLink, PEmicro, OpenSDA)
- FreeMASTER host application
- UART to USB converter if it is not included on the target board. (Please consult your boards documentation to check if UART-USB converter is present).

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K14xCVD-Q176 with S32K148 chip

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
FTM4 Channel 1 (PTE21)	RGB_RED - wired on the board
FTM4 Channel 2 (PTE22)	RGB_GREEN - wired on the board
FTM4 Channel 3 (PTE23)	RGB_BLUE - wired on the board

ADC0 Input 28 (PTC28)	POT - wired on the board
LPUART1 TX (PTC7)	UART_TX - wired on the board
LPUART1 RX (PTC6)	UART_RX - wired on the board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **ammclib_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace. Wait for the S32 Configuration to be initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has a blue chip symbol on the top of the toolbar). In the S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
ammclib_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
ammclib_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
ammclib_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEmicro debuggers
ammclib_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEmicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

A terminal emulator configured with the following communication parameters is needed by this application:

- 9600 Baud rate
- 8 Data bits
- 1 Stop bit
- No parity
- No flow control

For the first part of the application follow the instructions in the terminal.

For the second part of the application you need to:

1. exit the mathematical section by typing **exit** in the terminal

2. select second section by typing **2** in the terminal
3. disconnect the terminal and start FreeMASTER.

Open the FreeMASTER project (**ammclib.pmp**) and set the communication parameters:

- Go to **Project** -> **Options** -> **Comm**, choose **Direct RS232** and set the COM port and speed 9600.
- Go to **Project** -> **Options** -> **MAP Files** and make sure the *.elf file of your project's current Debug Configuration is selected and set file format to ELF/DWARF.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

FreeMASTER host application can be downloaded from [NXP's website](#).
FreeMASTER Serial Communication is included into the project (V2.0).

14.3.11 LIN MASTER

Example that shows the usage of the LIN driver in master mode

Application description

This example demonstrates the LIN communication between S32K148 Master and Slave using unconditional frames.

- The Master SeatECU is in NormalTable schedule table and it uses the LIN frame Motor1State_Cycl to receive temperature signal Motor1Temp from Slave Motor1 and send selection signal Motor1Selection to Slave Motor1 by frame Motor1Control. The first turn on GREEN_LED, then 5s GREEN_LED and BLUE_LED will toggle alternately.
- If value of temperature signal is higher than MOTOR1_OVER_TEMP value, Master SeatECU will send STOP command through Motor1Selection signal to stop motor and turn on RED_LED.
- If value of temperature signal is in range from MOTOR1_MAX_TEMP value to MOTOR1_OVER_TEMP value, master SeatECU will send DECREASE MOTOR SPEED command through Motor1Selection signal to reduce motor speed and turn on BLUE_LED.
- If value of temperature signal is lower than MOTOR1_MAX_TEMP value, master will send INCREASE MOTOR SPEED command through Motor1Selection signal to increase motor speed and turn on GREEN_LED.
- When users press button BUTTON 0 on the Master board, the Master SeatECU switches its schedule table to go-to-sleep table. So the Slave and Master enter sleep mode, RGB LEDS are off.
- When LIN cluster is in sleep mode, users press button BUTTON 1 on the Master board, the Master board sends a wakeup signal to wakeup slave nodes, then switches its table to NormalTable.

Prerequisites

To run the example you will need to have the following items:

- 2 S32K148 boards
- 1 Power Adapter 12V
- 2 Dupont female to female cable
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176 29644 PCB RevX1 SCH RevB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176-Slave	S32K148EVB-Q176-Master
BUTTON 0 (PTC12)	SW2 - wired on the board	SW2 - wired on the board
BUTTON 1 (PTC13)	SW3 - wired on the board	SW3 - wired on the board
RED_LED (PTE21)	RGB_RED - wired on the board	RGB_RED - wired on the board
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	RGB_GREEN - wired on the board
BLUE_LED (PTE23)	RGB_BLUE - wired on the board	RGB_BLUE - wired on the board
LIN (*)	J13-1 - LIN	J13-1 - LIN
GND (GND)	J13-4 - GND	J13-4 - GND

(*) Those lines must be modulated using a transceiver, if it is not specified the boards already include the LIN transceiver

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **lin_master_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**lin_master_s32k148**). Select the "ConfigTools" menu then click on the desired configuration (Pins, Clocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lin_master_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
lin_master_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation. The SBC's default mode is FORCE NORMAL mode. This mode enabled LIN transceiver. If SBC is another mode, user need move SBC to NORMAL mode by set SBC_FORCE_NORMAL_MODE to 0.

14.3.12 LIN SLAVE

Example that shows the usage of the LIN driver in slave mode

Application description

This example demonstrates the LIN communication between S32K148 Master and Slave using unconditional frames.

- The Master SeatECU is in NormalTable schedule table and it uses the LIN frame Motor1State_Cycl to receive temperature signal Motor1Temp from Slave Motor1 and send selection signal Motor1Selection to Slave Motor1 by frame Motor1Control. The first turn on GREEN_LED, then 5s GREEN_LED and BLUE_LED will toggle alternately.
- When user press button BUTTON 0 on the Slave board, value of temperature signal (Motor1_temp) will be increased 60 unit.
- When user press button BUTTON 1 on the Slave board, value of temperature signal will be set to value which is lower MOTOR1_MAX_TEMP value and turn on GREEN_LED.
- If value of temperature signal is higher than MOTOR1_OVER_TEMP value, Master SeatECU will send STOP command through Motor1Selection signal to stop motor and turn on RED_LED.
- If value of temperature signal is in range from MOTOR1_MAX_TEMP value to MOTOR1_OVER_TEMP value, master SeatECU will send DECREASE MOTOR SPEED command through Motor1Selection signal to reduce motor speed and turn on BLUE_LED.
- If value of temperature signal is lower than MOTOR1_MAX_TEMP value, master will send INCREASE MOTOR SPEED command through Motor1Selection signal to increase motor speed and turn on GREEN_LED.
- When users press button BUTTON 0 on the Master board, the Master SeatECU switches its schedule table to go-to-sleep table. So the Slave and Master enter sleep mode, all LEDs are off.
- When LIN cluster is in sleep mode, users press button BUTTON 1 on the Master board, the Master board sends a wakeup signal to wakeup slave nodes, then switches its table to NormalTable.

Prerequisites

To run the example you will need to have the following items:

- 2 S32K148 boards
- 1 Power Adapter 12V
- 2 Dupont female to female cable
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176 29644 PCB RevX1 SCH RevB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176-Slave	S32K148EVB-Q176-Master
BUTTON 0 (PTC12)	SW2 - wired on the board	SW2 - wired on the board
BUTTON 1 (PTC13)	SW3 - wired on the board	SW3 - wired on the board
RED_LED (PTE21)	RGB_RED - wired on the board	RGB_RED - wired on the board
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	RGB_GREEN - wired on the board
BLUE_LED (PTE23)	RGB_BLUE - wired on the board	RGB_BLUE - wired on the board
LIN (*)	J13-1 - LIN	J13-1 - LIN
GND (GND)	J13-4 - GND	J13-4 - GND

(*) Those lines must be modulated using a transceiver, if it is not specified the boards already include the LIN transceiver

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **lin_slave_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**lin_slave_s32k148**). Select the "ConfigTools" menu then click on the desired configuration (Pins, Clocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lin_slave_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
lin_slave_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation. The SBC's default mode is FORCE NORMAL mode. This mode enabled LIN transceiver. If SBC is another mode, user need move SBC to NORMAL mode by set SBC_FORCE_NORMAL_MODE to 0.

14.3.13 Structural Core Self Test Example

Basic application that presents the project scenarios for S32 SDK

Application description

The purpose of this demo application is to show you how to integrate the S32 SDK with sCST.

- The application will run the core self tests from the Structural Core Self Test library and will report the result using the user leds.
- Please consult the sCST manual for more information about the library.

Note

This application uses a modified version of the linker file which defines the section used by the library. As a consequence, the application will only run in flash.

Prerequisites

The run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- Debug probe (JLink, PEmicro, OpenSDA)

Boards supported

The following boards are supported by this application:

- S32K148EVb-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVb-Q176	S32K148-MB
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **scst_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be two debug configurations for this project:

Configuration Name	Description
scst_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
scst_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4 Driver Examples

Applications that show the user how to initialize the peripherals for the basic use cases

There are currently examples for the following categories:

Click on one of the categories to see the available projects

- [Analog Driver Examples](#)
- [Communication Driver Examples](#)
- [System Driver Examples](#)
- [Timer Driver Examples](#)

14.4.1 Analog Driver Examples

Applications that show the user how to initialize the analog peripherals

There are currently driver examples with the following modules:

Click on one of the module to see the available projects

- [ADC Hardware Trigger](#)
- [ADC PAL example](#)
- [ADC Software Trigger](#)
- [CMP DAC](#)

14.4.2 ADC Hardware Trigger

How to trigger the ADC by hardware

Application description

The purpose of this demo application is to show you the usage of the ADC module triggered in hardware by the Programmable Delay Block from the S32K148 CPU using the S32 SDK API.

- The application uses PDB to trigger ADC conversions every 1s.
- When the conversion is complete the data is sent to the host PC using LPUART.

See also

PDB_Example_group

For alternate ADC Hardware triggering scheme see ADC_LOW_POWER_group

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)
- UART to USB converter if it is not included on the target board. (Please consult your boards documentation to check if UART-USB converter is present).

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
LPUART1 TX (PTC7)	UART_TX - wired on the board	J11.26 - J20.2
LPUART1 RX (PTC6)	UART_RX - wired on the board	J11.25 - J20.5
ADC0 Input 28 (PTC28)	POT - wired on the board	J21.1 - J11.18

Make sure the following jumpers are set:

Jumper Name	S32K148EVB-Q176
J5	Set jumper on position 2-3

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **adc_hwtrigger_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace. Wait for the S32 Configuration to be initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
adc_hwtrigger_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
adc_hwtrigger_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
adc_hwtrigger_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
adc_hwtrigger_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

For this example it is necessary to open a terminal emulator and configure it with:

- 115200 baud
- One stop bit
- No parity
- No flow control

14.4.3 ADC PAL example

Example for ADC PAL usage

Application description

The purpose of this demo application is to present the basic functionality of the Analog to Digital Converter Peripheral Abstraction Layer (ADC PAL) on S32K14x MCU.

The application uses ADC PAL to trigger multiple executions of two groups of ADC conversions: first group configured for SW triggering and second group for HW triggering. For each execution of a group of conversions, an average conversion value is computed in SW, and the average value is printed on UART.

example is divided in 2 parts:

- Part 1: SW triggered group of conversions
After each complete execution of the group, results are read, the average value is calculated and printed to console. A delay is inserted and then the SW group is triggered again. The process is repeated for a fixed number of iterations.
- Part 2: HW triggered group of conversions
LPTMR is configured to provide a trigger event with a fixed periodicity. The selected HW group is enabled. After each complete execution of the group, results are read, the average value is calculated and printed to console. After a fixed number of iterations, the HW trigger group of conversions is disabled, and the LPTMR is stopped.

Note: both HW and SW triggered groups are configured to run all conversions on a single ADC InputChannel, because the development board contains only a single potentiometer connected to the MCU. However, the ADC PAL supports different InputChannels to be used in the same group. For more details please refer to the ADC PAL documentation.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)
- UART to USB converter if it is not included on the target board. (Please consult your boards documentation to check if UART-USB converter is present).

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
LPUART1 TX (PTC7)	UART_TX - wired on the board
LPUART1 RX (PTC6)	UART_RX - wired on the board
ADC0 Input 28 (PTC28)	POT - wired on the board

Make sure the following jumpers are set:

Jumper Name	S32K148EVb-Q176
J5	Set jumper on position 2-3

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **adc_pal_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace. Wait for the S32 Configuration to be initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
adc_pal_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
adc_pal_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
adc_pal_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEmicro debuggers
adc_pal_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEmicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

For this example it is necessary to open a terminal emulator and configure it with:

- 115200 baud
- One stop bit
- No parity
- No flow control

14.4.4 ADC Software Trigger

How to trigger ADC by software

Application description

The purpose of this demo application is to show you the usage of the ADC module triggered by software from the S32K148 CPU using the S32 SDK API.

- The application uses software to trigger ADC conversions every 1s.
- When the conversion is complete the data is sent to the host PC using LPUART.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)
- UART to USB converter if it is not included on the target board. (Please consult your boards documentation to check if UART-USB converter is present).

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
LPUART1 TX (PTC7)	UART_TX - wired on the board	J11.26 - J20.2
LPUART1 RX (PTC6)	UART_RX - wired on the board	J11.25 - J20.5
ADC0 Input 28 (PTC28)	POT - wired on the board	J21.1 - J11.18

Make sure the following jumpers are set:

Jumper Name	S32K148EVB-Q176
J5	Set jumper on position 2-3

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **adc_swtrigger_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration to be initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
adc_swtrigger_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
adc_swtrigger_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
adc_swtrigger_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
adc_swtrigger_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

For this example it is necessary to open a terminal emulator and configure it with:

- 115200 baud
- One stop bit
- No parity
- No flow control

14.4.5 CMP DAC

Driver examples showing the basic usage scenario of the CMP

Application description

The purpose of this demo application is to show you how to use the Analog Comparator of the S32K148 MCU using the S32 SDK API.

The Comparator is configured to compare analog input 0(AIN0) with half the reference voltage generated with the internal DAC. Based on the input from the potentiometer the LEDs light by the following rules:

- 1) $V_{in} < \text{DAC voltage}$: RED on, GREEN off
- 2) $V_{in} > \text{DAC voltage}$: RED off, GREEN on
- 3) Unknown state : RED on, GREEN on

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30
CMP Input 0 (PTA0)	J4.15 - J4.7	J21.1 - J9.31

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File** -> **New S32DS Project From...** and select **cmp_dac_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 Configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated.

The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar).

In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components.

Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user.

Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
cmp_dac_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
cmp_dac_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
cmp_dac_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
cmp_dac_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.6 Communication Driver Examples

Applications that show the user how to initialize the communication peripherals

There are currently driver examples with the following modules:

Click on one of the module to see the available projects

- [FLEXIO SPI](#)
- [ENET Loopback](#)
- [PHY TJA1101](#)
- [LPUART Echo](#)
- [UART PAL ECHO](#)
- [CAN PAL](#)
- [LPSPI Transfer](#)
- [LPSPI DMA](#)
- [SPI PAL](#)
- [SAI Transfer](#)
- [I2C PAL](#)
- [I2S PAL MASTER](#)

- [I2S PAL SLAVE](#)
- [FLEXIO I2C](#)
- [FLEXIO I2S MASTER](#)
- [FLEXIO I2S SLAVE](#)
- [FLEXIO UART](#)
- [LPI2C MASTER](#)
- [LPI2C SLAVE](#)
- [LIN MASTER BAREMETAL](#)
- [LIN SLAVE BAREMETAL](#)

14.4.7 FLEXIO SPI

Example application showing FlexIO SPI driver usage

Application description

The purpose of this demo application is to show you the usage of the FlexIO SPI driver found on the S32K148 SoC using S32 SDK API.

The application uses FlexIO SPI driver to make a data transfer of a defined size. The slave device for this example is a second FlexIO SPI driver using the same FlexIO instance, which is configured to act as a bus slave. The slave and master buffers will be checked after each transfer by the application, user shall check **isTransferOk** variable to see if the transmissions are successful(Green led will turn on), otherwise red led will turn on.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board can't be powered from the USB)
- 4 Dupont male to male cable
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
FLEXIO_MASTER CS (PTD19)	J6.22 - J6.28	J12.14 - J12.30
FLEXIO_MASTER SCK (PTD18)	J6.19 - J6.25	J12.12 - J12.29
FLEXIO_MASTER MOSI (PTC30)	J4.13 - J2.20	J11.1 - J13.21
FLEXIO_MASTER MISO (PTA11)	J5.6 - J2.23	J9.22 - J12.22
FLEXIO_SLAVE SS (PTD3)	J6.28 - J6.22	J12.30 - J12.14
FLEXIO_SLAVE SCK (PTD2)	J6.25 - J6.19	J12.29 - J12.12
FLEXIO_SLAVE MOSI (PTE10)	J2.20 - J4.13	J13.21 - J11.1
FLEXIO_SLAVE MISO (PTE11)	J2.23 - J5.6	J13.22 - J9.22
RED_LED (PTE21)	RGB_RED - wired on board	J13.12 - JP49.2
GREEN_LED (PTE22)	RGB_GREEN - wired on board	J13.9 - JP50.2

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File** -> **New S32DS Project From...** and select **flexio_spi_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There are four debug configurations for this project:

Configuration Name	Description
flexio_spi_s32k148_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
flexio_spi_s32k148_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
flexio_spi_s32k148_debug_ram_jlink	Debug the RAM configuration using Jlink debuggers
flexio_spi_s32k148_debug_flash_jlink	Debug the FLASH configuration using Jlink debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.8 ENET Loopback

Example application using the ENET driver

Application description

The purpose of this demo application is to show you how to use the ENET module from the S32K148 CPU using the S32 SDK API. The example continuously sends frames in loopback. Prior to sending a frame, the LED will be red. If the frame is successfully received, the LED will be green.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	12.16 - J11.30

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **enet_loopback_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
enet_loopback_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
enet_loopback_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
enet_loopback_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
enet_loopback_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.9 PHY TJA1101

Example application using the the PHY framework and TJA1101

Application description

The purpose of this demo application is to show you how to use the TJA1101 Ethernet PHY in conjunction with the S32K148 CPU using the S32 SDK API. The example performs initial configuration, monitors link status, and allows user interaction via push buttons.

There are in total three push buttons which can be used:

Button	Description
S32K148EVB BTN0	Toggle Loopback
S32K148EVB BTN1	Sleep request
TJA1101 WAKE	Wake request

BTN0 and BTN1 are connected as GPIOs to the processor. BTN0 allows to put the PHY into a loopback mode. This will also cause the Link to go up. BTN1 will trigger a sleep request. This will only work if another device is connected which supports TC10 wake/sleep. This can also be emulated by putting the device into loopback first. Pushing both buttons at the **same** time will change the master/slave mode selection. First activation will set it to master mode. Every following activation toggles mast/slave mode.

The button on the TJA1101 daughter card directly connects to the WAKE_IN_OUT pin of the PHY. When the device is in sleep, pushing the button will trigger a wake-up.

The current status of the PHY is indicated by the RGB LED. The following modes will be displayed.

LED status	Description
Red	Link down

Green	Link up
Blue	Sleep mode

Example usage: To go through all modes, press BTN0 to activate loopback. This will bring the Link up which is indicated by the green LED. Push BTN1 to set the device into sleep mode. Pushing the WAKE button on the TJA1101 daughter card will wake up the device, and the link should be back up.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 TJA1101 daughter card
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **phy_tja1101_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
phy_tja1101_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
phy_tja1101_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
phy_tja1101_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
phy_tja1101_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.10 LPUART Echo

Example application using the LPUART driver

Application description

The purpose of this demo application is to show you how to use the Low Power UART from the S32K148 CPU using the S32 SDK API.

- The welcome message is sent via UART: "This example is an simple echo using LPUART it will send back any character you send to it. The board will greet you if you send 'Hello Board' Now you can begin typing:" - User shall send "Hello Board" string. If the board receives the user's string, then the "Hello World" string shall be sent again. User need to add EOL character to string which will be sent to board.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 PEMicro debugger
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
LPUART1 TX (PTC7)	UART_TX - wired on the board	J11.26 - J20.2
LPUART1 RX (PTC6)	UART_RX - wired on the board	J11.25 - J20.5

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **lpuart_echo_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lpuart_echo_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
lpuart_echo_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
lpuart_echo_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
lpuart_echo_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

For this example it is necessary to open a terminal emulator and configure it with:

- 9600 baud
- One stop bit
- No parity
- No flow control
- '\n' line ending

14.4.11 UART PAL ECHO

Basic application that presents the project scenarios for S32 SDK

Application description

The purpose of this demo is to show the user how UART PAL works over FLEXIO_UART or LPUART peripherals. The user can choose whether to use FLEXIO_UART or LPUART (see USE_FLEXIO_UART define from The board sends a welcome message to the console with further instructions.)

- The welcome message is sent via UART: "This example is an simple echo using uart_pal_echo it will send back any character you send to it. The board will greet you if you send 'Hello!' Now you can begin typing:" - User shall send "Hello!" string. If the board receives the user's string, then the "Hello World!" string shall be sent again. User need to add EOL character to string which will be sent to board. Green led(devkit) or led 1(Motherboard) shall be turned on if the communication is done over FLEXIO_UART; similarly the led shall be turned off if the communication is done over LPUART.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 2 Dupont male to male cable
- 1 Personal Computer
- 1 PEmicro/Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	
LED1 (PTC1)		JP50 - jump 50 on motherboard
LPUART1 TX (PTC7)	UART_TX - wired on the board	J11.26 - J20.2
LPUART1 RX (PTC6)	UART_RX - wired on the board	J11.25 - J20.5
FLEXIO_UART RX (PTA0)	J6.11 - J4.15	J9.31 - J20.2
FLEXIO_UART TX (PTA11)	J6.8 - J5.6	J9.22 - J20.5

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **hello_world_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace. Wait for the S32 Configuration to be initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has a blue chip symbol on the top of the toolbar). In the S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
uart_pal_echo_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
uart_pal_echo_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
uart_pal_echo_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEmicro debuggers
uart_pal_echo_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEmicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

For this example it is necessary to open a terminal emulator and configure it with:

- 115200 baud
- One stop bit
- No parity
- No flow control
- '\n' line ending

14.4.12 CAN PAL

Demo application showing the CAN PAL functionalities

Application description

The purpose of this demo application is to show you the usage of the CAN PAL module configured to use Flexible Data Rate from the S32K148 CPU using the S32 SDK API.

- In the first part, the application will setup the board clocks, pins and other system functions such as SBC if the board uses this module as a CAN transceiver.
- Then it will configure the CAN PAL module features such as FD, Btrrate and buffers
- The application will wait for frames to be received on the configured buffer or for an event raised by pressing one of the two buttons which will trigger a frame send to the recipient.
- Pressing SW4 button of board 1 shall trigger a CAN transfer that results in toggling the RED led\ on board 2.
- Pressing SW3 button of board 1 shall trigger a CAN transfer that results in toggling the GREEN led on board 2.
- This demo application requires two boards, one configured as master and the other one configured as slave (see MASTER/SLAVE defines in application code).

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 2 Power Adapters 12V
- 3 Dupont female to female cable
- 1 Personal Computer
- 1 Jlink Lite Debugger/ PEmicro Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
CAN HIGH (*)	CAN HIGH - J11.1	CAN HIGH - J60.2
CAN LOW (*)	CAN LOW - J11.2	CAN LOW - J60.3
GND (GND)	GND - J11.4	GND - J6
BUTTON 1 (PTC13)	SW4 - wired on the board	BTN2 - wired on the board
BUTTON 2 (PTC12)	SW3 - wired on the board	BTN3 - wired on the board
RED_LED (PTE21)	RGB_RED - wired on the board	LED3 - wired on the board
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	LED2 - wired on the board

(*) Those lines must be modulated using a transceiver, if it is not specified the boards already include the CAN transceiver.

The CAN transceiver should be in Forced Normal Mode operation (default mode).

To reset the CAN transceiver to default mode connect the SBC transceiver in next configuration with the board S32K148EVB-Q176 power off:

- pin RSTN from SBC is held LOW
- CANH(J11.1) is pulled up to VBAT(J11.3)
- CANL(J11.2) is pulled down to GND(J11.4)

Power on the board with external supply 12V (J9)

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **can_pal_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace. Wait for the S32 Configuration to be initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has a blue chip symbol on the top of the toolbar). In the S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
can_pal_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
can_pal_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
can_pal_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEmicro debuggers
can_pal_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEmicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.13 LPSPi Transfer

Driver example that will show the LPSPi Master and Slave functionalities

Application description

The purpose of this application is to show the user how to use the Low Power Serial Peripheral Interface on the S32K148 using the S32 SDK API.

- The application uses two on board instances of LPSPI, one in master configuration and the other one is slave to communicate data via the SPI bus. Data will be gathered periodically from the ADC input and will be sent to the master device which transforms it into a PWM signal. In this way the potentiometer controls the LED intensity.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 4(6) Dupont male to male cables
- 1 Personal Computer
- 1 Jlink Lite Debugger or 1 PEmicro Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
LPSPi0 CS (PTB0)	J2.7 - J6.28	J10.31 - J12.30
LPSPi0 SCK (PTB2)	J2.16 - J6.29	J10.29 - J12.31
LPSPi0 MISO (PTE1)	J5.14 - J6.25	J13.32 - J12.29
LPSPi0 MOSI (PTB1)	J2.10 - J5.18	J10.27 - J12.32
LPSPi1 CS (PTD3)	J2.7 - J6.28	J10.31 - J12.30
LPSPi1 SCK (PTD0)	J2.16 - J6.29	J10.29 - J12.31
LPSPi1 MISO (PTD2)	J5.14 - J6.25	J13.32 - J12.29
LPSPi1 MOSI (PTD1)	J2.10 - J5.18	J10.27 - J12.32
ADC0 Input 28 (PTC28)	POT - wired on the board	J21.1 - J11.3
LED (PTE21)	LED - wired on the board	J13.12 - J5.13

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **lpspi_transfer_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 Configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated.

The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar).

In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components.

Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lpspi_transfer_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
lpspi_transfer_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
lpspi_transfer_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
lpspi_transfer_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.14 LPSPI DMA

Driver example that will show the LPSPI Master and Slave functionalities

Application description

The purpose of this application is to show you how to use the Low Power Serial Peripheral Interface on the S32K148 using the S32 SDK API.

The application uses two on board instances of LPSPI, one in master configuration and the other one is slave to communicate data via the SPI bus using DMA.

To check if the transmission is successful the user has to verify that the data sent is the same as the received data. If transfer is successful, RED led will be on, otherwise it will be off.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board

- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 4 Dupont male to male cables
- 1 Personal Computer
- 1 Jlink Lite Debugger or 1 PEMicro Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
LPSPi_MASTER CS (PTB0)	J2.7 - J6.28	PTB0 - PTD3
LPSPi_MASTER SCK (PTB2)	J2.16 - J5.15	PTB2 - PTB14
LPSPi_MASTER MOSI (PTE2)	J1.17 - J5.18	PTE2 - PTD1
LPSPi_MASTER MISO (PTE1)	J5.14 - J6.25	PTE1 - PTD2
LPSPi_SLAVE SS (PTD3)	J6.28 - J2.7	PTD3 - PTB0
LPSPi_SLAVE SCK (PTB14)	J5.15 - J2.16	PTB14 - PTB2
LPSPi_SLAVE MOSI (PTD1)	J5.18 - J1.17	PTD1 - PTE2
LPSPi_SLAVE MISO (PTD2)	J6.25 - J5.14	PTD2 - PTE1
LED (PTE21)	LED - wired on the board	J13.12 - J5.1

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File** -> **New S32DS Project From...** and select **lpspi_dma_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 Configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated.

The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar).

In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components.

Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user.

Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lpspi_dma_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
lpspi_dma_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
lpspi_dma_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
lpspi_dma_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.15 SPI PAL

Driver example using SPI

Application description

The purpose of this application is to show you how to use the LPSPI and FLEXIO Interfaces on the S32K148 using the S32 SDK API.

The application uses one board instance of LPSPI in slave configuration and one board instance of FLEXIO in master configuration to communicate data via the SPI bus using interrupts. It also verifies that the data sent is the same as the received data. If transfer is successful, RED led will be on, otherwise it will be off. The red led is turned on when data is sent correctly, and all the leds are off when data is incomplete or incorrect.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board can't be powered from the USB)
- 1 Personal Computer
- 4 Dupont male to male or female to female cable
- 1 Jlink Lite Debugger or 1 PEMicro Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
FLEXIO_MASTER CS (PTD19)	J6.22 - J2.7	PTD19 - PTB0
FLEXIO_MASTER SCK (PTD18)	J6.19 - J2.16	PTD18 - PTB2
FLEXIO_MASTER MOSI (PTC31)	J4.16 - J2.13	PTC31 - PTB3
FLEXIO_MASTER MISO (PTD0)	J6.29 - J2.10	PTD0 - PTB1
LPSPI_SLAVE SS (PTB0)	J2.7 - J6.22	PTB0 - PTD19
LPSPI_SLAVE SCK (PTB2)	J2.16 - J6.19	PTB2 - PTD18
LPSPI_SLAVE MOSI (PTB3)	J2.13 - J4.16	PTB3 - PTC31
LPSPI_SLAVE MISO (PTB1)	J2.10 - J6.29	PTB1 - PTD0
LED (PTE21)	LED - wired on the board	J13.12 - J5.1

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **spi_pal**. Then click on **Finish**.

The project should now be copied into your current workspace.

2. Generating the S32 Configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated.

The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar).

In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components.

Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user.

Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
spi_pal_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
spi_pal_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
spi_pal_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
spi_pal_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.16 SAI Transfer

Example application showing SAI driver usage

Application description

The purpose of this demo application is to show the usage of the SAI driver found on the S32K148 SoC using S32 SDK API.

The application uses SAI driver to make a data transfer of a defined size. SAI 0 instance shall be transmitter and SAI 1 instance shall be receiver. User can see other settings for SAI 0 and SAI 1 in S32 Configuration tool. To check if data is transferred correctly, put break point or let program run for about 2 second, then see if RecvData content is the same as SendData.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board can't be powered from the USB)
- 1 Personal Computer
- 1 Jlink Lite Debugger or 1 PEmicro Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
SAI0_DATA0 - SAI1_DATA0	P1.9 - P1.23
SAI0_BCLK - SAI1_BCLK	P1.11 - P1.25
SAI0_SYNC - SAI1_SYNC	P1.13 - P1.29

How to run**1. Importing the project into the workspace**

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **sai_transfer_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**sai_transfer_s32k148**). Select the "ConfigTools" menu then click on the desired configuration (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
sai_transfer_s32k148_debug_ram_jlink	Debug the RAM configuration using PEMicro debuggers
sai_transfer_s32k148_debug_flash_jlink	Debug the FLASH configuration using PEMicro debuggers
sai_transfer_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
sai_transfer_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.17 I2C PAL

Driver example using I2C

Application description

The purpose of this application is to show you how to use the LPI2C and FLEXIO Interfaces on the S32K148 using the S32 SDK API.

The application uses one board instance of LPI2C in slave configuration and one board instance of FLEXIO in master configuration to communicate data via the I2C bus using interrupts.

The RED or GREEN led will be turn on or turn off depending on the check result. Red led will turn on if data does not match. Green led will turn on if then data is transfered correctly.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board can't be powered from the USB)

- 1 Personal Computer
- 4 Dupont male to male cable
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
FLEXIO SDA (PTD0)	J6.29 - J4.16	J12.31 - J11.2
FLEXIO SCL (PTA11)	J5.6 - J5.14	J9.22 - J13.32
LPI2C SDA (PTC31)	J4.16 - J6.29	J11.2 - J12.31
LPI2C SCL (PTE1)	J5.14 - J5.6	J13.32 - J9.22

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **i2c_pal_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There are four debug configurations for this project:

Configuration Name	Description
i2c_pal_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers

i2c_pal_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
i2c_pal_s32k148_debug_ram_jlink	Debug the RAM configuration using Jlink debuggers
i2c_pal_s32k148_debug_flash_jlink	Debug the FLASH configuration using Jlink debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.18 I2S PAL MASTER

Driver example using I2S

Application description

The purpose of this application is to show you how to use the I2S_PAL on the S32K148.

The application uses one instance of FLEXIO in slave board and one instance of FLEXIO in master board to communicate data via the I2S bus using both of interrupts and DMA. The application will work in conjunction with the i2s_pal_slave demo on S32K1xx.

Run Slave first, after that run Master.

The slave buffers will be checked after each transfer by the application, RED or GREEN led will be lit depend on the check result. Red led will turn on if data does not match. Green led will turn on if then data is transferred correctly.

Note

After load the source code to flash memory and power cycle the boards maybe application will not work correctly due to noise. To fix this situation please keep power on and press reset button on boards.

Prerequisites

To run the example you will need to have the following items:

- 2 S32K148 board
- 1 Personal Computer
- 4 male to male jump wires
- 2 J-link Lite Debugger (optional, users can use Open SDA)
- 2 Power Adapter 12V (if the board can't be powered from the USB)

Boards supported

The following boards are supported by this application:

- S32K148-EVB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q64 MASTER	S32K148EVB-Q64 SLAVE
SCK	P1.11 (PTA12)	J2.20 (PTE10)
WS	P1.13 (PTA11)	J2.23 (PTE11)
MASTER TX - SLAVE RX	P1.9 (PTA13)	J3.23 (PTA9)
RED_LED (PTE7)	RGB_RED - wired on board	RGB_RED - wired on board
GREEN_LED (PTE0)	RGB_GREEN - wired on board	RGB_GREEN - wired on board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **i2s_pal_master_master_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**i2s_pal_master_master_s32k148**). Select the "ConfigTools" menu then click on the desired configuration (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be two debug configurations for this project:

Configuration Name	Description
i2s_pal_master_master_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
i2s_pal_master_master_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
i2s_pal_master_master_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
i2s_pal_master_master_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.19 I2S PAL SLAVE

Driver example using I2S

Application description

The purpose of this application is to show you how to use the I2S_PAL on the S32K148.

The application uses one instance of FLEXIO in slave board and one instance of FLEXIO in master board to communicate data via the I2S bus using both of interrupts and DMA. The application will work in conjunction with the `i2s_pal_master` demo on S32K1xx.

Run Slave first, after that run Master.

The slave buffers will be checked after each transfer by the application, RED or GREEN led will be lit depend on the check result. Red led will turn on if data does not match. Green led will turn on if then data is transferred correctly.

Prerequisites

To run the example you will need to have the following items:

- 2 S32K148 board
- 1 Personal Computer
- 4 male to male jump wires
- 2 J-link Lite Debugger (optional, users can use Open SDA)
- 2 Power Adapter 12V (if the board can't be powered from the USB)

Boards supported

The following boards are supported by this application:

- S32K148-EVB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q64 MASTER	S32K148EVB-Q64 SLAVE
SCK	P1.11 (PTA12)	J2.20 (PTE10)
WS	P1.13 (PTA11)	J2.23 (PTE11)
MASTER TX - SLAVE RX	P1.9 (PTA13)	J3.23 (PTA9)
RED_LED (PTE7)	RGB_RED - wired on board	RGB_RED - wired on board
GREEN_LED (PTE0)	RGB_GREEN - wired on board	RGB_GREEN - wired on board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select `i2s_pal_slave_master_↔s32k148`. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(`i2s_pal_slave_master_s32k148`). Select the "ConfigTools" menu then click on the desired configuration (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be two debug configurations for this project:

Configuration Name	Description
i2s_pal_slave_master_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
i2s_pal_slave_master_s32k148_debug_flash_↔ pemicro	Debug the FLASH configuration using PEmicro debuggers
i2s_pal_slave_master_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
i2s_pal_slave_master_s32k148_debug_ram_↔ pemicro	Debug the RAM configuration using PEmicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.20 FLEXIO I2C

Example application showing FlexIO I2C driver usage

Application description

The purpose of this demo application is to show you the usage of the FlexIO I2C driver found on the S32K148 SoC using S32 SDK API.

The application uses FlexIO I2C driver as master to make a send and a receive data request. The slave device for this example is the LPI2C instance, which is configured to act as a bus slave. The setup can't be changed to use FlexIO I2C as slave because this mode is not supported by FlexIO module. The slave and master buffers will be checked after each transfer by the application, user shall check **isTransferOk** variable to see if the transmissions are successful. If transfers is **Ok**, the **LED** on board will turn **Green**, otherwise the **LED** will turn **RED**.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148EVB-Q176 board
- 1 Power Adapter 12V (if the board can't be powered from the USB)
- 1 Personal Computer
- 1 PEmicro Multilink Debugger
- 1 Jlink Lite Debugger

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
FLEXIO SDA (PTA11)	J5.6 - J4.16	J9.22 - J11.2
FLEXIO SCL (PTA0)	J4.15 - J5.14	J9.31 - J13.32
LPI2C SDA (PTC31)	J4.16 - J5.6	J11.2 - J9.22
LPI2C SCL (PTE1)	J5.14 - J4.15	J13.32 - J9.31
RED_LED (PTE21)	RGB_RED - wired on board	
GREEN_LED (PTE22)	RGB_GREEN - wired on board	

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **flexio_i2c_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Debugging the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
flexio_i2c_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
flexio_i2c_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
flexio_i2c_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
flexio_i2c_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.21 FLEXIO I2S MASTER

Example application showing FlexIO I2S driver usage

Application description

The purpose of this demo application is to show you the usage of the FlexIO I2S driver found on the S32K148 SoC using S32 SDK API.

The application uses FlexIO I2S driver to make a data transfer of a defined size. The application will work in conjunction with the flexio_i2s_slave demo on S32K14x.

The application displays on the host PC terminal a menu in which the user can select to: For Slave board: "Press: 1) [Slave] Send data 2) [Slave] Received data Enter your input:"

For Master board: "Press: 1) [Master] Send data 2) [Master] Received data Enter your input:"

Select Send/Receive on Slave first. After that select Receive/Send on Master.

The slave buffers and master buffers will be checked after each transfer by the application, RED or GREEN led will be lit depend on the check result. Red led will turn if data does not match. Green led will turn if then data is transferred correctly.

The MASTER I2S driver is configured to use DMA for transfers.

Data size is configured by TRANSFER_SIZE define, by default is configured to be 64 Bytes.

Prerequisites

To run the example you will need to have the following items:

- 2 S32K148 board
- 2 Power Adapter 12V (if the board can't be powered from the USB)
- 4 Dupont male to male cable
- 1 Personal Computer
- 2 PEmicro Multilink Debugger (optional, users can use J-link)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work: Connect each FlexIO pin board master to pin board slave.

PIN FUNCTION	S32K148EVB-Q176 MASTER	S32K148EVB-Q176 SLAVE
--------------	------------------------	-----------------------

FLEXIO SCK	J6.29(PTD0)	J2.20(PTE10)
FLEXIO WS	J5.6(PTA11)	J2.23(PTE11)
FLEXIO MASTER TX - SLAVE RX	J4.15(PTA0)	J6.28(PTD3)
FLEXIO MASTER RX - SLAVE TX	J4.18(PTA1)	J6.25(PTD2)
RED_LED (PTE21)	RGB_RED - wired on board	RGB_RED - wired on board
GREEN_LED (PTE22)	RGB_GREEN - wired on board	RGB_GREEN - wired on board
UART	Wired on board	Wired on board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **flexio_i2s_master_↔s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Debugging the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
flexio_i2s_master_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
flexio_i2s_master_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
flexio_i2s_master_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
flexio_i2s_master_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

For this example it is necessary to open a terminal emulator and configure it with:

- 9600 baud
- One stop bit

- No parity
- No flow control
- '\n' line ending

14.4.22 FLEXIO I2S SLAVE

Example application showing FlexIO I2S driver usage

Application description

The purpose of this demo application is to show you the usage of the FlexIO I2S driver found on the S32K148 SoC using S32 SDK API.

The application uses FlexIO I2S driver to make a data transfer of a defined size. The application will work in conjunction with the flexio_i2s_master demo on S32K14x.

The application displays on the host PC terminal a menu in which the user can select to: For Slave board: "Press: 1) [Slave] Send data 2) [Slave] Received data Enter your input:"

For Master board: "Press: 1) [Master] Send data 2) [Master] Received data Enter your input:"

Select Send/Receive on Slave first. After that select Receive/Send on Master.

The slave buffers and master buffers will be checked after each transfer by the application, RED or GREEN led will be lit depend on the check result. Red led will turn if data does not match. Green led will turn if then data is transferred correctly.

The SLAVE I2S driver is configured to use interrupt for transfers.

Data size is configured by TRANSFER_SIZE define, by default is configured to be 64 Bytes.

Prerequisites

To run the example you will need to have the following items:

- 2 S32K148 board
- 2 Power Adapter 12V (if the board can't be powered from the USB)
- 4 Dupont male to male cable
- 1 Personal Computer
- 2 PEMicro Multilink Debugger (optional, users can use J-link)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work: Connect each FlexIO pin board master to pin board slave.

PIN FUNCTION	S32K148EVB-Q176 MASTER	S32K148EVB-Q176 SLAVE
FLEXIO SCK	J6.29(PTD0)	J2.20(PTE10)
FLEXIO WS	J5.6(PTA11)	J2.23(PTE11)
FLEXIO MASTER TX - SLAVE RX	J4.15(PTA0)	J6.28(PTD3)
FLEXIO MASTER RX - SLAVE TX	J4.18(PTA1)	J6.25(PTD2)
RED_LED (PTE21)	RGB_RED - wired on board	RGB_RED - wired on board
GREEN_LED (PTE22)	RGB_GREEN - wired on board	RGB_GREEN - wired on board
UART	Wired on board	Wired on board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **flexio_i2s_slave_↵s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Debugging the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
flexio_i2s_slave_s32k148debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
flexio_i2s_slave_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
flexio_i2s_slave_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
flexio_i2s_slave_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

For this example it is necessary to open a terminal emulator and configure it with:

- 9600 baud

- One stop bit
- No parity
- No flow control
- '\n' line ending

14.4.23 FLEXIO UART

Example application showing FlexIO UART driver usage

Application description

The purpose of this demo application is to show you the usage of the FlexIO UART driver found on the S32K148 SoC using S32 SDK API.

Two instances of the FlexIO UART driver are used to display a welcome message ("Hello World") and then echo the data received from host.

User shall send a string. If the board receives the user's string, then the same string shall be sent again.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board can't be powered from the USB)
- 2 Dupont female to female cable
- 1 Personal Computer
- 1 Jlink Lite Debugger or 1 PEmicro Debugger (optional, users can use Open SDA)
- UART to USB converter if it is not included on the target board. (Please consult your boards documentation to check if UART-USB converter is present).

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
FLEXIO_UART RX (PTA11)	J5.6 - J6.11
FLEXIO_UART TX (PTA0)	J4.15 - J6.8

Note

The application uses on board USB - UART chips to transfer data from board to host PC. Use an USB type B cable to connect to the J16 connector on the mainboard.

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **flexio_uart_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Debugging the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
flexio_uart_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
flexio_uart_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
flexio_uart_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
flexio_uart_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

For this example it is necessary to open a terminal emulator and configure it with:

- 115200 baud
- One stop bit
- No parity
- No flow control

14.4.24 LPI2C MASTER

Driver example that will show the LPI2C Master functionality

Application description

The purpose of this demo application is to show you the usage of the LPI2C module available on the S32K148 MCU as a **master** using S32 SDK.

- The application uses S32 SDK API to initialize the LPI2C module as a master node and in Fast operation speed after configuring the clocks and pins needed to use the I2C. The example sends to requests to a slave, found at the configured address, the first being a TX request, while the other being a RX request. Run Slave first, after that Run Master. The master buffers will be checked after each transfer by the application, RED or GREEN led will be turn on or turn off depending on the check result. Red led will turn on if data does not match. Green led will turn on if then data is transfered correctly.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 2 Dupont cables (male to male or female to female depending on the boards)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
LPI2C SCL (PTE1)	J5.14 - Slave SCL	J13.32 - Slave SCL
LPI2C SDA (PTC31)	J4.16- Slave SDA	J11.2 - Slave SDA
GND (GND)	J2.19 - Slave GND	J6 - Slave GND

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **lpi2c_master_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lpi2c_master_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
lpi2c_master_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
lpi2c_master_s32k148_debug_ram_jlink	Debug the RAM configuration using Jlink debuggers
lpi2c_master_s32k148_debug_flash_jlink	Debug the FLASH configuration using Jlink debugger

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.25 LPI2C SLAVE

Driver example that will show the LPI2C Slave functionality

Application description

The purpose of this demo application is to show you the usage of the LPI2C module available on the S32K148 MCU as a **slave** using S32 SDK.

- The application uses S32 SDK API to initialize the LPI2C module as a slave node and in Fast operation speed after configuring the clocks and pins needed to use the I2C. example uses the LPI2C callback to respond to requests such as:
 - data receive
 - data transmit
 - buffer full or empty. Run Slave first, after that Run Master. The slave buffers will be checked after each transfer by the application, RED or GREEN led will be turn on or turn off depending on the check result. Red led will turn on if data does not match. Green led will turn on if then data is transferred correctly.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 2 Dupont cables (male to male or female to female depending on the boards)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
LPI2C SCL (PTE1)	J5.14 - Master SCL	J13.32 - Master SCL
LPI2C SDA (PTC31)	J4.16 - Master SDA	J11.2 - Master SDA
GND (GND)	J2.19 - Master GND	J6 - Master GND

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New -> S32DS Project From** and select **lpi2c_slave_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lpi2c_slave_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
lpi2c_slave_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
lpi2c_slave_s32k148_debug_ram_jlink	Debug the RAM configuration using Jlink debuggers
lpi2c_slave_s32k148_debug_flash_jlink	Debug the FLASH configuration using Jlink debugger

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**. Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.26 LIN MASTER BAREMETAL

Example that shows the usage of the LIN driver in master mode

Application description

This example demonstrates the LIN communication between S32K148 EVB Master and Slave using LIN driver without LIN Stack

- A frame contains header and data. The Master node can send header and data, but Slave node only can send data. Base on header, Master node or Slave node will take corresponding action. On Master node:
- Press BUTTON 0:
 - For the first time, Master node sends FRAME_MASTER_RECEIVE_DATA header and require slave node responds by sending data (txBuff2).
 - For the second time, Master sends FRAME_SLAVE_RECEIVE_DATA header, then continue sending data (txBuff1) and slave node will receive the data.
 - If node successful receives data, this node will turn on GREEN_LED, otherwise turn on RED_LED.
- Press BUTTON 1:
 - Master node will check current node state. If the state is LIN_NODE_STATE_SLEEP_MODE, Master node will send wakeup signal and BLUE_LED will be turned on both nodes, otherwise Master node will send header to set Master node and Slave node to sleep mode and all LED will be turned off both nodes.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V
- 4 Dupont female to female cable
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176 29644 PCB RevX1 SCH RevB
- S32K-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K-MB
--------------	-----------------	---------

BUTTON 0 (PTC12)	SW3 - wired on the board	BTN2 - wired on the board
BUTTON 1 (PTC13)	SW4 - wired on the board	BTN3 - wired on the board
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30
BLUE_LED (PTE23)	RGB_BLUE - wired on the board	J12.31 - J11.29
GND (GND)	J13-4 - Slave GND	J6 - Slave GND
LIN (*)	J13-1 - Slave LIN	J48.4 - Slave LIN

(*) Those lines must be modulated using a transceiver, if it is not specified the boards already include the LIN transceiver. This example use LIN 0 interface on S32K148EVB-Q176.

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **lin_master_baremetal_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**lin_master_baremetal_s32k148**). Select the "ConfigTools" menu then click on the desired configuration (Pins, Clocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lin_master_baremetal_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
lin_master_baremetal_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
lin_master_baremetal_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEmicro debuggers
lin_master_baremetal_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEmicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation. The SBC's default mode is FORCE NORMAL mode. This mode enabled LIN transceiver. If SBC is another mode, user need move SBC to NORMAL mode by set SBC_FORCE_NORMAL_MODE to 0.

Notes

The default configuration of this example supports S32K148EVB-Q176.

14.4.27 LIN SLAVE BAREMETAL

Example that shows the usage of the LIN driver in slave mode

Application description

This example demonstrates the LIN communication between S32K148 EVB Master and Slave using LIN driver without LIN Stack

- A frame contains header and data. The Master node can send header and data, but Slave node only can send data. Base on header, Master node or Slave node will take corresponding action.
- If Slave node receives FRAME_MASTER_RECEIVE_DATA header, Slave node will respond by sending data (txBuff2).
- If Slave node receives FRAME_SLAVE_RECEIVE_DATA header, Slave node will receive and check data. If data is success, Slave node will turn on GREEN_LED, otherwise turn on RED_LED
- If Slave node receives FRAME_GO_TO_SLEEP header, Slave node will go to sleep mode and turn off all led.
- If Slave node receives a wakeup signal, it will check current node state, if the node state is sleep mode, Slave node will wakeup and turn on BLUE_LED, otherwise wakeup signal is aborted and keep the previous state.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V
- 4 Dupont female to female cable
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176 29644 PCB RevX1 SCH RevB
- S32K-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K-MB
BUTTON 0 (PTC12)	SW3 - wired on the board	BTN2 - wired on the board
BUTTON 1 (PTC13)	SW4 - wired on the board	BTN3 - wired on the board
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30
BLUE_LED (PTE23)	RGB_BLUE - wired on the board	J12.31 - J11.29
GND (GND)	J13-4 - Slave GND	J6 - Slave GND
LIN (*)	J13-1 - Slave LIN	J48.4 - Slave LIN

(*) Those lines must be modulated using a transceiver, if it is not specified the boards already include the LIN transceiver. This example use LIN 0 interface on S32K148EVb-Q176.

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **lin_slave_baremetal_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**lin_slave_baremetal_s32k148**). Select the "ConfigTools" menu then click on the desired configuration (Pins, Clocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lin_slave_baremetal_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
lin_slave_baremetal_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
lin_slave_baremetal_s32k148_debug_ram_↔ pemicro	Debug the RAM configuration using PEMicro debuggers
lin_slave_baremetal_s32k148_debug_flash_↔ pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation. The SBC's default mode is FORCE NORMAL mode. This mode enabled LIN transceiver. If SBC is another mode, user need move SBC to NORMAL mode by set SBC_FORCE_NORMAL_MODE to 0.

Notes

The default configuration of this example supports S32K148 EVb RevB.

14.4.28 System Driver Examples

Applications that show the user how to initialize the communication peripherals

There are currently driver examples with the following modules:
Click on one of the module to see the available projects

- [Trigger MUX Control](#)
- [CRC Checksum](#)
- [CSEc key configuration](#)
- [EDMA transfer](#)
- [EWM Interrupt](#)
- [FLASH Partitioning](#)
- [MPU Memory Protect Unit](#)
- [MPU PAL Memory Protection](#)
- [Power Mode Switch.](#)
- [WDOG Interrupt](#)
- [EIM INJECTION](#)
- [ERM REPORT](#)
- [WDG PAL Interrupt](#)
- [External Flash over QuadSPI](#)
- [SECURITY PAL](#)

14.4.29 Trigger MUX Control

Example application showing the usage of the TRGMUX module

Application description

The purpose of this demo application is to show you how to use the Trigger MUX Control of the S32K14x MCU with this SDK.

The examples use TRGMUX to connect Pin Trigger Mux In10 and LPIT channel 0.

- Initialize TRGMUX with source trigger from TRGMUX_IN10 and target module is LPIT_CH0

- Initialize the LPIT Channel 0.
- LED RED on EVB board or LED ORANGE on Motherboard is used to blink led
- Each time when user presses button SW3 on EVB board or SW4 on Motherboard will generate a trigger signal that activates LPIT channel 0 via TRGMUX. After 1ms, LPIT will create an event interrupt and toggle LED

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 PEmicro Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
RED_LED (PTE21)	RGB_RED - wired on the board	LED0 (JP49-2 connect J13-12)
BUTTON (PTC11)	SW3 (J1-7 connect J6-5)	SW4 (JP36-1 connect J11-22; JP63-1 connect JP63-2; JP64-2 connect JP64-3)

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **trgmux_ipit_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code". Wait for the code generation to be completed before continuing to the next step.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
trgmux_ipit_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
trgmux_ipit_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
trgmux_ipit_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
trgmux_ipit_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

The TRGMUX module in S32K platform supports both big endian and little endian in source data.

14.4.30 CRC Checksum

Example application showing the usage of the CRC module

Application description

The purpose of this demo application is to show you how to use the Cyclic Redundancy Check of the S32K148 with this SDK.

In this example, The CRC is configured to generate a configuration for CCITT standard following:

- CCITT 16 bits standard:

```
{
    .crcWidth = CRC_BITS_16,
    .seed = 0xFFFFU,
    .polynomial = 0x1021U,
    .writeTranspose = CRC_TRANSPOSE_NONE,
    .readTranspose = CRC_TRANSPOSE_NONE,
    .complementChecksum = false
}
```

The application:

1. After reset starts with both GREEN and RED LED turned off.
2. Initializes CRC module with the above CCITT 16 bits standard configuration.
3. Pressing the SW button CRC calculation is initialized with CRC_data array from input_data.c file.

4. If the result is correct GREEN LED is turned on. Otherwise RED LED will be turned on.
5. The program stops.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- Debug probe (JLink, PEmicro, OpenSDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
LED0 (PTE21/PTC0)	RGB_RED - wired on the board	J12.17 - J11.31
LED1 (PTE22/PTC1)	RGB_GREEN - wired on the board	J12.16 - J11.30
SW (PTC12/PTC12)	SW3 - wired on the board	BUTTON2 - wired on the board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From** and select **crc_checksum_s32k146**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
crc_checksum_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
crc_checksum_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
crc_checksum_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
crc_checksum_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Notes

The CRC module in S32K platform supports both big endian and little endian in source data.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.31 CSEc key configuration

Basic application that presents basic usecases for the CSEc driver

Note

This example works only for CSEc enabled parts. SIM_SDID indicates whether CSEc is available on your device.

The first time when running the example on the board, or after a key erase, this example should be ran from RAM.

The user keys are non-volatile. Once the key was loaded, in order to update it, the counter should be increased.

After the user key was loaded using this example, any further full erase of the Flash requires a Challenge-Authentication process. This can be done by setting the ERASE_ALL_KEYS macro to 1.

After partitioning Flash for CSEc operation, using the JLink Flash configuration of any other project will not work anymore. Workaround:

- Run csec_keyconfig example with ERASE_ALL_KEYS 1, using PEMicro Flash debug configuration

Application description

The purpose of this demo application is to show the user how to use the Cryptographic Services Engine module from the S32K148 MCU with the S32 SDK API.

The implementation demonstrates the following:

- the enablement of the CSEc module, by showing how the Flash should be partitioned (using the Flash driver);
- configuring the MASTER_ECU key;
- configuring the first user key, using the MASTER_ECU key as an authorization;
- using the user key for an encryption. In order to update the user key after they were configured using the example, the user should increase the counter used for loading the key. Please note that user should increase counter in order to keep the encryption take its place successfully for 2 cases:
- The user key was already loaded by previous run.

- The example already ran from RAM for CSEc partition. Erasing all the configured keys (including the MASTER_ECU key) can be done by changing the value of the ERASE_ALL_KEYS macro to 1. This will place the part back into factory status (the partition command will need to be run again). Please note that when the Flash is partitioned (the first time running the example on the board, or after a key erase), the example should not be run from Flash (please use the RAM configuration).

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 PEmicro/Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From** and select **csec_keyconfig_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
csec_keyconfig_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
csec_keyconfig_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
csec_keyconfig_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
csec_keyconfig_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.32 EDMA transfer

Example application showing the usage of the EDMA module

Application description

The purpose of this driver example is to show you how to use the eDMA in the following transfer scenarios for the S32K148 MCU using the S32 SDK API.

- Loop memory-to-memory transfer

If the application works correctly, the data shall be transferred correctly to destination memory and a transmission complete interrupt shall be triggered. And the application will not jump to any DEV_ASSERT.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board can't be powered from the USB)
- 1 Personal Computer
- 1 Jlink Lite Debugger or 1 PEMicro Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **edma_transfer_s32k148**. Then click on **Finish**.
The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**edma_transfer_s32k148**). Select the "Config↔Tools" menu then click on the desired configuration (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
edma_transfer_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
edma_transfer_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
edma_transfer_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
edma_transfer_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.33 EWM Interrupt

Driver example that shows the user how to use the External Watchdog Monitor

Application description

The purpose of this driver application is to show the user how to use the EWM from the S32K148 using the S32 SDK API.

Run the code

1. Turn off LED_RED and LED_GREEN.

2. The examples uses the SysTick timer from the ARM core to refresh the EWM counter for 30 times. After each refresh, LED_RED is also toggled. Within this interval the user can press the button associated with the EWM input pin to assert the interrupt and output pin.
3. After the EWM counter is refreshed 30 times or the user presses the button before refreshing ends, the EWM interrupt is triggered and both LED_RED and LED_GREEN are turned ON, then SysTick timer is disabled.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V
- 2 Dupont male to male cable
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
RED_LED (PTE21)	RGB_RED - wired on the board
GREEN_LED (PTE22)	RGB_GREEN - wired on the board
EWM INPUT (PTA14)	J6.5 (SW3_BTN0) - J1.20 (EWM INPUT)

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File** -> **New S32DS Project From...** and select **ewm_interrupt_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
ewm_interrupt_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
ewm_interrupt_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
ewm_interrupt_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
ewm_interrupt_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.34 FLASH Partitioning

Example application which shows the basic operations of the FLASH driver

Application description

The purpose of this demo application is to show you the usage of the FLASH driver with the S32 SDK API.

The examples does the following operations:

- Partitions the flash
- Configures FlexNVM region as EEPROM
- Erases flash
- Programs flash
- Write data to EEPROM. Check the status of API which confirms activities of flash module. In addition, user can view value at memory from address 0x17F000 when erases or programs flash. Checks the value at memory from address 0x14000000 when writes data to EEPROM.

Note

The FlexNVM memory is partitioned to EEPROM use and is blocked for some erase commands (Erase Sector and Erase Block). As a consequence, loading the program to flash memory may fail on some debuggers. Please perform a mass erase operation on Flash to remove this partitioning after running the example to be able to update your application on target.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)
- 1 micro_USB cable

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

No connections are required for this example.

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **flash_partitioning_↵ s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
flash_partitioning_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
flash_partitioning_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
flash_partitioning_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
flash_partitioning_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.35 MPU Memory Protect Unit

Basic application that presents the project scenarios for S32 SDK

Application description

The purpose of this demo application is to show you how to use the Memory Protection Unit of the S32K148 MCU with this SDK. In this example, MPU regions are configured to have access rights as following:

Region	Core	Debugger	DMA	Address
0	—	rwX	rwX	0x00000000 - 0xFFFFFFFF
1	rwX	rwX	rwX	0x00000000 - 0x0017FEFF
2	-wX	rwX	rwX	0x0017FF00 - 0x0017FF1F
3	r—	rwX	rwX	0x0017FF00 - 0x0017FF1F
4	rwX	rwX	rwX	0x0017FF20 - 0xFFFFFFFF

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Run the example

1. After reset, MPU will be initialized according to configuration above.
2. Read flash memory at address 0x0017FF04 is permitted.
3. Press button (SW) on the board to ignore read permission by disabling region 3.
4. Read flash memory at address 0x0017FF04 is violated.
5. MPU report the detail of error access on slave port 0 (Crossbar slave port 0 -> Flash Controller).

Verification

1. GREEN_LED on indicate that MPU initialization successful.
2. RED_LED on (GREEN_LED off) indicate that there is violated read access reported by MPU.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 PEmicro Debugger
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30
SW (PTC12)	SW3_BTN0 - wired on the board	BUTTON2 - wired on the board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **mpu_memory_↔ protection_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
mpu_memory_protection_s32k148_debug_ram_↔_jlink	Debug the RAM configuration using Segger Jlink debuggers
mpu_memory_protection_s32k148_debug_flash_↔_jlink	Debug the FLASH configuration using Segger Jlink debuggers
mpu_memory_protection_s32k148_debug_ram_↔_pemicro	Debug the RAM configuration using PEMicro debuggers
mpu_memory_protection_s32k148_debug_flash_↔_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.36 MPU PAL Memory Protection

Example application that shows how to use the MPU PAL

Application description

The purpose of this demo application is to show you how to use the Memory Protection Unit PAL of the S32K148 MCU with this SDK.

In this example, MPU PAL regions are configured to have access rights as following:

Region	Core	Debugger	DMA	ENET	Address
0	—	rwX	rwX	rwX	0x00000000 - 0xFFFFFFFF
1	rwX	rwX	rwX	rwX	0x00000000 - 0x0017FEFF
2	-wX	rwX	rwX	rwX	0x0017FF00 - 0x0017FF1F
3	r—	rwX	rwX	rwX	0x0017FF00 - 0x0017FF1F
4	rwX	rwX	rwX	rwX	0x0017FF20 - 0xFFFFFFFF

Run the example

1. After reset, MPU PAL will be initialized according to configuration above.
2. Read flash memory at address 0x0017FF04 is permitted.
3. Press button (SW) on the board to ignore read permission by disabling region 3.
4. Read flash memory at address 0x0017FF04 is violated.
5. MPU PAL report the detail of error access on slave port 0 (Crossbar slave port 0 -> Flash Controller).

Verification

1. GREEN LED on indicate that MPU PAL initialization successful.
2. RED LED on (GREEN LED off) indicate that there is violated read access reported by MPU PAL.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 PEmicro Debugger
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30
SW (PTC12)	SW3_BTN0 - wired on the board	BUTTON2 - wired on the board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **mpu_pal_memory_↔ protection_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
mpu_pal_memory_protection_s32k148_debug_↔ ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
mpu_pal_memory_protection_s32k148_debug_↔ flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
mpu_pal_memory_protection_s32k148_debug_↔ ram_pemicro	Debug the RAM configuration using PEMicro debuggers
mpu_pal_memory_protection_s32k148_debug_↔ flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.37 Power Mode Switch.

Example application demonstrating S32K148 power modes

Application description

The purpose of the application is to show the user how to enter various power modes of the S32K148 SoC using the S32 SDK API.

The application displays on the host PC terminal a menu in which the user can select to enter:

- High Speed Run (HSRUN)
- Normal Run (RUN)

- Very Low Power Run (VLPR)
- STOP mode 1 (STOP1)
- STOP mode 2 (STOP2)
- Very Low Power Stop (VLPS)

When user selects a mode, PC terminal will show the following text:

Press:

- 1) for HSRUN
- 2) for RUN
- 3) for VLPR
- 4) for STOP1
- 5) for STOP2
- 6) for VLPS

→ Press SW4 to wake up the CPU from STOP1, STOP2 or VLPS mode

Enter your input:

Expected Output:

- If STOP1, STOP2 or VLPS is selected by entering the character: '4', '5' or '6' into PC terminal, LED_RED will turn on, LED_GREEN will turn off and the PC terminal will show:

Mode	The content informs
STOP1	***** CPU is going in STOP1 mode...
STOP2	***** CPU is going in STOP2 mode...
VLPS	***** CPU is going in VLPS mode...

- The CPU can be woken up from sleep modes by pressing button SW4 in EVB board, then LED_RED turn off, LED_GREEN turn on and PC terminal will show:

Mode	The content informs
STOP1	CPU was entered STOP1 mode successfully and then woke up to exit STOP1 mode.
STOP2	CPU was entered STOP2 mode successfully and then woke up to exit STOP2 mode.
VLPS	CPU was entered VLPS mode successfully and then woke up to exit VLPS mode.

- If user selects HSRUN, RUN or VLPR, the PC terminal will show:

Mode	The content informs
HSRUN	***** CPU is in HSRUN mode ***** Core frequency: 112000000[Hz]
RUN	***** CPU is in RUN mode ***** Core frequency: 48000000[Hz]
VLPR	***** CPU is in VLPR mode ***** Core frequency: 4000000[Hz]

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
LPUART1 TX (PTC7)	UART_TX - wired on the board
LPUART1 RX (PTC6)	UART_RX - wired on the board
BUTTON (PTC13)	SW4 - wired on the board
LED_0	green led - wired on the board
LED_1	red led - wired on the board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From** and select **power_mode_switch_↔ s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated.

The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar).

In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components.

Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **RAM** (Debug_RAM) or **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
power_mode_switch_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
power_mode_switch_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
power_mode_switch_s32k148_debug_ram_↔ pemicro	Debug the RAM configuration using PEMicro debuggers
power_mode_switch_s32k148_debug_flash_↔ pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

Notes

For this example it is necessary to open a terminal emulator and configure it with:

- 9600 baud
- One stop bit
- No parity
- No flow control
- "\n" line ending

Clock source is remained in SIRC (8 MHz) before MCU switches from RUN to VLP mode.

In order to set to default clock for RUN mode. User presses option for RUN or re-initializes clock configuration.

14.4.38 WDOG Interrupt

Example application that will show the usage of the Watchdog

Application description

The purpose of this driver application is to show the user how to use the WDOG from the S32K148 using the S32 SDK API.

The examples uses the SysTick timer from the ARM core to refresh the WDOG counter for 8 times. After this the Watchdog counter will expire and the CPU will be reset. If the FLASH configuration will be used, then the code will use the Reset Control Module to detect if the reset was caused by the Watchdog and will stop the execution of the program.

Run the example on Devkit:

1. After reset, LED 0 and LED 1 is off.
2. Initialize WDOG Interrupt above then LED 0 is toggle 8 times(on 4 times and off 4 times).
3. Watchdog timeout happen then MCU reset and LED 0 and LED 1 is on and The program will stopped.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V
- 1 Personal Computer
- 1 PEmicro
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File** -> **New S32DS Project From...** and select **wdog_interrupt_s32k148**. Then click on **Finish**.
The project should now be copied into you current workspace.

2. Generating the S32CT configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be two debug configurations for this project:

Configuration Name	Description
wdog_interrupt_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
wdog_interrupt_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.39 EIM INJECTION

Driver example that shows the user how to use the Error Injection Module

Application description

The EIM module enables the user to inject 1 bit error or 2 bit errors into bus data, when read from a designated RAM area. The ECC module must correct all 1 bit errors. The ERM module reports any detected memory error. The example runs only on FLASH.

Run the code

1. After reset, LED_RED is turned off, LED_GREEN is turned on and the value of the test address is initialized.
2. Press button BUTTON0 to initialize the ERM and EIM modules.
3. Read the initialized address; if the value read from the test address is the same as the initialized value, then LED_GREEN will be turned off and LED_RED will be turned on.

If application runs success, LED_GREEN will be turned off and LED_RED will be turned on after press button 0.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger or 1 PEMicro Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
RED_LED (PTE21)	RGB_RED - wired on the board
GREEN_LED (PTE22)	RGB_GREEN - wired on the board
SW (PTC12)	SW3_BTN0 - wired on the board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File** -> **New S32DS Project From...** and select **eim_injection_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be one debug configuration for this project:

Configuration Name	Description
eim_injection_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
eim_injection_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.40 ERM REPORT

Driver example that shows the user how to use the Error reporting module

Application description

The EIM module enables the user to inject 1 bit error or 2 bit errors into bus data, when read from a designated RAM area. The ECC module must correct all 1 bit errors. The ERM module reports any detected memory error. The example runs only on FLASH

Run the code

1. After reset, LED_RED is turned off, LED_GREEN is turned on and the value for address used to test is initialized.
2. Press button SW3 to initialize ERM and EIM modules.
3. Read the address which was initialized, ERM will trigger an interrupt notification which also turns off LED_GREEN, and turns on the LED_RED to report a single-bit correction event.
4. Error event details are reported by ERM.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V
- 1 Personal Computer
- 1 Jlink Lite Debugger or 1 PEmicro Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
RED_LED (PTE21)	RGB_RED - wired on the board
GREEN_LED (PTE22)	RGB_GREEN - wired on the board
SW (PTC12)	SW3_BTN0 - wired on the board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **erm_report_s32k148**. Then click on **Finish**.
The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be one debug configuration for this project:

Configuration Name	Description
erm_report_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
erm_report_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.
This Example only run on Flash

14.4.41 WDG PAL Interrupt

Example application that will show the usage of the Watchdog

Application description

The purpose of this driver application is to show the user how to use the WDG PAL from the S32K148 using the S32 SDK API.

The example uses the SysTick timer from the ARM core to refresh the WDG PAL counter for 30 times. LED0 will toggle when WDG PAL counter is refreshed. After this the WDG PAL counter will expire, WDG PAL interrupt will happen and turn off LED0, LED1. Then the CPU will be reset. If the FLASH configuration will be used, then the program will use the Reset Control Module to detect if the reset was caused by the Watchdog and will stop the execution of the program and turn on LED0, LED1.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V
- 1 Personal Computer
- 1 PEMicro Debugger
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
LED0 (PTE21)	RGB_RED - wired on the boards	J12.17 - J11.31
LED1 (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **wdg_pal_interrupt_↔ s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code". Wait for the code generation to be completed before continuing to the next step.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be two debug configurations for this project:

Configuration Name	Description
wdg_pal_interrupt_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
wdg_pal_interrupt_s32k148_debug_flash_↔ pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.42 External Flash over QuadSPI

Driver example for external serial flash.

Application description

The purpose of this demo is to present the usage of the flash_mx25l6433f (external serial flash) and QSPI drivers. The flash_mx25l6433f driver allows the application to use an external Macronix MX25L6433F serial flash device, using the QuadSPI interface for communication.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
GPIO (PTE22)	LED_GREEN - wired on the board
Use the external power source	J8 - Set to position 1-2

Note: On the S32K148EVB-Q176 board, the external flash is by default not connected to the MCU. In order to run this example some hardware changes are required to the board:

Remove	Connect
R212	R213
R210	R211
R208	R209
R250	R244
R260	R254
R272	R271

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **qspi_external_flash_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**qspi_external_flash_s32k148**). Right click on the current project -> "S32 Configuration Tool" menu then click on the desired configuration (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration **FLASH** (Debug_FLASH) to be built by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There are two debug configuration for this project:

Configuration Name	Description
qspi_external_flash_s32k148_debug_flash_↔ pemicro	Debug the FLASH configuration using PEMicro debugger
qspi_external_flash_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debugger

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

5. Expected behaviour

After run Debug, the LED_GREEN wired on the board will be set.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.43 SECURITY PAL

Basic application that presents basic usecases for the Security PAL.

Note

This example works only for CSEc enabled parts. SIM_SDID indicates whether CSEc is available on your device.

The first time when running the example on the board, or after a key erase, this example should be ran from RAM.

This example generates a random number.

This example demonstrates CBC Encryption/Decryption.

Application description

The purpose of this demo application is to show the user how to use the Security PAL in conjunction with Cryptographic Services Engine module from the S32K14x MCU with the S32 SDK API.

The implementation demonstrates the following:

- the enablement of the Security PAL, used over CSEc module, by showing how the Flash should be partitioned (using the Flash driver);
- initializing the Random Number Generator and generating a vector of 128 random bits;
- configuring the RAM key, with a 128-bit plaintext;
- using the user key for a CBC encryption and a CBC decryption;

If no errors occur during the cryptographic operations, the green LED will be turned on upon completion; if the red LED is lit, the program failed during one of the steps.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 PEMicro/Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File** -> **New S32DS Project From...** and select **security_pal**. Select "Copy projects into workspace" and then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug** Configurations. There will be four debug configurations for this project:

Configuration Name	Description
security_pal_s32k148_debug_flash_jlink Debug_FLASH Jlink	Debug the FLASH configuration using Segger Jlink debuggers
security_pal_s32k148_debug_ram_jlink Debug_RAM Jlink	Debug the RAM configuration using Segger Jlink debuggers
security_pal_s32k148_debug_flash_pemicro Debug_FLASH PEMicro	Debug the FLASH configuration using PEMicro debuggers
security_pal_s32k148_debug_ram_pemicro Debug_RAM PEMicro	Debug the RAM configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.44 Timer Driver Examples

Applications that show the user how to initialize the timer peripherals

There are currently driver examples with the following modules:

Click on one of the module to see the available projects

- [FTM Combined PWM](#)
- [FTM Periodic Interrupt](#)
- [FTM PWM](#)
- [FTM Signal Measurement](#)
- [IC PAL](#)
- [LPTMR Periodic Interrupt](#)
- [LPTMR Pulse Counter](#)
- [PDB Periodic Interrupt](#)
- [RTC Alarm](#)
- [TIMING PAL](#)
- [PWM PAL](#)
- [OC PAL](#)
- [LPIT Periodic Interrupt](#)

14.4.45 FTM Combined PWM

Example application showing the FTM's combined PWM functionality

Application description

The purpose of this demo application is to show you the usage of the Combined PWM mode of the FlexTimer module on S32K148 using S32 SDK API

The example does the following operations:

- Increment or decrement duty cycle
- Update channel duty cycle
- Wait for a number of cycles to make the change visible

Run the example:

1. After run debug, the BLUE LED and GREEN LED of EVB board will increment or decrement light intensity
2. Use oscilloscope to verify the output signal

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
FTM4 Channel 2 (PTE22)	RGB_GREEN - wired on the board	J13.9 - J10.9
FTM4 Channel 3 (PTE23)	RGB_BLUE - wired on the board	J13.10 - J10.10

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **ftm_combined_pwm_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**ftm_combined_pwm_s32k148**). Right click on the current project -> "S32 Configuration Tool" menu then click on the desired configuration (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) to be built by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There are four debug configurations for this project:

Configuration Name	Description
ftm_combined_pwm_s32k148_debug_ram_↔ pemicro	Debug the RAM configuration using PEMicro debugger
ftm_combined_pwm_s32k148_debug_flash_↔ pemicro	Debug the FLASH configuration using PEMicro debugger
ftm_combined_pwm_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debugger
ftm_combined_pwm_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debugger

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.46 FTM Periodic Interrupt

Example application showing the FTM's Timer functionality

Application description

The purpose of this demo application is to show you the usage of the FlexTimer's Timer functionality on S32K148 using S32 SDK API

The example does the following operations:

- Configure FTM to generate an interrupt periodically
- The interrupt will blink the LED wired on the board

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
GPIO PIN	(PTE21) RGB_RED - wired on the board	(PTB22) LED0 - wired on the board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **ftm_periodic_interrupt_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**ftm_periodic_interrupt_s32k148**). Right click on the current project -> "S32 Configuration Tool" menu then click on the desired configuration (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) to be built by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There are four debug configurations for this project:

Configuration Name	Description
ftm_periodic_interrupt_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
ftm_periodic_interrupt_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
ftm_periodic_interrupt_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
ftm_periodic_interrupt_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.47 FTM PWM

Example application showing the FTM's PWM functionality

Application description

The purpose of this demo application is to show you the usage of the PWM mode of the FlexTimer module on S32K148 using S32 SDK API

The examples does the following operations:

- Increment or decrement duty cycle
- Update channel duty cycle
- Wait for a number of cycles to make the change visible

Run the example:

1. After run debug, the RED LED of EVB board will increment or decrement light intensity
2. Use oscilloscope to verify the output signal

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
FTM4 Channel 1 (PTE21)	RGB_RED - wired on the board	J11.31 - J12.18

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **ftm_pwm_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**ftm_pwm_s32k148**). Right click on the current project -> "S32 Configuration Tool" menu then click on the desired configuration (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) to be built by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There are four debug configurations for this project:

Configuration Name	Description
ftm_pwm_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debugger
ftm_pwm_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debugger
ftm_pwm_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debugger
ftm_pwm_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debugger

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.48 FTM Signal Measurement

Example application showing the FTM's Signal Measurement functionality

Application description

The purpose of this demo application is to show you the usage of the FlexTimer's Signal Measurement functionality on S32K148 using S32 SDK API

- The application is configured to generate a PWM signal with a variable frequency which will be measured by another FTM instance The frequency will range from 1000 Hz to 3000 Hz. Each step changes 100 Hz The measurement results will be sent to the host PC via LPUART User is able to compare pwm frequency and measurement frequency

The pwm frequency must be in measurable frequency range of FTM_IC. For example, here are the measurable ranges corresponding to the clock source = System clock (48 MHz)

Clock source prescaler	Maximum frequency (Hz)	Minimum frequency (Hz)
1	48,000,000	732.42
2	24,000,000	366.21
4	12,000,000	183.10
8	6,000,000	91.55
16	3,000,000	45.77
32	1,500,000	22.88
64	750,000	11.44
128	375,000	5.72

Note

Due to limited RAM size, this example contains only one build configuration for target flash memory (and the associated debug configuration)

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)
- 1 microUSB cable

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
FTM4 Out Channel 1 (PTE21)	J5.1 - J1.19	J11.31 - J10.29
FTM0 Input Channel 0 (PTD15)	J1.19 - J5.1	J10.29 - J11.31
LPUART1 TX (PTC7)	UART_TX - wired on the board	J11.26 - J20.2
LPUART1 RX (PTC6)	UART_RX - wired on the board	J11.25 - J20.5

Notes

For this example it is necessary to open a terminal emulator and configure it with:

- 9600 baud
- One stop bit
- No parity
- No flow control
- '\n' line ending

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **ftm_signal_↔ measurement_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**ftm_signal_measurement_s32k148**). Right click on the current project -> "S32 Configuration Tool" menu then click on the desired configuration (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration **FLASH** (Debug_FLASH) to be built by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There are two debug configurations for this project:

Configuration Name	Description
ftm_signal_measurement_s32k148_debug_↵ flash_pemicro	Debug the FLASH configuration using PEmicro debugger
ftm_signal_measurement_s32k148_debug_↵ flash_jlink	Debug the FLASH configuration using Segger Jlink debugger

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

5. Output display on Terminal

Welcome message:

```
This example will show you how to use FTM's signal measurement feature.
To achieve that we will generate a modifiable frequency PWM and read
it with Input Capture
Press any key to initiate a new conversion...
```

Expected output:

```
PWM frequency: 1000    Measured frequency: 1000    [Hz]
PWM frequency: 1100    Measured frequency: 1100    [Hz]
PWM frequency: 1200    Measured frequency: 1200    [Hz]
PWM frequency: 1300    Measured frequency: 1300    [Hz]
PWM frequency: 1400    Measured frequency: 1400    [Hz]
PWM frequency: 1500    Measured frequency: 1500    [Hz]
PWM frequency: 1600    Measured frequency: 1600    [Hz]
PWM frequency: 1700    Measured frequency: 1700    [Hz]
PWM frequency: 1800    Measured frequency: 1800    [Hz]
PWM frequency: 1900    Measured frequency: 1900    [Hz]
PWM frequency: 2000    Measured frequency: 2000    [Hz]
PWM frequency: 2100    Measured frequency: 2100    [Hz]
PWM frequency: 2200    Measured frequency: 2200    [Hz]
PWM frequency: 2300    Measured frequency: 2300    [Hz]
PWM frequency: 2400    Measured frequency: 2400    [Hz]
PWM frequency: 2500    Measured frequency: 2500    [Hz]
PWM frequency: 2600    Measured frequency: 2600    [Hz]
PWM frequency: 2700    Measured frequency: 2700    [Hz]
PWM frequency: 2800    Measured frequency: 2800    [Hz]
PWM frequency: 2900    Measured frequency: 2900    [Hz]
PWM frequency: 3000    Measured frequency: 3000    [Hz]
Press any key to initiate a new conversion...
```

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.49 IC PAL

Example application showing the IC's Signal Measurement functionality

Application description

The purpose of this demo application is to show you the usage of the IC's Signal Measurement functionality on S32K148 using S32 SDK API

- The application is configured to generate a PWM signal with a variable frequency which will be measured by IC_PAL. The frequency will range from 1000 Hz to 3000 Hz. Each step changes 100 Hz. The measurement result will be sent to the host PC via LPUART. User is able to compare pwm frequency and measurement frequency

Note

Due to limited RAM size, this example contains only one build configuration for target flash memory (and the associated debug configuration)

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)
- 1 microUSB cable

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
FTM4 Out Channel 1 (PTE21)	J5.1 - J1.19	J11.31 - J10.29
FTM0 Input Channel 0 (PTD15)	J5.1 - J1.19	J11.31 - J10.29
LPUART1 TX (PTC7)	UART_TX - wired on the board	J11.26 - J20.2
LPUART1 RX (PTC6)	UART_RX - wired on the board	J11.25 - J20.5

Notes

For this example it is necessary to open a terminal emulator and configure it with:

- 9600 baud
- One stop bit
- No parity
- No flow control
- '\n' line ending

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **ic_pal_s32k148**. Then click on **Finish**.

The project should now be copied into your current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**ic_pal_s32k148**). Right click on the current project -> "S32 Configuration Tool" menu then click on the desired configuration (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration **FLASH** (Debug_FLASH) to be built by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There are two debug configuration for this project:

Configuration Name	Description
ic_pal_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debugger
ic_pal_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debugger

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

5. Output display on Terminal

Welcome message:

```
This example will show you how to use IC's signal measurement feature.
To achieve that we will generate a modifiable frequency PWM and read
it with Input Capture
Press any key to initiate a new conversion...
```

Expected output:

```
PWM frequency: 1000      Measured frequency: 1000      [Hz]
PWM frequency: 1100      Measured frequency: 1100      [Hz]
PWM frequency: 1200      Measured frequency: 1200      [Hz]
PWM frequency: 1300      Measured frequency: 1300      [Hz]
PWM frequency: 1400      Measured frequency: 1400      [Hz]
PWM frequency: 1500      Measured frequency: 1500      [Hz]
PWM frequency: 1600      Measured frequency: 1600      [Hz]
PWM frequency: 1700      Measured frequency: 1700      [Hz]
PWM frequency: 1800      Measured frequency: 1800      [Hz]
PWM frequency: 1900      Measured frequency: 1900      [Hz]
PWM frequency: 2000      Measured frequency: 2000      [Hz]
PWM frequency: 2100      Measured frequency: 2100      [Hz]
PWM frequency: 2200      Measured frequency: 2200      [Hz]
PWM frequency: 2300      Measured frequency: 2300      [Hz]
PWM frequency: 2400      Measured frequency: 2400      [Hz]
PWM frequency: 2500      Measured frequency: 2500      [Hz]
PWM frequency: 2600      Measured frequency: 2600      [Hz]
PWM frequency: 2700      Measured frequency: 2700      [Hz]
```

```

PWM frequency: 2800      Measured frequency: 2800      [Hz]
PWM frequency: 2900      Measured frequency: 2900      [Hz]
PWM frequency: 3000      Measured frequency: 3000      [Hz]
Press any key to initiate a new conversion...

```

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.50 LPTMR Periodic Interrupt

Example application that shows the LPTMR's Timer feature

Application description

The purpose of this demo application is to show you how to use the LPTMR's Timer functionality from the S32K148 using the S32 SDK API.

- The LPTMR is configured to generate a periodic interrupt at 1 seconds which toggles a LED.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V
- 1 Dupont male to male cable
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
GPIO PIN (PTE23)	RGB_BLUE - wired on the board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **lptmr_periodic_interrupt_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**lptmr_periodic_interrupt_s32k148**). Select the "ConfigTools" menu then click on the desired configurator (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lptmr_periodic_interrupt_s32k148_debug_ram↔ jlink	Debug the RAM configuration using Segger Jlink debuggers
lptmr_periodic_interrupt_s32k148_debug_flash↔ _jlink	Debug the FLASH configuration using Segger Jlink debuggers
lptmr_periodic_interrupt_s32k148_debug_ram↔ pemicro	Debug the RAM configuration using PEMicro debuggers
lptmr_periodic_interrupt_s32k148_debug_flash↔ _pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.51 LPTMR Pulse Counter

Example application that shows the LPTMR's Pulse Counting feature

Application description

The purpose of this demo application is to show you how to use the Low Power Timer's Pulse Counter functionality from the S32K148 using the S32 SDK API.

- The example is configured to trigger an interrupt after three pulses, sourced from one of the board's buttons.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1(2) Dupont male to male cable
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
GPIO PIN (PTE23)	RGB_BLUE - wired on the board
BUTTON (PTC12)	SW3 - J6.5 connect to J2.23

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **lptmr_pulse_counter_↔s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**lptmr_pulse_counter_s32k148**). Select the "↔ConfigTools" menu then click on the desired configurator (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lptmr_pulse_counter_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
lptmr_pulse_counter_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
lptmr_pulse_counter_s32k148_debug_ram_↔pemicro	Debug the RAM configuration using PEMicro debuggers
lptmr_pulse_counter_s32k148_debug_flash_↔pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.52 PDB Periodic Interrupt

Driver example using PDB

Application description

The purpose of this demo application is to show you how to use the Programmable Delay Block from the S32K148 using the S32 SDK API.

The PDB is configured to generate a periodic interrupt which toggles a LED.

See also

`adc_hwtrigger_group`

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V
- 1 Personal Computer
- 1 PEmicro Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
GPIO Pin (PTD15)	RGB_RED - wired on the board	LED0 - J11.31 - J12.18

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **pdb_periodic_interrupt↔_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code". Wait for the code generation to be completed before continuing to the next step.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
pdb_periodic_interrupt_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
pdb_periodic_interrupt_s32k148_debug_flash_↔ jlink	Debug the FLASH configuration using Segger Jlink debuggers
pdb_periodic_interrupt_s32k148_debug_ram_↔ pemicro	Debug the RAM configuration using PEMicro debuggers
pdb_periodic_interrupt_s32k148_debug_flash_↔ pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.53 RTC Alarm

Example application showing basic use cases for the RTC module

Application description

The purpose of this demo application is to show you how to use the Real Time Clock module from the S32K148 MCU with the S32 SDK API.

The RTC is configured to generate an interrupt every 1 second toggling GREEN_LED. If the alarm button is pressed an alarm interrupt toggles the alarm RED_LED after 5 seconds.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V
- 2 Dupont female to female cable
- 1 Personal Computer
- 1 PEMicro
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
RED_LED (PTE21)	RGB_RED - wired on the board	J12.17 - J11.31
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J12.16 - J11.30
BUTTON (PTC13)	SW4 - wired on the board	SW7 - wired on the board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From** and select **rtc_alarm_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace. Wait for the S32 Configuration was initialized and ready.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
rtc_alarm_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
rtc_alarm_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
rtc_alarm_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
rtc_alarm_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Notes

If the example doesn't work, please Flash the Debug_FLASH configuration and enforce a power on reset of the board.

This is caused by the fact that the register which configures the RTC clock source can only be written once.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.54 TIMING PAL

Driver example using TIMING PAL

Application description

The purpose of this application is to show you how to use the TIMING PAL over LPIT, LPTMR and FTM timers on the S32K148 using the S32 SDK API.

The application uses one board instance of LPIT, LPTMR and FTM to periodically toggle 3 leds.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board can't be powered from the USB)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176
- S32K148-MB

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
BLUE_LED (PTE23)	RGB_BLUE - wired on the board	J13.10 - J11.31
RED_LED (PTE21)	RGB_RED - wired on the board	J13.12 - J11.32
GREEN_LED (PTE22)	RGB_GREEN - wired on the board	J13.9 - J11.29

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **timing_pal_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**timing_pal_s32k148**). Select the "ConfigTools" menu then click on the desired configurator (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
timing_pal_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
timing_pal_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
timing_pal_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
timing_pal_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.55 PWM PAL

Example application using the PWM PAL

Application description

The purpose of this demo application is to show you how to use the PWM PAL from the S32K148 CPU using the S32 SDK API. The example will dim the GREEN LED on EVB or ORANGE LED on Motherboard by varying the duty cycle of the PWM signal.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 PEmicro Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148-MB
- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176	S32K148-MB
FTM0 Channel 0 (PTE22)	RGB_GREEN - wired on the board	LED_ORANGE - Connected J13.9 to JP49.2

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **pwm_pal_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Right click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configuration (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
pwm_pal_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
pwm_pal_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers
pwm_pal_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
pwm_pal_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.56 OC PAL

Driver example using OC PAL

Application description

The purpose of this application is to show you how to use the OC PAL over FTM_OC on the S32K148 using the S32 SDK API.

This application will toggle green led with period 2 second.

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board can't be powered from the USB)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
FTM0 Channel 0 (PTE21)	RGB_RED - wired on the board

How to run**1. Importing the project into the workspace**

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **oc_pal_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. Left click on the current project, then click "Open S32 Configuration" (it has blue chip symbol on the top of the toolbar). In S32 Configuration menu, click on the desired configurator (Pins, Clock, Peripherals, etc.). Clicking on any one of those will generate all the components. Pay attention to any error and warning message. If any configured value is invalid, they will be shown for user. Make the desired changes (if any) then click "Update Code".

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
oc_pal_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
oc_pal_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
oc_pal_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEmicro debuggers
oc_pal_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEmicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

14.4.57 LPIT Periodic Interrupt

Driver example that will show the LPIT functionality

Application description

The purpose of this demo application is to show you how to use the Low Power Interrupt Timer from the S32K148 using the S32 SDK API.

- The example is configured to trigger an interrupt every second, which toggles a LED.

See also

For other LPIT usage scenario check: ADC_LOW_POWER_group

Prerequisites

To run the example you will need to have the following items:

- 1 S32K148 board
- 1 Power Adapter 12V (if the board cannot be powered from the USB port)
- 1 Personal Computer
- 1 Jlink Lite Debugger (optional, users can use Open SDA)

Boards supported

The following boards are supported by this application:

- S32K148EVB-Q176

Hardware Wiring

The following connections must be done to for this example application to work:

PIN FUNCTION	S32K148EVB-Q176
GPIO PIN (PTE23)	RGB_BLUE - wired on the board

How to run

1. Importing the project into the workspace

After opening S32 Design Studio, go to **File -> New S32DS Project From...** and select **lpit_periodic_interrupt_s32k148**. Then click on **Finish**.

The project should now be copied into you current workspace.

2. Generating the S32 configuration

The example will run without an active configuration, however if any changes are required, a configuration needs to be generated. The initial configuration will have the same settings as the default example settings. First go to **Project Explorer** View in S32 DS and select the current project(**lpit_periodic_interrupt_s32k148**). Select the "ConfigTools" menu then click on the desired configurator (Pins, Cocks, Peripherals etc...). Clicking on any one of those will generate all the components. Make the desired changes(if any) then click on the "ConfigTools->Update Code" button.

3. Building the project

Select the configuration to be built **FLASH** (Debug_FLASH) or **RAM** (Debug_RAM) by left clicking on the downward arrow corresponding to the **build** button(. Wait for the build action to be completed before continuing to the next step.

4. Running the project

Go to **Run** and select **Debug Configurations**. There will be four debug configurations for this project:

Configuration Name	Description
lpit_periodic_interrupt_s32k148_debug_ram_jlink	Debug the RAM configuration using Segger Jlink debuggers
lpit_periodic_interrupt_s32k148_debug_flash_jlink	Debug the FLASH configuration using Segger Jlink debuggers
lpit_periodic_interrupt_s32k148_debug_ram_pemicro	Debug the RAM configuration using PEMicro debuggers
lpit_periodic_interrupt_s32k148_debug_flash_pemicro	Debug the FLASH configuration using PEMicro debuggers

Select the desired debug configuration and click on **Launch**. Now the perspective will change to the **Debug Perspective**.

Use the controls to control the program flow.

Note

For more detailed information related to S32 Design Studio usage please consult the available documentation.

15 Module Index

15.1 Modules

Here is a list of all modules:

ADC Driver

Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL)	268
Automotive Math and Motor Control Library	281
Clock	315
Clock Manager	316
Clock Manager Driver	317
Comparator (CMP)	361
Comparator Driver	365
Controller Area Network - Peripheral Abstraction Layer (CAN PAL)	381
Controller Area Network with Flexible Data Rate (FlexCAN)	398
FlexCAN Driver	506
Cryptographic Services Engine (CSEc)	402
CSEc Driver	294
Cyclic Redundancy Check (CRC)	403
CRC Driver	289
Enhanced Direct Memory Access (eDMA)	473
EDMA Driver	410
Error Injection Module (EIM)	474
EIM Driver	435
Error Reporting Module (ERM)	476
ERM Driver	463
Ethernet MAC (ENET)	478
ENET Driver	440
Ethernet Transceiver (PHY)	481
PHY Framework	941
Generic PHY	662
TJA110x PHY	1136
External Watchdog Monitor (EWM)	482
EWM Driver	468
Flash Memory (Flash)	503
Flash Memory (Flash)	483
FlexTimer (FTM)	581
FlexTimer Input Capture Driver (FTM_IC)	619

FlexTimer Module Counter Driver (FTM_MC)	627
FlexTimer Output Compare Driver (FTM_OC)	631
FlexTimer Pulse Width Modulation Driver (FTM_PWM)	637
FlexTimer Quadrature Decoder Driver (FTM_QD)	654
Flexible I/O (FlexIO)	660
FlexIO Common Driver	528
FlexIO I2C Driver	531
FlexIO I2S Driver	540
FlexIO SPI Driver	558
FlexIO UART Driver	572
FreeRTOS	661
I2S - Peripheral Abstraction Layer (I2S PAL)	674
Input Capture - Peripheral Abstraction Layer (IC PAL)	683
Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL)	692
Interrupt Manager (Interrupt)	709
Local Interconnect Network (LIN)	816
LIN Driver	720
LIN Stack	739
Diagnostic services	405
Node configuration	900
Node identification	907
LIN Core API	719
Common Core API.	355
Driver and cluster management	409
Interface management	707
Notification	908
Schedule management	1079
Signal interaction	1113
User provided call-outs	1222
J2602 Specific API	715
LIN 2.1 Specific API	717
Low level API	824

Transport layer API	1167
Common Transport Layer API	357
Cooked API	400
Initialization	682
Raw API	1014
J2602 Transport Layer specific API	716
Node configuration	905
Low Power Inter-Integrated Circuit (LPI2C)	817
LPI2C Driver	742
Low Power Interrupt Timer (LPIT)	818
LPIT Driver	758
Low Power Serial Peripheral Interface (LPSPI)	819
LPSPI Driver	773
Low Power Timer (LPTMR)	822
LPTMR Driver	791
Low Power Universal Asynchronous Receiver-Transmitter (LPUART)	823
LPUART Driver	801
Memory Protection Unit (MPU)	893
MPU Driver	856
Memory Protection Unit Peripheral Abstraction Layer (MPU PAL)	895
MPU PAL	870
OS Interface (OSIF)	909
Output Compare - Peripheral Abstraction Layer (OC PAL)	918
Pins Driver (PINS)	964
PINS Driver	958
Power Manager	966
Power Manager Driver	976
Power_s32k1xx	978
Programmable Delay Block (PDB)	984
PDB Driver	929
Pulse-width modulation - Peripheral Abstraction Layer (PWM PAL)	985
Quad Serial Peripheral Interface (QuadSPI)	994

MX25L6433F Serial Flash Driver	881
QuadSPI Driver	995
Real Time Clock Driver (RTC)	1016
RTC Driver	999
Security Peripheral Abstraction Layer - SECURITY PAL	1098
Security PAL	1080
Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL)	1101
SoC Header file (SoC Header)	1114
S32K148 SoC Header file	1033
Backward Compatibility Symbols for S32K148	282
Interrupt vector numbers for S32K148	714
Peripheral access layer for S32K148	963
SoC Support	1115
S32K148 System Files	1034
Structural Core Self Test	1120
Synchronous Audio Interface (SAI)	1125
SAI Driver	1035
System Basis Chip Driver (SBC) - FS45xx Family	1126
SBC FS45 Driver	1048
System Basis Chip Driver (SBC) - UJA116xA Family	1129
UJA116xA SBC Driver	1168
System Basis Chip library (SBC) - UJA113x Family	1134
00. Library internals	178
Register address map	1020
01. Primary control	200
01. Mode handling	198
02. Watchdog	213
03. Fail-safe configuration	217
04. Lock control	232
02. Supply control	212
01. Regulator configuration	201
02. Battery monitor configuration	204

03. SMPS configuration	221
03. Transceiver control	224
01. CAN & CAN partial networking configuration	189
02. LIN configuration	208
04. HVIO bank 0 & 1 control	225
05. Timer control	235
06. Interrupts	239
Bank N fail interrupt enable configuration options (0x38/0x48)	283
Bank N wake-up interrupt enable configuration options (0x37/0x47)	286
Supply interrupt enable configuration options (0x1C)	1122
System interrupt enable configuration options (0x04)	1135
Transceiver interrupt enable configuration options (0x23)	1165
07. MTPNV and ID	243
HVIO high-side configuration options (0x71)	668
HVIO low-side configuration options (0x72)	671
SBC configuration control options (0x74)	1076
Start-up control configuration options (0x73)	1117
TRGMUX Driver	1147
Timing - Peripheral Abstraction Layer (TIMING PAL)	1154
Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL)	1209
Watchdog Peripheral Abstraction Layer (WDG PAL)	1239
WDG PAL	1223
Watchdog timer (WDOG)	1242
WDOG Driver	1230

16 Data Structure Index

16.1 Data Structures

Here are the data structures with brief descriptions:

__blake2b_param	1243
__blake2bp_state	1244
__blake2s_param	1244
__blake2sp_state	1246

adc_callback_info_t	
Defines a structure used to pass information to the ADC PAL callback	1246
adc_instance_t	
Structure storing PAL instance information	1247
Aes	1247
Arc4	1248
Arrays	1249
Base_entry	1250
Buffers	1251
bufferStatic	1253
BuildMsgArgs	1254
callback_functions	1255
can_instance_t	
Structure storing PAL instance information	1256
CertSignCtx	1256
Ciphers	1257
CipherSpecs	1258
ClientRow	1259
ClientSession	1260
CRL_Entry	1260
CRL_Monitor	1262
DckeArgs	1262
DcvArgs	1263
DecodedCert	1264
DecodedName	1269
DerBuffer	1272
Des	1272
Des3	1273
DhKey	1274
DhParams	1274
DNS_entry	1275
drv_config_t	1275
DsaKey	1276

DskeArgs	1277
DtIsFrag	1278
DtIsHandShakeHeader	1278
DtIsMsg	1279
DtIsRecordLayerHeader	1280
EncryptedInfo	1281
fp_int	1282
fs45_tx_data_t	
Structure representing transmit data frame	1282
func_args	1283
HandShakeHeader	1284
handShakeInfo_st	1284
Hash	1285
Hashes	1286
HC128	1286
Hmac	1287
HS_Hashes	1288
i2c_instance_t	
Structure storing PAL instance information	1289
i2s_instance_t	
Structure storing PAL instance information	1289
ic_instance_t	
Structure storing PAL instance information	1290
Keys	1290
lin_product_id_t	
Product id structure Implements : lin_product_id_t_Class	1292
Md4	1293
Md5	1293
mp_int	1294
mpu_instance_t	
Structure storing PAL instance information	1295
MsgsReceived	1296
oc_instance_t	
Structure storing PAL instance information	1297
oc_pal_state_t	
The internal context structure	1298

OcspEntry	1298
Options	1299
OS_Seed	1305
packetInfo_st	1305
phy_basicStatus_t	
Structure containing the basic status information	1306
ProcPeerCertArgs	1307
ProtocolVersion	1308
pwm_instance_t	
Structure storing PAL instance information	1309
qspi_ahb_config_t	
AHB configuration structure	1309
qspi_state_t	
Driver internal context structure	1310
qspi_user_config_t	
Driver configuration structure	1311
Rabbit	1313
RabbitCtx	1314
ReadDirCtx	1314
RecordLayerHeader	1315
RsaKey	1316
SckeArgs	1317
ScvArgs	1318
SessionRow	1319
Sha	1320
Sha256	1321
SignatureCtx	1322
Signer	1323
smtp_send_request	1324
spi_instance_t	
Structure storing PAL instance information	1325
SskeArgs	1326
Suites	1327
t_atcert	1328
tcp_ready	1329

timeoutInfo_st	1329
timer_chan_state_t	
Runtime state of the Timer channel	1330
timing_instance_t	
Structure storing PAL instance information	1330
uart_instance_t	
Structure storing PAL instance information	1331
WC_DerCertList	1332
wc_HashAlg	1332
WC_RNG	1333
wdg_instance_t	
Structure storing PAL instance information	1333
WOLF_EVENT	1334
WOLF_EVENT_QUEUE	1335
WOLFSSL	1336
WOLFSSL_ALERT	1340
WOLFSSL_ALERT_HISTORY	1340
WOLFSSL_ASN1_BIT_STRING	1341
WOLFSSL_ASN1_INTEGER	1341
WOLFSSL_ASN1_OBJECT	1342
WOLFSSL_ASN1_STRING	1342
WOLFSSL_ASN1_TIME	1343
WOLFSSL_BIGNUM	1343
WOLFSSL_BIO	1344
WOLFSSL_BIO_METHOD	1346
WOLFSSL_BUFFER_INFO	1346
WOLFSSL_CERT_MANAGER	1346
WOLFSSL_Cipher	1348
WOLFSSL_CIPHER	1349
WOLFSSL_COMP_METHOD	1349
WOLFSSL_CRL	1350
WOLFSSL_CTX	1351
WOLFSSL_DH	1355
WOLFSSL_DSA	1356

WOLFSSL_DTLS_CTX	1357
WOLFSSL_DTLS_PEERSEQ	1357
WOLFSSL_EC_GROUP	1358
WOLFSSL_EC_KEY	1359
WOLFSSL_EC_POINT	1360
WOLFSSL_ECDSA_SIG	1361
WOLFSSL_EVP_CIPHER_CTX	1361
WOLFSSL_EVP_MD_CTX	1362
WOLFSSL_EVP_PKEY	1363
WOLFSSL_Hasher	1363
WOLFSSL_HMAC_CTX	1364
WOLFSSL_MD4_CTX	1365
WOLFSSL_MD5_CTX	1365
WOLFSSL_METHOD	1365
WOLFSSL_OCSP	1366
WOLFSSL_RIPEMD_CTX	1367
WOLFSSL_RSA	1367
WOLFSSL_SESSION	1368
WOLFSSL_SHA256_CTX	1370
WOLFSSL_SHA_CTX	1370
WOLFSSL_SOCKADDR	1370
WOLFSSL_STACK	1371
wolfssl_TI_Hash	1372
WOLFSSL_X509	1373
WOLFSSL_X509_CHAIN	1375
WOLFSSL_X509_LOOKUP	1375
WOLFSSL_X509_LOOKUP_METHOD	1375
WOLFSSL_X509_NAME	1376
WOLFSSL_X509_OBJECT	1377
WOLFSSL_X509_REVOKED	1377
WOLFSSL_X509_STORE	1378
WOLFSSL_X509_STORE_CTX	1378

x509_buffer

1379

17 Module Documentation

17.1 00. Library internals

17.1.1 Detailed Description

17.1.2 Internals

This section describes the philosophy of the library, naming conventions and how to start using this library.

17.1.2.1 General description

The SBC incorporates several registers allowing the user to configure its behaviour. Following the SBCs SPI protocol, these registers can be read/written to get the status of the device or change the configuration. The `UJA113X_SbcTransfer()` function is the foundation of this library, which can be used to read/write from/into the SBC. Several functions are available to configure specific functionality of the SBC, however, these just wrap the `UJA113X_SbcTransfer()` function at the end. Advantage of these functions lies in just providing input parameters and the function takes care of the address, frame length etc.

As it makes no sense to provide different functions just to read a specific register, the `UJA113X_SbcTransfer()` function should be used in such a case.

Different SBC registers control specific functionality. The number of registers required to control each functionality differs, e.g. the SBC mode is controlled by a single register but to configure CAN, several registers need to be written. From this perspective dedicated functions are available to ease the configuration. Some of these functions configure only one register (e.g. `UJA113X_SetWatchdog()`, `UJA113X_SetMode()`) and thus bring only little advantage over `UJA113X_SbcTransfer()`, whereas others configure whole group (e.g. `UJA113X_SetCan()`). It's up to the user which form to use. See the [How to start](#) subsection for details.

Although the library supports connection of multiple UJA113x units to one MCU, the SDK doesn't allow to manipulate these from external user files. Thus the number of SBCs connected to the MCU is hardcoded to 2 in the source file.

Every SBC connected to the host MCU is represented by a structure (`uja113x_driver_t`) holding internal data by the library. An array of such structures is defined in the source code hidden from the user and is used throughout the library. Thus each SBC instance has to be registered to initialize the SBC internal data.

After an SBC has been registered, the user can configure each part of the SBC separately based on instance number and input arguments provided to the `UJA113X_SetXYZ` functions. Configuration of each functionality is described in separate sections.

In case there is no dedicated function for reading/writing a register, the `UJA113X_SbcTransfer()` function can be used.

17.1.2.2 Naming conventions

This section describes the naming conventions used in the library to ease the navigation in the source code. Although effort has been put to obey these rules, it's not always possible or easy to follow them.

Functions

A general naming scheme is used for functions:

`<sbx_family>_<action_name>(input_parameters)`

For functions configuring specific functionality, the action name always starts with a **Set** keyword as follows:

`<sbx_family>_Set<functionality>` (e.g. `UJA113X_SetCanPartNet()`)

Structures

A general naming scheme is used for configuration structure:

`<sbx_family>_<reg_fce_acronym>_cfg_t`

The functionality acronym is derived either from a register name or in case of multiple registers dedicated to one functionality by the functionality.

Examples:

`uja113x_fsc_cfg_t` -> Fail-Safe Control configuration structure

`uja113x_cpnc_cfg_t` -> CAN Partial Networking Control configuration structure

`uja113x_dm_cfg_t` -> Data Masks configuration structure

Enumerations

A general naming scheme is used for enumeration types:

`<sbx_family>_<reg_acronym>_<reg_bit>_t`

Examples:

`uja113x_canc_csc_t` - CAN Control register, bit CSC: CAN Shutdown Control

Naming scheme for enum members:

`<reg_bit>_<text>_<text>...`

Examples:

`CMC_TRANSCEIVER_OFF` - CAN Mode Control: Transceiver offline

`CSC_UNDERVOLTAGE` - CAN Shutdown Control: Shutdown transceiver during undervoltage

Defines

17.1.2.3 How to start

The first step before the SBC can be used is to configure the LPSPI peripheral, as the library relies on it. Afterwards the `UJA113X_RegisterDevice()` should be invoked for every SBC connected to the MCU. While registering a device, important information about the SBC is stored internally. Once a device has been registered, the rest of the functions can be invoked at will to configure the device, read status etc.

Step-by-step summary

- 1. Initialize the LPSPI peripheral
- 2. Declare and set the `uja113x_drv_cfg_t` structure for every SBC
- 3. Invoke the `UJA113X_RegisterDevice()` for every SBC
- 4. Configure SBC using the `UJA113X_SbcTransfer()` function or other library functions
- 5. Change mode to Normal by invoking the `UJA113X_SetMode()` to run the SBC
- 6. Implement your logic for error/interrupt/status handling

Example:

```
...
...
#define LPSPI_INSTANCE_0    0U    /* SPI instance */
#define LPSPI_TIMEOUT      100U  /* 100 ms timeout */
#define SBC0               0U    /* SBC instance */
...
...
...
void main (void)
{
    /* Init the MCU clock, system related stuff, peripherals etc */
    ...
}
```

```

/* 1. Initialize the LPSPI peripheral*/
...

/* 2. Declare and set the uja113x_drv_cfg_t structure for every SBC */
uja113x_drv_cfg_t sbcConfig =
{
    UJA1131HW5V0,
    LPSPI_INSTANCE_0,
    LPSPI_TIMEOUT
};

/* 3. Invoke the UJA113X_RegisterDevice() for every SBC */
UJA113X_RegisterDevice(SBC0, &sbcConfig); /* Mandatory */

/* 4. Configure SBC using the UJA113X_SbcTransfer() function of other library functions */
UJA113X_SetWatchdog(...); /* Optional/application specific */
UJA113X_SbcTransfer(...); /* read back the written register - Optional/application
specific */
UJA113X_SetCan(...); /* Optional/application specific */
...
...
UJA113X_SetMtpnv(...); /* Optional/application specific */
/* 5. Change mode to Normal by invoking the UJA113X_SetMode() to run the SBC */
UJA113X_SetMode(...);
}

```

Modules

- [Register address map](#)

Data Structures

- struct [uja113x_drv_cfg_t](#)
SBC driver configuration structure. [More...](#)
- struct [uja113x_hvio_bank_cfg_t](#)
HVIO bank configuration structure. [More...](#)
- struct [uja113x_init_cfg_t](#)
SBC global initialization structure. [More...](#)
- struct [uja113x_driver_t](#)
*Internal SBC driver structure
Implements : [uja113x_driver_t_Class](#). [More...](#)*

Enumerations

- enum [uja113x_chip_t](#) {
[UJA1131HW5V0](#) = 0x1100U, [UJA1131HW3V3](#) = 0x1000U, [UJA1132HW5V0](#) = 0x0100U, [UJA1132HW3V3](#) = 0x0000U,
[UJA1135HW5V0](#) = 0x1101U, [UJA1135HW3V3](#) = 0x1001U, [UJA1136HW5V0](#) = 0x0101U, [UJA1136HW3V3](#) = 0x0001U,
[UJA1131HWFD5V4](#) = 0x5100U, [UJA1131HWFD3V4](#) = 0x5000U, [UJA1131HWFD5V0](#) = 0x7100U, [UJA1131HWFD3V0](#) = 0x7000U,
[UJA1132HWFD5V4](#) = 0x4100U, [UJA1132HWFD3V4](#) = 0x4000U, [UJA1132HWFD5V0](#) = 0x6100U, [UJA1132HWFD3V0](#) = 0x6000U }
Driver types.

Functions

- status_t [UJA113X_SbcTransfer](#) (uint32_t instance, bool read, uint8_t *txData, uint8_t *rxData, uint8_t size)
Initiates a write/read operation to/from SBC.
- status_t [UJA113X_Init](#) (uint32_t instance, const [uja113x_init_cfg_t](#) *const deviceConfig, const [uja113x_drv_cfg_t](#) *drvConfig)

Initializes complete chip based on input parameters except MTPNV.

- status_t [UJA113X_RegisterDevice](#) (uint32_t instance, const [uja113x_drv_cfg_t](#) *drvConfig)

Registers SBC internal parameters.

Variables

- static [uja113x_driver_t g_drivers](#) [DRIVER_COUNT__]

Internal array of SBC units connected to MCU.

17.1.3 Data Structure Documentation

17.1.3.1 struct [uja113x_drv_cfg_t](#)

SBC driver configuration structure.

Every SBC is represented by an internal driver structure, which needs to be initialized first. This is achieved by defining Based on this structure an UJA113X SBC has to be registered.

See also

[UJA113X_RegisterDevice\(\)](#)

Implements : [uja113x_drv_cfg_t_Class](#)

Definition at line 1782 of file [sbc_uja113x.h](#).

Data Fields

- [uja113x_chip_t chipType](#)
Defines the SBC type used by this instance.
- uint32_t [lpspiInstance](#)
Defines which LPSPi is used to communicate with this device.
- uint32_t [timeout](#)
Defines the SPI timeout for a single transaction.

Field Documentation

17.1.3.1.1 [uja113x_chip_t chipType](#)

Defines the SBC type used by this instance.

Definition at line 1787 of file [sbc_uja113x.h](#).

17.1.3.1.2 uint32_t [lpspiInstance](#)

Defines which LPSPi is used to communicate with this device.

Definition at line 1791 of file [sbc_uja113x.h](#).

17.1.3.1.3 uint32_t [timeout](#)

Defines the SPI timeout for a single transaction.

Definition at line 1795 of file [sbc_uja113x.h](#).

17.1.3.2 struct [uja113x_hvio_bank_cfg_t](#)

HVIO bank configuration structure.

Implements : [uja113x_hvio_bank_cfg_t_Class](#)

Definition at line 1805 of file [sbc_uja113x.h](#).

Data Fields

- [uja113x_hvio_cfg_t hvioConfig](#) [BANK_HVIO_CNT]
Array of HVIO control register configuration structures (0x30 - 0x33; 0x40 - 0x44)
- [uja113x_bwtc_bnwtc_t bankWupThr](#)
Bank N wake-up threshold configuration options (0x34 / 0x44)
- [uint8_t bankWupIntMask](#)
Bank N wake-up interrupt masks (0x37 / 0x47)
- [uint8_t bankFailIntMask](#)
Bank N failure interrupt masks (0x38 / 0x48)
- [uja113x_bscdt_cfg_t bscdtBankShortCirc](#)
Bank N short-circuit detection threshold configuration structure (0x39 / 0x49)
- [uja113x_boldt_cfg_t boldtBankOpenLoad](#)
Bank N open-load detection threshold configuration structure (0x3A / 0x4A)

Field Documentation

17.1.3.2.1 [uint8_t bankFailIntMask](#)

Bank N failure interrupt masks (0x38 / 0x48)

Definition at line 1822 of file `sbc_uja113x.h`.

17.1.3.2.2 [uint8_t bankWupIntMask](#)

Bank N wake-up interrupt masks (0x37 / 0x47)

Definition at line 1818 of file `sbc_uja113x.h`.

17.1.3.2.3 [uja113x_bwtc_bnwtc_t bankWupThr](#)

Bank N wake-up threshold configuration options (0x34 / 0x44)

Definition at line 1814 of file `sbc_uja113x.h`.

17.1.3.2.4 [uja113x_boldt_cfg_t boldtBankOpenLoad](#)

Bank N open-load detection threshold configuration structure (0x3A / 0x4A)

Definition at line 1830 of file `sbc_uja113x.h`.

17.1.3.2.5 [uja113x_bscdt_cfg_t bscdtBankShortCirc](#)

Bank N short-circuit detection threshold configuration structure (0x39 / 0x49)

Definition at line 1826 of file `sbc_uja113x.h`.

17.1.3.2.6 [uja113x_hvio_cfg_t hvioConfig](#)[BANK_HVIO_CNT]

Array of HVIO control register configuration structures (0x30 - 0x33; 0x40 - 0x44)

Definition at line 1810 of file `sbc_uja113x.h`.

17.1.3.3 [struct uja113x_init_cfg_t](#)

SBC global initialization structure.

See also

[UJA113X_Init\(\)](#)

Implements : `uja113x_init_cfg_t_Class`

Definition at line 1841 of file `sbc_uja113x.h`.

Data Fields

- [uja113x_wtdc_cfg_t wdcWatchdogCfg](#)
Watchdog configuration.
- [uja113x_mc_mc_t mcSbcMode](#)
Desired mode after initialization.
- [uja113x_fsc_cfg_t fscCfg](#)
Fail-safe configuration.
- [uint8_t sysieMask](#)
Defines which system interrupts to enable.
- [uja113x_rc_cfg_t rcRegulatorCfg](#)
Regulator control configuration parameters (0x10)
- [uja113x_bmc_cfg_t bmcBatMonitorCfg](#)
Battery monitor configuration.
- [uja113x_smpsc_cfg_t smpscSmpsCfg](#)
SMPS output voltage control configuration parameter (0x1A)
- [uint8_t supieMask](#)
Supply interrupt enable configuration parameters (0x1C)
- [uja113x_canc_cfg_t canCanCfg](#)
CAN configuration.
- [uja113x_linc_cfg_t linxLinCtrl](#)
LIN 1 and 2 configuration.
- [uja113x_cpnc_cfg_t cpncCanPartNetCfg](#)
CAN partial networking configuration.
- [uja113x_dm_cfg_t dmCanDataMaskCfg](#)
Data mask configuration.
- [uint8_t tieMask](#)
Transceiver interrupt enable register configuration parameters (0x23)
- [const uja113x_hvio_bank_cfg_t * hvioBank0Cfg](#)
Configuration of HVIO bank 0 (HVIO 1 - 4)
- [const uja113x_hvio_bank_cfg_t * hvioBank1Cfg](#)
Configuration of HVIO bank 1 (HVIO 5 - 8)
- [const uja113x_timsc_cfg_t * timscTimer1Cfg](#)
Configuration of timer 1.
- [const uja113x_timsc_cfg_t * timscTimer2Cfg](#)
Configuration of timer 2.
- [const uja113x_timsc_cfg_t * timscTimer3Cfg](#)
Configuration of timer 3.
- [const uja113x_timsc_cfg_t * timscTimer4Cfg](#)
Configuration of timer 4.
- [const uja113x_lckc_cfg_t * lckcLockRegCfg](#)
Configuration of register lock.

General purpose memory settings (0x06 - 0x09)

- [uint8_t memory0](#)
- [uint8_t memory1](#)
- [uint8_t memory2](#)
- [uint8_t memory3](#)

Field Documentation

17.1.3.3.1 `uja113x_bmc_cfg_t` `bmcBatMonitorCfg`

Battery monitor configuration.

Definition at line 1874 of file `sbc_uja113x.h`.

17.1.3.3.2 `uja113x_canc_cfg_t` `cancCanCfg`

CAN configuration.

Definition at line 1886 of file `sbc_uja113x.h`.

17.1.3.3.3 `uja113x_cpnc_cfg_t` `cpncCanPartNetCfg`

CAN partial networking configuration.

Definition at line 1894 of file `sbc_uja113x.h`.

17.1.3.3.4 `uja113x_dm_cfg_t` `dmCanDataMaskCfg`

Data mask configuration.

Definition at line 1898 of file `sbc_uja113x.h`.

17.1.3.3.5 `uja113x_fsc_cfg_t` `fscCfg`

Fail-safe configuration.

Definition at line 1854 of file `sbc_uja113x.h`.

17.1.3.3.6 `const uja113x_hvio_bank_cfg_t*` `hvioBank0Cfg`

Configuration of HVIO bank 0 (HVIO 1 - 4)

Definition at line 1906 of file `sbc_uja113x.h`.

17.1.3.3.7 `const uja113x_hvio_bank_cfg_t*` `hvioBank1Cfg`

Configuration of HVIO bank 1 (HVIO 5 - 8)

Definition at line 1910 of file `sbc_uja113x.h`.

17.1.3.3.8 `const uja113x_lckc_cfg_t*` `lckcLockRegCfg`

Configuration of register lock.

Definition at line 1930 of file `sbc_uja113x.h`.

17.1.3.3.9 `uja113x_linc_cfg_t` `linxLinCtrl`

LIN 1 and 2 configuration.

Definition at line 1890 of file `sbc_uja113x.h`.

17.1.3.3.10 `uja113x_mc_mc_t` `mcSbcMode`

Desired mode after initialization.

Definition at line 1850 of file `sbc_uja113x.h`.

17.1.3.3.11 `uint8_t` `memory0`

Definition at line 1862 of file `sbc_uja113x.h`.

17.1.3.3.12 uint8_t memory1

Definition at line 1863 of file sbc_uja113x.h.

17.1.3.3.13 uint8_t memory2

Definition at line 1864 of file sbc_uja113x.h.

17.1.3.3.14 uint8_t memory3

Definition at line 1865 of file sbc_uja113x.h.

17.1.3.3.15 uja113x_rc_cfg_t rcRegulatorCfg

Regulator control configuration parameters (0x10)

Definition at line 1870 of file sbc_uja113x.h.

17.1.3.3.16 uja113x_smpsc_cfg_t smpscSmpsCfg

SMPS output voltage control configuration parameter (0x1A)

Definition at line 1878 of file sbc_uja113x.h.

17.1.3.3.17 uint8_t supieMask

Supply interrupt enable configuration parameters (0x1C)

Definition at line 1882 of file sbc_uja113x.h.

17.1.3.3.18 uint8_t sysieMask

Defines which system interrupts to enable.

Definition at line 1858 of file sbc_uja113x.h.

17.1.3.3.19 uint8_t tieMask

Transceiver interrupt enable register configuration parameters (0x23)

Definition at line 1902 of file sbc_uja113x.h.

17.1.3.3.20 const uja113x_timsc_cfg_t* timscTimer1Cfg

Configuration of timer 1.

Definition at line 1914 of file sbc_uja113x.h.

17.1.3.3.21 const uja113x_timsc_cfg_t* timscTimer2Cfg

Configuration of timer 2.

Definition at line 1918 of file sbc_uja113x.h.

17.1.3.3.22 const uja113x_timsc_cfg_t* timscTimer3Cfg

Configuration of timer 3.

Definition at line 1922 of file sbc_uja113x.h.

17.1.3.3.23 const uja113x_timsc_cfg_t* timscTimer4Cfg

Configuration of timer 4.

Definition at line 1926 of file sbc_uja113x.h.

17.1.3.3.24 `uja113x_wtdc_cfg_t` `wdcWatchdogCfg`

Watchdog configuration.

Definition at line 1846 of file `sbc_uja113x.h`.

17.1.3.4 `struct uja113x_driver_t`

Internal SBC driver structure

Implements : `uja113x_driver_t_Class`.

Definition at line 64 of file `sbc_uja113x.c`.

Data Fields

- [`uja113x_chip_t` `chipType`](#)
Chip ID.
- `uint32_t` [`lpspiInstance`](#)
LPSPi used to communicate with SBC.
- `uint32_t` [`timeout`](#)
SPI timeout.

Field Documentation

17.1.3.4.1 `uja113x_chip_t` `chipType`

Chip ID.

Definition at line 69 of file `sbc_uja113x.c`.

17.1.3.4.2 `uint32_t` `lpspiInstance`

LPSPi used to communicate with SBC.

Definition at line 73 of file `sbc_uja113x.c`.

17.1.3.4.3 `uint32_t` `timeout`

SPI timeout.

Definition at line 77 of file `sbc_uja113x.c`.

17.1.4 Enumeration Type Documentation

17.1.4.1 `enum uja113x_chip_t`

Driver types.

Implements : `uja113x_chip_t_Class`

Enumerator

`UJA1131HW5V0`
`UJA1131HW3V3`
`UJA1132HW5V0`
`UJA1132HW3V3`
`UJA1135HW5V0`
`UJA1135HW3V3`
`UJA1136HW5V0`

UJA1136HW3V3
UJA1131HWFD5V4
UJA1131HWFD3V4
UJA1131HWFD5V0
UJA1131HWFD3V0
UJA1132HWFD5V4
UJA1132HWFD3V4
UJA1132HWFD5V0
UJA1132HWFD3V0

Definition at line 43 of file sbc_uja113x.h.

17.1.5 Function Documentation

17.1.5.1 **status_t** UJA113X_Init (**uint32_t** *instance*, **const** **uja113x_init_cfg_t** ***const** *deviceConfig*, **const** **uja113x_drv_cfg_t** * *drvConfig*)

Initializes complete chip based on input parameters except MTPNV.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>deviceConfig</i>	SBC configuration structure
in	<i>drvConfig</i>	Driver internal data

Returns

Error or success status returned by API

Definition at line 148 of file sbc_uja113x.c.

17.1.5.2 **status_t** UJA113X_RegisterDevice (**uint32_t** *instance*, **const** **uja113x_drv_cfg_t** * *drvConfig*)

Registers SBC internal parameters.

The library allows use of multiple UJA113X SBCs to be connected to an MCU. From this perspective every SBC has a set of internal data necessary for proper functionality. This function should be used to set these parameters for a single SBC based on input parameters.

Parameters

in	<i>instance</i>	SBC index (must be lower than UJA113X_DRIVER_COUNT)
in	<i>drvConfig</i>	SBC configuration structure

Returns

SBC_SUCCESS Configuration successful SBC_ERR_NA SBC instance out of range

Definition at line 366 of file sbc_uja113x.c.

17.1.5.3 **status_t** UJA113X_SbcTransfer (**uint32_t** *instance*, **bool** *read*, **uint8_t** * *txData*, **uint8_t** * *rxData*, **uint8_t** *size*)

Initiates a write/read operation to/from SBC.

Based on input arguments the function initiates a data transfer with SBC. Although the function allows to transfer any amount of data, the minimum number of bytes to transfer is 2 (address + 1 byte), maximum is 4 (address + 3 bytes) as defined by the SBCs SPI protocol. Otherwise the frame is considered as invalid and an SPI failure is raised by the SBC. The read parameter defines, whether a read or write from/to SBC is requested.

The first byte of *txData* must contain the address to read/write from/to.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>read</i>	Read operation is carried out on true, write otherwise
in	<i>txData</i>	Buffer to write into SBC
out	<i>rxData</i>	Buffer for received data
in	<i>size</i>	Number of bytes to write/read

Returns

STATUS_SUCCESS Write/read successful STATUS_BUSY SPI peripheral busy STATUS_TIMEOUT SP↔
I communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the
repeated address, configuration failed.

Warning

The first byte of txData must contain the register address to read/write from/to!
The function doesn't check the size of data. Make sure you write 2 - 4 bytes!

Note

The LSB bit of the address in first byte is not taken into account. The read parameter determines, whether a
read/write will be performed.

See also

[Register address map](#)

Definition at line 106 of file sbc_uja113x.c.

17.1.6 Variable Documentation**17.1.6.1 uja113x_driver_t g_drivers[DRIVER_COUNT_] [static]**

Internal array of SBC units connected to MCU.

The count of SBC units can be influenced by UJA113X_DRIVER_COUNT which can be defined by the user in
sbc_uja113x_usr.h file. If not defined, the default value is 1!

Implements : multiple_sbc_support_Class

Definition at line 101 of file sbc_uja113x.c.

17.2 01. CAN & CAN partial networking configuration

17.2.1 Detailed Description

17.2.2 Introduction

Except configuring mode and shutdown control during over-/undervoltages, the transceiver also supports CAN partial networking (CAN PN) (only devices with CAN partial networking feature). The PN feature allows to wake-up only a single node connected to a bus. From this perspective, several parameters (ID, ID mask, data, data masks etc.) need to be configured to be able to wake up on a dedicated CAN wake-up frame.

17.2.2.1 CAN Partial networking

To enable the CAN PN functionality and confirm its configuration, the CPNC & PNCOK bit in 0x20 register has to be written. The write of PNCOK bit should be done after the CAN PN registers were written, otherwise the PNCOK gets cleared on any write access into registers related to the CAN PN. Thus it's advised to write the CAN PN registers first ([UJA113X_SetCanPartNet\(\)](#) & [UJA113X_SetDataMasks\(\)](#)). The 0x20 register should be configured afterwards ([UJA113X_SetCan\(\)](#)).

In case the CAN PN wake-up frame should not rely on data, the CAN data masks configuration can be skipped. Thus the CAN PN configuration is split in two parts.

Data Structures

- struct [uja113x_canc_cfg_t](#)
CAN control register configuration structure (0x20) [More...](#)
- struct [uja113x_cpnc_cfg_t](#)
CAN partial networking configuration structure (0x26 - 0x2F) [More...](#)
- struct [uja113x_dm_cfg_t](#)
CAN partial networking data mask registers configuration structure (0x68 - 0x6F) [More...](#)

Typedefs

- typedef bool [uja113x_canc_cfdc_t](#)
CAN FD control (0x20:CFDC[6])
- typedef bool [uja113x_canc_cpnc_t](#)
CAN partial networking control parameter (0x20:CPNC[4])
- typedef uint32_t [uja113x_id_id_t](#)
CAN partial networking ID (0x27 - 0x2A)
- typedef uint32_t [uja113x_idm_idm_t](#)
CAN partial networking ID mask (0x2B - 0x2E)
- typedef bool [uja113x_fc_ide_t](#)
CAN partial networking ID format options (0x2F:IDE[7])
- typedef bool [uja113x_fc_pndm_t](#)
CAN partial networking data mask options (0x2F:PNDM[6])

Enumerations

- enum [uja113x_canc_csc_t](#) { [CSC_NONE](#) = 0x00U, [CSC_UNDRVOLTAGE](#) = 0x04U, [CSC_OVERVOLTAGE](#) = 0x08U, [CSC_UNDRV_OVERV](#) = 0x0CU }
CAN shut-down control configuration options (0x20:CSC[3:2])
- enum [uja113x_canc_cmc_t](#) { [CMC_TRANSCEIVER_OFF](#) = 0x00U, [CMC_TRANSCEIVER_ACTIVE](#) = 0x01U, [CMC_TRANSCEIVER_ACTIVE2](#) = 0x02U, [CMC_TRANSCEIVER_LISTEN](#) = 0x03U }
CAN transceiver operating mode configuration options (0x20:CMC[1:0])

- enum [uja113x_dr_cdr_t](#) {
[CDR_DATA_RATE_50](#) = 0x00U, [CDR_DATA_RATE_100](#) = 0x01U, [CDR_DATA_RATE_125](#) = 0x02U, [CDR_DATA_RATE_250](#) = 0x03U,
[CDR_DATA_RATE_500a](#) = 0x04U, [CDR_DATA_RATE_500b](#) = 0x05U, [CDR_DATA_RATE_500c](#) = 0x06U,
[CDR_DATA_RATE_1000](#) = 0x07U }

CAN data rate configuration options (0x26:CDR[2:0])

- enum [uja113x_fc_dlc_t](#) {
[DLC_0](#) = 0x00U, [DLC_1](#) = 0x01U, [DLC_2](#) = 0x02U, [DLC_3](#) = 0x03U,
[DLC_4](#) = 0x04U, [DLC_5](#) = 0x05U, [DLC_6](#) = 0x06U, [DLC_7](#) = 0x07U,
[DLC_8](#) = 0x08U }

Number of data bytes in a CAN wake-up frame options (0x2F:DLC[3:0])

Functions

- status_t [UJA113X_SetCan](#) (uint32_t instance, const [uja113x_canc_cfg_t](#) *cancConfig)
Sets the CAN control register (0x20) based on input configuration object.
- status_t [UJA113X_SetCanPartNet](#) (uint32_t instance, const [uja113x_cpnc_cfg_t](#) *cpncConfig)
Sets the CAN partial networking control register (0x26 - 0x2F) based on input configuration object.
- status_t [UJA113X_SetDataMasks](#) (uint32_t instance, const [uja113x_dm_cfg_t](#) *dmConfig)
Sets the CAN partial networking data mask registers (0x68 - 0x6F) based on input configuration object.

17.2.3 Data Structure Documentation

17.2.3.1 struct [uja113x_canc_cfg_t](#)

CAN control register configuration structure (0x20)

Implements : [uja113x_canc_cfg_t_Class](#)

Definition at line 1538 of file [sbc_uja113x.h](#).

Data Fields

- [uja113x_canc_cfdc_t](#) [canFDCtrl](#)
Configures whether CAN FD frames are tolerated or not (0x20:CFDC[6])
- [uja113x_canc_cpnc_t](#) [canPartNetCtrl](#)
Disables/enables CAN selective wake-up (0x20:CPNC[4])
- [uja113x_canc_csc_t](#) [canShutdownCtrl](#)
Configures CAN shut-down behaviour during battery over- or undervoltage (0x20:CSC[3:2])
- [uja113x_canc_cmc_t](#) [canModeCtrl](#)
Selects the CAN transceiver operating mode (0x20:CMC[1:0])

Field Documentation

17.2.3.1.1 [uja113x_canc_cfdc_t](#) [canFDCtrl](#)

Configures whether CAN FD frames are tolerated or not (0x20:CFDC[6])

Definition at line 1543 of file [sbc_uja113x.h](#).

17.2.3.1.2 [uja113x_canc_cmc_t](#) [canModeCtrl](#)

Selects the CAN transceiver operating mode (0x20:CMC[1:0])

Definition at line 1555 of file [sbc_uja113x.h](#).

17.2.3.1.3 uja113x_canc_cpnc_t canPartNetCtrl

Disables/enables CAN selective wake-up (0x20:CPNC[4])

Definition at line 1547 of file sbc_uja113x.h.

17.2.3.1.4 uja113x_canc_csc_t canShutdownCtrl

Configures CAN shut-down behaviour during battery over- or undervoltage (0x20:CSC[3:2])

Definition at line 1551 of file sbc_uja113x.h.

17.2.3.2 struct uja113x_cpnc_cfg_t

CAN partial networking configuration structure (0x26 - 0x2F)

Implements : uja113x_cpnc_cfg_t_Class

Definition at line 1592 of file sbc_uja113x.h.

Data Fields

- [uja113x_dr_cdr_t canDataRate](#)
Configures CAN data rate (0x26:CDR[2:0])
- [uja113x_id_id_t id](#)
Configures CAN wake-up ID (0x27 - 0x2A)
- [uja113x_idm_idm_t idMask](#)
Configures CAN wake-up ID mask (0x2B - 0x2E)
- [uja113x_fc_ide_t ide](#)
Configures whether standard/extended ID is used for wake-up (0x2F:IDE[7])
- [uja113x_fc_pndm_t partNetDataMask](#)
Configures whether DLC and data are checked during wake-up (0x2F:PNDM[6])
- [uja113x_fc_dlc_t dataLenCode](#)
Configures the number of expected bytes during wake-up (0x2F:DLC[3:0])

Field Documentation**17.2.3.2.1 uja113x_dr_cdr_t canDataRate**

Configures CAN data rate (0x26:CDR[2:0])

Definition at line 1597 of file sbc_uja113x.h.

17.2.3.2.2 uja113x_fc_dlc_t dataLenCode

Configures the number of expected bytes during wake-up (0x2F:DLC[3:0])

Definition at line 1617 of file sbc_uja113x.h.

17.2.3.2.3 uja113x_id_id_t id

Configures CAN wake-up ID (0x27 - 0x2A)

Definition at line 1601 of file sbc_uja113x.h.

17.2.3.2.4 uja113x_fc_ide_t ide

Configures whether standard/extended ID is used for wake-up (0x2F:IDE[7])

Definition at line 1609 of file sbc_uja113x.h.

17.2.3.2.5 `uja113x_idm_idm_t idMask`

Configures CAN wake-up ID mask (0x2B - 0x2E)

Definition at line 1605 of file `sbc_uja113x.h`.

17.2.3.2.6 `uja113x_fc_pndm_t partNetDataMask`

Configures whether DLC and data are checked during wake-up (0x2F:PNDM[6])

Definition at line 1613 of file `sbc_uja113x.h`.

17.2.3.3 `struct uja113x_dm_cfg_t`

CAN partial networking data mask registers configuration structure (0x68 - 0x6F)

Implements : `uja113x_dm_cfg_t_Class`

Definition at line 1627 of file `sbc_uja113x.h`.

Data Fields

- `uint8_t dm0`
Data mask 0 configuration (0x68:DM0[7:0])
- `uint8_t dm1`
Data mask 1 configuration (0x69:DM1[7:0])
- `uint8_t dm2`
Data mask 2 configuration (0x6A:DM2[7:0])
- `uint8_t dm3`
Data mask 3 configuration (0x6B:DM3[7:0])
- `uint8_t dm4`
Data mask 4 configuration (0x6C:DM4[7:0])
- `uint8_t dm5`
Data mask 5 configuration (0x6D:DM5[7:0])
- `uint8_t dm6`
Data mask 6 configuration (0x6E:DM6[7:0])
- `uint8_t dm7`
Data mask 7 configuration (0x6F:DM7[7:0])

Field Documentation

17.2.3.3.1 `uint8_t dm0`

Data mask 0 configuration (0x68:DM0[7:0])

Definition at line 1629 of file `sbc_uja113x.h`.

17.2.3.3.2 `uint8_t dm1`

Data mask 1 configuration (0x69:DM1[7:0])

Definition at line 1630 of file `sbc_uja113x.h`.

17.2.3.3.3 `uint8_t dm2`

Data mask 2 configuration (0x6A:DM2[7:0])

Definition at line 1631 of file `sbc_uja113x.h`.

17.2.3.3.4 uint8_t dm3

Data mask 3 configuration (0x6B:DM3[7:0])

Definition at line 1632 of file sbc_uja113x.h.

17.2.3.3.5 uint8_t dm4

Data mask 4 configuration (0x6C:DM4[7:0])

Definition at line 1633 of file sbc_uja113x.h.

17.2.3.3.6 uint8_t dm5

Data mask 5 configuration (0x6D:DM5[7:0])

Definition at line 1634 of file sbc_uja113x.h.

17.2.3.3.7 uint8_t dm6

Data mask 6 configuration (0x6E:DM6[7:0])

Definition at line 1635 of file sbc_uja113x.h.

17.2.3.3.8 uint8_t dm7

Data mask 7 configuration (0x6F:DM7[7:0])

Definition at line 1636 of file sbc_uja113x.h.

17.2.4 Typedef Documentation

17.2.4.1 typedef bool uja113x_canc_cfdc_t

CAN FD control (0x20:CFDC[6])

false - CAN FD tolerance disabled, the CAN FD frames are detected as erroneous while in sleep with partial networking enabled

true - CAN FD tolerance enabled, the can FD frames are ignored while in sleep with partial networking enabled

Implements : uja113x_canc_cfdc_t_Class

Definition at line 586 of file sbc_uja113x.h.

17.2.4.2 typedef bool uja113x_canc_cpnc_t

CAN partial networking control parameter (0x20:CPNC[4])

false - Disable CAN selective wake-up

true - Enable CAN selective wake-up

Implements : uja113x_canc_cpnc_t_Class

Definition at line 597 of file sbc_uja113x.h.

17.2.4.3 typedef bool uja113x_fc_ide_t

CAN partial networking ID format options (0x2F:IDE[7])

false - standard frame format (11-bit)

true - extended frame format (11-bit)

Implements : uja113x_fc_ide_t_Class

Definition at line 799 of file sbc_uja113x.h.

17.2.4.4 `typedef bool uja113x_fc_pndm_t`

CAN partial networking data mask options (0x2F:PNDM[6])

false - data length code and data field are ignored for wake-up

true - data length code and data field are evaluated at wake-up

Implements : `uja113x_fc_pndm_t_Class`

Definition at line 810 of file `sbc_uja113x.h`.

17.2.4.5 `typedef uint32_t uja113x_id_id_t`

CAN partial networking ID (0x27 - 0x2A)

Implements : `uja113x_id_id_t_Class`

Definition at line 779 of file `sbc_uja113x.h`.

17.2.4.6 `typedef uint32_t uja113x_idm_idm_t`

CAN partial networking ID mask (0x2B - 0x2E)

Implements : `uja113x_idm_idm_t_Class`

Definition at line 788 of file `sbc_uja113x.h`.

17.2.5 Enumeration Type Documentation

17.2.5.1 `enum uja113x_canc_cmc_t`

CAN transceiver operating mode configuration options (0x20:CMC[1:0])

Implements : `uja113x_canc_cmc_t_Class`

Enumerator

`CMC_TRANSCEIVER_OFF` Offline/Offline bias mode.

`CMC_TRANSCEIVER_ACTIVE` Active mode (when the SBC is in normal mode).

`CMC_TRANSCEIVER_ACTIVE2` Active mode (when the SBC is in normal mode); VCAN undervoltage disabled.

`CMC_TRANSCEIVER_LISTEN` Listen-only mode.

Definition at line 628 of file `sbc_uja113x.h`.

17.2.5.2 `enum uja113x_canc_csc_t`

CAN shut-down control configuration options (0x20:CSC[3:2])

Implements : `uja113x_canc_csc_t_Class`

Enumerator

`CSC_NONE` CAN transceiver is not shut down when a battery monitor under- or overvoltage interrupt is generated.

`CSC_UNDRVOLTAGE` CAN transceiver shuts down in response to a battery monitor undervoltage (BMUI) interrupt (SBC in normal mode).

`CSC_OVERVOLTAGE` CAN transceiver shuts down in response to a battery monitor overvoltage (BMOI) interrupt (SBC in normal mode).

`CSC_UNDRV_OVERV` CAN transceiver shuts down in response to BMUI or BMOI interrupt (SBC in normal mode).

Definition at line 606 of file `sbc_uja113x.h`.

17.2.5.3 enum uja113x_dr_cdr_t

CAN data rate configuration options (0x26:CDR[2:0])

Implements : uja113x_dr_cdr_t_Class

Enumerator

CDR_DATA_RATE_50 50 kbit/s
CDR_DATA_RATE_100 100 kbit/s
CDR_DATA_RATE_125 125 kbit/s
CDR_DATA_RATE_250 250 kbit/s
CDR_DATA_RATE_500a reserved (intended for future use; currently selects 500 kbit/s)
CDR_DATA_RATE_500b 500 kbit/s
CDR_DATA_RATE_500c reserved (intended for future use; currently selects 500 kbit/s)
CDR_DATA_RATE_1000 1000 kbit/s

Definition at line 758 of file sbc_uja113x.h.

17.2.5.4 enum uja113x_fc_dlc_t

Number of data bytes in a CAN wake-up frame options (0x2F:DLC[3:0])

Implements : uja113x_fc_dlc_t_Class

Enumerator

DLC_0 0 bytes expected
DLC_1 1 bytes expected
DLC_2 2 bytes expected
DLC_3 3 bytes expected
DLC_4 4 bytes expected
DLC_5 5 bytes expected
DLC_6 6 bytes expected
DLC_7 7 bytes expected
DLC_8 8 bytes expected

Definition at line 819 of file sbc_uja113x.h.

17.2.6 Function Documentation

17.2.6.1 status_t UJA113X_SetCan (uint32_t instance, const uja113x_canc_cfg_t * canConfig)

Sets the CAN control register (0x20) based on input configuration object.

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the CAN control register has not been written properly and the process has to be repeated.

This function configures the PNCOK bit based on CPNC bit. In case the CAN Partial Networking is enabled (CPNC is set), this function automatically sets the PNCOK bit as well.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>cancConfig</i>	CAN control configuration object

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Note

Part of the CAN control configuration is also the PNCOK setting. This bit confirms that CAN partial networking configuration is valid, however, it is cleared after a write access to any of the CAN partial networking configuration registers (0x26 - 0x2F, 0x68 - 0x6F).

To use the CAN partial networking but avoid unnecessary writes into the SBC the CAN partial networking configuration prior to [UJA113X_SetCan\(\)](#) call is recommended. Afterwards, this function can be called with CPNC set which automatically sets the PNCOK.

Warning

The PNCOK bit is cleared after a write access to any of the CAN partial networking configuration registers (0x26 - 0x2F, 0x68 - 0x6F)

See also

[UJA113X_SetCanPartNet\(\)](#) [UJA113X_SetDataMasks\(\)](#)

Definition at line 641 of file sbc_uja113x.c.

17.2.6.2 `status_t UJA113X_SetCanPartNet (uint32_t instance, const uja113x_cpnc_cfg_t * cpncConfig)`

Sets the CAN partial networking control register (0x26 - 0x2F) based on input configuration object.

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the CAN partial networking control registers have not been written properly and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>cpncConfig</i>	CAN partial networking configuration object

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Note

It's possible to wake up on ID reception only and not evaluate the DLC & data content. From this perspective it would make no sense to configure data masks. Thus the data masks have to be configured with a separate function.

As the SPI protocol allows only 16/24/32 bit writes, four subsequent SPI transfers are carried out!

See also

[UJA113X_SetDataMasks\(\)](#)

Definition at line 746 of file sbc_uja113x.c.

17.2.6.3 status_t UJA113X_SetDataMasks (uint32_t instance, const uja113x_dm_cfg_t * dmConfig)

Sets the CAN partial networking data mask registers (0x68 - 0x6F) based on input configuration object.

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the CAN partial networking data mask registers have not been written properly and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>dmConfig</i>	CAN partial networking data masks configuration object

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Note

This function configures all the data masks. In case the user is interested in configuring a single mask, a general function for SBC register write can be used instead!
As the SPI protocol allows only 16/24/32 bit writes, three subsequent SPI transfers are carried out!

See also

UJA113X_WriteRegister()

Definition at line 827 of file sbc_uja113x.c.

17.3 01. Mode handling

17.3.1 Detailed Description

17.3.2 Introduction

The SBC has two debug modes, the Forced Normal Mode (FNMC) and Software Development mode (SDMC). These modes can be configured in the SBCs MTPNV memory and can be set using the [UJA113X_SetMtpnv\(\)](#) function. Be aware while writing the non-volatile memory, as these registers can't be rewritten again easily. Clearing the non-volatile memory requires special treatment, see [Restoring MTPNV factory preset values](#) for details. These modes influence the watchdog behaviour and the main purpose is to use them during development, although is not limited just for this use case.

Additionally, the SBC has 3 operating modes the user can switch to (the Normal, Standby and Sleep mode) with [UJA113X_SetMode\(\)](#).

17.3.2.1 Sleep mode

To be able to switch to the Sleep mode, the MTPNV memory has to be set accordingly. In case the Sleep mode is disabled, the request to switch to Sleep mode is ignored.

To enter the sleep mode, any pending interrupts or wake-up events need to be cleared and at least one regular wake-up source has to be enabled. Otherwise a system reset is triggered and the Reset Source Status bit (RSS) is set to 10100 (illegal Sleep mode command received).

17.3.2.2 Normal & Standby mode

There should be no limitation to switch into these two modes except constraints related to watchdog. As the watchdog can be still running, make sure to handle the watchdog properly, otherwise a reset can occur.

Enumerations

- enum [uja113x_mc_mc_t](#) { [MC_SLEEP](#) = 0x01U, [MC_STANDBY](#) = 0x04U, [MC_NORMAL](#) = 0x07U }
- SBC mode configuration options (0x01:MC[2:0])*

Functions

- status_t [UJA113X_SetMode](#) (uint32_t instance, [uja113x_mc_mc_t](#) modeConfig)
- Sets the mode control register (0x01) to get the SBC into a new mode.*

17.3.3 Enumeration Type Documentation

17.3.3.1 enum [uja113x_mc_mc_t](#)

SBC mode configuration options (0x01:MC[2:0])

Implements : [uja113x_mc_mc_t_Class](#)

Enumerator

[MC_SLEEP](#) Set SBC mode to Sleep.

[MC_STANDBY](#) Set SBC mode to Standby.

[MC_NORMAL](#) Set SBC mode to Normal.

Definition at line 257 of file [sbc_uja113x.h](#).

17.3.4 Function Documentation

17.3.4.1 `status_t UJA113X_SetMode (uint32_t instance, uja113x_mc_mc_t modeConfig)`

Sets the mode control register (0x01) to get the SBC into a new mode.

The function prepares a frame based on input parameter and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the watchdog register has not been written and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>modeConfig</i>	New mode

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Note

The SBC can be set into three modes (Normal, Standby, Sleep) based on the input parameter.

Warning

Entering the Normal or Standby mode requires no special treatment. However entering a Sleep mode requires to clear all pending interrupts/events (which would set the SBCs INTN1/INTN2 to high) and at least one wake-up source to be enabled. Otherwise the SBC can get stuck at Sleep mode without a possibility to wake it up!

Definition at line 411 of file `sbc_uja113x.c`.

17.4 01. Primary control

17.4.1 Detailed Description

The primary control registers (0x00 - 0x1F) allow:

- Configuring watchdog (0x00)
- Changing SBC mode (0x01)
- Configuring Fail-safe behaviour (0x02)
- Read SBCs main status (0x03)
- Enable system interrupts (0x04)
- Read watchdog status (0x05)
- Access (read/write) general purpose memory 0 - 3 (0x06 - 0x09)
- Lock specific memory areas (0x0A)

Interrupts and interrupt status is described in [06. Interrupts](#).

Modules

- [01. Mode handling](#)
- [02. Watchdog](#)
- [03. Fail-safe configuration](#)
- [04. Lock control](#)

17.5 01. Regulator configuration

17.5.1 Detailed Description

17.5.2 Introduction

The SBC incorporates two voltage regulators. Configurations influencing behaviour during start-up are stored in the MTPNV memory (see [Start-up control configuration options \(0x73\)](#) & [SBC configuration control options \(0x74\)](#)). After successful start-up, the regulators can be configured by invoking the [UJA113X_SetRegulator\(\)](#).

Data Structures

- struct [uja113x_rc_cfg_t](#)

Regulator control register configuration structure (0x10) [More...](#)

Enumerations

- enum [uja113x_rc_v2sc_t](#) { [V2SC_NONE](#) = 0x00U, [V2SC_UNDRVOLTAGE](#) = 0x10U, [V2SC_OVERVOLTAGE](#) = 0x20U, [V2SC_FULL](#) = 0x30U }

V2 shut-down response to over- or undervoltage configuration options (0x10:V2SC[5:4])

- enum [uja113x_rc_v2c_t](#) { [V2C_OFF](#) = 0x00U, [V2C_ON_N](#) = 0x04U, [V2C_ON_NSR](#) = 0x08U, [V2C_ON_NSSRF](#) = 0x0CU }

V2 control configuration options (0x10:V2C[3:2])

- enum [uja113x_rc_v1rtc_t](#) { [V1RTC_90_NOMINAL_OUT](#) = 0x00U, [V1RTC_80_NOMINAL_OUT](#) = 0x01U, [V1RTC_70_NOMINAL_OUT](#) = 0x02U, [V1RTC_60_NOMINAL_OUT](#) = 0x03U }

V1 undervoltage reset threshold configuration options (0x10:V1RTC[1:0])

Functions

- status_t [UJA113X_SetRegulator](#) (uint32_t instance, const [uja113x_rc_cfg_t](#) *rcConfig)

Sets the regulator control register (0x10) based on input configuration object.

17.5.3 Data Structure Documentation

17.5.3.1 struct [uja113x_rc_cfg_t](#)

Regulator control register configuration structure (0x10)

Implements : [uja113x_rc_cfg_t_Class](#)

Definition at line 1451 of file [sbc_uja113x.h](#).

Data Fields

- [uja113x_rc_v2sc_t](#) v2ShutdownCtrl

Configures V2 shut-down response to a battery over- or undervoltage configuration (0x10:V2SC[5:4])

- [uja113x_rc_v2c_t](#) v2Ctrl

Configures output behavior on V2 (0x10:V2C[3:2])

- [uja113x_rc_v1rtc_t](#) v1RstThrCtrl

Configures V1 undervoltage reset threshold (0x10:V1RTC[1:0])

Field Documentation

17.5.3.1.1 `uja113x_rc_v1rtc_t v1RstThrCtrl`

Configures V1 undervoltage reset threshold (0x10:V1RTC[1:0])

Definition at line 1464 of file `sbc_uja113x.h`.

17.5.3.1.2 `uja113x_rc_v2c_t v2Ctrl`

Configures output behavior on V2 (0x10:V2C[3:2])

Definition at line 1460 of file `sbc_uja113x.h`.

17.5.3.1.3 `uja113x_rc_v2sc_t v2ShutdownCtrl`

Configures V2 shut-down response to a battery over- or undervoltage configuration (0x10:V2SC[5:4])

Definition at line 1456 of file `sbc_uja113x.h`.

17.5.4 Enumeration Type Documentation

17.5.4.1 `enum uja113x_rc_v1rtc_t`

V1 undervoltage reset threshold configuration options (0x10:V1RTC[1:0])

Implements : `uja113x_rc_v1rtc_t_Class`

Enumerator

`V1RTC_90_NOMINAL_OUT` Reset threshold set to 90% of V1 nominal output voltage.

`V1RTC_80_NOMINAL_OUT` Reset threshold set to 80% of V1 nominal output voltage.

`V1RTC_70_NOMINAL_OUT` Reset threshold set to 70% of V1 nominal output voltage.

`V1RTC_60_NOMINAL_OUT` Reset threshold set to 60% of V1 nominal output voltage.

Definition at line 403 of file `sbc_uja113x.h`.

17.5.4.2 `enum uja113x_rc_v2c_t`

V2 control configuration options (0x10:V2C[3:2])

Implements : `uja113x_rc_v2c_t_Class`

Enumerator

`V2C_OFF` V2 off in all modes.

`V2C_ON_N` V2 on in Normal mode.

`V2C_ON_NSR` V2 on in Normal, Standby and Reset modes.

`V2C_ON_NSSRF` V2 on in Normal, Standby, Sleep, Reset and FSP mode.

Definition at line 388 of file `sbc_uja113x.h`.

17.5.4.3 `enum uja113x_rc_v2sc_t`

V2 shut-down response to over- or undervoltage configuration options (0x10:V2SC[5:4])

Implements : `uja113x_rc_v2sc_t_Class`

Enumerator

`V2SC_NONE` No shut-down in response to over- or undervoltage.

`V2SC_UNDRVOLTAGE` Shut-down in response to undervoltage.

V2SC_OVERVOLTAGE Shut-down in response to overvoltage.

V2SC_FULL Shut-down in response to over- or undervoltage.

Definition at line 373 of file sbc_uja113x.h.

17.5.5 Function Documentation

17.5.5.1 status_t UJA113X_SetRegulator (uint32_t instance, const uja113x_rc_cfg_t * rcConfig)

Sets the regulator control register (0x10) based on input configuration object.

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the regulator control register has not been written and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>rcConfig</i>	Regulator control configuration object

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Definition at line 519 of file sbc_uja113x.c.

17.6 02. Battery monitor configuration

17.6.1 Detailed Description

17.6.2 Introduction

The battery monitor can measure the voltage either on BAT or BATSENSE pin and is able to generate an interrupt in case of under-/overvoltage in Normal mode.

To read the content of the ADC, the [UJA113X_SbcTransfer\(\)](#) function can be used. No dedicated function for reading the ADC is available at the moment.

[UJA113X_SetBatteryMonitor\(\)](#) can be used to configure the whole battery monitor except interrupts.

Data Structures

- struct [uja113x_bmc_cfg_t](#)

Battery monitor registers configuration structure (0x11 - 0x14) [More...](#)

Typedefs

- typedef bool [uja113x_bmetsc_bmsc_t](#)
Battery monitor event trigger source control (0x11:BMSC[0])
- typedef uint8_t [uja113x_bmutc_bmutc_t](#)
Battery monitor undervoltage threshold control parameter (0x12:BMUTC[7:0])
- typedef uint8_t [uja113x_bmotc_bmotc_t](#)
Battery monitor overvoltage threshold control parameter (13:BMOTC[7:0])
- typedef uint8_t [uja113x_bmhc_bmhc_t](#)
Battery monitor hysteresis for overvoltage control parameter (0x14:BMHOC[7:4])
- typedef uint8_t [uja113x_bmhc_bmhc_t](#)
Battery monitor hysteresis for undervoltage control parameter (0x14:BMHUC[3:0])

Enumerations

- enum [uja113x_bscdt_ionsctc_t](#) { [IONSCTC_30_MA](#) = 0U, [IONSCTC_45_MA](#) = 1U, [IONSCTC_60_MA](#) = 2U, [IONSCTC_90_MA](#) = 3U }
Bank N short-circuit detection threshold configuration options (0x39 / 0x49)
- enum [uja113x_boldt_ionoltc_t](#) { [IONOLTC_2_MA](#) = 0U, [IONOLTC_5_MA](#) = 1U, [IONOLTC_10_MA](#) = 2U, [IONOLTC_20_MA](#) = 3U }
Bank N open-load detection threshold configuration options (0x3A / 0x4A)

Functions

- status_t [UJA113X_SetBatteryMonitor](#) (uint32_t instance, const [uja113x_bmc_cfg_t](#) *bmcConfig)
Sets the Battery monitor control registers (0x11 - 0x14) based on input configuration object.

17.6.3 Data Structure Documentation

17.6.3.1 struct [uja113x_bmc_cfg_t](#)

Battery monitor registers configuration structure (0x11 - 0x14)

Implements : [uja113x_bmc_cfg_t_Class](#)

Definition at line 1474 of file [sbc_uja113x.h](#).

Data Fields

- [uja113x_bmetsc_bmsc_t bmSrcCtrl](#)
Selects the battery monitor event trigger source (0x11:BMSC[0])
- [uja113x_bmutc_bmutc_t bmUndrVoltThr](#)
Configures the battery monitor undervoltage threshold (0x12:BMUTC[7:0])
- [uja113x_bmotc_bmotc_t bmOverVoltThr](#)
Configures the battery monitor overvoltage threshold (0x13:BMOTC[7:0])
- [uja113x_bmhc_bmhc_t bmOverVoltThrRel](#)
Configures the battery monitor hysteresis for overvoltage (0x14:BMHOC[7:4])
- [uja113x_bmhc_bmhc_t bmUndrVoltThrRel](#)
Configures the battery monitor hysteresis for undervoltage (0x14:BMHUC[3:0])

Field Documentation

17.6.3.1.1 [uja113x_bmotc_bmotc_t bmOverVoltThr](#)

Configures the battery monitor overvoltage threshold (0x13:BMOTC[7:0])

Threshold for triggering a battery overvoltage event and BMOI interrupt

threshold = BMOTC[7:0]/255 x 20V

Allowed range: 0 - 255

Definition at line 1491 of file sbc_uja113x.h.

17.6.3.1.2 [uja113x_bmhc_bmhc_t bmOverVoltThrRel](#)

Configures the battery monitor hysteresis for overvoltage (0x14:BMHOC[7:4])

Battery monitor overvoltage threshold release level;

release level = BMHOC[7:4] x 4/255 x 20V below threshold defined by BMOTC

Warning

Only 4 lsb are used! The upper part of byte is truncated!

Definition at line 1498 of file sbc_uja113x.h.

17.6.3.1.3 [uja113x_bmetsc_bmsc_t bmSrcCtrl](#)

Selects the battery monitor event trigger source (0x11:BMSC[0])

Definition at line 1479 of file sbc_uja113x.h.

17.6.3.1.4 [uja113x_bmutc_bmutc_t bmUndrVoltThr](#)

Configures the battery monitor undervoltage threshold (0x12:BMUTC[7:0])

Threshold for triggering a battery undervoltage event and BMUI interrupt;

threshold = BMUTC[7:0]/255 x 20V.

Allowed range: 0 - 255

Definition at line 1485 of file sbc_uja113x.h.

17.6.3.1.5 [uja113x_bmhc_bmhc_t bmUndrVoltThrRel](#)

Configures the battery monitor hysteresis for undervoltage (0x14:BMHUC[3:0])

Battery monitor undervoltage threshold release level;

release level = BMHUC[3:0] x 4/255 x 20V above threshold defined by BMUTC

Warning

Only 4 lsb are used! The upper part of byte is truncated!

Definition at line 1505 of file sbc_uja113x.h.

17.6.4 Typedef Documentation**17.6.4.1 typedef bool uja113x_bmetsc_bmsc_t**

Battery monitor event trigger source control (0x11:BMSC[0])

false - BAT pin is source of event triggers

true - BATSENSE pin is source of event triggers

Implements : uja113x_bmetsc_bmsc_t_Class

Definition at line 420 of file sbc_uja113x.h.

17.6.4.2 typedef uint8_t uja113x_bmhc_bmhoc_t

Battery monitor hysteresis for overvoltage control parameter (0x14:BMHOC[7:4])

Implements uja113x_bmhc_bmhoc_t_Class

Definition at line 447 of file sbc_uja113x.h.

17.6.4.3 typedef uint8_t uja113x_bmhc_bmhuc_t

Battery monitor hysteresis for undervoltage control parameter (0x14:BMHUC[3:0])

Implements uja113x_bmhc_bmhuc_t_Class

Definition at line 456 of file sbc_uja113x.h.

17.6.4.4 typedef uint8_t uja113x_bmotc_bmotc_t

Battery monitor overvoltage threshold control parameter (13:BMOTC[7:0])

Implements : uja113x_bmotc_bmotc_t_Class Allowed range: 0 - 255

Definition at line 438 of file sbc_uja113x.h.

17.6.4.5 typedef uint8_t uja113x_bmutc_bmutc_t

Battery monitor undervoltage threshold control parameter (0x12:BMUTC[7:0])

Implements : uja113x_bmutc_bmutc_t_Class Allowed range: 0 - 255

Definition at line 429 of file sbc_uja113x.h.

17.6.5 Enumeration Type Documentation**17.6.5.1 enum uja113x_boldt_ionoltc_t**

Bank N open-load detection threshold configuration options (0x3A / 0x4A)

Note

For details, consult the reference manual - "Static characteristics: lth(det)open"

Implements : uja113x_boldt_ionoltc_t_Class

Enumerator

IONOLTC_2_MA HVIO N open-load detection threshold set to 2 mA.

IONOLTC_5_MA HVIO N open-load detection threshold set to 5 mA.

IONOLTC_10_MA HVIO N open-load detection threshold set to 10 mA.

IONOLTC_20_MA HVIO N open-load detection threshold set to 20 mA.

Definition at line 1065 of file sbc_uja113x.h.

17.6.5.2 enum uja113x_bscdt_ionsctc_t

Bank N short-circuit detection threshold configuration options (0x39 / 0x49)

Note

For details consult the reference manual - "Static characteristics: lth(det)sc"

Implements : uja113x_bscdt_ionsctc_t_Class

Enumerator

IONSCTC_30_MA HVIO N short-circuit detection threshold set to 30 mA.

IONSCTC_45_MA HVIO N short-circuit detection threshold set to 45 mA.

IONSCTC_60_MA HVIO N short-circuit detection threshold set to 60 mA.

IONSCTC_90_MA HVIO N short-circuit detection threshold set to 90 mA.

Definition at line 1050 of file sbc_uja113x.h.

17.6.6 Function Documentation

17.6.6.1 status_t UJA113X_SetBatteryMonitor (uint32_t instance, const uja113x_bmc_cfg_t * bmcConfig)

Sets the Battery monitor control registers (0x11 - 0x14) based on input configuration object.

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the regulator control registers were not written properly and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>bmcConfig</i>	Battery monitor control configuration object

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Note

The function configures all the battery monitor features:

1. Battery monitor event trigger source (0x11)
2. Battery monitor undervoltage threshold (0x12)
3. Battery monitor overvoltage threshold (0x13)
4. Battery monitor hysteresis (0x14)

As the SPI protocol allows only 16/24/32 bit writes, two subsequent SPI transfers are carried out!

Definition at line 546 of file sbc_uja113x.c.

17.7 02. LIN configuration

17.7.1 Detailed Description

17.7.2 Introduction

A UJA113x device can incorporate up to 2 LIN transceivers minimum of 1. Configurable LIN features are:

- LIN slope
- LIN mode

To configure the LIN transceiver, [UJA113X_SetLin\(\)](#) function can be used.

Warning

In case the user decides to implement his own function or use the [UJA113X_SbcTransfer\(\)](#), to write the LIN control register (0x21), make sure LIN2 bits are cleared for devices with a single LIN transceiver (see reference manual, register 0x21 description, for details).

Data Structures

- struct [uja113x_linc_cfg_t](#)
LIN control register configuration structure (0x21) [More...](#)

Enumerations

- enum [uja113x_linc_lsc2_t](#) { [LSC2_SLOPE_ACTIVE](#) = 0x00U, [LSC2_SLOPE_ACTIVE2](#) = 0x40U, [LSC2_SLOPE_ACTIVE_TXDL_TIMEOUT](#) = 0x80U }
LIN2 slope control configuration options (0x21:LSC2[7:6])
- enum [uja113x_linc_lmc2_t](#) { [LMC2_TRANSCEIVER_OFF](#) = 0x00U, [LMC2_TRANSCEIVER_ON](#) = 0x10U, [LMC2_TRANSCEIVER_ON2](#) = 0x20U, [LMC2_TRANSCEIVER_LISTEN](#) = 0x30U }
LIN2 transceiver operating mode configuration options (0x21:LMC2[5:4])
- enum [uja113x_linc_lsc1_t](#) { [LSC1_SLOPE_ACTIVE](#) = 0x00U, [LSC1_SLOPE_ACTIVE2](#) = 0x04U, [LSC1_SLOPE_ACTIVE_TXDL_TIMEOUT](#) = 0x08U }
LIN/LIN1 slope control configuration options (0x21:LSC1[3:2])
- enum [uja113x_linc_lmc1_t](#) { [LMC1_TRANSCEIVER_OFF](#) = 0x00U, [LMC1_TRANSCEIVER_ON](#) = 0x01U, [LMC1_TRANSCEIVER_ON2](#) = 0x02U, [LMC1_TRANSCEIVER_LISTEN](#) = 0x03U }
LIN/LIN1 transceiver operating mode configuration options (0x21:LMC1[1:0])

Functions

- status_t [UJA113X_SetLin](#) (uint32_t instance, const [uja113x_linc_cfg_t](#) *lincConfig)
Sets the LIN control register (0x21) based on input configuration object.

17.7.3 Data Structure Documentation

17.7.3.1 struct [uja113x_linc_cfg_t](#)

LIN control register configuration structure (0x21)

Implements : [uja113x_linc_cfg_t_Class](#)

Definition at line 1565 of file [sbc_uja113x.h](#).

Data Fields

- [uja113x_linc_lsc2_t lin2SlopeCtrl](#)
Configures LIN2 slope control behaviour (0x21:LSC2[7:6])
- [uja113x_linc_lmc2_t lin2ModeCtrl](#)
Configures LIN2 transceiver operating mode (0x21:LMC2[5:4])
- [uja113x_linc_lsc1_t lin1SlopeCtrl](#)
Configures LIN1 slope control behaviour (0x21:LSC1[3:2])
- [uja113x_linc_lmc1_t lin1ModeCtrl](#)
Configures LIN1 transceiver operating mode (0x21:LMC1[1:0])

Field Documentation

17.7.3.1.1 [uja113x_linc_lmc1_t lin1ModeCtrl](#)

Configures LIN1 transceiver operating mode (0x21:LMC1[1:0])

Definition at line 1582 of file sbc_uja113x.h.

17.7.3.1.2 [uja113x_linc_lsc1_t lin1SlopeCtrl](#)

Configures LIN1 slope control behaviour (0x21:LSC1[3:2])

Definition at line 1578 of file sbc_uja113x.h.

17.7.3.1.3 [uja113x_linc_lmc2_t lin2ModeCtrl](#)

Configures LIN2 transceiver operating mode (0x21:LMC2[5:4])

Definition at line 1574 of file sbc_uja113x.h.

17.7.3.1.4 [uja113x_linc_lsc2_t lin2SlopeCtrl](#)

Configures LIN2 slope control behaviour (0x21:LSC2[7:6])

Definition at line 1570 of file sbc_uja113x.h.

17.7.4 Enumeration Type Documentation

17.7.4.1 [enum uja113x_linc_lmc1_t](#)

LIN/LIN1 transceiver operating mode configuration options (0x21:LMC1[1:0])

Implements : [uja113x_linc_lmc1_t_Class](#)

Enumerator

- LMC1_TRANSCEIVER_OFF** Offline.
- LMC1_TRANSCEIVER_ON** Active mode (when SBC in normal mode).
- LMC1_TRANSCEIVER_ON2** Active mode (when SBC in normal mode).
- LMC1_TRANSCEIVER_LISTEN** Listen-only mode.

Definition at line 691 of file sbc_uja113x.h.

17.7.4.2 [enum uja113x_linc_lmc2_t](#)

LIN2 transceiver operating mode configuration options (0x21:LMC2[5:4])

Implements : [uja113x_linc_lmc2_t_Class](#)

Enumerator

LMC2_TRANSCEIVER_OFF Offline.

LMC2_TRANSCEIVER_ON Active mode (when SBC in normal mode).

LMC2_TRANSCEIVER_ON2 Active mode (when SBC in normal mode).

LMC2_TRANSCEIVER_LISTEN Listen-only mode.

Definition at line 661 of file sbc_uja113x.h.

17.7.4.3 enum uja113x_linc_lsc1_t

LIN/LIN1 slope control configuration options (0x21:LSC1[3:2])

Implements : uja113x_linc_lsc1_t_Class

Enumerator

LSC1_SLOPE_ACTIVE Slope control active.

LSC1_SLOPE_ACTIVE2 Slope control active.

LSC1_SLOPE_ACTIVE_TXDL_TIMEOUT Slope control active and TXDL dominant time-out deactivated.

Definition at line 676 of file sbc_uja113x.h.

17.7.4.4 enum uja113x_linc_lsc2_t

LIN2 slope control configuration options (0x21:LSC2[7:6])

Implements : uja113x_linc_lsc2_t_Class

Enumerator

LSC2_SLOPE_ACTIVE Slope control active.

LSC2_SLOPE_ACTIVE2 Slope control active.

LSC2_SLOPE_ACTIVE_TXDL_TIMEOUT Slope control active and TXDL dominant time-out deactivated.

Definition at line 646 of file sbc_uja113x.h.

17.7.5 Function Documentation

17.7.5.1 status_t UJA113X_SetLin (uint32_t instance, const uja113x_linc_cfg_t * lincConfig)

Sets the LIN control register (0x21) based on input configuration object.

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the LIN control register has not been written properly and the process has to be repeated.

Parameters

in	instance	Index of SBC to configure
in	lincConfig	LIN control configuration object

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Note

The reference manual states, that bits 7:4 (LIN2 configuration) of register 0x21 should remain cleared for devices incorporating only LIN1. Therefore for these devices the function clears bits even when configured to non-zero value!

Definition at line 675 of file sbc_uja113x.c.

17.8 02. Supply control

17.8.1 Detailed Description

The supply control registers (0x10 - 0x1F) allow:

- Configuring voltage regulators (0x10)
- Configuring battery monitor (0x11 - 0x18)
- Configuring switched Mode Power Supply (0x19 - 0x1A)
- Read supply voltage status (0x1B)
- Enable supply interrupts (0x1C)

Interrupts and interrupt status is described in [06. Interrupts](#).

Modules

- [01. Regulator configuration](#)
- [02. Battery monitor configuration](#)
- [03. SMPS configuration](#)

17.9 02. Watchdog

17.9.1 Detailed Description

17.9.2 Introduction

The watchdog behaviour can be influenced by the debug modes (see mode [Introduction](#) for details) in combination with the watchdog mode (window, timeout or autonomous mode). The watchdog period is adjustable ranging from 8 ms to 4094 ms.

17.9.2.1 Watchdog in FNMC

In Forced Normal Mode the Watchdog is completely disabled. Thus, configuring the watchdog mode has no influence on it's operation!

17.9.2.2 Watchdog in SDMC

In Software Development Mode the watchdog can be activated or disabled based on configured watchdog mode. In case the timeout or window mode is selected, the watchdog is active independent from SDMC. For autonomous mode, the watchdog is active (only timeout mode) while SDMC = 0. For SDMC = 1, the watchdog stays inactive in autonomous mode!

Following table summarizes all the use cases.

SBC state	Watchdog Configurations			
	SDMC = x WMC = 100 (Window)	SDMC = x WMC = 010 (Timeout)	SDMC = 0 WMC = 001 (Autonomous)	SDMC = 1 WMC = 001 (Autonomous)
Normal mode	Window	Timeout	Timeout	Off
Standby mode (INTN1 HIGH)	Timeout	Timeout	Off	Off
Standby mode (INTN1 LOW)	Timeout	Timeout	Timeout	Off
Sleep mode	Timeout	Timeout	Off	Off
Forced Normal mode	Off	Off	Off	Off
Other modes	Off	Off	Off	Off

Table 1: Summary of Watchdog settings

17.9.2.3 Watchdog mode configuration

The watchdog mode can be reconfigured only in Standby mode using the [UJA113X_SetWatchdog\(\)](#). Writes leading to change the watchdog mode in other modes than Standby would cause a switch to reset mode and reset source status (RSS) bit will be set to 10000 (illegal watchdog mode control access).

From this perspective it's the users responsibility to switch the SBC into Standby mode prior to watchdog mode update.

17.9.2.4 Watchdog trigger

To reset the watchdog timer a successful write into the watchdog control register has to be performed. The [UJA113X_SetWatchdog\(\)](#) function can be used. If a new mode/period have changed as a result of the write access, the new values are valid immediately.

Warning

Writing a different mode while resetting the watchdog timer can cause a reset in case the SBC is not in Standby mode.

Writing a different period while resetting the watchdog timer can result in reset as a consequence of a watchdog counter overflow due to period change.

Data Structures

- struct [uja113x_wtdc_cfg_t](#)
Watchdog register configuration structure (reg 0x00) [More...](#)

Enumerations

- enum [uja113x_wtdc_wmc_t](#) { [WMC_AUTONOMOUS](#) = 0x20U, [WMC_TIMEOUT](#) = 0x40U, [WMC_WINDOW](#) = 0x80U }
Watchdog mode configuration options (0x00:WMC[7:5])
- enum [uja113x_wtdc_nwp_t](#) {
[NWP_PERIOD_8](#) = 0x08U, [NWP_PERIOD_16](#) = 0x01U, [NWP_PERIOD_32](#) = 0x02U, [NWP_PERIOD_64](#) = 0x0BU,
[NWP_PERIOD_128](#) = 0x04U, [NWP_PERIOD_256](#) = 0x0DU, [NWP_PERIOD_1024](#) = 0x0EU, [NWP_PERIOD_4096](#) = 0x07U }
Watchdog nominal period configuration options (0x00:NWP[3:0])

Functions

- status_t [UJA113X_SetWatchdog](#) (uint32_t instance, const [uja113x_wtdc_cfg_t](#) *wtdcConfig)
Sets the watchdog register (0x00) based on input configuration object.

17.9.3 Data Structure Documentation

17.9.3.1 struct [uja113x_wtdc_cfg_t](#)

Watchdog register configuration structure (reg 0x00)

Implements : [uja113x_wtdc_cfg_t_Class](#)

Definition at line 1373 of file [sbc_uja113x.h](#).

Data Fields

- [uja113x_wtdc_wmc_t wtdModeCtrl](#)
Configures the Watchdog Mode (0x00:WMC[7:5])
- [uja113x_wtdc_nwp_t nomWtdPeriod](#)
Configures the watchdog nominal period (0x00:NWP[3:0])

Field Documentation

17.9.3.1.1 [uja113x_wtdc_nwp_t nomWtdPeriod](#)

Configures the watchdog nominal period (0x00:NWP[3:0])

Definition at line 1382 of file [sbc_uja113x.h](#).

17.9.3.1.2 [uja113x_wtdc_wmc_t wtdModeCtrl](#)

Configures the Watchdog Mode (0x00:WMC[7:5])

Definition at line 1378 of file [sbc_uja113x.h](#).

17.9.4 Enumeration Type Documentation

17.9.4.1 enum [uja113x_wtdc_nwp_t](#)

Watchdog nominal period configuration options (0x00:NWP[3:0])

Implements : `uja113x_wtdc_nwp_t_Class`

Enumerator

`NWP_PERIOD_8` 8 ms nominal period.
`NWP_PERIOD_16` 16 ms nominal watchdog period.
`NWP_PERIOD_32` 32 ms nominal watchdog period.
`NWP_PERIOD_64` 64 ms nominal watchdog period.
`NWP_PERIOD_128` 128 ms nominal watchdog period.
`NWP_PERIOD_256` 256 ms nominal watchdog period.
`NWP_PERIOD_1024` 1024 ms nominal watchdog period.
`NWP_PERIOD_4096` 4096 ms nominal watchdog period.

Definition at line 238 of file `sbc_uja113x.h`.

17.9.4.2 enum `uja113x_wtdc_wmc_t`

Watchdog mode configuration options (0x00:WMC[7:5])

Implements : `uja113x_wtdc_wmc_t_Class`

Enumerator

`WMC_AUTONOMOUS` Watchdog autonomous mode
`WMC_TIMEOUT` Watchdog timeout mode.
`WMC_WINDOW` Watchdog window mode.

Definition at line 224 of file `sbc_uja113x.h`.

17.9.5 Function Documentation

17.9.5.1 `status_t UJA113X_SetWatchdog (uint32_t instance, const uja113x_wtdc_cfg_t * wtdcConfig)`

Sets the watchdog register (0x00) based on input configuration object.

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the watchdog register has not been written and the process has to be repeated.

Parameters

<code>in</code>	<code>instance</code>	Index of SBC to configure
<code>in</code>	<code>wtdcConfig</code>	Watchdog configuration object

Returns

`STATUS_SUCCESS` Configuration successful
`STATUS_BUSY` SPI peripheral is busy
`STATUS_TIMEOUT` SPI communication timed out, configuration aborted
`SBC_CMD_ERROR` First received byte doesn't match the repeated address, configuration failed.

Warning

The watchdog mode can be re-configured in Standby mode only! Changing the watchdog mode in Normal mode will cause the UJA113x to switch to Reset mode and the reset source status bits (RSS) will be set to 10000 (illegal watchdog mode control access). However writing the same values doesn't lead to SBC reset, but a watchdog trigger which clears the watchdog counter!

Note

To reset the watchdog counter, a successful write into the watchdog control register (0x00) has to be performed. This function can be used to reset the counter, however keep in mind that updating mode in non-↔ Standby modes leads to SBC reset!

Although updating the watchdog period is allowed, SBC reset due to an overflow can happen after configuring a shorter period!

See also

[UJA113X_SetMode\(\)](#)

Definition at line 385 of file sbc_uja113x.c.

17.10 03. Fail-safe configuration

17.10.1 Detailed Description

17.10.2 Introduction

The SBC incorporates following fail-safe features:

- EN pin
 - can control an external hardware
 - can operate as general purpose output when system is running properly
- LIMP pin
 - enables "limp home" hardware in case of ECU failure
- Advanced LIMP home function via HVIO 4 - 2 configurable in non-volatile memory (see MTPNV [Introduction](#) for details)
- Register locking (see lock control [Introduction](#) for details)
- Reset counter

17.10.2.1 Reset mechanism

If the system resets, the SBC initiates a reset process, during which a reset counter is incremented. In case the counter equals 3 when the UJA113x enters reset mode, the SBC assumes that a serious failure has occurred and switches to Forced Sleep mode (FSP), enabling the limp home function. A properly designed system should reset this counter to avoid its overflow.

The [UJA113X_SetFailSafe\(\)](#) function which configures the fail-safe functionality can be also used to update the reset counter. However the parameters for EN pin and LIMP home pin should reflect the current configuration!

The reset counter can be (pre)configured to any value providing additional level of safety. For instance, setting the counter to 3 would mean no errors allowed (in case an error occurs, the system would be forced to FSP immediately)!

Data Structures

- struct [uja113x_fsc_cfg_t](#)
Fail-safe register configuration structure (reg 0x02) [More...](#)

Typedefs

- typedef bool [uja113x_fsc_endc_t](#)
EN high-side driver activation options (0x02:ENDC[5])
- typedef bool [uja113x_fsc_lhc_t](#)
LIMP output configuration options (0x02:LHC[2])
- typedef uint8_t [uja113x_fsc_rcc_t](#)
SBC reset counter configuration option (0x02:RCC[1:0])

Enumerations

- enum [uja113x_fsc_ensc_t](#) { [ENSC_NONE](#) = 0x00U, [ENSC_UNDRVOLTAGE](#) = 0x40U, [ENSC_OVERVOLTAGE](#) = 0x80U, [ENSC_FULL](#) = 0xC0U }
EN pin shut-down control configuration options (0x02:ENSC[7:6])
- enum [uja113x_fsc_enc_t](#) { [ENC_LOW](#) = 0x00U, [ENC_HIGH_NRS](#) = 0x08U, [ENC_HIGH_N](#) = 0x10U, [ENC_TIMER](#) = 0x18U }
EN pin output control configuration options (0x02:ENC[4:3])

Functions

- [status_t UJA113X_SetFailSafe](#) (uint32_t instance, const [uja113x_fsc_cfg_t](#) *fscConfig)
Sets the fail-safe register (0x02) based on input configuration object.

17.10.3 Data Structure Documentation

17.10.3.1 struct [uja113x_fsc_cfg_t](#)

Fail-safe register configuration structure (reg 0x02)

Implements : [uja113x_fsc_cfg_t_Class](#)

Definition at line 1392 of file [sbc_uja113x.h](#).

Data Fields

- [uja113x_fsc_ensc_t enShutdownCtrl](#)
Configures the behaviour of EN pin during battery over-/undervoltage (0x02:ENSC[7:6])
- [uja113x_fsc_endc_t enDriverCtrl](#)
Enables/disables the EN high-side driver (0x02:ENDC[5])
- [uja113x_fsc_enc_t enCtrl](#)
Configures the output level behaviour of EN pin (0x02:ENC[4:3])
- [uja113x_fsc_lhc_t limpHomeCtrl](#)
Configures the Limp pin output behaviour (0x02:LHC[2])
- [uja113x_fsc_rcc_t resetCntCtrl](#)
Configures the Reset counter value (0x02:RCC[1:0])

Field Documentation

17.10.3.1.1 [uja113x_fsc_enc_t enCtrl](#)

Configures the output level behaviour of EN pin (0x02:ENC[4:3])

Definition at line 1405 of file [sbc_uja113x.h](#).

17.10.3.1.2 [uja113x_fsc_endc_t enDriverCtrl](#)

Enables/disables the EN high-side driver (0x02:ENDC[5])

Definition at line 1401 of file [sbc_uja113x.h](#).

17.10.3.1.3 [uja113x_fsc_ensc_t enShutdownCtrl](#)

Configures the behaviour of EN pin during battery over-/undervoltage (0x02:ENSC[7:6])

Definition at line 1397 of file [sbc_uja113x.h](#).

17.10.3.1.4 [uja113x_fsc_lhc_t limpHomeCtrl](#)

Configures the Limp pin output behaviour (0x02:LHC[2])

Definition at line 1409 of file [sbc_uja113x.h](#).

17.10.3.1.5 [uja113x_fsc_rcc_t resetCntCtrl](#)

Configures the Reset counter value (0x02:RCC[1:0])

Definition at line 1413 of file [sbc_uja113x.h](#).

17.10.4 Typedef Documentation

17.10.4.1 typedef bool uja113x_fsc_endc_t

EN high-side driver activation options (0x02:ENDC[5])

false - EN high-side driver enabled; push-pull output

true - EN high-side driver disabled; open-drain low-side driver

Implements : uja113x_fsc_endc_t_Class

Definition at line 288 of file sbc_uja113x.h.

17.10.4.2 typedef bool uja113x_fsc_lhc_t

LIMP output configuration options (0x02:LHC[2])

false - LIMP pin is floating

true - LIMP pin is driven LOW

Implements : uja113x_fsc_lhc_t_Class

Definition at line 316 of file sbc_uja113x.h.

17.10.4.3 typedef uint8_t uja113x_fsc_rcc_t

SBC reset counter configuration option (0x02:RCC[1:0])

Implements : uja113x_fsc_rcc_t_Class0 - 3

Definition at line 325 of file sbc_uja113x.h.

17.10.5 Enumeration Type Documentation

17.10.5.1 enum uja113x_fsc_enc_t

EN pin output control configuration options (0x02:ENC[4:3])

Implements : uja113x_fsc_enc_t_Class

Enumerator

ENC_LOW EN pin is driven permanently low.

ENC_HIGH_NRS EN pin is high (or floating if ENDC = 1) when SBC is in Normal, Reset or Standby mode.

ENC_HIGH_N EN pin is high (or floating if ENDC = 1) when SBC is in Normal mode.

ENC_TIMER EN pin is controller by Timer 2.

Definition at line 297 of file sbc_uja113x.h.

17.10.5.2 enum uja113x_fsc_ensc_t

EN pin shut-down control configuration options (0x02:ENSC[7:6])

Implements : uja113x_fsc_ensc_t_Class

Enumerator

ENSC_NONE EN pin not influenced by battery over- or undervoltage.

ENSC_UNDRVOLTAGE EN pin driven LOW when battery undervoltage detected.

ENSC_OVERVOLTAGE EN pin driven LOW when battery overvoltage detected.

ENSC_FULL EN pin driven LOW when battery over- or undervoltage detected.

Definition at line 271 of file sbc_uja113x.h.

17.10.6 Function Documentation

17.10.6.1 `status_t UJA113X_SetFailSafe (uint32_t instance, const uja113x_fsc_cfg_t * fscConfig)`

Sets the fail-safe register (0x02) based on input configuration object.

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the fail-safe control register has not been written and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>fscConfig</i>	Fail-safe configuration object

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Warning

Care has to be taken while configuring the reset counter (resetCntCtrl). In case the SBC reset counter is set to 3 and a reset occurs, the SBC will be switched into Forced Sleep Mode! This can be used as a safety measure, which doesn't allow any SBC resets, however can lead to unexpected behavior if configured improperly! Read the datasheet carefully to configure this parameter the right way.

Note

After every SBC reset the reset counter is incremented. To reset the counter, call this function with a requested reset counter value.

Bear in mind that "clearing" the reset counter requires you to write the whole register. This can clear your preconfigured values from SBC initialization step leading to unwanted behavior. So in case of reset counter reset, the rest of parameters has to be configured as well!

Definition at line 435 of file sbc_uja113x.c.

17.11 03. SMPS configuration

17.11.1 Detailed Description

17.11.2 Introduction

The Switched Mode Power Supply (SMPS) can be configured by invoking the [UJA113X_SetSmpls\(\)](#) function.

Data Structures

- struct [uja113x_smpsc_cfg_t](#)
SMPS (buck-boost converter) registers configuration structure (0x19 - 0x1A) [More...](#)

Typedefs

- typedef bool [uja113x_smpsc_smpsotc_t](#)
SMPS overtemperature configuration options (0x19:SMPSOTC[3])

Enumerations

- enum [uja113x_smpsc_smpsc_t](#) { [SMPSC_ON_NSR](#) = 0x00U, [SMPSC_ON_NSRS](#) = 0x01U, [SMPSC_PASSTHROUGH_NSS](#) = 0x03U }
SMPS on/off configuration options (0x19:SMPSOC[1:0])
- enum [uja113x_smpsovc_smpsoc_t](#) {
[SMPSOC_50V](#) = 0x00U, [SMPSOC_52V](#) = 0x01U, [SMPSOC_54V](#) = 0x02U, [SMPSOC_56V](#) = 0x03U,
[SMPSOC_58V](#) = 0x04U, [SMPSOC_60V](#) = 0x05U, [SMPSOC_62V](#) = 0x06U, [SMPSOC_64V](#) = 0x07U,
[SMPSOC_66V](#) = 0x08U, [SMPSOC_68V](#) = 0x09U, [SMPSOC_70V](#) = 0x0AU, [SMPSOC_72V](#) = 0x0BU,
[SMPSOC_74V](#) = 0x0CU, [SMPSOC_76V](#) = 0x0DU, [SMPSOC_78V](#) = 0x0EU, [SMPSOC_80V](#) = 0x0FU }
SMPS output voltage configuration options (0x1A:SMPSOC[3:0])

Functions

- status_t [UJA113X_SetSmpls](#) (uint32_t instance, const [uja113x_smpsc_cfg_t](#) *smpscConfig)
Sets the SMPS control registers (0x19 - 0x1A) based on input configuration object.

17.11.3 Data Structure Documentation

17.11.3.1 struct uja113x_smpsc_cfg_t

SMPS (buck-boost converter) registers configuration structure (0x19 - 0x1A)

Implements : [uja113x_smpsc_cfg_t_Class](#)

Definition at line 1515 of file [sbc_uja113x.h](#).

Data Fields

- [uja113x_smpsc_smpsotc_t smpsOvertempCtrl](#)
Configures the behavior of Vvsmps voltage output during overtemperature (0x19:SMPSOTC[3])
- [uja113x_smpsc_smpsc_t smpsCtrl](#)
Configures the SMPS on/off state in different modes (0x19:SMPSOC[1:0])
- [uja113x_smpsovc_smpsoc_t smpsOutVolt](#)
Configures the SMPS output voltage level (0x1A:SMPSOC[3:0])

Field Documentation

17.11.3.1.1 `uja113x_smpsc_smpsc_t smpsCtrl`

Configures the SMPS on/off state in different modes (0x19:SMPSOC[1:0])

Definition at line 1524 of file `sbc_uja113x.h`.

17.11.3.1.2 `uja113x_smpsovc_smpsoc_t smpsOutVolt`

Configures the SMPS output voltage level (0x1A:SMPSOC[3:0])

Definition at line 1528 of file `sbc_uja113x.h`.

17.11.3.1.3 `uja113x_smpsc_smpsotc_t smpsOvertempCtrl`

Configures the behavior of Vvsmps voltage output during overtemperature (0x19:SMPSOTC[3])

Definition at line 1520 of file `sbc_uja113x.h`.

17.11.4 Typedef Documentation

17.11.4.1 `typedef bool uja113x_smpsc_smpsotc_t`

SMPS overtemperature configuration options (0x19:SMPSOTC[3])

false - Vvsmps output not modified during overtemperature warning (OTWI interrupt)

true - Vvsmps output reduced to 5V when chip temperature is above the overtemperature warning threshold, T_{th(warn)otp}

Implements : `uja113x_smpsc_smpsotc_t_Class`

Definition at line 468 of file `sbc_uja113x.h`.

17.11.5 Enumeration Type Documentation

17.11.5.1 `enum uja113x_smpsc_smpsc_t`

SMPS on/off configuration options (0x19:SMPSOC[1:0])

Implements : `uja113x_smpsc_smpsc_t_Class`

Enumerator

SMPSOC_ON_NSR SMPS is on in Normal, Standby and Reset modes and shut-down in all other modes

SMPSOC_ON_NSRS SMPS is on in Normal, Standby, Reset and Sleep modes nad shut-down in all other modes

SMPSOC_PASS_THROUGH_NSS Pass-through mode is requested in Normal, Standby and Sleep modes

Definition at line 477 of file `sbc_uja113x.h`.

17.11.5.2 `enum uja113x_smpsovc_smpsoc_t`

SMPS output voltage configuration options (0x1A:SMPSOC[3:0])

Implements : `uja113x_smpsovc_smpsoc_t_Class`

Enumerator

SMPSOC_50V SMPS output voltage 5.0 V

SMPSOC_52V SMPS output voltage 5.2 V

SMPSOC_54V SMPS output voltage 5.4 V

SMPSOC_56V SMPS output voltage 5.6 V
SMPSOC_58V SMPS output voltage 5.8 V
SMPSOC_60V SMPS output voltage 6.0 V
SMPSOC_62V SMPS output voltage 6.2 V
SMPSOC_64V SMPS output voltage 6.4 V
SMPSOC_66V SMPS output voltage 6.6 V
SMPSOC_68V SMPS output voltage 6.8 V
SMPSOC_70V SMPS output voltage 7.0 V
SMPSOC_72V SMPS output voltage 7.2 V
SMPSOC_74V SMPS output voltage 7.4 V
SMPSOC_76V SMPS output voltage 7.6 V
SMPSOC_78V SMPS output voltage 7.8 V
SMPSOC_80V SMPS output voltage 8.0 V

Definition at line 494 of file sbc_uja113x.h.

17.11.6 Function Documentation

17.11.6.1 `status_t UJA113X_SetSmps (uint32_t instance, const uja113x_smpsc_cfg_t * smpscConfig)`

Sets the SMPS control registers (0x19 - 0x1A) based on input configuration object.

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the SMPS control registers were not written properly and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>smpscConfig</i>	SMPS control configuration object

Returns

STATUS_SUCCESS Configuration successful
 STATUS_BUSY SPI peripheral is busy
 STATUS_TIMEOUT SPI communication timed out, configuration aborted
 SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Note

The function configures all the SMPS features:

1. SMPS overtemperature control (0x19)
2. SMPS on/off control (0x19)
3. SMPS output voltage (0x1A)

Definition at line 589 of file sbc_uja113x.c.

17.12 03. Transceiver control

17.12.1 Detailed Description

The transceiver control registers (0x20 - 0x2F) allow:

- Configuring CAN (0x20)
- Configuring LIN1/2 (0x21)
- Read transceiver status (0x22)
- Enable transceiver interrupts (0x23)
- Configuring CAN partial networking
 - Data rate (0x26)
 - ID (0x27 - 0x2A)
 - ID mask (0x2B - 0x2E)
 - Frame control (0x2F)
 - Data masks (0x68 - 0x6F) (part of interrupt and status registers 0x60 - 0x6F)

Interrupts and interrupt status is described in [06. Interrupts](#).

Modules

- [01. CAN & CAN partial networking configuration](#)
- [02. LIN configuration](#)

17.13 04. HVIO bank 0 & 1 control

17.13.1 Detailed Description

17.13.2 Introduction

The HVIO control registers (0x30 - 0x3A / 0x40 - 0x4A) allow:

- Configuring the HVIO pin behaviour (0x30 - 0x33 / 0x40 - 0x43)
- Configuring the Bank N wake-up threshold (0x34 - 0x44)
- Read Bank N wake-up status (0x35 / 0x45)
- Read Bank N driver status (0x36 / 0x46)
- Configuring Bank N short-circuit detection threshold (0x39 / 0x49)
- Configuring Bank N open-load detection threshold (0x3A / 0x4A)
- Enabling/disabling HVIO N high-/low-side driver in non-volatile memory (0x71 / 0x72) (see [HVIO high-side configuration options \(0x71\)](#) & [HVIO low-side configuration options \(0x72\)](#) for details)

Note

Please, consult the details of HVIO capabilities with the reference manual, as this is out of the scope of this documentation.

17.13.2.1 Short-circuit handling

Every HVIO pin can be configured separately in it's dedicated HVIO control register (0x30 - 0x33 / 0x40 - 0x43) by setting the IOnCC (HVIO configuration control) bit and IOnAC (HVIO activation control). The HVIO can be disabled by either setting the IOnAC bit to deactivated (see [uja113x_hvion_ionac_t](#)) or by IOnCC to HVIO off state (see [uja113x_hvion_ioncc_t](#)).

However, during short circuit, to reset the function of the HVIO pin, the IOnAC bit has to be set to deactivated and afterwards a corresponding active mode set again. Resetting the HVIO pin by IOnCC will have no effect!

17.13.2.1.1 Example

```
/* Configuring the HVIO pin */
uja113x_hvio_cfg_t hvio1Config;
hvio1Config.ionShutdownCtrl = IONSC_OVERVOLTAGE;
hvio1Config.ionActivateCtrl = IONAC_ENABLED;
hvio1Config.ionConfCtrl = IONCC_HS_SLOPE;
UJA113X_SetHvio(SBC_INSTANCE_0, &hvio1Config, HVIO1);

/* Short-circuit detected on HVIO 1 */
hvio1Config.ionActivateCtrl = IONAC_DEACTIVATED;
UJA113X_SetHvio(SBC_INSTANCE_0, &hvio1Config, HVIO1);

/* delay/manage short-circuit etc. if necessary */
...
/* Activate HVIO again */
hvio1Config.ionActivateCtrl = IONAC_ENABLED;
UJA113X_SetHvio(SBC_INSTANCE_0, &hvio1Config, HVIO1);
```

Data Structures

- struct [uja113x_hvio_cfg_t](#)
HVIO pin control register configuration structure (0x3N; 0x4N; N = 0 - 3) [More...](#)
- struct [uja113x_bscdt_cfg_t](#)
Bank 0/1 short-circuit detection threshold configuration structure (0x39/0x49) [More...](#)
- struct [uja113x_bolddt_cfg_t](#)
Bank 0/1 open-load detection threshold configuration structure (0x3A/0x4A) [More...](#)

Typedefs

- typedef bool [uja113x_bwtc_bnwtc_t](#)
Bank N wake-up threshold configuration options (0x34 / 0x44)

Enumerations

- enum [uja113x_hvion_ionsc_t](#) { [IONSC_NONE](#) = 0x00U, [IONSC_UNDRVOLTAGE](#) = 0x40U, [IONSC_OVRVOLTAGE](#) = 0x80U, [IONSC_FULL](#) = 0xC0U }
HVION shut-down configuration options (0x3N:IONSC[7:6], N = 0, 1, 2, 3)
- enum [uja113x_hvion_ionac_t](#) { [IONAC_DEACTIVATED](#) = 0x00U, [IONAC_ENABLED](#) = 0x08U, [IONAC_TMR_1](#) = 0x10U, [IONAC_TMR_2](#) = 0x18U, [IONAC_TMR_3](#) = 0x20U, [IONAC_TMR_4](#) = 0x28U, [IONAC_HVIO_INV](#) = 0x30U, [IONAC_HVIO](#) = 0x38U }
HVION activation configuration options (0x3N:IONAC[5:3]; N = 0, 1, 2, 3)
- enum [uja113x_hvion_ioncc_t](#) { [IONCC_OFF](#) = 0x00U, [IONCC_HS_SLOPE](#) = 0x01U, [IONCC_LS_SLOPE](#) = 0x02U, [IONCC_WUP](#) = 0x03U, [IONCC_HS_WUP_SLOPE](#) = 0x04U, [IONCC_HS](#) = 0x05U, [IONCC_LS](#) = 0x06U, [IONCC_HS_WUP](#) = 0x07U }
HVION output configuration options (0x3N:IONCC[2:0]; N = 0, 1, 2, 3)

Functions

- status_t [UJA113X_SetHvio](#) (uint32_t instance, const [uja113x_hvio_cfg_t](#) *hvioConfig, uint8_t hviold)
Configures corresponding HVIO control register based on hviold (0x3N/0x4N; N = 0 - 3)
- status_t [UJA113X_SetBankWupThr](#) (uint32_t instance, [uja113x_bwtc_bnwtc_t](#) bankWupThrConfig, uint8_t bankId)
Configures corresponding bank wake-up control register based on bankId (0x34/0x44)
- status_t [UJA113X_SetBankShortCircThr](#) (uint32_t instance, const [uja113x_bscdt_cfg_t](#) *bscdtConfig, uint8_t bankId)
Configures all HVIO's short-circuit detection threshold level based on bankId (0x39/0x49)
- status_t [UJA113X_SetBankOpenLoadThr](#) (uint32_t instance, const [uja113x_boldt_cfg_t](#) *boldtConfig, uint8_t bankId)
Configures all HVIO's open-load detection threshold level based on bankId (0x3A/0x4A)

17.13.3 Data Structure Documentation

17.13.3.1 struct [uja113x_hvio_cfg_t](#)

HVION control register configuration structure (0x3N; 0x4N; N = 0 - 3)

Implements : [uja113x_hvio_cfg_t_Class](#)

Definition at line 1646 of file [sbc_uja113x.h](#).

Data Fields

- [uja113x_hvion_ionsc_t](#) [ionShutdownCtrl](#)
Configures HVION shut-down behavior (0x3N/0x4N:IONSC[7:6])
- [uja113x_hvion_ionac_t](#) [ionActivateCtrl](#)
Configures HVION activation behavior (0x3N/0x4N:IONAC[5:3])
- [uja113x_hvion_ioncc_t](#) [ionConfCtrl](#)
Configures HVION output behavior (0x3N/0x4N:IONCC[2:0])

Field Documentation

17.13.3.1.1 `uja113x_hvion_ionac_t ionActivateCtrl`

Configures HVIO activation behavior (0x3N/0x4N:[IOAC[5:3]])

Definition at line 1655 of file `sbc_uja113x.h`.

17.13.3.1.2 `uja113x_hvion_ioncc_t ionConfCtrl`

Configures HVIO output behavior (0x3N/0x4N:[IONCC[2:0]])

Definition at line 1659 of file `sbc_uja113x.h`.

17.13.3.1.3 `uja113x_hvion_ionsc_t ionShutdownCtrl`

Configures HVIO shut-down behavior (0x3N/0x4N:[IONSC[7:6]])

Definition at line 1651 of file `sbc_uja113x.h`.

17.13.3.2 `struct uja113x_bscdt_cfg_t`

Bank 0/1 short-circuit detection threshold configuration structure (0x39/0x49)

Implements : `uja113x_bscdt_cfg_t_Class`

Definition at line 1669 of file `sbc_uja113x.h`.

Data Fields

- [uja113x_bscdt_ionsctc_t io48ShortCircuitThrCtrl](#)
Configures HVIO4(8) short-circuit detection threshold (0x39/0x49:IO4(8)SCTC[7:6])
- [uja113x_bscdt_ionsctc_t io37ShortCircuitThrCtrl](#)
Configures HVIO3(7) short-circuit detection threshold (0x39/0x49:IO3(7)SCTC[5:4])
- [uja113x_bscdt_ionsctc_t io26ShortCircuitThrCtrl](#)
Configures HVIO2(6) short-circuit detection threshold (0x39/0x49:IO2(6)SCTC[3:2])
- [uja113x_bscdt_ionsctc_t io15ShortCircuitThrCtrl](#)
Configures HVIO1(5) short-circuit detection threshold (0x39/0x49:IO1(5)SCTC[1:0])

Field Documentation

17.13.3.2.1 `uja113x_bscdt_ionsctc_t io15ShortCircuitThrCtrl`

Configures HVIO1(5) short-circuit detection threshold (0x39/0x49:IO1(5)SCTC[1:0])

Definition at line 1686 of file `sbc_uja113x.h`.

17.13.3.2.2 `uja113x_bscdt_ionsctc_t io26ShortCircuitThrCtrl`

Configures HVIO2(6) short-circuit detection threshold (0x39/0x49:IO2(6)SCTC[3:2])

Definition at line 1682 of file `sbc_uja113x.h`.

17.13.3.2.3 `uja113x_bscdt_ionsctc_t io37ShortCircuitThrCtrl`

Configures HVIO3(7) short-circuit detection threshold (0x39/0x49:IO3(7)SCTC[5:4])

Definition at line 1678 of file `sbc_uja113x.h`.

17.13.3.2.4 `uja113x_bscdt_ionsctc_t io48ShortCircuitThrCtrl`

Configures HVIO4(8) short-circuit detection threshold (0x39/0x49:IO4(8)SCTC[7:6])

Definition at line 1674 of file `sbc_uja113x.h`.

17.13.3.3 struct uja113x_boldt_cfg_t

Bank 0/1 open-load detection threshold configuration structure (0x3A/0x4A)

Implements : uja113x_boldt_cfg_t_Class

Definition at line 1696 of file sbc_uja113x.h.

Data Fields

- [uja113x_boldt_ionoltc_t io48OpenLoadThrCtrl](#)
Configures HVIO4(8) open-load detection threshold (0x3A/4A:IO4(8)OLTC[7:6])
- [uja113x_boldt_ionoltc_t io37OpenLoadThrCtrl](#)
Configures HVIO4(8) open-load detection threshold (0x3A/4A:IO3(7)OLTC[5:4])
- [uja113x_boldt_ionoltc_t io26OpenLoadThrCtrl](#)
Configures HVIO4(8) open-load detection threshold (0x3A/4A:IO2(6)OLTC[3:2])
- [uja113x_boldt_ionoltc_t io15OpenLoadThrCtrl](#)
Configures HVIO4(8) open-load detection threshold (0x3A/4A:IO1(5)OLTC[1:0])

Field Documentation

17.13.3.3.1 uja113x_boldt_ionoltc_t io15OpenLoadThrCtrl

Configures HVIO4(8) open-load detection threshold (0x3A/4A:IO1(5)OLTC[1:0])

Definition at line 1713 of file sbc_uja113x.h.

17.13.3.3.2 uja113x_boldt_ionoltc_t io26OpenLoadThrCtrl

Configures HVIO4(8) open-load detection threshold (0x3A/4A:IO2(6)OLTC[3:2])

Definition at line 1709 of file sbc_uja113x.h.

17.13.3.3.3 uja113x_boldt_ionoltc_t io37OpenLoadThrCtrl

Configures HVIO4(8) open-load detection threshold (0x3A/4A:IO3(7)OLTC[5:4])

Definition at line 1705 of file sbc_uja113x.h.

17.13.3.3.4 uja113x_boldt_ionoltc_t io48OpenLoadThrCtrl

Configures HVIO4(8) open-load detection threshold (0x3A/4A:IO4(8)OLTC[7:6])

Definition at line 1701 of file sbc_uja113x.h.

17.13.4 Typedef Documentation

17.13.4.1 typedef bool uja113x_bwtc_bnwtc_t

Bank N wake-up threshold configuration options (0x34 / 0x44)

false - threshold is ratiometric to Vbaths1

true - threshold is absolute

Implements : uja113x_bwtc_bnwtc_t_Class

Definition at line 894 of file sbc_uja113x.h.

17.13.5 Enumeration Type Documentation

17.13.5.1 enum uja113x_hvion_ionac_t

HVION activation configuration options (0x3N:IONAC[5:3]; N = 0, 1, 2, 3)

Implements : `uja113x_hvion_ionac_t_Class`

Enumerator

IONAC_DEACTIVATED HVION is deactivated.
IONAC_ENABLED HVION is enabled.
IONAC_TMR_1 HVION is controlled by timer 1.
IONAC_TMR_2 HVION is controlled by timer 2.
IONAC_TMR_3 HVION is controlled by timer 3.
IONAC_TMR_4 HVION is controlled by timer 4.
IONAC_HVIO_INV HVION is controlled by HVION + 4 (inverted control; only available for bank 0)
IONAC_HVIO HVION is controlled by HVION + 4 (non-inverted control; only available for bank 0)

Definition at line 854 of file `sbc_uja113x.h`.

17.13.5.2 enum `uja113x_hvion_ioncc_t`

HVION output configuration options (0x3N:IONCC[2:0]; N = 0, 1, 2, 3)

Implements : `uja113x_hvion_ioncc_t_Class`

Enumerator

IONCC_OFF HVION is off.
IONCC_HS_SLOPE Configure HVION as high-side driver with slope control.
IONCC_LS_SLOPE Configure HVION as low-side driver with slope control.
IONCC_WUP Configure HVION as wake-up input.
IONCC_HS_WUP_SLOPE Configure HVION as high-side driver and wake-up input with slope control.
IONCC_HS Configure HVION as high-side driver without slope control.
IONCC_LS Configure HVION as low-side driver without slope control.
IONCC_HS_WUP Configure HVION as high-side driver and wake-up input without slope control.

Definition at line 873 of file `sbc_uja113x.h`.

17.13.5.3 enum `uja113x_hvion_ionsc_t`

HVION shut-down configuration options (0x3N:IONSC[7:6], N = 0, 1, 2, 3)

Implements : `uja113x_hvion_ionsc_t_Class`

Enumerator

IONSC_NONE HVION doesn't respond to over- or undervoltage.
IONSC_UNDRVOLTAGE HVION shuts down when battery undervoltage is detected in normal mode.
IONSC_OVERVOLTAGE HVION shuts down when battery overvoltage is detected in normal mode.
IONSC_FULL HVION shuts down when battery over- or undervoltage is detected in normal mode.

Definition at line 839 of file `sbc_uja113x.h`.

17.13.6 Function Documentation

17.13.6.1 `status_t UJA113X_SetBankOpenLoadThr (uint32_t instance, const uja113x_boldt_cfg_t * boldtConfig, uint8_t bankId)`

Configures all HVIO's open-load detection threshold level based on bankId (0x3A/0x4A)

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the open-load detection threshold control register identified by bankId has not been written properly and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>bscdtConfig</i>	Open-load threshold level configuration object
in	<i>bankId</i>	Bank identifier (0 - 1)

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Note

The hviold parameter determines, which HVIO shall be configured.

Definition at line 1028 of file sbc_uja113x.c.

17.13.6.2 `status_t UJA113X_SetBankShortCircThr (uint32_t instance, const uja113x_bscdt_cfg_t * bscdtConfig, uint8_t bankId)`

Configures all HVIO's short-circuit detection threshold level based on bankId (0x39/0x49)

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the short-circuit detection threshold control register identified by bankId has not been written properly and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>bscdtConfig</i>	Short-circuit threshold level configuration object
in	<i>bankId</i>	Bank identifier (0 - 1)

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Note

The bankId parameter determines, which bank shall be configured.

Definition at line 996 of file sbc_uja113x.c.

17.13.6.3 `status_t UJA113X_SetBankWupThr (uint32_t instance, uja113x_bwtc_bnwtc_t bankWupThrConfig, uint8_t bankId)`

Configures corresponding bank wake-up control register based on bankId (0x34/0x44)

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the bank N wake-up control register identified by bankId has not been written properly and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>bankWupThr↔ Config</i>	Bank N wake-up threshold configuration parameter
in	<i>bankId</i>	Bank identifier (0 - 1)

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Warning

This function only checks the maximum number of HVIO banks, as write to "non-existing" registers are allowed. Thus for devices without HVIO this function will perform an "empty" write.

Definition at line 914 of file sbc_uja113x.c.

17.13.6.4 `status_t UJA113X_SetHvio (uint32_t instance, const uja113x_hvio_cfg_t * hvioConfig, uint8_t hviold)`

Configures corresponding HVIO control register based on hviold (0x3N/0x4N; N = 0 - 3)

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the HVIO control register identified by hviold has not been written properly and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>hvioConfig</i>	HVIO configuration object
in	<i>hviold</i>	HVIO identifier (0 = HVIO1 - 7 = HVIO8)

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Note

The hviold parameter determines, which HVIO shall be configured.

Definition at line 877 of file sbc_uja113x.c.

17.14 04. Lock control

17.14.1 Detailed Description

17.14.2 Introduction

The Lock control allows the user to write protect specific memory areas. This way the SBC is protected against unintentional writes into the SBC registers providing additional level of safety/security.

An SPI failure interrupt is generated, if enabled (see [06. Interrupts](#)). Otherwise writes into locked areas are ignored.

- Lock 0: address area 0x06 - 0x09; general purpose memory
- Lock 1: address area 0x10 - 0x1F; supply control
- Lock 2: address area 0x20 - 0x2F; transceiver control
- Lock 3: address area 0x30 - 0x3F; HVIO1 - HVIO4 control
- Lock 4: address area 0x40 - 0x4F; HVIO5 - HVIO8 control
- Lock 5: address area 0x50 - 0x5F; timer control
- Lock 6: address area 0x68 - 0x6F; data mask (FD versions only)

Data Structures

- struct [uja113x_lckc_cfg_t](#)
Lock Control register configuration structure (reg 0x0A) [More...](#)

Typedefs

- typedef bool [uja113x_lckc_lkxc_t](#)
Lock Control configuration options (0x0A)

Functions

- status_t [UJA113X_SetLock](#) (uint32_t instance, const [uja113x_lckc_cfg_t](#) *lckcConfig)
Sets the lock control register (0x0A) based on input configuration object.

17.14.3 Data Structure Documentation

17.14.3.1 struct uja113x_lckc_cfg_t

Lock Control register configuration structure (reg 0x0A)

The structure defines, which address areas should be SPI write (un)protected.

See also

[UJA113X_SetLock\(\)](#)

Implements : [uja113x_lckc_cfg_t_Class](#)

Definition at line 1426 of file [sbc_uja113x.h](#).

Data Fields

- [uja113x_lckc_lkxc_t lock6](#)
Disables/enables SPI write access to address area 0x68 - 0x6F (FD version only) (0x0A:LK6C[6]).
- [uja113x_lckc_lkxc_t lock5](#)
Disables/enables SPI write access to address area 0x50 - 0x55 (0x0A:LK5C[5]).
- [uja113x_lckc_lkxc_t lock4](#)
Disables/enables SPI write access to address area 0x40 - 0x4F (0x0A:LK4C[4]).
- [uja113x_lckc_lkxc_t lock3](#)
Disables/enables SPI write access to address area 0x30 - 0x3F (0x0A:LK3C[3]).
- [uja113x_lckc_lkxc_t lock2](#)
Disables/enables SPI write access to address area 0x20 - 0x2F (0x0A:LK2C[2]).
- [uja113x_lckc_lkxc_t lock1](#)
Disables/enables SPI write access to address area 0x10 - 0x1F (0x0A:LK1C[1]).
- [uja113x_lckc_lkxc_t lock0](#)
Disables/enables SPI write access to address area 0x06 - 0x09 (0x0A:LK0C[0]).

Field Documentation

17.14.3.1.1 [uja113x_lckc_lkxc_t lock0](#)

Disables/enables SPI write access to address area 0x06 - 0x09 (0x0A:LK0C[0]).

Definition at line 1440 of file sbc_uja113x.h.

17.14.3.1.2 [uja113x_lckc_lkxc_t lock1](#)

Disables/enables SPI write access to address area 0x10 - 0x1F (0x0A:LK1C[1]).

Definition at line 1438 of file sbc_uja113x.h.

17.14.3.1.3 [uja113x_lckc_lkxc_t lock2](#)

Disables/enables SPI write access to address area 0x20 - 0x2F (0x0A:LK2C[2]).

Definition at line 1436 of file sbc_uja113x.h.

17.14.3.1.4 [uja113x_lckc_lkxc_t lock3](#)

Disables/enables SPI write access to address area 0x30 - 0x3F (0x0A:LK3C[3]).

Definition at line 1434 of file sbc_uja113x.h.

17.14.3.1.5 [uja113x_lckc_lkxc_t lock4](#)

Disables/enables SPI write access to address area 0x40 - 0x4F (0x0A:LK4C[4]).

Definition at line 1432 of file sbc_uja113x.h.

17.14.3.1.6 [uja113x_lckc_lkxc_t lock5](#)

Disables/enables SPI write access to address area 0x50 - 0x55 (0x0A:LK5C[5]).

Definition at line 1430 of file sbc_uja113x.h.

17.14.3.1.7 [uja113x_lckc_lkxc_t lock6](#)

Disables/enables SPI write access to address area 0x68 - 0x6F (FD version only) (0x0A:LK6C[6]).

Definition at line 1428 of file sbc_uja113x.h.

17.14.4 Typedef Documentation

17.14.4.1 typedef bool `uja113x_lckc_lkxc_t`

Lock Control configuration options (0x0A)

false - do not lock memory; SPI write access enabled

true - lock memory; SPI write access disabled

Implements : `uja113x_lckc_lkxc_t_Class`

Definition at line 364 of file `sbc_uja113x.h`.

17.14.5 Function Documentation

17.14.5.1 `status_t UJA113X_SetLock (uint32_t instance, const uja113x_lckc_cfg_t * lckcConfig)`

Sets the lock control register (0x0A) based on input configuration object.

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the lock control register has not been written and the process has to be repeated.

Parameters

<i>in</i>	<i>instance</i>	Index of SBC to configure
<i>in</i>	<i>lckcConfig</i>	Lock control configuration object

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Note

This function sets a lock on certain memory areas to prevent unintended register modifications over SPI, thus the function should be called after the whole SBC has been initialized!

Write accesses to locked memory areas can lead to SPI failure interrupt, if enabled.

The lock register is never locked, thus future (un)locking is possible.

Definition at line 488 of file `sbc_uja113x.c`.

17.15 05. Timer control

17.15.1 Detailed Description

17.15.2 Introduction

Devices incorporating HVIOs functionality contain 4 timers. Up to four configuration options are available (see [uja113x_timxc_txmc_t](#)). Configuring a single timer can be achieved by invoking [UJA113X_SetTimer\(\)](#). To change just the duty cycle, the [UJA113X_SbcTransfer\(\)](#) can be used. For more details, consult the reference manual.

Data Structures

- struct [uja113x_timsc_cfg_t](#)

Single timer control registers configuration structure (0x5x - 0x5x + 1) [More...](#)

Typedefs

- typedef uint8_t [uja113x_timxdcc_txdcc_t](#)

Timer X duty cycle configuration options (0x5N:TDCC[7:0]); (N = 1, 3, 5, 7)

Enumerations

- enum [uja113x_timxc_txpc_t](#) {
[TXPC_4MS_PERIOD](#) = 0x00U, [TXPC_8MS_PERIOD](#) = 0x04U, [TXPC_20MS_PERIOD](#) = 0x08U, [TXPC_30MS_PERIOD](#) = 0x0CU,
[TXPC_50MS_PERIOD](#) = 0x10U, [TXPC_100MS_PERIOD](#) = 0x14U, [TXPC_200MS_PERIOD](#) = 0x18U, [TXPC_400MS_PERIOD](#) = 0x1CU,
[TXPC_800MS_PERIOD](#) = 0x20U, [TXPC_1000MS_PERIOD](#) = 0x24U, [TXPC_2000MS_PERIOD](#) = 0x28U,
[TXPC_4000MS_PERIOD](#) = 0x2CU }

Timer X period configuration options (0x5N:TXPC[5:2]); (N = 0, 2, 4, 6)

- enum [uja113x_timxc_txmc_t](#) { [TXMC_PWM](#) = 0x00U, [TXMC_TIM](#) = 0x01U, [TXMC_TRIG_START](#) = 0x02U, [TXMC_TRIG_END](#) = 0x03U }

Timer X mode control configuration options (0x5N:TXMC[0]); (N = 0, 2, 4, 6)

Functions

- status_t [UJA113X_SetTimer](#) (uint32_t instance, const [uja113x_timsc_cfg_t](#) *timscConfig)

Sets a single timer configuration registers (0x5N - 0x5M) based on input configuration object (N = 0, 2, 4, 6; M = 1, 3, 5, 7)

17.15.3 Data Structure Documentation

17.15.3.1 struct uja113x_timsc_cfg_t

Single timer control registers configuration structure (0x5x - 0x5x + 1)

Implements : [uja113x_timsc_cfg_t_Class](#)

Definition at line 1724 of file [sbc_uja113x.h](#).

Data Fields

- [uint8_t nTimer](#)
Timer to configure (0 - 3)
- [uja113x_timxc_tnpc_t timXPeriodCtrl](#)
Configures Timer X period (reg 0x5N:TXPC[5:2]; N = 0, 2, 4, 6)
- [uja113x_timxc_txmc_t timXModeCtrl](#)
Configures Timer X mode (reg 0x5N:TXMC[1:0]); N = 0, 2, 4, 6)
- [uja113x_timxdcc_txdcc_t timXDutyCycleCtrl](#)
Configures Timer X duty cycle (reg 0x5N:TXDCC[7:0]; N = 1, 3, 5, 7)

Field Documentation

17.15.3.1.1 [uint8_t nTimer](#)

Timer to configure (0 - 3)

Definition at line 1729 of file sbc_uja113x.h.

17.15.3.1.2 [uja113x_timxdcc_txdcc_t timXDutyCycleCtrl](#)

Configures Timer X duty cycle (reg 0x5N:TXDCC[7:0]; N = 1, 3, 5, 7)

duty cycle = TXDCC / 255 x 100 [%]

Definition at line 1742 of file sbc_uja113x.h.

17.15.3.1.3 [uja113x_timxc_txmc_t timXModeCtrl](#)

Configures Timer X mode (reg 0x5N:TXMC[1:0]); N = 0, 2, 4, 6)

Definition at line 1737 of file sbc_uja113x.h.

17.15.3.1.4 [uja113x_timxc_tnpc_t timXPeriodCtrl](#)

Configures Timer X period (reg 0x5N:TXPC[5:2]; N = 0, 2, 4, 6)

Definition at line 1733 of file sbc_uja113x.h.

17.15.4 Typedef Documentation

17.15.4.1 [typedef uint8_t uja113x_timxdcc_txdcc_t](#)

Timer X duty cycle configuration options (0x5N:TXDCC[7:0]); (N = 1, 3, 5, 7)

Implements : [uja113x_timxdcc_txdcc_t_Class0](#) - 255;

duty cycle = TXDCC \ 255

Definition at line 1120 of file sbc_uja113x.h.

17.15.5 Enumeration Type Documentation

17.15.5.1 [enum uja113x_timxc_txmc_t](#)

Timer X mode control configuration options (0x5N:TXMC[0]); (N = 0, 2, 4, 6)

Warning

Last two options (TXMC_TRIG_START and TXMC_TRIG_END) are not valid for Timer 1!

Implements : [uja113x_timxc_txmc_t_Class](#)

Enumerator

TXMC_PWM Timer N is in PWM mode; **on-time** = $\text{TXDCC} \times \text{TXPC} / 255$.

TXMC_TIM Timer N is in Timer mode; **on-time** = $\text{TXDCC} \times \text{tw}(\text{base})\text{tmr us}$.

TXMC_TRIG_START Timer N pulse is triggered at the start of Timer 1 pulse (master-slave mode); **on-time** = $\text{TXDCC} \times \text{tw}(\text{base})\text{tmr us}$.

TXMC_TRIG_END Timer N pulse is triggered at the end of Timer 1 pulse (master-slave mode); **on-time** = $\text{TXDCC} \times \text{tw}(\text{base})\text{tmr us}$.

Definition at line 1105 of file sbc_uja113x.h.

17.15.5.2 enum uja113x_timxc_txpc_t

Timer X period configuration options (0x5N:TXPC[5:2]); (N = 0, 2, 4, 6)

Implements : uja113x_timxc_txpc_t_Class

Enumerator

TXPC_4MS_PERIOD Timer period 4 ms

TXPC_8MS_PERIOD Timer period 8 ms

TXPC_20MS_PERIOD Timer period 20 ms

TXPC_30MS_PERIOD Timer period 30 ms

TXPC_50MS_PERIOD Timer period 50 ms

TXPC_100MS_PERIOD Timer period 100 ms

TXPC_200MS_PERIOD Timer period 200 ms

TXPC_400MS_PERIOD Timer period 400 ms

TXPC_800MS_PERIOD Timer period 800 ms

TXPC_1000MS_PERIOD Timer period 1 s

TXPC_2000MS_PERIOD Timer period 2 s

TXPC_4000MS_PERIOD Timer period 4 s

Definition at line 1080 of file sbc_uja113x.h.

17.15.6 Function Documentation

17.15.6.1 status_t UJA113X_SetTimer (uint32_t instance, const uja113x_timsc_cfg_t * timscConfig)

Sets a single timer configuration registers (0x5N - 0x5M) based on input configuration object (N = 0, 2, 4, 6; M = 1, 3, 5, 7)

The function prepares a frame based on input configuration object and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the timer configuration registers have not been written properly and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>timscConfig</i>	Single timer configuration object

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Return values

<i>SBC_ERR_NA</i>	Timer with provided index is not present on this device.
-------------------	--

Note

This function configures a single timer. In case the user is interested in configuring the period or duty cycle only, [UJA113X_SbcTransfer\(\)](#) be used instead!

Warning

For Timer 1 the `timXPeriodCtrl` parameter is masked by 0x01! See [uja113x_timxc_txmc_t](#) for details!
This function only checks the maximum number of timer channels, as write to "non-existing" registers are allowed. Thus for devices without timers this function will perform an "empty" write.

See also

`UJA113X_WriteRegister()`

Definition at line 1059 of file `sbc_uja113x.c`.

17.16 06. Interrupts

17.16.1 Detailed Description

17.16.2 Introduction

The library provides one function for each interrupt group ([UJA113X_SetSystemInterrupts\(\)](#), [UJA113X_SetSupplyInterrupts\(\)](#) etc.) to enable/disable required interrupts. On the other hand, handling the interrupt's is not supported and it's the users responsibility to provide his own logic.

17.16.2.1 Handling pending interrupts

After an event related to enabled interrupt occurs, the corresponding pin INTN1/INTN2 is set low. This can be detected by the MCU and a pending interrupt can be processed.

The SBC provides a global interrupt status register (see [Register address map](#)). This should be read first, to identify the interrupt group source. Afterwards a dedicated interrupt status register should be read to identify the interrupt source. The [UJA113X_SbcTransfer\(\)](#) function can be used.

Modules

- [Bank N fail interrupt enable configuration options \(0x38/0x48\)](#)
- [Bank N wake-up interrupt enable configuration options \(0x37/0x47\)](#)
- [Supply interrupt enable configuration options \(0x1C\)](#)
- [System interrupt enable configuration options \(0x04\)](#)
- [Transceiver interrupt enable configuration options \(0x23\)](#)

Functions

- `status_t UJA113X_SetSystemInterrupts (uint32_t instance, uint8_t sysieMask)`
Sets the system interrupt enable register (0x04) based on input configuration paramater.
- `status_t UJA113X_SetSupplyInterrupts (uint32_t instance, uint8_t supieMask)`
Sets the supply interrupt enable register (0x1C) based on input parameter.
- `status_t UJA113X_SetTransceiverInterrupts (uint32_t instance, uint8_t tieMask)`
Sets the transceiver interrupt enable register (0x23) based on input configuration parameter.
- `status_t UJA113X_SetBankWupInterrupts (uint32_t instance, uint8_t bankWupIntMask, uint8_t bankId)`
Configures corresponding bank wake-up interrupt enable register based on bankId (0x37 / 0x47)
- `status_t UJA113X_SetBankFailInterrupts (uint32_t instance, uint8_t bankFailIntMask, uint8_t bankId)`
Configures corresponding bank fail interrupt enable register based on bankId (0x38 / 0x48)

17.16.3 Function Documentation

17.16.3.1 `status_t UJA113X_SetBankFailInterrupts (uint32_t instance, uint8_t bankFailIntMask, uint8_t bankId)`

Configures corresponding bank fail interrupt enable register based on bankId (0x38 / 0x48)

The function prepares a frame based on input configuration parameter and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the bank N fail interrupt enable register identified by bankId has not been written properly and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>bankFailIntMask</i>	Mask defining interrupts to be enabled
in	<i>bankId</i>	Bank identifier (0 - 1)

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

See also

[Bank N fail interrupt enable configuration options \(0x38/0x48\)](#)

Definition at line 969 of file sbc_uja113x.c.

17.16.3.2 `status_t UJA113X_SetBankWupInterrupts (uint32_t instance, uint8_t bankWupIntMask, uint8_t bankId)`

Configures corresponding bank wake-up interrupt enable register based on bankId (0x37 / 0x47)

The function prepares a frame based on input configuration parameter and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the bank N wake-up interrupt enable register identified by bankId has not been written properly and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>bankWupIntMask</i>	Mask defining interrupts to be enabled
in	<i>bankId</i>	Bank identifier (0 - 1)

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

Warning

This function only checks the maximum number of HVIO banks, as write to "non-existing" registers are allowed. Thus for devices without HVIO this function will perform an "empty" write.

See also

[Bank N wake-up interrupt enable configuration options \(0x37/0x47\)](#)

Definition at line 942 of file sbc_uja113x.c.

17.16.3.3 `status_t UJA113X_SetSupplyInterrupts (uint32_t instance, uint8_t supieMask)`

Sets the supply interrupt enable register (0x1C) based on input parameter.

The function prepares a frame based on input configuration parameter and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the supply interrupt register has not been written properly and the process has to be repeated.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>supieMask</i>	Defines which supply interrupts to enable

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

See also

[Supply interrupt enable configuration options \(0x1C\)](#)

Definition at line 617 of file sbc_uja113x.c.

17.16.3.4 status_t UJA113X_SetSystemInterrupts (uint32_t *instance*, uint8_t *sysieMask*)

Sets the system interrupt enable register (0x04) based on input configuration paramater.

The function prepares a frame based on input configuration parameter and initiates SPI communcation in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the system interrupt enable register has not been written and the process has to be repeated.

Bits 7 - 3 & 0 are cleared (reserved bits).

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>sysieMask</i>	Defines which system interrupts to enable

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

See also

[System interrupt enable configuration options \(0x04\)](#)

Definition at line 464 of file sbc_uja113x.c.

17.16.3.5 status_t UJA113X_SetTransceiverInterrupts (uint32_t *instance*, uint8_t *tieMask*)

Sets the transceiver interrupt enable register (0x23) based on input configuration parameter.

The function prepares a frame based on input configuration parameter and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the transceiver interrupt enable register has not been written properly and the process has to be repeated.

Bits 7 - 5 are cleared (reserved bits).

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>tieMask</i>	Defines which transceiver interrupts to enable

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI peripheral is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address, configuration failed.

See also

[Transceiver interrupt enable configuration options \(0x23\)](#)

Definition at line 722 of file sbc_uja113x.c.

17.17 07. MTPNV and ID

17.17.1 Detailed Description

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\middleware\sbc\sbc_uja113x\source\sbc_uja113x.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\middleware\sbc\sbc_uja113x\include
```

Compile symbols

No special symbols are required for this component

Dependencies

[Low Power Serial Peripheral Interface \(LPSPi\) OS Interface \(OSiF\)](#)

17.17.2 Introduction

The UJA113x devices incorporate non-volatile memory for SBC configuration. This memory is not reset during off state and influences the chip behavior:

- Register 0x71
 - HVIOs high-side driver control
- Register 0x72
 - HVIOs low-side driver control
- Register 0x73
 - Reset pulse width
 - V2 regulator start-up
 - HVIO 4 - 2 mode
- Register 0x74
 - V1 reset threshold at start-up
 - FNMC mode/debug feature control
 - SDMC mode/debug feature control
 - VEXTAC pin
 - Sleep mode activation

During SW development, to simplify the application debugging, the FNMC and SDMC modes can be used to (partially) disable the Watchdog. In production, the FNMC and SDMC should be disabled to have always full Watchdog functionality present! However, it could be demanding to restore the MTPNV back to factory settings (FNMC enabled) and configure the MTPNV parameters again, but this time with SDMC mode enabled for diagnostics purposes. Or simply enable debug feature by configuring the watchdog into autonomous mode.

Once a UJA113X device has been registered, the [UJA113X_SetMtpnv\(\)](#) can be invoked. This function is called with the parameter set of parameters to be programmed into the non-volatile memory.

This allows the user to define production parameters with FNMC & SDMC disabled and in case of need to enable it again without the need of reflashing the host MCU with some debug firmware.

17.17.2.1 Restoring MTPNV factory preset values

The values are restored when following conditions apply for at least `td(MTPNV)` during power-up:

- pin RSTN is held LOW
- CANH is pulled up to Vbat
- CANL is pulled down to GND

Warning

Restoring the devices MTPNV back to factory preset values is not supported by the library and it's the users responsibility to implement this feature either in SW or HW.

17.17.2.2 MTPNV debug flow control

To have the possibility to enable debugging features (through SDMC mode and watchdog autonomous mode) but keep the MCUs firmware untouched, an MTPNV control sequence depicted on the following figure is recommended: This mechanism allows to partially or completely disable the watchdog if required without the need of flashing a custom firmware into the host MCU. In case the MTPNV has been already programmed or it's not allowed by the application to clear the MTPNV, it's still possible to switch the watchdog mode into autonomous, which keeps the watchdog enabled only in normal mode.

Note

If it's requested to set the SDMC mode, the MTPNV has to be restored prior to the above procedure (not depicted in the diagram).

The idea is:

- Reprogramming the MTPNV to enable SDMC
 - 1. Restore factory settings of MTPNV (as described earlier)
 - 2. Program the MTPNV with SDMC enabled
 - 3. Depending on situation switch the watchdog mode to autonomous
 - 4. The watchdog is disabled all the time
- Keep the MTPNV untouched (SDMC disabled) and partially disable watchdog
 - 1. Switch the Watchdog mode to autonomous
 - 2. Watchdog disabled in all other modes then normal (in case there are no pending interrupts)

Note

See [02. Watchdog](#) section for more details on watchdog behaviour under different circumstances

17.17.2.3 Example

This example demonstrates one of many possible implemetnatations.

```
.
.
/* Define the MTPNV parameters */
ujall3x_mtpnv_cfg_t mtpnvConfig =
{
    /* highSideCtrl */
    HHSDC_IO8HOC_DISABLED | HHSDC_IO7HOC_DISABLED |
    HHSDC_IO6HOC_DISABLED | HHSDC_IO5HOC_DISABLED |
```



```

HNSDC_IO4HOC_DISABLED | HNSDC_IO3HOC_DISABLED |
HNSDC_IO2HOC_DISABLED | HNSDC_IO1HOC_DISABLED,

/* lowSideCtrl */
HNSDC_IO8LOC_DISABLED | HNSDC_IO7LOC_DISABLED |
HNSDC_IO6LOC_DISABLED | HNSDC_IO5LOC_DISABLED |
HNSDC_IO4LOC_DISABLED | HNSDC_IO3LOC_DISABLED |
HNSDC_IO2LOC_DISABLED | HNSDC_IO1LOC_DISABLED,

/* startupCtrl */
RLC_PULSE_WIDTH_10_12_MS | V2SUC_ALWAYS_ON |
IO4SFC_STD_IO | IO3SFC_STD_IO | IO2SFC_LIMP_HOME,

/* sbcConfigCtrl */
V1RTSUC_90_NOM | FNMC_DISABLE | SDMC_ENABLE |
VEXTAC_SENSOR_SUPPLY | SLPC_SLEEP_SUPPORTED
}
.
.

#define SBC0 0U

void main (void)
{
    /* Initialize the MCU - clock, peripherals etc. */
    ...
    /* Initialize the SPI periheral for SBC */
    ...
    /* Initialize the SBC */
    uja113x_drv_cfg_t sbcConfig =
    {
        UJA1132HW5V0, /* chipType */
        0U,           /* SPI instance */
        100U,         /* SPI timeout */
    };

    UJA113X_RegisterDevice(SBC0, &sbcConfig);

    bool enable_debug_mode = false;
    bool set_debug         = false;

    while (1U)
    {
        /*
         * Set enable_debug_mode and set_debug using some event over
         * CAN/LIN/USART etc. or GPIO inputs - application specific
         */
        ...

        if (true == enable_debug_mode)
        {
            /* Read the NVMPs status bit - UJA113X_SbcTransfer() can be used */
            ...

            if (1U == NVMPs)
            {
                /* Programm the MTPNV */
                UJA113X_SetMtpnv(SBC0, mtpnvConfig);
            }
            else
            {
                if (true == set_debug)
                {
                    /* Set Watchdog into autonomous mode - UJA113X_SetWatchdog() can be used */
                    ...
                }
                else
                {
                    /* Set Watchdog into application defined mode - UJA113X_SetWatchdog() can be used*/
                    ...
                }
            }
        }
    }
}

```

17.17.2.4 CRC calculation on MTPNV data

To confirm MTPNV write, last byte written into the SBC (register 0x75) has to be a CRC-8 computed over the written bytes (4 bytes!). This is handled automatically by the [UJA113X_SetMtpnv\(\)](#). However if the user wants to implemet his own programming procedure, the CRC function is available, see [UJA113X_ComputeCrc8\(\)](#) for details.

Note

During CRC computation for devices with partial/none HVIO's the respective bits in registers 0x71 & 0x72 should be considered as 0 even when set by user to 1!

17.17.2.5 Device ID

Although, there is no dedicated function for reading the devices ID, the [UJA113X_SbcTransfer\(\)](#) can be used to read the ID registers (0x7E & 0x7F).

Modules

- [HVIO high-side configuration options \(0x71\)](#)
- [HVIO low-side configuration options \(0x72\)](#)
- [SBC configuration control options \(0x74\)](#)
- [Start-up control configuration options \(0x73\)](#)

Data Structures

- struct [uja113x_mtpnv_cfg_t](#)
MTPNV registers configuration structure (0x71 - 0x74) [More...](#)
- struct [crc_spec_t](#)
Defines the CRC8 algorithm to be used. [More...](#)

Functions

- status_t [UJA113X_SetMtpnv](#) (uint32_t instance, const [uja113x_mtpnv_cfg_t](#) *mtpnvConfig)
Writes the non-volatile memory parameters (0x71 - 0x75) of SBC.
- uint8_t [UJA113X_ComputeCrc8](#) (const [crc_spec_t](#) *crcDesc, const uint8_t *data, uint8_t size)
Generic function for CRC8 computation.

17.17.3 Data Structure Documentation**17.17.3.1 struct uja113x_mtpnv_cfg_t**

MTPNV registers configuration structure (0x71 - 0x74)

Implements : [uja113x_mtpnv_cfg_t_Class](#)

Definition at line 1752 of file [sbc_uja113x.h](#).

Data Fields

- uint8_t [highSideCtrl](#)
Configures the HVIO high-side driver behavior (0x71); See [HVIO high-side configuration options \(0x71\)](#).
- uint8_t [lowSideCtrl](#)
Configures the HVIO low-side driver behavior (0x72); See [HVIO low-side configuration options \(0x72\)](#).
- uint8_t [startupCtrl](#)
Configures the start-up control register (0x73); See [Start-up control configuration options \(0x73\)](#).
- uint8_t [sbcConfigCtrl](#)
Configures the SBC configuration control register (0x74); See [SBC configuration control options \(0x74\)](#).

Field Documentation

17.17.3.1.1 uint8_t highSideCtrl

Configures the HVIO high-side driver behavior (0x71); See [HVIO high-side configuration options \(0x71\)](#).

Definition at line 1757 of file sbc_uja113x.h.

17.17.3.1.2 uint8_t lowSideCtrl

Configures the HVIO low-side driver behavior (0x72); See [HVIO low-side configuration options \(0x72\)](#).

Definition at line 1761 of file sbc_uja113x.h.

17.17.3.1.3 uint8_t sbcConfigCtrl

Configures the SBC configuration control register (0x74); See [SBC configuration control options \(0x74\)](#).

Definition at line 1769 of file sbc_uja113x.h.

17.17.3.1.4 uint8_t startupCtrl

Configures the start-up control register (0x73); See [Start-up control configuration options \(0x73\)](#).

Definition at line 1765 of file sbc_uja113x.h.

17.17.3.2 struct crc_spec_t

Defines the CRC8 algorithm to be used.

This structure describes the CRC algorithm. Based on this structure the [UJA113X_ComputeCrc8\(\)](#), knows, how to compute the CRC value.

Implements : `crc_spec_t_Class`

Definition at line 2638 of file sbc_uja113x.h.

Data Fields

- uint8_t [poly](#)
Generating polynomial.
- uint8_t [init](#)
Initial value.
- bool [refIn](#)
Reflect input data before computation.
- bool [refOut](#)
Reflect output data before computation.
- uint8_t [xorOut](#)
Output xored by this value.

Field Documentation

17.17.3.2.1 uint8_t init

Initial value.

Definition at line 2641 of file sbc_uja113x.h.

17.17.3.2.2 uint8_t poly

Generating polynomial.

Definition at line 2640 of file sbc_uja113x.h.

17.17.3.2.3 bool refln

Reflect input data before computation.

Definition at line 2642 of file sbc_uja113x.h.

17.17.3.2.4 bool refOut

Reflect output data before computation.

Definition at line 2643 of file sbc_uja113x.h.

17.17.3.2.5 uint8_t xorOut

Output xored by this value.

Definition at line 2644 of file sbc_uja113x.h.

17.17.4 Function Documentation

17.17.4.1 uint8_t UJA113X_ComputeCrc8 (const crc_spec_t * crcDesc, const uint8_t * data, uint8_t size)

Generic function for CRC8 computation.

The CRC algorithm is defined by `crc_spec_t` input parameter, which holds all the relevant information for CRC8 computation. A brute force mechanism is used instead of table driven.

Parameters

in	<i>crcDesc</i>	Pointer to CRC8 algorithm description
in	<i>data</i>	Array of data over which CRC should be calculated
in	<i>size</i>	Size of array in bytes

Returns

Computed CRC8 over *data* described by *crcDesc*

Note

For subsequent calls the CRC from previous computation should be used as initial seed.

Warning

The *refln* and *refOut* values have no influence on the computation! The functionality is not implemented yet!

17.17.4.2 status_t UJA113X_SetMtpnv (uint32_t instance, const uja113x_mtpnv_cfg_t * mtpnvConfig)

Writes the non-volatile memory parameters (0x71 - 0x75) of SBC.

The function prepares a frame based on input configuration parameters and initiates SPI communication in blocking mode. On successful transmission the first byte is verified. In case of a mismatch the MTPNV configuration registers have not been written properly and the process has to be repeated. In case a mismatch happens on CRC write, the outcome can be recognized by reading out the MTPNV registers, reading the MTPNV status bit and an SBC reset in case of success.

Parameters

in	<i>instance</i>	Index of SBC to configure
in	<i>mtpnvConfig</i>	Parameters to be loaded into SBC

Returns

STATUS_SUCCESS Configuration successful STATUS_BUSY SPI perihperal is busy STATUS_TIMEOUT SPI communication timed out, configuration aborted SBC_CMD_ERROR First received byte doesn't match the repeated address,

Note

The CRC value is calculated by the function.

Warning

During CRC computation for devices with partial/none HVIO's the respective bits in registers 0x71 & 0x72 should be considered as 0 even when set by user to 1! The function checks the chipType registered with [UJA113X_RegisterDevice\(\)](#) and clears these bits for the purpose of CRC computation.

Definition at line 1091 of file sbc_uja113x.c.

17.18 ADC Driver

17.18.1 Detailed Description

Analog to Digital Converter Peripheral Driver.

The ADC is a configurable 12-bit (selectable to between 8-bit, 10-bit and 12-bit resolution) single-ended SAR converter.

Features of the ADC include:

- up to 32 control channels (depending on the device variant), with configurable triggers
- up to 32 selectable external input sources (depending on the device variant) and multiple internal input sources
- hardware compare and average functions
- auto-calibration feature

Hardware background

The ADC included in the S32K14x series is a selectable resolution (8, 10, 12-bit), single-ended, SAR converter. Depending on the device variant, each ADC instance has up to 40 selectable input channels (up to 32 external and up to 8 internal) and up to 32 control channels (each with a result register, an input channel selection register and interrupt enable).

Sample time is configurable through selection of A/D clock and a configurable sample time (in A/D clocks).

Also provided are the Hardware Average and Hardware Compare Features.

Hardware Average will sample a selectable number of measurements and average them before signaling a Conversion Complete.

Hardware Compare can be used to signal if an input channel goes outside (or inside) of a predefined range.

The **Calibration** features can be used to automatically calibrate or fine-tune the ADC before use.

Driver consideration

The ADC Driver provides access to all features, but not all need to be configured to use the ADC. The user application can use the default for most settings, changing only what is necessary. For example, if Compare or Average features are not used, the user does not need to configure them.

The Driver uses structures for configuration. Each structure contains members that are specific to its respective functionality. There is a **converter** structure, a hardware **compare** structure, a hardware **average** structure and a **calibration** structure. Each struct has a corresponding `InitStruct()` method that can be used to initialize the members to reset values, so the user can change only the values that are specific to the application.

The Driver also includes support for configuring the Trigger Latching and Arbitration Unit controlled from a separate hardware module - System Integration Module (SIM).

Interrupt handling

The ADC Driver in S32 SDK does not use interrupts internally. These can be defined by the user application. There are two ways to add an ADC interrupt:

1. Using the weak symbols defined by start-up code. If the methods `ADCx_Handler(void)` (x denotes instance number) are not defined, the linker uses a default ISR. An error will be generated if methods with the same name are defined multiple times. This method works regardless of the placement of the interrupt vector table (Flash or RAM).
2. Using the Interrupt Manager's `INT_SYS_InstallHandler()` method. This can be used to dynamically change the ISR at run-time. This method works only if the interrupt vector table is located in RAM (S32 SDK behavior). To get the ADC instance's interrupt number, use `ADC_DRV_GetInterruptNumber()`.

Clocking and pin configuration

The ADC Driver does not handle clock setup (from PCC) or any kind of pin configuration (done by PORT module). This is handled by the Clock Manager and PORT module, respectively. The driver assumes that correct clock configurations have been made, so it is the user's responsibility to set up clocking and pin configurations correctly.

Triggering a conversion

There are two separate ways for triggering an ADC conversion from a control channel:

1. Software triggering Only conversion from first control channel may be triggered from software - must enabled at converter configuration Initiated by writing a valid input channel ID to the first control channel - use [ADC_Drv_ConfigChan\(\)](#).
2. Hardware triggering Conversion from any control channel may be hardware triggered - however for first control channel it must be enabled at converter configuration.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
* ${S32SDK_PATH}\platform\drivers\src\adc_driver.c
*
```

Include path

The following paths need to be added to the include path of the toolchain:

```
* ${S32SDK_PATH}\platform\drivers\inc\
*
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager](#)

Data Structures

- struct [adc_converter_config_t](#)
Defines the converter configuration. [More...](#)
- struct [adc_compare_config_t](#)
Defines the hardware compare configuration. [More...](#)
- struct [adc_average_config_t](#)
Defines the hardware average configuration. [More...](#)
- struct [adc_chan_config_t](#)
Defines the control channel configuration. [More...](#)
- struct [adc_calibration_t](#)
Defines the user calibration configuration. [More...](#)

Enumerations

- enum [adc_clk_divide_t](#) { [ADC_CLK_DIVIDE_1](#) = 0x00U, [ADC_CLK_DIVIDE_2](#) = 0x01U, [ADC_CLK_DIVIDE_4](#) = 0x02U, [ADC_CLK_DIVIDE_8](#) = 0x03U }

Clock Divider selection.

- enum `adc_resolution_t` { `ADC_RESOLUTION_8BIT` = 0x00U, `ADC_RESOLUTION_12BIT` = 0x01U, `ADC_RESOLUTION_10BIT` = 0x02U }

Conversion resolution selection.

- enum `adc_input_clock_t` { `ADC_CLK_ALT_1` = 0x00U, `ADC_CLK_ALT_2` = 0x01U, `ADC_CLK_ALT_3` = 0x02U, `ADC_CLK_ALT_4` = 0x03U }

Input clock source selection.

- enum `adc_trigger_t` { `ADC_TRIGGER_SOFTWARE` = 0x00U, `ADC_TRIGGER_HARDWARE` = 0x01U }

Trigger type selection.

- enum `adc_pretrigger_sel_t` { `ADC_PRETRIGGER_SEL_PDB` = 0x00U, `ADC_PRETRIGGER_SEL_TRGMUX` = 0x01U, `ADC_PRETRIGGER_SEL_SW` = 0x02U }

Pretrigger types selectable from Trigger Latching and Arbitration Unit.

- enum `adc_trigger_sel_t` { `ADC_TRIGGER_SEL_PDB` = 0x00U, `ADC_TRIGGER_SEL_TRGMUX` = 0x01U }

Trigger source selectable from Trigger Latching and Arbitration Unit.

- enum `adc_sw_pretrigger_t` { `ADC_SW_PRETRIGGER_DISABLED` = 0x00U, `ADC_SW_PRETRIGGER_0` = 0x04U, `ADC_SW_PRETRIGGER_1` = 0x05U, `ADC_SW_PRETRIGGER_2` = 0x06U, `ADC_SW_PRETRIGGER_3` = 0x07U }

Software pretriggers which may be set from Trigger Latching and Arbitration Unit.

- enum `adc_voltage_reference_t` { `ADC_VOLTAGEREF_VREF` = 0x00U, `ADC_VOLTAGEREF_VALT` = 0x01U }

Voltage reference selection.

- enum `adc_average_t` { `ADC_AVERAGE_4` = 0x00U, `ADC_AVERAGE_8` = 0x01U, `ADC_AVERAGE_16` = 0x02U, `ADC_AVERAGE_32` = 0x03U }

Hardware average selection.

- enum `adc_inputchannel_t` { `ADC_INPUTCHAN_EXT0` = 0x00U, `ADC_INPUTCHAN_EXT1` = 0x01U, `ADC_INPUTCHAN_EXT3` = 0x03U, `ADC_INPUTCHAN_EXT4` = 0x04U, `ADC_INPUTCHAN_EXT5` = 0x05U, `ADC_INPUTCHAN_EXT6` = 0x06U, `ADC_INPUTCHAN_EXT7` = 0x07U, `ADC_INPUTCHAN_EXT9` = 0x09U, `ADC_INPUTCHAN_EXT10` = 0x0AU, `ADC_INPUTCHAN_EXT11` = 0x0BU, `ADC_INPUTCHAN_EXT12` = 0x0CU, `ADC_INPUTCHAN_EXT13` = 0x0DU, `ADC_INPUTCHAN_EXT14` = 0x0EU, `ADC_INPUTCHAN_DISABLED` = `ADC_SC1_ADCH_MASK`, `ADC_INPUTCHAN_INT0` = 0x15, `ADC_INPUTCHAN_INT1` = 0x16, `ADC_INPUTCHAN_INT2` = 0x17, `ADC_INPUTCHAN_INT3` = 0x1C, `ADC_INPUTCHAN_TEMP` = 0x1A, `ADC_INPUTCHAN_BANDGAP` = 0x1B, `ADC_INPUTCHAN_VREFSH` = 0x1D, `ADC_INPUTCHAN_VREFSL` = 0x1E, `ADC_INPUTCHAN_SUPPLY_VDD` = 0xF00U, `ADC_INPUTCHAN_SUPPLY_VDDA` = 0xF01U, `ADC_INPUTCHAN_SUPPLY_VREFH` = 0xF02U, `ADC_INPUTCHAN_SUPPLY_VDD_3V` = 0xF03U, `ADC_INPUTCHAN_SUPPLY_VDD_FLASH_3V` = 0xF04U, `ADC_INPUTCHAN_SUPPLY_VDD_LV` = 0xF05U }

Enumeration of input channels assignable to a control channel.

Note 0: entries in this enum are affected by `::FEATURE_ADC_NUM_EXT_CHANS`, which is device dependent and controlled from "device_name" _features.h file.

- enum `adc_latch_clear_t` { `ADC_LATCH_CLEAR_WAIT`, `ADC_LATCH_CLEAR_FORCE` }

Defines the trigger latch clear method Implements : `adc_latch_clear_t` Class.

Converter

Converter specific methods. These are used to configure and use the A/D Converter specific functionality, including:

- clock input and divider
- sample time in A/D clocks

- resolution
- trigger source
- voltage reference
- enable DMA
- enable continuous conversion on one channel

To start a conversion, a control channel (see [Channel Configuration](#)) and a trigger source must be configured. Once a conversion is started, the user application can wait for it to be finished by calling the [ADC_DRV_WaitConvDone\(\)](#) function.

Only the first control channel can be triggered by software. To start a conversion in this case, an input channel must be written in the channel selection register using the [ADC_DRV_ConfigChan\(\)](#) method. Writing a value to the control channel while a conversion is being performed on that channel will start a new conversion.

- void [ADC_DRV_InitConverterStruct](#) ([adc_converter_config_t](#) *const config)
Initializes the converter configuration structure.
- void [ADC_DRV_ConfigConverter](#) (const uint32_t instance, const [adc_converter_config_t](#) *const config)
Configures the converter with the given configuration structure.
- void [ADC_DRV_GetConverterConfig](#) (const uint32_t instance, [adc_converter_config_t](#) *const config)
Gets the current converter configuration.
- void [ADC_DRV_Reset](#) (const uint32_t instance)
Resets the converter (sets all configurations to reset values)
- void [ADC_DRV_WaitConvDone](#) (const uint32_t instance)
Waits for a conversion/calibration to finish.
- bool [ADC_DRV_GetConvCompleteFlag](#) (const uint32_t instance, const uint8_t chanIndex)
Gets the control channel Conversion Complete Flag state.

Hardware Compare

The Hardware Compare feature of the S32K144 ADC is a versatile mechanism that can be used to monitor that a value is within certain values. Measurements can be monitored to be within certain ranges:

- less than/ greater than a fixed value
- inside or outside of a certain range

Two compare values can be configured (the second value is used only for range function mode). The compare values must be written in 12-bit resolution mode regardless of the actual used resolution mode.

Once the hardware compare feature is enabled, a conversion is considered complete only when the measured value is within the allowable range set by the configuration.

- void [ADC_DRV_InitHwCompareStruct](#) ([adc_compare_config_t](#) *const config)
Initializes the Hardware Compare configuration structure.
- void [ADC_DRV_ConfigHwCompare](#) (const uint32_t instance, const [adc_compare_config_t](#) *const config)
Configures the Hardware Compare feature with the given configuration structure.
- void [ADC_DRV_GetHwCompareConfig](#) (const uint32_t instance, [adc_compare_config_t](#) *const config)
Gets the current Hardware Compare configuration.

Hardware Average

The Hardware Average feature of the S32K144 allows for a set of measurements to be averaged together as a single conversion. The number of samples to be averaged is selectable (4, 8, 16 or 32 samples).

- void [ADC_DRV_InitHwAverageStruct](#) ([adc_average_config_t](#) *const config)
Initializes the Hardware Average configuration structure.
- void [ADC_DRV_ConfigHwAverage](#) (const uint32_t instance, const [adc_average_config_t](#) *const config)
Configures the Hardware Average feature with the given configuration structure.
- void [ADC_DRV_GetHwAverageConfig](#) (const uint32_t instance, [adc_average_config_t](#) *const config)
Gets the current Hardware Average configuration.

Channel configuration

Control register specific functions. These functions control configurations for each control channel (input channel selection and interrupt enable).

When software triggering is enabled, calling the [ADC_DRV_ConfigChan\(\)](#) method for control channel 0 starts a new conversion.

After a conversion is finished, the result can be retrieved using the [ADC_DRV_GetChanResult\(\)](#) method.

- void [ADC_DRV_InitChanStruct](#) ([adc_chan_config_t](#) *const config)
Initializes the control channel configuration structure.
- void [ADC_DRV_ConfigChan](#) (const uint32_t instance, const uint8_t chanIndex, const [adc_chan_config_t](#) *const config)
Configures the selected control channel with the given configuration structure.
- void [ADC_DRV_GetChanConfig](#) (const uint32_t instance, const uint8_t chanIndex, [adc_chan_config_t](#) *const config)
Gets the current control channel configuration for the selected channel index.
- void [ADC_DRV_SetSwPretrigger](#) (const uint32_t instance, const [adc_sw_pretrigger_t](#) swPretrigger)
This function sets the software pretrigger - affects only first 4 control channels.
- void [ADC_DRV_GetChanResult](#) (const uint32_t instance, const uint8_t chanIndex, uint16_t *const result)
Gets the last result for the selected control channel.

Automatic Calibration

These methods control the Calibration feature of the ADC.

The [ADC_DRV_AutoCalibration\(\)](#) method can be called to execute a calibration sequence, or a calibration can be retrieved with the [ADC_DRV_GetUserCalibration\(\)](#) and saved to non-volatile storage, to avoid calibration on every power-on. The calibration structure can be written with the [ADC_DRV_ConfigUserCalibration\(\)](#) method.

- void [ADC_DRV_AutoCalibration](#) (const uint32_t instance)
Executes an Auto-Calibration.
- void [ADC_DRV_InitUserCalibrationStruct](#) ([adc_calibration_t](#) *const config)
Initializes the User Calibration configuration structure.
- void [ADC_DRV_ConfigUserCalibration](#) (const uint32_t instance, const [adc_calibration_t](#) *const config)
Configures the User Calibration feature with the given configuration structure.
- void [ADC_DRV_GetUserCalibration](#) (const uint32_t instance, [adc_calibration_t](#) *const config)
Gets the current User Calibration configuration.

Interrupts

This method returns the interrupt number for an ADC instance, which can be used to configure the interrupt, like in Interrupt Manager.

- IRQn_Type [ADC_DRV_GetInterruptNumber](#) (const uint32_t instance)
Returns the interrupt number for the ADC instance.

Latched triggers processing

These functions provide basic operations for using the trigger latch mechanism.

- void [ADC_DRV_ClearLatchedTriggers](#) (const uint32_t instance, const [adc_latch_clear_t](#) clearMode)
Clear latched triggers under processing.
- void [ADC_DRV_ClearTriggerErrors](#) (const uint32_t instance)
Clear all latch trigger error.
- uint32_t [ADC_DRV_GetTriggerErrorFlags](#) (const uint32_t instance)
Get the trigger error flags bits of the ADC instance.

17.18.2 Data Structure Documentation

17.18.2.1 struct adc_converter_config_t

Defines the converter configuration.

This structure is used to configure the ADC converter

Implements : [adc_converter_config_t_Class](#)

Definition at line 249 of file [adc_driver.h](#).

Data Fields

- [adc_clk_divide_t](#) clockDivide
- uint8_t sampleTime
- [adc_resolution_t](#) resolution
- [adc_input_clock_t](#) inputClock
- [adc_trigger_t](#) trigger
- [adc_pretrigger_sel_t](#) pretriggerSel
- [adc_trigger_sel_t](#) triggerSel
- bool dmaEnable
- [adc_voltage_reference_t](#) voltageRef
- bool continuousConvEnable
- bool supplyMonitoringEnable

Field Documentation

17.18.2.1.1 [adc_clk_divide_t](#) clockDivide

Divider of the input clock for the ADC

Definition at line 251 of file [adc_driver.h](#).

17.18.2.1.2 bool continuousConvEnable

Enable Continuous conversions

Definition at line 260 of file [adc_driver.h](#).

17.18.2.1.3 bool dmaEnable

Enable DMA for the ADC

Definition at line 258 of file `adc_driver.h`.

17.18.2.1.4 adc_input_clock_t inputClock

Input clock source

Definition at line 254 of file `adc_driver.h`.

17.18.2.1.5 adc_pretrigger_sel_t pretriggerSel

Pretrigger source selected from Trigger Latching and Arbitration Unit - affects only the first 4 control channels

Definition at line 256 of file `adc_driver.h`.

17.18.2.1.6 adc_resolution_t resolution

ADC resolution (8,10,12 bit)

Definition at line 253 of file `adc_driver.h`.

17.18.2.1.7 uint8_t sampleTime

Sample time in AD Clocks

Definition at line 252 of file `adc_driver.h`.

17.18.2.1.8 bool supplyMonitoringEnable

Only available for ADC 0. Enable internal supply monitoring - enables measurement of ADC_INPUTCHAN_SUPPLY sources.

Definition at line 261 of file `adc_driver.h`.

17.18.2.1.9 adc_trigger_t trigger

ADC trigger type (software, hardware) - affects only the first control channel

Definition at line 255 of file `adc_driver.h`.

17.18.2.1.10 adc_trigger_sel_t triggerSel

Trigger source selected from Trigger Latching and Arbitration Unit

Definition at line 257 of file `adc_driver.h`.

17.18.2.1.11 adc_voltage_reference_t voltageRef

Voltage reference used

Definition at line 259 of file `adc_driver.h`.

17.18.2.2 struct adc_compare_config_t

Defines the hardware compare configuration.

This structure is used to configure the hardware compare feature for the ADC

Implements : `adc_compare_config_t_Class`

Definition at line 272 of file `adc_driver.h`.

Data Fields

- bool [compareEnable](#)

- bool [compareGreaterThanEnable](#)
- bool [compareRangeFuncEnable](#)
- uint16_t [compVal1](#)
- uint16_t [compVal2](#)

Field Documentation

17.18.2.2.1 bool compareEnable

Enable the compare feature

Definition at line 274 of file `adc_driver.h`.

17.18.2.2.2 bool compareGreaterThanEnable

Enable Greater-Than functionality

Definition at line 275 of file `adc_driver.h`.

17.18.2.2.3 bool compareRangeFuncEnable

Enable Range functionality

Definition at line 276 of file `adc_driver.h`.

17.18.2.2.4 uint16_t compVal1

First Compare Value

Definition at line 277 of file `adc_driver.h`.

17.18.2.2.5 uint16_t compVal2

Second Compare Value

Definition at line 278 of file `adc_driver.h`.

17.18.2.3 struct adc_average_config_t

Defines the hardware average configuration.

This structure is used to configure the hardware average feature for the ADC

Implements : `adc_average_config_t_Class`

Definition at line 289 of file `adc_driver.h`.

Data Fields

- bool [hwAvgEnable](#)
- [adc_average_t](#) [hwAverage](#)

Field Documentation

17.18.2.3.1 adc_average_t hwAverage

Selection for number of samples used for averaging

Definition at line 292 of file `adc_driver.h`.

17.18.2.3.2 bool hwAvgEnable

Enable averaging functionality

Definition at line 291 of file `adc_driver.h`.

17.18.2.4 struct adc_chan_config_t

Defines the control channel configuration.

This structure is used to configure a control channel of the ADC

Implements : `adc_chan_config_t_Class`

Definition at line 303 of file `adc_driver.h`.

Data Fields

- `bool` [interruptEnable](#)
- `adc_inputchannel_t` [channel](#)

Field Documentation

17.18.2.4.1 adc_inputchannel_t channel

Selection of input channel for measurement

Definition at line 306 of file `adc_driver.h`.

17.18.2.4.2 bool interruptEnable

Enable interrupts for this channel

Definition at line 305 of file `adc_driver.h`.

17.18.2.5 struct adc_calibration_t

Defines the user calibration configuration.

This structure is used to configure the user calibration parameters of the ADC.

Implements : `adc_calibration_t_Class`

Definition at line 317 of file `adc_driver.h`.

Data Fields

- `uint16_t` [userGain](#)
- `uint16_t` [userOffset](#)

Field Documentation

17.18.2.5.1 uint16_t userGain

User-configurable gain

Definition at line 319 of file `adc_driver.h`.

17.18.2.5.2 uint16_t userOffset

User-configurable Offset (2's complement, subtracted from result)

Definition at line 320 of file `adc_driver.h`.

17.18.3 Enumeration Type Documentation

17.18.3.1 enum adc_average_t

Hardware average selection.

Implements : `adc_average_t_Class`

Enumerator

- ADC_AVERAGE_4** Hardware average of 4 samples.
- ADC_AVERAGE_8** Hardware average of 8 samples.
- ADC_AVERAGE_16** Hardware average of 16 samples.
- ADC_AVERAGE_32** Hardware average of 32 samples.

Definition at line 154 of file `adc_driver.h`.

17.18.3.2 enum `adc_clk_divide_t`

Clock Divider selection.

Implements : `adc_clk_divide_t_Class`

Enumerator

- ADC_CLK_DIVIDE_1** Input clock divided by 1.
- ADC_CLK_DIVIDE_2** Input clock divided by 2.
- ADC_CLK_DIVIDE_4** Input clock divided by 4.
- ADC_CLK_DIVIDE_8** Input clock divided by 8.

Definition at line 57 of file `adc_driver.h`.

17.18.3.3 enum `adc_input_clock_t`

Input clock source selection.

Implements : `adc_input_clock_t_Class`

Enumerator

- ADC_CLK_ALT_1** Input clock alternative 1.
- ADC_CLK_ALT_2** Input clock alternative 2.
- ADC_CLK_ALT_3** Input clock alternative 3.
- ADC_CLK_ALT_4** Input clock alternative 4.

Definition at line 82 of file `adc_driver.h`.

17.18.3.4 enum `adc_inputchannel_t`

Enumeration of input channels assignable to a control channel.

Note 0: entries in this enum are affected by `::FEATURE_ADC_NUM_EXT_CHANS`, which is device dependent and controlled from `"device_name"_features.h` file.

Note 1: the actual number of external channels may differ between device packages and ADC instances. Reading a channel that is not connected externally, will return a random value within the range. Please refer to the Reference Manual for the maximum number of external channels for each device variant and ADC instance.

Note 2: `ADC_INPUTCHAN_SUPPLY_` select which internal supply channel to be measured. They are only available for ADC0 and measured internally via internal input channel 0. Please note that supply monitoring needs to be enabled separately via dedicated flag in [adc_converter_config_t](#).

Implements : `adc_inputchannel_t_Class`

Enumerator

- ADC_INPUTCHAN_EXT0** External input channel 0
- ADC_INPUTCHAN_EXT1** External input channel 1

ADC_INPUTCHAN_EXT3 External input channel 3
ADC_INPUTCHAN_EXT4 External input channel 4
ADC_INPUTCHAN_EXT5 External input channel 5
ADC_INPUTCHAN_EXT6 External input channel 6
ADC_INPUTCHAN_EXT7 External input channel 7
ADC_INPUTCHAN_EXT9 External input channel 9
ADC_INPUTCHAN_EXT10 External input channel 10
ADC_INPUTCHAN_EXT11 External input channel 11
ADC_INPUTCHAN_EXT12 External input channel 12
ADC_INPUTCHAN_EXT13 External input channel 13
ADC_INPUTCHAN_EXT14 External input channel 14
ADC_INPUTCHAN_DISABLED Channel disabled
ADC_INPUTCHAN_INT0 Internal input channel 0
ADC_INPUTCHAN_INT1 Internal input channel 1
ADC_INPUTCHAN_INT2 Internal input channel 2
ADC_INPUTCHAN_INT3 Internal input channel 3
ADC_INPUTCHAN_TEMP Temperature Sensor
ADC_INPUTCHAN_BANDGAP Band Gap
ADC_INPUTCHAN_VREFSH Voltage Reference Select High
ADC_INPUTCHAN_VREFSL Voltage Reference Select Low
ADC_INPUTCHAN_SUPPLY_VDD Monitor internal supply 5 V input VDD supply.
ADC_INPUTCHAN_SUPPLY_VDDA Monitor internal supply 5 V input analog supply.
ADC_INPUTCHAN_SUPPLY_VREFH Monitor internal supply ADC reference supply.
ADC_INPUTCHAN_SUPPLY_VDD_3V Monitor internal supply 3.3 V oscillator regulator output.
ADC_INPUTCHAN_SUPPLY_VDD_FLASH_3V Monitor internal supply 3.3 V flash regulator output.
ADC_INPUTCHAN_SUPPLY_VDD_LV Monitor internal supply 1.2 V core regulator output.

Definition at line 177 of file adc_driver.h.

17.18.3.5 enum adc_latch_clear_t

Defines the trigger latch clear method Implements : adc_latch_clear_t_Class.

Enumerator

ADC_LATCH_CLEAR_WAIT Clear by waiting all latched triggers to be processed
ADC_LATCH_CLEAR_FORCE Process current trigger and clear all latched

Definition at line 327 of file adc_driver.h.

17.18.3.6 enum adc_pretrigger_sel_t

Pretrigger types selectable from Trigger Latching and Arbitration Unit.

Implements : adc_pretrigger_sel_t_Class

Enumerator

ADC_PRETRIGGER_SEL_PDB PDB pretrigger selected.
ADC_PRETRIGGER_SEL_TRGMUX TRGMUX pretrigger selected.
ADC_PRETRIGGER_SEL_SW Software pretrigger selected.

Definition at line 106 of file adc_driver.h.

17.18.3.7 enum `adc_resolution_t`

Conversion resolution selection.

Implements : `adc_resolution_t_Class`

Enumerator

`ADC_RESOLUTION_8BIT` 8-bit resolution mode
`ADC_RESOLUTION_12BIT` 12-bit resolution mode
`ADC_RESOLUTION_10BIT` 10-bit resolution mode

Definition at line 70 of file `adc_driver.h`.

17.18.3.8 enum `adc_sw_pretrigger_t`

Software pretriggers which may be set from Trigger Latching and Arbitration Unit.

Implements : `adc_sw_pretrigger_t_Class`

Enumerator

`ADC_SW_PRETRIGGER_DISABLED` SW pretrigger disabled.
`ADC_SW_PRETRIGGER_0` SW pretrigger 0.
`ADC_SW_PRETRIGGER_1` SW pretrigger 1.
`ADC_SW_PRETRIGGER_2` SW pretrigger 2.
`ADC_SW_PRETRIGGER_3` SW pretrigger 3.

Definition at line 129 of file `adc_driver.h`.

17.18.3.9 enum `adc_trigger_sel_t`

Trigger source selectable from Trigger Latching and Arbitration Unit.

Implements : `adc_trigger_sel_t_Class`

Enumerator

`ADC_TRIGGER_SEL_PDB` PDB trigger selected.
`ADC_TRIGGER_SEL_TRGMUX` TRGMUX trigger selected.

Definition at line 118 of file `adc_driver.h`.

17.18.3.10 enum `adc_trigger_t`

Trigger type selection.

Implements : `adc_trigger_t_Class`

Enumerator

`ADC_TRIGGER_SOFTWARE` Software trigger.
`ADC_TRIGGER_HARDWARE` Hardware trigger.

Definition at line 95 of file `adc_driver.h`.

17.18.3.11 enum `adc_voltage_reference_t`

Voltage reference selection.

Implements : `adc_voltage_reference_t_Class`

Enumerator

ADC_VOLTAGEREF_VREF VrefH and VrefL as Voltage reference.

ADC_VOLTAGEREF_VALT ValtH and ValtL as Voltage reference.

Definition at line 143 of file adc_driver.h.

17.18.4 Function Documentation

17.18.4.1 void ADC_DRV_AutoCalibration (const uint32_t instance)

Executes an Auto-Calibration.

This functions executes an Auto-Calibration sequence. It is recommended to run this sequence before using the ADC converter.

Parameters

in	instance	instance number
----	----------	-----------------

Definition at line 555 of file adc_driver.c.

17.18.4.2 void ADC_DRV_ClearLatchedTriggers (const uint32_t instance, const adc_latch_clear_t clearMode)

Clear latched triggers under processing.

This function clears all trigger latched flags of the ADC instance. This function must be called after the hardware trigger source for the ADC has been deactivated.

Parameters

in	instance	instance number of the ADC
in	clearMode	The clearing method for the latched triggers <ul style="list-style-type: none"> • ADC_LATCH_CLEAR_WAIT : Wait for all latched triggers to be processed. • ADC_LATCH_CLEAR_FORCE : Clear latched triggers and wait for trigger being process to finish.

Definition at line 712 of file adc_driver.c.

17.18.4.3 void ADC_DRV_ClearTriggerErrors (const uint32_t instance)

Clear all latch trigger error.

This function clears all trigger error flags of the ADC instance.

Parameters

in	instance	instance number of the ADC
----	----------	----------------------------

Definition at line 737 of file adc_driver.c.

17.18.4.4 void ADC_DRV_ConfigChan (const uint32_t instance, const uint8_t chanIndex, const adc_chan_config_t *const config)

Configures the selected control channel with the given configuration structure.

When Software Trigger mode is enabled, configuring control channel index 0, implicitly triggers a new conversion on the selected ADC input channel. Therefore, ADC_DRV_ConfigChan can be used for sw-triggering conversions.

Configuring any control channel while it is actively controlling a conversion (sw or hw triggered) will implicitly abort the on-going conversion.

Parameters

in	<i>instance</i>	instance number
in	<i>chanIndex</i>	the control channel index
in	<i>config</i>	the configuration structure

Definition at line 381 of file `adc_driver.c`.

17.18.4.5 void `ADC_DRV_ConfigConverter (const uint32_t instance, const adc_converter_config_t *const config)`

Configures the converter with the given configuration structure.

This function configures the ADC converter with the options provided in the provided structure.

Parameters

in	<i>instance</i>	instance number
in	<i>config</i>	the configuration structure

Definition at line 94 of file `adc_driver.c`.

17.18.4.6 void `ADC_DRV_ConfigHwAverage (const uint32_t instance, const adc_average_config_t *const config)`

Configures the Hardware Average feature with the given configuration structure.

This function sets the configuration for the Hardware Average feature.

Parameters

in	<i>instance</i>	instance number
in	<i>config</i>	the configuration structure

Definition at line 318 of file `adc_driver.c`.

17.18.4.7 void `ADC_DRV_ConfigHwCompare (const uint32_t instance, const adc_compare_config_t *const config)`

Configures the Hardware Compare feature with the given configuration structure.

This functions sets the configuration for the Hardware Compare feature using the configuration structure.

Parameters

in	<i>instance</i>	instance number
in	<i>config</i>	the configuration structure

Definition at line 255 of file `adc_driver.c`.

17.18.4.8 void `ADC_DRV_ConfigUserCalibration (const uint32_t instance, const adc_calibration_t *const config)`

Configures the User Calibration feature with the given configuration structure.

This function sets the configuration for the user calibration registers.

Parameters

in	<i>instance</i>	instance number
in	<i>config</i>	the configuration structure

Definition at line 658 of file `adc_driver.c`.

17.18.4.9 void `ADC_DRV_GetChanConfig (const uint32_t instance, const uint8_t chanIndex, adc_chan_config_t *const config)`

Gets the current control channel configuration for the selected channel index.

This function returns the configuration for a control channel

Parameters

in	<i>instance</i>	instance number
in	<i>chanIndex</i>	the control channel index
out	<i>config</i>	the configuration structure

Definition at line 406 of file adc_driver.c.

17.18.4.10 void ADC_DRV_GetChanResult (const uint32_t *instance*, const uint8_t *chanIndex*, uint16_t *const *result*)

Gets the last result for the selected control channel.

This function returns the conversion result from a control channel.

Parameters

in	<i>instance</i>	instance number
in	<i>chanIndex</i>	the converter control channel index
out	<i>result</i>	the result raw value

Definition at line 517 of file adc_driver.c.

17.18.4.11 bool ADC_DRV_GetConvCompleteFlag (const uint32_t *instance*, const uint8_t *chanIndex*)

Gets the control channel Conversion Complete Flag state.

This function returns the state of the Conversion Complete flag for a control channel. This flag is set when a conversion is complete or the condition generated by the Hardware Compare feature is evaluated to true.

Parameters

in	<i>instance</i>	instance number
in	<i>chanIndex</i>	the adc control channel index

Returns

the Conversion Complete Flag state

Definition at line 490 of file adc_driver.c.

17.18.4.12 void ADC_DRV_GetConverterConfig (const uint32_t *instance*, adc_converter_config_t *const *config*)

Gets the current converter configuration.

This functions returns the configuration for converter in the form of a configuration structure.

Parameters

in	<i>instance</i>	instance number
out	<i>config</i>	the configuration structure

Definition at line 140 of file adc_driver.c.

17.18.4.13 void ADC_DRV_GetHwAverageConfig (const uint32_t *instance*, adc_average_config_t *const *config*)

Gets the current Hardware Average configuration.

This function returns the configuration for the Hardware Average feature.

Parameters

in	<i>instance</i>	instance number
----	-----------------	-----------------

out	<i>config</i>	the configuration structure
-----	---------------	-----------------------------

Definition at line 337 of file adc_driver.c.

17.18.4.14 void ADC_DRV_GetHwCompareConfig (const uint32_t *instance*, adc_compare_config_t *const *config*)

Gets the current Hardware Compare configuration.

This function returns the configuration for the Hardware Compare feature.

Parameters

in	<i>instance</i>	instance number
out	<i>config</i>	the configuration structure

Definition at line 277 of file adc_driver.c.

17.18.4.15 IRQn_Type ADC_DRV_GetInterruptNumber (const uint32_t *instance*)

Returns the interrupt number for the ADC instance.

This function returns the interrupt number for the specified ADC instance.

Parameters

in	<i>instance</i>	instance number of the ADC
----	-----------------	----------------------------

Returns

irq_number: the interrupt number (index) of the ADC instance, used to configure the interrupt

Definition at line 695 of file adc_driver.c.

17.18.4.16 uint32_t ADC_DRV_GetTriggerErrorFlags (const uint32_t *instance*)

Get the trigger error flags bits of the ADC instance.

This function returns the trigger error flags bits of the ADC instance.

Parameters

in	<i>instance</i>	instance number of the ADC
----	-----------------	----------------------------

Returns

trigErrorFlags The Trigger Error Flags bit-mask

Definition at line 753 of file adc_driver.c.

17.18.4.17 void ADC_DRV_GetUserCalibration (const uint32_t *instance*, adc_calibration_t *const *config*)

Gets the current User Calibration configuration.

This function returns the current user calibration register values.

Parameters

in	<i>instance</i>	instance number
out	<i>config</i>	the configuration structure

Definition at line 677 of file adc_driver.c.

17.18.4.18 void ADC_DRV_InitChanStruct (adc_chan_config_t *const *config*)

Initializes the control channel configuration structure.

This function initializes the control channel configuration structure to default values (Reference Manual resets). This function should be called on a structure before using it to configure a channel (ADC_DRV_ConfigChan), otherwise all members must be written by the caller. This function insures that all members are written with safe values, so the user can modify only the desired members.

Parameters

out	config	the configuration structure
-----	--------	-----------------------------

Definition at line 359 of file adc_driver.c.

17.18.4.19 void ADC_DRV_InitConverterStruct (adc_converter_config_t *const config)

Initializes the converter configuration structure.

This function initializes the members of the [adc_converter_config_t](#) structure to default values (Reference Manual resets). This function should be called on a structure before using it to configure the converter with [ADC_DRV_InitConverterStruct\(\)](#), otherwise all members must be written (initialized) by the user. This function insures that all members are written with safe values, so the user can modify only the desired members.

Parameters

out	config	the configuration structure
-----	--------	-----------------------------

Definition at line 69 of file adc_driver.c.

17.18.4.20 void ADC_DRV_InitHwAverageStruct (adc_average_config_t *const config)

Initializes the Hardware Average configuration structure.

This function initializes the Hardware Average configuration structure to default values (Reference Manual resets). This function should be called before configuring the Hardware Average feature (ADC_DRV_ConfigHwAverage), otherwise all members must be written by the caller. This function insures that all members are written with safe values, so the user can modify the desired members.

Parameters

out	config	the configuration structure
-----	--------	-----------------------------

Definition at line 302 of file adc_driver.c.

17.18.4.21 void ADC_DRV_InitHwCompareStruct (adc_compare_config_t *const config)

Initializes the Hardware Compare configuration structure.

This function initializes the Hardware Compare configuration structure to default values (Reference Manual resets). This function should be called before configuring the Hardware Compare feature (ADC_DRV_ConfigHwCompare), otherwise all members must be written by the caller. This function insures that all members are written with safe values, so the user can modify the desired members.

Parameters

out	config	the configuration structure
-----	--------	-----------------------------

Definition at line 236 of file adc_driver.c.

17.18.4.22 void ADC_DRV_InitUserCalibrationStruct (adc_calibration_t *const config)

Initializes the User Calibration configuration structure.

This function initializes the User Calibration configuration structure to default values (Reference Manual resets). This function should be called on a structure before using it to configure the User Calibration feature (ADC_DRV_InitUserCalibration), otherwise all members must be written by the caller. This function insures that all members are written with safe values, so the user can modify only the desired members. this function will check and reset clock divide based the adc frequency. an error will be displayed if frequency is greater than required clock for calibration.

Parameters

out	<i>config</i>	the configuration structure
-----	---------------	-----------------------------

Definition at line 642 of file adc_driver.c.

17.18.4.23 void ADC_DRV_Reset (const uint32_t *instance*)

Resets the converter (sets all configurations to reset values)

This function resets all the internal ADC registers to reset values.

Parameters

in	<i>instance</i>	instance number
----	-----------------	-----------------

Definition at line 178 of file adc_driver.c.

17.18.4.24 void ADC_DRV_SetSwPretrigger (const uint32_t *instance*, const adc_sw_pretrigger_t *swPretrigger*)

This function sets the software pretrigger - affects only first 4 control channels.

Parameters

in	<i>instance</i>	instance number
in	<i>swPretrigger</i>	the swPretrigger to be enabled

Definition at line 426 of file adc_driver.c.

17.18.4.25 void ADC_DRV_WaitConvDone (const uint32_t *instance*)

Waits for a conversion/calibration to finish.

This functions waits for a conversion to complete by continuously polling the Conversion Active Flag.

Parameters

in	<i>instance</i>	instance number
----	-----------------	-----------------

Definition at line 470 of file adc_driver.c.

17.19 Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL)

17.19.1 Detailed Description

Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL).

ADC PAL general consideration

The ADC PAL is an interface abstraction layer for multiple Analog to Digital Converter peripherals.

The ADC PAL allows configuration of groups of successive conversions started by a single trigger event.

Each conversion in a group is mapped to an ADC input channel - the **conversion group** is actually defined by an array of input channels, which is a member of the `adc_group_config_t` structure. The order of the input channels will also give the order of execution of the conversions within the group.

Note: all conversion groups need to be configured at PAL initialization time.

The trigger event for a group can be SW or HW, and needs to be selected at configuration time.

1. Execution of **SW triggered groups** may be started/stopped by calling a dedicated function `ADC_StartGroupConversion()`, `ADC_StopGroupConversion()`.
2. **HW triggered groups** need to be enabled for execution by calling a dedicated function - the actual execution will be started by the occurrence of the selected hardware trigger event `ADC_EnableHardwareTrigger()`, `ADC_DisableHardwareTrigger()`.

Note: for HW triggered groups the ADC PAL does not configure the peripherals which provide the triggering events (timers, counters, etc.) - they will need to be configured separately by the ADC PAL user.

Each group needs to have associated a **result buffer** which needs to be allocated by the PAL user. The length of the result buffer is defined by two configuration parameters:

* `numChannels` - defines also the size of the `inputChannelArray`

* `numSetsResultBuffer` - defines the number of sets of results which can be stored in the result buffer.

The *length of the result buffer* = `numChannels * numSetsResultBuffer`. Each time a group of conversions finishes execution, a set of results for all conversions in the group will be copied by the PAL into the corresponding result buffer. The PAL considers the result buffer as circular, with the length configured via previously described.

On some platforms, HW triggered groups may support **delay(s)** between the occurrence of the HW trigger event and the actual start of conversions. This feature can be controlled for each HW triggered group via `delayType` and `delayArray` parameters in `adc_group_config_t`. For SW triggered groups, these parameters are ignored. For details please refer to ADC PAL platform specific information.

Each group can also have associated a **notification callback** which will be executed when all conversions finish execution. The callback shall receive as parameter a pointer to `adc_callback_info_t` containing the *group index* for which the notification is called, and *result buffer tail* - offset of the most recent conversion result in the result buffer. Notifications can be enabled and disabled using `ADC_EnableNotification()` and `ADC_DisableNotification()`. By default the notification is set to active when enabling a HW triggered group or starting a SW triggered group.

Note: The notification callback may be set to NULL and thus it will not be called.

For SW triggered groups, **continuous mode** can be enabled at configuration time.

E.g.: a group with 3 conversions `InputCh0`, `InputCh1`, `InputCh2` -> with continuous mode enabled will continuously repeat the series of conversions until it is stopped: `InputCh0`, `InputCh1`, `InputCh2`, `InputCh0`, `InputCh1`, `InputCh2`,...

The user needs to dimension accordingly the result buffer, such that it has sufficient time to read the results before they are overwritten.

For HW triggered groups, continuous mode parameter is not available.

The ADC PAL implicitly configures and uses other peripherals besides ADC - these resources should not be used simultaneously from other parts of the application. For details please refer to the platform specific details.

The ADC PAL module needs to include a configuration file named `adc_pal_cfg.h`, which defines which IPs are used.

The ADC PAL allows configuration of platform specific parameters via a pointer to a platform specific structure, following the naming convention: `extension_adc_<platform>_t`. E.g.: `extension_adc_s32k1xx_t`

Important note

The ADC PAL configuration structure passed via reference to [ADC_Init\(\)](#), including all arrays referenced by structure members, must be persistent throughout the usage of the ADC PAL. Storing them to memory sections which get freed or altered during ADC PAL usage, will lead to unpredictable behavior.

Platform specific details**S32K1xx device family**

On these platforms, each instance of ADC PAL uses:

- one instance of PDB linked to the selected ADC (ADCn - PDBn) - used for both SW and HW triggered groups
- the TRGMUX_TARGET_MODULE_PDBn_TRG_IN targets from TRGMUX - used only for HW triggered groups

These platforms are supported by the ADC PAL of type **ADC_PAL_S32K1xx**.

Important details:

1. The PAL supports configuring any number of conversion groups at PAL initialization time, but every time a HW/SW triggered group is enabled/started, the underlying hardware peripherals are reconfigured.
2. The same input channel may appear multiple times in a group.

Group delay support:

- no delay between HW trigger event and conversions start:
delayType = ADC_DELAY_TYPE_NO_DELAY and *delayArray* = NULL
- group delay between HW trigger event and the start of the first conversion in the group - the rest of conversions start right after the previous one
delayType = ADC_DELAY_TYPE_GROUP_DELAY and *delayArray* set to point to a single uint16_t variable storing the delay value, expressed in PDB ticks (affected by PDB prescaler configurable via config extension)
- individual delays between HW trigger event and the start of each conversion in the group *delayType* = ADC↔_DELAY_TYPE_INDIVIDUAL_DELAY and *delayArray* set to point to an uin16_t array with length equal with the number of conversions in the group
Delays are expressed in PDB ticks (affected by PDB prescaler configurable via config extension). Delay values are measured relative to the trigger event. When a delay expires, a PDB pretrigger is issued.
Note: the pretriggers must not occur while another conversion in the group is running, otherwise the ADC freezes. It is the user's responsibility to make sure they do not overlap, i.e. *delayN_plus_1* > (*delayN* + *conversion_duration*).

MPC5746C and MPC5748G device families

On these platforms, each instance of ADC PAL uses:

- one instance of BCTU - used only for HW triggered groups
- all ADC instances connected to the selected BCTU instance. Please note that the ADC instances may have different resolutions

These platforms are supported by the ADC PAL of type **ADC_PAL_MPC574xC_G_R**.

Group delay support:

- groups do not support delays, so in `adc_group_config_t` structures `delayType` must be set to `ADC_DELAY_TYPE_NO_DELAY` and `delayArray` to `NULL`, in `adc_group_config_t`.

Important details:

- The PAL supports any number of **SW triggered** conversion groups at PAL initialization time. SW triggered groups will be configured directly in ADC, each time `ADC_StartGroupConversion()` is called.
- The maximum supported number of **HW triggered** conversion groups is expressed in two steps:
 - for groups which include a minimum of 2 conversions: the total number of conversions within all these groups shall be less than or equal with the number of BCTU LIST HW registers. (E.g. 1 group of 8 conversions & 1 group of 24 conversions: $8 + 24 \leq 32$)
 - for groups which include a single conversion: the total number of such groups shall be less than or equal with the total number of BCTU Triggers minus the number of configured groups with at least 2 conversions
- An input channel may only appear once in the group, otherwise the last conversion result will appear for each occurrence of the channel index in the group. This is a platform limitation: BCTU has only a single result register per ADC instance, and the ADC has a single result register per channel.
- A conversion group (SW and HW triggered) can target only conversions on a single ADC instance.
- The same trigger source cannot be assigned to multiple HW triggered groups.
- Multiple HW triggered groups may be enabled simultaneously.
However, the user must make sure that the actual HW trigger events do not occur simultaneously and that conversions from multiple groups do not overlap in time. Otherwise hardware errors may occur and results may be overwritten.

MPC574xP and S32Rx7x device families

On these platforms, each instance of ADC PAL uses:

- one instance of CTU - used only for HW triggered groups and statically configured to CTU triggered mode
- all ADC instances connected to the selected CTU instance

These platforms are supported by the ADC PAL of type **ADC_PAL_SAR_CTU**.

Group delay support:

- no delay between HW trigger event and conversions start:
`delayType = ADC_DELAY_TYPE_NO_DELAY` and `delayArray = NULL`
- group delay between HW trigger event and the start of the first conversion in the group - the rest of conversions start right after the previous one
`delayType = ADC_DELAY_TYPE_GROUP_DELAY` and `delayArray` set to point to a single `uint16_t` variable storing the delay value, expressed in CTU ticks (affected by CTU prescaler)

Important details:

- The PAL supports any number of **SW triggered** conversion groups at PAL initialization time. SW triggered groups will be configured directly in ADC, each time `ADC_StartGroupConversion()` is called.
- The maximum supported number of **HW triggered** conversion groups is equal with the number of CTU result FIFOs - defined in platform header file as `CTU_FR_COUNT`. The total number of conversions in all HW triggered groups must be \leq the length of the CTU ADC command list - defined in platform header file as `CTU_CHANNEL_COUNT`.

3. A conversion group (SW and HW triggered) can target only conversions on a single ADC instance.
4. An input channel may only appear once in a SW triggered group, otherwise the last conversion result will appear for each occurrence of the channel index in the group. This is a platform limitation: the ADC has a single result register per channel. For HW triggered groups this restriction doesn't apply.
5. All HW triggered groups can be enabled simultaneously.
However, the user must make sure that the actual HW trigger events do not occur simultaneously and that conversions from multiple groups do not overlap in time. Otherwise hardware errors may occur and results may be overwritten.
6. Each HW triggered group has assigned a CTU result FIFO. The number of channels in each group must be less than the CTU result FIFO length - note that not all FIFOs have the same length. FIFOs are assigned in the same order in which the HW triggered groups are configured in the PAL init state: FIFO#0 assigned to first group, FIFO#1 to second, etc.
7. The trigger sources enabled for a group can implicitly start also the rest of the enabled HW triggered groups. E.g. SourceX configured for group0, sourceY configured for group1. If both groups are enabled, when event from sourceX occurs, both group0 and group1 will execute; the same when event from sourceY occurs.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\pal\src\adc\adc_pal.c
{S32SDK_PATH}\platform\pal\src\adc\adc_irq.c
```

Additionally, it is required to compile also the .c files from the dependencies listed for each ADC PAL type (please see Dependencies subsection below).

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\pal\inc\
{S32SDK_PATH}\platform\drivers\inc\
```

An additional file, named *adc_pal_cfg.h*, must be created by the user and added to one of the include paths. The user has to add to the file the definitions of preprocessor symbols according to the ADC PAL type used. These symbols are specified in the next subsection.

When using the S32 SDK configuration tool, the file is generated by the configurator.

The pal type ADC_PAL_S32K1xx also requires:

```
{S32SDK_PATH}\platform\drivers\src\adc\
```

Compile symbols

1. Define for selecting one of the ADC PAL type to be used:

```
ADC_PAL_S32K1xx
ADC_PAL_MPC574xC_G_R
ADC_PAL_SAR_CTU
```

2. Define the maximum number of HW triggered groups which may be enabled simultaneously. For ADC_PAL_S32K1xx the maximum value of the define is 1.

```
ADC_PAL_MAX_NUM_HW_GROUPS_EN
```

3. For ADC_PAL_MPC574xC_G_R and ADC_PAL_SAR_CTU types, define the total number of configured groups.

```
ADC_PAL_TOTAL_NUM_GROUPS
```

Dependencies

[Interrupt Manager \(Interrupt\)](#)
[OS Interface \(OSIF\)](#)

- The pal type `ADC_PAL_S32K1xx` also depends on:
[ADC Driver](#)
[PDB Driver](#)
[TRGMUX Driver](#)
- The pal type `ADC_PAL_MPC574xC_G_R` also depends on:
`adc_c55_driver`
`bctu_driver`
- The pal type `ADC_PAL_SAR_CTU` also depends on:
`adc_c55_driver`
`ctu_driver`

Data Structures

- struct [adc_group_config_t](#)
Defines the configuration structure for an ADC PAL conversion group. [More...](#)
- struct [adc_config_t](#)
Defines the configuration structure for ADC PAL. [More...](#)
- struct [extension_adc_s32k1xx_t](#)
Defines the extension structure for ADC S32K1xx. [More...](#)

Typedefs

- typedef [adc_inputchannel_t](#) [adc_input_chan_t](#)
Defines the enumeration with ADC PAL input channels.
- typedef [trgmux_trigger_source_t](#) [adc_trigger_source_t](#)
Defines the enumeration with ADC PAL hardware trigger sources.

Enumerations

- enum [adc_delay_type_t](#) { `ADC_DELAY_TYPE_NO_DELAY` = 0u, `ADC_DELAY_TYPE_GROUP_DELAY` = 1u, `ADC_DELAY_TYPE_INDIVIDUAL_DELAY` = 2u }
Defines an enumeration which contains the types of delay configurations for ADC conversions within a group.

Functions

- status_t [ADC_Init](#) (const [adc_instance_t](#) *const instance, const [adc_config_t](#) *const config)
Initializes the ADC PAL instance.
- status_t [ADC_Deinit](#) (const [adc_instance_t](#) *const instance)
Deinitializes the ADC PAL instance.
- status_t [ADC_EnableHardwareTrigger](#) (const [adc_instance_t](#) *const instance, const uint32_t groupIdx)

Enables the selected HW trigger for a conversion group, if the conversion group has support for HW trigger.

- status_t [ADC_DisableHardwareTrigger](#) (const [adc_instance_t](#) *const instance, const uint32_t groupIdx, const uint32_t timeout)

Disables the selected HW trigger for a conversion group, if the conversion group is HW triggered.

- status_t [ADC_StartGroupConversion](#) (const [adc_instance_t](#) *const instance, const uint32_t groupIdx)

Starts the execution of a selected SW triggered ADC conversion group.

- status_t [ADC_StopGroupConversion](#) (const [adc_instance_t](#) *const instance, const uint32_t groupIdx, const uint32_t timeout)

Stops the selected SW triggered ADC conversion group execution.

- status_t [ADC_EnableNotification](#) (const [adc_instance_t](#) *const instance, const uint32_t groupIdx)

Enables the notification callback for a configured group.

- status_t [ADC_DisableNotification](#) (const [adc_instance_t](#) *const instance, const uint32_t groupIdx)

Disables the notification callback for a configured group.

17.19.2 Data Structure Documentation

17.19.2.1 struct [adc_group_config_t](#)

Defines the configuration structure for an ADC PAL conversion group.

Implements : [adc_group_config_t_Class](#)

Definition at line 129 of file [adc_pal.h](#).

Data Fields

- const [adc_input_chan_t](#) * [inputChannelArray](#)
- uint16_t * [resultBuffer](#)
- uint8_t [numChannels](#)
- uint8_t [numSetsResultBuffer](#)
- bool [hwTriggerSupport](#)
- [adc_trigger_source_t](#) [triggerSource](#)
- [adc_delay_type_t](#) [delayType](#)
- uint16_t * [delayArray](#)
- bool [continuousConvEn](#)
- [adc_callback_t](#) [callback](#)
- void * [callbackUserData](#)

Field Documentation

17.19.2.1.1 [adc_callback_t](#) [callback](#)

Callback function associated with group conversion complete

Definition at line 145 of file [adc_pal.h](#).

17.19.2.1.2 void* [callbackUserData](#)

Pointer to additional user data to be passed by the callback

Definition at line 146 of file [adc_pal.h](#).

17.19.2.1.3 bool [continuousConvEn](#)

Flag for enabling continuous conversions of a group - used only for SW triggered groups i.e. [hwTriggerSupport](#)==false.

Definition at line 143 of file [adc_pal.h](#).

17.19.2.1.4 uint16_t* delayArray

Pointer to array of delay values introduced from the occurrence of a HW trigger event until each ADC conversion in the group can start execution. Expressed in clock ticks. Note: the delay might be bigger if there is an overlap with another conversion already executing.

Definition at line 141 of file `adc_pal.h`.

17.19.2.1.5 adc_delay_type_t delayType

Type of delay configuration. Supported values are platform dependent.

Definition at line 140 of file `adc_pal.h`.

17.19.2.1.6 bool hwTriggerSupport

Conversion group is HW triggered (true) or SW triggered (false).

Definition at line 137 of file `adc_pal.h`.

17.19.2.1.7 const adc_input_chan_t* inputChannelArray

Pointer to the array of ADC input channels. Each entry in this array corresponds to an individual conversion in the group. Only on some of the platforms the same input channel may appear multiple times - see device family specific details in the ADC PAL documentation.

Definition at line 131 of file `adc_pal.h`.

17.19.2.1.8 uint8_t numChannels

Number of input channels in the array

Definition at line 134 of file `adc_pal.h`.

17.19.2.1.9 uint8_t numSetsResultBuffer

Number of sets of results which can be stored in result buffer: length of the result buffer = numChannels x numSetsResultBuffer

Definition at line 135 of file `adc_pal.h`.

17.19.2.1.10 uint16_t* resultBuffer

Pointer to the array for conversion results

Definition at line 133 of file `adc_pal.h`.

17.19.2.1.11 adc_trigger_source_t triggerSource

HW trigger source associated with the conversion group. Will be ignored if (`hwTriggerSupport == false`). Note for ADC_SAR_CTU: this enables the HW trigger source for all other groups; the actual order of execution of groups depends on the order of occurrence of triggers.

Definition at line 138 of file `adc_pal.h`.

17.19.2.2 struct adc_config_t

Defines the configuration structure for ADC PAL.

Implements : `adc_config_t_Class`

Definition at line 155 of file `adc_pal.h`.

Data Fields

- const `adc_group_config_t * groupConfigArray`

- uint16_t numGroups
- uint8_t sampleTicks
- void * extension

Field Documentation

17.19.2.2.1 void* extension

This field is used to add extra IP specific settings to the basic configuration.

Definition at line 161 of file adc_pal.h.

17.19.2.2.2 const adc_group_config_t* groupConfigArray

Array of group configurations

Definition at line 157 of file adc_pal.h.

17.19.2.2.3 uint16_t numGroups

Number of elements in groupConfigArray

Definition at line 158 of file adc_pal.h.

17.19.2.2.4 uint8_t sampleTicks

Duration of sample time expressed in ADC clock ticks

Definition at line 160 of file adc_pal.h.

17.19.2.3 struct extension_adc_s32k1xx_t

Defines the extension structure for ADC S32K1xx.

Implements : extension_adc_s32k1xx_t_Class

Definition at line 171 of file adc_pal.h.

Data Fields

- adc_clk_divide_t clockDivide
- adc_resolution_t resolution
- adc_input_clock_t inputClock
- adc_voltage_reference_t voltageRef
- bool supplyMonitoringEnable
- pdb_clk_prescaler_div_t pdbPrescaler

Field Documentation

17.19.2.3.1 adc_clk_divide_t clockDivide

Divider of the input clock for the ADC

Definition at line 173 of file adc_pal.h.

17.19.2.3.2 adc_input_clock_t inputClock

Input clock source

Definition at line 175 of file adc_pal.h.

17.19.2.3.3 pdb_clk_prescaler_div_t pdbPrescaler

PDB clock prescaler. Delays are measured based on PDB clock divided by prescaler. Only relevant if delays are used.

Definition at line 178 of file adc_pal.h.

17.19.2.3.4 **adc_resolution_t** resolution

ADC resolution (8,10,12 bit)

Definition at line 174 of file adc_pal.h.

17.19.2.3.5 **bool** supplyMonitoringEnable

Enable internal supply monitoring

Definition at line 177 of file adc_pal.h.

17.19.2.3.6 **adc_voltage_reference_t** voltageRef

Voltage reference used

Definition at line 176 of file adc_pal.h.

17.19.3 Typedef Documentation

17.19.3.1 **typedef** adc_inputchannel_t adc_input_chan_t

Defines the enumeration with ADC PAL input channels.

Implements : adc_input_chan_t_Class

Definition at line 54 of file adc_pal.h.

17.19.3.2 **typedef** trgmux_trigger_source_t adc_trigger_source_t

Defines the enumeration with ADC PAL hardware trigger sources.

Implements : adc_trigger_source_t_Class

Definition at line 61 of file adc_pal.h.

17.19.4 Enumeration Type Documentation

17.19.4.1 **enum** adc_delay_type_t

Defines an enumeration which contains the types of delay configurations for ADC conversions within a group.

Implements : adc_delay_type_t_Class

Enumerator

ADC_DELAY_TYPE_NO_DELAY First conversion can start right after the trigger occurrence, and the rest of conversions execute one after another

ADC_DELAY_TYPE_GROUP_DELAY Delay only first conversion, and the rest execute one after another

ADC_DELAY_TYPE_INDIVIDUAL_DELAY Individual delay for each conversion in the group (each measured from the occurrence of the trigger)

Definition at line 117 of file adc_pal.h.

17.19.5 Function Documentation

17.19.5.1 **status_t** ADC_Deinit (**const** adc_instance_t *const *instance*)

Deinitializes the ADC PAL instance.

This function resets the ADC PAL instance, including the other platform specific HW units used together with ADC, if there are no active conversions.

Parameters

<i>in</i>	<i>instance</i>	Pointer to ADC PAL instance number structure
-----------	-----------------	--

Returns

status:

- STATUS_BUSY: there is already a HW triggered group enabled or executing, or a SW triggered group executing
- STATUS_BUSY: on MPC574x platforms, if the BCTU module could not be reset
- STATUS_SUCCESS: ADC PAL initialized successfully

Definition at line 338 of file `adc_pal.c`.

17.19.5.2 `status_t ADC_DisableHardwareTrigger (const adc_instance_t *const instance, const uint32_t groupidx, const uint32_t timeout)`

Disables the selected HW trigger for a conversion group, if the conversion group is HW triggered.

This function disables the HW trigger for a configured conversion group and also may stop its execution (depending on platform), if called when a conversion group is executing. If stopping is supported, the execution shall be stopped according to device specific procedures. The function shall wait for the procedures to complete within the given timeout interval and return error code if they do not succeed. : the function prevents new conversions from the group from starting, then waits until the current active conversion finishes execution (if the function call occurred while an ADC conversion from the group is executing) or timeout occurs. : the execution of a HW triggered group of conversions cannot be stopped, so the function shall wait until it is complete or timeout occurs. : the function always returns STATUS_SUCCESS (even if a conversion is still executing) and doesn't use 'timeout' parameter. If it is called during a control cycle, between MRS and actual group conversion start, there will be an additional execution of the group, without callback.

Parameters

<i>in</i>	<i>instance</i>	Pointer to ADC PAL instance number structure
<i>in</i>	<i>groupidx</i>	Index of the selected group configured via groupConfigArray in adc_config_t
<i>in</i>	<i>timeout</i>	Timeout interval in milliseconds

Returns

status:

- STATUS_TIMEOUT: the operation did not complete successfully within the provided timeout interval
- STATUS_SUCCESS: the operation completed successfully within the provided timeout interval

Definition at line 529 of file `adc_pal.c`.

17.19.5.3 `status_t ADC_DisableNotification (const adc_instance_t *const instance, const uint32_t groupidx)`

Disables the notification callback for a configured group.

This function disables the notification callback for a selected group of ADC conversions.

Parameters

<i>in</i>	<i>instance</i>	Pointer to ADC PAL instance number structure
<i>in</i>	<i>groupidx</i>	Index of the selected group configured via groupConfigArray in adc_config_t

Returns

status:

- STATUS_ERROR: the selected group is not active (SW triggered running or HW triggered running or enabled)
- STATUS_SUCCESS: the notification has been disabled successfully

Definition at line 870 of file `adc_pal.c`.

17.19.5.4 `status_t ADC_EnableHardwareTrigger (const adc_instance_t *const instance, const uint32_t groupidx)`

Enables the selected HW trigger for a conversion group, if the conversion group has support for HW trigger.

Enables the selected HW trigger for a conversion group, if the conversion group has support for HW trigger. The function will return an error code if there is a conversion group already active. If the function succeeds, the conversion group will be triggered for execution when the selected HW trigger occurs.

Parameters

in	<i>instance</i>	Pointer to ADC PAL instance number structure
in	<i>groupidx</i>	Index of the selected group configured via groupConfigArray in adc_config_t

Returns

status:

- STATUS_BUSY: there is already a HW triggered group enabled or executing, or a SW triggered group executing
- STATUS_SUCCESS: HW trigger enabled successfully for the selected conversion group

Definition at line 437 of file adc_pal.c.

17.19.5.5 `status_t ADC_EnableNotification (const adc_instance_t *const instance, const uint32_t groupidx)`

Enables the notification callback for a configured group.

This function enables the notification callback for a selected group of ADC conversions.

Parameters

in	<i>instance</i>	Pointer to ADC PAL instance number structure
in	<i>groupidx</i>	Index of the selected group configured via groupConfigArray in adc_config_t

Returns

status:

- STATUS_ERROR: the selected group is not active (SW triggered running or HW triggered running or enabled)
- STATUS_SUCCESS: the notification has been enabled successfully

Definition at line 820 of file adc_pal.c.

17.19.5.6 `status_t ADC_Init (const adc_instance_t *const instance, const adc_config_t *const config)`

Initializes the ADC PAL instance.

This function initializes the ADC PAL instance, including the other platform specific HW units used together with ADC. Notifications are default enabled after init.

Parameters

in	<i>instance</i>	Pointer to ADC PAL instance number structure
in	<i>config</i>	The ADC PAL configuration structure

Returns

status:

- STATUS_ERROR: platform specific error encountered while initializing one of the HW modules used by ADC PAL. On MPC574x returned if ADC calibration did not succeed for all the selected ADCs. On S32K1xx returned if it cannot reconfigure successfully the TRGMUX trigger source of the used PDB instance.
- STATUS_BUSY: on MPC574x platforms, if the BCTU module could not be reset
- STATUS_SUCCESS: ADC PAL initialized successfully

Definition at line 255 of file adc_pal.c.

17.19.5.7 `status_t ADC_StartGroupConversion (const adc_instance_t *const instance, const uint32_t groupidx)`

Starts the execution of a selected SW triggered ADC conversion group.

This function starts execution of a selected ADC conversion group, if there is no other conversion group active. Conversion groups started by `ADC_StartGroupConversion` shall not be preempted by HW triggered conversion groups.

Parameters

in	<i>instance</i>	Pointer to ADC PAL instance number structure
in	<i>groupidx</i>	Index of the selected group configured via groupConfigArray in adc_config_t

Returns

status:

- STATUS_BUSY: there is already a HW triggered group enabled or executing, or a SW triggered group executing
- STATUS_SUCCESS: group conversion successfully triggered

Definition at line 640 of file `adc_pal.c`.

17.19.5.8 `status_t ADC_StopGroupConversion (const adc_instance_t *const instance, const uint32_t groupidx, const uint32_t timeout)`

Stops the selected SW triggered ADC conversion group execution.

This function stops the execution of a SW triggered conversion group. The execution shall be stopped according to device specific procedures. The function shall wait for the procedures to complete within the given timeout interval and return error code if they do not succeed. For `ADC_SAR_CTU` type and `MPC574xC_G_R` a conversion already started for execution cannot be stopped, so the function shall wait until it finishes or timeout occurs.

Parameters

in	<i>instance</i>	Pointer to ADC PAL instance number structure
in	<i>groupidx</i>	Index of the selected group configured via groupConfigArray in adc_config_t
in	<i>timeout</i>	Timeout interval in milliseconds

Returns

status:

- STATUS_TIMEOUT: the operation did not complete successfully within the provided timeout interval
- STATUS_SUCCESS: the operation completed successfully within the provided timeout interval

Definition at line 720 of file `adc_pal.c`.

17.20 Automotive Math and Motor Control Library

Automotive Math and Motor Control Library integration with S32 SDK

General Information

The Automotive Math and Motor Control Library Set is a precompiled off-the-shelf software library containing the building blocks for a wide range of motor control and general mathematical applications. The Automotive Math and Motor Control Library Set is delivered as a precompiled or source code library, and provides production-ready, highly speed-optimized, intensively tested and easy to use solution for the rapid development of user motor control and general mathematical applications. An integral part of the Automotive Math and Motor Control Library Set are the Matlab/Simulink® models of all supported functions to allow modelling of the user application using the Matlab/Simulink® environment, and extensive user documentation. The Automotive Math and Motor Control Library Set support three major arithmetic: 32-bit fixed-point, 16-bit fixed-point and single precision floating-point. For more information, application notes and demos please visit [AMMCLib page](#) from NXP website. AMMCLIB package contains the following:

- **bam** : contains Bit Accurate Models of all the functions for Matlab/Simulink
- **doc** : contains the User Manual
- **include** : contains all the header files, including the master header files of each library to be included in the user application
- **lib** : contains the compiled library file to be included in the user application

Note

For an overview of what is included in the Automotive Math and Motor Control Library and its capabilities you can check the document found in [<SDK_Location>/doc/AMMCLIB_OnePager_S32SDK.pdf](#). This is just a brief description of the Automotive Math and Motor Control Library, for more information please check the full library documentation found in [<SDK_Location>/lib/<CPU_Family>/AMMCLIB/doc/S32K14XMCLUG.pdf](#). The library is provided in binary format, compiled using GCC, GHS, IAR and for evaluation purposes only. Please consult license.txt file for more information found in [<SDK_Location>/lib/<CPU_Family>/AMMCLIB/license.txt](#).

How to use

To add AMMCLib in your application you need to follow four steps:

- 1) Add AMMCLib S32CT component into your project. The component will automatically add the required include paths.
- 2) Add `":S32K14x_AMMCLIB.a"` in Libraries (-l) and add `"${workspace_loc:${ProjName}/SDK/lib/AMMCLIB/lib/<compiler>}"` in Library search path (-L)
- 3) Select the implementations from the AMMCLib component (Fixed 16, Fixed 32 or Float). If you are using the float implementation you need to enable FPU in the toolchain settings.
- 4) Use the library API to execute the required tests.

You can use the AMMCLib examples as a practical implementation of the steps described above.

Note

IAR compiler:

- The compiler is not able to distinguish the sequence of read and write operations inside an inline assembly block in GFLIB_VMin.h and it makes the Warning[Pe549] messages. In that case, C option `"--diag_suppress Pe549"` should be added to suppress those warnings or `"--warnings_are_errors"` should be removed to not treat those warnings as errors.

17.21 Backward Compatibility Symbols for S32K148

This module covers backward compatibility symbols.

17.22 Bank N fail interrupt enable configuration options (0x38/0x48)

17.22.1 Detailed Description

This section lists all the possible options of 0x38/48 registers related to:

- HVIO-N short-circuit interrupt
- HVIO-N open load interrupt

Note

As HVIO bank 0 & 1 has the same memory layout, these macros can be used for Bank 0 & Bank 1 fail interrupt configuration

See also

[UJA113X_SetBankFailInterrupts\(\)](#)

HVIO4/8 short circuit interrupt configuration options (0x38:IO4SCIE[7] / 0x48:IO8SCIE[7])

- #define [IO48SCIE_DISABLE](#) 0x00U
Disable HVIO 4/8 short circuit interrupt.
- #define [IO48SCIE_ENABLE](#) 0x80U
Enable HVIO 4/8 short circuit interrupt.

HVIO4/8 open load interrupt configuration options (0x38:IO4OLIE[6] / 0x48:IO8OLIE[6])

- #define [IO48OLIE_DISABLE](#) 0x00U
Disable HVIO 4/8 open load interrupt.
- #define [IO48OLIE_ENABLE](#) 0x40U
Enable HVIO 4/8 open load interrupt.

HVIO3/7 short circuit interrupt configuration options (0x38:IO3SCIE[5] / 0x48:IO7SCIE[5])

- #define [IO37SCIE_DISABLE](#) 0x00U
Disable HVIO 3/7 short circuit interrupt.
- #define [IO37SCIE_ENABLE](#) 0x20U
Enable HVIO 3/7 short circuit interrupt.

HVIO3/7 open load interrupt configuration options (0x38:IO3OLIE[4] / 0x48:IO7OLIE[4])

- #define [IO37OLIE_DISABLE](#) 0x00U
Disable HVIO 3/7 open load interrupt.
- #define [IO37OLIE_ENABLE](#) 0x10U
Enable HVIO 3/7 open load interrupt.

HVIO2/6 short circuit interrupt configuration options (0x38:IO2SCIE[3] / 0x48:IO6SCIE[3])

- #define [IO26SCIE_DISABLE](#) 0x00U
Disable HVIO 2/6 short circuit interrupt.
- #define [IO26SCIE_ENABLE](#) 0x08U
Enable HVIO 2/6 short circuit interrupt.

HVIO2/6 open load interrupt configuration options (0x38:IO2OLIE[2] / 0x48:IO6OLIE[2])

- `#define IO26OLIE_DISABLE 0x00U`
Disable HVIO 2/6 open load interrupt.
- `#define IO26OLIE_ENABLE 0x04U`
Enable HVIO 2/6 open load interrupt.

HVIO1/5 short circuit interrupt configuration options (0x38:IO1SCIE[1] / 0x48:IO5SCIE[1])

- `#define IO15SCIE_DISABLE 0x00U`
Disable HVIO 1/5 short circuit interrupt.
- `#define IO15SCIE_ENABLE 0x02U`
Enable HVIO 1/5 short circuit interrupt.

HVIO1/5 open load interrupt configuration options (0x38:IO1OLIE[0] / 0x48:IO5OLIE[1])

- `#define IO15OLIE_DISABLE 0x00U`
Disable HVIO 1/5 open load interrupt.
- `#define IO15OLIE_ENABLE 0x01U`
Enable HVIO 1/5 open load interrupt.

17.22.2 Macro Definition Documentation

17.22.2.1 `#define IO15OLIE_DISABLE 0x00U`

Disable HVIO 1/5 open load interrupt.

Definition at line 1037 of file `sbc_uja113x.h`.

17.22.2.2 `#define IO15OLIE_ENABLE 0x01U`

Enable HVIO 1/5 open load interrupt.

Definition at line 1038 of file `sbc_uja113x.h`.

17.22.2.3 `#define IO15SCIE_DISABLE 0x00U`

Disable HVIO 1/5 short circuit interrupt.

Definition at line 1030 of file `sbc_uja113x.h`.

17.22.2.4 `#define IO15SCIE_ENABLE 0x02U`

Enable HVIO 1/5 short circuit interrupt.

Definition at line 1031 of file `sbc_uja113x.h`.

17.22.2.5 `#define IO26OLIE_DISABLE 0x00U`

Disable HVIO 2/6 open load interrupt.

Definition at line 1023 of file `sbc_uja113x.h`.

17.22.2.6 `#define IO26OLIE_ENABLE 0x04U`

Enable HVIO 2/6 open load interrupt.

Definition at line 1024 of file `sbc_uja113x.h`.

17.22.2.7 #define IO26SCIE_DISABLE 0x00U

Disable HVIO 2/6 short circuit interrupt.

Definition at line 1016 of file sbc_uja113x.h.

17.22.2.8 #define IO26SCIE_ENABLE 0x08U

Enable HVIO 2/6 short circuit interrupt.

Definition at line 1017 of file sbc_uja113x.h.

17.22.2.9 #define IO37OLIE_DISABLE 0x00U

Disable HVIO 3/7 open load interrupt.

Definition at line 1009 of file sbc_uja113x.h.

17.22.2.10 #define IO37OLIE_ENABLE 0x10U

Enable HVIO 3/7 open load interrupt.

Definition at line 1010 of file sbc_uja113x.h.

17.22.2.11 #define IO37SCIE_DISABLE 0x00U

Disable HVIO 3/7 short circuit interrupt.

Definition at line 1002 of file sbc_uja113x.h.

17.22.2.12 #define IO37SCIE_ENABLE 0x20U

Enable HVIO 3/7 short circuit interrupt.

Definition at line 1003 of file sbc_uja113x.h.

17.22.2.13 #define IO48OLIE_DISABLE 0x00U

Disable HVIO 4/8 open load interrupt.

Definition at line 995 of file sbc_uja113x.h.

17.22.2.14 #define IO48OLIE_ENABLE 0x40U

Enable HVIO 4/8 open load interrupt.

Definition at line 996 of file sbc_uja113x.h.

17.22.2.15 #define IO48SCIE_DISABLE 0x00U

Disable HVIO 4/8 short circuit interrupt.

Definition at line 988 of file sbc_uja113x.h.

17.22.2.16 #define IO48SCIE_ENABLE 0x80U

Enable HVIO 4/8 short circuit interrupt.

Definition at line 989 of file sbc_uja113x.h.

17.23 Bank N wake-up interrupt enable configuration options (0x37/0x47)

17.23.1 Detailed Description

This section lists all the possible options of 0x37/47 registers related to:

- HVIO-N falling edge interrupt
- HVIO-N rising edge interrupt

Note

As HVIO bank 0 & 1 has the same memory layout, these macros can be used for Bank 0 & Bank 1 wake-up interrupt configuration

See also

[UJA113X_SetBankWupInterrupts\(\)](#)

HVIO4/8 falling edge interrupt configuration options (0x37:IO4FEIE[7]/0x47:IO8FEIE[7])

- #define [IO48FEIE_DISABLE](#) 0x00U
Disable HVIO 4/8 falling edge interrupt.
- #define [IO48FEIE_ENABLE](#) 0x80U
Enable HVIO 4/8 falling edge interrupt.

HVIO4/8 rising edge interrupt configuration options (0x37:IO4REIE[6]/0x47:IO8REIE[6])

- #define [IO48REIE_DISABLE](#) 0x00U
Disable HVIO 4/8 rising edge interrupt.
- #define [IO48REIE_ENABLE](#) 0x40U
Enable HVIO 4/8 rising edge interrupt.

HVIO3/7 falling edge interrupt configuration options (0x37:IO3FEIE[5]/0x47:IO7FEIE[5])

- #define [IO37FEIE_DISABLE](#) 0x00U
Disable HVIO 3/7 falling edge interrupt.
- #define [IO37FEIE_ENABLE](#) 0x20U
Enable HVIO 3/7 falling edge interrupt.

HVIO3/7 rising edge interrupt configuration options (0x37:IO3REIE[4]/0x47:IO7REIE[4])

- #define [IO37REIE_DISABLE](#) 0x00U
Disable HVIO 3/7 rising edge interrupt.
- #define [IO37REIE_ENABLE](#) 0x10U
Enable HVIO 3/7 rising edge interrupt.

HVIO2/6 falling edge interrupt configuration options (0x37:IO2FEIE[3]/0x47:IO6FEIE[3])

- #define [IO26FEIE_DISABLE](#) 0x00U
Disable HVIO 2/6 falling edge interrupt.
- #define [IO26FEIE_ENABLE](#) 0x08U
Enable HVIO 2/6 falling edge interrupt.

HVIO2/6 rising edge interrupt configuration options (0x37:IO2REIE[2]/0x47:IO6[REIE[2]])

- #define `IO26REIE_DISABLE` 0x00U
Disable HVIO 2/6 rising edge interrupt.
- #define `IO26REIE_ENABLE` 0x04U
Enable HVIO 2/6 rising edge interrupt.

HVIO1/5 falling edge interrupt configuration options (0x37:IO1FEIE[1]/0x47:IO5FEIE[1])

- #define `IO15FEIE_DISABLE` 0x00U
Disable HVIO 1/5 falling edge interrupt.
- #define `IO15FEIE_ENABLE` 0x02U
Enable HVIO 1/5 falling edge interrupt.

HVIO1/5 rising edge interrupt configuration options (0x37:IO1REIE[0]/0x47:IO1REIE[0])

- #define `IO15REIE_DISABLE` 0x00U
Disable HVIO 1/5 rising edge interrupt.
- #define `IO15REIE_ENABLE` 0x01U
Enable HVIO 1/5 rising edge interrupt.

17.23.2 Macro Definition Documentation

17.23.2.1 #define `IO15FEIE_DISABLE` 0x00U

Disable HVIO 1/5 falling edge interrupt.

Definition at line 957 of file `sbc_uja113x.h`.

17.23.2.2 #define `IO15FEIE_ENABLE` 0x02U

Enable HVIO 1/5 falling edge interrupt.

Definition at line 958 of file `sbc_uja113x.h`.

17.23.2.3 #define `IO15REIE_DISABLE` 0x00U

Disable HVIO 1/5 rising edge interrupt.

Definition at line 964 of file `sbc_uja113x.h`.

17.23.2.4 #define `IO15REIE_ENABLE` 0x01U

Enable HVIO 1/5 rising edge interrupt.

Definition at line 965 of file `sbc_uja113x.h`.

17.23.2.5 #define `IO26FEIE_DISABLE` 0x00U

Disable HVIO 2/6 falling edge interrupt.

Definition at line 943 of file `sbc_uja113x.h`.

17.23.2.6 #define `IO26FEIE_ENABLE` 0x08U

Enable HVIO 2/6 falling edge interrupt.

Definition at line 944 of file `sbc_uja113x.h`.

17.23.2.7 #define IO26REIE_DISABLE 0x00U

Disable HVIO 2/6 rising edge interrupt.

Definition at line 950 of file sbc_uja113x.h.

17.23.2.8 #define IO26REIE_ENABLE 0x04U

Enable HVIO 2/6 rising edge interrupt.

Definition at line 951 of file sbc_uja113x.h.

17.23.2.9 #define IO37FEIE_DISABLE 0x00U

Disable HVIO 3/7 falling edge interrupt.

Definition at line 929 of file sbc_uja113x.h.

17.23.2.10 #define IO37FEIE_ENABLE 0x20U

Enable HVIO 3/7 falling edge interrupt.

Definition at line 930 of file sbc_uja113x.h.

17.23.2.11 #define IO37REIE_DISABLE 0x00U

Disable HVIO 3/7 rising edge interrupt.

Definition at line 936 of file sbc_uja113x.h.

17.23.2.12 #define IO37REIE_ENABLE 0x10U

Enable HVIO 3/7 rising edge interrupt.

Definition at line 937 of file sbc_uja113x.h.

17.23.2.13 #define IO48FEIE_DISABLE 0x00U

Disable HVIO 4/8 falling edge interrupt.

Definition at line 915 of file sbc_uja113x.h.

17.23.2.14 #define IO48FEIE_ENABLE 0x80U

Enable HVIO 4/8 falling edge interrupt.

Definition at line 916 of file sbc_uja113x.h.

17.23.2.15 #define IO48REIE_DISABLE 0x00U

Disable HVIO 4/8 rising edge interrupt.

Definition at line 922 of file sbc_uja113x.h.

17.23.2.16 #define IO48REIE_ENABLE 0x40U

Enable HVIO 4/8 rising edge interrupt.

Definition at line 923 of file sbc_uja113x.h.

17.24 CRC Driver

17.24.1 Detailed Description

Cyclic Redundancy Check Peripheral Driver.

This section describes the programming interface of the CRC driver.

Data Structures

- struct [crc_user_config_t](#)
CRC configuration structure. Implements : [crc_user_config_t_Class](#). [More...](#)

Enumerations

- enum [crc_transpose_t](#) { [CRC_TRANSPOSE_NONE](#) = 0x00U, [CRC_TRANSPOSE_BITS](#) = 0x01U, [CRC_TRANSPOSE_BITS_AND_BYTES](#) = 0x02U, [CRC_TRANSPOSE_BYTES](#) = 0x03U }
- CRC type of transpose of read write data Implements : [crc_transpose_t_Class](#).

CRC DRIVER API

- status_t [CRC_DRV_Init](#) (uint32_t instance, const [crc_user_config_t](#) *userConfigPtr)
Initializes the CRC module.
- status_t [CRC_DRV_Deinit](#) (uint32_t instance)
Sets the default configuration.
- uint32_t [CRC_DRV_GetCrc32](#) (uint32_t instance, uint32_t data, bool newSeed, uint32_t seed)
Appends 32-bit data to the current CRC calculation and returns new result.
- uint32_t [CRC_DRV_GetCrc16](#) (uint32_t instance, uint16_t data, bool newSeed, uint32_t seed)
Appends 16-bit data to the current CRC calculation and returns new result.
- uint32_t [CRC_DRV_GetCrc8](#) (uint32_t instance, uint8_t data, bool newSeed, uint32_t seed)
Appends 8-bit data to the current CRC calculation and returns new result.
- void [CRC_DRV_WriteData](#) (uint32_t instance, const uint8_t *data, uint32_t dataSize)
Appends a block of bytes to the current CRC calculation.
- uint32_t [CRC_DRV_GetCrcResult](#) (uint32_t instance)
Returns the current result of the CRC calculation.
- status_t [CRC_DRV_Configure](#) (uint32_t instance, const [crc_user_config_t](#) *userConfigPtr)
Configures the CRC module from a user configuration structure.
- status_t [CRC_DRV_GetConfig](#) (uint32_t instance, [crc_user_config_t](#) *const userConfigPtr)
Get configures of the CRC module currently.
- status_t [CRC_DRV_GetDefaultConfig](#) ([crc_user_config_t](#) *const userConfigPtr)
Get default configures the CRC module for configuration structure.

17.24.2 Data Structure Documentation

17.24.2.1 struct [crc_user_config_t](#)

CRC configuration structure. Implements : [crc_user_config_t_Class](#).

Definition at line 83 of file [crc_driver.h](#).

Data Fields

- [crc_transpose_t](#) writeTranspose
- bool complementChecksum
- uint32_t seed

Field Documentation

17.24.2.1.1 `bool complementChecksum`

True if the result shall be complement of the actual checksum.

Definition at line 95 of file `crc_driver.h`.

17.24.2.1.2 `uint32_t seed`

Starting checksum value.

Definition at line 96 of file `crc_driver.h`.

17.24.2.1.3 `crc_transpose_t writeTranspose`

Type of transpose when writing CRC input data.

Definition at line 94 of file `crc_driver.h`.

17.24.3 Enumeration Type Documentation

17.24.3.1 `enum crc_transpose_t`

CRC type of transpose of read write data Implements : `crc_transpose_t_Class`.

Enumerator

`CRC_TRANSPOSE_NONE` No transpose

`CRC_TRANSPOSE_BITS` Transpose bits in bytes

`CRC_TRANSPOSE_BITS_AND_BYTES` Transpose bytes and bits in bytes

`CRC_TRANSPOSE_BYTES` Transpose bytes

Definition at line 44 of file `crc_driver.h`.

17.24.4 Function Documentation

17.24.4.1 `status_t CRC_DRV_Configure (uint32_t instance, const crc_user_config_t * userConfigPtr)`

Configures the CRC module from a user configuration structure.

This function configures the CRC module from a user configuration structure

Parameters

<code>in</code>	<code>instance</code>	The CRC instance number
<code>in</code>	<code>userConfigPtr</code>	Pointer to structure of initialization

Returns

Execution status (success)

Definition at line 236 of file `crc_driver.c`.

17.24.4.2 `status_t CRC_DRV_Deinit (uint32_t instance)`

Sets the default configuration.

This function sets the default configuration

Parameters

in	<i>instance</i>	The CRC instance number
----	-----------------	-------------------------

Returns

Execution status (success)

Definition at line 88 of file `crc_driver.c`.

17.24.4.3 `status_t CRC_DRV_GetConfig (uint32_t instance, crc_user_config_t *const userConfigPtr)`

Get configures of the CRC module currently.

This function Get configures of the CRC module currently

Parameters

in	<i>instance</i>	The CRC instance number
out	<i>userConfigPtr</i>	Pointer to structure of initialization

Returns

Execution status (success)

Definition at line 268 of file `crc_driver.c`.

17.24.4.4 `uint32_t CRC_DRV_GetCrc16 (uint32_t instance, uint16_t data, bool newSeed, uint32_t seed)`

Appends 16-bit data to the current CRC calculation and returns new result.

This function appends 16-bit data to the current CRC calculation and returns new result. If the `newSeed` is true, seed set and result are calculated from the seed new value (new CRC calculation)

Parameters

in	<i>instance</i>	The CRC instance number
in	<i>data</i>	Input data for CRC calculation
in	<i>newSeed</i>	Sets new CRC calculation <ul style="list-style-type: none"> • true: New seed set and used for new calculation. • false: Seed argument ignored, continues old calculation.
in	<i>seed</i>	New seed if <code>newSeed</code> is true, else ignored

Returns

New CRC result

Definition at line 139 of file `crc_driver.c`.

17.24.4.5 `uint32_t CRC_DRV_GetCrc32 (uint32_t instance, uint32_t data, bool newSeed, uint32_t seed)`

Appends 32-bit data to the current CRC calculation and returns new result.

This function appends 32-bit data to the current CRC calculation and returns new result. If the `newSeed` is true, seed set and result are calculated from the seed new value (new CRC calculation)

Parameters

in	<i>instance</i>	The CRC instance number
in	<i>data</i>	Input data for CRC calculation
in	<i>newSeed</i>	Sets new CRC calculation <ul style="list-style-type: none"> • true: New seed set and used for new calculation. • false: Seed argument ignored, continues old calculation.
in	<i>seed</i>	New seed if newSeed is true, else ignored

Returns

New CRC result

Definition at line 108 of file `crc_driver.c`.

17.24.4.6 `uint32_t CRC_DRV_GetCrc8 (uint32_t instance, uint8_t data, bool newSeed, uint32_t seed)`

Appends 8-bit data to the current CRC calculation and returns new result.

This function appends 8-bit data to the current CRC calculation and returns new result. If the newSeed is true, seed set and result are calculated from the seed new value (new CRC calculation)

Parameters

in	<i>instance</i>	The CRC instance number
in	<i>data</i>	Input data for CRC calculation
in	<i>newSeed</i>	Sets new CRC calculation <ul style="list-style-type: none"> • true: New seed set and used for new calculation. • false: Seed argument ignored, continues old calculation.
in	<i>seed</i>	New seed if newSeed is true, else ignored

Returns

New CRC result

Definition at line 169 of file `crc_driver.c`.

17.24.4.7 `uint32_t CRC_DRV_GetCrcResult (uint32_t instance)`

Returns the current result of the CRC calculation.

This function returns the current result of the CRC calculation

Parameters

in	<i>instance</i>	The CRC instance number
----	-----------------	-------------------------

Returns

Result of CRC calculation

Definition at line 220 of file `crc_driver.c`.

17.24.4.8 `status_t CRC_DRV_GetDefaultConfig (crc_user_config_t *const userConfigPtr)`

Get default configures the CRC module for configuration structure.

This function Get default configures the CRC module for user configuration structure

Parameters

out	<i>userConfigPtr</i>	Pointer to structure of initialization
-----	----------------------	--

Returns

Execution status (success)

Definition at line 300 of file `crc_driver.c`.

17.24.4.9 `status_t CRC_DRV_Init (uint32_t instance, const crc_user_config_t * userConfigPtr)`

Initializes the CRC module.

This function initializes CRC driver based on user configuration input. The user must make sure that the clock is enabled

Parameters

in	<i>instance</i>	The CRC instance number
in	<i>userConfigPtr</i>	Pointer to structure of initialization

Returns

Execution status (success)

Definition at line 65 of file `crc_driver.c`.

17.24.4.10 `void CRC_DRV_WriteData (uint32_t instance, const uint8_t * data, uint32_t dataSize)`

Appends a block of bytes to the current CRC calculation.

This function appends a block of bytes to the current CRC calculation

Parameters

in	<i>instance</i>	The CRC instance number
in	<i>data</i>	Data for current CRC calculation
in	<i>dataSize</i>	Length of data to be calculated

Definition at line 197 of file `crc_driver.c`.

17.25 CSEc Driver

17.25.1 Detailed Description

Cryptographic Services Engine Peripheral Driver.

How to use the CSEc driver in your application

To access the command feature set, the part must be configured for EEE operation, using the PGMPART command. This can be implemented by using the Flash driver. By enabling security features and configuring a number of user keys, the total size of the 4 KByte EEERAM will be reduced by the space required to store the user keys. The user key space will then effectively be unaddressable space in the EEERAM.

At the bottom of this page is an example of making this configuration using the Flash driver. For more details related to the FLASH_DRV_DEFlashPartition function, please refer to the Flash driver documentation. Please note that this configuration is required only once and should not be launched from Flash memory.

In order to use the CSEc driver in your application, the **CSEC_DRV_Init** function should be called prior to using the rest of the API. The parameter of this function is used for holding the internal state of the driver throughout the lifetime of the application.

Key/seed/random number generation

This is the high level flow in which to initialize and generate random numbers.

1. Run **CSEC_DRV_InitTRNG** to initialize a random seed from the internal TRNG
 - **CSEC_DRV_InitTRNG** must be run after every POR, and before the first execution of **CSEC_DRV_GenerateRND**
 - Note that if the next step (run **CSEC_DRV_GenerateRND**) is run without initializing the seed, **CSEC_DRV_RNG_SEED** will be returned.
2. Run **CSEC_DRV_GenerateRND** to generate a random number. The PRNG uses the PRNG_STATE/KEY and Seed per SHE spec and the AIS20 standard.
3. For additional random numbers the user may continue executing **CSEC_DRV_GenerateRND** unless a POR event occurred.

Memory update protocol

In order to update a key, the user must have knowledge of a valid authentication secret, i.e. another key (AuthID). If the key AuthID is empty, the key update will only work if AuthID = ID (the key that will be updated will represent the AuthID from now on), otherwise **CSEC_KEY_EMPTY** is returned.

The M1-M3 values need to be computed according to the SHE Specification in order to update a key slot. The **CSEC_DRV_LoadKey** function will require those values. After successfully updating the key slot, two verification values will be returned: M4 and M5. The user can compute the two values and compare them with the ones returned by the **CSEC_DRV_LoadKey** function in order to ensure the slot was updated as desired. Please refer to the CSEc driver example for a reference implementation of the memory update protocol.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\drivers\src\csec\csec_driver.c
{S32SDK_PATH}\platform\drivers\src\csec\csec_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\drivers\inc\
```

Preprocessor symbols

No special symbols are required for this component

Important Note

While executing CSEC_DRV_GenerateMACAddrMode and CSEC_DRV_VerifyMACAddrMode functions, it is not possible to execute code from the FLASH block targeted by the current operation. This includes interrupt handlers for any interrupt that might occur during this time. It is the responsibility of the application to ensure that any such code is placed in a different FLASH block or in RAM. Functions can be placed in RAM section by using the START/END_FUNCTION_DEFINITION/DECLARATION_RAMSECTION macros.

Dependencies

Interrupt Manager (Interrupt) OS Interface (OSIF)

Examples:

Using the Flash driver to partition Flash for CSEc operation, the below code section applies for S32K14x:

```
flash_ssd_config_t flashSSDConfig;

FLASH_DRV_Init(&flashl_InitConfig0, &flashSSDConfig);

/* Configure the part for EEE operation, with 20 keys for CSEc */
FLASH_DRV_DEFlashPartition(&flashSSDConfig, 0x2, 0x4, 0x3, false, true);
```

The example partition code for S32K11x:

```
flash_ssd_config_t flashSSDConfig;

FLASH_DRV_Init(&flashl_InitConfig0, &flashSSDConfig);

/* Configure the part for EEE operation, with 20 keys for CSEc */
FLASH_DRV_DEFlashPartition(&flashSSDConfig, 0x3, 0x3, 0x3, false, true);
```

Encryption using AES EBC mode

```
uint8_t plainText[16] = {0x00, 0x11, 0x22, 0x33, 0x44, 0x55, 0x66, 0x77, 0x88,
    0x99, 0xAA, 0xBB, 0xCC, 0xDD, 0xEE, 0xFF};
uint8_t plainKey[16] = {0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08,
    0x09, 0x0a, 0x0b, 0x0c, 0x0d, 0x0e, 0x0f};

csec_error_code_t stat;
uint8_t cipherText[16];

csec_state_t csecState;

CSEC_DRV_Init(&csecState);

stat = CSEC_DRV_LoadPlainKey(plainKey);
if (stat != CSEC_NO_ERROR)
{
    /* Loading the key failed, encryption will not have the expected result */
    return false;
}

stat = CSEC_DRV_EncryptECB(CSEC_RAM_KEY, plainText, 16U, cipherText, 1U);
if (stat != CSEC_NO_ERROR)
{
    /* Encryption was successful */
    return true;
}
```

Generating and verifying CMAC for a message

```
uint8_t plainKey[16] = {0x2b, 0x7e, 0x15, 0x16, 0x28, 0xae, 0xd2, 0xa6, 0xab,
    0xf7, 0x15, 0x88, 0x09, 0xcf, 0x4f, 0x3c};
uint8_t msg[16] = {0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08,
    0x09, 0x0a, 0x0b, 0x0c, 0x0d, 0x0e, 0x0f};
uint8_t cmac[16];
bool verifStatus;
csec_error_code_t stat;
```

```

csec_state_t csecState;

CSEC_DRV_Init(&csecState);

stat = CSEC_DRV_LoadPlainKey(plainKey);
if (stat != CSEC_NO_ERROR)
    return false;

stat = CSEC_DRV_GenerateMAC(CSEC_RAM_KEY, msg, 128U, cmac, 1U);
if (stat != CSEC_NO_ERROR)
    return false;

stat = CSEC_DRV_VerifyMAC(CSEC_RAM_KEY, msg, 128U, cmac, 128U, &verifStatus,
    1U);
if (stat != CSEC_NO_ERROR)
    return false;

if (!verifStatus)
{
    /* The given CMAC did not matched with the one computed internally */
    return false;
}

```

Generating random bits

```

csec_error_code_t stat;
csec_status_t status;
uint8_t rnd[16];

csec_state_t csecState;

CSEC_DRV_Init(&csecState);

stat = CSEC_DRV_InitRNG();
if (stat != CSEC_NO_ERROR)
    return false;

/* Check RNG is initialized */
status = CSEC_DRV_GetStatus();
if (!(status & CSEC_STATUS_RND_INIT))
    return false;

stat = CSEC_DRV_GenerateRND(rnd);
if (stat != CSEC_NO_ERROR)
    return false;

```

Data Structures

- struct `csec_state_t`
Internal driver state information. [More...](#)

Macros

- #define `CSEC_STATUS_BUSY` (0x1U)
The bit is set whenever SHE is processing a command.
- #define `CSEC_STATUS_SECURE_BOOT` (0x2U)
The bit is set if the secure booting is activated.
- #define `CSEC_STATUS_BOOT_INIT` (0x4U)
The bit is set if the secure booting has been personalized during the boot sequence.
- #define `CSEC_STATUS_BOOT_FINISHED` (0x8U)
The bit is set when the secure booting has been finished by calling either `CMD_BOOT_FAILURE` or `CMD_BOOT_OK` or if `CMD_SECURE_BOOT` failed in verifying `BOOT_MAC`.
- #define `CSEC_STATUS_BOOT_OK` (0x10U)
The bit is set if the secure booting (`CMD_SECURE_BOOT`) succeeded. If `CMD_BOOT_FAILURE` is called the bit is erased.
- #define `CSEC_STATUS_RND_INIT` (0x20U)
The bit is set if the random number generator has been initialized.
- #define `CSEC_STATUS_EXT_DEBUGGER` (0x40U)

The bit is set if an external debugger is connected to the chip.

- #define `CSEC_STATUS_INT_DEBUGGER` (0x80U)

The bit is set if the internal debugging mechanisms of SHE are activated.

Typedefs

- typedef uint8_t `csec_status_t`

Represents the status of the CSEc module. Provides one bit for each status code as per SHE specification. `CSEC_STATUS_*` masks can be used for verifying the status.

Enumerations

- enum `csec_key_id_t` {
`CSEC_SECRET_KEY` = 0x0U, `CSEC_MASTER_ECU`, `CSEC_BOOT_MAC_KEY`, `CSEC_BOOT_MAC`,
`CSEC_KEY_1`, `CSEC_KEY_2`, `CSEC_KEY_3`, `CSEC_KEY_4`,
`CSEC_KEY_5`, `CSEC_KEY_6`, `CSEC_KEY_7`, `CSEC_KEY_8`,
`CSEC_KEY_9`, `CSEC_KEY_10`, `CSEC_RAM_KEY` = 0xFU, `CSEC_KEY_11` = 0x14U,
`CSEC_KEY_12`, `CSEC_KEY_13`, `CSEC_KEY_14`, `CSEC_KEY_15`,
`CSEC_KEY_16`, `CSEC_KEY_17` }

Specify the KeyID to be used to implement the requested cryptographic operation.

- enum `csec_cmd_t` {
`CSEC_CMD_ENC_ECB` = 0x1U, `CSEC_CMD_ENC_CBC`, `CSEC_CMD_DEC_ECB`, `CSEC_CMD_DEC_CBC`,
`CSEC_CMD_GENERATE_MAC`, `CSEC_CMD_VERIFY_MAC`, `CSEC_CMD_LOAD_KEY`, `CSEC_CMD_LOAD_PLAIN_KEY`,
`CSEC_CMD_EXPORT_RAM_KEY`, `CSEC_CMD_INIT_RNG`, `CSEC_CMD_EXTEND_SEED`, `CSEC_CMD_D_RND`,
`CSEC_CMD_RESERVED_1`, `CSEC_CMD_BOOT_FAILURE`, `CSEC_CMD_BOOT_OK`, `CSEC_CMD_GET_ID`,
`CSEC_CMD_BOOT_DEFINE`, `CSEC_CMD_DBG_CHAL`, `CSEC_CMD_DBG_AUTH`, `CSEC_CMD_RESERVED_2`,
`CSEC_CMD_RESERVED_3`, `CSEC_CMD_MP_COMPRESS` }

CSEc commands which follow the same values as the SHE command definition.

- enum `csec_call_sequence_t` { `CSEC_CALL_SEQ_FIRST`, `CSEC_CALL_SEQ_SUBSEQUENT` }

Specifies if the information is the first or a following function call.

- enum `csec_boot_flavor_t` { `CSEC_BOOT_STRICT`, `CSEC_BOOT_SERIAL`, `CSEC_BOOT_PARALLEL`, `CSEC_BOOT_NOT_DEFINED` }

Specifies the boot type for the `BOOT_DEFINE` command.

Functions

- void `CSEC_DRV_Init` (`csec_state_t` *state)
 Initializes the internal state of the driver and enables the FTFC interrupt.
- void `CSEC_DRV_Deinit` (void)
 Clears the internal state of the driver and disables the FTFC interrupt.
- status_t `CSEC_DRV_EncryptECB` (`csec_key_id_t` keyId, const uint8_t *plainText, uint32_t length, uint8_t *cipherText, uint32_t timeout)
 Performs the AES-128 encryption in ECB mode.
- status_t `CSEC_DRV_DecryptECB` (`csec_key_id_t` keyId, const uint8_t *cipherText, uint32_t length, uint8_t *plainText, uint32_t timeout)
 Performs the AES-128 decryption in ECB mode.
- status_t `CSEC_DRV_EncryptCBC` (`csec_key_id_t` keyId, const uint8_t *plainText, uint32_t length, const uint8_t *iv, uint8_t *cipherText, uint32_t timeout)

- Performs the AES-128 encryption in CBC mode.*

 - status_t [CSEC_DRV_DecryptCBC](#) (csec_key_id_t keyId, const uint8_t *cipherText, uint32_t length, const uint8_t *iv, uint8_t *plainText, uint32_t timeout)
- Performs the AES-128 decryption in CBC mode.*

 - status_t [CSEC_DRV_GenerateMAC](#) (csec_key_id_t keyId, const uint8_t *msg, uint32_t msgLen, uint8_t *mac, uint32_t timeout)
- Calculates the MAC of a given message using CMAC with AES-128.*

 - status_t [CSEC_DRV_GenerateMACAddrMode](#) (csec_key_id_t keyId, const uint8_t *msg, uint32_t msgLen, uint8_t *mac)
- Calculates the MAC of a given message (located in Flash) using CMAC with AES-128.*

 - status_t [CSEC_DRV_VerifyMAC](#) (csec_key_id_t keyId, const uint8_t *msg, uint32_t msgLen, const uint8_t *mac, uint16_t macLen, bool *verifStatus, uint32_t timeout)
- Verifies the MAC of a given message using CMAC with AES-128.*

 - status_t [CSEC_DRV_VerifyMACAddrMode](#) (csec_key_id_t keyId, const uint8_t *msg, uint32_t msgLen, const uint8_t *mac, uint16_t macLen, bool *verifStatus)
- Verifies the MAC of a given message (located in Flash) using CMAC with AES-128.*

 - status_t [CSEC_DRV_LoadKey](#) (csec_key_id_t keyId, const uint8_t *m1, const uint8_t *m2, const uint8_t *m3, uint8_t *m4, uint8_t *m5)
- Updates an internal key per the SHE specification.*

 - status_t [CSEC_DRV_LoadPlainKey](#) (const uint8_t *plainKey)
- Updates the RAM key memory slot with a 128-bit plaintext.*

 - status_t [CSEC_DRV_ExportRAMKey](#) (uint8_t *m1, uint8_t *m2, uint8_t *m3, uint8_t *m4, uint8_t *m5)
- Exports the RAM_KEY into a format protected by SECRET_KEY.*

 - status_t [CSEC_DRV_InitRNG](#) (void)
- Initializes the seed and derives a key for the PRNG.*

 - status_t [CSEC_DRV_ExtendSeed](#) (const uint8_t *entropy)
- Extends the seed of the PRNG.*

 - status_t [CSEC_DRV_GenerateRND](#) (uint8_t *rnd)
- Generates a vector of 128 random bits.*

 - status_t [CSEC_DRV_BootFailure](#) (void)
- Signals a failure detected during later stages of the boot process.*

 - status_t [CSEC_DRV_BootOK](#) (void)
- Marks a successful boot verification during later stages of the boot process.*

 - status_t [CSEC_DRV_BootDefine](#) (uint32_t bootSize, csec_boot_flavor_t bootFlavor)
- Implements an extension of the SHE standard to define both the user boot size and boot method.*

 - static csec_status_t [CSEC_DRV_GetStatus](#) (void)
- Returns the content of the status register.*

 - status_t [CSEC_DRV_GetID](#) (const uint8_t *challenge, uint8_t *uid, uint8_t *sreg, uint8_t *mac)
- Returns the identity (UID) and the value of the status register protected by a MAC over a challenge and the data.*

 - status_t [CSEC_DRV_DbgChal](#) (uint8_t *challenge)
- Obtains a random number which the user shall use along with the MASTER_ECU_KEY and UID to return an authorization request.*

 - status_t [CSEC_DRV_DbgAuth](#) (const uint8_t *authorization)
- Erases all keys (actual and outdated) stored in NVM Memory if the authorization is confirmed by CSEc.*

 - status_t [CSEC_DRV_MPCompress](#) (const uint8_t *msg, uint16_t msgLen, uint8_t *mpCompress, uint32_t timeout)
- Compresses the given messages by accessing the Miyaguchi-Prenell compression feature with in the CSEc feature set.*

 - status_t [CSEC_DRV_EncryptECBAsync](#) (csec_key_id_t keyId, const uint8_t *plainText, uint32_t length, uint8_t *cipherText)
- Asynchronously performs the AES-128 encryption in ECB mode.*

- status_t [CSEC_DRV_DecryptECBAsync](#) (csec_key_id_t keyId, const uint8_t *cipherText, uint32_t length, uint8_t *plainText)
Asynchronously performs the AES-128 decryption in ECB mode.
- status_t [CSEC_DRV_EncryptCBCAsync](#) (csec_key_id_t keyId, const uint8_t *plainText, uint32_t length, const uint8_t *iv, uint8_t *cipherText)
Asynchronously performs the AES-128 encryption in CBC mode.
- status_t [CSEC_DRV_DecryptCBCAsync](#) (csec_key_id_t keyId, const uint8_t *cipherText, uint32_t length, const uint8_t *iv, uint8_t *plainText)
Asynchronously performs the AES-128 decryption in CBC mode.
- status_t [CSEC_DRV_GenerateMACAsync](#) (csec_key_id_t keyId, const uint8_t *msg, uint32_t msgLen, uint8_t *cmac)
Asynchronously calculates the MAC of a given message using CMAC with AES-128.
- status_t [CSEC_DRV_VerifyMACAsync](#) (csec_key_id_t keyId, const uint8_t *msg, uint32_t msgLen, const uint8_t *mac, uint16_t macLen, bool *verifStatus)
Asynchronously verifies the MAC of a given message using CMAC with AES-128.
- status_t [CSEC_DRV_GetAsyncCmdStatus](#) (void)
Checks the status of the execution of an asynchronous command.
- void [CSEC_DRV_InstallCallback](#) (security_callback_t callbackFunc, void *callbackParam)
Installs a callback function which will be invoked when an asynchronous command finishes its execution.
- void [CSEC_DRV_CancelCommand](#) (void)
Cancels a previously launched asynchronous command.

17.25.2 Data Structure Documentation

17.25.2.1 struct csec_state_t

Internal driver state information.

Note

The contents of this structure are internal to the driver and should not be modified by users. Also, contents of the structure are subject to change in future releases.

Implements : csec_state_t_Class

Definition at line 183 of file csec_driver.h.

Data Fields

- bool [cmdInProgress](#)
- [csec_cmd_t](#) cmd
- const uint8_t * [inputBuff](#)
- uint8_t * [outputBuff](#)
- uint32_t [index](#)
- uint32_t [fullSize](#)
- uint32_t [partSize](#)
- [csec_key_id_t](#) keyId
- status_t [errCode](#)
- const uint8_t * [iv](#)
- [csec_call_sequence_t](#) seq
- uint32_t [msgLen](#)
- bool * [verifStatus](#)
- bool [macWritten](#)
- const uint8_t * [mac](#)
- uint32_t [macLen](#)
- security_callback_t [callback](#)
- void * [callbackParam](#)

Field Documentation

17.25.2.1.1 `security_callback_t callback`

The callback invoked when an asynchronous command is completed

Definition at line 200 of file `csec_driver.h`.

17.25.2.1.2 `void* callbackParam`

User parameter for the command completion callback

Definition at line 201 of file `csec_driver.h`.

17.25.2.1.3 `csec_cmd_t cmd`

Specifies the type of the command in execution

Definition at line 185 of file `csec_driver.h`.

17.25.2.1.4 `bool cmdInProgress`

Specifies if a command is in progress

Definition at line 184 of file `csec_driver.h`.

17.25.2.1.5 `status_t errCode`

Specifies the error code of the last executed command

Definition at line 192 of file `csec_driver.h`.

17.25.2.1.6 `uint32_t fullSize`

Specifies the size of the input of the command in execution

Definition at line 189 of file `csec_driver.h`.

17.25.2.1.7 `uint32_t index`

Specifies the index in the input buffer of the command in execution

Definition at line 188 of file `csec_driver.h`.

17.25.2.1.8 `const uint8_t* inputBuff`

Specifies the input of the command in execution

Definition at line 186 of file `csec_driver.h`.

17.25.2.1.9 `const uint8_t* iv`

Specifies the IV of the command in execution (for encryption/decryption using CBC mode)

Definition at line 193 of file `csec_driver.h`.

17.25.2.1.10 `csec_key_id_t keyId`

Specifies the key used for the command in execution

Definition at line 191 of file `csec_driver.h`.

17.25.2.1.11 `const uint8_t* mac`

Specifies the MAC to be verified for a MAC verification command

Definition at line 198 of file `csec_driver.h`.

17.25.2.1.12 uint32_t macLen

Specifies the number of bits of the MAC to be verified for a MAC verification command

Definition at line 199 of file csec_driver.h.

17.25.2.1.13 bool macWritten

Specifies if the MAC to be verified was written in CSE_PRAM for a MAC verification command

Definition at line 197 of file csec_driver.h.

17.25.2.1.14 uint32_t msgLen

Specifies the message size (in bits) for the command in execution (for MAC generation/verification)

Definition at line 195 of file csec_driver.h.

17.25.2.1.15 uint8_t* outputBuff

Specifies the output of the command in execution

Definition at line 187 of file csec_driver.h.

17.25.2.1.16 uint32_t partSize

Specifies the size of the chunk of the input currently processed

Definition at line 190 of file csec_driver.h.

17.25.2.1.17 csec_call_sequence_t seq

Specifies if the information is the first or a following function call.

Definition at line 194 of file csec_driver.h.

17.25.2.1.18 bool* verifStatus

Specifies the result of the last executed MAC verification command

Definition at line 196 of file csec_driver.h.

17.25.3 Macro Definition Documentation**17.25.3.1 #define CSEC_STATUS_BOOT_FINISHED (0x8U)**

The bit is set when the secure booting has been finished by calling either CMD_BOOT_FAILURE or CMD_BOOT_OK or if CMD_SECURE_BOOT failed in verifying BOOT_MAC.

Definition at line 70 of file csec_driver.h.

17.25.3.2 #define CSEC_STATUS_BOOT_INIT (0x4U)

The bit is set if the secure booting has been personalized during the boot sequence.

Definition at line 66 of file csec_driver.h.

17.25.3.3 #define CSEC_STATUS_BOOT_OK (0x10U)

The bit is set if the secure booting (CMD_SECURE_BOOT) succeeded. If CMD_BOOT_FAILURE is called the bit is erased.

Definition at line 73 of file csec_driver.h.

17.25.3.4 `#define CSEC_STATUS_BUSY (0x1U)`

The bit is set whenever SHE is processing a command.

Definition at line 61 of file `csec_driver.h`.

17.25.3.5 `#define CSEC_STATUS_EXT_DEBUGGER (0x40U)`

The bit is set if an external debugger is connected to the chip.

Definition at line 77 of file `csec_driver.h`.

17.25.3.6 `#define CSEC_STATUS_INT_DEBUGGER (0x80U)`

The bit is set if the internal debugging mechanisms of SHE are activated.

Definition at line 80 of file `csec_driver.h`.

17.25.3.7 `#define CSEC_STATUS_RND_INIT (0x20U)`

The bit is set if the random number generator has been initialized.

Definition at line 75 of file `csec_driver.h`.

17.25.3.8 `#define CSEC_STATUS_SECURE_BOOT (0x2U)`

The bit is set if the secure booting is activated.

Definition at line 63 of file `csec_driver.h`.

17.25.4 Typedef Documentation

17.25.4.1 `typedef uint8_t csec_status_t`

Represents the status of the CSEc module. Provides one bit for each status code as per SHE specification. CSE↔
C_STATUS_* masks can be used for verifying the status.

Implements : `csec_status_t_Class`

Definition at line 89 of file `csec_driver.h`.

17.25.5 Enumeration Type Documentation

17.25.5.1 `enum csec_boot_flavor_t`

Specifies the boot type for the BOOT_DEFINE command.

Implements : `csec_boot_flavor_t_Class`

Enumerator

`CSEC_BOOT_STRICT`

`CSEC_BOOT_SERIAL`

`CSEC_BOOT_PARALLEL`

`CSEC_BOOT_NOT_DEFINED`

Definition at line 167 of file `csec_driver.h`.

17.25.5.2 `enum csec_call_sequence_t`

Specifies if the information is the first or a following function call.

Implements : `csec_call_sequence_t_Class`

Enumerator

CSEC_CALL_SEQ_FIRST
CSEC_CALL_SEQ_SUBSEQUENT

Definition at line 157 of file csec_driver.h.

17.25.5.3 enum csec_cmd_t

CSEc commands which follow the same values as the SHE command definition.

Implements : csec_cmd_t_Class

Enumerator

CSEC_CMD_ENC_ECB
CSEC_CMD_ENC_CBC
CSEC_CMD_DEC_ECB
CSEC_CMD_DEC_CBC
CSEC_CMD_GENERATE_MAC
CSEC_CMD_VERIFY_MAC
CSEC_CMD_LOAD_KEY
CSEC_CMD_LOAD_PLAIN_KEY
CSEC_CMD_EXPORT_RAM_KEY
CSEC_CMD_INIT_RNG
CSEC_CMD_EXTEND_SEED
CSEC_CMD_RND
CSEC_CMD_RESERVED_1
CSEC_CMD_BOOT_FAILURE
CSEC_CMD_BOOT_OK
CSEC_CMD_GET_ID
CSEC_CMD_BOOT_DEFINE
CSEC_CMD_DBG_CHAL
CSEC_CMD_DBG_AUTH
CSEC_CMD_RESERVED_2
CSEC_CMD_RESERVED_3
CSEC_CMD_MP_COMPRESS

Definition at line 127 of file csec_driver.h.

17.25.5.4 enum csec_key_id_t

Specify the KeyID to be used to implement the requested cryptographic operation.

Implements : csec_key_id_t_Class

Enumerator

CSEC_SECRET_KEY
CSEC_MASTER_ECU
CSEC_BOOT_MAC_KEY
CSEC_BOOT_MAC
CSEC_KEY_1

CSEC_KEY_2
CSEC_KEY_3
CSEC_KEY_4
CSEC_KEY_5
CSEC_KEY_6
CSEC_KEY_7
CSEC_KEY_8
CSEC_KEY_9
CSEC_KEY_10
CSEC_RAM_KEY
CSEC_KEY_11
CSEC_KEY_12
CSEC_KEY_13
CSEC_KEY_14
CSEC_KEY_15
CSEC_KEY_16
CSEC_KEY_17

Definition at line 97 of file csec_driver.h.

17.25.6 Function Documentation

17.25.6.1 `status_t CSEC_DRV_BootDefine (uint32_t bootSize, csec_boot_flavor_t bootFlavor)`

Implements an extension of the SHE standard to define both the user boot size and boot method.

The function implements an extension of the SHE standard to define both the user boot size and boot method.

Parameters

in	<i>bootSize</i>	Number of blocks of 128-bit data to check on boot. Maximum size is 512k↔ Bytes.
in	<i>bootFlavor</i>	The boot method.

Returns

Error Code after command execution.

Definition at line 928 of file csec_driver.c.

17.25.6.2 `status_t CSEC_DRV_BootFailure (void)`

Signals a failure detected during later stages of the boot process.

The function is called during later stages of the boot process to detect a failure.

Returns

Error Code after command execution.

Definition at line 860 of file csec_driver.c.

17.25.6.3 status_t CSEC_DRV_BootOK (void)

Marks a successful boot verification during later stages of the boot process.

The function is called during later stages of the boot process to mark successful boot verification.

Returns

Error Code after command execution.

Definition at line 894 of file csec_driver.c.

17.25.6.4 void CSEC_DRV_CancelCommand (void)

Cancels a previously launched asynchronous command.

Definition at line 1784 of file csec_driver.c.

17.25.6.5 status_t CSEC_DRV_DbgAuth (const uint8_t * *authorization*)

Erases all keys (actual and outdated) stored in NVM Memory if the authorization is confirmed by CSEc.

This function erases all keys (actual and outdated) stored in NVM Memory if the authorization is confirmed by CSEc.

Parameters

<i>in</i>	<i>authorization</i>	Pointer to the 128-bit buffer containing the authorization value.
-----------	----------------------	---

Returns

Error Code after command execution.

Definition at line 1059 of file csec_driver.c.

17.25.6.6 status_t CSEC_DRV_DbgChal (uint8_t * *challenge*)

Obtains a random number which the user shall use along with the MASTER_ECU_KEY and UID to return an authorization request.

This function obtains a random number which the user shall use along with the MASTER_ECU_KEY and UID to return an authorization request.

Parameters

<i>out</i>	<i>challenge</i>	Pointer to the 128-bit buffer where the challenge data will be stored.
------------	------------------	--

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 1019 of file csec_driver.c.

17.25.6.7 status_t CSEC_DRV_DecryptCBC (csec_key_id_t *keyId*, const uint8_t * *cipherText*, uint32_t *length*, const uint8_t * *iv*, uint8_t * *plainText*, uint32_t *timeout*)

Performs the AES-128 decryption in CBC mode.

This function performs the AES-128 decryption in CBC mode of the input cipher text buffer.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>cipherText</i>	Pointer to the cipher text buffer.
in	<i>length</i>	Number of bytes of cipher text message to be decrypted. It should be multiple of 16 bytes.
in	<i>iv</i>	Pointer to the initialization vector buffer.
out	<i>plainText</i>	Pointer to the plain text buffer. The buffer shall have the same size as the cipher text buffer.
in	<i>timeout</i>	Timeout in milliseconds.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 327 of file csec_driver.c.

17.25.6.8 `status_t CSEC_DRV_DecryptCBCAsync (csec_key_id_t keyId, const uint8_t * cipherText, uint32_t length, const uint8_t * iv, uint8_t * plainText)`

Asynchronously performs the AES-128 decryption in CBC mode.

This function performs the AES-128 decryption in CBC mode of the input cipher text buffer, in an asynchronous manner.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>cipherText</i>	Pointer to the cipher text buffer.
in	<i>length</i>	Number of bytes of cipher text message to be decrypted. It should be multiple of 16 bytes.
in	<i>iv</i>	Pointer to the initialization vector buffer.
out	<i>plainText</i>	Pointer to the plain text buffer. The buffer shall have the same size as the cipher text buffer.

Returns

STATUS_SUCCESS if the command was successfully launched, STATUS_BUSY if another command was already launched. CSEC_DRV_GetAsyncCmdStatus can be used in order to check the execution status.

Definition at line 1282 of file csec_driver.c.

17.25.6.9 `status_t CSEC_DRV_DecryptECB (csec_key_id_t keyId, const uint8_t * cipherText, uint32_t length, uint8_t * plainText, uint32_t timeout)`

Performs the AES-128 decryption in ECB mode.

This function performs the AES-128 decryption in ECB mode of the input cipher text buffer.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation
in	<i>cipherText</i>	Pointer to the cipher text buffer.
in	<i>length</i>	Number of bytes of cipher text message to be decrypted. It should be multiple of 16 bytes.
out	<i>plainText</i>	Pointer to the plain text buffer. The buffer shall have the same size as the cipher text buffer.

in	<i>timeout</i>	Timeout in milliseconds.
----	----------------	--------------------------

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 219 of file csec_driver.c.

17.25.6.10 `status_t CSEC_DRV_DecryptECBAsync (csec_key_id_t keyId, const uint8_t * cipherText, uint32_t length, uint8_t * plainText)`

Asynchronously performs the AES-128 decryption in ECB mode.

This function performs the AES-128 decryption in ECB mode of the input cipher text buffer, in an asynchronous manner.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation
in	<i>cipherText</i>	Pointer to the cipher text buffer.
in	<i>length</i>	Number of bytes of cipher text message to be decrypted. It should be multiple of 16 bytes.
out	<i>plainText</i>	Pointer to the plain text buffer. The buffer shall have the same size as the cipher text buffer.

Returns

STATUS_SUCCESS if the command was successfully launched, STATUS_BUSY if another command was already launched. CSEC_DRV_GetAsyncCmdStatus can be used in order to check the execution status.

Definition at line 1215 of file csec_driver.c.

17.25.6.11 `void CSEC_DRV_Deinit (void)`

Clears the internal state of the driver and disables the FTFC interrupt.

Definition at line 151 of file csec_driver.c.

17.25.6.12 `status_t CSEC_DRV_EncryptCBC (csec_key_id_t keyId, const uint8_t * plainText, uint32_t length, const uint8_t * iv, uint8_t * cipherText, uint32_t timeout)`

Performs the AES-128 encryption in CBC mode.

This function performs the AES-128 encryption in CBC mode of the input plaintext buffer.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>plainText</i>	Pointer to the plain text buffer.
in	<i>length</i>	Number of bytes of plain text message to be encrypted. It should be multiple of 16 bytes.
in	<i>iv</i>	Pointer to the initialization vector buffer.
in	<i>timeout</i>	Timeout in milliseconds.
out	<i>cipherText</i>	Pointer to the cipher text buffer. The buffer shall have the same size as the plain text buffer.
in	<i>timeout</i>	Timeout in milliseconds.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 271 of file csec_driver.c.

17.25.6.13 `status_t CSEC_DRV_EncryptCBCAsync (csec_key_id_t keyId, const uint8_t * plainText, uint32_t length, const uint8_t * iv, uint8_t * cipherText)`

Asynchronously performs the AES-128 encryption in CBC mode.

This function performs the AES-128 encryption in CBC mode of the input plaintext buffer, in an asynchronous manner.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>plainText</i>	Pointer to the plain text buffer.
in	<i>length</i>	Number of bytes of plain text message to be encrypted. It should be multiple of 16 bytes.
in	<i>iv</i>	Pointer to the initialization vector buffer.
out	<i>cipherText</i>	Pointer to the cipher text buffer. The buffer shall have the same size as the plain text buffer.

Returns

STATUS_SUCCESS if the command was successfully launched, STATUS_BUSY if another command was already launched. CSEC_DRV_GetAsyncCmdStatus can be used in order to check the execution status.

Definition at line 1247 of file csec_driver.c.

17.25.6.14 `status_t CSEC_DRV_EncryptECB (csec_key_id_t keyId, const uint8_t * plainText, uint32_t length, uint8_t * cipherText, uint32_t timeout)`

Performs the AES-128 encryption in ECB mode.

This function performs the AES-128 encryption in ECB mode of the input plain text buffer

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>plainText</i>	Pointer to the plain text buffer.
in	<i>length</i>	Number of bytes of plain text message to be encrypted. It should be multiple of 16 bytes.
out	<i>cipherText</i>	Pointer to the cipher text buffer. The buffer shall have the same size as the plain text buffer.
in	<i>timeout</i>	Timeout in milliseconds.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 166 of file csec_driver.c.

17.25.6.15 `status_t CSEC_DRV_EncryptECBAsync (csec_key_id_t keyId, const uint8_t * plainText, uint32_t length, uint8_t * cipherText)`

Asynchronously performs the AES-128 encryption in ECB mode.

This function performs the AES-128 encryption in ECB mode of the input plain text buffer, in an asynchronous manner.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>plainText</i>	Pointer to the plain text buffer.
in	<i>length</i>	Number of bytes of plain text message to be encrypted. It should be multiple of 16 bytes.
out	<i>cipherText</i>	Pointer to the cipher text buffer. The buffer shall have the same size as the plain text buffer.

Returns

STATUS_SUCCESS if the command was successfully launched, STATUS_BUSY if another command was already launched. CSEC_DRV_GetAsyncCmdStatus can be used in order to check the execution status.

Definition at line 1183 of file csec_driver.c.

17.25.6.16 `status_t CSEC_DRV_ExportRAMKey (uint8_t * m1, uint8_t * m2, uint8_t * m3, uint8_t * m4, uint8_t * m5)`

Exports the RAM_KEY into a format protected by SECRET_KEY.

This function exports the RAM_KEY into a format protected by SECRET_KEY.

Parameters

out	<i>m1</i>	Pointer to a buffer where the M1 parameter will be exported.
out	<i>m2</i>	Pointer to a buffer where the M2 parameter will be exported.
out	<i>m3</i>	Pointer to a buffer where the M3 parameter will be exported.
out	<i>m4</i>	Pointer to a buffer where the M4 parameter will be exported.
out	<i>m5</i>	Pointer to a buffer where the M5 parameter will be exported.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 693 of file csec_driver.c.

17.25.6.17 `status_t CSEC_DRV_ExtendSeed (const uint8_t * entropy)`

Extends the seed of the PRNG.

Extends the seed of the PRNG by compressing the former seed value and the supplied entropy into a new seed. This new seed is then to be used to generate a random number by invoking the CMD_RND command. The random number generator must be initialized by CMD_INIT_RNG before the seed may be extended.

Parameters

in	<i>entropy</i>	Pointer to a 128-bit buffer containing the entropy.
----	----------------	---

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 782 of file csec_driver.c.

17.25.6.18 `status_t CSEC_DRV_GenerateMAC (csec_key_id_t keyId, const uint8_t * msg, uint32_t msgLen, uint8_t * cmac, uint32_t timeout)`

Calculates the MAC of a given message using CMAC with AES-128.

This function calculates the MAC of a given message using CMAC with AES-128.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>msg</i>	Pointer to the message buffer.
in	<i>msgLen</i>	Number of bits of message on which CMAC will be computed.
out	<i>cmac</i>	Pointer to the buffer containing the result of the CMAC computation.
in	<i>timeout</i>	Timeout in milliseconds.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 383 of file csec_driver.c.

17.25.6.19 `status_t CSEC_DRV_GenerateMACAddrMode (csec_key_id_t keyId, const uint8_t * msg, uint32_t msgLen, uint8_t * cmac)`

Calculates the MAC of a given message (located in Flash) using CMAC with AES-128.

This function calculates the MAC of a given message using CMAC with AES-128. It is different from the CSEC_DRV_GenerateMAC function in the sense that it does not involve an extra copy of the data on which the CMAC is computed and the message pointer should be a pointer to Flash memory.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>msg</i>	Pointer to the message buffer (pointing to Flash memory).
in	<i>msgLen</i>	Number of bits of message on which CMAC will be computed.
out	<i>cmac</i>	Pointer to the buffer containing the result of the CMAC computation.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 439 of file csec_driver.c.

17.25.6.20 `status_t CSEC_DRV_GenerateMACAsync (csec_key_id_t keyId, const uint8_t * msg, uint32_t msgLen, uint8_t * cmac)`

Asynchronously calculates the MAC of a given message using CMAC with AES-128.

This function calculates the MAC of a given message using CMAC with AES-128, in an asynchronous manner.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>msg</i>	Pointer to the message buffer.
in	<i>msgLen</i>	Number of bits of message on which CMAC will be computed.
out	<i>cmac</i>	Pointer to the buffer containing the result of the CMAC computation.

Returns

STATUS_SUCCESS if the command was successfully launched, STATUS_BUSY if another command was already launched. CSEC_DRV_GetAsyncCmdStatus can be used in order to check the execution status.

Definition at line 1317 of file csec_driver.c.

17.25.6.21 `status_t CSEC_DRV_GenerateRND (uint8_t * rnd)`

Generates a vector of 128 random bits.

The function returns a vector of 128 random bits. The random number generator has to be initialized by calling CSEC_DRV_InitRNG before random numbers can be supplied.

Parameters

out	<i>rnd</i>	Pointer to a 128-bit buffer where the generated random number has to be stored.
-----	------------	---

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 820 of file csec_driver.c.

17.25.6.22 status_t CSEC_DRV_GetAsyncCmdStatus (void)

Checks the status of the execution of an asynchronous command.

This function checks the status of the execution of an asynchronous command. If the command is still in progress, returns STATUS_BUSY.

Returns

Error Code after command execution.

Definition at line 1390 of file csec_driver.c.

17.25.6.23 status_t CSEC_DRV_GetID (const uint8_t * challenge, uint8_t * uid, uint8_t * sreg, uint8_t * mac)

Returns the identity (UID) and the value of the status register protected by a MAC over a challenge and the data.

This function returns the identity (UID) and the value of the status register protected by a MAC over a challenge and the data.

Parameters

in	<i>challenge</i>	Pointer to the 128-bit buffer containing Challenge data.
out	<i>uid</i>	Pointer to 120 bit buffer where the UID will be stored.
out	<i>sreg</i>	Value of the status register.
out	<i>mac</i>	Pointer to the 128 bit buffer where the MAC generated over challenge and UID and status will be stored.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 967 of file csec_driver.c.

17.25.6.24 static csec_status_t CSEC_DRV_GetStatus (void) [inline],[static]

Returns the content of the status register.

The function shall return the content of the status register.

Returns

Value of the status register.

Implements : CSEC_DRV_GetStatus_Activity

Definition at line 526 of file csec_driver.h.

17.25.6.25 void CSEC_DRV_Init (csec_state_t * state)

Initializes the internal state of the driver and enables the FTFC interrupt.

Parameters

<i>in</i>	<i>state</i>	Pointer to the state structure which will be used for holding the internal state of the driver.
-----------	--------------	---

Definition at line 131 of file `csec_driver.c`.

17.25.6.26 `status_t CSEC_DRV_InitRNG (void)`

Initializes the seed and derives a key for the PRNG.

The function initializes the seed and derives a key for the PRNG. The function must be called before `CMD_RND` after every power cycle/reset.

Returns

Error Code after command execution.

Definition at line 745 of file `csec_driver.c`.

17.25.6.27 `void CSEC_DRV_InstallCallback (security_callback_t callbackFunc, void * callbackParam)`

Installs a callback function which will be invoked when an asynchronous command finishes its execution.

Parameters

<i>in</i>	<i>callbackFunc</i>	The function to be invoked.
<i>in</i>	<i>callbackParam</i>	The parameter to be passed to the callback function.

Definition at line 1769 of file `csec_driver.c`.

17.25.6.28 `status_t CSEC_DRV_LoadKey (csec_key_id_t keyId, const uint8_t * m1, const uint8_t * m2, const uint8_t * m3, uint8_t * m4, uint8_t * m5)`

Updates an internal key per the SHE specification.

This function updates an internal key per the SHE specification.

Parameters

<i>in</i>	<i>keyId</i>	KeyID of the key to be updated.
<i>in</i>	<i>m1</i>	Pointer to the 128-bit M1 message containing the UID, Key ID and Authentication Key ID.
<i>in</i>	<i>m2</i>	Pointer to the 256-bit M2 message contains the new security flags, counter and the key value all encrypted using a derived key generated from the Authentication Key.
<i>in</i>	<i>m3</i>	Pointer to the 128-bit M3 message is a MAC generated over messages M1 and M2.
<i>out</i>	<i>m4</i>	Pointer to a 256 bits buffer where the computed M4 parameter is stored.
<i>out</i>	<i>m5</i>	Pointer to a 128 bits buffer where the computed M5 parameters is stored.

Returns

Error Code after command execution. Output parameters are valid if the error code is `STATUS_SUCCESS`.

Definition at line 602 of file `csec_driver.c`.

17.25.6.29 `status_t CSEC_DRV_LoadPlainKey (const uint8_t * plainKey)`

Updates the RAM key memory slot with a 128-bit plaintext.

The function updates the RAM key memory slot with a 128-bit plaintext. The key is loaded without encryption and verification of the key, i.e. the key is handed over in plaintext. A plain key can only be loaded into the `RAM_KEY` slot.

Parameters

in	<i>plainKey</i>	Pointer to the 128-bit buffer containing the key that needs to be copied in R↔AM_KEY slot.
----	-----------------	--

Returns

Error Code after command execution.

Definition at line 656 of file csec_driver.c.

17.25.6.30 `status_t CSEC_DRV_MPCompress (const uint8_t * msg, uint16_t msgLen, uint8_t * mpCompress, uint32_t timeout)`

Compresses the given messages by accessing the Miyaguchi-Prenell compression feature with in the CSEc feature set.

This function accesses a Miyaguchi-Prenell compression feature within the CSEc feature set to compress the given messages.

Parameters

in	<i>msg</i>	Pointer to the messages to be compressed. Messages must be pre-processed per SHE specification if they do not already meet the full 128-bit block size requirement.
in	<i>msgLen</i>	The number of 128 bit messages to be compressed.
out	<i>mpCompress</i>	Pointer to the 128 bit buffer storing the compressed data.
in	<i>timeout</i>	Timeout in milliseconds.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 1096 of file csec_driver.c.

17.25.6.31 `status_t CSEC_DRV_VerifyMAC (csec_key_id_t keyId, const uint8_t * msg, uint32_t msgLen, const uint8_t * mac, uint16_t macLen, bool * verifStatus, uint32_t timeout)`

Verifies the MAC of a given message using CMAC with AES-128.

This function verifies the MAC of a given message using CMAC with AES-128.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>msg</i>	Pointer to the message buffer.
in	<i>msgLen</i>	Number of bits of message on which CMAC will be computed.
in	<i>mac</i>	Pointer to the buffer containing the CMAC to be verified.
in	<i>macLen</i>	Number of bits of the CMAC to be compared. A macLength value of zero indicates that all 128-bits are compared.
out	<i>verifStatus</i>	Status of MAC verification command (true: verification operation passed, false: verification operation failed).
in	<i>timeout</i>	Timeout in milliseconds.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 484 of file csec_driver.c.

17.25.6.32 `status_t CSEC_DRV_VerifyMACAddrMode (csec_key_id_t keyId, const uint8_t * msg, uint32_t msgLen, const uint8_t * mac, uint16_t macLen, bool * verifStatus)`

Verifies the MAC of a given message (located in Flash) using CMAC with AES-128.

This function verifies the MAC of a given message using CMAC with AES-128. It is different from the `CSEC_DRV_VerifyMAC` function in the sense that it does not involve an extra copy of the data on which the CMAC is computed and the message pointer should be a pointer to Flash memory.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>msg</i>	Pointer to the message buffer (pointing to Flash memory).
in	<i>msgLen</i>	Number of bits of message on which CMAC will be computed.
in	<i>mac</i>	Pointer to the buffer containing the CMAC to be verified.
in	<i>macLen</i>	Number of bits of the CMAC to be compared. A <i>macLength</i> value of zero indicates that all 128-bits are compared.
out	<i>verifStatus</i>	Status of MAC verification command (true: verification operation passed, false: verification operation failed).

Returns

Error Code after command execution. Output parameters are valid if the error code is `STATUS_SUCCESS`.

Definition at line 547 of file `csec_driver.c`.

17.25.6.33 `status_t CSEC_DRV_VerifyMACAsync (csec_key_id_t keyId, const uint8_t * msg, uint32_t msgLen, const uint8_t * mac, uint16_t macLen, bool * verifStatus)`

Asynchronously verifies the MAC of a given message using CMAC with AES-128.

This function verifies the MAC of a given message using CMAC with AES-128, in an asynchronous manner.

Parameters

in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>msg</i>	Pointer to the message buffer.
in	<i>msgLen</i>	Number of bits of message on which CMAC will be computed.
in	<i>mac</i>	Pointer to the buffer containing the CMAC to be verified.
in	<i>macLen</i>	Number of bits of the CMAC to be compared. A <i>macLength</i> value of zero indicates that all 128-bits are compared.
out	<i>verifStatus</i>	Status of MAC verification command (true: verification operation passed, false: verification operation failed).

Returns

`STATUS_SUCCESS` if the command was successfully launched, `STATUS_BUSY` if another command was already launched. `CSEC_DRV_GetAsyncCmdStatus` can be used in order to check the execution status.

Definition at line 1350 of file `csec_driver.c`.

17.26 Clock

17.26.1 Detailed Description

Dynamic clock setting

- status_t [CLOCK_DRV_GetFreq](#) (clock_names_t clockName, uint32_t *frequency)
Gets the clock frequency for a specific clock name.
- status_t [CLOCK_DRV_Init](#) (clock_user_config_t const *config)
Set clock configuration according to pre-defined structure.

17.26.2 Function Documentation

17.26.2.1 status_t CLOCK_DRV_GetFreq (clock_names_t clockName, uint32_t * frequency)

Gets the clock frequency for a specific clock name.

This function checks the current clock configurations and then calculates the clock frequency for a specific clock name defined in clock_names_t. Clock modules must be properly configured before using this function. See features.h for supported clock names for different chip families. The returned value is in Hertz. If it cannot find the clock name or the name is not supported for a specific chip family, it returns an STATUS_UNSUPPORTED. If frequency is required for a peripheral and the module is not clocked, then STATUS_MCU_GATED_OFF status is returned. Frequency is returned if a valid address is provided. If frequency is required for a peripheral that doesn't support protocol clock, the zero value is provided.

Parameters

in	clockName	Clock names defined in clock_names_t
out	frequency	Returned clock frequency value in Hertz

Returns

status Error code defined in status_t

Definition at line 1902 of file clock_S32K1xx.c.

17.26.2.2 status_t CLOCK_DRV_Init (clock_user_config_t const * config)

Set clock configuration according to pre-defined structure.

This function sets system to target clock configuration; It sets the clock modules registers for clock mode change.

Parameters

in	config	Pointer to configuration structure.
----	--------	-------------------------------------

Returns

Error code.

Note

If external clock is used in the target mode, please make sure it is enabled, for example, if the external oscillator is used, please setup correctly.

If the configuration structure is NULL, the function will set a default configuration for clock.

Definition at line 603 of file clock_S32K1xx.c.

17.27 Clock Manager

17.27.1 Detailed Description

This module covers the clock management API and clock related functionality.

This section describes the programming interface of the clock_manager driver. Clock_manager achieves its functionality by configuring the hardware modules involved in clock distribution and management.

Driver consideration

The Clock Manager driver is developed on top of an appropriate hardware access layer. The Clock Manager provides API to handle the clock configuration. The Driver uses structures for configuration. The actual format of the structure is defined by the underlying device specific header file. These structures may be generated using S32DS configuration. The user application can use the default for most settings, changing only what is necessary.

This driver provides functions for initializing system clock and peripheral clock.

All methods that access the hardware layer will return an error code to signal if the operation succeeded or failed. The values are defined by the status_t enumeration, and the possible values include: success, error.

Modules

- [Clock Manager Driver](#)

This module covers the device-specific clock_manager functionality implemented for S32K1xx SOC.

17.28 Clock Manager Driver

17.28.1 Detailed Description

This module covers the device-specific clock_manager functionality implemented for S32K1xx SOC.

The support for S32K1xx consist in the following items:

1. Clock names enumeration clock_names_t is an enumeration which contains all clock names which are relevant for S32K1xx.
2. Submodule configuration structures
 - [scg_config_t](#)
 - [pcc_config_t](#)
 - [sim_clock_config_t](#)
 - [pmc_config_t](#)
3. Submodule configuration functions The following functions were implemented for S32K1xx:
 - CLOCK_SYS_SetScgConfiguration
 - CLOCK_SYS_SetPccConfiguration
 - CLOCK_SYS_SetSimConfiguration
 - CLOCK_SYS_SetPmcConfiguration

Hardware background

Features of clock_manager module include the following clock sources:

- 4 - 40 MHz fast external oscillator (SOSC)
- 48 MHz Fast Internal RC oscillator (FIRC)
- 8 MHz Slow Internal RC oscillator (SIRC)
- 128 kHz Low Power Oscillator (LPO)
- Up to 112 MHz (HSRUN) System Phased Lock Loop (SPLL)

How to use the CLOCK_MANAGER driver in your application

In order to be able to use the clock_manager in your application, **CLOCK_DRV_Init** function has to be called. The same function is called when another configuration is loaded and clock configuration is updated.

Code Example

This is an example for switching between two configurations:

```
CLOCK_SYS_Init(g_clockManConfigsArr,  
              CLOCK_MANAGER_CONFIG_CNT,  
              g_clockManCallbacksArr,  
              CLOCK_MANAGER_CALLBACK_CNT);  
  
CLOCK_SYS_UpdateConfiguration(0,  
                             CLOCK_MANAGER_POLICY_FORCIBLE);  
CLOCK_SYS_UpdateConfiguration(1,  
                             CLOCK_MANAGER_POLICY_FORCIBLE);
```

Notes

Current implementation assumes that the clock configurations are valid and are applied in a valid sequence. Mainly this means that the configuration doesn't reinitialize the clock used as the system clock.

According to Errata e10777, when the power mode is being switched, the core clock frequency is incorrectly read. As a result, when switching from VLPR mode to HSRUN, the frequency has to be read twice or after some time has passed.

The S32DS do not support generate Callbacks configuration. It's alway empty.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\clock\S32K1xx\clock_S32K1xx.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc\  
${S32SDK_PATH}\platform\drivers\src\clock\  
${S32SDK_PATH}\platform\drivers\src\clock\S32K1xx\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Interrupt Manager \(Interrupt\)](#)

Data Structures

- struct [sim_clock_out_config_t](#)
SIM ClockOut configuration. Implements sim_clock_out_config_t_Class. [More...](#)
- struct [sim_lpo_clock_config_t](#)
SIM LPO Clocks configuration. Implements sim_lpo_clock_config_t_Class. [More...](#)
- struct [sim_tclk_config_t](#)
SIM Platform Gate Clock configuration. Implements sim_tclk_config_t_Class. [More...](#)
- struct [sim_plat_gate_config_t](#)
SIM Platform Gate Clock configuration. Implements sim_plat_gate_config_t_Class. [More...](#)
- struct [sim_qspi_ref_clk_gating_t](#)
SIM QSPI reference clock gating. Implements sim_qspi_ref_clk_gating_t_Class. [More...](#)
- struct [sim_trace_clock_config_t](#)
SIM Debug Trace clock configuration. Implements sim_trace_clock_config_t_Class. [More...](#)
- struct [sim_clock_config_t](#)
SIM configure structure. Implements sim_clock_config_t_Class. [More...](#)
- struct [scg_system_clock_config_t](#)
SCG system clock configuration. Implements scg_system_clock_config_t_Class. [More...](#)
- struct [scg_sosc_config_t](#)
SCG system OSC configuration. Implements scg_sosc_config_t_Class. [More...](#)
- struct [scg_sirc_config_t](#)
SCG slow IRC clock configuration. Implements scg_sirc_config_t_Class. [More...](#)
- struct [scg_firc_config_t](#)

- SCG fast IRC clock configuration. Implements `scg_firc_config_t` Class. [More...](#)*
- struct `scg_spll_config_t`
 - SCG system PLL configuration. Implements `scg_spll_config_t` Class. [More...](#)*
- struct `scg_rtc_config_t`
 - SCG RTC configuration. Implements `scg_rtc_config_t` Class. [More...](#)*
- struct `scg_clock_mode_config_t`
 - SCG Clock Mode Configuration structure. Implements `scg_clock_mode_config_t` Class. [More...](#)*
- struct `scg_clockout_config_t`
 - SCG ClockOut Configuration structure. Implements `scg_clockout_config_t` Class. [More...](#)*
- struct `scg_config_t`
 - SCG configure structure. Implements `scg_config_t` Class. [More...](#)*
- struct `peripheral_clock_config_t`
 - PCC peripheral instance clock configuration. Implements `peripheral_clock_config_t` Class. [More...](#)*
- struct `pcc_config_t`
 - PCC configuration. Implements `pcc_config_t` Class. [More...](#)*
- struct `pmc_lpo_clock_config_t`
 - PMC LPO configuration. Implements `pmc_lpo_clock_config_t` Class. [More...](#)*
- struct `pmc_config_t`
 - PMC configure structure. Implements `pmc_config_t` Class. [More...](#)*
- struct `clock_manager_user_config_t`
 - Clock configuration structure. Implements `clock_manager_user_config_t` Class. [More...](#)*
- struct `module_clk_config_t`
 - module clock configuration. Implements `module_clk_config_t` Class [More...](#)*
- struct `sys_clk_config_t`
 - System clock configuration. Implements `sys_clk_config_t` Class. [More...](#)*
- struct `clock_source_config_t`
 - Clock source configuration. Implements `clock_source_config_t` Class. [More...](#)*
- struct `clock_notify_struct_t`
 - Clock notification structure passed to clock callback function. Implements `clock_notify_struct_t` Class. [More...](#)*
- struct `clock_manager_callback_user_config_t`
 - Structure for callback function and its parameter. Implements `clock_manager_callback_user_config_t` Class. [More...](#)*
- struct `clock_manager_state_t`
 - Clock manager state structure. Implements `clock_manager_state_t` Class. [More...](#)*

Macros

- #define `NUMBER_OF_TCLK_INPUTS` 3U
 - TClk clock frequency.*
- #define `SYS_CLK_MAX_NO` 3U
 - The maximum number of system clock dividers and system clock divider indexes.*
- #define `CORE_CLK_INDEX` 0U
- #define `BUS_CLK_INDEX` 1U
- #define `SLOW_CLK_INDEX` 2U
- #define `CLK_SRC_OFF` 0x00U
- #define `CLK_SRC_SOSC` 0x01U
- #define `CLK_SRC_SIRC` 0x02U
- #define `CLK_SRC_FIRC` 0x03U
- #define `CLK_SRC_SPLL` 0x06U
- #define `CLK_SRC_SOSC_DIV1` 0x01U
- #define `CLK_SRC_SIRC_DIV1` 0x02U
- #define `CLK_SRC_FIRC_DIV1` 0x03U

- #define CLK_SRC_SPLL_DIV1 0x06U
- #define CLK_SRC_SOSC_DIV2 0x01U
- #define CLK_SRC_SIRC_DIV2 0x02U
- #define CLK_SRC_FIRC_DIV2 0x03U
- #define CLK_SRC_SPLL_DIV2 0x06U

Typedefs

- typedef uint8_t peripheral_clock_source_t
PCC clock source select Implements peripheral_clock_source_t Class.
- typedef clock_manager_user_config_t clock_user_config_t
- typedef status_t(* clock_manager_callback_t) (clock_notify_struct_t *notify, void *callbackData)
Type of clock callback functions.

Enumerations

- enum sim_rtc_clk_sel_src_t { SIM_RTCCLK_SEL_SOSCDIV1_CLK = 0x0U, SIM_RTCCLK_SEL_LPO_32K = 0x1U, SIM_RTCCLK_SEL_RTC_CLKIN = 0x2U, SIM_RTCCLK_SEL_FIRCDIV1_CLK = 0x3U }
SIM CLK32KSEL clock source select Implements sim_rtc_clk_sel_src_t Class.
- enum sim_lpclk_sel_src_t { SIM_LPO_CLK_SEL_LPO_128K = 0x0, SIM_LPO_CLK_SEL_NO_CLOCK = 0x1, SIM_LPO_CLK_SEL_LPO_32K = 0x2, SIM_LPO_CLK_SEL_LPO_1K = 0x3 }
SIM LPOCLKSEL clock source select Implements sim_lpclk_sel_src_t Class.
- enum sim_clkout_src_t {
SIM_CLKOUT_SEL_SYSTEM_SCG_CLKOUT = 0U, SIM_CLKOUT_SEL_SYSTEM_SOSC_DIV2_CLK = 2U, SIM_CLKOUT_SEL_SYSTEM_SIRC_DIV2_CLK = 4U, SIM_CLKOUT_SEL_SYSTEM_FIRC_DIV2_CLK = 6U,
SIM_CLKOUT_SEL_SYSTEM_HCLK = 7U, SIM_CLKOUT_SEL_SYSTEM_SPLL_DIV2_CLK = 8U, SIM_CLKOUT_SEL_SYSTEM_BUS_CLK = 9U, SIM_CLKOUT_SEL_SYSTEM_LPO_128K_CLK = 10U,
SIM_CLKOUT_SEL_SYSTEM_LPO_CLK = 12U, SIM_CLKOUT_SEL_SYSTEM_RTC_CLK = 14U }
SIM CLKOUT select Implements sim_clkout_src_t Class.
- enum sim_clkout_div_t {
SIM_CLKOUT_DIV_BY_1 = 0x0U, SIM_CLKOUT_DIV_BY_2 = 0x1U, SIM_CLKOUT_DIV_BY_3 = 0x2U, SIM_CLKOUT_DIV_BY_4 = 0x3U,
SIM_CLKOUT_DIV_BY_5 = 0x4U, SIM_CLKOUT_DIV_BY_6 = 0x5U, SIM_CLKOUT_DIV_BY_7 = 0x6U, SIM_CLKOUT_DIV_BY_8 = 0x7U }
SIM CLKOUT divider Implements sim_clkout_div_t Class.
- enum clock_trace_src_t { CLOCK_TRACE_SRC_CORE_CLK = 0x0 }
Debug trace clock source select Implements clock_trace_src_t Class.
- enum scg_system_clock_src_t { SCG_SYSTEM_CLOCK_SRC_SYS_OSC = 1U, SCG_SYSTEM_CLOCK_SRC_SIRC = 2U, SCG_SYSTEM_CLOCK_SRC_FIRC = 3U, SCG_SYSTEM_CLOCK_SRC_NONE = 255U }
SCG system clock source. Implements scg_system_clock_src_t Class.
- enum scg_system_clock_div_t {
SCG_SYSTEM_CLOCK_DIV_BY_1 = 0U, SCG_SYSTEM_CLOCK_DIV_BY_2 = 1U, SCG_SYSTEM_CLOCK_DIV_BY_3 = 2U, SCG_SYSTEM_CLOCK_DIV_BY_4 = 3U,
SCG_SYSTEM_CLOCK_DIV_BY_5 = 4U, SCG_SYSTEM_CLOCK_DIV_BY_6 = 5U, SCG_SYSTEM_CLOCK_DIV_BY_7 = 6U, SCG_SYSTEM_CLOCK_DIV_BY_8 = 7U,
SCG_SYSTEM_CLOCK_DIV_BY_9 = 8U, SCG_SYSTEM_CLOCK_DIV_BY_10 = 9U, SCG_SYSTEM_CLOCK_DIV_BY_11 = 10U, SCG_SYSTEM_CLOCK_DIV_BY_12 = 11U,
SCG_SYSTEM_CLOCK_DIV_BY_13 = 12U, SCG_SYSTEM_CLOCK_DIV_BY_14 = 13U, SCG_SYSTEM_CLOCK_DIV_BY_15 = 14U, SCG_SYSTEM_CLOCK_DIV_BY_16 = 15U }
SCG system clock divider value. Implements scg_system_clock_div_t Class.

- enum `scg_async_clock_div_t` {
`SCG_ASYNC_CLOCK_DISABLE` = 0U, `SCG_ASYNC_CLOCK_DIV_BY_1` = 1U, `SCG_ASYNC_CLOCK_DIV_BY_2` = 2U, `SCG_ASYNC_CLOCK_DIV_BY_4` = 3U,
`SCG_ASYNC_CLOCK_DIV_BY_8` = 4U, `SCG_ASYNC_CLOCK_DIV_BY_16` = 5U, `SCG_ASYNC_CLOCK_DIV_BY_32` = 6U, `SCG_ASYNC_CLOCK_DIV_BY_64` = 7U }
SCG asynchronous clock divider value. Implements `scg_async_clock_div_t` Class.
- enum `scg_sosc_monitor_mode_t` { `SCG_SOSC_MONITOR_DISABLE` = 0U, `SCG_SOSC_MONITOR_INT` = 1U, `SCG_SOSC_MONITOR_RESET` = 2U }
SCG system OSC monitor mode. Implements `scg_sosc_monitor_mode_t` Class.
- enum `scg_sosc_range_t` { `SCG_SOSC_RANGE_MID` = 2U, `SCG_SOSC_RANGE_HIGH` = 3U }
SCG OSC frequency range select Implements `scg_sosc_range_t` Class.
- enum `scg_sosc_gain_t` { `SCG_SOSC_GAIN_LOW` = 0x0, `SCG_SOSC_GAIN_HIGH` = 0x1 }
SCG OSC high gain oscillator select. Implements `scg_sosc_gain_t` Class.
- enum `scg_sosc_ext_ref_t` { `SCG_SOSC_REF_EXT` = 0x0, `SCG_SOSC_REF_OSC` = 0x1 }
SCG OSC external reference clock select. Implements `scg_sosc_ext_ref_t` Class.
- enum `scg_sirc_range_t` { `SCG_SIRC_RANGE_HIGH` = 1U }
SCG slow IRC clock frequency range. Implements `scg_sirc_range_t` Class.
- enum `scg_firc_range_t` { `SCG_FIRC_RANGE_48M` }
SCG fast IRC clock frequency range. Implements `scg_firc_range_t` Class.
- enum `scg_sppll_monitor_mode_t` { `SCG_SPPLL_MONITOR_DISABLE` = 0U, `SCG_SPPLL_MONITOR_INT` = 1U, `SCG_SPPLL_MONITOR_RESET` = 2U }
SCG system PLL monitor mode. Implements `scg_sppll_monitor_mode_t` Class.
- enum `scg_sppll_clock_prediv_t` {
`SCG_SPPLL_CLOCK_PREDIV_BY_1` = 0U, `SCG_SPPLL_CLOCK_PREDIV_BY_2` = 1U, `SCG_SPPLL_CLOCK_PREDIV_BY_3` = 2U, `SCG_SPPLL_CLOCK_PREDIV_BY_4` = 3U,
`SCG_SPPLL_CLOCK_PREDIV_BY_5` = 4U, `SCG_SPPLL_CLOCK_PREDIV_BY_6` = 5U, `SCG_SPPLL_CLOCK_PREDIV_BY_7` = 6U, `SCG_SPPLL_CLOCK_PREDIV_BY_8` = 7U }
SCG system PLL predivider.
- enum `scg_sppll_clock_multiply_t` {
`SCG_SPPLL_CLOCK_MULTIPLY_BY_16` = 0U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_17` = 1U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_18` = 2U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_19` = 3U,
`SCG_SPPLL_CLOCK_MULTIPLY_BY_20` = 4U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_21` = 5U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_22` = 6U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_23` = 7U,
`SCG_SPPLL_CLOCK_MULTIPLY_BY_24` = 8U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_25` = 9U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_26` = 10U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_27` = 11U,
`SCG_SPPLL_CLOCK_MULTIPLY_BY_28` = 12U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_29` = 13U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_30` = 14U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_31` = 15U,
`SCG_SPPLL_CLOCK_MULTIPLY_BY_32` = 16U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_33` = 17U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_34` = 18U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_35` = 19U,
`SCG_SPPLL_CLOCK_MULTIPLY_BY_36` = 20U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_37` = 21U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_38` = 22U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_39` = 23U,
`SCG_SPPLL_CLOCK_MULTIPLY_BY_40` = 24U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_41` = 25U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_42` = 26U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_43` = 27U,
`SCG_SPPLL_CLOCK_MULTIPLY_BY_44` = 28U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_45` = 29U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_46` = 30U, `SCG_SPPLL_CLOCK_MULTIPLY_BY_47` = 31U }
SCG system PLL multiplier.
- enum `peripheral_clock_frac_t` { `MULTIPLY_BY_ONE` = 0x00U, `MULTIPLY_BY_TWO` = 0x01U }
PCC fractional value select Implements `peripheral_clock_frac_t` Class.
- enum `peripheral_clock_divider_t` {
`DIVIDE_BY_ONE` = 0x00U, `DIVIDE_BY_TWO` = 0x01U, `DIVIDE_BY_THREE` = 0x02U, `DIVIDE_BY_FOUR` = 0x03U,
`DIVIDE_BY_FIVE` = 0x04U, `DIVIDE_BY_SIX` = 0x05U, `DIVIDE_BY_SEVEN` = 0x06U, `DIVIDE_BY_EIGHTH` = 0x07U }
PCC divider value select Implements `peripheral_clock_divider_t` Class.

- enum `pwr_modes_t` {
`NO_MODE` = 0U, `RUN_MODE` = (1U<<0U), `VLPR_MODE` = (1U<<1U), `HSRUN_MODE` = (1U<<2U),
`STOP_MODE` = (1U<<3U), `VLPS_MODE` = (1U<<4U), `ALL_MODES` = 0x7FFFFFFF }
Power mode. Implements `pwr_modes_t` Class.
- enum `xosc_ref_t` { `XOSC_EXT_REF` = 0U, `XOSC_INT_OSC` = 1U }
XOSC reference clock select (internal oscillator is bypassed or not) Implements `xosc_ref_t` Class.
- enum `clock_manager_notify_t` { `CLOCK_MANAGER_NOTIFY_RECOVER` = 0x00U, `CLOCK_MANAGER_NOTIFY_BEFORE` = 0x01U, `CLOCK_MANAGER_NOTIFY_AFTER` = 0x02U }
The clock notification type. Implements `clock_manager_notify_t` Class.
- enum `clock_manager_callback_type_t` { `CLOCK_MANAGER_CALLBACK_BEFORE` = 0x01U, `CLOCK_MANAGER_CALLBACK_AFTER` = 0x02U, `CLOCK_MANAGER_CALLBACK_BEFORE_AFTER` = 0x03U }
The callback type, indicates what kinds of notification this callback handles. Implements `clock_manager_callback_type_t` Class.
- enum `clock_manager_policy_t` { `CLOCK_MANAGER_POLICY_AGREEMENT`, `CLOCK_MANAGER_POLICY_FORCIBLE` }
Clock transition policy. Implements `clock_manager_policy_t` Class.

Functions

- void `CLOCK_DRV_SetModuleClock` (`clock_names_t` peripheralClock, const `module_clk_config_t` *moduleClkConfig)
Configures module clock.
- status_t `CLOCK_DRV_SetSystemClock` (const `pwr_modes_t` *mode, const `sys_clk_config_t` *sysClkConfig)
Configures the system clocks.
- void `CLOCK_DRV_GetSystemClockSource` (`sys_clk_config_t` *sysClkConfig)
Gets the system clock source.
- status_t `CLOCK_DRV_SetClockSource` (`clock_names_t` clockSource, const `clock_source_config_t` *clkSrcConfig)
This function configures a clock source.
- status_t `CLOCK_SYS_Init` (`clock_manager_user_config_t` const **clockConfigsPtr, uint8_t configsNumber, `clock_manager_callback_user_config_t` **callbacksPtr, uint8_t callbacksNumber)
Install pre-defined clock configurations.
- status_t `CLOCK_SYS_UpdateConfiguration` (uint8_t targetConfigIndex, `clock_manager_policy_t` policy)
Set system clock configuration according to pre-defined structure.
- status_t `CLOCK_SYS_SetConfiguration` (`clock_manager_user_config_t` const *config)
Set system clock configuration.
- uint8_t `CLOCK_SYS_GetCurrentConfiguration` (void)
Get current system clock configuration.
- `clock_manager_callback_user_config_t` * `CLOCK_SYS_GetErrorCallback` (void)
Get the callback which returns error in last clock switch.
- status_t `CLOCK_SYS_GetFreq` (`clock_names_t` clockName, uint32_t *frequency)
Wrapper over `CLOCK_DRV_GetFreq` function. It's part of the old API.

Variables

- const uint8_t `peripheralFeaturesList` [CLOCK_NAME_COUNT]
Peripheral features list Constant array storing the mappings between clock names of the peripherals and feature lists.
- uint32_t `g_TClkFreq` [NUMBER_OF_TCLK_INPUTS]
EXTAL0 clock frequency.
- uint32_t `g_xtal0ClkFreq`
EXTAL0 clock frequency.
- uint32_t `g_RtcClkInFreq`
RTC_CLKIN clock frequency.

SCG Clockout.

- enum [scg_clockout_src_t](#) {
[SCG_CLOCKOUT_SRC_SCG_SLOW](#) = 0U, [SCG_CLOCKOUT_SRC_SOSC](#) = 1U, [SCG_CLOCKOUT_SRC_SIRC](#) = 2U, [SCG_CLOCKOUT_SRC_FIRC](#) = 3U,
[SCG_CLOCKOUT_SRC_SPLL](#) = 6U }

SCG ClockOut type. Implements [scg_clockout_src_t](#) Class.

17.28.2 Data Structure Documentation

17.28.2.1 struct [sim_clock_out_config_t](#)

SIM ClockOut configuration. Implements [sim_clock_out_config_t](#) Class.

Definition at line 142 of file [clock_S32K1xx.h](#).

Data Fields

- bool [initialize](#)
- bool [enable](#)
- [sim_clkout_src_t](#) [source](#)
- [sim_clkout_div_t](#) [divider](#)

Field Documentation

17.28.2.1.1 [sim_clkout_div_t](#) [divider](#)

SIM ClockOut divide ratio.

Definition at line 147 of file [clock_S32K1xx.h](#).

17.28.2.1.2 bool [enable](#)

SIM ClockOut enable.

Definition at line 145 of file [clock_S32K1xx.h](#).

17.28.2.1.3 bool [initialize](#)

Initialize or not the ClockOut clock.

Definition at line 144 of file [clock_S32K1xx.h](#).

17.28.2.1.4 [sim_clkout_src_t](#) [source](#)

SIM ClockOut source select.

Definition at line 146 of file [clock_S32K1xx.h](#).

17.28.2.2 struct [sim_lpo_clock_config_t](#)

SIM LPO Clocks configuration. Implements [sim_lpo_clock_config_t](#) Class.

Definition at line 155 of file [clock_S32K1xx.h](#).

Data Fields

- bool [initialize](#)
- [sim_rtc_clk_sel_src_t](#) [sourceRtcClk](#)
- [sim_lpoclk_sel_src_t](#) [sourceLpoClk](#)
- bool [enableLpo32k](#)
- bool [enableLpo1k](#)

Field Documentation

17.28.2.2.1 bool enableLpo1k

MSCM Clock Gating Control enable.

Definition at line 161 of file clock_S32K1xx.h.

17.28.2.2.2 bool enableLpo32k

MSCM Clock Gating Control enable.

Definition at line 160 of file clock_S32K1xx.h.

17.28.2.2.3 bool initialize

Initialize or not the LPO clock.

Definition at line 157 of file clock_S32K1xx.h.

17.28.2.2.4 sim_lpoclk_sel_src_t sourceLpoClk

LPO clock source select.

Definition at line 159 of file clock_S32K1xx.h.

17.28.2.2.5 sim_rtc_clk_sel_src_t sourceRtcClk

RTC_CLK source select.

Definition at line 158 of file clock_S32K1xx.h.

17.28.2.3 struct sim_tclk_config_t

SIM Platform Gate Clock configuration. Implements sim_tclk_config_t_Class.

Definition at line 168 of file clock_S32K1xx.h.

Data Fields

- bool [initialize](#)
- uint32_t [tclkFreq](#) [[NUMBER_OF_TCLK_INPUTS](#)]
- uint32_t [extPinSrc](#) [[FTM_INSTANCE_COUNT](#)]

Field Documentation

17.28.2.3.1 uint32_t extPinSrc[FTM_INSTANCE_COUNT]

FTMx frequency.

Definition at line 172 of file clock_S32K1xx.h.

17.28.2.3.2 bool initialize

Initialize or not the TCLK clock.

Definition at line 170 of file clock_S32K1xx.h.

17.28.2.3.3 uint32_t tclkFreq[NUMBER_OF_TCLK_INPUTS]

TCLKx frequency.

Definition at line 171 of file clock_S32K1xx.h.

17.28.2.4 struct sim_plat_gate_config_t

SIM Platform Gate Clock configuration. Implements sim_plat_gate_config_t_Class.

Definition at line 179 of file clock_S32K1xx.h.

Data Fields

- bool [initialize](#)
- bool [enableMscm](#)
- bool [enableMpu](#)
- bool [enableDma](#)
- bool [enableErm](#)
- bool [enableEim](#)

Field Documentation

17.28.2.4.1 bool enableDma

DMA Clock Gating Control enable.

Definition at line 184 of file clock_S32K1xx.h.

17.28.2.4.2 bool enableEim

EIM Clock Gating Control enable.

Definition at line 186 of file clock_S32K1xx.h.

17.28.2.4.3 bool enableErm

ERM Clock Gating Control enable.

Definition at line 185 of file clock_S32K1xx.h.

17.28.2.4.4 bool enableMpu

MPU Clock Gating Control enable.

Definition at line 183 of file clock_S32K1xx.h.

17.28.2.4.5 bool enableMscm

MSCM Clock Gating Control enable.

Definition at line 182 of file clock_S32K1xx.h.

17.28.2.4.6 bool initialize

Initialize or not the Trace clock.

Definition at line 181 of file clock_S32K1xx.h.

17.28.2.5 struct sim_qspi_ref_clk_gating_t

SIM QSPI reference clock gating. Implements sim_qspi_ref_clk_gating_t_Class.

Definition at line 193 of file clock_S32K1xx.h.

Data Fields

- bool [enableQspiRefClk](#)

Field Documentation

17.28.2.5.1 bool enableQspiRefClk

qspi internal reference clock gating control enable.

Definition at line 195 of file clock_S32K1xx.h.

17.28.2.6 struct sim_trace_clock_config_t

SIM Debug Trace clock configuration. Implements sim_trace_clock_config_t_Class.

Definition at line 213 of file clock_S32K1xx.h.

Data Fields

- bool [initialize](#)
- bool [divEnable](#)
- [clock_trace_src_t](#) [source](#)
- [uint8_t](#) [divider](#)
- bool [divFraction](#)

Field Documentation

17.28.2.6.1 bool divEnable

Trace clock divider enable.

Definition at line 216 of file clock_S32K1xx.h.

17.28.2.6.2 bool divFraction

Trace clock divider fraction.

Definition at line 219 of file clock_S32K1xx.h.

17.28.2.6.3 uint8_t divider

Trace clock divider divisor.

Definition at line 218 of file clock_S32K1xx.h.

17.28.2.6.4 bool initialize

Initialize or not the Trace clock.

Definition at line 215 of file clock_S32K1xx.h.

17.28.2.6.5 clock_trace_src_t source

Trace clock select.

Definition at line 217 of file clock_S32K1xx.h.

17.28.2.7 struct sim_clock_config_t

SIM configure structure. Implements sim_clock_config_t_Class.

Definition at line 226 of file clock_S32K1xx.h.

Data Fields

- [sim_clock_out_config_t](#) [clockOutConfig](#)
- [sim_lpo_clock_config_t](#) [lpoClockConfig](#)
- [sim_tclk_config_t](#) [tclkConfig](#)
- [sim_plat_gate_config_t](#) [platGateConfig](#)
- [sim_trace_clock_config_t](#) [traceClockConfig](#)
- [sim_qspi_ref_clk_gating_t](#) [qspiRefClkGating](#)

Field Documentation

17.28.2.7.1 `sim_clock_out_config_t` clockOutConfig

Clock Out configuration.

Definition at line 228 of file clock_S32K1xx.h.

17.28.2.7.2 `sim_lpo_clock_config_t` lpoClockConfig

Low Power Clock configuration.

Definition at line 229 of file clock_S32K1xx.h.

17.28.2.7.3 `sim_plat_gate_config_t` platGateConfig

Platform Gate Clock configuration.

Definition at line 231 of file clock_S32K1xx.h.

17.28.2.7.4 `sim_qspi_ref_clk_gating_t` qspiRefClkGating

Qspi Reference Clock Gating.

Definition at line 233 of file clock_S32K1xx.h.

17.28.2.7.5 `sim_tclk_config_t` tclkConfig

TCLK, FTM option Clock configuration.

Definition at line 230 of file clock_S32K1xx.h.

17.28.2.7.6 `sim_trace_clock_config_t` traceClockConfig

Trace clock configuration.

Definition at line 232 of file clock_S32K1xx.h.

17.28.2.8 `struct scg_system_clock_config_t`

SCG system clock configuration. Implements `scg_system_clock_config_t_Class`.

Definition at line 280 of file clock_S32K1xx.h.

Data Fields

- [scg_system_clock_div_t](#) divSlow
- [scg_system_clock_div_t](#) divBus
- [scg_system_clock_div_t](#) divCore
- [scg_system_clock_src_t](#) src

Field Documentation

17.28.2.8.1 `scg_system_clock_div_t` divBus

BUS clock divider.

Definition at line 283 of file clock_S32K1xx.h.

17.28.2.8.2 `scg_system_clock_div_t` divCore

Core clock divider.

Definition at line 284 of file clock_S32K1xx.h.

17.28.2.8.3 `scg_system_clock_div_t` divSlow

Slow clock divider.

Definition at line 282 of file `clock_S32K1xx.h`.

17.28.2.8.4 `scg_system_clock_src_t` src

System clock source.

Definition at line 285 of file `clock_S32K1xx.h`.

17.28.2.9 `struct scg_sosc_config_t`

SCG system OSC configuration. Implements `scg_sosc_config_t_Class`.

Definition at line 370 of file `clock_S32K1xx.h`.

Data Fields

- `uint32_t freq`
- `scg_sosc_monitor_mode_t monitorMode`
- `scg_sosc_ext_ref_t extRef`
- `scg_sosc_gain_t gain`
- `scg_sosc_range_t range`
- `scg_async_clock_div_t div1`
- `scg_async_clock_div_t div2`
- `bool enableInStop`
- `bool enableInLowPower`
- `bool locked`
- `bool initialize`

Field Documentation

17.28.2.9.1 `scg_async_clock_div_t` div1

Asynchronous peripheral source.

Definition at line 381 of file `clock_S32K1xx.h`.

17.28.2.9.2 `scg_async_clock_div_t` div2

Asynchronous peripheral source.

Definition at line 382 of file `clock_S32K1xx.h`.

17.28.2.9.3 `bool enableInLowPower`

System OSC is enable or not in low power mode.

Definition at line 385 of file `clock_S32K1xx.h`.

17.28.2.9.4 `bool enableInStop`

System OSC is enable or not in stop mode.

Definition at line 384 of file `clock_S32K1xx.h`.

17.28.2.9.5 `scg_sosc_ext_ref_t` extRef

System OSC External Reference Select.

Definition at line 376 of file `clock_S32K1xx.h`.

17.28.2.9.6 uint32_t freq

System OSC frequency.

Definition at line 372 of file clock_S32K1xx.h.

17.28.2.9.7 scg_sosc_gain_t gain

System OSC high-gain operation.

Definition at line 377 of file clock_S32K1xx.h.

17.28.2.9.8 bool initialize

Initialize or not the System OSC module.

Definition at line 389 of file clock_S32K1xx.h.

17.28.2.9.9 bool locked

System OSC Control Register can be written.

Definition at line 387 of file clock_S32K1xx.h.

17.28.2.9.10 scg_sosc_monitor_mode_t monitorMode

System OSC Clock monitor mode.

Definition at line 374 of file clock_S32K1xx.h.

17.28.2.9.11 scg_sosc_range_t range

System OSC frequency range.

Definition at line 379 of file clock_S32K1xx.h.

17.28.2.10 struct scg_sirc_config_t

SCG slow IRC clock configuration. Implements scg_sirc_config_t_Class.

Definition at line 405 of file clock_S32K1xx.h.

Data Fields

- [scg_sirc_range_t range](#)
- [scg_async_clock_div_t div1](#)
- [scg_async_clock_div_t div2](#)
- [bool initialize](#)
- [bool enableInStop](#)
- [bool enableInLowPower](#)
- [bool locked](#)

Field Documentation**17.28.2.10.1 scg_async_clock_div_t div1**

Asynchronous peripheral source.

Definition at line 409 of file clock_S32K1xx.h.

17.28.2.10.2 scg_async_clock_div_t div2

Asynchronous peripheral source.

Definition at line 410 of file clock_S32K1xx.h.

17.28.2.10.3 bool enableInLowPower

SIRC is enable or not in low power mode.

Definition at line 414 of file clock_S32K1xx.h.

17.28.2.10.4 bool enableInStop

SIRC is enable or not in stop mode.

Definition at line 413 of file clock_S32K1xx.h.

17.28.2.10.5 bool initialize

Initialize or not the SIRC module.

Definition at line 412 of file clock_S32K1xx.h.

17.28.2.10.6 bool locked

SIRC Control Register can be written.

Definition at line 416 of file clock_S32K1xx.h.

17.28.2.10.7 scg_sirc_range_t range

Slow IRC frequency range.

Definition at line 407 of file clock_S32K1xx.h.

17.28.2.11 struct scg_firc_config_t

SCG fast IRC clock configuration. Implements scg_firc_config_t_Class.

Definition at line 432 of file clock_S32K1xx.h.

Data Fields

- [scg_firc_range_t range](#)
- [scg_async_clock_div_t div1](#)
- [scg_async_clock_div_t div2](#)
- bool [enableInStop](#)
- bool [enableInLowPower](#)
- bool [regulator](#)
- bool [locked](#)
- bool [initialize](#)

Field Documentation**17.28.2.11.1 scg_async_clock_div_t div1**

Asynchronous peripheral source.

Definition at line 436 of file clock_S32K1xx.h.

17.28.2.11.2 scg_async_clock_div_t div2

Asynchronous peripheral source.

Definition at line 437 of file clock_S32K1xx.h.

17.28.2.11.3 bool enableInLowPower

FIRC is enable or not in lowpower mode.

Definition at line 440 of file clock_S32K1xx.h.

17.28.2.11.4 bool enableInStop

FIRC is enable or not in stop mode.

Definition at line 439 of file clock_S32K1xx.h.

17.28.2.11.5 bool initialize

Initialize or not the FIRC module.

Definition at line 444 of file clock_S32K1xx.h.

17.28.2.11.6 bool locked

FIRC Control Register can be written.

Definition at line 442 of file clock_S32K1xx.h.

17.28.2.11.7 scg_firc_range_t range

Fast IRC frequency range.

Definition at line 434 of file clock_S32K1xx.h.

17.28.2.11.8 bool regulator

FIRC regulator is enable or not.

Definition at line 441 of file clock_S32K1xx.h.

17.28.2.12 struct scg_spll_config_t

SCG system PLL configuration. Implements scg_spll_config_t_Class.

Definition at line 518 of file clock_S32K1xx.h.

Data Fields

- [scg_spll_monitor_mode_t monitorMode](#)
- [uint8_t prediv](#)
- [uint8_t mult](#)
- [uint8_t src](#)
- [scg_async_clock_div_t div1](#)
- [scg_async_clock_div_t div2](#)
- [bool enableInStop](#)
- [bool locked](#)
- [bool initialize](#)

Field Documentation**17.28.2.12.1 scg_async_clock_div_t div1**

Asynchronous peripheral source.

Definition at line 526 of file clock_S32K1xx.h.

17.28.2.12.2 scg_async_clock_div_t div2

Asynchronous peripheral source.

Definition at line 527 of file clock_S32K1xx.h.

17.28.2.12.3 bool enableInStop

System PLL clock is enable or not in stop mode.

Definition at line 529 of file clock_S32K1xx.h.

17.28.2.12.4 bool initialize

Initialize or not the System PLL module.

Definition at line 532 of file clock_S32K1xx.h.

17.28.2.12.5 bool locked

System PLL Control Register can be written.

Definition at line 531 of file clock_S32K1xx.h.

17.28.2.12.6 scg_spill_monitor_mode_t monitorMode

Clock monitor mode selected.

Definition at line 520 of file clock_S32K1xx.h.

17.28.2.12.7 uint8_t mult

System PLL multiplier.

Definition at line 523 of file clock_S32K1xx.h.

17.28.2.12.8 uint8_t prediv

PLL reference clock divider.

Definition at line 522 of file clock_S32K1xx.h.

17.28.2.12.9 uint8_t src

System PLL source.

Definition at line 524 of file clock_S32K1xx.h.

17.28.2.13 struct scg_rtc_config_t

SCG RTC configuration. Implements scg_rtc_config_t_Class.

Definition at line 539 of file clock_S32K1xx.h.

Data Fields

- uint32_t [rtcClkInFreq](#)
- bool [initialize](#)

Field Documentation

17.28.2.13.1 bool initialize

Initialize or not the RTC.

Definition at line 542 of file clock_S32K1xx.h.

17.28.2.13.2 uint32_t rtcClkInFreq

RTC_CLKIN frequency.

Definition at line 541 of file clock_S32K1xx.h.

17.28.2.14 struct scg_clock_mode_config_t

SCG Clock Mode Configuration structure. Implements scg_clock_mode_config_t_Class.

Definition at line 549 of file clock_S32K1xx.h.

Data Fields

- [scg_system_clock_config_t rccrConfig](#)
- [scg_system_clock_config_t vccrConfig](#)
- [scg_system_clock_config_t hccrConfig](#)
- [scg_system_clock_src_t alternateClock](#)
- [bool initialize](#)

Field Documentation

17.28.2.14.1 [scg_system_clock_src_t alternateClock](#)

Alternate clock used during initialization

Definition at line 554 of file clock_S32K1xx.h.

17.28.2.14.2 [scg_system_clock_config_t hccrConfig](#)

HSRUN Clock Control configuration.

Definition at line 553 of file clock_S32K1xx.h.

17.28.2.14.3 [bool initialize](#)

Initialize or not the Clock Mode Configuration.

Definition at line 555 of file clock_S32K1xx.h.

17.28.2.14.4 [scg_system_clock_config_t rccrConfig](#)

Run Clock Control configuration.

Definition at line 551 of file clock_S32K1xx.h.

17.28.2.14.5 [scg_system_clock_config_t vccrConfig](#)

VLPR Clock Control configuration.

Definition at line 552 of file clock_S32K1xx.h.

17.28.2.15 [struct scg_clockout_config_t](#)

SCG ClockOut Configuration structure. Implements [scg_clockout_config_t_Class](#).

Definition at line 562 of file clock_S32K1xx.h.

Data Fields

- [scg_clockout_src_t source](#)
- [bool initialize](#)

Field Documentation

17.28.2.15.1 [bool initialize](#)

Initialize or not the ClockOut.

Definition at line 565 of file clock_S32K1xx.h.

17.28.2.15.2 [scg_clockout_src_t source](#)

ClockOut source select.

Definition at line 564 of file clock_S32K1xx.h.

17.28.2.16 struct scg_config_t

SCG configure structure. Implements scg_config_t_Class.

Definition at line 572 of file clock_S32K1xx.h.

Data Fields

- [scg_sirc_config_t sircConfig](#)
- [scg_firc_config_t fircConfig](#)
- [scg_sosc_config_t soscConfig](#)
- [scg_spill_config_t spillConfig](#)
- [scg_rtc_config_t rtcConfig](#)
- [scg_clockout_config_t clockOutConfig](#)
- [scg_clock_mode_config_t clockModeConfig](#)

Field Documentation

17.28.2.16.1 scg_clock_mode_config_t clockModeConfig

SCG Clock Mode Configuration.

Definition at line 580 of file clock_S32K1xx.h.

17.28.2.16.2 scg_clockout_config_t clockOutConfig

SCG ClockOut Configuration.

Definition at line 579 of file clock_S32K1xx.h.

17.28.2.16.3 scg_firc_config_t fircConfig

Fast internal reference clock configuration.

Definition at line 575 of file clock_S32K1xx.h.

17.28.2.16.4 scg_rtc_config_t rtcConfig

Real Time Clock configuration.

Definition at line 578 of file clock_S32K1xx.h.

17.28.2.16.5 scg_sirc_config_t sircConfig

Slow internal reference clock configuration.

Definition at line 574 of file clock_S32K1xx.h.

17.28.2.16.6 scg_sosc_config_t soscConfig

System oscillator configuration.

Definition at line 576 of file clock_S32K1xx.h.

17.28.2.16.7 scg_spill_config_t spillConfig

System Phase locked loop configuration.

Definition at line 577 of file clock_S32K1xx.h.

17.28.2.17 struct peripheral_clock_config_t

PCC peripheral instance clock configuration. Implements peripheral_clock_config_t_Class.

Definition at line 632 of file clock_S32K1xx.h.

Data Fields

- `clock_names_t` [clockName](#)
- `bool` [clkGate](#)
- `peripheral_clock_source_t` [clkSrc](#)
- `peripheral_clock_frac_t` [frac](#)
- `peripheral_clock_divider_t` [divider](#)

Field Documentation

17.28.2.17.1 `bool` [clkGate](#)

Peripheral clock gate.

Definition at line 642 of file `clock_S32K1xx.h`.

17.28.2.17.2 `peripheral_clock_source_t` [clkSrc](#)

Peripheral clock source.

Definition at line 643 of file `clock_S32K1xx.h`.

17.28.2.17.3 `clock_names_t` [clockName](#)

Definition at line 641 of file `clock_S32K1xx.h`.

17.28.2.17.4 `peripheral_clock_divider_t` [divider](#)

Peripheral clock divider value.

Definition at line 645 of file `clock_S32K1xx.h`.

17.28.2.17.5 `peripheral_clock_frac_t` [frac](#)

Peripheral clock fractional value.

Definition at line 644 of file `clock_S32K1xx.h`.

17.28.2.18 `struct` [pcc_config_t](#)

PCC configuration. Implements `pcc_config_t_Class`.

Definition at line 651 of file `clock_S32K1xx.h`.

Data Fields

- `uint32_t` [count](#)
- `peripheral_clock_config_t` * [peripheralClocks](#)

Field Documentation

17.28.2.18.1 `uint32_t` [count](#)

Number of peripherals to be configured.

Definition at line 653 of file `clock_S32K1xx.h`.

17.28.2.18.2 `peripheral_clock_config_t`* [peripheralClocks](#)

Pointer to the peripheral clock configurations array.

Definition at line 654 of file `clock_S32K1xx.h`.

17.28.2.19 struct pmc_lpo_clock_config_t

PMC LPO configuration. Implements pmc_lpo_clock_config_t_Class.

Definition at line 660 of file clock_S32K1xx.h.

Data Fields

- bool [initialize](#)
- bool [enable](#)
- int8_t [trimValue](#)

Field Documentation

17.28.2.19.1 bool enable

Enable/disable LPO

Definition at line 663 of file clock_S32K1xx.h.

17.28.2.19.2 bool initialize

Initialize or not the PMC LPO settings.

Definition at line 662 of file clock_S32K1xx.h.

17.28.2.19.3 int8_t trimValue

LPO trimming value

Definition at line 664 of file clock_S32K1xx.h.

17.28.2.20 struct pmc_config_t

PMC configure structure. Implements pmc_config_t_Class.

Definition at line 671 of file clock_S32K1xx.h.

Data Fields

- [pmc_lpo_clock_config_t](#) lpoClockConfig

Field Documentation

17.28.2.20.1 pmc_lpo_clock_config_t lpoClockConfig

Low Power Clock configuration.

Definition at line 673 of file clock_S32K1xx.h.

17.28.2.21 struct clock_manager_user_config_t

Clock configuration structure. Implements clock_manager_user_config_t_Class.

Definition at line 680 of file clock_S32K1xx.h.

Data Fields

- [scg_config_t](#) scgConfig
- [sim_clock_config_t](#) simConfig
- [pcc_config_t](#) pccConfig
- [pmc_config_t](#) pmcConfig

Field Documentation

17.28.2.21.1 pcc_config_t pccConfig

PCC Clock configuration.

Definition at line 684 of file clock_S32K1xx.h.

17.28.2.21.2 pmc_config_t pmcConfig

PMC Clock configuration.

Definition at line 685 of file clock_S32K1xx.h.

17.28.2.21.3 scg_config_t scgConfig

SCG Clock configuration.

Definition at line 682 of file clock_S32K1xx.h.

17.28.2.21.4 sim_clock_config_t simConfig

SIM Clock configuration.

Definition at line 683 of file clock_S32K1xx.h.

17.28.2.22 struct module_clk_config_t

module clock configuration. Implements module_clk_config_t_Class

Definition at line 720 of file clock_S32K1xx.h.

Data Fields

- bool [gating](#)
- clock_names_t [source](#)
- uint16_t [mul](#)
- uint16_t [div](#)

Field Documentation

17.28.2.22.1 uint16_t div

Divider (some modules don't have divider)

Definition at line 725 of file clock_S32K1xx.h.

17.28.2.22.2 bool gating

Clock gating.

Definition at line 722 of file clock_S32K1xx.h.

17.28.2.22.3 uint16_t mul

Multiplier (some modules don't have fractional)

Definition at line 724 of file clock_S32K1xx.h.

17.28.2.22.4 clock_names_t source

Clock source input (some modules don't have protocol clock)

Definition at line 723 of file clock_S32K1xx.h.

17.28.2.23 struct sys_clk_config_t

System clock configuration. Implements sys_clk_config_t_Class.

Definition at line 733 of file clock_S32K1xx.h.

Data Fields

- clock_names_t [src](#)
- uint16_t [dividers](#) [[SYS_CLK_MAX_NO](#)]

Field Documentation

17.28.2.23.1 uint16_t dividers[SYS_CLK_MAX_NO]

System clock dividers. Value by which system clock is divided. 0 means that system clock is not divided.

Definition at line 736 of file clock_S32K1xx.h.

17.28.2.23.2 clock_names_t src

System clock source.

Definition at line 735 of file clock_S32K1xx.h.

17.28.2.24 struct clock_source_config_t

Clock source configuration. Implements clock_source_config_t_Class.

Definition at line 743 of file clock_S32K1xx.h.

Data Fields

- bool [enable](#)
- [xosc_ref_t](#) [refClk](#)
- [uint32_t](#) [refFreq](#)
- [uint16_t](#) [mul](#)
- [uint16_t](#) [div](#)
- [uint16_t](#) [outputDiv1](#)
- [uint16_t](#) [outputDiv2](#)

Field Documentation

17.28.2.24.1 uint16_t div

Divider. It applies to PLL clock sources. Valid range is 1-8.

Definition at line 749 of file clock_S32K1xx.h.

17.28.2.24.2 bool enable

Enable/disable clock source.

Definition at line 745 of file clock_S32K1xx.h.

17.28.2.24.3 uint16_t mul

Multiplier. It applies to PLL clock sources. Valid range is 16 - 47.

Definition at line 748 of file clock_S32K1xx.h.

17.28.2.24.4 uint16_t outputDiv1

First output divider. It's used as protocol clock by modules. Zero means that divider is disabled. / Possible values 0(disabled), 1, 2, 4, 8, 16, 32, 64; all the other values are not valid. /

Definition at line 751 of file clock_S32K1xx.h.

17.28.2.24.5 uint16_t outputDiv2

Second output divider. It's used as protocol clock by modules. Zero means that divider is disabled. / Possible values 0(disabled), 1, 2, 4, 8, 16, 32, 64; all the other values are not valid. /

Definition at line 754 of file clock_S32K1xx.h.

17.28.2.24.6 xosc_ref_t refClk

Bypass option. It applies to external oscillator clock sources

Definition at line 746 of file clock_S32K1xx.h.

17.28.2.24.7 uint32_t refFreq

Frequency of the input reference clock. It applies to external oscillator clock sources

Definition at line 747 of file clock_S32K1xx.h.

17.28.2.25 struct clock_notify_struct_t

Clock notification structure passed to clock callback function. Implements clock_notify_struct_t_Class.

Definition at line 797 of file clock_S32K1xx.h.

Data Fields

- [uint8_t targetClockConfigIndex](#)
- [clock_manager_policy_t policy](#)
- [clock_manager_notify_t notifyType](#)

Field Documentation

17.28.2.25.1 clock_manager_notify_t notifyType

Clock notification type.

Definition at line 801 of file clock_S32K1xx.h.

17.28.2.25.2 clock_manager_policy_t policy

Clock transition policy.

Definition at line 800 of file clock_S32K1xx.h.

17.28.2.25.3 uint8_t targetClockConfigIndex

Target clock configuration index.

Definition at line 799 of file clock_S32K1xx.h.

17.28.2.26 struct clock_manager_callback_user_config_t

Structure for callback function and its parameter. Implements clock_manager_callback_user_config_t_Class.

Definition at line 814 of file clock_S32K1xx.h.

Data Fields

- [clock_manager_callback_t callback](#)
- [clock_manager_callback_type_t callbackType](#)
- void * [callbackData](#)

Field Documentation

17.28.2.26.1 `clock_manager_callback_t` callback

Entry of callback function.

Definition at line 816 of file `clock_S32K1xx.h`.

17.28.2.26.2 `void* callbackData`

Parameter of callback function.

Definition at line 818 of file `clock_S32K1xx.h`.

17.28.2.26.3 `clock_manager_callback_type_t` callbackType

Callback type.

Definition at line 817 of file `clock_S32K1xx.h`.

17.28.2.27 `struct clock_manager_state_t`

Clock manager state structure. Implements `clock_manager_state_t_Class`.

Definition at line 825 of file `clock_S32K1xx.h`.

Data Fields

- `clock_manager_user_config_t` const ** `configTable`
- `uint8_t` `clockConfigNum`
- `uint8_t` `curConfigIndex`
- `clock_manager_callback_user_config_t` ** `callbackConfig`
- `uint8_t` `callbackNum`
- `uint8_t` `errorCallbackIndex`

Field Documentation

17.28.2.27.1 `clock_manager_callback_user_config_t**` callbackConfig

Pointer to callback table.

Definition at line 830 of file `clock_S32K1xx.h`.

17.28.2.27.2 `uint8_t` callbackNum

Number of clock callbacks.

Definition at line 831 of file `clock_S32K1xx.h`.

17.28.2.27.3 `uint8_t` clockConfigNum

Number of clock configurations.

Definition at line 828 of file `clock_S32K1xx.h`.

17.28.2.27.4 `clock_manager_user_config_t` const** configTable

Pointer to clock configure table.

Definition at line 827 of file `clock_S32K1xx.h`.

17.28.2.27.5 `uint8_t` curConfigIndex

Index of current configuration.

Definition at line 829 of file `clock_S32K1xx.h`.

17.28.2.27.6 uint8_t errorCallbackIndex

Index of callback returns error.

Definition at line 832 of file clock_S32K1xx.h.

17.28.3 Macro Definition Documentation

17.28.3.1 #define BUS_CLK_INDEX 1U

Definition at line 69 of file clock_S32K1xx.h.

17.28.3.2 #define CLK_SRC_FIRC 0x03U

SCGFIRCLK - Fast IRC Clock

Definition at line 591 of file clock_S32K1xx.h.

17.28.3.3 #define CLK_SRC_FIRC_DIV1 0x03U

SCGFIRCLK - Fast IRC Clock

Definition at line 595 of file clock_S32K1xx.h.

17.28.3.4 #define CLK_SRC_FIRC_DIV2 0x03U

SCGFIRCLK - Fast IRC Clock

Definition at line 599 of file clock_S32K1xx.h.

17.28.3.5 #define CLK_SRC_OFF 0x00U

Clock is off

Definition at line 588 of file clock_S32K1xx.h.

17.28.3.6 #define CLK_SRC_SIRC 0x02U

SCGIRCLK - Slow IRC Clock

Definition at line 590 of file clock_S32K1xx.h.

17.28.3.7 #define CLK_SRC_SIRC_DIV1 0x02U

SCGIRCLK - Slow IRC Clock

Definition at line 594 of file clock_S32K1xx.h.

17.28.3.8 #define CLK_SRC_SIRC_DIV2 0x02U

SCGIRCLK - Slow IRC Clock

Definition at line 598 of file clock_S32K1xx.h.

17.28.3.9 #define CLK_SRC_SOSC 0x01U

OSCCLK - System Oscillator Bus Clock

Definition at line 589 of file clock_S32K1xx.h.

17.28.3.10 #define CLK_SRC_SOSC_DIV1 0x01U

OSCCLK - System Oscillator Bus Clock

Definition at line 593 of file clock_S32K1xx.h.

17.28.3.11 `#define CLK_SRC_SOSC_DIV2 0x01U`

OSCCLK - System Oscillator Bus Clock

Definition at line 597 of file clock_S32K1xx.h.

17.28.3.12 `#define CLK_SRC_SPLL 0x06U`

SCGPCLK System PLL clock

Definition at line 592 of file clock_S32K1xx.h.

17.28.3.13 `#define CLK_SRC_SPLL_DIV1 0x06U`

SCGPCLK System PLL clock

Definition at line 596 of file clock_S32K1xx.h.

17.28.3.14 `#define CLK_SRC_SPLL_DIV2 0x06U`

SCGPCLK System PLL clock

Definition at line 600 of file clock_S32K1xx.h.

17.28.3.15 `#define CORE_CLK_INDEX 0U`

Definition at line 68 of file clock_S32K1xx.h.

17.28.3.16 `#define NUMBER_OF_TCLK_INPUTS 3U`

TCLK clock frequency.

Definition at line 57 of file clock_S32K1xx.h.

17.28.3.17 `#define SLOW_CLK_INDEX 2U`

Definition at line 70 of file clock_S32K1xx.h.

17.28.3.18 `#define SYS_CLK_MAX_NO 3U`

The maximum number of system clock dividers and system clock divider indexes.

Definition at line 67 of file clock_S32K1xx.h.

17.28.4 Typedef Documentation

17.28.4.1 `typedef status_t(* clock_manager_callback_t)(clock_notify_struct_t *notify, void *callbackData)`

Type of clock callback functions.

Definition at line 807 of file clock_S32K1xx.h.

17.28.4.2 `typedef clock_manager_user_config_t clock_user_config_t`

Definition at line 688 of file clock_S32K1xx.h.

17.28.4.3 `typedef uint8_t peripheral_clock_source_t`

PCC clock source select Implements peripheral_clock_source_t_Class.

Definition at line 586 of file clock_S32K1xx.h.

17.28.5 Enumeration Type Documentation

17.28.5.1 enum clock_manager_callback_type_t

The callback type, indicates what kinds of notification this callback handles. Implements clock_manager_callback_type_t_Class.

Enumerator

CLOCK_MANAGER_CALLBACK_BEFORE Callback handles BEFORE notification.

CLOCK_MANAGER_CALLBACK_AFTER Callback handles AFTER notification.

CLOCK_MANAGER_CALLBACK_BEFORE_AFTER Callback handles BEFORE and AFTER notification

Definition at line 776 of file clock_S32K1xx.h.

17.28.5.2 enum clock_manager_notify_t

The clock notification type. Implements clock_manager_notify_t_Class.

Enumerator

CLOCK_MANAGER_NOTIFY_RECOVER Notify IP to recover to previous work state.

CLOCK_MANAGER_NOTIFY_BEFORE Notify IP that system will change clock setting.

CLOCK_MANAGER_NOTIFY_AFTER Notify IP that have changed to new clock setting.

Definition at line 765 of file clock_S32K1xx.h.

17.28.5.3 enum clock_manager_policy_t

Clock transition policy. Implements clock_manager_policy_t_Class.

Enumerator

CLOCK_MANAGER_POLICY_AGREEMENT Clock transfers gracefully.

CLOCK_MANAGER_POLICY_FORCIBLE Clock transfers forcefully.

Definition at line 787 of file clock_S32K1xx.h.

17.28.5.4 enum clock_trace_src_t

Debug trace clock source select Implements clock_trace_src_t_Class.

Enumerator

CLOCK_TRACE_SRC_CORE_CLK core clock

Definition at line 203 of file clock_S32K1xx.h.

17.28.5.5 enum peripheral_clock_divider_t

PCC divider value select Implements peripheral_clock_divider_t_Class.

Enumerator

DIVIDE_BY_ONE Divide by 1 (pass-through, no clock divide)

DIVIDE_BY_TWO Divide by 2

DIVIDE_BY_THREE Divide by 3

DIVIDE_BY_FOUR Divide by 4

DIVIDE_BY_FIVE Divide by 5

DIVIDE_BY_SIX Divide by 6

DIVIDE_BY_SEVEN Divide by 7

DIVIDE_BY_EIGHTH Divide by 8

Definition at line 617 of file clock_S32K1xx.h.

17.28.5.6 enum peripheral_clock_frac_t

PCC fractional value select Implements peripheral_clock_frac_t_Class.

Enumerator

MULTIPLY_BY_ONE Fractional value is zero

MULTIPLY_BY_TWO Fractional value is one

Definition at line 608 of file clock_S32K1xx.h.

17.28.5.7 enum pwr_modes_t

Power mode. Implements pwr_modes_t_Class.

Enumerator

NO_MODE

RUN_MODE

VLPR_MODE

HSRUN_MODE

STOP_MODE

VLPS_MODE

ALL_MODES

Definition at line 694 of file clock_S32K1xx.h.

17.28.5.8 enum scg_async_clock_div_t

SCG asynchronous clock divider value. Implements scg_async_clock_div_t_Class.

Enumerator

SCG_ASYNC_CLOCK_DISABLE Clock output is disabled.

SCG_ASYNC_CLOCK_DIV_BY_1 Divided by 1.

SCG_ASYNC_CLOCK_DIV_BY_2 Divided by 2.

SCG_ASYNC_CLOCK_DIV_BY_4 Divided by 4.

SCG_ASYNC_CLOCK_DIV_BY_8 Divided by 8.

SCG_ASYNC_CLOCK_DIV_BY_16 Divided by 16.

SCG_ASYNC_CLOCK_DIV_BY_32 Divided by 32.

SCG_ASYNC_CLOCK_DIV_BY_64 Divided by 64.

Definition at line 312 of file clock_S32K1xx.h.

17.28.5.9 enum scg_clockout_src_t

SCG ClockOut type. Implements scg_clockout_src_t_Class.

Enumerator

SCG_CLOCKOUT_SRC_SCG_SLOW SCG SLOW.

SCG_CLOCKOUT_SRC_SOSC System OSC.

SCG_CLOCKOUT_SRC_SIRC Slow IRC.

SCG_CLOCKOUT_SRC_FIRC Fast IRC.

SCG_CLOCKOUT_SRC_SPLL System PLL.

Definition at line 297 of file clock_S32K1xx.h.

17.28.5.10 enum `scg_firc_range_t`

SCG fast IRC clock frequency range. Implements `scg_firc_range_t_Class`.

Enumerator

SCG_FIRC_RANGE_48M Fast IRC is trimmed to 48MHz.

Definition at line 423 of file `clock_S32K1xx.h`.

17.28.5.11 enum `scg_sirc_range_t`

SCG slow IRC clock frequency range. Implements `scg_sirc_range_t_Class`.

Enumerator

SCG_SIRC_RANGE_HIGH Slow IRC high range clock (8 MHz).

Definition at line 396 of file `clock_S32K1xx.h`.

17.28.5.12 enum `scg_sosc_ext_ref_t`

SCG OSC external reference clock select. Implements `scg_sosc_ext_ref_t_Class`.

Enumerator

SCG_SOSC_REF_EXT External reference clock requested

SCG_SOSC_REF_OSC Internal oscillator of OSC requested.

Definition at line 360 of file `clock_S32K1xx.h`.

17.28.5.13 enum `scg_sosc_gain_t`

SCG OSC high gain oscillator select. Implements `scg_sosc_gain_t_Class`.

Enumerator

SCG_SOSC_GAIN_LOW Configure crystal oscillator for low-power operation

SCG_SOSC_GAIN_HIGH Configure crystal oscillator for high-gain operation

Definition at line 350 of file `clock_S32K1xx.h`.

17.28.5.14 enum `scg_sosc_monitor_mode_t`

SCG system OSC monitor mode. Implements `scg_sosc_monitor_mode_t_Class`.

Enumerator

SCG_SOSC_MONITOR_DISABLE Monitor disable.

SCG_SOSC_MONITOR_INT Interrupt when system OSC error detected.

SCG_SOSC_MONITOR_RESET Reset when system OSC error detected.

Definition at line 329 of file `clock_S32K1xx.h`.

17.28.5.15 enum `scg_sosc_range_t`

SCG OSC frequency range select Implements `scg_sosc_range_t_Class`.

Enumerator

SCG_SOSC_RANGE_MID Medium frequency range selected for the crystal OSC (4 Mhz to 8 Mhz).

SCG_SOSC_RANGE_HIGH High frequency range selected for the crystal OSC (8 Mhz to 40 Mhz).

Definition at line 340 of file `clock_S32K1xx.h`.

17.28.5.16 enum scg_spll_clock_multiply_t

SCG system PLL multiplier.

Enumerator

SCG_SPLL_CLOCK_MULTIPLY_BY_16
SCG_SPLL_CLOCK_MULTIPLY_BY_17
SCG_SPLL_CLOCK_MULTIPLY_BY_18
SCG_SPLL_CLOCK_MULTIPLY_BY_19
SCG_SPLL_CLOCK_MULTIPLY_BY_20
SCG_SPLL_CLOCK_MULTIPLY_BY_21
SCG_SPLL_CLOCK_MULTIPLY_BY_22
SCG_SPLL_CLOCK_MULTIPLY_BY_23
SCG_SPLL_CLOCK_MULTIPLY_BY_24
SCG_SPLL_CLOCK_MULTIPLY_BY_25
SCG_SPLL_CLOCK_MULTIPLY_BY_26
SCG_SPLL_CLOCK_MULTIPLY_BY_27
SCG_SPLL_CLOCK_MULTIPLY_BY_28
SCG_SPLL_CLOCK_MULTIPLY_BY_29
SCG_SPLL_CLOCK_MULTIPLY_BY_30
SCG_SPLL_CLOCK_MULTIPLY_BY_31
SCG_SPLL_CLOCK_MULTIPLY_BY_32
SCG_SPLL_CLOCK_MULTIPLY_BY_33
SCG_SPLL_CLOCK_MULTIPLY_BY_34
SCG_SPLL_CLOCK_MULTIPLY_BY_35
SCG_SPLL_CLOCK_MULTIPLY_BY_36
SCG_SPLL_CLOCK_MULTIPLY_BY_37
SCG_SPLL_CLOCK_MULTIPLY_BY_38
SCG_SPLL_CLOCK_MULTIPLY_BY_39
SCG_SPLL_CLOCK_MULTIPLY_BY_40
SCG_SPLL_CLOCK_MULTIPLY_BY_41
SCG_SPLL_CLOCK_MULTIPLY_BY_42
SCG_SPLL_CLOCK_MULTIPLY_BY_43
SCG_SPLL_CLOCK_MULTIPLY_BY_44
SCG_SPLL_CLOCK_MULTIPLY_BY_45
SCG_SPLL_CLOCK_MULTIPLY_BY_46
SCG_SPLL_CLOCK_MULTIPLY_BY_47

Definition at line 478 of file clock_S32K1xx.h.

17.28.5.17 enum scg_spll_clock_prediv_t

SCG system PLL predivider.

Enumerator

SCG_SPLL_CLOCK_PREDIV_BY_1
SCG_SPLL_CLOCK_PREDIV_BY_2

SCG_SPLL_CLOCK_PREDIV_BY_3
SCG_SPLL_CLOCK_PREDIV_BY_4
SCG_SPLL_CLOCK_PREDIV_BY_5
SCG_SPLL_CLOCK_PREDIV_BY_6
SCG_SPLL_CLOCK_PREDIV_BY_7
SCG_SPLL_CLOCK_PREDIV_BY_8

Definition at line 462 of file clock_S32K1xx.h.

17.28.5.18 enum scg_spll_monitor_mode_t

SCG system PLL monitor mode. Implements scg_spll_monitor_mode_t_Class.

Enumerator

SCG_SPLL_MONITOR_DISABLE Monitor disable.
SCG_SPLL_MONITOR_INT Interrupt when system PLL error detected.
SCG_SPLL_MONITOR_RESET Reset when system PLL error detected.

Definition at line 451 of file clock_S32K1xx.h.

17.28.5.19 enum scg_system_clock_div_t

SCG system clock divider value. Implements scg_system_clock_div_t_Class.

Enumerator

SCG_SYSTEM_CLOCK_DIV_BY_1 Divided by 1.
SCG_SYSTEM_CLOCK_DIV_BY_2 Divided by 2.
SCG_SYSTEM_CLOCK_DIV_BY_3 Divided by 3.
SCG_SYSTEM_CLOCK_DIV_BY_4 Divided by 4.
SCG_SYSTEM_CLOCK_DIV_BY_5 Divided by 5.
SCG_SYSTEM_CLOCK_DIV_BY_6 Divided by 6.
SCG_SYSTEM_CLOCK_DIV_BY_7 Divided by 7.
SCG_SYSTEM_CLOCK_DIV_BY_8 Divided by 8.
SCG_SYSTEM_CLOCK_DIV_BY_9 Divided by 9.
SCG_SYSTEM_CLOCK_DIV_BY_10 Divided by 10.
SCG_SYSTEM_CLOCK_DIV_BY_11 Divided by 11.
SCG_SYSTEM_CLOCK_DIV_BY_12 Divided by 12.
SCG_SYSTEM_CLOCK_DIV_BY_13 Divided by 13.
SCG_SYSTEM_CLOCK_DIV_BY_14 Divided by 14.
SCG_SYSTEM_CLOCK_DIV_BY_15 Divided by 15.
SCG_SYSTEM_CLOCK_DIV_BY_16 Divided by 16.

Definition at line 256 of file clock_S32K1xx.h.

17.28.5.20 enum scg_system_clock_src_t

SCG system clock source. Implements scg_system_clock_src_t_Class.

Enumerator

SCG_SYSTEM_CLOCK_SRC_SYS_OSC System OSC.
SCG_SYSTEM_CLOCK_SRC_SIRC Slow IRC.
SCG_SYSTEM_CLOCK_SRC_FIRC Fast IRC.
SCG_SYSTEM_CLOCK_SRC_NONE MAX value.

Definition at line 241 of file clock_S32K1xx.h.

17.28.5.21 enum **sim_clkout_div_t**

SIM CLKOUT divider Implements **sim_clkout_div_t_Class**.

Enumerator

SIM_CLKOUT_DIV_BY_1 Divided by 1
SIM_CLKOUT_DIV_BY_2 Divided by 2
SIM_CLKOUT_DIV_BY_3 Divided by 3
SIM_CLKOUT_DIV_BY_4 Divided by 4
SIM_CLKOUT_DIV_BY_5 Divided by 5
SIM_CLKOUT_DIV_BY_6 Divided by 6
SIM_CLKOUT_DIV_BY_7 Divided by 7
SIM_CLKOUT_DIV_BY_8 Divided by 8

Definition at line 125 of file clock_S32K1xx.h.

17.28.5.22 enum **sim_clkout_src_t**

SIM CLKOUT select Implements **sim_clkout_src_t_Class**.

Enumerator

SIM_CLKOUT_SEL_SYSTEM_SCG_CLKOUT SCG CLKOUT
SIM_CLKOUT_SEL_SYSTEM_SOSC_DIV2_CLK SOSC DIV2 CLK
SIM_CLKOUT_SEL_SYSTEM_SIRC_DIV2_CLK SIRC DIV2 CLK
SIM_CLKOUT_SEL_SYSTEM_FIRC_DIV2_CLK FIRC DIV2 CLK
SIM_CLKOUT_SEL_SYSTEM_HCLK HCLK
SIM_CLKOUT_SEL_SYSTEM_SPLL_DIV2_CLK SPLL DIV2 CLK
SIM_CLKOUT_SEL_SYSTEM_BUS_CLK BUS_CLK
SIM_CLKOUT_SEL_SYSTEM_LPO_128K_CLK LPO_CLK 128 Khz
SIM_CLKOUT_SEL_SYSTEM_LPO_CLK LPO_CLK as selected by SIM LPO CLK Select
SIM_CLKOUT_SEL_SYSTEM_RTC_CLK RTC CLK as selected by SIM CLK 32 KHz Select

Definition at line 100 of file clock_S32K1xx.h.

17.28.5.23 enum **sim_lpclock_sel_src_t**

SIM LPOCLKSEL clock source select Implements **sim_lpclock_sel_src_t_Class**.

Enumerator

SIM_LPO_CLK_SEL_LPO_128K 128 kHz LPO clock
SIM_LPO_CLK_SEL_NO_CLOCK No clock
SIM_LPO_CLK_SEL_LPO_32K 32 kHz LPO clock which is divided by the 128 kHz LPO clock
SIM_LPO_CLK_SEL_LPO_1K 1 kHz LPO clock which is divided by the 128 kHz LPO clock

Definition at line 88 of file clock_S32K1xx.h.

17.28.5.24 enum `sim_rtc_clk_sel_src_t`

SIM CLK32KSEL clock source select Implements `sim_rtc_clk_sel_src_t_Class`.

Enumerator

SIM_RTCCLK_SEL_SOSCDIV1_CLK SOSCDIV1 clock

SIM_RTCCLK_SEL_LPO_32K 32 kHz LPO clock

SIM_RTCCLK_SEL_RTC_CLKIN RTC_CLKIN clock

SIM_RTCCLK_SEL_FIRCDIV1_CLK FIRCDIV1 clock

Definition at line 76 of file `clock_S32K1xx.h`.

17.28.5.25 enum `xosc_ref_t`

XOSC reference clock select (internal oscillator is bypassed or not) Implements `xosc_ref_t_Class`.

Enumerator

XOSC_EXT_REF Internal oscillator is bypassed, external reference clock requested.

XOSC_INT_OSC Internal oscillator of XOSC requested.

Definition at line 711 of file `clock_S32K1xx.h`.

17.28.6 Function Documentation

17.28.6.1 void `CLOCK_DRV_GetSystemClockSource (sys_clk_config_t * sysClkConfig)`

Gets the system clock source.

This function gets the current system clock source.

Returns

Value of the current system clock source.

Definition at line 3713 of file `clock_S32K1xx.c`.

17.28.6.2 status_t `CLOCK_DRV_SetClockSource (clock_names_t clockSource, const clock_source_config_t * clkSrcConfig)`

This function configures a clock source.

The clock source is configured based on the provided configuration. All values from the previous configuration of clock source are overwritten. If no configuration is provided, then a default one is used.

Parameters

in	<i>clockSource</i>	Clock name of the configured clock source
in	<i>clkSrcConfig</i>	Pointer to the configuration structure

Returns

Status of clock source initialization

Definition at line 4065 of file `clock_S32K1xx.c`.

17.28.6.3 void CLOCK_DRV_SetModuleClock (clock_names_t *peripheralClock*, const module_clk_config_t *
moduleClkConfig)

Configures module clock.

This function configures a module clock according to the configuration. If no configuration is provided (*moduleClkConfig* is null), then a default one is used *moduleClkConfig* must be passed as null when module doesn't support protocol clock.

Parameters

in	<i>peripheralClock</i>	Clock name of the configured module clock
in	<i>moduleClkConfig</i>	Pointer to the configuration structure.

Definition at line 3490 of file clock_S32K1xx.c.

17.28.6.4 `status_t CLOCK_DRV_SetSystemClock (const pwr_modes_t * mode, const sys_clk_config_t * sysClkConfig)`

Configures the system clocks.

This function configures the system clocks (core, bus and flash clocks) in the specified power mode. If no power mode is specified (null parameter) then it is the current power mode.

Parameters

in	<i>mode</i>	Pointer to power mode for which the configured system clocks apply
in	<i>sysClkConfig</i>	Pointer to the system clocks configuration structure.

Definition at line 3644 of file clock_S32K1xx.c.

17.28.6.5 `uint8_t CLOCK_SYS_GetCurrentConfiguration (void)`

Get current system clock configuration.

Returns

Current clock configuration index.

Definition at line 4292 of file clock_S32K1xx.c.

17.28.6.6 `clock_manager_callback_user_config_t* CLOCK_SYS_GetErrorCallback (void)`

Get the callback which returns error in last clock switch.

When graceful policy is used, if some IP is not ready to change clock setting, the callback will return error and system stay in current configuration. Applications can use this function to check which IP callback returns error.

Returns

Pointer to the callback which returns error.

Definition at line 4304 of file clock_S32K1xx.c.

17.28.6.7 `status_t CLOCK_SYS_GetFreq (clock_names_t clockName, uint32_t * frequency)`

Wrapper over CLOCK_DRV_GetFreq function. It's part of the old API.

Parameters

in	<i>clockName</i>	Clock names defined in clock_names_t
out	<i>frequency</i>	Returned clock frequency value in Hertz

Returns

status Error code defined in status_t

Definition at line 4327 of file clock_S32K1xx.c.

17.28.6.8 `status_t CLOCK_SYS_Init (clock_manager_user_config_t const ** clockConfigsPtr, uint8_t configsNumber, clock_manager_callback_user_config_t ** callbacksPtr, uint8_t callbacksNumber)`

Install pre-defined clock configurations.

This function installs the pre-defined clock configuration table to clock manager.

Parameters

in	<i>clockConfigsPtr</i>	Pointer to the clock configuration table.
in	<i>configsNumber</i>	Number of clock configurations in table.
in	<i>callbacksPtr</i>	Pointer to the callback configuration table.
in	<i>callbacks↔ Number</i>	Number of callback configurations in table.

Returns

Error code.

Definition at line 4140 of file clock_S32K1xx.c.

17.28.6.9 status_t CLOCK_SYS_SetConfiguration (clock_manager_user_config_t const * config)

Set system clock configuration.

This function sets the system to target configuration, it only sets the clock modules registers for clock mode change, but not send notifications to drivers. This function is different by different SoCs.

Parameters

in	<i>config</i>	Target configuration.
----	---------------	-----------------------

Returns

Error code.

Note

If external clock is used in the target mode, please make sure it is enabled, for example, if the external oscillator is used, please setup EREFS/HGO correctly and make sure OSCINIT is set. This function should be called only on run mode.

Definition at line 4339 of file clock_S32K1xx.c.

17.28.6.10 status_t CLOCK_SYS_UpdateConfiguration (uint8_t targetConfigIndex, clock_manager_policy_t policy)

Set system clock configuration according to pre-defined structure.

This function sets system to target clock configuration; before transition, clock manager will send notifications to all drivers registered to the callback table. When graceful policy is used, if some drivers are not ready to change, clock transition will not occur, all drivers still work in previous configuration and error is returned. When forceful policy is used, all drivers should stop work and system changes to new clock configuration. The function should be called only on run mode.

Parameters

in	<i>targetConfig↔ Index</i>	Index of the clock configuration.
in	<i>policy</i>	Transaction policy, graceful or forceful.

Returns

Error code.

Note

If external clock is used in the target mode, please make sure it is enabled, for example, if the external oscillator is used, please setup EREFS/HGO correctly and make sure OSCINIT is set.

Definition at line 4173 of file clock_S32K1xx.c.

17.28.7 Variable Documentation

17.28.7.1 `uint32_t g_RtcClkInFreq`

RTC_CLKIN clock frequency.

Definition at line 81 of file `clock_S32K1xx.c`.

17.28.7.2 `uint32_t g_TClkFreq[NUMBER_OF_TCLK_INPUTS]`

TCLKx clocks

Definition at line 78 of file `clock_S32K1xx.c`.

17.28.7.3 `uint32_t g_xtal0ClkFreq`

EXTAL0 clock frequency.

Definition at line 84 of file `clock_S32K1xx.c`.

17.28.7.4 `const uint8_t peripheralFeaturesList[CLOCK_NAME_COUNT]`

Peripheral features list Constant array storing the mappings between clock names of the peripherals and feature lists.

Definition at line 432 of file `clock_S32K1xx.c`.

17.29 Common Core API.

17.29.1 Detailed Description

This group contains general core APIs that used for both protocol LIN 2.1 and J2602.

Modules

- [Driver and cluster management](#)
API perform the initialization of the LIN core.
- [Interface management](#)
This group contains APIs that help users manage interface(s) in LIN node.
- [Notification](#)
This group contains APIs that let users know when a signal's value changed.
- [Schedule management](#)
This group contains APIs that help users manage schedule tables in master node only.
- [Signal interaction](#)
This group contains APIs that help users interact with signals of LIN node.
- [User provided call-outs](#)
This group contains APIs which may be called from within the LIN module in order to enable/disable LIN communication interrupts.

Macros

- `#define SAVE_CONFIG_SET 0x0040U`
- `#define EVENT_TRIGGER_COLLISION_SET 0x0020U`
- `#define BUS_ACTIVITY_SET 0x0010U`
- `#define GO_TO_SLEEP_SET 0x0008U`
- `#define OVERRUN 0x0004U`
- `#define SUCCESSFULL_TRANSFER 0x0002U`
- `#define ERROR_IN_RESPONSE 0x0001U`

17.29.2 Macro Definition Documentation

17.29.2.1 `#define BUS_ACTIVITY_SET 0x0010U`

Bus activity

Definition at line 32 of file `lin_common_api.h`.

17.29.2.2 `#define ERROR_IN_RESPONSE 0x0001U`

Error in response

Definition at line 36 of file `lin_common_api.h`.

17.29.2.3 `#define EVENT_TRIGGER_COLLISION_SET 0x0020U`

Event triggered frame collision

Definition at line 31 of file `lin_common_api.h`.

17.29.2.4 `#define GO_TO_SLEEP_SET 0x0008U`

Go to sleep

Definition at line 33 of file `lin_common_api.h`.

17.29.2.5 #define OVERRUN 0x0004U

Overflow

Definition at line 34 of file lin_common_api.h.

17.29.2.6 #define SAVE_CONFIG_SET 0x0040U

Save configuration

Definition at line 30 of file lin_common_api.h.

17.29.2.7 #define SUCCESSFULL_TRANSFER 0x0002U

Successful transfer

Definition at line 35 of file lin_common_api.h.

17.30 Common Transport Layer API

17.30.1 Detailed Description

Contains Transport Layer APIs that used for both protocols LIN 2.1 and J2602.

Modules

- [Cooked API](#)

Cooked processing of diagnostic messages manages one complete message at a time.

- [Initialization](#)

Initialize transport layer (queues, status, ...).

- [Raw API](#)

The raw API is operating on PDU level and it is typically used to gateway PDUs between CAN and LIN.

Macros

- `#define LD_READ_OK 0x33U`
- `#define LD_LENGTH_TOO_SHORT 0x34U`
- `#define LD_DATA_ERROR 0x43U`
- `#define LD_LENGTH_NOT_CORRECT 0x44U`
- `#define LD_SET_OK 0x45U`
- `#define SERVICE_TARGET_RESET 0xB5U`
- `#define RES_POSITIVE 0x40U`
- `#define LIN_PRODUCT_ID 0x00U`
- `#define LIN_SERIAL_NUMBER 0x01U`
- `#define LD_BROADCAST 0x7FU`
- `#define LD_FUNCTIONAL_NAD 0x7EU`
- `#define LD_ANY_SUPPLIER 0x7FFFU`
- `#define LD_ANY_FUNCTION 0xFFFFU`
- `#define LD_ANY_MESSAGE 0xFFFFU`
- `#define RES_NEGATIVE 0x7FU`
- `#define GENERAL_REJECT 0x10U`
- `#define SERVICE_NOT_SUPPORTED 0x11U`
- `#define SUBFUNCTION_NOT_SUPPORTED 0x12U`
- `#define NEGATIVE 0U`
- `#define POSITIVE 1U`
- `#define TRANSMITTING 0U`
- `#define RECEIVING 1U`
- `#define DIAG_SERVICE_CALLBACK_HANDLER(iii, sid) lin_diag_service_callback((iii), (sid))`

Functions

- void [lin_diag_service_callback](#) (l_ifc_handle iii, l_u8 sid)

17.30.2 Macro Definition Documentation

17.30.2.1 `#define DIAG_SERVICE_CALLBACK_HANDLER(iii, sid) lin_diag_service_callback((iii), (sid))`

Definition at line 86 of file `lin_commontl_api.h`.

17.30.2.2 #define GENERAL_REJECT 0x10U

Error code raised when request for service not supported comes

Definition at line 71 of file lin_commontl_api.h.

17.30.2.3 #define LD_ANY_FUNCTION 0xFFFFU

Function

Definition at line 66 of file lin_commontl_api.h.

17.30.2.4 #define LD_ANY_MESSAGE 0xFFFFU

Message

Definition at line 67 of file lin_commontl_api.h.

17.30.2.5 #define LD_ANY_SUPPLIER 0x7FFFU

Supplier

Definition at line 65 of file lin_commontl_api.h.

17.30.2.6 #define LD_BROADCAST 0x7FU

Broadcast NAD

Definition at line 63 of file lin_commontl_api.h.

17.30.2.7 #define LD_DATA_ERROR 0x43U

Data error

Definition at line 50 of file lin_commontl_api.h.

17.30.2.8 #define LD_FUNCTIONAL_NAD 0x7EU

Functional NAD

Definition at line 64 of file lin_commontl_api.h.

17.30.2.9 #define LD_LENGTH_NOT_CORRECT 0x44U

Length not correct

Definition at line 51 of file lin_commontl_api.h.

17.30.2.10 #define LD_LENGTH_TOO_SHORT 0x34U

Length too short

Definition at line 48 of file lin_commontl_api.h.

17.30.2.11 #define LD_READ_OK 0x33U

Read OK

Definition at line 47 of file lin_commontl_api.h.

17.30.2.12 #define LD_SET_OK 0x45U

Set OK

Definition at line 52 of file lin_commontl_api.h.

17.30.2.13 #define LIN_PRODUCT_ID 0x00U

Node product identifier

Definition at line 59 of file lin_commontl_api.h.

17.30.2.14 #define LIN_SERIAL_NUMBER 0x01U

Serial number

Definition at line 60 of file lin_commontl_api.h.

17.30.2.15 #define NEGATIVE 0U

Negative response

Definition at line 76 of file lin_commontl_api.h.

17.30.2.16 #define POSITIVE 1U

Positive response

Definition at line 77 of file lin_commontl_api.h.

17.30.2.17 #define RECEIVING 1U

Receiving

Definition at line 80 of file lin_commontl_api.h.

17.30.2.18 #define RES_NEGATIVE 0x7FU

Negative response

Definition at line 70 of file lin_commontl_api.h.

17.30.2.19 #define RES_POSITIVE 0x40U

Positive response

Definition at line 56 of file lin_commontl_api.h.

17.30.2.20 #define SERVICE_NOT_SUPPORTED 0x11U

Error code in negative response for not supported service

Definition at line 72 of file lin_commontl_api.h.

17.30.2.21 #define SERVICE_TARGET_RESET 0xB5U

Target reset service

Definition at line 55 of file lin_commontl_api.h.

17.30.2.22 #define SUBFUNCTION_NOT_SUPPORTED 0x12U

Error code in negative response for not supported sub function

Definition at line 73 of file lin_commontl_api.h.

17.30.2.23 #define TRANSMITTING 0U

Transmitting

Definition at line 79 of file lin_commontl_api.h.

17.30.3 Function Documentation

17.30.3.1 void lin_diag_service_callback (l_ifc_handle *iii*, l_u8 *sid*)

Definition at line 1041 of file lin_diagnostic_service.c.

17.31 Comparator (CMP)

17.31.1 Detailed Description

Hardware background

The comparator (CMP) module is an analog comparator integrated in MCU.

Features of the CMP module include:

- 8 bit DAC with 2 voltage reference source
- 8 analog inputs from external pins
- Round robin check. In summary, this allow the CMP to operate independently in STOP and VLPS mode, whilst being triggered periodically to sample up to 8 inputs. Only if an input changes state is a full wakeup generated.
- Operational over the entire supply range
- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising or falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as: sampled, windowed, which is ideal for certain PWM zero-crossing-detection applications and digitally filtered
- A comparison event can be selected to trigger a DMA transfer
- The window and filter functions are not available in STOP modes.

How to use the CMP driver in your application

The user can configure the CMP in many ways: -CMP_DRV_Init - configures all CMP features -CMP_DRV_↔ ConfigDAC - configures only DAC features -CMP_DRV_ConfigTriggerMode - configures only trigger mode features -CMP_DRV_ConfigComparator - configures only analog comparator features -CMP_DRV_ConfigMUX - configures only MUX features

Also the current configuration can be read using: -CMP_DRV_GetConfigAll - gets all CMP configuration -CM↔ P_DRV_GetDACConfig - gets only DAC configuration -CMP_DRV_GetMUXConfig - gets only MUX configuration -CMP_DRV_GetInitTriggerMode - gets only trigger mode configuration -CMP_DRV_GetComparatorConfig - gets only analog comparator features

A default configuration can be read using: -CMP_DRV_GetDefaultConfig - gets a default configuration for the comparator

When the MCU exits from STOP mode CMP_DRV_GetInputFlags can be used to get the channel which triggered the wakeup. Please use this function only in this use case. CMP_DRV_ClearInputFlags will be used to clear this input change flags.

CMP_DRV_GetOutputFlags can be used to get output flag state and CMP_DRV_ClearOutputFlags to clear them.

The main structure used to configure your application is [cmp_module_t](#). This structure includes configuration structures for trigger mode, MUX, DAC and comparator: [cmp_comparator_t](#), [cmp_anmux_t](#), [cmp_dac_t](#) and [cmp_trigger_mode_t](#)

If application use CMP as wakeup source from Standby mode on MPC574x devices is mandatory to enable channel 3

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\drivers\src\cmp\cmp_driver.c
{S32SDK_PATH}\platform\drivers\src\cmp\cmp_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\drivers\inc\
{S32SDK_PATH}\platform\drivers\src\cmp\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager Interrupt Manager \(Interrupt\) PinSettings](#)

Example for S32K14x:

The next example will compare 2 external signals (CMP input 0 an CMP input 1). The output can be measured on port E, pin 4.

```
const cmp_module_t cmp_general_config =
{
    {
        .dmaTriggerState      = false,
        .outputInterruptTrigger = CMP_NO_EVENT,
        .mode                 = CMP_CONTINUOUS,
        .filterSamplePeriod   = 0,
        .filterSampleCount    = 0,
        .powerMode            = CMP_LOW_SPEED,
        .inverterState        = CMP_NORMAL,
        .outputSelect         = CMP_COUT,
        .pinState             = CMP_AVAILABLE,
        .offsetLevel          = CMP_LEVEL_OFFSET_0,
        .hysteresisLevel      = CMP_LEVEL_HYS_0
    },
    {
        .positivePortMux      = CMP_MUX,
        .negativePortMux      = CMP_MUX,
        .positiveInputMux     = 0,
        .negativeInputMux     = 1
    },
    {
        .voltageReferenceSource = CMP_VIN1,
        .voltage                = 120,
        .state                  = false
    },
    {
        .roundRobinState      = false,
        .roundRobinInterruptState = false,
        .fixedPort            = CMP_PLUS_FIXED,
        .fixedChannel         = 0,
        .samples              = 0,
        .initializationDelay   = 0,
        /* Channel 0 is enabled for round robin check */
        /* Channel 1 is enabled for round robin check */
        /* Channel 2 is enabled for round robin check */
        /* Channel 3 is enabled for round robin check */
        /* Channel 4 is enabled for round robin check */
        /* Channel 5 is enabled for round robin check */
        /* Channel 6 is enabled for round robin check */
        /* Channel 7 is enabled for round robin check */
        .roundRobinChannelsState = 255,
        /* Initial comparison result for channel 0 is 1 */
        /* Initial comparison result for channel 1 is 1 */
        /* Initial comparison result for channel 2 is 1 */
        /* Initial comparison result for channel 3 is 1 */
        /* Initial comparison result for channel 4 is 1 */
    }
}
```

```

        /* Initial comparison result for channel 5 is 1 */
        /* Initial comparison result for channel 6 is 1 */
        /* Initial comparison result for channel 7 is 1 */
        .programedState      = 255
    }
};

#define COMPARATOR_PORT      PORTA
#define COMPARATOR_INPUT1_PIN 0UL
#define COMPARATOR_INPUT2_PIN 1UL
#define COMPARATOR_OUTPUT    4UL
#define COMPARATOR_INSTANCE  0UL

int main(void)
{
    /* Initialize and configure clocks
     * - Setup system clocks
     * - Enable clock feed for Ports and Comparator
     * - See Clock Manager component for more info
     */
    CLOCK_SYS_Init(g_clockManConfigsArr, CLOCK_MANAGER_CONFIG_CNT,
                  g_clockManCallbacksArr, CLOCK_MANAGER_CALLBACK_CNT);
    CLOCK_SYS_UpdateConfiguration(0U,
                                  CLOCK_MANAGER_POLICY_AGREEMENT);

    /* Set pins used by CMP */
    /* The negative port is connected to PTA0 and positive port is connected to PTA1. The
     * comparator output can be visualized on PTA4 */
    /* Initialize pins
     * - Setup input pins for Comparator
     * - Setup output pins for LEDs
     * - See PinSettings component for more info
     */
    PINS_DRV_Init(NUM_OF_CONFIGURED_PINS, g_pin_mux_InitConfigArr);

    /* Init CMP module */
    CMP_DRV_Init(COMPARATOR_INSTANCE, &cmp_general_config);
    for (;;)
    {
    }
    return(0);
}

```

Example for MPC574XG:

The next example will compare 2 external signals (CMP input 0 an CMP input 1). The output can be measured on port E, pin 4.

```

const cmp_module_t cmp_general_config =
{
    {
        .dmaTriggerState      = false,
        .outputInterruptTrigger = CMP_NO_EVENT,
        .mode                  = CMP_CONTINUOUS,
        .filterSamplePeriod    = 0,
        .filterSampleCount     = 0,
        .powerMode              = CMP_LOW_SPEED,
        .inverterState          = CMP_NORMAL,
        .outputSelect           = CMP_COUT,
        .pinState                = CMP_AVAILABLE,
        .hysteresisLevel        = CMP_LEVEL_HYS_0
    },
    {
        .positivePortMux       = CMP_MUX,
        .negativePortMux        = CMP_MUX,
        .positiveInputMux       = 0,
        .negativeInputMux       = 1
    },
    {
        .voltageReferenceSource = CMP_VIN1,
        .voltage                 = 120,
        .state                    = false,
        .fixRefInputMux           = false
    },
    {
        .roundRobinState        = false,
        .roundRobinInterruptState = false,
        .fixedPort                = CMP_PLUS_FIXED,
        .fixedChannel             = 0,
        .samples                  = 0,
        /* Channel 0 is enabled for round robin check */
        /* Channel 1 is enabled for round robin check */
    }
}

```

```

        /* Channel 2 is enabled for round robin check */
        /* Channel 3 is enabled for round robin check */
        /* Channel 4 is enabled for round robin check */
        /* Channel 5 is enabled for round robin check */
        /* Channel 6 is enabled for round robin check */
        /* Channel 7 is enabled for round robin check */
        .roundRobinChannelsState = 255,
        /* Initial comparison result for channel 0 is 1 */
        /* Initial comparison result for channel 1 is 1 */
        /* Initial comparison result for channel 2 is 1 */
        /* Initial comparison result for channel 3 is 1 */
        /* Initial comparison result for channel 4 is 1 */
        /* Initial comparison result for channel 5 is 1 */
        /* Initial comparison result for channel 6 is 1 */
        /* Initial comparison result for channel 7 is 1 */
        .programedState = 255
    }
};

#define COMPARATOR_PORT          PORTA
#define COMPARATOR_INPUT1_PIN    0UL
#define COMPARATOR_INPUT2_PIN    1UL
#define COMPARATOR_OUTPUT        4UL
#define COMPARATOR_INSTANCE      0UL

int main(void)
{
    /* Write your local variable definition here */
    /* Initialize and configure clocks
     * - Setup system clocks
     * - Enable clock feed for Ports and Comparator
     * - See Clock Manager component for more info
     */
    CLOCK_SYS_Init(g_clockManConfigsArr, CLOCK_MANAGER_CONFIG_CNT,
                   g_clockManCallbacksArr, CLOCK_MANAGER_CALLBACK_CNT);
    CLOCK_SYS_UpdateConfiguration(0U,
                                   CLOCK_MANAGER_POLICY_AGREEMENT);

    /* Set pins used by CMP */
    /* The negative port is connected to PTA0 and positive port is connected to PTA1. The
     * comparator output can be visualized on PTA4 */
    /* Initialize pins
     * - Setup input pins for Comparator
     * - Setup output pins for LEDs
     * - See PinSettings component for more info
     */
    PINS_DRV_Init(NUM_OF_CONFIGURED_PINS, g_pin_mux_InitConfigArr);

    /* Init CMP module */
    CMP_DRV_Init(COMPARATOR_INSTANCE, &cmp_general_config);
    for (;;)
    {
        return(0);
    }
}

```

Modules

- [Comparator Driver](#)

Comparator Peripheral Driver.

17.32 Comparator Driver

17.32.1 Detailed Description

Comparator Peripheral Driver.

Definitions

Data Structures

- struct [cmp_comparator_t](#)
Defines the block configuration. [More...](#)
- struct [cmp_anmux_t](#)
Defines the analog mux. [More...](#)
- struct [cmp_dac_t](#)
Defines the DAC block. [More...](#)
- struct [cmp_trigger_mode_t](#)
Defines the trigger mode. [More...](#)
- struct [cmp_module_t](#)
Defines the comparator module configuration. [More...](#)

Macros

- #define [CMP_INPUT_FLAGS_MASK](#) 0xFF0000
- #define [CMP_INPUT_FLAGS_SHIFT](#) 16U
- #define [CMP_ROUND_ROBIN_CHANNELS_MASK](#) 0xFF0000
- #define [CMP_ROUND_ROBIN_CHANNELS_SHIFT](#) 16U

Typedefs

- typedef uint8_t [cmp_ch_list_t](#)
Comparator channels list (1bit/channel) |-----|-----|---|-----|-----| |CH7_state|CH6_state|.....|CH1_↔state|CH0_state| |-----|-----|---|-----|-----| Implements : [cmp_ch_list_t_Class](#).
- typedef uint8_t [cmp_ch_number_t](#)
Number of channel Implements : [cmp_ch_number_t_Class](#).

Enumerations

- enum [cmp_power_mode_t](#) { [CMP_LOW_SPEED](#) = 0U, [CMP_HIGH_SPEED](#) = 1U }
Power Modes selection Implements : [cmp_power_mode_t_Class](#).
- enum [cmp_voltage_reference_t](#) { [CMP_VIN1](#) = 0U, [CMP_VIN2](#) = 1U }
Voltage Reference selection Implements : [cmp_voltage_reference_t_Class](#).
- enum [cmp_port_mux_t](#) { [CMP_DAC](#) = [CMP_DAC_SOURCE](#), [CMP_MUX](#) = [CMP_MUX_SOURCE](#) }
Port Mux Source selection Implements : [cmp_port_mux_t_Class](#).
- enum [cmp_inverter_t](#) { [CMP_NORMAL](#) = 0U, [CMP_INVERT](#) = 1U }
Comparator output invert selection Implements : [cmp_inverter_t_Class](#).
- enum [cmp_output_select_t](#) { [CMP_COUT](#) = 0U, [CMP_COUTA](#) = 1U }
Comparator output select selection Implements : [cmp_output_select_t_Class](#).
- enum [cmp_output_enable_t](#) { [CMP_UNAVAILABLE](#) = 0U, [CMP_AVAILABLE](#) = 1U }
Comparator output pin enable selection Implements : [cmp_output_enable_t_Class](#).
- enum [cmp_hysteresis_t](#) { [CMP_LEVEL_HYS_0](#) = 0U, [CMP_LEVEL_HYS_1](#) = 1U, [CMP_LEVEL_HYS_2](#) = 2U, [CMP_LEVEL_HYS_3](#) = 3U }

Comparator hysteresis control Implements : *cmp_hysteresis_t_Class*.

- enum `cmp_fixed_port_t` { `CMP_PLUS_FIXED` = 0U, `CMP_MINUS_FIXED` = 1U }

Comparator Round-Robin fixed port Implements : *cmp_fixed_port_t_Class*.

- enum `cmp_output_trigger_t` { `CMP_NO_EVENT` = 0U, `CMP_FALLING_EDGE` = 1U, `CMP_RISING_EDGE` = 2U, `CMP_BOTH_EDGES` = 3U }

Comparator output interrupt configuration Implements : *cmp_output_trigger_t_Class*.

- enum `cmp_mode_t` {
`CMP_DISABLED` = 0U, `CMP_CONTINUOUS` = 1U, `CMP_SAMPLED_NONFILTRED_INT_CLK` = 2U, `CMP_SAMPLED_NONFILTRED_EXT_CLK` = 3U,
`CMP_SAMPLED_FILTRED_INT_CLK` = 4U, `CMP_SAMPLED_FILTRED_EXT_CLK` = 5U, `CMP_WINDOWED_RESAMPLED` = 6U, `CMP_WINDOWED_FILTRED` = 7U,
`CMP_WINDOWED_FILTRED` = 8U }

Comparator functional modes Implements : *cmp_mode_t_Class*.

cMP DRV.

- status_t `CMP_DRV_Reset` (const uint32_t instance)
Reset all registers.
- status_t `CMP_DRV_GetInitConfigAll` (cmp_module_t *config)
Get reset configuration for all registers.
- status_t `CMP_DRV_GetDefaultConfig` (cmp_module_t *const config)
Gets a default comparator configuration.
- status_t `CMP_DRV_Init` (const uint32_t instance, const cmp_module_t *const config)
Configure all comparator features with the given configuration structure.
- status_t `CMP_DRV_GetConfigAll` (const uint32_t instance, cmp_module_t *const config)
Gets the current comparator configuration.
- status_t `CMP_DRV_GetInitConfigDAC` (cmp_dac_t *config)
Get reset configuration for registers related with DAC.
- status_t `CMP_DRV_ConfigDAC` (const uint32_t instance, const cmp_dac_t *config)
Configure only the DAC component.
- status_t `CMP_DRV_GetDACConfig` (const uint32_t instance, cmp_dac_t *const config)
Return current configuration for DAC.
- status_t `CMP_DRV_GetInitConfigMUX` (cmp_anmux_t *config)
Get reset configuration for registers related with MUX.
- status_t `CMP_DRV_ConfigMUX` (const uint32_t instance, const cmp_anmux_t *config)
Configure only the MUX component.
- status_t `CMP_DRV_GetMUXConfig` (const uint32_t instance, cmp_anmux_t *const config)
Return configuration only for the MUX component.
- status_t `CMP_DRV_GetInitTriggerMode` (cmp_trigger_mode_t *config)
Get reset configuration for registers related with Trigger Mode.
- status_t `CMP_DRV_ConfigTriggerMode` (const uint32_t instance, const cmp_trigger_mode_t *config)
Configure trigger mode.
- status_t `CMP_DRV_GetTriggerModeConfig` (const uint32_t instance, cmp_trigger_mode_t *const config)
Get current trigger mode configuration.
- status_t `CMP_DRV_GetOutputFlags` (const uint32_t instance, cmp_output_trigger_t *flags)
Get comparator output flags.
- status_t `CMP_DRV_ClearOutputFlags` (const uint32_t instance)
Clear comparator output flags.
- status_t `CMP_DRV_GetInputFlags` (const uint32_t instance, cmp_ch_list_t *flags)
Gets input channels change flags.
- status_t `CMP_DRV_ClearInputFlags` (const uint32_t instance)

Clear comparator input channels flags.

- status_t [CMP_DRV_GetInitConfigComparator](#) (cmp_comparator_t *config)

Get reset configuration for registers related with comparator features.

- status_t [CMP_DRV_ConfigComparator](#) (const uint32_t instance, const cmp_comparator_t *config)

Configure only comparator features.

- status_t [CMP_DRV_GetComparatorConfig](#) (const uint32_t instance, cmp_comparator_t *config)

Return configuration for comparator from CMP module.

17.32.2 Data Structure Documentation

17.32.2.1 struct cmp_comparator_t

Defines the block configuration.

This structure is used to configure only comparator block module(filtering, sampling, power_mode etc.) Implements : cmp_comparator_t_Class

Definition at line 178 of file cmp_driver.h.

Data Fields

- bool [dmaTriggerState](#)
- [cmp_output_trigger_t](#) outputInterruptTrigger
- [cmp_mode_t](#) mode
- uint8_t [filterSamplePeriod](#)
- uint8_t [filterSampleCount](#)
- [cmp_power_mode_t](#) powerMode
- [cmp_inverter_t](#) inverterState
- [cmp_output_enable_t](#) pinState
- [cmp_output_select_t](#) outputSelect
- [cmp_hysteresis_t](#) hysteresisLevel

Field Documentation

17.32.2.1.1 bool dmaTriggerState

True if DMA transfer trigger from comparator is enable.

Definition at line 180 of file cmp_driver.h.

17.32.2.1.2 uint8_t filterSampleCount

Number of sample count for filtering.

Definition at line 187 of file cmp_driver.h.

17.32.2.1.3 uint8_t filterSamplePeriod

Filter sample period.

Definition at line 186 of file cmp_driver.h.

17.32.2.1.4 cmp_hysteresis_t hysteresisLevel

CMP_LEVEL_HYS_0 if hard block output has level 0 hysteresis. CMP_LEVEL_HYS_1 if hard block output has level 1 hysteresis. CMP_LEVEL_HYS_2 if hard block output has level 2 hysteresis. CMP_LEVEL_HYS_3 if hard block output has level 3 hysteresis.

Definition at line 200 of file cmp_driver.h.

17.32.2.1.5 `cmp_inverter_t` `inverterState`

CMP_NORMAL if does not invert the comparator output. CMP_INVERT if inverts the comparator output.

Definition at line 190 of file `cmp_driver.h`.

17.32.2.1.6 `cmp_mode_t` `mode`

Configuration structure which define: the comparator functional mode, sample period and sample count.

Definition at line 185 of file `cmp_driver.h`.

17.32.2.1.7 `cmp_output_trigger_t` `outputInterruptTrigger`

CMP_NO_INTERRUPT comparator output would not trigger any interrupt. CMP_FALLING_EDGE comparator output would trigger an interrupt on falling edge. CMP_RISING_EDGE comparator output would trigger an interrupt on rising edge. CMP_BOTH_EDGES comparator output would trigger an interrupt on rising and falling edges.

Definition at line 181 of file `cmp_driver.h`.

17.32.2.1.8 `cmp_output_select_t` `outputSelect`

CMP_COUT if output signal is equal to COUT(filtered). CMP_COUTA if output signal is equal to COUTA(unfiltered).

Definition at line 194 of file `cmp_driver.h`.

17.32.2.1.9 `cmp_output_enable_t` `pinState`

CMP_UNAVAILABLE if comparator output is not available to package pin. CMP_AVAILABLE if comparator output is available to package pin.

Definition at line 192 of file `cmp_driver.h`.

17.32.2.1.10 `cmp_power_mode_t` `powerMode`

CMP_LOW_SPEED if low speed mode is selected. CMP_HIGH_SPEED if high speed mode is selected

Definition at line 188 of file `cmp_driver.h`.

17.32.2.2 `struct cmp_anmux_t`

Defines the analog mux.

This structure is used to configure the analog multiplexor to select compared signals Implements : `cmp_anmux_t` ↔ `t_Class`

Definition at line 212 of file `cmp_driver.h`.

Data Fields

- [cmp_port_mux_t](#) `positivePortMux`
- [cmp_port_mux_t](#) `negativePortMux`
- [cmp_ch_number_t](#) `positiveInputMux`
- [cmp_ch_number_t](#) `negativeInputMux`

Field Documentation

17.32.2.2.1 `cmp_ch_number_t` `negativeInputMux`

Select which channel is selected for the minus mux.

Definition at line 222 of file `cmp_driver.h`.

17.32.2.2.2 `cmp_port_mux_t` `negativePortMux`

Select negative port signal. CMP_DAC if source is digital to analog converter. CMP_MUX if source is 8 ch MUX

Definition at line 217 of file cmp_driver.h.

17.32.2.2.3 `cmp_ch_number_t` positiveInputMux

Select which channel is selected for the plus mux.

Definition at line 221 of file cmp_driver.h.

17.32.2.2.4 `cmp_port_mux_t` positivePortMux

Select positive port signal. CMP_DAC if source is digital to analog converter. CMP_MUX if source is 8 ch MUX

Definition at line 214 of file cmp_driver.h.

17.32.2.3 `struct cmp_dac_t`

Defines the DAC block.

This structure is used to configure the DAC block integrated in comparator module Implements : `cmp_dac_t_Class`

Definition at line 231 of file cmp_driver.h.

Data Fields

- `cmp_voltage_reference_t` voltageReferenceSource
- `uint8_t` voltage
- `bool` state

Field Documentation

17.32.2.3.1 `bool` state

True if DAC is enabled.

Definition at line 236 of file cmp_driver.h.

17.32.2.3.2 `uint8_t` voltage

The digital value which is converted to analog signal.

Definition at line 235 of file cmp_driver.h.

17.32.2.3.3 `cmp_voltage_reference_t` voltageReferenceSource

CMP_VIN1 if selected voltage reference is VIN1. CMP_VIN2 if selected voltage reference is VIN2.

Definition at line 233 of file cmp_driver.h.

17.32.2.4 `struct cmp_trigger_mode_t`

Defines the trigger mode.

This structure is used to configure the trigger mode operation when MCU enters STOP modes Implements : `cmp_trigger_mode_t_Class`

Definition at line 251 of file cmp_driver.h.

Data Fields

- `bool` roundRobinState
- `bool` roundRobinInterruptState
- `cmp_fixed_port_t` fixedPort
- `cmp_ch_number_t` fixedChannel
- `uint8_t` samples
- `cmp_ch_list_t` roundRobinChannelsState
- `cmp_ch_list_t` programmedState

Field Documentation

17.32.2.4.1 `cmp_ch_number_t` fixedChannel

Select which channel would be assigned to the fixed port.

Definition at line 257 of file `cmp_driver.h`.

17.32.2.4.2 `cmp_fixed_port_t` fixedPort

CMP_PLUS_FIXED if plus port is fixed. CMP_MINUS_FIXED if minus port is fixed.

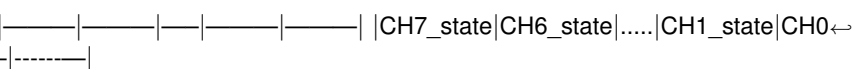
Definition at line 255 of file `cmp_driver.h`.

17.32.2.4.3 `cmp_ch_list_t` programmedState

Pre-programmed state for comparison result.

Definition at line 266 of file `cmp_driver.h`.

17.32.2.4.4 `cmp_ch_list_t` roundRobinChannelsState

One bite for each channel state. |CH7_state|CH6_state|.....|CH1_state|CH0_state|

Definition at line 262 of file `cmp_driver.h`.

17.32.2.4.5 `bool` roundRobinInterruptState

True if Round-Robin interrupt is enabled.

Definition at line 254 of file `cmp_driver.h`.

17.32.2.4.6 `bool` roundRobinState

True if Round-Robin is enabled.

Definition at line 253 of file `cmp_driver.h`.

17.32.2.4.7 `uint8_t` samples

Select number of round-robin clock cycles for a given channel.

Definition at line 258 of file `cmp_driver.h`.

17.32.2.5 `struct cmp_module_t`

Defines the comparator module configuration.

This structure is used to configure all components of comparator module Implements : `cmp_module_t_Class`

Definition at line 275 of file `cmp_driver.h`.

Data Fields

- [cmp_comparator_t](#) comparator
- [cmp_anmux_t](#) mux
- [cmp_dac_t](#) dac
- [cmp_trigger_mode_t](#) triggerMode

Field Documentation

17.32.2.5.1 `cmp_comparator_t` comparator

Definition at line 277 of file `cmp_driver.h`.

17.32.2.5.2 `cmp_dac_t` `dac`

Definition at line 279 of file `cmp_driver.h`.

17.32.2.5.3 `cmp_anmux_t` `mux`

Definition at line 278 of file `cmp_driver.h`.

17.32.2.5.4 `cmp_trigger_mode_t` `triggerMode`

Definition at line 280 of file `cmp_driver.h`.

17.32.3 Macro Definition Documentation

17.32.3.1 `#define CMP_INPUT_FLAGS_MASK 0xFF0000`

Definition at line 39 of file `cmp_driver.h`.

17.32.3.2 `#define CMP_INPUT_FLAGS_SHIFT 16U`

Definition at line 40 of file `cmp_driver.h`.

17.32.3.3 `#define CMP_ROUND_ROBIN_CHANNELS_MASK 0xFF0000`

Definition at line 41 of file `cmp_driver.h`.

17.32.3.4 `#define CMP_ROUND_ROBIN_CHANNELS_SHIFT 16U`

Definition at line 42 of file `cmp_driver.h`.

17.32.4 Typedef Documentation

17.32.4.1 `typedef uint8_t cmp_ch_list_t`

Comparator channels list (1bit/channel) |-----|-----|---|-----|-----| |CH7_state|CH6_state|.....|CH1_↔
state|CH0_state| |-----|-----|---|-----|-----| Implements : `cmp_ch_list_t_Class`.

Definition at line 165 of file `cmp_driver.h`.

17.32.4.2 `typedef uint8_t cmp_ch_number_t`

Number of channel Implements : `cmp_ch_number_t_Class`.

Definition at line 170 of file `cmp_driver.h`.

17.32.5 Enumeration Type Documentation

17.32.5.1 `enum cmp_fixed_port_t`

Comparator Round-Robin fixed port Implements : `cmp_fixed_port_t_Class`.

Enumerator

CMP_PLUS_FIXED The Plus port is fixed. Only the inputs to the Minus port are swept in each round.

CMP_MINUS_FIXED The Minus port is fixed. Only the inputs to the Plus port are swept in each round.

Definition at line 126 of file `cmp_driver.h`.

17.32.5.2 enum **cmp_hysteresis_t**

Comparator hysteresis control Implements : **cmp_hysteresis_t_Class**.

Enumerator

CMP_LEVEL_HYS_0

CMP_LEVEL_HYS_1

CMP_LEVEL_HYS_2

CMP_LEVEL_HYS_3

Definition at line 115 of file **cmp_driver.h**.

17.32.5.3 enum **cmp_inverter_t**

Comparator output invert selection Implements : **cmp_inverter_t_Class**.

Enumerator

CMP_NORMAL Output signal isn't inverted.

CMP_INVERT Output signal is inverted.

Definition at line 77 of file **cmp_driver.h**.

17.32.5.4 enum **cmp_mode_t**

Comparator functional modes Implements : **cmp_mode_t_Class**.

Enumerator

CMP_DISABLED

CMP_CONTINUOUS

CMP_SAMPLED_NONFILTRD_INT_CLK

CMP_SAMPLED_NONFILTRD_EXT_CLK

CMP_SAMPLED_FILTRD_INT_CLK

CMP_SAMPLED_FILTRD_EXT_CLK

CMP_WINDOWED

CMP_WINDOWED_RESAMPLED

CMP_WINDOWED_FILTRD

Definition at line 146 of file **cmp_driver.h**.

17.32.5.5 enum **cmp_output_enable_t**

Comparator output pin enable selection Implements : **cmp_output_enable_t_Class**.

Enumerator

CMP_UNAVAILABLE Comparator output isn't available to a specific pin

CMP_AVAILABLE Comparator output is available to a specific pin

Definition at line 95 of file **cmp_driver.h**.

17.32.5.6 enum **cmp_output_select_t**

Comparator output select selection Implements : **cmp_output_select_t_Class**.

Enumerator

CMP_COUT Select COUT as comparator output signal.

CMP_COUTA Select COUTA as comparator output signal.

Definition at line 86 of file **cmp_driver.h**.

17.32.5.7 enum **cmp_output_trigger_t**

Comparator output interrupt configuration Implements : **cmp_output_trigger_t_Class**.

Enumerator

CMP_NO_EVENT Comparator output interrupts are disabled OR no event occurred.

CMP_FALLING_EDGE Comparator output interrupts will be generated only on falling edge OR only falling edge event occurred.

CMP_RISING_EDGE Comparator output interrupts will be generated only on rising edge OR only rising edge event occurred.

CMP_BOTH_EDGES Comparator output interrupts will be generated on both edges OR both edges event occurred.

Definition at line 135 of file **cmp_driver.h**.

17.32.5.8 enum **cmp_port_mux_t**

Port Mux Source selection Implements : **cmp_port_mux_t_Class**.

Enumerator

CMP_DAC Select DAC as source for the comparator port.

CMP_MUX Select MUX8 as source for the comparator port.

Definition at line 68 of file **cmp_driver.h**.

17.32.5.9 enum **cmp_power_mode_t**

Power Modes selection Implements : **cmp_power_mode_t_Class**.

Enumerator

CMP_LOW_SPEED Module in low speed mode.

CMP_HIGH_SPEED Module in high speed mode.

Definition at line 50 of file **cmp_driver.h**.

17.32.5.10 enum **cmp_voltage_reference_t**

Voltage Reference selection Implements : **cmp_voltage_reference_t_Class**.

Enumerator

CMP_VIN1 Use Vin1 as supply reference source for DAC.

CMP_VIN2 Use Vin2 as supply reference source for DAC.

Definition at line 59 of file **cmp_driver.h**.

17.32.6 Function Documentation

17.32.6.1 `status_t CMP_DRV_ClearInputFlags (const uint32_t instance)`

Clear comparator input channels flags.

This function clear comparator input channels flags.

Parameters

<i>instance</i>	- instance number
-----------------	-------------------

Returns

- `STATUS_SUCCESS` : Completed successfully.
- `STATUS_ERROR` : Error occurred.

Definition at line 562 of file `cmp_driver.c`.

17.32.6.2 `status_t CMP_DRV_ClearOutputFlags (const uint32_t instance)`

Clear comparator output flags.

This function clear comparator output flags(rising and falling edge).

Parameters

<i>instance</i>	- instance number
-----------------	-------------------

Returns

- `STATUS_SUCCESS` : Completed successfully.
- `STATUS_ERROR` : Error occurred.

Definition at line 517 of file `cmp_driver.c`.

17.32.6.3 `status_t CMP_DRV_ConfigComparator (const uint32_t instance, const cmp_comparator_t * config)`

Configure only comparator features.

This function configure only features related with comparator: DMA request, power mode, output select, interrupts enable, invert, offset, hysteresis.

Parameters

<i>instance</i>	- instance number
<i>config</i>	- the configuration structure

Returns

- `STATUS_SUCCESS` : Completed successfully.
- `STATUS_ERROR` : Error occurred.

Definition at line 611 of file `cmp_driver.c`.

17.32.6.4 `status_t CMP_DRV_ConfigDAC (const uint32_t instance, const cmp_dac_t * config)`

Configure only the DAC component.

This function configures the DAC with the options provided in the config structure.

Parameters

<i>instance</i>	- instance number
<i>config</i>	- the configuration structure

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 316 of file cmp_driver.c.

17.32.6.5 `status_t CMP_DRV_ConfigMUX (const uint32_t instance, const cmp_anmux_t * config)`

Configure only the MUX component.

This function configures the MUX with the options provided in the config structure.

Parameters

<i>instance</i>	- instance number
<i>config</i>	- the configuration structure

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 381 of file cmp_driver.c.

17.32.6.6 `status_t CMP_DRV_ConfigTriggerMode (const uint32_t instance, const cmp_trigger_mode_t * config)`

Configure trigger mode.

This function configures the trigger mode with the options provided in the config structure.

Parameters

<i>instance</i>	- instance number
<i>config</i>	- the configuration structure

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 445 of file cmp_driver.c.

17.32.6.7 `status_t CMP_DRV_GetComparatorConfig (const uint32_t instance, cmp_comparator_t * config)`

Return configuration for comparator from CMP module.

This function return configuration for features related with comparator: DMA request, power mode, output select, interrupts enable, invert, offset, hysteresis.

Parameters

<i>instance</i>	- instance number
-----------------	-------------------

<i>config</i>	- the configuration structure returned
---------------	--

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 641 of file cmp_driver.c.

17.32.6.8 status_t CMP_DRV_GetConfigAll (const uint32_t instance, cmp_module_t *const config)

Gets the current comparator configuration.

This function returns the current configuration for comparator as a configuration structure.

Parameters

<i>instance</i>	- instance number
<i>config</i>	- the configuration structure

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 242 of file cmp_driver.c.

17.32.6.9 status_t CMP_DRV_GetDACConfig (const uint32_t instance, cmp_dac_t *const config)

Return current configuration for DAC.

This function returns current configuration only for DAC.

Parameters

<i>instance</i>	- instance number
<i>config</i>	- the configuration structure

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 340 of file cmp_driver.c.

17.32.6.10 status_t CMP_DRV_GetDefaultConfig (cmp_module_t *const config)

Gets a default comparator configuration.

This function returns a default configuration for the comparator as a configuration structure.

Parameters

<i>instance</i>	- instance number
<i>config</i>	- the configuration structure

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 137 of file cmp_driver.c.

17.32.6.11 status_t CMP_DRV_GetInitConfigAll (cmp_module_t * config)

Get reset configuration for all registers.

This function returns a configuration structure with reset values for all registers from comparator module.

Parameters

<i>config</i>	- the configuration structure
---------------	-------------------------------

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 85 of file cmp_driver.c.

17.32.6.12 status_t CMP_DRV_GetInitConfigComparator (cmp_comparator_t * config)

Get reset configuration for registers related with comparator features.

This function return a configuration structure with reset values for features associated with comparator (DMA request, power mode, output select, interrupts enable, invert, offset, hysteresis).

Parameters

<i>config</i>	- the configuration structure
---------------	-------------------------------

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 584 of file cmp_driver.c.

17.32.6.13 status_t CMP_DRV_GetInitConfigDAC (cmp_dac_t * config)

Get reset configuration for registers related with DAC.

This function returns a configuration structure with reset values for features associated with DAC.

Parameters

<i>config</i>	- the configuration structure
---------------	-------------------------------

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 295 of file cmp_driver.c.

17.32.6.14 status_t CMP_DRV_GetInitConfigMUX (cmp_anmux_t * config)

Get reset configuration for registers related with MUX.

This function returns a configuration structure with reset values for features associated with MUX.

Parameters

<i>config</i>	- the configuration structure
---------------	-------------------------------

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 362 of file cmp_driver.c.

17.32.6.15 `status_t CMP_DRV_GetInitTriggerMode (cmp_trigger_mode_t * config)`

Get reset configuration for registers related with Trigger Mode.

This function returns a configuration structure with reset values for features associated with Trigger Mode.

Parameters

<i>config</i>	- the configuration structure
---------------	-------------------------------

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 422 of file cmp_driver.c.

17.32.6.16 `status_t CMP_DRV_GetInputFlags (const uint32_t instance, cmp_ch_list_t * flags)`

Gets input channels change flags.

This function return in <flags> all input channels flags as uint8_t(1 bite for each channel flag).

Parameters

<i>instance</i>	- instance number
<i>flags</i>	- pointer to input flags

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 544 of file cmp_driver.c.

17.32.6.17 `status_t CMP_DRV_GetMUXConfig (const uint32_t instance, cmp_anmux_t *const config)`

Return configuration only for the MUX component.

This function returns current configuration to determine which signals go to comparator ports.

Parameters

<i>instance</i>	- instance number
<i>config</i>	- the configuration structure

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 402 of file cmp_driver.c.

17.32.6.18 `status_t CMP_DRV_GetOutputFlags (const uint32_t instance, cmp_output_trigger_t * flags)`

Get comparator output flags.

This function returns in <flags> comparator output flags(rising and falling edge).

Parameters

<i>instance</i>	- instance number
-	flags - pointer to output flags NO_EVENT RISING_EDGE FALLING_EDGE BOTH_EDGE

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 499 of file cmp_driver.c.

17.32.6.19 `status_t CMP_DRV_GetTriggerModeConfig (const uint32_t instance, cmp_trigger_mode_t *const config)`

Get current trigger mode configuration.

This function returns the current trigger mode configuration for trigger mode.

Parameters

<i>instance</i>	- instance number
<i>config</i>	- the configuration structure

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 472 of file cmp_driver.c.

17.32.6.20 `status_t CMP_DRV_Init (const uint32_t instance, const cmp_module_t *const config)`

Configure all comparator features with the given configuration structure.

This function configures the comparator module with the options provided in the config structure.

Parameters

<i>instance</i>	- instance number
<i>config</i>	- the configuration structure

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 188 of file cmp_driver.c.

17.32.6.21 `status_t CMP_DRV_Reset (const uint32_t instance)`

Reset all registers.

This function set all CMP registers to reset values.

Parameters

<i>instance</i>	- instance number
-----------------	-------------------

Returns

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 66 of file cmp_driver.c.

17.33 Controller Area Network - Peripheral Abstraction Layer (CAN PAL)

17.33.1 Detailed Description

The S32 SDK provides a Peripheral Abstraction Layer for Controller Area Network (CAN) modules of S32 SDK devices.

The CAN PAL driver allows communication over a CAN bus. It was designed to be portable across all platforms and IPs which support CAN communication.

How to integrate CAN PAL in your application

Unlike the other drivers, CAN PAL modules need to include a configuration file named `can_pal_cfg.h`, which allows the user to specify which IPs are used and how many resources are allocated for each of them (state structures). The following code example shows how to configure one instance for each available CAN IP.

```
#ifndef can_pal_cfg_H
#define can_pal_cfg_H

/* Define which IP instance will be used in current project */
#define CAN_OVER_FLEXCAN

/* Define the resources necessary for current project */
#define NO_OF_FLEXCAN_INSTS_FOR_CAN    1U

#endif /* can_pal_cfg_H */
```

The following table contains the matching between platforms and available IPs

IP↔ M↔ CU	S32↔ K116	S32↔ K118	S32↔ K142	S32↔ K144	S32↔ K146	S32↔ K148	S32↔ V234	MP↔ C5748 G	MP↔ C5746 C	MP↔ C5744 P	S32↔ R274	S32↔ R372
Flex↔ CAN	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES

Features

- Standard data frames
- Extended data frames
- Flexible data rate (FD)
- Bitrate switch inside FD format frames (BRS)
- Zero to sixty four bytes data length
- Programmable bit rate
- Flexible buffers configurable to store 0 to 8, 16, 32 or 64 bytes data length depending of platform support
- Each buffer configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Masking per buffer
- Loop-Back mode
- Remote request frames

The following table contains the matching between platforms and available features

FE↔ A↔ T↔ U↔ R↔ E/↔ M↔ CU	S32↔ K116	S32↔ K118	S32↔ K142	S32↔ K144	S32↔ K146	S32↔ K148	S32↔ V234	M↔ P↔ C5748 G	M↔ P↔ C5746 C	M↔ P↔ C5744 P	S32↔ R274	S32↔ R372
F↔ D/↔ B↔ RS	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	NO	Y↔ ES	Y↔ ES
data length > 8B	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	NO	Y↔ ES	Y↔ ES

Functionality

Initialization

In order to use the CAN PAL driver it must be first initialized, using [CAN_Init\(\)](#) function. Once initialized, it cannot be initialized again for the same CAN module instance until it is de-initialized, using [CAN_Deinit\(\)](#). Different CAN modules instances can function independently of each other.

The [can_user_config_t](#) structure allows you to configure the following:

- the number of buffers needed;
- the operation mode, which can be one of the following:
 - normal mode;
 - loopback mode;
 - disable mode;
- the Protocol Engine clock source:
 - oscillator clock;
 - peripheral clock;
- the payload size of the buffers:
 - 8 bytes;
 - 16 bytes (only available with the FD feature enabled);
 - 32 bytes (only available with the FD feature enabled);
 - 64 bytes (only available with the FD feature enabled);
- enable/disable the Flexible Data-rate feature;
- the bitrate used for standard frames or for the arbitration phase of FD frames;
- the bitrate used for the data phase of FD frames;

The bitrate is represented by a [can_time_segment_t](#) structure, with the following fields:

- propagation segment;
- phase segment 1;
- phase segment 2;
- clock prescaler division factor;

- resync jump width.

In order to use a buffer for transmission/reception, it has to be initialized using either **CAN_ConfigRxBuff** or **CAN_ConfigTxBuff**.

After having the buffer configured, you can start sending/receiving data by calling one of the following functions:

- CAN_Send;
- CAN_SendBlocking;
- CAN_Receive;
- CAN_ReceiveBlocking.

FlexCAN Rx FIFO extension

When used over FlexCAN, the PAL allows extending the basic configuration with an Rx FIFO feature. The Rx FIFO is receive-only and 6-message deep. The application can read the received messages sequentially, in the order they were received, by repeatedly reading the data from buffer 0 (zero). A powerful filtering scheme is provided to accept only frames intended for the target application. The FIFO and filtering criteria are configured by passing a structure of **extension_flexcan_rx_fifo_t** type, through the extension field of the user configuration structure.

```
/* ID Filter table */
flexcan_id_table_t filterTable[] = {
    {
        .isExtendedFrame = false,
        .isRemoteFrame = false,
        .id = 1U
    },
    ...
};

/* Rx FIFO extension */
extension_flexcan_rx_fifo_t can_pall_rx_fifo_ext0 = {
    .numIdFilters = FLEXCAN_RX_FIFO_ID_FILTERS_8,
    .idFormat = FLEXCAN_RX_FIFO_ID_FORMAT_A,
    /* User must pass reference to the ID filter table. */
    .idFilterTable = NULL
};

can_pall_rx_fifo_ext0.idFilterTable = filterTable;
```

The number of elements in the ID filter table is defined by the following formula:

- for format A: the number of Rx FIFO ID filters
- for format B: twice the number of Rx FIFO ID filters
- for format C: four times the number of Rx FIFO ID filters The user must provide the exact number of elements in order to avoid any misconfiguration.

Each element in the ID filter table specifies an ID to be used as acceptance criteria for the FIFO as follows:

- for format A: In the standard frame format, bits 10 to 0 of the ID are used for frame identification. In the extended frame format, bits 28 to 0 are used.
- for format B: In the standard frame format, bits 10 to 0 of the ID are used for frame identification. In the extended frame format, only the 14 most significant bits (28 to 15) of the ID are compared to the 14 most significant bits (28 to 15) of the received ID.
- for format C: In both standard and extended frame formats, only the 8 most significant bits (7 to 0 for standard, 28 to 21 for extended) of the ID are compared to the 8 most significant bits (7 to 0 for standard, 28 to 21 for extended) of the received ID.

When Rx FIFO feature is enabled, buffer 0 (zero) cannot be used for transmission or reconfigured for reception using **CAN_ConfigRxBuff()** and **CAN_SetRxFilter()** functions.

Important Notes

- Before using the CAN PAL driver the module clock must be configured. Refer to **Clock Manager** component for clock configuration.
- The driver enables the interrupts for the corresponding CAN module, but any interrupt priority must be done by the application.
- The board specific configurations must be done prior to driver calls; the driver has no influence on the functionality of the RX/TX pins - they must be configured by application. Refer to **PinSettings** component for pin configuration.
- Some features are not available for all platforms (see the table above for the matching between platforms and available features).
- When used **CAN_ReceiveBlocking()** and **CAN_SendBlocking()** with timeout parameter 0 and the message is already in mailbox configured will report timeout and successful transmit or receive the message.

Example code

```
#define TX_BUFF_IDX      0U
#define RX_BUFF_IDX      1U

uint32_t msgID = 0xAB;

/* CAN PAL instance information */
const can_instance_t can_pall_instance = {CAN_INST_TYPE_FLEXCAN, 0U};

/* User configuration structure */
can_user_config_t config = {
    .maxBuffNum = 2U,
    .mode = CAN_LOOPBACK_MODE,
    .peClkSrc = CAN_CLK_SOURCE_OSC,
    .enableFD = false,
    .payloadSize = CAN_PAYLOAD_SIZE_8,
    .nominalBitrate = {
        .propSeg = 7,
        .phaseSeg1 = 4,
        .phaseSeg2 = 1,
        .preDivider = 0,
        .rJumpwidth = 1
    },
    .dataBitrate = {
        .propSeg = 7,
        .phaseSeg1 = 4,
        .phaseSeg2 = 1,
        .preDivider = 0,
        .rJumpwidth = 1
    },
    .extension = NULL
};

/* Initialize CAN */
CAN_Init(&can_pall_instance, &config);

/* Buffer configuration */
can_buff_config_t buffConfig = {
    .enableFD = false,
    .enableBRS = false,
    .fdPadding = 0xCC,
    .idType = CAN_MSG_ID_STD,
    .isRemote = false
};

CAN_ConfigTxBuff(&can_pall_instance, TX_BUFF_IDX, &buffConfig);
CAN_ConfigRxBuff(&can_pall_instance, RX_BUFF_IDX, &buffConfig, msgID);

can_message_t recvMsg, sendMsg = {
    .id = msgID,
    .length = 5U,
    .data = {"Hello"}
};

/* Send data using buffer configured for transmission */
CAN_Send(&can_pall_instance, TX_BUFF_IDX, &sendMsg);
while(CAN_GetTransferStatus(&can_pall_instance, TX_BUFF_IDX) == STATUS_BUSY);

/* Receive data using buffer configured for reception */
CAN_Receive(&can_pall_instance, RX_BUFF_IDX, &recvMsg);
while(CAN_GetTransferStatus(&can_pall_instance, RX_BUFF_IDX) == STATUS_BUSY);
```

```
/* De-initialize CAN */
CAN_Deinit(&can_pal_instance);
```

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\pal\src\can\can_pal.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\pal\inc\
```

Preprocessor symbols

No special symbols are required for this component

Dependencies

Controller Area Network with Flexible Data Rate (FlexCAN) Clock Manager Interrupt Manager (Interrupt) Enhanced Direct Memory Access (eDMA)

Data Structures

- struct [can_time_segment_t](#)
CAN bit timing variables Implements : [can_time_segment_t_Class](#). [More...](#)
- struct [can_buff_config_t](#)
CAN buffer configuration Implements : [can_buff_config_t_Class](#). [More...](#)
- struct [can_message_t](#)
CAN message format Implements : [can_message_t_Class](#). [More...](#)
- struct [can_user_config_t](#)
CAN controller configuration Implements : [can_user_config_t_Class](#). [More...](#)
- struct [extension_flexcan_rx_fifo_t](#)
FlexCAN Rx FIFO configuration Implements : [extension_flexcan_rx_fifo_t_Class](#). [More...](#)

Enumerations

- enum [can_operation_modes_t](#) { [CAN_NORMAL_MODE](#) = 0U, [CAN_LOOPBACK_MODE](#) = 2U, [CAN_DISABLE_MODE](#) = 4U }
- enum [can_operation_modes_t](#)
CAN controller operation modes Implements : [can_operation_modes_t_Class](#).
- enum [can_fd_payload_size_t](#) { [CAN_PAYLOAD_SIZE_8](#) = 0, [CAN_PAYLOAD_SIZE_16](#), [CAN_PAYLOAD_SIZE_32](#), [CAN_PAYLOAD_SIZE_64](#) }
- enum [can_fd_payload_size_t](#)
CAN buffer payload sizes Implements : [can_fd_payload_size_t_Class](#).
- enum [can_bitrate_phase_t](#) { [CAN_NOMINAL_BITRATE](#), [CAN_FD_DATA_BITRATE](#) }
- enum [can_bitrate_phase_t](#)
CAN bitrate phase (nominal/data) Implements : [can_bitrate_phase_t_Class](#).
- enum [can_msg_id_type_t](#) { [CAN_MSG_ID_STD](#), [CAN_MSG_ID_EXT](#) }
- enum [can_msg_id_type_t](#)
CAN Message Buffer ID type Implements : [can_msg_id_type_t_Class](#).
- enum [can_clk_source_t](#) { [CAN_CLK_SOURCE_OSC](#) = 0U, [CAN_CLK_SOURCE_PERIPH](#) = 1U }
- enum [can_clk_source_t](#)
CAN PE clock sources Implements : [can_clk_source_t_Class](#).

Functions

- status_t **CAN_Init** (const [can_instance_t](#) *const instance, const [can_user_config_t](#) *config)
Initializes the CAN module.
- status_t **CAN_Deinit** (const [can_instance_t](#) *const instance)
De-initializes the CAN module.
- status_t **CAN_SetBtrrate** (const [can_instance_t](#) *const instance, [can_bitrate_phase_t](#) phase, const [can_time_segment_t](#) *bitTiming)
Configures the CAN bitrate.
- status_t **CAN_GetBtrrate** (const [can_instance_t](#) *const instance, [can_bitrate_phase_t](#) phase, [can_time_segment_t](#) *bitTiming)
Returns the CAN bitrate.
- status_t **CAN_ConfigTxBuff** (const [can_instance_t](#) *const instance, uint32_t buffIdx, const [can_buff_config_t](#) *config)
Configures a buffer for transmission.
- status_t **CAN_ConfigRemoteResponseBuff** (const [can_instance_t](#) *const instance, uint32_t buffIdx, const [can_buff_config_t](#) *config, const [can_message_t](#) *message)
Configures a transmit buffer for remote frame response.
- status_t **CAN_ConfigRxBuff** (const [can_instance_t](#) *const instance, uint32_t buffIdx, const [can_buff_config_t](#) *config, uint32_t acceptedId)
Configures a buffer for reception.
- status_t **CAN_Send** (const [can_instance_t](#) *const instance, uint32_t buffIdx, const [can_message_t](#) *message)
Sends a CAN frame using the specified buffer.
- status_t **CAN_SendBlocking** (const [can_instance_t](#) *const instance, uint32_t buffIdx, const [can_message_t](#) *message, uint32_t timeoutMs)
Sends a CAN frame using the specified buffer, in a blocking manner.
- status_t **CAN_Receive** (const [can_instance_t](#) *const instance, uint32_t buffIdx, [can_message_t](#) *message)
Receives a CAN frame using the specified message buffer.
- status_t **CAN_ReceiveBlocking** (const [can_instance_t](#) *const instance, uint32_t buffIdx, [can_message_t](#) *message, uint32_t timeoutMs)
Receives a CAN frame using the specified buffer, in a blocking manner.
- status_t **CAN_AbortTransfer** (const [can_instance_t](#) *const instance, uint32_t buffIdx)
Ends a non-blocking CAN transfer early.
- status_t **CAN_SetRxFilter** (const [can_instance_t](#) *const instance, [can_msg_id_type_t](#) idType, uint32_t buffIdx, uint32_t mask)
Configures an ID filter for a specific reception buffer.
- status_t **CAN_GetTransferStatus** (const [can_instance_t](#) *const instance, uint32_t buffIdx)
Returns the state of the previous CAN transfer.
- status_t **CAN_InstallEventCallback** (const [can_instance_t](#) *const instance, [can_callback_t](#) callback, void *callbackParam)
Installs a callback function for the IRQ handler.
- void **CAN_GetDefaultConfig** ([can_instance_t](#) *instance, [can_user_config_t](#) *config)
Returns the Default configuration for CAN_PAL instance 0 over FlexCan with a 500K Baud in normal mode, without flexible datarate with oscillator clock source for PE and 8 Bytes payload size.

17.33.2 Data Structure Documentation

17.33.2.1 struct [can_time_segment_t](#)

CAN bit timing variables Implements : [can_time_segment_t](#)_Class.

Definition at line 59 of file [can_pal.h](#).

Data Fields

- uint32_t [propSeg](#)
- uint32_t [phaseSeg1](#)
- uint32_t [phaseSeg2](#)
- uint32_t [preDivider](#)
- uint32_t [rJumpwidth](#)

Field Documentation

17.33.2.1.1 uint32_t phaseSeg1

Phase segment 1

Definition at line 61 of file can_pal.h.

17.33.2.1.2 uint32_t phaseSeg2

Phase segment 2

Definition at line 62 of file can_pal.h.

17.33.2.1.3 uint32_t preDivider

Clock prescaler division factor

Definition at line 63 of file can_pal.h.

17.33.2.1.4 uint32_t propSeg

Propagation segment

Definition at line 60 of file can_pal.h.

17.33.2.1.5 uint32_t rJumpwidth

Resync jump width

Definition at line 64 of file can_pal.h.

17.33.2.2 struct can_buff_config_t

CAN buffer configuration Implements : can_buff_config_t_Class.

Definition at line 94 of file can_pal.h.

Data Fields

- bool [enableFD](#)
- bool [enableBRS](#)
- uint8_t [fdPadding](#)
- [can_msg_id_type_t](#) idType
- bool [isRemote](#)

Field Documentation

17.33.2.2.1 bool enableBRS

Enable bit rate switch inside a CAN FD frame

Definition at line 96 of file can_pal.h.

17.33.2.2.2 `bool enableFD`

Enable flexible data rate

Definition at line 95 of file `can_pal.h`.

17.33.2.2.3 `uint8_t fdPadding`

Value used for padding when the data length code (DLC) specifies a bigger payload size than the actual data length

Definition at line 97 of file `can_pal.h`.

17.33.2.2.4 `can_msg_id_type_t idType`

Specifies whether the frame format is standard or extended

Definition at line 99 of file `can_pal.h`.

17.33.2.2.5 `bool isRemote`

Specifies if the frame is standard or remote

Definition at line 100 of file `can_pal.h`.

17.33.2.3 `struct can_message_t`

CAN message format Implements : `can_message_t_Class`.

Definition at line 106 of file `can_pal.h`.

Data Fields

- `uint32_t cs`
- `uint32_t id`
- `uint8_t data` [64]
- `uint8_t length`

Field Documentation

17.33.2.3.1 `uint32_t cs`

Code and Status

Definition at line 107 of file `can_pal.h`.

17.33.2.3.2 `uint8_t data`[64]

Data bytes of the CAN message

Definition at line 109 of file `can_pal.h`.

17.33.2.3.3 `uint32_t id`

ID of the message

Definition at line 108 of file `can_pal.h`.

17.33.2.3.4 `uint8_t length`

Length of payload in bytes

Definition at line 110 of file `can_pal.h`.

17.33.2.4 `struct can_user_config_t`

CAN controller configuration Implements : `can_user_config_t_Class`.

Definition at line 116 of file can_pal.h.

Data Fields

- uint32_t [maxBuffNum](#)
- [can_operation_modes_t](#) mode
- [can_clk_source_t](#) peClkSrc
- bool [enableFD](#)
- [can_fd_payload_size_t](#) payloadSize
- [can_time_segment_t](#) nominalBitrate
- [can_time_segment_t](#) dataBitrate
- void * [extension](#)

Field Documentation

17.33.2.4.1 [can_time_segment_t](#) dataBitrate

Bit timing segments for data bitrate

Definition at line 124 of file can_pal.h.

17.33.2.4.2 [bool](#) enableFD

Enable flexible data rate

Definition at line 121 of file can_pal.h.

17.33.2.4.3 [void*](#) extension

This field will be used to add extra settings to the basic configuration like FlexCAN Rx FIFO settings

Definition at line 125 of file can_pal.h.

17.33.2.4.4 [uint32_t](#) maxBuffNum

Set maximum number of buffers

Definition at line 118 of file can_pal.h.

17.33.2.4.5 [can_operation_modes_t](#) mode

Set operation mode

Definition at line 119 of file can_pal.h.

17.33.2.4.6 [can_time_segment_t](#) nominalBitrate

Bit timing segments for nominal bitrate

Definition at line 123 of file can_pal.h.

17.33.2.4.7 [can_fd_payload_size_t](#) payloadSize

Set size of buffer payload

Definition at line 122 of file can_pal.h.

17.33.2.4.8 [can_clk_source_t](#) peClkSrc

The clock source of the CAN Protocol Engine (PE).

Definition at line 120 of file can_pal.h.

17.33.2.5 struct extension_flexcan_rx_fifo_t

FlexCAN Rx FIFO configuration Implements : extension_flexcan_rx_fifo_t_Class.

Definition at line 133 of file can_pal.h.

Data Fields

- flexcan_rx_fifo_id_filter_num_t numIdFilters
- flexcan_rx_fifo_id_element_format_t idFormat
- flexcan_id_table_t * idFilterTable

Field Documentation

17.33.2.5.1 flexcan_id_table_t* idFilterTable

Rx FIFO ID table

Definition at line 137 of file can_pal.h.

17.33.2.5.2 flexcan_rx_fifo_id_element_format_t idFormat

RX FIFO ID format

Definition at line 136 of file can_pal.h.

17.33.2.5.3 flexcan_rx_fifo_id_filter_num_t numIdFilters

The number of Rx FIFO ID filters needed

Definition at line 135 of file can_pal.h.

17.33.3 Enumeration Type Documentation

17.33.3.1 enum can_bitrate_phase_t

CAN bitrate phase (nominal/data) Implements : can_bitrate_phase_t_Class.

Enumerator

CAN_NOMINAL_BITRATE Nominal (FD arbitration) bitrate

CAN_FD_DATA_BITRATE FD data bitrate

Definition at line 70 of file can_pal.h.

17.33.3.2 enum can_clk_source_t

CAN PE clock sources Implements : can_clk_source_t_Class.

Enumerator

CAN_CLK_SOURCE_OSC The CAN engine clock source is the oscillator clock.

CAN_CLK_SOURCE_PERIPH The CAN engine clock source is the peripheral clock.

Definition at line 86 of file can_pal.h.

17.33.3.3 enum can_fd_payload_size_t

CAN buffer payload sizes Implements : can_fd_payload_size_t_Class.

Enumerator

CAN_PAYLOAD_SIZE_8 CAN message buffer payload size in bytes

CAN_PAYLOAD_SIZE_16 CAN message buffer payload size in bytes

CAN_PAYLOAD_SIZE_32 CAN message buffer payload size in bytes

CAN_PAYLOAD_SIZE_64 CAN message buffer payload size in bytes

Definition at line 49 of file can_pal.h.

17.33.3.4 enum can_msg_id_type_t

CAN Message Buffer ID type Implements : can_msg_id_type_t_Class.

Enumerator

CAN_MSG_ID_STD Standard ID

CAN_MSG_ID_EXT Extended ID

Definition at line 78 of file can_pal.h.

17.33.3.5 enum can_operation_modes_t

CAN controller operation modes Implements : can_operation_modes_t_Class.

Enumerator

CAN_NORMAL_MODE Normal mode or user mode

CAN_LOOPBACK_MODE Loop-back mode

CAN_DISABLE_MODE Module disable mode

Definition at line 40 of file can_pal.h.

17.33.4 Function Documentation

17.33.4.1 status_t CAN_AbortTransfer (const can_instance_t *const instance, uint32_t buffidx)

Ends a non-blocking CAN transfer early.

Note

When the Rx FIFO extension is used, buffer 0 (zero) is used to read the contents of the FIFO and is configured at the initialization of the driver.

Parameters

in	<i>instance</i>	Instance information structure.
in	<i>buffidx</i>	buffer index.

Returns

STATUS_SUCCESS if successful; STATUS_CAN_NO_TRANSFER_IN_PROGRESS if no transfer was running

Definition at line 903 of file can_pal.c.

17.33.4.2 status_t CAN_ConfigRemoteResponseBuff (const can_instance_t *const instance, uint32_t buffidx, const can_buff_config_t * config, const can_message_t * message)

Configures a transmit buffer for remote frame response.

Parameters

in	<i>instance</i>	Instance information structure.
in	<i>buffidx</i>	buffer index.
in	<i>config</i>	buffer configuration.
in	<i>message</i>	frame to be sent as remote response.

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the buffer index is out of range; STATUS_ERROR if invalid instance number is used;

Definition at line 553 of file can_pal.c.

17.33.4.3 **status_t** CAN_ConfigRxBuff (**const can_instance_t** *const *instance*, **uint32_t** *buffidx*, **const can_buff_config_t** * *config*, **uint32_t** *acceptedId*)

Configures a buffer for reception.

This function configures a buffer for reception.

Note

When the Rx FIFO extension is used, buffer 0 (zero) is used to read the contents of the FIFO and is configured at the initialization of the driver. The user should not reconfigure this buffer for classical buffer reception.

Parameters

in	<i>instance</i>	Instance information structure.
in	<i>buffidx</i>	buffer index.
in	<i>config</i>	buffer configuration.
in	<i>acceptedId</i>	ID used for accepting frames.

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the buffer index is out of range; STATUS_ERROR if invalid instance number is used;

Definition at line 616 of file can_pal.c.

17.33.4.4 **status_t** CAN_ConfigTxBuff (**const can_instance_t** *const *instance*, **uint32_t** *buffidx*, **const can_buff_config_t** * *config*)

Configures a buffer for transmission.

This function configures a buffer for transmission.

Note

When the Rx FIFO extension is used, buffer 0 (zero) is used to read the contents of the FIFO and is configured at the initialization of the driver. The user should not reconfigure this buffer for transmission.

Parameters

in	<i>instance</i>	Instance information structure.
in	<i>buffidx</i>	buffer index.

<i>in</i>	<i>config</i>	buffer configuration.
-----------	---------------	-----------------------

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the buffer index is out of range; STATUS_ERROR if invalid instance number is used;

Definition at line 489 of file can_pal.c.

17.33.4.5 status_t CAN_Deinit (const can_instance_t *const *instance*)

De-initializes the CAN module.

This function de-initializes the CAN module.

Parameters

<i>in</i>	<i>instance</i>	Instance information structure
-----------	-----------------	--------------------------------

Returns

STATUS_SUCCESS if successful; STATUS_ERROR if unsuccessful or invalid instance number;

Definition at line 369 of file can_pal.c.

17.33.4.6 status_t CAN_GetBitrate (const can_instance_t *const *instance*, can_bitrate_phase_t *phase*, can_time_segment_t * *bitTiming*)

Returns the CAN bitrate.

This function returns the CAN configured bitrate.

Parameters

<i>in</i>	<i>instance</i>	Instance information structure.
<i>in</i>	<i>phase</i>	selects between nominal/data phase bitrate.
<i>out</i>	<i>bitTiming</i>	configured bit timing variables.

Returns

STATUS_SUCCESS if successful; STATUS_ERROR if invalid instance number is used;

Definition at line 449 of file can_pal.c.

17.33.4.7 void CAN_GetDefaultConfig (can_instance_t * *instance*, can_user_config_t * *config*)

Returns the Default configuration for CAN_PAL instance 0 over FlexCan with a 500K Baud in normal mode, without flexible datarate with oscillator clock source for PE and 8 Bytes payload size.

Parameters

<i>out</i>	<i>instance</i>	Pointer for can_instance structure.
<i>out</i>	<i>config</i>	Pointer for can_user_config structure.

Definition at line 1072 of file can_pal.c.

17.33.4.8 status_t CAN_GetTransferStatus (const can_instance_t *const *instance*, uint32_t *buffIdx*)

Returns the state of the previous CAN transfer.

When performing an async transfer, call this function to ascertain the state of the current transfer: in progress or complete.

Note

When the Rx FIFO extension is used, buffer 0 (zero) is used to read the contents of the FIFO and is configured at the initialization of the driver.

Parameters

in	<i>instance</i>	Instance information structure.
in	<i>buffidx</i>	buffer index.

Returns

STATUS_SUCCESS if successful; STATUS_BUSY if a resource is busy; STATUS_ERROR if invalid instance number is used;

Definition at line 985 of file can_pal.c.

17.33.4.9 `status_t CAN_Init (const can_instance_t *const instance, const can_user_config_t * config)`

Initializes the CAN module.

This function initializes and enables the requested CAN module.

Note

When the Rx FIFO extension is used, buffer 0 (zero) is used to read the contents of the FIFO and is configured at the initialization of the driver.

Parameters

in	<i>instance</i>	Instance information structure
in	<i>config</i>	The configuration structure

Returns

STATUS_SUCCESS if successful; STATUS_ERROR if unsuccessful or invalid instance number;

Definition at line 263 of file can_pal.c.

17.33.4.10 `status_t CAN_InstallEventCallback (const can_instance_t *const instance, can_callback_t callback, void * callbackParam)`

Installs a callback function for the IRQ handler.

Parameters

in	<i>instance</i>	Instance information structure.
in	<i>callback</i>	The callback function.
in	<i>callbackParam</i>	User parameter passed to the callback function through the state parameter.

Returns

STATUS_SUCCESS if successful; STATUS_ERROR if invalid instance number is used;

Definition at line 1024 of file can_pal.c.

17.33.4.11 `status_t CAN_Receive (const can_instance_t *const instance, uint32_t buffidx, can_message_t * message)`

Receives a CAN frame using the specified message buffer.

This function receives a CAN frame using a configured buffer. The function returns immediately. If a callback is installed, it will be invoked after the frame was received and read into the specified buffer.

Note

When the Rx FIFO extension is used, buffer 0 (zero) is used to read the contents of the FIFO and is configured at the initialization of the driver. The user should use this buffer to receive frames in the FIFO.

Parameters

in	<i>instance</i>	Instance information structure.
in	<i>buffidx</i>	buffer index.
out	<i>message</i>	received message.

Returns

STATUS_SUCCESS if successful; STATUS_BUSY if the current buffer is involved in another transfer; STATUS_CAN_BUFF_OUT_OF_RANGE if the buffer index is out of range; STATUS_ERROR if invalid instance number is used;

Definition at line 797 of file can_pal.c.

17.33.4.12 `status_t CAN_ReceiveBlocking (const can_instance_t *const instance, uint32_t buffidx, can_message_t *message, uint32_t timeoutMs)`

Receives a CAN frame using the specified buffer, in a blocking manner.

This function receives a CAN frame using a configured buffer. The function blocks until either a frame was received, or the specified timeout expired.

Note

When the Rx FIFO extension is used, buffer 0 (zero) is used to read the contents of the FIFO and is configured at the initialization of the driver. The user should use this buffer to receive frames in the FIFO.

Parameters

in	<i>instance</i>	Instance information structure.
in	<i>buffidx</i>	buffer index.
out	<i>message</i>	received message.
in	<i>timeoutMs</i>	A timeout for the transfer in milliseconds.

Returns

STATUS_SUCCESS if successful; STATUS_BUSY if the current buffer is involved in another transfer; STATUS_TIMEOUT if the timeout is reached; STATUS_CAN_BUFF_OUT_OF_RANGE if the buffer index is out of range; STATUS_ERROR if invalid instance number is used;

Definition at line 849 of file can_pal.c.

17.33.4.13 `status_t CAN_Send (const can_instance_t *const instance, uint32_t buffidx, const can_message_t *message)`

Sends a CAN frame using the specified buffer.

This function sends a CAN frame using a configured buffer. The function returns immediately. If a callback is installed, it will be invoked after the frame was sent.

Note

When the Rx FIFO extension is used, buffer 0 (zero) is used to read the contents of the FIFO and is configured at the initialization of the driver. The user should not use this buffer for transmission.

Parameters

in	<i>instance</i>	Instance information structure.
in	<i>buffIdx</i>	buffer index.
in	<i>message</i>	message to be sent.

Returns

STATUS_SUCCESS if successful; STATUS_BUSY if the current buffer is involved in another transfer; STATUS_CAN_BUFF_OUT_OF_RANGE if the buffer index is out of range; STATUS_ERROR if invalid instance number is used;

Definition at line 678 of file can_pal.c.

17.33.4.14 `status_t CAN_SendBlocking (const can_instance_t *const instance, uint32_t buffIdx, const can_message_t * message, uint32_t timeoutMs)`

Sends a CAN frame using the specified buffer, in a blocking manner.

This function sends a CAN frame using a configured buffer. The function blocks until either the frame was sent, or the specified timeoutMs expired.

Note

When the Rx FIFO extension is used, buffer 0 (zero) is used to read the contents of the FIFO and is configured at the initialization of the driver. The user should not use this buffer for transmission.

Parameters

in	<i>instance</i>	Instance information structure.
in	<i>buffIdx</i>	buffer index.
in	<i>message</i>	message to be sent.
in	<i>timeoutMs</i>	A timeout for the transfer in milliseconds.

Returns

STATUS_SUCCESS if successful; STATUS_BUSY if the current buffer is involved in another transfer; STATUS_TIMEOUT if the timeout is reached; STATUS_CAN_BUFF_OUT_OF_RANGE if the buffer index is out of range; STATUS_ERROR if invalid instance number is used;

Definition at line 737 of file can_pal.c.

17.33.4.15 `status_t CAN_SetBtrRate (const can_instance_t *const instance, can_bitrate_phase_t phase, const can_time_segment_t * bitTiming)`

Configures the CAN bitrate.

This function configures the CAN bit timing variables.

Parameters

in	<i>instance</i>	Instance information structure.
in	<i>phase</i>	selects between nominal/data phase bitrate.
in	<i>bitTiming</i>	bit timing variables.

Returns

STATUS_SUCCESS if successful; STATUS_ERROR if invalid instance number is used;

Definition at line 402 of file can_pal.c.

17.33.4.16 `status_t CAN_SetRxFilter (const can_instance_t *const instance, can_msg_id_type_t idType, uint32_t buffIdx, uint32_t mask)`

Configures an ID filter for a specific reception buffer.

This function configures an ID filter for each reception buffer.

Note

When the Rx FIFO extension is used, buffer 0 (zero) is used to read the contents of the FIFO and is configured at the initialization of the driver. The user should not reconfigure the Rx filter for this buffer.

Parameters

<code>in</code>	<code>instance</code>	Instance information structure.
<code>in</code>	<code>idType</code>	selects between standard and extended ID.
<code>in</code>	<code>buffIdx</code>	buffer index.
<code>in</code>	<code>mask</code>	mask value for ID filtering.

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the buffer index is out of range; STATUS_ERROR if invalid instance number is used;

Definition at line 942 of file can_pal.c.

17.34 Controller Area Network with Flexible Data Rate (FlexCAN)

17.34.1 Detailed Description

The S32 SDK provides a Peripheral Driver for the FlexCAN module of S32 SDK devices.

Hardware background

The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1 standard and CAN 2.0 B protocol specifications. The FlexCAN module is a full implementation of the CAN protocol specification, the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads up to 64 bytes transferred at faster rates up to 8 Mbps. The message buffers are stored in an embedded RAM dedicated to the FlexCAN module.

The FlexCAN module includes these distinctive features:

- Full implementation of the CAN with Flexible Data Rate (CAN FD) protocol specification and CAN protocol specification, Version 2.0 B (see the `FEATURE_CAN_HAS_FD` define for the availability of this feature on each platform)
 - Standard data frames
 - Extended data frames
 - Zero to sixty four bytes data length
 - Programmable bit rate (see the chip-specific FlexCAN information for the specific maximum bit rate configuration)
 - Content-related addressing
- Compliant with the ISO 11898-1 standard
- Flexible mailboxes configurable to store 0 to 8, 16, 32 or 64 bytes data length (payloads longer than 8 bytes are available only for some platforms, see the `FEATURE_CAN_HAS_FD` define)
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Rx FIFO with storage capacity for up to six frames and automatic internal pointer handling with DMA support (DMA support is available only for some platforms, see the `FEATURE_CAN_HAS_DMA_ENABLE` define)
- Transmission abort capability
- Flexible message buffers (MBs) configurable as Rx or Tx (see the `FEATURE_CAN_MAX_MB_NUM` define for the specific maximum number of message buffers configurable on each platform)
- Programmable clock source to the CAN Protocol Interface, either peripheral clock or oscillator clock (this feature might differ depending on the platform, see `FEATURE_CAN_HAS_PE_CLKSRC_SELECT` define for the availability of this feature on each platform)
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Maskable interrupts
- Short latency time due to an arbitration scheme for high-priority messages
- Low power modes or matching with received frames - Pretended Networking (see `FEATURE_CAN_HAS_PRETENDED_NETWORKING` define for the availability of this feature on each platform)
- Transceiver Delay Compensation feature when transmitting CAN FD messages at faster data rates (see the `FEATURE_CAN_HAS_FD` define for the availability of this feature on each platform)

- Remote request frames may be handled automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- SYNCH bit available in Error in Status 1 register to inform that the module is synchronous with CAN bus
- CRC status for transmitted message
- Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 individual masking capability
- 100% backward compatibility with previous FlexCAN version
- Supports Pretended Networking functionality in low power: Stop mode (see FEATURE_CAN_HAS_PRETENDED_NETWORKING define for the availability of this feature on each platform)
- Supports detection and correction of errors in memory read accesses. Errors in one bit can be corrected and errors in 2 bits can be detected but not corrected (this feature might not be available on some platforms, see chip-specific FlexCAN information for details)
- Supports Self Wake Up feature when FlexCAN is in a low power mode: Stop mode (see FEATURE_CAN_HAS_SELF_WAKE_UP define for the availability of this feature on each platform)
- Disable Detection and Correction of Memory Errors Feature for devices that supports it. This feature can cause Freeze Mode of CAN interface. (see FEATURE_CAN_HAS_MEM_ERR_DET define availability of the feature in module)

Modules

- [FlexCAN Driver](#)

17.35 Cooked API

17.35.1 Detailed Description

Cooked processing of diagnostic messages manages one complete message at a time.

Functions

- void [ld_send_message](#) (I_ifc_handle iii, I_u16 length, I_u8 NAD, const I_u8 *const data)
Pack the information specified by data and length into one or multiple diagnostic frames.
- void [ld_receive_message](#) (I_ifc_handle iii, I_u16 *const length, I_u8 *const NAD, I_u8 *const data)
Prepare the LIN diagnostic module to receive one message and store it in the buffer pointed to by data.
- I_u8 [ld_tx_status](#) (I_ifc_handle iii)
Get the status of the last made call to ld_send_message.
- I_u8 [ld_rx_status](#) (I_ifc_handle iii)
Get the status of the last made call to ld_send_message.

17.35.2 Function Documentation

17.35.2.1 void ld_receive_message (I_ifc_handle iii, I_u16 *const length, I_u8 *const NAD, I_u8 *const data)

Prepare the LIN diagnostic module to receive one message and store it in the buffer pointed to by data.

Parameters

in	iii	Lin interface handle
in	length	Length of data to receive
in	NAD	Node address of slave node
in	data	Data to be sent

Returns

void

Prepare the LIN diagnostic module to receive one message and store it in the buffer pointed to by data. At the call, length shall specify the maximum length allowed. When the reception has completed, length is changed to the actual length and NAD to the NAD in the message.

Definition at line 261 of file lin_commontl_api.c.

17.35.2.2 I_u8 ld_rx_status (I_ifc_handle iii)

Get the status of the last made call to ld_send_message.

Parameters

in	iii	Lin interface handle
----	-----	----------------------

Returns

I_u8

The call returns the status of the last made call to ld_receive_message. < br / > The following values can be returned: < br / > LD_IN_PROGRESS: The reception is not yet completed. < br / > LD_COMPLETED: The reception has completed successfully and all < br / > information (length, NAD, data) is available. (You can < br / > also issue a new ld_receive_message call). This < br / > value is also returned after initialization of the < br / > transport layer. < br / > LD_FAILED: The reception ended in an error. The data was only < br / > partially received and should not be trusted. Initialize < br / > before processing further transport layer messages. < br /

> For LIN2.0 and J2602 Users can make a new call to `ld_receive_message`. For LIN2.1 and above, the transport layer shall be reinitialized before processing further messages. To find out why a transmission has failed, check the status management function `l_ifc_read_status`. * `LD_N_CR_TIMEOUT` The reception failed because of a `N_Cr` timeout (For LIN2.1 and above only) < br / > `LD_WRONG_SN` The reception failed because of an unexpected sequence number. (For LIN2.1 and above only)

Definition at line 307 of file `lin_commontl_api.c`.

17.35.2.3 `void ld_send_message (l_ifc_handle iii, l_u16 length, l_u8 NAD, const l_u8 *const data)`

Pack the information specified by data and length into one or multiple diagnostic frames.

Parameters

in	<i>iii</i>	Lin interface handle
in	<i>length</i>	Length of data to send
in	<i>NAD</i>	Node address of slave node
in	<i>data</i>	Data to be sent

Returns

void

Pack the information specified by data and length into one or multiple diagnostic frames. If the call is made in a master node application the frames are transmitted to the slave node with the address `NAD`. If the call is made in a slave node application the frames are transmitted to the master node with the address `NAD`. The parameter `NAD` is not used in slave nodes.

Definition at line 207 of file `lin_commontl_api.c`.

17.35.2.4 `l_u8 ld_tx_status (l_ifc_handle iii)`

Get the status of the last made call to `ld_send_message`.

Parameters

in	<i>iii</i>	Lin interface handle
----	------------	----------------------

Returns

`l_u8`

Get the status of the last made call to `ld_send_message`. The following values can be returned: `LD_IN_PROGRESS`: The transmission is not yet completed. `LD_COMPLETED`: The transmission has completed successfully (and you can issue a new `ld_send_message` call). This value is also returned after initialization of the transport layer. `LD_FAILED`: The transmission ended in an error. The data was only partially sent. The transport layer shall be reinitialized before processing further messages. To find out why a transmission has failed, check the status management function `l_read_status`. For LIN2.0 and J2602 Users can make a new call to `ld_send_message`. For LIN2.1 and above, the transport layer shall be reinitialized before processing further messages. `LD_N_AS_TIMEOUT`: The transmission failed because of a `N_As` timeout. This applies for LIN2.1 and above only.

Definition at line 291 of file `lin_commontl_api.c`.

17.36 Cryptographic Services Engine (CSEc)

17.36.1 Detailed Description

The S32 SDK provides a Peripheral Driver for the Cryptographic Services Engine (CSEc) module of S32 SDK devices.

The FTFC module has added features to comply with the SHE specification. By using an embedded processor, firmware and hardware assisted AES-128 sub-block, the FTFC macro enables encryption, decryption and message generation and authentication algorithms for secure messaging applications. Additionally a TRNG and Miyaguchi-Prenell compression sub-blocks enables true random number generation (entropy generator for PRNG in AES sub-block).

Hardware background

Features of the CSEc module include:

- Secure cryptographic key storage (ranging from 3 to 21 user keys)
- AES-128 encryption and decryption
- AES-128 CMAC (Cipher-based Message Authentication Code) calculation and authentication
- ECB (Electronic Cypher Book) Mode - encryption and decryption
- CBC (Cipher Block Chaining) Mode - encryption and decryption
- True and Pseudo random number generation
- Miyaguchi-Prenell compression function
- Secure Boot Mode (user configurable)
 - Sequential Boot Mode
 - Parallel Boot Mode
 - Strict Sequential Boot Mode (unchangeable once set)

Modules

- [CSEc Driver](#)
Cryptographic Services Engine Peripheral Driver.

17.37 Cyclic Redundancy Check (CRC)

17.37.1 Detailed Description

The S32 SDK provides Peripheral Drivers for the Cyclic Redundancy Check (CRC) module.

1. CRC with S32K1xx and **S32K1xxW**:

- Generate 16/32-bit CRC code for error detection.
- Provides a programmable polynomial, seed, and other parameters required to implement 16/32-bit CRC standard.
- Calculate 16/32-bit code for 32 bits of data at a time.

2. CRC with MPC574x and S32Rx7x:

- Generate 8/16/32-bit CRC code for error detection.
- Provides a programmable polynomial, seed, and other parameters required to implement 8/16/32-bit CRC standard.
- Calculate 8/16/32-bit code for 32 bits of data at a time.

Important note when use CRC module with MPC574x and S32Rx7x devices:

- When generating CRC-32 for the ITU-T V.42 standard the user needs to set SWAP_BYTEWISE together with INV and SWAP.
- When generating CRC-16-CCITT(0x1021) standard the user needs to set SWAP_BITWISE bit.

Basic Operations of CRC

1. To initialize the CRC module, call [CRC_DRV_Init\(\)](#) function and pass the user configuration data structure to it. This is example code to configure the CRC driver using [CRC_DRV_GetDefaultConfig\(\)](#) function:

```
#define INST_CRC1 (0U)

/* Configuration structure crc1_InitConfig0 */
crc_user_config_t crc1_InitConfig0;

/* Get default configuration for CRC module: CRC-16-CCITT (0x1021) standard */
CRC_DRV_GetDefaultConfig(&crc1_InitConfig0);

/* Initializes the CRC */
CRC_DRV_Init(INST_CRC1, &crc1_InitConfig0);
```

2. To configure and operate the CRC module: Function [CRC_DRV_Configure\(\)](#) shall be used to write user configuration to CRC hardware module before starting operation by calling [CRC_DRV_WriteData\(\)](#). Finally, using [CRC_DRV_GetCrcResult\(\)](#) function to get the result of CRC calculation. This is example code to configure and get CRC block for S32K1xx:

```
#define INST_CRC1 (0U)

uint8_t buffer[] = { 0x31, 0x32, 0x33, 0x34, 0x35, 0x36, 0x37, 0x38, 0x39, 0x30 };
uint32_t result;

/* Set the CRC configuration: CRC-16-CCITT (0x1021) standard */
CRC_DRV_Configure(INST_CRC1, &crc1_InitConfig0);
/* Write data to the current CRC calculation */
CRC_DRV_WriteData(INST_CRC1, buffer, 10U);
/* Get result of CRC calculation (0x3218U) */
result = CRC_DRV_GetCrcResult(INST_CRC1);

/* De-init */
CRC_DRV_Deinit(INST_CRC1);
```

3. To get result of 32-bit data call [CRC_DRV_GetCrc32\(\)](#) function.

```

#define INST_CRC1 (0U)

uint32_t seed = 0xFFFFU;
uint32_t data = 0x12345678U;
uint32_t result;

/* Get result of 32-bit data (0x30EC) at CRC-16-CCITT (0x1021) standard configuration mode */
result = CRC_DRV_GetCrc32(INST_CRC1, data, true, seed);

```

4. To get result of 16-bit data call [CRC_DRV_GetCrc16\(\)](#) function.

```

#define INST_CRC1 (0U)

uint32_t seed = 0xFFFFU;
uint16_t data = 0x1234U;
uint32_t result;

/* Get result of 16-bit data (0x0EC9) at CRC-16-CCITT (0x1021) standard configuration mode */
result = CRC_DRV_GetCrc16(INST_CRC1, data, true, seed);

```

5. To get current configuration of the CRC module, just call [CRC_DRV_GetConfig\(\)](#) function.

```

#define INST_CRC1 (0U)
crc_user_config_t crc1_InitConfig0;

/* Get current configuration of the CRC module */
CRC_DRV_GetConfig(INST_CRC1, &crc1_InitConfig0);

```

6. To Get default configuration of the CRC module, just call [CRC_DRV_GetDefaultConfig\(\)](#) function.

```

#define INST_CRC1 (0U)
crc_user_config_t crc1_InitConfig0;

/* Get default configuration of the CRC module */
CRC_DRV_GetDefaultConfig(&crc1_InitConfig0);

```

Integration guideline

Compilation units

The following files need to be compiled in the project: For **S32K1xx** and **S32K1xxW**:

```

${S32SDK_PATH}\platform\drivers\src\crc\crc_driver.c
${S32SDK_PATH}\platform\drivers\src\crc\crc_hw_access.c

```

For **MPC574x** and **S32Rx7x**:

```

${S32SDK_PATH}\platform\drivers\src\crc\crc_driver.c
${S32SDK_PATH}\platform\drivers\src\crc\crc_c55_hw_access.c

```

Include path

The following paths need to be added to the include path of the toolchain:

```

${S32SDK_PATH}\platform\drivers\inc\

```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager](#)

Modules

- [CRC Driver](#)

Cyclic Redundancy Check Peripheral Driver.

17.38 Diagnostic services

17.38.1 Detailed Description

Diagnostic services defines methods to implement diagnostic data transfer between a master node connected with a diagnostic tester and the slave nodes.

Three different classes of diagnostic nodes are supported.

The master node and the diagnostic tester are connected via a back-bone bus (e.g. CAN). The master node shall receive all diagnostic requests addressed to the slave nodes from the back-bone bus, and gateway them to the correct LIN cluster(s). Responses from the slave nodes shall be gatewayed back to the back-bone bus through the master node.

All diagnostic requests and responses (services) addressed to the slave nodes can be routed in the network layer (i.e. no application layer routing). In this case, the master node must implement the LIN transport protocol, see Transport Layer Specification, as well as the transport protocols used on the back-bone busses (e.g. ISO15765-2 on CAN).

Currently, LinStack support some service. With other service which LinStack doesn't support or user want to add action when any service is received, user can choose or create service in supported services of PEX GUI and use API of transport layer to implement it. in application.

Example in slave node:

```
for(;;)
{
    /* length shall specify the maximum length allowed */
    length = 106;
    ld_receive_message(LI0,&length, &nad, req_data);
    /* if receive READ_DATA_BY_IDENTIFIER master request successfully */
    if(diag_get_flag(LI0, LI0_DIAGSRV_READ_DATA_BY_IDENTIFIER_ORDER))
    {
        diag_clear_flag(LI0, LI0_DIAGSRV_READ_DATA_BY_IDENTIFIER_ORDER);
        /* implement what you want to do when receive this message
           length will return real length of this message
           req_data will contain SID and data of this message */
        /* send back response data */
        ld_send_message(LI0,17,nad, res_data);
    }
}
```

Modules

- [Node configuration](#)
This group contains APIs that used for node configuration purpose.
- [Node identification](#)
This group contains API that used for node identification purpose.

Functions

- void [diag_read_data_by_identifier](#) (l_ifc_handle iii, const l_u8 NAD, const l_u8 number_of_id, const l_u16 *const list_of_id)
This function reads data by identifier, Diagnostic Class II service (0x22).
- void [diag_write_data_by_identifier](#) (l_ifc_handle iii, const l_u8 NAD, l_u16 data_length, const l_u8 *const data)
Write Data by Identifier for a specified node - Diagnostic Class II service (0x2E)
- void [diag_session_control](#) (l_ifc_handle iii, const l_u8 NAD, const l_u8 session_type)
This function is used for master node only. It will pack data and send request to slave node with service ID = 0x10: Session control.
- void [diag_fault_memory_read](#) (l_ifc_handle iii, const l_u8 NAD, l_u16 data_length, const l_u8 *const data)

This function is used for master node only. It will pack data and send request to slave node with service ID = 0x19: Fault memory read.

- void [diag_fault_memory_clear](#) (I_ifc_handle iii, const I_u8 NAD, const I_u8 *const groupOfDTC)

This function is used for master node only. It will pack data and send request to slave node with service ID = 0x14: Fault memory clear.

- void [diag_IO_control](#) (I_ifc_handle iii, const I_u8 NAD, I_u16 data_length, const I_u8 *const data)

This function is used for master node only. It will pack data and send request to slave node with service ID = 0x2F: Input/Output control service.

- I_u8 [diag_get_flag](#) (I_ifc_handle iii, I_u8 flag_order)

This function will return flag of diagnostic service, if LIN slave node receive master request of the diagnostic service.

- void [diag_clear_flag](#) (I_ifc_handle iii, I_u8 flag_order)

This function will clear flag of diagnostic service,.

17.38.2 Function Documentation

17.38.2.1 void [diag_clear_flag](#) (I_ifc_handle iii, I_u8 flag_order)

This function will clear flag of diagnostic service,.

Parameters

in	iii	LIN interface handle
in	flag_order	Order of service flag

Returns

void

Definition at line 1013 of file lin_diagnostic_service.c.

17.38.2.2 void [diag_fault_memory_clear](#) (I_ifc_handle iii, const I_u8 NAD, const I_u8 *const groupOfDTC)

This function is used for master node only. It will pack data and send request to slave node with service ID = 0x14: Fault memory clear.

Parameters

in	iii	LIN interface handle
in	NAD	Node address value of the destination node for the transmission
in	groupOfDTC	contain 3 byte will be transmit follow (byte 0: HighByte, byte 1: Middle Byte, byte 2: Low Byte) to be transmitted

Returns

void

Definition at line 759 of file lin_diagnostic_service.c.

17.38.2.3 void [diag_fault_memory_read](#) (I_ifc_handle iii, const I_u8 NAD, I_u16 data_length, const I_u8 *const data)

This function is used for master node only. It will pack data and send request to slave node with service ID = 0x19: Fault memory read.

Parameters

in	<i>iii</i>	LIN interface handle
in	<i>NAD</i>	Node address value of the destination node for the transmission
in	<i>data_length</i>	Data length of frame
in	<i>data</i>	Buffer for the data to be transmitted

Returns

void

Definition at line 713 of file lin_diagnostic_service.c.

17.38.2.4 I_u8 diag_get_flag (I_ifc_handle *iii*, I_u8 *flag_order*)

This function will return flag of diagnostic service, if LIN slave node receive master request of the diagnostic service.

Parameters

in	<i>iii</i>	LIN interface handle
in	<i>flag_order</i>	Order of service flag

Returns

1 if LIN Slave node receives master request of the diagnostic service, and the flag has not been cleared by diag_clear_flag
 0 default value
 0xFF if service is not supported

Definition at line 982 of file lin_diagnostic_service.c.

17.38.2.5 void diag_IO_control (I_ifc_handle *iii*, const I_u8 *NAD*, I_u16 *data_length*, const I_u8 *const *data*)

This function is used for master node only. It will pack data and send request to slave node with service ID = 0x2F: Input/Output control service.

Parameters

in	<i>iii</i>	LIN interface handle
in	<i>NAD</i>	Node address value of the destination node for the transmission
in	<i>data_length</i>	Data length of frame
in	<i>data</i>	Buffer for the data to be transmitted

Returns

void

Definition at line 796 of file lin_diagnostic_service.c.

17.38.2.6 void diag_read_data_by_identifier (I_ifc_handle *iii*, const I_u8 *NAD*, const I_u8 *number_of_id*, const I_u16 *const *list_of_id*)

This function reads data by identifier, Diagnostic Class II service (0x22).

Parameters

in	<i>iii</i>	LIN interface handle
in	<i>NAD</i>	Node address value of the destination node for the transmission

in	<i>number_of_id</i>	number id that send in this request
in	<i>list_of_id</i>	list of id that send in this request

Returns

void

This function is for Master node only.

Definition at line 580 of file lin_diagnostic_service.c.

17.38.2.7 void diag_session_control (I_ifc_handle *iii*, const I_u8 *NAD*, const I_u8 *session_type*)

This function is used for master node only. It will pack data and send request to slave node with service ID = 0x10: Session control.

Parameters

in	<i>iii</i>	LIN interface handle
in	<i>NAD</i>	Node address value of the destination node for the transmission
in	<i>session_type</i>	is sub function of diagnostic session master request

Returns

void

Definition at line 679 of file lin_diagnostic_service.c.

17.38.2.8 void diag_write_data_by_identifier (I_ifc_handle *iii*, const I_u8 *NAD*, I_u16 *data_length*, const I_u8 *const *data*)

Write Data by Identifier for a specified node - Diagnostic Class II service (0x2E)

Parameters

in	<i>iii</i>	Lin interface handle
in	<i>NAD</i>	Node address value of the destination node for the transmission
in	<i>data_length</i>	Data length of frame
in	<i>data</i>	Buffer for the data to be transmitted

Returns

void

This function is for Master node only.

Definition at line 629 of file lin_diagnostic_service.c.

17.39 Driver and cluster management

17.39.1 Detailed Description

API perform the initialization of the LIN core.

Functions

- `I_bool I_sys_init (void)`

This function performs the initialization of the LIN core; is the first call a user must use in the LIN core before using any other API functions. The implementation of this function can be replaced by user if needed.

17.39.2 Function Documentation

17.39.2.1 `I_bool I_sys_init (void)`

This function performs the initialization of the LIN core; is the first call a user must use in the LIN core before using any other API functions. The implementation of this function can be replaced by user if needed.

Returns

Operation status = Zero, which is equivalent to 'Initialization was successful'.

Definition at line 57 of file `lin_common_api.c`.

17.40 EDMA Driver

17.40.1 Detailed Description

This module covers the functionality of the Enhanced Direct Memory Access (eDMA) peripheral driver.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32KSDK_PATH}\platform\drivers\src\edma\edma_driver.c  
${S32KSDK_PATH}\platform\drivers\src\edma\edma_hw_access.c  
${S32KSDK_PATH}\platform\drivers\src\edma\edma_irq.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32KSDK_PATH}\platform\drivers\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager Interrupt Manager \(Interrupt\)](#)

The eDMA driver implements direct memory access functionality with multiple features: (single block/multi block/loop/scatter-gather transfers); the main usage of this module is to offload the bus read/write accesses from the core to the eDMA engine.

Features

- Memory-to-memory, peripheral-to-memory, memory-to-peripheral transfers
- Simple single-block transfers with minimum configuration
- Multi-block transfers with minimum configuration (based on subsequent requests)
- Loop transfers for complex use-cases (e.g. double buffering)
- Scatter/gather
- Dynamic channel allocation

Functionality

Initialization

In order to use the eDMA driver, the module must be first initialized, using [EDMA_DRV_Init\(\)](#) function. Once initialized, it cannot be initialized again until it is de-initialized, using [EDMA_DRV_Deinit\(\)](#). The initialization function does the following operations:

- resets eDMA and DMAMUX modules
- clears the eDMA driver state structure
- sets the arbitration mode and halt settings
- enables error and channel interrupts

Upon module initialization, the application must initialize the channel(s) to be used, using [EDMA_DRV_ChannelInit\(\)](#) function. This operation means enabling an eDMA channel number (or dynamically allocating one), selecting a source trigger (eDMA request multiplexed via DMAMUX) and setting the channel priority. Additionally, a user callback can be installed for each channel, which will be called when the corresponding interrupt is triggered.

Transfer Configuration

After initialization, the transfer control descriptor for the selected channel must be configured before use. Depending on the application use-case, one of the three transfer configuration methods should be called.

Single-block transfer

For the simplest use-case where a contiguous chunk of data must be transferred, the most suitable function is [EDMA_DRV_ConfigSingleBlockTransfer\(\)](#). This takes the source/destination addresses as parameters, as well as transfer type/size and data buffer size, and configures the channel TCD to read/write the data in a single request. The looping and scatter/gather features are not used in this scenario. The driver computes the appropriate offsets for source/destination addresses and sets the other TCD fields.

Multi-block transfer

This type of transfer can be seen as a sequence of single-block transfers, as described above, which are triggered by subsequent requests. This configuration is suitable for contiguous chunks of data which need to be transferred in multiple steps (e.g. writing one/several bytes from a memory buffer to a peripheral data register each time the module is free - eDMA-based communication). In order to configure this kind of transfer, [EDMA_DRV_ConfigMultiBlockTransfer\(\)](#) function should be used; aside from the [EDMA_DRV_ConfigSingleBlockTransfer](#) parameters, this function also takes two additional parameters: the number of transfer loops (expected number of requests to finish the data) and a boolean variable configuring whether requests should be disabled for the current channel upon transfer completion.

Loop transfer

The eDMA IP supports complex addressing modes. One of the methods to configure complex transfers in multiple requests is using the minor/major loop support. The [EDMA_DRV_ConfigLoopTransfer\(\)](#) function sets up the transfer control descriptor for subsequent requests to trigger multiple transfers. The addresses are adjusted after each minor/major loop, according to user setup. This method takes a transfer configuration structure as parameter, with settings for all the fields that control addressing mode (source/destination offsets, minor loop offset, channel linking, minor/major loop count, address last adjustments). It is the responsibility of the application to correctly initialize the configuration structure passed to this function, according to the addressed use-case.

Scatter/gather

The eDMA driver also supports scatter/gather feature, which allows various transfer scenarios. When scatter/gather is enabled, a new TCD structure is automatically loaded in the current channel's TCD registers when a transfer is complete, allowing the application to define multiple different subsequent transfers. The [EDMA_DRV_ConfigScatterGatherTransfer\(\)](#) function sets up a list of TCD structures based on the parameters received and configures the eDMA channel for the first transfer; upon completion, the second TCD from the list will be loaded and the channel will be ready to start the new transfer when a new request is received.

The application must allocate memory for the TCD list passed to this function (with an extra 32-bytes buffer, as the TCD structures need to be 32 bytes aligned); nevertheless, the driver will take care of initializing the array of descriptors, based on the other parameters passed. The function also received two lists of scatter/gather configuration structures (for source and destination, respectively), which define the address, length and type for each transfer. Besides these, the other parameters received are the transfer size, the number of bytes to be transferred on each request and the number of TCD structures to be used. This method will initialize all the descriptors according to user input and link them together; the linkage is done by writing the address of the next descriptor in the appropriate field of each one, similar to a linked-list data structure. The first descriptor is also copied to the TCD registers of the selected channel; if no errors are returned, after calling this function the channel is configured for the transfer defined by the first descriptor.

Virtual Channel Definition

The virtual channel is used to map multiple hardware channels across multiple eDMA instances. If only one eDMA instance is available, then the virtual channels will map one-on-one with the hardware channels. If more than one eDMA instance is available, then the virtual channels will map continuously and linearly over all of the hardware channels. Example: If the SOC has 4 eDMA modules, each with 32 channels, then the user will be able to address a total of 128 virtual channels, that seamlessly map onto the hardware channels.

Virtual Channel Control

The eDMA driver provides functions that allow the user to start, stop, allocate and release an eDMA virtual channel. The [EDMA_DRV_StartChannel\(\)](#) enables the eDMA requests for a virtual channel; this function should be called when the virtual channel is already initialized, as the first request received after the function call will trigger the transfer based on the current values of the virtual channel's TCD registers.

The [EDMA_DRV_StopChannel\(\)](#) function disables requests for the selected virtual channel; this function should be called whenever the application needs to ignore eDMA requests for a virtual channel. It is automatically called when the virtual channel is released.

The [EDMA_DRV_SetChannelRequestAndTrigger\(\)](#) function configures the selected virtual channel request and also configures the periodic trigger functionality of the eDMA channel.

Periodic triggering is used by an internal timer to control an eDMA channel.

The [EDMA_DRV_ReleaseChannel\(\)](#) function frees the hardware and software resources allocated for that virtual channel; it clears the virtual channel state structure, updates the driver state and disables requests for that virtual channel.

Important Notes

- Before using the eDMA driver the clock for eDMA and DMAMUX modules must be configured
- The driver enables the interrupts for the eDMA module, but any interrupt priority must be done by the application
- When using the modulo feature, application is responsible with ensuring that the source/destination address is properly aligned on a modulo-size boundary.
- The source/destination address must be aligned with transfer size. Ex: With transfer size is 8 bytes, the source/destination address is multiple of 8.
- When using Single-block transfer or Multi-block transfer, NBYTES (Number of bytes to be transferred in each service request of the channel) shall be always configurable on 30 bits instead of 32 bits. This is a limitation only on EDMA Hardware version 2 (S32K1xx platform).
- Limitation of IAR compiler: function alignment is not supported using `ALIGNED()` macro.

Data Structures

- struct [edma_user_config_t](#)
The user configuration structure for the eDMA driver. [More...](#)
- struct [edma_chn_state_t](#)
Data structure for the eDMA channel state. Implements : [edma_chn_state_t_Class](#). [More...](#)
- struct [edma_channel_config_t](#)
The user configuration structure for the an eDMA driver channel. [More...](#)
- struct [edma_scatter_gather_list_t](#)
Data structure for configuring a discrete memory transfer. Implements : [edma_scatter_gather_list_t_Class](#). [More...](#)
- struct [edma_state_t](#)
Runtime state structure for the eDMA driver. [More...](#)
- struct [edma_loop_transfer_config_t](#)
eDMA loop transfer configuration. [More...](#)
- struct [edma_transfer_config_t](#)

eDMA transfer size configuration. [More...](#)

- struct [edma_software_tcd_t](#)
eDMA TCD Implements : [edma_software_tcd_t_Class](#) [More...](#)

Macros

- #define [STCD_SIZE](#)(number) (((number) * 32U) - 1U)
Macro for the memory size needed for the software TCD.
- #define [STCD_ADDR](#)(address) (((uint32_t)address + 31UL) & ~0x1FUL)
- #define [EDMA_ERR_LSB_MASK](#) 1U
Macro for accessing the least significant bit of the ERR register.

Typedefs

- typedef void(* [edma_callback_t](#)) (void *parameter, [edma_chn_status_t](#) status)
Definition for the eDMA channel callback function.

Enumerations

- enum [edma_channel_interrupt_t](#) { [EDMA_CHN_ERR_INT](#) = 0U, [EDMA_CHN_HALF_MAJOR_LOOP_INT](#), [EDMA_CHN_MAJOR_LOOP_INT](#) }
eDMA channel interrupts. Implements : [edma_channel_interrupt_t_Class](#)
- enum [edma_arbitration_algorithm_t](#) { [EDMA_ARBITRATION_FIXED_PRIORITY](#) = 0U, [EDMA_ARBITRATION_ROUND_ROBIN](#) }
eDMA channel arbitration algorithm used for selection among channels. Implements : [edma_arbitration_algorithm_t_Class](#)
- enum [edma_channel_priority_t](#) { [EDMA_CHN_PRIORITY_0](#) = 0U, [EDMA_CHN_PRIORITY_1](#) = 1U, [EDMA_CHN_PRIORITY_2](#) = 2U, [EDMA_CHN_PRIORITY_3](#) = 3U, [EDMA_CHN_PRIORITY_4](#) = 4U, [EDMA_CHN_PRIORITY_5](#) = 5U, [EDMA_CHN_PRIORITY_6](#) = 6U, [EDMA_CHN_PRIORITY_7](#) = 7U, [EDMA_CHN_PRIORITY_8](#) = 8U, [EDMA_CHN_PRIORITY_9](#) = 9U, [EDMA_CHN_PRIORITY_10](#) = 10U, [EDMA_CHN_PRIORITY_11](#) = 11U, [EDMA_CHN_PRIORITY_12](#) = 12U, [EDMA_CHN_PRIORITY_13](#) = 13U, [EDMA_CHN_PRIORITY_14](#) = 14U, [EDMA_CHN_PRIORITY_15](#) = 15U, [EDMA_CHN_DEFAULT_PRIORITY](#) = 255U }
eDMA channel priority setting Implements : [edma_channel_priority_t_Class](#)
- enum [edma_modulo_t](#) { [EDMA_MODULO_OFF](#) = 0U, [EDMA_MODULO_2B](#), [EDMA_MODULO_4B](#), [EDMA_MODULO_8B](#), [EDMA_MODULO_16B](#), [EDMA_MODULO_32B](#), [EDMA_MODULO_64B](#), [EDMA_MODULO_128B](#), [EDMA_MODULO_256B](#), [EDMA_MODULO_512B](#), [EDMA_MODULO_1KB](#), [EDMA_MODULO_2KB](#), [EDMA_MODULO_4KB](#), [EDMA_MODULO_8KB](#), [EDMA_MODULO_16KB](#), [EDMA_MODULO_32KB](#), [EDMA_MODULO_64KB](#), [EDMA_MODULO_128KB](#), [EDMA_MODULO_256KB](#), [EDMA_MODULO_512KB](#), [EDMA_MODULO_1MB](#), [EDMA_MODULO_2MB](#), [EDMA_MODULO_4MB](#), [EDMA_MODULO_8MB](#), [EDMA_MODULO_16MB](#), [EDMA_MODULO_32MB](#), [EDMA_MODULO_64MB](#), [EDMA_MODULO_128MB](#), [EDMA_MODULO_256MB](#), [EDMA_MODULO_512MB](#), [EDMA_MODULO_1GB](#), [EDMA_MODULO_2GB](#) }
eDMA modulo configuration Implements : [edma_modulo_t_Class](#)
- enum [edma_transfer_size_t](#) { [EDMA_TRANSFER_SIZE_1B](#) = 0x0U, [EDMA_TRANSFER_SIZE_2B](#) = 0x1U, [EDMA_TRANSFER_SIZE_4B](#) = 0x2U }
eDMA transfer configuration Implements : [edma_transfer_size_t_Class](#)
- enum [edma_chn_status_t](#) { [EDMA_CHN_NORMAL](#) = 0U, [EDMA_CHN_ERROR](#) }
Channel status for eDMA channel.
- enum [edma_transfer_type_t](#) { [EDMA_TRANSFER_PERIPH2MEM](#) = 0U, [EDMA_TRANSFER_MEM2PERIPH](#), [EDMA_TRANSFER_MEM2MEM](#), [EDMA_TRANSFER_PERIPH2PERIPH](#) }
A type for the DMA transfer. Implements : [edma_transfer_type_t_Class](#).

eDMA peripheral driver module level functions

- status_t [EDMA_DRV_Init](#) (edma_state_t *edmaState, const edma_user_config_t *userConfig, edma_chn_state_t *const chnStateArray[], const edma_channel_config_t *const chnConfigArray[], uint32_t chnCount)
Initializes the eDMA module.
- status_t [EDMA_DRV_Deinit](#) (void)
De-initializes the eDMA module.

eDMA peripheral driver channel management functions

- status_t [EDMA_DRV_Channellnit](#) (edma_chn_state_t *edmaChannelState, const edma_channel_config_t *edmaChannelConfig)
Initializes an eDMA channel.
- status_t [EDMA_DRV_ReleaseChannel](#) (uint8_t virtualChannel)
Releases an eDMA channel.

eDMA peripheral driver transfer setup functions

- void [EDMA_DRV_PushConfigToReg](#) (uint8_t virtualChannel, const edma_transfer_config_t *tcd)
Copies the channel configuration to the TCD registers.
- void [EDMA_DRV_PushConfigToSTCD](#) (const edma_transfer_config_t *config, edma_software_tcd_t *stcd)
Copies the channel configuration to the software TCD structure.
- status_t [EDMA_DRV_ConfigSingleBlockTransfer](#) (uint8_t virtualChannel, edma_transfer_type_t type, uint32_t srcAddr, uint32_t destAddr, edma_transfer_size_t transferSize, uint32_t dataBufferSize)
Configures a simple single block data transfer with DMA.
- status_t [EDMA_DRV_ConfigMultiBlockTransfer](#) (uint8_t virtualChannel, edma_transfer_type_t type, uint32_t srcAddr, uint32_t destAddr, edma_transfer_size_t transferSize, uint32_t blockSize, uint32_t blockCount, bool disableReqOnCompletion)
Configures a multiple block data transfer with DMA.
- status_t [EDMA_DRV_ConfigLoopTransfer](#) (uint8_t virtualChannel, const edma_transfer_config_t *transferConfig)
Configures the DMA transfer in loop mode.
- status_t [EDMA_DRV_ConfigScatterGatherTransfer](#) (uint8_t virtualChannel, edma_software_tcd_t *stcd, edma_transfer_size_t transferSize, uint32_t bytesOnEachRequest, const edma_scatter_gather_list_t *srcList, const edma_scatter_gather_list_t *destList, uint8_t tcdCount)
Configures the DMA transfer in a scatter-gather mode.
- void [EDMA_DRV_CancelTransfer](#) (bool error)
Cancel the running transfer.

eDMA Peripheral driver channel operation functions

- status_t [EDMA_DRV_StartChannel](#) (uint8_t virtualChannel)
Starts an eDMA channel.
- status_t [EDMA_DRV_StopChannel](#) (uint8_t virtualChannel)
Stops the eDMA channel.
- status_t [EDMA_DRV_SetChannelRequestAndTrigger](#) (uint8_t virtualChannel, uint8_t request, bool enableTrigger)
Configures the DMA request for the eDMA channel.
- void [EDMA_DRV_ClearTCD](#) (uint8_t virtualChannel)
Clears all registers to 0 for the channel's TCD.
- void [EDMA_DRV_SetSrcAddr](#) (uint8_t virtualChannel, uint32_t address)
Configures the source address for the eDMA channel.

- void [EDMA_DRV_SetSrcOffset](#) (uint8_t virtualChannel, int16_t offset)
Configures the source address signed offset for the eDMA channel.
- void [EDMA_DRV_SetSrcReadChunkSize](#) (uint8_t virtualChannel, [edma_transfer_size_t](#) size)
Configures the source data chunk size (transferred in a read sequence).
- void [EDMA_DRV_SetSrcLastAddrAdjustment](#) (uint8_t virtualChannel, int32_t adjust)
Configures the source address last adjustment.
- void [EDMA_DRV_SetDestAddr](#) (uint8_t virtualChannel, uint32_t address)
Configures the destination address for the eDMA channel.
- void [EDMA_DRV_SetDestOffset](#) (uint8_t virtualChannel, int16_t offset)
Configures the destination address signed offset for the eDMA channel.
- void [EDMA_DRV_SetDestWriteChunkSize](#) (uint8_t virtualChannel, [edma_transfer_size_t](#) size)
Configures the destination data chunk size (transferred in a write sequence).
- void [EDMA_DRV_SetDestLastAddrAdjustment](#) (uint8_t virtualChannel, int32_t adjust)
Configures the destination address last adjustment.
- void [EDMA_DRV_SetMinorLoopBlockSize](#) (uint8_t virtualChannel, uint32_t nbytes)
Configures the number of bytes to be transferred in each service request of the channel.
- void [EDMA_DRV_SetMajorLoopIterationCount](#) (uint8_t virtualChannel, uint32_t majorLoopCount)
Configures the number of major loop iterations.
- uint32_t [EDMA_DRV_GetRemainingMajorIterationsCount](#) (uint8_t virtualChannel)
Returns the remaining major loop iteration count.
- void [EDMA_DRV_SetScatterGatherLink](#) (uint8_t virtualChannel, uint32_t nextTCDAddr)
Configures the memory address of the next TCD, in scatter/gather mode.
- void [EDMA_DRV_DisableRequestsOnTransferComplete](#) (uint8_t virtualChannel, bool disable)
Disables/Enables the DMA request after the major loop completes for the TCD.
- void [EDMA_DRV_ConfigureInterrupt](#) (uint8_t virtualChannel, [edma_channel_interrupt_t](#) intSrc, bool enable)
Disables/Enables the channel interrupt requests.
- void [EDMA_DRV_TriggerSwRequest](#) (uint8_t virtualChannel)
Triggers a sw request for the current channel.

eDMA Peripheral callback and interrupt functions

- status_t [EDMA_DRV_InstallCallback](#) (uint8_t virtualChannel, [edma_callback_t](#) callback, void *parameter)
Registers the callback function and the parameter for eDMA channel.

eDMA Peripheral driver miscellaneous functions

- [edma_chn_status_t](#) [EDMA_DRV_GetChannelStatus](#) (uint8_t virtualChannel)
Gets the eDMA channel status.

17.40.2 Data Structure Documentation

17.40.2.1 struct edma_user_config_t

The user configuration structure for the eDMA driver.

Use an instance of this structure with the [EDMA_DRV_Init\(\)](#) function. This allows the user to configure settings of the EDMA peripheral with a single function call. Implements : [edma_user_config_t_Class](#)

Definition at line 232 of file [edma_driver.h](#).

Data Fields

- [edma_arbitration_algorithm_t](#) chnArbitration
- bool haltOnError

Field Documentation

17.40.2.1.1 `edma_arbitration_algorithm_t` `chnArbitration`

eDMA channel arbitration.

Definition at line 233 of file `edma_driver.h`.

17.40.2.1.2 `bool` `haltOnError`

Any error causes the HALT bit to set. Subsequently, all service requests are ignored until the HALT bit is cleared.

Definition at line 241 of file `edma_driver.h`.

17.40.2.2 `struct edma_chn_state_t`

Data structure for the eDMA channel state. Implements : `edma_chn_state_t_Class`.

Definition at line 268 of file `edma_driver.h`.

Data Fields

- `uint8_t` `virtChn`
- `edma_callback_t` `callback`
- `void *` `parameter`
- `volatile edma_chn_status_t` `status`

Field Documentation

17.40.2.2.1 `edma_callback_t` `callback`

Callback function pointer for the eDMA channel. It will be called at the eDMA channel complete and eDMA channel error.

Definition at line 270 of file `edma_driver.h`.

17.40.2.2.2 `void*` `parameter`

Parameter for the callback function pointer.

Definition at line 273 of file `edma_driver.h`.

17.40.2.2.3 `volatile edma_chn_status_t` `status`

eDMA channel status.

Definition at line 274 of file `edma_driver.h`.

17.40.2.2.4 `uint8_t` `virtChn`

Virtual channel number.

Definition at line 269 of file `edma_driver.h`.

17.40.2.3 `struct edma_channel_config_t`

The user configuration structure for the an eDMA driver channel.

Use an instance of this structure with the `EDMA_DRV_ChannelInit()` function. This allows the user to configure settings of the EDMA channel with a single function call. Implements : `edma_channel_config_t_Class`

Definition at line 284 of file `edma_driver.h`.

Data Fields

- `edma_channel_priority_t` `channelPriority`

- uint8_t [virtChnConfig](#)
- [edma_callback_t](#) callback
- void * [callbackParam](#)
- bool [enableTrigger](#)

Field Documentation

17.40.2.3.1 [edma_callback_t](#) callback

Callback that will be registered for this channel

Definition at line 297 of file [edma_driver.h](#).

17.40.2.3.2 void* [callbackParam](#)

Parameter passed to the channel callback

Definition at line 298 of file [edma_driver.h](#).

17.40.2.3.3 [edma_channel_priority_t](#) channelPriority

eDMA channel priority - only used when channel arbitration mode is 'Fixed priority'.

Definition at line 291 of file [edma_driver.h](#).

17.40.2.3.4 bool [enableTrigger](#)

Enables the periodic trigger capability for the DMA channel.

Definition at line 299 of file [edma_driver.h](#).

17.40.2.3.5 uint8_t [virtChnConfig](#)

eDMA virtual channel number

Definition at line 293 of file [edma_driver.h](#).

17.40.2.4 struct [edma_scatter_gather_list_t](#)

Data structure for configuring a discrete memory transfer. Implements : [edma_scatter_gather_list_t_Class](#).

Definition at line 315 of file [edma_driver.h](#).

Data Fields

- uint32_t [address](#)
- uint32_t [length](#)
- [edma_transfer_type_t](#) type

Field Documentation

17.40.2.4.1 uint32_t [address](#)

Address of buffer.

Definition at line 316 of file [edma_driver.h](#).

17.40.2.4.2 uint32_t [length](#)

Length of buffer.

Definition at line 317 of file [edma_driver.h](#).

17.40.2.4.3 [edma_transfer_type_t](#) type

Type of the DMA transfer

Definition at line 318 of file `edma_driver.h`.

17.40.2.5 struct `edma_state_t`

Runtime state structure for the eDMA driver.

This structure holds data that is used by the eDMA peripheral driver to manage multi eDMA channels. The user passes the memory for this run-time state structure and the eDMA driver populates the members. Implements : `edma_state_t_Class`

Definition at line 330 of file `edma_driver.h`.

Data Fields

- `edma_chn_state_t` *volatile `virtChnState` [(uint32_t) FEATURE_DMA_VIRTUAL_CHANNELS]

Field Documentation

17.40.2.5.1 `edma_chn_state_t`* volatile `virtChnState`[(uint32_t) FEATURE_DMA_VIRTUAL_CHANNELS]

Pointer array storing channel state.

Definition at line 331 of file `edma_driver.h`.

17.40.2.6 struct `edma_loop_transfer_config_t`

eDMA loop transfer configuration.

This structure configures the basic minor/major loop attributes. Implements : `edma_loop_transfer_config_t_Class`

Definition at line 340 of file `edma_driver.h`.

Data Fields

- uint32_t `majorLoopIterationCount`
- bool `srcOffsetEnable`
- bool `dstOffsetEnable`
- int32_t `minorLoopOffset`
- bool `minorLoopChnLinkEnable`
- uint8_t `minorLoopChnLinkNumber`
- bool `majorLoopChnLinkEnable`
- uint8_t `majorLoopChnLinkNumber`

Field Documentation

17.40.2.6.1 bool `dstOffsetEnable`

Selects whether the minor loop offset is applied to the destination address upon minor loop completion.

Definition at line 344 of file `edma_driver.h`.

17.40.2.6.2 bool `majorLoopChnLinkEnable`

Enables channel-to-channel linking on major loop complete.

Definition at line 351 of file `edma_driver.h`.

17.40.2.6.3 uint8_t `majorLoopChnLinkNumber`

The number of the next channel to be started by DMA engine when major loop completes.

Definition at line 352 of file `edma_driver.h`.

17.40.2.6.4 uint32_t majorLoopIterationCount

Number of major loop iterations.

Definition at line 341 of file edma_driver.h.

17.40.2.6.5 bool minorLoopChnLinkEnable

Enables channel-to-channel linking on minor loop complete.

Definition at line 348 of file edma_driver.h.

17.40.2.6.6 uint8_t minorLoopChnLinkNumber

The number of the next channel to be started by DMA engine when minor loop completes.

Definition at line 349 of file edma_driver.h.

17.40.2.6.7 int32_t minorLoopOffset

Sign-extended offset applied to the source or destination address to form the next-state value after the minor loop completes.

Definition at line 346 of file edma_driver.h.

17.40.2.6.8 bool srcOffsetEnable

Selects whether the minor loop offset is applied to the source address upon minor loop completion.

Definition at line 342 of file edma_driver.h.

17.40.2.7 struct edma_transfer_config_t

eDMA transfer size configuration.

This structure configures the basic source/destination transfer attribute. Implements : edma_transfer_config_t ↔ Class

Definition at line 362 of file edma_driver.h.

Data Fields

- uint32_t srcAddr
- uint32_t destAddr
- edma_transfer_size_t srcTransferSize
- edma_transfer_size_t destTransferSize
- int16_t srcOffset
- int16_t destOffset
- int32_t srcLastAddrAdjust
- int32_t destLastAddrAdjust
- edma_modulo_t srcModulo
- edma_modulo_t destModulo
- uint32_t minorByteTransferCount
- bool scatterGatherEnable
- uint32_t scatterGatherNextDescAddr
- bool interruptEnable
- edma_loop_transfer_config_t * loopTransferConfig

Field Documentation

17.40.2.7.1 uint32_t destAddr

Memory address pointing to the destination data.

Definition at line 364 of file edma_driver.h.

17.40.2.7.2 int32_t destLastAddrAdjust

Last destination address adjustment. Note here it is only valid when scatter/gather feature is not enabled.

Definition at line 374 of file edma_driver.h.

17.40.2.7.3 edma_modulo_t destModulo

Destination address modulo.

Definition at line 377 of file edma_driver.h.

17.40.2.7.4 int16_t destOffset

Sign-extended offset applied to the current destination address to form the next-state value as each source read/write is completed.

Definition at line 370 of file edma_driver.h.

17.40.2.7.5 edma_transfer_size_t destTransferSize

Destination data transfer size.

Definition at line 366 of file edma_driver.h.

17.40.2.7.6 bool interruptEnable

Enable the interrupt request when the major loop count completes

Definition at line 385 of file edma_driver.h.

17.40.2.7.7 edma_loop_transfer_config_t* loopTransferConfig

Pointer to loop transfer configuration structure (defines minor/major loop attributes) Note: this field is only used when minor loop mapping is enabled from DMA configuration.

Definition at line 387 of file edma_driver.h.

17.40.2.7.8 uint32_t minorByteTransferCount

Number of bytes to be transferred in each service request of the channel.

Definition at line 378 of file edma_driver.h.

17.40.2.7.9 bool scatterGatherEnable

Enable scatter gather feature.

Definition at line 380 of file edma_driver.h.

17.40.2.7.10 uint32_t scatterGatherNextDescAddr

The address of the next descriptor to be used, when scatter/gather feature is enabled. Note: this value is not used when scatter/gather feature is disabled.

Definition at line 381 of file edma_driver.h.

17.40.2.7.11 uint32_t srcAddr

Memory address pointing to the source data.

Definition at line 363 of file edma_driver.h.

17.40.2.7.12 int32_t srcLastAddrAdjust

Last source address adjustment.

Definition at line 373 of file edma_driver.h.

17.40.2.7.13 edma_modulo_t srcModulo

Source address modulo.

Definition at line 376 of file edma_driver.h.

17.40.2.7.14 int16_t srcOffset

Sign-extended offset applied to the current source address to form the next-state value as each source read/write is completed.

Definition at line 367 of file edma_driver.h.

17.40.2.7.15 edma_transfer_size_t srcTransferSize

Source data transfer size.

Definition at line 365 of file edma_driver.h.

17.40.2.8 struct edma_software_tcd_t

eDMA TCD Implements : edma_software_tcd_t_Class

Definition at line 397 of file edma_driver.h.

Data Fields

- uint32_t [SADDR](#)
- int16_t [SOFF](#)
- uint16_t [ATTR](#)
- uint32_t [NBYTES](#)
- int32_t [SLAST](#)
- uint32_t [DADDR](#)
- int16_t [DOFF](#)
- uint16_t [CITER](#)
- int32_t [DLAST_SGA](#)
- uint16_t [CSR](#)
- uint16_t [BITER](#)

Field Documentation

17.40.2.8.1 uint16_t ATTR

Definition at line 400 of file edma_driver.h.

17.40.2.8.2 uint16_t BITER

Definition at line 408 of file edma_driver.h.

17.40.2.8.3 uint16_t CITER

Definition at line 405 of file edma_driver.h.

17.40.2.8.4 uint16_t CSR

Definition at line 407 of file edma_driver.h.

17.40.2.8.5 uint32_t DADDR

Definition at line 403 of file edma_driver.h.

17.40.2.8.6 int32_t DLAST_SGA

Definition at line 406 of file edma_driver.h.

17.40.2.8.7 int16_t DOFF

Definition at line 404 of file edma_driver.h.

17.40.2.8.8 uint32_t NBYTES

Definition at line 401 of file edma_driver.h.

17.40.2.8.9 uint32_t SADDR

Definition at line 398 of file edma_driver.h.

17.40.2.8.10 int32_t SLAST

Definition at line 402 of file edma_driver.h.

17.40.2.8.11 int16_t SOFF

Definition at line 399 of file edma_driver.h.

17.40.3 Macro Definition Documentation

17.40.3.1 #define EDMA_ERR_LSB_MASK 1U

Macro for accessing the least significant bit of the ERR register.

The erroneous channels are retrieved from ERR register by subsequently right shifting all the ERR bits + "AND"-ing the result with this mask.

Definition at line 65 of file edma_driver.h.

17.40.3.2 #define STCD_ADDR(address) (((uint32_t)address + 31UL) & ~0x1FUL)

Definition at line 57 of file edma_driver.h.

17.40.3.3 #define STCD_SIZE(number) (((number) * 32U) - 1U)

Macro for the memory size needed for the software TCD.

Software TCD is aligned to 32 bytes. We don't need a software TCD structure for the first descriptor, since the configuration is pushed directly to registers. To make sure the software TCD can meet the eDMA module requirement regarding alignment, allocate memory for the remaining descriptors with extra 31 bytes.

Definition at line 56 of file edma_driver.h.

17.40.4 Typedef Documentation

17.40.4.1 typedef void(* edma_callback_t)(void *parameter, edma_chn_status_t status)

Definition for the eDMA channel callback function.

Prototype for the callback function registered in the eDMA driver. Implements : edma_callback_t_Class

Definition at line 263 of file edma_driver.h.

17.40.5 Enumeration Type Documentation

17.40.5.1 enum `edma_arbitration_algorithm_t`

eDMA channel arbitration algorithm used for selection among channels. Implements : `edma_arbitration_algorithm_t_Class`

Enumerator

`EDMA_ARBITRATION_FIXED_PRIORITY` Fixed Priority

`EDMA_ARBITRATION_ROUND_ROBIN` Round-Robin arbitration

Definition at line 79 of file `edma_driver.h`.

17.40.5.2 enum `edma_channel_interrupt_t`

eDMA channel interrupts. Implements : `edma_channel_interrupt_t_Class`

Enumerator

`EDMA_CHN_ERR_INT` Error interrupt

`EDMA_CHN_HALF_MAJOR_LOOP_INT` Half major loop interrupt.

`EDMA_CHN_MAJOR_LOOP_INT` Complete major loop interrupt.

Definition at line 70 of file `edma_driver.h`.

17.40.5.3 enum `edma_channel_priority_t`

eDMA channel priority setting Implements : `edma_channel_priority_t_Class`

Enumerator

`EDMA_CHN_PRIORITY_0`

`EDMA_CHN_PRIORITY_1`

`EDMA_CHN_PRIORITY_2`

`EDMA_CHN_PRIORITY_3`

`EDMA_CHN_PRIORITY_4`

`EDMA_CHN_PRIORITY_5`

`EDMA_CHN_PRIORITY_6`

`EDMA_CHN_PRIORITY_7`

`EDMA_CHN_PRIORITY_8`

`EDMA_CHN_PRIORITY_9`

`EDMA_CHN_PRIORITY_10`

`EDMA_CHN_PRIORITY_11`

`EDMA_CHN_PRIORITY_12`

`EDMA_CHN_PRIORITY_13`

`EDMA_CHN_PRIORITY_14`

`EDMA_CHN_PRIORITY_15`

`EDMA_CHN_DEFAULT_PRIORITY`

Definition at line 87 of file `edma_driver.h`.

17.40.5.4 enum edma_chn_status_t

Channel status for eDMA channel.

A structure describing the eDMA channel status. The user can get the status by callback parameter or by calling EDMA_DRV_getStatus() function. Implements : edma_chn_status_t_Class

Enumerator

EDMA_CHN_NORMAL eDMA channel normal state.

EDMA_CHN_ERROR An error occurred in the eDMA channel.

Definition at line 252 of file edma_driver.h.

17.40.5.5 enum edma_modulo_t

eDMA modulo configuration Implements : edma_modulo_t_Class

Enumerator

EDMA_MODULO_OFF

EDMA_MODULO_2B

EDMA_MODULO_4B

EDMA_MODULO_8B

EDMA_MODULO_16B

EDMA_MODULO_32B

EDMA_MODULO_64B

EDMA_MODULO_128B

EDMA_MODULO_256B

EDMA_MODULO_512B

EDMA_MODULO_1KB

EDMA_MODULO_2KB

EDMA_MODULO_4KB

EDMA_MODULO_8KB

EDMA_MODULO_16KB

EDMA_MODULO_32KB

EDMA_MODULO_64KB

EDMA_MODULO_128KB

EDMA_MODULO_256KB

EDMA_MODULO_512KB

EDMA_MODULO_1MB

EDMA_MODULO_2MB

EDMA_MODULO_4MB

EDMA_MODULO_8MB

EDMA_MODULO_16MB

EDMA_MODULO_32MB

EDMA_MODULO_64MB

EDMA_MODULO_128MB

EDMA_MODULO_256MB

EDMA_MODULO_512MB

EDMA_MODULO_1GB

EDMA_MODULO_2GB

Definition at line 159 of file edma_driver.h.

17.40.5.6 enum `edma_transfer_size_t`

eDMA transfer configuration Implements : `edma_transfer_size_t_Class`

Enumerator

`EDMA_TRANSFER_SIZE_1B`

`EDMA_TRANSFER_SIZE_2B`

`EDMA_TRANSFER_SIZE_4B`

Definition at line 197 of file `edma_driver.h`.

17.40.5.7 enum `edma_transfer_type_t`

A type for the DMA transfer. Implements : `edma_transfer_type_t_Class`.

Enumerator

`EDMA_TRANSFER_PERIPH2MEM` Transfer from peripheral to memory

`EDMA_TRANSFER_MEM2PERIPH` Transfer from memory to peripheral

`EDMA_TRANSFER_MEM2MEM` Transfer from memory to memory

`EDMA_TRANSFER_PERIPH2PERIPH` Transfer from peripheral to peripheral

Definition at line 305 of file `edma_driver.h`.

17.40.6 Function Documentation

17.40.6.1 void `EDMA_DRV_CancelTransfer (bool error)`

Cancel the running transfer.

This function cancels the current transfer, optionally signalling an error.

Parameters

<i>bool</i>	error If true, an error will be logged for the current transfer.
-------------	--

Definition at line 1487 of file `edma_driver.c`.

17.40.6.2 status_t `EDMA_DRV_Channellnit (edma_chn_state_t * edmaChannelState, const edma_channel_config_t * edmaChannelConfig)`

Initializes an eDMA channel.

This function initializes the run-time state structure for a eDMA channel, based on user configuration. It will request the channel, set up the channel priority and install the callback.

Parameters

<i>edmaChannelState</i>	Pointer to the eDMA channel state structure. The user passes the memory for this run-time state structure and the eDMA peripheral driver populates the members. This run-time state structure keeps track of the eDMA channel status. The memory must be kept valid before calling the <code>EDMA_DRV_ReleaseChannel</code> .
-------------------------	---

<i>edmaChannel</i> ↔ <i>Config</i>	User configuration structure for eDMA channel. The user populates the members of this structure and passes the pointer of this structure into the function.
---------------------------------------	---

Returns

STATUS_ERROR or STATUS_SUCCESS.

Definition at line 287 of file edma_driver.c.

17.40.6.3 void EDMA_DRV_ClearTCD (uint8_t *virtualChannel*)

Clears all registers to 0 for the channel's TCD.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
-----------------------	------------------------------

Definition at line 1019 of file edma_driver.c.

17.40.6.4 status_t EDMA_DRV_ConfigLoopTransfer (uint8_t *virtualChannel*, const edma_transfer_config_t * *transferConfig*)

Configures the DMA transfer in loop mode.

This function configures the DMA transfer in a loop chain. The user passes a block of memory into this function that configures the loop transfer properties (minor/major loop count, address offsets, channel linking). The DMA driver copies the configuration to TCD registers, only when the loop properties are set up correctly and minor loop mapping is enabled for the eDMA module.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>transferConfig</i>	Pointer to the transfer configuration structure; this structure defines fields for setting up the basic transfer and also a pointer to a memory structure that defines the loop chain properties (minor/major).

Returns

STATUS_ERROR or STATUS_SUCCESS

Definition at line 689 of file edma_driver.c.

17.40.6.5 status_t EDMA_DRV_ConfigMultiBlockTransfer (uint8_t *virtualChannel*, edma_transfer_type_t *type*, uint32_t *srcAddr*, uint32_t *destAddr*, edma_transfer_size_t *transferSize*, uint32_t *blockSize*, uint32_t *blockCount*, bool *disableReqOnCompletion*)

Configures a multiple block data transfer with DMA.

This function configures the descriptor for a multi-block transfer. The function considers contiguous memory blocks, thus it configures the TCD source/destination offset fields to cover the data buffer without gaps, according to "transferSize" parameter (the offset is equal to the number of bytes transferred in a source read/destination write). The buffer is divided in multiple block, each block being transferred upon a single DMA request.

NOTE: For transfers to/from peripherals, make sure the transfer size is equal to the data buffer size of the peripheral used, otherwise only truncated chunks of data may be transferred (e.g. for a communication IP with an 8-bit data register the transfer size should be 1B, whereas for a 32-bit data register, the transfer size should be 4B). The rationale of this constraint is that, on the peripheral side, the address offset is set to zero, allowing to read/write data from/to the peripheral in a single source read/destination write operation.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>type</i>	Transfer type (M->M, P->M, M->P, P->P).
<i>srcAddr</i>	A source register address or a source memory address.
<i>destAddr</i>	A destination register address or a destination memory address.
<i>transferSize</i>	The number of bytes to be transferred on every DMA write/read. Source/Dest share the same write/read size.
<i>blockSize</i>	The total number of bytes inside a block.
<i>blockCount</i>	The total number of data blocks (one block is transferred upon a DMA request).
<i>disableReqOnCompletion</i>	This parameter specifies whether the DMA channel should be disabled when the transfer is complete (further requests will remain untreated).

Returns

STATUS_ERROR or STATUS_SUCCESS

Definition at line 629 of file edma_driver.c.

17.40.6.6 `status_t EDMA_DRV_ConfigScatterGatherTransfer (uint8_t virtualChannel, edma_software_tcd_t * stcd, edma_transfer_size_t transferSize, uint32_t bytesOnEachRequest, const edma_scatter_gather_list_t * srcList, const edma_scatter_gather_list_t * destList, uint8_t tcdCount)`

Configures the DMA transfer in a scatter-gather mode.

This function configures the descriptors into a single-ended chain. The user passes blocks of memory into this function. The interrupt is triggered only when the last memory block is completed. The memory block information is passed with the `edma_scatter_gather_list_t` data structure, which can tell the memory address and length. The DMA driver configures the descriptor for each memory block, transfers the descriptor from the first one to the last one, and stops.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>stcd</i>	Array of empty software TCD structures. The user must prepare this memory block. We don't need a software TCD structure for the first descriptor, since the configuration is pushed directly to registers. The "stcd" buffer must align with 32 bytes; if not, an error occurs in the eDMA driver. Thus, the required memory size for "stcd" is equal to <code>tcdCount * size_of(edma_software_tcd_t) - 1</code> ; the driver will take care of the memory alignment if the provided memory buffer is big enough. For proper allocation of the "stcd" buffer it is recommended to use <code>STCD_SIZE</code> macro.
<i>transferSize</i>	The number of bytes to be transferred on every DMA write/read.
<i>bytesOnEachRequest</i>	Bytes to be transferred in each DMA request.
<i>srcList</i>	Data structure storing the address, length and type of transfer (M->M, M->P, P->M, P->P) for the bytes to be transferred for source memory blocks. If the source memory is peripheral, the length is not used.
<i>destList</i>	Data structure storing the address, length and type of transfer (M->M, M->P, P->M, P->P) for the bytes to be transferred for destination memory blocks. In the memory-to-memory transfer mode, the user must ensure that the length of the destination scatter gather list is equal to the source scatter gather list. If the destination memory is a peripheral register, the length is not used.

<i>tcdCount</i>	The number of TCD memory blocks contained in the scatter gather list.
-----------------	---

Returns

STATUS_ERROR or STATUS_SUCCESS

Definition at line 759 of file edma_driver.c.

17.40.6.7 `status_t EDMA_DRV_ConfigSingleBlockTransfer (uint8_t virtualChannel, edma_transfer_type_t type, uint32_t srcAddr, uint32_t destAddr, edma_transfer_size_t transferSize, uint32_t dataBufferSize)`

Configures a simple single block data transfer with DMA.

This function configures the descriptor for a single block transfer. The function considers contiguous memory blocks, thus it configures the TCD source/destination offset fields to cover the data buffer without gaps, according to "transferSize" parameter (the offset is equal to the number of bytes transferred in a source read/destination write).

NOTE: For memory-to-peripheral or peripheral-to-memory transfers, make sure the transfer size is equal to the data buffer size of the peripheral used, otherwise only truncated chunks of data may be transferred (e.g. for a communication IP with an 8-bit data register the transfer size should be 1B, whereas for a 32-bit data register, the transfer size should be 4B). The rationale of this constraint is that, on the peripheral side, the address offset is set to zero, allowing to read/write data from/to the peripheral in a single source read/destination write operation.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>type</i>	Transfer type (M->M, P->M, M->P, P->P).
<i>srcAddr</i>	A source register address or a source memory address.
<i>destAddr</i>	A destination register address or a destination memory address.
<i>transferSize</i>	The number of bytes to be transferred on every DMA write/read. Source/Dest share the same write/read size.
<i>dataBufferSize</i>	The total number of bytes to be transferred.

Returns

STATUS_ERROR or STATUS_SUCCESS

Definition at line 509 of file edma_driver.c.

17.40.6.8 `void EDMA_DRV_ConfigureInterrupt (uint8_t virtualChannel, edma_channel_interrupt_t intSrc, bool enable)`

Disables/Enables the channel interrupt requests.

This function enables/disables error, half major loop and complete major loop interrupts for the current channel.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>interrupt</i>	Interrupt event (error/half major loop/complete major loop).
<i>enable</i>	Enable (true)/Disable (false) interrupts for the current channel.

Definition at line 1439 of file edma_driver.c.

17.40.6.9 `status_t EDMA_DRV_Deinit (void)`

De-initializes the eDMA module.

This function resets the eDMA module to reset state and disables the interrupt to the core.

Returns

STATUS_ERROR or STATUS_SUCCESS.

Definition at line 239 of file edma_driver.c.

17.40.6.10 void EDMA_DRV_DisableRequestsOnTransferComplete (uint8_t *virtualChannel*, bool *disable*)

Disables/Enables the DMA request after the major loop completes for the TCD.

If disabled, the eDMA hardware automatically clears the corresponding DMA request when the current major iteration count reaches zero.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>disable</i>	Disable (true)/Enable (false) DMA request after TCD complete.

Definition at line 1409 of file edma_driver.c.

17.40.6.11 edma_chn_status_t EDMA_DRV_GetChannelStatus (uint8_t *virtualChannel*)

Gets the eDMA channel status.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
-----------------------	------------------------------

Returns

Channel status.

Definition at line 1711 of file edma_driver.c.

17.40.6.12 uint32_t EDMA_DRV_GetRemainingMajorIterationsCount (uint8_t *virtualChannel*)

Returns the remaining major loop iteration count.

Gets the number minor loops yet to be triggered (major loop iterations).

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
-----------------------	------------------------------

Returns

number of major loop iterations yet to be triggered

Definition at line 1348 of file edma_driver.c.

17.40.6.13 status_t EDMA_DRV_Init (edma_state_t * *edmaState*, const edma_user_config_t * *userConfig*, edma_chn_state_t *const *chnStateArray*[], const edma_channel_config_t *const *chnConfigArray*[], uint32_t *chnCount*)

Initializes the eDMA module.

This function initializes the run-time state structure to provide the eDMA channel allocation release, protect, and track the state for channels. This function also resets the eDMA modules, initializes the module to user-defined settings and default settings.

Parameters

<i>edmaState</i>	The pointer to the eDMA peripheral driver state structure. The user passes the memory for this run-time state structure and the eDMA peripheral driver populates the members. This run-time state structure keeps track of the eDMA channels status. The memory must be kept valid before calling the EDMA_DRV_DeInit.
------------------	--

<i>userConfig</i>	User configuration structure for eDMA peripheral drivers. The user populates the members of this structure and passes the pointer of this structure into the function.
<i>chnStateArray</i>	Array of pointers to run-time state structures for eDMA channels; will populate the state structures inside the eDMA driver state structure.
<i>chnConfigArray</i>	Array of pointers to channel initialization structures.
<i>chnCount</i>	The number of eDMA channels to be initialized.

Returns

STATUS_ERROR or STATUS_SUCCESS.

Definition at line 123 of file edma_driver.c.

17.40.6.14 `status_t EDMA_DRV_InstallCallback (uint8_t virtualChannel, edma_callback_t callback, void * parameter)`

Registers the callback function and the parameter for eDMA channel.

This function registers the callback function and the parameter into the eDMA channel state structure. The callback function is called when the channel is complete or a channel error occurs. The eDMA driver passes the channel status to this callback function to indicate whether it is caused by the channel complete event or the channel error event.

To un-register the callback function, set the callback function to "NULL" and call this function.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>callback</i>	The pointer to the callback function.
<i>parameter</i>	The pointer to the callback function's parameter.

Returns

STATUS_ERROR or STATUS_SUCCESS.

Definition at line 365 of file edma_driver.c.

17.40.6.15 `void EDMA_DRV_PushConfigToReg (uint8_t virtualChannel, const edma_transfer_config_t * tcd)`

Copies the channel configuration to the TCD registers.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>tcd</i>	Pointer to the channel configuration structure.

Definition at line 1589 of file edma_driver.c.

17.40.6.16 `void EDMA_DRV_PushConfigToSTCD (const edma_transfer_config_t * config, edma_software_tcd_t * stcd)`

Copies the channel configuration to the software TCD structure.

This function copies the properties from the channel configuration to the software TCD structure; the address of the software TCD can be used to enable scatter/gather operation (pointer to the next TCD).

Parameters

<i>config</i>	Pointer to the channel configuration structure.
---------------	---

<i>stcd</i>	Pointer to the software TCD structure.
-------------	--

Definition at line 1545 of file edma_driver.c.

17.40.6.17 `status_t EDMA_DRV_ReleaseChannel (uint8_t virtualChannel)`

Releases an eDMA channel.

This function stops the eDMA channel and disables the interrupt of this channel. The channel state structure can be released after this function is called.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
-----------------------	------------------------------

Returns

STATUS_ERROR or STATUS_SUCCESS.

Definition at line 391 of file edma_driver.c.

17.40.6.18 `status_t EDMA_DRV_SetChannelRequestAndTrigger (uint8_t virtualChannel, uint8_t request, bool enableTrigger)`

Configures the DMA request for the eDMA channel.

Selects which DMA source is routed to a DMA channel. The DMA sources are defined in the file <MCU>_↔ Features.h Configures the periodic trigger capability for the triggered DMA channel.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>request</i>	DMA request source.
<i>enableTrigger</i>	DMA channel periodic trigger.

Returns

STATUS_SUCCESS or STATUS_UNSUPPORTED.

Definition at line 970 of file edma_driver.c.

17.40.6.19 `void EDMA_DRV_SetDestAddr (uint8_t virtualChannel, uint32_t address)`

Configures the destination address for the eDMA channel.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>address</i>	The pointer to the destination memory address.

Definition at line 1198 of file edma_driver.c.

17.40.6.20 `void EDMA_DRV_SetDestLastAddrAdjustment (uint8_t virtualChannel, int32_t adjust)`

Configures the destination address last adjustment.

Adjustment value added to the destination address at the completion of the major iteration count. This value can be applied to restore the destination address to the initial value, or adjust the address to reference the next data structure.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>adjust</i>	Adjustment value.

Definition at line 1168 of file edma_driver.c.

17.40.6.21 void EDMA_DRV_SetDestOffset (uint8_t *virtualChannel*, int16_t *offset*)

Configures the destination address signed offset for the eDMA channel.

Sign-extended offset applied to the current destination address to form the next-state value as each destination write is complete.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>offset</i>	signed-offset

Definition at line 1228 of file edma_driver.c.

17.40.6.22 void EDMA_DRV_SetDestWriteChunkSize (uint8_t *virtualChannel*, edma_transfer_size_t *size*)

Configures the destination data chunk size (transferred in a write sequence).

Destination data write transfer size (1/2/4/16/32 bytes).

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>size</i>	Destination transfer size.

Definition at line 1258 of file edma_driver.c.

17.40.6.23 void EDMA_DRV_SetMajorLoopIterationCount (uint8_t *virtualChannel*, uint32_t *majorLoopCount*)

Configures the number of major loop iterations.

Sets the number of major loop iterations; each major loop iteration will be served upon a request for the current channel, transferring the data block configured for the minor loop (NBYTES).

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>majorLoopCount</i>	Number of major loop iterations.

Definition at line 1318 of file edma_driver.c.

17.40.6.24 void EDMA_DRV_SetMinorLoopBlockSize (uint8_t *virtualChannel*, uint32_t *nbytes*)

Configures the number of bytes to be transferred in each service request of the channel.

Sets the number of bytes to be transferred each time a request is received (one major loop iteration). This number needs to be a multiple of the source/destination transfer size, as the data block will be transferred within multiple read/write sequences (minor loops).

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>nbytes</i>	Number of bytes to be transferred in each service request of the channel

Definition at line 1288 of file edma_driver.c.

17.40.6.25 void EDMA_DRV_SetScatterGatherLink (uint8_t *virtualChannel*, uint32_t *nextTCDAddr*)

Configures the memory address of the next TCD, in scatter/gather mode.

This function configures the address of the next TCD to be loaded from memory, when scatter/gather feature is enabled. This address points to the beginning of a 0-modulo-32 byte region containing the next transfer TCD to be

loaded into this channel. The channel reload is performed as the major iteration count completes. The scatter/gather address must be 0-modulo-32-byte. Otherwise, a configuration error is reported.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>nextTCDAddr</i>	The address of the next TCD to be linked to this TCD.

Definition at line 1379 of file edma_driver.c.

17.40.6.26 void EDMA_DRV_SetSrcAddr (uint8_t *virtualChannel*, uint32_t *address*)

Configures the source address for the eDMA channel.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>address</i>	The pointer to the source memory address.

Definition at line 1048 of file edma_driver.c.

17.40.6.27 void EDMA_DRV_SetSrcLastAddrAdjustment (uint8_t *virtualChannel*, int32_t *adjust*)

Configures the source address last adjustment.

Adjustment value added to the source address at the completion of the major iteration count. This value can be applied to restore the source address to the initial value, or adjust the address to reference the next data structure.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>adjust</i>	Adjustment value.

Definition at line 1138 of file edma_driver.c.

17.40.6.28 void EDMA_DRV_SetSrcOffset (uint8_t *virtualChannel*, int16_t *offset*)

Configures the source address signed offset for the eDMA channel.

Sign-extended offset applied to the current source address to form the next-state value as each source read is complete.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>offset</i>	Signed-offset for source address.

Definition at line 1078 of file edma_driver.c.

17.40.6.29 void EDMA_DRV_SetSrcReadChunkSize (uint8_t *virtualChannel*, edma_transfer_size_t *size*)

Configures the source data chunk size (transferred in a read sequence).

Source data read transfer size (1/2/4/16/32 bytes).

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
<i>size</i>	Source transfer size.

Definition at line 1108 of file edma_driver.c.

17.40.6.30 status_t EDMA_DRV_StartChannel (uint8_t *virtualChannel*)

Starts an eDMA channel.

This function enables the eDMA channel DMA request.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
-----------------------	------------------------------

Returns

STATUS_ERROR or STATUS_SUCCESS.

Definition at line 907 of file edma_driver.c.

17.40.6.31 `status_t EDMA_DRV_StopChannel (uint8_t virtualChannel)`

Stops the eDMA channel.

This function disables the eDMA channel DMA request.

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
-----------------------	------------------------------

Returns

STATUS_ERROR or STATUS_SUCCESS.

Definition at line 938 of file edma_driver.c.

17.40.6.32 `void EDMA_DRV_TriggerSwRequest (uint8_t virtualChannel)`

Triggers a sw request for the current channel.

This function starts a transfer using the current channel (sw request).

Parameters

<i>virtualChannel</i>	eDMA virtual channel number.
-----------------------	------------------------------

Definition at line 1516 of file edma_driver.c.

17.41 EIM Driver

17.41.1 Detailed Description

Error Injection Module Peripheral Driver.

EIM PD provides a set of high-level APIs/services to configure the Error Injection Module (EIM) module.

Important Note:

1. Make sure that STACK memory is located in RAM different than where EIM will inject a non-correctable error.
2. For single bit error generation, flip only one bit out of DATA_MASK or CHKBIT_MASK bit-fields in EIM control registers.
3. For Double bit error generation, flip only two bits out of DATA_MASK or CHKBIT_MASK bit-fields in EIM control registers.
4. If more than 2 bits are flipped that there is no guarantee in design that what type of error get generated.
5. When generating double bit error or more than 2 bits error:
 - S32K11x: After injecting the error, the program jumps to HardFault_Handler(). User needs to cancel the HardFault_Handler() by disabling the EIM module inside the HardFault_Handler() function. Example shown below: HardFault_Handler() { EIM_DRV_Deinit(INST_EIM1); }
 - S32Rx7x An uncorrectable ECC error occurs on an access generated by the DMA only. If a CPU access to the TCD causes an uncorrectable ECC error, that access will receive a bus error response.
6. When using double bit error generation on S32K11x, user needs to define one region called ram_low then move the stack and m_interrupts to that region, otherwise the module can't be enabled because the RAM ECC mechanism can only correct one single error.

Basic Operations of EIM

1. To initialize EIM, call [EIM_DRV_Init\(\)](#) with an user channel configuration array. In the following code, EIM is initialized with default settings (after reset) for check-bit mask and data mask and both channels is enabled.

```

1.1 With instance S32K14x
#define INST_EIM1 (0U)

#define EIM_CHANNEL_COUNT0 (2U)
/* Configuration structure array */
eim_user_channel_config_t userChannelConfigArr[] =
{
    /* Configuration channel 0 */
    {
        .channel = 0x0U,
        .checkBitMask = 0x00U,
        .dataMask = 0x00U,
        .enable = true
    },
    /* Configuration channel 1 */
    {
        .channel = 0x1U,
        .checkBitMask = 0x00U,
        .dataMask = 0x00U,
        .enable = true
    }
};
1.2 With instance S32K11x

```

```

#define INST_EIM1 (0U)

#define EIM_CHANNEL_COUNT0 (1U)
/* Configuration structure array */
eim_user_channel_config_t userChannelConfigArr[] =
{
    /* Configuration channel 0 */
    {
        .channel = 0x0U,
        .checkBitMask = 0x01U,
        .dataMask = 0x00U,
        .enable = true
    },
};
1.3 With instance S32Rx7x
#define INST_EIM1 (0U)

#define EIM_CHANNEL_COUNT0 (1U)
/* Configuration structure array */
eim_user_channel_config_t userChannelConfigArr[] =
{
    /* Configuration channel 0 */
    {
        .channel = 0x0U,
        .checkBitMask = 0x01U,
        .dataMask = 0x00U,
        .dataMask1= 0x00U,
        .enable = true
    },
};
/* Initialize the EIM instance 0 with configured channel number of 2 and userChannelConfigArr */
EIM_DRV_Init(INST_EIM1, EIM_CHANNEL_COUNT0 , userChannelConfigArr);

```

2. To get the default configuration (data mask, check-bit mask and enable status) of a channel in EIM, just call [EIM_DRV_GetDefaultConfig\(\)](#). Make sure that the operation is not execute in target RAM where EIM inject the error

```

eim_user_channel_config_t channelConfig;

/* Get default configuration of EIM channel 1*/
EIM_DRV_GetDefaultConfig(1U, &channelConfig);

```

3. To de-initialize EIM, just call the [EIM_DRV_Deinit\(\)](#) function. This function sets all registers to reset values and disables EIM.

```

/* De-initializes the EIM module */
EIM_DRV_Deinit(INST_EIM1);

```

Data Structures

- struct [eim_user_channel_config_t](#)
EIM channel configuration structure. [More...](#)

Macros

- #define [EIM_CHECKBITMASK_DEFAULT](#) (0x01U)
The value default of EIM check-bit mask.
- #define [EIM_DATAMASK_DEFAULT](#) (0x00U)
The value default of EIM data mask.

EIM Driver API

- void [EIM_DRV_Init](#) (uint32_t instance, uint8_t channelCnt, const [eim_user_channel_config_t](#) *channelConfigArr)
Initializes the EIM module.

- void `EIM_DRV_Deinit` (uint32_t instance)
De-initializes the EIM module.
- void `EIM_DRV_ConfigChannel` (uint32_t instance, const `eim_user_channel_config_t` *userChannelConfig)
Configures the EIM channel.
- void `EIM_DRV_GetChannelConfig` (uint32_t instance, uint8_t channel, `eim_user_channel_config_t` *channelConfig)
Gets the EIM channel configuration.
- void `EIM_DRV_GetDefaultConfig` (uint8_t channel, `eim_user_channel_config_t` *channelConfig)
Gets the EIM channel configuration default.

17.41.2 Data Structure Documentation

17.41.2.1 struct `eim_user_channel_config_t`

EIM channel configuration structure.

This structure holds the configuration settings for the EIM channel Implements : `eim_user_channel_config_t_Class`
Definition at line 55 of file `eim_driver.h`.

Data Fields

- uint8_t `channel`
- uint8_t `checkBitMask`
- uint32_t `dataMask`
- bool `enable`

Field Documentation

17.41.2.1.1 uint8_t channel

EIM channel number

Definition at line 57 of file `eim_driver.h`.

17.41.2.1.2 uint8_t checkBitMask

Specifies whether the corresponding bit of the check-bit bus from the target RAM should be inverted or remain unmodified

Definition at line 58 of file `eim_driver.h`.

17.41.2.1.3 uint32_t dataMask

Specifies whether the corresponding bit of the read data bus from the target RAM should be inverted or remain unmodified

Definition at line 60 of file `eim_driver.h`.

17.41.2.1.4 bool enable

true : EIM channel operation is enabled false : EIM channel operation is disabled

Definition at line 66 of file `eim_driver.h`.

17.41.3 Macro Definition Documentation

17.41.3.1 #define `EIM_CHECKBITMASK_DEFAULT` (0x01U)

The value default of EIM check-bit mask.

Definition at line 45 of file `eim_driver.h`.

17.41.3.2 #define EIM_DATAMASK_DEFAULT (0x00U)

The value default of EIM data mask.

Definition at line 47 of file eim_driver.h.

17.41.4 Function Documentation

17.41.4.1 void EIM_DRV_ConfigChannel (uint32_t instance, const eim_user_channel_config_t * userChannelConfig)

Configures the EIM channel.

This function configures check-bit mask, data mask and operation status(enable/disable) for EIM channel. The EIM channel configuration structure shall be passed as arguments.

This is an example demonstrating how to define a EIM channel configuration structure:

```
1 eim_user_channel_config_t eimTestInit = {
2     .channel = 0x1U,
3     .checkBitMask = 0x25U,
4     .dataMask = 0x11101100U,
5     .enable = true
6 };
```

Parameters

in	<i>instance</i>	EIM module instance number
in	<i>userChannelConfig</i>	Pointer to EIM channel configuration structure

Definition at line 115 of file eim_driver.c.

17.41.4.2 void EIM_DRV_Deinit (uint32_t instance)

De-initializes the EIM module.

This function sets all registers to reset value and disables EIM module. In order to use the EIM module again, EIM_DRV_Init must be called.

Parameters

in	<i>instance</i>	EIM module instance number
----	-----------------	----------------------------

Definition at line 92 of file eim_driver.c.

17.41.4.3 void EIM_DRV_GetChannelConfig (uint32_t instance, uint8_t channel, eim_user_channel_config_t * channelConfig)

Gets the EIM channel configuration.

This function gets check bit mask, data mask and operation status of EIM channel.

Parameters

in	<i>instance</i>	EIM module instance number
in	<i>channel</i>	EIM channel number
out	<i>channelConfig</i>	Pointer to EIM channel configuration structure

Definition at line 145 of file eim_driver.c.

17.41.4.4 void EIM_DRV_GetDefaultConfig (uint8_t channel, eim_user_channel_config_t * channelConfig)

Gets the EIM channel configuration default.

This function gets check bit mask, data mask and operation status default of EIM channel.

Parameters

in	<i>channel</i>	EIM channel number
out	<i>channelConfig</i>	Pointer to EIM channel configuration structure default

Definition at line 176 of file eim_driver.c.

17.41.4.5 void EIM_DRV_Init (uint32_t *instance*, uint8_t *channelCnt*, const eim_user_channel_config_t * *channelConfigArr*)

Initializes the EIM module.

This function configures for EIM channels. The EIM channel configuration structure array and number of configured channels shall be passed as arguments. This function should be called before calling any other EIM driver function.

This is an example demonstrating how to define a EIM channel configuration structure array:

```

1 eim_user_channel_config_t channelConfigArr[] =
2 {
3 {
4 .channel = 0x0U,
5 .checkBitMask = 0x12U,
6 .dataMask = 0x01234567U,
7 .enable = true
8 },
9 {
10 .channel = 0x1U,
11 .checkBitMask = 0x22U,
12 .dataMask = 0x01234444U,
13 .enable = false
14 }
15 };

```

Parameters

in	<i>instance</i>	EIM module instance number.
in	<i>channelCnt</i>	Number of configured channels
in	<i>channelConfigArr</i>	EIM channel configuration structure array

Definition at line 62 of file eim_driver.c.

17.42 ENET Driver

17.42.1 Detailed Description

How to use the ENET driver in your application

In order to use the ENET driver in your application, the [ENET_DRV_Init\(\)](#) function should be called prior to using the rest of the API. The parameters of this function specify:

- the ENET instance to be initialized
- a structure which will hold the internal state of the driver
- a structure specifying the configuration of the ENET module
- an array of structures specifying the configuration of the buffers (one structure for each pair of Rx and Tx rings)
- the MAC address to be configured for the module

The configuration of the module is specified through the [enet_config_t](#) structure and contains:

- MII-related configurations (mode, speed, duplex)
- acceleration options for the receive and transmit path
- the maximum frame length
- the MAC interrupt sources which should be enabled
- other special configurations of the receive and transmit path
- a callback function to be invoked on events
- the number of Rx and Tx pairs of rings used by the driver

The buffers configuration is specified through the [enet_buffer_config_t](#) structure and contains:

- the size of the Rx and Tx rings
- pointers to the beginning of the Rx and Tx buffer descriptors rings (should be 64-bit aligned)
- pointer to the beginning of the memory area where the received data shall be saved (should be 64-bit aligned)

In order to de-initialize the driver, the [ENET_DRV_Deinit\(\)](#) function shall be used. This function will disable the ENET interrupts and the module, so calling other ENET driver functions after de-initializing the driver will have undefined behavior. In order to use the driver again, [ENET_DRV_Init\(\)](#) should be called.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\enet\enet_driver.c  
${S32SDK_PATH}\platform\drivers\src\enet\enet_irq.c  
${S32SDK_PATH}\platform\drivers\src\enet\enet_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager Interrupt Manager \(Interrupt\) OS Interface \(OSIF\)](#)

Examples:

Initializing the module

```
#define INST_ETHERNET1 (0U)

#define ENET_RXBD_NUM0_0 (5U)

#define ENET_TXBD_NUM0_0 (5U)

#define ENET_RXBD_NUM0_1 (3U)

#define ENET_TXBD_NUM0_1 (4U)

enet_state_t ethernet1_State;

uint8_t ethernet1_MacAddr[6] = {0x11, 0x22, 0x33, 0x44, 0x55, 0x66};

enet_config_t ethernet1_InitConfig0 =
{
    .interrupts = ENET_RX_FRAME_INTERRUPT,
    .maxFrameLen = 1518U,
    .miiMode = ENET_MII_MODE,
    .miiSpeed = ENET_MII_SPEED_100M,
    .miiDuplex = ENET_MII_FULL_DUPLEX,
    .rxAccelerConfig = 0,
    .txAccelerConfig = ENET_TX_ACCEL_INSERT_IP_CHECKSUM | ENET_TX_ACCEL_INSERT_PROTO_CHECKSUM,
    .rxConfig = 0,
    .txConfig = ENET_TX_CONFIG_ENABLE_MAC_ADDR_INSERTION,
    .ringCount = 2,
    .callback = rx_callback
};

ALIGNED(FEATURE_ENET_BUFFDESCR_ALIGNMENT) enet_buffer_descriptor_t
    ethernet1_rxBuffDescrip0_0[ENET_RXBD_NUM0_0];
ALIGNED(FEATURE_ENET_BUFFDESCR_ALIGNMENT) enet_buffer_descriptor_t
    ethernet1_txBuffDescrip0_0[ENET_TXBD_NUM0_0];
ALIGNED(FEATURE_ENET_BUFFDESCR_ALIGNMENT) enet_buffer_descriptor_t
    ethernet1_rxBuffDescrip0_1[ENET_RXBD_NUM0_1];
ALIGNED(FEATURE_ENET_BUFFDESCR_ALIGNMENT) enet_buffer_descriptor_t
    ethernet1_txBuffDescrip0_1[ENET_TXBD_NUM0_1];

ALIGNED(FEATURE_ENET_BUFF_ALIGNMENT) uint8_t ethernet1_rxDataBuff0_0[ENET_RXBD_NUM0_0 *
    ENET_BUFF_ALIGN(1518U)];
ALIGNED(FEATURE_ENET_BUFF_ALIGNMENT) uint8_t ethernet1_rxDataBuff0_1[ENET_RXBD_NUM0_1 *
    ENET_BUFF_ALIGN(1518U)];

const enet_buffer_config_t ethernet1_buffConfigArr0[] = {
    {
        ENET_RXBD_NUM0_0,
        ENET_TXBD_NUM0_0,
        &ethernet1_rxBuffDescrip0_0[0],
        &ethernet1_txBuffDescrip0_0[0],
        &ethernet1_rxDataBuff0_0[0]
    },
    {
        ENET_RXBD_NUM0_1,
        ENET_TXBD_NUM0_1,
        &ethernet1_rxBuffDescrip0_1[0],
        &ethernet1_txBuffDescrip0_1[0],
        &ethernet1_rxDataBuff0_1[0]
    }
};

ENET_DRV_Init(INST_ETHERNET1, &ethernet1_State, &ethernet1_InitConfig0,
    ethernet1_buffConfigArr0, ethernet1_MacAddr);

/* ... */

ENET_DRV_Deinit(INST_ETHERNET1);
```

Sending a frame

```
enet_buffer_t buff;
```

```
uint8_t data[8] = {0, 1, 2, 3, 4, 5, 6, 7};

buff.data = data;
buff.length = 8;

ENET_DRV_SendFrame(INST_ETHERNET1, 0, &buff, NULL);
```

Receiving a frame - polling method

```
enet_buffer_t buff;
status_t status;

for (;;)
{
    status = ENET_DRV_ReadFrame(INST_ETHERNET1, 0, &buff, NULL);
    if (status == STATUS_SUCCESS)
    {
        /* Process buff */

        /* buff is no longer needed, provide it to the driver in order to be
        used by the reception mechanism */
        ENET_DRV_ProvideRxBuff(INST_ETHERNET1, 0, &buff);
    }
}
```

Receiving a frame - interrupt method

```
void rx_callback(uint8_t instance, enet_event_t event)
{
    if (event == ENET_RX_EVENT)
    {
        enet_buffer_t buff;

        status = ENET_DRV_ReadFrame(INST_ETHERNET1, 0, &buff, NULL);
        if (status == STATUS_SUCCESS)
        {
            /* Process buff */

            /* buff is no longer needed, provide it to the driver in order to be
            used by the reception mechanism */
            ENET_DRV_ProvideRxBuff(INST_ETHERNET1, 0, &buff);
        }
    }
}

int main(void)
{
    /* ... */

    /* The ethernet1_InitConfig0 shall enable the receive interrupts and shall specify the callback - see
    the
    configuration example above */
    ENET_DRV_Init(INST_ETHERNET1, &ethernet1_State, &ethernet1_InitConfig0,
        ethernet1_buffConfigArr0, ethernet1_MacAddr);

    /* ... */
}
```

Data Structures

- struct [enet_buffer_t](#)
Send/Receive buffer information for the user Implements : [enet_buffer_t_Class](#). [More...](#)
- struct [enet_buffer_descriptor_t](#)
Send/Receive internal buffer descriptor Implements : [enet_buffer_descriptor_t_Class](#). [More...](#)
- struct [enet_buffer_config_t](#)
Defines the ENET buffer descriptors ring configuration structure Implements : [enet_buffer_config_t_Class](#). [More...](#)
- struct [enet_config_t](#)
Defines the ENET module configuration structure Implements : [enet_config_t_Class](#). [More...](#)
- struct [enet_state_t](#)
Internal driver state structure Implements : [enet_state_t_Class](#). [More...](#)
- struct [enet_rx_enh_info_t](#)
Enhanced information related to a receive buffer descriptor Implements : [enet_rx_enh_info_t_Class](#). [More...](#)

- struct [enet_tx_enh_info_t](#)
Enhanced information related to a transmit buffer descriptor Implements : [enet_tx_enh_info_t](#) Class. [More...](#)
- struct [enet_tx_options_t](#)
Transmit options for a particular frame. Implements : [enet_tx_options_t](#) Class. [More...](#)

Macros

- #define [ENET_FRAME_MAX_FRAMELEN](#) 1518U
Defines the maximum Ethernet frame size.
- #define [ENET_MIN_BUFFERSIZE](#) 64U
ENET minimum buffer size.
- #define [ENET_BUFF_ALIGN](#)(x) (((uint32_t)(x) + (FEATURE_ENET_BUFF_ALIGNMENT - 1UL)) & ~(FEATURE_ENET_BUFF_ALIGNMENT - 1UL))
Definitions used for aligning the data buffers.
- #define [ENET_BUFF_IS_ALIGNED](#)(x) (((uint32_t)(x) & ~(FEATURE_ENET_BUFF_ALIGNMENT - 1UL)) != 0UL)
- #define [ENET_BUFFDESCR_ALIGN](#)(x) (((uint32_t)(x) + (FEATURE_ENET_BUFFDESCR_ALIGNMENT - 1UL)) & ~(FEATURE_ENET_BUFFDESCR_ALIGNMENT - 1UL))
Definitions used for aligning the buffer descriptors.
- #define [ENET_BUFFDESCR_IS_ALIGNED](#)(x) (((uint32_t)(x) & ~(FEATURE_ENET_BUFFDESCR_ALIGNMENT - 1UL)) != 0UL)
- #define [ENET_TX_WATERMARK_SHIFT](#) (6U)
- #define [ENET_TX_WATERMARK_MASK](#) (0x3FU)
- #define [ENET_RX_ENH_ERR_PROTO_CHECKSUM](#) (0x00000010U)
- #define [ENET_RX_ENH_ERR_IPHDR_CHECKSUM](#) (0x00000020U)
- #define [ENET_RX_ENH_ERR_COLLISION](#) (0x02000000U)
- #define [ENET_RX_ENH_ERR_PHY](#) (0x04000000U)
- #define [ENET_RX_ENH_ERR_MAC](#) (0x80000000U)
- #define [ENET_TX_ENH_ERR_TIMESTAMP](#) (0x00000100U)
- #define [ENET_TX_ENH_ERR_OVERFLOW](#) (0x00000200U)
- #define [ENET_TX_ENH_ERR_LATE_COLLISION](#) (0x00000400U)
- #define [ENET_TX_ENH_ERR_FRAME](#) (0x00000800U)
- #define [ENET_TX_ENH_ERR_EXCESS_COLLISION](#) (0x00001000U)
- #define [ENET_TX_ENH_ERR_UNDERFLOW](#) (0x00002000U)

Typedefs

- typedef void(* [enet_callback_t](#)) (uint8_t instance, [enet_event_t](#) event, uint8_t ring)
Callback function invoked when one of the events in "enet_event_t" is encountered Implements : [enet_callback_t](#) Class.

Enumerations

- enum [enet_mii_mode_t](#) { [ENET_MII_MODE](#) = 0U, [ENET_RMII_MODE](#) }
Media Independent Interface mode selection Implements : [enet_mii_mode_t](#) Class.
- enum [enet_mii_speed_t](#) { [ENET_MII_SPEED_10M](#) = 0U, [ENET_MII_SPEED_100M](#) }
Media Independent Interface speed selection Implements : [enet_mii_speed_t](#) Class.
- enum [enet_mii_duplex_t](#) { [ENET_MII_HALF_DUPLEX](#) = 0U, [ENET_MII_FULL_DUPLEX](#) }
Media Independent Interface full-/half-duplex selection Implements : [enet_mii_duplex_t](#) Class.

- enum `enet_interrupt_t` {
`ENET_BABR_INTERRUPT` = `ENET_EIR_BABR_MASK`, `ENET_BABT_INTERRUPT` = `ENET_EIR_BABT`
`_MASK`, `ENET_GRACE_STOP_INTERRUPT` = `ENET_EIR_GRA_MASK`, `ENET_TX_FRAME_INTERRUPT`
`_PT` = `ENET_EIR_TXF_MASK`,
`ENET_TX_BUFFER_INTERRUPT` = `ENET_EIR_TXB_MASK`, `ENET_RX_FRAME_INTERRUPT` = `ENET`
`_EIR_RXF_MASK`, `ENET_RX_BUFFER_INTERRUPT` = `ENET_EIR_RXB_MASK`, `ENET_MII_INTERRUPT`
= `ENET_EIR_MII_MASK`,
`ENET_EBERR_INTERRUPT` = `ENET_EIR_EBERR_MASK`, `ENET_LATE_COLLISION_INTERRUPT` = `E`
`NET_EIR_LC_MASK`, `ENET_RETRY_LIMIT_INTERRUPT` = `ENET_EIR_RL_MASK`, `ENET_UNDERRUN`
`_INTERRUPT` = `ENET_EIR_UN_MASK` }

Interrupt sources Implements : `enet_interrupt_t` Class.

- enum `enet_event_t` {
`ENET_RX_EVENT`, `ENET_TX_EVENT`, `ENET_ERR_EVENT`, `ENET_WAKE_UP_EVENT`,
`ENET_PARSER_EVENT` }

Event specifier for the callback function Implements : `enet_event_t` Class.

- enum `enet_counter_t` {
`ENET_CTR_RMON_T_DROP` = 0U, `ENET_CTR_RMON_T_PACKETS`, `ENET_CTR_RMON_T_BC_PK`
`T`, `ENET_CTR_RMON_T_MC_PKT`,
`ENET_CTR_RMON_T_CRC_ALIGN`, `ENET_CTR_RMON_T_UNDERSIZE`, `ENET_CTR_RMON_T_OVE`
`RSIZE`, `ENET_CTR_RMON_T_FRAG`,
`ENET_CTR_RMON_T_JAB`, `ENET_CTR_RMON_T_COL`, `ENET_CTR_RMON_T_P64`, `ENET_CTR_RM`
`ON_T_P65TO127`,
`ENET_CTR_RMON_T_P128TO255`, `ENET_CTR_RMON_T_P256TO511`, `ENET_CTR_RMON_T_P512T`
`O1023`, `ENET_CTR_RMON_T_P1024TO2047`,
`ENET_CTR_RMON_T_P_GTE2048`, `ENET_CTR_RMON_T_OCTETS`, `ENET_CTR_IEEE_T_DROP`, `EN`
`ET_CTR_IEEE_T_FRAME_OK`,
`ENET_CTR_IEEE_T_1COL`, `ENET_CTR_IEEE_T_MCOL`, `ENET_CTR_IEEE_T_DEF`, `ENET_CTR_IEEE`
`_T_LCOL`,
`ENET_CTR_IEEE_T_EXCOL`, `ENET_CTR_IEEE_T_MACERR`, `ENET_CTR_IEEE_T_CSERR`, `ENET_CT`
`R_IEEE_T_SQE`,
`ENET_CTR_IEEE_T_FDXFC`, `ENET_CTR_IEEE_T_OCTETS_OK` = 29U, `ENET_CTR_RMON_R_PACK`
`ETS` = 33U, `ENET_CTR_RMON_R_BC_PKT`,
`ENET_CTR_RMON_R_MC_PKT`, `ENET_CTR_RMON_R_CRC_ALIGN`, `ENET_CTR_RMON_R_UNDER`
`SIZE`, `ENET_CTR_RMON_R_OVERSIZE`,
`ENET_CTR_RMON_R_FRAG`, `ENET_CTR_RMON_R_JAB`, `ENET_CTR_RMON_R_RESVD_0`, `ENET_C`
`TR_RMON_R_P64`,
`ENET_CTR_RMON_R_P65TO127`, `ENET_CTR_RMON_R_P128TO255`, `ENET_CTR_RMON_R_P256T`
`O511`, `ENET_CTR_RMON_R_P512TO1023`,
`ENET_CTR_RMON_R_P1024TO2047`, `ENET_CTR_RMON_R_P_GTE2048`, `ENET_CTR_RMON_R_OC`
`TETS`, `ENET_CTR_IEEE_R_DROP`,
`ENET_CTR_IEEE_R_FRAME_OK`, `ENET_CTR_IEEE_R_CRC`, `ENET_CTR_IEEE_R_ALIGN`, `ENET_CT`
`R_IEEE_R_MACERR`,
`ENET_CTR_IEEE_R_FDXFC`, `ENET_CTR_IEEE_R_OCTETS_OK` }

Statistics counters enumeration Implements : `enet_counter_t` Class.

- enum `enet_fifo_threshold_t` {
`ENET_RX_SECTION_FULL` = 0U, `ENET_RX_SECTION_EMPTY`, `ENET_RX_ALMOST_EMPTY`, `ENET`
`RX_ALMOST_FULL`,
`ENET_TX_SECTION_EMPTY`, `ENET_TX_ALMOST_EMPTY`, `ENET_TX_ALMOST_FULL` }

Available FIFO threshold levels. Implements : `enet_fifo_threshold_t` Class.

Initialization and De-initialization

- void `ENET_DRV_GetDefaultConfig` (`enet_config_t` *config)
Gets the default configuration structure.
- void `ENET_DRV_Init` (`uint8_t` instance, `enet_state_t` *state, const `enet_config_t` *config, const `enet_buffer`
`_config_t` bufferConfig[], const `uint8_t` *macAddr)

Initializes the ENET module.

- void [ENET_DRV_Deinit](#) (uint8_t instance)

Deinitializes the ENET module.

Transmission and reception operations

- status_t [ENET_DRV_ReadFrame](#) (uint8_t instance, uint8_t queue, [enet_buffer_t](#) *buff, [enet_rx_enh_info_t](#) *info)

Reads a received Ethernet frame.

- void [ENET_DRV_ProvideRxBuff](#) (uint8_t instance, uint8_t queue, [enet_buffer_t](#) *buff)

Provides a receive buffer to be used by the driver for reception.

- status_t [ENET_DRV_SendFrame](#) (uint8_t instance, uint8_t queue, const [enet_buffer_t](#) *buff, [enet_tx_options_t](#) *options)

Sends an Ethernet frame.

- status_t [ENET_DRV_GetTransmitStatus](#) (uint8_t instance, uint8_t queue, const [enet_buffer_t](#) *buff, [enet_tx_enh_info_t](#) *info)

Checks if the transmission of a buffer is complete and extracts information related to the transmission.

MDIO configuration and operation

- void [ENET_DRV_EnableMDIO](#) (uint8_t instance, bool miiPreambleDisabled)

Enables the MDIO interface.

- status_t [ENET_DRV_MDIORead](#) (uint8_t instance, uint8_t phyAddr, uint8_t phyReg, uint16_t *data, uint32_t timeoutMs)

Reads the selected register of the PHY.

- status_t [ENET_DRV_MDIOWrite](#) (uint8_t instance, uint8_t phyAddr, uint8_t phyReg, uint16_t data, uint32_t timeoutMs)

Writes the selected register of the PHY.

- status_t [ENET_DRV_MDIOReadMMD](#) (uint8_t instance, uint8_t phyAddr, uint8_t mmd, uint16_t phyReg, uint16_t *data, uint32_t timeoutMs)

Reads a register of the specified MMD in a PHY device.

- status_t [ENET_DRV_MDIOWriteMMD](#) (uint8_t instance, uint8_t phyAddr, uint8_t mmd, uint16_t phyReg, uint16_t data, uint32_t timeoutMs)

Writes a register of the specified MMD in a PHY device.

MAC Address configuration

- void [ENET_DRV_SetMacAddr](#) (uint8_t instance, const uint8_t *macAddr)

Configures the physical address of the MAC.

- void [ENET_DRV_GetMacAddr](#) (uint8_t instance, uint8_t *macAddr)

Gets the physical address of the MAC.

- void [ENET_DRV_SetUnicastForward](#) (uint8_t instance, const uint8_t *macAddr, bool enable)

Enables/Disables forwarding of unicast traffic having a specific MAC address as destination.

- void [ENET_DRV_SetMulticastForward](#) (uint8_t instance, const uint8_t *macAddr, bool enable)

Enables/Disables forwarding of multicast traffic having a specific MAC address as destination.

- void [ENET_DRV_SetMulticastForwardAll](#) (uint8_t instance, bool enable)

Enables/Disables forwarding of the multicast traffic, irrespective of the destination MAC address.

Other basic operations

- void [ENET_DRV_ConfigCounters](#) (uint8_t instance, bool enable)
Enables/Disables the MIB counters.
- uint32_t [ENET_DRV_GetCounter](#) (uint8_t instance, [enet_counter_t](#) counter)
Gets statistics from the specified counter.
- uint32_t [ENET_DRV_GetInterruptFlags](#) (uint8_t instance)
Gets a mask of the interrupt events which occurred.
- void [ENET_DRV_SetSpeed](#) (uint8_t instance, [enet_mii_speed_t](#) speed)
Sets the speed of the MII interface.

17.42.2 Data Structure Documentation

17.42.2.1 struct enet_buffer_t

Send/Receive buffer information for the user Implements : [enet_buffer_t_Class](#).

Definition at line 233 of file [enet_driver.h](#).

Data Fields

- uint8_t * [data](#)
- uint16_t [length](#)

Field Documentation

17.42.2.1.1 uint8_t* data

Definition at line 235 of file [enet_driver.h](#).

17.42.2.1.2 uint16_t length

Definition at line 236 of file [enet_driver.h](#).

17.42.2.2 struct enet_buffer_descriptor_t

Send/Receive internal buffer descriptor Implements : [enet_buffer_descriptor_t_Class](#).

Definition at line 263 of file [enet_driver.h](#).

Data Fields

- uint16_t [length](#)
- uint16_t [control](#)
- uint8_t * [buffer](#)

Field Documentation

17.42.2.2.1 uint8_t* buffer

Data buffer pointer.

Definition at line 267 of file [enet_driver.h](#).

17.42.2.2.2 uint16_t control

Buffer descriptor control and status.

Definition at line 266 of file [enet_driver.h](#).

17.42.2.2.3 uint16_t length

Buffer descriptor data length.

Definition at line 265 of file enet_driver.h.

17.42.2.3 struct enet_buffer_config_t

Defines the ENET buffer descriptors ring configuration structure Implements : enet_buffer_config_t_Class.

Definition at line 316 of file enet_driver.h.

Data Fields

- uint16_t [rxRingSize](#)
- uint16_t [txRingSize](#)
- [enet_buffer_descriptor_t](#) * [rxRingAligned](#)
- [enet_buffer_descriptor_t](#) * [txRingAligned](#)
- uint8_t * [rxBufferAligned](#)

Field Documentation

17.42.2.3.1 uint8_t* rxBufferAligned

Receive data buffers start address.

Definition at line 322 of file enet_driver.h.

17.42.2.3.2 enet_buffer_descriptor_t* rxRingAligned

Aligned receive buffer descriptor ring start address.

Definition at line 320 of file enet_driver.h.

17.42.2.3.3 uint16_t rxRingSize

Receive buffer descriptors number.

Definition at line 318 of file enet_driver.h.

17.42.2.3.4 enet_buffer_descriptor_t* txRingAligned

Aligned transmit buffer descriptor ring start address.

Definition at line 321 of file enet_driver.h.

17.42.2.3.5 uint16_t txRingSize

Transmit buffer descriptors number.

Definition at line 319 of file enet_driver.h.

17.42.2.4 struct enet_config_t

Defines the ENET module configuration structure Implements : enet_config_t_Class.

Definition at line 329 of file enet_driver.h.

Data Fields

- uint16_t [maxFrameLen](#)
- uint32_t [interrupts](#)
- [enet_mii_mode_t](#) [miiMode](#)
- [enet_mii_speed_t](#) [miiSpeed](#)
- [enet_mii_duplex_t](#) [miiDuplex](#)

- [enet_callback_t callback](#)
- [uint8_t ringCount](#)

Field Documentation

17.42.2.4.1 [enet_callback_t callback](#)

Definition at line 351 of file `enet_driver.h`.

17.42.2.4.2 [uint32_t interrupts](#)

MAC interrupt source. A logical OR of "enet_interrupt_t".

Definition at line 338 of file `enet_driver.h`.

17.42.2.4.3 [uint16_t maxFrameLen](#)

Maximum frame length.

Definition at line 337 of file `enet_driver.h`.

17.42.2.4.4 [enet_mii_duplex_t miiDuplex](#)

MII duplex.

Definition at line 342 of file `enet_driver.h`.

17.42.2.4.5 [enet_mii_mode_t miiMode](#)

MII mode.

Definition at line 340 of file `enet_driver.h`.

17.42.2.4.6 [enet_mii_speed_t miiSpeed](#)

MII Speed.

Definition at line 341 of file `enet_driver.h`.

17.42.2.4.7 [uint8_t ringCount](#)

The number of rings to be used by the driver.

Definition at line 352 of file `enet_driver.h`.

17.42.2.5 [struct enet_state_t](#)

Internal driver state structure Implements : `enet_state_t_Class`.

Definition at line 359 of file `enet_driver.h`.

Data Fields

- [enet_buffer_descriptor_t * rxBdBase](#) [FEATURE_ENET_RING_COUNT]
- [enet_buffer_descriptor_t * rxBdCurrent](#) [FEATURE_ENET_RING_COUNT]
- [enet_buffer_descriptor_t * rxBdAlloc](#) [FEATURE_ENET_RING_COUNT]
- [enet_buffer_descriptor_t * txBdBase](#) [FEATURE_ENET_RING_COUNT]
- [enet_buffer_descriptor_t * txBdCurrent](#) [FEATURE_ENET_RING_COUNT]
- [enet_callback_t callback](#)
- [uint8_t ringCount](#)

Field Documentation

17.42.2.5.1 `enet_callback_t` callback

Callback function.

Definition at line 366 of file `enet_driver.h`.

17.42.2.5.2 `uint8_t` ringCount

The number of rings used by the driver.

Definition at line 370 of file `enet_driver.h`.

17.42.2.5.3 `enet_buffer_descriptor_t*` `rxBdAlloc[FEATURE_ENET_RING_COUNT]`

Pointer array used for enqueueing Rx buffers provided using `ENET_DRV_ProvideRxBuff`.

Definition at line 363 of file `enet_driver.h`.

17.42.2.5.4 `enet_buffer_descriptor_t*` `rxBdBase[FEATURE_ENET_RING_COUNT]`

Receive buffer descriptor base address pointer array.

Definition at line 361 of file `enet_driver.h`.

17.42.2.5.5 `enet_buffer_descriptor_t*` `rxBdCurrent[FEATURE_ENET_RING_COUNT]`

The current available receive buffer descriptor pointer array.

Definition at line 362 of file `enet_driver.h`.

17.42.2.5.6 `enet_buffer_descriptor_t*` `txBdBase[FEATURE_ENET_RING_COUNT]`

Transmit buffer descriptor base address pointer array.

Definition at line 364 of file `enet_driver.h`.

17.42.2.5.7 `enet_buffer_descriptor_t*` `txBdCurrent[FEATURE_ENET_RING_COUNT]`

The current available transmit buffer descriptor pointer array.

Definition at line 365 of file `enet_driver.h`.

17.42.2.6 `struct enet_rx_enh_info_t`

Enhanced information related to a receive buffer descriptor Implements : `enet_rx_enh_info_t_Class`.

Definition at line 439 of file `enet_driver.h`.

Data Fields

- `uint32_t` [errMask](#)
- `uint32_t` [timestamp](#)
- `uint16_t` [checksum](#)
- `uint8_t` [vlanPrio](#)
- `uint8_t` [headerLen](#)
- `uint8_t` [proto](#)
- `bool` [unicast](#)
- `bool` [ipv6](#)
- `bool` [ipv4Frag](#)

Field Documentation

17.42.2.6.1 `uint16_t` checksum

One's complement sum of the payload section of the IP frame.

Definition at line 442 of file enet_driver.h.

17.42.2.6.2 uint32_t errMask

Mask of ENET_RX_ENH_ERR_*, representing the errors that occurred.

Definition at line 440 of file enet_driver.h.

17.42.2.6.3 uint8_t headerLen

Number of 32-bit words found within the IP and its following protocol headers.

Definition at line 444 of file enet_driver.h.

17.42.2.6.4 bool ipv4Frag

Indicates that the frame is an IPv4 fragment frame.

Definition at line 448 of file enet_driver.h.

17.42.2.6.5 bool ipv6

Indicates that the frame is an IPv6 frame.

Definition at line 447 of file enet_driver.h.

17.42.2.6.6 uint8_t proto

The 8-bit protocol field found within the IP header of the frame.

Definition at line 445 of file enet_driver.h.

17.42.2.6.7 uint32_t timestamp

Timestamp of the received frame.

Definition at line 441 of file enet_driver.h.

17.42.2.6.8 bool unicast

Indicates that the frame is an unicast frame.

Definition at line 446 of file enet_driver.h.

17.42.2.6.9 uint8_t vlanPrio

Frame priority level. Valid values are from 0 (best effort) to 7 (highest).

Definition at line 443 of file enet_driver.h.

17.42.2.7 struct enet_tx_enh_info_t

Enhanced information related to a transmit buffer descriptor Implements : enet_tx_enh_info_t_Class.

Definition at line 455 of file enet_driver.h.

Data Fields

- uint32_t [errMask](#)
- uint32_t [timestamp](#)

Field Documentation

17.42.2.7.1 uint32_t errMask

Mask of ENET_TX_ENH_ERR_*, representing the errors that occurred.

Definition at line 456 of file enet_driver.h.

17.42.2.7.2 uint32_t timestamp

Timestamp of the transmitted frame.

Definition at line 457 of file enet_driver.h.

17.42.2.8 struct enet_tx_options_t

Transmit options for a particular frame. Implements : enet_tx_options_t_Class.

Definition at line 547 of file enet_driver.h.

Data Fields

- bool [noCRC](#)
- bool [noInt](#)

Field Documentation

17.42.2.8.1 bool noCRC

Do not append CRC. It will be provided by the application.

Definition at line 548 of file enet_driver.h.

17.42.2.8.2 bool noInt

Do not generate a transmit interrupt.

Definition at line 549 of file enet_driver.h.

17.42.3 Macro Definition Documentation

17.42.3.1 **#define ENET_BUFF_ALIGN(x) (((uint32_t)(x) + (FEATURE_ENET_BUFF_ALIGNMENT - 1UL)) & ~ (FEATURE_ENET_BUFF_ALIGNMENT - 1UL))**

Definitions used for aligning the data buffers.

Definition at line 66 of file enet_driver.h.

17.42.3.2 **#define ENET_BUFF_IS_ALIGNED(x) (((uint32_t)(x) & ~ (FEATURE_ENET_BUFF_ALIGNMENT - 1UL)) != 0UL)**

Definition at line 67 of file enet_driver.h.

17.42.3.3 **#define ENET_BUFFDESCR_ALIGN(x) (((uint32_t)(x) + (FEATURE_ENET_BUFFDESCR_ALIGNMENT - 1UL)) & ~ (FEATURE_ENET_BUFFDESCR_ALIGNMENT - 1UL))**

Definitions used for aligning the buffer descriptors.

Definition at line 70 of file enet_driver.h.

17.42.3.4 **#define ENET_BUFFDESCR_IS_ALIGNED(x) (((uint32_t)(x) & ~ (FEATURE_ENET_BUFFDESCR_ALIGNMENT - 1UL)) != 0UL)**

Definition at line 71 of file enet_driver.h.

17.42.3.5 **#define ENET_FRAME_MAX_FRAMELEN 1518U**

Defines the maximum Ethernet frame size.

Definition at line 61 of file enet_driver.h.

17.42.3.6 #define ENET_MIN_BUFFERSIZE 64U

ENET minimum buffer size.

Definition at line 63 of file enet_driver.h.

17.42.3.7 #define ENET_RX_ENH_ERR_COLLISION (0x02000000U)

Set when the frame was received with a collision detected during reception.

Definition at line 467 of file enet_driver.h.

17.42.3.8 #define ENET_RX_ENH_ERR_IPHDR_CHECKSUM (0x00000020U)

Set when either a non-IP frame is received or the IP header checksum was invalid.

Definition at line 464 of file enet_driver.h.

17.42.3.9 #define ENET_RX_ENH_ERR_MAC (0x80000000U)

Set when the frame stored in the system memory was received with an error (typically, a receive FIFO overflow).

Definition at line 473 of file enet_driver.h.

17.42.3.10 #define ENET_RX_ENH_ERR_PHY (0x04000000U)

Set when the frame was received with an Error character on the PHY interface.

Definition at line 470 of file enet_driver.h.

17.42.3.11 #define ENET_RX_ENH_ERR_PROTO_CHECKSUM (0x00000010U)

Set when the checksum of the protocol is invalid or an unknown protocol is found and checksumming could not be performed.

Definition at line 461 of file enet_driver.h.

17.42.3.12 #define ENET_TX_ENH_ERR_EXCESS_COLLISION (0x00001000U)

Indicates that the MAC reported an excess collision error on transmit.

Definition at line 489 of file enet_driver.h.

17.42.3.13 #define ENET_TX_ENH_ERR_FRAME (0x00000800U)

Indicates that the MAC reported that the uDMA reported an error when providing the packet.

Definition at line 486 of file enet_driver.h.

17.42.3.14 #define ENET_TX_ENH_ERR_LATE_COLLISION (0x00000400U)

Indicates that the MAC reported that there was a Late Collision on transmit.

Definition at line 483 of file enet_driver.h.

17.42.3.15 #define ENET_TX_ENH_ERR_OVERFLOW (0x00000200U)

Indicates that the MAC reported that there was a FIFO overflow condition on transmit.

Definition at line 480 of file enet_driver.h.

17.42.3.16 #define ENET_TX_ENH_ERR_TIMESTAMP (0x00000100U)

Indicates that the MAC reported a different frame type than a timestamp frame.

Definition at line 477 of file enet_driver.h.

17.42.3.17 `#define ENET_TX_ENH_ERR_UNDERFLOW (0x00002000U)`

Indicates that the MAC reported an underflow error on transmit.

Definition at line 492 of file `enet_driver.h`.

17.42.3.18 `#define ENET_TX_WATERMARK_MASK (0x3FU)`

Definition at line 74 of file `enet_driver.h`.

17.42.3.19 `#define ENET_TX_WATERMARK_SHIFT (6U)`

Definition at line 73 of file `enet_driver.h`.

17.42.4 Typedef Documentation

17.42.4.1 `typedef void(* enet_callback_t)(uint8_t instance, enet_event_t event, uint8_t ring)`

Callback function invoked when one of the events in "enet_event_t" is encountered Implements : `enet_callback_t↔_Class`.

Definition at line 298 of file `enet_driver.h`.

17.42.5 Enumeration Type Documentation

17.42.5.1 `enum enet_counter_t`

Statistics counters enumeration Implements : `enet_counter_t_Class`.

Enumerator

ENET_CTR_RMON_T_DROP
ENET_CTR_RMON_T_PACKETS
ENET_CTR_RMON_T_BC_PKT
ENET_CTR_RMON_T_MC_PKT
ENET_CTR_RMON_T_CRC_ALIGN
ENET_CTR_RMON_T_UNDERSIZE
ENET_CTR_RMON_T_OVERSIZE
ENET_CTR_RMON_T_FRAG
ENET_CTR_RMON_T_JAB
ENET_CTR_RMON_T_COL
ENET_CTR_RMON_T_P64
ENET_CTR_RMON_T_P65TO127
ENET_CTR_RMON_T_P128TO255
ENET_CTR_RMON_T_P256TO511
ENET_CTR_RMON_T_P512TO1023
ENET_CTR_RMON_T_P1024TO2047
ENET_CTR_RMON_T_P_GTE2048
ENET_CTR_RMON_T_OCTETS
ENET_CTR_IEEE_T_DROP
ENET_CTR_IEEE_T_FRAME_OK
ENET_CTR_IEEE_T_1COL
ENET_CTR_IEEE_T_MCOL

ENET_CTR_IEEE_T_DEF
ENET_CTR_IEEE_T_LCOL
ENET_CTR_IEEE_T_EXCOL
ENET_CTR_IEEE_T_MACERR
ENET_CTR_IEEE_T_CSERR
ENET_CTR_IEEE_T_SQE
ENET_CTR_IEEE_T_FDXFC
ENET_CTR_IEEE_T_OCTETS_OK
ENET_CTR_RMON_R_PACKETS
ENET_CTR_RMON_R_BC_PKT
ENET_CTR_RMON_R_MC_PKT
ENET_CTR_RMON_R_CRC_ALIGN
ENET_CTR_RMON_R_UNDERSIZE
ENET_CTR_RMON_R_OVERSIZE
ENET_CTR_RMON_R_FRAG
ENET_CTR_RMON_R_JAB
ENET_CTR_RMON_R_RESVD_0
ENET_CTR_RMON_R_P64
ENET_CTR_RMON_R_P65TO127
ENET_CTR_RMON_R_P128TO255
ENET_CTR_RMON_R_P256TO511
ENET_CTR_RMON_R_P512TO1023
ENET_CTR_RMON_R_P1024TO2047
ENET_CTR_RMON_R_P_GTE2048
ENET_CTR_RMON_R_OCTETS
ENET_CTR_IEEE_R_DROP
ENET_CTR_IEEE_R_FRAME_OK
ENET_CTR_IEEE_R_CRC
ENET_CTR_IEEE_R_ALIGN
ENET_CTR_IEEE_R_MACERR
ENET_CTR_IEEE_R_FDXFC
ENET_CTR_IEEE_R_OCTETS_OK

Definition at line 377 of file enet_driver.h.

17.42.5.2 enum enet_event_t

Event specifier for the callback function Implements : enet_event_t_Class.

Enumerator

ENET_RX_EVENT
ENET_TX_EVENT
ENET_ERR_EVENT
ENET_WAKE_UP_EVENT
ENET_PARSER_EVENT

Definition at line 285 of file enet_driver.h.

17.42.5.3 enum enet_fifo_threshold_t

Available FIFO threshold levels. Implements : enet_fifo_threshold_t_Class.

Enumerator

ENET_RX_SECTION_FULL

ENET_RX_SECTION_EMPTY

ENET_RX_ALMOST_EMPTY

ENET_RX_ALMOST_FULL

ENET_TX_SECTION_EMPTY Value, in 64-bit words, of the transmit FIFO section empty threshold. When the FIFO level reaches this value, a MAC status signal indicates that the transmit FIFO is getting full. This gives the ENET module an indication to slow or stop its write transaction to avoid a buffer overflow.

ENET_TX_ALMOST_EMPTY Value, in 64-bit words, of the transmit FIFO almost empty threshold. When the FIFO level reaches this level and no end-of-frame is available for the frame, the MAC transmit logic, to avoid FIFO underflow, stops reading the FIFO and transmits a frame with an MII error indication.

ENET_TX_ALMOST_FULL Value, in 64-bit words, of the transmit FIFO almost full threshold. A minimum value of six is required. When the FIFO level comes close to the maximum, so that there is no more space for at least TX_ALMOST_FULL number of words, the FIFO write control logic, to avoid FIFO overflow, truncates the current frame and sets the error status. As a result, the frame will be transmitted with an GMII/MII error indication.

Definition at line 575 of file enet_driver.h.

17.42.5.4 enum enet_interrupt_t

Interrupt sources Implements : enet_interrupt_t_Class.

Enumerator

ENET_BABR_INTERRUPT

ENET_BABT_INTERRUPT

ENET_GRACE_STOP_INTERRUPT

ENET_TX_FRAME_INTERRUPT

ENET_TX_BUFFER_INTERRUPT

ENET_RX_FRAME_INTERRUPT

ENET_RX_BUFFER_INTERRUPT

ENET_MII_INTERRUPT

ENET_EBERR_INTERRUPT

ENET_LATE_COLLISION_INTERRUPT

ENET_RETRY_LIMIT_INTERRUPT

ENET_UNDERRUN_INTERRUPT

Definition at line 158 of file enet_driver.h.

17.42.5.5 enum enet_mii_duplex_t

Media Independent Interface full-/half-duplex selection Implements : enet_mii_duplex_t_Class.

Enumerator

ENET_MII_HALF_DUPLEX Half-duplex mode.

ENET_MII_FULL_DUPLEX Full-duplex mode.

Definition at line 106 of file enet_driver.h.

17.42.5.6 enum enet_mii_mode_t

Media Independent Interface mode selection Implements : enet_mii_mode_t_Class.

Enumerator

ENET_MII_MODE MII mode for data interface.

ENET_RMII_MODE RMII mode for data interface.

Definition at line 80 of file enet_driver.h.

17.42.5.7 enum enet_mii_speed_t

Media Independent Interface speed selection Implements : enet_mii_speed_t_Class.

Enumerator

ENET_MII_SPEED_10M Speed 10 Mbps.

ENET_MII_SPEED_100M Speed 100 Mbps.

Definition at line 93 of file enet_driver.h.

17.42.6 Function Documentation

17.42.6.1 void ENET_DRV_ConfigCounters (uint8_t instance, bool enable)

Enables/Disables the MIB counters.

Note: When enabling the counters, their values are reset.

Parameters

in	instance	Instance number
in	enable	Enable/Disable MIB counters

Definition at line 1218 of file enet_driver.c.

17.42.6.2 void ENET_DRV_Deinit (uint8_t instance)

Deinitializes the ENET module.

This function disables the interrupts and then disables the ENET module.

Parameters

in	instance	Instance number
----	----------	-----------------

Definition at line 537 of file enet_driver.c.

17.42.6.3 void ENET_DRV_EnableMDIO (uint8_t instance, bool miiPreambleDisabled)

Enables the MDIO interface.

Parameters

in	instance	Instance number
in	miiPreambleDisabled	Enables/disables prepending a preamble to the MII management frame.

Definition at line 867 of file enet_driver.c.

17.42.6.4 uint32_t ENET_DRV_GetCounter (uint8_t instance, enet_counter_t counter)

Gets statistics from the specified counter.

Parameters

in	<i>instance</i>	Instance number
in	<i>counter</i>	The counter to be read

Returns

The value of the requested counter

Definition at line 1233 of file enet_driver.c.

17.42.6.5 void ENET_DRV_GetDefaultConfig (enet_config_t * config)

Gets the default configuration structure.

This function gets the default configuration structure, with the following settings:

- no interrupt enabled
- maximum receive frame length equal to the maximum Ethernet frame length
- no special receive/transmit control configuration
- no acceleration function enabled
- RMII mode, full-duplex, 100Mbps for MAC and PHY data interface
- no callback installed

Parameters

out	<i>config</i>	The configuration structure
-----	---------------	-----------------------------

Definition at line 349 of file enet_driver.c.

17.42.6.6 uint32_t ENET_DRV_GetInterruptFlags (uint8_t instance)

Gets a mask of the interrupt events which occurred.

Parameters

in	<i>instance</i>	Instance number
----	-----------------	-----------------

Returns

A logical OR of "enet_interrupt_t"

Definition at line 1252 of file enet_driver.c.

17.42.6.7 void ENET_DRV_GetMacAddr (uint8_t instance, uint8_t * macAddr)

Gets the physical address of the MAC.

Parameters

in	<i>instance</i>	Instance number
out	<i>macAddr</i>	The physical address of the MAC

Definition at line 1066 of file enet_driver.c.

17.42.6.8 status_t ENET_DRV_GetTransmitStatus (uint8_t instance, uint8_t queue, const enet_buffer_t * buff, enet_tx_enh_info_t * info)

Checks if the transmission of a buffer is complete and extracts information related to the transmission.

This function checks if the transmission of the given buffer is complete and extracts information related to the transmission.

Note: If the buffer is not found in the Tx ring, the function will return STATUS_ENET_BUFF_NOT_FOUND; in this case, the enhanced information will not be extracted.

Parameters

in	<i>instance</i>	Instance number
in	<i>queue</i>	The queue number
in	<i>buff</i>	The transmit buffer for which the status shall be checked
out	<i>info</i>	Enhanced information related to the buffer. If this information is not needed, this parameter should be NULL.

Returns

STATUS_BUSY if the frame is still enqueued for transmission, STATUS_ENET_BUFF_NOT_FOUND if the buffer was not found in the Tx queue, STATUS_SUCCESS otherwise,.

Definition at line 755 of file enet_driver.c.

17.42.6.9 void ENET_DRV_Init (uint8_t *instance*, enet_state_t * *state*, const enet_config_t * *config*, const enet_buffer_config_t *bufferConfig*[], const uint8_t * *macAddr*)

Initializes the ENET module.

This function initializes and enables the ENET module, configuring receive and transmit control settings, the receive and transmit descriptors rings, and the MAC physical address.

Parameters

in	<i>instance</i>	Instance number
in	<i>state</i>	Pointer to the state structure which will be used for holding the internal state of the driver.
in	<i>config</i>	The module configuration structure
in	<i>bufferConfig</i>	The array of buffer descriptors configuration structures (one per ring)
in	<i>macAddr</i>	The physical address of the MAC

Definition at line 391 of file enet_driver.c.

17.42.6.10 status_t ENET_DRV_MDIORead (uint8_t *instance*, uint8_t *phyAddr*, uint8_t *phyReg*, uint16_t * *data*, uint32_t *timeoutMs*)

Reads the selected register of the PHY.

Parameters

in	<i>instance</i>	Instance number
in	<i>phyAddr</i>	PHY device address
in	<i>phyReg</i>	PHY register address
out	<i>data</i>	Data read from the PHY
in	<i>timeoutMs</i>	Timeout for the read operation (in milliseconds)

Returns

STATUS_SUCCESS if the operation completed successfully, STATUS_TIMEOUT if the specified timeout expired before completing the operation.

Definition at line 926 of file enet_driver.c.

17.42.6.11 status_t ENET_DRV_MDIOReadMMD (uint8_t *instance*, uint8_t *phyAddr*, uint8_t *mmd*, uint16_t *phyReg*, uint16_t * *data*, uint32_t *timeoutMs*)

Reads a register of the specified MMD in a PHY device.

Parameters

in	<i>instance</i>	Instance number
in	<i>phyAddr</i>	PHY device address
in	<i>mmd</i>	The MMD index of the target register
in	<i>phyReg</i>	PHY register address
out	<i>data</i>	Data read from the PHY
in	<i>timeoutMs</i>	Timeout for the read operation (in milliseconds)

Returns

STATUS_SUCCESS if the operation completed successfully, STATUS_TIMEOUT if the specified timeout expired before completing the operation.

Definition at line 994 of file enet_driver.c.

17.42.6.12 `status_t ENET_DRV_MDIOWrite (uint8_t instance, uint8_t phyAddr, uint8_t phyReg, uint16_t data, uint32_t timeoutMs)`

Writes the selected register of the PHY.

Parameters

in	<i>instance</i>	Instance number
in	<i>phyAddr</i>	PHY device address
in	<i>phyReg</i>	PHY register address
in	<i>data</i>	Data to be written in the specified register of the PHY
in	<i>timeoutMs</i>	Timeout for the write operation (in milliseconds)

Returns

STATUS_SUCCESS if the operation completed successfully, STATUS_TIMEOUT if the specified timeout expired before completing the operation.

Definition at line 898 of file enet_driver.c.

17.42.6.13 `status_t ENET_DRV_MDIOWriteMMD (uint8_t instance, uint8_t phyAddr, uint8_t mmd, uint16_t phyReg, uint16_t data, uint32_t timeoutMs)`

Writes a register of the specified MMD in a PHY device.

Parameters

in	<i>instance</i>	Instance number
in	<i>phyAddr</i>	PHY device address
in	<i>mmd</i>	The MMD index of the target register
in	<i>phyReg</i>	PHY register address
in	<i>data</i>	Data to be written in the specified register of the PHY
in	<i>timeoutMs</i>	Timeout for the write operation (in milliseconds)

Returns

STATUS_SUCCESS if the operation completed successfully, STATUS_TIMEOUT if the specified timeout expired before completing the operation.

Definition at line 959 of file enet_driver.c.

17.42.6.14 `void ENET_DRV_ProvideRxBuff (uint8_t instance, uint8_t queue, enet_buffer_t * buff)`

Provides a receive buffer to be used by the driver for reception.

This function provides a buffer which can further be used by the reception mechanism in order to store the received data.

Note: The application can either provide a buffer previously obtained in a `ENET_DRV_ReadFrame` call (when it is no longer needed after being fully processed), or allocate a new buffer, pointing to a memory area having the required alignment (see `FEATURE_ENET_BUFF_ALIGNMENT`). The former approach is recommended as it has a simpler usage model and re-uses the same initial memory range for the entire driver lifetime operation. The later approach could provide more flexibility, but since it involves constant memory free/alloc operations it is only recommended with an efficient pool-based memory allocator.

Important: The driver does not ensure synchronization between different threads trying to provide a buffer at the same time. This synchronization shall be implemented by the application.

Important: The application is responsible for providing one Rx buffer for every frame it receives, otherwise the reception ring can fill-up, affecting further reception.

Usage example:

```
stat = ENET_DRV_ReadFrame(INST_ETHERNET1, &rxBuff);

if (stat == STATUS_SUCCESS) { process_buffer(&rxBuff); ENET_DRV_ProvideRxBuff(INST_ETHERNET1, &rxBuff); }
```

Parameters

in	<i>instance</i>	Instance number
in	<i>queue</i>	The queue number
in	<i>buff</i>	The buffer to be added to the reception ring

Definition at line 821 of file `enet_driver.c`.

17.42.6.15 `status_t ENET_DRV_ReadFrame (uint8_t instance, uint8_t queue, enet_buffer_t * buff, enet_rx_enh_info_t * info)`

Reads a received Ethernet frame.

This function reads the first received Ethernet frame in the Rx queue. The buffer received as parameter will be updated by the driver and the `.data` field will point to a memory area containing the frame data.

Note: Once the application finished processing the buffer, it could be reused by the driver for further receptions by invoking `ENET_DRV_ProvideRxBuff`.

Important: The driver does not ensure synchronization between different threads trying to read a frame at the same time. This synchronization shall be implemented by the application.

Parameters

in	<i>instance</i>	Instance number
in	<i>queue</i>	The queue number
out	<i>buff</i>	The buffer containing the frame
out	<i>info</i>	Enhanced information related to the buffer. If this information is not needed, this parameter should be NULL.

Returns

`STATUS_SUCCESS` if a frame was successfully read, `STATUS_ENET_RX_QUEUE_EMPTY` if there is no available frame in the queue.

Definition at line 609 of file `enet_driver.c`.

17.42.6.16 `status_t ENET_DRV_SendFrame (uint8_t instance, uint8_t queue, const enet_buffer_t * buff, enet_tx_options_t * options)`

Sends an Ethernet frame.

This function sends an Ethernet frame, contained in the buffer received as parameter.

Note: Since the transmission of the frame is not complete when this function returns, the application must not change/alter/re-use the provided buffer until after a call to ENET_DRV_GetTransmitStatus for the same buffer returns STATUS_SUCCESS.

Important: The driver does not ensure synchronization between different threads trying to send a frame at the same time. This synchronization shall be implemented by the application.

Parameters

in	<i>instance</i>	Instance number
in	<i>queue</i>	The queue number
in	<i>buff</i>	The buffer containing the frame
in	<i>options</i>	Transmit options for this buffer. Can be NULL, if no special option is required.

Returns

STATUS_SUCCESS if the frame was successfully enqueued for transmission, STATUS_ENET_TX_QUEUE_FULL if there is no available space for the frame in the queue.

Definition at line 677 of file enet_driver.c.

17.42.6.17 void ENET_DRV_SetMacAddr (uint8_t *instance*, const uint8_t* *macAddr*)

Configures the physical address of the MAC.

Parameters

in	<i>instance</i>	Instance number
in	<i>macAddr</i>	The MAC address to be configured

Definition at line 1034 of file enet_driver.c.

17.42.6.18 void ENET_DRV_SetMulticastForward (uint8_t *instance*, const uint8_t* *macAddr*, bool *enable*)

Enables/Disables forwarding of multicast traffic having a specific MAC address as destination.

Parameters

in	<i>instance</i>	Instance number
in	<i>macAddr</i>	The physical address
in	<i>enable</i>	If true, the application will receive all the multicast traffic having as destination address the provided MAC address; if false, stop forwarding this kind of traffic

Definition at line 1129 of file enet_driver.c.

17.42.6.19 void ENET_DRV_SetMulticastForwardAll (uint8_t *instance*, bool *enable*)

Enables/Disables forwarding of the multicast traffic, irrespective of the destination MAC address.

Parameters

in	<i>instance</i>	Instance number
in	<i>enable</i>	If true, the application will receive all the multicast traffic; if false, stop forwarding this kind of traffic

Definition at line 1160 of file enet_driver.c.

17.42.6.20 void ENET_DRV_SetSpeed (uint8_t *instance*, enet_mii_speed_t *speed*)

Sets the speed of the MII interface.

Parameters

in	<i>instance</i>	Instance number
in	<i>speed</i>	MII speed

Definition at line 1270 of file enet_driver.c.

17.42.6.21 void ENET_DRV_SetUnicastForward (uint8_t *instance*, const uint8_t * *macAddr*, bool *enable*)

Enables/Disables forwarding of unicast traffic having a specific MAC address as destination.

Parameters

in	<i>instance</i>	Instance number
in	<i>macAddr</i>	The physical address
in	<i>enable</i>	If true, the application will receive all the unicast traffic having as destination address the provided MAC address; if false, stop forwarding this kind of traffic

Definition at line 1098 of file enet_driver.c.

17.43 ERM Driver

17.43.1 Detailed Description

Error Reporting Module Peripheral Driver.

This section describes the programming interface of the ERM driver.

17.43.2 ERM Driver Initialization

In order to be able to use the error reporting in your application, the first thing to do is initializing it with user configuration input. This is done by calling the **ERM_DRV_Init** function. Note that: channelCnt takes values between 1 and the maximum channel count supported by the hardware.

17.43.3 ERM Driver Operation

After ERM initialization, the **ERM_DRV_SetInterruptConfig()** shall be used to set interrupt notification based on interrupt notification configuration.

The **ERM_DRV_GetInterruptConfig()** shall be used to get the current interrupt configuration of the available events (which interrupts are enabled/disabled).

The **ERM_DRV_GetErrorDetail()** shall be used to get the address of the last ECC event in Memory n and ECC event.

The **ERM_DRV_ClearEvent()** shall be used to clear both the record of an event and the corresponding interrupt notification.

This is example code to configure the ERM driver:

```
/* Device instance number */
#define INST_ERM1 (0U)

/* 1.1 With instance for S32K14x: */
/* The number of configured channel(s) */
#define ERM_NUM_OF_CFG_CHANNEL (2U)

/* Interrupt configuration 0 */
const erm_interrupt_config_t erm1_interrupt0 =
{
    .enableSingleCorrection = false,
    .enableNonCorrectable   = true
};

/* Interrupt configuration 1 */
const erm_interrupt_config_t erm1_interrupt1 =
{
    .enableSingleCorrection = true,
    .enableNonCorrectable   = true
};

/* User configuration */
const erm_user_config_t erm1_InitConfig[] =
{
    /* Channel 0U */
    {
        .channel      = 0U,
        .interruptCfg = &erm1_interrupt0
    },

    /* Channel 1U */
    {
        .channel      = 1U,
        .interruptCfg = &erm1_interrupt1
    }
};

/* 1.2 With instance for S32K11x: */
/* The number of configured channel(s) */
#define ERM_NUM_OF_CFG_CHANNEL (1U)
```

```

/* Interrupt configuration 0 */
const erm_interrupt_config_t erm1_interrupt0 =
{
    .enableSingleCorrection = false,
    .enableNonCorrectable   = true
};

/* User configuration */
const erm_user_config_t erm1_InitConfig[] =
{
    /* Channel 0U */
    {
        .channel      = 0U,
        .interruptCfg = &erm1_interrupt0
    }
};

int main()
{
    /* Initializes the ERM module */
    ERM_DRV_Init(INST_ERM1, ERM_NUM_OF_CFG_CHANNEL, erm1_InitConfig);
    ...
    /* De-Initializes the ERM module */
    ERM_DRV_Deinit(INST_ERM1);
    ...
    return 0;
}

/* Interrupt handler */
/* Interrupt handler for single bit */
void ERM_single_fault_IRQHandler()
{
    /* Clears the event for channel 1 */
    ERM_DRV_ClearEvent(INST_ERM1, 1U, ERM_EVENT_SINGLE_BIT);
    ...
}

/* Interrupt handler for non correctable */
void ERM_double_fault_IRQHandler()
{
    /* Clears the event for channel 0 */
    ERM_DRV_ClearEvent(INST_ERM1, 0U,
        ERM_EVENT_NON_CORRECTABLE);
    /* Clears the event for channel 1 */
    ERM_DRV_ClearEvent(INST_ERM1, 1U,
        ERM_EVENT_NON_CORRECTABLE);
    ...
}

```

Data Structures

- struct [erm_interrupt_config_t](#)
ERM interrupt notification configuration structure Implements : [erm_interrupt_config_t_Class](#). [More...](#)
- struct [erm_user_config_t](#)
ERM user configuration structure Implements : [erm_user_config_t_Class](#). [More...](#)

Enumerations

- enum [erm_ecc_event_t](#) { [ERM_EVENT_NONE](#) = 0U, [ERM_EVENT_SINGLE_BIT](#) = 1U, [ERM_EVENT_NON_CORRECTABLE](#) = 2U }
- ERM types of ECC events Implements : [erm_ecc_event_t_Class](#).

ERM DRIVER API

- void [ERM_DRV_Init](#) (uint32_t instance, uint8_t channelCnt, const [erm_user_config_t](#) *userConfigArr)
Initializes the ERM module.
- void [ERM_DRV_Deinit](#) (uint32_t instance)
Sets the default configuration.
- void [ERM_DRV_SetInterruptConfig](#) (uint32_t instance, uint8_t channel, [erm_interrupt_config_t](#) interruptCfg)

Sets interrupt notification.

- void [ERM_DRV_GetInterruptConfig](#) (uint32_t instance, uint8_t channel, [erm_interrupt_config_t](#) *const interruptPtr)

Gets interrupt notification.

- void [ERM_DRV_ClearEvent](#) (uint32_t instance, uint8_t channel, [erm_ecc_event_t](#) eccEvent)

Clears error event and the corresponding interrupt notification.

- [erm_ecc_event_t](#) [ERM_DRV_GetErrorDetail](#) (uint32_t instance, uint8_t channel, uint32_t *addressPtr)

Gets the address of the last ECC event in Memory n and ECC event.

17.43.4 Data Structure Documentation

17.43.4.1 struct [erm_interrupt_config_t](#)

ERM interrupt notification configuration structure Implements : [erm_interrupt_config_t_Class](#).

Definition at line 53 of file [erm_driver.h](#).

Data Fields

- bool [enableSingleCorrection](#)
- bool [enableNonCorrectable](#)

Field Documentation

17.43.4.1.1 bool [enableNonCorrectable](#)

Enable Non-Correctable Interrupt Notification

Definition at line 56 of file [erm_driver.h](#).

17.43.4.1.2 bool [enableSingleCorrection](#)

Enable Single Correction Interrupt Notification

Definition at line 55 of file [erm_driver.h](#).

17.43.4.2 struct [erm_user_config_t](#)

ERM user configuration structure Implements : [erm_user_config_t_Class](#).

Definition at line 63 of file [erm_driver.h](#).

Data Fields

- uint8_t [channel](#)
- const [erm_interrupt_config_t](#) * [interruptCfg](#)

Field Documentation

17.43.4.2.1 uint8_t [channel](#)

The channel assignments

Definition at line 65 of file [erm_driver.h](#).

17.43.4.2.2 const [erm_interrupt_config_t](#)* [interruptCfg](#)

Interrupt configuration

Definition at line 66 of file [erm_driver.h](#).

17.43.5 Enumeration Type Documentation

17.43.5.1 enum erm_ecc_event_t

ERM types of ECC events Implements : erm_ecc_event_t_Class.

Enumerator

ERM_EVENT_NONE None events

ERM_EVENT_SINGLE_BIT Single-bit correction ECC events

ERM_EVENT_NON_CORRECTABLE Non-correctable ECC events

Definition at line 42 of file erm_driver.h.

17.43.6 Function Documentation

17.43.6.1 void ERM_DRV_ClearEvent (uint32_t instance, uint8_t channel, erm_ecc_event_t eccEvent)

Clears error event and the corresponding interrupt notification.

This function clears the record of an event. If the corresponding interrupt is enabled, the interrupt notification will be cleared

Parameters

in	instance	The ERM instance number
in	channel	The configured memory channel
in	eccEvent	The types of ECC events

Definition at line 142 of file erm_driver.c.

17.43.6.2 void ERM_DRV_Deinit (uint32_t instance)

Sets the default configuration.

This function sets the default configuration

Parameters

in	instance	The ERM instance number
----	----------	-------------------------

Definition at line 82 of file erm_driver.c.

17.43.6.3 erm_ecc_event_t ERM_DRV_GetErrorDetail (uint32_t instance, uint8_t channel, uint32_t * addressPtr)

Gets the address of the last ECC event in Memory n and ECC event.

This function gets the address of the last ECC event in Memory n and the types of the event

Parameters

in	instance	The ERM instance number
in	channel	The examined memory channel
out	addressPtr	The pointer to address of the last ECC event in Memory n with ECC event

Returns

The last occurred ECC event

Definition at line 174 of file erm_driver.c.

17.43.6.4 void ERM_DRV_GetInterruptConfig (uint32_t *instance*, uint8_t *channel*, erm_interrupt_config_t *const *interruptPtr*)

Gets interrupt notification.

This function gets the current interrupt configuration of the available events (which interrupts are enabled/disabled)

Parameters

in	<i>instance</i>	The ERM instance number
in	<i>channel</i>	The examined memory channel
out	<i>interruptPtr</i>	The pointer to the ERM interrupt configuration structure

Definition at line 120 of file erm_driver.c.

17.43.6.5 void ERM_DRV_Init (uint32_t *instance*, uint8_t *channelCnt*, const erm_user_config_t * *userConfigArr*)

Initializes the ERM module.

This function initializes ERM driver based on user configuration input, channelCnt takes values between 1 and the maximum channel count supported by the hardware

Parameters

in	<i>instance</i>	The ERM instance number
in	<i>channelCnt</i>	The number of channels
in	<i>userConfigArr</i>	The pointer to the array of ERM user configure structure

Definition at line 54 of file erm_driver.c.

17.43.6.6 void ERM_DRV_SetInterruptConfig (uint32_t *instance*, uint8_t *channel*, erm_interrupt_config_t *interruptCfg*)

Sets interrupt notification.

This function sets interrupt notification based on interrupt notification configuration input

Parameters

in	<i>instance</i>	The ERM instance number
in	<i>channel</i>	The configured memory channel
in	<i>interruptCfg</i>	The ERM interrupt configuration structure

Definition at line 99 of file erm_driver.c.

17.44 EWM Driver

17.44.1 Detailed Description

External Watchdog Monitor Peripheral Driver.

Hardware background

Features:

- Independent LPO clock source
- Programmable time-out period specified in terms of number of EWM LPO clock cycles.
- Windowed refresh option
 - Provides robust check that program flow is faster than expected.
 - Programmable window.
 - Refresh outside window leads to assertion of **EWM_out**.
- Robust refresh mechanism
 - Write values of **0xB4** and **0x2C** to EWM Refresh Register within 15 (**EWM_service_time**) peripheral bus clock cycles.
- One output port, **EWM_out**, when asserted is used to reset or place the external circuit into safe mode
- One Input port, **EWM_in**, allows an external circuit to control the **EWM_out** signal.

The EWM can be initialized only once as all the configuration registers are write once per reset

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
* ${S32SDK_PATH}\platform\drivers\src\ewm\ewm_driver.c
*
```

Include path

The following paths need to be added to the include path of the toolchain:

```
* ${S32SDK_PATH}\platform\drivers\inc\
*
```

Compile symbols

No special symbols are required for this component

Dependencies

No special dependencies are required for this component

Clocking and pin configuration

The EWM Driver does not handle clock setup (from PCC) or any kind of pin configuration (done by PORT module). This is handled by the Clock Manager and PORT module, respectively. The driver assumes that correct clock configurations have been made, so it is the user's responsibility to set up clocking and pin configurations correctly.

Interrupts

The EWM module can generate interrupts, if enabled on `EWM_DRV_Init()` but they are not handled by the driver. The EWM shares the interrupt vector with the Watchdog Timer. The following code snippet is an example of how enable the interrupt and assign a handler:

```
/* EWM and watchdog interrupt service routine */
void EWM_Watchdog_ISR()
{
    /* Do something(e.g perform a clean reset) */
    ...
}

int main()
{
    /* Init clocks, pins, other modules */
    ...
    /* Install interrupt handler for EWM and Watchdog */
    INT_SYS_InstallHandler(WDOG_EWM_IRQn, &EWM_Watchdog_ISR, (
        isr_t *)0);
    /* Enable the interrupt */
    INT_SYS_EnableIRQ(WDOG_EWM_IRQn);

    /* Init EWM */
    ...
    /* Infinite loop*/
    while(1)
    {
        /* Do something until the counter needs to be refreshed */
        ...
        /* Refresh the counter */
        EWM_DRV_Refresh(EWM_INSTANCE);
    }
}
```

Using the EWM driver in your application

```
/* Declare the EWM instance you want to use */
#define EWM_INSTANCE    OUL

int main()
{
    /* Declare the EWM configuration structure */
    ewm_init_config_t ewmConfig;
    /* Variable where to store the init status */
    status_t ewmStatus;
    /* Init clocks, pins, other modules */
    ...

    /* Get the default configuration values */
    EWM_DRV_GetDefaultConfig(&ewmConfig);
    /* Init the module instance */
    ewmStatus = EWM_DRV_Init(EWM_INSTANCE, &ewmConfig);

    /* Infinite loop*/
    while(1)
    {
        /* Do something until the counter needs to be refreshed */
        ...
        /* Refresh the counter */
        EWM_DRV_Refresh(EWM_INSTANCE);
    }
}
```

Data Structures

- struct `ewm_init_config_t`

*EWM configuration structure This structure is used to configure the EWM prescaler, window, interrupt and input pin.
More...*

Enumerations

- enum `ewm_in_assert_logic_t` { `EWM_IN_ASSERT_DISABLED` = 0x00U, `EWM_IN_ASSERT_ON_LOGIC_ZERO` = 0x01U, `EWM_IN_ASSERT_ON_LOGIC_ONE` = 0x02U }

EWM input pin configuration Configures if the input pin is enabled and when is asserted Implements : ewm_in_assert_logic_t Class.

EWM Driver API

- status_t [EWM_DRV_Init](#) (uint32_t instance, const [ewm_init_config_t](#) *config)
Init EWM. This method initializes EWM instance to the configuration from the passed structure. The user must make sure that the clock is enabled. This is the only method needed to be called to start the module.
- void [EWM_DRV_GetDefaultConfig](#) ([ewm_init_config_t](#) *config)
Init configuration structure to default values.
- void [EWM_DRV_Refresh](#) (uint32_t instance)
Refresh EWM. This method needs to be called within the window period specified by the Compare Low and Compare High registers.
- [ewm_in_assert_logic_t](#) [EWM_DRV_GetInputPinAssertLogic](#) (uint32_t instance)
Get the Input pin assert logic.

17.44.2 Data Structure Documentation

17.44.2.1 struct [ewm_init_config_t](#)

EWM configuration structure This structure is used to configure the EWM prescaler, window, interrupt and input pin.

Implements : [ewm_init_config_t_Class](#)

Definition at line 54 of file [ewm_driver.h](#).

Data Fields

- [ewm_in_assert_logic_t](#) [assertLogic](#)
- bool [interruptEnable](#)
- uint8_t [prescaler](#)
- uint8_t [compareLow](#)
- uint8_t [compareHigh](#)

Field Documentation

17.44.2.1.1 [ewm_in_assert_logic_t](#) [assertLogic](#)

Assert logic for EWM input pin

Definition at line 56 of file [ewm_driver.h](#).

17.44.2.1.2 uint8_t [compareHigh](#)

Compare high value

Definition at line 60 of file [ewm_driver.h](#).

17.44.2.1.3 uint8_t [compareLow](#)

Compare low value

Definition at line 59 of file [ewm_driver.h](#).

17.44.2.1.4 bool [interruptEnable](#)

Enable EWM interrupt

Definition at line 57 of file [ewm_driver.h](#).

17.44.2.1.5 uint8_t [prescaler](#)

EWM clock prescaler

Definition at line 58 of file [ewm_driver.h](#).

17.44.3 Enumeration Type Documentation

17.44.3.1 enum ewm_in_assert_logic_t

EWM input pin configuration Configures if the input pin is enabled and when is asserted Implements : ewm_in_assert_logic_t_Class.

Enumerator

- EWM_IN_ASSERT_DISABLED** Input pin disabled
EWM_IN_ASSERT_ON_LOGIC_ZERO Input pin asserts EWM when on logic 0
EWM_IN_ASSERT_ON_LOGIC_ONE Input pin asserts EWM when on logic 1

Definition at line 40 of file ewm_driver.h.

17.44.4 Function Documentation

17.44.4.1 void EWM_DRV_GetDefaultConfig (ewm_init_config_t * config)

Init configuration structure to default values.

Parameters

out	config	Pointer to the configuration structure to initialize
-----	--------	--

Returns

None

Definition at line 128 of file ewm_driver.c.

17.44.4.2 ewm_in_assert_logic_t EWM_DRV_GetInputPinAssertLogic (uint32_t instance)

Get the Input pin assert logic.

Parameters

in	instance	EWM instance number
----	----------	---------------------

Returns

The input pin assert logic:

- EWM_IN_ASSERT_DISABLED - EWM in disabled
- EWM_IN_ASSERT_ON_LOGIC_ZERO - EWM is asserted when EWM_in is logic 0
- EWM_IN_ASSERT_ON_LOGIC_ONE - EWM is asserted when EWM_in is logic 1

Definition at line 172 of file ewm_driver.c.

17.44.4.3 status_t EWM_DRV_Init (uint32_t instance, const ewm_init_config_t * config)

Init EWM. This method initializes EWM instance to the configuration from the passed structure. The user must make sure that the clock is enabled. This is the only method needed to be called to start the module.

Example configuration structure:

```
1 ewm_init_config_t ewmUserCfg = {
2     .assertLogic      = EWM_IN_ASSERT_ON_LOGIC_ZERO,
3     .interruptEnable   = true,
4     .prescaler        = 128,
5     .compareLow       = 0,
6     .compareHigh      = 254
7 };
```

This configuration will enable the peripheral, with input pin configured to assert on logic low, interrupt enabled, prescaler 128 and maximum refresh window.

The EWM can be initialized only once per CPU reset as the registers are write once.

Parameters

<i>in</i>	<i>instance</i>	EWM instance number
<i>in</i>	<i>config</i>	Pointer to the module configuration structure.

Returns

`status_t` Will return the status of the operation:

- `STATUS_SUCCESS` if the operation is successful
- `STATUS_ERROR` if the windows values are not correct or if the instance is already enabled

Definition at line 60 of file `ewm_driver.c`.

17.44.4.4 void EWM_DRV_Refresh (uint32_t *instance*)

Refresh EWM. This method needs to be called within the window period specified by the Compare Low and Compare High registers.

Parameters

<i>in</i>	<i>instance</i>	EWM instance number
-----------	-----------------	---------------------

Returns

None

Definition at line 150 of file `ewm_driver.c`.

17.45 Enhanced Direct Memory Access (eDMA)

17.45.1 Detailed Description

The S32 SDK provides Peripheral Driver for the Enhanced Direct Memory Access (eDMA) module.

The direct memory access engine features are used for performing complex data transfers with minimal intervention from the host processor. These sections describe the S32 SDK software modules API that can be used for initializing, configuring and triggering eDMA transfers.

Modules

- [EDMA Driver](#)

This module covers the functionality of the Enhanced Direct Memory Access (eDMA) peripheral driver.

17.46 Error Injection Module (EIM)

17.46.1 Detailed Description

The S32 SDK provides Peripheral Drivers for the Error Injection Module (EIM) of S32 MCU.

The Error Injection Module (EIM) is mainly used for diagnostic purposes. It provides a method for diagnostic coverage of the peripheral memories and offers support for inducing single-bit and multi-bit inversions on read data when accessing peripheral RAMs.

Injecting faults on memory accesses can be used to exercise the SEC-DED ECC function of the related system. Each EIM channel *n* corresponds to a source of potential memory error events.

The following table shows the channel assignments of the module:

EIM channel <i>n</i>	S32K14x	S32↔ K14xW	S32K11x	S32Rx7x	MP↔ C5746R	MP↔ C5777C	S32V23x
0	SRAM_L	SRAM_L	SRAM_U	DMA TCD RAM	DMA TCD RAM	PRAMC↔ _0	Cortex-M4 TCM upper (bits31-0)
1	SRAM_U	SRAM_U	Reserved	Reserved	Reserved	PRAMC↔ _1	Cortex-M4 TCM upper (bits63-32)
2	Reserved	Reserved	Reserved	Reserved	Reserved	FEC MIB	Cortex-M4 TCM lower (bits31-0)
3	Reserved	Reserved	Reserved	Reserved	Reserved	FEC RIF	Cortex-M4 TCM lower (bits63-32)
4	Reserved	Reserved	Reserved	Reserved	Reserved	eDMA_0 TCD RAM	Cortex-M4 Code Cache Tag Way0
5	Reserved	Reserved	Reserved	Reserved	Reserved	eDMA_1 TCD RAM	Cortex-M4 Code Cache Tag Way1
6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Cortex-M4 Code Cache Data Way0
7	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Cortex-M4 Code Cache Data Way1
8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Cortex-M4 System Cache Tag Way0
9	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Cortex-M4 System Cache Tag Way1

10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Cortex-M4 System Cache Data Way0
11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Cortex-M4 System Cache Data Way1
12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DMA TCD RAM

/*!

Integration guideline

Compilation units

The following files need to be compiled in the project:

```

${S32SDK_PATH}\platform\drivers\src\eim\eim_driver.c
${S32SDK_PATH}\platform\drivers\src\eim\eim_hw_access.c

```

Include path

The following paths need to be added to the include path of the toolchain:

```

${S32SDK_PATH}\platform\drivers\inc\

```

Compile symbols

No special symbols are required for this component

Dependencies

No special dependencies are required for this component

Modules

- [EIM Driver](#)

Error Injection Module Peripheral Driver.

EIM PD provides a set of high-level APIs/services to configure the Error Injection Module (EIM) module.

17.47 Error Reporting Module (ERM)

17.47.1 Detailed Description

The S32 SDK provides Peripheral Drivers for the Error Reporting Module (ERM) module of S32 SDK devices.

The Error Reporting Module (ERM) provides information and optional interrupt notification on memory errors events associated with ECC (Error Correction Code).

The ERM includes the following features:

- Capture of address information on single-bit correction and non-correctable ECC events.
- Optional interrupt notification on captured ECC events.
- Support for ECC event capturing for memory sources, with individual reporting fields and interrupt configuration per memory channel.

Each ERM channel *n* corresponds to a source of potential memory error events. The following table shows the channel assignments:

ERM channel <i>n</i>	S32K14x	S32K14xW	S32K11x	MPC5777C	S32V23x
0	SRAM_L	SRAM_L	SRAM_U	PRAMC_0	Cortex-M4 TCM upper
1	SRAM_U	SRAM_U	Reserved	PRAMC_1	Cortex-M4 TCM lower
2	Reserved	Reserved	Reserved	eDMA_0 TCD RAM	Cortex-M4 Code Cache Tag
3	Reserved	Reserved	Reserved	eDMA_1 TCD RAM	Cortex-M4 Code Cache Data
4	Reserved	Reserved	Reserved	FEC MIB	Cortex-M4 System Cache Tag
5	Reserved	Reserved	Reserved	FEC RIF	Cortex-M4 System Cache Data
6	Reserved	Reserved	Reserved	PFLASH port 0	DMA TCD RAM
7	Reserved	Reserved	Reserved	PFLASH port 1	Reserved
8	Reserved	Reserved	Reserved	AIPS_0	Reserved
9	Reserved	Reserved	Reserved	AIPS_1	Reserved
10	Reserved	Reserved	Reserved	FEC e2eECC	Reserved
11	Reserved	Reserved	Reserved	CSE	Reserved
12	Reserved	Reserved	Reserved	SIPI	Reserved
13	Reserved	Reserved	Reserved	Core0 instruction	Reserved
14	Reserved	Reserved	Reserved	Core0 data	Reserved
15	Reserved	Reserved	Reserved	Core1 instruction	Reserved
16	Reserved	Reserved	Reserved	Core1 data	Reserved
17	Reserved	Reserved	Reserved	eDMA_0 e2eECC	Reserved

18	Reserved	Reserved	Reserved	eDMA_1 e2eECC	Reserved
19	Reserved	Reserved	Reserved	EBI e2eECC	Reserved

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\erm\erm_driver.c  
${S32SDK_PATH}\platform\drivers\src\erm\erm_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

No special dependencies are required for this component

Modules

- [ERM Driver](#)
Error Reporting Module Peripheral Driver.

17.48 Ethernet MAC (ENET)

17.48.1 Detailed Description

The S32 SDK provides a peripheral driver for the Ethernet MAC (ENET) module of S32 SDK devices.

The core implements a dual-speed 10/100-Mbit/s (some platforms might also support 1000Mbit/s) Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full-duplex 10/100-Mbit/s Ethernet LANs (and full-duplex gigabit for some platforms).

The MAC operation is fully programmable and can be used in Network Interface Card (NIC), bridging, or switching applications. The core implements the remote network monitoring (RMON) counters according to IETF RFC 2819.

The core also implements a hardware acceleration block to optimize the performance of network controllers providing TCP/IP, UDP, and ICMP protocol services. The acceleration block performs critical functions in hardware, which are typically implemented with large software overhead.

The core implements programmable embedded FIFOs that can provide buffering on the receive path for lossless flow control.

Advanced power management features are available with magic packet detection and programmable power-down modes.

A unified DMA (uDMA), internal to the ENET module, optimizes data transfer between the ENET core and the SoC, and supports an enhanced buffer descriptor programming model to support IEEE 1588 functionality.

The programmable Ethernet MAC with IEEE 1588 integrates a standard IEEE 802.3 Ethernet MAC with a time-stamping module. The IEEE 1588 standard provides accurate clock synchronization for distributed control nodes for industrial automation applications.

Hardware background

Features of the ENET module include:

- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking
- Supports zero-length preamble
- Dynamically configurable to support 10/100-Mbit/s operation
- Supports 10/100 Mbit/s full-duplex and configurable half-duplex operation
- Compliant with the AMD magic packet detection with interrupt for node remote power management
- Seamless interface to commercial ethernet PHY devices via one of the following:
 - 4-bit Media Independent Interface (MII) operating at 2.5/25 MHz.
 - 4-bit non-standard MII-Lite (MII without the CRS and COL signals) operating at 2.5/25 MHz.
 - 2-bit Reduced MII (RMII) operating at 50 MHz.
- Simple 64-Bit FIFO user-application interface
- CRC-32 checking at full speed with optional forwarding of the frame check sequence (FCS) field to the client
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- In full-duplex mode:
 - Implements automated pause frame (802.3 x31A) generation and termination, providing flow control without user application intervention
 - Pause quanta used to form pause frames — dynamically programmable
 - Pause frame generation additionally controllable by user application offering flexible traffic flow control

- Optional forwarding of received pause frames to the user application
- Implements standard flow-control mechanism
- In half-duplex mode: provides full collision support, including jamming, backoff, and automatic retransmission
- Supports VLAN-tagged frames according to IEEE 802.1Q
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (except broadcast and pause frames)
- Programmable promiscuous mode support to omit MAC destination address checking on receive
- Multicast and unicast address filtering on receive based on 64-entry hash table, reducing higher layer processing load
- Programmable frame maximum length providing support for any standard or proprietary frame length
- Statistics indicators for frame traffic and errors (alignment, CRC, length) and pause frames providing for IEEE 802.3 basic and mandatory management information database (MIB) package and remote network monitoring (RFC 2819)
- Simple handshake user application FIFO interface with fully programmable depth and threshold levels
- Provides separate status word for each received frame on the user interface providing information such as frame length, frame type, VLAN tag, and error information
- Multiple internal loopback options
- MDIO master interface for PHY device configuration and management
- Supports legacy FEC buffer descriptors

IP protocol performance optimization features:

- Operates on TCP/IP and UDP/IP and ICMP/IP protocol data or IP header only
- Enables wire-speed processing
- Supports IPv4 and IPv6
- Transparent passing of frames of other types and protocols
- Supports VLAN tagged frames according to IEEE 802.1Q with transparent forwarding of VLAN tag and control field
- Automatic IP-header and payload (protocol specific) checksum calculation and verification on receive
- Automatic IP-header and payload (protocol specific) checksum generation and automatic insertion on transmit configurable on a per-frame basis
- Supports IP and TCP, UDP, ICMP data for checksum generation and checking
- Supports full header options for IPv4 and TCP protocol headers
- Provides IPv6 support to datagrams with base header only — datagrams with extension headers are passed transparently unmodified/unchecked
- Provides statistics information for received IP and protocol errors
- Configurable automatic discard of erroneous frames
- Configurable automatic host-to-network (RX) and network-to-host (TX) byte order conversion for IP and TCP/UDP/ICMP headers within the frame
- Configurable padding remove for short IP datagrams on receive
- Configurable Ethernet payload alignment to allow for 32-bit word-aligned header and payload processing

- Programmable store-and-forward operation with clock and rate decoupling FIFOs

Platform-dependent features (not be available on some platforms, see chip-specific ENET information for details):

- Gigabit full-duplex operation (actual throughput is greater than 100 Mbit/s but significantly less than 1000 Mbit/s)
- Interrupt coalescing reduces the number of interrupts generated by the MAC, reducing CPU loading
- Traffic-shaping bandwidth distribution supports credit-based and round-robin-based policies. Either policy can be combined with time-based shaping.
- AVB (Audio Video Bridging, IEEE 802.1Qav) features:
 - Credit-based bandwidth distribution policy can be combined with time-basedshaping
 - AVB endpoint talker and listener support
 - Support for arbitration between different priority traffic (for example, AVB class A, AVB class B, and non-AVB)
- Receive frame parser enables flexible Ethernet frame pattern matching in order to finally accept or reject a frame.

Modules

- [ENET Driver](#)

17.49 Ethernet Transceiver (PHY)

17.49.1 Detailed Description

The S32 SDK provides a peripheral driver for some of the Ethernet Transceivers on the supported devices.

Hardware background

One of the devices supported by the current framework is TJA1100. The TJA1100 is a 100BASE-T1 compliant Ethernet PHY optimized for automotive use cases. The device provides 100 Mbit/s transmit and receive capability over a single Unshielded Twisted Pair (UTP) cable, supporting a cable length of up to at least 15 m. Optimized for automotive use cases such as IP camera links, driver assistance systems and back-bone networks, the TJA1100 has been designed to minimize power consumption and system costs, while still providing the robustness required for automotive use cases.

Modules

- [PHY Framework](#)

PHY Driver containing API for operating PHYs managed in the PHY framework.

17.50 External Watchdog Monitor (EWM)

17.50.1 Detailed Description

The S32 SDK provides the Peripheral Drivers for the External Watchdog Monitor (EWM) module of S32K devices.

For safety, a redundant watchdog system, External Watchdog Monitor (EWM), is designed to monitor external circuits, as well as the MCU software flow. This provides a back-up mechanism to the internal watchdog that resets the MCU's CPU and peripherals.

The EWM differs from the internal watchdog in that it does not reset the MCU's CPU and peripherals. The EWM if allowed to time-out, provides an independent EWM_out pin that when asserted resets or places an external circuit into a safe mode. The CPU resets the EWM counter that is logically ANDed with an external digital input pin. This pin allows an external circuit to influence the reset_out signal.

Modules

- [EWM Driver](#)

External Watchdog Monitor Peripheral Driver.

17.51 Flash Memory (Flash)

17.51.1 Detailed Description

This section describes the programming interface of the Flash Peripheral Driver.

Data Structures

- struct `flash_user_config_t`
Flash User Configuration Structure. [More...](#)
- struct `flash_ssd_config_t`
Flash SSD Configuration Structure. [More...](#)
- struct `flash_eeprom_status_t`
EEPROM status structure. [More...](#)

Macros

- #define `CLEAR_FTFx_FSTAT_ERROR_BITS` `FTFx_FSTAT = (uint8_t)(FTFx_FSTAT_FPVIOL_MASK | FTFx_FSTAT_ACCERR_MASK | FTFx_FSTAT_RDCOLERR_MASK)`
- #define `FTFx_WORD_SIZE` `0x0002U`
- #define `FTFx_LONGWORD_SIZE` `0x0004U`
- #define `FTFx_PHRASE_SIZE` `0x0008U`
- #define `FTFx_DPHRASE_SIZE` `0x0010U`
- #define `FTFx_RSRC_CODE_REG` `FTFx_FCCOB8`
- #define `FTFx_VERIFY_BLOCK` `0x00U`
- #define `FTFx_VERIFY_SECTION` `0x01U`
- #define `FTFx_PROGRAM_CHECK` `0x02U`
- #define `FTFx_READ_RESOURCE` `0x03U`
- #define `FTFx_PROGRAM_LONGWORD` `0x06U`
- #define `FTFx_PROGRAM_PHRASE` `0x07U`
- #define `FTFx_ERASE_BLOCK` `0x08U`
- #define `FTFx_ERASE_SECTOR` `0x09U`
- #define `FTFx_PROGRAM_SECTION` `0x0BU`
- #define `FTFx_VERIFY_ALL_BLOCK` `0x40U`
- #define `FTFx_READ_ONCE` `0x41U`
- #define `FTFx_PROGRAM_ONCE` `0x43U`
- #define `FTFx_ERASE_ALL_BLOCK` `0x44U`
- #define `FTFx_SECURITY_BY_PASS` `0x45U`
- #define `FTFx_PFLASH_SWAP` `0x46U`
- #define `FTFx_ERASE_ALL_BLOCK_UNSECURE` `0x49U`
- #define `FTFx_PROGRAM_PARTITION` `0x80U`
- #define `FTFx_SET_EERAM` `0x81U`
- #define `RESUME_WAIT_CNT` `0x20U`
Resume wait count used in FLASH_DRV_EraseResume function.
- #define `SUSPEND_WAIT_CNT` `0x40U`
Suspend wait count used in FLASH_DRV_EraseSuspend function.
- #define `DFLASH_IFR_READRESOURCE_ADDRESS` `0x8000FCU`
- #define `GET_BIT_0_7(value)` `((uint8_t)((((uint32_t)(value)) & 0xFFU))`
- #define `GET_BIT_8_15(value)` `((uint8_t)((((uint32_t)(value)) >> 8) & 0xFFU))`
- #define `GET_BIT_16_23(value)` `((uint8_t)((((uint32_t)(value)) >> 16) & 0xFFU))`
- #define `GET_BIT_24_31(value)` `((uint8_t)((((uint32_t)(value)) >> 24))`
- #define `FLASH_SECURITY_STATE_KEYEN` `0x80U`
- #define `FLASH_SECURITY_STATE_UNSECURED` `0x02U`

- #define `CSE_KEY_SIZE_CODE_MAX` 0x03U
- #define `FTFx_FSTAT_ERROR_BITS` (FTFx_FSTAT & (FTFx_FSTAT_MGSTAT0_MASK | FTFx_FSTAT_FPVIO↵
_MASK | FTFx_FSTAT_ACCERR_MASK | FTFx_FSTAT_RDCOLERR_MASK))
- #define `FLASH_CALLBACK_CS` 0x0AU

Callback period count for FlashChecksum.

Typedefs

- typedef void(* `flash_callback_t`) (void)

Call back function pointer data type.

Enumerations

- enum `flash_flexRam_function_control_code_t` {
 `EEE_ENABLE` = 0x00U, `EEE_QUICK_WRITE` = 0x55U, `EEE_STATUS_QUERY` = 0x77U, `EEE_COMPL↵
ETE_INTERRUPT_QUICK_WRITE` = 0xAAU,
 `EEE_DISABLE` = 0xFFU }

FlexRAM Function control Code.

Variables

- uint32_t `PFlashBase`
- uint32_t `PFlashSize`
- uint32_t `DFlashBase`
- uint32_t `EERAMBase`
- `flash_callback_t` `CallBack`
- uint32_t `PFlashBase`
- uint32_t `PFlashSize`
- uint32_t `DFlashBase`
- uint32_t `DFlashSize`
- uint32_t `EERAMBase`
- uint32_t `EEESize`
- `flash_callback_t` `CallBack`
- uint8_t `brownOutCode`
- uint16_t `numOfRecordReqMaintain`
- uint16_t `sectorEraseCount`

PFlash swap control codes

- #define `FTFx_SWAP_SET_INDICATOR_ADDR` 0x01U
Initialize Swap System control code.
- #define `FTFx_SWAP_SET_IN_PREPARE` 0x02U
Set Swap in Update State.
- #define `FTFx_SWAP_SET_IN_COMPLETE` 0x04U
Set Swap in Complete State.
- #define `FTFx_SWAP_REPORT_STATUS` 0x08U

Report Swap Status.

PFlash swap states

- #define `FTFx_SWAP_UNINIT` 0x00U
Uninitialized swap mode.
- #define `FTFx_SWAP_READY` 0x01U
Ready swap mode.
- #define `FTFx_SWAP_UPDATE` 0x02U
Update swap mode.
- #define `FTFx_SWAP_UPDATE_ERASED` 0x03U
Update-Erased swap mode.
- #define `FTFx_SWAP_COMPLETE` 0x04U
Complete swap mode.

Flash security status

- #define `FLASH_NOT_SECURE` 0x01U
Flash currently not in secure state.
- #define `FLASH_SECURE_BACKDOOR_ENABLED` 0x02U
Flash is secured and backdoor key access enabled.
- #define `FLASH_SECURE_BACKDOOR_DISABLED` 0x04U
Flash is secured and backdoor key access disabled.

Null Callback function definition

- #define `NULL_CALLBACK` ((flash_callback_t)0xFFFFFFFFU)
Null callback.

Flash driver APIs

- status_t `FLASH_DRV_Init` (const flash_user_config_t *const pUserConf, flash_ssd_config_t *const pSSDConfig)
Initializes Flash.
- void `FLASH_DRV_GetPFlashProtection` (uint32_t *protectStatus)
P-Flash get protection.
- status_t `FLASH_DRV_SetPFlashProtection` (uint32_t protectStatus)
P-Flash set protection.
- void `FLASH_DRV_GetSecurityState` (uint8_t *securityState)
Flash get security state.
- status_t `FLASH_DRV_SecurityBypass` (const flash_ssd_config_t *pSSDConfig, const uint8_t *keyBuffer)
Flash security bypass.
- status_t `FLASH_DRV_EraseAllBlock` (const flash_ssd_config_t *pSSDConfig)
Flash erase all blocks.
- status_t `FLASH_DRV_VerifyAllBlock` (const flash_ssd_config_t *pSSDConfig, uint8_t marginLevel)
Flash verify all blocks.
- status_t `FLASH_DRV_EraseSector` (const flash_ssd_config_t *pSSDConfig, uint32_t dest, uint32_t size)
Flash erase sector.
- status_t `FLASH_DRV_VerifySection` (const flash_ssd_config_t *pSSDConfig, uint32_t dest, uint16_t number, uint8_t marginLevel)
Flash verify section.
- void `FLASH_DRV_EraseSuspend` (void)
Flash erase suspend.

- void [FLASH_DRV_EraseResume](#) (void)
Flash erase resume.
- status_t [FLASH_DRV_ReadOnce](#) (const [flash_ssd_config_t](#) *pSSDConfig, uint8_t recordIndex, uint8_t *p←
dataArray)
Flash read once.
- status_t [FLASH_DRV_ProgramOnce](#) (const [flash_ssd_config_t](#) *pSSDConfig, uint8_t recordIndex, const
uint8_t *pDataArray)
Flash program once.
- status_t [FLASH_DRV_Program](#) (const [flash_ssd_config_t](#) *pSSDConfig, uint32_t dest, uint32_t size, const
uint8_t *pData)
Flash program.
- status_t [FLASH_DRV_ProgramCheck](#) (const [flash_ssd_config_t](#) *pSSDConfig, uint32_t dest, uint32_t size,
const uint8_t *pExpectedData, uint32_t *pFailAddr, uint8_t marginLevel)
Flash program check.
- status_t [FLASH_DRV_CheckSum](#) (const [flash_ssd_config_t](#) *pSSDConfig, uint32_t dest, uint32_t size,
uint32_t *pSum)
Calculates check sum.
- status_t [FLASH_DRV_EnableCmdCompleteInterrupt](#) (void)
Enable the command complete interrupt.
- void [FLASH_DRV_DisableCmdCompleteInterrupt](#) (void)
Disable the command complete interrupt.
- static bool [FLASH_DRV_GetCmdCompleteFlag](#) (void)
Check the command complete flag has completed or not.
- status_t [FLASH_DRV_EnableReadCollisionInterrupt](#) (void)
Enable the read collision error interrupt.
- void [FLASH_DRV_DisableReadCollisionInterrupt](#) (void)
Disable the read collision error interrupt.
- static bool [FLASH_DRV_GetReadCollisionFlag](#) (void)
Check the read collision error flag is detected or not.
- static void [FLASH_DRV_ClearReadCollisionFlag](#) (void)
Clear the read collision error flag.
- void [FLASH_DRV_GetDefaultConfig](#) ([flash_user_config_t](#) *const config)
Get default flash configuration.

17.51.2 Data Structure Documentation

17.51.2.1 struct flash_user_config_t

Flash User Configuration Structure.

Implements : [flash_user_config_t_Class](#)

Definition at line 786 of file [flash_driver.h](#).

Data Fields

- uint32_t [PFlashBase](#)
- uint32_t [PFlashSize](#)
- uint32_t [DFlashBase](#)
- uint32_t [EERAMBase](#)
- [flash_callback_t](#) [Callback](#)

17.51.2.2 struct flash_ssd_config_t

Flash SSD Configuration Structure.

The structure includes the static parameters for C90TFS/FTFx which are device-dependent. The fields including PFlashBlockBase, PFlashBlockSize, DFlashBlockBase, EERAMBlockBase, and CallBack are passed via [flash_user_config_t](#). The rest of parameters such as DFlashBlockSize, and EEERAMBlockSize will be initialized in [FLASH_DRV_Init\(\)](#) automatically.

Implements : flash_ssd_config_t_Class

Definition at line 810 of file flash_driver.h.

Data Fields

- uint32_t [PFlashBase](#)
- uint32_t [PFlashSize](#)
- uint32_t [DFlashBase](#)
- uint32_t [DFlashSize](#)
- uint32_t [EERAMBase](#)
- uint32_t [EEERAMSize](#)
- [flash_callback_t](#) CallBack

17.51.2.3 struct flash_eeprom_status_t

EEPROM status structure.

Implements : flash_eeprom_status_t_Class

Definition at line 832 of file flash_driver.h.

Data Fields

- uint8_t [brownOutCode](#)
- uint16_t [numOfRecordReqMaintain](#)
- uint16_t [sectorEraseCount](#)

17.51.3 Macro Definition Documentation

17.51.3.1 **#define CLEAR_FTFx_FSTAT_ERROR_BITS** FTFx_FSTAT = (uint8_t)(FTFx_FSTAT_FPVIOL_MASK | FTFx_FSTAT_ACCERR_MASK | FTFx_FSTAT_RDCOLERR_MASK)

Definition at line 602 of file flash_driver.h.

17.51.3.2 **#define CSE_KEY_SIZE_CODE_MAX** 0x03U

Definition at line 699 of file flash_driver.h.

17.51.3.3 **#define DFLASH_IFR_READRESOURCE_ADDRESS** 0x8000FCU

Definition at line 681 of file flash_driver.h.

17.51.3.4 **#define FLASH_CALLBACK_CS** 0x0AU

Callback period count for FlashCheckSum.

This value is only relevant for FlashCheckSum operation, where a high rate of calling back can impair performance. The rest of the flash operations invoke the callback as often as possible while waiting for the flash controller to finish the requested operation.

Definition at line 744 of file flash_driver.h.

17.51.3.5 #define FLASH_NOT_SECURE 0x01U

Flash currently not in secure state.

Definition at line 727 of file flash_driver.h.

17.51.3.6 #define FLASH_SECURE_BACKDOOR_DISABLED 0x04U

Flash is secured and backdoor key access disabled.

Definition at line 731 of file flash_driver.h.

17.51.3.7 #define FLASH_SECURE_BACKDOOR_ENABLED 0x02U

Flash is secured and backdoor key access enabled.

Definition at line 729 of file flash_driver.h.

17.51.3.8 #define FLASH_SECURITY_STATE_KEYEN 0x80U

Definition at line 690 of file flash_driver.h.

17.51.3.9 #define FLASH_SECURITY_STATE_UNSECURED 0x02U

Definition at line 691 of file flash_driver.h.

17.51.3.10 #define FTFx_DPHRASE_SIZE 0x0010U

Definition at line 611 of file flash_driver.h.

17.51.3.11 #define FTFx_ERASE_ALL_BLOCK 0x44U

Definition at line 635 of file flash_driver.h.

17.51.3.12 #define FTFx_ERASE_ALL_BLOCK_UNSECURE 0x49U

Definition at line 638 of file flash_driver.h.

17.51.3.13 #define FTFx_ERASE_BLOCK 0x08U

Definition at line 629 of file flash_driver.h.

17.51.3.14 #define FTFx_ERASE_SECTOR 0x09U

Definition at line 630 of file flash_driver.h.

17.51.3.15 #define FTFx_FSTAT_ERROR_BITS (FTFx_FSTAT & (FTFx_FSTAT_MGSTAT0_MASK | FTFx_FSTAT_FPVIOL_MASK | FTFx_FSTAT_ACCERR_MASK | FTFx_FSTAT_RDCOLERR_MASK))

Definition at line 700 of file flash_driver.h.

17.51.3.16 #define FTFx_LONGWORD_SIZE 0x0004U

Definition at line 607 of file flash_driver.h.

17.51.3.17 #define FTFx_PFLASH_SWAP 0x46U

Definition at line 637 of file flash_driver.h.

17.51.3.18 #define FTFx_PHRASE_SIZE 0x0008U

Definition at line 609 of file flash_driver.h.

17.51.3.19 **#define FTFx_PROGRAM_CHECK 0x02U**

Definition at line 625 of file flash_driver.h.

17.51.3.20 **#define FTFx_PROGRAM_LONGWORD 0x06U**

Definition at line 627 of file flash_driver.h.

17.51.3.21 **#define FTFx_PROGRAM_ONCE 0x43U**

Definition at line 634 of file flash_driver.h.

17.51.3.22 **#define FTFx_PROGRAM_PARTITION 0x80U**

Definition at line 639 of file flash_driver.h.

17.51.3.23 **#define FTFx_PROGRAM_PHRASE 0x07U**

Definition at line 628 of file flash_driver.h.

17.51.3.24 **#define FTFx_PROGRAM_SECTION 0x0BU**

Definition at line 631 of file flash_driver.h.

17.51.3.25 **#define FTFx_READ_ONCE 0x41U**

Definition at line 633 of file flash_driver.h.

17.51.3.26 **#define FTFx_READ_RESOURCE 0x03U**

Definition at line 626 of file flash_driver.h.

17.51.3.27 **#define FTFx_RSRC_CODE_REG FTFx_FCCOB8**

Definition at line 617 of file flash_driver.h.

17.51.3.28 **#define FTFx_SECURITY_BY_PASS 0x45U**

Definition at line 636 of file flash_driver.h.

17.51.3.29 **#define FTFx_SET_EERAM 0x81U**

Definition at line 640 of file flash_driver.h.

17.51.3.30 **#define FTFx_SWAP_COMPLETE 0x04U**

Complete swap mode.

Definition at line 670 of file flash_driver.h.

17.51.3.31 **#define FTFx_SWAP_READY 0x01U**

Ready swap mode.

Definition at line 664 of file flash_driver.h.

17.51.3.32 **#define FTFx_SWAP_REPORT_STATUS 0x08U**

Report Swap Status.

Definition at line 654 of file flash_driver.h.

17.51.3.33 **#define FTFx_SWAP_SET_IN_COMPLETE 0x04U**

Set Swap in Complete State.

Definition at line 652 of file flash_driver.h.

17.51.3.34 **#define FTFx_SWAP_SET_IN_PREPARE 0x02U**

Set Swap in Update State.

Definition at line 650 of file flash_driver.h.

17.51.3.35 **#define FTFx_SWAP_SET_INDICATOR_ADDR 0x01U**

Initialize Swap System control code.

Definition at line 648 of file flash_driver.h.

17.51.3.36 **#define FTFx_SWAP_UNINIT 0x00U**

Uninitialized swap mode.

Definition at line 662 of file flash_driver.h.

17.51.3.37 **#define FTFx_SWAP_UPDATE 0x02U**

Update swap mode.

Definition at line 666 of file flash_driver.h.

17.51.3.38 **#define FTFx_SWAP_UPDATE_ERASED 0x03U**

Update-Erased swap mode.

Definition at line 668 of file flash_driver.h.

17.51.3.39 **#define FTFx_VERIFY_ALL_BLOCK 0x40U**

Definition at line 632 of file flash_driver.h.

17.51.3.40 **#define FTFx_VERIFY_BLOCK 0x00U**

Definition at line 623 of file flash_driver.h.

17.51.3.41 **#define FTFx_VERIFY_SECTION 0x01U**

Definition at line 624 of file flash_driver.h.

17.51.3.42 **#define FTFx_WORD_SIZE 0x0002U**

Definition at line 605 of file flash_driver.h.

17.51.3.43 **#define GET_BIT_0_7(value) ((uint8_t)((uint32_t)(value)) & 0xFFU)**

Definition at line 684 of file flash_driver.h.

17.51.3.44 **#define GET_BIT_16_23(value) ((uint8_t)((((uint32_t)(value)) >> 16) & 0xFFU))**

Definition at line 686 of file flash_driver.h.

17.51.3.45 **#define GET_BIT_24_31(value) ((uint8_t)((((uint32_t)(value)) >> 24))**

Definition at line 687 of file flash_driver.h.

17.51.3.46 `#define GET_BIT_8_15(value) (((uint8_t)((((uint32_t)(value)) >> 8) & 0xFFU))`

Definition at line 685 of file flash_driver.h.

17.51.3.47 `#define NULL_CALLBACK ((flash_callback_t)0xFFFFFFFFU)`

Null callback.

Definition at line 755 of file flash_driver.h.

17.51.3.48 `#define RESUME_WAIT_CNT 0x20U`

Resume wait count used in FLASH_DRV_EraseResume function.

Definition at line 674 of file flash_driver.h.

17.51.3.49 `#define SUSPEND_WAIT_CNT 0x40U`

Suspend wait count used in FLASH_DRV_EraseSuspend function.

Definition at line 676 of file flash_driver.h.

17.51.4 Typedef Documentation

17.51.4.1 `typedef void(* flash_callback_t) (void)`

Call back function pointer data type.

If using callback in the application, any code reachable from this function must not be placed in a Flash block targeted for a program/erase operation. Functions can be placed in RAM section by using the START/END_FUNCTION_DEFINITION/DECLARATION_RAMSECTION macros.

Definition at line 772 of file flash_driver.h.

17.51.5 Enumeration Type Documentation

17.51.5.1 `enum flash_flexRam_function_control_code_t`

FlexRAM Function control Code.

Implements : flash_flexRAM_function_control_code_t_Class

Enumerator

EEE_ENABLE Make FlexRAM available for emulated EEPROM

EEE_QUICK_WRITE Make FlexRAM available for EEPROM quick writes

EEE_STATUS_QUERY EEPROM quick write status query

EEE_COMPLETE_INTERRUPT_QUICK_WRITE Complete interrupted EEPROM quick write process

EEE_DISABLE Make FlexRAM available as RAM

Definition at line 713 of file flash_driver.h.

17.51.6 Function Documentation

17.51.6.1 `status_t FLASH_DRV_CheckSum (const flash_ssd_config_t * pSSDConfig, uint32_t dest, uint32_t size, uint32_t * pSum)`

Calculates check sum.

This API performs 32 bit sum of each byte data over a specified Flash memory range without carry which provides rapid method for checking data integrity. The callback time period of this API is determined via FLASH_CALLBACK_CS macro in [flash_driver.h](#) which is used as a counter value for the CallBack() function calling in this API. This value can be changed as per the user requirement. User can change this value to obtain the maximum permissible callback time period. This API always returns STATUS_SUCCESS if size provided by user is zero regardless of the input validation.

Parameters

in	<i>pSSDConfig</i>	The SSD configuration structure pointer.
in	<i>dest</i>	Start address of the Flash range to be summed.
in	<i>size</i>	Size in byte of the Flash range to be summed.
in	<i>pSum</i>	To return the sum value.

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failure was occurred.

Definition at line 1041 of file flash_driver.c.

17.51.6.2 `static void FLASH_DRV_ClearReadCollisionFlag (void) [inline],[static]`

Clear the read collision error flag.

Implements : FLASH_DRV_ClearReadCollisionFlag_Activity

Definition at line 1690 of file flash_driver.h.

17.51.6.3 `void FLASH_DRV_DisableCmdCompleteInterrupt (void)`

Disable the command complete interrupt.

Definition at line 2004 of file flash_driver.c.

17.51.6.4 `void FLASH_DRV_DisableReadCollisionInterrupt (void)`

Disable the read collision error interrupt.

Definition at line 2039 of file flash_driver.c.

17.51.6.5 `status_t FLASH_DRV_EnableCmdCompleteInterrupt (void)`

Enable the command complete interrupt.

This function will enable the command complete interrupt is generated when an FTFC command completes.

Returns

operation status

- STATUS_SUCCESS: Operation was successful.

Definition at line 1986 of file flash_driver.c.

17.51.6.6 `status_t FLASH_DRV_EnableReadCollisionInterrupt (void)`

Enable the read collision error interrupt.

This function will enable the read collision error interrupt generation when an FTFC read collision error occurs.

Returns

operation status

- STATUS_SUCCESS: Operation was successful.

Definition at line 2021 of file flash_driver.c.

17.51.6.7 status_t FLASH_DRV_EraseAllBlock (const flash_ssd_config_t * pSSDConfig)

Flash erase all blocks.

This API erases all Flash memory, initializes the FlexRAM, verifies all memory contents, and then releases the MCU security.

Parameters

in	pSSDConfig	The SSD configuration structure pointer.
----	------------	--

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failure was occurred.
- STATUS_BUSY: Operation was busy.

Definition at line 461 of file flash_driver.c.

17.51.6.8 void FLASH_DRV_EraseResume (void)

Flash erase resume.

This API is used to resume a previous suspended operation of Flash erase sector command. This function must be located in RAM memory or different Flash blocks which are targeted for writing to avoid RWW error.

Definition at line 707 of file flash_driver.c.

17.51.6.9 status_t FLASH_DRV_EraseSector (const flash_ssd_config_t * pSSDConfig, uint32_t dest, uint32_t size)

Flash erase sector.

This API erases one or more sectors in P-Flash or D-Flash memory. This API always returns FTFx_OK if size provided by the user is zero regardless of the input validation.

Parameters

in	pSSDConfig	The SSD configuration structure pointer.								
in	dest	Address in the first sector to be erased. User need to make sure the dest address in of P-FLASH or D-FLASH block. This address should be aligned to bytes following a below table								
		FL↔ ASH TY↔ P↔ E/↔ M↔ CU	S32↔ K116	S32↔ K118	S32↔ K142	S32↔ K144	S32↔ K146	S32↔ K148	S32↔ K142↔ W	S32↔ K144↔ W
		P↔ FL↔ ASH	8	8	8	16	16	16	8	16
		D↔ FL↔ ASH	8	8	8	8	8	16	8	8
in	size	Size to be erased in bytes. It is used to determine number of sectors to be erased. This size should be aligned to bytes following a below table								
		FL↔ ASH TY↔ P↔ E/↔ M↔ CU	S32↔ K116	S32↔ K118	S32↔ K142	S32↔ K144	S32↔ K146	S32↔ K148	S32↔ K142↔ W	S32↔ K144↔ W
		P↔ FL↔ ASH	8	8	8	16	16	16	8	16
		D↔ FL↔ ASH	8	8	8	8	8	16	8	8

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failure was occurred.
- STATUS_BUSY: Operation was busy.

Definition at line 531 of file flash_driver.c.

17.51.6.10 void FLASH_DRV_EraseSuspend (void)

Flash erase suspend.

This API is used to suspend a current operation of Flash erase sector command. This function must be located in RAM memory or different Flash blocks which are targeted for writing to avoid the RWW error.

Definition at line 682 of file flash_driver.c.

17.51.6.11 static bool FLASH_DRV_GetCmdCompleteFlag (void) [inline],[static]

Check the command complete flag has completed or not.

Returns

the command complete flag

- true: The FTFC command has completed.
- false: The FTFC command is in progress.

Implements : FLASH_DRV_GetCmdCompleteFlag_Activity

Definition at line 1649 of file flash_driver.h.

17.51.6.12 void FLASH_DRV_GetDefaultConfig (flash_user_config_t *const config)

Get default flash configuration.

This API will get default flash user configuration.

Parameters

out	config	Pointer flash user configuration structure.
-----	--------	---

Definition at line 2191 of file flash_driver.c.

17.51.6.13 void FLASH_DRV_GetPFlashProtection (uint32_t * protectStatus)

P-Flash get protection.

This API retrieves the current P-Flash protection status. Considering the time consumption for getting protection is very low and even can be ignored. It is not necessary to utilize the Callback function to support the time-critical events.

Parameters

out	protectStatus	<p>To return the current value of the P-Flash Protection. Each bit is corresponding to protection of 1/32 of the total P-Flash. The least significant bit is corresponding to the lowest address area of P-Flash. The most significant bit is corresponding to the highest address area of P-Flash and so on. There are two possible cases as below:</p> <ul style="list-style-type: none"> • 0: this area is protected. • 1: this area is unprotected.
-----	---------------	---

Definition at line 314 of file flash_driver.c.

17.51.6.14 static bool FLASH_DRV_GetReadCollisionFlag (void) [inline], [static]

Check the read collision error flag is detected or not.

Returns

the read collision error flag

- true: Collision error detected.
- false: No collision error detected.

Implements : FLASH_DRV_GetReadCollisionFlag_Activity

Definition at line 1680 of file flash_driver.h.

17.51.6.15 void FLASH_DRV_GetSecurityState (uint8_t * securityState)

Flash get security state.

This API retrieves the current Flash security status, including the security enabling state and the back door key enabling state.

Parameters

out	<i>securityState</i>	To return the current security status code. <ul style="list-style-type: none"> FLASH_NOT_SECURE (0x01U): Flash currently not in secure state FLASH_SECURE_BACKDOOR_ENABLED (0x02U): Flash is secured and back door key access enabled FLASH_SECURE_BACKDOOR_DISABLED (0x04U): Flash is secured and back door key access disabled.
-----	----------------------	--

Definition at line 378 of file flash_driver.c.

17.51.6.16 `status_t FLASH_DRV_Init (const flash_user_config_t *const pUserConf, flash_ssd_config_t *const pSSDConfig)`

Initializes Flash.

This API initializes Flash module by reporting the memory configuration via SSD configuration structure.

Parameters

in	<i>pUserConf</i>	The user configuration structure pointer.
in	<i>pSSDConfig</i>	The SSD configuration structure pointer.

Returns

operation status

- STATUS_SUCCESS: Operation was successful.

Definition at line 225 of file flash_driver.c.

17.51.6.17 `status_t FLASH_DRV_Program (const flash_ssd_config_t * pSSDConfig, uint32_t dest, uint32_t size, const uint8_t * pData)`

Flash program.

This API is used to program 4 consecutive bytes (for program long word command) and 8 consecutive bytes (for program phrase command) on P-Flash or D-Flash block. This API always returns FTFx_OK if size provided by user is zero regardless of the input validation

Parameters

in	<i>pSSDConfig</i>	The SSD configuration structure pointer.
in	<i>dest</i>	Start address for the intended program operation. This address should be aligned to 8 bytes.
in	<i>size</i>	Size in byte to be programmed. This size should be aligned to 8 bytes.
in	<i>pData</i>	Pointer of source address from which data has to be taken for program operation.

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failure was occurred.
- STATUS_BUSY: Operation was busy.

Definition at line 908 of file flash_driver.c.

17.51.6.18 `status_t FLASH_DRV_ProgramCheck (const flash_ssd_config_t * pSSDConfig, uint32_t dest, uint32_t size, const uint8_t * pExpectedData, uint32_t * pFailAddr, uint8_t marginLevel)`

Flash program check.

This API tests a previously programmed P-Flash or D-Flash long word to see if it reads correctly at the specified margin level. This API always returns FTFx_OK if size provided by user is zero regardless of the input validation

Parameters

in	<i>pSSDConfig</i>	The SSD configuration structure pointer.
in	<i>dest</i>	Start address for the intended program check operation. This address should be aligned to 4 bytes.
in	<i>size</i>	Size in byte to check accuracy of program operation. This size should be aligned to 4 bytes.
in	<i>pExpectedData</i>	The pointer to the expected data.
in	<i>pFailAddr</i>	Returned the first aligned failing address.
in	<i>marginLevel</i>	Read margin choice as follows: <ul style="list-style-type: none"> • <code>marginLevel = 0x1U</code>: read at User margin 1/0 level. • <code>marginLevel = 0x2U</code>: read at Factory margin 1/0 level.

Returns

operation status

- `STATUS_SUCCESS`: Operation was successful.
- `STATUS_ERROR`: Operation failure was occurred.
- `STATUS_BUSY`: Operation was busy.

Definition at line 1000 of file `flash_driver.c`.

17.51.6.19 `status_t FLASH_DRV_ProgramOnce (const flash_ssd_config_t * pSSDConfig, uint8_t recordIndex, const uint8_t * pDataArray)`

Flash program once.

This API is used to program to a reserved 64 byte field located in the P-Flash IFR via given number of record. See the corresponding reference manual to get correct value of this number.

Parameters

in	<i>pSSDConfig</i>	The SSD configuration structure pointer.
in	<i>recordIndex</i>	The record index will be read. It can be from 0x0U to 0x7U or from 0x0U to 0xF according to specific derivative.
in	<i>pdataArray</i>	Pointer to the array from which data will be taken for program once command.

Returns

operation status

- `STATUS_SUCCESS`: Operation was successful.
- `STATUS_ERROR`: Operation failure was occurred.
- `STATUS_BUSY`: Operation was busy.

Definition at line 783 of file `flash_driver.c`.

17.51.6.20 `status_t FLASH_DRV_ReadOnce (const flash_ssd_config_t * pSSDConfig, uint8_t recordIndex, uint8_t * pDataArray)`

Flash read once.

This API is used to read out a reserved 64 byte field located in the P-Flash IFR via given number of record. See the corresponding reference manual to get the correct value of this number.

Parameters

in	<i>pSSDConfig</i>	The SSD configuration structure pointer.
in	<i>recordIndex</i>	The record index will be read. It can be from 0x0U to 0x7U or from 0x0U to 0xF according to specific derivative.
in	<i>pdataArray</i>	Pointer to the array to return the data read by the read once command.

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failure was occurred.
- STATUS_BUSY: Operation was busy.

Definition at line 732 of file flash_driver.c.

17.51.6.21 `status_t FLASH_DRV_SecurityBypass (const flash_ssd_config_t * pSSDConfig, const uint8_t * keyBuffer)`

Flash security bypass.

This API un-secures the device by comparing the user's provided back door key with the ones in the Flash Configuration Field. If they are matched, the security is released. Otherwise, an error code is returned.

Parameters

in	<i>pSSDConfig</i>	The SSD configuration structure pointer.
in	<i>keyBuffer</i>	Point to the user buffer containing the back door key.

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failure was occurred.
- STATUS_BUSY: Operation was busy.

Definition at line 420 of file flash_driver.c.

17.51.6.22 `status_t FLASH_DRV_SetPFlashProtection (uint32_t protectStatus)`

P-Flash set protection.

This API sets the P-Flash protection to the intended protection status. Setting P-Flash protection status is subject to a protection, transition restriction. If there is a setting violation, it returns an error code and the current protection status will not be changed.

Parameters

in	<i>protectStatus</i>	<p>The expected protect status user wants to set to P-Flash protection register. Each bit is corresponding to protection of 1/32 of the total P-Flash. The least significant bit is corresponding to the lowest address area of P-Flash. The most significant bit is corresponding to the highest address area of P-Flash, and so on. There are two possible cases as shown below:</p> <ul style="list-style-type: none"> • 0: this area is protected. • 1: this area is unprotected.
----	----------------------	---

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failure was occurred.

Definition at line 337 of file flash_driver.c.

17.51.6.23 `status_t FLASH_DRV_VerifyAllBlock (const flash_ssd_config_t * pSSDConfig, uint8_t marginLevel)`

Flash verify all blocks.

This function checks to see if the P-Flash and/or D-Flash, EEPROM backup area, and D-Flash IFR have been erased to the specified read margin level, if applicable, and releases security if the readout passes.

Parameters

in	<i>pSSDConfig</i>	The SSD configuration structure pointer.
in	<i>marginLevel</i>	Read Margin Choice as follows: <ul style="list-style-type: none"> • marginLevel = 0x0U: use the Normal read level • marginLevel = 0x1U: use the User read • marginLevel = 0x2U: use the Factory read

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failure was occurred.
- STATUS_BUSY: Operation was busy.

Definition at line 495 of file flash_driver.c.

17.51.6.24 `status_t FLASH_DRV_VerifySection (const flash_ssd_config_t * pSSDConfig, uint32_t dest, uint16_t number, uint8_t marginLevel)`

Flash verify section.

This API checks if a section of the P-Flash or the D-Flash memory is erased to the specified read margin level.

Parameters

in	<i>pSSDConfig</i>	The SSD configuration structure pointer.								
in	<i>dest</i>	Start address for the intended verify operation. User need to make sure the dest address in of P-FLASH or D-FLASH block. This address should be aligned to bytes following a below table								
		FL ASH TY P E/ M CU	S32 K116	S32 K118	S32 K142	S32 K144	S32 K146	S32 K148	S32 K142 W	S32 K144 W
		P- FL- ASH	8	8	8	16	16	16	8	16
		D- FL- ASH	8	8	8	8	8	16	8	8
in	<i>number</i>	Number of alignment unit to be verified. Refer to corresponding reference manual to get correct information of alignment constrain.								
in	<i>marginLevel</i>	Read Margin Choice as follows: <ul style="list-style-type: none">• marginLevel = 0x0U: use Normal read level• marginLevel = 0x1U: use the User read• marginLevel = 0x2U: use the Factory read								

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failure was occurred.
- STATUS_BUSY: Operation was busy.

Definition at line 612 of file flash_driver.c.

17.51.7 Variable Documentation

17.51.7.1 uint8_t brownOutCode

Brown-out detection code

Definition at line 834 of file flash_driver.h.

17.51.7.2 flash_callback_t Callback

Call back function to service the time critical events. Any code reachable from this function must not be placed in a Flash block targeted for a program/erase operation

Definition at line 794 of file flash_driver.h.

17.51.7.3 flash_callback_t Callback

Call back function to service the time critical events. Any code reachable from this function must not be placed in a Flash block targeted for a program/erase operation

Definition at line 823 of file flash_driver.h.

17.51.7.4 uint32_t DFlashBase

For FlexNVM device, this is the base address of D-Flash memory (FlexNVM memory); For non-FlexNVM device, this field is unused

Definition at line 790 of file flash_driver.h.

17.51.7.5 uint32_t DFlashBase

For FlexNVM device, this is the base address of D-Flash memory (FlexNVM memory); For non-FlexNVM device, this field is unused

Definition at line 814 of file flash_driver.h.

17.51.7.6 uint32_t DFlashSize

For FlexNVM device, this is the size in byte of area which is used as D-Flash from FlexNVM memory; For non-FlexNVM device, this field is unused

Definition at line 816 of file flash_driver.h.

17.51.7.7 uint32_t EEESize

For FlexNVM device, this is the size in byte of EEPROM area which was partitioned from FlexRAM; For non-FlexNVM device, this field is unused

Definition at line 821 of file flash_driver.h.

17.51.7.8 uint32_t EERAMBase

The base address of FlexRAM (for FlexNVM device) or acceleration RAM memory (for non-FlexNVM device)

Definition at line 792 of file flash_driver.h.

17.51.7.9 uint32_t EERAMBase

The base address of FlexRAM (for FlexNVM device) or acceleration RAM memory (for non-FlexNVM device)

Definition at line 819 of file flash_driver.h.

17.51.7.10 uint16_t numOfRecordReqMaintain

Number of EEPROM quick write records requiring maintenance

Definition at line 835 of file flash_driver.h.

17.51.7.11 uint32_t PFlashBase

The base address of P-Flash memory

Definition at line 788 of file flash_driver.h.

17.51.7.12 uint32_t PFlashBase

The base address of P-Flash memory

Definition at line 812 of file flash_driver.h.

17.51.7.13 uint32_t PFlashSize

The size in byte of P-Flash memory

Definition at line 789 of file flash_driver.h.

17.51.7.14 uint32_t PFlashSize

The size in byte of P-Flash memory

Definition at line 813 of file flash_driver.h.

17.51.7.15 uint16_t sectorEraseCount

EEPROM sector erase count

Definition at line 836 of file flash_driver.h.

17.52 Flash Memory (Flash)

17.52.1 Detailed Description

Flash Memory Module provides the general flash APIs.

Flash memory is ideal for single-supply applications, permitting in-the-field erase and reprogramming operations without the need for any external high voltage power sources. The flash module includes a memory controller that executes commands to modify flash memory contents. An erased bit reads '1' and a programmed bit reads '0'. The programming operation is unidirectional; it can only move bits from the '1' state (erased) to the '0' state (programmed). Only the erase operation restores bits from '0' to '1'; bits cannot be programmed from a '0' to a '1'.

C90TFS Flash Driver

The C90TFS flash module includes the following accessible memory regions.

1. Program flash memory for vector space and code store.
2. FlexNVM for data store, additional code store and also non-volatile storage for the EEPROM filing system representing data written to the FlexRAM requiring highest endurance.
3. FlexRAM for high-endurance EEPROM data store or traditional RAM.

Some platforms may be designed to have only program flash memory or all of them.

The S32 SDK provides the C90TFS Flash driver of S32K platforms. The driver includes general APIs to handle specific operations on C90TFS Flash module. The user can use those APIs directly in the application.

EEPROM feature

For platforms with FlexNVM, the flash module provides a built-in hardware emulation scheme to emulate the characteristics of an EEPROM by effectively providing a high-endurance, byte write-able NVM. The EEPROM system is shown in the following figure.

Figure 1. EEPROM Architecture

To handle with various customer's requirements, the FlexRAM and FlexNVM blocks can be split into partitions:

1. EEPROM partition(EESIZE) — The amount of FlexRAM used for EEPROM can be set from 0 Bytes (no EEPROM) to the maximum FlexRAM size. The remainder of the FlexRAM not used for EEPROM is not accessible while the FlexRAM is configured for EEPROM. The EEPROM partition grows upward from the bottom of the FlexRAM address space.
2. Data flash partition(DEPART) — The amount of FlexNVM memory used for data flash can be programmed from 0 bytes (all of the FlexNVM block is available for EEPROM backup) to the maximum size of the FlexNVM block.
3. FlexNVM EEPROM partition — The amount of FlexNVM memory used for EEPROM backup, which is equal to the FlexNVM block size minus the data flash memory partition size. The EEPROM backup size must be at least 16 times the EEPROM partition size in FlexRAM.

The partition information (EESIZE, DEPART) is programmed using the **#FLASH_DRV_DEFlashPartition** API.

The function of FlexRAM can be changed from EEPROM usage to traditional RAM for accelerate programming in **#FLASH_DRV_ProgramSection** API and vice versa by **#FLASH_DRV_SetFlexRamFunction** API.

This is example code of EEE usage sequence:

```
/* Provide information about the flash blocks. */
const flash_user_config_t Flash_InitConfig0 = {
    .PFlashBase = 0x00000000U, /* Base address of Program Flash block */
    .PFlashSize = 0x00100000U, /* Size of Program Flash block */
    .DFlashBase = 0x10000000U, /* Base address of Data Flash block */
}
```

```

.EERAMBase = 0x14000000U, /* Base address of FlexRAM block */
/* If using callback, any code reachable from this function must not be placed in a Flash block
   targeted for a program/erase operation.*/
.CallBack = NULL_CALLBACK
};

/* Declare a FLASH configuration structure which is initialized by FlashInit, and will be used by all
   flash APIs */
flash_ssd_config_t flashSSDConfig;
status_t ret; /* Store the driver APIs return code */

/* Data source for program operation */
#define BUFFER_SIZE 0x100u /* Size of data source */
#define SIZE_WRITE_EEE 0x7u /* Size of data write in EEPROM */
uint8_t sourceBuffer[BUFFER_SIZE];

/* Init source data */
for (i = 0u; i < BUFFER_SIZE; i++)
{
    sourceBuffer[i] = i;
}

/* Always initialize the driver before calling other functions */
ret = FLASH_DRV_Init(&Flash_InitConfig0, &flashSSDConfig);
if (ret != STATUS_SUCCESS)
{
    return ret;
}

#if ((FEATURE_FLS_HAS_FLEX_NVM == 1u) & (FEATURE_FLS_HAS_FLEX_RAM == 1u))
/* Configure FlexRAM as EEPROM if it is currently used as traditional RAM */
if (flashSSDConfig.EEESize == 0u)
{
    /* Configure FlexRAM as EEPROM and FlexNVM as EEPROM backup region,
       DEFflashPartition will be failed if the IFR region isn't blank.
       Refer to the device document for valid EEPROM Data Size Code
       and FlexNVM Partition Code. For example on S32K144:
       - EEEDataSizeCode = 0x02u: EEPROM size = 4 Kbytes
       - DEPartitionCode = 0x08u: EEPROM backup size = 64 Kbytes */
    ret = FLASH_DRV_DEFlashPartition(&flashSSDConfig, 0x02u, 0x08u, 0x0, false, true);
    DEV_ASSERT(STATUS_SUCCESS == ret);
    else
    {
        /* Re-initialize the driver to update the new EEPROM configuration */
        ret = FLASH_DRV_Init(&Flash_InitConfig0, &flashSSDConfig);
        if (ret != STATUS_SUCCESS)
        {
            return ret;
        }

        /* Make FlexRAM available for EEPROM */
        ret = FLASH_DRV_SetFlexRamFunction(&flashSSDConfig, EEE_ENABLE, 0x0u, NULL);
        DEV_ASSERT(STATUS_SUCCESS == ret);
    }
}
else /* FLeXRAM is already configured as EEPROM */
{
    /* Make FlexRAM available for EEPROM, make sure that FlexNVM and FlexRAM
       are already partitioned successfully before */
    ret = FLASH_DRV_SetFlexRamFunction(&flashSSDConfig, EEE_ENABLE, 0x0u, NULL);
    DEV_ASSERT(STATUS_SUCCESS == ret);
}
#endif

/* Erase the sixth PFlash sector */
/* Configure address, size to erase sector function. For example on S32K144 */
address = 6u * FEATURE_FLS_PF_BLOCK_SECTOR_SIZE; /* A sector size is 4KB */
size = FEATURE_FLS_PF_BLOCK_SECTOR_SIZE;
ret = FLASH_DRV_EraseSector(&flashSSDConfig, address, size);
DEV_ASSERT(STATUS_SUCCESS == ret);

/* Verify the erase operation at margin level value of 1, user read */
ret = FLASH_DRV_VerifySection(&flashSSDConfig, address, size, 1u);
DEV_ASSERT(STATUS_SUCCESS == ret);

/* Write some data to the erased PFlash sector */
size = BUFFER_SIZE;
ret = FLASH_DRV_Program(&flashSSDConfig, address, size, sourceBuffer);
DEV_ASSERT(STATUS_SUCCESS == ret);

/* Verify the program operation at margin level value of 1, user margin */
ret = FLASH_DRV_ProgramCheck(&flashSSDConfig, address, size, sourceBuffer, &
    failAddr, 1u);
DEV_ASSERT(STATUS_SUCCESS == ret);

/* Try to write data to EEPROM if FlexRAM is configured as EEPROM */
if (flashSSDConfig.EEESize != 0u)

```

```

{
    address = flashSSDConfig.EERAMBase;
    size = SIZE_WRITE_EEE;
    ret = FLASH_DRV_EEEWrite(&flashSSDConfig, address, size, sourceBuffer);
    DEV_ASSERT(STATUS_SUCCESS == ret);
}

```

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\flash\flash_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

Clock Manager

Important Note

1. If using callback in the application, any code reachable from this function must not be placed in a Flash block targeted for a program/erase operation to avoid the RWW error. Functions can be placed in RAM section by using the START/END_FUNCTION_DEFINITION/DECLARATION_RAMSECTION macros.
2. To suspend the sector erase operation for a simple method, invoke the [FLASH_DRV_EraseSuspend](#) function within callback of [FLASH_DRV_EraseSector](#). In this case, the [FLASH_DRV_EraseSuspend](#) must not be placed in the same block in which the Flash erase sector command is going on.
3. [#FLASH_DRV_CommandSequence](#), [FLASH_DRV_EraseSuspend](#) and [FLASH_DRV_EraseResume](#) should be executed from RAM or different Flash blocks which are targeted for writing to avoid the RWW error. [FLASH_DRV_EraseSuspend](#) and [FLASH_DRV_EraseResume](#) functions should be called in pairs.
4. To guarantee the correct execution of this driver, the Flash cache in the Flash memory controller module should be disabled before invoking any API.
5. Partitioning FlexNVM and FlexRAM for EEPROM usage shall be executed only once in the lifetime of the device.
6. After successfully partitioning FlexNVM and FlexRAM for EEPROM usage, user needs to call [FLASH_DRV_V_Init](#) to update memory information in global structure.
7. Can not erase or program flash when MCU is high speed run mode or very low power mode.
8. S32K14xW needs to enable FlexRAM as traditional RAM for the first time using silicon.

Modules

- [Flash Memory \(Flash\)](#)

17.53 FlexCAN Driver

17.53.1 Detailed Description

How to use the FlexCAN driver in your application

In order to be able to use the FlexCAN in your application, the first thing to do is initializing it with the desired configuration. This is done by calling the **FLEXCAN_DRV_Init** function. One of the arguments passed to this function is the configuration which will be used for the FlexCAN module, specified by the [flexcan_user_config_t](#) structure.

The [flexcan_user_config_t](#) structure allows you to configure the following:

- the number of message buffers needed;
- the number of Rx FIFO ID filters needed;
- enable/disable the Rx FIFO feature;
- the operation mode, which can be one of the following:
 - normal mode;
 - listen-only mode;
 - loopback mode;
 - freeze mode;
 - disable mode;
- the payload size of the message buffers:
 - 8 bytes;
 - 16 bytes (only available with the FD feature enabled);
 - 32 bytes (only available with the FD feature enabled);
 - 64 bytes (only available with the FD feature enabled);
- enable/disable the Flexible Data-rate feature;
- the clock source of the CAN Protocol Engine (PE);
- the bitrate used for standard frames or for the arbitration phase of FD frames;
- the bitrate used for the data phase of FD frames;
- the Rx FIFO transfer type, which can be one of the following:
 - using interrupts;
 - using DMA, only on supported platforms;
- the DMA channel number to be used for DMA transfers, only on supported platforms;

The bitrate is represented by a [flexcan_time_segment_t](#) structure, with the following fields:

- propagation segment;
- phase segment 1;
- phase segment 2;
- clock prescaler division factor;
- resync jump width.

Details about these fields can be found in the reference manual.

In order to use a mailbox for transmission/reception, it should be initialized using either **FLEXCAN_DRV_Config**, **RxMb**, **FLEXCAN_DRV_ConfigRxFifo** or **FLEXCAN_DRV_ConfigTxMb**.

After having the mailbox configured, you can start sending/receiving data using the specified mailbox, by calling one of the following functions:

- FLEXCAN_DRV_Send;
- FLEXCAN_DRV_SendBlocking;
- FLEXCAN_DRV_Receive;
- FLEXCAN_DRV_ReceiveBlocking;
- FLEXCAN_DRV_RxFifo;
- FLEXCAN_DRV_RxFifoBlocking.

A default FlexCAN configuration can be accessed by calling the **FLEXCAN_DRV_GetDefaultConfig** function. This function takes as argument a **flexcan_user_config_t** structure and fills it according to the following settings:

- 16 message buffers
- flexible data rate disabled
- Rx FIFO disabled
- normal operation mode
- 8 byte payload size
- Protocol Engine clock = Oscillator clock
- bitrate of 500 Kbit/s (computed for PE clock = 8 MHz with sample point = 87.5)

FlexCAN Rx FIFO configuration

The Rx FIFO is receive-only and 6-message deep. The user can read the received messages sequentially, in the order they were received, by repeatedly reading Message Buffer 0 (zero). The Rx FIFO ID filter table (configurable from 8 to 128 table elements) specifies filtering criteria for accepting frames into the FIFO. This table is represented through a structure of **flexcan_id_table_t** type, which specifies if Remote Frames are accepted into the FIFO if they match the target ID, whether extended or standard frames are accepted into the FIFO if they match the target ID and the target ID.

```
/* ID Filter table */
const flexcan_id_table_t filterTable[] = {
    {
        .isExtendedFrame = false,
        .isRemoteFrame = false,
        .id = 1U
    },
    ...
};

FLEXCAN_DRV_ConfigRxFifo(INST_CANCOM1,
    FLEXCAN_RX_FIFO_ID_FORMAT_A, filterTable);
```

The number of elements in the ID filter table is defined by the following formula:

- for format A: the number of Rx FIFO ID filters
- for format B: twice the number of Rx FIFO ID filters
- for format C: four times the number of Rx FIFO ID filters The user must provide the exact number of elements in order to avoid any misconfiguration.

Each element in the ID filter table specifies an ID to be used as acceptance criteria for the FIFO, as follows:

- for format A: In the standard frame format, bits 10 to 0 of the ID are used for frame identification. In the extended frame format, bits 28 to 0 are used.
- for format B: In the standard frame format, bits 10 to 0 of the ID are used for frame identification. In the extended frame format, only the 14 most significant bits (28 to 15) of the ID are compared to the 14 most significant bits (28 to 15) of the received ID.
- for format C: In both standard and extended frame formats, only the 8 most significant bits (7 to 0 for standard, 28 to 21 for extended) of the ID are compared to the 8 most significant bits (7 to 0 for standard, 28 to 21 for extended) of the received ID.

When Rx FIFO feature is enabled, buffer 0 (zero) cannot be used for transmission. The transfer status in case of FIFO enable feature can be monitored by calling **FLEXCAN_DRV_GetTransferStatus** for buffer index 0.

In order to use Rx FIFO filter mask options, enabled by **FLEXCAN_DRV_SetRxIndividualMask()** and **FLEXCAN_DRV_SetRxFifoGlobalMask()** user needs to call **FLEXCAN_DRV_ConfigRxFifo()** before using these functions in Rx FIFO mode. In case of Rx FIFO ID filter format B or C the **FLEXCAN_DRV_SetRxFifoGlobalMask()** will apply the same mask for all filters IDs.

The **FLEXCAN_DRV_SetRxIndividualMask()** can self determine if CAN is in normal mode and will only set acceptance ID Mask. If CAN is in Rx FIFO mode, will determine the ID format type and will set the acceptance ID Mask as corresponding Id Filter Format corresponding to individual mask number the user must ensure that the ID Element is not affected by Rx FIFO Global Mask in this case the ID Filter will be set as normal configuration to allow functionality of receiving as normal MB of the remaining MBs outside of Rx FIFO use.

Important Notes

- The FlexCAN driver does not handle clock setup or any kind of pin configuration. This is handled by the **Clock Manager** and **PinSettings** modules, respectively. The driver assumes that the correct clock configurations have been made, so it is the user's responsibility to set up clocking and pin configurations correctly.
- For some platforms, the clock source of the CAN Protocol Engine (PE) is not configurable from the FlexCAN module. If this feature is not supported, the *pe_clock* field from the FlexCAN configuration structure is not present.
- DMA module has to be initialized prior to FlexCAN Rx FIFO usage in DMA mode; also, the DMA channel needs to be allocated by the application (the driver only takes care of configuring the DMA channel received in the configuration structure).
- When used **FLEXCAN_DRV_ReceiveBlocking()** and **FLEXCAN_DRV_SendBlocking()** with timeout parameter 0 and the message is already in mailbox configured will report timeout and successful transmit or receive the message.
- For Cortex-M0 architecture S32K116 and S32K118 CPUs need to pass as transmission/reception buffers memory aligned, the only allowed exceptions are for **FLEXCAN_DRV_Send()**, **FLEXCAN_DRV_SendBlocking()**, **FLEXCAN_DRV_ConfigRemoteResponseMb** with a payload length less than 3 bytes
- When used the Pretended Network Mode, in Stop Mode the Interface Clock(CHI) (from Clock_Manager) need to be disabled and Protocol Engine (PE) clock source enabled as selected from Can Module. Be aware that on wakeup Run Mode to have enabled the Interface Clock(CHI).
- In case inside the callback function is called another blocking reception (**FLEXCAN_DRV_ReceiveBlocking/FLEXCAN_DRV_RxFifoBlocking**) or abort **FLEXCAN_DRV_AbortTransfer** without polling previous operation status this can lead to undetermined behavior.

Example:

```
#define INST_CANCOM1 (0U)
#define RX_MAILBOX (1U)
#define MSG_ID (2U)

flexcan_state_t canCom1_State;
```



```

const flexcan_user_config_t canCom1_InitConfig0 = {
    .fd_enable = true,
    .pe_clock = FLEXCAN_CLK_SOURCE_OSC,
    .max_num_mb = 16,
    .num_id_filters = FLEXCAN_RX_FIFO_ID_FILTERS_8,
    .is_rx_fifo_needed = false,
    .flexcanMode = FLEXCAN_NORMAL_MODE,
    .payload = FLEXCAN_PAYLOAD_SIZE_8,
    .bitrate = {
        .propSeg = 7,
        .phaseSeg1 = 4,
        .phaseSeg2 = 1,
        .preDivider = 0,
        .rJumpwidth = 1
    },
    .bitrate_cbt = {
        .propSeg = 11,
        .phaseSeg1 = 1,
        .phaseSeg2 = 1,
        .preDivider = 0,
        .rJumpwidth = 1
    },
    .transfer_type = FLEXCAN_RX_FIFO_USING_INTERRUPTS,
    .rxFifoDMAChannel = 0U
};

/* Initialize FlexCAN driver */
FLEXCAN_DRV_Init(INST_CANCOM1, &canCom1_State, &canCom1_InitConfig0);

/* Set information about the data to be received */
flexcan_data_info_t dataInfo =
{
    .data_length = 1U,
    .msg_id_type = FLEXCAN_MSG_ID_STD,
    .enable_brs = true,
    .fd_enable = true,
    .fd_padding = 0U
};

/* Configure Rx message buffer with index 1 to receive frames with ID 2 */
FLEXCAN_DRV_ConfigRxMb(INST_CANCOM1, RX_MAILBOX, &dataInfo, MSG_ID);

/* Receive a frame in the recvBuff variable */
flexcan_msgbuff_t recvBuff;

FLEXCAN_DRV_Receive(INST_CANCOM1, RX_MAILBOX, &recvBuff);
/* Wait for the message to be received */
while (FLEXCAN_DRV_GetTransferStatus(INST_CANCOM1, RX_MAILBOX) == STATUS_BUSY)
    ;

/* De-initialize driver */
FLEXCAN_DRV_Deinit(INST_CANCOM1);

```

Integration guideline

Compilation units

The following files need to be compiled in the project:

```

${S32SDK_PATH}\platform\drivers\src\flexcan\flexcan_driver.c
${S32SDK_PATH}\platform\drivers\src\flexcan\flexcan_hw_access.c
${S32SDK_PATH}\platform\drivers\src\flexcan\flexcan_irq.c

```

Include path

The following paths need to be added to the include path of the toolchain:

```

${S32SDK_PATH}\platform\drivers\inc\

```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager](#) [Interrupt Manager \(Interrupt\)](#) [Enhanced Direct Memory Access \(eDMA\)](#)

Data Structures

- struct [flexcan_msgbuff_t](#)
FlexCAN message buffer structure Implements : flexcan_msgbuff_t_Class. [More...](#)
- struct [flexcan_mb_handle_t](#)
Information needed for internal handling of a given MB. Implements : flexcan_mb_handle_t_Class. [More...](#)
- struct [FlexCANState](#)
Internal driver state information. [More...](#)
- struct [flexcan_data_info_t](#)
FlexCAN data info from user Implements : flexcan_data_info_t_Class. [More...](#)
- struct [flexcan_id_table_t](#)
FlexCAN Rx FIFO ID filter table structure Implements : flexcan_id_table_t_Class. [More...](#)
- struct [flexcan_time_segment_t](#)
FlexCAN bitrate related structures Implements : flexcan_time_segment_t_Class. [More...](#)
- struct [flexcan_user_config_t](#)
FlexCAN configuration. [More...](#)

Typedefs

- typedef struct [FlexCANState flexcan_state_t](#)
Internal driver state information.
- typedef void(* [flexcan_callback_t](#)) (uint8_t instance, [flexcan_event_type_t](#) eventType, uint32_t buffIdx, [flexcan_state_t](#) *flexcanState)
FlexCAN Driver callback function type Implements : flexcan_callback_t_Class.
- typedef void(* [flexcan_error_callback_t](#)) (uint8_t instance, [flexcan_event_type_t](#) eventType, [flexcan_state_t](#) *flexcanState)
FlexCAN Driver error callback function type Implements : flexcan_error_callback_t_Class.

Enumerations

- enum [flexcan_rxfifo_transfer_type_t](#) { [FLEXCAN_RXFIFO_USING_INTERRUPTS](#) }
The type of the RxFIFO transfer (interrupts/DMA). Implements : flexcan_rxfifo_transfer_type_t_Class.
- enum [flexcan_event_type_t](#) {
[FLEXCAN_EVENT_RX_COMPLETE](#), [FLEXCAN_EVENT_RXFIFO_COMPLETE](#), [FLEXCAN_EVENT_RXFIFO_WARNING](#), [FLEXCAN_EVENT_RXFIFO_OVERFLOW](#),
[FLEXCAN_EVENT_TX_COMPLETE](#), [FLEXCAN_EVENT_ERROR](#) }
The type of the event which occurred when the callback was invoked. Implements : flexcan_event_type_t_Class.
- enum [flexcan_mb_state_t](#) { [FLEXCAN_MB_IDLE](#), [FLEXCAN_MB_RX_BUSY](#), [FLEXCAN_MB_TX_BUSY](#) }
The state of a given MB (idle/Rx busy/Tx busy). Implements : flexcan_mb_state_t_Class.
- enum [flexcan_msgbuff_id_type_t](#) { [FLEXCAN_MSG_ID_STD](#), [FLEXCAN_MSG_ID_EXT](#) }
FlexCAN Message Buffer ID type Implements : flexcan_msgbuff_id_type_t_Class.
- enum [flexcan_rx_fifo_id_filter_num_t](#) {
[FLEXCAN_RX_FIFO_ID_FILTERS_8](#) = 0x0, [FLEXCAN_RX_FIFO_ID_FILTERS_16](#) = 0x1, [FLEXCAN_RX_FIFO_ID_FILTERS_24](#) = 0x2, [FLEXCAN_RX_FIFO_ID_FILTERS_32](#) = 0x3,
[FLEXCAN_RX_FIFO_ID_FILTERS_40](#) = 0x4, [FLEXCAN_RX_FIFO_ID_FILTERS_48](#) = 0x5, [FLEXCAN_RX_FIFO_ID_FILTERS_56](#) = 0x6, [FLEXCAN_RX_FIFO_ID_FILTERS_64](#) = 0x7,
[FLEXCAN_RX_FIFO_ID_FILTERS_72](#) = 0x8, [FLEXCAN_RX_FIFO_ID_FILTERS_80](#) = 0x9, [FLEXCAN_RX_FIFO_ID_FILTERS_88](#) = 0xA, [FLEXCAN_RX_FIFO_ID_FILTERS_96](#) = 0xB,
[FLEXCAN_RX_FIFO_ID_FILTERS_104](#) = 0xC, [FLEXCAN_RX_FIFO_ID_FILTERS_112](#) = 0xD, [FLEXCAN_RX_FIFO_ID_FILTERS_120](#) = 0xE, [FLEXCAN_RX_FIFO_ID_FILTERS_128](#) = 0xF }
FlexCAN Rx FIFO filters number Implements : flexcan_rx_fifo_id_filter_num_t_Class.
- enum [flexcan_rx_mask_type_t](#) { [FLEXCAN_RX_MASK_GLOBAL](#), [FLEXCAN_RX_MASK_INDIVIDUAL](#) }

FlexCAN Rx mask type. Implements : flexcan_rx_mask_type_t Class.

- enum `flexcan_rx_fifo_id_element_format_t` { `FLEXCAN_RX_FIFO_ID_FORMAT_A`, `FLEXCAN_RX_FIFO_ID_FORMAT_B`, `FLEXCAN_RX_FIFO_ID_FORMAT_C`, `FLEXCAN_RX_FIFO_ID_FORMAT_D` }

ID formats for Rx FIFO Implements : flexcan_rx_fifo_id_element_format_t Class.

- enum `flexcan_operation_modes_t` { `FLEXCAN_NORMAL_MODE`, `FLEXCAN_LISTEN_ONLY_MODE`, `FLEXCAN_LOOPBACK_MODE`, `FLEXCAN_FREEZE_MODE`, `FLEXCAN_DISABLE_MODE` }

FlexCAN operation modes Implements : flexcan_operation_modes_t Class.

Bit rate

- void `FLEXCAN_DRV_SetBitrate` (uint8_t instance, const `flexcan_time_segment_t` *bitrate)
Sets the FlexCAN bit rate for standard frames or the arbitration phase of FD frames.
- void `FLEXCAN_DRV_GetBitrate` (uint8_t instance, `flexcan_time_segment_t` *bitrate)
Gets the FlexCAN bit rate for standard frames or the arbitration phase of FD frames.

Rx MB and Rx FIFO masks

- void `FLEXCAN_DRV_SetRxMaskType` (uint8_t instance, `flexcan_rx_mask_type_t` type)
Sets the Rx masking type.
- void `FLEXCAN_DRV_SetRxFifoGlobalMask` (uint8_t instance, `flexcan_msgbuff_id_type_t` id_type, uint32_t mask)
Sets the FlexCAN Rx FIFO global mask (standard or extended). This mask is applied to all filters ID regardless the ID Filter format.
- void `FLEXCAN_DRV_SetRxMbGlobalMask` (uint8_t instance, `flexcan_msgbuff_id_type_t` id_type, uint32_t mask)
Sets the FlexCAN Rx MB global mask (standard or extended).
- void `FLEXCAN_DRV_SetRxMb14Mask` (uint8_t instance, `flexcan_msgbuff_id_type_t` id_type, uint32_t mask)
Sets the FlexCAN Rx MB 14 mask (standard or extended).
- void `FLEXCAN_DRV_SetRxMb15Mask` (uint8_t instance, `flexcan_msgbuff_id_type_t` id_type, uint32_t mask)
Sets the FlexCAN Rx MB 15 mask (standard or extended).
- status_t `FLEXCAN_DRV_SetRxIndividualMask` (uint8_t instance, `flexcan_msgbuff_id_type_t` id_type, uint8_t mb_idx, uint32_t mask)
Sets the FlexCAN Rx individual mask (standard or extended).

Initialization and Shutdown

- uint32_t `FLEXCAN_DRV_GetDefaultConfig` (`flexcan_user_config_t` *config)
Gets the default configuration structure.
- status_t `FLEXCAN_DRV_Init` (uint8_t instance, `flexcan_state_t` *state, const `flexcan_user_config_t` *data)
Initializes the FlexCAN peripheral.
- status_t `FLEXCAN_DRV_Deinit` (uint8_t instance)
Shuts down a FlexCAN instance.

Send configuration

- status_t `FLEXCAN_DRV_ConfigTxMb` (uint8_t instance, uint8_t mb_idx, const `flexcan_data_info_t` *tx_info, uint32_t msg_id)
FlexCAN transmit message buffer field configuration.
- status_t `FLEXCAN_DRV_ConfigRemoteResponseMb` (uint8_t instance, uint8_t mb_idx, const `flexcan_data_info_t` *tx_info, uint32_t msg_id, const uint8_t *mb_data)

Configures a transmit message buffer for remote frame response.

- status_t [FLEXCAN_DRV_SendBlocking](#) (uint8_t instance, uint8_t mb_idx, const [flexcan_data_info_t](#) *tx_info, uint32_t msg_id, const uint8_t *mb_data, uint32_t timeout_ms)

Sends a CAN frame using the specified message buffer, in a blocking manner.

- status_t [FLEXCAN_DRV_Send](#) (uint8_t instance, uint8_t mb_idx, const [flexcan_data_info_t](#) *tx_info, uint32_t msg_id, const uint8_t *mb_data)

Sends a CAN frame using the specified message buffer.

Receive configuration

- status_t [FLEXCAN_DRV_ConfigRxMb](#) (uint8_t instance, uint8_t mb_idx, const [flexcan_data_info_t](#) *rx_info, uint32_t msg_id)

FlexCAN receive message buffer field configuration.

- void [FLEXCAN_DRV_ConfigRxFifo](#) (uint8_t instance, [flexcan_rx_fifo_id_element_format_t](#) id_format, const [flexcan_id_table_t](#) *id_filter_table)

FlexCAN Rx FIFO field configuration.

- status_t [FLEXCAN_DRV_ReceiveBlocking](#) (uint8_t instance, uint8_t mb_idx, [flexcan_msgbuff_t](#) *data, uint32_t timeout_ms)

Receives a CAN frame using the specified message buffer, in a blocking manner.

- status_t [FLEXCAN_DRV_Receive](#) (uint8_t instance, uint8_t mb_idx, [flexcan_msgbuff_t](#) *data)

Receives a CAN frame using the specified message buffer.

- status_t [FLEXCAN_DRV_RxFifoBlocking](#) (uint8_t instance, [flexcan_msgbuff_t](#) *data, uint32_t timeout_ms)

Receives a CAN frame using the message FIFO, in a blocking manner.

- status_t [FLEXCAN_DRV_RxFifo](#) (uint8_t instance, [flexcan_msgbuff_t](#) *data)

Receives a CAN frame using the message FIFO.

Transfer status

- status_t [FLEXCAN_DRV_AbortTransfer](#) (uint8_t instance, uint8_t mb_idx)

Ends a non-blocking FlexCAN transfer early.

- status_t [FLEXCAN_DRV_GetTransferStatus](#) (uint8_t instance, uint8_t mb_idx)

Returns whether the previous FlexCAN transfer has finished.

- uint32_t [FLEXCAN_DRV_GetErrorStatus](#) (uint8_t instance)

Returns reported error conditions.

IRQ handler callback

- void [FLEXCAN_DRV_InstallEventCallback](#) (uint8_t instance, [flexcan_callback_t](#) callback, void *callbackParam)

Installs a callback function for the IRQ handler.

- void [FLEXCAN_DRV_InstallErrorCallback](#) (uint8_t instance, [flexcan_error_callback_t](#) callback, void *callbackParam)

Installs an error callback function for the IRQ handler and enables error interrupts.

17.53.2 Data Structure Documentation

17.53.2.1 struct flexcan_msgbuff_t

FlexCAN message buffer structure Implements : flexcan_msgbuff_t_Class.

Definition at line 100 of file flexcan_driver.h.

Data Fields

- [uint32_t cs](#)
- [uint32_t msgId](#)
- [uint8_t data](#) [64]
- [uint8_t dataLen](#)

Field Documentation

17.53.2.1.1 [uint32_t cs](#)

Code and Status

Definition at line 101 of file flexcan_driver.h.

17.53.2.1.2 [uint8_t data](#)[64]

Data bytes of the FlexCAN message

Definition at line 103 of file flexcan_driver.h.

17.53.2.1.3 [uint8_t dataLen](#)

Length of data in bytes

Definition at line 104 of file flexcan_driver.h.

17.53.2.1.4 [uint32_t msgId](#)

Message Buffer ID

Definition at line 102 of file flexcan_driver.h.

17.53.2.2 [struct flexcan_mb_handle_t](#)

Information needed for internal handling of a given MB. Implements : [flexcan_mb_handle_t_Class](#).

Definition at line 110 of file flexcan_driver.h.

Data Fields

- [flexcan_msgbuff_t * mb_message](#)
- [semaphore_t mbSema](#)
- [volatile flexcan_mb_state_t state](#)
- [bool isBlocking](#)
- [bool isRemote](#)

Field Documentation

17.53.2.2.1 [bool isBlocking](#)

True if the transfer is blocking

Definition at line 114 of file flexcan_driver.h.

17.53.2.2.2 [bool isRemote](#)

True if the frame is a remote frame

Definition at line 115 of file flexcan_driver.h.

17.53.2.2.3 [flexcan_msgbuff_t* mb_message](#)

The FlexCAN MB structure

Definition at line 111 of file flexcan_driver.h.

17.53.2.2.4 semaphore_t mbSema

Semaphore used for signaling completion of a blocking transfer

Definition at line 112 of file flexcan_driver.h.

17.53.2.2.5 volatile flexcan_mb_state_t state

The state of the current MB (idle/Rx busy/Tx busy)

Definition at line 113 of file flexcan_driver.h.

17.53.2.3 struct FlexCANState

Internal driver state information.

Note

The contents of this structure are internal to the driver and should not be modified by users. Also, contents of the structure are subject to change in future releases. Implements : flexcan_state_t_Class

Definition at line 126 of file flexcan_driver.h.

Data Fields

- flexcan_mb_handle_t mbs [FEATURE_CAN_MAX_MB_NUM]
- void(* callback)(uint8_t instance, flexcan_event_type_t eventType, uint32_t buffIdx, struct FlexCANState *driverState)
- void * callbackParam
- void(* error_callback)(uint8_t instance, flexcan_event_type_t eventType, struct FlexCANState *driverState)
- void * errorCallbackParam
- flexcan_rxfifo_transfer_type_t transferType

Field Documentation

17.53.2.3.1 void(* callback)(uint8_t instance, flexcan_event_type_t eventType, uint32_t buffIdx, struct FlexCANState *driverState)

IRQ handler callback function.

Definition at line 129 of file flexcan_driver.h.

17.53.2.3.2 void* callbackParam

Parameter used to pass user data when invoking the callback function.

Definition at line 133 of file flexcan_driver.h.

17.53.2.3.3 void(* error_callback)(uint8_t instance, flexcan_event_type_t eventType, struct FlexCANState *driverState)

Error IRQ handler callback function.

Definition at line 136 of file flexcan_driver.h.

17.53.2.3.4 void* errorCallbackParam

Parameter used to pass user data when invoking the error callback function.

Definition at line 140 of file flexcan_driver.h.

17.53.2.3.5 flexcan_mb_handle_t mbs[FEATURE_CAN_MAX_MB_NUM]

Array containing information related to each MB

Definition at line 127 of file flexcan_driver.h.

17.53.2.3.6 flexcan_rxfifo_transfer_type_t transferType

Type of RxFIFO transfer.

Definition at line 147 of file flexcan_driver.h.

17.53.2.4 struct flexcan_data_info_t

FlexCAN data info from user Implements : flexcan_data_info_t_Class.

Definition at line 153 of file flexcan_driver.h.

Data Fields

- flexcan_msgbuff_id_type_t msg_id_type
- uint32_t data_length
- bool is_remote

Field Documentation

17.53.2.4.1 uint32_t data_length

Length of Data in Bytes

Definition at line 155 of file flexcan_driver.h.

17.53.2.4.2 bool is_remote

Specifies if the frame is standard or remote

Definition at line 162 of file flexcan_driver.h.

17.53.2.4.3 flexcan_msgbuff_id_type_t msg_id_type

Type of message ID (standard or extended)

Definition at line 154 of file flexcan_driver.h.

17.53.2.5 struct flexcan_id_table_t

FlexCAN Rx FIFO ID filter table structure Implements : flexcan_id_table_t_Class.

Definition at line 209 of file flexcan_driver.h.

Data Fields

- bool isRemoteFrame
- bool isExtendedFrame
- uint32_t id

Field Documentation

17.53.2.5.1 uint32_t id

Rx FIFO ID filter element

Definition at line 212 of file flexcan_driver.h.

17.53.2.5.2 bool isExtendedFrame

Extended frame

Definition at line 211 of file flexcan_driver.h.

17.53.2.5.3 bool isRemoteFrame

Remote frame

Definition at line 210 of file flexcan_driver.h.

17.53.2.6 struct flexcan_time_segment_t

FlexCAN bitrate related structures Implements : flexcan_time_segment_t_Class.

Definition at line 241 of file flexcan_driver.h.

Data Fields

- uint32_t [propSeg](#)
- uint32_t [phaseSeg1](#)
- uint32_t [phaseSeg2](#)
- uint32_t [preDivider](#)
- uint32_t [rJumpwidth](#)

Field Documentation

17.53.2.6.1 uint32_t phaseSeg1

Phase segment 1

Definition at line 243 of file flexcan_driver.h.

17.53.2.6.2 uint32_t phaseSeg2

Phase segment 2

Definition at line 244 of file flexcan_driver.h.

17.53.2.6.3 uint32_t preDivider

Clock prescaler division factor

Definition at line 245 of file flexcan_driver.h.

17.53.2.6.4 uint32_t propSeg

Propagation segment

Definition at line 242 of file flexcan_driver.h.

17.53.2.6.5 uint32_t rJumpwidth

Resync jump width

Definition at line 246 of file flexcan_driver.h.

17.53.2.7 struct flexcan_user_config_t

FlexCAN configuration.

Definition at line 253 of file flexcan_driver.h.

Data Fields

- uint32_t [max_num_mb](#)
- [flexcan_rx_fifo_id_filter_num_t](#) num_id_filters
- bool [is_rx_fifo_needed](#)
- [flexcan_operation_modes_t](#) flexcanMode
- [flexcan_time_segment_t](#) bitrate
- [flexcan_rxfifo_transfer_type_t](#) transfer_type

Field Documentation

17.53.2.7.1 flexcan_time_segment_t bitrate

The bitrate used for standard frames or for the arbitration phase of FD frames.

Definition at line 269 of file flexcan_driver.h.

17.53.2.7.2 flexcan_operation_modes_t flexcanMode

User configurable FlexCAN operation modes.

Definition at line 260 of file flexcan_driver.h.

17.53.2.7.3 bool is_rx_fifo_needed

1 if needed; 0 if not. This controls whether the Rx FIFO feature is enabled or not.

Definition at line 258 of file flexcan_driver.h.

17.53.2.7.4 uint32_t max_num_mb

The maximum number of Message [Buffers](#)

Definition at line 254 of file flexcan_driver.h.

17.53.2.7.5 flexcan_rx_fifo_id_filter_num_t num_id_filters

The number of RX FIFO ID filters needed

Definition at line 256 of file flexcan_driver.h.

17.53.2.7.6 flexcan_rxfifo_transfer_type_t transfer_type

Specifies if the Rx FIFO uses interrupts or DMA.

Definition at line 273 of file flexcan_driver.h.

17.53.3 Typedef Documentation

17.53.3.1 typedef void(* flexcan_callback_t) (uint8_t instance, flexcan_event_type_t eventType, uint32_t buffIdx, flexcan_state_t *flexcanState)

FlexCAN Driver callback function type Implements : flexcan_callback_t_Class.

Definition at line 335 of file flexcan_driver.h.

17.53.3.2 typedef void(* flexcan_error_callback_t) (uint8_t instance, flexcan_event_type_t eventType, flexcan_state_t *flexcanState)

FlexCAN Driver error callback function type Implements : flexcan_error_callback_t_Class.

Definition at line 341 of file flexcan_driver.h.

17.53.3.3 typedef struct FlexCANState flexcan_state_t

Internal driver state information.

Note

The contents of this structure are internal to the driver and should not be modified by users. Also, contents of the structure are subject to change in future releases. Implements : flexcan_state_t_Class

17.53.4 Enumeration Type Documentation

17.53.4.1 enum flexcan_event_type_t

The type of the event which occurred when the callback was invoked. Implements : flexcan_event_type_t_Class.

Enumerator

FLEXCAN_EVENT_RX_COMPLETE A frame was received in the configured Rx MB.

FLEXCAN_EVENT_RXFIFO_COMPLETE A frame was received in the Rx FIFO.

FLEXCAN_EVENT_RXFIFO_WARNING Rx FIFO is almost full (5 frames).

FLEXCAN_EVENT_RXFIFO_OVERFLOW Rx FIFO is full (incoming message was lost).

FLEXCAN_EVENT_TX_COMPLETE A frame was sent from the configured Tx MB.

FLEXCAN_EVENT_ERROR

Definition at line 49 of file flexcan_driver.h.

17.53.4.2 enum flexcan_mb_state_t

The state of a given MB (idle/Rx busy/Tx busy). Implements : flexcan_mb_state_t_Class.

Enumerator

FLEXCAN_MB_IDLE The MB is not used by any transfer.

FLEXCAN_MB_RX_BUSY The MB is used for a reception.

FLEXCAN_MB_TX_BUSY The MB is used for a transmission.

Definition at line 70 of file flexcan_driver.h.

17.53.4.3 enum flexcan_msgbuff_id_type_t

FlexCAN Message Buffer ID type Implements : flexcan_msgbuff_id_type_t_Class.

Enumerator

FLEXCAN_MSG_ID_STD Standard ID

FLEXCAN_MSG_ID_EXT Extended ID

Definition at line 82 of file flexcan_driver.h.

17.53.4.4 enum flexcan_operation_modes_t

FlexCAN operation modes Implements : flexcan_operation_modes_t_Class.

Enumerator

FLEXCAN_NORMAL_MODE Normal mode or user mode

FLEXCAN_LISTEN_ONLY_MODE Listen-only mode

FLEXCAN_LOOPBACK_MODE Loop-back mode

FLEXCAN_FREEZE_MODE Freeze mode

FLEXCAN_DISABLE_MODE Module disable mode

Definition at line 218 of file flexcan_driver.h.

17.53.4.5 enum flexcan_rx_fifo_id_element_format_t

ID formats for Rx FIFO Implements : flexcan_rx_fifo_id_element_format_t_Class.

Enumerator

- FLEXCAN_RX_FIFO_ID_FORMAT_A** One full ID (standard and extended) per ID Filter Table element.
FLEXCAN_RX_FIFO_ID_FORMAT_B Two full standard IDs or two partial 14-bit (standard and extended) IDs per ID Filter Table element.
FLEXCAN_RX_FIFO_ID_FORMAT_C Four partial 8-bit Standard IDs per ID Filter Table element.
FLEXCAN_RX_FIFO_ID_FORMAT_D All frames rejected.

Definition at line 198 of file flexcan_driver.h.

17.53.4.6 enum flexcan_rx_fifo_id_filter_num_t

FlexCAN Rx FIFO filters number Implements : flexcan_rx_fifo_id_filter_num_t_Class.

Enumerator

- FLEXCAN_RX_FIFO_ID_FILTERS_8** 8 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_16 16 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_24 24 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_32 32 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_40 40 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_48 48 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_56 56 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_64 64 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_72 72 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_80 80 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_88 88 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_96 96 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_104 104 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_112 112 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_120 120 Rx FIFO Filters.
FLEXCAN_RX_FIFO_ID_FILTERS_128 128 Rx FIFO Filters.

Definition at line 168 of file flexcan_driver.h.

17.53.4.7 enum flexcan_rx_mask_type_t

FlexCAN Rx mask type. Implements : flexcan_rx_mask_type_t_Class.

Enumerator

- FLEXCAN_RX_MASK_GLOBAL** Rx global mask
FLEXCAN_RX_MASK_INDIVIDUAL Rx individual mask

Definition at line 190 of file flexcan_driver.h.

17.53.4.8 enum flexcan_rxfifo_transfer_type_t

The type of the RxFIFO transfer (interrupts/DMA). Implements : flexcan_rxfifo_transfer_type_t_Class.

Enumerator

- FLEXCAN_RXFIFO_USING_INTERRUPTS** Use interrupts for RxFIFO.

Definition at line 39 of file flexcan_driver.h.

17.53.5 Function Documentation

17.53.5.1 `status_t FLEXCAN_DRV_AbortTransfer (uint8_t instance, uint8_t mb_idx)`

Ends a non-blocking FlexCAN transfer early.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>mb_idx</i>	The index of the message buffer

Returns

STATUS_SUCCESS if successful; STATUS_CAN_NO_TRANSFER_IN_PROGRESS if no transfer was running

Definition at line 1950 of file flexcan_driver.c.

17.53.5.2 `status_t FLEXCAN_DRV_ConfigRemoteResponseMb (uint8_t instance, uint8_t mb_idx, const flexcan_data_info_t * tx_info, uint32_t msg_id, const uint8_t * mb_data)`

Configures a transmit message buffer for remote frame response.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>mb_idx</i>	Index of the message buffer
<i>tx_info</i>	Data info
<i>msg_id</i>	ID of the message to transmit
<i>mb_data</i>	Bytes of the FlexCAN message

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the index of the message buffer is invalid

Definition at line 931 of file flexcan_driver.c.

17.53.5.3 `void FLEXCAN_DRV_ConfigRxFifo (uint8_t instance, flexcan_rx_fifo_id_element_format_t id_format, const flexcan_id_table_t * id_filter_table)`

FlexCAN Rx FIFO field configuration.

Note

The number of elements in the ID filter table is defined by the following formula:

- for format A: the number of Rx FIFO ID filters
- for format B: twice the number of Rx FIFO ID filters
- for format C: four times the number of Rx FIFO ID filters The user must provide the exact number of elements in order to avoid any misconfiguration.

Each element in the ID filter table specifies an ID to be used as acceptance criteria for the FIFO as follows:

- for format A: In the standard frame format, bits 10 to 0 of the ID are used for frame identification. In the extended frame format, bits 28 to 0 are used.
- for format B: In the standard frame format, bits 10 to 0 of the ID are used for frame identification. In the extended frame format, only the 14 most significant bits (28 to 15) of the ID are compared to the 14 most significant bits (28 to 15) of the received ID.
- for format C: In both standard and extended frame formats, only the 8 most significant bits (7 to 0 for standard, 28 to 21 for extended) of the ID are compared to the 8 most significant bits (7 to 0 for standard, 28 to 21 for extended) of the received ID.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>id_format</i>	The format of the Rx FIFO ID Filter Table Elements
<i>id_filter_table</i>	The ID filter table elements which contain RTR bit, IDE bit, and Rx message ID

Definition at line 1175 of file flexcan_driver.c.

17.53.5.4 `status_t FLEXCAN_DRV_ConfigRxMb (uint8_t instance, uint8_t mb_idx, const flexcan_data_info_t * rx_info, uint32_t msg_id)`

FlexCAN receive message buffer field configuration.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>mb_idx</i>	Index of the message buffer
<i>rx_info</i>	Data info
<i>msg_id</i>	ID of the message to transmit

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the index of a message buffer is invalid;

Definition at line 1113 of file flexcan_driver.c.

17.53.5.5 `status_t FLEXCAN_DRV_ConfigTxMb (uint8_t instance, uint8_t mb_idx, const flexcan_data_info_t * tx_info, uint32_t msg_id)`

FlexCAN transmit message buffer field configuration.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>mb_idx</i>	Index of the message buffer
<i>tx_info</i>	Data info
<i>msg_id</i>	ID of the message to transmit

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the index of the message buffer is invalid

Definition at line 887 of file flexcan_driver.c.

17.53.5.6 `status_t FLEXCAN_DRV_Deinit (uint8_t instance)`

Shuts down a FlexCAN instance.

Parameters

<i>instance</i>	A FlexCAN instance number
-----------------	---------------------------

Returns

STATUS_SUCCESS if successful; STATUS_ERROR if failed

Definition at line 1379 of file flexcan_driver.c.

17.53.5.7 `void FLEXCAN_DRV_GetBitrate (uint8_t instance, flexcan_time_segment_t * bitrate)`

Gets the FlexCAN bit rate for standard frames or the arbitration phase of FD frames.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>bitrate</i>	A pointer to a variable for returning the FlexCAN bit rate settings

Definition at line 236 of file flexcan_driver.c.

17.53.5.8 uint32_t FLEXCAN_DRV_GetDefaultConfig (flexcan_user_config_t * config)

Gets the default configuration structure.

This function gets the default configuration structure, with the following settings:

- 16 message buffers
- flexible data rate disabled
- Rx FIFO disabled
- normal operation mode
- 8 byte payload size
- Protocol Engine clock = Oscillator clock
- bitrate of 500 Kbit/s (computed for sample point = 87.5)

Parameters

out	config	The configuration structure
-----	--------	-----------------------------

Returns

The bitrate for generated configuration structure.

Definition at line 2759 of file flexcan_driver.c.

17.53.5.9 uint32_t FLEXCAN_DRV_GetErrorStatus (uint8_t instance)

Returns reported error conditions.

Reports various error conditions detected in the reception and transmission of a CAN frame and some general status of the device.

Parameters

<i>instance</i>	The FlexCAN instance number.
-----------------	------------------------------

Returns

value of the Error and Status 1 register;

Definition at line 1931 of file flexcan_driver.c.

17.53.5.10 status_t FLEXCAN_DRV_GetTransferStatus (uint8_t instance, uint8_t mb_idx)

Returns whether the previous FlexCAN transfer has finished.

When performing an async transfer, call this function to ascertain the state of the current transfer: in progress (or busy) or complete (success).

Parameters

<i>instance</i>	The FlexCAN instance number.
<i>mb_idx</i>	The index of the message buffer.

Returns

STATUS_SUCCESS if successful; STATUS_BUSY if a resource is busy; STATUS_ERROR in case of a DMA error transfer;

Definition at line 1898 of file flexcan_driver.c.

```
17.53.5.11 status_t FLEXCAN_DRV_Init ( uint8_t instance, flexcan_state_t * state, const flexcan_user_config_t * data )
```

Initializes the FlexCAN peripheral.

This function initializes

Parameters

<i>instance</i>	A FlexCAN instance number
<i>state</i>	Pointer to the FlexCAN driver state structure.
<i>data</i>	The FlexCAN platform data

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the index of a message buffer is invalid; STATUS_ERROR if other error occurred

Definition at line 687 of file flexcan_driver.c.

```
17.53.5.12 void FLEXCAN_DRV_InstallErrorCallback ( uint8_t instance, flexcan_error_callback_t callback, void * callbackParam )
```

Installs an error callback function for the IRQ handler and enables error interrupts.

Parameters

<i>instance</i>	The FlexCAN instance number.
<i>callback</i>	The error callback function.
<i>callbackParam</i>	User parameter passed to the error callback function through the state parameter.

Definition at line 2469 of file flexcan_driver.c.

```
17.53.5.13 void FLEXCAN_DRV_InstallEventCallback ( uint8_t instance, flexcan_callback_t callback, void * callbackParam )
```

Installs a callback function for the IRQ handler.

Parameters

<i>instance</i>	The FlexCAN instance number.
<i>callback</i>	The callback function.
<i>callbackParam</i>	User parameter passed to the callback function through the state parameter.

Definition at line 2449 of file flexcan_driver.c.

```
17.53.5.14 status_t FLEXCAN_DRV_Receive ( uint8_t instance, uint8_t mb_idx, flexcan_msgbuff_t * data )
```

Receives a CAN frame using the specified message buffer.

This function receives a CAN frame using a configured message buffer. The function returns immediately. If a callback is installed, it will be invoked after the frame was received and read into the specified buffer.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>mb_idx</i>	Index of the message buffer
<i>data</i>	The FlexCAN receive message buffer data.

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the index of a message buffer is invalid; STATUS_BUSY if a resource is busy

Definition at line 1268 of file flexcan_driver.c.

17.53.5.15 `status_t FLEXCAN_DRV_ReceiveBlocking (uint8_t instance, uint8_t mb_idx, flexcan_msgbuff_t * data, uint32_t timeout_ms)`

Receives a CAN frame using the specified message buffer, in a blocking manner.

This function receives a CAN frame using a configured message buffer. The function blocks until either a frame was received, or the specified timeout expired.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>mb_idx</i>	Index of the message buffer
<i>data</i>	The FlexCAN receive message buffer data.
<i>timeout_ms</i>	A timeout for the transfer in milliseconds.

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the index of a message buffer is invalid; STATUS_BUSY if a resource is busy; STATUS_TIMEOUT if the timeout is reached

Definition at line 1209 of file flexcan_driver.c.

17.53.5.16 `status_t FLEXCAN_DRV_RxFifo (uint8_t instance, flexcan_msgbuff_t * data)`

Receives a CAN frame using the message FIFO.

This function receives a CAN frame using the Rx FIFO. The function returns immediately. If a callback is installed, it will be invoked after the frame was received and read into the specified buffer.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>data</i>	The FlexCAN receive message buffer data.

Returns

STATUS_SUCCESS if successful; STATUS_BUSY if a resource is busy; STATUS_ERROR if other error occurred

Definition at line 1358 of file flexcan_driver.c.

17.53.5.17 `status_t FLEXCAN_DRV_RxFifoBlocking (uint8_t instance, flexcan_msgbuff_t * data, uint32_t timeout_ms)`

Receives a CAN frame using the message FIFO, in a blocking manner.

This function receives a CAN frame using the Rx FIFO. The function blocks until either a frame was received, or the specified timeout expired.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>data</i>	The FlexCAN receive message buffer data.
<i>timeout_ms</i>	A timeout for the transfer in milliseconds.

Returns

STATUS_SUCCESS if successful; STATUS_BUSY if a resource is busy; STATUS_TIMEOUT if the timeout is reached; STATUS_ERROR if other error occurred

Definition at line 1298 of file flexcan_driver.c.

17.53.5.18 `status_t FLEXCAN_DRV_Send (uint8_t instance, uint8_t mb_idx, const flexcan_data_info_t * tx_info, uint32_t msg_id, const uint8_t * mb_data)`

Sends a CAN frame using the specified message buffer.

This function sends a CAN frame using a configured message buffer. The function returns immediately. If a callback is installed, it will be invoked after the frame was sent.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>mb_idx</i>	Index of the message buffer
<i>tx_info</i>	Data info
<i>msg_id</i>	ID of the message to transmit
<i>mb_data</i>	Bytes of the FlexCAN message.

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the index of a message buffer is invalid; STATUS_BUSY if a resource is busy

Definition at line 1070 of file flexcan_driver.c.

17.53.5.19 `status_t FLEXCAN_DRV_SendBlocking (uint8_t instance, uint8_t mb_idx, const flexcan_data_info_t * tx_info, uint32_t msg_id, const uint8_t * mb_data, uint32_t timeout_ms)`

Sends a CAN frame using the specified message buffer, in a blocking manner.

This function sends a CAN frame using a configured message buffer. The function blocks until either the frame was sent, or the specified timeout expired.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>mb_idx</i>	Index of the message buffer
<i>tx_info</i>	Data info
<i>msg_id</i>	ID of the message to transmit
<i>mb_data</i>	Bytes of the FlexCAN message
<i>timeout_ms</i>	A timeout for the transfer in milliseconds.

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the index of a message buffer is invalid; STATUS_BUSY if a resource is busy; STATUS_TIMEOUT if the timeout is reached

Definition at line 968 of file flexcan_driver.c.

17.53.5.20 `void FLEXCAN_DRV_SetBitrate (uint8_t instance, const flexcan_time_segment_t * bitrate)`

Sets the FlexCAN bit rate for standard frames or the arbitration phase of FD frames.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>bitrate</i>	A pointer to the FlexCAN bit rate settings.

Definition at line 159 of file flexcan_driver.c.

17.53.5.21 void FLEXCAN_DRV_SetRxFifoGlobalMask (uint8_t *instance*, flexcan_msgbuff_id_type_t *id_type*, uint32_t *mask*)

Sets the FlexCAN Rx FIFO global mask (standard or extended). This mask is applied to all filters ID regardless the ID Filter format.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>id_type</i>	Standard ID or extended ID mask type
<i>mask</i>	Mask Value. In FIFO mode, when using ID Format A or B, bit 31 encodes RTR check and bit 30 encodes IDE check respectively. For ID Format C, bits 31 and 30 are ignored.

Definition at line 317 of file flexcan_driver.c.

17.53.5.22 status_t FLEXCAN_DRV_SetRxIndividualMask (uint8_t *instance*, flexcan_msgbuff_id_type_t *id_type*, uint8_t *mb_idx*, uint32_t *mask*)

Sets the FlexCAN Rx individual mask (standard or extended).

Parameters

<i>instance</i>	A FlexCAN instance number
<i>id_type</i>	A standard ID or an extended ID
<i>mb_idx</i>	Index of the message buffer
<i>mask</i>	Mask Value. In FIFO mode, when using ID Format A or B, bit 31 encodes RTR check and bit 30 encodes IDE check respectively. For ID Format C, bits 31 and 30 are ignored.

Returns

STATUS_SUCCESS if successful; STATUS_CAN_BUFF_OUT_OF_RANGE if the index of the message buffer is invalid.

Definition at line 504 of file flexcan_driver.c.

17.53.5.23 void FLEXCAN_DRV_SetRxMaskType (uint8_t *instance*, flexcan_rx_mask_type_t *type*)

Sets the Rx masking type.

Parameters

<i>instance</i>	A FlexCAN instance number
<i>type</i>	The FlexCAN RX mask type

Definition at line 288 of file flexcan_driver.c.

17.53.5.24 void FLEXCAN_DRV_SetRxMb14Mask (uint8_t *instance*, flexcan_msgbuff_id_type_t *id_type*, uint32_t *mask*)

Sets the FlexCAN Rx MB 14 mask (standard or extended).

Parameters

<i>instance</i>	A FlexCAN instance number
-----------------	---------------------------

<i>id_type</i>	Standard ID or extended ID
<i>mask</i>	Mask value

Definition at line 416 of file flexcan_driver.c.

17.53.5.25 void FLEXCAN_DRV_SetRxMb15Mask (uint8_t *instance*, flexcan_msgbuff_id_type_t *id_type*, uint32_t *mask*)

Sets the FlexCAN Rx MB 15 mask (standard or extended).

Parameters

<i>instance</i>	A FlexCAN instance number
<i>id_type</i>	Standard ID or extended ID
<i>mask</i>	Mask value

Definition at line 460 of file flexcan_driver.c.

17.53.5.26 void FLEXCAN_DRV_SetRxMbGlobalMask (uint8_t *instance*, flexcan_msgbuff_id_type_t *id_type*, uint32_t *mask*)

Sets the FlexCAN Rx MB global mask (standard or extended).

Parameters

<i>instance</i>	A FlexCAN instance number
<i>id_type</i>	Standard ID or extended ID
<i>mask</i>	Mask value

Definition at line 372 of file flexcan_driver.c.

17.54 FlexIO Common Driver

17.54.1 Detailed Description

Common services for FlexIO drivers.

The Flexio Common driver layer contains services used by all Flexio drivers. The need for this layer derives from the requirement to allow multiple Flexio drivers to run in parallel on the same device, to the extent that enough hardware resources (shifters and timers) are available.

Functionality

The Flexio Common driver layer provides functions for device initialization and reset. Before using any Flexio driver the device must first be initialized using function [FLEXIO_DRV_InitDevice\(\)](#). Then any number of Flexio drivers can be initialized on the same device, to the extent that enough hardware resources (shifters and timers) are available. Driver initialization functions will return STATUS_ERROR if not enough resources are available for a new driver.

Important Notes

Calling any Flexio common function will destroy any driver that is active on that device. Normally these functions should be called only when there are no active driver instances on the device.

Enumerations

- enum [flexio_driver_type_t](#) { [FLEXIO_DRIVER_TYPE_INTERRUPTS](#) = 0U, [FLEXIO_DRIVER_TYPE_POLLING](#) = 1U, [FLEXIO_DRIVER_TYPE_DMA](#) = 2U }

Driver type: interrupts/polling/DMA Implements : flexio_driver_type_t Class.

FLEXIO_I2C Driver

- status_t [FLEXIO_DRV_InitDevice](#) (uint32_t instance, flexio_device_state_t *deviceState)
Initializes the FlexIO device.
- status_t [FLEXIO_DRV_DeinitDevice](#) (uint32_t instance)
De-initializes the FlexIO device.
- status_t [FLEXIO_DRV_Reset](#) (uint32_t instance)
Resets the FlexIO device.

17.54.2 Enumeration Type Documentation

17.54.2.1 enum flexio_driver_type_t

Driver type: interrupts/polling/DMA Implements : flexio_driver_type_t Class.

Enumerator

FLEXIO_DRIVER_TYPE_INTERRUPTS Driver uses interrupts for data transfers

FLEXIO_DRIVER_TYPE_POLLING Driver is based on polling

FLEXIO_DRIVER_TYPE_DMA Driver uses DMA for data transfers

Definition at line 46 of file flexio.h.

17.54.3 Function Documentation

17.54.3.1 status_t FLEXIO_DRV_DeinitDevice (uint32_t instance)

De-initializes the FlexIO device.

This function de-initializes the FlexIO device.

Parameters

<i>instance</i>	FLEXIO peripheral instance number
-----------------	-----------------------------------

Returns

Error or success status returned by API

Definition at line 125 of file flexio_common.c.

17.54.3.2 `status_t FLEXIO_DRV_InitDevice (uint32_t instance, flexio_device_state_t * deviceState)`

Initializes the FlexIO device.

This function resets the FlexIO device, enables interrupts in interrupt manager and enables the device.

Parameters

<i>instance</i>	FLEXIO peripheral instance number
<i>deviceState</i>	Pointer to the FLEXIO device context structure. The driver uses this memory area for its internal logic. The application must make no assumptions about the content of this structure, and must not free this memory until the device is de-initialized using FLEXIO_DRV_DeinitDevice() .

Returns

Error or success status returned by API

Definition at line 86 of file flexio_common.c.

17.54.3.3 `status_t FLEXIO_DRV_Reset (uint32_t instance)`

Resets the FlexIO device.

This function resets the FlexIO device.

Parameters

<i>instance</i>	FLEXIO peripheral instance number
-----------------	-----------------------------------

Returns

Error or success status returned by API

Definition at line 150 of file flexio_common.c.

17.55 FlexIO I2C Driver

17.55.1 Detailed Description

I2C communication over FlexIO module (FLEXIO_I2C)

The FLEXIO_I2C Driver allows communication on an I2C bus using the FlexIO module in the S32K1xx processors.

Features

- Master operation only
- Interrupt, DMA or polling mode
- Provides blocking and non-blocking transmit and receive functions
- 7-bit addressing
- Clock stretching
- Configurable baud rate

Functionality

Before using any FlexIO driver the device must first be initialized using function `FLEXIO_DRV_InitDevice`. Then the FLEXIO_I2C Driver must be initialized using functions `FLEXIO_I2C_DRV_MasterInit()`. It is possible to use more driver instances on the same FlexIO device, as long as sufficient resources are available. Different driver instances on the same FlexIO device can function independently of each other. When it is no longer needed, the driver can be de-initialized, using `FLEXIO_I2C_DRV_MasterDeinit()`. This will release the hardware resources, allowing other driver instances to be initialized.

Master Mode

Master Mode provides functions for transmitting or receiving data to/from any I2C slave. Slave address and baud rate are provided at initialization time through the master configuration structure, but they can be changed at runtime by using `FLEXIO_I2C_DRV_MasterSetBaudRate()` or `FLEXIO_I2C_DRV_MasterSetSlaveAddr()`. Note that due to module limitation not any baud rate can be achieved. The driver will set a baud rate as close as possible to the requested baud rate, but there may still be substantial differences, for example if requesting a high baud rate while using a low-frequency FlexIO clock. The application should call `FLEXIO_I2C_DRV_MasterGetBaudRate()` after `FLEXIO_I2C_DRV_MasterSetBaudRate()` to check what baud rate was actually set.

To send or receive data to/from the currently configured slave address, use functions `FLEXIO_I2C_DRV_MasterSendData()` or `FLEXIO_I2C_DRV_MasterReceiveData()` (or their blocking counterparts). Parameter `sendStop` can be used to chain multiple transfers with repeated START condition between them, for example when sending a command and then immediately receiving a response. The application should ensure that any send or receive transfer with `sendStop` set to `false` is followed by another transfer. The last transfer from a chain should always have `sendStop` set to `true`. This driver does not support continuous send/receive using a user callback function. The callback function is only used to signal the end of a transfer.

Blocking operations will return only when the transfer is completed, either successfully or with error. Non-blocking operations will initiate the transfer and return `STATUS_SUCCESS`, but the module is still busy with the transfer and another transfer can't be initiated until the current transfer is complete. The application will be notified through the user callback when the transfer completes, or it can check the status of the current transfer by calling `FLEXIO_I2C_DRV_MasterGetStatus()`. If the transfer is still ongoing this function will return `STATUS_BUSY`. If the transfer is completed, the function will return either `STATUS_SUCCESS` or an error code, depending on the outcome of the last transfer.

The driver supports interrupt, DMA and polling mode. In polling mode the function `FLEXIO_I2C_DRV_MasterGetStatus()` ensures the progress of the transfer by checking and handling transmit and receive events reported by the FlexIO module. The application should ensure that this function is called often enough (at least once per transferred byte) to avoid Tx underflows or Rx overflows. In DMA mode the DMA channels that will be used by the driver are received through the configuration structure. The channels must be initialized by the application before the flexio_i2c driver is initialized. The flexio_i2c driver will only set the DMA request source.

Important Notes

- There is one limitation of flexio_i2c which no Stop condition is generated when aborting a transfer due to NACK reception.
- Before using the FLEXIO_I2C Driver the FlexIO clock must be configured. Refer to Clock Manager for clock configuration.
- Before using the FLEXIO_I2C Driver the pins must be routed to the FlexIO module. Refer to PINS Driver for pin routing configuration. Note that any of the available FlexIO pins can be used for SDA and SCL (configurable at initialization time).
- The driver enables the interrupts for the corresponding FlexIO module, but any interrupt priority setting must be done by the application.
- Aborting a transfer with the function [FLEXIO_I2C_DRV_MasterTransferAbort\(\)](#) can't generally be done safely due to device limitation; there is no way to know the exact stage of the transfer, and if we disable the module during the ACK bit (transmit) or during a 0 data bit (receive) the slave will hold the SDA line low forever and block the I2C bus. Therefore this function should only be used in extreme circumstances, and the application must have a way to reset the I2C slave. NACK reception is the only exception, as there is no slave to hold the line low, so in this case the driver will automatically abort the transfer.
- The module can handle clock stretching done by the slave, but will not do clock stretching when the application does not provide data fast enough, so Tx underflows and Rx overflows are possible. This can be an issue especially in polling mode if the function [FLEXIO_I2C_DRV_MasterGetStatus\(\)](#) is not called often enough.
- Due to device limitations it is not always possible to tell the difference between NACK reception and receiver overflow. When in doubt, the driver will treat these events as overflow and continue the transfer, in order to avoid the risk of blocking the i2c bus.
- The driver does not support multi-master mode. It does not detect arbitration loss condition.
- Timeout feature for blocking transfers does not work in polling mode.
- This driver needs two shifters and two timers for its operation. Initialization will fail if there are not enough shifters and timers available on the FlexIO device.
- This driver needs two DMA channels for its operation when it is initialized in DMA mode. The DMA channels must be initialized by the application before initializing the driver. Refer to EDMA driver for DMA channels initialization.
- If the application uses an RTOS, this driver uses a semaphore for blocking transfers. Initialization will fail if the semaphore cannot be created. If the driver uses polling mode no semaphore is used.
- If the application uses an RTOS, the FlexIO drivers use a mutex for channel allocation. Only one mutex per device is needed, not per driver instance. Device initialization will fail if the mutex cannot be created.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\flexio\flexio_common.c
${S32SDK_PATH}\platform\drivers\src\flexio\flexio_i2c_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc
${S32SDK_PATH}\platform\drivers\src\flexio
```


Compile symbols

No special symbols are required for this component

Dependencies

Clock Manager OS Interface (OSIF) Interrupt Manager (Interrupt) Enhanced Direct Memory Access (eDMA)

Data Structures

- struct [flexio_i2c_master_user_config_t](#)
Master configuration structure. [More...](#)
- struct [flexio_i2c_master_state_t](#)
Master internal context structure. [More...](#)

FLEXIO_I2C Driver

- status_t [FLEXIO_I2C_DRV_MasterInit](#) (uint32_t instance, const [flexio_i2c_master_user_config_t](#) *userConfigPtr, [flexio_i2c_master_state_t](#) *master)
Initialize the FLEXIO_I2C master mode driver.
- status_t [FLEXIO_I2C_DRV_MasterDeinit](#) ([flexio_i2c_master_state_t](#) *master)
De-initialize the FLEXIO_I2C master mode driver.
- status_t [FLEXIO_I2C_DRV_MasterSetBaudRate](#) ([flexio_i2c_master_state_t](#) *master, uint32_t baudRate)
Set the baud rate for any subsequent I2C communication.
- status_t [FLEXIO_I2C_DRV_MasterGetBaudRate](#) ([flexio_i2c_master_state_t](#) *master, uint32_t *baudRate)
Get the currently configured baud rate.
- status_t [FLEXIO_I2C_DRV_MasterSetSlaveAddr](#) ([flexio_i2c_master_state_t](#) *master, const uint16_t address)
Set the slave address for any subsequent I2C communication.
- status_t [FLEXIO_I2C_DRV_MasterSendData](#) ([flexio_i2c_master_state_t](#) *master, const uint8_t *txBuff, uint32_t txSize, bool sendStop)
Perform a non-blocking send transaction on the I2C bus.
- status_t [FLEXIO_I2C_DRV_MasterSendDataBlocking](#) ([flexio_i2c_master_state_t](#) *master, const uint8_t *txBuff, uint32_t txSize, bool sendStop, uint32_t timeout)
Perform a blocking send transaction on the I2C bus.
- status_t [FLEXIO_I2C_DRV_MasterReceiveData](#) ([flexio_i2c_master_state_t](#) *master, uint8_t *rxBuff, uint32_t rxSize, bool sendStop)
Perform a non-blocking receive transaction on the I2C bus.
- status_t [FLEXIO_I2C_DRV_MasterReceiveDataBlocking](#) ([flexio_i2c_master_state_t](#) *master, uint8_t *rxBuff, uint32_t rxSize, bool sendStop, uint32_t timeout)
Perform a blocking receive transaction on the I2C bus.
- status_t [FLEXIO_I2C_DRV_MasterTransferAbort](#) ([flexio_i2c_master_state_t](#) *master)
Aborts a non-blocking I2C master transaction.
- status_t [FLEXIO_I2C_DRV_MasterGetStatus](#) ([flexio_i2c_master_state_t](#) *master, uint32_t *bytesRemaining)
Get the status of the current non-blocking I2C master transaction.
- void [FLEXIO_I2C_DRV_GetDefaultConfig](#) ([flexio_i2c_master_user_config_t](#) *userConfigPtr)
Returns default configuration structure for FLEXIO_I2C.
- status_t [FLEXIO_I2C_DRV_GenerateNineClock](#) ([flexio_i2c_master_state_t](#) *master)
Generate nine clock on SCL line to free SDA line.
- status_t [FLEXIO_I2C_DRV_StatusGenerateNineClock](#) ([flexio_i2c_master_state_t](#) *master)
Indicate the generation nine clock is done or not.
- bool [FLEXIO_I2C_DRV_GetBusStatus](#) (const [flexio_i2c_master_state_t](#) *master, bool sdaLine)
Check status whether SDA or SCL line be low or high.

17.55.2 Data Structure Documentation

17.55.2.1 struct flexio_i2c_master_user_config_t

Master configuration structure.

This structure is used to provide configuration parameters for the flexio_i2c master at initialization time. Implements : flexio_i2c_master_user_config_t_Class

Definition at line 84 of file flexio_i2c_driver.h.

Data Fields

- uint16_t [slaveAddress](#)
- [flexio_driver_type_t](#) driverType
- uint32_t [baudRate](#)
- uint8_t [sdaPin](#)
- uint8_t [sclPin](#)
- i2c_master_callback_t [callback](#)
- void * [callbackParam](#)
- uint8_t [rxDMAChannel](#)
- uint8_t [txDMAChannel](#)

Field Documentation

17.55.2.1.1 uint32_t baudRate

Baud rate in hertz

Definition at line 88 of file flexio_i2c_driver.h.

17.55.2.1.2 i2c_master_callback_t callback

User callback function. Note that this function will be called from the interrupt service routine, so its execution time should be as small as possible. It can be NULL if it is not needed

Definition at line 91 of file flexio_i2c_driver.h.

17.55.2.1.3 void* callbackParam

Parameter for the callback function

Definition at line 95 of file flexio_i2c_driver.h.

17.55.2.1.4 flexio_driver_type_t driverType

Driver type: interrupts/polling/DMA

Definition at line 87 of file flexio_i2c_driver.h.

17.55.2.1.5 uint8_t rxDMAChannel

Rx DMA channel number. Only used in DMA mode

Definition at line 96 of file flexio_i2c_driver.h.

17.55.2.1.6 uint8_t sclPin

Flexio pin to use as I2C SCL pin

Definition at line 90 of file flexio_i2c_driver.h.

17.55.2.1.7 uint8_t sdaPin

Flexio pin to use as I2C SDA pin

Definition at line 89 of file flexio_i2c_driver.h.

17.55.2.1.8 uint16_t slaveAddress

Slave address, 7-bit

Definition at line 86 of file flexio_i2c_driver.h.

17.55.2.1.9 uint8_t txDMAChannel

Tx DMA channel number. Only used in DMA mode

Definition at line 97 of file flexio_i2c_driver.h.

17.55.2.2 struct flexio_i2c_master_state_t

Master internal context structure.

This structure is used by the driver for its internal logic. It must be provided by the application through the [FLEXIO_I2C_DRV_MasterInit\(\)](#) function, then it cannot be freed until the driver is de-initialized using [FLEXIO_I2C_DRV_MasterDeinit\(\)](#). The application should make no assumptions about the content of this structure.

Definition at line 109 of file flexio_i2c_driver.h.

17.55.3 Function Documentation

17.55.3.1 status_t FLEXIO_I2C_DRV_GenerateNineClock (flexio_i2c_master_state_t * master)

Generate nine clock on SCL line to free SDA line.

This function should be called when SDA line be stuck in low.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
---------------	--

Returns

STATUS_BUSY: Driver is transferring data, STATUS_SUCCESS: Function started generating clock

Definition at line 1681 of file flexio_i2c_driver.c.

17.55.3.2 bool FLEXIO_I2C_DRV_GetBusStatus (const flexio_i2c_master_state_t * master, bool sdaLine)

Check status whether SDA or SCL line be low or high.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
<i>sdaLine</i>	true - function return status of SDA line. false - function return status of SCL line.

Returns

true: Pin selected is high, false: Pin selected is low

Definition at line 1766 of file flexio_i2c_driver.c.

17.55.3.3 void FLEXIO_I2C_DRV_GetDefaultConfig (flexio_i2c_master_user_config_t * userConfigPtr)

Returns default configuration structure for FLEXIO_I2C.

Parameters

<i>userConfigPtr</i>	Pointer to the FLEXIO_I2C user configuration structure.
----------------------	---

Definition at line 1658 of file flexio_i2c_driver.c.

17.55.3.4 `status_t FLEXIO_I2C_DRV_MasterDeinit (flexio_i2c_master_state_t * master)`

De-initialize the FLEXIO_I2C master mode driver.

This function de-initializes the FLEXIO_I2C driver in master mode. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
---------------	--

Returns

Error or success status returned by API

Definition at line 1286 of file flexio_i2c_driver.c.

17.55.3.5 `status_t FLEXIO_I2C_DRV_MasterGetBaudRate (flexio_i2c_master_state_t * master, uint32_t * baudRate)`

Get the currently configured baud rate.

This function returns the currently configured I2C baud rate.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
<i>baudRate</i>	the current baud rate in hertz

Returns

Error or success status returned by API

Definition at line 1356 of file flexio_i2c_driver.c.

17.55.3.6 `status_t FLEXIO_I2C_DRV_MasterGetStatus (flexio_i2c_master_state_t * master, uint32_t * bytesRemaining)`

Get the status of the current non-blocking I2C master transaction.

This function returns the current status of a non-blocking I2C master transaction. A return code of STATUS_BUSY means the transfer is still in progress. Otherwise the function returns a status reflecting the outcome of the last transfer. When the driver is initialized in polling mode this function also advances the transfer by checking and handling the transmit and receive events, so it must be called frequently to avoid overflows or underflows.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
<i>bytesRemaining</i>	The remaining number of bytes to be transferred

Returns

Error or success status returned by API

Definition at line 1603 of file flexio_i2c_driver.c.

17.55.3.7 `status_t FLEXIO_I2C_DRV_MasterInit (uint32_t instance, const flexio_i2c_master_user_config_t * userConfigPtr, flexio_i2c_master_state_t * master)`

Initialize the FLEXIO_I2C master mode driver.

This function initializes the FLEXIO_I2C driver in master mode.

Parameters

<i>instance</i>	FLEXIO peripheral instance number
<i>userConfigPtr</i>	Pointer to the FLEXIO_I2C master user configuration structure. The function reads configuration data from this structure and initializes the driver accordingly. The application may free this structure after the function returns.
<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure. The driver uses this memory area for its internal logic. The application must make no assumptions about the content of this structure, and must not free this memory until the driver is de-initialized using FLEXIO_I2C_DRV_MasterDeinit() .

Returns

Error or success status returned by API

Definition at line 1195 of file flexio_i2c_driver.c.

17.55.3.8 `status_t FLEXIO_I2C_DRV_MasterReceiveData (flexio_i2c_master_state_t * master, uint8_t * rxBuff, uint32_t rxSize, bool sendStop)`

Perform a non-blocking receive transaction on the I2C bus.

This function starts the reception of a block of data from the currently configured slave address and returns immediately. The rest of the transmission is handled by the interrupt service routine (if the driver is initialized in interrupt mode) or by the [FLEXIO_I2C_DRV_MasterGetStatus](#) function (if the driver is initialized in polling mode). Use [FLEXIO_I2C_DRV_MasterGetStatus\(\)](#) to check the progress of the reception.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred
<i>sendStop</i>	specifies whether or not to generate stop condition after the reception

Returns

Error or success status returned by API

Definition at line 1494 of file flexio_i2c_driver.c.

17.55.3.9 `status_t FLEXIO_I2C_DRV_MasterReceiveDataBlocking (flexio_i2c_master_state_t * master, uint8_t * rxBuff, uint32_t rxSize, bool sendStop, uint32_t timeout)`

Perform a blocking receive transaction on the I2C bus.

This function receives a block of data from the currently configured slave address, and only returns when the transmission is complete.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred
<i>sendStop</i>	specifies whether or not to generate stop condition after the reception
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 1523 of file flexio_i2c_driver.c.

17.55.3.10 `status_t FLEXIO_I2C_DRV_MasterSendData (flexio_i2c_master_state_t * master, const uint8_t * txBuff, uint32_t txSize, bool sendStop)`

Perform a non-blocking send transaction on the I2C bus.

This function starts the transmission of a block of data to the currently configured slave address and returns immediately. The rest of the transmission is handled by the interrupt service routine (if the driver is initialized in interrupt mode) or by the `FLEXIO_I2C_DRV_MasterGetStatus` function (if the driver is initialized in polling mode). Use `FLEXIO_I2C_DRV_MasterGetStatus()` to check the progress of the transmission.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred
<i>sendStop</i>	specifies whether or not to generate stop condition after the transmission

Returns

Error or success status returned by API

Definition at line 1417 of file `flexio_i2c_driver.c`.

17.55.3.11 `status_t FLEXIO_I2C_DRV_MasterSendDataBlocking (flexio_i2c_master_state_t * master, const uint8_t * txBuff, uint32_t txSize, bool sendStop, uint32_t timeout)`

Perform a blocking send transaction on the I2C bus.

This function sends a block of data to the currently configured slave address, and only returns when the transmission is complete.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred
<i>sendStop</i>	specifies whether or not to generate stop condition after the transmission
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 1446 of file `flexio_i2c_driver.c`.

17.55.3.12 `status_t FLEXIO_I2C_DRV_MasterSetBaudRate (flexio_i2c_master_state_t * master, uint32_t baudRate)`

Set the baud rate for any subsequent I2C communication.

This function sets the baud rate (SCL frequency) for the I2C master. Note that due to module limitation not any baud rate can be achieved. The driver will set a baud rate as close as possible to the requested baud rate, but there may still be substantial differences, for example if requesting a high baud rate while using a low-frequency FlexIO clock. The application should call `FLEXIO_I2C_DRV_MasterGetBaudRate()` after `FLEXIO_I2C_DRV_MasterSetBaudRate()` to check what baud rate was actually set.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
---------------	--

<i>baudRate</i>	the desired baud rate in hertz
-----------------	--------------------------------

Returns

Error or success status returned by API

Definition at line 1312 of file flexio_i2c_driver.c.

17.55.3.13 `status_t FLEXIO_I2C_DRV_MasterSetSlaveAddr (flexio_i2c_master_state_t * master, const uint16_t address)`

Set the slave address for any subsequent I2C communication.

This function sets the slave address which will be used for any future transfer.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
<i>address</i>	slave address, 7-bit

Returns

Error or success status returned by API

Definition at line 1395 of file flexio_i2c_driver.c.

17.55.3.14 `status_t FLEXIO_I2C_DRV_MasterTransferAbort (flexio_i2c_master_state_t * master)`

Aborts a non-blocking I2C master transaction.

This function aborts a non-blocking I2C transfer.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
---------------	--

Returns

Error or success status returned by API

Definition at line 1571 of file flexio_i2c_driver.c.

17.55.3.15 `status_t FLEXIO_I2C_DRV_StatusGenerateNineClock (flexio_i2c_master_state_t * master)`

Indicate the generation nine clock is done or not.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2C master driver context structure.
---------------	--

Returns

STATUS_BUSY: Clock generation not done yet, STATUS_SUCCESS: Device finished generating nine clock

Definition at line 1730 of file flexio_i2c_driver.c.

17.56 FlexIO I2S Driver

17.56.1 Detailed Description

I2S communication over FlexIO module (FLEXIO_I2S)

The FLEXIO_I2S Driver allows communication on an I2S bus using the FlexIO module in the S32K1xx processors.

Features

- Master or slave operation
- Interrupt, DMA or polling mode
- Provides blocking and non-blocking transmit and receive functions
- Configurable baud rate and bit count

Functionality

Before using any Flexio driver the device must first be initialized using function `FLEXIO_DRV_InitDevice`. Then the FLEXIO_I2S Driver must be initialized, using functions `FLEXIO_I2S_DRV_MasterInit()` or `FLEXIO_I2S_DRV_SlaveInit()`. It is possible to use more driver instances on the same FlexIO device, as long as sufficient resources are available. Different driver instances on the same FlexIO device can function independently of each other. When it is no longer needed, the driver can be de-initialized, using `FLEXIO_I2S_DRV_MasterDeinit()` or `FLEXIO_I2S_DRV_SlaveDeinit()`. This will release the hardware resources, allowing other driver instances to be initialized.

Master Mode

Master Mode provides functions for transmitting or receiving data to/from any I2S slave. The number of bits per word and the baud rate are provided at initialization time through the master configuration structure, but they can be changed at runtime by using `FLEXIO_I2S_DRV_MasterSetConfig()`. Note that due to module limitation not any baud rate can be achieved. The driver will set a baud rate as close as possible to the requested baud rate, but there may still be substantial differences, for example if requesting a high baud rate while using a low-frequency FlexIO clock. The application should call `FLEXIO_I2S_DRV_MasterGetBaudRate()` to check what baud rate was actually set.

To send or receive data to/from the currently configured slave address, use functions `FLEXIO_I2S_DRV_MasterSendData()` or `FLEXIO_I2S_DRV_MasterReceiveData()` (or their blocking counterparts). The driver is not full-duplex, only one direction (send or receive) can be used at one time. It is possible to configure both Rx and Tx pin to use the same Flexio pin.

Continuous send/receive can be realized by registering a user callback function. When the driver completes the transmission or reception of the current buffer, it will invoke the user callback with an appropriate event. The callback function can use `FLEXIO_I2S_DRV_MasterSetTxBuffer()` or `FLEXIO_I2S_DRV_MasterSetRxBuffer()` to provide a new buffer.

Blocking operations will return only when the transfer is completed, either successfully or with error. Non-blocking operations will initiate the transfer and return `STATUS_SUCCESS`, but the module is still busy with the transfer and another transfer can't be initiated until the current transfer is complete. The application will be notified through the user callback when the transfer completes, or it can check the status of the current transfer by calling `FLEXIO_I2S_DRV_MasterGetStatus()`. If the transfer is still ongoing this function will return `STATUS_BUSY`. If the transfer is completed, the function will return either `STATUS_SUCCESS` or an error code, depending on the outcome of the last transfer.

The driver supports interrupt, DMA and polling mode. In polling mode the function `FLEXIO_I2S_DRV_MasterGetStatus()` ensures the progress of the transfer by checking and handling transmit and receive events reported by the FlexIO module. The application should ensure that this function is called often enough (at least once per transferred byte) to avoid Tx underflows or Rx overflows. In DMA mode the DMA channels that will be used by the driver are received through the configuration structure. The channels must be initialized by the application before the flexio_i2s driver is initialized. The flexio_i2s driver will only set the DMA request source.

Slave Mode

Slave Mode is very similar to master mode, the main difference being that the [FLEXIO_I2S_DRV_SlaveInit\(\)](#) function initializes the FlexIO module to use the clock signal received from the master instead of generating it. Consequently, there is no baud rate setting in slave mode. Other than that, the slave mode offers a similar interface to the master mode. [FLEXIO_I2S_DRV_MasterSendData\(\)](#) or [FLEXIO_I2S_DRV_MasterReceiveData\(\)](#) (or their blocking counterparts) can be used to initiate transfers, and [FLEXIO_I2S_DRV_SlaveGetStatus\(\)](#) is used to check the status of the transfer and advance the transfer in polling mode. All other specifications from the Master Mode description apply for Slave Mode too.

Important Notes

- Before using the FLEXIO_I2S Driver the FlexIO clock must be configured. Refer to Clock Manager for clock configuration.
- Before using the FLEXIO_I2S Driver the pins must be routed to the FlexIO module. Refer to PINS Driver for pin routing configuration. Note that any of the available FlexIO pins can be used for any of the TX, RX, SCK and WS signals (configurable at initialization time). If more than one driver instance is used on the same Flexio module, it is the responsibility of the application to ensure there are no conflicts between pins.
- The driver enables the interrupts for the corresponding FlexIO module, but any interrupt priority setting must be done by the application.
- Timeout feature for blocking transfers does not work in polling mode.
- This driver needs two shifters and two timers for its operation. Initialization will fail if there are not enough shifters and timers available on the FlexIO device.
- This driver needs two DMA channels for its operation when it is initialized in DMA mode. The DMA channels must be initialized by the application before initializing the driver. Refer to EDMA driver for DMA channels initialization.
- If the application uses an RTOS, this driver uses a semaphore for blocking transfers. Initialization will fail if the semaphore cannot be created. If the driver uses polling mode no semaphore is used.
- If the application uses an RTOS, the FlexIO drivers use a mutex for channel allocation. Only one mutex per device is needed, not per driver instance. Device initialization will fail if the mutex cannot be created.
- For transfers where the data size is more than 1 byte (bitsWidth is greater than 8) the driver assumes that the data buffers are defined with the proper type (uint16_t or uint32_t) and are properly aligned.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\flexio\flexio_common.c
${S32SDK_PATH}\platform\drivers\src\flexio\flexio_i2s_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc
${S32SDK_PATH}\platform\drivers\src\flexio
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager OS Interface \(OSIF\)](#) [Interrupt Manager \(Interrupt\)](#) [Enhanced Direct Memory Access \(eDMA\)](#)

Data Structures

- struct [flexio_i2s_master_user_config_t](#)
Master configuration structure. [More...](#)
- struct [flexio_i2s_slave_user_config_t](#)
Slave configuration structure. [More...](#)
- struct [flexio_i2s_master_state_t](#)
Master internal context structure. [More...](#)

Typedefs

- typedef [flexio_i2s_master_state_t](#) [flexio_i2s_slave_state_t](#)
Slave internal context structure.

FLEXIO_I2S Driver

- status_t [FLEXIO_I2S_DRV_MasterInit](#) (uint32_t instance, const [flexio_i2s_master_user_config_t](#) *userConfigPtr, [flexio_i2s_master_state_t](#) *master)
Initialize the FLEXIO_I2S master mode driver.
- status_t [FLEXIO_I2S_DRV_MasterDeinit](#) ([flexio_i2s_master_state_t](#) *master)
De-initialize the FLEXIO_I2S master mode driver.
- status_t [FLEXIO_I2S_DRV_MasterSetConfig](#) ([flexio_i2s_master_state_t](#) *master, uint32_t baudRate, uint8_t bitsWidth)
Set the baud rate and bit width for any subsequent I2S communication.
- status_t [FLEXIO_I2S_DRV_MasterGetBaudRate](#) ([flexio_i2s_master_state_t](#) *master, uint32_t *baudRate)
Get the currently configured baud rate.
- status_t [FLEXIO_I2S_DRV_MasterSendData](#) ([flexio_i2s_master_state_t](#) *master, const uint8_t *txBuff, uint32_t txSize)
Perform a non-blocking send transaction on the I2S bus.
- status_t [FLEXIO_I2S_DRV_MasterSendDataBlocking](#) ([flexio_i2s_master_state_t](#) *master, const uint8_t *txBuff, uint32_t txSize, uint32_t timeout)
Perform a blocking send transaction on the I2S bus.
- status_t [FLEXIO_I2S_DRV_MasterReceiveData](#) ([flexio_i2s_master_state_t](#) *master, uint8_t *rxBuff, uint32_t rxSize)
Perform a non-blocking receive transaction on the I2S bus.
- status_t [FLEXIO_I2S_DRV_MasterReceiveDataBlocking](#) ([flexio_i2s_master_state_t](#) *master, uint8_t *rxBuff, uint32_t rxSize, uint32_t timeout)
Perform a blocking receive transaction on the I2S bus.
- status_t [FLEXIO_I2S_DRV_MasterTransferAbort](#) ([flexio_i2s_master_state_t](#) *master)
Aborts a non-blocking I2S master transaction.
- status_t [FLEXIO_I2S_DRV_MasterGetStatus](#) ([flexio_i2s_master_state_t](#) *master, uint32_t *bytesRemaining)
Get the status of the current non-blocking I2S master transaction.
- status_t [FLEXIO_I2S_DRV_MasterSetRxBuffer](#) ([flexio_i2s_master_state_t](#) *master, uint8_t *rxBuff, uint32_t rxSize)
Provide a buffer for receiving data.
- status_t [FLEXIO_I2S_DRV_MasterSetTxBuffer](#) ([flexio_i2s_master_state_t](#) *master, const uint8_t *txBuff, uint32_t txSize)
Provide a buffer for transmitting data.
- status_t [FLEXIO_I2S_DRV_Slavelnit](#) (uint32_t instance, const [flexio_i2s_slave_user_config_t](#) *userConfigPtr, [flexio_i2s_slave_state_t](#) *slave)
Initialize the FLEXIO_I2S slave mode driver.

- status_t [FLEXIO_I2S_DRV_SlaveDeinit](#) ([flexio_i2s_slave_state_t](#) *slave)
De-initialize the FLEXIO_I2S slave mode driver.
- status_t [FLEXIO_I2S_DRV_SlaveSetConfig](#) ([flexio_i2s_slave_state_t](#) *slave, uint8_t bitsWidth)
Set the bit width for any subsequent I2S communication.
- status_t [FLEXIO_I2S_DRV_SlaveSendData](#) ([flexio_i2s_slave_state_t](#) *slave, const uint8_t *txBuff, uint32_t txSize)
Perform a non-blocking send transaction on the I2S bus.
- status_t [FLEXIO_I2S_DRV_SlaveSendDataBlocking](#) ([flexio_i2s_slave_state_t](#) *slave, const uint8_t *txBuff, uint32_t txSize, uint32_t timeout)
Perform a blocking send transaction on the I2S bus.
- status_t [FLEXIO_I2S_DRV_SlaveReceiveData](#) ([flexio_i2s_slave_state_t](#) *slave, uint8_t *rxBuff, uint32_t rxSize)
Perform a non-blocking receive transaction on the I2S bus.
- status_t [FLEXIO_I2S_DRV_SlaveReceiveDataBlocking](#) ([flexio_i2s_slave_state_t](#) *slave, uint8_t *rxBuff, uint32_t rxSize, uint32_t timeout)
Perform a blocking receive transaction on the I2S bus.
- status_t [FLEXIO_I2S_DRV_SlaveTransferAbort](#) ([flexio_i2s_slave_state_t](#) *slave)
Aborts a non-blocking I2S slave transaction.
- status_t [FLEXIO_I2S_DRV_SlaveGetStatus](#) ([flexio_i2s_slave_state_t](#) *slave, uint32_t *bytesRemaining)
Get the status of the current non-blocking I2S slave transaction.
- status_t [FLEXIO_I2S_DRV_SlaveSetRxBuffer](#) ([flexio_i2s_slave_state_t](#) *slave, uint8_t *rxBuff, uint32_t rxSize)
Provide a buffer for receiving data.
- status_t [FLEXIO_I2S_DRV_SlaveSetTxBuffer](#) ([flexio_i2s_slave_state_t](#) *slave, const uint8_t *txBuff, uint32_t txSize)
Provide a buffer for transmitting data.
- void [FLEXIO_I2S_DRV_MasterGetDefaultConfig](#) ([flexio_i2s_master_user_config_t](#) *userConfigPtr)
Returns default configuration structure for FLEXIO_I2S master.
- void [FLEXIO_I2S_DRV_SlaveGetDefaultConfig](#) ([flexio_i2s_slave_user_config_t](#) *userConfigPtr)
Returns default configuration structure for FLEXIO_I2S slave.

17.56.2 Data Structure Documentation

17.56.2.1 struct flexio_i2s_master_user_config_t

Master configuration structure.

This structure is used to provide configuration parameters for the flexio_i2s master at initialization time. Implements : flexio_i2s_master_user_config_t_Class

Definition at line 67 of file flexio_i2s_driver.h.

Data Fields

- [flexio_driver_type_t](#) driverType
- uint32_t baudRate
- uint8_t bitsWidth
- uint8_t txPin
- uint8_t rxPin
- uint8_t sckPin
- uint8_t wsPin
- i2s_callback_t callback
- void * callbackParam
- uint8_t rxDMAChannel
- uint8_t txDMAChannel

Field Documentation

17.56.2.1.1 uint32_t baudRate

Baud rate in hertz

Definition at line 70 of file flexio_i2s_driver.h.

17.56.2.1.2 uint8_t bitsWidth

Number of bits in a word - multiple of 8

Definition at line 71 of file flexio_i2s_driver.h.

17.56.2.1.3 i2s_callback_t callback

User callback function. Note that this function will be called from the interrupt service routine, so its execution time should be as small as possible. It can be NULL if it is not needed

Definition at line 76 of file flexio_i2s_driver.h.

17.56.2.1.4 void* callbackParam

Parameter for the callback function

Definition at line 80 of file flexio_i2s_driver.h.

17.56.2.1.5 flexio_driver_type_t driverType

Driver type: interrupts/polling/DMA

Definition at line 69 of file flexio_i2s_driver.h.

17.56.2.1.6 uint8_t rxDMAChannel

Rx DMA channel number. Only used in DMA mode

Definition at line 81 of file flexio_i2s_driver.h.

17.56.2.1.7 uint8_t rxPin

Flexio pin to use for receive

Definition at line 73 of file flexio_i2s_driver.h.

17.56.2.1.8 uint8_t sckPin

Flexio pin to use for serial clock

Definition at line 74 of file flexio_i2s_driver.h.

17.56.2.1.9 uint8_t txDMAChannel

Tx DMA channel number. Only used in DMA mode

Definition at line 82 of file flexio_i2s_driver.h.

17.56.2.1.10 uint8_t txPin

Flexio pin to use for transmit

Definition at line 72 of file flexio_i2s_driver.h.

17.56.2.1.11 uint8_t wsPin

Flexio pin to use for word select

Definition at line 75 of file flexio_i2s_driver.h.

17.56.2.2 struct flexio_i2s_slave_user_config_t

Slave configuration structure.

This structure is used to provide configuration parameters for the flexio_i2s slave at initialization time. Implements : flexio_i2s_slave_user_config_t_Class

Definition at line 92 of file flexio_i2s_driver.h.

Data Fields

- flexio_driver_type_t driverType
- uint8_t bitsWidth
- uint8_t txPin
- uint8_t rxPin
- uint8_t sckPin
- uint8_t wsPin
- i2s_callback_t callback
- void * callbackParam
- uint8_t rxDMAChannel
- uint8_t txDMAChannel

Field Documentation

17.56.2.2.1 uint8_t bitsWidth

Number of bits in a word - multiple of 8

Definition at line 95 of file flexio_i2s_driver.h.

17.56.2.2.2 i2s_callback_t callback

User callback function. Note that this function will be called from the interrupt service routine, so its execution time should be as small as possible. It can be NULL if it is not needed

Definition at line 100 of file flexio_i2s_driver.h.

17.56.2.2.3 void* callbackParam

Parameter for the callback function

Definition at line 104 of file flexio_i2s_driver.h.

17.56.2.2.4 flexio_driver_type_t driverType

Driver type: interrupts/polling/DMA

Definition at line 94 of file flexio_i2s_driver.h.

17.56.2.2.5 uint8_t rxDMAChannel

Rx DMA channel number. Only used in DMA mode

Definition at line 105 of file flexio_i2s_driver.h.

17.56.2.2.6 uint8_t rxPin

Flexio pin to use for receive

Definition at line 97 of file flexio_i2s_driver.h.

17.56.2.2.7 `uint8_t sckPin`

Flexio pin to use for serial clock

Definition at line 98 of file `flexio_i2s_driver.h`.

17.56.2.2.8 `uint8_t txDMAChannel`

Tx DMA channel number. Only used in DMA mode

Definition at line 106 of file `flexio_i2s_driver.h`.

17.56.2.2.9 `uint8_t txPin`

Flexio pin to use for transmit

Definition at line 96 of file `flexio_i2s_driver.h`.

17.56.2.2.10 `uint8_t wsPin`

Flexio pin to use for word select

Definition at line 99 of file `flexio_i2s_driver.h`.

17.56.2.3 `struct flexio_i2s_master_state_t`

Master internal context structure.

This structure is used by the driver for its internal logic. It must be provided by the application through the [FLEXIO_I2S_DRV_MasterInit\(\)](#) function, then it cannot be freed until the driver is de-initialized using [FLEXIO_I2S_DRV_MasterDeinit\(\)](#). The application should make no assumptions about the content of this structure.

Definition at line 118 of file `flexio_i2s_driver.h`.

17.56.3 Typedef Documentation

17.56.3.1 `typedef flexio_i2s_master_state_t flexio_i2s_slave_state_t`

Slave internal context structure.

This structure is used by the driver for its internal logic. It must be provided by the application through the [FLEXIO_I2S_DRV_SlaveInit\(\)](#) function, then it cannot be freed until the driver is de-initialized using [FLEXIO_I2S_DRV_SlaveDeinit\(\)](#). The application should make no assumptions about the content of this structure.

Definition at line 150 of file `flexio_i2s_driver.h`.

17.56.4 Function Documentation

17.56.4.1 `status_t FLEXIO_I2S_DRV_MasterDeinit (flexio_i2s_master_state_t * master)`

De-initialize the FLEXIO_I2S master mode driver.

This function de-initializes the FLEXIO_I2S driver in master mode. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2S master driver context structure.
---------------	--

Returns

Error or success status returned by API

Definition at line 1082 of file `flexio_i2s_driver.c`.

17.56.4.2 `status_t FLEXIO_I2S_DRV_MasterGetBaudRate (flexio_i2s_master_state_t * master, uint32_t * baudRate)`

Get the currently configured baud rate.

This function returns the currently configured I2S baud rate.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2S master driver context structure.
<i>baudRate</i>	the current baud rate in hertz

Returns

Error or success status returned by API

Definition at line 1161 of file flexio_i2s_driver.c.

17.56.4.3 `void FLEXIO_I2S_DRV_MasterGetDefaultConfig (flexio_i2s_master_user_config_t * userConfigPtr)`

Returns default configuration structure for FLEXIO_I2S master.

Parameters

<i>userConfigPtr</i>	Pointer to the FLEXIO_I2S user configuration structure.
----------------------	---

Definition at line 1655 of file flexio_i2s_driver.c.

17.56.4.4 `status_t FLEXIO_I2S_DRV_MasterGetStatus (flexio_i2s_master_state_t * master, uint32_t * bytesRemaining)`

Get the status of the current non-blocking I2S master transaction.

This function returns the current status of a non-blocking I2S master transaction. A return code of STATUS_BUSY means the transfer is still in progress. Otherwise the function returns a status reflecting the outcome of the last transfer. When the driver is initialized in polling mode this function also advances the transfer by checking and handling the transmit and receive events, so it must be called frequently to avoid overflows or underflows.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2S master driver context structure.
<i>bytesRemaining</i>	the remaining number of bytes to be transferred

Returns

Error or success status returned by API

Definition at line 1429 of file flexio_i2s_driver.c.

17.56.4.5 `status_t FLEXIO_I2S_DRV_MasterInit (uint32_t instance, const flexio_i2s_master_user_config_t * userConfigPtr, flexio_i2s_master_state_t * master)`

Initialize the FLEXIO_I2S master mode driver.

This function initializes the FLEXIO_I2S driver in master mode.

Parameters

<i>instance</i>	FLEXIO peripheral instance number
<i>userConfigPtr</i>	Pointer to the FLEXIO_I2S master user configuration structure. The function reads configuration data from this structure and initializes the driver accordingly. The application may free this structure after the function returns.

<i>master</i>	Pointer to the FLEXIO_I2S master driver context structure. The driver uses this memory area for its internal logic. The application must make no assumptions about the content of this structure, and must not free this memory until the driver is de-initialized using FLEXIO_I2S_DRV_MasterDeinit() .
---------------	--

Returns

Error or success status returned by API

Definition at line 991 of file flexio_i2s_driver.c.

17.56.4.6 `status_t FLEXIO_I2S_DRV_MasterReceiveData (flexio_i2s_master_state_t * master, uint8_t * rxBuff, uint32_t rxSize)`

Perform a non-blocking receive transaction on the I2S bus.

This function starts the reception of a block of data and returns immediately. The rest of the reception is handled by the interrupt service routine (if the driver is initialized in interrupt mode) or by the FLEXIO_I2S_DRV_MasterGetStatus function (if the driver is initialized in polling mode). Use [FLEXIO_I2S_DRV_MasterGetStatus\(\)](#) to check the progress of the reception.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2S master driver context structure.
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 1302 of file flexio_i2s_driver.c.

17.56.4.7 `status_t FLEXIO_I2S_DRV_MasterReceiveDataBlocking (flexio_i2s_master_state_t * master, uint8_t * rxBuff, uint32_t rxSize, uint32_t timeout)`

Perform a blocking receive transaction on the I2S bus.

This function receives a block of data and only returns when the reception is complete.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2S master driver context structure.
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 1372 of file flexio_i2s_driver.c.

17.56.4.8 `status_t FLEXIO_I2S_DRV_MasterSendData (flexio_i2s_master_state_t * master, const uint8_t * txBuff, uint32_t txSize)`

Perform a non-blocking send transaction on the I2S bus.

This function starts the transmission of a block of data and returns immediately. The rest of the transmission is handled by the interrupt service routine (if the driver is initialized in interrupt mode) or by the FLEXIO_I2S_DRV_MasterGetStatus function (if the driver is initialized in polling mode). Use [FLEXIO_I2S_DRV_MasterGetStatus\(\)](#) to check the progress of the transmission.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2S master driver context structure.
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 1201 of file flexio_i2s_driver.c.

17.56.4.9 `status_t FLEXIO_I2S_DRV_MasterSendDataBlocking (flexio_i2s_master_state_t * master, const uint8_t * txBuff, uint32_t txSize, uint32_t timeout)`

Perform a blocking send transaction on the I2S bus.

This function sends a block of data, and only returns when the transmission is complete.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2S master driver context structure.
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 1269 of file flexio_i2s_driver.c.

17.56.4.10 `status_t FLEXIO_I2S_DRV_MasterSetConfig (flexio_i2s_master_state_t * master, uint32_t baudRate, uint8_t bitsWidth)`

Set the baud rate and bit width for any subsequent I2S communication.

This function sets the baud rate (SCK frequency) and bit width for the I2S master. Note that due to module limitation not any baud rate can be achieved. The driver will set a baud rate as close as possible to the requested baud rate, but there may still be substantial differences, for example if requesting a high baud rate while using a low-frequency FlexIO clock. The application should call [FLEXIO_I2S_DRV_MasterGetBaudRate\(\)](#) after [FLEXIO_I2S_DRV_MasterSetConfig\(\)](#) to check what baud rate was actually set.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2S master driver context structure.
<i>baudRate</i>	the desired baud rate in hertz
<i>bitsWidth</i>	number of bits per word

Returns

Error or success status returned by API

Definition at line 1108 of file flexio_i2s_driver.c.

17.56.4.11 `status_t FLEXIO_I2S_DRV_MasterSetRxBuffer (flexio_i2s_master_state_t * master, uint8_t * rxBuff, uint32_t rxSize)`

Provide a buffer for receiving data.

This function can be used to provide a new buffer for receiving data to the driver. It can be called from the user callback when event STATUS_I2S_RX_OVERRUN is reported. This way the reception will continue without interruption.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2S master driver context structure.
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 1484 of file flexio_i2s_driver.c.

17.56.4.12 `status_t FLEXIO_I2S_DRV_MasterSetTxBuffer (flexio_i2s_master_state_t * master, const uint8_t * txBuff, uint32_t txSize)`

Provide a buffer for transmitting data.

This function can be used to provide a new buffer for transmitting data to the driver. It can be called from the user callback when event STATUS_I2S_TX_UNDERRUN is reported. This way the transmission will continue without interruption.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2S master driver context structure.
<i>txBuff</i>	pointer to the buffer containing transmit data
<i>txSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 1506 of file flexio_i2s_driver.c.

17.56.4.13 `status_t FLEXIO_I2S_DRV_MasterTransferAbort (flexio_i2s_master_state_t * master)`

Aborts a non-blocking I2S master transaction.

This function aborts a non-blocking I2S transfer.

Parameters

<i>master</i>	Pointer to the FLEXIO_I2S master driver context structure.
---------------	--

Returns

Error or success status returned by API

Definition at line 1405 of file flexio_i2s_driver.c.

17.56.4.14 `status_t FLEXIO_I2S_DRV_SlaveDeinit (flexio_i2s_slave_state_t * slave)`

De-initialize the FLEXIO_I2S slave mode driver.

This function de-initializes the FLEXIO_I2S driver in slave mode. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
--------------	---

Returns

Error or success status returned by API

This function de-initializes the FLEXIO_I2S driver in slave mode. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
--------------	---

Returns

Error or success status returned by API Implements : FLEXIO_I2S_DRV_SlaveDeinit_Activity

Definition at line 1708 of file flexio_i2s_driver.c.

17.56.4.15 void FLEXIO_I2S_DRV_SlaveGetDefaultConfig (flexio_i2s_slave_user_config_t * userConfigPtr)

Returns default configuration structure for FLEXIO_I2S slave.

Parameters

<i>userConfigPtr</i>	Pointer to the FLEXIO_I2S user configuration structure.
----------------------	---

Definition at line 1680 of file flexio_i2s_driver.c.

17.56.4.16 status_t FLEXIO_I2S_DRV_SlaveGetStatus (flexio_i2s_slave_state_t * slave, uint32_t * bytesRemaining)

Get the status of the current non-blocking I2S slave transaction.

This function returns the current status of a non-blocking I2S slave transaction. A return code of STATUS_BUSY means the transfer is still in progress. Otherwise the function returns a status reflecting the outcome of the last transfer. When the driver is initialized in polling mode this function also advances the transfer by checking and handling the transmit and receive events, so it must be called frequently to avoid overflows or underflows.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>bytesRemaining</i>	the remaining number of bytes to be transferred

Returns

Error or success status returned by API

This function returns the current status of a non-blocking I2S slave transaction. A return code of STATUS_BUSY means the transfer is still in progress. Otherwise the function returns a status reflecting the outcome of the last transfer. When the driver is initialized in polling mode this function also advances the transfer by checking and handling the transmit and receive events, so it must be called frequently to avoid overflows or underflows.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>bytesRemaining</i>	the remaining number of bytes to be transferred

Returns

Error or success status returned by API Implements : FLEXIO_I2S_DRV_SlaveGetStatus_Activity

Definition at line 1834 of file flexio_i2s_driver.c.

17.56.4.17 status_t FLEXIO_I2S_DRV_SlaveInit (uint32_t instance, const flexio_i2s_slave_user_config_t * userConfigPtr, flexio_i2s_slave_state_t * slave)

Initialize the FLEXIO_I2S slave mode driver.

This function initializes the FLEXIO_I2S driver in slave mode.

Parameters

<i>instance</i>	FLEXIO peripheral instance number
<i>userConfigPtr</i>	Pointer to the FLEXIO_I2S slave user configuration structure. The function reads configuration data from this structure and initializes the driver accordingly. The application may free this structure after the function returns.
<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure. The driver uses this memory area for its internal logic. The application must make no assumptions about the content of this structure, and must not free this memory until the driver is de-initialized using FLEXIO_I2S_DRV_SlaveDeinit() .

Returns

Error or success status returned by API

Definition at line 1530 of file flexio_i2s_driver.c.

17.56.4.18 `status_t FLEXIO_I2S_DRV_SlaveReceiveData (flexio_i2s_slave_state_t * slave, uint8_t * rxBuff, uint32_t rxSize)`

Perform a non-blocking receive transaction on the I2S bus.

This function starts the reception of a block of data and returns immediately. The rest of the reception is handled by the interrupt service routine (if the driver is initialized in interrupt mode) or by the [FLEXIO_I2S_DRV_SlaveGetStatus\(\)](#) function (if the driver is initialized in polling mode). Use [FLEXIO_I2S_DRV_SlaveGetStatus\(\)](#) to check the progress of the reception.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

This function starts the reception of a block of data and returns immediately. The rest of the reception is handled by the interrupt service routine (if the driver is initialized in interrupt mode) or by the [FLEXIO_I2S_DRV_SlaveGetStatus\(\)](#) function (if the driver is initialized in polling mode). Use [FLEXIO_I2S_DRV_SlaveGetStatus\(\)](#) to check the progress of the reception.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API Implements : [FLEXIO_I2S_DRV_SlaveReceiveData_Activity](#)

Definition at line 1775 of file flexio_i2s_driver.c.

17.56.4.19 `status_t FLEXIO_I2S_DRV_SlaveReceiveDataBlocking (flexio_i2s_slave_state_t * slave, uint8_t * rxBuff, uint32_t rxSize, uint32_t timeout)`

Perform a blocking receive transaction on the I2S bus.

This function receives a block of data and only returns when the reception is complete.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

This function receives a block of data and only returns when the reception is complete.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API Implements : FLEXIO_I2S_DRV_SlaveReceiveDataBlocking_Activity

Definition at line 1795 of file flexio_i2s_driver.c.

17.56.4.20 `status_t FLEXIO_I2S_DRV_SlaveSendData (flexio_i2s_slave_state_t * slave, const uint8_t * txBuff, uint32_t txSize)`

Perform a non-blocking send transaction on the I2S bus.

This function starts the transmission of a block of data and returns immediately. The rest of the transmission is handled by the interrupt service routine (if the driver is initialized in interrupt mode) or by the FLEXIO_I2S_DRV_SlaveGetStatus function (if the driver is initialized in polling mode). Use [FLEXIO_I2S_DRV_SlaveGetStatus\(\)](#) to check the progress of the transmission.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

This function starts the transmission of a block of data and returns immediately. The rest of the transmission is handled by the interrupt service routine (if the driver is initialized in interrupt mode) or by the FLEXIO_I2S_DRV_SlaveGetStatus function (if the driver is initialized in polling mode). Use [FLEXIO_I2S_DRV_SlaveGetStatus\(\)](#) to check the progress of the transmission.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API Implements : FLEXIO_I2S_DRV_SlaveSendData_Activity

Definition at line 1729 of file flexio_i2s_driver.c.

17.56.4.21 `status_t FLEXIO_I2S_DRV_SlaveSendDataBlocking (flexio_i2s_slave_state_t * slave, const uint8_t * txBuff, uint32_t txSize, uint32_t timeout)`

Perform a blocking send transaction on the I2S bus.

This function sends a block of data, and only returns when the transmission is complete.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

This function sends a block of data, and only returns when the transmission is complete.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API Implements : FLEXIO_I2S_DRV_SlaveSendDataBlocking_Activity

Definition at line 1751 of file flexio_i2s_driver.c.

17.56.4.22 `status_t FLEXIO_I2S_DRV_SlaveSetConfig (flexio_i2s_slave_state_t * slave, uint8_t bitsWidth)`

Set the bit width for any subsequent I2S communication.

This function sets the bit width for the I2S slave.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>bitsWidth</i>	number of bits per word

Returns

Error or success status returned by API

Definition at line 1612 of file flexio_i2s_driver.c.

17.56.4.23 `status_t FLEXIO_I2S_DRV_SlaveSetRxBuffer (flexio_i2s_slave_state_t * slave, uint8_t * rxBuff, uint32_t rxSize)`

Provide a buffer for receiving data.

This function can be used to provide a driver with a new buffer for receiving data. It can be called from the user callback when event STATUS_I2S_RX_OVERRUN is reported. This way the reception will continue without interruption.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

This function can be used to provide a driver with a new buffer for receiving data. It can be called from the user callback when event STATUS_I2S_RX_OVERRUN is reported. This way the reception will continue without interruption.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API Implements : FLEXIO_I2S_DRV_SlaveSetRxBuffer_Activity

Definition at line 1853 of file flexio_i2s_driver.c.

17.56.4.24 `status_t FLEXIO_I2S_DRV_SlaveSetTxBuffer (flexio_i2s_slave_state_t * slave, const uint8_t * txBuff, uint32_t txSize)`

Provide a buffer for transmitting data.

This function can be used to provide a driver with a new buffer for transmitting data. It can be called from the user callback when event STATUS_I2S_TX_UNDERRUN is reported. This way the transmission will continue without interruption.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>txBuff</i>	pointer to the buffer containing transmit data
<i>txSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

This function can be used to provide a driver with a new buffer for transmitting data. It can be called from the user callback when event STATUS_I2S_TX_UNDERRUN is reported. This way the transmission will continue without interruption.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
<i>txBuff</i>	pointer to the buffer containing transmit data
<i>txSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API Implements : FLEXIO_I2S_DRV_SlaveSetTxBuffer_Activity

Definition at line 1874 of file flexio_i2s_driver.c.

17.56.4.25 `status_t FLEXIO_I2S_DRV_SlaveTransferAbort (flexio_i2s_slave_state_t * slave)`

Aborts a non-blocking I2S slave transaction.

This function aborts a non-blocking I2S transfer.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
--------------	---

Returns

Error or success status returned by API

This function aborts a non-blocking I2S transfer.

Parameters

<i>slave</i>	Pointer to the FLEXIO_I2S slave driver context structure.
--------------	---

Returns

Error or success status returned by API Implements : FLEXIO_I2S_DRV_SlaveTransferAbort_Activity

Definition at line 1813 of file flexio_i2s_driver.c.

17.57 FlexIO SPI Driver

17.57.1 Detailed Description

SPI communication over FlexIO module (FLEXIO_SPI)

The FLEXIO_SPI Driver allows communication on an SPI bus using the FlexIO module in the S32K1xx processors.

Features

- Master or slave operation
- Interrupt, DMA or polling mode
- Provides blocking and non-blocking transfer functions
- Configurable baud rate
- Configurable clock polarity and phase
- Configurable bit order and data size

Functionality

Before using any Flexio driver the device must first be initialized using function `FLEXIO_DRV_InitDevice`. Then the FLEXIO_SPI Driver must be initialized, using functions `FLEXIO_SPI_DRV_MasterInit()` or `FLEXIO_SPI_DRV_SlaveInit()`. It is possible to use more driver instances on the same FlexIO device, as long as sufficient resources are available. Different driver instances on the same FlexIO device can function independently of each other. When it is no longer needed, the driver can be de-initialized, using `FLEXIO_SPI_DRV_MasterDeinit()` or `FLEXIO_SPI_DRV_SlaveDeinit()`. This will release the hardware resources, allowing other driver instances to be initialized other.

Master Mode

Master Mode provides functions for transmitting or receiving data to/from an SPI slave. Baud rate is provided at initialization time through the master configuration structure, but can be changed at runtime by using `FLEXIO_SPI_DRV_MasterSetBaudRate()` function. Note that due to module limitation not any baud rate can be achieved. The driver will set a baud rate as close as possible to the requested baud rate, but there may still be substantial differences, for example if requesting a high baud rate while using a low-frequency FlexIO clock. The application should call `FLEXIO_SPI_DRV_MasterGetBaudRate()` after `FLEXIO_SPI_DRV_MasterSetBaudRate()` to check what baud rate was actually set.

To send or receive data, use function `FLEXIO_SPI_DRV_MasterTransfer()`. The transmit and receive buffers, together with parameters for the transfer are provided through the `flexio_spi_transfer_t` structure. If only transmit or receive is desired, any one of the Rx/Tx buffers can be set to NULL. This driver does not support continuous send/receive using a user callback function. The callback function is only used to signal the end of a transfer.

Blocking operations will return only when the transfer is completed, either successfully or with error. Non-blocking operations will initiate the transfer and return `STATUS_SUCCESS`, but the module is still busy with the transfer and another transfer can't be initiated until the current transfer is complete. The application will be notified through the user callback when the transfer completes, or it can check the status of the current transfer by calling `FLEXIO_SPI_DRV_MasterGetStatus()`. If the transfer is still ongoing this function will return `STATUS_BUSY`. If the transfer is completed, the function will return either `STATUS_SUCCESS` or an error code, depending on the outcome of the last transfer.

The driver supports interrupt, DMA and polling mode. In polling mode the function `FLEXIO_SPI_DRV_MasterGetStatus()` ensures the progress of the transfer by checking and handling transmit and receive events reported by the FlexIO module. The application should ensure that this function is called often enough (at least once per transferred byte) to avoid Tx underflows or Rx overflows. In DMA mode the DMA channels that will be used by the driver are received through the configuration structure. The channels must be initialized by the application before the `flexio_spi` driver is initialized. The `flexio_spi` driver will only set the DMA request source.

Slave Mode

Slave Mode is very similar to master mode, the main difference being that the `FLEXIO_SPI_DRV_SlaveInit()` function initializes the FlexIO module to use the clock signal received from the master instead of generating it. Consequently, there is no `SetBaudRate` function in slave mode. Other than that, the slave mode offers a similar interface to the master mode. `FLEXIO_SPI_DRV_MasterTransfer()` can be used to initiate transfers, and `FLEXIO_SPI_DRV_SlaveGetStatus()` is used to check the status of the transfer and advance the transfer in polling mode. All other specifications from the Master Mode description apply for Slave Mode too

Important Notes

- Before using the FLEXIO_SPI Driver the protocol clock of the module must be configured. Refer to Clock Manager for clock configuration.
- Before using the FLEXIO_SPI Driver the pins must be routed to the FlexIO module. Refer to PINS Driver for pin routing configuration. Note that any of the available FlexIO pins can be used for MOSI, MISO, SCK and SS (configurable at initialization time).
- The driver enables the interrupts for the corresponding FlexIO module, but any interrupt priority setting must be done by the application.
- The driver does not support back-to-back transmission mode for CPHA = 1
- The driver does not support configurable polarity for SS signal (only active-low is supported)
- Timeout feature for blocking transfers does not work in polling mode.
- This driver needs two shifters and two timers for its operation. Initialization will fail if there are not enough shifters and timers available on the FlexIO device.
- This driver needs two DMA channels for its operation when it is initialized in DMA mode. The DMA channels must be initialized by the application before initializing the driver. Refer to EDMA driver for DMA channels initialization.
- If the application uses an RTOS, this driver uses a semaphore for blocking transfers. Initialization will fail if the semaphore cannot be created. If the driver uses polling mode no semaphore is used.
- If the application uses an RTOS, the FlexIO drivers use a mutex for channel allocation. Only one mutex per device is needed, not per driver instance. Device initialization will fail if the mutex cannot be created.
- For transfers where the data size is more than 1 byte (transferSize is 2 or 4) the driver assumes that the data buffers are defined with the proper type (uint16_t or uint32_t) and are properly aligned.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\flexio\flexio_common.c
${S32SDK_PATH}\platform\drivers\src\flexio\flexio_spi_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc
${S32SDK_PATH}\platform\drivers\src\flexio
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager OS Interface \(OSIF\)](#) [Interrupt Manager \(Interrupt\)](#) [Enhanced Direct Memory Access \(eDMA\)](#)

Data Structures

- struct [flexio_spi_master_user_config_t](#)
Master configuration structure. [More...](#)
- struct [flexio_spi_slave_user_config_t](#)
Slave configuration structure. [More...](#)
- struct [flexio_spi_master_state_t](#)
Master internal context structure. [More...](#)

Typedefs

- typedef [flexio_spi_master_state_t](#) [flexio_spi_slave_state_t](#)
Slave internal context structure.

Enumerations

- enum [flexio_spi_transfer_bit_order_t](#) { [FLEXIO_SPI_TRANSFER_MSB_FIRST](#) = 0U, [FLEXIO_SPI_TRANSFER_LSB_FIRST](#) = 1U }
Order in which the data bits are transferred Implements : [flexio_spi_transfer_bit_order_t](#) Class.
- enum [flexio_spi_transfer_size_t](#) { [FLEXIO_SPI_TRANSFER_1BYTE](#) = 1U, [FLEXIO_SPI_TRANSFER_2BYTE](#) = 2U, [FLEXIO_SPI_TRANSFER_4BYTE](#) = 4U }
Size of transferred data in bytes Implements : [flexio_spi_transfer_size_t](#) Class.

FLEXIO_SPI Driver

- status_t [FLEXIO_SPI_DRV_MasterInit](#) (uint32_t instance, const [flexio_spi_master_user_config_t](#) *userConfigPtr, [flexio_spi_master_state_t](#) *master)
Initialize the FLEXIO_SPI master mode driver.
- status_t [FLEXIO_SPI_DRV_MasterDeinit](#) ([flexio_spi_master_state_t](#) *master)
De-initialize the FLEXIO_SPI master mode driver.
- status_t [FLEXIO_SPI_DRV_MasterSetBaudRate](#) ([flexio_spi_master_state_t](#) *master, uint32_t baudRate)
Set the baud rate for any subsequent SPI communication.
- status_t [FLEXIO_SPI_DRV_MasterGetBaudRate](#) ([flexio_spi_master_state_t](#) *master, uint32_t *baudRate)
Get the currently configured baud rate.
- status_t [FLEXIO_SPI_DRV_MasterTransfer](#) ([flexio_spi_master_state_t](#) *master, const uint8_t *txData, uint8_t *rxData, uint32_t dataSize)
Perform a non-blocking SPI master transaction.
- status_t [FLEXIO_SPI_DRV_MasterTransferBlocking](#) ([flexio_spi_master_state_t](#) *master, const uint8_t *txData, uint8_t *rxData, uint32_t dataSize, uint32_t timeout)
Perform a blocking SPI master transaction.
- status_t [FLEXIO_SPI_DRV_MasterTransferAbort](#) ([flexio_spi_master_state_t](#) *master)
Aborts a non-blocking SPI master transaction.
- status_t [FLEXIO_SPI_DRV_MasterGetStatus](#) ([flexio_spi_master_state_t](#) *master, uint32_t *bytesRemaining)
Get the status of the current non-blocking SPI master transaction.
- status_t [FLEXIO_SPI_DRV_SlaveInit](#) (uint32_t instance, const [flexio_spi_slave_user_config_t](#) *userConfigPtr, [flexio_spi_slave_state_t](#) *slave)

Initialize the FLEXIO_SPI slave mode driver.

- status_t [FLEXIO_SPI_DRV_SlaveDeinit](#) ([flexio_spi_slave_state_t](#) *slave)

De-initialize the FLEXIO_SPI slave mode driver.

- status_t [FLEXIO_SPI_DRV_SlaveTransfer](#) ([flexio_spi_slave_state_t](#) *slave, const uint8_t *txData, uint8_t *rxData, uint32_t dataSize)

Perform a non-blocking SPI slave transaction.

- status_t [FLEXIO_SPI_DRV_SlaveTransferBlocking](#) ([flexio_spi_slave_state_t](#) *slave, const uint8_t *txData, uint8_t *rxData, uint32_t dataSize, uint32_t timeout)

Perform a blocking SPI slave transaction.

- status_t [FLEXIO_SPI_DRV_SlaveTransferAbort](#) ([flexio_spi_slave_state_t](#) *slave)

Aborts a non-blocking SPI slave transaction.

- status_t [FLEXIO_SPI_DRV_SlaveGetStatus](#) ([flexio_spi_slave_state_t](#) *slave, uint32_t *bytesRemaining)

Get the status of the current non-blocking SPI slave transaction.

- void [FLEXIO_SPI_DRV_MasterGetDefaultConfig](#) ([flexio_spi_master_user_config_t](#) *userConfigPtr)

Returns default configuration structure for FLEXIO_SPI master.

- void [FLEXIO_SPI_DRV_SlaveGetDefaultConfig](#) ([flexio_spi_slave_user_config_t](#) *userConfigPtr)

Returns default configuration structure for FLEXIO_SPI slave.

17.57.2 Data Structure Documentation

17.57.2.1 struct flexio_spi_master_user_config_t

Master configuration structure.

This structure is used to provide configuration parameters for the flexio_spi master at initialization time. Implements : flexio_spi_master_user_config_t_Class

Definition at line 67 of file flexio_spi_driver.h.

Data Fields

- uint32_t [baudRate](#)
- [flexio_driver_type_t](#) driverType
- [flexio_spi_transfer_bit_order_t](#) bitOrder
- [flexio_spi_transfer_size_t](#) transferSize
- uint8_t [clockPolarity](#)
- uint8_t [clockPhase](#)
- uint8_t [mosiPin](#)
- uint8_t [misoPin](#)
- uint8_t [sckPin](#)
- uint8_t [ssPin](#)
- spi_callback_t [callback](#)
- void * [callbackParam](#)
- uint8_t [rxDMACHannel](#)
- uint8_t [txDMACHannel](#)

Field Documentation

17.57.2.1.1 uint32_t baudRate

Baud rate in hertz

Definition at line 69 of file flexio_spi_driver.h.

17.57.2.1.2 flexio_spi_transfer_bit_order_t bitOrder

Bit order: LSB-first / MSB-first

Definition at line 71 of file flexio_spi_driver.h.

17.57.2.1.3 `spi_callback_t` callback

User callback function. Note that this function will be called from the interrupt service routine, so its execution time should be as small as possible. It can be NULL if it is not needed

Definition at line 79 of file `flexio_spi_driver.h`.

17.57.2.1.4 `void*` callbackParam

Parameter for the callback function

Definition at line 83 of file `flexio_spi_driver.h`.

17.57.2.1.5 `uint8_t` clockPhase

Clock Phase (CPHA) 0 = sample on leading clock edge; 1 = sample on trailing clock edge

Definition at line 74 of file `flexio_spi_driver.h`.

17.57.2.1.6 `uint8_t` clockPolarity

Clock Polarity (CPOL) 0 = active-high clock; 1 = active-low clock

Definition at line 73 of file `flexio_spi_driver.h`.

17.57.2.1.7 `flexio_driver_type_t` driverType

Driver type: interrupts/polling/DMA

Definition at line 70 of file `flexio_spi_driver.h`.

17.57.2.1.8 `uint8_t` misoPin

Flexio pin to use as MISO pin

Definition at line 76 of file `flexio_spi_driver.h`.

17.57.2.1.9 `uint8_t` mosiPin

Flexio pin to use as MOSI pin

Definition at line 75 of file `flexio_spi_driver.h`.

17.57.2.1.10 `uint8_t` rxDMAChannel

Rx DMA channel number. Only used in DMA mode

Definition at line 84 of file `flexio_spi_driver.h`.

17.57.2.1.11 `uint8_t` sckPin

Flexio pin to use as SCK pin

Definition at line 77 of file `flexio_spi_driver.h`.

17.57.2.1.12 `uint8_t` ssPin

Flexio pin to use as SS pin

Definition at line 78 of file `flexio_spi_driver.h`.

17.57.2.1.13 `flexio_spi_transfer_size_t` transferSize

Transfer size in bytes: 1/2/4

Definition at line 72 of file `flexio_spi_driver.h`.

17.57.2.1.14 uint8_t txDMAChannel

Tx DMA channel number. Only used in DMA mode

Definition at line 85 of file flexio_spi_driver.h.

17.57.2.2 struct flexio_spi_slave_user_config_t

Slave configuration structure.

This structure is used to provide configuration parameters for the flexio_spi slave at initialization time. Implements : flexio_spi_slave_user_config_t_Class

Definition at line 94 of file flexio_spi_driver.h.

Data Fields

- [flexio_driver_type_t driverType](#)
- [flexio_spi_transfer_bit_order_t bitOrder](#)
- [flexio_spi_transfer_size_t transferSize](#)
- [uint8_t clockPolarity](#)
- [uint8_t clockPhase](#)
- [uint8_t mosiPin](#)
- [uint8_t misoPin](#)
- [uint8_t sckPin](#)
- [uint8_t ssPin](#)
- [spi_callback_t callback](#)
- [void * callbackParam](#)
- [uint8_t rxDMAChannel](#)
- [uint8_t txDMAChannel](#)

Field Documentation**17.57.2.2.1 flexio_spi_transfer_bit_order_t bitOrder**

Bit order: LSB-first / MSB-first

Definition at line 97 of file flexio_spi_driver.h.

17.57.2.2.2 spi_callback_t callback

User callback function. Note that this function will be called from the interrupt service routine, so its execution time should be as small as possible. It can be NULL if it is not needed

Definition at line 105 of file flexio_spi_driver.h.

17.57.2.2.3 void* callbackParam

Parameter for the callback function

Definition at line 109 of file flexio_spi_driver.h.

17.57.2.2.4 uint8_t clockPhase

Clock Phase (CPHA) 0 = sample on leading clock edge; 1 = sample on trailing clock edge

Definition at line 100 of file flexio_spi_driver.h.

17.57.2.2.5 uint8_t clockPolarity

Clock Polarity (CPOL) 0 = active-low clock; 1 = active-high clock

Definition at line 99 of file flexio_spi_driver.h.

17.57.2.2.6 `flexio_driver_type_t` `driverType`

Driver type: interrupts/polling/DMA

Definition at line 96 of file `flexio_spi_driver.h`.

17.57.2.2.7 `uint8_t` `misoPin`

Flexio pin to use as MISO pin

Definition at line 102 of file `flexio_spi_driver.h`.

17.57.2.2.8 `uint8_t` `mosiPin`

Flexio pin to use as MOSI pin

Definition at line 101 of file `flexio_spi_driver.h`.

17.57.2.2.9 `uint8_t` `rxDMAChannel`

Rx DMA channel number. Only used in DMA mode

Definition at line 110 of file `flexio_spi_driver.h`.

17.57.2.2.10 `uint8_t` `sckPin`

Flexio pin to use as SCK pin

Definition at line 103 of file `flexio_spi_driver.h`.

17.57.2.2.11 `uint8_t` `ssPin`

Flexio pin to use as SS pin

Definition at line 104 of file `flexio_spi_driver.h`.

17.57.2.2.12 `flexio_spi_transfer_size_t` `transferSize`

Transfer size in bytes: 1/2/4

Definition at line 98 of file `flexio_spi_driver.h`.

17.57.2.2.13 `uint8_t` `txDMAChannel`

Tx DMA channel number. Only used in DMA mode

Definition at line 111 of file `flexio_spi_driver.h`.

17.57.2.3 `struct flexio_spi_master_state_t`

Master internal context structure.

This structure is used by the master-mode driver for its internal logic. It must be provided by the application through the `FLEXIO_SPI_DRV_MasterInit()` function, then it cannot be freed until the driver is de-initialized using `FLEXIO_SPI_DRV_MasterDeinit()`. The application should make no assumptions about the content of this structure.

Definition at line 123 of file `flexio_spi_driver.h`.

17.57.3 Typedef Documentation

17.57.3.1 `typedef flexio_spi_master_state_t flexio_spi_slave_state_t`

Slave internal context structure.

This structure is used by the slave-mode driver for its internal logic. It must be provided by the application through the `FLEXIO_SPI_DRV_SlaveInit()` function, then it cannot be freed until the driver is de-initialized using `FLEXIO_SPI_DRV_SlaveDeinit()`.

[_SPI_DRV_SlaveDeinit\(\)](#). The application should make no assumptions about the content of this structure.

Definition at line 155 of file flexio_spi_driver.h.

17.57.4 Enumeration Type Documentation

17.57.4.1 enum flexio_spi_transfer_bit_order_t

Order in which the data bits are transferred Implements : flexio_spi_transfer_bit_order_t_Class.

Enumerator

FLEXIO_SPI_TRANSFER_MSB_FIRST Transmit data starting with most significant bit

FLEXIO_SPI_TRANSFER_LSB_FIRST Transmit data starting with least significant bit

Definition at line 39 of file flexio_spi_driver.h.

17.57.4.2 enum flexio_spi_transfer_size_t

Size of transferred data in bytes Implements : flexio_spi_transfer_size_t_Class.

Enumerator

FLEXIO_SPI_TRANSFER_1BYTE Data size is 1-byte

FLEXIO_SPI_TRANSFER_2BYTE Data size is 2-bytes

FLEXIO_SPI_TRANSFER_4BYTE Data size is 4-bytes

Definition at line 48 of file flexio_spi_driver.h.

17.57.5 Function Documentation

17.57.5.1 status_t FLEXIO_SPI_DRV_MasterDeinit (flexio_spi_master_state_t * master)

De-initialize the FLEXIO_SPI master mode driver.

This function de-initializes the FLEXIO_SPI driver in master mode. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

<i>master</i>	Pointer to the FLEXIO_SPI master driver context structure.
---------------	--

Returns

Error or success status returned by API

Definition at line 982 of file flexio_spi_driver.c.

17.57.5.2 status_t FLEXIO_SPI_DRV_MasterGetBaudRate (flexio_spi_master_state_t * master, uint32_t * baudRate)

Get the currently configured baud rate.

This function returns the currently configured SPI baud rate.

Parameters

<i>master</i>	Pointer to the FLEXIO_SPI master driver context structure.
<i>baudRate</i>	the current baud rate in hertz

Returns

Error or success status returned by API

Definition at line 1054 of file flexio_spi_driver.c.

17.57.5.3 void FLEXIO_SPI_DRV_MasterGetDefaultConfig (flexio_spi_master_user_config_t * userConfigPtr)

Returns default configuration structure for FLEXIO_SPI master.

Parameters

<i>userConfigPtr</i>	Pointer to the FLEXIO_SPI user configuration structure.
----------------------	---

Definition at line 1352 of file flexio_spi_driver.c.

17.57.5.4 status_t FLEXIO_SPI_DRV_MasterGetStatus (flexio_spi_master_state_t * master, uint32_t * bytesRemaining)

Get the status of the current non-blocking SPI master transaction.

This function returns the current status of a non-blocking SPI master transaction. A return code of STATUS_BUSY means the transfer is still in progress. Otherwise the function returns a status reflecting the outcome of the last transfer. When the driver is initialized in polling mode this function also advances the transfer by checking and handling the transmit and receive events, so it must be called frequently to avoid overflows or underflows.

Parameters

<i>master</i>	Pointer to the FLEXIO_SPI master driver context structure.
<i>bytesRemaining</i>	the remaining number of bytes to be transferred

Returns

Error or success status returned by API

Definition at line 1225 of file flexio_spi_driver.c.

17.57.5.5 status_t FLEXIO_SPI_DRV_MasterInit (uint32_t instance, const flexio_spi_master_user_config_t * userConfigPtr, flexio_spi_master_state_t * master)

Initialize the FLEXIO_SPI master mode driver.

This function initializes the FLEXIO_SPI driver in master mode.

Parameters

<i>instance</i>	FLEXIO peripheral instance number
<i>userConfigPtr</i>	Pointer to the FLEXIO_SPI master user configuration structure. The function reads configuration data from this structure and initializes the driver accordingly. The application may free this structure after the function returns.
<i>master</i>	Pointer to the FLEXIO_SPI master driver context structure. The driver uses this memory area for its internal logic. The application must make no assumptions about the content of this structure, and must not free this memory until the driver is de-initialized using FLEXIO_SPI_DRV_MasterDeinit() .

Returns

Error or success status returned by API

Definition at line 893 of file flexio_spi_driver.c.

17.57.5.6 `status_t FLEXIO_SPI_DRV_MasterSetBaudRate (flexio_spi_master_state_t * master, uint32_t baudRate)`

Set the baud rate for any subsequent SPI communication.

This function sets the baud rate for the SPI master. Note that due to module limitation not any baud rate can be achieved. The driver will set a baud rate as close as possible to the requested baud rate, but there may still be substantial differences, for example if requesting a high baud rate while using a low-frequency FlexIO clock. The application should call [FLEXIO_SPI_DRV_MasterGetBaudRate\(\)](#) after [FLEXIO_SPI_DRV_MasterSetBaudRate\(\)](#) to check what baud rate was actually set.

Parameters

<i>master</i>	Pointer to the FLEXIO_SPI master driver context structure.
<i>baudRate</i>	the desired baud rate in hertz

Returns

Error or success status returned by API

Definition at line 1009 of file flexio_spi_driver.c.

17.57.5.7 `status_t FLEXIO_SPI_DRV_MasterTransfer (flexio_spi_master_state_t * master, const uint8_t * txData, uint8_t * rxData, uint32_t dataSize)`

Perform a non-blocking SPI master transaction.

This function performs an SPI full-duplex transaction, transmit and receive in parallel. If only transmit or receive are required, it is possible to provide NULL pointers for txData or rxData. The transfer is non-blocking, the function only initiates the transfer and then returns, leaving the transfer to complete asynchronously). [FLEXIO_SPI_DRV_MasterGetStatus\(\)](#) can be called to check the status of the transfer.

Parameters

<i>master</i>	Pointer to the FLEXIO_SPI master driver context structure.
<i>txData</i>	pointer to the data to be transmitted
<i>rxData</i>	pointer to the buffer where to store received data
<i>dataSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 1095 of file flexio_spi_driver.c.

17.57.5.8 `status_t FLEXIO_SPI_DRV_MasterTransferAbort (flexio_spi_master_state_t * master)`

Aborts a non-blocking SPI master transaction.

This function aborts a non-blocking SPI transfer.

Parameters

<i>master</i>	Pointer to the FLEXIO_SPI master driver context structure.
---------------	--

Returns

Error or success status returned by API

Definition at line 1201 of file flexio_spi_driver.c.

17.57.5.9 `status_t FLEXIO_SPI_DRV_MasterTransferBlocking (flexio_spi_master_state_t * master, const uint8_t * txData, uint8_t * rxData, uint32_t dataSize, uint32_t timeout)`

Perform a blocking SPI master transaction.

This function performs an SPI full-duplex transaction, transmit and receive in parallel. If only transmit or receive are required, it is possible to provide NULL pointers for txData or rxData. The transfer is blocking, the function only returns when the transfer is complete.

Parameters

<i>master</i>	Pointer to the FLEXIO_SPI master driver context structure.
<i>txData</i>	pointer to the data to be transmitted
<i>rxData</i>	pointer to the buffer where to store received data
<i>dataSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 1160 of file flexio_spi_driver.c.

17.57.5.10 `status_t FLEXIO_SPI_DRV_SlaveDeinit (flexio_spi_slave_state_t * slave)`

De-initialize the FLEXIO_SPI slave mode driver.

This function de-initializes the FLEXIO_SPI driver in slave mode. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

<i>slave</i>	Pointer to the FLEXIO_SPI slave driver context structure.
--------------	---

Returns

Error or success status returned by API

This function de-initializes the FLEXIO_SPI driver in slave mode. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

<i>slave</i>	Pointer to the FLEXIO_SPI slave driver context structure.
--------------	---

Returns

Error or success status returned by API Implements : FLEXIO_SPI_DRV_SlaveDeinit_Activity

Definition at line 1411 of file flexio_spi_driver.c.

17.57.5.11 `void FLEXIO_SPI_DRV_SlaveGetDefaultConfig (flexio_spi_slave_user_config_t * userConfigPtr)`

Returns default configuration structure for FLEXIO_SPI slave.

Parameters

<i>userConfigPtr</i>	Pointer to the FLEXIO_SPI user configuration structure.
----------------------	---

Definition at line 1380 of file flexio_spi_driver.c.

17.57.5.12 `status_t FLEXIO_SPI_DRV_SlaveGetStatus (flexio_spi_slave_state_t * slave, uint32_t * bytesRemaining)`

Get the status of the current non-blocking SPI slave transaction.

This function returns the current status of a non-blocking SPI slave transaction. A return code of STATUS_BUSY means the transfer is still in progress. Otherwise the function returns a status reflecting the outcome of the last transfer. When the driver is initialized in polling mode this function also advances the transfer by checking and handling the transmit and receive events, so it must be called frequently to avoid overflows or underflows.

Parameters

<i>slave</i>	Pointer to the FLEXIO_SPI slave driver context structure.
<i>bytesRemaining</i>	the remaining number of bytes to be transferred

Returns

Error or success status returned by API

This function returns the current status of a non-blocking SPI slave transaction. A return code of STATUS_BUSY means the transfer is still in progress. Otherwise the function returns a status reflecting the outcome of the last transfer. When the driver is initialized in polling mode this function also advances the transfer by checking and handling the transmit and receive events, so it must be called frequently to avoid overflows or underflows.

Parameters

<i>slave</i>	Pointer to the FLEXIO_SPI slave driver context structure.
<i>bytesRemaining</i>	the remaining number of bytes to be transferred

Returns

Error or success status returned by API Implements : FLEXIO_SPI_DRV_SlaveGetStatus_Activity

Definition at line 1498 of file flexio_spi_driver.c.

17.57.5.13 `status_t FLEXIO_SPI_DRV_SlaveInit (uint32_t instance, const flexio_spi_slave_user_config_t * userConfigPtr, flexio_spi_slave_state_t * slave)`

Initialize the FLEXIO_SPI slave mode driver.

This function initializes the FLEXIO_SPI driver in slave mode.

Parameters

<i>instance</i>	FLEXIO peripheral instance number
<i>userConfigPtr</i>	Pointer to the FLEXIO_SPI slave user configuration structure. The function reads configuration data from this structure and initializes the driver accordingly. The application may free this structure after the function returns.
<i>slave</i>	Pointer to the FLEXIO_SPI slave driver context structure. The driver uses this memory area for its internal logic. The application must make no assumptions about the content of this structure, and must not free this memory until the driver is de-initialized using FLEXIO_SPI_DRV_SlaveDeinit() .

Returns

Error or success status returned by API

Definition at line 1273 of file flexio_spi_driver.c.

17.57.5.14 `status_t FLEXIO_SPI_DRV_SlaveTransfer (flexio_spi_slave_state_t * slave, const uint8_t * txData, uint8_t * rxData, uint32_t dataSize)`

Perform a non-blocking SPI slave transaction.

This function performs an SPI full-duplex transaction, transmit and receive in parallel. If only transmit or receive are required, it is possible to provide NULL pointers for txData or rxData. The transfer is non-blocking, the function only initiates the transfer and then returns, leaving the transfer to complete asynchronously). [FLEXIO_SPI_DRV_SlaveGetStatus\(\)](#) can be called to check the status of the transfer.

Parameters

<i>slave</i>	Pointer to the FLEXIO_SPI slave driver context structure.
<i>txData</i>	pointer to the data to be transmitted
<i>rxData</i>	pointer to the buffer where to store received data
<i>dataSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

This function performs an SPI full-duplex transaction, transmit and receive in parallel. If only transmit or receive are required, it is possible to provide NULL pointers for txData or rxData. The transfer is non-blocking, the function only initiates the transfer and then returns, leaving the transfer to complete asynchronously). [FLEXIO_SPI_DRV_SlaveGetStatus\(\)](#) can be called to check the status of the transfer.

Parameters

<i>slave</i>	Pointer to the FLEXIO_SPI slave driver context structure.
<i>txData</i>	pointer to the data to be transmitted
<i>rxData</i>	pointer to the buffer where to store received data
<i>dataSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API Implements : FLEXIO_SPI_DRV_SlaveTransfer_Activity

Definition at line 1433 of file flexio_spi_driver.c.

17.57.5.15 `status_t FLEXIO_SPI_DRV_SlaveTransferAbort (flexio_spi_slave_state_t * slave)`

Aborts a non-blocking SPI slave transaction.

This function aborts a non-blocking SPI transfer.

Parameters

<i>slave</i>	Pointer to the FLEXIO_SPI slave driver context structure.
--------------	---

Returns

Error or success status returned by API

This function aborts a non-blocking SPI transfer.

Parameters

<i>slave</i>	Pointer to the FLEXIO_SPI slave driver context structure.
--------------	---

Returns

Error or success status returned by API Implements : FLEXIO_SPI_DRV_SlaveTransferAbort_Activity

Definition at line 1477 of file flexio_spi_driver.c.

17.57.5.16 `status_t FLEXIO_SPI_DRV_SlaveTransferBlocking (flexio_spi_slave_state_t * slave, const uint8_t * txData, uint8_t * rxData, uint32_t dataSize, uint32_t timeout)`

Perform a blocking SPI slave transaction.

This function performs an SPI full-duplex transaction, transmit and receive in parallel. If only transmit or receive are required, it is possible to provide NULL pointers for txData or rxData. The transfer is blocking, the function only returns when the transfer is complete.

Parameters

<i>slave</i>	Pointer to the FLEXIO_SPI slave driver context structure.
<i>txData</i>	pointer to the data to be transmitted
<i>rxData</i>	pointer to the buffer where to store received data
<i>dataSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

This function performs an SPI full-duplex transaction, transmit and receive in parallel. If only transmit or receive are required, it is possible to provide NULL pointers for txData or rxData. The transfer is blocking, the function only returns when the transfer is complete.

Parameters

<i>slave</i>	Pointer to the FLEXIO_SPI slave driver context structure.
<i>txData</i>	pointer to the data to be transmitted
<i>rxData</i>	pointer to the buffer where to store received data
<i>dataSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API Implements : FLEXIO_SPI_DRV_SlaveTransferBlocking_Activity

Definition at line 1458 of file flexio_spi_driver.c.

17.58 FlexIO UART Driver

17.58.1 Detailed Description

UART communication over FlexIO module (FLEXIO_UART)

The FLEXIO_UART Driver allows UART communication using the FlexIO module in the S32K1xx processors.

Features

- Interrupt, DMA or polling mode
- Provides blocking and non-blocking transmit and receive functions
- Configurable baud rate and number of bits
- Single stop bit only
- Parity bit not supported

Functionality

Initialization

Before using any Flexio driver the device must first be initialized using function `FLEXIO_DRV_InitDevice`. Then the FLEXIO_UART Driver must be initialized, using function `FLEXIO_UART_DRV_Init()`. It is possible to use more driver instances on the same FlexIO device, as long as sufficient resources are available. Different driver instances on the same FlexIO device can function independently of each other. When it is no longer needed, the driver can be de-initialized, using `FLEXIO_UART_DRV_Deinit()`. This will release the hardware resources, allowing other driver instances to be initialized.

Choosing transmit/receive mode

To initialize the UART driver in transmit / receive mode the `direction` field of the configuration structure must be set to `FLEXIO_UART_DIRECTION_TX` / `FLEXIO_UART_DIRECTION_RX` when calling `FLEXIO_UART_DRV_Init()`. Once configured for one direction the driver must be used only for the chosen direction until it is de-initialized. One driver instance can only work in one direction at a time, but more driver instances can be created on the same device, up to the number of shifters present on the device (for example on S32K144 up to 4 driver instances can run in parallel on one device).

Setting the baud rate and bit count

The baud rate and bit count are provided at initialization time through the master configuration structure, but they can be changed at runtime by using function `FLEXIO_UART_DRV_SetConfig()`. Note that due to module limitation not any baud rate can be achieved. The driver will set a baud rate as close as possible to the requested baud rate, but there may still be substantial differences, for example if requesting a high baud rate while using a low-frequency FlexIO clock. The application should call `FLEXIO_UART_DRV_GetBaudRate()` to check what baud rate was actually set.

Transmitting / Receiving

To send or receive data to/from the currently configured slave address, use functions `FLEXIO_UART_DRV_SendData()` or `FLEXIO_UART_DRV_ReceiveData()` (or their blocking counterparts). Continuous send/receive can be realized by registering a user callback function. When the driver completes the transmission or reception of the current buffer, it will invoke the user callback with an appropriate event. The callback function can use `FLEXIO_UART_DRV_SetTxBuffer()` or `FLEXIO_UART_DRV_SetRxBuffer()` to provide a new buffer.

Blocking operations will return only when the transfer is completed, either successfully or with error. Non-blocking operations will initiate the transfer and return `STATUS_SUCCESS`, but the module is still busy with the transfer and another transfer can't be initiated until the current transfer is complete. The application will be notified through the user callback when the transfer completes, or it can check the status of the current transfer by calling `FLEXIO_UART_DRV_GetStatus()`. If the transfer is still ongoing this function will return `STATUS_BUSY`. If the transfer is

completed, the function will return either STATUS_SUCCESS or an error code, depending on the outcome of the last transfer.

The driver supports interrupt, DMA and polling mode. In polling mode the function [FLEXIO_UART_DRV_GetStatus\(\)](#) ensures the progress of the transfer by checking and handling transmit and receive events reported by the FlexIO module. The application should ensure that this function is called often enough (at least once per transferred byte) to avoid Tx underflows or Rx overflows. In DMA mode the DMA channel that will be used by the driver is received through the configuration structure. The channel must be initialized by the application before the flexio_ uart driver is initialized. The flexio_uart driver will only set the DMA request source.

Important Notes

- Before using the FLEXIO_UART Driver the FlexIO clock must be configured. Refer to Clock Manager for clock configuration.
- Before using the FLEXIO_UART Driver the pins must be routed to the FlexIO module. Refer to PINS Driver for pin routing configuration. Note that any of the available FlexIO pins can be used for the UART TX / RX line (configurable at initialization time). If more than one driver instance is used on the same Flexio module, it is the responsibility of the application to ensure there are no conflicts between pins.
- The driver enables the interrupts for the corresponding FlexIO module, but any interrupt priority setting must be done by the application.
- Timeout feature for blocking transfers does not work in polling mode.
- This driver needs one shifter and one timer for its operation. Initialization will fail if there are not enough shifters and timers available on the FlexIO device.
- This driver needs one DMA channel for its operation when it is initialized in DMA mode. The DMA channels must be initialized by the application before initializing the driver. Refer to EDMA driver for DMA channels initialization.
- If the application uses an RTOS, this driver uses a semaphore for blocking transfers. Initialization will fail if the semaphore cannot be created. If the driver uses polling mode no semaphore is used.
- If the application uses an RTOS, the FlexIO drivers use a mutex for channel allocation. Only one mutex per device is needed, not per driver instance. Device initialization will fail if the mutex cannot be created.
- For transfers where the data size is 2 bytes (bitCount is greater than 8) the driver assumes that the data buffers are defined with the proper type (uint16_t) and are properly aligned.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\drivers\src\flexio\flexio_common.c
{S32SDK_PATH}\platform\drivers\src\flexio\flexio_uart_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\drivers\inc
{S32SDK_PATH}\platform\drivers\src\flexio
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager OS Interface \(OSIF\)](#) [Interrupt Manager \(Interrupt\)](#) [Enhanced Direct Memory Access \(eDMA\)](#)

Data Structures

- struct [flexio_uart_user_config_t](#)
Driver configuration structure. [More...](#)
- struct [flexio_uart_state_t](#)
Driver internal context structure. [More...](#)

Enumerations

- enum [flexio_uart_driver_direction_t](#) { [FLEXIO_UART_DIRECTION_TX](#) = 0x01U, [FLEXIO_UART_DIRECTION_RX](#) = 0x00U }
flexio_uart driver direction (tx or rx)

FLEXIO_UART Driver

- status_t [FLEXIO_UART_DRV_Init](#) (uint32_t instance, const [flexio_uart_user_config_t](#) *userConfigPtr, [flexio_uart_state_t](#) *state)
Initialize the FLEXIO_UART driver.
- status_t [FLEXIO_UART_DRV_Deinit](#) ([flexio_uart_state_t](#) *state)
De-initialize the FLEXIO_UART driver.
- status_t [FLEXIO_UART_DRV_SetConfig](#) ([flexio_uart_state_t](#) *state, uint32_t baudRate, uint8_t bitCount)
Set the baud rate and bit width for any subsequent UART communication.
- status_t [FLEXIO_UART_DRV_GetBaudRate](#) ([flexio_uart_state_t](#) *state, uint32_t *baudRate)
Get the currently configured baud rate.
- status_t [FLEXIO_UART_DRV_SendDataBlocking](#) ([flexio_uart_state_t](#) *state, const uint8_t *txBuff, uint32_t txSize, uint32_t timeout)
Perform a blocking UART transmission.
- status_t [FLEXIO_UART_DRV_SendData](#) ([flexio_uart_state_t](#) *state, const uint8_t *txBuff, uint32_t txSize)
Perform a non-blocking UART transmission.
- status_t [FLEXIO_UART_DRV_ReceiveDataBlocking](#) ([flexio_uart_state_t](#) *state, uint8_t *rxBuff, uint32_t rxSize, uint32_t timeout)
Perform a blocking UART reception.
- status_t [FLEXIO_UART_DRV_ReceiveData](#) ([flexio_uart_state_t](#) *state, uint8_t *rxBuff, uint32_t rxSize)
Perform a non-blocking UART reception.
- status_t [FLEXIO_UART_DRV_GetStatus](#) ([flexio_uart_state_t](#) *state, uint32_t *bytesRemaining)
Get the status of the current non-blocking UART transfer.
- status_t [FLEXIO_UART_DRV_TransferAbort](#) ([flexio_uart_state_t](#) *state)
Aborts a non-blocking UART transfer.
- status_t [FLEXIO_UART_DRV_SetRxBuffer](#) ([flexio_uart_state_t](#) *state, uint8_t *rxBuff, uint32_t rxSize)
Provide a buffer for receiving data.
- status_t [FLEXIO_UART_DRV_SetTxBuffer](#) ([flexio_uart_state_t](#) *state, const uint8_t *txBuff, uint32_t txSize)
Provide a buffer for transmitting data.
- void [FLEXIO_UART_DRV_GetDefaultConfig](#) ([flexio_uart_user_config_t](#) *userConfigPtr)
Returns default configuration structure for FLEXIO_UART.

17.58.2 Data Structure Documentation

17.58.2.1 struct flexio_uart_user_config_t

Driver configuration structure.

This structure is used to provide configuration parameters for the flexio_uart driver at initialization time. Implements : [flexio_uart_user_config_t_Class](#)

Definition at line 60 of file flexio_uart_driver.h.

Data Fields

- [flexio_driver_type_t driverType](#)
- [uint32_t baudRate](#)
- [uint8_t bitCount](#)
- [flexio_uart_driver_direction_t direction](#)
- [uint8_t dataPin](#)
- [uart_callback_t callback](#)
- [void * callbackParam](#)
- [uint8_t dmaChannel](#)

Field Documentation

17.58.2.1.1 [uint32_t baudRate](#)

Baud rate in hertz

Definition at line 63 of file [flexio_uart_driver.h](#).

17.58.2.1.2 [uint8_t bitCount](#)

Number of bits per word

Definition at line 64 of file [flexio_uart_driver.h](#).

17.58.2.1.3 [uart_callback_t callback](#)

User callback function. Note that this function will be called from the interrupt service routine, so its execution time should be as small as possible. It can be NULL if it is not needed

Definition at line 67 of file [flexio_uart_driver.h](#).

17.58.2.1.4 [void* callbackParam](#)

Parameter for the callback function

Definition at line 71 of file [flexio_uart_driver.h](#).

17.58.2.1.5 [uint8_t dataPin](#)

Flexio pin to use as Tx or Rx pin

Definition at line 66 of file [flexio_uart_driver.h](#).

17.58.2.1.6 [flexio_uart_driver_direction_t direction](#)

Driver direction: Tx or Rx

Definition at line 65 of file [flexio_uart_driver.h](#).

17.58.2.1.7 [uint8_t dmaChannel](#)

DMA channel number. Only used in DMA mode

Definition at line 72 of file [flexio_uart_driver.h](#).

17.58.2.1.8 [flexio_driver_type_t driverType](#)

Driver type: interrupts/polling/DMA

Definition at line 62 of file [flexio_uart_driver.h](#).

17.58.2.2 [struct flexio_uart_state_t](#)

Driver internal context structure.

This structure is used by the flexio_uart driver for its internal logic. It must be provided by the application through the `FLEXIO_UART_DRV_Init()` function, then it cannot be freed until the driver is de-initialized using `FLEXIO_UART_DRV_Deinit()`. The application should make no assumptions about the content of this structure.

Definition at line 84 of file flexio_uart_driver.h.

17.58.3 Enumeration Type Documentation

17.58.3.1 enum flexio_uart_driver_direction_t

flexio_uart driver direction (tx or rx)

This structure describes the direction configuration options for the flexio_uart driver. Implements : flexio_uart_driver_direction_t_Class

Enumerator

FLEXIO_UART_DIRECTION_TX Tx UART driver

FLEXIO_UART_DIRECTION_RX Rx UART driver

Definition at line 42 of file flexio_uart_driver.h.

17.58.4 Function Documentation

17.58.4.1 status_t FLEXIO_UART_DRV_Deinit (flexio_uart_state_t * state)

De-initialize the FLEXIO_UART driver.

This function de-initializes the FLEXIO_UART driver. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

<i>state</i>	Pointer to the FLEXIO_UART driver context structure.
--------------	--

Returns

Error or success status returned by API

Definition at line 1065 of file flexio_uart_driver.c.

17.58.4.2 status_t FLEXIO_UART_DRV_GetBaudRate (flexio_uart_state_t * state, uint32_t * baudRate)

Get the currently configured baud rate.

This function returns the currently configured UART baud rate.

Parameters

<i>state</i>	Pointer to the FLEXIO_UART driver context structure.
<i>baudRate</i>	the current baud rate in hertz

Returns

Error or success status returned by API

Definition at line 1142 of file flexio_uart_driver.c.

17.58.4.3 void FLEXIO_UART_DRV_GetDefaultConfig (flexio_uart_user_config_t * userConfigPtr)

Returns default configuration structure for FLEXIO_UART.

Parameters

<i>userConfigPtr</i>	Pointer to the FLEXIO_UART user configuration structure.
----------------------	--

Definition at line 1495 of file flexio_uart_driver.c.

17.58.4.4 `status_t FLEXIO_UART_DRV_GetStatus (flexio_uart_state_t * state, uint32_t * bytesRemaining)`

Get the status of the current non-blocking UART transfer.

This function returns the current status of a non-blocking UART transfer. A return code of STATUS_BUSY means the transfer is still in progress. Otherwise the function returns a status reflecting the outcome of the last transfer. When the driver is initialized in polling mode this function also advances the transfer by checking and handling the transmit and receive events, so it must be called frequently to avoid overflows or underflows.

Parameters

<i>state</i>	Pointer to the FLEXIO_UART driver context structure.
<i>bytesRemaining</i>	the remaining number of bytes to be transferred

Note

In DMA mode, this parameter may not be accurate, in case the transfer completes right after calling this function; in this edge-case, the parameter will reflect the initial transfer size, due to automatic reloading of the major loop count in the DMA transfer descriptor.

Returns

Error or success status returned by API

Definition at line 1396 of file flexio_uart_driver.c.

17.58.4.5 `status_t FLEXIO_UART_DRV_Init (uint32_t instance, const flexio_uart_user_config_t * userConfigPtr, flexio_uart_state_t * state)`

Initialize the FLEXIO_UART driver.

This function initializes the FLEXIO_UART driver.

Parameters

<i>instance</i>	FLEXIO peripheral instance number
<i>userConfigPtr</i>	Pointer to the FLEXIO_UART user configuration structure. The function reads configuration data from this structure and initializes the driver accordingly. The application may free this structure after the function returns.
<i>state</i>	Pointer to the FLEXIO_UART driver context structure. The driver uses this memory area for its internal logic. The application must make no assumptions about the content of this structure, and must not free this memory until the driver is de-initialized using FLEXIO_UART_DRV_Deinit() .

Returns

Error or success status returned by API

Definition at line 959 of file flexio_uart_driver.c.

17.58.4.6 `status_t FLEXIO_UART_DRV_ReceiveData (flexio_uart_state_t * state, uint8_t * rxBuff, uint32_t rxSize)`

Perform a non-blocking UART reception.

This function receives a block of data and returns immediately. The rest of the transmission is handled by the interrupt service routine (if the driver is initialized in interrupt mode) or by the [FLEXIO_UART_DRV_GetReceiveStatus\(\)](#) function (if the driver is initialized in polling mode).

Parameters

<i>state</i>	Pointer to the FLEXIO_UART driver context structure.
<i>rxBuff</i>	pointer to the receive buffer
<i>rxSize</i>	length in bytes of the data to be received

Returns

Error or success status returned by API

Definition at line 1278 of file flexio_uart_driver.c.

17.58.4.7 `status_t FLEXIO_UART_DRV_ReceiveDataBlocking (flexio_uart_state_t * state, uint8_t * rxBuff, uint32_t rxSize, uint32_t timeout)`

Perform a blocking UART reception.

This function receives a block of data and only returns when the transmission is complete.

Parameters

<i>state</i>	Pointer to the FLEXIO_UART driver context structure.
<i>rxBuff</i>	pointer to the receive buffer
<i>rxSize</i>	length in bytes of the data to be received
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 1339 of file flexio_uart_driver.c.

17.58.4.8 `status_t FLEXIO_UART_DRV_SendData (flexio_uart_state_t * state, const uint8_t * txBuff, uint32_t txSize)`

Perform a non-blocking UART transmission.

This function sends a block of data and returns immediately. The rest of the transmission is handled by the interrupt service routine (if the driver is initialized in interrupt mode) or by the FLEXIO_UART_DRV_GetTransmitStatus() function (if the driver is initialized in polling mode).

Parameters

<i>state</i>	Pointer to the FLEXIO_UART driver context structure.
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 1182 of file flexio_uart_driver.c.

17.58.4.9 `status_t FLEXIO_UART_DRV_SendDataBlocking (flexio_uart_state_t * state, const uint8_t * txBuff, uint32_t txSize, uint32_t timeout)`

Perform a blocking UART transmission.

This function sends a block of data and only returns when the transmission is complete.

Parameters

<i>state</i>	Pointer to the FLEXIO_UART driver context structure.
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 1245 of file flexio_uart_driver.c.

17.58.4.10 `status_t FLEXIO_UART_DRV_SetConfig (flexio_uart_state_t * state, uint32_t baudRate, uint8_t bitCount)`

Set the baud rate and bit width for any subsequent UART communication.

This function sets the baud rate and bit width for the UART driver. Note that due to module limitation not any baud rate can be achieved. The driver will set a baud rate as close as possible to the requested baud rate, but there may still be substantial differences, for example if requesting a high baud rate while using a low-frequency FlexIO clock. The application should call [FLEXIO_UART_DRV_GetBaudRate\(\)](#) after [FLEXIO_UART_DRV_SetConfig\(\)](#) to check what baud rate was actually set.

Parameters

<i>state</i>	Pointer to the FLEXIO_UART driver context structure.
<i>baudRate</i>	the desired baud rate in hertz
<i>bitCount</i>	number of bits per word

Returns

Error or success status returned by API

Definition at line 1092 of file flexio_uart_driver.c.

17.58.4.11 `status_t FLEXIO_UART_DRV_SetRxBuffer (flexio_uart_state_t * state, uint8_t * rxBuff, uint32_t rxSize)`

Provide a buffer for receiving data.

This function can be used to provide a new buffer for receiving data to the driver. It can be called from the user callback when event STATUS_UART_RX_OVERRUN is reported. This way the reception will continue without interruption.

Parameters

<i>state</i>	Pointer to the FLEXIO_UART driver context structure.
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 1449 of file flexio_uart_driver.c.

17.58.4.12 `status_t FLEXIO_UART_DRV_SetTxBuffer (flexio_uart_state_t * state, const uint8_t * txBuff, uint32_t txSize)`

Provide a buffer for transmitting data.

This function can be used to provide a new buffer for transmitting data to the driver. It can be called from the user callback when event STATUS_UART_TX_UNDERRUN is reported. This way the transmission will continue without interruption.

Parameters

<i>state</i>	Pointer to the FLEXIO_UART driver context structure.
<i>txBuff</i>	pointer to the buffer containing transmit data
<i>txSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 1471 of file flexio_uart_driver.c.

17.58.4.13 `status_t FLEXIO_UART_DRV_TransferAbort(flexio_uart_state_t * state)`

Aborts a non-blocking UART transfer.

This function aborts a non-blocking UART transfer.

Parameters

<i>state</i>	Pointer to the FLEXIO_UART driver context structure.
--------------	--

Returns

Error or success status returned by API

Definition at line 1372 of file flexio_uart_driver.c.

17.59 FlexTimer (FTM)

17.59.1 Detailed Description

FlexTimer Peripheral Driver.

Hardware background

The FTM of the S32K1xx is based on a 16 bits counter and supports: input capture, output compare, PWM and some instances include quadrature decoder. The main features are:

- FTM source clock is selectable (Source clock can be the system clock, the fixed frequency clock, or an external clock)
- Prescaler: 1, 2, 4, 8, 16, 32, 64, 128
- 16 bit counter (up and up-down counting)
- Each channel can be configured for input capture, output compare, or PWM mode.
- Input Capture mode (single edge, dual edge or measure period/duty cycle)
- Output Compare mode (set, cleared or toggle on match)
- All channels can be configured for center-aligned PWM mode.
- Each pair of channels can be combined to generate a PWM signal with independent control of both edges of PWM signal and with dead-time insertion.
- Up to 4 fault inputs for global fault control
- Dual edge capture for pulse and period width measurement
- Quadrature decoder with input filters, relative position counting, and interrupt on position count or capture of position count on external event.

Modules

- [FlexTimer Input Capture Driver \(FTM_IC\)](#)
FlexTimer Input Capture Peripheral Driver.
- [FlexTimer Module Counter Driver \(FTM_MC\)](#)
FlexTimer Module Counter Peripheral Driver.
- [FlexTimer Output Compare Driver \(FTM_OC\)](#)
FlexTimer Output Compare Peripheral Driver.
- [FlexTimer Pulse Width Modulation Driver \(FTM_PWM\)](#)
FlexTimer Pulse Width Modulation Peripheral Driver.
- [FlexTimer Quadrature Decoder Driver \(FTM_QD\)](#)
FlexTimer Quadrature Decoder Peripheral Driver.

Data Structures

- struct [ftm_state_t](#)
FlexTimer state structure of the driver. [More...](#)
- struct [ftm_pwm_sync_t](#)
FlexTimer Registers sync parameters Please don't use software and hardware trigger simultaneously Implements : [ftm_pwm_sync_t_Class](#). [More...](#)
- struct [ftm_user_config_t](#)
Configuration structure that the user needs to set. [More...](#)

Macros

- #define **FTM_RMW_SC**(base, mask, value) (((base)->SC) = (((base)->SC) & ~(mask)) | (value)))
FTM_SC - Read and modify and write to Status And Control (RW)
- #define **FTM_RMW_CNT**(base, mask, value) (((base)->CNT) = (((base)->CNT) & ~(mask)) | (value)))
FTM_CNT - Read and modify and write to Counter (RW)
- #define **FTM_RMW_MOD**(base, mask, value) (((base)->MOD) = (((base)->MOD) & ~(mask)) | (value)))
FTM_MOD - Read and modify and write Modulo (RW)
- #define **FTM_RMW_CNTIN**(base, mask, value) (((base)->CNTIN) = (((base)->CNTIN) & ~(mask)) | (value)))
FTM_CNTIN - Read and modify and write Counter Initial Value (RW)
- #define **FTM_RMW_STATUS**(base, mask, value) (((base)->STATUS) = (((base)->STATUS) & ~(mask)) | (value)))
FTM_STATUS - Read and modify and write Capture And Compare Status (RW)
- #define **FTM_RMW_MODE**(base, mask, value) (((base)->MODE) = (((base)->MODE) & ~(mask)) | (value)))
FTM_MODE - Read and modify and write Counter Features Mode Selection (RW)
- #define **FTM_RMW_CnSCV_REG**(base, channel, mask, value) (((base)->CONTROLS[channel].CnSC) = (((base)->CONTROLS[channel].CnSC) & ~(mask)) | (value)))
FTM_CnSCV - Read and modify and write Channel (n) Status And Control (RW)
- #define **FTM_RMW_DEADTIME**(base, mask, value) (((base)->DEADTIME) = (((base)->DEADTIME) & ~(mask)) | (value)))
FTM_DEADTIME - Read and modify and write Dead-time Insertion Control (RW)
- #define **FTM_RMW_EXTTRIG_REG**(base, mask, value) (((base)->EXTTRIG) = (((base)->EXTTRIG) & ~(mask)) | (value)))
FTM_EXTTRIG - Read and modify and write External Trigger Control (RW)
- #define **FTM_RMW_FLTCTRL**(base, mask, value) (((base)->FLTCTRL) = (((base)->FLTCTRL) & ~(mask)) | (value)))
FTM_FLTCTRL - Read and modify and write Fault Control (RW)
- #define **FTM_RMW_FMS**(base, mask, value) (((base)->FMS) = (((base)->FMS) & ~(mask)) | (value)))
FTM_FMS - Read and modify and write Fault Mode Status (RW)
- #define **FTM_RMW_CONF**(base, mask, value) (((base)->CONF) = (((base)->CONF) & ~(mask)) | (value)))
FTM_CONF - Read and modify and write Configuration (RW)
- #define **FTM_RMW_POL**(base, mask, value) (((base)->POL) = (((base)->POL) & ~(mask)) | (value)))
POL - Read and modify and write Polarity (RW)
- #define **FTM_RMW_FILTER**(base, mask, value) (((base)->FILTER) = (((base)->FILTER) & ~(mask)) | (value)))
FILTER - Read and modify and write Filter (RW)
- #define **FTM_RMW_SYNC**(base, mask, value) (((base)->SYNC) = (((base)->SYNC) & ~(mask)) | (value)))
SYNC - Read and modify and write Synchronization (RW)
- #define **FTM_RMW_QDCTRL**(base, mask, value) (((base)->QDCTRL) = (((base)->QDCTRL) & ~(mask)) | (value)))
QDCTRL - Read and modify and write Quadrature Decoder Control And Status (RW)
- #define **FTM_RMW_PAIR0DEADTIME**(base, mask, value) (((base)->PAIR0DEADTIME) = (((base)->PAIR0DEADTIME) & ~(mask)) | (value)))
FTM_PAIR0DEADTIME - Read and modify and write Dead-time Insertion Control for the pair 0 (RW)
- #define **FTM_RMW_PAIR1DEADTIME**(base, mask, value) (((base)->PAIR1DEADTIME) = (((base)->PAIR1DEADTIME) & ~(mask)) | (value)))
FTM_PAIR1DEADTIME - Read and modify and write Dead-time Insertion Control for the pair 1 (RW)
- #define **FTM_RMW_PAIR2DEADTIME**(base, mask, value) (((base)->PAIR2DEADTIME) = (((base)->PAIR2DEADTIME) & ~(mask)) | (value)))
FTM_PAIR2DEADTIME - Read and modify and write Dead-time Insertion Control for the pair 2 (RW)

- #define `FTM_RMW_PAIR3DEADTIME`(base, mask, value) (((base)->PAIR3DEADTIME) = (((base)->PAIR3DEADTIME) & ~(mask)) | (value)))
FTM_PAIR3DEADTIME - Read and modify and write Dead-time Insertion Control for the pair 3 (RW)
- #define `CHAN0_IDX` (0U)
Channel number for CHAN1.
- #define `CHAN1_IDX` (1U)
Channel number for CHAN2.
- #define `CHAN2_IDX` (2U)
Channel number for CHAN3.
- #define `CHAN3_IDX` (3U)
Channel number for CHAN4.
- #define `CHAN4_IDX` (4U)
Channel number for CHAN5.
- #define `CHAN5_IDX` (5U)
Channel number for CHAN6.
- #define `CHAN6_IDX` (6U)
Channel number for CHAN7.
- #define `CHAN7_IDX` (7U)

Enumerations

- enum `ftm_config_mode_t` {
`FTM_MODE_NOT_INITIALIZED` = 0x00U, `FTM_MODE_INPUT_CAPTURE` = 0x01U, `FTM_MODE_OUTPUT_COMPARE` = 0x02U, `FTM_MODE_EDGE_ALIGNED_PWM` = 0x03U,
`FTM_MODE_CEN_ALIGNED_PWM` = 0x04U, `FTM_MODE_QUADRATURE_DECODER` = 0x05U, `FTM_MODE_UP_TIMER` = 0x06U, `FTM_MODE_UP_DOWN_TIMER` = 0x07U,
`FTM_MODE_EDGE_ALIGNED_PWM_AND_INPUT_CAPTURE` = 0x08U }
FlexTimer operation mode.
- enum `ftm_clock_source_t` { `FTM_CLOCK_SOURCE_NONE` = 0x00U, `FTM_CLOCK_SOURCE_SYSTEM_CLK` = 0x01U, `FTM_CLOCK_SOURCE_FIXEDCLK` = 0x02U, `FTM_CLOCK_SOURCE_EXTERNALCLK` = 0x03U }
FlexTimer clock source selection.
- enum `ftm_clock_ps_t` {
`FTM_CLOCK_DIVID_BY_1` = 0x00U, `FTM_CLOCK_DIVID_BY_2` = 0x01U, `FTM_CLOCK_DIVID_BY_4` = 0x02U, `FTM_CLOCK_DIVID_BY_8` = 0x03U,
`FTM_CLOCK_DIVID_BY_16` = 0x04U, `FTM_CLOCK_DIVID_BY_32` = 0x05U, `FTM_CLOCK_DIVID_BY_64` = 0x06U, `FTM_CLOCK_DIVID_BY_128` = 0x07U }
FlexTimer pre-scaler factor selection for the clock source. In quadrature decoder mode set FTM_CLOCK_DIVID_BY_1.
- enum `ftm_interrupt_option_t` {
`FTM_CHANNEL0_INT_ENABLE` = 0x00000001U, `FTM_CHANNEL1_INT_ENABLE` = 0x00000002U, `FTM_CHANNEL2_INT_ENABLE` = 0x00000004U, `FTM_CHANNEL3_INT_ENABLE` = 0x00000008U,
`FTM_CHANNEL4_INT_ENABLE` = 0x00000010U, `FTM_CHANNEL5_INT_ENABLE` = 0x00000020U, `FTM_CHANNEL6_INT_ENABLE` = 0x00000040U, `FTM_CHANNEL7_INT_ENABLE` = 0x00000080U,
`FTM_FAULT_INT_ENABLE` = 0x00000100U, `FTM_TIME_OVER_FLOW_INT_ENABLE` = 0x00000200U, `FTM_RELOAD_INT_ENABLE` = 0x00000400U }
List of FTM interrupts.
- enum `ftm_status_flag_t` {
`FTM_CHANNEL0_FLAG` = 0x00000001U, `FTM_CHANNEL1_FLAG` = 0x00000002U, `FTM_CHANNEL2_FLAG` = 0x00000004U, `FTM_CHANNEL3_FLAG` = 0x00000008U,
`FTM_CHANNEL4_FLAG` = 0x00000010U, `FTM_CHANNEL5_FLAG` = 0x00000020U, `FTM_CHANNEL6_FLAG` = 0x00000040U, `FTM_CHANNEL7_FLAG` = 0x00000080U,
`FTM_FAULT_FLAG` = 0x00000100U, `FTM_TIME_OVER_FLOW_FLAG` = 0x00000200U, `FTM_RELOAD_FLAG` = 0x00000400U, `FTM_CHANNEL_TRIGGER_FLAG` = 0x00000800U }

List of FTM flags.

- enum `ftm_reg_update_t` { `FTM_SYSTEM_CLOCK` = 0U, `FTM_PWM_SYNC` = 1U }

FTM sync source.

- enum `ftm_pwm_sync_mode_t` { `FTM_WAIT_LOADING_POINTS` = 0U, `FTM_UPDATE_NOW` = 1U }

FTM update register.

- enum `ftm_deadtime_ps_t` { `FTM_DEADTIME_DIVID_BY_1` = 0x01U, `FTM_DEADTIME_DIVID_BY_4` = 0x02U, `FTM_DEADTIME_DIVID_BY_16` = 0x03U }

FlexTimer pre-scaler factor for the dead-time insertion.

- enum `ftm_bdm_mode_t` { `FTM_BDM_MODE_00` = 0x00U, `FTM_BDM_MODE_01` = 0x01U, `FTM_BDM_MODE_10` = 0x02U, `FTM_BDM_MODE_11` = 0x03U }

Options for the FlexTimer behavior in BDM Mode.

Functions

- static void `FTM_DRV_SetClockFilterPs` (FTM_Type *const ftmBase, uint8_t filterPrescale)
Sets the filter Pre-scaler divider.
- static uint8_t `FTM_DRV_GetClockFilterPs` (const FTM_Type *ftmBase)
Reads the FTM filter clock divider.
- static uint16_t `FTM_DRV_GetCounter` (const FTM_Type *ftmBase)
Returns the FTM peripheral current counter value.
- static uint16_t `FTM_DRV_GetMod` (const FTM_Type *ftmBase)
Returns the FTM peripheral counter modulo value.
- static uint16_t `FTM_DRV_GetCounterInitVal` (const FTM_Type *ftmBase)
Returns the FTM peripheral counter initial value.
- static void `FTM_DRV_ClearChSC` (FTM_Type *const ftmBase, uint8_t channel)
Clears the content of Channel (n) Status And Control.
- static uint8_t `FTM_DRV_GetChnEdgeLevel` (const FTM_Type *ftmBase, uint8_t channel)
Gets the FTM peripheral timer channel edge level.
- static void `FTM_DRV_SetChnIcrstCmd` (FTM_Type *const ftmBase, uint8_t channel, bool enable)
Configure the feature of FTM counter reset by the selected input capture event.
- static bool `FTM_DRV_IsChnIcrst` (const FTM_Type *ftmBase, uint8_t channel)
Returns whether the FTM FTM counter is reset.
- static void `FTM_DRV_SetChnDmaCmd` (FTM_Type *const ftmBase, uint8_t channel, bool enable)
Enables or disables the FTM peripheral timer channel DMA.
- static bool `FTM_DRV_IsChnDma` (const FTM_Type *ftmBase, uint8_t channel)
Returns whether the FTM peripheral timer channel DMA is enabled.
- static void `FTM_DRV_SetTrigModeControlCmd` (FTM_Type *const ftmBase, uint8_t channel, bool enable)
Enables or disables the trigger generation on FTM channel outputs.
- static bool `FTM_DRV_GetTriggerControlled` (const FTM_Type *ftmBase, uint8_t channel)
Returns whether the trigger mode is enabled.
- static bool `FTM_DRV_GetChnInputState` (const FTM_Type *ftmBase, uint8_t channel)
Get the state of channel input.
- static bool `FTM_DRV_GetChnOutputValue` (const FTM_Type *ftmBase, uint8_t channel)
Get the value of channel output.
- static uint16_t `FTM_DRV_GetChnCountVal` (const FTM_Type *ftmBase, uint8_t channel)
Gets the FTM peripheral timer channel counter value.
- static bool `FTM_DRV_GetChnEventStatus` (const FTM_Type *ftmBase, uint8_t channel)
Gets the FTM peripheral timer channel event status.
- static uint32_t `FTM_DRV_GetEventStatus` (const FTM_Type *ftmBase)
Gets the FTM peripheral timer status info for all channels.
- static void `FTM_DRV_ClearChnEventStatus` (FTM_Type *const ftmBase, uint8_t channel)

- Clears the FTM peripheral timer all channel event status.*
- static void [FTM_DRV_SetChnOutputMask](#) (FTM_Type *const ftmBase, uint8_t channel, bool mask)
Sets the FTM peripheral timer channel output mask.
- static void [FTM_DRV_SetChnOutputInitStateCmd](#) (FTM_Type *const ftmBase, uint8_t channel, bool state)
Sets the FTM peripheral timer channel output initial state 0 or 1.
- static void [FTM_DRV_DisableFaultInt](#) (FTM_Type *const ftmBase)
Disables the FTM peripheral timer fault interrupt.
- static void [FTM_DRV_SetCaptureTestCmd](#) (FTM_Type *const ftmBase, bool enable)
Enables or disables the FTM peripheral timer capture test mode.
- static bool [FTM_DRV_IsFtmEnable](#) (const FTM_Type *ftmBase)
Get status of the FTMEN bit in the FTM_MODE register.
- static void [FTM_DRV_SetCountReinitSyncCmd](#) (FTM_Type *const ftmBase, bool enable)
Determines if the FTM counter is re-initialized when the selected trigger for synchronization is detected.
- static bool [FTM_DRV_IsWriteProtectionEnabled](#) (const FTM_Type *ftmBase)
Checks whether the write protection is enabled.
- static bool [FTM_DRV_IsFaultInputEnabled](#) (const FTM_Type *ftmBase)
Checks whether the logic OR of the fault inputs is enabled.
- static bool [FTM_DRV_IsFaultFlagDetected](#) (const FTM_Type *ftmBase, uint8_t channel)
Checks whether a fault condition is detected at the fault input.
- static void [FTM_DRV_ClearFaultFlagDetected](#) (FTM_Type *const ftmBase, uint8_t channel)
Clear a fault condition is detected at the fault input.
- static void [FTM_DRV_SetDualChnInvertCmd](#) (FTM_Type *const ftmBase, uint8_t chnIPairNum, bool enable)
Enables or disables the channel invert for a channel pair.
- static void [FTM_DRV_SetChnSoftwareCtrlCmd](#) (FTM_Type *const ftmBase, uint8_t channel, bool enable)
Enables or disables the channel software output control.
- static void [FTM_DRV_SetChnSoftwareCtrlVal](#) (FTM_Type *const ftmBase, uint8_t channel, bool enable)
Sets the channel software output control value. Despite the odd channels are configured as HIGH/LOW, they will be inverted in the following configuration: COMP bit = 1 and CH(n)OCV and CH(n+1)OCV are HIGH. Please check Software output control behavior chapter from RM.
- static void [FTM_DRV_SetGlobalLoadCmd](#) (FTM_Type *const ftmBase)
Set the global load mechanism.
- static void [FTM_DRV_SetLoadCmd](#) (FTM_Type *const ftmBase, bool enable)
Enable the global load.
- static void [FTM_DRV_SetHalfCycleCmd](#) (FTM_Type *const ftmBase, bool enable)
Enable the half cycle reload.
- static void [FTM_DRV_SetPwmLoadCmd](#) (FTM_Type *const ftmBase, bool enable)
Enables or disables the loading of MOD, CNTIN and CV with values of their write buffer.
- static void [FTM_DRV_SetPwmLoadChnSelCmd](#) (FTM_Type *const ftmBase, uint8_t channel, bool enable)
Includes or excludes the channel in the matching process.
- static void [FTM_DRV_SetInitTrigOnReloadCmd](#) (FTM_Type *const ftmBase, bool enable)
Enables or disables the FTM initialization trigger on Reload Point.
- static void [FTM_DRV_SetGlobalTimeBaseOutputCmd](#) (FTM_Type *const ftmBase, bool enable)
Enables or disables the FTM global time base signal generation to other FTM's.
- static void [FTM_DRV_SetGlobalTimeBaseCmd](#) (FTM_Type *const ftmBase, bool enable)
Enables or disables the FTM timer global time base.
- static void [FTM_DRV_SetLoadFreq](#) (FTM_Type *const ftmBase, uint8_t val)
Sets the frequency of reload points.
- static void [FTM_DRV_SetExtPairDeadtimeValue](#) (FTM_Type *const ftmBase, uint8_t channelPair, uint8_t value)
Sets the FTM extended dead-time value for the channel pair.

- static void [FTM_DRV_SetPairDeadtimePrescale](#) (FTM_Type *const ftmBase, uint8_t channelPair, [ftm_deadtime_ps_t](#) divider)
Sets the FTM dead time divider for the channel pair.
- static void [FTM_DRV_SetPairDeadtimeCount](#) (FTM_Type *const ftmBase, uint8_t channelPair, uint8_t count)
Sets the FTM dead-time value for the channel pair.
- status_t [FTM_DRV_Init](#) (uint32_t instance, const [ftm_user_config_t](#) *info, [ftm_state_t](#) *state)
Initializes the FTM driver.
- status_t [FTM_DRV_Deinit](#) (uint32_t instance)
Shuts down the FTM driver.
- void [FTM_DRV_GetDefaultConfig](#) ([ftm_user_config_t](#) *const config)
This function will get the default configuration values in the structure which is used as a common use-case.
- status_t [FTM_DRV_MaskOutputChannels](#) (uint32_t instance, uint32_t channelsMask, bool softwareTrigger)
This function will mask the output of the channels and at match events will be ignored by the masked channels.
- status_t [FTM_DRV_SetInitialCounterValue](#) (uint32_t instance, uint16_t counterValue, bool softwareTrigger)
This function configure the initial counter value. The counter will get this value after an overflow event.
- status_t [FTM_DRV_SetHalfCycleReloadPoint](#) (uint32_t instance, uint16_t reloadPoint, bool softwareTrigger)
This function configure the value of the counter which will generates an reload point.
- status_t [FTM_DRV_SetSoftOutChnValue](#) (uint32_t instance, uint8_t channelsValues, bool softwareTrigger)
This function will force the output value of a channel to a specific value. Before using this function it's mandatory to mask the match events using [FTM_DRV_MaskOutputChannels](#) and to enable software output control using [FTM_DRV_SetSoftwareOutputChannelControl](#). : When the PWM signal is configured with LOW/HIGH polarity on the channel (n). It should be set the safe state as LOW level state. However, We will have an issue with COMP bit is zero and CH(n)OCV is HIGH and CH(n+1)OCV is LOW.in the independent channel configuration. Code configuration: { .polarity = FTM_POLARITY_HIGH, .safeState = FTM_POLARITY_LOW, .enableSecondChannelOutput = true, .secondChannelPolarity = FTM_MAIN_DUPLICATED, }.
- status_t [FTM_DRV_SetSoftwareOutputChannelControl](#) (uint32_t instance, uint8_t channelsMask, bool softwareTrigger)
This function will configure which output channel can be software controlled. Software output control forces the following values on channels (n) and (n+1) when the COMP bit is zero and POL bit is zero. CH(n)OCV|CH(n+1)OCV|CH(n)OCV|CH(n+1)OCV|Channel (n) Output | Channel (n+1) Output 0 | 0 | X | X | is not modified by SWOC | is not modified by SWOC 1 | 1 | 0 | 0 | is forced to zero | is forced to zero 1 | 1 | 0 | 1 | is forced to zero | is forced to one 1 | 1 | 1 | 0 | is forced to one | is forced to zero 1 | 1 | 1 | 1 | is forced to one | is forced to one.
- status_t [FTM_DRV_SetAllChnSoftwareOutputControl](#) (uint32_t instance, uint8_t channelMask, uint8_t channelValueMask, bool softwareTrigger)
This function will control list of channels by software to force the output to specified value. Despite the odd channels are configured as HIGH/LOW, they will be inverted in the following configuration: COMP bit = 1 and CH(n)OCV and CH(n+1)OCV are HIGH. Please check software output control behavior chapter from reference manual. : When the PWM signal is configured with LOW/HIGH polarity on the channel (n). It should be set the safe state as LOW level state. However, We will have an issue with COMP bit is zero and CH(n)OCV is HIGH and CH(n+1)OCV is LOW.in the independent channel configuration. Code configuration: { .polarity = FTM_POLARITY_HIGH, .safeState = FTM_POLARITY_LOW, .enableSecondChannelOutput = true, .secondChannelPolarity = FTM_MAIN_DUPLICATED, }.
- status_t [FTM_DRV_SetInvertingControl](#) (uint32_t instance, uint8_t channelsPairMask, bool softwareTrigger)
This function will configure if the second channel of a pair will be inverted or not.
- status_t [FTM_DRV_SetModuloCounterValue](#) (uint32_t instance, uint16_t counterValue, bool softwareTrigger)
This function configure the maximum counter value.
- status_t [FTM_DRV_SetOutputlevel](#) (uint32_t instance, uint8_t channel, uint8_t level)
This function will set the channel edge or level on the selection of the channel mode.
- status_t [FTM_DRV_SetSync](#) (uint32_t instance, const [ftm_pwm_sync_t](#) *param)
This function configures sync mechanism for some FTM registers (MOD, CNINT, HCR, CnV, OUTMASK, INVCTRL, SWOCTRL).
- status_t [FTM_DRV_GenerateHardwareTrigger](#) (uint32_t instance)
This function is used to configure a trigger source for FTM instance. This allow a hardware trigger input which can be used in PWM synchronization. Note that the hardware trigger is implemented only on trigger 1 for each instance.
- status_t [FTM_DRV_EnableInterrupts](#) (uint32_t instance, uint32_t interruptMask)

This function will enable the generation a list of interrupts. It includes the FTM overflow interrupts, the reload point interrupt, the fault interrupt and the channel (n) interrupt.

- void [FTM_DRV_DisableInterrupts](#) (uint32_t instance, uint32_t interruptMask)

This function is used to disable some interrupts.

- uint32_t [FTM_DRV_GetEnabledInterrupts](#) (uint32_t instance)

This function will get the enabled FTM interrupts.

- uint32_t [FTM_DRV_GetStatusFlags](#) (uint32_t instance)

This function will get the FTM status flags. : Regarding the duty cycle is 100% at the channel output, the match interrupt has no event due to the C(n)V and C(n+1)V value are not between CNTIN value and MOD value.

- void [FTM_DRV_ClearStatusFlags](#) (uint32_t instance, uint32_t flagMask)

This function is used to clear the FTM status flags.

- uint32_t [FTM_DRV_GetFrequency](#) (uint32_t instance)

Retrieves the frequency of the clock source feeding the FTM counter.

- uint16_t [FTM_DRV_ConvertFreqToPeriodTicks](#) (uint32_t instance, uint32_t frequencyHz)

This function is used to covert the given frequency to period in ticks.

- status_t [FTM_DRV_CounterReset](#) (uint32_t instance, bool softwareTrigger)

This function will allow the FTM to restart the counter to its initial counting value in the register. Note that the configuration is set in the [FTM_DRV_SetSync\(\)](#) function to make sure that the FTM registers are updated by software trigger or hardware trigger.

Variables

- FTM_Type *const [g_ftmBase](#) [FTM_INSTANCE_COUNT]

Table of base addresses for FTM instances.

- const IRQn_Type [g_ftmIrqlId](#) [FTM_INSTANCE_COUNT][FEATURE_FTM_CHANNEL_COUNT]

Interrupt vectors for the FTM peripheral.

- const IRQn_Type [g_ftmFaultIrqlId](#) [FTM_INSTANCE_COUNT]
- const IRQn_Type [g_ftmOverflowIrqlId](#) [FTM_INSTANCE_COUNT]
- const IRQn_Type [g_ftmReloadIrqlId](#) [FTM_INSTANCE_COUNT]
- [ftm_state_t](#) * [ftmStatePtr](#) [FTM_INSTANCE_COUNT]

Pointer to runtime state structure.

17.59.2 Data Structure Documentation

17.59.2.1 struct ftm_state_t

FlexTimer state structure of the driver.

Implements : [ftm_state_t_Class](#)

Definition at line 376 of file [ftm_common.h](#).

Data Fields

- [ftm_clock_source_t](#) [ftmClockSource](#)
- [ftm_config_mode_t](#) [ftmMode](#)
- uint16_t [ftmModValue](#)
- uint16_t [ftmPeriod](#)
- uint32_t [ftmSourceClockFrequency](#)
- uint16_t [measurementResults](#) [FEATURE_FTM_CHANNEL_COUNT]
- void * [channelsCallbacksParams](#) [FEATURE_FTM_CHANNEL_COUNT]
- ic_callback_t [channelsCallbacks](#) [FEATURE_FTM_CHANNEL_COUNT]
- bool [enableNotification](#) [FEATURE_FTM_CHANNEL_COUNT]

Field Documentation

17.59.2.1.1 `ic_callback_t channelsCallbacks[FEATURE_FTM_CHANNEL_COUNT]`

The callback function for channels events

Definition at line 385 of file `ftm_common.h`.

17.59.2.1.2 `void* channelsCallbacksParams[FEATURE_FTM_CHANNEL_COUNT]`

The parameters of callback function for channels events

Definition at line 384 of file `ftm_common.h`.

17.59.2.1.3 `bool enableNotification[FEATURE_FTM_CHANNEL_COUNT]`

To save channels enable the notification on the callback application

Definition at line 386 of file `ftm_common.h`.

17.59.2.1.4 `ftm_clock_source_t ftmClockSource`

Clock source used by FTM counter

Definition at line 378 of file `ftm_common.h`.

17.59.2.1.5 `ftm_config_mode_t ftmMode`

Mode of operation for FTM

Definition at line 379 of file `ftm_common.h`.

17.59.2.1.6 `uint16_t ftmModValue`

This field is used only in input capture mode to store MOD value

Definition at line 380 of file `ftm_common.h`.

17.59.2.1.7 `uint16_t ftmPeriod`

This field is used only in PWM mode to store signal period

Definition at line 381 of file `ftm_common.h`.

17.59.2.1.8 `uint32_t ftmSourceClockFrequency`

The clock frequency is used for counting

Definition at line 382 of file `ftm_common.h`.

17.59.2.1.9 `uint16_t measurementResults[FEATURE_FTM_CHANNEL_COUNT]`

This field is used only in input capture mode to store edges time stamps

Definition at line 383 of file `ftm_common.h`.

17.59.2.2 `struct ftm_pwm_sync_t`

FlexTimer Registers sync parameters Please don't use software and hardware trigger simultaneously Implements : `ftm_pwm_sync_t_Class`.

Definition at line 394 of file `ftm_common.h`.

Data Fields

- bool [softwareSync](#)
- bool [hardwareSync0](#)

- bool [hardwareSync1](#)
- bool [hardwareSync2](#)
- bool [maxLoadingPoint](#)
- bool [minLoadingPoint](#)
- [ftm_reg_update_t](#) [inverterSync](#)
- [ftm_reg_update_t](#) [outRegSync](#)
- [ftm_reg_update_t](#) [maskRegSync](#)
- [ftm_reg_update_t](#) [initCounterSync](#)
- bool [autoClearTrigger](#)
- [ftm_pwm_sync_mode_t](#) [syncPoint](#)

Field Documentation

17.59.2.2.1 bool [autoClearTrigger](#)

Available only for hardware trigger

Definition at line 412 of file [ftm_common.h](#).

17.59.2.2.2 bool [hardwareSync0](#)

True - enable hardware 0 sync, False - disable hardware 0 sync

Definition at line 398 of file [ftm_common.h](#).

17.59.2.2.3 bool [hardwareSync1](#)

True - enable hardware 1 sync, False - disable hardware 1 sync

Definition at line 400 of file [ftm_common.h](#).

17.59.2.2.4 bool [hardwareSync2](#)

True - enable hardware 2 sync, False - disable hardware 2 sync

Definition at line 402 of file [ftm_common.h](#).

17.59.2.2.5 [ftm_reg_update_t](#) [initCounterSync](#)

Configures CNTIN sync

Definition at line 411 of file [ftm_common.h](#).

17.59.2.2.6 [ftm_reg_update_t](#) [inverterSync](#)

Configures INVCTRL sync

Definition at line 408 of file [ftm_common.h](#).

17.59.2.2.7 [ftm_reg_update_t](#) [maskRegSync](#)

Configures OUTMASK sync

Definition at line 410 of file [ftm_common.h](#).

17.59.2.2.8 bool [maxLoadingPoint](#)

True - enable maximum loading point, False - disable maximum loading point

Definition at line 404 of file [ftm_common.h](#).

17.59.2.2.9 bool [minLoadingPoint](#)

True - enable minimum loading point, False - disable minimum loading point

Definition at line 406 of file ftm_common.h.

17.59.2.2.10 `ftm_reg_update_t` outRegSync

Configures SWOCTRL sync

Definition at line 409 of file ftm_common.h.

17.59.2.2.11 `bool` softwareSync

True - enable software sync, False - disable software sync

Definition at line 396 of file ftm_common.h.

17.59.2.2.12 `ftm_pwm_sync_mode_t` syncPoint

Configure synchronization method (waiting next loading point or immediate)

Definition at line 413 of file ftm_common.h.

17.59.2.3 `struct ftm_user_config_t`

Configuration structure that the user needs to set.

Implements : `ftm_user_config_t` Class

Definition at line 422 of file ftm_common.h.

Data Fields

- [ftm_pwm_sync_t](#) syncMethod
- [ftm_config_mode_t](#) ftmMode
- [ftm_clock_ps_t](#) ftmPrescaler
- [ftm_clock_source_t](#) ftmClockSource
- [ftm_bdm_mode_t](#) BDMMode
- `bool` isToflsrEnabled
- `bool` [enableInitializationTrigger](#)

Field Documentation

17.59.2.3.1 `ftm_bdm_mode_t` BDMMode

Select FTM behavior in BDM mode

Definition at line 430 of file ftm_common.h.

17.59.2.3.2 `bool` enableInitializationTrigger

true: enable the generation of initialization trigger false: disable the generation of initialization trigger

Definition at line 433 of file ftm_common.h.

17.59.2.3.3 `ftm_clock_source_t` ftmClockSource

Select clock source for FTM

Definition at line 429 of file ftm_common.h.

17.59.2.3.4 `ftm_config_mode_t` ftmMode

Mode of operation for FTM

Definition at line 426 of file ftm_common.h.

17.59.2.3.5 `ftm_clock_ps_t` `ftmPrescaler`

Register pre-scaler options available in the `ftm_clock_ps_t` enumeration

Definition at line 427 of file `ftm_common.h`.

17.59.2.3.6 `bool` `isToflsrEnabled`

true: enable interrupt, false: write interrupt is disabled

Definition at line 431 of file `ftm_common.h`.

17.59.2.3.7 `ftm_pwm_sync_t` `syncMethod`

Register sync options available in the `ftm_sync_method_t` enumeration

Definition at line 424 of file `ftm_common.h`.

17.59.3 Macro Definition Documentation

17.59.3.1 `#define` `CHAN0_IDX` (0U)

Channel number for CHAN1.

Definition at line 205 of file `ftm_common.h`.

17.59.3.2 `#define` `CHAN1_IDX` (1U)

Channel number for CHAN2.

Definition at line 207 of file `ftm_common.h`.

17.59.3.3 `#define` `CHAN2_IDX` (2U)

Channel number for CHAN3.

Definition at line 209 of file `ftm_common.h`.

17.59.3.4 `#define` `CHAN3_IDX` (3U)

Channel number for CHAN4.

Definition at line 211 of file `ftm_common.h`.

17.59.3.5 `#define` `CHAN4_IDX` (4U)

Channel number for CHAN5.

Definition at line 213 of file `ftm_common.h`.

17.59.3.6 `#define` `CHAN5_IDX` (5U)

Channel number for CHAN6.

Definition at line 215 of file `ftm_common.h`.

17.59.3.7 `#define` `CHAN6_IDX` (6U)

Channel number for CHAN7.

Definition at line 217 of file `ftm_common.h`.

17.59.3.8 `#define` `CHAN7_IDX` (7U)

Definition at line 219 of file `ftm_common.h`.

17.59.3.9 **#define FTM_RMW_CnSCV_REG(base, channel, mask, value)** (((base)->CONTROLS[channel].CnSC) = (((base)->CONTROLS[channel].CnSC) & ~(mask)) | (value)))

FTM_CnSCV - Read and modify and write Channel (n) Status And Control (RW)

Definition at line 112 of file ftm_common.h.

17.59.3.10 **#define FTM_RMW_CNT(base, mask, value)** (((base)->CNT) = (((base)->CNT) & ~(mask)) | (value)))

FTM_CNT - Read and modify and write to Counter (RW)

Definition at line 87 of file ftm_common.h.

17.59.3.11 **#define FTM_RMW_CNTIN(base, mask, value)** (((base)->CNTIN) = (((base)->CNTIN) & ~(mask)) | (value)))

FTM_CNTIN - Read and modify and write Counter Initial Value (RW)

Definition at line 97 of file ftm_common.h.

17.59.3.12 **#define FTM_RMW_CONF(base, mask, value)** (((base)->CONF) = (((base)->CONF) & ~(mask)) | (value)))

FTM_CONF - Read and modify and write Configuration (RW)

Definition at line 136 of file ftm_common.h.

17.59.3.13 **#define FTM_RMW_DEADTIME(base, mask, value)** (((base)->DEADTIME) = (((base)->DEADTIME) & ~(mask)) | (value)))

FTM_DEADTIME - Read and modify and write Dead-time Insertion Control (RW)

Definition at line 117 of file ftm_common.h.

17.59.3.14 **#define FTM_RMW_EXTTRIG_REG(base, mask, value)** (((base)->EXTTRIG) = (((base)->EXTTRIG) & ~(mask)) | (value)))

FTM_EXTTRIG - Read and modify and write External Trigger Control (RW)

Definition at line 121 of file ftm_common.h.

17.59.3.15 **#define FTM_RMW_FILTER(base, mask, value)** (((base)->FILTER) = (((base)->FILTER) & ~(mask)) | (value)))

FILTER - Read and modify and write Filter (RW)

Definition at line 146 of file ftm_common.h.

17.59.3.16 **#define FTM_RMW_FLTCTRL(base, mask, value)** (((base)->FLTCTRL) = (((base)->FLTCTRL) & ~(mask)) | (value)))

FTM_FLTCTRL - Read and modify and write Fault Control (RW)

Definition at line 126 of file ftm_common.h.

17.59.3.17 **#define FTM_RMW_FMS(base, mask, value)** (((base)->FMS) = (((base)->FMS) & ~(mask)) | (value)))

FTM_FMS - Read and modify and write Fault Mode Status (RW)

Definition at line 131 of file ftm_common.h.

17.59.3.18 **#define FTM_RMW_MOD(base, mask, value)** (((base)->MOD) = (((base)->MOD) & ~(mask)) | (value)))

FTM_MOD - Read and modify and write Modulo (RW)

Definition at line 92 of file ftm_common.h.

17.59.3.19 `#define FTM_RMW_MODE(base, mask, value) (((base)->MODE) = (((base)->MODE) & ~(mask)) | (value)))`

FTM_MODE - Read and modify and write Counter Features Mode Selection (RW)

Definition at line 107 of file `ftm_common.h`.

17.59.3.20 `#define FTM_RMW_PAIR0DEADTIME(base, mask, value) (((base)->PAIR0DEADTIME) = (((base)->PAIR0DEADTIME) & ~(mask)) | (value)))`

FTM_PAIR0DEADTIME - Read and modify and write Dead-time Insertion Control for the pair 0 (RW)

Definition at line 161 of file `ftm_common.h`.

17.59.3.21 `#define FTM_RMW_PAIR1DEADTIME(base, mask, value) (((base)->PAIR1DEADTIME) = (((base)->PAIR1DEADTIME) & ~(mask)) | (value)))`

FTM_PAIR1DEADTIME - Read and modify and write Dead-time Insertion Control for the pair 1 (RW)

Definition at line 166 of file `ftm_common.h`.

17.59.3.22 `#define FTM_RMW_PAIR2DEADTIME(base, mask, value) (((base)->PAIR2DEADTIME) = (((base)->PAIR2DEADTIME) & ~(mask)) | (value)))`

FTM_PAIR2DEADTIME - Read and modify and write Dead-time Insertion Control for the pair 2 (RW)

Definition at line 171 of file `ftm_common.h`.

17.59.3.23 `#define FTM_RMW_PAIR3DEADTIME(base, mask, value) (((base)->PAIR3DEADTIME) = (((base)->PAIR3DEADTIME) & ~(mask)) | (value)))`

FTM_PAIR3DEADTIME - Read and modify and write Dead-time Insertion Control for the pair 3 (RW)

Channel number for CHAN0.

Definition at line 176 of file `ftm_common.h`.

17.59.3.24 `#define FTM_RMW_POL(base, mask, value) (((base)->POL) = (((base)->POL) & ~(mask)) | (value)))`

POL - Read and modify and write Polarity (RW)

Definition at line 141 of file `ftm_common.h`.

17.59.3.25 `#define FTM_RMW_QDCTRL(base, mask, value) (((base)->QDCTRL) = (((base)->QDCTRL) & ~(mask)) | (value)))`

QDCTRL - Read and modify and write Quadrature Decoder Control And Status (RW)

Definition at line 156 of file `ftm_common.h`.

17.59.3.26 `#define FTM_RMW_SC(base, mask, value) (((base)->SC) = (((base)->SC) & ~(mask)) | (value)))`

FTM_SC - Read and modify and write to Status And Control (RW)

Definition at line 82 of file `ftm_common.h`.

17.59.3.27 `#define FTM_RMW_STATUS(base, mask, value) (((base)->STATUS) = (((base)->STATUS) & ~(mask)) | (value)))`

FTM_STATUS - Read and modify and write Capture And Compare Status (RW)

Definition at line 102 of file `ftm_common.h`.

17.59.3.28 `#define FTM_RMW_SYNC(base, mask, value) (((base)->SYNC) = (((base)->SYNC) & ~(mask)) | (value)))`

SYNC - Read and modify and write Synchronization (RW)

Definition at line 151 of file `ftm_common.h`.

17.59.4 Enumeration Type Documentation

17.59.4.1 enum `ftm_bdm_mode_t`

[Options](#) for the FlexTimer behavior in BDM Mode.

Implements : `ftm_bdm_mode_t_Class`

Enumerator

FTM_BDM_MODE_00 FTM counter stopped, CH(n)F bit can be set, FTM channels in functional mode, writes to MOD,CNTIN and C(n)V registers bypass the register buffers

FTM_BDM_MODE_01 FTM counter stopped, CH(n)F bit is not set, FTM channels outputs are forced to their safe value , writes to MOD,CNTIN and C(n)V registers bypass the register buffers

FTM_BDM_MODE_10 FTM counter stopped, CH(n)F bit is not set, FTM channels outputs are frozen when chip enters in BDM mode, writes to MOD, CNTIN and C(n)V registers bypass the register buffers

FTM_BDM_MODE_11 FTM counter in functional mode, CH(n)F bit can be set, FTM channels in functional mode, writes to MOD,CNTIN and C(n)V registers is in fully functional mode

Definition at line 355 of file `ftm_common.h`.

17.59.4.2 enum `ftm_clock_ps_t`

FlexTimer pre-scaler factor selection for the clock source. In quadrature decoder mode set `FTM_CLOCK_DIVID_BY_1`.

Implements : `ftm_clock_ps_t_Class`

Enumerator

FTM_CLOCK_DIVID_BY_1 Divide by 1

FTM_CLOCK_DIVID_BY_2 Divide by 2

FTM_CLOCK_DIVID_BY_4 Divide by 4

FTM_CLOCK_DIVID_BY_8 Divide by 8

FTM_CLOCK_DIVID_BY_16 Divide by 16

FTM_CLOCK_DIVID_BY_32 Divide by 32

FTM_CLOCK_DIVID_BY_64 Divide by 64

FTM_CLOCK_DIVID_BY_128 Divide by 128

Definition at line 261 of file `ftm_common.h`.

17.59.4.3 enum `ftm_clock_source_t`

FlexTimer clock source selection.

Implements : `ftm_clock_source_t_Class`

Enumerator

FTM_CLOCK_SOURCE_NONE None use clock for FTM

FTM_CLOCK_SOURCE_SYSTEMCLK System clock

FTM_CLOCK_SOURCE_FIXEDCLK Fixed clock

FTM_CLOCK_SOURCE_EXTERNALCLK External clock

Definition at line 247 of file `ftm_common.h`.

17.59.4.4 enum `ftm_config_mode_t`

FlexTimer operation mode.

Implements : `ftm_config_mode_t_Class`

Enumerator

- `FTM_MODE_NOT_INITIALIZED`** The driver is not initialized
- `FTM_MODE_INPUT_CAPTURE`** Input capture
- `FTM_MODE_OUTPUT_COMPARE`** Output compare
- `FTM_MODE_EDGE_ALIGNED_PWM`** Edge aligned PWM
- `FTM_MODE_CEN_ALIGNED_PWM`** Center aligned PWM
- `FTM_MODE_QUADRATURE_DECODER`** Quadrature decoder
- `FTM_MODE_UP_TIMER`** Timer with up counter
- `FTM_MODE_UP_DOWN_TIMER`** timer with up-down counter
- `FTM_MODE_EDGE_ALIGNED_PWM_AND_INPUT_CAPTURE`** Edge aligned PWM and input capture

Definition at line 229 of file `ftm_common.h`.

17.59.4.5 enum `ftm_deadtime_ps_t`

FlexTimer pre-scaler factor for the dead-time insertion.

Implements : `ftm_deadtime_ps_t_Class`

Enumerator

- `FTM_DEADTIME_DIVID_BY_1`** Divide by 1
- `FTM_DEADTIME_DIVID_BY_4`** Divide by 4
- `FTM_DEADTIME_DIVID_BY_16`** Divide by 16

Definition at line 343 of file `ftm_common.h`.

17.59.4.6 enum `ftm_interrupt_option_t`

List of FTM interrupts.

Implements : `ftm_interrupt_option_t_Class`

Enumerator

- `FTM_CHANNEL0_INT_ENABLE`** Channel 0 interrupt
- `FTM_CHANNEL1_INT_ENABLE`** Channel 1 interrupt
- `FTM_CHANNEL2_INT_ENABLE`** Channel 2 interrupt
- `FTM_CHANNEL3_INT_ENABLE`** Channel 3 interrupt
- `FTM_CHANNEL4_INT_ENABLE`** Channel 4 interrupt
- `FTM_CHANNEL5_INT_ENABLE`** Channel 5 interrupt
- `FTM_CHANNEL6_INT_ENABLE`** Channel 6 interrupt
- `FTM_CHANNEL7_INT_ENABLE`** Channel 7 interrupt
- `FTM_FAULT_INT_ENABLE`** Fault interrupt
- `FTM_TIME_OVERFLOW_INT_ENABLE`** Time overflow interrupt
- `FTM_RELOAD_INT_ENABLE`** Reload interrupt; Available only on certain SoC's

Definition at line 278 of file `ftm_common.h`.

17.59.4.7 enum `ftm_pwm_sync_mode_t`

FTM update register.

Implements : `ftm_pwm_sync_mode_t_Class`

Enumerator

FTM_WAIT_LOADING_POINTS FTM register is updated at first loading point

FTM_UPDATE_NOW FTM register is updated immediately

Definition at line 332 of file `ftm_common.h`.

17.59.4.8 enum `ftm_reg_update_t`

FTM sync source.

Implements : `ftm_reg_update_t_Class`

Enumerator

FTM_SYSTEM_CLOCK Register is updated with its buffer value at all rising edges of system clock

FTM_PWM_SYNC Register is updated with its buffer value at the FTM synchronization

Definition at line 319 of file `ftm_common.h`.

17.59.4.9 enum `ftm_status_flag_t`

List of FTM flags.

Implements : `ftm_status_flag_t_Class`

Enumerator

FTM_CHANNEL0_FLAG Channel 0 Flag

FTM_CHANNEL1_FLAG Channel 1 Flag

FTM_CHANNEL2_FLAG Channel 2 Flag

FTM_CHANNEL3_FLAG Channel 3 Flag

FTM_CHANNEL4_FLAG Channel 4 Flag

FTM_CHANNEL5_FLAG Channel 5 Flag

FTM_CHANNEL6_FLAG Channel 6 Flag

FTM_CHANNEL7_FLAG Channel 7 Flag

FTM_FAULT_FLAG Fault Flag

FTM_TIME_OVER_FLOW_FLAG Time overflow Flag

FTM_RELOAD_FLAG Reload Flag; Available only on certain SoC's

FTM_CHANNEL_TRIGGER_FLAG Channel trigger Flag

Definition at line 298 of file `ftm_common.h`.

17.59.5 Function Documentation

17.59.5.1 `static void FTM_DRV_ClearChnEventStatus (FTM_Type *const ftmBase, uint8_t channel)` `[inline]`,
`[static]`

Clears the FTM peripheral timer all channel event status.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number

Implements : FTM_DRV_ClearChnEventStatus_Activity

Definition at line 782 of file ftm_common.h.

17.59.5.2 static void FTM_DRV_ClearChSC (FTM_Type *const *ftmBase*, uint8_t *channel*) [inline],[static]

Clears the content of Channel (n) Status And Control.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number

Implements : FTM_DRV_ClearChSC_Activity

Definition at line 529 of file ftm_common.h.

17.59.5.3 static void FTM_DRV_ClearFaultFlagDetected (FTM_Type *const *ftmBase*, uint8_t *channel*) [inline],[static]

Clear a fault condition is detected at the fault input.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel

Implements : FTM_DRV_ClearFaultFlagDetected_Activity

Definition at line 968 of file ftm_common.h.

17.59.5.4 void FTM_DRV_ClearStatusFlags (uint32_t *instance*, uint32_t *flagMask*)

This function is used to clear the FTM status flags.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>flagMask</i>	The status flags to clear. This is a logical OR of members of the enumeration ftm_status_flag_t

Definition at line 739 of file ftm_common.c.

17.59.5.5 uint16_t FTM_DRV_ConvertFreqToPeriodTicks (uint32_t *instance*, uint32_t *frequencyHz*)

This function is used to covert the given frequency to period in ticks.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>frequencyHz</i>	Frequency value in Hz.

Returns

The value in ticks of the frequency

Definition at line 835 of file ftm_common.c.

17.59.5.6 status_t FTM_DRV_CounterReset (uint32_t *instance*, bool *softwareTrigger*)

This function will allow the FTM to restart the counter to its initial counting value in the register. Note that the configuration is set in the [FTM_DRV_SetSync\(\)](#) function to make sure that the FTM registers are updated by software trigger or hardware trigger.

Parameters

<i>in</i>	<i>instance</i>	The FTM peripheral instance number.
<i>in</i>	<i>softwareTrigger</i>	Selects the software trigger or hardware trigger to update COUNT register. <ul style="list-style-type: none"> • true: A software trigger is generate to update register • false: A software trigger is not implemented and need to update later or select a hardware trigger and waiting an external trigger for updating register.

Definition at line 857 of file ftm_common.c.

17.59.5.7 `status_t FTM_DRV_Deinit (uint32_t instance)`

Shuts down the FTM driver.

Parameters

<i>in</i>	<i>instance</i>	The FTM peripheral instance number.
-----------	-----------------	-------------------------------------

Returns

operation status

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 196 of file ftm_common.c.

17.59.5.8 `static void FTM_DRV_DisableFaultInt (FTM_Type *const ftmBase)` [inline],[static]

Disables the FTM peripheral timer fault interrupt.

Parameters

<i>in</i>	<i>ftmBase</i>	The FTM base address pointer
-----------	----------------	------------------------------

Implements : FTM_DRV_DisableFaultInt_Activity

Definition at line 855 of file ftm_common.h.

17.59.5.9 `void FTM_DRV_DisableInterrupts (uint32_t instance, uint32_t interruptMask)`

This function is used to disable some interrupts.

Parameters

<i>in</i>	<i>instance</i>	The FTM peripheral instance number.
<i>in</i>	<i>interruptMask</i>	The mask of interrupt. This is a logical OR of members of the enumeration ftm_interrupt_option_t

Definition at line 594 of file ftm_common.c.

17.59.5.10 `status_t FTM_DRV_EnableInterrupts (uint32_t instance, uint32_t interruptMask)`

This function will enable the generation a list of interrupts. It includes the FTM overflow interrupts, the reload point interrupt, the fault interrupt and the channel (n) interrupt.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>interruptMask</i>	The mask of interrupt. This is a logical OR of members of the enumeration ftm_interrupt_option_t

Returns

operation status

- STATUS_SUCCESS : Completed successfully.

Definition at line 543 of file ftm_common.c.

17.59.5.11 status_t FTM_DRV_GenerateHardwareTrigger (uint32_t instance)

This function is used to configure a trigger source for FTM instance. This allow a hardware trigger input which can be used in PWM synchronization. Note that the hardware trigger is implemented only on trigger 1 for each instance.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
----	-----------------	-------------------------------------

Returns

operation status

- STATUS_SUCCESS : Completed successfully.

Definition at line 524 of file ftm_common.c.

17.59.5.12 static bool FTM_DRV_GetChInputState (const FTM_Type * ftmBase, uint8_t channel) [inline], [static]

Get the state of channel input.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number

Returns

State of the channel inputs

- true : The channel input is one
- false: The channel input is zero

Implements : FTM_DRV_GetChInputState_Activity

Definition at line 695 of file ftm_common.h.

17.59.5.13 static uint16_t FTM_DRV_GetChnCountVal (const FTM_Type * ftmBase, uint8_t channel) [inline], [static]

Gets the FTM peripheral timer channel counter value.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number

Returns

Channel counter value

Implements : FTM_DRV_GetChnCountVal_Activity

Definition at line 732 of file ftm_common.h.

```
17.59.5.14 static uint8_t FTM_DRV_GetChnEdgeLevel ( const FTM_Type * ftmBase, uint8_t channel ) [inline],
[static]
```

Gets the FTM peripheral timer channel edge level.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number

Returns

The ELSnB:ELSnA mode value, will be 00, 01, 10, 11

Implements : FTM_DRV_GetChnEdgeLevel_Activity

Definition at line 551 of file ftm_common.h.

```
17.59.5.15 static bool FTM_DRV_GetChnEventStatus ( const FTM_Type * ftmBase, uint8_t channel ) [inline],
[static]
```

Gets the FTM peripheral timer channel event status.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number

Returns

Channel event status

- true : A channel event has occurred
- false : No channel event has occurred

Implements : FTM_DRV_GetChnEventStatus_Activity

Definition at line 752 of file ftm_common.h.

```
17.59.5.16 static bool FTM_DRV_GetChOutputValue ( const FTM_Type * ftmBase, uint8_t channel ) [inline],
[static]
```

Get the value of channel output.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number

Returns

Value of the channel outputs

- true : The channel output is one
- false: The channel output is zero

Implements : FTM_DRV_GetChOutputValue_Activity

Definition at line 714 of file ftm_common.h.

```
17.59.5.17 static uint8_t FTM_DRV_GetClockFilterPs ( const FTM_Type * ftmBase ) [inline],[static]
```

Reads the FTM filter clock divider.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
----	----------------	------------------------------

Returns

The FTM filter clock pre-scale divider

Implements : FTM_DRV_GetClockFilterPs_Activity

Definition at line 474 of file ftm_common.h.

17.59.5.18 static uint16_t FTM_DRV_GetCounter (const FTM_Type * *ftmBase*) [inline], [static]

Returns the FTM peripheral current counter value.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
----	----------------	------------------------------

Returns

The current FTM timer counter value

Implements : FTM_DRV_GetCounter_Activity

Definition at line 488 of file ftm_common.h.

17.59.5.19 static uint16_t FTM_DRV_GetCounterInitVal (const FTM_Type * *ftmBase*) [inline], [static]

Returns the FTM peripheral counter initial value.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
----	----------------	------------------------------

Returns

FTM timer counter initial value

Implements : FTM_DRV_GetCounterInitVal_Activity

Definition at line 516 of file ftm_common.h.

17.59.5.20 void FTM_DRV_GetDefaultConfig (ftm_user_config_t *const *config*)

This function will get the default configuration values in the structure which is used as a common use-case.

Parameters

out	<i>config</i>	Pointer to the structure in which the configuration will be saved.
-----	---------------	--

Returns

None

Definition at line 216 of file ftm_common.c.

17.59.5.21 uint32_t FTM_DRV_GetEnabledInterrupts (uint32_t *instance*)

This function will get the enabled FTM interrupts.

Parameters

<i>in</i>	<i>instance</i>	The FTM peripheral instance number.
-----------	-----------------	-------------------------------------

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [ftm_interrupt_option_t](#)

Definition at line 643 of file ftm_common.c.

17.59.5.22 `static uint32_t FTM_DRV_GetEventStatus (const FTM_Type * ftmBase) [inline],[static]`

Gets the FTM peripheral timer status info for all channels.

Parameters

<i>in</i>	<i>ftmBase</i>	The FTM base address pointer
-----------	----------------	------------------------------

Returns

Channel event status value

Implements : FTM_DRV_GetEventStatus_Activity

Definition at line 769 of file ftm_common.h.

17.59.5.23 `uint32_t FTM_DRV_GetFrequency (uint32_t instance)`

Retrieves the frequency of the clock source feeding the FTM counter.

Function will return a 0 if no clock source is selected and the FTM counter is disabled

Parameters

<i>in</i>	<i>instance</i>	The FTM peripheral instance number.
-----------	-----------------	-------------------------------------

Returns

The frequency of the clock source running the FTM counter (0 if counter is disabled)

Definition at line 791 of file ftm_common.c.

17.59.5.24 `static uint16_t FTM_DRV_GetMod (const FTM_Type * ftmBase) [inline],[static]`

Returns the FTM peripheral counter modulo value.

Parameters

<i>in</i>	<i>ftmBase</i>	The FTM base address pointer
-----------	----------------	------------------------------

Returns

FTM timer modulo value

Implements : FTM_DRV_GetMod_Activity

Definition at line 502 of file ftm_common.h.

17.59.5.25 `uint32_t FTM_DRV_GetStatusFlags (uint32_t instance)`

This function will get the FTM status flags. : Regarding the duty cycle is 100% at the channel output, the match interrupt has no event due to the C(n)V and C(n+1)V value are not between CNTIN value and MOD value.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
----	-----------------	-------------------------------------

Returns

The status flags. This is the logical OR of members of the enumeration [ftm_status_flag_t](#)

Definition at line 689 of file `ftm_common.c`.

17.59.5.26 `static bool FTM_DRV_GetTriggerControlled (const FTM_Type * ftmBase, uint8_t channel) [inline], [static]`

Returns whether the trigger mode is enabled.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number

Returns

State of the channel outputs

- true : Enabled a trigger generation on channel output
- false: PWM outputs without generating a pulse

Implements : `FTM_DRV_GetTriggerControlled_Activity`

Definition at line 676 of file `ftm_common.h`.

17.59.5.27 `status_t FTM_DRV_Init (uint32_t instance, const ftm_user_config_t * info, ftm_state_t * state)`

Initializes the FTM driver.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>info</i>	The FTM user configuration structure, see ftm_user_config_t .
out	<i>state</i>	The FTM state structure of the driver.

Returns

operation status

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 114 of file `ftm_common.c`.

17.59.5.28 `static bool FTM_DRV_IsChnDma (const FTM_Type * ftmBase, uint8_t channel) [inline], [static]`

Returns whether the FTM peripheral timer channel DMA is enabled.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number

Returns

State of the FTM peripheral timer channel DMA

- true : Enabled DMA transfers
- false: Disabled DMA transfers

Implements : FTM_DRV_IsChnDma_Activity

Definition at line 636 of file ftm_common.h.

17.59.5.29 static bool FTM_DRV_IsChnIcrst (const FTM_Type * *ftmBase*, uint8_t *channel*) [inline],[static]

Returns whether the FTM FTM counter is reset.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number

Returns

State of the FTM peripheral timer channel ICRST

- true : Enabled the FTM counter reset
- false: Disabled the FTM counter reset

Implements : FTM_DRV_IsChnIcrst_Activity

Definition at line 596 of file ftm_common.h.

17.59.5.30 static bool FTM_DRV_IsFaultFlagDetected (const FTM_Type * *ftmBase*, uint8_t *channel*) [inline],[static]

Checks whether a fault condition is detected at the fault input.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel

Returns

the fault condition status

- true : A fault condition was detected at the fault input
- false: No fault condition was detected at the fault input

Implements : FTM_DRV_IsFaultFlagDetected_Activity

Definition at line 952 of file ftm_common.h.

17.59.5.31 static bool FTM_DRV_IsFaultInputEnabled (const FTM_Type * *ftmBase*) [inline],[static]

Checks whether the logic OR of the fault inputs is enabled.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
----	----------------	------------------------------

Returns

the enabled fault inputs status

- true : The logic OR of the enabled fault inputs is 1

- false: The logic OR of the enabled fault inputs is 0

Implements : FTM_DRV_IsFaultInputEnabled_Activity

Definition at line 935 of file ftm_common.h.

17.59.5.32 static bool FTM_DRV_IsFtmEnable (const FTM_Type * *ftmBase*) [inline],[static]

Get status of the FTMEN bit in the FTM_MODE register.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
----	----------------	------------------------------

Returns

the FTM Enable status

- true : TPM compatibility. Free running counter and synchronization compatible with TPM
- false: Free running counter and synchronization are different from TPM behavior

Implements : FTM_DRV_IsFtmEnable_Activity

Definition at line 886 of file ftm_common.h.

17.59.5.33 static bool FTM_DRV_IsWriteProtectionEnabled (const FTM_Type * *ftmBase*) [inline],[static]

Checks whether the write protection is enabled.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
----	----------------	------------------------------

Returns

Write-protection status

- true : If enabled
- false: If not

Implements : FTM_DRV_IsWriteProtectionEnabled_Activity

Definition at line 919 of file ftm_common.h.

17.59.5.34 status_t FTM_DRV_MaskOutputChannels (uint32_t *instance*, uint32_t *channelsMask*, bool *softwareTrigger*)

This function will mask the output of the channels and at match events will be ignored by the masked channels.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>channelsMask</i>	The mask which will select which channels will ignore match events.
in	<i>softwareTrigger</i>	If true a software trigger is generate to update PWM parameters.

Returns

success

- STATUS_SUCCESS : Completed successfully.

Definition at line 249 of file ftm_common.c.

17.59.5.35 `status_t FTM_DRV_SetAllChnSoftwareOutputControl (uint32_t instance, uint8_t channelMask, uint8_t channelValueMask, bool softwareTrigger)`

This function will control list of channels by software to force the output to specified value. Despite the odd channels are configured as HIGH/LOW, they will be inverted in the following configuration: COMP bit = 1 and CH(n)OCV and CH(n+1)OCV are HIGH. Please check software output control behavior chapter from reference manual. : When the PWM signal is configured with LOW/HIGH polarity on the channel (n). It should be set the safe state as LOW level state. However, We will have an issue with COMP bit is zero and CH(n)OCV is HIGH and CH(n+1)OCV is LOW.in the independent channel configuration. Code configuration: { .polarity = FTM_POLARITY_HIGH, .safeState = FTM_POLARITY_LOW, .enableSecondChannelOutput = true, .secondChannelPolarity = FTM_MAIN_DUPLICATED, }.

Workaround: Configure the safe state as HIGH level state. The expected output will be correctly controlling Should change configuration as following: { .polarity = FTM_POLARITY_HIGH, .safeState = FTM_HIGH_STATE, .enableSecondChannelOutput = true, .secondChannelPolarity = FTM_MAIN_DUPLICATED, }

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>channelMask</i>	The mask which will configure the channels which can be software controlled.
in	<i>channelValueMask</i>	The values which will be software configured for channels.
in	<i>softwareTrigger</i>	If true a software trigger is generate to update registers.

Returns

success

- STATUS_SUCCESS : Completed successfully.

Definition at line 357 of file `ftm_common.c`.

17.59.5.36 `static void FTM_DRV_SetCaptureTestCmd (FTM_Type *const ftmBase, bool enable) [inline], [static]`

Enables or disables the FTM peripheral timer capture test mode.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>enable</i>	Capture Test Mode Enable <ul style="list-style-type: none"> • true : Capture test mode is enabled • false: Capture test mode is disabled

Implements : `FTM_DRV_SetCaptureTestCmd_Activity`

Definition at line 870 of file `ftm_common.h`.

17.59.5.37 `static void FTM_DRV_SetChnDmaCmd (FTM_Type *const ftmBase, uint8_t channel, bool enable) [inline], [static]`

Enables or disables the FTM peripheral timer channel DMA.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number
in	<i>enable</i>	Enable DMA transfers for the channel <ul style="list-style-type: none"> • true : Enabled DMA transfers • false: Disabled DMA transfers

Implements : `FTM_DRV_SetChnDmaCmd_Activity`

Definition at line 615 of file ftm_common.h.

```
17.59.5.38 static void FTM_DRV_SetChnIcrstCmd ( FTM_Type *const ftmBase, uint8_t channel, bool enable ) [inline],
[static]
```

Configure the feature of FTM counter reset by the selected input capture event.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number
in	<i>enable</i>	Enable the FTM counter reset <ul style="list-style-type: none"> • true : FTM counter is reset • false: FTM counter is not reset

Implements : FTM_DRV_SetChnIcrstCmd_Activity

Definition at line 575 of file ftm_common.h.

```
17.59.5.39 static void FTM_DRV_SetChnOutputInitStateCmd ( FTM_Type *const ftmBase, uint8_t channel, bool state )
[inline],[static]
```

Sets the FTM peripheral timer channel output initial state 0 or 1.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number
in	<i>state</i>	Initial state for channels output <ul style="list-style-type: none"> • true : The initialization value is 1 • false: The initialization value is 0

Implements : FTM_DRV_SetChnOutputInitStateCmd_Activity

Definition at line 832 of file ftm_common.h.

```
17.59.5.40 static void FTM_DRV_SetChnOutputMask ( FTM_Type *const ftmBase, uint8_t channel, bool mask )
[inline],[static]
```

Sets the FTM peripheral timer channel output mask.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number
in	<i>mask</i>	Value to set Output Mask <ul style="list-style-type: none"> • true : Channel output is masked • false: Channel output is not masked

Implements : FTM_DRV_SetChnOutputMask_Activity

Definition at line 805 of file ftm_common.h.

```
17.59.5.41 static void FTM_DRV_SetChnSoftwareCtrlCmd ( FTM_Type *const ftmBase, uint8_t channel, bool enable )
[inline],[static]
```

Enables or disables the channel software output control.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	Channel to be enabled or disabled
in	<i>enable</i>	State of channel software output control <ul style="list-style-type: none"> • true : To enable the channel output will be affected by software output control • false: To disable the channel output is unaffected

Implements : FTM_DRV_SetChnSoftwareCtrlCmd_Activity

Definition at line 1018 of file ftm_common.h.

17.59.5.42 static void FTM_DRV_SetChnSoftwareCtrlVal (FTM_Type *const *ftmBase*, uint8_t *channel*, bool *enable*)
[inline], [static]

Sets the channel software output control value. Despite the odd channels are configured as HIGH/LOW, they will be inverted in the following configuration: COMP bit = 1 and CH(n)OCV and CH(n+1)OCV are HIGH. Please check Software output control behavior chapter from RM.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer.
in	<i>channel</i>	Channel to be configured
in	<i>enable</i>	State of software output control value <ul style="list-style-type: none"> • true : to force 1 to the channel output • false: to force 0 to the channel output

Implements : FTM_DRV_SetChnSoftwareCtrlVal_Activity

Definition at line 1048 of file ftm_common.h.

17.59.5.43 static void FTM_DRV_SetClockFilterPs (FTM_Type *const *ftmBase*, uint8_t *filterPrescale*) [inline],
[static]

Sets the filter Pre-scaler divider.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>filterPrescale</i>	The FTM peripheral clock pre-scale divider

Implements : FTM_DRV_SetClockFilterPs_Activity

Definition at line 459 of file ftm_common.h.

17.59.5.44 static void FTM_DRV_SetCountReinitSyncCmd (FTM_Type *const *ftmBase*, bool *enable*) [inline],
[static]

Determines if the FTM counter is re-initialized when the selected trigger for synchronization is detected.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>enable</i>	FTM counter re-initialization selection <ul style="list-style-type: none"> • true : To update FTM counter when triggered • false: To count normally

Implements : FTM_DRV_SetCountReinitSyncCmd_Activity

Definition at line 902 of file `ftm_common.h`.

```
17.59.5.45 static void FTM_DRV_SetDualChnInvertCmd ( FTM_Type *const ftmBase, uint8_t chnlPairNum, bool enable )
           [inline],[static]
```

Enables or disables the channel invert for a channel pair.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>chnlPairNum</i>	The FTM peripheral channel pair number
in	<i>enable</i>	State of channel invert for a channel pair <ul style="list-style-type: none"> • true : To enable channel inverting • false: To disable channel inversion

Implements : `FTM_DRV_SetDualChnInvertCmd_Activity`

Definition at line 991 of file `ftm_common.h`.

```
17.59.5.46 static void FTM_DRV_SetExtPairDeadtimeValue ( FTM_Type *const ftmBase, uint8_t channelPair, uint8_t value )
           [inline],[static]
```

Sets the FTM extended dead-time value for the channel pair.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channelPair</i>	The FTM peripheral channel pair (n)
in	<i>value</i>	The FTM peripheral extend pre-scale divider using the concatenation with the dead-time value

Implements : `FTM_DRV_SetExtPairDeadtimeValue_Activity`

Definition at line 1245 of file `ftm_common.h`.

```
17.59.5.47 static void FTM_DRV_SetGlobalLoadCmd ( FTM_Type *const ftmBase ) [inline],[static]
```

Set the global load mechanism.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
----	----------------	------------------------------

Implements : `FTM_DRV_SetGlobalLoadCmd_Activity`

Definition at line 1072 of file `ftm_common.h`.

```
17.59.5.48 static void FTM_DRV_SetGlobalTimeBaseCmd ( FTM_Type *const ftmBase, bool enable ) [inline],
           [static]
```

Enables or disables the FTM timer global time base.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>enable</i>	State of global time base <ul style="list-style-type: none"> • true : To enable an external global time base signal • false: To disable an external global time base signal

Implements : `FTM_DRV_SetGlobalTimeBaseCmd_Activity`

Definition at line 1216 of file `ftm_common.h`.

17.59.5.49 `static void FTM_DRV_SetGlobalTimeBaseOutputCmd (FTM_Type *const ftmBase, bool enable) [inline],
[static]`

Enables or disables the FTM global time base signal generation to other FTM's.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>enable</i>	State of global time base signal <ul style="list-style-type: none"> • true : To enable the global time base generation to other FTM instances • false: To disable the global time base generation to other FTM instances

Implements : FTM_DRV_SetGlobalTimeBaseOutputCmd_Activity

Definition at line 1200 of file ftm_common.h.

17.59.5.50 static void FTM_DRV_SetHalfCycleCmd (FTM_Type *const *ftmBase*, bool *enable*) [inline],[static]

Enable the half cycle reload.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>enable</i>	State of the half cycle match as a reload opportunity <ul style="list-style-type: none"> • true : Half cycle reload is enabled • false: Half cycle reload is disabled

Implements : FTM_DRV_SetHalfCycleCmd_Activity

Definition at line 1110 of file ftm_common.h.

17.59.5.51 status_t FTM_DRV_SetHalfCycleReloadPoint (uint32_t *instance*, uint16_t *reloadPoint*, bool *softwareTrigger*)

This function configure the value of the counter which will generates an reload point.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>reloadPoint</i>	Counter value which generates the reload point.
in	<i>softwareTrigger</i>	If true a software trigger is generate to update parameters.

Returns

success

- STATUS_SUCCESS : Completed successfully.

Definition at line 291 of file ftm_common.c.

17.59.5.52 status_t FTM_DRV_SetInitialCounterValue (uint32_t *instance*, uint16_t *counterValue*, bool *softwareTrigger*)

This function configure the initial counter value. The counter will get this value after an overflow event.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>counterValue</i>	Initial counter value.
in	<i>softwareTrigger</i>	If true a software trigger is generate to update parameters.

Returns

success

- STATUS_SUCCESS : Completed successfully.

Definition at line 270 of file ftm_common.c.

17.59.5.53 `static void FTM_DRV_SetInitTrigOnReloadCmd (FTM_Type *const ftmBase, bool enable) [inline],
[static]`

Enables or disables the FTM initialization trigger on Reload Point.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>enable</i>	bit controls whether an initialization trigger is generated <ul style="list-style-type: none"> • true : Trigger is generated when a reload point is reached • false: Trigger is generated on counter wrap events

Implements : FTM_DRV_SetInitTrigOnReloadCmd_Activity

Definition at line 1184 of file ftm_common.h.

17.59.5.54 `status_t FTM_DRV_SetInvertingControl (uint32_t instance, uint8_t channelsPairMask, bool softwareTrigger)`

This function will configure if the second channel of a pair will be inverted or not.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>channelsPairMask</i>	The mask which will configure which channel pair will invert the second channel.
in	<i>softwareTrigger</i>	If true a software trigger is generate to update registers.

Returns

success

- STATUS_SUCCESS : Completed successfully.

Definition at line 383 of file ftm_common.c.

17.59.5.55 `static void FTM_DRV_SetLoadCmd (FTM_Type *const ftmBase, bool enable) [inline],[static]`

Enable the global load.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>enable</i>	State of the global load mechanism <ul style="list-style-type: none"> • true : Global Load OK enabled • false: Global Load OK disabled

Implements : FTM_DRV_SetLoadCmd_Activity

Definition at line 1087 of file ftm_common.h.

17.59.5.56 `static void FTM_DRV_SetLoadFreq (FTM_Type *const ftmBase, uint8_t val) [inline],[static]`

Sets the frequency of reload points.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>val</i>	Value of the TOF bit set frequency

Implements : FTM_DRV_SetLoadFreq_Activity

Definition at line 1230 of file ftm_common.h.

17.59.5.57 `status_t FTM_DRV_SetModuloCounterValue (uint32_t instance, uint16_t counterValue, bool softwareTrigger)`

This function configure the maximum counter value.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>counterValue</i>	Maximum counter value
in	<i>softwareTrigger</i>	If true a software trigger is generate to update parameters.

Returns

success

- STATUS_SUCCESS : Completed successfully.

Definition at line 403 of file ftm_common.c.

17.59.5.58 `status_t FTM_DRV_SetOutputlevel (uint32_t instance, uint8_t channel, uint8_t level)`

This function will set the channel edge or level on the selection of the channel mode.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>channel</i>	The channel number.
in	<i>level</i>	The level or edge selection for channel mode.

Returns

success

- STATUS_SUCCESS : Completed successfully.

Definition at line 424 of file ftm_common.c.

17.59.5.59 `static void FTM_DRV_SetPairDeadtimeCount (FTM_Type *const ftmBase, uint8_t channelPair, uint8_t count)`
`[inline], [static]`

Sets the FTM dead-time value for the channel pair.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channelPair</i>	The FTM peripheral channel pair (n)
in	<i>count</i>	The FTM peripheral selects the dead-time value <ul style="list-style-type: none"> • 0U : no counts inserted • 1U : 1 count is inserted • 2U : 2 count is inserted • ... up to a possible 63 counts

Implements : FTM_DRV_SetPairDeadtimeCount_Activity

Definition at line 1323 of file ftm_common.h.

17.59.5.60 `static void FTM_DRV_SetPairDeadtimePrescale (FTM_Type *const ftmBase, uint8_t channelPair,`
`ftm_deadtime_ps_t divider) [inline], [static]`

Sets the FTM dead time divider for the channel pair.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channelPair</i>	The FTM peripheral channel pair (n)
in	<i>divider</i>	The FTM peripheral pre-scaler divider <ul style="list-style-type: none"> • FTM_DEADTIME_DIVID_BY_1 : Divide by 1 • FTM_DEADTIME_DIVID_BY_4 : Divide by 4 • FTM_DEADTIME_DIVID_BY_16: Divide by 16

Implements : FTM_DRV_SetPairDeadtimePrescale_Activity

Definition at line 1284 of file ftm_common.h.

17.59.5.61 static void FTM_DRV_SetPwmLoadChnSelCmd (FTM_Type *const *ftmBase*, uint8_t *channel*, bool *enable*)
[inline],[static]

Includes or excludes the channel in the matching process.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	Channel to be configured
in	<i>enable</i>	State of channel <ul style="list-style-type: none"> • true : means include the channel in the matching process • false: means do not include channel in the matching process

Implements : FTM_DRV_SetPwmLoadChnSelCmd_Activity

Definition at line 1157 of file ftm_common.h.

17.59.5.62 static void FTM_DRV_SetPwmLoadCmd (FTM_Type *const *ftmBase*, bool *enable*) [inline],[static]

Enables or disables the loading of MOD, CNTIN and CV with values of their write buffer.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>enable</i>	State of loading updated values <ul style="list-style-type: none"> • true : To enable the loading of value of their buffer • false: To disable the loading of value of their buffer

Implements : FTM_DRV_SetPwmLoadCmd_Activity

Definition at line 1133 of file ftm_common.h.

17.59.5.63 status_t FTM_DRV_SetSoftOutChnValue (uint32_t *instance*, uint8_t *channelsValues*, bool *softwareTrigger*)

This function will force the output value of a channel to a specific value. Before using this function it's mandatory to mask the match events using FTM_DRV_MaskOutputChannels and to enable software output control using FTM_DRV_SetSoftwareOutputChannelControl. : When the PWM signal is configured with LOW/HIGH polarity on the channel (n). It should be set the safe state as LOW level state. However, We will have an issue with COMP bit is zero and CH(n)OCV is HIGH and CH(n+1)OCV is LOW in the independent channel configuration. Code configuration : { .polarity = FTM_POLARITY_HIGH, .safeState = FTM_POLARITY_LOW, .enableSecondChannelOutput = true, .secondChannelPolarity = FTM_MAIN_DUPLICATED, }.

Workaround: Configure the safe state as HIGH level state. The expected output will be correctly controlling Should change configuration as following: { .polarity = FTM_POLARITY_HIGH, .safeState = FTM_HIGH_STATE, .enableSecondChannelOutput = true, .secondChannelPolarity = FTM_MAIN_DUPLICATED, }

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>channelsValues</i>	The values which will be software configured for channels.
in	<i>softwareTrigger</i>	If true a software trigger is generate to update registers.

Returns

success

- STATUS_SUCCESS : Completed successfully.

Definition at line 314 of file ftm_common.c.

17.59.5.64 `status_t FTM_DRV_SetSoftwareOutputChannelControl (uint32_t instance, uint8_t channelsMask, bool softwareTrigger)`

This function will configure which output channel can be software controlled. Software output control forces the following values on channels (n) and (n+1) when the COMP bit is zero and POL bit is zero. CH(n)OC|CH(n+1)OC|CH(n)OCV|CH(n+1)OCV|Channel (n) Output | Channel (n+1) Output 0 | 0 | X | X | is not modified by SWOC | is not modified by SWOC 1 | 1 | 0 | 0 | is forced to zero | is forced to zero 1 | 1 | 0 | 1 | is forced to zero | is forced to one 1 | 1 | 1 | 0 | is forced to one | is forced to zero 1 | 1 | 1 | 1 | is forced to one | is forced to one.

Software output control forces the following values on channels (n) and (n+1) when the COMP bit is one and POL bit is zero. CH(n)OC|CH(n+1)OC|CH(n)OCV|CH(n+1)OCV|Channel (n) Output | Channel (n+1) Output 0 | 0 | X | X | is not modified by SWOC | is not modified by SWOC 1 | 1 | 0 | 0 | is forced to zero | is forced to zero 1 | 1 | 0 | 1 | is forced to zero | is forced to one 1 | 1 | 1 | 0 | is forced to one | is forced to zero 1 | 1 | 1 | 1 | is forced to one | is forced to zero

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>channelsMask</i>	The mask which will configure the channels which can be software controlled.
in	<i>softwareTrigger</i>	If true a software trigger is generate to update registers.

Returns

success

- STATUS_SUCCESS : Completed successfully.

Definition at line 334 of file ftm_common.c.

17.59.5.65 `status_t FTM_DRV_SetSync (uint32_t instance, const ftm_pwm_sync_t * param)`

This function configures sync mechanism for some FTM registers (MOD, CNINT, HCR, CnV, OUTMASK, INVCTRL, SWOCTRL).

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>param</i>	The sync configuration structure.

Returns

operation status

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 448 of file ftm_common.c.

```
17.59.5.66 static void FTM_DRV_SetTrigModeControlCmd ( FTM_Type *const ftmBase, uint8_t channel, bool enable )  
           [inline],[static]
```

Enables or disables the trigger generation on FTM channel outputs.

Parameters

in	<i>ftmBase</i>	The FTM base address pointer
in	<i>channel</i>	The FTM peripheral channel number
in	<i>enable</i>	Trigger mode control <ul style="list-style-type: none"> • false : Enable PWM output without generating a pulse • true : Disable a trigger generation on channel output

Implements : FTM_DRV_SetTrigModeControlCmd_Activity

Definition at line 655 of file ftm_common.h.

17.59.6 Variable Documentation**17.59.6.1 `ftm_state_t* ftmStatePtr[FTM_INSTANCE_COUNT]`**

Pointer to runtime state structure.

Definition at line 81 of file ftm_common.c.

17.59.6.2 `FTM_Type* const g_ftmBase[FTM_INSTANCE_COUNT]`

Table of base addresses for FTM instances.

Definition at line 68 of file ftm_common.c.

17.59.6.3 `const IRQn_Type g_ftmFaultIrqlId[FTM_INSTANCE_COUNT]`

Definition at line 72 of file ftm_common.c.

17.59.6.4 `const IRQn_Type g_ftmIrqlId[FTM_INSTANCE_COUNT][FEATURE_FTM_CHANNEL_COUNT]`

Interrupt vectors for the FTM peripheral.

Definition at line 71 of file ftm_common.c.

17.59.6.5 `const IRQn_Type g_ftmOverflowIrqlId[FTM_INSTANCE_COUNT]`

Definition at line 73 of file ftm_common.c.

17.59.6.6 `const IRQn_Type g_ftmReloadIrqlId[FTM_INSTANCE_COUNT]`

Definition at line 74 of file ftm_common.c.

17.60 FlexTimer Input Capture Driver (FTM_IC)

17.60.1 Detailed Description

FlexTimer Input Capture Peripheral Driver.

Hardware background

The FTM of the S32K1xx is based on a 16 bits counter and supports: input capture, output compare, PWM and some instances include quadrature decoder.

How to use FTM driver in your application

For all operation modes (without Quadrature Decoder mode) the user need to configure [ftm_user_config_t](#). This structure will be used for initialization (FTM_DRV_Init). The next functions used are specific for each operation mode.

Single edge input capture mode

For this mode the user needs to configure parameters such: maximum counter value, number of channels, input capture operation mode (for single edge input are used edge detect mode) and edge alignment. All this information is included in the [ftm_input_param_t](#) structure.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_ic_driver.c
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_common.c
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\drivers\inc\
{S32SDK_PATH}\platform\drivers\src\ftm\
```

Compile symbols

No special symbols are required for this component

Dependencies

Clock Manager Interrupt Manager (Interrupt)

Example:

```
/* The state structure of instance in the input capture mode */
ftm_state_t stateInputCapture;
#define FTM_IC_INSTANCE OUL
/* Channels configuration structure for inputCapture input capture */
ftm_input_ch_param_t inputCapture_InputCaptureChannelConfig[1] =
{
    {
        OU, /* Channel Id */
        FTM_EDGE_DETECT, /* Input capture operation Mode */
        FTM_RISING_EDGE, /* Edge alignment Mode */
        FTM_NO_MEASUREMENT, /* Signal measurement operation type */
        OU, /* Filter value */
        false, /* Filter disabled */
        true, /* Continuous mode measurement */
        NULL, /* Vector of callbacks parameters for channels events */
        NULL /* Vector of callbacks for channels events */
    }
}
```

```

};
/* Input capture configuration for inputCapture */
ftm_input_param_t inputCapture_InitConfig =
{
    1U,                                     /* Number of channels */
    65535U,                                /* Maximum count value */
    inputCapture_InitConfigChannelConfig /* Channels configuration */
};
/* Timer mode configuration for inputCapture */
/* Global configuration of inputCapture */
ftm_user_config_t inputCapture_InitConfig =
{
    {
        false,                             /* Software trigger state */
        false,                             /* Hardware trigger 1 state */
        false,                             /* Hardware trigger 2 state */
        false,                             /* Hardware trigger 3 state */
        false,                             /* Maximum loading point state */
        false,                             /* Min loading point state */
        FTM_SYSTEM_CLOCK,                  /* Update mode for INVCTRL register */
        FTM_SYSTEM_CLOCK,                  /* Update mode for SWOCTRL register */
        FTM_SYSTEM_CLOCK,                  /* Update mode for OUTMASK register */
        FTM_SYSTEM_CLOCK,                  /* Update mode for CNTIN register */
        false,                             /* Auto clear trigger state for hardware trigger */
        FTM_UPDATE_NOW,                    /* Select synchronization method */
    },
    FTM_MODE_INPUT_CAPTURE,                /* Mode of operation for FTM */
    FTM_CLOCK_DIVID_BY_4,                  /* FTM clock pre-scaler */
    FTM_CLOCK_SOURCE_SYSTEMCLK,            /* FTM clock source */
    FTM_BDM_MODE_00,                      /* FTM debug mode */
    false,                                 /* Interrupt state */
    false                                  /* Initialization trigger */
};
FTM_DRV_Init(FTM_IC_INSTANCE, &inputCapture_InitConfig, &stateInputCapture);
FTM_DRV_InitInputCapture(FTM_IC_INSTANCE, &inputCapture_InitConfig);
counter = FTM_DRV_GetInputCaptureMeasurement(FTM_IC_INSTANCE, 0U);

```

FTM_DRV_GetInputCaptureMeasurement is now used in interrupt mode and this function is used to save time stamps in internal buffers.

Edge-Aligned PWM and Input Capture mode

- Support both Edge-Aligned PWM and Input Capture mode can work over the same FTM instance.
- The guideline can be found here [FlexTimer Pulse Width Modulation Driver \(FTM_PWM\)](#)

Data Structures

- struct [ftm_input_ch_param_t](#)
FlexTimer driver Input capture parameters for each channel. [More...](#)
- struct [ftm_input_param_t](#)
FlexTimer driver input capture parameters. [More...](#)

Enumerations

- enum [ftm_input_op_mode_t](#) { [FTM_EDGE_DETECT](#) = 0U, [FTM_SIGNAL_MEASUREMENT](#) = 1U, [FTM_NO_OPERATION](#) = 2U }
Selects mode operation in the input capture.
- enum [ftm_signal_measurement_mode_t](#) { [FTM_NO_MEASUREMENT](#) = 0x00U, [FTM_RISING_EDGE_PERIOD_MEASUREMENT](#) = 0x01U, [FTM_FALLING_EDGE_PERIOD_MEASUREMENT](#) = 0x02U, [FTM_PERIOD_ON_MEASUREMENT](#) = 0x03U, [FTM_PERIOD_OFF_MEASUREMENT](#) = 0x04U }
FlexTimer input capture measurement type for dual edge input capture.
- enum [ftm_edge_alignment_mode_t](#) { [FTM_NO_PIN_CONTROL](#) = 0x00U, [FTM_RISING_EDGE](#) = 0x01U, [FTM_FALLING_EDGE](#) = 0x02U, [FTM_BOTH_EDGES](#) = 0x03U }
FlexTimer input capture edge mode as rising edge or falling edge.

- enum `ftm_ic_op_mode_t` {
`FTM_DISABLE_OPERATION` = 0x00U, `FTM_TIMESTAMP_RISING_EDGE` = 0x01U, `FTM_TIMESTAMP_FALLING_EDGE` = 0x02U, `FTM_TIMESTAMP_BOTH_EDGES` = 0x03U,
`FTM_MEASURE_RISING_EDGE_PERIOD` = 0x04U, `FTM_MEASURE_FALLING_EDGE_PERIOD` = 0x05U, `FTM_MEASURE_PULSE_HIGH` = 0x06U, `FTM_MEASURE_PULSE_LOW` = 0x07U }

The measurement type for input capture mode Implements : `ftm_ic_op_mode_t_Class`.

Functions

- status_t `FTM_DRV_InitInputCapture` (uint32_t instance, const `ftm_input_param_t` *param)
This function configures the channel in the Input Capture mode for either getting time-stamps on edge detection or on signal measurement. When the edge specified in the captureMode argument occurs on the channel and then the FTM counter is captured into the CnV register. The user have to read the CnV register separately to get this value. The filter function is disabled if the filterVal argument passed as 0. The filter feature. is available only on channels 0,1,2,3.
- status_t `FTM_DRV_DeinitInputCapture` (uint32_t instance, const `ftm_input_param_t` *param)
Disables input capture mode and clears FTM timer configuration.
- uint16_t `FTM_DRV_GetInputCaptureMeasurement` (uint32_t instance, uint8_t channel)
This function is used to calculate the measurement and/or time stamps values which are read from the C(n, n+1)V registers and stored to the static buffers.
- status_t `FTM_DRV_StartNewSignalMeasurement` (uint32_t instance, uint8_t channel)
Starts new single-shot signal measurement of the given channel.
- status_t `FTM_IC_DRV_SetChannelMode` (uint32_t instance, uint8_t channel, `ftm_ic_op_mode_t` inputMode, bool enableContinuousCapture)
Set mode operation for channel in the input capture mode.

17.60.2 Data Structure Documentation

17.60.2.1 struct `ftm_input_ch_param_t`

FlexTimer driver Input capture parameters for each channel.

Implements : `ftm_input_ch_param_t_Class`

Definition at line 96 of file `ftm_ic_driver.h`.

Data Fields

- uint8_t `hwChannelId`
- `ftm_input_op_mode_t` `inputMode`
- `ftm_edge_alignment_mode_t` `edgeAlignement`
- `ftm_signal_measurement_mode_t` `measurementType`
- uint16_t `filterValue`
- bool `filterEn`
- bool `continuousModeEn`
- void * `channelsCallbacksParams`
- `ic_callback_t` `channelsCallbacks`

Field Documentation

17.60.2.1.1 `ic_callback_t` `channelsCallbacks`

The callback function for channels events

Definition at line 106 of file `ftm_ic_driver.h`.

17.60.2.1.2 void* channelsCallbacksParams

The parameters of callback functions for channels events

Definition at line 105 of file ftm_ic_driver.h.

17.60.2.1.3 bool continuousModeEn

Continuous measurement state

Definition at line 104 of file ftm_ic_driver.h.

17.60.2.1.4 ftm_edge_alignment_mode_t edgeAlignement

Edge alignment Mode for signal measurement

Definition at line 100 of file ftm_ic_driver.h.

17.60.2.1.5 bool filterEn

Input capture filter state

Definition at line 103 of file ftm_ic_driver.h.

17.60.2.1.6 uint16_t filterValue

Filter Value

Definition at line 102 of file ftm_ic_driver.h.

17.60.2.1.7 uint8_t hwChannelId

Physical hardware channel ID

Definition at line 98 of file ftm_ic_driver.h.

17.60.2.1.8 ftm_input_op_mode_t inputMode

FlexTimer module mode of operation

Definition at line 99 of file ftm_ic_driver.h.

17.60.2.1.9 ftm_signal_measurement_mode_t measurementType

Measurement Mode for signal measurement

Definition at line 101 of file ftm_ic_driver.h.

17.60.2.2 struct ftm_input_param_t

FlexTimer driver input capture parameters.

Implements : ftm_input_param_t_Class

Definition at line 114 of file ftm_ic_driver.h.

Data Fields

- uint8_t [nNumChannels](#)
- uint16_t [nMaxCountValue](#)
- [ftm_input_ch_param_t](#) * [inputChConfig](#)

Field Documentation

17.60.2.2.1 ftm_input_ch_param_t* inputChConfig

Input capture channels configuration

Definition at line 118 of file ftm_ic_driver.h.

17.60.2.2.2 uint16_t nMaxCountValue

Maximum counter value. Minimum value is 0 for this mode

Definition at line 117 of file ftm_ic_driver.h.

17.60.2.2.3 uint8_t nNumChannels

Number of input capture channel used

Definition at line 116 of file ftm_ic_driver.h.

17.60.3 Enumeration Type Documentation

17.60.3.1 enum ftm_edge_alignment_mode_t

FlexTimer input capture edge mode as rising edge or falling edge.

Implements : ftm_edge_alignment_mode_t_Class

Enumerator

FTM_NO_PIN_CONTROL No trigger
FTM_RISING_EDGE Rising edge trigger
FTM_FALLING_EDGE Falling edge trigger
FTM_BOTH_EDGES Rising and falling edge trigger

Definition at line 67 of file ftm_ic_driver.h.

17.60.3.2 enum ftm_ic_op_mode_t

The measurement type for input capture mode Implements : ftm_ic_op_mode_t_Class.

Enumerator

FTM_DISABLE_OPERATION Have no operation
FTM_TIMESTAMP_RISING_EDGE Rising edge trigger
FTM_TIMESTAMP_FALLING_EDGE Falling edge trigger
FTM_TIMESTAMP_BOTH_EDGES Rising and falling edge trigger
FTM_MEASURE_RISING_EDGE_PERIOD Period measurement between two consecutive rising edges
FTM_MEASURE_FALLING_EDGE_PERIOD Period measurement between two consecutive falling edges
FTM_MEASURE_PULSE_HIGH The time measurement taken for the pulse to remain ON or HIGH state
FTM_MEASURE_PULSE_LOW The time measurement taken for the pulse to remain OFF or LOW state

Definition at line 79 of file ftm_ic_driver.h.

17.60.3.3 enum ftm_input_op_mode_t

Selects mode operation in the input capture.

Implements : ftm_input_op_mode_t_Class

Enumerator

FTM_EDGE_DETECT FTM edge detect
FTM_SIGNAL_MEASUREMENT FTM signal measurement
FTM_NO_OPERATION FTM no operation

Definition at line 41 of file ftm_ic_driver.h.

17.60.3.4 enum `ftm_signal_measurement_mode_t`

FlexTimer input capture measurement type for dual edge input capture.

Implements : `ftm_signal_measurement_mode_t_Class`

Enumerator

`FTM_NO_MEASUREMENT` No measurement

`FTM_RISING_EDGE_PERIOD_MEASUREMENT` Period measurement between two consecutive rising edges

`FTM_FALLING_EDGE_PERIOD_MEASUREMENT` Period measurement between two consecutive falling edges

`FTM_PERIOD_ON_MEASUREMENT` The time measurement taken for the pulse to remain ON or HIGH state

`FTM_PERIOD_OFF_MEASUREMENT` The time measurement taken for the pulse to remain OFF or LOW state

Definition at line 53 of file `ftm_ic_driver.h`.

17.60.4 Function Documentation

17.60.4.1 `status_t FTM_DRV_DeinitInputCapture (uint32_t instance, const ftm_input_param_t * param)`

Disables input capture mode and clears FTM timer configuration.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>param</i>	Configuration of the output compare channel.

Returns

success

- `STATUS_SUCCESS` : Completed successfully.
- `STATUS_ERROR` : Error occurred.

Definition at line 333 of file `ftm_ic_driver.c`.

17.60.4.2 `uint16_t FTM_DRV_GetInputCaptureMeasurement (uint32_t instance, uint8_t channel)`

This function is used to calculate the measurement and/or time stamps values which are read from the C(n, n+1)V registers and stored to the static buffers.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>channel</i>	For getting the time stamp of the last edge (in normal input capture) this parameter represents the channel number. For getting the last measured value (in dual edge input capture) this parameter is the lowest channel number of the pair (EX: 0, 2, 4, 6).

Returns

value The measured value

Definition at line 403 of file `ftm_ic_driver.c`.

17.60.4.3 status_t FTM_DRV_InitInputCapture (uint32_t instance, const ftm_input_param_t * param)

This function configures the channel in the Input Capture mode for either getting time-stamps on edge detection or on signal measurement. When the edge specified in the captureMode argument occurs on the channel and then the FTM counter is captured into the CnV register. The user have to read the CnV register separately to get this value. The filter function is disabled if the filterVal argument passed as 0. The filter feature. is available only on channels 0,1,2,3.

Parameters

in	instance	The FTM peripheral instance number.
in	param	Configuration of the input capture channel.

Returns

success

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 215 of file ftm_ic_driver.c.

17.60.4.4 status_t FTM_DRV_StartNewSignalMeasurement (uint32_t instance, uint8_t channel)

Starts new single-shot signal measurement of the given channel.

Parameters

in	instance	The FTM peripheral instance number.
in	channel	Configuration of the output compare channel.

Returns

success

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 427 of file ftm_ic_driver.c.

17.60.4.5 status_t FTM_IC_DRV_SetChannelMode (uint32_t instance, uint8_t channel, ftm_ic_op_mode_t inputMode, bool enableContinuousCapture)

Set mode operation for channel in the input capture mode.

This function will change the channel mode at run time or when stopping channel. The channel mode is selected in the ftm_ic_op_mode_t enumeration type.

Parameters

in	instance	The input capture instance number.
in	channel	The channel number.
in	inputMode	The channel operation mode.
in	enable↔ Continuous↔ Capture	Enable/disable the continuous capture mode.

Returns

success

- STATUS_SUCCESS : Completed successfully.

Definition at line 466 of file ftm_ic_driver.c.

17.61 FlexTimer Module Counter Driver (FTM_MC)

17.61.1 Detailed Description

FlexTimer Module Counter Peripheral Driver.

Hardware background

The FTM of the S32K1xx is based on a 16 bits counter and supports: input capture, output compare, PWM and some instances include quadrature decoder.

How to use FTM driver in your application

For all operation modes (without Quadrature Decoder mode) the user need to configure [ftm_user_config_t](#). This structure will be used for initialization (FTM_DRV_Init). The next functions used are specific for each operation mode.

Counter mode

For this mode the user needs to configure parameters like: counter mode (up-counting or up-down counting), maximum counter value, initial counter value. All this information is included in the [ftm_timer_param_t](#) structure.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_mc_driver.c
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_common.c
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\drivers\inc\
{S32SDK_PATH}\platform\drivers\src\ftm\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager Interrupt Manager \(Interrupt\)](#)

Example:

```
/* The state structure of instance in the input capture mode */
ftm_state_t stateTimer;
#define FTM_TIMER_INSTANCE 1UL
/* Timer mode configuration for Timer */
ftm_timer_param_t Timer_TimerConfig =
{
    FTM_MODE_UP_TIMER,          /* Counter mode */
    0U,                         /* Initial counter value */
    0x8000U                     /* Final counter value */
};

/* Global configuration of Timer*/
ftm_user_config_t Timer_InitConfig =
{
    {
        false,                 /* Software trigger state */
        false,                 /* Hardware trigger 1 state */
        false,                 /* Hardware trigger 2 state */
        false,                 /* Hardware trigger 3 state */
    }
}
```

```

        false,                /* Maximum loading point state */
        false,                /* Min loading point state */
        FTM_SYSTEM_CLOCK,    /* Update mode for INVCTRL register */
        FTM_SYSTEM_CLOCK,    /* Update mode for SWOCTRL register */
        FTM_SYSTEM_CLOCK,    /* Update mode for OUTMASK register */
        FTM_SYSTEM_CLOCK,    /* Update mode for CNTIN register */
        false,                /* Auto clear trigger state for hardware trigger */
        FTM_UPDATE_NOW,      /* Select synchronization method */
    },
    FTM_MODE_UP_TIMER,        /* Mode of operation for FTM */
    FTM_CLOCK_DIVID_BY_2,     /* FTM clock pre-scaler */
    FTM_CLOCK_SOURCE_SYSTEMCLK, /* FTM clock source */
    FTM_BDM_MODE_11,         /* FTM debug mode */
    false,                    /* Interrupt state */
    false,                    /* Initialization trigger */
};
FTM_DRV_Init(FTM_TIMER_INSTANCE, &Timer_InitConfig, &stateTimer);
FTM_DRV_InitCounter(FTM_TIMER_INSTANCE, &Timer_TimerConfig);
FTM_DRV_CounterStart(FTM_TIMER_INSTANCE);

```

Data Structures

- struct [ftm_timer_param_t](#)

The configuration structure in timer mode. [More...](#)

Functions

- status_t [FTM_DRV_InitCounter](#) (uint32_t instance, const [ftm_timer_param_t](#) *timer)

Initialize the FTM counter.

- status_t [FTM_DRV_CounterStart](#) (uint32_t instance)

Starts the FTM counter.

- status_t [FTM_DRV_CounterStop](#) (uint32_t instance)

Stops the FTM counter.

- uint32_t [FTM_DRV_CounterRead](#) (uint32_t instance)

Reads back the current value of the FTM counter.

- void [FTM_MC_DRV_GetDefaultConfig](#) ([ftm_timer_param_t](#) *const config)

This function will get the default configuration values in the structure which is used as a common use-case.

17.61.2 Data Structure Documentation

17.61.2.1 struct [ftm_timer_param_t](#)

The configuration structure in timer mode.

Implements : [ftm_timer_param_t_Class](#)

Definition at line 41 of file [ftm_mc_driver.h](#).

Data Fields

- [ftm_config_mode_t](#) mode
- uint16_t initialValue
- uint16_t finalValue

Field Documentation

17.61.2.1.1 uint16_t finalValue

Final counter value

Definition at line 45 of file [ftm_mc_driver.h](#).

17.61.2.1.2 uint16_t initialValue

Initial counter value

Definition at line 44 of file ftm_mc_driver.h.

17.61.2.1.3 ftm_config_mode_t mode

FTM mode

Definition at line 43 of file ftm_mc_driver.h.

17.61.3 Function Documentation

17.61.3.1 uint32_t FTM_DRV_CounterRead (uint32_t *instance*)

Reads back the current value of the FTM counter.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
----	-----------------	-------------------------------------

Returns

The current counter value

Definition at line 150 of file ftm_mc_driver.c.

17.61.3.2 status_t FTM_DRV_CounterStart (uint32_t *instance*)

Starts the FTM counter.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
----	-----------------	-------------------------------------

Returns

operation status

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 111 of file ftm_mc_driver.c.

17.61.3.3 status_t FTM_DRV_CounterStop (uint32_t *instance*)

Stops the FTM counter.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
----	-----------------	-------------------------------------

Returns

operation status

- STATUS_SUCCESS : Completed successfully.

Definition at line 132 of file ftm_mc_driver.c.

17.61.3.4 `status_t FTM_DRV_InitCounter (uint32_t instance, const ftm_timer_param_t * timer)`

Initialize the FTM counter.

Starts the FTM counter. This function provides access to the FTM counter settings. The counter can be run in Up counting and Up-down counting modes. To run the counter in Free running mode, choose Up counting option and provide 0x0 value for the initialValue and 0xFFFF for finalValue. Please call this function only when FTM is used as timer/counter. User must call the FTM_DRV_Deinit and the FTM_DRV_Init to Re-Initialize the FTM before calling FTM_DRV_InitCounter for the second time and afterwards.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>timer</i>	Timer configuration structure.

Returns

operation status

- STATUS_SUCCESS : Initialized successfully.

Definition at line 52 of file ftm_mc_driver.c.

17.61.3.5 `void FTM_MC_DRV_GetDefaultConfig (ftm_timer_param_t *const config)`

This function will get the default configuration values in the structure which is used as a common use-case.

Parameters

out	<i>config</i>	Pointer to the structure in which the configuration will be saved.
-----	---------------	--

Returns

None

Definition at line 166 of file ftm_mc_driver.c.

17.62 FlexTimer Output Compare Driver (FTM_OC)

17.62.1 Detailed Description

FlexTimer Output Compare Peripheral Driver.

Hardware background

The FTM of the S32K1xx is based on a 16 bits counter and supports: input capture, output compare, PWM and some instances include quadrature decoder.

How to use FTM driver in your application

For all operation modes (without Quadrature Decoder mode) the user need to configure [ftm_user_config_t](#). This structure will be used for initialization (FTM_DRV_Init). The next functions used are specific for each operation mode.

Output compare mode

For this mode the user needs to configure maximum counter value, number of channels used and output mode for each channel (toggle/clear/set on match). This information is stored in [ftm_output_cmp_param_t](#) structure type and are used in FTM_DRV_InitOutputCompare function. Next step is to set a value for comparison with the FTM_DRV_UpdateOutputCompareChannel function.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_oc_driver.c
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_common.c
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\drivers\inc\
{S32SDK_PATH}\platform\drivers\src\ftm\
```

Compile symbols

No special symbols are required for this component

Dependencies

Clock Manager Interrupt Manager (Interrupt)

Example:

```
/* The state structure of instance in the output compare mode */
ftm_state_t stateOutputCompare;
#define FTM_OUTPUT_COMPARE_INSTANCE 1UL
/* Channels configuration structure for PWM output compare */
ftm_output_cmp_ch_param_t PWM_OutputCompareChannelConfig[2] =
{
    {
        0U, /* Channel id */
        FTM_TOGGLE_ON_MATCH, /* Output mode */
        10000U, /* Compared value */
        false, /* External Trigger */
    },
    {
        1U, /* Channel id */
        FTM_TOGGLE_ON_MATCH, /* Output mode */
        20000U, /* Compared value */
    }
}
```

```

        false,                /* External Trigger */
    }
};

/* Output compare configuration for PWM */
ftm_output_cmp_param_t PWM_OutputCompareConfig =
{
    2U,                        /* Number of channels */
    FTM_MODE_OUTPUT_COMPARE,   /* FTM mode */
    40000U,                    /* Maximum count value */
    PWM_OutputCompareChannelConfig /* Channels configuration */
};

/* Timer mode configuration for PWM */
/* Global configuration of PWM */
ftm_user_config_t PWM_InitConfig =
{
    {
        true,                  /* Software trigger state */
        false,                 /* Hardware trigger 1 state */
        false,                 /* Hardware trigger 2 state */
        false,                 /* Hardware trigger 3 state */
        true,                  /* Maximum loading point state */
        true,                  /* Min loading point state */
        FTM_SYSTEM_CLOCK,      /* Update mode for INVCTRL register */
        FTM_SYSTEM_CLOCK,      /* Update mode for SWOCTRL register */
        FTM_SYSTEM_CLOCK,      /* Update mode for OUTMASK register */
        FTM_SYSTEM_CLOCK,      /* Update mode for CNTIN register */
        false,                 /* Auto clear trigger state for hardware trigger */
        FTM_UPDATE_NOW,        /* select synchronization method */
    },
    FTM_MODE_OUTPUT_COMPARE,    /* Mode of operation for FTM */
    FTM_CLOCK_DIVID_BY_4,       /* FTM clock pre-scaler */
    FTM_CLOCK_SOURCE_SYSTEMCLK, /* FTM clock source */
    FTM_BDM_MODE_11,           /* FTM debug mode */
    false,                     /* Interrupt state */
    false,                     /* Initialization trigger */
};

FTM_DRV_Init(FTM_OUTPUT_COMPARE_INSTANCE, &PWM_InitConfig, &stateOutputCompare);
FTM_DRV_InitOutputCompare(FTM_OUTPUT_COMPARE_INSTANCE, &PWM_OutputCompareConfig);
/* If you want to change compared value */
FTM_DRV_UpdateOutputCompareChannel(FTM_OUTPUT_COMPARE_INSTANCE, 0UL, 1500
0U );

```

Data Structures

- struct `ftm_output_cmp_ch_param_t`
FlexTimer driver PWM parameters each channel in the output compare mode. [More...](#)
- struct `ftm_output_cmp_param_t`
FlexTimer driver PWM parameters which is configured for the list of channels. [More...](#)

Enumerations

- enum `ftm_output_compare_mode_t` { `FTM_DISABLE_OUTPUT` = 0x00U, `FTM_TOGGLE_ON_MATCH` = 0x01U, `FTM_CLEAR_ON_MATCH` = 0x02U, `FTM_SET_ON_MATCH` = 0x03U }
FlexTimer Mode configuration for output compare mode.
- enum `ftm_output_compare_update_t` { `FTM_RELATIVE_VALUE` = 0x00U, `FTM_ABSOLUTE_VALUE` = 0x01U }
FlexTimer input capture type of the next output compare value.

Functions

- status_t `FTM_DRV_InitOutputCompare` (uint32_t instance, const `ftm_output_cmp_param_t` *param)
Configures the FTM to generate timed pulses (Output compare mode).
- status_t `FTM_DRV_DeinitOutputCompare` (uint32_t instance, const `ftm_output_cmp_param_t` *param)
Disables compare match output control and clears FTM timer configuration.
- status_t `FTM_DRV_UpdateOutputCompareChannel` (uint32_t instance, uint8_t channel, uint16_t next←ComparematchValue, `ftm_output_compare_update_t` update, bool softwareTrigger)
Sets the next compare match value based on the current counter value.

17.62.2 Data Structure Documentation

17.62.2.1 struct ftm_output_cmp_ch_param_t

FlexTimer driver PWM parameters each channel in the output compare mode.

Implements : ftm_output_cmp_ch_param_t_Class

Definition at line 65 of file ftm_oc_driver.h.

Data Fields

- uint8_t [hwChannelId](#)
- [ftm_output_compare_mode_t](#) chMode
- uint16_t [comparedValue](#)
- bool [enableExternalTrigger](#)

Field Documentation

17.62.2.1.1 ftm_output_compare_mode_t chMode

Channel output mode

Definition at line 68 of file ftm_oc_driver.h.

17.62.2.1.2 uint16_t comparedValue

The compared value

Definition at line 69 of file ftm_oc_driver.h.

17.62.2.1.3 bool enableExternalTrigger

true: enable the generation of a trigger is used for on-chip modules false: disable the generation of a trigger

Definition at line 70 of file ftm_oc_driver.h.

17.62.2.1.4 uint8_t hwChannelId

Physical hardware channel ID

Definition at line 67 of file ftm_oc_driver.h.

17.62.2.2 struct ftm_output_cmp_param_t

FlexTimer driver PWM parameters which is configured for the list of channels.

Implements : ftm_output_cmp_param_t_Class

Definition at line 79 of file ftm_oc_driver.h.

Data Fields

- uint8_t [nNumOutputChannels](#)
- [ftm_config_mode_t](#) mode
- uint16_t [maxCountValue](#)
- [ftm_output_cmp_ch_param_t](#) * [outputChannelConfig](#)

Field Documentation

17.62.2.2.1 uint16_t maxCountValue

Maximum count value in ticks

Definition at line 83 of file ftm_oc_driver.h.

17.62.2.2.2 `ftm_config_mode_t` mode

FlexTimer PWM operation mode

Definition at line 82 of file `ftm_oc_driver.h`.

17.62.2.2.3 `uint8_t` `nNumOutputChannels`

Number of output compare channels

Definition at line 81 of file `ftm_oc_driver.h`.

17.62.2.2.4 `ftm_output_cmp_ch_param_t*` `outputChannelConfig`

Output compare channels configuration

Definition at line 84 of file `ftm_oc_driver.h`.

17.62.3 Enumeration Type Documentation

17.62.3.1 `enum` `ftm_output_compare_mode_t`

FlexTimer Mode configuration for output compare mode.

Implements : `ftm_output_compare_mode_t_Class`

Enumerator

FTM_DISABLE_OUTPUT No action on output pin

FTM_TOGGLE_ON_MATCH Toggle on match

FTM_CLEAR_ON_MATCH Clear on match

FTM_SET_ON_MATCH Set on match

Definition at line 41 of file `ftm_oc_driver.h`.

17.62.3.2 `enum` `ftm_output_compare_update_t`

FlexTimer input capture type of the next output compare value.

Implements : `ftm_output_compare_update_t_Class`

Enumerator

FTM_RELATIVE_VALUE Next compared value is relative to current value

FTM_ABSOLUTE_VALUE Next compared value is absolute

Definition at line 54 of file `ftm_oc_driver.h`.

17.62.4 Function Documentation

17.62.4.1 `status_t` `FTM_DRV_DeinitOutputCompare` (`uint32_t` *instance*, `const` `ftm_output_cmp_param_t*` *param*)

Disables compare match output control and clears FTM timer configuration.

Parameters

<code>in</code>	<i>instance</i>	The FTM peripheral instance number.
-----------------	-----------------	-------------------------------------

<i>in</i>	<i>param</i>	Configuration of the output compare channel
-----------	--------------	---

Returns**success**

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 107 of file ftm_oc_driver.c.

17.62.4.2 `status_t FTM_DRV_InitOutputCompare (uint32_t instance, const ftm_output_cmp_param_t * param)`

Configures the FTM to generate timed pulses (Output compare mode).

When the FTM counter matches the value of CnV, the channel output is changed based on what is specified in the mode argument. The signal period can be modified using param->maxCountValue. After this function when the max counter value and CnV are equal. FTM_DRV_UpdateOutputCompareChannel function can be used to change CnV value.

Parameters

<i>in</i>	<i>instance</i>	The FTM peripheral instance number.
<i>in</i>	<i>param</i>	configuration of the output compare channels

Returns**success**

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 42 of file ftm_oc_driver.c.

17.62.4.3 `status_t FTM_DRV_UpdateOutputCompareChannel (uint32_t instance, uint8_t channel, uint16_t nextComparematchValue, ftm_output_compare_update_t update, bool softwareTrigger)`

Sets the next compare match value based on the current counter value.

Parameters

<i>in</i>	<i>instance</i>	The FTM peripheral instance number.
<i>in</i>	<i>channel</i>	Configuration of the output compare channel
<i>in</i>	<i>nextComparematchValue</i>	Timer value in ticks until the next compare match event should appear
<i>in</i>	<i>update</i>	<ul style="list-style-type: none"> • FTM_RELATIVE_VALUE : nextComparematchValue will be added to current counter value • FTM_ABSOLUTE_VALUE : nextComparematchValue will be written in counter register as it is

in	<i>softwareTrigger</i>	This parameter will be true if software trigger sync is enabled and the user want to generate a software trigger (the value from buffer will be moved to register immediate or at next loading point depending on the sync configuration). Otherwise this parameter must be false and the next compared value will be stored in buffer until a trigger signal will be received.
----	------------------------	---

Returns

success

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 150 of file ftm_oc_driver.c.

17.63 FlexTimer Pulse Width Modulation Driver (FTM_PWM)

17.63.1 Detailed Description

FlexTimer Pulse Width Modulation Peripheral Driver.

Hardware background

The FlexTimer module is based on a 16 bits counter and supports: input capture, output compare, PWM and some instances include quadrature decoder.

How to use FTM driver in your application

For all operation modes (without Quadrature Decoder mode) the user need to configure [ftm_user_config_t](#). This structure will be used for initialization (FTM_DRV_Init). The next functions used are specific for each operation mode.

PWM mode

For this mode, the user needs to configure parameters such: number of PWM channels, frequency, dead time, fault channels and duty cycle, alignment (edge or center). All this information is included in the [ftm_pwm_param_t](#) structure.

FTM_DRV_UpdatePwmChannel can be used to update duty cycles at run time. If the type of update in the duty cycle when the duty cycle can have value between 0x0 (0%) and 0x8000 (100%). If the type of update in ticks when the firstEdge and secondEdge variables can have value between 0 and ftmPeriod which is stored in the state structure.

Safe state and polarity of the PWM channels

These 2 parameters are dependent from FTM hardware perspective, but the FTM_PWM driver can handle them independently, so polarity field configures the final polarity measured at MCU pins and safeState field is the value of the PWM channel when fault is detected and fault is configured to use safe state, not tri-state mode. The same behavior is available for combined mode, polarity and safe state can be configured independently.

API code changes

In BETA 2.9.0 the following changes were made in FTM_PWM API:

- from [ftm_independent_ch_param_t](#) the following fields were removed: levelSelect
- in [ftm_independent_ch_param_t](#) safeState field was added
- from [ftm_combined_ch_param_t](#) the following fields were removed: levelSelect, levelSelectOnNextChn.
- in [ftm_combined_ch_param_t](#) mainChannelSafeState and secondChannelSafeState fields were added.
- [ftm_safe_state_polarity_t](#) enum was changed

From application perspective the impact is the following:

- second channel can't be used in independent channels, just in combined channels
- polarity and safe state should be checked with the new API.

The advantages of the FTM_PWM API from BETA 2.9,0 are:

- safe state and polarity can be configured without strong understatement of the Reference Manual
- dead time will be always inserted Note that:

- In the `ftm_independent_ch_param_t` structure has the "ftm_safe_state_polarity_t safeState" variable which user can configure the polarity of PWM signal on the channel n+1. and the "ftm_second_channel_polarity_t secondChannelPolarity" is only used to configure the channel n+1 in the complementary mode for the inverted or duplicated channel n.
- In the combined channel, the configuration structure has same feature as in the independent mode. It is only difference which the "ftm_safe_state_polarity_t secondChannelSafeState" variable should be set the channel (n+1) polarity if needed.
- When the fault input is disabled in the configuration the user should be set the `ftm_safe_state_polarity_t` as `FTM_LOW_STATE` for both cases in the independent and combined channel because it is not necessary.
- On S32K1xx, the clock source for Deadtime is always the System Clock, regardless of the current Clock Source used for FTM (Fixed, External).

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_pwm_driver.c
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_common.c
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\drivers\inc\
{S32SDK_PATH}\platform\drivers\src\ftm\
```

Preprocessor symbols

No special symbols are required for this component

Dependencies

Clock Manager Interrupt Manager (Interrupt)

Example:

```
/* The state structure of instance in the PWM mode */
ftm_state_t statePwm;
#define FTM_PWM_INSTANCE 1UL
/* Fault configuration structure */
ftm_pwm_fault_param_t PWM_FaultConfig =
{
    false,
    true,
    5U,
    FTM_FAULT_CONTROL_MAN_EVEN,
    {
        {
            true,
            false,
            FTM_POLARITY_HIGH,
        },
        {
            false,
            false,
            FTM_POLARITY_LOW
        },
        {
            false,
            false,
            FTM_POLARITY_LOW
        },
        {
            false,
            false,
        }
    },
    {
        false,
        false,
    },
    {
        false,
        false,
    }
}
```

```

        FTM_POLARITY_LOW          /* Channel output state on fault */
    }
}
};

/* Independent channels configuration structure for PWM */
ftm_independent_ch_param_t PWM_IndependentChannelsConfig[1] =
{
    {
        0U,                      /* hwChannelId */
        FTM_POLARITY_LOW,        /* Polarity of the PWM signal */
        4096U,                   /* Duty cycle percent 0-0x8000 */
        false,                   /* External Trigger */
        FTM_LOW_STATE,           /* Safe state of the PWM channel when faults are detected */
    }
};

/* PWM configuration for PWM */
ftm_pwm_param_t PWM_PwmConfig =
{
    1U,                          /* Number of independent PWM channels */
    0U,                          /* Number of combined PWM channels */
    FTM_MODE_EDGE_ALIGNED_PWM,   /* PWM mode */
    0U,                          /* DeadTime Value */
    FTM_DEADTIME_DIVID_BY_4,     /* DeadTime clock divider */
    7481U,                      /* PWM frequency */
    PWM_IndependentChannelsConfig, /* Independent PWM channels configuration structure */
    NULL,                       /* Combined PWM channels configuration structure */
    &PWM_FaultConfig             /* PWM fault configuration structure */
};

/* Timer mode configuration for PWM */
/* Global configuration of PWM */
ftm_user_config_t PWM_InitConfig =
{
    {
        true,                    /* Software trigger state */
        false,                   /* Hardware trigger 1 state */
        false,                   /* Hardware trigger 2 state */
        false,                   /* Hardware trigger 3 state */
        true,                    /* Maximum loading point state */
        true,                    /* Min loading point state */
        FTM_SYSTEM_CLOCK,        /* Update mode for INVCTRL register */
        FTM_SYSTEM_CLOCK,        /* Update mode for SWOCTRL register */
        FTM_SYSTEM_CLOCK,        /* Update mode for OUTMASK register */
        FTM_SYSTEM_CLOCK,        /* Update mode for CNTIN register */
        false,                   /* Auto clear trigger state for hardware trigger */
        FTM_UPDATE_NOW,          /* Select synchronization method */
    },
    FTM_MODE_EDGE_ALIGNED_PWM,   /* PWM mode */
    FTM_CLOCK_DIVID_BY_4,        /* FTM clock pre-scaler */
    FTM_CLOCK_SOURCE_SYSTEMCLK,  /* FTM clock source */
    FTM_BDM_MODE_11,            /* FTM debug mode */
    false,                      /* Interrupt state */
    false                        /* Initialization trigger */
};
FTM_DRV_Init(FTM_PWM_INSTANCE, &PWM_InitConfig, &statePwm);
FTM_DRV_InitPwm(FTM_PWM_INSTANCE, &PWM_PwmConfig);
/* It's recommended to use softwareTrigger = true */
/* The SECOND_EDGE value is used only when PWM is used in combined mode */
FTM_DRV_UpdatePwmChannel(FTM_PWM_INSTANCE, 0UL,
    FTM_PWM_UPDATE_IN_DUTY_CYCLE, 0x800U, 0x2000U, true);

```

PWM in Modified Combine mode

For this mode the user needs to configure parameters such: number of PWM channels, frequency, dead time, fault channels and duty cycle, alignment (edge or center). All this information is included in `ftm_pwm_param_t` data type. The Modified Combine PWM mode is intended to support the generation of PWM signals where the period is not modified while the signal is being generated, but the duty cycle will be varied. `FTM_DRV_UpdatePwmChannel` can be used to update duty cycles at run time. If the type of update in the duty cycle when the duty cycle can have value between 0x0 (0%) and 0x8000 (100%). If the type of update in ticks when the firstEdge and secondEdge variables can have value between 0 and ftmPeriod which is stored in the state structure. In this mode, an even channel (n) and adjacent odd channel (n+1) are combined to generate a PWM signal in the channel (n) output. Thus, the channel (n) match edge is fixed and the channel (n+1) match edge can be varied.

Example:

```

/* The state structure of instance in the PWM mode */
ftm_state_t statePwm;
#define FTM_PWM_INSTANCE          0UL

```

```

/* Fault configuration structure */
ftm_pwm_fault_param_t PWM_FaultConfig =
{
    false,
    true,
    5U,
    FTM_FAULT_CONTROL_MAN_EVEN,
    {
        {
            true,
            false,
            FTM_POLARITY_HIGH,
        },
        {
            false,
            false,
            FTM_POLARITY_LOW
        },
        {
            false,
            false,
            FTM_POLARITY_LOW
        },
        {
            false,
            false,
            FTM_POLARITY_LOW
        }
    }
};

/* Combine channels configuration structure for PWM */
ftm_combined_ch_param_t flexTimer1_CombinedChannelsConfig[1] =
{
    {
        2U,
        0U,
        0U,
        true,
        true,
        FTM_POLARITY_HIGH,
        true,
        FTM_MAIN_INVERTED,
        false,
        false,
        FTM_LOW_STATE,
        FTM_LOW_STATE,
    }
};

/* PWM configuration for PWM */
ftm_pwm_param_t PWM_PwmConfig =
{
    0U,
    1U,
    FTM_MODE_EDGE_ALIGNED_PWM,
    0U,
    FTM_DEADTIME_DIVID_BY_4,
    7481U,
    NULL,
    flexTimer1_CombinedChannelsConfig,
    &PWM_FaultConfig
};

/* Timer mode configuration for PWM */
/* Global configuration of PWM */
ftm_user_config_t PWM_InitConfig =
{
    {
        true,
        false,
        false,
        false,
        true,
        true,
        FTM_SYSTEM_CLOCK,
        FTM_SYSTEM_CLOCK,
        FTM_SYSTEM_CLOCK,
        FTM_SYSTEM_CLOCK,
        false,
        FTM_UPDATE_NOW,
    },
    FTM_MODE_EDGE_ALIGNED_PWM,
    FTM_CLOCK_DIVID_BY_4,
    FTM_CLOCK_SOURCE_SYSTEMCLK,
    FTM_BDM_MODE_11,
    false,
    false
};

```

```
FTM_DRV_Init(FTM_PWM_INSTANCE, &PWM_InitConfig, &statePwm);
FTM_DRV_InitPwm(FTM_PWM_INSTANCE, &PWM_PwmConfig);
/* It's recommended to use softwareTrigger = true */
/* Only second edge can be updated when FTM is running. */
FTM_DRV_UpdatePwmChannel(FTM_PWM_INSTANCE, 0UL,
    FTM_PWM_UPDATE_IN_DUTY_CYCLE, 0x0U, 0x2000U, true);
```

Edge-Aligned PWM and Input Capture mode

Support an additional Input Capture mode on other channels in the same FTM instance:

- The measurement range of Input Capture will depend on PWM configuration. The frequency of measured signal must be greater than frequency of PWM signal.
- For this mode, the recommended synchronization point is the next loading point (not immediately) to avoid breaking the current measurement signal from Input Capture.
- The S32CT configuration is not possible to add both drivers on the same instance, even if the driver supports this. The initialization sequences below:

```
/* The state structure of instance in the PWM and Input Capture mode */
ftm_state_t statePwmIc;
#define FTM_PWM_IC_INSTANCE 0UL
/* Fault configuration structure */
ftm_pwm_fault_param_t PWM_FaultConfig =
{
    false,
    true,
    5U,
    FTM_FAULT_CONTROL_MAN_EVEN,
    {
        {
            true,
            false,
            FTM_POLARITY_HIGH,
        },
        {
            false,
            false,
            FTM_POLARITY_LOW,
        },
        {
            false,
            false,
            FTM_POLARITY_LOW,
        },
        {
            false,
            false,
            FTM_POLARITY_LOW,
        }
    }
};
/* Combine channels configuration structure for PWM */
ftm_combined_ch_param_t flexTimer1_CombinedChannelsConfig[1] =
{
    {
        0U,
        0U,
        0x2000U,
        true,
        true,
        FTM_POLARITY_HIGH,
        true,
        FTM_MAIN_INVERTED,
        false,
        false,
        FTM_LOW_STATE,
        FTM_LOW_STATE,
    }
};
/* PWM configuration for PWM */
ftm_pwm_param_t PWM_PwmConfig =
{
    0U,
    1U,
    FTM_MODE_EDGE_ALIGNED_PWM,
    0U,
    FTM_DEADTIME_DIVID_BY_4,
    7481U,
    /* Number of independent PWM channels */
    /* Number of combined PWM channels */
    /* PWM mode */
    /* DeadTime Value */
    /* DeadTime clock divider */
    /* PWM frequency */
};
```

```

    NULL, /* Independent PWM channels configuration structure */
    flexTimer1_CombinedChannelsConfig, /* Combined PWM channels configuration structure */
    &PWM_FaultConfig /* PWM fault configuration structure */
};
/* Channels configuration structure for inputCapture input capture */
ftm_input_ch_param_t inputCapture_InputCaptureChannelConfig[1] =
{
    {
        3U, /* Channel 3 (Make sure that the channel ID must different than PWM
            channels) */
        FTM_EDGE_DETECT, /* Input capture operation Mode */
        FTM_RISING_EDGE, /* Edge alignment Mode */
        FTM_NO_MEASUREMENT, /* Signal measurement operation type */
        0U, /* Filter value */
        false, /* Filter disabled */
        true, /* Continuous mode measurement */
        NULL, /* Vector of callbacks parameters for channels events */
        NULL /* Vector of callbacks for channels events */
    }
};
/* Input capture configuration for inputCapture */
ftm_input_param_t inputCapture_InputCaptureConfig =
{
    1U, /* Number of channels */
    65535U, /* Maximum count value (This value is ignored and replaced by
        period value calculated from PWM configuration) */
    inputCapture_InputCaptureChannelConfig /* Channels configuration */
};
/* Timer mode configuration for PWM and Input Capture */
ftm_user_config_t PWM_IC_InitConfig =
{
    {
        true, /* Software trigger state */
        false, /* Hardware trigger 1 state */
        false, /* Hardware trigger 2 state */
        false, /* Hardware trigger 3 state */
        true, /* Maximum loading point state */
        true, /* Min loading point state */
        FTM_SYSTEM_CLOCK, /* Update mode for INVCTRL register */
        FTM_SYSTEM_CLOCK, /* Update mode for SWOCTRL register */
        FTM_SYSTEM_CLOCK, /* Update mode for OUTMASK register */
        FTM_SYSTEM_CLOCK, /* Update mode for CNTIN register */
        false, /* Auto clear trigger state for hardware trigger */
        FTM_WAIT_LOADING_POINTS, /* Select synchronization method (Next Loading
            Point is recommended) */
    },
    FTM_MODE_EDGE_ALIGNED_PWM, /* Edge-Align PWM mode that can be used with
        Input Capture mode */
    FTM_CLOCK_DIVID_BY_4, /* FTM clock pre-scaler */
    FTM_CLOCK_SOURCE_SYSTEMCLK, /* FTM clock source */
    FTM_BDM_MODE_11, /* FTM debug mode */
    false, /* Interrupt state */
    false /* Initialization trigger */
};

/* Initialize FTM module */
FTM_DRV_Init(FTM_PWM_IC_INSTANCE, &PWM_IC_InitConfig, &statePwmIc);
/* Initialize PWM configuration (Clock configuration for both PWM and Input Capture mode)
 * Initialize the additional Input Capture mode for other channels
 * FTM_DRV_InitPwm() must be called first before user calls FTM_DRV_InitInputCapture()
 */
FTM_DRV_InitPwm(FTM_PWM_IC_INSTANCE, &PWM_PwmConfig);
FTM_DRV_InitInputCapture(FTM_PWM_IC_INSTANCE, &inputCapture_InputCaptureConfig);

...

/* De-initialize Input Capture first
 * PWM signal still work normally
 */
FTM_DRV_DeinitInputCapture(FTM_PWM_IC_INSTANCE, &inputCapture_InputCaptureConfig);
/* De-initialize PWM (FTM counter will be disabled) */
FTM_DRV_DeinitPwm(FTM_PWM_IC_INSTANCE);

```

Data Structures

- struct `ftm_pwm_ch_fault_param_t`
FlexTimer driver PWM Fault channel parameters. [More...](#)
- struct `ftm_pwm_fault_param_t`
FlexTimer driver PWM Fault parameter. [More...](#)
- struct `ftm_independent_ch_param_t`
FlexTimer driver independent PWM parameter. [More...](#)

- struct [ftm_combined_ch_param_t](#)
FlexTimer driver combined PWM parameter. [More...](#)
- struct [ftm_pwm_param_t](#)
FlexTimer driver PWM parameters. [More...](#)

Macros

- #define [FTM_MAX_DUTY_CYCLE](#) (0x8000U)
Maximum value for PWM duty cycle.
- #define [FTM_DUTY_TO_TICKS_SHIFT](#) (15U)
Shift value which converts duty to ticks.

Enumerations

- enum [ftm_pwm_update_option_t](#) { [FTM_PWM_UPDATE_IN_DUTY_CYCLE](#) = 0x00U, [FTM_PWM_UPDATE_IN_TICKS](#) = 0x01U }
FlexTimer Configure type of PWM update in the duty cycle or in ticks.
- enum [ftm_polarity_t](#) { [FTM_POLARITY_LOW](#) = 0x00U, [FTM_POLARITY_HIGH](#) = 0x01U }
The polarity of the channel output is configured in PWM signal.
- enum [ftm_second_channel_polarity_t](#) { [FTM_MAIN_INVERTED](#) = 0x01U, [FTM_MAIN_DUPLICATED](#) = 0x00U }
FlexTimer PWM channel (n+1) polarity for combine mode.
- enum [ftm_fault_mode_t](#) { [FTM_FAULT_CONTROL_DISABLED](#) = 0x00U, [FTM_FAULT_CONTROL_MANUAL_EVEN](#) = 0x01U, [FTM_FAULT_CONTROL_MANUAL_ALL](#) = 0x02U, [FTM_FAULT_CONTROL_AUTO_ALL](#) = 0x03U }
FlexTimer fault control.
- enum [ftm_safe_state_polarity_t](#) { [FTM_LOW_STATE](#) = 0x00U, [FTM_HIGH_STATE](#) = 0x01U }
Select level of the channel (n) output at the beginning.

Functions

- status_t [FTM_DRV_DeinitPwm](#) (uint32_t instance)
Stops all PWM channels .
- status_t [FTM_DRV_InitPwm](#) (uint32_t instance, const [ftm_pwm_param_t](#) *param)
Configures the duty cycle and frequency and starts the output of the PWM on all channels configured in the param structure. The independent channel configuration need to clarify the polarity and safe state as following:
- status_t [FTM_DRV_UpdatePwmChannel](#) (uint32_t instance, uint8_t channel, [ftm_pwm_update_option_t](#) typeOfUpdate, uint16_t firstEdge, uint16_t secondEdge, bool softwareTrigger)
This function updates the waveform output in PWM mode (duty cycle and phase).
- status_t [FTM_DRV_FastUpdatePwmChannels](#) (uint32_t instance, uint8_t numberOfChannels, const uint8_t *channels, const uint16_t *duty, bool softwareTrigger)
This function will update the duty cycle of PWM output for multiple channels.
- status_t [FTM_DRV_UpdatePwmPeriod](#) (uint32_t instance, [ftm_pwm_update_option_t](#) typeOfUpdate, uint32_t newValue, bool softwareTrigger)
This function will update the new period in the frequency or in the counter value into mode register which modify the period of PWM signal on the channel output.
- status_t [FTM_DRV_ControlChannelOutput](#) (uint32_t instance, uint8_t channel, bool enableChannelOutput)
This function is used to control the final logic of the channel output.

17.63.2 Data Structure Documentation

17.63.2.1 struct ftm_pwm_ch_fault_param_t

FlexTimer driver PWM Fault channel parameters.

Implements : ftm_pwm_ch_fault_param_t_Class

Definition at line 112 of file ftm_pwm_driver.h.

Data Fields

- bool [faultChannelEnabled](#)
- bool [faultFilterEnabled](#)
- [ftm_polarity_t](#) [ftmFaultPinPolarity](#)

Field Documentation

17.63.2.1.1 bool faultChannelEnabled

Fault channel state

Definition at line 114 of file ftm_pwm_driver.h.

17.63.2.1.2 bool faultFilterEnabled

Fault channel filter state

Definition at line 115 of file ftm_pwm_driver.h.

17.63.2.1.3 ftm_polarity_t ftmFaultPinPolarity

Channel output state on fault

Definition at line 116 of file ftm_pwm_driver.h.

17.63.2.2 struct ftm_pwm_fault_param_t

FlexTimer driver PWM Fault parameter.

Implements : ftm_pwm_fault_param_t_Class

Definition at line 124 of file ftm_pwm_driver.h.

Data Fields

- bool [pwmOutputStateOnFault](#)
- bool [pwmFaultInterrupt](#)
- uint8_t [faultFilterValue](#)
- [ftm_fault_mode_t](#) [faultMode](#)
- [ftm_pwm_ch_fault_param_t](#) [ftmFaultChannelParam](#) [FTM_FEATURE_FAULT_CHANNELS]

Field Documentation

17.63.2.2.1 uint8_t faultFilterValue

Fault filter value

Definition at line 128 of file ftm_pwm_driver.h.

17.63.2.2.2 ftm_fault_mode_t faultMode

Fault mode

Definition at line 129 of file ftm_pwm_driver.h.

17.63.2.2.3 `ftm_pwm_ch_fault_param_t` `ftmFaultChannelParam`[FTM_FEATURE_FAULT_CHANNELS]

Fault channels configuration

Definition at line 130 of file `ftm_pwm_driver.h`.

17.63.2.2.4 `bool` `pwmFaultInterrupt`

PWM fault interrupt state

Definition at line 127 of file `ftm_pwm_driver.h`.

17.63.2.2.5 `bool` `pwmOutputStateOnFault`

Output pin state on fault (safe state or tri-state)

Definition at line 126 of file `ftm_pwm_driver.h`.

17.63.2.3 `struct` `ftm_independent_ch_param_t`

FlexTimer driver independent PWM parameter.

Implements : `ftm_independent_ch_param_t_Class`

Definition at line 138 of file `ftm_pwm_driver.h`.

Data Fields

- `uint8_t` `hwChannelId`
- `ftm_polarity_t` `polarity`
- `uint16_t` `uDutyCyclePercent`
- `bool` `enableExternalTrigger`
- `ftm_safe_state_polarity_t` `safeState`
- `bool` `enableSecondChannelOutput`
- `ftm_second_channel_polarity_t` `secondChannelPolarity`
- `bool` `deadTime`

Field Documentation

17.63.2.3.1 `bool` `deadTime`

Enable/disable dead time for channel

Definition at line 150 of file `ftm_pwm_driver.h`.

17.63.2.3.2 `bool` `enableExternalTrigger`

true: enable the generation of a trigger is used for on-chip modules false: disable the generation of a trigger

Definition at line 144 of file `ftm_pwm_driver.h`.

17.63.2.3.3 `bool` `enableSecondChannelOutput`

Enable complementary mode on next channel

Definition at line 148 of file `ftm_pwm_driver.h`.

17.63.2.3.4 `uint8_t` `hwChannelId`

Physical hardware channel ID

Definition at line 140 of file `ftm_pwm_driver.h`.

17.63.2.3.5 `ftm_polarity_t` `polarity`

Polarity of the PWM signal generated on MCU pin.

Definition at line 141 of file ftm_pwm_driver.h.

17.63.2.3.6 `ftm_safe_state_polarity_t` safeState

Logical state of the PWM channel n when an fault is detected and to set up the polarity of PWM signal on the channel (n+1)

Definition at line 146 of file ftm_pwm_driver.h.

17.63.2.3.7 `ftm_second_channel_polarity_t` secondChannelPolarity

Polarity of the channel n+1 relative to channel n in the complementary mode

Definition at line 149 of file ftm_pwm_driver.h.

17.63.2.3.8 `uint16_t` uDutyCyclePercent

PWM pulse width, value should be between 0 (0%) to FTM_MAX_DUTY_CYCLE (100%)

Definition at line 142 of file ftm_pwm_driver.h.

17.63.2.4 `struct ftm_combined_ch_param_t`

FlexTimer driver combined PWM parameter.

Implements : `ftm_combined_ch_param_t` Class

Definition at line 159 of file ftm_pwm_driver.h.

Data Fields

- `uint8_t` hwChannelId
- `uint16_t` firstEdge
- `uint16_t` secondEdge
- `bool` deadTime
- `bool` enableModifiedCombine
- `ftm_polarity_t` mainChannelPolarity
- `bool` enableSecondChannelOutput
- `ftm_second_channel_polarity_t` secondChannelPolarity
- `bool` enableExternalTrigger
- `bool` enableExternalTriggerOnNextChn
- `ftm_safe_state_polarity_t` mainChannelSafeState
- `ftm_safe_state_polarity_t` secondChannelSafeState

Field Documentation

17.63.2.4.1 `bool` deadTime

Enable/disable dead time for channel

Definition at line 166 of file ftm_pwm_driver.h.

17.63.2.4.2 `bool` enableExternalTrigger

The generation of the channel (n) trigger true: enable the generation of a trigger on the channel (n) false: disable the generation of a trigger on the channel (n)

Definition at line 171 of file ftm_pwm_driver.h.

17.63.2.4.3 `bool` enableExternalTriggerOnNextChn

The generation of the channel (n+1) trigger true: enable the generation of a trigger on the channel (n+1) false: disable the generation of a trigger on the channel (n+1)

Definition at line 174 of file ftm_pwm_driver.h.

17.63.2.4.4 bool enableModifiedCombine

Enable/disable the modified combine mode for channels (n) and (n+1)

Definition at line 167 of file ftm_pwm_driver.h.

17.63.2.4.5 bool enableSecondChannelOutput

Select if channel (n+1) output is enabled/disabled for the complementary mode

Definition at line 169 of file ftm_pwm_driver.h.

17.63.2.4.6 uint16_t firstEdge

First edge time. This time is relative to signal period. The value for this parameter is between 0 and FTM_MAX_DUTY_CYCLE(0 = 0% from period and FTM_MAX_DUTY_CYCLE = 100% from period)

Definition at line 162 of file ftm_pwm_driver.h.

17.63.2.4.7 uint8_t hwChannelId

Physical hardware channel ID for channel (n)

Definition at line 161 of file ftm_pwm_driver.h.

17.63.2.4.8 ftm_polarity_t mainChannelPolarity

Polarity of the PWM signal generated on MCU pin for channel n.

Definition at line 168 of file ftm_pwm_driver.h.

17.63.2.4.9 ftm_safe_state_polarity_t mainChannelSafeState

The selection of the channel (n) state when fault is detected

Definition at line 177 of file ftm_pwm_driver.h.

17.63.2.4.10 ftm_second_channel_polarity_t secondChannelPolarity

Select channel (n+1) polarity relative to channel (n) in the complementary mode

Definition at line 170 of file ftm_pwm_driver.h.

17.63.2.4.11 ftm_safe_state_polarity_t secondChannelSafeState

The selection of the channel (n+1) state when fault is detected and set up the polarity of PWM signal on the channel (n+1)

Definition at line 178 of file ftm_pwm_driver.h.

17.63.2.4.12 uint16_t secondEdge

Second edge time. This time is relative to signal period. The value for this parameter is between 0 and FTM_MAX_DUTY_CYCLE(0 = 0% from period and FTM_MAX_DUTY_CYCLE = 100% from period)

Definition at line 164 of file ftm_pwm_driver.h.

17.63.2.5 struct ftm_pwm_param_t

FlexTimer driver PWM parameters.

Implements : ftm_pwm_param_t_Class

Definition at line 187 of file ftm_pwm_driver.h.

Data Fields

- `uint8_t nNumIndependentPwmChannels`
- `uint8_t nNumCombinedPwmChannels`
- `ftm_config_mode_t mode`
- `uint8_t deadTimeValue`
- `ftm_deadtime_ps_t deadTimePrescaler`
- `uint32_t uFrequencyHZ`
- `ftm_independent_ch_param_t * pwmIndependentChannelConfig`
- `ftm_combined_ch_param_t * pwmCombinedChannelConfig`
- `ftm_pwm_fault_param_t * faultConfig`

Field Documentation

17.63.2.5.1 `ftm_deadtime_ps_t deadTimePrescaler`

Dead time pre-scaler value[ticks]

Definition at line 193 of file `ftm_pwm_driver.h`.

17.63.2.5.2 `uint8_t deadTimeValue`

Dead time value in [ticks]

Definition at line 192 of file `ftm_pwm_driver.h`.

17.63.2.5.3 `ftm_pwm_fault_param_t* faultConfig`

Configuration for PWM fault

Definition at line 197 of file `ftm_pwm_driver.h`.

17.63.2.5.4 `ftm_config_mode_t mode`

FTM mode

Definition at line 191 of file `ftm_pwm_driver.h`.

17.63.2.5.5 `uint8_t nNumCombinedPwmChannels`

Number of combined PWM channels

Definition at line 190 of file `ftm_pwm_driver.h`.

17.63.2.5.6 `uint8_t nNumIndependentPwmChannels`

Number of independent PWM channels

Definition at line 189 of file `ftm_pwm_driver.h`.

17.63.2.5.7 `ftm_combined_ch_param_t* pwmCombinedChannelConfig`

Configuration for combined PWM channels

Definition at line 196 of file `ftm_pwm_driver.h`.

17.63.2.5.8 `ftm_independent_ch_param_t* pwmIndependentChannelConfig`

Configuration for independent PWM channels

Definition at line 195 of file `ftm_pwm_driver.h`.

17.63.2.5.9 `uint32_t uFrequencyHZ`

PWM period in Hz

Definition at line 194 of file ftm_pwm_driver.h.

17.63.3 Macro Definition Documentation

17.63.3.1 `#define FTM_DUTY_TO_TICKS_SHIFT (15U)`

Shift value which converts duty to ticks.

Definition at line 42 of file ftm_pwm_driver.h.

17.63.3.2 `#define FTM_MAX_DUTY_CYCLE (0x8000U)`

Maximum value for PWM duty cycle.

Definition at line 40 of file ftm_pwm_driver.h.

17.63.4 Enumeration Type Documentation

17.63.4.1 `enum ftm_fault_mode_t`

FlexTimer fault control.

Implements : `ftm_fault_mode_t_Class`

Enumerator

FTM_FAULT_CONTROL_DISABLED Fault control is disabled for all channels

FTM_FAULT_CONTROL_MAN_EVEN Fault control is enabled for even channels only (channels 0, 2, 4, and 6), and the selected mode is the manual fault clearing

FTM_FAULT_CONTROL_MAN_ALL Fault control is enabled for all channels, and the selected mode is the manual fault clearing

FTM_FAULT_CONTROL_AUTO_ALL Fault control is enabled for all channels, and the selected mode is the automatic fault clearing

Definition at line 84 of file ftm_pwm_driver.h.

17.63.4.2 `enum ftm_polarity_t`

The polarity of the channel output is configured in PWM signal.

Implements : `ftm_polarity_t_Class`

Enumerator

FTM_POLARITY_LOW The channel polarity is active LOW which is defined again

FTM_POLARITY_HIGH The channel polarity is active HIGH which is defined again

Definition at line 60 of file ftm_pwm_driver.h.

17.63.4.3 `enum ftm_pwm_update_option_t`

FlexTimer Configure type of PWM update in the duty cycle or in ticks.

Implements : `ftm_pwm_update_option_t_Class`

Enumerator

FTM_PWM_UPDATE_IN_DUTY_CYCLE The type of PWM update in the duty cycle/pulse or also use in frequency update

FTM_PWM_UPDATE_IN_TICKS The type of PWM update in ticks

Definition at line 49 of file ftm_pwm_driver.h.

17.63.4.4 enum `ftm_safe_state_polarity_t`

Select level of the channel (n) output at the beginning.

Implements : `ftm_safe_state_polarity_t_Class`

Enumerator

FTM_LOW_STATE When fault is detected PWM channel is low.

FTM_HIGH_STATE When fault is detected PWM channel is high.

Definition at line 101 of file `ftm_pwm_driver.h`.

17.63.4.5 enum `ftm_second_channel_polarity_t`

FlexTimer PWM channel (n+1) polarity for combine mode.

Implements : `ftm_second_channel_polarity_t_Class`

Enumerator

FTM_MAIN_INVERTED The channel (n+1) output is the inverse of the channel (n) output

FTM_MAIN_DUPLICATED The channel (n+1) output is the same as the channel (n) output

Definition at line 71 of file `ftm_pwm_driver.h`.

17.63.5 Function Documentation

17.63.5.1 `status_t FTM_DRV_ControlChannelOutput (uint32_t instance, uint8_t channel, bool enableChannelOutput)`

This function is used to control the final logic of the channel output.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>channel</i>	The channel which is used in PWM mode.
in	<i>enableChannelOutput</i>	Enable/disable the channel output.

Returns

success

- **STATUS_SUCCESS** : Completed successfully.

Definition at line 675 of file `ftm_pwm_driver.c`.

17.63.5.2 `status_t FTM_DRV_DeinitPwm (uint32_t instance)`

Stops all PWM channels .

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
----	-----------------	-------------------------------------

Returns

counter the current counter value

Definition at line 382 of file `ftm_pwm_driver.c`.

17.63.5.3 `status_t FTM_DRV_FastUpdatePwmChannels (uint32_t instance, uint8_t numberOfChannels, const uint8_t * channels, const uint16_t * duty, bool softwareTrigger)`

This function will update the duty cycle of PWM output for multiple channels.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>numberOfChannels</i>	The number of channels which should be updated.
in	<i>channels</i>	The list of channels which should be updated.
in	<i>duty</i>	The list of duty cycles for selected channels.
in	<i>softwareTrigger</i>	If true a software trigger is generate to update PWM parameters.

Returns

success

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 643 of file ftm_pwm_driver.c.

17.63.5.4 status_t FTM_DRV_InitPwm (uint32_t *instance*, const ftm_pwm_param_t * *param*)

Configures the duty cycle and frequency and starts the output of the PWM on all channels configured in the param structure. The independent channel configuration need to clarify the polarity and safe state as following:

- In the first channel, the POL bit is the value of safeState variable. In the second channel, the POL bit is the same value of safeState with the inverted channel and the POL bit is inverted safeState with the duplicated channel.
- If the polarity and safe state are the value, it will be Low-true pulses. It means the ELSB:ELSA = 0:1. Otherwise, it will be High-true pulses. It means the ELSB:ELSA = 1:0. Regarding the combined channel configuration:
- In both channels, the POL bit is the same value with the safeState variable
- If the polarity and safe state are the value, it will be Low-true pulses. It means the ELSB:ELSA = 0:1. Otherwise, it will be High-true pulses. It means the ELSB:ELSA = 1:0.
- COMP bit will be true when the polarity and safeState are the same value, the second channel is inverted .the first channel or when the polarity and safeState are difference value, the second channel is duplicated the first channel.
- COMP bit will be false when the polarity and safeState are the same value, the second channel is duplicated .the first channel or when the polarity and safeState are difference value, the second channel is inverted the first channel.

: These configuration will impact to the FTM_DRV_SetSoftwareOutputChannelControl and FTM_DRV_SetAllChnSoftwareOutputControl function. Because the software output control behavior depends on the polarity and COMP bit.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>param</i>	FTM driver PWM parameter to configure PWM options.

Returns

success

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 258 of file ftm_pwm_driver.c.

17.63.5.5 `status_t FTM_DRV_UpdatePwmChannel (uint32_t instance, uint8_t channel, ftm_pwm_update_option_t typeOfUpdate, uint16_t firstEdge, uint16_t secondEdge, bool softwareTrigger)`

This function updates the waveform output in PWM mode (duty cycle and phase).

: Regarding the type of updating PWM in the duty cycle, if the expected duty is 100% then the value that is to be written to hardware will be exceed value of period. It means that the FTM counter will not match the value of the CnV register in this case.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>channel</i>	The channel number. In combined mode, the code finds the channel.
in	<i>typeOfUpdate</i>	The type of PWM update in the duty cycle/pulse or in ticks.
in	<i>firstEdge</i>	Duty cycle or first edge time for PWM mode. Can take value between 0 - F _{TM_MAX_DUTY_CYCLE} (0 = 0% from period and F _{TM_MAX_DUTY_CYCLE} = 100% from period) Or value in ticks for the first of the PWM mode in which can have value between 0 and ftmPeriod is stored in the state structure.
in	<i>secondEdge</i>	Second edge time - only for combined mode. Can take value between 0 - F _{TM_MAX_DUTY_CYCLE} (0 = 0% from period and F _{TM_MAX_DUTY_CYCLE} = 100% from period). Or value in ticks for the second of the PWM mode in which can have value between 0 and ftmPeriod is stored in the state structure.
in	<i>softwareTrigger</i>	If true a software trigger is generate to update PWM parameters.

Returns

success

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 447 of file ftm_pwm_driver.c.

17.63.5.6 `status_t FTM_DRV_UpdatePwmPeriod (uint32_t instance, ftm_pwm_update_option_t typeOfUpdate, uint32_t newValue, bool softwareTrigger)`

This function will update the new period in the frequency or in the counter value into mode register which modify the period of PWM signal on the channel output.

Parameters

in	<i>instance</i>	The FTM peripheral instance number.
in	<i>typeOfUpdate</i>	The type of PWM update is a period in Hz or in ticks. <ul style="list-style-type: none"> • For FTM_PWM_UPDATE_IN_DUTY_CYCLE which reuse in FTM_DRV_UpdatePwmChannel function will update in Hz. • For FTM_PWM_UPDATE_IN_TICKS will update in ticks.
in	<i>newValue</i>	The frequency or the counter value which will select with modified value for PWM signal. If the type of update in the duty cycle, the newValue parameter must be value between 1U and maximum is the frequency of the FTM counter. If the type of update in ticks, the newValue parameter must be value between 1U and 0xFFFFU.

in	<i>softwareTrigger</i>	If true a software trigger is generate to update PWM parameters.
----	------------------------	--

Returns

operation status

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 576 of file ftm_pwm_driver.c.

17.64 FlexTimer Quadrature Decoder Driver (FTM_QD)

17.64.1 Detailed Description

FlexTimer Quadrature Decoder Peripheral Driver.

Hardware background

The FTM of the S32K1xx is based on a 16 bits counter and supports: input capture, output compare, PWM and some instances include quadrature decoder.

How to use FTM driver in your application

For all operation modes (without Quadrature Decoder mode) the user need to configure [ftm_user_config_t](#). This structure will be used for initialization (FTM_DRV_Init). The next functions used are specific for each operation mode.

Quadrature decoder mode

For this mode the user needs to configure parameters like: maximum counter value, initial counter value, mode (Count and Direction Encoding mode), and for both input phases polarity and filtering. All this information is included in [ftm_quad_decode_config_t](#). In this mode, the counter is clocked by the phase A and phase B. The current state of the decoder can be obtained using FTM_DRV_QuadGetState.

Hardware limitation:

In count and direction mode if initial value of the PHASE_A is HIGH the counter will be incremented.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_qd_driver.c
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_common.c
{S32SDK_PATH}\platform\drivers\src\ftm\ftm_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\drivers\inc\
{S32SDK_PATH}\platform\drivers\src\ftm\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager Interrupt Manager \(Interrupt\)](#)

Example:

```
/* The state structure of instance in the quadrature mode */
ftm_state_t stateQuad;
#define FTM_QUADRATURE_INSTANCE 1UL
ftm_quad_decoder_state_t quadra_state;
ftm_quad_decode_config_t quadrature_decoder_configuration =
{
    FTM_QUAD_COUNT_AND_DIR, /* Quadrature decoder mode */
    0U, /* Initial counter value */
    32500U, /* Maximum counter value */
    {
```

```

        false,                /* Filter state */
        0U,                   /* Filter value */
        FTM_QUAD_PHASE_NORMAL /* Phase polarity */
    },
    {
        false,                /* Filter state */
        0U,                   /* Filter value */
        FTM_QUAD_PHASE_NORMAL /* Phase polarity */
    }
};

/* Timer mode configuration for Quadrature */
/* Global configuration of Quadrature */
ftm_user_config_t Quadrature_InitConfig =
{
    {
        false,                /* Software trigger state */
        false,                /* Hardware trigger 1 state */
        false,                /* Hardware trigger 2 state */
        false,                /* Hardware trigger 3 state */
        false,                /* Maximum loading point state */
        false,                /* Min loading point state */
        FTM_SYSTEM_CLOCK,     /* Update mode for INVCTRL register */
        FTM_SYSTEM_CLOCK,     /* Update mode for SWOCTRL register */
        FTM_SYSTEM_CLOCK,     /* Update mode for OUTMASK register */
        FTM_SYSTEM_CLOCK,     /* Update mode for CNTIN register */
        false,                /* Auto clear trigger state for hardware trigger */
        FTM_UPDATE_NOW,       /* Select synchronization method */
    },
    FTM_MODE_QUADRATURE_DECODER, /* Mode of operation for FTM */
    FTM_CLOCK_DIVID_BY_2,       /* FTM clock pre-scaler */
    FTM_CLOCK_SOURCE_SYSTEMCLK, /* FTM clock source */
    FTM_BDM_MODE_11,           /* FTM debug mode */
    false,                     /* Interrupt state */
    false                       /* Initialization trigger */
};

FTM_DRV_Init(FTM_QUADRATURE_INSTANCE, &Quadrature_InitConfig, &stateQuad);
FTM_DRV_QuadDecodeStart(FTM_QUADRATURE_INSTANCE, &quadrature_decoder_configuration);
quadra_state = FTM_DRV_QuadGetState(FTM_QUADRATURE_INSTANCE);

```

Data Structures

- struct [ftm_phase_params_t](#)
FlexTimer quadrature decoder channel parameters. [More...](#)
- struct [ftm_quad_decode_config_t](#)
FTM quadrature configure structure. [More...](#)
- struct [ftm_quad_decoder_state_t](#)
FTM quadrature state(counter value and flags) [More...](#)

Enumerations

- enum [ftm_quad_decode_mode_t](#) { [FTM_QUAD_PHASE_ENCODE](#) = 0x00U, [FTM_QUAD_COUNT_AND_DIRECTION](#) = 0x01U }
 - enum [ftm_quad_phase_polarity_t](#) { [FTM_QUAD_PHASE_NORMAL](#) = 0x00U, [FTM_QUAD_PHASE_INVERTED](#) = 0x01U }
- FlexTimer quadrature decode modes, phase encode or count and direction mode.*
- FlexTimer quadrature phase polarities, normal or inverted polarity.*

Functions

- status_t [FTM_DRV_QuadDecodeStart](#) (uint32_t instance, const [ftm_quad_decode_config_t](#) *config)
Configures the quadrature mode and starts measurement.
- status_t [FTM_DRV_QuadDecodeStop](#) (uint32_t instance)
De-activates the quadrature decode mode.
- [ftm_quad_decoder_state_t](#) [FTM_DRV_QuadGetState](#) (uint32_t instance)
Return the current quadrature decoder state (counter value, overflow flag and overflow direction)
- void [FTM_QD_DRV_GetDefaultConfig](#) ([ftm_quad_decode_config_t](#) *const config)
This function will get the default configuration values in the structure which is used as a common use-case.

17.64.2 Data Structure Documentation

17.64.2.1 struct ftm_phase_params_t

FlexTimer quadrature decoder channel parameters.

Implements : `ftm_phase_params_t_Class`

Definition at line 64 of file `ftm_qd_driver.h`.

Data Fields

- bool `phaseInputFilter`
- uint8_t `phaseFilterVal`
- `ftm_quad_phase_polarity_t` `phasePolarity`

Field Documentation

17.64.2.1.1 uint8_t phaseFilterVal

Filter value (if input filter is enabled)

Definition at line 68 of file `ftm_qd_driver.h`.

17.64.2.1.2 bool phaseInputFilter

false: disable phase filter, true: enable phase filter

Definition at line 66 of file `ftm_qd_driver.h`.

17.64.2.1.3 ftm_quad_phase_polarity_t phasePolarity

Phase polarity

Definition at line 69 of file `ftm_qd_driver.h`.

17.64.2.2 struct ftm_quad_decode_config_t

FTM quadrature configure structure.

Implements : `ftm_quad_decode_config_t_Class`

Definition at line 77 of file `ftm_qd_driver.h`.

Data Fields

- `ftm_quad_decode_mode_t` `mode`
- uint16_t `initialVal`
- uint16_t `maxVal`
- `ftm_phase_params_t` `phaseAConfig`
- `ftm_phase_params_t` `phaseBConfig`

Field Documentation

17.64.2.2.1 uint16_t initialVal

Initial counter value

Definition at line 80 of file `ftm_qd_driver.h`.

17.64.2.2.2 uint16_t maxVal

Maximum counter value

Definition at line 81 of file `ftm_qd_driver.h`.

17.64.2.2.3 `ftm_quad_decode_mode_t` mode

FTM_QUAD_PHASE_ENCODE or FTM_QUAD_COUNT_AND_DIR

Definition at line 79 of file `ftm_qd_driver.h`.

17.64.2.2.4 `ftm_phase_params_t` phaseAConfig

Configuration for the input phase a

Definition at line 82 of file `ftm_qd_driver.h`.

17.64.2.2.5 `ftm_phase_params_t` phaseBConfig

Configuration for the input phase b

Definition at line 83 of file `ftm_qd_driver.h`.

17.64.2.3 `struct ftm_quad_decoder_state_t`

FTM quadrature state(counter value and flags)

Implements : `ftm_quad_decoder_state_t_Class`

Definition at line 91 of file `ftm_qd_driver.h`.

Data Fields

- `uint16_t` [counter](#)
- `bool` [overflowFlag](#)
- `bool` [overflowDirection](#)
- `bool` [counterDirection](#)

Field Documentation

17.64.2.3.1 `uint16_t` counter

Counter value

Definition at line 93 of file `ftm_qd_driver.h`.

17.64.2.3.2 `bool` counterDirection

False FTM counter is decreasing, True FTM counter is increasing

Definition at line 98 of file `ftm_qd_driver.h`.

17.64.2.3.3 `bool` overflowDirection

False if overflow occurred at minimum value, True if overflow occurred at maximum value

Definition at line 96 of file `ftm_qd_driver.h`.

17.64.2.3.4 `bool` overflowFlag

True if overflow occurred, False if overflow doesn't occurred

Definition at line 94 of file `ftm_qd_driver.h`.

17.64.3 Enumeration Type Documentation

17.64.3.1 `enum ftm_quad_decode_mode_t`

FlexTimer quadrature decode modes, phase encode or count and direction mode.

Implements : `ftm_quad_decode_mode_t_Class`

Enumerator

FTM_QUAD_PHASE_ENCODE Phase encoding mode

FTM_QUAD_COUNT_AND_DIR Counter and direction encoding mode

Definition at line 40 of file `ftm_qd_driver.h`.

17.64.3.2 enum `ftm_quad_phase_polarity_t`

FlexTimer quadrature phase polarities, normal or inverted polarity.

Implements : `ftm_quad_phase_polarity_t_Class`

Enumerator

FTM_QUAD_PHASE_NORMAL Phase input signal is not inverted before identifying the rising and falling edges of this signal

FTM_QUAD_PHASE_INVERT Phase input signal is inverted before identifying the rising and falling edges of this signal

Definition at line 51 of file `ftm_qd_driver.h`.

17.64.4 Function Documentation

17.64.4.1 `status_t FTM_DRV_QuadDecodeStart (uint32_t instance, const ftm_quad_decode_config_t * config)`

Configures the quadrature mode and starts measurement.

Parameters

<code>in</code>	<code>instance</code>	Instance number of the FTM module.
<code>in</code>	<code>config</code>	Configuration structure (quadrature decode mode, polarity for both phases, initial and maximum value for the counter, filter configuration).

Returns

success

- `STATUS_SUCCESS` : Completed successfully.
- `STATUS_ERROR` : Error occurred.

Definition at line 47 of file `ftm_qd_driver.c`.

17.64.4.2 `status_t FTM_DRV_QuadDecodeStop (uint32_t instance)`

De-activates the quadrature decode mode.

Parameters

<code>in</code>	<code>instance</code>	Instance number of the FTM module.
-----------------	-----------------------	------------------------------------

Returns

success

- `STATUS_SUCCESS` : Completed successfully.
- `STATUS_ERROR` : Error occurred.

Definition at line 106 of file `ftm_qd_driver.c`.

17.64.4.3 `ftm_quad_decoder_state_t FTM_DRV_QuadGetState (uint32_t instance)`

Return the current quadrature decoder state (counter value, overflow flag and overflow direction)

Parameters

<i>in</i>	<i>instance</i>	Instance number of the FTM module.
-----------	-----------------	------------------------------------

Returns

The current state of quadrature decoder

Definition at line 128 of file ftm_qd_driver.c.

17.64.4.4 void FTM_QD_DRV_GetDefaultConfig (ftm_quad_decode_config_t *const *config*)

This function will get the default configuration values in the structure which is used as a common use-case.

Parameters

<i>out</i>	<i>config</i>	Pointer to the structure in which the configuration will be saved.
------------	---------------	--

Returns

None

Definition at line 150 of file ftm_qd_driver.c.

17.65 Flexible I/O (FlexIO)

17.65.1 Detailed Description

The FlexIO is a highly configurable module providing a wide range of functionality including:

- Emulation of a variety of serial communication protocols, such as SPI, I2C, I2S or UART, while requiring low CPU overhead and being more efficient than having multiple dedicated peripherals for each protocol.
- Flexible 16-bit timers with support for a variety of trigger, reset, enable and disable conditions
- PWM/Waveform generation

Several drivers are provided for this device, implementing a variety of communication protocols. There is also a common layer on which all the drivers are based, allowing more driver instances, either of the same type or different types, to function in parallel on the same FlexIO device. Each driver instance needs a certain number of FlexIO resources (shifters and timers) and as long as there are enough free resources new driver instances can be initialized. The table below shows the driver types and the number of resources needed by each one:

Drivers	Timers	Shifters	Pins
SPI	2	2	4
I2C	2	2	2
I2S	2	2	4
UART	1	1	1

The number of timers and shifters available on a specific device can be found in the reference manual.

Modules

- [FlexIO Common Driver](#)
Common services for FlexIO drivers.
- [FlexIO I2C Driver](#)
I2C communication over FlexIO module (FLEXIO_I2C)
- [FlexIO I2S Driver](#)
I2S communication over FlexIO module (FLEXIO_I2S)
- [FlexIO SPI Driver](#)
SPI communication over FlexIO module (FLEXIO_SPI)
- [FlexIO UART Driver](#)
UART communication over FlexIO module (FLEXIO_UART)

17.66 FreeRTOS

FreeRTOS is a Real Time Operating System (RTOS) design to run on microcontrollers which have size constraints and dedicated end applications.

FreeRTOS provides:

- core real time scheduling functionality
- inter-task communication
- timing and synchronisation primitives

Additional functionality can be included with add-on components.

More information about FreeRTOS can be found on the FreeRTOS website: www.freertos.org

Compiler Settings

Please refer to the "Compiler options" section in Release Notes document when creating a new project. The provided compiler options must match with the project to avoid compilation issue or undefined behavior.

17.67 Generic PHY

17.67.1 Detailed Description

Generic PHY driver for 10/100/1000 PHYs following IEEE 802.3-Clause 22.

Supported devices

This driver supports generic devices, supporting Clause 22 IEEE standardized registers. This includes typical 10/100/1000 PHYs like 100BASE-TX or 1000BASE-T

Unsupported API

The following functions are not supported by this driver:

- PHY_SleepAbortReject
- PHY_Sleep
- PHY_Wakeup
- PHY_SelectTestMode
- PHY_EnableInterrupts
- PHY_HandleInterrupt

Device specific configuration options

N/A

Files

- file [phy_generic.c](#)

Macros

- `#define T_RST_MAX 500U`
- `#define BASIC_CONTROL_ADDR 0U`
- `#define ID_1_ADDR 2U`
- `#define ID_2_ADDR 3U`
- `#define AUTONEG_ADVERT_ADDR 4U`
- `#define AUTONEG_LPABILITY_ADDR 5U`
- `#define CONTROL_1000BASET_ADDR 9U`
- `#define STATUS_1000BASET_ADDR 10U`
- `#define EXTENDED_STATUS_ADDR 15U`
- `#define BASIC_CONTROL_RESET_FLAG 0x8000U`
- `#define BASIC_CONTROL_LOOPBACK_FLAG 0x4000U`
- `#define BASIC_CONTROL_AUTONEG_FLAG 0x1000U`
- `#define BASIC_CONTROL_PDOWN_FLAG 0x0800U`
- `#define BASIC_CONTROL_RESTART_AUTONEG_FLAG 0x0200U`
- `#define BASIC_CONTROL_SPEED_LSB_FLAG 0x2000U`
- `#define BASIC_CONTROL_SPEED_MSB_FLAG 0x0040U`
- `#define AUTONEG_100BASETXFD 0x0100U`
- `#define AUTONEG_100BASETXHD 0x0080U`
- `#define AUTONEG_10BASETFD 0x0040U`
- `#define AUTONEG_10BASETHD 0x0020U`
- `#define CONTROL_1000BASET_CONFIG_ENABLE_FLAG 0x1000U`

- `#define CONTROL_1000BASET_CONFIG_VALUE_FLAG 0x0800U`
- `#define AUTONEG_1000BASETFD 0x0200U`
- `#define AUTONEG_1000BASETHD 0x0100U`
- `#define EXTENDED_STATUS_1000BASETHD_FLAG 0x1000U`
- `#define EXTENDED_STATUS_1000BASETFD_FLAG 0x2000U`
- `#define CONTROL_STATUS_1000BASET_OFFSET 0x2U`

Functions

- static status_t `init` (uint8_t phy)
- static status_t `reset` (uint8_t phy)
- static status_t `mainFunction` (uint8_t phy)
- static status_t `getId` (uint8_t phy, phy_id_t *id)
- static status_t `getState` (uint8_t phy, phy_state_t *state)
- static status_t `getLinkStatus` (uint8_t phy, bool *linkUp)
- static status_t `getLinkSpeed` (uint8_t phy, phy_speed_t *speed)
- static status_t `getDelay` (uint8_t phy, phy_delay_t *delay)
- static status_t `suspend` (uint8_t phy)
- static status_t `resume` (uint8_t phy)
- static status_t `enableAutoneg` (uint8_t phy)
- static status_t `disableAutoneg` (uint8_t phy)
- static status_t `restartAutoneg` (uint8_t phy)
- static status_t `setRole` (uint8_t phy, phy_role_t role)
- static status_t `setLoopback` (uint8_t phy, phy_loopback_t loopbackMode)
- static status_t `checkCapabilities` (uint8_t phy)
- static status_t `returnNotSupportUint8Param` (uint8_t phy, uint8_t parameter)

Variables

- `phy_driver_t PHY_driver_generic`
Generic PHY driver structure.
- `phy_driver_t PHY_driver_generic`
Generic PHY driver structure.

17.67.2 Macro Definition Documentation

17.67.2.1 `#define AUTONEG_1000BASETFD 0x0200U`

Definition at line 81 of file phy_generic.c.

17.67.2.2 `#define AUTONEG_1000BASETHD 0x0100U`

Definition at line 82 of file phy_generic.c.

17.67.2.3 `#define AUTONEG_100BASETXFD 0x0100U`

Definition at line 73 of file phy_generic.c.

17.67.2.4 `#define AUTONEG_100BASETXHD 0x0080U`

Definition at line 74 of file phy_generic.c.

17.67.2.5 `#define AUTONEG_10BASETFD 0x0040U`

Definition at line 75 of file phy_generic.c.

17.67.2.6 **#define AUTONEG_10BASETHD 0x0020U**

Definition at line 76 of file phy_generic.c.

17.67.2.7 **#define AUTONEG_ADVERT_ADDR 4U**

Definition at line 59 of file phy_generic.c.

17.67.2.8 **#define AUTONEG_LPABILITY_ADDR 5U**

Definition at line 60 of file phy_generic.c.

17.67.2.9 **#define BASIC_CONTROL_ADDR 0U**

Definition at line 56 of file phy_generic.c.

17.67.2.10 **#define BASIC_CONTROL_AUTONEG_FLAG 0x1000U**

Definition at line 67 of file phy_generic.c.

17.67.2.11 **#define BASIC_CONTROL_LOOPBACK_FLAG 0x4000U**

Definition at line 66 of file phy_generic.c.

17.67.2.12 **#define BASIC_CONTROL_PDOWN_FLAG 0x0800U**

Definition at line 68 of file phy_generic.c.

17.67.2.13 **#define BASIC_CONTROL_RESET_FLAG 0x8000U**

Definition at line 65 of file phy_generic.c.

17.67.2.14 **#define BASIC_CONTROL_RESTART_AUTONEG_FLAG 0x0200U**

Definition at line 69 of file phy_generic.c.

17.67.2.15 **#define BASIC_CONTROL_SPEED_LSB_FLAG 0x2000U**

Definition at line 70 of file phy_generic.c.

17.67.2.16 **#define BASIC_CONTROL_SPEED_MSB_FLAG 0x0040U**

Definition at line 71 of file phy_generic.c.

17.67.2.17 **#define CONTROL_1000BASET_ADDR 9U**

Definition at line 61 of file phy_generic.c.

17.67.2.18 **#define CONTROL_1000BASET_CONFIG_ENABLE_FLAG 0x1000U**

Definition at line 78 of file phy_generic.c.

17.67.2.19 **#define CONTROL_1000BASET_CONFIG_VALUE_FLAG 0x0800U**

Definition at line 79 of file phy_generic.c.

17.67.2.20 **#define CONTROL_STATUS_1000BASET_OFFSET 0x2U**

Definition at line 87 of file phy_generic.c.

17.67.2.21 `#define EXTENDED_STATUS_1000BASETFD_FLAG 0x2000U`

Definition at line 85 of file `phy_generic.c`.

17.67.2.22 `#define EXTENDED_STATUS_1000BASETHD_FLAG 0x1000U`

Definition at line 84 of file `phy_generic.c`.

17.67.2.23 `#define EXTENDED_STATUS_ADDR 15U`

Definition at line 63 of file `phy_generic.c`.

17.67.2.24 `#define ID_1_ADDR 2U`

Definition at line 57 of file `phy_generic.c`.

17.67.2.25 `#define ID_2_ADDR 3U`

Definition at line 58 of file `phy_generic.c`.

17.67.2.26 `#define STATUS_1000BASET_ADDR 10U`

Definition at line 62 of file `phy_generic.c`.

17.67.2.27 `#define T_RST_MAX 500U`

Maximum reset time in ms according to IEEE

Definition at line 52 of file `phy_generic.c`.

17.67.3 Function Documentation

17.67.3.1 `static status_t checkCapabilities (uint8_t phy) [static]`

Definition at line 665 of file `phy_generic.c`.

17.67.3.2 `static status_t disableAutoneg (uint8_t phy) [static]`

Definition at line 424 of file `phy_generic.c`.

17.67.3.3 `static status_t enableAutoneg (uint8_t phy) [static]`

Definition at line 401 of file `phy_generic.c`.

17.67.3.4 `static status_t getDelay (uint8_t phy, phy_delay_t * delay) [static]`

Definition at line 583 of file `phy_generic.c`.

17.67.3.5 `static status_t getId (uint8_t phy, phy_id_t * id) [static]`

Definition at line 329 of file `phy_generic.c`.

17.67.3.6 `static status_t getLinkSpeed (uint8_t phy, phy_speed_t * speed) [static]`

Definition at line 493 of file `phy_generic.c`.

17.67.3.7 `static status_t getLinkStatus (uint8_t phy, bool * linkUp) [static]`

Definition at line 469 of file `phy_generic.c`.

17.67.3.8 `static status_t getState (uint8_t phy, phy_state_t * state) [static]`

Definition at line 356 of file `phy_generic.c`.

17.67.3.9 `static status_t init (uint8_t phy) [static]`

Definition at line 161 of file `phy_generic.c`.

17.67.3.10 `static status_t mainFunction (uint8_t phy) [static]`

Definition at line 255 of file `phy_generic.c`.

17.67.3.11 `static status_t reset (uint8_t phy) [static]`

Definition at line 224 of file `phy_generic.c`.

17.67.3.12 `static status_t restartAutoneg (uint8_t phy) [static]`

Definition at line 447 of file `phy_generic.c`.

17.67.3.13 `static status_t resume (uint8_t phy) [static]`

Definition at line 389 of file `phy_generic.c`.

17.67.3.14 `static status_t returnNotSupportUint8Param (uint8_t phy, uint8_t parameter) [static]`

Definition at line 735 of file `phy_generic.c`.

17.67.3.15 `static status_t setLoopback (uint8_t phy, phy_loopback_t loopbackMode) [static]`

Definition at line 637 of file `phy_generic.c`.

17.67.3.16 `static status_t setRole (uint8_t phy, phy_role_t role) [static]`

Definition at line 596 of file `phy_generic.c`.

17.67.3.17 `static status_t suspend (uint8_t phy) [static]`

Definition at line 377 of file `phy_generic.c`.

17.67.4 Variable Documentation

17.67.4.1 `phy_driver_t` `PHY_driver_generic`

Generic PHY driver structure.

Definition at line 120 of file `phy_generic.c`.

17.67.4.2 `phy_driver_t` `PHY_driver_generic`

Initial value:

```
=
{
    .init           = init,
    .reset          = reset,
    .mainFunction   = mainFunction,
    .getId          = getId,
    .getState       = getState,
    .getLinkStatus  = getLinkStatus,
    .getLinkSpeed   = getLinkSpeed,
    .getDelay       = getDelay,
    .suspend        = suspend,
    .resume         = resume,
    .sleepAbortReject = PHY_SHARED_ReturnNotSupported,
    .sleep          = PHY_SHARED_ReturnNotSupported,
```

```
.wakeup          = PHY_SHARED_ReturnNotSupported,  
.setRole         = setRole,  
.setLoopback     = setLoopback,  
.selectTestMode  = returnNotSupportUint8Param,  
.enableInterrupts = PHY_SHARED_ReturnNotSupported,  
.handleInterrupt = PHY_SHARED_ReturnNotSupported,  
.enableAutoneg   = enableAutoneg,  
.disableAutoneg  = disableAutoneg,  
.restartAutoneg   = restartAutoneg,  
.write           = NULL,  
.read            = NULL,  
.rmw             = NULL,  
.writeMMD        = NULL,  
.readMMD         = NULL,  
.rmwMMD          = NULL  
}
```

Generic PHY driver structure.

Definition at line 120 of file phy_generic.c.

17.68 HVIO high-side configuration options (0x71)

17.68.1 Detailed Description

This section lists all the possible options of 0x71 register related to:

- HVIO N high-side driver configurations

See also

[UJA113X_SetMtpnv\(\)](#)

HVIO8 high-side driver configuration options (0x71:IO8HOC[7])

- #define [HHSDC_IO8HOC_ENABLED](#) 0x00U
HVIO8 high-side driver is controlled by the setting in the HVIO8 control register (See [uja113x_hvio_cfg_t](#))
- #define [HHSDC_IO8HOC_DISABLED](#) 0x80U
HVIO8 high-side driver is off, regardless of the setting in the HVIO8 control register.

HVIO7 high-side driver configuration options (0x71:IO7HOC[6])

- #define [HHSDC_IO7HOC_ENABLED](#) 0x00U
HVIO7 high-side driver is controlled by the setting in the HVIO7 control register (See [uja113x_hvio_cfg_t](#))
- #define [HHSDC_IO7HOC_DISABLED](#) 0x40U
HVIO7 high-side driver is off, regardless of the setting in the HVIO7 control register.

HVIO6 high-side driver configuration options (0x71:IO6HOC[5])

- #define [HHSDC_IO6HOC_ENABLED](#) 0x00U
HVIO6 high-side driver is controlled by the setting in the HVIO6 control register (See [uja113x_hvio_cfg_t](#))
- #define [HHSDC_IO6HOC_DISABLED](#) 0x20U
HVIO6 high-side driver is off, regardless of the setting in the HVIO6 control register.

HVIO5 high-side driver configuration options (0x71:IO5HOC[4])

- #define [HHSDC_IO5HOC_ENABLED](#) 0x00U
HVIO5 high-side driver is controlled by the setting in the HVIO5 control register (See [uja113x_hvio_cfg_t](#))
- #define [HHSDC_IO5HOC_DISABLED](#) 0x10U
HVIO5 high-side driver is off, regardless of the setting in the HVIO5 control register.

HVIO4 high-side driver configuration options (0x71:IO4HOC[3])

- #define [HHSDC_IO4HOC_ENABLED](#) 0x00U
HVIO4 high-side driver is controlled by the setting in the HVIO4 control register (See [uja113x_hvio_cfg_t](#))
- #define [HHSDC_IO4HOC_DISABLED](#) 0x08U
HVIO4 high-side driver is off, regardless of the setting in the HVIO4 control register.

HVIO3 high-side driver configuration options (0x71:IO3HOC[2])

- #define [HHSDC_IO3HOC_ENABLED](#) 0x00U
HVIO3 high-side driver is controlled by the setting in the HVIO3 control register (See [uja113x_hvio_cfg_t](#))
- #define [HHSDC_IO3HOC_DISABLED](#) 0x04U
HVIO3 high-side driver is off, regardless of the setting in the HVIO3 control register.

HVIO2 high-side driver configuration options (0x71:IO2HOC[1])

- `#define HHSDC_IO2HOC_ENABLED 0x00U`
HVIO2 high-side driver is controlled by the setting in the HVIO2 control register (See [uja113x_hvio_cfg_t](#))
- `#define HHSDC_IO2HOC_DISABLED 0x02U`
HVIO2 high-side driver is off, regardless of the setting in the HVIO2 control register.

HVIO1 high-side driver configuration options (0x71:IO1HOC[0])

- `#define HHSDC_IO1HOC_ENABLED 0x00U`
HVIO1 high-side driver is controlled by the setting in the HVIO1 control register (See [uja113x_hvio_cfg_t](#))
- `#define HHSDC_IO1HOC_DISABLED 0x01U`
HVIO1 high-side driver is off, regardless of the setting in the HVIO1 control register.

17.68.2 Macro Definition Documentation

17.68.2.1 `#define HHSDC_IO1HOC_DISABLED 0x01U`

HVIO1 high-side driver is off, regardless of the setting in the HVIO1 control register.

Definition at line 1187 of file `sbc_uja113x.h`.

17.68.2.2 `#define HHSDC_IO1HOC_ENABLED 0x00U`

HVIO1 high-side driver is controlled by the setting in the HVIO1 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1186 of file `sbc_uja113x.h`.

17.68.2.3 `#define HHSDC_IO2HOC_DISABLED 0x02U`

HVIO2 high-side driver is off, regardless of the setting in the HVIO2 control register.

Definition at line 1180 of file `sbc_uja113x.h`.

17.68.2.4 `#define HHSDC_IO2HOC_ENABLED 0x00U`

HVIO2 high-side driver is controlled by the setting in the HVIO2 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1179 of file `sbc_uja113x.h`.

17.68.2.5 `#define HHSDC_IO3HOC_DISABLED 0x04U`

HVIO3 high-side driver is off, regardless of the setting in the HVIO3 control register.

Definition at line 1173 of file `sbc_uja113x.h`.

17.68.2.6 `#define HHSDC_IO3HOC_ENABLED 0x00U`

HVIO3 high-side driver is controlled by the setting in the HVIO3 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1172 of file `sbc_uja113x.h`.

17.68.2.7 `#define HHSDC_IO4HOC_DISABLED 0x08U`

HVIO4 high-side driver is off, regardless of the setting in the HVIO4 control register.

Definition at line 1166 of file `sbc_uja113x.h`.

17.68.2.8 `#define HHSDC_IO4HOC_ENABLED 0x00U`

HVIO4 high-side driver is controlled by the setting in the HVIO4 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1165 of file `sbc_uja113x.h`.

17.68.2.9 #define HHSDC_IO5HOC_DISABLED 0x10U

HVIO5 high-side driver is off, regardless of the setting in the HVIO5 control register.

Definition at line 1159 of file sbc_uja113x.h.

17.68.2.10 #define HHSDC_IO5HOC_ENABLED 0x00U

HVIO5 high-side driver is controlled by the setting in the HVIO5 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1158 of file sbc_uja113x.h.

17.68.2.11 #define HHSDC_IO6HOC_DISABLED 0x20U

HVIO6 high-side driver is off, regardless of the setting in the HVIO6 control register.

Definition at line 1152 of file sbc_uja113x.h.

17.68.2.12 #define HHSDC_IO6HOC_ENABLED 0x00U

HVIO6 high-side driver is controlled by the setting in the HVIO6 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1151 of file sbc_uja113x.h.

17.68.2.13 #define HHSDC_IO7HOC_DISABLED 0x40U

HVIO7 high-side driver is off, regardless of the setting in the HVIO7 control register.

Definition at line 1145 of file sbc_uja113x.h.

17.68.2.14 #define HHSDC_IO7HOC_ENABLED 0x00U

HVIO7 high-side driver is controlled by the setting in the HVIO7 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1144 of file sbc_uja113x.h.

17.68.2.15 #define HHSDC_IO8HOC_DISABLED 0x80U

HVIO8 high-side driver is off, regardless of the setting in the HVIO8 control register.

Definition at line 1138 of file sbc_uja113x.h.

17.68.2.16 #define HHSDC_IO8HOC_ENABLED 0x00U

HVIO8 high-side driver is controlled by the setting in the HVIO8 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1137 of file sbc_uja113x.h.

17.69 HVIO low-side configuration options (0x72)

17.69.1 Detailed Description

This section lists all the possible options of 0x72 register related to:

- HVIO N low-side driver configurations

See also

[UJA113X_SetMtpnv\(\)](#)

HVIO8 low-side driver configuration options (0x72:IO8LOC[7])

- #define [HLSDC_IO8LOC_ENABLED](#) 0x00U
HVIO8 low-side driver is controlled by the setting in the HVIO8 control register (See [uja113x_hvio_cfg_t](#))
- #define [HLSDC_IO8LOC_DISABLED](#) 0x80U
HVIO8 low-side driver is off, regardless of the setting in the HVIO8 control register.

HVIO7 low-side driver configuration options (0x72:IO7LOC[6])

- #define [HLSDC_IO7LOC_ENABLED](#) 0x00U
HVIO7 low-side driver is controlled by the setting in the HVIO8 control register (See [uja113x_hvio_cfg_t](#))
- #define [HLSDC_IO7LOC_DISABLED](#) 0x40U
HVIO4 low-side driver is off, regardless of the setting in the HVIO8 control register.

HVIO6 low-side driver configuration options (0x72:IO6LOC[5])

- #define [HLSDC_IO6LOC_ENABLED](#) 0x00U
HVIO6 low-side driver is controlled by the setting in the HVIO6 control register (See [uja113x_hvio_cfg_t](#))
- #define [HLSDC_IO6LOC_DISABLED](#) 0x20U
HVIO6 low-side driver is off, regardless of the setting in the HVIO6 control register.

HVIO5 low-side driver configuration options (0x72:IO5LOC[4])

- #define [HLSDC_IO5LOC_ENABLED](#) 0x00U
HVIO5 low-side driver is controlled by the setting in the HVIO5 control register (See [uja113x_hvio_cfg_t](#))
- #define [HLSDC_IO5LOC_DISABLED](#) 0x10U
HVIO5 low-side driver is off, regardless of the setting in the HVIO5 control register.

HVIO4 low-side driver configuration options (0x72:IO4LOC[3])

- #define [HLSDC_IO4LOC_ENABLED](#) 0x00U
HVIO4 low-side driver is controlled by the setting in the HVIO4 control register (See [uja113x_hvio_cfg_t](#))
- #define [HLSDC_IO4LOC_DISABLED](#) 0x08U
HVIO4 low-side driver is off, regardless of the setting in the HVIO4 control register.

HVIO3 low-side driver configuration options (0x72:IO3LOC[2])

- #define [HLSDC_IO3LOC_ENABLED](#) 0x00U
HVIO3 low-side driver is controlled by the setting in the HVIO3 control register (See [uja113x_hvio_cfg_t](#))
- #define [HLSDC_IO3LOC_DISABLED](#) 0x04U
HVIO3 low-side driver is off, regardless of the setting in the HVIO3 control register.

HVIO2 low-side driver configuration options (0x72:IO2LOC[1])

- `#define HLSDC_IO2LOC_ENABLED 0x00U`
HVIO2 low-side driver is controlled by the setting in the HVIO2 control register (See [uja113x_hvio_cfg_t](#))
- `#define HLSDC_IO2LOC_DISABLED 0x02U`
HVIO2 low-side driver is off, regardless of the setting in the HVIO2 control register.

HVIO1 low-side driver configuration options (0x72:IO1LOC[0])

- `#define HLSDC_IO1LOC_ENABLED 0x00U`
HVIO1 low-side driver is controlled by the setting in the HVIO1 control register (See [uja113x_hvio_cfg_t](#))
- `#define HLSDC_IO1LOC_DISABLED 0x01U`
HVIO1 low-side driver is off, regardless of the setting in the HVIO1 control register.

17.69.2 Macro Definition Documentation

17.69.2.1 `#define HLSDC_IO1LOC_DISABLED 0x01U`

HVIO1 low-side driver is off, regardless of the setting in the HVIO1 control register.

Definition at line 1256 of file `sbc_uja113x.h`.

17.69.2.2 `#define HLSDC_IO1LOC_ENABLED 0x00U`

HVIO1 low-side driver is controlled by the setting in the HVIO1 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1255 of file `sbc_uja113x.h`.

17.69.2.3 `#define HLSDC_IO2LOC_DISABLED 0x02U`

HVIO2 low-side driver is off, regardless of the setting in the HVIO2 control register.

Definition at line 1249 of file `sbc_uja113x.h`.

17.69.2.4 `#define HLSDC_IO2LOC_ENABLED 0x00U`

HVIO2 low-side driver is controlled by the setting in the HVIO2 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1248 of file `sbc_uja113x.h`.

17.69.2.5 `#define HLSDC_IO3LOC_DISABLED 0x04U`

HVIO3 low-side driver is off, regardless of the setting in the HVIO3 control register.

Definition at line 1242 of file `sbc_uja113x.h`.

17.69.2.6 `#define HLSDC_IO3LOC_ENABLED 0x00U`

HVIO3 low-side driver is controlled by the setting in the HVIO3 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1241 of file `sbc_uja113x.h`.

17.69.2.7 `#define HLSDC_IO4LOC_DISABLED 0x08U`

HVIO4 low-side driver is off, regardless of the setting in the HVIO4 control register.

Definition at line 1235 of file `sbc_uja113x.h`.

17.69.2.8 `#define HLSDC_IO4LOC_ENABLED 0x00U`

HVIO4 low-side driver is controlled by the setting in the HVIO4 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1234 of file `sbc_uja113x.h`.

17.69.2.9 #define HLSDC_IO5LOC_DISABLED 0x10U

HVIO5 low-side driver is off, regardless of the setting in the HVIO5 control register.

Definition at line 1228 of file sbc_uja113x.h.

17.69.2.10 #define HLSDC_IO5LOC_ENABLED 0x00U

HVIO5 low-side driver is controlled by the setting in the HVIO5 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1227 of file sbc_uja113x.h.

17.69.2.11 #define HLSDC_IO6LOC_DISABLED 0x20U

HVIO6 low-side driver is off, regardless of the setting in the HVIO6 control register.

Definition at line 1221 of file sbc_uja113x.h.

17.69.2.12 #define HLSDC_IO6LOC_ENABLED 0x00U

HVIO6 low-side driver is controlled by the setting in the HVIO6 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1220 of file sbc_uja113x.h.

17.69.2.13 #define HLSDC_IO7LOC_DISABLED 0x40U

HVIO4 low-side driver is off, regardless of the setting in the HVIO8 control register.

Definition at line 1214 of file sbc_uja113x.h.

17.69.2.14 #define HLSDC_IO7LOC_ENABLED 0x00U

HVIO7 low-side driver is controlled by the setting in the HVIO8 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1213 of file sbc_uja113x.h.

17.69.2.15 #define HLSDC_IO8LOC_DISABLED 0x80U

HVIO8 low-side driver is off, regardless of the setting in the HVIO8 control register.

Definition at line 1207 of file sbc_uja113x.h.

17.69.2.16 #define HLSDC_IO8LOC_ENABLED 0x00U

HVIO8 low-side driver is controlled by the setting in the HVIO8 control register (See [uja113x_hvio_cfg_t](#))

Definition at line 1206 of file sbc_uja113x.h.

17.70 I2S - Peripheral Abstraction Layer (I2S PAL)

17.70.1 Detailed Description

The S32 SDK provides a Peripheral Abstraction Layer for I2S modules of S32 SDK devices.

The I2S PAL is designed to be portable across all platforms and IPs which support I2S communication.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\pal\src\i2s\i2s_pal.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\pal\inc  
i2s_pal_cfg.h path (this file is provided by user or generated by pex)
```

Compile symbols

No special symbols are required for this component

Dependencies

[Synchronous Audio Interface \(SAI\)](#) [flexio_i2s](#) [Enhanced Direct Memory Access \(eDMA\)](#) [OS Interface \(OSIF\)](#) [Clock manager](#) [Interrupt Manager \(Interrupt\)](#)

How to integrate I2S PAL in your application

Unlike the other drivers, I2S PAL modules need to include a configuration file named `i2s_pal_cfg.h`, which allows the user to specify which IPs are used and how many resources are allocated for each of them (state structures). The following code example shows how to configure one instance for each available I2S IPs.

```
#ifndef i2s_pal_cfg_H  
#define i2s_pal_cfg_H  
  
/* Define which IP instance will be used in current project */  
#define I2S_OVER_FLEXIO  
#define I2S_OVER_SAI  
  
/* Define the resources necessary for current project */  
#define NO_OF_FLEXIO_MASTER_INSTS_FOR_I2S 1U  
#define NO_OF_FLEXIO_SLAVE_INSTS_FOR_I2S 1U  
#define NO_OF_SAI_INSTS_FOR_I2S 1U  
  
#endif /* i2s_pal_cfg_H */
```

The following table contains the matching between platforms and available IPs

IP/MCU	S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	MP↔ C5748G	MP↔ C5746C
SAI	NO	NO	NO	NO	NO	YES	YES	YES
FLEXIO↔ O_I2S	YES	YES	YES	YES	YES	YES	NO	NO

In order to use the I2S driver it must be first initialized using function `I2S_Init`. Once initialized, it cannot be initialized again for the same instance until it is de-initialized, using `I2S_Deinit`. Different instances can work independently of each other.

Important Notes

- I2S PAL only works in half duplex mode, meaning it cannot send and receive simultaneously over one instance.

- The driver enables the interrupts for the corresponding module, but any interrupt priority setting must be done by the application.
- When using SAI module for I2S, a success status of sending operation means that all data has been pushed to hardware fifo (not output pin), up to 8 tx words will be discarded if users call deinit or switch to receiving operation right after that.

Example code

```

/* Buffers */
uint8_t tx[6] = {1,2,3,4,5,6};

/* Callback to continue sending data */
void i2s_Callback0(i2s_event_t event, void *userData)
{
    /* Get from userData the I2S instance of the I2S module */
    i2s_instance_t* instance;
    instance = (i2s_instance_t*)(userData);

    /* Check the event type:
     * - set TX buffers on I2S_EVENT_TX_EMPTY
     */
    if (event == I2S_EVENT_TX_EMPTY)
    {
        I2S_SetTxBuffer(instance, tx, 6UL);
    }
}

/* Define I2S instance */
i2s_instance_t flexioInst = {I2S_INST_TYPE_FLEXIO, 0UL};
/* Configure I2S */
i2s_user_config_t i2sUserConfig0 =
{
    .baudRate      = 100000U,
    .mode          = I2S_MASTER,
    .wordWidth     = 8U,
    .transferType  = I2S_USING_INTERRUPT,
    .rxDMACHannel  = 0U,
    .txDMACHannel  = 0U,
    .callback      = i2s_Callback0,
    .callbackParam = &flexioInst,
    .extension     = NULL
};

/* Configure FLEXIO pins routing */
extension_flexio_for_i2s_t extension;
extension.txPin = 0U;
extension.rxPin = 1U;
extension.sckPin = 2U;
extension.wsPin = 3U;
i2sUserConfig0.extension = &extension;

/* Initializes i2s master for flexio 0 and send 6 words */
I2S_Init(&flexioInst, &i2sUserConfig0);
I2S_SendData(&flexioInst, tx, 6UL);
/* Wait for sending complete */
while (I2S_GetStatus(&flexioInst, NULL) == STATUS_BUSY);
I2S_Deinit(&flexioInst);

```

Data Structures

- struct [i2s_user_config_t](#)
I2S user configuration structure. [More...](#)
- struct [extension_flexio_for_i2s_t](#)
Defines the extension structure for the I2S over FLEXIO. [More...](#)

Enumerations

- enum [i2s_transfer_type_t](#) { [I2S_USING_INTERRUPT](#) = 0U, [I2S_USING_DMA](#) = 1U }
Defines the transfer type.
- enum [i2s_mode_t](#) { [I2S_MASTER](#) = 0U, [I2S_SLAVE](#) = 1U }
Master or slave.

Functions

- `status_t I2S_Init` (const `i2s_instance_t` *instance, const `i2s_user_config_t` *config)
Initializes the I2S module.
- `status_t I2S_Deinit` (const `i2s_instance_t` *instance)
De-initializes the I2S module.
- `status_t I2S_GetBaudRate` (const `i2s_instance_t` *instance, `uint32_t` *configuredBaudRate)
Returns the i2s baud rate.
- `status_t I2S_SetTxBuffer` (const `i2s_instance_t` *instance, const `uint8_t` *txBuff, `uint32_t` txSize)
Keep sending.
- `status_t I2S_SetRxBuffer` (const `i2s_instance_t` *instance, `uint8_t` *rxBuff, `uint32_t` rxSize)
Keep receiving.
- `status_t I2S_SendDataBlocking` (const `i2s_instance_t` *instance, const `uint8_t` *txBuff, `uint32_t` txSize, `uint32_t` timeout)
Perform a blocking I2S transmission.
- `status_t I2S_SendData` (const `i2s_instance_t` *instance, const `uint8_t` *txBuff, `uint32_t` txSize)
Perform a non-blocking I2S transmission.
- `status_t I2S_GetStatus` (const `i2s_instance_t` *instance, `uint32_t` *countRemaining)
Get the status of the current I2S transfer.
- `status_t I2S_ReceiveDataBlocking` (const `i2s_instance_t` *instance, `uint8_t` *rxBuff, `uint32_t` rxSize, `uint32_t` timeout)
Perform a blocking I2S reception.
- `status_t I2S_ReceiveData` (const `i2s_instance_t` *instance, `uint8_t` *rxBuff, `uint32_t` rxSize)
Perform a non-blocking I2S reception.
- `status_t I2S_Abort` (const `i2s_instance_t` *instance)
Terminates a non-blocking transfer early.
- `void I2S_GetDefaultConfig` (`i2s_user_config_t` *const config)
Return default configuration.

17.70.2 Data Structure Documentation

17.70.2.1 struct `i2s_user_config_t`

I2S user configuration structure.

Implements : `i2s_user_config_t_Class`

Definition at line 59 of file `i2s_pal.h`.

Data Fields

- `i2s_transfer_type_t` transferType
- `i2s_mode_t` mode
- `uint32_t` baudRate
- `uint8_t` wordWidth
- `i2s_callback_t` callback
- `void *` callbackParam
- `uint8_t` rxDMACchannel
- `uint8_t` txDMACchannel
- `void *` extension

Field Documentation

17.70.2.1.1 `uint32_t` baudRate

Baud rate in hertz

Definition at line 63 of file `i2s_pal.h`.

17.70.2.1.2 `i2s_callback_t` callback

User callback function. Can be null if not needed.

Definition at line 67 of file `i2s_pal.h`.

17.70.2.1.3 `void*` callbackParam

Parameter for the callback function

Definition at line 68 of file `i2s_pal.h`.

17.70.2.1.4 `void*` extension

This field will be used to add extra settings to the basic configuration like FlexIO data pins

Definition at line 71 of file `i2s_pal.h`.

17.70.2.1.5 `i2s_mode_t` mode

Master or slave

Definition at line 62 of file `i2s_pal.h`.

17.70.2.1.6 `uint8_t` rxDMAChannel

Rx DMA channel number. Only used in DMA mode

Definition at line 69 of file `i2s_pal.h`.

17.70.2.1.7 `i2s_transfer_type_t` transferType

Driver type: interrupts/DMA

Definition at line 61 of file `i2s_pal.h`.

17.70.2.1.8 `uint8_t` txDMAChannel

Tx DMA channel number. Only used in DMA mode

Definition at line 70 of file `i2s_pal.h`.

17.70.2.1.9 `uint8_t` wordWidth

Number of bits in a word - multiple of 8. The word size in transfer functions depends on this parameter Word size for each buffer read/write is 1 byte, 2 bytes or 4 byte, whichever larger and close to wordWidth the most

Definition at line 64 of file `i2s_pal.h`.

17.70.2.2 `struct extension_flexio_for_i2s_t`

Defines the extension structure for the I2S over FLEXIO.

Definition at line 78 of file `i2s_pal.h`.

Data Fields

- `uint8_t` txPin
- `uint8_t` rxPin
- `uint8_t` sckPin
- `uint8_t` wsPin

Field Documentation

17.70.2.2.1 uint8_t rxPin

Flexio pin to use for receive

Definition at line 81 of file i2s_pal.h.

17.70.2.2.2 uint8_t sckPin

Flexio pin to use for serial clock

Definition at line 82 of file i2s_pal.h.

17.70.2.2.3 uint8_t txPin

Flexio pin to use for transmit

Definition at line 80 of file i2s_pal.h.

17.70.2.2.4 uint8_t wsPin

Flexio pin to use for word select

Definition at line 83 of file i2s_pal.h.

17.70.3 Enumeration Type Documentation

17.70.3.1 enum i2s_mode_t

Master or slave.

Implements : i2s_mode_t_Class

Enumerator

I2S_MASTER Generate bit clock and word select signal

I2S_SLAVE Receive bit clock and word select signal

Definition at line 48 of file i2s_pal.h.

17.70.3.2 enum i2s_transfer_type_t

Defines the transfer type.

Implements : i2s_transfer_type_t_Class

Enumerator

I2S_USING_INTERRUPT Driver uses interrupts for data transfers

I2S_USING_DMA Driver uses DMA for data transfers

Definition at line 37 of file i2s_pal.h.

17.70.4 Function Documentation

17.70.4.1 status_t I2S_Abort (const i2s_instance_t * instance)

Terminates a non-blocking transfer early.

Parameters

<i>instance</i>	Instance number
-----------------	-----------------

Definition at line 694 of file i2s_pal.c.

17.70.4.2 `status_t I2S_Deinit (const i2s_instance_t * instance)`

De-initializes the I2S module.

This function de-initializes the I2S module.

Parameters

<i>in</i>	<i>instance</i>	Instance number
-----------	-----------------	-----------------

Definition at line 453 of file i2s_pal.c.

17.70.4.3 `status_t I2S_GetBaudRate (const i2s_instance_t * instance, uint32_t * configuredBaudRate)`

Returns the i2s baud rate.

This function returns the i2s configured baud rate, only call this when instance is configured as master.

Parameters

	<i>instance</i>	Instance number.
<i>out</i>	<i>configured↔ BaudRate</i>	configured baud rate.

Returns

STATUS_SUCCESS

Definition at line 494 of file i2s_pal.c.

17.70.4.4 `void I2S_GetDefaultConfig (i2s_user_config_t *const config)`

Return default configuration.

Return default config for 8 kHz sample rate, 16 bit sample width and 2 channels.

Parameters

<i>out</i>	<i>Pointer</i>	to configuration structure
------------	----------------	----------------------------

Definition at line 907 of file i2s_pal.c.

17.70.4.5 `status_t I2S_GetStatus (const i2s_instance_t * instance, uint32_t * countRemaining)`

Get the status of the current I2S transfer.

Parameters

<i>instance</i>	Instance number
<i>countRemaining</i>	Pointer to value that is populated with the number of words that have been sent in the active transfer

Returns

The transmit status.

Return values

<i>STATUS_SUCCESS</i>	The transmit has completed successfully.
<i>STATUS_BUSY</i>	The transmit is still in progress. will be filled with the number of words that have been transferred so far.
<i>STATUS_I2S_ABORTED</i>	The transmit was aborted.
<i>STATUS_TIMEOUT</i>	A timeout was reached.
<i>STATUS_ERROR</i>	An error occurred.

Definition at line 749 of file i2s_pal.c.

17.70.4.6 `status_t I2S_Init (const i2s_instance_t * instance, const i2s_user_config_t * config)`

Initializes the I2S module.

This function initializes and enables the requested I2S module. Note that when use I2S over SAI, tx and rx line are separated with SAI0, with other SAI instance tx and rx share one line.

Parameters

in	<i>instance</i>	Instance number
in	<i>config</i>	The configuration structure

Definition at line 294 of file i2s_pal.c.

17.70.4.7 `status_t I2S_ReceiveData (const i2s_instance_t * instance, uint8_t * rxBuff, uint32_t rxSize)`

Perform a non-blocking I2S reception.

This function receives a block of data and returns immediately. The rest of the transmission is handled by the interrupt service routine (if the driver is initialized in interrupt mode).

Parameters

in	<i>instance</i>	Instance number
in	<i>rxBuff</i>	pointer to the data to be transferred
in	<i>rxSize</i>	length in words of the data to be transferred

Definition at line 858 of file i2s_pal.c.

17.70.4.8 `status_t I2S_ReceiveDataBlocking (const i2s_instance_t * instance, uint8_t * rxBuff, uint32_t rxSize, uint32_t timeout)`

Perform a blocking I2S reception.

This function receives a block of data and only returns when the transmission is complete.

Parameters

in	<i>instance</i>	Instance number
	<i>rxBuff</i>	pointer to the receive buffer
	<i>rxSize</i>	length in words of the data to be received
	<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error, success or timed out status

Definition at line 808 of file i2s_pal.c.

17.70.4.9 `status_t I2S_SendData (const i2s_instance_t * instance, const uint8_t * txBuff, uint32_t txSize)`

Perform a non-blocking I2S transmission.

This function sends a block of data and returns immediately. The rest of the transmission is handled by the interrupt service routine (if the driver is initialized in interrupt mode).

Parameters

in	<i>instance</i>	Instance number
in	<i>txBuff</i>	pointer to the data to be transferred
in	<i>txSize</i>	length in words of the data to be transferred

Definition at line 649 of file i2s_pal.c.

17.70.4.10 `status_t I2S_SendDataBlocking (const i2s_instance_t * instance, const uint8_t * txBuff, uint32_t txSize, uint32_t timeout)`

Perform a blocking I2S transmission.

This function sends a block of data and only returns when the transmission is complete.

Parameters

in	<i>instance</i>	Instance number
in	<i>txBuff</i>	pointer to the data to be transferred
in	<i>txSize</i>	length in words of the data to be transferred
in	<i>timeout</i>	timeout value in milliseconds

Returns

Error, success or timed out status

Definition at line 526 of file i2s_pal.c.

17.70.4.11 `status_t I2S_SetRxBuffer (const i2s_instance_t * instance, uint8_t * rxBuff, uint32_t rxSize)`

Keep receiving.

This function must be called in callback function when RX_FULI event is reported to ensure rx operation working continuously.

Parameters

in	<i>instance</i>	Instance number
in	<i>rxBuff</i>	pointer to the data to be transferred
in	<i>rxSize</i>	length in words of the data to be transferred

Definition at line 572 of file i2s_pal.c.

17.70.4.12 `status_t I2S_SetTxBuffer (const i2s_instance_t * instance, const uint8_t * txBuff, uint32_t txSize)`

Keep sending.

This function must be called in callback function when TX_EMPTY event is reported to ensure tx operation working continuously.

Parameters

in	<i>instance</i>	Instance number
in	<i>txBuff</i>	pointer to the data to be transferred
in	<i>txSize</i>	length in words of the data to be transferred

Definition at line 611 of file i2s_pal.c.

17.71 Initialization

17.71.1 Detailed Description

Initialize transport layer (queues, status, ...).

Functions

- void [ld_init](#) (l_ifc_handle *iii*)
Initialize or reinitialize the raw and cooked layers.

17.71.2 Function Documentation

17.71.2.1 void ld_init (l_ifc_handle *iii*)

Initialize or reinitialize the raw and cooked layers.

Parameters

<i>in</i>	<i>iii</i>	Interface name
-----------	------------	----------------

Returns

void

Initialize or reinitialize the raw and cooked layers on the interface *iii*. All the transport layer buffers will be initialized.

Definition at line 49 of file `lin_commontl_api.c`.

17.72 Input Capture - Peripheral Abstraction Layer (IC PAL)

17.72.1 Detailed Description

The S32 SDK provides a Peripheral Abstraction Layer for the input capture mode of S32 SDK devices.

The IC PAL driver allows to detect the input signal and measure pulse width or period of the channel input signal. It was designed to be portable across all platforms and IPs which support FTM , eMIOS, FLEXPWM and ETIMER.

How to integrate IC PAL in your application

Unlike the other drivers, IC PAL modules need to include a configuration file named `ic_pal_cfg.h`, which allows the user to specify which IPs are used. The following code example shows how to configure one instance for each available IC IPs.

```
#ifndef IC_PAL_CFG_H
#define IC_PAL_CFG_H

/* Define which IP instance will be used in current project */
#define IC_PAL_OVER_FTM

#endif /* IC_PAL_CFG_H */
```

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\pal\src\ic\ic_pal.c
${S32SDK_PATH}\platform\pal\src\ic\ic_irq.c
${S32SDK_PATH}\platform\pal\src\ic\ic_irq.h
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\pal\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

ftm_ic emios_ic etimer flexpwm

The following table contains the matching between platforms and available IPs

IP/ M CU	S32 K116	S32 K118	S32 K142	S32 K144	S32 K146	S32 K148	M P C5748 G	M P C5746 C	M P C5744 P	S32 R274	S32 R372	S32 K142 W	S32 K144 W
FT M _IC	Y ES	Y ES	Y ES	Y ES	Y ES	Y ES	NO	NO	NO	NO	NO	Y ES	Y ES
e MI O S_ IC	NO	NO	NO	NO	NO	NO	Y ES	Y ES	NO	NO	NO	NO	NO

E↔ TI↔ M↔ ER	NO	NO	NO	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES	Y↔ ES	NO	NO
FL↔ E↔ X↔ P↔ WM	NO	NO	NO	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES	Y↔ ES	NO	NO

Features

- Start timer channel counting with period in ticks function
- Start/stop the channel in the input capture mode
- Get the measured value in ticks for the detection or measurement

Functionality

Initialization

In order to use the IC PAL driver it must be first initialized, using [IC_Init\(\)](#) function. Once initialized, it should be de-initialized before initialized again for the same IC module instance, using [IC_Deinit\(\)](#). The initialization function does the following operations:

- sets the clock source, clock prescaler
- sets the number of channel input capture are used
- configures in the input capture mode for detection or measurement signal

Example:

```

/*PAL instance information */
ic_instance_t ic_pall_instance = { IC_INST_TYPE_FTM, 0U };

ic_input_ch_param_t icPalChnConfig[1] =
{
    {
        .hwChannelId      = 0U,
        .inputCaptureMode = IC_DETECT_RISING_EDGE,
        .filterEn         = false,
        .filterValue      = 0U,
        .channelExtension  = &ftmChnExtension0,
        .channelCallbackParams = NULL,
        .channelCallbacks  = ic_pall_channel_callBack0
    }
};

channel_extension_ftm_for_ic_t ftmChnExtension0 =
{
    .continuousModeEn = true
};

extension_ftm_for_ic_t ftmExtensionConfig =
{
    .ftmClockSource = FTM_CLOCK_SOURCE_SYSTEMCLK,
    .ftmPrescaler   = FTM_CLOCK_DIVID_BY_1
};

ic_config_t icPall_InitConfig =
{
    .numChannels = 1U,
    .inputChConfig = icPalChnConfig,
    .extension     = &ftmExtensionConfig
};

/* Initialize input capture mode */
IC_Init(&ic_pall_instance, &icPall_InitConfig);

```

De-initialize a input capture instance

This function will disable the input capture mode. The driver can't be used again until reinitialized. All register are reset to default value and counter is stopped.

Example:

```
/* De-initialize input capture mode */  
IC_Deinit(&ic_pall_instance);
```

Start the channel in the input capture mode

This function will set the channel is in the input capture mode.

Example:

```
uint8_t hwChannel = icPall_InitConfig.inputChConfig[0].hwChannelId;  
  
/* Start channel in the input capture mode */  
IC_StartChannel(&ic_pall_instance, hwChannel);
```

Stop the channel in the input capture mode

This function will set the channel is used in GPIO mode or other peripheral.

Example:

```
uint8_t hwChannel = icPall_InitConfig.inputChConfig[0].hwChannelId;  
  
/* Stop channel in the input capture mode */  
IC_StopChannel(&ic_pall_instance, hwChannel);
```

Get the measured value

The pulse width measurement and the period measurement can be made after the channel input is in the input capture mode. The value is last captured by count. Note that to get true value of measurement at the first of pulse, please use the IC_GetValueMeasurement function in interrupt.

Example:

```
uint16_t retResult = 0U;  
uint8_t hwChannel = icPall_InitConfig.inputChConfig[0].hwChannelId;  
  
/* Get the last captured value */  
retResult = IC_GetMeasurement(&ic_pall_instance, hwChannel);
```

Enable notifications on the channel

The notification is executed in the callback application with the IC_EVENT_MEASUREMENT_COMPLETE event which indicates that the measurement of input signal is completed.

Example:

```
uint8_t hwChannel = icPall_InitConfig.inputChConfig[0].hwChannelId;  
  
/* Enable the notification */  
IC_EnableNotification(&ic_pall_instance, hwChannel);
```

Disable notifications on the channel

The callback application will be not executed when the notification is disabled.

Example:

```
uint8_t hwChannel = icPall_InitConfig.inputChConfig[0].hwChannelId;  
  
/* Disable the notification */  
IC_DisableNotification(&ic_pall_instance, hwChannel);
```


Important Notes

- Before using the IC PAL driver the module clock must be configured. Refer to Clock Manager for clock configuration.
- The board specific configurations must be done prior to driver after that can call APIs.
- Some features are not available for all IC IPs and incorrect parameters will be handled by DEV_ASSERT.

Data Structures

- struct [ic_input_ch_param_t](#)
The configuration structure of input capture parameters for each channel. [More...](#)
- struct [ic_config_t](#)
Defines the configuration structures are used in the input capture mode. [More...](#)
- struct [channel_extension_ftm_for_ic_t](#)
Defines the extension structure for the channel configuration over FTM. [More...](#)
- struct [extension_ftm_for_ic_t](#)
Defines the extension structure for the input capture mode over FTM. [More...](#)
- struct [ic_pal_state_t](#)
The internal context structure. [More...](#)

Enumerations

- enum [ic_option_mode_t](#) {
[IC_DISABLE_OPERATION](#) = 0x00U, [IC_TIMESTAMP_RISING_EDGE](#) = 0x01U, [IC_TIMESTAMP_FALLING_EDGE](#) = 0x02U, [IC_TIMESTAMP_BOTH_EDGES](#) = 0x03U,
[IC_MEASURE_RISING_EDGE_PERIOD](#) = 0x04U, [IC_MEASURE_FALLING_EDGE_PERIOD](#) = 0x05U, [IC_MEASURE_PULSE_HIGH](#) = 0x06U, [IC_MEASURE_PULSE_LOW](#) = 0x07U }
The measurement type for input capture mode Implements : [ic_option_mode_t](#) Class.

Functions

- status_t [IC_Init](#) (const [ic_instance_t](#) *const instance, const [ic_config_t](#) *configPtr)
Initializes the input capture mode.
- status_t [IC_Deinit](#) (const [ic_instance_t](#) *const instance)
De-initialize a input capture instance.
- void [IC_StartChannel](#) (const [ic_instance_t](#) *const instance, uint8_t channel)
Start the counter.
- void [IC_StopChannel](#) (const [ic_instance_t](#) *const instance, uint8_t channel)
Stop the counter.
- status_t [IC_SetChannelMode](#) (const [ic_instance_t](#) *const instance, uint8_t channel, [ic_option_mode_t](#) channelMode)
Get the measured value.
- uint16_t [IC_GetMeasurement](#) (const [ic_instance_t](#) *const instance, uint8_t channel)
Get the measured value.
- void [IC_EnableNotification](#) (const [ic_instance_t](#) *const instance, uint8_t channel)
Enable channel notifications.
- void [IC_DisableNotification](#) (const [ic_instance_t](#) *const instance, uint8_t channel)
Disable channel notifications.

17.72.2 Data Structure Documentation

17.72.2.1 struct ic_input_ch_param_t

The configuration structure of input capture parameters for each channel.

Implements : ic_input_ch_param_t_Class

Definition at line 132 of file ic_pal.h.

Data Fields

- uint8_t [hwChannelId](#)
- [ic_option_mode_t](#) [inputCaptureMode](#)
- bool [filterEn](#)
- uint16_t [filterValue](#)
- void * [channelExtension](#)
- void * [channelCallbackParams](#)
- [ic_callback_t](#) [channelCallbacks](#)

Field Documentation

17.72.2.1.1 void* channelCallbackParams

The parameter of callback application for channels event

Definition at line 139 of file ic_pal.h.

17.72.2.1.2 ic_callback_t channelCallbacks

The callback function for channels event

Definition at line 140 of file ic_pal.h.

17.72.2.1.3 void* channelExtension

The IP specific configuration structure for channel

Definition at line 138 of file ic_pal.h.

17.72.2.1.4 bool filterEn

Input capture filter state

Definition at line 136 of file ic_pal.h.

17.72.2.1.5 uint16_t filterValue

Filter Value

Definition at line 137 of file ic_pal.h.

17.72.2.1.6 uint8_t hwChannelId

Physical hardware channel ID

Definition at line 134 of file ic_pal.h.

17.72.2.1.7 ic_option_mode_t inputCaptureMode

Input capture mode of operation

Definition at line 135 of file ic_pal.h.

17.72.2.2 struct ic_config_t

Defines the configuration structures are used in the input capture mode.

Implements : `ic_config_t_Class`

Definition at line 148 of file `ic_pal.h`.

Data Fields

- `uint8_t nNumChannels`
- `const ic_input_ch_param_t * inputChConfig`
- `void * extension`

Field Documentation**17.72.2.2.1 void* extension**

IP specific configuration structure

Definition at line 152 of file `ic_pal.h`.

17.72.2.2.2 const ic_input_ch_param_t* inputChConfig

Input capture channels configuration

Definition at line 151 of file `ic_pal.h`.

17.72.2.2.3 uint8_t nNumChannels

Number of input capture channel used

Definition at line 150 of file `ic_pal.h`.

17.72.2.3 struct channel_extension_ftm_for_ic_t

Defines the extension structure for the channel configuration over FTM.

Part of FTM channel configuration structure Implements : `channel_extension_ftm_for_ic_t_Class`

Definition at line 162 of file `ic_pal.h`.

Data Fields

- `bool continuousModeEn`

Field Documentation**17.72.2.3.1 bool continuousModeEn**

Continuous measurement state

Definition at line 164 of file `ic_pal.h`.

17.72.2.4 struct extension_ftm_for_ic_t

Defines the extension structure for the input capture mode over FTM.

Part of FTM configuration structure Implements : `extension_ftm_for_ic_t_Class`

Definition at line 173 of file `ic_pal.h`.

Data Fields

- `ftm_clock_source_t ftmClockSource`
- `ftm_clock_ps_t ftmPrescaler`

Field Documentation

17.72.2.4.1 `ftm_clock_source_t` `ftmClockSource`

Select clock source for FTM

Definition at line 175 of file `ic_pal.h`.

17.72.2.4.2 `ftm_clock_ps_t` `ftmPrescaler`

Register pre-scaler options available in the `ftm_clock_ps_t` enumeration

Definition at line 176 of file `ic_pal.h`.

17.72.2.5 `struct ic_pal_state_t`

The internal context structure.

This structure is used by the driver for its internal logic. It must be provided by the application through the [IC_Init\(\)](#) function, then it cannot be freed until the driver is de-initialized using [IC_Deinit\(\)](#). The application should make no assumptions about the content of this structure.

Definition at line 248 of file `ic_pal.h`.

17.72.3 Enumeration Type Documentation

17.72.3.1 `enum ic_option_mode_t`

The measurement type for input capture mode Implements : `ic_option_mode_t_Class`.

Enumerator

- `IC_DISABLE_OPERATION`** Have no operation
- `IC_TIMESTAMP_RISING_EDGE`** Rising edge trigger
- `IC_TIMESTAMP_FALLING_EDGE`** Falling edge trigger
- `IC_TIMESTAMP_BOTH_EDGES`** Rising and falling edge trigger
- `IC_MEASURE_RISING_EDGE_PERIOD`** Period measurement between two consecutive rising edges
- `IC_MEASURE_FALLING_EDGE_PERIOD`** Period measurement between two consecutive falling edges
- `IC_MEASURE_PULSE_HIGH`** The time measurement taken for the pulse to remain ON or HIGH state
- `IC_MEASURE_PULSE_LOW`** The time measurement taken for the pulse to remain OFF or LOW state

Definition at line 115 of file `ic_pal.h`.

17.72.4 Function Documentation

17.72.4.1 `status_t IC_Deinit (const ic_instance_t *const instance)`

De-initialize a input capture instance.

This function will disable the input capture mode. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

<code>in</code>	<code>instance</code>	The pointer to instance number structure.
-----------------	-----------------------	---

Returns

Operation status

- STATUS_SUCCESS: Operation was successful

Definition at line 1043 of file ic_pal.c.

17.72.4.2 void IC_DisableNotification (const ic_instance_t *const instance, uint8_t channel)

Disable channel notifications.

This function disables channel notification.

Parameters

in	instance	The pointer to instance number structure.
in	channel	The channel number.

Definition at line 1551 of file ic_pal.c.

17.72.4.3 void IC_EnableNotification (const ic_instance_t *const instance, uint8_t channel)

Enable channel notifications.

This function enables channel notification.

Parameters

in	instance	The pointer to instance number structure.
in	channel	The channel number.

Definition at line 1500 of file ic_pal.c.

17.72.4.4 uint16_t IC_GetMeasurement (const ic_instance_t *const instance, uint8_t channel)

Get the measured value.

This function will get the value of measured signal in ticks.

Parameters

in	instance	The pointer to instance number structure.
in	channel	The channel number.

Returns

The last value of measured signal in ticks.

Definition at line 1423 of file ic_pal.c.

17.72.4.5 status_t IC_Init (const ic_instance_t *const instance, const ic_config_t * configPtr)

Initializes the input capture mode.

This function will initialize the IC PAL instance, including the other platform specific HW units used together in the input capture mode. This function configures a group of channels in instance to detect or measure the input signal. : If the filter input is enabled on the channel 0,1,2 or 3 over FTM. The filter pre-scaler will be configured to divide by 4. The maximum frequency for the channel input to be detected correctly is FTM input clock divided by 16.

Parameters

in	instance	The pointer to instance number structure.
----	----------	---

<i>in</i>	<i>configPtr</i>	The pointer to configuration structure.
-----------	------------------	---

Returns

Operation status

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 971 of file ic_pal.c.

17.72.4.6 `status_t IC_SetChannelMode (const ic_instance_t *const instance, uint8_t channel, ic_option_mode_t channelMode)`

Get the measured value.

This function will get the value of measured signal in ticks.

Parameters

<i>in</i>	<i>instance</i>	The pointer to instance number structure.
<i>in</i>	<i>channel</i>	The channel number.

Returns

The last value of measured signal in ticks.

Definition at line 1297 of file ic_pal.c.

17.72.4.7 `void IC_StartChannel (const ic_instance_t *const instance, uint8_t channel)`

Start the counter.

This function start channel counting.

Parameters

<i>in</i>	<i>instance</i>	The pointer to instance number structure.
<i>in</i>	<i>channel</i>	The channel number.

Definition at line 1160 of file ic_pal.c.

17.72.4.8 `void IC_StopChannel (const ic_instance_t *const instance, uint8_t channel)`

Stop the counter.

This function stop channel counting.

Parameters

<i>in</i>	<i>instance</i>	The pointer to instance number structure.
<i>in</i>	<i>channel</i>	The channel number.

Definition at line 1232 of file ic_pal.c.

17.73 Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL)

17.73.1 Detailed Description

Inter Integrated Circuit- Peripheral Abstraction Layer.

The I2C PAL driver allows communication on an I2C bus. It was designed to be portable across all platforms and IPs which support I2C communication.

How to integrate I2C in your application

I2C PAL modules need to include a configuration file named `i2c_pal_cfg.h`, which allows the user to specify which IPs are used and how many resources are allocated for each of them (state structures). The following code example shows how to configure one instance for each available I2C IPs.

```
#ifndef I2C_PAL_cfg_H
#define I2C_PAL_cfg_H

/* Define which IP instance will be used in current project */
#define I2C_OVER_LPI2C
#define I2C_OVER_FLEXIO
#define I2C_OVER_I2C
#define I2C_OVER_SWI2C

/* Define the resources necessary for current project */
#define NO_OF_LPI2C_INSTS_FOR_I2C 2
#define NO_OF_FLEXIO_INSTS_FOR_I2C 1
#define NO_OF_I2C_INSTS_FOR_I2C 0
#define NO_OF_SWI2C_INSTS_FOR_I2C 1
#endif /* I2C_PAL_cfg_H */
```

The following table contains the matching between platforms and available IPs

IP/ M↔ CU	S32↔ K116	S32↔ K118	S32↔ K142	S32↔ K144	S32↔ K146	S32↔ K148	M↔ P↔ C5748 G	M↔ P↔ C5746 C	M↔ P↔ C5744 P	S32↔ R274	S32↔ R372	S32↔ K144↔ W	S32↔ K142↔ W
LP↔ I2C	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES
Flex↔ IO	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES
I2C	NO	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES	NO	Y↔ ES	Y↔ ES	NO	NO
S↔ W↔ I2C	NO	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES	Y↔ ES	NO	NO	NO	NO

In order to use the I2C driver it must be first initialized in either master or slave mode, using functions [I2C_Master↔Init\(\)](#) or [I2C_SlaveInit\(\)](#). Once initialized, it cannot be initialized again for the same I2C module instance until it is de-initialized, using [I2C_SlaveDeinit\(\)](#) or [I2C_MasterDeinit](#). Different I2C module instances can work independently of each other.

In each mode (master/slave) are available two types of transfers: blocking and non-blocking. The functions which initiate blocking transfers will configure the time out for transmission. If time expires the blocking functions will return `STATUS_TIMEOUT` and transmission will be aborted. The blocking functions are: `I2C_MasterSendDataBlocking`, `I2C_MasterReceiveDataBlocking`, `I2C_SlaveSendDataBlocking` and `I2C_SlaveReceiveDataBlocking`.

Slave Mode provides functions for transmitting or receiving data to/from any I2C master. There are two slave operating modes, selected by the field `slaveListening` in the slave configuration structure:

- Slave always listening: the slave interrupt is enabled at initialization time and the slave always listens to the line for a master addressing it. Any events are reported to the application through the callback function provided at initialization time.
- On-demand operation: the slave is commanded to transmit or receive data through the call of [I2C_Slave↔SendData\(\)](#) and [I2C_SlaveReceiveData\(\)](#) (or their blocking counterparts). The actual moment of the transfer

depends on the I2C master.

The configuration structure includes a special field named `extension`. It will be used only for I2C transfers over FLEXIO and should contain a pointer to `extension_flexio_for_i2c_t` structure. The purpose of this structure is to configure which FLEXIO pins are used by the applications and their functionality (SDA and SCL).

Important Notes

- The I2C transfers could be done using interrupts and DMA mode.
- FlexIO driver only supports master mode.
- The driver enables the interrupts for the corresponding module, but any interrupt priority setting must be done by the application.
- SWI2C driver supports only master mode.
- For send/receive blocking functions the timeout parameter is unused for SWI2C driver. The driver has a timeout independent of this parameter.
- The baud rate for SWI2C can reach a maximum value of 90Kbps.
- SWI2C baud rate depends on many parameters such as CPU frequency, compiler, optimizations and pull-up resistors. The `I2C_MasterSetBaudrate` is considering the maximum baud rate for swi2c device to be 90Kbps and it was tested using gcc compiler with -O1 optimizations, system clock of 200MHz and external pull-up resistors of 2KOhm each.
- Aborting a transfer with the function `I2C_MasterAbortTransferData()` can't be done safely due to device limitation; the user must ensure that the address is sent before aborting the transfer.

Example code

```

/* Configure I2C master */
i2c_master_t i2c1_MasterConfig0 =
{
    .slaveAddress      = 10,
    .is10bitAddr       = false,
    .baudRate          = 100000,
    .transferType       = I2C_PAL_USING_INTERRUPTS,
    .operatingMode      = I2C_PAL_STANDARD_MODE,
    .dmaChannel1        = 255,
    .dmaChannel2        = 255,
    .callback           = NULL,
    .callbackParam      = NULL,
    .extension          = NULL
};

/* Configure I2C slave */
i2c_slave_t i2c2_SlaveConfig0 =
{
    .slaveAddress      = 10,
    .is10bitAddr       = false,
    .slaveListening     = true,
    .transferType       = I2C_PAL_USING_INTERRUPTS,
    .dmaChannel         = 255,
    .callback           = i2c2_SlaveCallback0,
    .callbackParam      = NULL
};

i2c_instance_t i2c1_instance = {I2C_INST_TYPE_FLEXIO, 0U};
i2c_instance_t i2c2_instance = {I2C_INST_TYPE_LPI2C, 0U};
i2c_instance_t i2c3_instance = {I2C_INST_TYPE_LPI2C, 1U};

/* Callback for I2C slave */
void i2c2_SlaveCallback0(i2c_slave_event_t slaveEvent, void *userData)
{
    /* Get instance number from userData */
    i2c_instance_t * instance;
    instance = (i2c_instance_t *) userData;

    /* Check the event type:
     * - set RX or TX buffers depending on the master request type
     */
    if (slaveEvent == I2C_SLAVE_EVENT_RX_REQ)
        I2C_SlaveSetRxBuffer(instance, slaveRxBuffer, TRANSFER_SIZE);
}

```



```

    if (slaveEvent == I2C_SLAVE_EVENT_TX_REQ)
        I2C_SlaveSetTxBuffer(instance, slaveTxBuffer, TRANSFER_SIZE);
}

/* Configure FLEXIO pins routing */
extension_flexio_for_i2c_t extension;
extension.sclPin = 1;
extension.sdaPin = 0;
i2c1_MasterConfig0.extension = &extension;

/* Buffers */
uint8_t slaveTxBuffer[16] = {0x0, 0x1, 0x2, 0x3, 0x4, 0x5, 0x6, 0x7, 0x8, 0x9, 0xA, 0xB, 0xC, 0xD, 0xE,
0xF};
uint8_t slaveRxBuffer[16] = {0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0,
0x0};
uint8_t masterTxBuffer[16] = {0x0, 0x1, 0x2, 0x3, 0x4, 0x5, 0x6, 0x7, 0x8, 0x9, 0xA, 0xB, 0xC, 0xD, 0xE,
0xF};
uint8_t masterRxBuffer[16] = {0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0,
0x0};

/* Initializes I2C master for FlexIO */
I2C_MasterInit(&i2c1_instance, &i2c1_MasterConfig0);

/* Initialize I2C slave instance for LPI2C driver*/
I2C_SlaveInit(&i2c2_instance, &i2c2_SlaveConfig0);

/* FlexIO master sends masterTxBuffer to LPI2C0 configured as slave */
I2C_MasterSendDataBlocking(&i2c1_instance, masterTxBuffer, BUFFER_SIZE, true, 0
xFF);

/* Initialize I2C master for LPI2C1 instance */
I2C_MasterInit(&i2c3_instance, &i2c1_MasterConfig0);

/* LPI2C1 master sends data to LPI2C0 configured as slave */
I2C_MasterSendDataBlocking(&i2c3_instance, masterTxBuffer, BUFFER_SIZE, true, 0
xFF);

/* De-initialize I2C modules */
I2C_MasterDeinit(&i2c1_instance);
I2C_MasterDeinit(&i2c3_instance);
I2C_SlaveDeinit(&i2c2_instance);

```

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\pal\src\i2c\i2c_pal.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\pal\inc
i2c_pal_cfg.h path
```

Compile symbols

No special symbols are required for this component

Dependencies

i2c swi2c [Low Power Inter-Integrated Circuit \(LPI2C\)](#) flexio_i2c [Enhanced Direct Memory Access \(eDMA\)](#) OS Inter-
face (OSIF) [Clock manager](#) [Interrupt Manager \(Interrupt\)](#)

Data Structures

- struct [extension_flexio_for_i2c_t](#)
Defines the extension structure for the I2C over FLEXIO Implements : [extension_flexio_for_i2c_t](#) Class. [More...](#)
- struct [i2c_master_t](#)
Defines the configuration structure for I2C master Implements : [i2c_master_t](#) Class. [More...](#)

- struct [i2c_slave_t](#)

Defines the configuration structure for I2C slave Implements : [i2c_slave_t_Class](#). [More...](#)

Enumerations

- enum [i2c_pal_transfer_type_t](#) { [I2C_PAL_USING_DMA](#) = 0U, [I2C_PAL_USING_INTERRUPTS](#) = 1U }

Defines the mechanism to update the rx or tx buffers Implements : [i2c_pal_transfer_type_t_Class](#).

- enum [i2c_operating_mode_t](#) {
[I2C_PAL_STANDARD_MODE](#) = 0x0U, [I2C_PAL_FAST_MODE](#) = 0x1U, [I2C_PAL_FASTPLUS_MODE](#) = 0x2U, [I2C_PAL_HIGHSPEED_MODE](#) = 0x3U,
[I2C_PAL_ULTRAFast_MODE](#) = 0x4U }

Defines the operation mode of the i2c pal Implements : [i2c_operating_mode_t_Class](#).

Functions

- status_t [I2C_MasterInit](#) (const [i2c_instance_t](#) *const instance, const [i2c_master_t](#) *config)
Initializes the I2C module in master mode.
- status_t [I2C_MasterSendData](#) (const [i2c_instance_t](#) *const instance, const uint8_t *txBuff, uint32_t txSize, bool sendStop)
Perform a non-blocking send transaction on the I2C bus.
- status_t [I2C_MasterSendDataBlocking](#) (const [i2c_instance_t](#) *const instance, const uint8_t *txBuff, uint32_t txSize, bool sendStop, uint32_t timeout)
Perform a blocking send transaction on the I2C bus.
- status_t [I2C_MasterReceiveData](#) (const [i2c_instance_t](#) *const instance, uint8_t *rxBuff, uint32_t rxSize, bool sendStop)
Perform a non-blocking receive transaction on the I2C bus.
- status_t [I2C_MasterReceiveDataBlocking](#) (const [i2c_instance_t](#) *const instance, uint8_t *rxBuff, uint32_t rxSize, bool sendStop, uint32_t timeout)
Perform a blocking receive transaction on the I2C bus.
- status_t [I2C_MasterSetSlaveAddress](#) (const [i2c_instance_t](#) *const instance, const uint16_t address, const bool is10bitAddr)
Set the slave address for the I2C communication.
- status_t [I2C_MasterDeinit](#) (const [i2c_instance_t](#) *const instance)
De-initializes the I2C master module.
- status_t [I2C_GetDefaultMasterConfig](#) ([i2c_master_t](#) *config)
Gets the default configuration structure for master.
- status_t [I2C_GetDefaultSlaveConfig](#) ([i2c_slave_t](#) *config)
Gets the default configuration structure for slave.
- status_t [I2C_SlaveInit](#) (const [i2c_instance_t](#) *const instance, const [i2c_slave_t](#) *config)
Initializes the I2C module in slave mode.
- status_t [I2C_SlaveSendData](#) (const [i2c_instance_t](#) *const instance, const uint8_t *txBuff, uint32_t txSize)
Perform a non-blocking send transaction on the I2C bus.
- status_t [I2C_SlaveSendDataBlocking](#) (const [i2c_instance_t](#) *const instance, const uint8_t *txBuff, uint32_t txSize, uint32_t timeout)
Perform a blocking send transaction on the I2C bus.
- status_t [I2C_SlaveReceiveData](#) (const [i2c_instance_t](#) *const instance, uint8_t *rxBuff, uint32_t rxSize)
Perform a non-blocking receive transaction on the I2C bus.
- status_t [I2C_SlaveReceiveDataBlocking](#) (const [i2c_instance_t](#) *const instance, uint8_t *rxBuff, uint32_t rxSize, uint32_t timeout)
Perform a blocking receive transaction on the I2C bus.
- status_t [I2C_SlaveSetRxBuffer](#) (const [i2c_instance_t](#) *const instance, uint8_t *rxBuff, uint32_t rxSize)
Provide a buffer for receiving data.

- status_t [I2C_SlaveSetTxBuffer](#) (const [i2c_instance_t](#) *const instance, const uint8_t *txBuff, uint32_t txSize)
Provide a buffer for transmitting data.
- status_t [I2C_SlaveDeinit](#) (const [i2c_instance_t](#) *const instance)
De-initializes the i2c slave module.
- status_t [I2C_MasterGetTransferStatus](#) (const [i2c_instance_t](#) *const instance, uint32_t *bytesRemaining)
Return the current status of the I2C master transfer.
- status_t [I2C_SlaveGetTransferStatus](#) (const [i2c_instance_t](#) *const instance, uint32_t *bytesRemaining)
Return the current status of the I2C slave transfer.
- status_t [I2C_MasterSetBaudRate](#) (const [i2c_instance_t](#) *const instance, const [i2c_master_t](#) *config, uint32_t baudRate)
Set the master baud rate for the I2C communication.
- status_t [I2C_MasterGetBaudRate](#) (const [i2c_instance_t](#) *const instance, uint32_t *baudRate)
Get the master baud rate for the I2C communication.
- status_t [I2C_MasterAbortTransfer](#) (const [i2c_instance_t](#) *const instance)
Abort a non-blocking I2C Master transmission or reception.
- status_t [I2C_SlaveAbortTransfer](#) (const [i2c_instance_t](#) *const instance)
Abort a non-blocking I2C slave transmission or reception.

17.73.2 Data Structure Documentation

17.73.2.1 struct extension_flexio_for_i2c_t

Defines the extension structure for the I2C over FLEXIO Implements : [extension_flexio_for_i2c_t_Class](#).

Definition at line 62 of file [i2c_pal.h](#).

Data Fields

- uint8_t [sclPin](#)
- uint8_t [sdaPin](#)

Field Documentation

17.73.2.1.1 uint8_t sclPin

FlexIO pin for SCL

Definition at line 64 of file [i2c_pal.h](#).

17.73.2.1.2 uint8_t sdaPin

FlexIO pin for SDA

Definition at line 65 of file [i2c_pal.h](#).

17.73.2.2 struct i2c_master_t

Defines the configuration structure for I2C master Implements : [i2c_master_t_Class](#).

Definition at line 101 of file [i2c_pal.h](#).

Data Fields

- uint16_t [slaveAddress](#)
- bool [is10bitAddr](#)
- uint32_t [baudRate](#)
- uint8_t [dmaChannel1](#)
- uint8_t [dmaChannel2](#)

- [i2c_pal_transfer_type_t](#) transferType
- [i2c_operating_mode_t](#) operatingMode
- [i2c_master_callback_t](#) callback
- void * [callbackParam](#)
- void * [extension](#)

Field Documentation

17.73.2.2.1 uint32_t baudRate

Baud rate in hertz

Definition at line 105 of file [i2c_pal.h](#).

17.73.2.2.2 i2c_master_callback_t callback

User callback function. Note that this function will be called from the interrupt service routine, so its execution time should be as small as possible. It can be NULL if it is not needed

Definition at line 111 of file [i2c_pal.h](#).

17.73.2.2.3 void* callbackParam

Parameter for the callback function

Definition at line 115 of file [i2c_pal.h](#).

17.73.2.2.4 uint8_t dmaChannel1

DMA channel number. Only used in DMA mode

Definition at line 106 of file [i2c_pal.h](#).

17.73.2.2.5 uint8_t dmaChannel2

DMA channel used only by FlexIO I2C which needs two DMA channels, one for receiving and one for transmitting.

Definition at line 107 of file [i2c_pal.h](#).

17.73.2.2.6 void* extension

This field will be used to add extra settings to the basic configuration like FlexIO pins

Definition at line 116 of file [i2c_pal.h](#).

17.73.2.2.7 bool is10bitAddr

Selects 7-bit or 10-bit slave address

Definition at line 104 of file [i2c_pal.h](#).

17.73.2.2.8 i2c_operating_mode_t operatingMode

I2C Operating mode

Definition at line 110 of file [i2c_pal.h](#).

17.73.2.2.9 uint16_t slaveAddress

Slave address, 7-bit or 10-bit

Definition at line 103 of file [i2c_pal.h](#).

17.73.2.2.10 i2c_pal_transfer_type_t transferType

Type of I2C transfer (interrupts or DMA)

Definition at line 109 of file i2c_pal.h.

17.73.2.3 struct i2c_slave_t

Defines the configuration structure for I2C slave Implements : i2c_slave_t_Class.

Definition at line 124 of file i2c_pal.h.

Data Fields

- uint16_t [slaveAddress](#)
- bool [is10bitAddr](#)
- bool [slaveListening](#)
- [i2c_operating_mode_t](#) [operatingMode](#)
- [i2c_pal_transfer_type_t](#) [transferType](#)
- uint8_t [dmaChannel](#)
- [i2c_slave_callback_t](#) [callback](#)
- void * [callbackParam](#)

Field Documentation

17.73.2.3.1 i2c_slave_callback_t callback

Callback function.

Definition at line 133 of file i2c_pal.h.

17.73.2.3.2 void* callbackParam

Parameter for the slave callback function

Definition at line 134 of file i2c_pal.h.

17.73.2.3.3 uint8_t dmaChannel

Channel number for DMA channel. If DMA mode is not supported or is not used this field will be ignored.

Definition at line 131 of file i2c_pal.h.

17.73.2.3.4 bool is10bitAddr

Selects 7-bit or 10-bit slave address

Definition at line 127 of file i2c_pal.h.

17.73.2.3.5 i2c_operating_mode_t operatingMode

I2C Operating mode

Definition at line 129 of file i2c_pal.h.

17.73.2.3.6 uint16_t slaveAddress

Slave address, 7-bit or 10-bit

Definition at line 126 of file i2c_pal.h.

17.73.2.3.7 bool slaveListening

Slave mode (always listening or on demand only)

Definition at line 128 of file i2c_pal.h.

17.73.2.3.8 i2c_pal_transfer_type_t transferType

Type of the I2C transfer

Definition at line 130 of file i2c_pal.h.

17.73.3 Enumeration Type Documentation

17.73.3.1 enum i2c_operating_mode_t

Defines the operation mode of the i2c pal Implements : i2c_operating_mode_t_Class.

Enumerator

I2C_PAL_STANDARD_MODE Standard-mode (Sm), bidirectional data transfers up to 100 kbit/s

I2C_PAL_FAST_MODE Fast-mode (Fm), bidirectional data transfers up to 400 kbit/s

I2C_PAL_FASTPLUS_MODE Fast-mode Plus (Fm+), bidirectional data transfers up to 1 Mbit/s

I2C_PAL_HIGHSPEED_MODE High-speed Mode (Hs-mode), bidirectional data transfers up to 3.4 Mbit/s

I2C_PAL_ULTRAFAST_MODE Ultra Fast Mode (UFm), unidirectional data transfers up to 5 Mbit/s

Definition at line 87 of file i2c_pal.h.

17.73.3.2 enum i2c_pal_transfer_type_t

Defines the mechanism to update the rx or tx buffers Implements : i2c_pal_transfer_type_t_Class.

Enumerator

I2C_PAL_USING_DMA The driver will use DMA to perform I2C transfer

I2C_PAL_USING_INTERRUPTS The driver will use interrupts to perform I2C transfer

Definition at line 52 of file i2c_pal.h.

17.73.4 Function Documentation

17.73.4.1 status_t I2C_GetDefaultMasterConfig (i2c_master_t * config)

Gets the default configuration structure for master.

The default configuration structure is:

Parameters

out	config	Pointer to configuration structure
-----	--------	------------------------------------

Returns

Error or success status returned by API

Definition at line 876 of file i2c_pal.c.

17.73.4.2 status_t I2C_GetDefaultSlaveConfig (i2c_slave_t * config)

Gets the default configuration structure for slave.

The default configuration structure is:

Parameters

out	config	Pointer to configuration structure
-----	--------	------------------------------------

Returns

Error or success status returned by API

17.73.4.3 status_t I2C_MasterAbortTransfer (const i2c_instance_t *const instance)

Abort a non-blocking I2C Master transmission or reception.

Parameters

instance	I2C peripheral instance number
----------	--------------------------------

Returns

Error or success status returned by API

Definition at line 1372 of file i2c_pal.c.

17.73.4.4 status_t I2C_MasterDeinit (const i2c_instance_t *const instance)

De-initializes the I2C master module.

This function de-initialized the I2C master module.

Parameters

in	instance	The name of the instance
----	----------	--------------------------

Returns

Error or success status returned by API

Definition at line 635 of file i2c_pal.c.

17.73.4.5 status_t I2C_MasterGetBaudRate (const i2c_instance_t *const instance, uint32_t * baudRate)

Get the master baud rate for the I2C communication.

This function returns the master baud rate of the I2C master module.

Parameters

instance	I2C peripheral instance number
----------	--------------------------------

Returns

the baud rate in Hz

Definition at line 821 of file i2c_pal.c.

17.73.4.6 status_t I2C_MasterGetTransferStatus (const i2c_instance_t *const instance, uint32_t * bytesRemaining)

Return the current status of the I2C master transfer.

This function can be called during a non-blocking transmission to check the status of the transfer.

Parameters

<i>instance</i>	I2C peripheral instance number
<i>bytesRemaining</i>	the number of remaining bytes in the active I2C transfer

Returns

Error or success status returned by API

Definition at line 1267 of file i2c_pal.c.

17.73.4.7 `status_t I2C_MasterInit (const i2c_instance_t *const instance, const i2c_master_t * config)`

Initializes the I2C module in master mode.

This function initializes and enables the requested I2C module in master mode, configuring the bus parameters.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance
<i>in</i>	<i>config</i>	The configuration structure

Returns

Error or success status returned by API

Definition at line 210 of file i2c_pal.c.

17.73.4.8 `status_t I2C_MasterReceiveData (const i2c_instance_t *const instance, uint8_t * rxBuff, uint32_t rxSize, bool sendStop)`

Perform a non-blocking receive transaction on the I2C bus.

This function starts the reception of a block of data from the currently configured slave address and returns immediately. The rest of the reception is handled by the interrupt service routine.

Parameters

<i>instance</i>	The name of the instance
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred
<i>sendStop</i>	specifies whether or not to generate stop condition after the reception

Returns

Error or success status returned by API

Definition at line 533 of file i2c_pal.c.

17.73.4.9 `status_t I2C_MasterReceiveDataBlocking (const i2c_instance_t *const instance, uint8_t * rxBuff, uint32_t rxSize, bool sendStop, uint32_t timeout)`

Perform a blocking receive transaction on the I2C bus.

This function receives a block of data from the currently configured slave address, and only returns when the transmission is complete.

Parameters

<i>instance</i>	The name of the instance
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred
<i>sendStop</i>	specifies whether or not to generate stop condition after the reception
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 585 of file i2c_pal.c.

17.73.4.10 `status_t I2C_MasterSendData (const i2c_instance_t *const instance, const uint8_t * txBuff, uint32_t txSize, bool sendStop)`

Perform a non-blocking send transaction on the I2C bus.

This function starts the transmission of a block of data to the currently configured slave address and returns immediately. The rest of the transmission is handled by the interrupt service routine.

Parameters

<i>instance</i>	The name of the instance
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred
<i>sendStop</i>	specifies whether or not to generate stop condition after the transmission

Returns

Error or success status returned by API

Definition at line 422 of file i2c_pal.c.

17.73.4.11 `status_t I2C_MasterSendDataBlocking (const i2c_instance_t *const instance, const uint8_t * txBuff, uint32_t txSize, bool sendStop, uint32_t timeout)`

Perform a blocking send transaction on the I2C bus.

This function sends a block of data to the currently configured slave address, and only returns when the transmission is complete.

Parameters

<i>instance</i>	The name of the instance
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred
<i>sendStop</i>	specifies whether or not to generate stop condition after the transmission
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 479 of file i2c_pal.c.

17.73.4.12 `status_t I2C_MasterSetBaudRate (const i2c_instance_t *const instance, const i2c_master_t * config, uint32_t baudRate)`

Set the master baud rate for the I2C communication.

This function sets the master baud rate of the I2C master module.

Parameters

<i>instance</i>	I2C peripheral instance number
<i>baudRate</i>	the desired baud rate in Hz

Definition at line 742 of file i2c_pal.c.

17.73.4.13 `status_t I2C_MasterSetSlaveAddress (const i2c_instance_t *const instance, const uint16_t address, const bool is10bitAddr)`

Set the slave address for the I2C communication.

This function sets the slave address which will be used for any future transfer initiated by the I2C master.

Parameters

<i>instance</i>	I2C peripheral instance number
<i>address</i>	slave 7-bit or 10-bit address

Definition at line 689 of file i2c_pal.c.

17.73.4.14 `status_t I2C_SlaveAbortTransfer (const i2c_instance_t *const instance)`

Abort a non-blocking I2C slave transmission or reception.

Parameters

<i>instance</i>	I2C peripheral instance number
-----------------	--------------------------------

Returns

Error or success status returned by API

Definition at line 1425 of file i2c_pal.c.

17.73.4.15 `status_t I2C_SlaveDeinit (const i2c_instance_t *const instance)`

De-initializes the i2c slave module.

This function de-initialized the i2c slave module.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance
-----------	-----------------	--------------------------

Returns

Error or success status returned by API

Definition at line 1224 of file i2c_pal.c.

17.73.4.16 `status_t I2C_SlaveGetTransferStatus (const i2c_instance_t *const instance, uint32_t * bytesRemaining)`

Return the current status of the I2C slave transfer.

This function can be called during a non-blocking transmission to check the status of the transfer.

Parameters

<i>instance</i>	I2C peripheral instance number
<i>bytesRemaining</i>	the number of remaining bytes in the active I2C transfer

Returns

Error or success status returned by API

Definition at line 1324 of file i2c_pal.c.

17.73.4.17 `status_t I2C_SlaveInit (const i2c_instance_t *const instance, const i2c_slave_t * config)`

Initializes the I2C module in slave mode.

This function initializes and enables the requested I2C module in slave mode, configuring the bus parameters.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance
<i>in</i>	<i>config</i>	The configuration structure

Returns

Error or success status returned by API

Definition at line 350 of file i2c_pal.c.

17.73.4.18 `status_t I2C_SlaveReceiveData (const i2c_instance_t *const instance, uint8_t * rxBuff, uint32_t rxSize)`

Perform a non-blocking receive transaction on the I2C bus.

Performs a non-blocking receive transaction on the I2C bus when the slave is not in listening mode (initialized with slaveListening = false). It starts the reception and returns immediately. The rest of the reception is handled by the interrupt service routine.

Parameters

<i>instance</i>	The name of the instance
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 1024 of file i2c_pal.c.

17.73.4.19 `status_t I2C_SlaveReceiveDataBlocking (const i2c_instance_t *const instance, uint8_t * rxBuff, uint32_t rxSize, uint32_t timeout)`

Perform a blocking receive transaction on the I2C bus.

Performs a blocking receive transaction on the I2C bus when the slave is not in listening mode (initialized with slaveListening = false). It sets up the reception and then waits for the transfer to complete before returning.

Parameters

<i>instance</i>	The name of the instance
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 1074 of file i2c_pal.c.

17.73.4.20 `status_t I2C_SlaveSendData (const i2c_instance_t *const instance, const uint8_t * txBuff, uint32_t txSize)`

Perform a non-blocking send transaction on the I2C bus.

Performs a non-blocking send transaction on the I2C bus when the slave is not in listening mode (initialized with slaveListening = false). It starts the transmission and returns immediately. The rest of the transmission is handled by the interrupt service routine.

Parameters

<i>instance</i>	The name of the instance
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 924 of file i2c_pal.c.

17.73.4.21 `status_t I2C_SlaveSendDataBlocking (const i2c_instance_t *const instance, const uint8_t * txBuff, uint32_t txSize, uint32_t timeout)`

Perform a blocking send transaction on the I2C bus.

Performs a blocking send transaction on the I2C bus when the slave is not in listening mode (initialized with slave↔ Listening = false). It sets up the transmission and then waits for the transfer to complete before returning.

Parameters

<i>instance</i>	The name of the instance
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 973 of file i2c_pal.c.

17.73.4.22 `status_t I2C_SlaveSetRxBuffer (const i2c_instance_t *const instance, uint8_t * rxBuff, uint32_t rxSize)`

Provide a buffer for receiving data.

This function provides a buffer in which the I2C slave-mode driver can store received data. It can be called for example from the user callback provided at initialization time, when the driver reports events I2C_SLAVE_EVENT↔ T_RX_REQ or I2C_SLAVE_EVENT_RX_FULL.

Parameters

<i>instance</i>	I2C peripheral instance number
<i>rxBuff</i>	pointer to the data to be transferred
<i>rxSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 1126 of file i2c_pal.c.

17.73.4.23 `status_t I2C_SlaveSetTxBuffer (const i2c_instance_t *const instance, const uint8_t * txBuff, uint32_t txSize)`

Provide a buffer for transmitting data.

This function provides a buffer from which the I2C slave-mode driver can transmit data. It can be called for example from the user callback provided at initialization time, when the driver reports events I2C_SLAVE_EVENT_TX_REQ↔ or I2C_SLAVE_EVENT_TX_EMPTY.

Parameters

<i>instance</i>	I2C peripheral instance number
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 1174 of file i2c_pal.c.

17.74 Interface management

17.74.1 Detailed Description

This group contains APIs that help users manage interface(s) in LIN node.

Functions

- `I_bool I_ifc_init (I_ifc_handle iii)`
Initialize the controller specified by name, i.e. sets up internal functions such as the baud rate. The default schedule set by the `I_ifc_init` call will be the `L_NULL_SCHEDULE` where no frames will be sent and received. This is the first call a user must perform, before using any other interface related LIN API functions. The function returns zero if the initialization was successful and non-zero if failed.
- `void I_ifc_goto_sleep (I_ifc_handle iii)`
Request slave nodes on the cluster connected to the interface to enter bus sleep mode by issuing one go to sleep command. This API is available only for Master nodes.
- `void I_ifc_wake_up (I_ifc_handle iii)`
Transmit the wake up signal.
- `I_u16 I_ifc_read_status (I_ifc_handle iii)`
This function will return the status of the previous communication.

17.74.2 Function Documentation

17.74.2.1 void I_ifc_goto_sleep (I_ifc_handle iii)

Request slave nodes on the cluster connected to the interface to enter bus sleep mode by issuing one go to sleep command. This API is available only for Master nodes.

Note

After sending go to sleep command successfully, the master node sets go to sleep flag to 1 and goes to sleep mode. At the end of Go to sleep schedule table, at the end of frame slot of go to sleep command, in `I_sch_tick()` the master node actually switches its active schedule table to Null to stop all communication. To start LIN communication, the master node shall call `I_ifc_wake_up()` to wake up LIN cluster and `I_sch_set()` to activate normal schedule table.

Parameters

<code>in</code>	<code>iii</code>	Interface name
-----------------	------------------	----------------

Returns

void

Definition at line 376 of file `lin_common_api.c`.

17.74.2.2 I_bool I_ifc_init (I_ifc_handle iii)

Initialize the controller specified by name, i.e. sets up internal functions such as the baud rate. The default schedule set by the `I_ifc_init` call will be the `L_NULL_SCHEDULE` where no frames will be sent and received. This is the first call a user must perform, before using any other interface related LIN API functions. The function returns zero if the initialization was successful and non-zero if failed.

Parameters

<i>in</i>	<i>iii</i>	Interface name
-----------	------------	----------------

Returns

Operation status

- Zero: Initialization was successful.
- Non-zero: Initialization failed.

Definition at line 405 of file lin_common_api.c.

17.74.2.3 I_u16 I_ifc_read_status (I_ifc_handle *iii*)

This function will return the status of the previous communication.

Parameters

<i>in</i>	<i>iii</i>	Interface name
-----------	------------	----------------

Returns

I_u16

Definition at line 469 of file lin_common_api.c.

17.74.2.4 void I_ifc_wake_up (I_ifc_handle *iii*)

Transmit the wake up signal.

Parameters

<i>in</i>	<i>iii</i>	Interface name
-----------	------------	----------------

Returns

void

Definition at line 455 of file lin_common_api.c.

17.75 Interrupt Manager (Interrupt)

17.75.1 Detailed Description

The S32 SDK Interrupt Manager provides a set of API/services to configure the Interrupt Controller (NVIC).

The Nested-Vectored Interrupt Controller (NVIC) module implements a relocatable vector table supporting many external interrupts, a single non-maskable interrupt (NMI), and priority levels. The NVIC contains the address of the function to execute for a particular handler. The address is fetched via the instruction port allowing parallel register stacking and look-up. The first sixteen entries are allocated to internal sources with the others mapping to MCU-defined interrupts.

Overview

The Interrupt Manager provides a set of APIs so that the application can enable or disable an interrupt for a specific device and also set priority, and other features. Additionally, it provides a way to update the vector table for a specific device interrupt handler.

Interrupt Names

Each chip has its own set of supported interrupt names defined in the chip-specific header file (see `IRQn_Type`).

This is an example to enable/disable an interrupt for the `ADC0_IRQn`:

```
#include "interrupt_manager.h"

INT_SYS_EnableIRQ(ADC0_IRQn);
INT_SYS_DisableIRQ(ADC0_IRQn);
```

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\interrupt\interrupt_manager.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

This component does not have any dependencies.

Note

1. When the vector table is not in ram (**flash_vector_table = 1**):
 - `INT_SYS_InstallHandler` shall check if the function pointer provided as parameter for the new handler is already present in the vector table for the given IRQ number.
 - The user will be required to manually add the correct handlers in the startup files

Typedefs

- typedef void(* [isr_t](#)) (void)
Interrupt handler type.

Functions

- void [DefaultISR](#) (void)
Default ISR.

Interrupt manager APIs

- void [INT_SYS_InstallHandler](#) (IRQn_Type irqNumber, const [isr_t](#) newHandler, [isr_t](#) *const oldHandler)
Installs an interrupt handler routine for a given IRQ number.
- void [INT_SYS_EnableIRQ](#) (IRQn_Type irqNumber)
Enables an interrupt for a given IRQ number.
- void [INT_SYS_DisableIRQ](#) (IRQn_Type irqNumber)
Disables an interrupt for a given IRQ number.
- void [INT_SYS_EnableIRQGlobal](#) (void)
Enables system interrupt.
- void [INT_SYS_DisableIRQGlobal](#) (void)
Disable system interrupt.
- void [INT_SYS_SetPriority](#) (IRQn_Type irqNumber, uint8_t priority)
Set Interrupt Priority.
- uint8_t [INT_SYS_GetPriority](#) (IRQn_Type irqNumber)
Get Interrupt Priority.

17.75.2 Typedef Documentation

17.75.2.1 typedef void(* [isr_t](#)) (void)

Interrupt handler type.

Definition at line 76 of file interrupt_manager.h.

17.75.3 Function Documentation

17.75.3.1 void [DefaultISR](#) (void)

Default ISR.

17.75.3.2 void [INT_SYS_DisableIRQ](#) (IRQn_Type *irqNumber*)

Disables an interrupt for a given IRQ number.

This function disables the individual interrupt for a specified IRQ number.

Parameters

<i>irqNumber</i>	IRQ number
------------------	------------

Definition at line 219 of file interrupt_manager.c.

17.75.3.3 void INT_SYS_DisableIRQGlobal (void)

Disable system interrupt.

This function disables the global interrupt by calling the core API.

Definition at line 271 of file interrupt_manager.c.

17.75.3.4 void INT_SYS_EnableIRQ (IRQn_Type irqNumber)

Enables an interrupt for a given IRQ number.

This function enables the individual interrupt for a specified IRQ number.

Parameters

<i>irqNumber</i>	IRQ number
------------------	------------

Definition at line 190 of file interrupt_manager.c.

17.75.3.5 void INT_SYS_EnableIRQGlobal (void)

Enables system interrupt.

This function enables the global interrupt by calling the core API.

Definition at line 248 of file interrupt_manager.c.

17.75.3.6 uint8_t INT_SYS_GetPriority (IRQn_Type irqNumber)

Get Interrupt Priority.

The function gets the priority of an interrupt.

Parameters

<i>irqNumber</i>	Interrupt number.
------------------	-------------------

Returns

priority Priority of the interrupt.

Definition at line 354 of file interrupt_manager.c.

17.75.3.7 void INT_SYS_InstallHandler (IRQn_Type irqNumber, const isr_t newHandler, isr_t *const oldHandler)

Installs an interrupt handler routine for a given IRQ number.

This function lets the application register/replace the interrupt handler for a specified IRQ number. See a chip-specific reference manual for details and the startup_<SoC>.s file for each chip family to find out the default interrupt handler for each device.

Note

This method is applicable only if interrupt vector is copied in RAM.

Parameters

<i>irqNumber</i>	IRQ number
<i>newHandler</i>	New interrupt handler routine address pointer
<i>oldHandler</i>	Pointer to a location to store current interrupt handler

Definition at line 114 of file interrupt_manager.c.

17.75.3.8 void INT_SYS_SetPriority (IRQn_Type irqNumber, uint8_t priority)

Set Interrupt Priority.

The function sets the priority of an interrupt.

Parameters

<i>irqNumber</i>	Interrupt number.
<i>priority</i>	Priority to set.

Definition at line 289 of file interrupt_manager.c.

17.76 Interrupt vector numbers for S32K148

This module covers interrupt number allocation.

17.77 J2602 Specific API

J2602 protocol is LIN 2.0 based. It contains LIN 2.0's modules to support Signal management, network management, scheduler and J2602 status management. The goal of J2602 is to improve the interoperability and interchangeability of LIN devices within a network by resolving those LIN2.0 requirements that are ambiguous, conflicting, or optional. Moreover, J2602 provides additional requirements that are not present in LIN2.0. For example: fault tolerant, operation, network topology, etc. Different to LIN2.1 protocol, J2602 does not support sporadic and event trigger frames in communication.

17.78 J2602 Transport Layer specific API

17.78.1 Detailed Description

Contains Transport Layer APIs that only used for J2602 protocol.

Modules

- [Node configuration](#)

This group contains APIs that used for node configuration purpose.

17.79 LIN 2.1 Specific API

17.79.1 Detailed Description

LIN 2.1 is extended from in LIN 2.0 specification through diagnostic services and few functions were removed as obsolete.

1. LIN 2.1 is compatible with LIN 2.0:

- A LIN 2.1 master node may handle a LIN 2.0 slave node if the master node also contains all functionality of a LIN 2.0 master node, e.g. obsolete functions like Assign frame Id.
- A LIN 2.1 slave node can be used in a cluster with a LIN 2.0 master node if the LIN 2.1 slave node is pre-configured, i.e. the LIN 2.1 slave node has a valid configuration after reset.

2. Changes between LIN 2.0 and LIN 2.1:

- LIN2.1 enhance the capacity of LIN2.0 on event-triggered frame collision handling and diagnostic services supported. Besides, several features are added to fulfill powerful capacity of LIN network such as configuration service, assign frame ID range configuration, etc.

Functions

- void [lin_collision_resolve](#) ([l_ifc_handle](#) *iii*, [l_u8](#) *pid*)
Switch to collision resolve table.
- void [lin_update_word_status_lin21](#) ([l_ifc_handle](#) *iii*, [lin_lld_event_id_t](#) *event_id*)
Update node status flags.
- void [lin_update_err_signal](#) ([l_ifc_handle](#) *iii*, [l_u8](#) *frm_id*)
Update error signal.
- void [lin_make_res_evnt_frame](#) ([l_ifc_handle](#) *iii*, [l_u8](#) *pid*)
This function packs signals associated with event trigger frame into buffer.
- void [lin_update_rx_evnt_frame](#) ([l_ifc_handle](#) *iii*, [l_u8](#) *pid*)
The function updates the receive flags associated with signals/frames in case receive an event trigger frame.

17.79.2 Function Documentation

17.79.2.1 void [lin_collision_resolve](#) ([l_ifc_handle](#) *iii*, [l_u8](#) *pid*)

Switch to collision resolve table.

Parameters

in	iii	Interface name
in	pid	PID to process

Returns

void

Definition at line 32 of file [lin_lin21_proto.c](#).

17.79.2.2 void [lin_make_res_evnt_frame](#) ([l_ifc_handle](#) *iii*, [l_u8](#) *pid*)

This function packs signals associated with event trigger frame into buffer.

Parameters

in	<i>iii</i>	Interface name
in	<i>pid</i>	PID to process

Returns

void

Definition at line 221 of file lin_lin21_proto.c.

17.79.2.3 void lin_update_err_signal (I_ifc_handle *iii*, I_u8 *frm_id*)

Update error signal.

Parameters

in	<i>iii</i>	Interface name
in	<i>frm_id</i>	Frame index

Returns

void

Definition at line 147 of file lin_lin21_proto.c.

17.79.2.4 void lin_update_rx_evt_frame (I_ifc_handle *iii*, I_u8 *pid*)

The function updates the receive flags associated with signals/frames in case receive an event trigger frame.

Parameters

in	<i>iii</i>	Interface name
in	<i>pid</i>	PID to process

Returns

void

Definition at line 184 of file lin_lin21_proto.c.

17.79.2.5 void lin_update_word_status_lin21 (I_ifc_handle *iii*, lin_lld_event_id_t *event_id*)

Update node status flags.

Parameters

in	<i>iii</i>	Interface name
in	<i>event_id</i>	Event id

Returns

void

Definition at line 67 of file lin_lin21_proto.c.

17.80 LIN Core API

17.80.1 Detailed Description

The LIN core API handles initialization, processing and a signal based interaction between the application and the LIN core. Refer to chapter 7, LIN 2.2A specification.

- Core API layer consists of API functions as defined by the LIN2.1/J2602 specifications.
- Enabling the user to utilize the LIN2.1/J2602 communication within the user application.
- Both the static and dynamic modes for calling the API functions are supported.
- The core API layer interacts with the low level layer and can be called by such upper layers as LIN2.1 TL API, LIN TL J2602 or application for diagnostic implementation.

Modules

- [Common Core API.](#)
- [J2602 Specific API](#)
- [LIN 2.1 Specific API](#)

17.81 LIN Driver

17.81.1 Detailed Description

This section describes the programming interface of the Peripheral driver for LIN.

17.81.2 LIN Driver Overview

The LIN (Local Interconnect Network) Driver is an use-case driven High Level Peripheral Driver. The driver provides users important key features. NXP provides LIN Stack as a middleware software package that is developed on LIN driver. Users also can create their own LIN applications and LIN stack that are compatible with LIN Specification. In this release package, LIN Driver is built on LPUART interface.

17.81.3 LIN Driver Device structures

The driver uses instantiations of the [lin_state_t](#) to maintain the current state of a particular LIN Hardware instance module driver.

The user is required to provide memory for the driver state structures during the initialization. The driver itself does not statically allocate memory.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\lin\lin_common.c  
${S32SDK_PATH}\platform\drivers\src\lin\lin_driver.c  
${S32SDK_PATH}\platform\drivers\src\lin\lin_irq.c  
${S32SDK_PATH}\platform\drivers\src\lpuart\lin_lpuart_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc\  
${S32SDK_PATH}\platform\drivers\src\lpuart\
```

Compile symbols

No special symbols are required for this component

Dependencies

- [Clock Manager](#)
- [Interrupt Manager \(Interrupt\)](#)
- [OS Interface \(OSIF\)](#)
- [Low Power Universal Asynchronous Receiver-Transmitter \(LPUART\)](#)

17.81.4 LIN Driver Initialization

1. To initialize the LIN driver, call the `LIN_DRV_Init()` function and pass the instance number of the relevant LIN hardware interface instance which is LPUART instance in this release.
For example: to use LPUART0 pass value 0 to the initialization function.

2. Pass a user configuration structure `lin_user_config_t` as shown here:

```
/* LIN Driver configuration structure */
typedef struct {
    uint32_t baudRate;
    bool nodeFunction;
    bool autobaudEnable;
    lin_timer_get_time_interval_t timerGetTimeIntervalCallback;
} lin_user_config_t;
```

3. For LIN, typically the user configures the `lin_user_config_t` instantiation with a baudrate from 1000bps to 20000bps.
-E.g. 19200 bps `linUserConfig.baudRate = 19200U`.
4. Node function can be MASTER or SLAVE.
-E.g. `linUserConfig.nodeFunction = MASTER`
5. If users do not want to use Autobaud feature, then just configure `linUserConfig.autobaudEnable = FALSE`.
6. Users shall assign measurement callback function pointer that is `timerGetTimeIntervalCallback`. This function must return time period between two consecutive calls in nano seconds with accuracy at least 0.1 microsecond and if this function is called for the first time, it will start the timer to measure time. When an event (such as detecting a falling edge of a dominant signal while node is in sleep mode) occurs, LIN driver will call `timerGetTimeIntervalCallback` to start time measurement. Then on rising edge of that signal, LIN driver will call `timerGetTimeIntervalCallback` function to get time interval of that dominant signal in nano seconds. If Autobaud feature is enabled, LIN driver uses `timerGetTimeIntervalCallback` to measure two bit time length between two consecutive falling edges of the sync byte in order to evaluate Master's baudrate. Users can implement this function in their applications. -E.g. `linUserConfig.timerGetTimeIntervalCallback = timerGetTimeIntervalCallback0`; This is a code example to set up a FTM0 for LIN Driver:

```
/* Global variables */
uint16_t timerCounterValue[2] = {0u};
uint16_t timerOverflowInterruptCount = 0u;

/* Callback function to get time interval in nano seconds */
uint32_t timerGetTimeIntervalCallback0(uint32_t *ns)
{
    timerCounterValue[1] = (uint16_t) (ftmBase->CNT);
    *ns = ((uint32_t) (timerCounterValue[1] + timerOverflowInterruptCount*65536u - timerCounterValue[0]))*1000 / TIMER_1US;
    timerOverflowInterruptCount = 0U;
    timerCounterValue[0] = timerCounterValue[1];
    return 0U;
}
```

7. This is a code example to set up a user LIN Driver configuration instantiation:

```
/* Device instance number as LPUART instance*/
#define LIO (0U)

lin_state_t linState;
lin_user_config_t linUserConfig;
/* Set baudrate 19200 bps */
linUserConfig.baudRate = 19200U;
/* Node is MASTER */
linUserConfig.nodeFunction = MASTER;
/* Disable autobaud feature */
linUserConfig.autobaudEnable = FALSE;
/* Callback function to get time interval in nano seconds */
linUserConfig.timerGetTimeIntervalCallback = (lin_timer_get_time_t)
    timerGetTimeIntervalCallback0;

/* Initialize LIN Hardware interface */
LIN_DRV_Init(LIO, (lin_user_config_t *) &linUserConfig, (
    lin_state_t *) &linState);
```

8. The users are required to initialize a timer for LIN.

E.g. a Flex Timer (FTM). FTM instance should be initialized in Output Compare mode with an interrupt(E.g. FTM0_Ch0_Ch1_IRQHandler) period of about 500 us. Users can choose a different interrupt period that is appropriate to their applications. In timer interrupt handler, users shall call LIN_DRV_TimeoutService to handle linCurrentState->timeoutCounter while sending or receiving data.

17.81.5 LIN Data Transfers

The driver implements transmit and receive functions to transfer buffers of data by blocking and non-blocking modes.

The blocking transmit and receive functions include [LIN_DRV_SendFrameDataBlocking\(\)](#) and the [LIN_DRV_ReceiveFrameDataBlocking\(\)](#) functions.

The non-blocking (async) transmit and receive functions include the [LIN_DRV_SendFrameData\(\)](#) and the [LIN_DRV_ReceiveFrameData\(\)](#) functions.

The [LIN_DRV_ReceiveFrameData\(\)](#) function is recommended to be called in an interrupt event of receiving PID as implemented in LIN Stack middleware.

The [LIN_DRV_ReceiveFrameData\(\)](#) function should be called before data is transferring on the LIN bus. The [LIN_DRV_ReceiveFrameDataBlocking\(\)](#) function should be called before frame is transferring on the LIN bus. Otherwise, some data may be lost.

Master nodes can transmit frame headers in non-blocking mode using [LIN_DRV_MasterSendHeader\(\)](#).

In all these cases, the functions are interrupt-driven.

17.81.6 Autobaud feature

AUTOBAUD is an extensive feature in LIN Driver which allows a slave node to automatically detect baudrate of LIN bus and adapt its original baudrate to bus value. Auto Baud is applied when the baudrate of the incoming data is unknown. Currently autobaud feature is supported to detect LIN bus baudrates 2400, 4800, 9600, 14400, 19200 bps.

1. If autobaud feature is enabled, at LIN driver initialization slave's baudrate is set to 19200bps. The application should use a timer interrupt in input capture mode of both rising and falling edges(E.g FTM), call [LIN_DRV_AutoBaudCapture\(uint32_t instance\)](#) function to calculate and set Slave's baudrate like Master's baudrate. When receiving a frame header, the slave detect LIN bus's baudrate based on the synchronization byte and adapts its baudrate accordingly. On changing baudrate, the slave set current event ID to LIN_BAUDRATE_ADJUSTED and call the callback function. In that callback function users might change the frame data count timeout. Users can look at CallbackHandler() in [lin.c](#) of lin middleware for a reference.

Note: Lin driver should be initiated before initiating a timer interrupt(E.g FTM).

2. Baudrate evaluation process is executed until autobaud successfully. During run-time if LIN bus's baudrate is changed suddenly to a value other than the slave's current baudrate, users shall reset MCU to execute baudrate evaluation process.

Note

1. When the vector table is not in ram (**flash_vector_table = 1**):
 - INT_SYS_InstallHandler shall check if the function pointer provided as parameter for the new handler is already present in the vector table for the given IRQ number.
 - The user will be required to manually add the correct handlers in the startup files

Data Structures

- struct [lin_user_config_t](#)

LIN hardware configuration structure Implements : [lin_user_config_t](#) Class. [More...](#)

- struct [lin_state_t](#)

Runtime state of the LIN driver. [More...](#)

Macros

- #define [SLAVE](#) 0U
- #define [MASTER](#) 1U
- #define [MAKE_PARITY](#) 0U
- #define [CHECK_PARITY](#) 1U

Typedefs

- typedef uint32_t(* [lin_timer_get_time_interval_t](#)) (uint32_t *nanoSeconds)
Callback function to get time interval in nanoseconds Implements : [lin_timer_get_time_interval_t](#) Class.
- typedef void(* [lin_callback_t](#)) (uint32_t instance, void *linState)
LIN Driver callback function type Implements : [lin_callback_t](#) Class.

Enumerations

- enum [lin_event_id_t](#) {
[LIN_NO_EVENT](#) = 0x00U, [LIN_WAKEUP_SIGNAL](#) = 0x01U, [LIN_BAUDRATE_ADJUSTED](#) = 0x02U, [LIN_RECV_BREAK_FIELD_OK](#) = 0x03U,
[LIN_SYNC_OK](#) = 0x04U, [LIN_SYNC_ERROR](#) = 0x05U, [LIN_PID_OK](#) = 0x06U, [LIN_PID_ERROR](#) = 0x07U,
[LIN_FRAME_ERROR](#) = 0x08U, [LIN_READBACK_ERROR](#) = 0x09U, [LIN_CHECKSUM_ERROR](#) = 0x0AU,
[LIN_TX_COMPLETED](#) = 0x0BU,
[LIN_RX_COMPLETED](#) = 0x0CU, [LIN_RX_OVERRUN](#) = 0x0DU }
Defines types for an enumerating event related to an Identifier. Implements : [lin_event_id_t](#) Class.
- enum [lin_node_state_t](#) {
[LIN_NODE_STATE_UNINIT](#) = 0x00U, [LIN_NODE_STATE_SLEEP_MODE](#) = 0x01U, [LIN_NODE_STATE_IDLE](#) = 0x02U, [LIN_NODE_STATE_SEND_BREAK_FIELD](#) = 0x03U,
[LIN_NODE_STATE_RECV_SYNC](#) = 0x04U, [LIN_NODE_STATE_SEND_PID](#) = 0x05U, [LIN_NODE_STATE_RECV_PID](#) = 0x06U, [LIN_NODE_STATE_RECV_DATA](#) = 0x07U,
[LIN_NODE_STATE_RECV_DATA_COMPLETED](#) = 0x08U, [LIN_NODE_STATE_SEND_DATA](#) = 0x09U, [LIN_NODE_STATE_SEND_DATA_COMPLETED](#) = 0x0AU }
Define type for an enumerating LIN Node state. Implements : [lin_node_state_t](#) Class.

Variables

- [isr_t](#) [g_linLpuartIsrs](#) [LPUART_INSTANCE_COUNT]

LIN DRIVER

- status_t [LIN_DRV_Init](#) (uint32_t instance, [lin_user_config_t](#) *linUserConfig, [lin_state_t](#) *linCurrentState)
Initializes an instance LIN Hardware Interface for LIN Network.
- void [LIN_DRV_Deinit](#) (uint32_t instance)
Shuts down the LIN Hardware Interface by disabling interrupts and transmitter/receiver.
- void [LIN_DRV_GetDefaultConfig](#) (bool isMaster, [lin_user_config_t](#) *linUserConfig)
Initializes the LIN user configuration structure with default values.
- [lin_callback_t](#) [LIN_DRV_InstallCallback](#) (uint32_t instance, [lin_callback_t](#) function)
Installs callback function that is used for [LIN_DRV_IRQHandler](#).

- status_t [LIN_DRV_SendFrameDataBlocking](#) (uint32_t instance, const uint8_t *txBuff, uint8_t txSize, uint32_t timeoutMSec)

Sends Frame data out through the LIN Hardware Interface using blocking method. This function will calculate the checksum byte and send it with the frame data. Blocking means that the function does not return until the transmission is complete. This function checks if txSize is in range from 1 to 8. If not, it will return STATUS_ERROR. This function also returns STATUS_ERROR if node's current state is in SLEEP mode. This function checks if the isBusBusy is false, if not it will return LIN_BUS_BUSY. The function does not return until the transmission is complete. If the transmission is successful, it will return STATUS_SUCCESS. If not, it will return STATUS_TIMEOUT.
- status_t [LIN_DRV_SendFrameData](#) (uint32_t instance, const uint8_t *txBuff, uint8_t txSize)

Sends frame data out through the LIN Hardware Interface using non-blocking method. This enables an a-sync method for transmitting data. Non-blocking means that the function returns immediately. The application has to get the transmit status to know when the transmit is complete. This function will calculate the checksum byte and send it with the frame data. The function will return immediately after calling this function. If txSize is equal to 0 or greater than 8 or node's current state is in SLEEP mode then the function will return STATUS_ERROR. If isBusBusy is currently true then the function will return LIN_BUS_BUSY.
- status_t [LIN_DRV_GetTransmitStatus](#) (uint32_t instance, uint8_t *bytesRemaining)

Get status of an on-going non-blocking transmission While sending frame data using non-blocking method, users can use this function to get status of that transmission. The bytesRemaining shows number of bytes that still needed to transmit.
- status_t [LIN_DRV_ReceiveFrameDataBlocking](#) (uint32_t instance, uint8_t *rxBuff, uint8_t rxSize, uint32_t timeoutMSec)

Receives frame data through the LIN Hardware Interface using blocking method. This function receives data from LPUART module using blocking method, the function does not return until the receive is complete. The interrupt handler LIN_LPUART_DRV_IRQHandler will check the checksum byte. If the checksum is correct, it will receive the frame data. If the checksum is incorrect, this function will return STATUS_TIMEOUT and data in rxBuff might be wrong. This function also check if rxSize is in range from 1 to 8. If not, it will return STATUS_ERROR. This function also returns STATUS_ERROR if node's current state is in SLEEP mode. This function checks if the isBusBusy is false, if not it will return LIN_BUS_BUSY.
- status_t [LIN_DRV_ReceiveFrameData](#) (uint32_t instance, uint8_t *rxBuff, uint8_t rxSize)

Receives frame data through the LIN Hardware Interface using non-blocking method. This function will check the checksum byte. If the checksum is correct, it will receive it with the frame data. Non-blocking means that the function returns immediately. The application has to get the receive status to know when the reception is complete. The interrupt handler LIN_LPUART_DRV_IRQHandler will check the checksum byte. If the checksum is correct, it will receive the frame data. If the checksum is incorrect, this function will return STATUS_TIMEOUT and data in rxBuff might be wrong. This function also check if rxSize is in range from 1 to 8. If not, it will return STATUS_ERROR. This function also returns STATUS_ERROR if node's current state is in SLEEP mode. This function checks if the isBusBusy is false, if not it will return LIN_BUS_BUSY.
- status_t [LIN_DRV_AbortTransferData](#) (uint32_t instance)

Aborts an on-going non-blocking transmission/reception. While performing a non-blocking transferring data, users can call this function to terminate immediately the transferring.
- status_t [LIN_DRV_GetReceiveStatus](#) (uint32_t instance, uint8_t *bytesRemaining)

Get status of an on-going non-blocking reception. This function returns whether the data reception is complete. When performing non-blocking transmit, the user can call this function to ascertain the state of the current receive progress: in progress (STATUS_BUSY) or timeout (STATUS_TIMEOUT) or complete (STATUS_SUCCESS). In addition, if the reception is still in progress, the user can obtain the number of bytes that still needed to receive.
- status_t [LIN_DRV_GoToSleepMode](#) (uint32_t instance)

Puts current LIN node to sleep mode This function changes current node state to LIN_NODE_STATE_SLEEP_MODE.
- status_t [LIN_DRV_GotIdleState](#) (uint32_t instance)

Puts current LIN node to Idle state This function changes current node state to LIN_NODE_STATE_IDLE.
- status_t [LIN_DRV_SendWakeupSignal](#) (uint32_t instance)

Sends a wakeup signal through the LIN Hardware Interface.
- lin_node_state_t [LIN_DRV_GetCurrentNodeState](#) (uint32_t instance)

Get the current LIN node state.
- void [LIN_DRV_TimeoutService](#) (uint32_t instance)

Callback function for Timer Interrupt Handler Users may use (optional, not required) `LIN_DRV_TimeoutService` to check if timeout has occurred during non-blocking frame data transmission and reception. User may initialize a timer (for example FTM) in Output Compare Mode with period of 500 micro seconds (recommended). In timer IRQ handler, call this function.

- void `LIN_DRV_SetTimeoutCounter` (uint32_t instance, uint32_t timeoutValue)
Set Value for Timeout Counter that is used in `LIN_DRV_TimeoutService`.
- status_t `LIN_DRV_MasterSendHeader` (uint32_t instance, uint8_t id)
Sends frame header out through the LIN Hardware Interface using a non-blocking method. This function sends LIN Break field, sync field then the ID with correct parity. This function checks if the interface is Master, if not, it will return `STATUS_ERROR`. This function checks if id is in range from 0 to 0x3F, if not it will return `STATUS_ERROR`.
- status_t `LIN_DRV_EnableIRQ` (uint32_t instance)
Enables LIN hardware interrupts.
- status_t `LIN_DRV_DisableIRQ` (uint32_t instance)
Disables LIN hardware interrupts.
- void `LIN_DRV_IRQHandler` (uint32_t instance)
Interrupt handler for LIN Hardware Interface.
- uint8_t `LIN_DRV_ProcessParity` (uint8_t PID, uint8_t typeAction)
Makes or checks parity bits. If action is checking parity, the function returns ID value if parity bits are correct or 0xFF if parity bits are incorrect. If action is making parity bits, then from input value of ID, the function returns PID. This is not a public API as it is called by other API functions.
- uint8_t `LIN_DRV_MakeChecksumByte` (const uint8_t *buffer, uint8_t sizeBuffer, uint8_t PID)
Makes the checksum byte for a frame. For PID of identifiers, if PID is 0x3C (ID 0x3C) or 0x7D (ID 0x3D) or 0xFE (ID 0x3E) or 0xBF (ID 0x3F) apply classic checksum and apply enhanced checksum for other PID. In case user want to calculate classic checksum please set PID to zero.
- status_t `LIN_DRV_AutoBaudCapture` (uint32_t instance)
Captures time interval to capture baudrate automatically when enable autobaud feature. This function should only be used in Slave. The timer should be in input capture mode of both rising and falling edges. The timer input capture pin should be externally connected to RXD pin.

17.81.7 Data Structure Documentation

17.81.7.1 struct lin_user_config_t

LIN hardware configuration structure Implements : `lin_user_config_t_Class`.

Definition at line 70 of file `lin_driver.h`.

Data Fields

- uint32_t `baudRate`
- bool `nodeFunction`
- bool `autobaudEnable`
- `lin_timer_get_time_interval_t` `timerGetTimeIntervalCallback`
- uint8_t * `classicPID`
- uint8_t `numOfClassicPID`

Field Documentation

17.81.7.1.1 bool autobaudEnable

Enable Autobaud feature

Definition at line 73 of file `lin_driver.h`.

17.81.7.1.2 uint32_t baudRate

baudrate of LIN Hardware Interface to configure

Definition at line 71 of file `lin_driver.h`.

17.81.7.1.3 uint8_t* classicPID

List of PIDs use classic checksum

Definition at line 75 of file lin_driver.h.

17.81.7.1.4 bool nodeFunction

Node function as Master or Slave

Definition at line 72 of file lin_driver.h.

17.81.7.1.5 uint8_t numOfClassicPID

Number of PIDs use classic checksum

Definition at line 76 of file lin_driver.h.

17.81.7.1.6 lin_timer_get_time_interval_t timerGetTimeIntervalCallback

Callback function to get time interval in nanoseconds

Definition at line 74 of file lin_driver.h.

17.81.7.2 struct lin_state_t

Runtime state of the LIN driver.

Note that the caller provides memory for the driver state structures during initialization because the driver does not statically allocate memory. Implements : lin_state_t_Class

Definition at line 131 of file lin_driver.h.

Data Fields

- const uint8_t * txBuff
- uint8_t * rxBuff
- uint8_t cntByte
- volatile uint8_t txSize
- volatile uint8_t rxSize
- uint8_t checksum
- volatile bool isTxBusy
- volatile bool isRxBusy
- volatile bool isBusBusy
- volatile bool isTxBlocking
- volatile bool isRxBlocking
- lin_callback_t Callback
- uint8_t currentId
- uint8_t currentPid
- volatile lin_event_id_t currentEventId
- volatile lin_node_state_t currentNodeState
- volatile uint32_t timeoutCounter
- volatile bool timeoutCounterFlag
- volatile bool baudrateEvalEnable
- volatile uint8_t fallingEdgeInterruptCount
- uint32_t linSourceClockFreq
- semaphore_t txCompleted
- semaphore_t rxCompleted

Field Documentation

17.81.7.2.1 `volatile bool baudrateEvalEnable`

Baudrate Evaluation Process Enable

Definition at line 150 of file `lin_driver.h`.

17.81.7.2.2 `lin_callback_t` Callback

Callback function to invoke after receiving a byte or transmitting a byte.

Definition at line 143 of file `lin_driver.h`.

17.81.7.2.3 `uint8_t checksum`

Checksum byte.

Definition at line 137 of file `lin_driver.h`.

17.81.7.2.4 `uint8_t cntByte`

To count number of bytes already transmitted or received.

Definition at line 134 of file `lin_driver.h`.

17.81.7.2.5 `volatile lin_event_id_t currentEventId`

Current ID Event

Definition at line 146 of file `lin_driver.h`.

17.81.7.2.6 `uint8_t currentId`

Current ID

Definition at line 144 of file `lin_driver.h`.

17.81.7.2.7 `volatile lin_node_state_t currentNodeState`

Current Node state

Definition at line 147 of file `lin_driver.h`.

17.81.7.2.8 `uint8_t currentPid`

Current PID

Definition at line 145 of file `lin_driver.h`.

17.81.7.2.9 `volatile uint8_t fallingEdgeInterruptCount`

Falling Edge count of a sync byte

Definition at line 151 of file `lin_driver.h`.

17.81.7.2.10 `volatile bool isBusBusy`

True if there are data, frame headers being transferred on bus

Definition at line 140 of file `lin_driver.h`.

17.81.7.2.11 `volatile bool isRxBlocking`

True if receive is blocking transaction.

Definition at line 142 of file `lin_driver.h`.

17.81.7.2.12 volatile bool isRxBusy

True if the LIN interface is receiving frame data.

Definition at line 139 of file lin_driver.h.

17.81.7.2.13 volatile bool isTxBlocking

True if transmit is blocking transaction.

Definition at line 141 of file lin_driver.h.

17.81.7.2.14 volatile bool isTxBusy

True if the LIN interface is transmitting frame data.

Definition at line 138 of file lin_driver.h.

17.81.7.2.15 uint32_t linSourceClockFreq

Frequency of the source clock for LIN

Definition at line 152 of file lin_driver.h.

17.81.7.2.16 uint8_t* rxBuff

The buffer of received data.

Definition at line 133 of file lin_driver.h.

17.81.7.2.17 semaphore_t rxCompleted

Used to wait for LIN interface ISR to complete reception

Definition at line 154 of file lin_driver.h.

17.81.7.2.18 volatile uint8_t rxSize

The remaining number of bytes to be received.

Definition at line 136 of file lin_driver.h.

17.81.7.2.19 volatile uint32_t timeoutCounter

Value of the timeout counter

Definition at line 148 of file lin_driver.h.

17.81.7.2.20 volatile bool timeoutCounterFlag

Timeout counter flag

Definition at line 149 of file lin_driver.h.

17.81.7.2.21 const uint8_t* txBuff

The buffer of data being sent.

Definition at line 132 of file lin_driver.h.

17.81.7.2.22 semaphore_t txCompleted

Used to wait for LIN interface ISR to complete transmission.

Definition at line 153 of file lin_driver.h.

17.81.7.2.23 volatile uint8_t txSize

The remaining number of bytes to be transmitted.

Definition at line 135 of file lin_driver.h.

17.81.8 Macro Definition Documentation

17.81.8.1 #define CHECK_PARITY 1U

Definition at line 50 of file lin_driver.h.

17.81.8.2 #define MAKE_PARITY 0U

Definition at line 49 of file lin_driver.h.

17.81.8.3 #define MASTER 1U

Definition at line 48 of file lin_driver.h.

17.81.8.4 #define SLAVE 0U

Definition at line 47 of file lin_driver.h.

17.81.9 Typedef Documentation

17.81.9.1 typedef void(* lin_callback_t)(uint32_t instance, void *linState)

LIN Driver callback function type Implements : lin_callback_t_Class.

Definition at line 122 of file lin_driver.h.

17.81.9.2 typedef uint32_t(* lin_timer_get_time_interval_t)(uint32_t *nanoSeconds)

Callback function to get time interval in nanoseconds Implements : lin_timer_get_time_interval_t_Class.

Definition at line 64 of file lin_driver.h.

17.81.10 Enumeration Type Documentation

17.81.10.1 enum lin_event_id_t

Defines types for an enumerating event related to an Identifier. Implements : lin_event_id_t_Class.

Enumerator

LIN_NO_EVENT No event yet

LIN_WAKEUP_SIGNAL Received a wakeup signal

LIN_BAUDRATE_ADJUSTED Indicate that baudrate was adjusted to Master's baudrate

LIN_RECV_BREAK_FIELD_OK Indicate that correct Break Field was received

LIN_SYNC_OK Sync byte is correct

LIN_SYNC_ERROR Sync byte is incorrect

LIN_PID_OK PID correct

LIN_PID_ERROR PID incorrect

LIN_FRAME_ERROR Framing Error

LIN_READBACK_ERROR Readback data is incorrect

LIN_CHECKSUM_ERROR Checksum byte is incorrect

LIN_TX_COMPLETED Sending data completed

LIN_RX_COMPLETED Receiving data completed

LIN_RX_OVERRUN RX overrun flag

Definition at line 83 of file lin_driver.h.

17.81.10.2 enum lin_node_state_t

Define type for an enumerating LIN Node state. Implements : lin_node_state_t_Class.

Enumerator

LIN_NODE_STATE_UNINIT Uninitialized state

LIN_NODE_STATE_SLEEP_MODE Sleep mode state

LIN_NODE_STATE_IDLE Idle state

LIN_NODE_STATE_SEND_BREAK_FIELD Send break field state

LIN_NODE_STATE_RECV_SYNC Receive the synchronization byte state

LIN_NODE_STATE_SEND_PID Send PID state

LIN_NODE_STATE_RECV_PID Receive PID state

LIN_NODE_STATE_RECV_DATA Receive data state

LIN_NODE_STATE_RECV_DATA_COMPLETED Receive data completed state

LIN_NODE_STATE_SEND_DATA Send data state

LIN_NODE_STATE_SEND_DATA_COMPLETED Send data completed state

Definition at line 104 of file lin_driver.h.

17.81.11 Function Documentation

17.81.11.1 status_t LIN_DRV_AbortTransferData (uint32_t instance)

Aborts an on-going non-blocking transmission/reception. While performing a non-blocking transferring data, users can call this function to terminate immediately the transferring.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
-----------------	--

Returns

function always return STATUS_SUCCESS

Definition at line 266 of file lin_driver.c.

17.81.11.2 status_t LIN_DRV_AutoBaudCapture (uint32_t instance)

Captures time interval to capture baudrate automatically when enable autobaud feature. This function should only be used in Slave. The timer should be in input capture mode of both rising and falling edges. The timer input capture pin should be externally connected to RXD pin.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
-----------------	--

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_BUSY: Operation is running.
- STATUS_ERROR: Operation failed due to break char incorrect, wakeup signal incorrect or calculate baudrate failed.

Definition at line 493 of file lin_driver.c.

17.81.11.3 void LIN_DRV_Deinit (uint32_t *instance*)

Shuts down the LIN Hardware Interface by disabling interrupts and transmitter/receiver.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
-----------------	--

Returns

void

Definition at line 80 of file lin_driver.c.

17.81.11.4 status_t LIN_DRV_DisableIRQ (uint32_t *instance*)

Disables LIN hardware interrupts.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
-----------------	--

Returns

function always return STATUS_SUCCESS.

Definition at line 455 of file lin_driver.c.

17.81.11.5 status_t LIN_DRV_EnableIRQ (uint32_t *instance*)

Enables LIN hardware interrupts.

Parameters

<i>instance</i>	LIN Hardware Interface instance number.
-----------------	---

Returns

function always return STATUS_SUCCESS.

Definition at line 437 of file lin_driver.c.

17.81.11.6 lin_node_state_t LIN_DRV_GetCurrentNodeState (uint32_t *instance*)

Get the current LIN node state.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
-----------------	--

Returns

current LIN node state

Definition at line 363 of file lin_driver.c.

17.81.11.7 void LIN_DRV_GetDefaultConfig (bool *isMaster*, lin_user_config_t * *linUserConfig*)

Initializes the LIN user configuration structure with default values.

This function initializes a configuration structure received from the application with default values. Note: Users shall assign measurement callback function pointer that is timerGetTimeIntervalCallback for linUserConfig. Users can see detail in doxygen.

Parameters

in	<i>isMaster</i>	Node function: <ul style="list-style-type: none"> • true if node is MASTER • false if node is SLAVE
out	<i>linUserConfig</i>	the default configuration

Returns

void

Definition at line 95 of file lin_driver.c.

17.81.11.8 status_t LIN_DRV_GetReceiveStatus (uint32_t *instance*, uint8_t * *bytesRemaining*)

Get status of an on-going non-blocking reception. This function returns whether the data reception is complete. When performing non-blocking transmit, the user can call this function to ascertain the state of the current receive progress: in progress (STATUS_BUSY) or timeout (STATUS_TIMEOUT) or complete (STATUS_SUCCESS). In addition, if the reception is still in progress, the user can obtain the number of bytes that still needed to receive.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
<i>bytesRemaining</i>	Number of bytes still needed to receive

Returns

operation status:

- STATUS_SUCCESS : The reception is complete.
- STATUS_TIMEOUT : The reception isn't complete.
- STATUS_BUSY : The reception is on going

Definition at line 289 of file lin_driver.c.

17.81.11.9 status_t LIN_DRV_GetTransmitStatus (uint32_t *instance*, uint8_t * *bytesRemaining*)

Get status of an on-going non-blocking transmission While sending frame data using non-blocking method, users can use this function to get status of that transmission. The bytesRemaining shows number of bytes that still needed to transmit.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
<i>bytesRemaining</i>	Number of bytes still needed to transmit

Returns

operation status:

- STATUS_SUCCESS : The transmission is successful.
- STATUS_BUSY : The transmission is sending
- STATUS_TIMEOUT : Operation failed due to timeout has occurred.

Definition at line 187 of file lin_driver.c.

17.81.11.10 `status_t LIN_DRV_GotIdleState (uint32_t instance)`

Puts current LIN node to Idle state This function changes current node state to LIN_NODE_STATE_IDLE.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
-----------------	--

Returns

function always return STATUS_SUCCESS

Definition at line 327 of file lin_driver.c.

17.81.11.11 `status_t LIN_DRV_GoToSleepMode (uint32_t instance)`

Puts current LIN node to sleep mode This function changes current node state to LIN_NODE_STATE_SLEEP_↔MODE.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
-----------------	--

Returns

function always return STATUS_SUCCESS

Definition at line 309 of file lin_driver.c.

17.81.11.12 `status_t LIN_DRV_Init (uint32_t instance, lin_user_config_t * linUserConfig, lin_state_t * linCurrentState)`

Initializes an instance LIN Hardware Interface for LIN Network.

The caller provides memory for the driver state structures during initialization. The user must select the LIN Hardware Interface clock source in the application to initialize the LIN Hardware Interface.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
<i>linUserConfig</i>	user configuration structure of type lin_user_config_t
<i>linCurrentState</i>	pointer to the LIN Hardware Interface driver state structure

Returns

operation status:

- STATUS_SUCCESS : Operation was successful.
- STATUS_ERROR : Operation failed due to semaphores initialize error.

Definition at line 59 of file lin_driver.c.

17.81.11.13 `lin_callback_t` LIN_DRV_InstallCallback (`uint32_t` *instance*, `lin_callback_t` *function*)

Installs callback function that is used for LIN_DRV_IRQHandler.

Note

After a callback is installed, it bypasses part of the LIN Hardware Interface IRQHandler logic. Therefore, the callback needs to handle the indexes of txBuff and txSize.

Parameters

<i>instance</i>	LIN Hardware Interface instance number.
<i>function</i>	the LIN receive callback function.

Returns

Former LIN callback function pointer.

Definition at line 111 of file lin_driver.c.

17.81.11.14 `void` LIN_DRV_IRQHandler (`uint32_t` *instance*)

Interrupt handler for LIN Hardware Interface.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
-----------------	--

Returns

`void`

Definition at line 475 of file lin_driver.c.

17.81.11.15 `uint8_t` LIN_DRV_MakeChecksumByte (`const` `uint8_t` * *buffer*, `uint8_t` *sizeBuffer*, `uint8_t` *PID*)

Makes the checksum byte for a frame. For PID of identifiers, if PID is 0x3C (ID 0x3C) or 0x7D (ID 0x3D) or 0xFE (ID 0x3E) or 0xBF (ID 0x3F) apply classic checksum and apply enhanced checksum for other PID. In case user want to calculate classic checksum please set PID to zero.

Parameters

<i>buffer</i>	Pointer to Tx buffer
<i>sizeBuffer</i>	Number of bytes that are contained in the buffer.
<i>PID</i>	Protected Identifier byte.

Returns

the checksum byte.

Definition at line 100 of file lin_common.c.

17.81.11.16 `status_t` LIN_DRV_MasterSendHeader (`uint32_t` *instance*, `uint8_t` *id*)

Sends frame header out through the LIN Hardware Interface using a non-blocking method. This function sends LIN Break field, sync field then the ID with correct parity. This function checks if the interface is Master, if not, it will return STATUS_ERROR. This function checks if id is in range from 0 to 0x3F, if not it will return STATUS_ERROR.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
<i>id</i>	Frame Identifier

Returns

operation status:

- STATUS_SUCCESS : The transmission is successful.
- STATUS_BUSY : Bus busy flag is true.
- STATUS_ERROR : The interface isn't Master or id isn't in range from 0 to 0x3F or node's current state is in SLEEP mode.

Definition at line 418 of file lin_driver.c.

17.81.11.17 uint8_t LIN_DRV_ProcessParity (uint8_t PID, uint8_t typeAction)

Makes or checks parity bits. If action is checking parity, the function returns ID value if parity bits are correct or 0xFF if parity bits are incorrect. If action is making parity bits, then from input value of ID, the function returns PID. This is not a public API as it is called by other API functions.

Parameters

<i>PID</i>	PID byte in case of checking parity bits or ID byte in case of making parity bits.
<i>typeAction</i>	1 for Checking parity bits, 0 for making parity bits

Returns

Value has 8 bit:

- 0xFF : Parity bits are incorrect,
- ID : Checking parity bits are correct.
- PID : typeAction is making parity bits.

Definition at line 55 of file lin_common.c.

17.81.11.18 status_t LIN_DRV_ReceiveFrameData (uint32_t instance, uint8_t * rxBuff, uint8_t rxSize)

Receives frame data through the LIN Hardware Interface using non-blocking method. This function will check the checksum byte. If the checksum is correct, it will receive it with the frame data. Non-blocking means that the function returns immediately. The application has to get the receive status to know when the reception is complete. The interrupt handler LIN_LPUART_DRV_IRQHandler will check the checksum byte. If the checksum is correct, it will receive the frame data. If the checksum is incorrect, this function will return STATUS_TIMEOUT and data in rxBuff might be wrong. This function also check if rxSize is in range from 1 to 8. If not, it will return STATUS_ERROR. This function also returns STATUS_ERROR if node's current state is in SLEEP mode. This function checks if the isBusBusy is false, if not it will return LIN_BUS_BUSY.

Note

If users use LIN_DRV_TimeoutService in a timer interrupt handler, then before using this function, users have to set timeout counter to an appropriate value by using LIN_DRV_SetTimeoutCounter(instance, timeout↵ Value). The timeout value should be big enough to complete the reception. Timeout in real time is (timeout↵ Value) * (time period that LIN_DRV_TimeoutService is called). For example, if LIN_DRV_TimeoutService is called in an timer interrupt with period of 500 micro seconds, then timeout in real time is timeoutValue * 500 micro seconds.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
<i>rxBuff</i>	buffer containing 8-bit received data
<i>rxSize</i>	the number of bytes to receive

Returns

operation status:

- STATUS_SUCCESS : The receives frame data is successful.
- STATUS_TIMEOUT : The checksum is incorrect.
- STATUS_BUSY : Bus busy flag is true.
- STATUS_ERROR : Operation failed due is equal to 0 or greater than 8 or node's current state is in SLEEP mode

Definition at line 244 of file lin_driver.c.

17.81.11.19 `status_t LIN_DRV_ReceiveFrameDataBlocking (uint32_t instance, uint8_t * rxBuff, uint8_t rxSize, uint32_t timeoutMSec)`

Receives frame data through the LIN Hardware Interface using blocking method. This function receives data from LPUART module using blocking method, the function does not return until the receive is complete. The interrupt handler LIN_LPUART_DRV_IRQHandler will check the checksum byte. If the checksum is correct, it will receive the frame data. If the checksum is incorrect, this function will return STATUS_TIMEOUT and data in rxBuff might be wrong. This function also check if rxSize is in range from 1 to 8. If not, it will return STATUS_ERROR. This function also returns STATUS_ERROR if node's current state is in SLEEP mode. This function checks if the isBusBusy is false, if not it will return LIN_BUS_BUSY.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
<i>rxBuff</i>	buffer containing 8-bit received data
<i>rxSize</i>	the number of bytes to receive
<i>timeoutMSec</i>	timeout value in milliseconds

Returns

operation status:

- STATUS_SUCCESS : The receives frame data is successful.
- STATUS_TIMEOUT : The checksum is incorrect.
- STATUS_BUSY : Bus busy flag is true.
- STATUS_ERROR : Operation failed due is equal to 0 or greater than 8 or node's current state is in SLEEP mode

Definition at line 214 of file lin_driver.c.

17.81.11.20 `status_t LIN_DRV_SendFrameData (uint32_t instance, const uint8_t * txBuff, uint8_t txSize)`

Sends frame data out through the LIN Hardware Interface using non-blocking method. This enables an a-sync method for transmitting data. Non-blocking means that the function returns immediately. The application has to get the transmit status to know when the transmit is complete. This function will calculate the checksum byte and send it with the frame data. The function will return immediately after calling this function. If txSize is equal to 0 or greater than 8 or node's current state is in SLEEP mode then the function will return STATUS_ERROR. If isBusBusy is currently true then the function will return LIN_BUS_BUSY.

Note

If users use LIN_DRV_TimeoutService in a timer interrupt handler, then before using this function, users have to set timeout counter to an appropriate value by using LIN_DRV_SetTimeoutCounter(instance, timeout↵Value). The timeout value should be big enough to complete the transmission. Timeout in real time is (timeoutValue) * (time period that LIN_DRV_TimeoutService is called). For example, if LIN_DRV_Timeout↵Service is called in an timer interrupt with period of 500 micro seconds, then timeout in real time is timeout↵Value * 500 micro seconds.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
<i>txBuff</i>	source buffer containing 8-bit data chars to send
<i>txSize</i>	the number of bytes to send

Returns

operation status:

- STATUS_SUCCESS : The transmission is successful.
- STATUS_BUSY : Operation failed due to isBusBusy is currently true.
- STATUS_ERROR : Operation failed due to txSize is equal to 0 or greater than 8 or node's current state is in SLEEP mode

Definition at line 162 of file lin_driver.c.

17.81.11.21 `status_t LIN_DRV_SendFrameDataBlocking (uint32_t instance, const uint8_t * txBuff, uint8_t txSize, uint32_t timeoutMSec)`

Sends Frame data out through the LIN Hardware Interface using blocking method. This function will calculate the checksum byte and send it with the frame data. Blocking means that the function does not return until the transmission is complete. This function checks if txSize is in range from 1 to 8. If not, it will return STATUS_ER↵ROR. This function also returns STATUS_ERROR if node's current state is in SLEEP mode. This function checks if the isBusBusy is false, if not it will return LIN_BUS_BUSY. The function does not return until the transmission is complete. If the transmission is successful, it will return STATUS_SUCCESS. If not, it will return STATUS_TIME↵OUT.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
<i>txBuff</i>	source buffer containing 8-bit data chars to send
<i>txSize</i>	the number of bytes to send
<i>timeoutMSec</i>	timeout value in milliseconds

Returns

operation status:

- STATUS_SUCCESS : The transmission is successful.
- STATUS_TIMEOUT : The transmission isn't successful.

Definition at line 137 of file lin_driver.c.

17.81.11.22 `status_t LIN_DRV_SendWakeupSignal (uint32_t instance)`

Sends a wakeup signal through the LIN Hardware Interface.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
-----------------	--

Returns

operation status:

- STATUS_SUCCESS : Bus busy flag is false.
- STATUS_BUSY : Bus busy flag is true.

Definition at line 345 of file lin_driver.c.

17.81.11.23 void LIN_DRV_SetTimeoutCounter (uint32_t *instance*, uint32_t *timeoutValue*)

Set Value for Timeout Counter that is used in LIN_DRV_TimeoutService.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
<i>timeoutValue</i>	Timeout Value to be set

Returns

void

Definition at line 398 of file lin_driver.c.

17.81.11.24 void LIN_DRV_TimeoutService (uint32_t *instance*)

Callback function for Timer Interrupt Handler Users may use (optional, not required) LIN_DRV_TimeoutService to check if timeout has occurred during non-blocking frame data transmission and reception. User may initialize a timer (for example FTM) in Output Compare Mode with period of 500 micro seconds (recommended). In timer IRQ handler, call this function.

Parameters

<i>instance</i>	LIN Hardware Interface instance number
-----------------	--

Returns

void

Definition at line 383 of file lin_driver.c.

17.81.12 Variable Documentation

17.81.12.1 isr_t g_linLpuartIsrs[LPUART_INSTANCE_COUNT]

Definition at line 88 of file lin_irq.c.

17.82 LIN Stack

17.82.1 Detailed Description

This section covers the functionality of the LIN Stack middleware layer in S32 SDK.

Introduction

LIN Stack Package Components

LIN Stack is a Middleware package that supports the LIN 1.3, 2.0, 2.1 and above, **LIN2.1** and **J2602** specifications. In LIN Stack, LIN 2.1 covers all LIN 2.1, LIN 2.2 and LIN 2.2A specifications, as the changes following LIN 2.1 are only spelling corrections and clarifications.

- 1. **LIN Stack:**

The layered architecture of the LIN Stack is shown on [Figure 1](#). Such architecture aims maximum reusability of common code base for **LIN2.1** and **J2602** specifications for S32 Freescale automotive MCU portfolio.

The core API layer of **LIN2.1/J2602** handles initialization, processing and signal based interaction between applications and LIN Core.

The **LIN2.1** TL (Transport Layer) provides methods for diagnostic services.

The low level layer offers methods for handling signal transmission between user applications and hardware such as interface initialization and deinitialization, frame header sending, response receiving, etc. The low level layer is built on top of **LIN Driver** which is built on top of LPUART HAL layer in the current release.

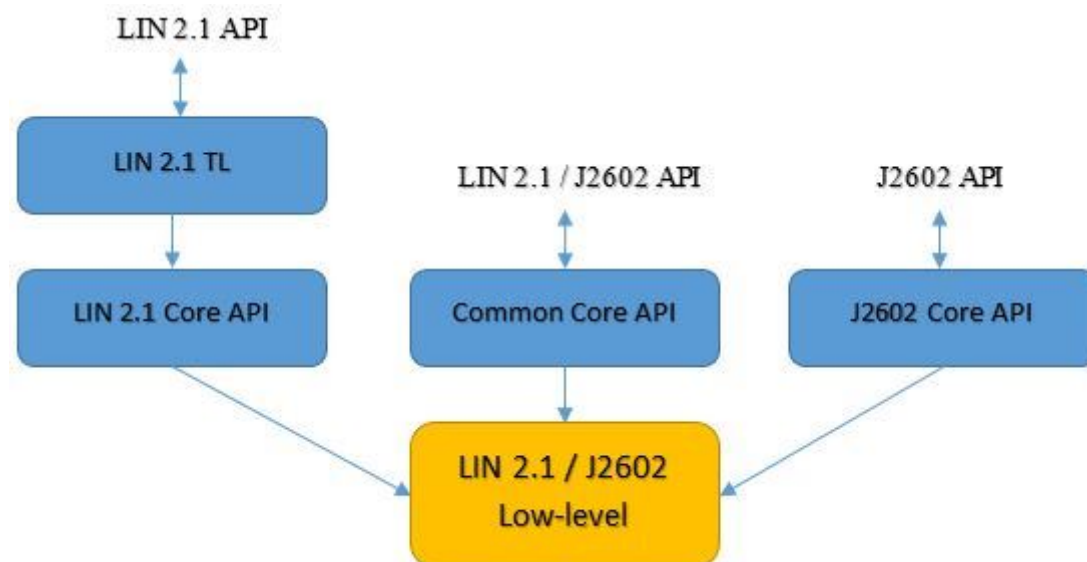


Figure 1. LIN Stack Architecture diagram

2. Node Configuration Tool:

To generate configuration files, users can use the Node Configuration Tool that is LIN Stack PEX component which allows to parse existed LDF files and reflect their contents to LIN Stack component GUI, to create new LDF files, to configure LIN cluster definitions and Node definitions. Using LIN Stack PEX component, users can easily generate the node configuration files (`lin_cfg.h` and `lin_cfg.c`) that are needed for LIN Stack to work properly.

[Figure 2](#). Shows the diagram of configuration data flow.

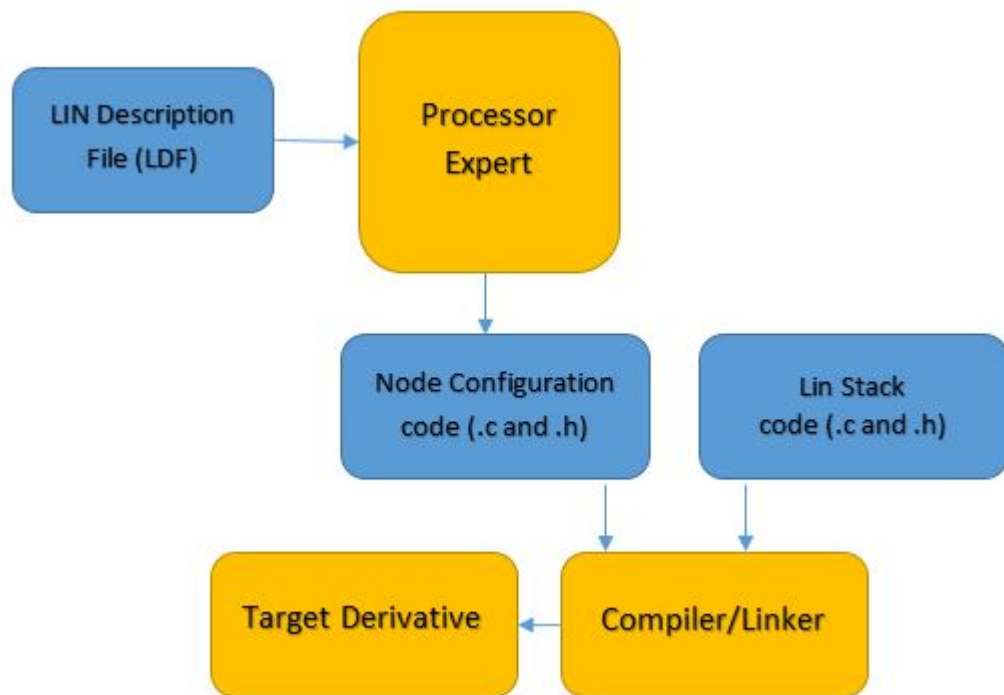


Figure 2. Configuration data

The LDF files describe complete LIN cluster definition including Master/slave mode definition, signals, frames, schedules, timing, etc.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```

* ${S32SDK_PATH}\middleware\lin\coreapi\lin_common_api.c
* ${S32SDK_PATH}\middleware\lin\coreapi\lin_common_proto.c
* ${S32SDK_PATH}\middleware\lin\coreapi\lin_j2602_proto.c
* ${S32SDK_PATH}\middleware\lin\coreapi\lin_lin21_proto.c
* ${S32SDK_PATH}\middleware\lin\diagnostic\lin_diagnostic_service.c
* ${S32SDK_PATH}\middleware\lin\lowlevel\lin.c
* ${S32SDK_PATH}\middleware\lin\transport\lin_commontl_api.c
* ${S32SDK_PATH}\middleware\lin\transport\lin_commontl_proto.c
*

```

Include path

The following paths need to be added to the include path of the toolchain:

```

* ${S32SDK_PATH}\rtos\osif
* ${S32SDK_PATH}\platform\drivers\inc
* ${S32SDK_PATH}\platform\drivers\src\lin
* ${S32SDK_PATH}\platform\drivers\src\lpuart
* ${S32SDK_PATH}\middleware\lin\include
* ${S32SDK_PATH}\middleware\lin\lowlevel
* ${S32SDK_PATH}\middleware\lin\coreapi
* ${S32SDK_PATH}\middleware\lin\transport
*

```

Compile symbols

No special symbols are required for this component

Dependencies

Clock Manager Pins Driver (PINS) LIN Driver Low Power Universal Asynchronous Receiver-Transmitter (LPUART)

Modules

- [Diagnostic services](#)

Diagnostic services defines methods to implement diagnostic data transfer between a master node connected with a diagnostic tester and the slave nodes.

- [LIN Core API](#)

The LIN core API handles initialization, processing and a signal based interaction between the application and the LIN core. Refer to chapter 7, LIN 2.2A specification.

- [Low level API](#)

Low level layer consists of functions that call LIN driver API.

- [Transport layer API](#)

Transport layer stands between the application layer and the core API layer.

17.83 LPI2C Driver

17.83.1 Detailed Description

Low Power Inter-Integrated Circuit (LPI2C) Peripheral Driver.

Low Power Inter-Integrated Circuit Driver.

The LPI2C driver allows communication on an I2C bus using the LPI2C module in the S32144K processor.

Features

- Interrupt based
- Master or slave operation
- Provides blocking and non-blocking transmit and receive functions
- 7-bit or 10-bit addressing
- Configurable baud rate
- Provides support for all operating modes supported by the hardware
 - Standard-mode (Sm): bidirectional data transfers up to 100 kbit/s
 - Fast-mode (Fm): bidirectional data transfers up to 400 kbit/s

Functionality

In order to use the LPI2C driver it must be first initialized in either master or slave mode, using functions [LPI2C_DRV_MasterInit\(\)](#) or [LPI2C_DRV_SlaveInit\(\)](#). Once initialized, it cannot be initialized again for the same LPI2C module instance until it is de-initialized, using [LPI2C_DRV_MasterDeinit\(\)](#) or [LPI2C_DRV_SlaveDeinit\(\)](#). Different LPI2C module instances can function independently of each other.

Master Mode

Master Mode provides functions for transmitting or receiving data to/from any I2C slave. Slave address and baud rate are provided at initialization time through the master configuration structure, but they can be changed at run-time by using [LPI2C_DRV_MasterSetBaudRate\(\)](#) or [LPI2C_DRV_MasterSetSlaveAddr\(\)](#). Note that due to module limitation not any baud rate can be achieved. The driver will set a baud rate as close as possible to the requested baud rate, but there may still be substantial differences, for example if requesting a high baud rate while using a low-frequency protocol clock for the LPI2C module. The application should call [LPI2C_DRV_MasterGetBaudRate\(\)](#) after [LPI2C_DRV_MasterSetBaudRate\(\)](#) to check what baud rate was actually set.

To send or receive data to/from the currently configured slave address, use functions [LPI2C_DRV_MasterSendData\(\)](#) or [LPI2C_DRV_MasterReceiveData\(\)](#) (or their blocking counterparts). Parameter `sendStop` can be used to chain multiple transfers with repeated START condition between them, for example when sending a command and then immediately receiving a response. The application should ensure that any send or receive transfer with `sendStop` set to `false` is followed by another transfer, otherwise the LPI2C master will hold the SCL line low indefinitely and block the I2C bus. The last transfer from a chain should always have `sendStop` set to `true`.

Blocking operations will return only when the transfer is completed, either successfully or with error. Non-blocking operations will initiate the transfer and return `STATUS_SUCCESS`, but the module is still busy with the transfer and another transfer can't be initiated until the current transfer is complete. The application can check the status of the current transfer by calling [LPI2C_DRV_MasterGetTransferStatus\(\)](#). If the transfer is completed, the functions will return either `STATUS_SUCCESS` or an error code, depending on the outcome of the last transfer.

The driver supports any operating mode supported by the module. The operating mode is set together with the baud rate, by [LPI2C_DRV_MasterSetBaudRate\(\)](#). For High-Speed mode a second baud rate is required, for high-speed communication. Note that due to module limitation (common prescaler setting for normal and fast baud rate) there is a limit on the maximum difference between the two baud rates. [LPI2C_DRV_MasterGetBaudRate\(\)](#) can be used to check the baud rate setting for both modes.

Slave Mode

Slave Mode provides functions for transmitting or receiving data to/from any I2C master. There are two slave operating modes, selected by the field `slaveListening` in the slave configuration structure:

- Slave always listening: the slave interrupt is enabled at initialization time and the slave always listens to the line for a master addressing it. Any events are reported to the application through the callback function provided at initialization time. The callback can use [LPI2C_DRV_SlaveSetRxBuffer\(\)](#) or [LPI2C_DRV_SlaveSetTxBuffer\(\)](#) to provide the appropriate buffers for transmit or receive, as needed.
- On-demand operation: the slave is commanded to transmit or receive data through the call of [LPI2C_DRV_SlaveSendData\(\)](#) and [LPI2C_DRV_SlaveReceiveData\(\)](#) (or their blocking counterparts). The actual moment of the transfer depends on the I2C master. The use of callbacks optional in this case, for example to treat events like `LPI2C_SLAVE_EVENT_TX_EMPTY` or `LPI2C_SLAVE_EVENT_RX_FULL`. Outside the commanded receive / transmit operations the LPI2C interrupts are disabled and the module will not react to master transfer requests.

Important Notes

- Before using the LPI2C driver in master mode the protocol clock of the module must be configured. Refer to SCG HAL and PCC HAL for clock configuration.
- Before using the LPI2C driver the pins must be routed to the LPI2C module. Refer to PORT HAL for pin routing configuration.
- The driver enables the interrupts for the corresponding LPI2C module, but any interrupt priority setting must be done by the application.
- Fast+, high-speed and ultra-fast mode aren't supported.
- Aborting a master reception is not currently supported due to hardware behavior (the module will continue a started reception even if the FIFO is reset).
- In listening mode, the init function must be called before the master starts the transfer. In non-listening mode, the init function and the appropriate send/receive function must be called before the master starts the transfer.
- Aborting a transfer with the function [LPI2C_DRV_MasterAbortTransferData\(\)](#) can't be done safely due to device limitation; the user must ensure that the address is sent before aborting the transfer.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\lpi2c\lpi2c_irq.c
${S32SDK_PATH}\platform\drivers\src\lpi2c\lpi2c_hw_access.c
${S32SDK_PATH}\platform\drivers\src\lpi2c\lpi2c_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc
${S32SDK_PATH}\platform\drivers\src\lpi2c
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager OS Interface \(OSIF\)](#) [Interrupt Manager \(Interrupt\)](#) [Enhanced Direct Memory Access \(eDMA\)](#)

Data Structures

- struct [lpi2c_master_user_config_t](#)
Defines the example structure. [More...](#)
- struct [lpi2c_slave_user_config_t](#)
Slave configuration structure. [More...](#)
- struct [lpi2c_baud_rate_params_t](#)
Baud rate structure. [More...](#)
- struct [lpi2c_master_state_t](#)
Master internal context structure. [More...](#)
- struct [lpi2c_slave_state_t](#)
Slave internal context structure. [More...](#)

Enumerations

- enum [lpi2c_mode_t](#) { [LPI2C_STANDARD_MODE](#) = 0x0U, [LPI2C_FAST_MODE](#) = 0x1U }
I2C operating modes Implements : [lpi2c_mode_t](#) Class.
- enum [lpi2c_transfer_type_t](#) { [LPI2C_USING_DMA](#) = 0, [LPI2C_USING_INTERRUPTS](#) = 1 }
Type of LPI2C transfer (based on interrupts or DMA). Implements : [lpi2c_transfer_type_t](#) Class.

LPI2C Driver

- status_t [LPI2C_DRV_MasterInit](#) (uint32_t instance, const [lpi2c_master_user_config_t](#) *userConfigPtr, [lpi2c_master_state_t](#) *master)
Initialize the LPI2C master mode driver.
- status_t [LPI2C_DRV_MasterDeinit](#) (uint32_t instance)
De-initialize the LPI2C master mode driver.
- void [LPI2C_DRV_MasterGetBaudRate](#) (uint32_t instance, [lpi2c_baud_rate_params_t](#) *baudRate)
Get the currently configured baud rate.
- status_t [LPI2C_DRV_MasterSetBaudRate](#) (uint32_t instance, const [lpi2c_mode_t](#) operatingMode, const [lpi2c_baud_rate_params_t](#) baudRate)
Set the baud rate for any subsequent I2C communication.
- void [LPI2C_DRV_MasterSetSlaveAddr](#) (uint32_t instance, const uint16_t address, const bool is10bitAddr)
Set the slave address for any subsequent I2C communication.
- status_t [LPI2C_DRV_MasterSendData](#) (uint32_t instance, const uint8_t *txBuff, uint32_t txSize, bool sendStop)
Perform a non-blocking send transaction on the I2C bus.
- status_t [LPI2C_DRV_MasterSendDataBlocking](#) (uint32_t instance, const uint8_t *txBuff, uint32_t txSize, bool sendStop, uint32_t timeout)
Perform a blocking send transaction on the I2C bus.
- status_t [LPI2C_DRV_MasterAbortTransferData](#) (uint32_t instance)
Abort a non-blocking I2C Master transmission or reception.
- status_t [LPI2C_DRV_MasterReceiveData](#) (uint32_t instance, uint8_t *rxBuff, uint32_t rxSize, bool sendStop)
Perform a non-blocking receive transaction on the I2C bus.
- status_t [LPI2C_DRV_MasterReceiveDataBlocking](#) (uint32_t instance, uint8_t *rxBuff, uint32_t rxSize, bool sendStop, uint32_t timeout)
Perform a blocking receive transaction on the I2C bus.
- status_t [LPI2C_DRV_MasterGetTransferStatus](#) (uint32_t instance, uint32_t *bytesRemaining)
Return the current status of the I2C master transfer.
- void [LPI2C_DRV_MasterIRQHandler](#) (uint32_t instance)
Handle master operation when I2C interrupt occurs.

- status_t [LPI2C_DRV_SlaveInit](#) (uint32_t instance, const [lpi2c_slave_user_config_t](#) *userConfigPtr, [lpi2c_slave_state_t](#) *slave)

Initialize the I2C slave mode driver.
- status_t [LPI2C_DRV_SlaveDeinit](#) (uint32_t instance)

De-initialize the I2C slave mode driver.
- status_t [LPI2C_DRV_SlaveSetTxBuffer](#) (uint32_t instance, const uint8_t *txBuff, uint32_t txSize)

Provide a buffer for transmitting data.
- status_t [LPI2C_DRV_SlaveSetRxBuffer](#) (uint32_t instance, uint8_t *rxBuff, uint32_t rxSize)

Provide a buffer for receiving data.
- status_t [LPI2C_DRV_SlaveSendData](#) (uint32_t instance, const uint8_t *txBuff, uint32_t txSize)

Perform a non-blocking send transaction on the I2C bus.
- status_t [LPI2C_DRV_SlaveSendDataBlocking](#) (uint32_t instance, const uint8_t *txBuff, uint32_t txSize, uint32_t timeout)

Perform a blocking send transaction on the I2C bus.
- status_t [LPI2C_DRV_SlaveReceiveData](#) (uint32_t instance, uint8_t *rxBuff, uint32_t rxSize)

Perform a non-blocking receive transaction on the I2C bus.
- status_t [LPI2C_DRV_SlaveReceiveDataBlocking](#) (uint32_t instance, uint8_t *rxBuff, uint32_t rxSize, uint32_t timeout)

Perform a blocking receive transaction on the I2C bus.
- status_t [LPI2C_DRV_SlaveGetTransferStatus](#) (uint32_t instance, uint32_t *bytesRemaining)

Return the current status of the I2C slave transfer.
- status_t [LPI2C_DRV_SlaveAbortTransferData](#) (uint32_t instance)

Abort a non-blocking I2C Master transmission or reception.
- void [LPI2C_DRV_SlaveIRQHandler](#) (uint32_t instance)

Handle slave operation when I2C interrupt occurs.
- void [LPI2C_DRV_MasterGetDefaultConfig](#) ([lpi2c_master_user_config_t](#) *config)

Gets the default configuration structure for master.
- void [LPI2C_DRV_SlaveGetDefaultConfig](#) ([lpi2c_slave_user_config_t](#) *config)

Gets the default configuration structure for slave.
- void [LPI2C_DRV_SetMasterBusIdleTimeout](#) (uint32_t instance, uint16_t timeout)

Set bus idle timeout for LPI2C.

17.83.2 Data Structure Documentation

17.83.2.1 struct [lpi2c_master_user_config_t](#)

Defines the example structure.

This structure is used as an example.

Master configuration structure

This structure is used to provide configuration parameters for the LPI2C master at initialization time. Implements : [lpi2c_master_user_config_t_Class](#)

Definition at line 111 of file [lpi2c_driver.h](#).

Data Fields

- uint16_t [slaveAddress](#)
- bool [is10bitAddr](#)
- [lpi2c_mode_t](#) [operatingMode](#)
- uint32_t [baudRate](#)
- [lpi2c_transfer_type_t](#) [transferType](#)
- uint8_t [dmaChannel](#)
- [i2c_master_callback_t](#) [masterCallback](#)
- void * [callbackParam](#)

Field Documentation

17.83.2.1.1 uint32_t baudRate

The baud rate in hertz to use with current slave device

Definition at line 116 of file lpi2c_driver.h.

17.83.2.1.2 void* callbackParam

Parameter for the master callback function

Definition at line 127 of file lpi2c_driver.h.

17.83.2.1.3 uint8_t dmaChannel

Channel number for DMA channel. If DMA mode isn't used this field will be ignored.

Definition at line 122 of file lpi2c_driver.h.

17.83.2.1.4 bool is10bitAddr

Selects 7-bit or 10-bit slave address

Definition at line 114 of file lpi2c_driver.h.

17.83.2.1.5 i2c_master_callback_t masterCallback

Master callback function. Note that this function will be called from the interrupt service routine at the end of a transfer, so its execution time should be as small as possible. It can be NULL if you want to check manually the status of the transfer.

Definition at line 123 of file lpi2c_driver.h.

17.83.2.1.6 lpi2c_mode_t operatingMode

I2C Operating mode

Definition at line 115 of file lpi2c_driver.h.

17.83.2.1.7 uint16_t slaveAddress

Slave address, 7-bit or 10-bit

Definition at line 113 of file lpi2c_driver.h.

17.83.2.1.8 lpi2c_transfer_type_t transferType

Type of LPI2C transfer

Definition at line 121 of file lpi2c_driver.h.

17.83.2.2 struct lpi2c_slave_user_config_t

Slave configuration structure.

This structure is used to provide configuration parameters for the LPI2C slave at initialization time. Implements : lpi2c_slave_user_config_t_Class

Definition at line 136 of file lpi2c_driver.h.

Data Fields

- uint16_t [slaveAddress](#)
- bool [is10bitAddr](#)
- [lpi2c_mode_t](#) [operatingMode](#)

- bool [slaveListening](#)
- [lpi2c_transfer_type_t](#) transferType
- [uint8_t](#) dmaChannel
- [i2c_slave_callback_t](#) [slaveCallback](#)
- void * [callbackParam](#)

Field Documentation

17.83.2.2.1 void* callbackParam

Parameter for the slave callback function

Definition at line 149 of file [lpi2c_driver.h](#).

17.83.2.2.2 uint8_t dmaChannel

Channel number for DMA rx channel. If DMA mode isn't used this field will be ignored.

Definition at line 143 of file [lpi2c_driver.h](#).

17.83.2.2.3 bool is10bitAddr

Selects 7-bit or 10-bit slave address

Definition at line 139 of file [lpi2c_driver.h](#).

17.83.2.2.4 lpi2c_mode_t operatingMode

I2C Operating mode

Definition at line 140 of file [lpi2c_driver.h](#).

17.83.2.2.5 uint16_t slaveAddress

Slave address, 7-bit or 10-bit

Definition at line 138 of file [lpi2c_driver.h](#).

17.83.2.2.6 i2c_slave_callback_t slaveCallback

Slave callback function. Note that this function will be called from the interrupt service routine, so its execution time should be as small as possible. It can be NULL if the slave is not in listening mode ([slaveListening](#) = false)

Definition at line 144 of file [lpi2c_driver.h](#).

17.83.2.2.7 bool slaveListening

Slave mode (always listening or on demand only)

Definition at line 141 of file [lpi2c_driver.h](#).

17.83.2.2.8 lpi2c_transfer_type_t transferType

Type of LPI2C transfer

Definition at line 142 of file [lpi2c_driver.h](#).

17.83.2.3 struct lpi2c_baud_rate_params_t

Baud rate structure.

This structure is used for setting or getting the baud rate. Implements : [lpi2c_baud_rate_params_t_Class](#)

Definition at line 158 of file [lpi2c_driver.h](#).

Data Fields

- uint32_t [baudRate](#)

Field Documentation

17.83.2.3.1 uint32_t baudRate

Definition at line 160 of file lpi2c_driver.h.

17.83.2.4 struct lpi2c_master_state_t

Master internal context structure.

This structure is used by the master-mode driver for its internal logic. It must be provided by the application through the [LPI2C_DRV_MasterInit\(\)](#) function, then it cannot be freed until the driver is de-initialized using [LPI2C_DRV_MasterDeinit\(\)](#). The application should make no assumptions about the content of this structure.

Definition at line 200 of file lpi2c_driver.h.

17.83.2.5 struct lpi2c_slave_state_t

Slave internal context structure.

This structure is used by the slave-mode driver for its internal logic. It must be provided by the application through the [LPI2C_DRV_SlaveInit\(\)](#) function, then it cannot be freed until the driver is de-initialized using [LPI2C_DRV_SlaveDeinit\(\)](#). The application should make no assumptions about the content of this structure.

Definition at line 238 of file lpi2c_driver.h.

17.83.3 Enumeration Type Documentation

17.83.3.1 enum lpi2c_mode_t

I2C operating modes Implements : lpi2c_mode_t_Class.

Enumerator

LPI2C_STANDARD_MODE Standard-mode (Sm), bidirectional data transfers up to 100 kbit/s

LPI2C_FAST_MODE Fast-mode (Fm), bidirectional data transfers up to 400 kbit/s

Definition at line 71 of file lpi2c_driver.h.

17.83.3.2 enum lpi2c_transfer_type_t

Type of LPI2C transfer (based on interrupts or DMA). Implements : lpi2c_transfer_type_t_Class.

Enumerator

LPI2C_USING_DMA The driver will use DMA to perform I2C transfer

LPI2C_USING_INTERRUPTS The driver will use interrupts to perform I2C transfer

Definition at line 89 of file lpi2c_driver.h.

17.83.4 Function Documentation

17.83.4.1 status_t LPI2C_DRV_MasterAbortTransferData (uint32_t instance)

Abort a non-blocking I2C Master transmission or reception.

Parameters

<i>instance</i>	LPI2C peripheral instance number
-----------------	----------------------------------

Returns

Error or success status returned by API

Definition at line 1653 of file lpi2c_driver.c.

17.83.4.2 status_t LPI2C_DRV_MasterDeinit (uint32_t instance)

De-initialize the LPI2C master mode driver.

This function de-initializes the LPI2C driver in master mode. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

<i>instance</i>	LPI2C peripheral instance number
-----------------	----------------------------------

Returns

Error or success status returned by API

Definition at line 1221 of file lpi2c_driver.c.

17.83.4.3 void LPI2C_DRV_MasterGetBaudRate (uint32_t instance, lpi2c_baud_rate_params_t * baudRate)

Get the currently configured baud rate.

This function returns the currently configured baud rate.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>baudRate</i>	structure that contains the current baud rate in hertz and the baud rate in hertz for High-speed mode (unused in other modes, can be NULL)

Definition at line 1285 of file lpi2c_driver.c.

17.83.4.4 void LPI2C_DRV_MasterGetDefaultConfig (lpi2c_master_user_config_t * config)

Gets the default configuration structure for master.

The default configuration structure is:

Parameters

<i>config</i>	Pointer to configuration structure
---------------	------------------------------------

Definition at line 1879 of file lpi2c_driver.c.

17.83.4.5 status_t LPI2C_DRV_MasterGetTransferStatus (uint32_t instance, uint32_t * bytesRemaining)

Return the current status of the I2C master transfer.

This function can be called during a non-blocking transmission to check the status of the transfer.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>bytesRemaining</i>	the number of remaining bytes in the active I2C transfer

Returns

Error or success status returned by API

Definition at line 1837 of file lpi2c_driver.c.

17.83.4.6 `status_t LPI2C_DRV_MasterInit (uint32_t instance, const lpi2c_master_user_config_t * userConfigPtr, lpi2c_master_state_t * master)`

Initialize the LPI2C master mode driver.

This function initializes the LPI2C driver in master mode.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>userConfigPtr</i>	Pointer to the LPI2C master user configuration structure. The function reads configuration data from this structure and initializes the driver accordingly. The application may free this structure after the function returns.
<i>master</i>	Pointer to the LPI2C master driver context structure. The driver uses this memory area for its internal logic. The application must make no assumptions about the content of this structure, and must not free this memory until the driver is de-initialized using LPI2C_DRV_MasterDeinit() .

Returns

Error or success status returned by API

Definition at line 1136 of file lpi2c_driver.c.

17.83.4.7 `void LPI2C_DRV_MasterIRQHandler (uint32_t instance)`

Handle master operation when I2C interrupt occurs.

This is the interrupt service routine for the LPI2C master mode driver. It handles the rest of the transfer started by one of the send/receive functions.

Parameters

<i>instance</i>	LPI2C peripheral instance number
-----------------	----------------------------------

Definition at line 1897 of file lpi2c_driver.c.

17.83.4.8 `status_t LPI2C_DRV_MasterReceiveData (uint32_t instance, uint8_t * rxBuff, uint32_t rxSize, bool sendStop)`

Perform a non-blocking receive transaction on the I2C bus.

This function starts the reception of a block of data from the currently configured slave address and returns immediately. The rest of the reception is handled by the interrupt service routine. Use [LPI2C_DRV_MasterGetReceiveStatus\(\)](#) to check the progress of the reception.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred

<i>sendStop</i>	specifies whether or not to generate stop condition after the reception
-----------------	---

Returns

Error or success status returned by API

Definition at line 1686 of file lpi2c_driver.c.

17.83.4.9 `status_t LPI2C_DRV_MasterReceiveDataBlocking (uint32_t instance, uint8_t * rxBuff, uint32_t rxSize, bool sendStop, uint32_t timeout)`

Perform a blocking receive transaction on the I2C bus.

This function receives a block of data from the currently configured slave address, and only returns when the transmission is complete.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred
<i>sendStop</i>	specifies whether or not to generate stop condition after the reception
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 1782 of file lpi2c_driver.c.

17.83.4.10 `status_t LPI2C_DRV_MasterSendData (uint32_t instance, const uint8_t * txBuff, uint32_t txSize, bool sendStop)`

Perform a non-blocking send transaction on the I2C bus.

This function starts the transmission of a block of data to the currently configured slave address and returns immediately. The rest of the transmission is handled by the interrupt service routine. Use LPI2C_DRV_MasterGetSendStatus() to check the progress of the transmission.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred
<i>sendStop</i>	specifies whether or not to generate stop condition after the transmission

Returns

Error or success status returned by API

Definition at line 1532 of file lpi2c_driver.c.

17.83.4.11 `status_t LPI2C_DRV_MasterSendDataBlocking (uint32_t instance, const uint8_t * txBuff, uint32_t txSize, bool sendStop, uint32_t timeout)`

Perform a blocking send transaction on the I2C bus.

This function sends a block of data to the currently configured slave address, and only returns when the transmission is complete.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred
<i>sendStop</i>	specifies whether or not to generate stop condition after the transmission
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 1613 of file lpi2c_driver.c.

17.83.4.12 `status_t LPI2C_DRV_MasterSetBaudRate (uint32_t instance, const lpi2c_mode_t operatingMode, const lpi2c_baud_rate_params_t baudRate)`

Set the baud rate for any subsequent I2C communication.

This function sets the baud rate (SCL frequency) for the I2C master. It can also change the operating mode. If the operating mode is High-Speed, a second baud rate must be provided for high-speed communication. Note that due to module limitation not any baud rate can be achieved. The driver will set a baud rate as close as possible to the requested baud rate, but there may still be substantial differences, for example if requesting a high baud rate while using a low-frequency protocol clock for the LPI2C module. The application should call [LPI2C_DRV_MasterGetBaudRate\(\)](#) after [LPI2C_DRV_MasterSetBaudRate\(\)](#) to check what baud rate was actually set.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>operatingMode</i>	I2C operating mode
<i>baudRate</i>	structure that contains the baud rate in hertz to use by current slave device and also the baud rate in hertz for High-speed mode (unused in other modes)

Returns

Error or success status returned by API

Definition at line 1337 of file lpi2c_driver.c.

17.83.4.13 `void LPI2C_DRV_MasterSetSlaveAddr (uint32_t instance, const uint16_t address, const bool is10bitAddr)`

Set the slave address for any subsequent I2C communication.

This function sets the slave address which will be used for any future transfer initiated by the LPI2C master.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>address</i>	slave address, 7-bit or 10-bit
<i>is10bitAddr</i>	specifies if provided address is 10-bit

Definition at line 1511 of file lpi2c_driver.c.

17.83.4.14 `void LPI2C_DRV_SetMasterBusIdleTimeout (uint32_t instance, uint16_t timeout)`

Set bus idle timeout for LPI2C.

This function sets time out for bus idle for Master. If both SCL and SDA are high for longer than Timeout cycles, then the I2C bus is assumed to be idle and the master can generate a START condition

Parameters

<i>baseAddr</i>	base address of the LPI2C module
<i>timeout</i>	bus idle timeout period in clock cycle. Zero means no bus idle timeout

Definition at line 1253 of file lpi2c_driver.c.

17.83.4.15 `status_t LPI2C_DRV_SlaveAbortTransferData (uint32_t instance)`

Abort a non-blocking I2C Master transmission or reception.

Parameters

<i>instance</i>	LPI2C peripheral instance number
-----------------	----------------------------------

Returns

Error or success status returned by API

Definition at line 2524 of file lpi2c_driver.c.

17.83.4.16 `status_t LPI2C_DRV_SlaveDeinit (uint32_t instance)`

De-initialize the I2C slave mode driver.

This function de-initializes the LPI2C driver in slave mode. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

<i>instance</i>	LPI2C peripheral instance number
-----------------	----------------------------------

Returns

Error or success status returned by API

Definition at line 2153 of file lpi2c_driver.c.

17.83.4.17 `void LPI2C_DRV_SlaveGetDefaultConfig (lpi2c_slave_user_config_t * config)`

Gets the default configuration structure for slave.

The default configuration structure is:

Parameters

<i>config</i>	Pointer to configuration structure
---------------	------------------------------------

Definition at line 2551 of file lpi2c_driver.c.

17.83.4.18 `status_t LPI2C_DRV_SlaveGetTransferStatus (uint32_t instance, uint32_t * bytesRemaining)`

Return the current status of the I2C slave transfer.

This function can be called during a non-blocking transmission to check the status of the transfer.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>bytesRemaining</i>	the number of remaining bytes in the active I2C transfer

Returns

Error or success status returned by API

Definition at line 2485 of file lpi2c_driver.c.

```
17.83.4.19 status_t LPI2C_DRV_SlaveInit ( uint32_t instance, const lpi2c_slave_user_config_t * userConfigPtr,  
lpi2c_slave_state_t * slave )
```

Initialize the I2C slave mode driver.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>userConfigPtr</i>	Pointer to the LPI2C slave user configuration structure. The function reads configuration data from this structure and initializes the driver accordingly. The application may free this structure after the function returns.
<i>slave</i>	Pointer to the LPI2C slave driver context structure. The driver uses this memory area for its internal logic. The application must make no assumptions about the content of this structure, and must not free this memory until the driver is de-initialized using LPI2C_DRV_Slave↔Deinit() .

Returns

Error or success status returned by API

Definition at line 2032 of file lpi2c_driver.c.

17.83.4.20 void LPI2C_DRV_SlaveIRQHandler (uint32_t *instance*)

Handle slave operation when I2C interrupt occurs.

This is the interrupt service routine for the LPI2C slave mode driver. It handles any transfer initiated by an I2C master and notifies the application via the provided callback when relevant events occur.

Parameters

<i>instance</i>	LPI2C peripheral instance number
-----------------	----------------------------------

Definition at line 2606 of file lpi2c_driver.c.

17.83.4.21 status_t LPI2C_DRV_SlaveReceiveData (uint32_t *instance*, uint8_t * *rxBuff*, uint32_t *rxSize*)

Perform a non-blocking receive transaction on the I2C bus.

Performs a non-blocking receive transaction on the I2C bus when the slave is not in listening mode (initialized with slaveListening = false). It starts the reception and returns immediately. The rest of the reception is handled by the interrupt service routine. Use LPI2C_DRV_SlaveGetReceiveStatus() to check the progress of the reception.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 2370 of file lpi2c_driver.c.

17.83.4.22 status_t LPI2C_DRV_SlaveReceiveDataBlocking (uint32_t *instance*, uint8_t * *rxBuff*, uint32_t *rxSize*, uint32_t *timeout*)

Perform a blocking receive transaction on the I2C bus.

Performs a blocking receive transaction on the I2C bus when the slave is not in listening mode (initialized with slaveListening = false). It sets up the reception and then waits for the transfer to complete before returning.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>rxBuff</i>	pointer to the buffer where to store received data
<i>rxSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 2443 of file lpi2c_driver.c.

17.83.4.23 `status_t LPI2C_DRV_SlaveSendData (uint32_t instance, const uint8_t * txBuff, uint32_t txSize)`

Perform a non-blocking send transaction on the I2C bus.

Performs a non-blocking send transaction on the I2C bus when the slave is not in listening mode (initialized with slaveListening = false). It starts the transmission and returns immediately. The rest of the transmission is handled by the interrupt service routine. Use LPI2C_DRV_SlaveGetTransmitStatus() to check the progress of the transmission.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 2246 of file lpi2c_driver.c.

17.83.4.24 `status_t LPI2C_DRV_SlaveSendDataBlocking (uint32_t instance, const uint8_t * txBuff, uint32_t txSize, uint32_t timeout)`

Perform a blocking send transaction on the I2C bus.

Performs a blocking send transaction on the I2C bus when the slave is not in listening mode (initialized with slaveListening = false). It sets up the transmission and then waits for the transfer to complete before returning.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred
<i>timeout</i>	timeout for the transfer in milliseconds

Returns

Error or success status returned by API

Definition at line 2332 of file lpi2c_driver.c.

17.83.4.25 `status_t LPI2C_DRV_SlaveSetRxBuffer (uint32_t instance, uint8_t * rxBuff, uint32_t rxSize)`

Provide a buffer for receiving data.

This function provides a buffer in which the LPI2C slave-mode driver can store received data. It can be called for example from the user callback provided at initialization time, when the driver reports events LPI2C_SLAVE_EVENT_RX_REQ or LPI2C_SLAVE_EVENT_RX_FULL.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>rxBuff</i>	pointer to the data to be transferred
<i>rxSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 2219 of file lpi2c_driver.c.

17.83.4.26 `status_t LPI2C_DRV_SlaveSetTxBuffer (uint32_t instance, const uint8_t * txBuff, uint32_t txSize)`

Provide a buffer for transmitting data.

This function provides a buffer from which the LPI2C slave-mode driver can transmit data. It can be called for example from the user callback provided at initialization time, when the driver reports events LPI2C_SLAVE_EVENT_TX_REQ or LPI2C_SLAVE_EVENT_TX_EMPTY.

Parameters

<i>instance</i>	LPI2C peripheral instance number
<i>txBuff</i>	pointer to the data to be transferred
<i>txSize</i>	length in bytes of the data to be transferred

Returns

Error or success status returned by API

Definition at line 2192 of file lpi2c_driver.c.

17.84 LPIT Driver

17.84.1 Detailed Description

Low Power Interrupt Timer Peripheral Driver.

Hardware background

Each LPIT timer channel can be configured to run in one of 4 modes:

32-bit Periodic Counter: In this mode the counter will load and then decrement down to zero. It will then set the timer interrupt flag and assert the output pre-trigger.

Dual 16-bit Periodic Counter: In this mode, the counter will load and then the lower 16-bits will decrement down to zero, which will assert the output pre-trigger. The upper 16-bits will then decrement down to zero, which will negate the output pre-trigger and set the timer interrupt flag.

32-bit Trigger Accumulator: In this mode, the counter will load on the first trigger rising edge and then decrement down to zero on each trigger rising edge. It will then set the timer interrupt flag and assert the output pre-trigger.

32-bit Trigger Input Capture: In this mode, the counter will load with 0xFFFF_FFFF and then decrement down to zero. If a trigger rising edge is detected, it will store the inverse of the current counter value in the load value register, set the timer interrupt flag and assert the output pre-trigger.

In these modes, the timer channel operation is further controlled by Trigger Control bits (TSOT, TSOI, TROT) which control the load, reload, start and restart of the timer channels.

Driver consideration

The Driver uses structures for configuration. Each structure contains members that are specific to its respective functionality. There are [lpit_user_config_t](#) and [lpit_user_channel_config_t](#).

Interrupt handling

Each LPIT timer channel has a corresponding interrupt handler. The LPIT Driver does not define interrupt handler internally. These interrupt handler methods can be defined by the user application. There are two ways to add an LPIT interrupt handler:

1. Using the weak symbols defined by start-up code. If the methods `LPITx_Handler(void)` (x denotes instance number) are not defined, the linker use a default ISR. An error will be generated if methods with the same name are defined multiple times. This method works regardless of the placement of the interrupt vector table (Flash or RAM).
2. Using the Interrupt Manager's `INT_SYS_InstallHandler()` method. This can be used to dynamically change the ISR at run-time. This method works only if the interrupt vector table is located in RAM.

Clocking configuration

The LPIT Driver does not handle clock setup (from PCC) configuration. This is handled by the Clock Manager. The driver assumes that clock configurations have been made, so it is the user's responsibility to set up clocking and pin configurations correctly.

Basic operations

1. Pre-Initialization information of LPIT module
 - Before using the LPIT driver, the protocol clock of the module must be configured by the application using PCC module.
 - Configures Trigger MUX Control (TRGMUX) if want to use external trigger for LPIT module.
 - Configures different peripherals if want to use them in LPIT interrupt routine.
 - Provides configuration data structure to LPIT initialization API.
2. To initialize the LPIT module, just call the [LPIT_DRV_Init\(\)](#) function with the user configuration data structure. This function configures LPIT module operation when MCU enters DEBUG and DOZE (Low power mode) modes and enables LPIT module. This function must be called firstly.

In the following code, LPIT module is initialized to continue to run when MCU enters both Debug and DOZE modes.

```
#define BOARD_LPIT_INSTANCE OU
/* LPIT module configuration structure */
lpit_user_config_t lpitconfig =
{
    .enableRunInDebug = true,
    .enableRunInDoze = true
};
/* Initializes the LPIT module. */
LPIT_DRV_Init(BOARD_LPIT_INSTANCE, &lpitconfig);
```

3. After calling the `LPIT_DRV_Init()` function, call `LPIT_DRV_InitChannel()` function with user channel configuration structure to initialize timer channel.

This function configures timer channel chaining, timer channel mode, timer channel period, interrupt generation, trigger source, trigger select, reload on trigger, stop on interrupt and start on trigger. In the following code, timer channel is initialized with the channel chaining is disabled, interrupt generation is enabled, operation mode is 32 bit periodic counter mode, trigger source is external, reload on trigger is disabled, stop on interrupt is disabled, start on trigger is disabled and timer period is 1 second. Note that:

- Trigger select is not effective if trigger source is external.
- Timer channel period must be suitable for operation mode.
- The timer channel 0 can not be chained.

```
/* Channel 0 configuration structure */
lpit_user_channel_config_t chnlconfig =
{
    .timerMode = LPIT_PERIODIC_COUNTER,
    .periodUnits = LPIT_PERIOD_UNITS_MICROSECONDS,
    .period = 1000000U,
    .triggerSource = LPIT_TRIGGER_SOURCE_INTERNAL,
    .triggerSelect = 1U,
    .enableReloadOnTrigger = false,
    .enableStopOnInterrupt = false,
    .enableStartOnTrigger = false,
    .chainChannel = false,
    .isInterruptEnabled = true
};
/* Initializes the channel 0 */
LPIT_DRV_InitChannel(BOARD_LPIT_INSTANCE, 0, &chnlconfig);
```

4. To reconfigure timer channel period, just call `LPIT_DRV_SetTimerPeriodByUs()` or `LPIT_DRV_SetTimerPeriodByCount()` with corresponding new period. In the following code, the timer channel period is reconfigured with new period in count unit.

```
/* Reconfigures timer channel period with new period of 10000 count*/
LPIT_DRV_SetTimerPeriodByCount(BOARD_LPIT_INSTANCE, 0, 10000);
```

5. To start timer channel counting, just call `LPIT_DRV_StartTimerChannels()` with timer channels starting mask. In the following code, the timer channel 0 is started with the mask of 0x1U.

```
/* Starts channel 0 counting*/
LPIT_DRV_StartTimerChannels(BOARD_LPIT_INSTANCE, 0x1U);
```

6. To stop timer channel counting, just call `LPIT_DRV_StopTimerChannels()` with timer channels stopping mask. In the following code, the timer channel 0 is stopped with the mask of 0x1U.

```
/* Stops channel 0 counting*/
LPIT_DRV_StopTimerChannels(BOARD_LPIT_INSTANCE, 0x1U);
```

7. To disable LPIT module, just call `LPIT_DRV_Deinit()`.

```
/* Disables LPIT module*/
LPIT_DRV_Deinit(BOARD_LPIT_INSTANCE);
```

API

Some of the features exposed by the API are targeted specifically for timer channel mode. For example, set/get timer period in dual 16 mode function makes sense if timer channel mode is dual 16 mode, so therefor it is restricted for use in other modes.

For any invalid configuration the functions will either return an error code or trigger DEV_ASSERT (if enabled). For more details, please refer to each function description.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\lpit_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager Interrupt Manager \(Interrupt\)](#)

Data Structures

- struct [lpit_user_config_t](#)
LPIT configuration structure. [More...](#)
- struct [lpit_user_channel_config_t](#)
Structure to configure the channel timer. [More...](#)

Macros

- #define [MAX_PERIOD_COUNT](#) (0xFFFFFFFFU)
Max period in count of all operation mode except for dual 16 bit periodic counter mode.
- #define [MAX_PERIOD_COUNT_IN_DUAL_16BIT_MODE](#) (0x1FFFEU)
Max period in count of dual 16 bit periodic counter mode.
- #define [MAX_PERIOD_COUNT_16_BIT](#) (0xFFFFU)
Max count of 16 bit.

Enumerations

- enum [lpit_timer_modes_t](#) { [LPIT_PERIODIC_COUNTER](#) = 0x00U, [LPIT_DUAL_PERIODIC_COUNTER](#) = 0x01U, [LPIT_TRIGGER_ACCUMULATOR](#) = 0x02U, [LPIT_INPUT_CAPTURE](#) = 0x03U }
Mode options available for the LPIT timer Implements : [lpit_timer_modes_t](#) Class.
- enum [lpit_trigger_source_t](#) { [LPIT_TRIGGER_SOURCE_EXTERNAL](#) = 0x00U, [LPIT_TRIGGER_SOURCE_INTERNAL](#) = 0x01U }
Trigger source options.
- enum [lpit_period_units_t](#) { [LPIT_PERIOD_UNITS_COUNTS](#) = 0x00U, [LPIT_PERIOD_UNITS_MICROSECONDS](#) = 0x01U }
Unit options for LPIT period.

Initialization and De-initialization

- void [LPIT_DRV_GetDefaultConfig](#) ([lpit_user_config_t](#) *const config)
Gets the default LPIT configuration.
- void [LPIT_DRV_GetDefaultChanConfig](#) ([lpit_user_channel_config_t](#) *const config)
Gets the default timer channel configuration.
- void [LPIT_DRV_Init](#) (uint32_t instance, const [lpit_user_config_t](#) *userConfig)
Initializes the LPIT module.
- void [LPIT_DRV_Deinit](#) (uint32_t instance)
De-Initializes the LPIT module.
- status_t [LPIT_DRV_InitChannel](#) (uint32_t instance, uint32_t channel, const [lpit_user_channel_config_t](#) *userChannelConfig)
Initializes the LPIT channel.

Timer Start and Stop

- void [LPIT_DRV_StartTimerChannels](#) (uint32_t instance, uint32_t mask)
Starts the timer channel counting.
- void [LPIT_DRV_StopTimerChannels](#) (uint32_t instance, uint32_t mask)
Stops the timer channel counting.

Timer Period

- status_t [LPIT_DRV_SetTimerPeriodByUs](#) (uint32_t instance, uint32_t channel, uint32_t periodUs)
Sets the timer channel period in microseconds.
- status_t [LPIT_DRV_SetTimerPeriodInDual16ModeByUs](#) (uint32_t instance, uint32_t channel, uint16_t periodHigh, uint16_t periodLow)
Sets the timer channel period in microseconds.
- uint64_t [LPIT_DRV_GetTimerPeriodByUs](#) (uint32_t instance, uint32_t channel)
Gets the timer channel period in microseconds.
- uint64_t [LPIT_DRV_GetCurrentTimerUs](#) (uint32_t instance, uint32_t channel)
Gets the current timer channel counting value in microseconds.
- void [LPIT_DRV_SetTimerPeriodByCount](#) (uint32_t instance, uint32_t channel, uint32_t count)
Sets the timer channel period in count unit.
- void [LPIT_DRV_SetTimerPeriodInDual16ModeByCount](#) (uint32_t instance, uint32_t channel, uint16_t periodHigh, uint16_t periodLow)
Sets the timer channel period in count unit.
- uint32_t [LPIT_DRV_GetTimerPeriodByCount](#) (uint32_t instance, uint32_t channel)
Gets the current timer channel period in count unit.
- uint32_t [LPIT_DRV_GetCurrentTimerCount](#) (uint32_t instance, uint32_t channel)
Gets the current timer channel counting value in count.

Interrupt

- void [LPIT_DRV_EnableTimerChannelInterrupt](#) (uint32_t instance, uint32_t mask)
Enables the interrupt generation of timer channel.
- void [LPIT_DRV_DisableTimerChannelInterrupt](#) (uint32_t instance, uint32_t mask)
Disables the interrupt generation of timer channel.
- uint32_t [LPIT_DRV_GetInterruptFlagTimerChannels](#) (uint32_t instance, uint32_t mask)
Gets the current interrupt flag of timer channels.
- void [LPIT_DRV_ClearInterruptFlagTimerChannels](#) (uint32_t instance, uint32_t mask)
Clears the interrupt flag of timer channels.

17.84.2 Data Structure Documentation

17.84.2.1 struct `lpit_user_config_t`

LPIT configuration structure.

This structure holds the configuration settings for the LPIT peripheral to enable or disable LPIT module in DEBUG and DOZE mode Implements : `lpit_user_config_t_Class`

Definition at line 108 of file `lpit_driver.h`.

Data Fields

- bool `enableRunInDebug`
- bool `enableRunInDoze`

Field Documentation

17.84.2.1.1 bool `enableRunInDebug`

True: Timer channels continue to run in debug mode False: Timer channels stop in debug mode

Definition at line 110 of file `lpit_driver.h`.

17.84.2.1.2 bool `enableRunInDoze`

True: Timer channels continue to run in doze mode False: Timer channels stop in doze mode

Definition at line 112 of file `lpit_driver.h`.

17.84.2.2 struct `lpit_user_channel_config_t`

Structure to configure the channel timer.

This structure holds the configuration settings for the LPIT timer channel Implements : `lpit_user_channel_config_t_Class`

Definition at line 121 of file `lpit_driver.h`.

Data Fields

- `lpit_timer_modes_t` `timerMode`
- `lpit_period_units_t` `periodUnits`
- `uint32_t` `period`
- `lpit_trigger_source_t` `triggerSource`
- `uint32_t` `triggerSelect`
- bool `enableReloadOnTrigger`
- bool `enableStopOnInterrupt`
- bool `enableStartOnTrigger`
- bool `chainChannel`
- bool `isInterruptEnabled`

Field Documentation

17.84.2.2.1 bool `chainChannel`

Channel chaining enable

Definition at line 137 of file `lpit_driver.h`.

17.84.2.2.2 bool `enableReloadOnTrigger`

True: Timer channel will reload on selected trigger False: Timer channel will not reload on selected trigger

Definition at line 129 of file `lpit_driver.h`.

17.84.2.2.3 bool enableStartOnTrigger

True: Timer channel starts to decrement when rising edge on selected trigger is detected. False: Timer starts to decrement immediately based on restart condition

Definition at line 133 of file lpit_driver.h.

17.84.2.2.4 bool enableStopOnInterrupt

True: Timer will stop after timeout False: Timer channel does not stop after timeout

Definition at line 131 of file lpit_driver.h.

17.84.2.2.5 bool isInterruptEnabled

Timer channel interrupt generation enable

Definition at line 138 of file lpit_driver.h.

17.84.2.2.6 uint32_t period

Period of timer channel

Definition at line 125 of file lpit_driver.h.

17.84.2.2.7 lpit_period_units_t periodUnits

Timer period value units

Definition at line 124 of file lpit_driver.h.

17.84.2.2.8 lpit_timer_modes_t timerMode

Operation mode of timer channel

Definition at line 123 of file lpit_driver.h.

17.84.2.2.9 uint32_t triggerSelect

Selects one trigger from the internal trigger sources this field makes sense if trigger source is internal

Definition at line 127 of file lpit_driver.h.

17.84.2.2.10 lpit_trigger_source_t triggerSource

Selects between internal and external trigger sources

Definition at line 126 of file lpit_driver.h.

17.84.3 Macro Definition Documentation**17.84.3.1 #define MAX_PERIOD_COUNT (0xFFFFFFFFU)**

Max period in count of all operation mode except for dual 16 bit periodic counter mode.

Definition at line 58 of file lpit_driver.h.

17.84.3.2 #define MAX_PERIOD_COUNT_16_BIT (0xFFFFU)

Max count of 16 bit.

Definition at line 62 of file lpit_driver.h.

17.84.3.3 #define MAX_PERIOD_COUNT_IN_DUAL_16BIT_MODE (0x1FFFEU)

Max period in count of dual 16 bit periodic counter mode.

Definition at line 60 of file lpit_driver.h.

17.84.4 Enumeration Type Documentation

17.84.4.1 enum lpit_period_units_t

Unit options for LPIT period.

This is used to determine unit of timer period Implements : lpit_period_units_t_Class

Enumerator

LPIT_PERIOD_UNITS_COUNTS Period value unit is count

LPIT_PERIOD_UNITS_MICROSECONDS Period value unit is microsecond

Definition at line 95 of file lpit_driver.h.

17.84.4.2 enum lpit_timer_modes_t

Mode options available for the LPIT timer Implements : lpit_timer_modes_t_Class.

Enumerator

LPIT_PERIODIC_COUNTER 32-bit Periodic Counter

LPIT_DUAL_PERIODIC_COUNTER Dual 16-bit Periodic Counter

LPIT_TRIGGER_ACCUMULATOR 32-bit Trigger Accumulator

LPIT_INPUT_CAPTURE 32-bit Trigger Input Capture

Definition at line 68 of file lpit_driver.h.

17.84.4.3 enum lpit_trigger_source_t

Trigger source options.

This is used for both internal and external trigger sources. The actual trigger options available is SoC specific, user should refer to the reference manual. Implements : lpit_trigger_source_t_Class

Enumerator

LPIT_TRIGGER_SOURCE_EXTERNAL Use external trigger

LPIT_TRIGGER_SOURCE_INTERNAL Use internal trigger

Definition at line 83 of file lpit_driver.h.

17.84.5 Function Documentation

17.84.5.1 void LPIT_DRV_ClearInterruptFlagTimerChannels (uint32_t instance, uint32_t mask)

Clears the interrupt flag of timer channels.

This function clears the interrupt flag of timer channels after their interrupt event occurred.

Parameters

<i>in</i>	<i>instance</i>	LPIT module instance number
<i>in</i>	<i>mask</i>	<p>The interrupt flag clearing mask that decides which channels will be cleared interrupt flag</p> <ul style="list-style-type: none"> • For example: <ul style="list-style-type: none"> – with mask = 0x01u then the interrupt flag of channel 0 only will be cleared – with mask = 0x02u then the interrupt flag of channel 1 only will be cleared – with mask = 0x03u then the interrupt flags of channel 0 and channel 1 will be cleared

Definition at line 744 of file lpit_driver.c.

17.84.5.2 void LPIT_DRV_Deinit (uint32_t instance)

De-Initializes the LPIT module.

This function disables LPIT module. In order to use the LPIT module again, LPIT_DRV_Init must be called.

Parameters

<i>in</i>	<i>instance</i>	LPIT module instance number
-----------	-----------------	-----------------------------

Definition at line 177 of file lpit_driver.c.

17.84.5.3 void LPIT_DRV_DisableTimerChannelInterrupt (uint32_t instance, uint32_t mask)

Disables the interrupt generation of timer channel.

This function allows disabling interrupt generation of timer channel when timeout occurs or input trigger occurs.

Parameters

<i>in</i>	<i>instance</i>	LPIT module instance number
<i>in</i>	<i>mask</i>	<p>The mask that decides which channels will be disable interrupt.</p> <ul style="list-style-type: none"> • For example: <ul style="list-style-type: none"> – with mask = 0x01u then the interrupt of channel 0 will be disable – with mask = 0x02u then the interrupt of channel 1 will be disable – with mask = 0x03u then the interrupt of channel 0 and channel 1 will be disable

Definition at line 701 of file lpit_driver.c.

17.84.5.4 void LPIT_DRV_EnableTimerChannelInterrupt (uint32_t instance, uint32_t mask)

Enables the interrupt generation of timer channel.

This function allows enabling interrupt generation of timer channel when timeout occurs or input trigger occurs.

Parameters

<i>in</i>	<i>instance</i>	LPIT module instance number.
-----------	-----------------	------------------------------

<i>in</i>	<i>mask</i>	<p>The mask that decides which channels will be enabled interrupt.</p> <ul style="list-style-type: none"> • For example: <ul style="list-style-type: none"> – with mask = 0x01u then the interrupt of channel 0 will be enabled – with mask = 0x02u then the interrupt of channel 1 will be enabled – with mask = 0x03u then the interrupt of channel 0 and channel 1 will be enabled
-----------	-------------	--

Definition at line 680 of file lpit_driver.c.

17.84.5.5 uint32_t LPIT_DRV_GetCurrentTimerCount (uint32_t *instance*, uint32_t *channel*)

Gets the current timer channel counting value in count.

This function returns the real-time timer channel counting value, the value in a range from 0 to timer channel period. Need to make sure the running time does not exceed the timer channel period.

Parameters

<i>in</i>	<i>instance</i>	LPIT module instance number
<i>in</i>	<i>channel</i>	Timer channel number

Returns

Current timer channel counting value in count

Definition at line 648 of file lpit_driver.c.

17.84.5.6 uint64_t LPIT_DRV_GetCurrentTimerUs (uint32_t *instance*, uint32_t *channel*)

Gets the current timer channel counting value in microseconds.

This function returns an absolute time stamp in microseconds. One common use of this function is to measure the running time of a part of code. Call this function at both the beginning and end of code. The time difference between these two time stamps is the running time. The return counting value here makes sense if the operation mode of timer channel is 32 bit periodic counter or dual 16 bit periodic counter or 32-bit trigger input capture. Need to make sure the running time will not exceed the timer channel period.

Parameters

<i>in</i>	<i>instance</i>	LPIT module instance number
<i>in</i>	<i>channel</i>	Timer channel number

Returns

Current timer channel counting value in microseconds

Definition at line 512 of file lpit_driver.c.

17.84.5.7 void LPIT_DRV_GetDefaultChanConfig (lpit_user_channel_config_t *const *config*)

Gets the default timer channel configuration.

This function gets the default timer channel configuration structure, with the following settings:

- Timer mode: 32-bit Periodic Counter
- Period unit: Period value unit is microsecond
- Period: 1000000 microseconds(1 second)
- Trigger sources: External trigger

- Trigger select: Trigger from channel 0
- Reload on trigger: Disable
- Stop on interrupt : Disable
- Start on trigger: Disable
- Channel chaining: Disable
- Interrupt generating: Enable

Parameters

out	<i>config</i>	The channel configuration structure
-----	---------------	-------------------------------------

Definition at line 102 of file lpit_driver.c.

17.84.5.8 void LPIT_DRV_GetDefaultConfig (lpit_user_config_t *const config)

Gets the default LPIT configuration.

This function gets default LPIT module configuration structure, with the following settings:

- PIT runs in debug mode: Disable
- PIT runs in doze mode: Disable

Parameters

out	<i>config</i>	The configuration structure
-----	---------------	-----------------------------

Definition at line 87 of file lpit_driver.c.

17.84.5.9 uint32_t LPIT_DRV_GetInterruptFlagTimerChannels (uint32_t instance, uint32_t mask)

Gets the current interrupt flag of timer channels.

This function gets the current interrupt flag of timer channels. In compare modes, the flag sets to 1 at the end of the timer period. In capture modes, the flag sets to 1 when the trigger asserts.

Parameters

in	<i>instance</i>	LPIT module instance number.
in	<i>mask</i>	<p>The interrupt flag getting mask that decides which channels will be got interrupt flag.</p> <ul style="list-style-type: none"> • For example: <ul style="list-style-type: none"> – with mask = 0x01u then the interrupt flag of channel 0 only will be got – with mask = 0x02u then the interrupt flag of channel 1 only will be got – with mask = 0x03u then the interrupt flags of channel 0 and channel 1 will be got

Returns

Current the interrupt flag of timer channels

Definition at line 723 of file lpit_driver.c.

17.84.5.10 `uint32_t LPIT_DRV_GetTimerPeriodByCount (uint32_t instance, uint32_t channel)`

Gets the current timer channel period in count unit.

This function returns current period of timer channel given as argument.

Parameters

in	<i>instance</i>	LPIT module instance number
in	<i>channel</i>	Timer channel number

Returns

Timer channel period in count unit

Definition at line 614 of file lpit_driver.c.

17.84.5.11 `uint64_t LPIT_DRV_GetTimerPeriodByUs (uint32_t instance, uint32_t channel)`

Gets the timer channel period in microseconds.

This function gets the timer channel period in microseconds. The returned period here makes sense if the operation mode of timer channel is 32 bit periodic counter or dual 16 bit periodic counter.

Parameters

in	<i>instance</i>	LPIT module instance number
in	<i>channel</i>	Timer channel number

Returns

Timer channel period in microseconds

Definition at line 453 of file lpit_driver.c.

17.84.5.12 `void LPIT_DRV_Init (uint32_t instance, const lpit_user_config_t * userConfig)`

Initializes the LPIT module.

This function resets LPIT module, enables the LPIT module, configures LPIT module operation in Debug and DOZE mode. The LPIT configuration structure shall be passed as arguments. This configuration structure affects all timer channels. This function should be called before calling any other LPIT driver function.

This is an example demonstrating how to define a LPIT configuration structure:

```
1 lpit_user_config_t lpitInit =
2 {
3     .enableRunInDebug = false,
4     .enableRunInDoze = true
5 };
```

Parameters

in	<i>instance</i>	LPIT module instance number.
in	<i>userConfig</i>	Pointer to LPIT configuration structure.

Definition at line 130 of file lpit_driver.c.

17.84.5.13 `status_t LPIT_DRV_InitChannel (uint32_t instance, uint32_t channel, const lpit_user_channel_config_t * userChannelConfig)`

Initializes the LPIT channel.

This function initializes the LPIT timers by using a channel, this function configures timer channel chaining, timer channel mode, timer channel period, interrupt generation, trigger source, trigger select, reload on trigger, stop on interrupt and start on trigger. The timer channel number and its configuration structure shall be passed as arguments. Timer channels do not start counting by default after calling this function. The function LPIT_DRV_StartTimerChannels must be called to start the timer channel counting. In order to re-configures the period, call the LPIT_DRV_SetTimerPeriodByUs or LPIT_DRV_SetTimerPeriodByCount.

This is an example demonstrating how to define a LPIT channel configuration structure:

```

1 lpit_user_channel_config_t lpitTestInit =
2 {
3     .timerMode = LPIT_PERIODIC_COUNTER,
4     .periodUnits = LPTT_PERIOD_UNITS_MICROSECONDS,
5     .period = 1000000U,
6     .triggerSource = LPIT_TRIGGER_SOURCE_INTERNAL,
7     .triggerSelect = 1U,
8     .enableReloadOnTrigger = false,
9     .enableStopOnInterrupt = false,
10    .enableStartOnTrigger = false,
11    .chainChannel = false,
12    .isInterruptEnabled = true
13 };

```

Parameters

in	<i>instance</i>	LPIT module instance number
in	<i>channel</i>	Timer channel number
in	<i>userChannelConfig</i>	Pointer to LPIT channel configuration structure

Returns

Operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: The channel 0 is chained.
- STATUS_ERROR: The input period is invalid.

Definition at line 204 of file lpit_driver.c.

17.84.5.14 void LPIT_DRV_SetTimerPeriodByCount (uint32_t *instance*, uint32_t *channel*, uint32_t *count*)

Sets the timer channel period in count unit.

This function sets the timer channel period in count unit. The counter period of a running timer channel can be modified by first setting a new load value, the value will be loaded after the timer channel expires. To abort the current cycle and start a timer channel period with the new value, the timer channel must be disabled and enabled again.

Parameters

in	<i>instance</i>	LPIT module instance number
in	<i>channel</i>	Timer channel number
in	<i>count</i>	Timer channel period in count unit

Definition at line 560 of file lpit_driver.c.

17.84.5.15 status_t LPIT_DRV_SetTimerPeriodByUs (uint32_t *instance*, uint32_t *channel*, uint32_t *periodUs*)

Sets the timer channel period in microseconds.

This function sets the timer channel period in microseconds when timer channel mode is 32 bit periodic or dual 16 bit counter mode. The period range depends on the frequency of the LPIT functional clock and operation mode of timer channel. If the required period is out of range, use the suitable mode if applicable. This function is only valid for one single channel.

Parameters

in	<i>instance</i>	LPIT module instance number
in	<i>channel</i>	Timer channel number

<i>in</i>	<i>periodUs</i>	Timer channel period in microseconds
-----------	-----------------	--------------------------------------

Returns

Operation status

- STATUS_SUCCESS: Input period of timer channel is valid.
- STATUS_ERROR: Input period of timer channel is invalid.

Definition at line 329 of file lpit_driver.c.

17.84.5.16 void LPIT_DRV_SetTimerPeriodInDual16ModeByCount (uint32_t *instance*, uint32_t *channel*, uint16_t *periodHigh*, uint16_t *periodLow*)

Sets the timer channel period in count unit.

This function sets the timer channel period in count unit when timer channel mode is dual 16 periodic counter mode. The counter period of a running timer channel can be modified by first setting a new load value, the value will be loaded after the timer channel expires. To abort the current cycle and start a timer channel period with the new value, the timer channel must be disabled and enabled again.

Parameters

<i>in</i>	<i>instance</i>	LPIT module instance number
<i>in</i>	<i>channel</i>	Timer channel number
<i>in</i>	<i>periodHigh</i>	Period of higher 16 bit in count unit
<i>in</i>	<i>periodLow</i>	Period of lower 16 bit in count unit

Definition at line 588 of file lpit_driver.c.

17.84.5.17 status_t LPIT_DRV_SetTimerPeriodInDual16ModeByUs (uint32_t *instance*, uint32_t *channel*, uint16_t *periodHigh*, uint16_t *periodLow*)

Sets the timer channel period in microseconds.

This function sets the timer channel period in microseconds when timer channel mode is dual 16 bit periodic counter mode. The period range depends on the frequency of the LPIT functional clock and operation mode of timer channel. If the required period is out of range, use the suitable mode if applicable. This function is only valid for one single channel.

Parameters

<i>in</i>	<i>instance</i>	LPIT module instance number
<i>in</i>	<i>channel</i>	Timer channel number
<i>in</i>	<i>periodHigh</i>	Period of higher 16 bit in microseconds
<i>in</i>	<i>periodLow</i>	Period of lower 16 bit in microseconds

Returns

Operation status

- STATUS_SUCCESS: Input period of timer channel is valid.
- STATUS_ERROR: Input period of timer channel is invalid.

Definition at line 400 of file lpit_driver.c.

17.84.5.18 void LPIT_DRV_StartTimerChannels (uint32_t *instance*, uint32_t *mask*)

Starts the timer channel counting.

This function allows starting timer channels simultaneously . After calling this function, timer channels are going operate depend on mode and control bits which controls timer channel start, reload and restart.

Parameters

<i>in</i>	<i>instance</i>	LPIT module instance number
<i>in</i>	<i>mask</i>	Timer channels starting mask that decides which channels will be started <ul style="list-style-type: none"> • For example: <ul style="list-style-type: none"> – with mask = 0x01U then channel 0 will be started – with mask = 0x02U then channel 1 will be started – with mask = 0x03U then channel 0 and channel 1 will be started

Definition at line 279 of file lpit_driver.c.

17.84.5.19 void LPIT_DRV_StopTimerChannels (uint32_t *instance*, uint32_t *mask*)

Stops the timer channel counting.

This function allows stop timer channels simultaneously from counting. Timer channels reload their periods respectively after the next time they call the LPIT_DRV_StartTimerChannels. Note that: In 32-bit Trigger Accumulator mode, the counter will load on the first trigger rising edge.

Parameters

<i>in</i>	<i>instance</i>	LPIT module instance number
<i>in</i>	<i>mask</i>	Timer channels stopping mask that decides which channels will be stopped <ul style="list-style-type: none"> • For example: <ul style="list-style-type: none"> – with mask = 0x01U then channel 0 will be stopped – with mask = 0x02U then channel 1 will be stopped – with mask = 0x03U then channel 0 and channel 1 will be stopped

Definition at line 303 of file lpit_driver.c.

17.85 LPSPI Driver

17.85.1 Detailed Description

Low Power Serial Peripheral Interface Peripheral Driver.

Data Structures

- struct [lpspi_master_config_t](#)
Data structure containing information about a device on the SPI bus. [More...](#)
- struct [lpspi_state_t](#)
Runtime state structure for the LPSPI master driver. [More...](#)
- struct [lpspi_slave_config_t](#)
User configuration structure for the SPI slave driver. Implements : [lpspi_slave_config_t_Class](#). [More...](#)

Enumerations

- enum [lpspi_which_pcs_t](#) { [LPSPI_PCS0](#) = 0U, [LPSPI_PCS1](#) = 1U, [LPSPI_PCS2](#) = 2U, [LPSPI_PCS3](#) = 3U }
LPSPI Peripheral Chip Select (PCS) configuration (which PCS to configure). Implements : [lpspi_which_pcs_t_Class](#).
- enum [lpspi_signal_polarity_t](#) { [LPSPI_ACTIVE_HIGH](#) = 1U, [LPSPI_ACTIVE_LOW](#) = 0U }
LPSPI Signal (PCS and Host Request) Polarity configuration. Implements : [lpspi_signal_polarity_t_Class](#).
- enum [lpspi_clock_phase_t](#) { [LPSPI_CLOCK_PHASE_1ST_EDGE](#) = 0U, [LPSPI_CLOCK_PHASE_2ND_EDGE](#) = 1U }
LPSPI clock phase configuration. Implements : [lpspi_clock_phase_t_Class](#).
- enum [lpspi_sck_polarity_t](#) { [LPSPI_SCK_ACTIVE_HIGH](#) = 0U, [LPSPI_SCK_ACTIVE_LOW](#) = 1U }
LPSPI Clock Signal (SCK) Polarity configuration. Implements : [lpspi_sck_polarity_t_Class](#).
- enum [lpspi_transfer_type](#) { [LPSPI_USING_DMA](#) = 0, [LPSPI_USING_INTERRUPTS](#) }
Type of LPSPI transfer (based on interrupts or DMA). Implements : [lpspi_transfer_type_Class](#).
- enum [transfer_status_t](#) { [LPSPI_TRANSFER_OK](#) = 0U, [LPSPI_TRANSMIT_FAIL](#), [LPSPI_RECEIVE_FAIL](#) }
Type of error reported by LPSPI.

Functions

- void [LPSPI_DRV_SlaveIRQHandler](#) (uint32_t instance)
Interrupt handler for LPSPI slave mode. This handler uses the buffers stored in the [lpspi_master_state_t](#) structs to transfer data.
- void [LPSPI_DRV_IRQHandler](#) (uint32_t instance)
The function [LPSPI_DRV_IRQHandler](#) passes IRQ control to either the master or slave driver.
- void [LPSPI_DRV_FillupTxBuffer](#) (uint32_t instance)
The function [LPSPI_DRV_FillupTxBuffer](#) writes data in TX hardware buffer depending on driver state and number of bytes remained to send.
- void [LPSPI_DRV_ReadRXBuffer](#) (uint32_t instance)
The function [LPSPI_DRV_ReadRXBuffer](#) reads data from RX hardware buffer and writes this data in RX software buffer.
- void [LPSPI_DRV_DisableTEIEInterrupts](#) (uint32_t instance)
Disable the TEIE interrupts at the end of a transfer. Disable the interrupts and clear the status for transmit/receive errors.
- void [LPSPI_DRV_SlaveGetDefaultConfig](#) ([lpspi_slave_config_t](#) *spiConfig)
Return default configuration for SPI master.
- status_t [LPSPI_DRV_SlaveInit](#) (uint32_t instance, [lpspi_state_t](#) *lpspiState, const [lpspi_slave_config_t](#) *slaveConfig)
Initializes a LPSPI instance for a slave mode operation, using interrupt mechanism.

- status_t [LPSPi_DRV_SlaveDeinit](#) (uint32_t instance)
Shuts down an LPSPi instance interrupt mechanism.
- status_t [LPSPi_DRV_SlaveTransferBlocking](#) (uint32_t instance, const uint8_t *sendBuffer, uint8_t *receiveBuffer, uint16_t transferByteCount, uint32_t timeout)
Transfers data on LPSPi bus using a blocking call.
- status_t [LPSPi_DRV_SlaveTransfer](#) (uint32_t instance, const uint8_t *sendBuffer, uint8_t *receiveBuffer, uint16_t transferByteCount)
Starts the transfer data on LPSPi bus using a non-blocking call.
- status_t [LPSPi_DRV_SlaveAbortTransfer](#) (uint32_t instance)
Aborts the transfer that started by a non-blocking call transfer function.
- status_t [LPSPi_DRV_SlaveGetTransferStatus](#) (uint32_t instance, uint32_t *bytesRemained)
Returns whether the previous transfer is finished.
- void [LPSPi0_IRQHandler](#) (void)
This function is the implementation of LPSPi0 handler named in startup code.
- void [LPSPi1_IRQHandler](#) (void)
This function is the implementation of LPSPi1 handler named in startup code.
- void [LPSPi2_IRQHandler](#) (void)
This function is the implementation of LPSPi2 handler named in startup code.

Variables

- LPSPi_Type * [g_lpspiBase](#) [LPSPi_INSTANCE_COUNT]
Table of base pointers for SPI instances.
- IRQn_Type [g_lpspiIrqlId](#) [LPSPi_INSTANCE_COUNT]
Table to save LPSPi IRQ enumeration numbers defined in the CMSIS header file.
- [lpspi_state_t](#) * [g_lpspiStatePtr](#) [LPSPi_INSTANCE_COUNT]

Initialization and shutdown

- void [LPSPi_DRV_MasterGetDefaultConfig](#) (lpspi_master_config_t *spiConfig)
Return default configuration for SPI master.
- status_t [LPSPi_DRV_MasterInit](#) (uint32_t instance, [lpspi_state_t](#) *lpspiState, const [lpspi_master_config_t](#) *spiConfig)
Initializes a LPSPi instance for interrupt driven master mode operation.
- status_t [LPSPi_DRV_MasterDeinit](#) (uint32_t instance)
Shuts down a LPSPi instance.
- status_t [LPSPi_DRV_MasterSetDelay](#) (uint32_t instance, uint32_t delayBetweenTransfers, uint32_t delaySCKtoPCS, uint32_t delayPCStoSCK)
Configures the LPSPi master mode bus timing delay options.

Bus configuration

- status_t [LPSPi_DRV_MasterConfigureBus](#) (uint32_t instance, const [lpspi_master_config_t](#) *spiConfig, uint32_t *calculatedBaudRate)
Configures the LPSPi port physical parameters to access a device on the bus when the LPSPi instance is configured for interrupt operation.
- status_t [LPSPi_DRV_SetPcs](#) (uint32_t instance, [lpspi_which_pcs_t](#) whichPcs, [lpspi_signal_polarity_t](#) polarity)
Select the chip to communicate with.

Blocking transfers

- status_t [LPSPI_DRV_MasterTransferBlocking](#) (uint32_t instance, const uint8_t *sendBuffer, uint8_t *receiveBuffer, uint16_t transferByteCount, uint32_t timeout)

Performs an interrupt driven blocking SPI master mode transfer.

Non-blocking transfers

- status_t [LPSPI_DRV_MasterTransfer](#) (uint32_t instance, const uint8_t *sendBuffer, uint8_t *receiveBuffer, uint16_t transferByteCount)

Performs an interrupt driven non-blocking SPI master mode transfer.

- status_t [LPSPI_DRV_MasterGetTransferStatus](#) (uint32_t instance, uint32_t *bytesRemained)

Returns whether the previous interrupt driven transfer is completed.

- status_t [LPSPI_DRV_MasterAbortTransfer](#) (uint32_t instance)

Terminates an interrupt driven asynchronous transfer early.

- void [LPSPI_DRV_MasterIRQHandler](#) (uint32_t instance)

Interrupt handler for LPSPI master mode. This handler uses the buffers stored in the `lpspi_master_state_t` structs to transfer data.

17.85.2 Data Structure Documentation

17.85.2.1 struct `lpspi_master_config_t`

Data structure containing information about a device on the SPI bus.

The user must populate these members to set up the LPSPI master and properly communicate with the SPI device.

Implements : `lpspi_master_config_t_Class`

Definition at line 49 of file `lpspi_master_driver.h`.

Data Fields

- uint32_t [bitsPerSec](#)
- [lpspi_which_pcs_t](#) `whichPcs`
- [lpspi_signal_polarity_t](#) `pcsPolarity`
- bool [isPcsContinuous](#)
- uint16_t [bitcount](#)
- uint32_t [lpspiSrcClk](#)
- [lpspi_clock_phase_t](#) `clkPhase`
- [lpspi_sck_polarity_t](#) `clkPolarity`
- bool [lsbFirst](#)
- [lpspi_transfer_type](#) `transferType`
- uint8_t [rxDMAChannel](#)
- uint8_t [txDMAChannel](#)
- [spi_callback_t](#) `callback`
- void * [callbackParam](#)

Field Documentation

17.85.2.1.1 uint16_t `bitcount`

Number of bits/frame, minimum is 8-bits

Definition at line 55 of file `lpspi_master_driver.h`.

17.85.2.1.2 uint32_t bitsPerSec

Baud rate in bits per second

Definition at line 51 of file `lpspi_master_driver.h`.

17.85.2.1.3 spi_callback_t callback

Select the callback to transfer complete

Definition at line 63 of file `lpspi_master_driver.h`.

17.85.2.1.4 void* callbackParam

Select additional callback parameters if it's necessary

Definition at line 64 of file `lpspi_master_driver.h`.

17.85.2.1.5 lpspi_clock_phase_t clkPhase

Selects which phase of clock to capture data

Definition at line 57 of file `lpspi_master_driver.h`.

17.85.2.1.6 lpspi_sck_polarity_t clkPolarity

Selects clock polarity

Definition at line 58 of file `lpspi_master_driver.h`.

17.85.2.1.7 bool isPcsContinuous

Keeps PCS asserted until transfer complete

Definition at line 54 of file `lpspi_master_driver.h`.

17.85.2.1.8 uint32_t lpspiSrcClk

Module source clock

Definition at line 56 of file `lpspi_master_driver.h`.

17.85.2.1.9 bool lsbFirst

Option to transmit LSB first

Definition at line 59 of file `lpspi_master_driver.h`.

17.85.2.1.10 lpspi_signal_polarity_t pcsPolarity

PCS polarity

Definition at line 53 of file `lpspi_master_driver.h`.

17.85.2.1.11 uint8_t rxDMAChannel

Channel number for DMA rx channel. If DMA mode isn't used this field will be ignored.

Definition at line 61 of file `lpspi_master_driver.h`.

17.85.2.1.12 lpspi_transfer_type transferType

Type of LPSPI transfer

Definition at line 60 of file `lpspi_master_driver.h`.

17.85.2.1.13 uint8_t txDMAChannel

Channel number for DMA tx channel. If DMA mode isn't used this field will be ignored.

Definition at line 62 of file `lpspi_master_driver.h`.

17.85.2.1.14 lpspi_which_pcs_t whichPcs

Selects which PCS to use

Definition at line 52 of file `lpspi_master_driver.h`.

17.85.2.2 struct lpspi_state_t

Runtime state structure for the LPSPi master driver.

This structure holds data that is used by the LPSPi peripheral driver to communicate between the transfer function and the interrupt handler. The interrupt handler also uses this information to keep track of its progress. The user must pass the memory for this run-time state structure. The LPSPi master driver populates the members. Implements : `lpspi_state_t_Class`

Definition at line 124 of file `lpspi_shared_function.h`.

Data Fields

- uint16_t [bitsPerFrame](#)
- uint16_t [bytesPerFrame](#)
- bool [isPcsContinuous](#)
- bool [isBlocking](#)
- uint32_t [lpspiSrcClk](#)
- volatile bool [isTransferInProgress](#)
- const uint8_t * [txBuff](#)
- uint8_t * [rxBuff](#)
- volatile uint16_t [txCount](#)
- volatile uint16_t [rxCount](#)
- volatile uint16_t [txFrameCnt](#)
- volatile uint16_t [rxFrameCnt](#)
- volatile bool [lsb](#)
- uint8_t [fifoSize](#)
- uint8_t [rxDMAChannel](#)
- uint8_t [txDMAChannel](#)
- [lpspi_transfer_type](#) [transferType](#)
- semaphore_t [lpspiSemaphore](#)
- [transfer_status_t](#) [status](#)
- spi_callback_t [callback](#)
- void * [callbackParam](#)
- uint32_t [dummy](#)

Field Documentation

17.85.2.2.1 uint16_t bitsPerFrame

Number of bits per frame: 8- to 4096-bits; needed for TCR programming

Definition at line 126 of file `lpspi_shared_function.h`.

17.85.2.2.2 uint16_t bytesPerFrame

Number of bytes per frame: 1- to 512-bytes

Definition at line 128 of file `lpspi_shared_function.h`.

17.85.2.2.3 spi_callback_t callback

Select the callback to transfer complete

Definition at line 147 of file lpspi_shared_function.h.

17.85.2.2.4 void* callbackParam

Select additional callback parameters if it's necessary

Definition at line 148 of file lpspi_shared_function.h.

17.85.2.2.5 uint32_t dummy

This field is used for the cases when TX is NULL and LPSPI is in DMA mode

Definition at line 149 of file lpspi_shared_function.h.

17.85.2.2.6 uint8_t fifoSize

RX/TX fifo size

Definition at line 141 of file lpspi_shared_function.h.

17.85.2.2.7 bool isBlocking

Save the transfer type

Definition at line 131 of file lpspi_shared_function.h.

17.85.2.2.8 bool isPcsContinuous

Option to keep chip select asserted until transfer complete; needed for TCR programming

Definition at line 129 of file lpspi_shared_function.h.

17.85.2.2.9 volatile bool isTransferInProgress

True if there is an active transfer

Definition at line 133 of file lpspi_shared_function.h.

17.85.2.2.10 semaphore_t lpspiSemaphore

The semaphore used for blocking transfers

Definition at line 145 of file lpspi_shared_function.h.

17.85.2.2.11 uint32_t lpspiSrcClk

Module source clock

Definition at line 132 of file lpspi_shared_function.h.

17.85.2.2.12 volatile bool lsb

True if first bit is LSB and false if first bit is MSB

Definition at line 140 of file lpspi_shared_function.h.

17.85.2.2.13 uint8_t* rxBuff

The buffer into which received bytes are placed

Definition at line 135 of file lpspi_shared_function.h.

17.85.2.2.14 volatile uint16_t rxCount

Number of bytes remaining to receive

Definition at line 137 of file `lpspi_shared_function.h`.

17.85.2.2.15 uint8_t rxDMAChannel

Channel number for DMA rx channel

Definition at line 142 of file `lpspi_shared_function.h`.

17.85.2.2.16 volatile uint16_t rxFrameCnt

Number of bytes from current frame which were already received

Definition at line 139 of file `lpspi_shared_function.h`.

17.85.2.2.17 transfer_status_t status

The status of the current

Definition at line 146 of file `lpspi_shared_function.h`.

17.85.2.2.18 lpspi_transfer_type transferType

Type of LPSPI transfer

Definition at line 144 of file `lpspi_shared_function.h`.

17.85.2.2.19 const uint8_t* txBuff

The buffer from which transmitted bytes are taken

Definition at line 134 of file `lpspi_shared_function.h`.

17.85.2.2.20 volatile uint16_t txCount

Number of bytes remaining to send

Definition at line 136 of file `lpspi_shared_function.h`.

17.85.2.2.21 uint8_t txDMAChannel

Channel number for DMA tx channel

Definition at line 143 of file `lpspi_shared_function.h`.

17.85.2.2.22 volatile uint16_t txFrameCnt

Number of bytes from current frame which were already sent

Definition at line 138 of file `lpspi_shared_function.h`.

17.85.2.3 struct lpspi_slave_config_t

User configuration structure for the SPI slave driver. Implements : `lpspi_slave_config_t_Class`.

Definition at line 47 of file `lpspi_slave_driver.h`.

Data Fields

- [lpspi_signal_polarity_t pcsPolarity](#)
- [uint16_t bitcount](#)
- [lpspi_clock_phase_t clkPhase](#)
- [lpspi_which_pcs_t whichPcs](#)
- [lpspi_sck_polarity_t clkPolarity](#)

- bool [lsbFirst](#)
- [lpspi_transfer_type](#) transferType
- [uint8_t rxDMAChannel](#)
- [uint8_t txDMAChannel](#)
- [spi_callback_t](#) callback
- void * [callbackParam](#)

Field Documentation

17.85.2.3.1 [uint16_t bitcount](#)

Number of bits/frame, minimum is 8-bits

Definition at line 50 of file [lpspi_slave_driver.h](#).

17.85.2.3.2 [spi_callback_t](#) callback

Select the callback to transfer complete

Definition at line 58 of file [lpspi_slave_driver.h](#).

17.85.2.3.3 [void*](#) callbackParam

Select additional callback parameters if it's necessary

Definition at line 59 of file [lpspi_slave_driver.h](#).

17.85.2.3.4 [lpspi_clock_phase_t](#) clkPhase

Selects which phase of clock to capture data

Definition at line 51 of file [lpspi_slave_driver.h](#).

17.85.2.3.5 [lpspi_sck_polarity_t](#) clkPolarity

Selects clock polarity

Definition at line 53 of file [lpspi_slave_driver.h](#).

17.85.2.3.6 [bool](#) lsbFirst

Option to transmit LSB first

Definition at line 54 of file [lpspi_slave_driver.h](#).

17.85.2.3.7 [lpspi_signal_polarity_t](#) pcsPolarity

PCS polarity

Definition at line 49 of file [lpspi_slave_driver.h](#).

17.85.2.3.8 [uint8_t](#) rxDMAChannel

Channel number for DMA rx channel. If DMA mode isn't used this field will be ignored.

Definition at line 56 of file [lpspi_slave_driver.h](#).

17.85.2.3.9 [lpspi_transfer_type](#) transferType

Type of LPSPI transfer

Definition at line 55 of file [lpspi_slave_driver.h](#).

17.85.2.3.10 [uint8_t](#) txDMAChannel

Channel number for DMA tx channel. If DMA mode isn't used this field will be ignored.

Definition at line 57 of file `lpspi_slave_driver.h`.

17.85.2.3.11 `lpspi_which_pcs_t` whichPcs

Definition at line 52 of file `lpspi_slave_driver.h`.

17.85.3 Enumeration Type Documentation

17.85.3.1 `enum lpspi_clock_phase_t`

LPSPi clock phase configuration. Implements : `lpspi_clock_phase_t_Class`.

Enumerator

`LPSPi_CLOCK_PHASE_1ST_EDGE` Data captured on SCK 1st edge, changed on 2nd.

`LPSPi_CLOCK_PHASE_2ND_EDGE` Data changed on SCK 1st edge, captured on 2nd.

Definition at line 80 of file `lpspi_shared_function.h`.

17.85.3.2 `enum lpspi_sck_polarity_t`

LPSPi Clock Signal (SCK) Polarity configuration. Implements : `lpspi_sck_polarity_t_Class`.

Enumerator

`LPSPi_SCK_ACTIVE_HIGH` Signal is Active High (idles low).

`LPSPi_SCK_ACTIVE_LOW` Signal is Active Low (idles high).

Definition at line 89 of file `lpspi_shared_function.h`.

17.85.3.3 `enum lpspi_signal_polarity_t`

LPSPi Signal (PCS and Host Request) Polarity configuration. Implements : `lpspi_signal_polarity_t_Class`.

Enumerator

`LPSPi_ACTIVE_HIGH` Signal is Active High (idles low).

`LPSPi_ACTIVE_LOW` Signal is Active Low (idles high).

Definition at line 71 of file `lpspi_shared_function.h`.

17.85.3.4 `enum lpspi_transfer_type`

Type of LPSPi transfer (based on interrupts or DMA). Implements : `lpspi_transfer_type_Class`.

Enumerator

`LPSPi_USING_DMA` The driver will use DMA to perform SPI transfer

`LPSPi_USING_INTERRUPTS` The driver will use interrupts to perform SPI transfer

Definition at line 99 of file `lpspi_shared_function.h`.

17.85.3.5 `enum lpspi_which_pcs_t`

LPSPi Peripheral Chip Select (PCS) configuration (which PCS to configure). Implements : `lpspi_which_pcs_t_Class`.

Enumerator

`LPSPi_PCS0` PCS[0]

LPSPI_PCS1 PCS[1]

LPSPI_PCS2 PCS[2]

LPSPI_PCS3 PCS[3]

Definition at line 60 of file `lpspi_shared_function.h`.

17.85.3.6 enum transfer_status_t

Type of error reported by LPSPI.

Enumerator

LPSPI_TRANSFER_OK Transfer OK

LPSPI_TRANSMIT_FAIL Error during transmission

LPSPI_RECEIVE_FAIL Error during reception

Definition at line 107 of file `lpspi_shared_function.h`.

17.85.4 Function Documentation

17.85.4.1 void LPSPI0_IRQHandler (void)

This function is the implementation of LPSPI0 handler named in startup code.

It passes the instance to the shared LPSPI IRQ handler.

Definition at line 115 of file `lpspi_irq.c`.

17.85.4.2 void LPSPI1_IRQHandler (void)

This function is the implementation of LPSPI1 handler named in startup code.

It passes the instance to the shared LPSPI IRQ handler.

Definition at line 127 of file `lpspi_irq.c`.

17.85.4.3 void LPSPI2_IRQHandler (void)

This function is the implementation of LPSPI2 handler named in startup code.

It passes the instance to the shared LPSPI IRQ handler.

Definition at line 139 of file `lpspi_irq.c`.

17.85.4.4 void LPSPI_DRV_DisableTEIEInterrupts (uint32_t instance)

Disable the TEIE interrupts at the end of a transfer. Disable the interrupts and clear the status for transmit/receive errors.

Definition at line 235 of file `lpspi_shared_function.c`.

17.85.4.5 void LPSPI_DRV_FillupTxBuffer (uint32_t instance)

The function `LPSPI_DRV_FillupTxBuffer` writes data in TX hardware buffer depending on driver state and number of bytes remained to send.

The function `LPSPI_DRV_FillupTxBuffer` writes data in TX hardware buffer depending on driver state and number of bytes remained to send.

Definition at line 123 of file `lpspi_shared_function.c`.

17.85.4.6 void LPSPI_DRV_IRQHandler (uint32_t instance)

The function LPSPI_DRV_IRQHandler passes IRQ control to either the master or slave driver.

The address of the IRQ handlers are checked to make sure they are non-zero before they are called. If the IRQ handler's address is zero, it means that driver was not present in the link (because the IRQ handlers are marked as weak). This would actually be a program error, because it means the master/slave config for the IRQ was set incorrectly.

Definition at line 100 of file lpspi_shared_function.c.

17.85.4.7 status_t LPSPI_DRV_MasterAbortTransfer (uint32_t instance)

Terminates an interrupt driven asynchronous transfer early.

During an a-sync (non-blocking) transfer, the user has the option to terminate the transfer early if the transfer is still in progress.

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
-----------------	--

Returns

STATUS_SUCCESS The transfer was successful, or LPSPI_STATUS_NO_TRANSFER_IN_PROGRESS No transfer is currently in progress.

Definition at line 578 of file lpspi_master_driver.c.

17.85.4.8 status_t LPSPI_DRV_MasterConfigureBus (uint32_t instance, const lpspi_master_config_t * spiConfig, uint32_t * calculatedBaudRate)

Configures the LPSPI port physical parameters to access a device on the bus when the LSPI instance is configured for interrupt operation.

In this function, the term "spiConfig" is used to indicate the SPI device for which the LPSPI master is communicating. This is an optional function as the spiConfig parameters are normally configured in the initialization function or the transfer functions, where these various functions would call the configure bus function. This is an example to set up the [lpspi_master_config_t](#) structure to call the LPSPI_DRV_MasterConfigureBus function by passing in these parameters:

```
1 lpspi_master_config_t spiConfig1;  You can also declare spiConfig2, spiConfig3, etc
2 spiConfig1.bitsPerSec = 500000;
3 spiConfig1.whichPcs = LPSPI_PCS0;
4 spiConfig1.pcsPolarity = LPSPI_ACTIVE_LOW;
5 spiConfig1.isPcsContinuous = false;
6 spiConfig1.bitCount = 16;
7 spiConfig1.clkPhase = LPSPI_CLOCK_PHASE_1ST_EDGE;
8 spiConfig1.clkPolarity = LPSPI_ACTIVE_HIGH;
9 spiConfig1.lsbFirst= false;
10 spiConfig.transferType = LPSPI_USING_INTERRUPTS;
```

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
<i>spiConfig</i>	Pointer to the spiConfig structure. This structure contains the settings for the SPI bus configuration. The SPI device parameters are the desired baud rate (in bits-per-sec), bits-per-frame, chip select attributes, clock attributes, and data shift direction.

<i>calculated↔ BaudRate</i>	The calculated baud rate passed back to the user to determine if the calculated baud rate is close enough to meet the needs. The baud rate never exceeds the desired baud rate.
---------------------------------	---

Returns

STATUS_SUCCESS The transfer has completed successfully, or STATUS_ERROR if driver is error and needs to clean error.

Definition at line 309 of file lpspi_master_driver.c.

17.85.4.9 status_t LPSPI_DRV_MasterDeinit (uint32_t *instance*)

Shuts down a LPSPI instance.

This function resets the LPSPI peripheral, gates its clock, and disables the interrupt to the core. It first checks to see if a transfer is in progress and if so returns an error status.

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
-----------------	--

Returns

STATUS_SUCCESS The transfer has completed successfully, or STATUS_BUSY The transfer is still in progress. STATUS_ERROR if driver is error and needs to clean error.

Definition at line 219 of file lpspi_master_driver.c.

17.85.4.10 void LPSPI_DRV_MasterGetDefaultConfig (lpspi_master_config_t * *spiConfig*)

Return default configuration for SPI master.

Initializes a structured provided by user with the configuration of an interrupt based LPSPI transfer. Source clock for LPSPI is configured to 8MHz. If the applications uses other frequency is necessary to update lpspiSrcClk field.

Parameters

<i>spiConfig</i>	Pointer to configuration structure which is filled with default configuration
------------------	---

Definition at line 131 of file lpspi_master_driver.c.

17.85.4.11 status_t LPSPI_DRV_MasterGetTransferStatus (uint32_t *instance*, uint32_t * *bytesRemained*)

Returns whether the previous interrupt driven transfer is completed.

When performing an a-sync (non-blocking) transfer, the user can call this function to ascertain the state of the current transfer: in progress (or busy) or complete (success). In addition, if the transfer is still in progress, the user can get the number of words that have been transferred up to now.

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
<i>bytesRemained</i>	Pointer to a value that is filled in with the number of bytes that must be received.

Returns

STATUS_SUCCESS The transfer has completed successfully, or STATUS_BUSY The transfer is still in progress. framesTransferred is filled with the number of words that have been transferred so far.

Definition at line 549 of file lpspi_master_driver.c.

17.85.4.12 status_t LPSPI_DRV_MasterInit (uint32_t *instance*, lpspi_state_t * *lpspiState*, const lpspi_master_config_t * *spiConfig*)

Initializes a LPSPI instance for interrupt driven master mode operation.

This function uses an interrupt-driven method for transferring data. In this function, the term "spiConfig" is used to indicate the SPI device for which the LPSPI master is communicating. This function initializes the run-time state structure to track the ongoing transfers, un-gates the clock to the LPSPI module, resets the LPSPI module, configures the IRQ state structure, enables the module-level interrupt to the core, and enables the LPSPI module. This is an example to set up the `lpspi_master_state_t` and call the `LPSPI_DRV_MasterInit` function by passing in these parameters:

```
1 lpspi_master_state_t lpspiMasterState; <- the user allocates memory for this structure
2 lpspi_master_config_t spiConfig; Can declare more configs for use in transfer functions
3 spiConfig.bitsPerSec = 500000;
4 spiConfig.whichPcs = LPSPI_PCS0;
5 spiConfig.pcsPolarity = LPSPI_ACTIVE_LOW;
6 spiConfig.isPcsContinuous = false;
7 spiConfig.bitCount = 16;
8 spiConfig.clkPhase = LPSPI_CLOCK_PHASE_1ST_EDGE;
9 spiConfig.clkPolarity = LPSPI_ACTIVE_HIGH;
10 spiConfig.lsbFirst= false;
11 spiConfig.transferType = LPSPI_USING_INTERRUPTS;
12 LPSPI_DRV_MasterInit(masterInstance, &lpspiMasterState, &spiConfig);
```

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
<i>lpspiState</i>	The pointer to the LPSPI master driver state structure. The user passes the memory for this run-time state structure. The LPSPI master driver populates the members. This run-time state structure keeps track of the transfer in progress.
<i>spiConfig</i>	The data structure containing information about a device on the SPI bus

Returns

An error code or `STATUS_SUCCESS`.

Definition at line 166 of file `lpspi_master_driver.c`.

17.85.4.13 void LPSPI_DRV_MasterIRQHandler (uint32_t instance)

Interrupt handler for LPSPI master mode. This handler uses the buffers stored in the `lpspi_master_state_t` structs to transfer data.

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
-----------------	--

Interrupt handler for LPSPI master mode. This handler uses the buffers stored in the `lpspi_master_state_t` structs to transfer data.

Definition at line 867 of file `lpspi_master_driver.c`.

17.85.4.14 status_t LPSPI_DRV_MasterSetDelay (uint32_t instance, uint32_t delayBetweenTransfers, uint32_t delaySCKtoPCS, uint32_t delayPCStoSCK)

Configures the LPSPI master mode bus timing delay options.

This function involves the LPSPI module's delay options to "fine tune" some of the signal timings and match the timing needs of a slower peripheral device. This is an optional function that can be called after the LPSPI module has been initialized for master mode. The timings are adjusted in terms of cycles of the baud rate clock. The bus timing delays that can be adjusted are listed below:

SCK to PCS Delay: Adjustable delay option between the last edge of SCK to the de-assertion of the PCS signal.

PCS to SCK Delay: Adjustable delay option between the assertion of the PCS signal to the first SCK edge.

Delay between Transfers: Adjustable delay option between the de-assertion of the PCS signal for a frame to the assertion of the PCS signal for the next frame.

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
<i>delayBetween↔ Transfers</i>	Minimum delay between 2 transfers in clock cycles
<i>delaySCKtoP↔ CS</i>	Minimum delay between SCK and PCS in clock cycles
<i>delayPCStoS↔ CK</i>	Minimum delay between PCS and SCK in clock cycles

Returns

STATUS_SUCCESS The transfer has completed successfully, or STATUS_ERROR if driver is error and needs to clean error.

Definition at line 266 of file lpspi_master_driver.c.

17.85.4.15 `status_t LPSPI_DRV_MasterTransfer (uint32_t instance, const uint8_t * sendBuffer, uint8_t * receiveBuffer, uint16_t transferByteCount)`

Performs an interrupt driven non-blocking SPI master mode transfer.

This function simultaneously sends and receives data on the SPI bus, as SPI is naturally a full-duplex bus. The function returns immediately after initiating the transfer. The user needs to check whether the transfer is complete using the LPSPI_DRV_MasterGetTransferStatus function. This function allows the user to optionally pass in a SPI configuration structure which allows the user to change the SPI bus attributes in conjunction with initiating a SPI transfer. The difference between passing in the SPI configuration structure here as opposed to the configure bus function is that the configure bus function returns the calculated baud rate where this function does not. The user can also call the configure bus function prior to the transfer in which case the user would simply pass in a NULL to the transfer function's device structure parameter. Depending on frame size sendBuffer and receiveBuffer must be aligned like this: -1 byte if frame size ≤ 8 bits -2 bytes if 8 bits < frame size ≤ 16 bits -4 bytes if 16 bits < frame size

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
<i>spiConfig</i>	Pointer to the SPI configuration structure. This structure contains the settings for the SPI bus configuration in this transfer. You may pass NULL for this parameter, in which case the current bus configuration is used unmodified. The device can be configured separately by calling the LPSPI_DRV_MasterConfigureBus function.
<i>sendBuffer</i>	The pointer to the data buffer of the data to send. You may pass NULL for this parameter and bytes with a value of 0 (zero) is sent.
<i>receiveBuffer</i>	Pointer to the buffer where the received bytes are stored. If you pass NULL for this parameter, the received bytes are ignored.
<i>transferByte↔ Count</i>	The number of bytes to send and receive which is equal to size of send or receive buffers

Returns

STATUS_SUCCESS The transfer was successful, or STATUS_BUSY Cannot perform transfer because a transfer is already in progress

Definition at line 511 of file lpspi_master_driver.c.

17.85.4.16 `status_t LPSPI_DRV_MasterTransferBlocking (uint32_t instance, const uint8_t * sendBuffer, uint8_t * receiveBuffer, uint16_t transferByteCount, uint32_t timeout)`

Performs an interrupt driven blocking SPI master mode transfer.

This function simultaneously sends and receives data on the SPI bus, as SPI is naturally a full-duplex bus. The function does not return until the transfer is complete. This function allows the user to optionally pass in a SPI

configuration structure which allows the user to change the SPI bus attributes in conjunction with initiating a SPI transfer. The difference between passing in the SPI configuration structure here as opposed to the configure bus function is that the configure bus function returns the calculated baud rate where this function does not. The user can also call the configure bus function prior to the transfer in which case the user would simply pass in a NULL to the transfer function's device structure parameter. Depending on frame size sendBuffer and receiveBuffer must be aligned like this: -1 byte if frame size <= 8 bits -2 bytes if 8 bits < frame size <= 16 bits -4 bytes if 16 bits < frame size

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
<i>sendBuffer</i>	The pointer to the data buffer of the data to send. You may pass NULL for this parameter and bytes with a value of 0 (zero) is sent.
<i>receiveBuffer</i>	Pointer to the buffer where the received bytes are stored. If you pass NULL for this parameter, the received bytes are ignored.
<i>transferByte↔ Count</i>	The number of bytes to send and receive which is equal to size of send or receive buffers
<i>timeout</i>	A timeout for the transfer in milliseconds. If the transfer takes longer than this amount of time, the transfer is aborted and a STATUS_TIMEOUT error returned.

Returns

STATUS_SUCCESS The transfer was successful, or STATUS_BUSY Cannot perform transfer because a transfer is already in progress, or STATUS_TIMEOUT The transfer timed out and was aborted.

Definition at line 424 of file lpspi_master_driver.c.

17.85.4.17 void LPSPI_DRV_ReadRXBuffer (uint32_t instance)

The function LPSPI_DRV_ReadRXBuffer reads data from RX hardware buffer and writes this data in RX software buffer.

The function LPSPI_DRV_ReadRXBuffer reads data from RX hardware buffer and writes this data in RX software buffer.

Definition at line 192 of file lpspi_shared_function.c.

17.85.4.18 status_t LPSPI_DRV_SetPcs (uint32_t instance, lpspi_which_pcs_t whichPcs, lpspi_signal_polarity_t polarity)

Select the chip to communicate with.

The main purpose of this function is to set the PCS and the appropriate polarity.

Parameters

<i>instance</i>	LPSPI instance
<i>whichPcs</i>	selected chip
<i>polarity</i>	chip select line polarity

Returns

STATUS_SUCCESS The transfer has completed successfully, or STATUS_ERROR if driver is error and needs to clean error.

Definition at line 600 of file lpspi_master_driver.c.

17.85.4.19 status_t LPSPI_DRV_SlaveAbortTransfer (uint32_t instance)

Aborts the transfer that started by a non-blocking call transfer function.

This function stops the transfer which was started by the calling the SPI_DRV_SlaveTransfer() function.

Parameters

<i>instance</i>	The instance number of SPI peripheral
-----------------	---------------------------------------

Returns

STATUS_SUCCESS if everything is OK.

Definition at line 512 of file `lpspi_slave_driver.c`.

17.85.4.20 `status_t LPSPI_DRV_SlaveDeinit (uint32_t instance)`

Shuts down an LPSPI instance interrupt mechanism.

Disables the LPSPI module, gates its clock, and changes the LPSPI slave driver state to NonInit for the LPSPI slave module which is initialized with interrupt mechanism. After de-initialization, the user can re-initialize the LPSPI slave module with other mechanisms.

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
-----------------	--

Returns

STATUS_SUCCESS if driver starts to send/receive data successfully. STATUS_ERROR if driver is error and needs to clean error. STATUS_BUSY if a transfer is in progress

Definition at line 201 of file `lpspi_slave_driver.c`.

17.85.4.21 `void LPSPI_DRV_SlaveGetDefaultConfig (lpspi_slave_config_t * spiConfig)`

Return default configuration for SPI master.

Initializes a structured provided by user with the configuration of an interrupt based LPSPI transfer.

Definition at line 105 of file `lpspi_slave_driver.c`.

17.85.4.22 `status_t LPSPI_DRV_SlaveGetTransferStatus (uint32_t instance, uint32_t * bytesRemained)`

Returns whether the previous transfer is finished.

When performing an a-sync transfer, the user can call this function to ascertain the state of the current transfer: in progress (or busy) or complete (success). In addition, if the transfer is still in progress, the user can get the number of bytes that have been transferred up to now.

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
<i>bytesRemained</i>	Pointer to value that is filled in with the number of frames that have been sent in the active transfer. A frame is defined as the number of bits per frame.

Returns

STATUS_SUCCESS The transfer has completed successfully, or STATUS_BUSY The transfer is still in progress. STATUS_ERROR if driver is error and needs to clean error.

Definition at line 550 of file `lpspi_slave_driver.c`.

17.85.4.23 `status_t LPSPI_DRV_SlaveInit (uint32_t instance, lpspi_state_t * lpspiState, const lpspi_slave_config_t * slaveConfig)`

Initializes a LPSPI instance for a slave mode operation, using interrupt mechanism.

This function un-gates the clock to the LPSPI module, initializes the LPSPI for slave mode. After it is initialized, the LPSPI module is configured in slave mode and the user can start transmitting and receiving data by calling send, receive, and transfer functions. This function indicates LPSPI slave uses an interrupt mechanism.

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
<i>lpspiState</i>	The pointer to the LPSPI slave driver state structure.
<i>slaveConfig</i>	The configuration structure <code>lpspi_slave_user_config_t</code> which configures the data bus format.

Returns

An error code or STATUS_SUCCESS.

Definition at line 125 of file `lpspi_slave_driver.c`.

17.85.4.24 void LPSPI_DRV_SlaveIRQHandler (uint32_t instance)

Interrupt handler for LPSPI slave mode. This handler uses the buffers stored in the `lpspi_master_state_t` structs to transfer data.

Parameters

<i>instance</i>	The instance number of the LPSPI peripheral.
-----------------	--

Definition at line 437 of file `lpspi_slave_driver.c`.

17.85.4.25 status_t LPSPI_DRV_SlaveTransfer (uint32_t instance, const uint8_t * sendBuffer, uint8_t * receiveBuffer, uint16_t transferByteCount)

Starts the transfer data on LPSPI bus using a non-blocking call.

This function checks the driver status and mechanism and transmits/receives data through the LPSPI bus. If the `sendBuffer` is NULL, the transmit process is ignored. If the `receiveBuffer` is NULL, the receive process is ignored. If both the `receiveBuffer` and the `sendBuffer` are available, the transmit and the receive progress is processed. If only the `receiveBuffer` is available, the receive is processed. Otherwise, the transmit is processed. This function only returns when the processes are completed. This function uses an interrupt mechanism. Depending on frame size `sendBuffer` and `receiveBuffer` must be aligned like this: -1 byte if frame size ≤ 8 bits -2 bytes if 8 bits < frame size ≤ 16 bits -4 bytes if 16 bits < frame size

Parameters

<i>instance</i>	The instance number of LPSPI peripheral
<i>sendBuffer</i>	The pointer to data that user wants to transmit.
<i>receiveBuffer</i>	The pointer to data that user wants to store received data.
<i>transferByteCount</i>	The number of bytes to send and receive which is equal to size of send or receive buffers

Returns

STATUS_SUCCESS if driver starts to send/receive data successfully. STATUS_ERROR if driver is error and needs to clean error. STATUS_BUSY if a transfer is in progress

Definition at line 280 of file `lpspi_slave_driver.c`.

17.85.4.26 status_t LPSPI_DRV_SlaveTransferBlocking (uint32_t instance, const uint8_t * sendBuffer, uint8_t * receiveBuffer, uint16_t transferByteCount, uint32_t timeout)

Transfers data on LPSPI bus using a blocking call.

This function checks the driver status and mechanism and transmits/receives data through the LPSPI bus. If the `sendBuffer` is NULL, the transmit process is ignored. If the `receiveBuffer` is NULL, the receive process is ignored. If both the `receiveBuffer` and the `sendBuffer` are available, the transmit and the receive progress is processed. If only the `receiveBuffer` is available, the receive is processed. Otherwise, the transmit is processed. This function only returns when the processes are completed. This function uses an interrupt mechanism. Depending on frame size `sendBuffer` and `receiveBuffer` must be aligned like this: -1 byte if frame size ≤ 8 bits -2 bytes if 8 bits < frame size ≤ 16 bits -4 bytes if 16 bits < frame size

Parameters

<i>instance</i>	The instance number of LPSPI peripheral
<i>sendBuffer</i>	The pointer to data that user wants to transmit.
<i>receiveBuffer</i>	The pointer to data that user wants to store received data.
<i>transferByteCount</i>	The number of bytes to send and receive which is equal to size of send or receive buffers
<i>timeout</i>	The maximum number of milliseconds that function waits before timed out reached.

Returns

STATUS_SUCCESS if driver starts to send/receive data successfully. STATUS_ERROR if driver is error and needs to clean error. STATUS_BUSY if a transfer is in progress STATUS_TIMEOUT if time out reached while transferring is in progress.

Definition at line 230 of file `lpspi_slave_driver.c`.

17.85.5 Variable Documentation

17.85.5.1 LPSPI_Type* g_lpspiBase[LPSPI_INSTANCE_COUNT]

Table of base pointers for SPI instances.

Definition at line 78 of file `lpspi_shared_function.c`.

17.85.5.2 IRQn_Type g_lpspiIrqlId[LPSPI_INSTANCE_COUNT]

Table to save LPSPI IRQ enumeration numbers defined in the CMSIS header file.

Definition at line 81 of file `lpspi_shared_function.c`.

17.85.5.3 lpspi_state_t* g_lpspiStatePtr[LPSPI_INSTANCE_COUNT]

Definition at line 84 of file `lpspi_shared_function.c`.

17.86 LPTMR Driver

17.86.1 Detailed Description

Low Power Timer Peripheral Driver.

The LPTMR is a configurable general-purpose 16-bit counter that has two operational modes: Timer and Pulse-Counter.

Depending on the configured operational mode, the counter in the LPTMR can be incremented using a clock input (Timer mode) or an event counter (external events like button presses or internal events from different trigger sources).

Timer Mode

In Timer mode, the LPTMR increments the internal counter from a selectable clock source. An optional 16-bit prescaler can be configured.

Pulse-Counter Mode

In Pulse-Counter Mode, the LPTMR counter increments from a selectable trigger source, input pin, which can be an external event (like a button press) or internal events (like triggers from TRGMUX).

An optional 16-bit glitch-filter can be configured to reject events that have a duration below a set period.

Initialization prerequisites

Before configuring the LPTMR, the peripheral clock must be enabled from the PCC module.

The peripheral clock must not be confused with the counter clock, which is selectable within the LPTMR.

Driver configuration

The LPTMR driver allows configuring the LPTMR for Pulse-Counter Mode or Timer Mode via the general configuration structure.

Configurable options:

- work mode (timer or pulse-counter)
- enable interrupts and DMA requests
- free running mode (overflow mode of the counter)
- compare value (interrupt generation on counter value)
- compare value measurement units (counter ticks or microseconds)
- input clock selection
- prescaler/glitch filter configuration
- enable bypass prescaler
- pin select (for pulse-counter mode)
- input pin and polarity (for pulse-counter mode)

```
/* LPTMR initialization of config structure */
lptmr_config_t config = {
    .workMode = LPTMR_WORKMODE_TIMER,
    .dmaRequest = false,
    .interruptEnable = false,
    .freeRun = false,
    .compareValue = 1000U,
    .counterUnits = LPTMR_COUNTER_UNITS_TICKS,
    .clockSelect = LPTMR_CLOCKSOURCE_SIRCDIV2,
    .prescaler = LPTMR_PRESCALE_2,
    .bypassPrescaler = false,
```

```

        .pinSelect = LPTMR_PINSELECT_TRGMUX,
        .pinPolarity = LPTMR_PINPOLARITY_RISING,
    };

    /* Initialize the LPTMR and start the counter in a separate operation */
    status = LPTMR_DRV_Init(0, &config, false);
    /* Start timer counting */
    LPTMR_DRV_StartCounter(0);

```

API

Some of the features exposed by the API are targeted specifically for Timer Mode or Pulse-Counter Mode. For example, configuring the Compare Value in microseconds makes sense only for Timer Mode, so therefore it is restricted for use in Pulse-Counter mode.

For any invalid configuration the functions will either return an error code or trigger DEV_ASSERT (if enabled). For more details, please refer to each function description.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```

${S32SDK_PATH}\platform\drivers\src\lptmr_driver.c
${S32SDK_PATH}\platform\drivers\src\lptmr_hw_access.c

```

Include path

The following paths need to be added to the include path of the toolchain:

```

${S32SDK_PATH}\platform\drivers\inc\

```

Compile symbols

No special symbols are required for this component

Dependencies

Clock Manager

Data Structures

- struct [lptmr_config_t](#)
Defines the configuration structure for LPTMR. [More...](#)

Enumerations

- enum [lptmr_pinselect_t](#) { [LPTMR_PINSELECT_TRGMUX](#) = 0x00u, [LPTMR_PINSELECT_ALT2](#) = 0x02u, [LPTMR_PINSELECT_ALT3](#) = 0x03u }
Pulse Counter Input selection Implements : [lptmr_pinselect_t_Class](#).
- enum [lptmr_pinpolarity_t](#) { [LPTMR_PINPOLARITY_RISING](#) = 0u, [LPTMR_PINPOLARITY_FALLING](#) = 1u }
Pulse Counter input polarity Implements : [lptmr_pinpolarity_t_Class](#).
- enum [lptmr_workmode_t](#) { [LPTMR_WORKMODE_TIMER](#) = 0u, [LPTMR_WORKMODE_PULSECOUNTER](#) = 1u }
Work Mode Implements : [lptmr_workmode_t_Class](#).
- enum [lptmr_prescaler_t](#) { [LPTMR_PRESCALE_2](#) = 0x00u, [LPTMR_PRESCALE_4_GLITCHFILTER_2](#) = 0x01u, [LPTMR_PRESCALE_4_GLITCHFILTER_4](#) = 0x02u, [LPTMR_PRESCALE_16_GLITCHFILTER_8](#) = 0x03u, [LPTMR_PRESCALE_32_GLITCHFILTER_16](#) = 0x04u, [LPTMR_PRESCALE_64_GLITCHFILTER_32](#) = 0x05u }

```
0x05u, LPTMR_PRESCALE_128_GLITCHFILTER_64 = 0x06u, LPTMR_PRESCALE_256_GLITCHFILTER_128 = 0x07u,
LPTMR_PRESCALE_512_GLITCHFILTER_256 = 0x08u, LPTMR_PRESCALE_1024_GLITCHFILTER_512 = 0x09u,
LPTMR_PRESCALE_2048_GLITCHFILTER_1024 = 0x0Au, LPTMR_PRESCALE_4096_GLITCHFILTER_2048 = 0x0Bu,
LPTMR_PRESCALE_8192_GLITCHFILTER_4096 = 0x0Cu, LPTMR_PRESCALE_16384_GLITCHFILTER_8192 = 0x0Du,
LPTMR_PRESCALE_32768_GLITCHFILTER_16384 = 0x0Eu, LPTMR_PRESCALE_65536_GLITCHFILTER_32768 = 0x0Fu }
```

Prescaler Selection Implements : `lptmr_prescaler_t` Class.

- enum `lptmr_clocksource_t` { `LPTMR_CLOCKSOURCE_SIRCDIV2` = 0x00u, `LPTMR_CLOCKSOURCE_1_KHZ_LPO` = 0x01u, `LPTMR_CLOCKSOURCE_RTC` = 0x02u, `LPTMR_CLOCKSOURCE_PCC` = 0x03u }

Clock Source selection Implements : `lptmr_clocksource_t` Class.

- enum `lptmr_counter_units_t` { `LPTMR_COUNTER_UNITS_TICKS` = 0x00U, `LPTMR_COUNTER_UNITS_MICROSECONDS` = 0x01U }

Defines the LPTMR counter units available for configuring or reading the timer compare value.

LPTMR Driver Functions

- void `LPTMR_DRV_InitConfigStruct` (`lptmr_config_t` *const config)
Initialize a configuration structure with default values.
- void `LPTMR_DRV_Init` (const uint32_t instance, const `lptmr_config_t` *const config, const bool startCounter)
Initialize a LPTMR instance with values from an input configuration structure.
- void `LPTMR_DRV_SetConfig` (const uint32_t instance, const `lptmr_config_t` *const config)
Configure a LPTMR instance.
- void `LPTMR_DRV_GetConfig` (const uint32_t instance, `lptmr_config_t` *const config)
Get the current configuration of a LPTMR instance.
- void `LPTMR_DRV_Deinit` (const uint32_t instance)
De-initialize a LPTMR instance.
- status_t `LPTMR_DRV_SetCompareValueByCount` (const uint32_t instance, const uint16_t compareValueByCount)
Set the compare value in counter tick units, for a LPTMR instance.
- void `LPTMR_DRV_GetCompareValueByCount` (const uint32_t instance, uint16_t *const compareValueByCount)
Get the compare value in counter tick units, of a LPTMR instance.
- status_t `LPTMR_DRV_SetCompareValueByUs` (const uint32_t instance, const uint32_t compareValueUs)
Set the compare value for Timer Mode in microseconds, for a LPTMR instance.
- void `LPTMR_DRV_GetCompareValueByUs` (const uint32_t instance, uint32_t *const compareValueUs)
Get the compare value in microseconds, of a LPTMR instance.
- bool `LPTMR_DRV_GetCompareFlag` (const uint32_t instance)
Get the current state of the Compare Flag of a LPTMR instance.
- void `LPTMR_DRV_ClearCompareFlag` (const uint32_t instance)
Clear the Compare Flag of a LPTMR instance.
- bool `LPTMR_DRV_IsRunning` (const uint32_t instance)
Get the run state of a LPTMR instance.
- void `LPTMR_DRV_SetInterrupt` (const uint32_t instance, const bool enableInterrupt)
Enable/disable the LPTMR interrupt.
- uint16_t `LPTMR_DRV_GetCounterValueByCount` (const uint32_t instance)
Get the current counter value in counter tick units.
- void `LPTMR_DRV_StartCounter` (const uint32_t instance)
Enable the LPTMR / Start the counter.
- void `LPTMR_DRV_StopCounter` (const uint32_t instance)
Disable the LPTMR / Stop the counter.

- void [LPTMR_DRV_SetPinConfiguration](#) (const uint32_t instance, const [lptmr_pinselect_t](#) pinSelect, const [lptmr_pinpolarity_t](#) pinPolarity)

Set the Input Pin configuration for Pulse Counter mode.

17.86.2 Data Structure Documentation

17.86.2.1 struct lptmr_config_t

Defines the configuration structure for LPTMR.

Implements : [lptmr_config_t_Class](#)

Definition at line 110 of file [lptmr_driver.h](#).

Data Fields

- bool [dmaRequest](#)
- bool [interruptEnable](#)
- bool [freeRun](#)
- [lptmr_workmode_t](#) workMode
- [lptmr_clocksource_t](#) clockSelect
- [lptmr_prescaler_t](#) prescaler
- bool [bypassPrescaler](#)
- uint32_t [compareValue](#)
- [lptmr_counter_units_t](#) counterUnits
- [lptmr_pinselect_t](#) pinSelect
- [lptmr_pinpolarity_t](#) pinPolarity

Field Documentation

17.86.2.1.1 bool bypassPrescaler

Enable/Disable prescaler bypass

Definition at line 120 of file [lptmr_driver.h](#).

17.86.2.1.2 lptmr_clocksource_t clockSelect

Clock selection for Timer/Glitch filter

Definition at line 118 of file [lptmr_driver.h](#).

17.86.2.1.3 uint32_t compareValue

Compare value

Definition at line 121 of file [lptmr_driver.h](#).

17.86.2.1.4 lptmr_counter_units_t counterUnits

Compare value units

Definition at line 122 of file [lptmr_driver.h](#).

17.86.2.1.5 bool dmaRequest

Enable/Disable DMA requests

Definition at line 113 of file [lptmr_driver.h](#).

17.86.2.1.6 bool freeRun

Enable/Disable Free Running Mode

Definition at line 115 of file lptmr_driver.h.

17.86.2.1.7 bool interruptEnable

Enable/Disable Interrupt

Definition at line 114 of file lptmr_driver.h.

17.86.2.1.8 lptmr_pinpolarity_t pinPolarity

Pin Polarity for Pulse-Counter

Definition at line 125 of file lptmr_driver.h.

17.86.2.1.9 lptmr_pinselect_t pinSelect

Pin selection for Pulse-Counter

Definition at line 124 of file lptmr_driver.h.

17.86.2.1.10 lptmr_prescaler_t prescaler

Prescaler Selection

Definition at line 119 of file lptmr_driver.h.

17.86.2.1.11 lptmr_workmode_t workMode

Time/Pulse Counter Mode

Definition at line 116 of file lptmr_driver.h.

17.86.3 Enumeration Type Documentation

17.86.3.1 enum lptmr_clocksource_t

Clock Source selection Implements : lptmr_clocksource_t_Class.

Enumerator

LPTMR_CLOCKSOURCE_SIRCDIV2 SIRC clock

LPTMR_CLOCKSOURCE_1KHZ_LPO 1kHz LPO clock

LPTMR_CLOCKSOURCE_RTC RTC clock

LPTMR_CLOCKSOURCE_PCC PCC configured clock

Definition at line 87 of file lptmr_driver.h.

17.86.3.2 enum lptmr_counter_units_t

Defines the LPTMR counter units available for configuring or reading the timer compare value.

Implements : lptmr_counter_units_t_Class

Enumerator

LPTMR_COUNTER_UNITS_TICKS

LPTMR_COUNTER_UNITS_MICROSECONDS

Definition at line 99 of file lptmr_driver.h.

17.86.3.3 enum `lptmr_pinpolarity_t`

Pulse Counter input polarity Implements : `lptmr_pinpolarity_t_Class`.

Enumerator

`LPTMR_PINPOLARITY_RISING` Count pulse on rising edge
`LPTMR_PINPOLARITY_FALLING` Count pulse on falling edge

Definition at line 49 of file `lptmr_driver.h`.

17.86.3.4 enum `lptmr_pinselect_t`

Pulse Counter Input selection Implements : `lptmr_pinselect_t_Class`.

Enumerator

`LPTMR_PINSELECT_TRGMUX` Count pulses from TRGMUX trigger
`LPTMR_PINSELECT_ALT2` Count pulses from pin alternative 2
`LPTMR_PINSELECT_ALT3` Count pulses from pin alternative 3

Definition at line 37 of file `lptmr_driver.h`.

17.86.3.5 enum `lptmr_prescaler_t`

Prescaler Selection Implements : `lptmr_prescaler_t_Class`.

Enumerator

`LPTMR_PRESCALE_2` Timer mode: prescaler 2, Glitch filter mode: invalid
`LPTMR_PRESCALE_4_GLITCHFILTER_2` Timer mode: prescaler 4, Glitch filter mode: 2 clocks
`LPTMR_PRESCALE_8_GLITCHFILTER_4` Timer mode: prescaler 8, Glitch filter mode: 4 clocks
`LPTMR_PRESCALE_16_GLITCHFILTER_8` Timer mode: prescaler 16, Glitch filter mode: 8 clocks
`LPTMR_PRESCALE_32_GLITCHFILTER_16` Timer mode: prescaler 32, Glitch filter mode: 16 clocks
`LPTMR_PRESCALE_64_GLITCHFILTER_32` Timer mode: prescaler 64, Glitch filter mode: 32 clocks
`LPTMR_PRESCALE_128_GLITCHFILTER_64` Timer mode: prescaler 128, Glitch filter mode: 64 clocks
`LPTMR_PRESCALE_256_GLITCHFILTER_128` Timer mode: prescaler 256, Glitch filter mode: 128 clocks
`LPTMR_PRESCALE_512_GLITCHFILTER_256` Timer mode: prescaler 512, Glitch filter mode: 256 clocks
`LPTMR_PRESCALE_1024_GLITCHFILTER_512` Timer mode: prescaler 1024, Glitch filter mode: 512 clocks

`LPTMR_PRESCALE_2048_GLITCHFILTER_1024` Timer mode: prescaler 2048, Glitch filter mode: 1024 clocks
`LPTMR_PRESCALE_4096_GLITCHFILTER_2048` Timer mode: prescaler 4096, Glitch filter mode: 2048 clocks
`LPTMR_PRESCALE_8192_GLITCHFILTER_4096` Timer mode: prescaler 8192, Glitch filter mode: 4096 clocks
`LPTMR_PRESCALE_16384_GLITCHFILTER_8192` Timer mode: prescaler 16384, Glitch filter mode: 8192 clocks
`LPTMR_PRESCALE_32768_GLITCHFILTER_16384` Timer mode: prescaler 32768, Glitch filter mode: 16384 clocks
`LPTMR_PRESCALE_65536_GLITCHFILTER_32768` Timer mode: prescaler 65536, Glitch filter mode: 32768 clocks

Definition at line 65 of file `lptmr_driver.h`.

17.86.3.6 enum `lptmr_workmode_t`

Work Mode Implements : `lptmr_workmode_t_Class`.

Enumerator

`LPTMR_WORKMODE_TIMER` Timer

`LPTMR_WORKMODE_PULSECOUNTER` Pulse counter

Definition at line 57 of file `lptmr_driver.h`.

17.86.4 Function Documentation

17.86.4.1 void `LPTMR_DRV_ClearCompareFlag (const uint32_t instance)`

Clear the Compare Flag of a LPTMR instance.

Parameters

in	<i>instance</i>	- LPTMR instance number
----	-----------------	-------------------------

17.86.4.2 void `LPTMR_DRV_Deinit (const uint32_t instance)`

De-initialize a LPTMR instance.

Parameters

in	<i>instance</i>	- LPTMR instance number
----	-----------------	-------------------------

17.86.4.3 bool `LPTMR_DRV_GetCompareFlag (const uint32_t instance)`

Get the current state of the Compare Flag of a LPTMR instance.

Parameters

in	<i>instance</i>	- LPTMR instance number
----	-----------------	-------------------------

Returns

The state of the Compare Flag

17.86.4.4 void `LPTMR_DRV_GetCompareValueByCount (const uint32_t instance, uint16_t *const compareValueByCount)`

Get the compare value in counter tick units, of a LPTMR instance.

Parameters

in	<i>instance</i>	- LPTMR instance number
out	<i>compareValueByCount</i>	- Pointer to current compare value, in counter ticks

17.86.4.5 void `LPTMR_DRV_GetCompareValueByUs (const uint32_t instance, uint32_t *const compareValueUs)`

Get the compare value in microseconds, of a LPTMR instance.

Parameters

in	<i>instance</i>	- LPTMR instance number
out	<i>compareValue</i> ↔ <i>Us</i>	- Pointer to current compare value, in microseconds

17.86.4.6 void LPTMR_DRV_GetConfig (const uint32_t *instance*, lptmr_config_t *const *config*)

Get the current configuration of a LPTMR instance.

Parameters

in	<i>instance</i>	- LPTMR instance number
out	<i>config</i>	- Pointer to the output configuration structure

17.86.4.7 uint16_t LPTMR_DRV_GetCounterValueByCount (const uint32_t *instance*)

Get the current counter value in counter tick units.

Parameters

in	<i>instance</i>	- LPTMR instance number
----	-----------------	-------------------------

Returns

The current counter value

17.86.4.8 void LPTMR_DRV_Init (const uint32_t *instance*, const lptmr_config_t *const *config*, const bool *startCounter*)

Initialize a LPTMR instance with values from an input configuration structure.

When (counterUnits == LPTMR_COUNTER_UNITS_MICROSECONDS) the function will automatically configure the timer for the input compareValue in microseconds. The input parameters for 'prescaler' and 'bypassPrescaler' will be ignored - their values will be adapted by the function, to best fit the input compareValue (in microseconds) for the operating clock frequency.

LPTMR_COUNTER_UNITS_MICROSECONDS may only be used for LPTMR_WORKMODE_TIMER mode. Otherwise the function shall not convert 'compareValue' in ticks and this is likely to cause erroneous behavior.

When (counterUnits == LPTMR_COUNTER_UNITS_TICKS) the function will use the 'prescaler' and 'bypassPrescaler' provided in the input configuration structure.

Parameters

in	<i>instance</i>	- LPTMR instance number
in	<i>config</i>	- Pointer to the input configuration structure
in	<i>startCounter</i>	- Flag for starting the counter immediately after configuration

17.86.4.9 void LPTMR_DRV_InitConfigStruct (lptmr_config_t *const *config*)

Initialize a configuration structure with default values.

Parameters

out	<i>config</i>	- Pointer to the configuration structure to be initialized
-----	---------------	--

17.86.4.10 bool LPTMR_DRV_IsRunning (const uint32_t *instance*)

Get the run state of a LPTMR instance.

Parameters

<i>in</i>	<i>instance</i>	- LPTMR instance number
-----------	-----------------	-------------------------

Returns

The run state of the LPTMR instance:

- true: Timer/Counter started
- false: Timer/Counter stopped

17.86.4.11 `status_t LPTMR_DRV_SetCompareValueByCount (const uint32_t instance, const uint16_t compareValueByCount)`

Set the compare value in counter tick units, for a LPTMR instance.

Parameters

<i>in</i>	<i>instance</i>	- LPTMR instance number
<i>in</i>	<i>compareValue↔ ByCount</i>	- The compare value in counter ticks, to be written

Returns

Operation status:

- STATUS_SUCCESS: completed successfully
- STATUS_ERROR: cannot reconfigure compare value (TCF not set)
- STATUS_TIMEOUT: compare value greater then current counter value

17.86.4.12 `status_t LPTMR_DRV_SetCompareValueByUs (const uint32_t instance, const uint32_t compareValueUs)`

Set the compare value for Timer Mode in microseconds, for a LPTMR instance.

Parameters

<i>in</i>	<i>instance</i>	- LPTMR peripheral instance number
<i>in</i>	<i>compareValue↔ Us</i>	- Compare value in microseconds

Returns

Operation status:

- STATUS_SUCCESS: completed successfully
- STATUS_ERROR: cannot reconfigure compare value
- STATUS_TIMEOUT: compare value greater then current counter value

17.86.4.13 `void LPTMR_DRV_SetConfig (const uint32_t instance, const lptmr_config_t *const config)`

Configure a LPTMR instance.

When (counterUnits == LPTMR_COUNTER_UNITS_MICROSECONDS) the function will automatically configure the timer for the input compareValue in microseconds. The input parameters for 'prescaler' and 'bypassPrescaler' will be ignored - their values will be adapted by the function, to best fit the input compareValue (in microseconds) for the operating clock frequency.

LPTMR_COUNTER_UNITS_MICROSECONDS may only be used for LPTMR_WORKMODE_TIMER mode. Otherwise the function shall not convert 'compareValue' in ticks and this is likely to cause erroneous behavior.

When (counterUnits == LPTMR_COUNTER_UNITS_TICKS) the function will use the 'prescaler' and 'bypass↔Prescaler' provided in the input configuration structure.

Parameters

in	<i>instance</i>	- LPTMR instance number
in	<i>config</i>	- Pointer to the input configuration structure

17.86.4.14 void LPTMR_DRV_SetInterrupt (const uint32_t *instance*, const bool *enableInterrupt*)

Enable/disable the LPTMR interrupt.

Parameters

in	<i>instance</i>	- LPTMR instance number
in	<i>enableInterrupt</i>	- The new state of the LPTMR interrupt enable flag.

17.86.4.15 void LPTMR_DRV_SetPinConfiguration (const uint32_t *instance*, const lptmr_pinselect_t *pinSelect*, const lptmr_pinpolarity_t *pinPolarity*)

Set the Input Pin configuration for Pulse Counter mode.

Parameters

in	<i>instance</i>	- LPTMR instance number
in	<i>pinSelect</i>	- LPTMR pin selection
in	<i>pinPolarity</i>	- Polarity on which to increment counter (rising/falling edge)

17.86.4.16 void LPTMR_DRV_StartCounter (const uint32_t *instance*)

Enable the LPTMR / Start the counter.

Parameters

in	<i>instance</i>	- LPTMR instance number
----	-----------------	-------------------------

17.86.4.17 void LPTMR_DRV_StopCounter (const uint32_t *instance*)

Disable the LPTMR / Stop the counter.

Parameters

in	<i>instance</i>	- LPTMR instance number
----	-----------------	-------------------------

17.87 LPUART Driver

17.87.1 Detailed Description

This module covers the functionality of the Low Power Universal Asynchronous Receiver-Transmitter (LPUART) peripheral driver.

The LPUART driver implements serial communication using the LPUART module in the S32K1xx platforms.

Features

- Interrupt based, DMA based and polling communication
- Provides blocking and non-blocking transmit and receive functions
- Configurable baud rate
- 8/9/10 bits per char

Functionality

In order to use the LPUART driver it must be first initialized, using [LPUART_DRV_Init\(\)](#) function. Once initialized, it cannot be initialized again for the same LPUART module instance until it is de-initialized, using [LPUART_DRV_Deinit\(\)](#). The initialization function does the following operations:

- sets the baud rate
- sets parity/bit count/stop bits count
- initializes the state structure for the current instance Different LPUART module instances can function independently of each other.

Interrupt-based communication

After initialization, a serial communication can be triggered by calling [LPUART_DRV_SendData\(\)](#) function; this will save the reference of the data buffer received as parameter in the internal tx buffer pointer, then copy the first byte to the data register. The transmitter then automatically shifts the data and triggers a 'Transmit buffer empty' interrupt when all bits are shifted. The drivers interrupt handler takes care of transmitting the next byte in the buffer, by increasing the data pointer and decreasing the data size. The same sequence of operations is executed until all bytes in the tx buffer have been transmitted.

Similarly, data reception is triggered by calling [LPUART_DRV_ReceiveData\(\)](#) function, passing the rx buffer as parameter. When the receiver copies the received bits in the data register, the 'Receive buffer full' interrupt is triggered; the driver irq handler clears the flag by reading the received byte, saves it in the rx buffer, then increments the data pointer and decrements the data size. This is repeated until all bytes are received.

The workflow applies to send/receive operations using blocking method (triggered by [LPUART_DRV_SendDataBlocking\(\)](#) and [LPUART_DRV_ReceiveDataBlocking\(\)](#)), with the single difference that the send/receive function will not return until the send/receive operation is complete (all bytes are successfully transferred or a timeout occurred). The timeout for the blocking method is passed as parameter by the user.

DMA-based communication

In DMA operation, both blocking and non-blocking transmission methods configure a DMA channel to copy data from the buffer to the data register (for tx), or viceversa (for rx). The driver assumes the DMA channel is already allocated and the proper requests are routed to it via DMAMUX. After configuring the DMA channel, the driver enables DMA requests for rx/tx, then the DMA engine takes care of moving data to/from the data buffer.

Polling mode

The driver also provides polling methods for send and receive ([LPUART_DRV_SendDataPolling\(\)](#) and [LPUART_DRV_ReceiveDataPolling\(\)](#)). These functions are blocking (return only when the transfer is complete) and do not use interrupt or DMA services. The tx buffer empty and rx buffer full flags are polled by software in order to copy data to/from the data register.

Error handling

The driver treats the following errors on reception:

- rx overrun
- parity error
- framing error
- noise error

In case any of these error events occur on the rx line during an ongoing reception, the transfer is aborted and rx status is updated accordingly. [LPUART_DRV_GetReceiveStatus\(\)](#) function can be called to retrieve the status of the last reception. If a receive callback is installed, it is called right after aborting the current transfer (with `UART_EVENT_ERROR` parameter).

Callbacks

The driver provides callback notifications for asynchronous transfers. [LPUART_DRV_InstallTxCallback\(\)](#) function can be used for installing a callback routine to be called when the transmission is finished. The tx callback is called twice: first when the tx buffer becomes empty (no more data to be transmitted) - at this point the application can call [LPUART_DRV_SetTxBuffer\(\)](#) inside the callback in order to provide more data, resulting in a continuous transmission; if there is no more data to be transmitted, the callback is called again when the transmission is complete (all the bytes have been shifted out on the line). The event parameter in the callback signature differentiates these two calls - the values are `UART_EVENT_TX_EMPTY` and `UART_EVENT_END_TRANSFER`, respectively.

Similarly, [LPUART_DRV_InstallRxCallback\(\)](#) installs a callback routine for reception. This callback is called twice (`UART_EVENT_RX_FULL` and `UART_EVENT_END_TRANSFER`); if a new buffer is provided within the first callback call ([LPUART_DRV_SetRxBuffer\(\)](#)), the reception will continue without interruption. In case of an error detected during an ongoing reception, the transfer is aborted and the callback is called with `UART_EVENT_ERROR` parameter. The driver treats rx overrun, parity, framing and noise errors.

Important Notes

- Before using the LPUART driver the module clock must be configured
- The driver enables the interrupts for the corresponding LPUART module, but any interrupt priority must be done by the application
- The board specific configurations must be done prior to driver calls; the driver has no influence on the functionality of the rx/tx pins - they must be configured by application
- DMA module has to be initialized prior to LPUART usage in DMA mode; also, DMA channels need to be allocated for LPUART usage by the application (the driver only takes care of configuring the DMA channels received in the configuration structure)
- For 9/10 bits characters, the application must provide the appropriate buffers; the size of the tx/rx buffers in this scenario needs to be an even number, as the transferred characters will be split in two bytes (bit 8 for 9-bits chars and bits 8 & 9 for 10-bits chars will be stored in the subsequent byte). 9/10 bits chars are only supported in interrupt-based and polling communications
- For 10-bits word length, parity cannot be enabled.
- When the vector table is not in ram (**flash_vector_table** = 1):
 - `INT_SYS_InstallHandler` shall check if the function pointer provided as parameter for the new handler is already present in the vector table for the given IRQ number.
 - The user will be required to manually add the correct handlers in the startup files

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\drivers\src\lpuart\lpuart_driver.c
{S32SDK_PATH}\platform\drivers\src\lpuart\lpuart_hw_access.c
{S32SDK_PATH}\platform\drivers\src\lpuart\lpuart_irq.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\drivers\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager Interrupt Manager \(Interrupt\) Enhanced Direct Memory Access \(eDMA\)](#)

Data Structures

- struct [lpuart_state_t](#)
Runtime state of the LPUART driver. [More...](#)
- struct [lpuart_user_config_t](#)
LPUART configuration structure. [More...](#)

Enumerations

- enum [lpuart_transfer_type_t](#) { LPUART_USING_DMA = 0, LPUART_USING_INTERRUPTS }
Type of LPUART transfer (based on interrupts or DMA).
- enum [lpuart_bit_count_per_char_t](#) { LPUART_8_BITS_PER_CHAR = 0x0U, LPUART_9_BITS_PER_CHAR = 0x1U, LPUART_10_BITS_PER_CHAR = 0x2U }
LPUART number of bits in a character.
- enum [lpuart_parity_mode_t](#) { LPUART_PARITY_DISABLED = 0x0U, LPUART_PARITY_EVEN = 0x2U, LPUART_PARITY_ODD = 0x3U }
LPUART parity mode.
- enum [lpuart_stop_bit_count_t](#) { LPUART_ONE_STOP_BIT = 0x0U, LPUART_TWO_STOP_BIT = 0x1U }
LPUART number of stop bits.

LPUART Driver

- void [LPUART_DRV_GetDefaultConfig](#) ([lpuart_user_config_t](#) *lpuartUserConfig)
Initializes the LPUART configuration structure with default values.
- status_t [LPUART_DRV_Init](#) (uint32_t instance, [lpuart_state_t](#) *lpuartStatePtr, const [lpuart_user_config_t](#) *lpuartUserConfig)
Initializes an LPUART operation instance.
- status_t [LPUART_DRV_Deinit](#) (uint32_t instance)
Shuts down the LPUART by disabling interrupts and transmitter/receiver.
- uart_callback_t [LPUART_DRV_InstallRxCallback](#) (uint32_t instance, uart_callback_t function, void *callbackParam)

Installs callback function for the LPUART receive.

- `uart_callback_t LPUART_DRV_InstallTxCallback` (`uint32_t` instance, `uart_callback_t` function, `void *callbackParam`)

Installs callback function for the LPUART transmit.

- `status_t LPUART_DRV_SendDataBlocking` (`uint32_t` instance, `const uint8_t *txBuff`, `uint32_t` txSize, `uint32_t` timeout)

Sends data out through the LPUART module using a blocking method.

- `status_t LPUART_DRV_SendDataPolling` (`uint32_t` instance, `const uint8_t *txBuff`, `uint32_t` txSize)

Send out multiple bytes of data using polling method.

- `status_t LPUART_DRV_SendData` (`uint32_t` instance, `const uint8_t *txBuff`, `uint32_t` txSize)

Sends data out through the LPUART module using a non-blocking method. This enables an a-sync method for transmitting data. When used with a non-blocking receive, the LPUART can perform a full duplex operation. Non-blocking means that the function returns immediately. The application has to get the transmit status to know when the transmit is complete.

- `status_t LPUART_DRV_GetTransmitStatus` (`uint32_t` instance, `uint32_t *bytesRemaining`)

Returns whether the previous transmit is complete.

- `status_t LPUART_DRV_AbortSendingData` (`uint32_t` instance)

Terminates a non-blocking transmission early.

- `status_t LPUART_DRV_ReceiveDataBlocking` (`uint32_t` instance, `uint8_t *rxBuff`, `uint32_t` rxSize, `uint32_t` timeout)

Gets data from the LPUART module by using a blocking method. Blocking means that the function does not return until the receive is complete.

- `status_t LPUART_DRV_ReceiveDataPolling` (`uint32_t` instance, `uint8_t *rxBuff`, `uint32_t` rxSize)

Receive multiple bytes of data using polling method.

- `status_t LPUART_DRV_ReceiveData` (`uint32_t` instance, `uint8_t *rxBuff`, `uint32_t` rxSize)

Gets data from the LPUART module by using a non-blocking method. This enables an a-sync method for receiving data. When used with a non-blocking transmission, the LPUART can perform a full duplex operation. Non-blocking means that the function returns immediately. The application has to get the receive status to know when the receive is complete.

- `status_t LPUART_DRV_GetReceiveStatus` (`uint32_t` instance, `uint32_t *bytesRemaining`)

Returns whether the previous receive is complete.

- `status_t LPUART_DRV_AbortReceivingData` (`uint32_t` instance)

Terminates a non-blocking receive early.

- `status_t LPUART_DRV_SetBaudRate` (`uint32_t` instance, `uint32_t` desiredBaudRate)

Configures the LPUART baud rate.

- `void LPUART_DRV_GetBaudRate` (`uint32_t` instance, `uint32_t *configuredBaudRate`)

Returns the LPUART baud rate.

- `status_t LPUART_DRV_SetTxBuffer` (`uint32_t` instance, `const uint8_t *txBuff`, `uint32_t` txSize)

Sets the internal driver reference to the tx buffer.

- `status_t LPUART_DRV_SetRxBuffer` (`uint32_t` instance, `uint8_t *rxBuff`, `uint32_t` rxSize)

Sets the internal driver reference to the rx buffer.

17.87.2 Data Structure Documentation

17.87.2.1 struct lpuart_state_t

Runtime state of the LPUART driver.

Note that the caller provides memory for the driver state structures during initialization because the driver does not statically allocate memory.

Implements : `lpuart_state_t` Class

Definition at line 89 of file `lpuart_driver.h`.

Data Fields

- `const uint8_t * txBuff`
- `uint8_t * rxBuff`
- `volatile uint32_t txSize`
- `volatile uint32_t rxSize`
- `volatile bool isTxBusy`
- `volatile bool isRxBusy`
- `volatile bool isTxBlocking`
- `volatile bool isRxBlocking`
- `lpuart_bit_count_per_char_t bitCountPerChar`
- `uart_callback_t rxCallback`
- `void * rxCallbackParam`
- `uart_callback_t txCallback`
- `void * txCallbackParam`
- `lpuart_transfer_type_t transferType`
- `semaphore_t rxComplete`
- `semaphore_t txComplete`
- `volatile status_t transmitStatus`
- `volatile status_t receiveStatus`

Field Documentation

17.87.2.1.1 `lpuart_bit_count_per_char_t bitCountPerChar`

number of bits in a char (8/9/10)

Definition at line 99 of file `lpuart_driver.h`.

17.87.2.1.2 `volatile bool isRxBlocking`

True if receive is blocking transaction.

Definition at line 98 of file `lpuart_driver.h`.

17.87.2.1.3 `volatile bool isRxBusy`

True if there is an active receive.

Definition at line 96 of file `lpuart_driver.h`.

17.87.2.1.4 `volatile bool isTxBlocking`

True if transmit is blocking transaction.

Definition at line 97 of file `lpuart_driver.h`.

17.87.2.1.5 `volatile bool isTxBusy`

True if there is an active transmit.

Definition at line 95 of file `lpuart_driver.h`.

17.87.2.1.6 `volatile status_t receiveStatus`

Status of last driver receive operation

Definition at line 120 of file `lpuart_driver.h`.

17.87.2.1.7 `uint8_t* rxBuff`

The buffer of received data.

Definition at line 92 of file `lpuart_driver.h`.

17.87.2.1.8 uart_callback_t rxCallback

Callback to invoke for data receive Note: when the transmission is interrupt based, the callback is being called upon receiving a byte; when DMA transmission is used, the bytes are copied to the rx buffer by the DMA engine and the callback is called when all the bytes have been transferred.

Definition at line 100 of file lpuart_driver.h.

17.87.2.1.9 void* rxCallbackParam

Receive callback parameter pointer.

Definition at line 105 of file lpuart_driver.h.

17.87.2.1.10 semaphore_t rxComplete

Synchronization object for blocking Rx timeout condition

Definition at line 117 of file lpuart_driver.h.

17.87.2.1.11 volatile uint32_t rxSize

The remaining number of bytes to be received.

Definition at line 94 of file lpuart_driver.h.

17.87.2.1.12 lpuart_transfer_type_t transferType

Type of LPUART transfer (interrupt/dma based)

Definition at line 112 of file lpuart_driver.h.

17.87.2.1.13 volatile status_t transmitStatus

Status of last driver transmit operation

Definition at line 119 of file lpuart_driver.h.

17.87.2.1.14 const uint8_t* txBuff

The buffer of data being sent.

Definition at line 91 of file lpuart_driver.h.

17.87.2.1.15 uart_callback_t txCallback

Callback to invoke for data send Note: when the transmission is interrupt based, the callback is being called upon sending a byte; when DMA transmission is used, the bytes are copied to the tx buffer by the DMA engine and the callback is called when all the bytes have been transferred.

Definition at line 106 of file lpuart_driver.h.

17.87.2.1.16 void* txCallbackParam

Transmit callback parameter pointer.

Definition at line 111 of file lpuart_driver.h.

17.87.2.1.17 semaphore_t txComplete

Synchronization object for blocking Tx timeout condition

Definition at line 118 of file lpuart_driver.h.

17.87.2.1.18 volatile uint32_t txSize

The remaining number of bytes to be transmitted.

Definition at line 93 of file lpuart_driver.h.

17.87.2.2 struct lpuart_user_config_t

LPUART configuration structure.

Implements : lpuart_user_config_t_Class

Definition at line 127 of file lpuart_driver.h.

Data Fields

- uint32_t [baudRate](#)
- [lpuart_parity_mode_t](#) parityMode
- [lpuart_stop_bit_count_t](#) stopBitCount
- [lpuart_bit_count_per_char_t](#) bitCountPerChar
- [lpuart_transfer_type_t](#) transferType
- uint8_t rxDMAChannel
- uint8_t txDMAChannel

Field Documentation

17.87.2.2.1 uint32_t baudRate

LPUART baud rate

Definition at line 129 of file lpuart_driver.h.

17.87.2.2.2 lpuart_bit_count_per_char_t bitCountPerChar

number of bits in a character (8-default, 9 or 10); for 9/10 bits chars, users must provide appropriate buffers to the send/receive functions (bits 8/9 in subsequent bytes); for DMA transmission only 8-bit char is supported.

Definition at line 132 of file lpuart_driver.h.

17.87.2.2.3 lpuart_parity_mode_t parityMode

parity mode, disabled (default), even, odd

Definition at line 130 of file lpuart_driver.h.

17.87.2.2.4 uint8_t rxDMAChannel

Channel number for DMA rx channel. If DMA mode isn't used this field will be ignored.

Definition at line 137 of file lpuart_driver.h.

17.87.2.2.5 lpuart_stop_bit_count_t stopBitCount

number of stop bits, 1 stop bit (default) or 2 stop bits

Definition at line 131 of file lpuart_driver.h.

17.87.2.2.6 lpuart_transfer_type_t transferType

Type of LPUART transfer (interrupt/dma based)

Definition at line 136 of file lpuart_driver.h.

17.87.2.2.7 uint8_t txDMAChannel

Channel number for DMA tx channel. If DMA mode isn't used this field will be ignored.

Definition at line 139 of file lpuart_driver.h.

17.87.3 Enumeration Type Documentation

17.87.3.1 enum lpuart_bit_count_per_char_t

LPUART number of bits in a character.

Implements : lpuart_bit_count_per_char_t_Class

Enumerator

LPUART_8_BITS_PER_CHAR 8-bit data characters
LPUART_9_BITS_PER_CHAR 9-bit data characters
LPUART_10_BITS_PER_CHAR 10-bit data characters

Definition at line 53 of file lpuart_driver.h.

17.87.3.2 enum lpuart_parity_mode_t

LPUART parity mode.

Implements : lpuart_parity_mode_t_Class

Enumerator

LPUART_PARITY_DISABLED parity disabled
LPUART_PARITY_EVEN parity enabled, type even, bit setting: PE|PT = 10
LPUART_PARITY_ODD parity enabled, type odd, bit setting: PE|PT = 11

Definition at line 64 of file lpuart_driver.h.

17.87.3.3 enum lpuart_stop_bit_count_t

LPUART number of stop bits.

Implements : lpuart_stop_bit_count_t_Class

Enumerator

LPUART_ONE_STOP_BIT one stop bit
LPUART_TWO_STOP_BIT two stop bits

Definition at line 75 of file lpuart_driver.h.

17.87.3.4 enum lpuart_transfer_type_t

Type of LPUART transfer (based on interrupts or DMA).

Implements : lpuart_transfer_type_t_Class

Enumerator

LPUART_USING_DMA The driver will use DMA to perform UART transfer
LPUART_USING_INTERRUPTS The driver will use interrupts to perform UART transfer

Definition at line 43 of file lpuart_driver.h.

17.87.4 Function Documentation

17.87.4.1 status_t LPUART_DRV_AbortReceivingData (uint32_t instance)

Terminates a non-blocking receive early.

Parameters

<i>instance</i>	LPUART instance number
-----------------	------------------------

Returns

Whether the receiving was successful or not.

Definition at line 891 of file lpuart_driver.c.

17.87.4.2 status_t LPUART_DRV_AbortSendingData (uint32_t *instance*)

Terminates a non-blocking transmission early.

Parameters

<i>instance</i>	LPUART instance number
-----------------	------------------------

Returns

Whether the aborting is successful or not.

Definition at line 580 of file lpuart_driver.c.

17.87.4.3 status_t LPUART_DRV_Deinit (uint32_t *instance*)

Shuts down the LPUART by disabling interrupts and transmitter/receiver.

Parameters

<i>instance</i>	LPUART instance number
-----------------	------------------------

Returns

STATUS_SUCCESS if successful; STATUS_ERROR if an error occurred

Definition at line 278 of file lpuart_driver.c.

17.87.4.4 void LPUART_DRV_GetBaudRate (uint32_t *instance*, uint32_t * *configuredBaudRate*)

Returns the LPUART baud rate.

This function returns the LPUART configured baud rate.

Parameters

	<i>instance</i>	LPUART instance number.
out	<i>configuredBaudRate</i>	LPUART configured baud rate.

Definition at line 1036 of file lpuart_driver.c.

17.87.4.5 void LPUART_DRV_GetDefaultConfig (lpuart_user_config_t * *lpuartUserConfig*)

Initializes the LPUART configuration structure with default values.

This function initializes a configuration structure received from the application with default values.

Parameters

<i>lpuartUserConfig</i>	user configuration structure of type lpuart_user_config_t
-------------------------	---

Definition at line 145 of file `lpuart_driver.c`.

17.87.4.6 `status_t LPUART_DRV_GetReceiveStatus (uint32_t instance, uint32_t * bytesRemaining)`

Returns whether the previous receive is complete.

Parameters

<i>instance</i>	LPUART instance number
<i>bytesRemaining</i>	pointer to value that is filled with the number of bytes that still need to be received in the active transfer.

Note

In DMA mode, this parameter may not be accurate, in case the transfer completes right after calling this function; in this edge-case, the parameter will reflect the initial transfer size, due to automatic reloading of the major loop count in the DMA transfer descriptor.

Returns

The receive status.

Return values

<i>STATUS_SUCCESS</i>	the receive has completed successfully.
<i>STATUS_BUSY</i>	the receive is still in progress. <i>bytesReceived</i> will be filled with the number of bytes that have been received so far.
<i>STATUS_UART_ABORTED</i>	The receive was aborted.
<i>STATUS_TIMEOUT</i>	A timeout was reached.
<i>STATUS_UART_RX_OVERRUN, STATUS_UART_FRAMING_ERROR, STATUS_UART_PARITY_ERROR, or</i>	<i>STATUS_UART_NOISE_ERROR, STATUS_ERROR</i> An error occurred during reception.

Definition at line 846 of file `lpuart_driver.c`.

17.87.4.7 `status_t LPUART_DRV_GetTransmitStatus (uint32_t instance, uint32_t * bytesRemaining)`

Returns whether the previous transmit is complete.

Parameters

<i>instance</i>	LPUART instance number
<i>bytesRemaining</i>	Pointer to value that is populated with the number of bytes that have been sent in the active transfer

Note

In DMA mode, this parameter may not be accurate, in case the transfer completes right after calling this function; in this edge-case, the parameter will reflect the initial transfer size, due to automatic reloading of the major loop count in the DMA transfer descriptor.

Returns

The transmit status.

Return values

<i>STATUS_SUCCESS</i>	The transmit has completed successfully.
<i>STATUS_BUSY</i>	The transmit is still in progress. <i>bytesRemaining</i> will be filled with the number of bytes that are yet to be transmitted.
<i>STATUS_UART_ABORTED</i>	The transmit was aborted.
<i>STATUS_TIMEOUT</i>	A timeout was reached.
<i>STATUS_ERROR</i>	An error occurred.

Definition at line 534 of file `lpuart_driver.c`.

17.87.4.8 `status_t LPUART_DRV_Init (uint32_t instance, lpuart_state_t * lpuartStatePtr, const lpuart_user_config_t * lpuartUserConfig)`

Initializes an LPUART operation instance.

The caller provides memory for the driver state structures during initialization. The user must select the LPUART clock source in the application to initialize the LPUART.

Parameters

<i>instance</i>	LPUART instance number
<i>lpuartUserConfig</i>	user configuration structure of type <code>lpuart_user_config_t</code>
<i>lpuartStatePtr</i>	pointer to the LPUART driver state structure

Returns

`STATUS_SUCCESS` if successful; `STATUS_ERROR` if an error occurred

Definition at line 181 of file `lpuart_driver.c`.

17.87.4.9 `uart_callback_t LPUART_DRV_InstallRxCallback (uint32_t instance, uart_callback_t function, void * callbackParam)`

Installs callback function for the LPUART receive.

Note

After a callback is installed, it bypasses part of the LPUART IRQHandler logic. Therefore, the callback needs to handle the indexes of `txBuff` and `txSize`.

Parameters

<i>instance</i>	The LPUART instance number.
<i>function</i>	The LPUART receive callback function.
<i>rxBuff</i>	The receive buffer used inside IRQHandler. This buffer must be kept as long as the callback is alive.
<i>callbackParam</i>	The LPUART receive callback parameter pointer.

Returns

Former LPUART receive callback function pointer.

Definition at line 319 of file `lpuart_driver.c`.

17.87.4.10 `uart_callback_t LPUART_DRV_InstallTxCallback (uint32_t instance, uart_callback_t function, void * callbackParam)`

Installs callback function for the LPUART transmit.

Note

After a callback is installed, it bypasses part of the LPUART IRQHandler logic. Therefore, the callback needs to handle the indexes of txBuff and txSize.

Parameters

<i>instance</i>	The LPUART instance number.
<i>function</i>	The LPUART transmit callback function.
<i>txBuff</i>	The transmit buffer used inside IRQHandler. This buffer must be kept as long as the callback is alive.
<i>callbackParam</i>	The LPUART transmit callback parameter pointer.

Returns

Former LPUART transmit callback function pointer.

Definition at line 342 of file lpuart_driver.c.

17.87.4.11 status_t LPUART_DRV_ReceiveData (uint32_t instance, uint8_t * rxBuff, uint32_t rxSize)

Gets data from the LPUART module by using a non-blocking method. This enables an a-sync method for receiving data. When used with a non-blocking transmission, the LPUART can perform a full duplex operation. Non-blocking means that the function returns immediately. The application has to get the receive status to know when the receive is complete.

Parameters

<i>instance</i>	LPUART instance number
<i>rxBuff</i>	buffer containing 8-bit read data chars received
<i>rxSize</i>	the number of bytes to receive

Returns

STATUS_SUCCESS if successful; STATUS_BUSY if the resource is busy

Definition at line 803 of file lpuart_driver.c.

17.87.4.12 status_t LPUART_DRV_ReceiveDataBlocking (uint32_t instance, uint8_t * rxBuff, uint32_t rxSize, uint32_t timeout)

Gets data from the LPUART module by using a blocking method. Blocking means that the function does not return until the receive is complete.

Parameters

<i>instance</i>	LPUART instance number
<i>rxBuff</i>	buffer containing 8-bit read data chars received
<i>rxSize</i>	the number of bytes to receive
<i>timeout</i>	timeout value in milliseconds

Returns

STATUS_SUCCESS if successful; STATUS_TIMEOUT if the timeout was reached; STATUS_BUSY if the resource is busy; STATUS_UART_FRAMING_ERROR if a framing error occurred; STATUS_UART_NOISE_ERROR if a noise error occurred; STATUS_UART_PARITY_ERROR if a parity error occurred; STATUS_UART_RX_OVERRUN if an overrun error occurred; STATUS_ERROR if a DMA error occurred;

Definition at line 618 of file lpuart_driver.c.

17.87.4.13 status_t LPUART_DRV_ReceiveDataPolling (uint32_t instance, uint8_t * rxBuff, uint32_t rxSize)

Receive multiple bytes of data using polling method.

Parameters

<i>instance</i>	LPUART instance number.
<i>rxBuff</i>	The buffer pointer which saves the data to be received.
<i>rxSize</i>	Size of data need to be received in unit of byte.

Returns

STATUS_SUCCESS if the transaction is successful; STATUS_BUSY if the resource is busy; STATUS_UART_RX_OVERRUN if an overrun error occurred.

Definition at line 683 of file lpuart_driver.c.

17.87.4.14 `status_t LPUART_DRV_SendData (uint32_t instance, const uint8_t * txBuff, uint32_t txSize)`

Sends data out through the LPUART module using a non-blocking method. This enables an a-sync method for transmitting data. When used with a non-blocking receive, the LPUART can perform a full duplex operation. Non-blocking means that the function returns immediately. The application has to get the transmit status to know when the transmit is complete.

Parameters

<i>instance</i>	LPUART instance number
<i>txBuff</i>	source buffer containing 8-bit data chars to send
<i>txSize</i>	the number of bytes to send

Returns

STATUS_SUCCESS if successful; STATUS_BUSY if the resource is busy;

Definition at line 490 of file lpuart_driver.c.

17.87.4.15 `status_t LPUART_DRV_SendDataBlocking (uint32_t instance, const uint8_t * txBuff, uint32_t txSize, uint32_t timeout)`

Sends data out through the LPUART module using a blocking method.

Blocking means that the function does not return until the transmission is complete.

Parameters

<i>instance</i>	LPUART instance number
<i>txBuff</i>	source buffer containing 8-bit data chars to send
<i>txSize</i>	the number of bytes to send
<i>timeout</i>	timeout value in milliseconds

Returns

STATUS_SUCCESS if successful; STATUS_TIMEOUT if the timeout was reached; STATUS_BUSY if the resource is busy; STATUS_ERROR if an error occurred

Definition at line 365 of file lpuart_driver.c.

17.87.4.16 `status_t LPUART_DRV_SendDataPolling (uint32_t instance, const uint8_t * txBuff, uint32_t txSize)`

Send out multiple bytes of data using polling method.

Parameters

<i>instance</i>	LPUART instance number.
<i>txBuff</i>	The buffer pointer which saves the data to be sent.
<i>txSize</i>	Size of data to be sent in unit of byte.

Returns

STATUS_SUCCESS if successful; STATUS_BUSY if the resource is busy;

Definition at line 430 of file lpuart_driver.c.

17.87.4.17 status_t LPUART_DRV_SetBaudRate (uint32_t instance, uint32_t desiredBaudRate)

Configures the LPUART baud rate.

This function configures the LPUART baud rate. In some LPUART instances the user must disable the transmitter/receiver before calling this function. Generally, this may be applied to all LPUARTs to ensure safe operation.

Parameters

<i>instance</i>	LPUART instance number.
<i>desiredBaudRate</i>	LPUART desired baud rate.

Returns

STATUS_BUSY if called during an on-going transfer, STATUS_SUCCESS otherwise

Definition at line 931 of file lpuart_driver.c.

17.87.4.18 status_t LPUART_DRV_SetRxBuffer (uint32_t instance, uint8_t * rxBuff, uint32_t rxSize)

Sets the internal driver reference to the rx buffer.

This function can be called from the rx callback to provide the driver with a new buffer, for continuous reception.

Parameters

<i>instance</i>	LPUART instance number
<i>rxBuff</i>	destination buffer containing 8-bit data chars to receive
<i>rxSize</i>	the number of bytes to receive

Returns

STATUS_SUCCESS

Definition at line 1089 of file lpuart_driver.c.

17.87.4.19 status_t LPUART_DRV_SetTxBuffer (uint32_t instance, const uint8_t * txBuff, uint32_t txSize)

Sets the internal driver reference to the tx buffer.

This function can be called from the tx callback to provide the driver with a new buffer, for continuous transmission.

Parameters

<i>instance</i>	LPUART instance number
-----------------	------------------------

<i>txBuff</i>	source buffer containing 8-bit data chars to send
<i>txSize</i>	the number of bytes to send

Returns

STATUS_SUCCESS

Definition at line 1065 of file lpuart_driver.c.

17.88 Local Interconnect Network (LIN)

17.88.1 Detailed Description

The S32 SDK provides both driver and middleware layers for the Local Interconnect Network (LIN) protocol, emulated on top of LPUART serial communication IP.

Modules

- [LIN Driver](#)

This section describes the programming interface of the Peripheral driver for LIN.

- [LIN Stack](#)

This section covers the functionality of the LIN Stack middleware layer in S32 SDK.

17.89 Low Power Inter-Integrated Circuit (LPI2C)

17.89.1 Detailed Description

The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master and/or a slave.

Modules

- [LPI2C Driver](#)

Low Power Inter-Integrated Circuit (LPI2C) Peripheral Driver.

17.90 Low Power Interrupt Timer (LPIT)

17.90.1 Detailed Description

The Low Power Periodic Interrupt Timer (LPIT) is a multi-channel timer module generating independent pre-trigger and trigger outputs. These timer channels can operate individually or can be chained together. The LPIT can operate in low power modes if configured to do so. The pre-trigger and trigger outputs can be used to trigger other modules on the device.

The S32 SDK provides Peripheral Drivers for the Low Power Interrupt Timer (LPIT) module of S32 devices.

Modules

- [LPIT Driver](#)

Low Power Interrupt Timer Peripheral Driver.

17.91 Low Power Serial Peripheral Interface (LPSPi)

17.91.1 Detailed Description

Low Power Serial Peripheral Interface (LPSPi) Peripheral Driver.

The LPSPi driver allows communication on an SPI bus using the LPSPi module in the S32K1xx processors.

Features

- Interrupt based
- Master or slave operation
- Provides blocking and non-blocking transmit and receive functions
- RX and TX hardware buffers (4 words)
- 4 configurable chip select
- Configurable baud rate

How to integrate LPSPi in your application

In order to use the LPSPi driver it must be first initialized in either master or slave mode, using functions [LPSPi_DRV_MasterInit\(\)](#) or [LPSPi_DRV_SlaveInit\(\)](#). Once initialized, it cannot be initialized again for the same LPSPi module instance until it is de-initialized, using [LPSPi_DRV_MasterDeinit\(\)](#) or [LPSPi_DRV_SlaveDeinit\(\)](#). Different LPSPi module instances can function independently of each other.

In each mode (master/slave) are available two types of transfers: blocking and non-blocking. The functions which initiate blocking transfers will configure the time out for transmission. If time expires [LPSPi_MasterTransferBlocking\(\)](#) or [LPSPi_SlaveTransferBlocking\(\)](#) will return error and the transmission will be aborted.

Depending on frame size receive and transmit buffers must be aligned as is presented in the next table:

Bits/frame	less or equal with 8	between 9 and 16	more than 16
Alignment	1 byte	2 bytes	4 bytes

This alignment requirements should be taken into consideration when "transferByteCount" is configured. For a better understanding these are some examples of how to calculate the right value to "transferByteCount":

Bits/frame	number of frames	bytes per frame	transferByteCount
8	10	1	10
10	10	2	20
24	10	4	40
32	10	4	40
40	10	8	80
64	10	8	80

If frame size is bigger than 32 bits MSB/LSB option is applicable for each uint32_t, not for the entire frame. The application should ensure the uint32_t order in buffers, depending on MSB/LSB configuration.

Important Notes

- The driver enables the interrupts for the corresponding LPSPi module, but any interrupt priority setting must be done by the application.
- The watermarks will be set by the application.
- The driver will configure SCK to PCS delay, PCS to SCK delay, delay between transfers with default values. If your application needs other values for this parameters [LPSPi_DRV_MasterSetDelay](#) function can be used.
- The driver cannot be used in the case SPI transfer in slave mode over DMA with invalid address of tx buffer, the driver will never finish the transfer.

- The driver cannot be used with a configuration with bit/frame greater than 32 bits and MSB endianness in either slave or master mode.
- LPSPI2 instance is only available on 64-pin variant of S32K14xW and not available on 48-pin variant. If you need a frame larger than 32 bits with MSB the application must handle the data positioning.

Example code

```
const lpspi_master_config_t Send_MasterConfig0 = {
    .bitsPerSec = 50000U,
    .whichPcs = LPSPI_PCS0,
    .pcsPolarity = LPSPI_ACTIVE_HIGH,
    .isPcsContinuous = false,
    .bitcount = 8U,
    .lpspiSrcClk = 8000000U,
    .clkPhase = LPSPI_CLOCK_PHASE_1ST_EDGE,
    .clkPolarity = LPSPI_SCK_ACTIVE_HIGH,
    .lsbFirst = false,
    .transferType = LPSPI_USING_INTERRUPTS,
};

const lpspi_slave_config_t Receive_SlaveConfig0 = {
    .pcsPolarity = LPSPI_ACTIVE_HIGH,
    .bitcount = 8U,
    .clkPhase = LPSPI_CLOCK_PHASE_1ST_EDGE,
    .whichPcs = LPSPI_PCS0,
    .clkPolarity = LPSPI_SCK_ACTIVE_HIGH,
    .lsbFirst = false,
    .transferType = LPSPI_USING_INTERRUPTS,
};

/* Initialize clock and pins */
LPSPI_DRV_MasterInit(0U, &masterState, &Send_MasterConfig0);
/* Set delay between transfer, PCStoSCK and SCKtoPCS to 10 microseconds. */
LPSPI_DRV_MasterSetDelay(0U, 10U, 10U, 10U);
/* Initialize LPSPI1 (Slave)*/
LPSPI_DRV_SlaveInit(1U, &slaveState, &Receive_SlaveConfig0);
/* Allocate memory */
masterDataSend = (uint8_t*)calloc(100, sizeof(uint8_t));
masterDataReceive = (uint8_t*)calloc(100, sizeof(uint8_t));
slaveDataSend = (uint8_t*)calloc(100, sizeof(uint8_t));
slaveDataReceive = (uint8_t*)calloc(100, sizeof(uint8_t));
bufferSize = 100U;
testStatus[0] = true;
LPSPI_DRV_SlaveTransfer(0U, slaveDataSend,
    slaveDataReceive, bufferSize);
LPSPI_DRV_MasterTransferBlocking(1U, &Send_MasterConfig0, masterDataSend,
    masterDataReceive, bufferSize, TIMEOUT);
```

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\lpspi\lpspi_irq.c
${S32SDK_PATH}\platform\drivers\src\lpspi\lpspi_master_driver.c
${S32SDK_PATH}\platform\drivers\src\lpspi\lpspi_shared_function.c
${S32SDK_PATH}\platform\drivers\src\lpspi\lpspi_slave_driver.c
${S32SDK_PATH}\platform\drivers\src\lpspi\lpspi_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc
${S32SDK_PATH}\platform\drivers\src\lpspi
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager OS Interface \(OSIF\)](#) [Interrupt Manager \(Interrupt\)](#) [Enhanced Direct Memory Access \(eDMA\)](#)

Modules

- [LPSPI Driver](#)

Low Power Serial Peripheral Interface Peripheral Driver.

17.92 Low Power Timer (LPTMR)

17.92.1 Detailed Description

The S32 SDK provides Peripheral Drivers for the Low Power Timer (LPTMR) module of S32 SDK devices.

The LPTMR is a configurable 16-bit counter that can operate in two functional modes:

- Timer mode with selectable prescaler and clock source (periodic or free-running).
- Pulse-Counter mode, with configurable glitch filter, that can count events (internal or external)

Modules

- [LPTMR Driver](#)

Low Power Timer Peripheral Driver.

17.93 Low Power Universal Asynchronous Receiver-Transmitter (LPUART)

17.93.1 Detailed Description

The S32 SDK provides a Peripheral Driver for the Low Power Universal Asynchronous Receiver-Transmitter (LP↔UART) module of S32 SDK devices.

The LPUART module is used for serial communication, supporting LIN master and slave operation. These sections describe the S32 SDK software modules API that can be used for initializing and configuring the module, as well as initiating serial communications using the interrupt-based method.

Modules

- [LPUART Driver](#)

This module covers the functionality of the Low Power Universal Asynchronous Receiver-Transmitter (LPUART) peripheral driver.

17.94 Low level API

17.94.1 Detailed Description

Low level layer consists of functions that call LIN driver API.

This layer contains the implementation of LIN hardware initialization and deinitialization, getting LIN node's current state, sending wakeup signals, enabling and disabling interrupts, sending frame data from a buffer, receiving frame data into a buffer, handling timeout and callbacks from LIN driver.

Data Structures

- struct [lin_word_status_str_t](#)
status of LIN bus Implements : [lin_word_status_str_t_Class](#). [More...](#)
- struct [lin_serial_number_t](#)
Serial number Implements : [lin_serial_number_t_Class](#). [More...](#)
- struct [lin_node_attribute_t](#)
Attributes of LIN node Implements : [lin_node_attribute_t_Class](#). [More...](#)
- struct [lin_associate_frame_t](#)
Informations of associated frame Implements : [lin_associate_frame_t_Class](#). [More...](#)
- struct [lin_frame_t](#)
Frame description structure Implements : [lin_frame_t_Class](#). [More...](#)
- struct [lin_schedule_data_t](#)
LIN schedule structure Implements : [lin_schedule_data_t_Class](#). [More...](#)
- struct [lin_schedule_t](#)
Schedule table description Implements : [lin_schedule_t_Class](#). [More...](#)
- struct [lin_transport_layer_queue_t](#)
Transport layer queue Implements : [lin_transport_layer_queue_t_Class](#). [More...](#)
- struct [lin_tl_descriptor_t](#)
Transport layer description Implements : [lin_tl_descriptor_t_Class](#). [More...](#)
- struct [lin_protocol_user_config_t](#)
Configuration structure Implements : [lin_protocol_user_config_t_Class](#). [More...](#)
- struct [lin_master_data_t](#)
LIN master configuration structure Implements : [lin_master_data_t_Class](#). [More...](#)
- struct [lin_protocol_state_t](#)
LIN protocol status structure Implements : [lin_protocol_state_t_Class](#). [More...](#)

Macros

- `#define SERVICE_ASSIGN_NAD 0xB0U`
- `#define SERVICE_ASSIGN_FRAME_ID 0xB1U`
- `#define SERVICE_READ_BY_IDENTIFY 0xB2U`
- `#define SERVICE_CONDITIONAL_CHANGE_NAD 0xB3U`
- `#define SERVICE_SAVE_CONFIGURATION 0xB6U`
- `#define SERVICE_ASSIGN_FRAME_ID_RANGE 0xB7U`
- `#define SERVICE_READ_DATA_BY_IDENTIFY 0x22U`
- `#define SERVICE_WRITE_DATA_BY_IDENTIFY 0x2EU`
- `#define SERVICE_SESSION_CONTROL 0x10U`
- `#define SERVICE_IO_CONTROL_BY_IDENTIFY 0x2FU`
- `#define SERVICE_FAULT_MEMORY_READ 0x19U`
- `#define SERVICE_FAULT_MEMORY_CLEAR 0x14U`
- `#define PCI_SAVE_CONFIGURATION 0x01U`
- `#define PCI_RES_READ_BY_IDENTIFY 0x06U`

- #define `PCI_RES_SAVE_CONFIGURATION` 0x01U
- #define `PCI_RES_ASSIGN_FRAME_ID_RANGE` 0x01U
- #define `LIN_READ_USR_DEF_MIN` 32U
- #define `LIN_READ_USR_DEF_MAX` 63U
- #define `LD_NEGATIVE_RESPONSE` 0x53U
- #define `LD_POSITIVE_RESPONSE` 0x54U
- #define `LIN_LLD_OK` 0x00U
- #define `LIN_LLD_ERROR` 0xFFU
- #define `LIN_SLAVE` 0
Mode of LIN node (master or slave)
- #define `LIN_MASTER` 1
- #define `LIN_TL_CALLBACK_HANDLER`(iii, tl_event_id, id) `lin_tl_callback_handler`((iii), (tl_event_id), (id))
- #define `CALLBACK_HANDLER`(iii, event_id, id) `lin_pid_resp_callback_handler`((iii), (event_id), (id))
CALLBACK_HANDLER.

Typedefs

- typedef `l_u8 lin_tl_pdu_data_t`[8]
PDU data. Implements : lin_tl_pdu_data_t_Class.
- typedef `l_u8 lin_tl_queue_t`[8]
LIN transport layer queue Implements : lin_tl_queue_t_Class.

Enumerations

- enum `lin_llid_event_id_t` {
`LIN_LLD_PID_OK` = 0x00U, `LIN_LLD_TX_COMPLETED` = 0x01U, `LIN_LLD_RX_COMPLETED` = 0x02U,
`LIN_LLD_PID_ERR` = 0x03U,
`LIN_LLD_FRAME_ERR` = 0x04U, `LIN_LLD_CHECKSUM_ERR` = 0x05U, `LIN_LLD_READBACK_ERR` =
0x06U, `LIN_LLD_NODATA_TIMEOUT` = 0x07U,
`LIN_LLD_BUS_ACTIVITY_TIMEOUT` = 0x08U }
Event id Implements : lin_llid_event_id_t_Class.
- enum `lin_protocol_handle_t` { `LIN_PROTOCOL_21` = 0x00U, `LIN_PROTOCOL_J2602` = 0x01U, `LIN_PROTOCOL_13` = 0x02U, `LIN_PROTOCOL_20` = 0x03U }
List of protocols Implements : lin_protocol_handle_t_Class.
- enum `lin_diagnostic_class_t` { `LIN_DIAGNOSTIC_CLASS_I` = 0x01U, `LIN_DIAGNOSTIC_CLASS_II` =
0x02U, `LIN_DIAGNOSTIC_CLASS_III` = 0x03U }
List of diagnostic classes Implements : lin_diagnostic_class_t_Class.
- enum `lin_frame_type_t` { `LIN_FRM_UNCD` = 0x00U, `LIN_FRM_EVNT` = 0x01U, `LIN_FRM_SPRDC` = 0x10U,
`LIN_FRM_DIAG` = 0x11U }
Types of frame Implements : lin_frame_type_t_Class.
- enum `lin_frame_response_t` { `LIN_RES_PUB` = 0x00U, `LIN_RES_SUB` = 0x01U }
LIN frame response Implements : lin_frame_response_t_Class.
- enum `lin_sch_tbl_type_t` {
`LIN_SCH_TBL_NULL` = 0x00U, `LIN_SCH_TBL_NORM` = 0x01U, `LIN_SCH_TBL_DIAG` = 0x02U, `LIN_SCH_TBL_GO_TO_SLEEP` = 0x03U,
`LIN_SCH_TBL_COLL_RESOLV` = 0x04U }
Types of schedule tables Implements : lin_sch_tbl_type_t_Class.
- enum `l_diagnostic_mode_t` { `DIAG_NONE` = 0x00U, `DIAG_INTERLEAVE_MODE` = 0x01U, `DIAG_ONLY_MODE` = 0x02U }
Diagnostic mode Implements : l_diagnostic_mode_t_Class.
- enum `lin_service_status_t` { `LD_SERVICE_BUSY` = 0x00U, `LD_REQUEST_FINISHED` = 0x01U, `LD_SERVICE_IDLE` = 0x02U, `LD_SERVICE_ERROR` = 0x03U }
Status of the last configuration call for LIN 2.1 Implements : lin_service_status_t_Class.

- enum `lin_last_cfg_result_t` { `LD_SUCCESS` = 0x00U, `LD_NEGATIVE` = 0x01U, `LD_NO_RESPONSE` = 0x02U, `LD_OVERWRITTEN` = 0x03U }
Status of the last configuration call completed Implements : lin_last_cfg_result_t_Class.
- enum `lin_tl_event_id_t` {
`TL_MAKE_RES_DATA` = 0x00U, `TL_SLAVE_GET_ACTION` = 0x01U, `TL_TX_COMPLETED` = 0x02U, `TL_RX_COMPLETED` = 0x03U,
`TL_ERROR` = 0x04U, `TL_TIMEOUT_SERVICE` = 0x05U, `TL_HANDLER_INTERLEAVE_MODE` = 0x06U,
`TL_RECEIVE_MESSAGE` = 0x07U }
Transport layer event IDs Implements : lin_tl_event_id_t_Class.
- enum `lin_tl_callback_return_t` { `TL_ACTION_NONE` = 0x00U, `TL_ACTION_ID_IGNORE` = 0x01U }
Transport layer event IDs Implements : lin_tl_callback_return_t_Class.
- enum `ld_queue_status_t` {
`LD_NO_DATA` = 0x00U, `LD_DATA_AVAILABLE` = 0x01U, `LD_RECEIVE_ERROR` = 0x02U, `LD_QUEUE_FULL` = 0x03U,
`LD_QUEUE_AVAILABLE` = 0x04U, `LD_QUEUE_EMPTY` = 0x05U, `LD_TRANSMIT_ERROR` = 0x06U, `LD_TRANSFER_ERROR` = 0x07U }
Status of queue Implements : ld_queue_status_t_Class.
- enum `lin_message_status_t` {
`LD_NO_MSG` = 0x00U, `LD_IN_PROGRESS` = 0x01U, `LD_COMPLETED` = 0x02U, `LD_FAILED` = 0x03U,
`LD_N_AS_TIMEOUT` = 0x04U, `LD_N_CR_TIMEOUT` = 0x05U, `LD_WRONG_SN` = 0x06U }
Status of LIN message Implements : lin_message_status_t_Class.
- enum `lin_diagnostic_state_t` {
`LD_DIAG_IDLE` = 0x01U, `LD_DIAG_TX_PHY` = 0x02U, `LD_DIAG_TX_FUNCTIONAL` = 0x03U, `LD_DIAG_TX_INTERLEAVED` = 0x04U,
`LD_DIAG_RX_PHY` = 0x05U, `LD_DIAG_RX_FUNCTIONAL` = 0x06U, `LD_DIAG_RX_INTERLEAVED` = 0x07U }
LIN diagnostic state Implements : lin_diagnostic_state_t_Class.
- enum `lin_message_timeout_type_t` { `LD_NO_CHECK_TIMEOUT` = 0x00U, `LD_CHECK_N_AS_TIMEOUT` = 0x01U, `LD_CHECK_N_CR_TIMEOUT` = 0x02U }
Types of message timeout Implements : lin_message_timeout_type_t_Class.
- enum `diag_interleaved_state_t` { `DIAG_NOT_START` = 0x00U, `DIAG_NO_RESPONSE` = 0x01U, `DIAG_RESPONSE` = 0x02U }
State of diagnostic interleaved mode Implements : diag_interleaved_state_t_Class.

Functions

- `lin_tl_callback_return_t lin_tl_callback_handler` (l_ifc_handle iii, `lin_tl_event_id_t` tl_event_id, l_u8 id)
`l_u8 ld_read_by_id_callout` (l_ifc_handle iii, l_u8 id, l_u8 *data)
`static l_u16 lin_calc_max_header_timeout_cnt` (l_u32 baudRate)
Computes maximum header timeout.
- `static l_u16 lin_calc_max_res_timeout_cnt` (l_u32 baudRate, l_u8 size)
Computes the maximum response timeout.
- `l_u8 lin_process_parity` (l_u8 pid, l_u8 typeAction)
Makes or checks parity bits. If action is checking parity, the function returns ID value if parity bits are correct or 0xFF if parity bits are incorrect. If action is making parity bits, then from input value of ID, the function returns PID.
- `void lin_pid_resp_callback_handler` (l_ifc_handle iii, const `lin_lld_event_id_t` event_id, l_u8 id)
Callback handler for low level events.
- `l_bool lin_lld_init` (l_ifc_handle iii)
This function initializes a LIN hardware instance for operation. This function will initialize the run-time state structure to keep track of the on-going transfers, initialize the module to user defined settings and default settings, configure the IRQ state structure and enable the module-level interrupt to the core, and enable the LIN hardware module transmitter and receiver.
- `void lin_lld_deinit` (l_ifc_handle iii)
This function disconnect the node from the cluster and free all hardware used.

- `I_u8 lin_llc_int_enable` (`I_ifc_handle iii`)
Enable the interrupt related to the interface.
- `I_u8 lin_llc_int_disable` (`I_ifc_handle iii`)
Disable the interrupt related to the interface.
- `lin_node_state_t lin_llc_get_state` (`I_ifc_handle iii`)
This function gets current state of an interface.
- `I_u8 lin_llc_tx_header` (`I_ifc_handle iii`, `I_u8 id`)
This function sends frame header for the input PID.
- `I_u8 lin_llc_tx_wake_up` (`I_ifc_handle iii`)
This function send a wakeup signal.
- `I_u8 lin_llc_ignore_response` (`I_ifc_handle iii`)
This function terminates an on-going data transmission/reception.
- `I_u8 lin_llc_set_low_power_mode` (`I_ifc_handle iii`)
Let the low level driver go to low power mode.
- `I_u8 lin_llc_set_response` (`I_ifc_handle iii`, `I_u8 response_length`)
This function sends frame data that is contained in `LIN_llc_response_buffer[iii]`.
- `I_u8 lin_llc_rx_response` (`I_ifc_handle iii`, `I_u8 response_length`)
This function receives frame data into the `LIN_llc_response_buffer[iii]` buffer.
- `void lin_llc_timeout_service` (`I_ifc_handle iii`)
*Callback function for Timer Interrupt Handler In timer IRQ handler, call this function. Used to check if frame timeout has occurred during frame data transmission and reception, to check for `N_As` and `N_Cr` timeout for LIN 2.1 and above. This function also check if there is no LIN bus communication (no headers and no frame data transferring) for Idle timeout (s), then put LIN node to Sleep mode. Users may initialize a timer (for example FTM) with period of Timeout unit (default: 500 micro seconds) to call `lin_llc_timeout_service()`. For an interface `iii`, Idle timeout (s) = `max_idle_timeout_cnt * Timeout unit (us)` frame timeout (us) = `frame_timeout_cnt * Timeout unit (us)` `N_As` timeout (us) = `N_As_timeout * Timeout unit (us)` `N_Cr` timeout (us) = `N_Cr_timeout * Timeout unit (us)`*

Variables

- `const lin_node_attribute_t g_lin_node_attribute_array` [`LIN_NUM_OF_SLAVE_IFCS`]
- `lin_master_data_t g_lin_master_data_array` [`LIN_NUM_OF_MASTER_IFCS`]
- `lin_tl_descriptor_t g_lin_tl_descriptor_array` [`LIN_NUM_OF_IFCS`]
- `const lin_protocol_user_config_t g_lin_protocol_user_cfg_array` [`LIN_NUM_OF_IFCS`]
- `lin_protocol_state_t g_lin_protocol_state_array` [`LIN_NUM_OF_IFCS`]
- `volatile I_u8 g_lin_frame_data_buffer` [`LIN_FRAME_BUF_SIZE`]
- `volatile I_u8 g_lin_flag_handle_tbl` [`LIN_FLAG_BUF_SIZE`]
- `volatile I_bool g_lin_frame_flag_handle_tbl` [`LIN_NUM_OF_FRMS`]
- `const I_u32 g_lin_virtual_ifc` [`LIN_NUM_OF_IFCS`]
- `const I_ifc_handle g_lin_hardware_ifc` [`HARDWARE_INSTANCE_COUNT`]
- `const lin_timer_get_time_interval_t timerGetTimeIntervalCallbackArr` [`LIN_NUM_OF_IFCS`]
- `volatile I_u8 g_buffer_backup_data` [8]
- `volatile I_u8 g_lin_frame_updating_flag_tbl` [`LIN_NUM_OF_FRMS`]

17.94.2 Data Structure Documentation

17.94.2.1 struct `lin_word_status_str_t`

status of LIN bus Implements : `lin_word_status_str_t` Class

Definition at line 148 of file `lin.h`.

Data Fields

- unsigned int [error_in_res](#): 1
- unsigned int [successful_transfer](#): 1
- unsigned int [overrun](#): 1
- unsigned int [go_to_sleep_flg](#): 1
- unsigned int [bus_activity](#): 1
- unsigned int [event_trigger_collision_flg](#): 1
- unsigned int [save_config_flg](#): 1
- unsigned int [reserved](#): 1
- unsigned int [last_pid](#): 8

Field Documentation

17.94.2.1.1 unsigned int bus_activity

Bus activity

Definition at line 154 of file lin.h.

17.94.2.1.2 unsigned int error_in_res

Error in response

Definition at line 150 of file lin.h.

17.94.2.1.3 unsigned int event_trigger_collision_flg

Event trigger collision

Definition at line 155 of file lin.h.

17.94.2.1.4 unsigned int go_to_sleep_flg

Goto sleep

Definition at line 153 of file lin.h.

17.94.2.1.5 unsigned int last_pid

Last PID

Definition at line 158 of file lin.h.

17.94.2.1.6 unsigned int overrun

Overrun

Definition at line 152 of file lin.h.

17.94.2.1.7 unsigned int reserved

Dummy

Definition at line 157 of file lin.h.

17.94.2.1.8 unsigned int save_config_flg

Save configuration

Definition at line 156 of file lin.h.

17.94.2.1.9 unsigned int successful_transfer

Successful transfer

Definition at line 151 of file lin.h.

17.94.2.2 struct lin_serial_number_t

Serial number Implements : lin_serial_number_t_Class.

Definition at line 175 of file lin.h.

Data Fields

- [l_u8 serial_0](#)
- [l_u8 serial_1](#)
- [l_u8 serial_2](#)
- [l_u8 serial_3](#)

Field Documentation

17.94.2.2.1 l_u8 serial_0

Serial 0

Definition at line 177 of file lin.h.

17.94.2.2.2 l_u8 serial_1

Serial 1

Definition at line 178 of file lin.h.

17.94.2.2.3 l_u8 serial_2

Serial 2

Definition at line 179 of file lin.h.

17.94.2.2.4 l_u8 serial_3

Serial 3

Definition at line 180 of file lin.h.

17.94.2.3 struct lin_node_attribute_t

Attributes of LIN node Implements : lin_node_attribute_t_Class.

Definition at line 187 of file lin.h.

Data Fields

- [l_u8 * configured_NAD_ptr](#)
- [l_u8 initial_NAD](#)
- [lin_product_id_t product_id](#)
- [lin_serial_number_t serial_number](#)
- [l_u8 * resp_err_frm_id_ptr](#)
- [l_u8 num_frame_have_esignal](#)
- [l_signal_handle response_error](#)
- [l_u16 * response_error_byte_offset_ptr](#)
- [l_u8 * response_error_bit_offset_ptr](#)
- [l_u8 num_of_fault_state_signal](#)
- [const l_signal_handle * fault_state_signal_ptr](#)
- [l_u16 P2_min](#)
- [l_u16 ST_min](#)
- [l_u16 N_As_timeout](#)

- `I_u16 N_Cr_timeout`
- `I_u8 number_support_sid`
- `const I_u8 * service_supported_ptr`
- `I_u8 * service_flags_ptr`

Field Documentation

17.94.2.3.1 `I_u8* configured_NAD_ptr`

NAD value used in configuration command

Definition at line 189 of file lin.h.

17.94.2.3.2 `const I_signal_handle* fault_state_signal_ptr`

List of fault state signal

Definition at line 199 of file lin.h.

17.94.2.3.3 `I_u8 initial_NAD`

Initial NAD

Definition at line 190 of file lin.h.

17.94.2.3.4 `I_u16 N_As_timeout`

`N_As_timeout`

Definition at line 202 of file lin.h.

17.94.2.3.5 `I_u16 N_Cr_timeout`

`N_Cr_timeout`

Definition at line 203 of file lin.h.

17.94.2.3.6 `I_u8 num_frame_have_esignal`

Number of frame contain error signal

Definition at line 194 of file lin.h.

17.94.2.3.7 `I_u8 num_of_fault_state_signal`

Number of Fault state signal

Definition at line 198 of file lin.h.

17.94.2.3.8 `I_u8 number_support_sid`

Number of supported diagnostic services

Definition at line 204 of file lin.h.

17.94.2.3.9 `I_u16 P2_min`

`P2_min`

Definition at line 200 of file lin.h.

17.94.2.3.10 `lin_product_id_t product_id`

Product ID

Definition at line 191 of file lin.h.

17.94.2.3.11 I_u8* resp_err_frm_id_ptr

List index of frame contain response error signal

Definition at line 193 of file lin.h.

17.94.2.3.12 I_signal_handle response_error

Signal used to update response error

Definition at line 195 of file lin.h.

17.94.2.3.13 I_u8* response_error_bit_offset_ptr

Bit offset of response error signal

Definition at line 197 of file lin.h.

17.94.2.3.14 I_u16* response_error_byte_offset_ptr

Byte offset of response error signal

Definition at line 196 of file lin.h.

17.94.2.3.15 lin_serial_number_t serial_number

Serial number

Definition at line 192 of file lin.h.

17.94.2.3.16 I_u8* service_flags_ptr

List of associated flags with supported diagnostic services

Definition at line 206 of file lin.h.

17.94.2.3.17 const I_u8* service_supported_ptr

List of supported diagnostic service

Definition at line 205 of file lin.h.

17.94.2.3.18 I_u16 ST_min

ST min

Definition at line 201 of file lin.h.

17.94.2.4 struct lin_associate_frame_t

Informations of associated frame Implements : lin_associate_frame_t_Class.

Definition at line 238 of file lin.h.

Data Fields

- I_u8 [num_of_associated_uncond_frames](#)
- const I_frame_handle * [associated_uncond_frame_ptr](#)
- I_u8 [coll_resolv_schd](#)

Field Documentation**17.94.2.4.1 const I_frame_handle* associated_uncond_frame_ptr**

Associated unconditional frame ID

Definition at line 241 of file lin.h.

17.94.2.4.2 `_u8 coll_resolv_schd`

Collision resolver index in the schedule table, used in event trigger frame case MASTER

Definition at line 242 of file lin.h.

17.94.2.4.3 `_u8 num_of_associated_uncond_frames`

Number of associated unconditional frame ID

Definition at line 240 of file lin.h.

17.94.2.5 `struct lin_frame_t`

Frame description structure Implements : `lin_frame_t_Class`.

Definition at line 249 of file lin.h.

Data Fields

- [lin_frame_type_t frm_type](#)
- [_u8 frm_len](#)
- [lin_frame_response_t frm_response](#)
- [_u16 frm_offset](#)
- [_u16 flag_offset](#)
- [_u8 flag_size](#)
- const [lin_associate_frame_t](#) * `frame_data_ptr`

Field Documentation

17.94.2.5.1 `_u16 flag_offset`

Flag byte offset in flag buffer

Definition at line 255 of file lin.h.

17.94.2.5.2 `_u8 flag_size`

Flag size in flag buffer

Definition at line 256 of file lin.h.

17.94.2.5.3 `const lin_associate_frame_t* frame_data_ptr`

List of Signal to which the frame is associated and its offset

Definition at line 257 of file lin.h.

17.94.2.5.4 `_u8 frm_len`

Length of the frame

Definition at line 252 of file lin.h.

17.94.2.5.5 `_u16 frm_offset`

Frame byte offset in frame buffer

Definition at line 254 of file lin.h.

17.94.2.5.6 `lin_frame_response_t frm_response`

Action response when received PID

Definition at line 253 of file lin.h.

17.94.2.5.7 `lin_frame_type_t frm_type`

Frame information (unconditional or event triggered..)

Definition at line 251 of file lin.h.

17.94.2.6 `struct lin_schedule_data_t`

LIN schedule structure Implements : `lin_schedule_data_t_Class`.

Definition at line 286 of file lin.h.

Data Fields

- `I_frame_handle` [frm_id](#)
- `I_u8` [delay_integer](#)
- [lin_tl_queue_t](#) [tl_queue_data](#)

Field Documentation

17.94.2.6.1 `I_u8 delay_integer`

Actual slot time in INTEGER for one frame

Definition at line 289 of file lin.h.

17.94.2.6.2 `I_frame_handle frm_id`

Frame ID, in case of unconditional or event triggered frame. For sporadic frame the value will be 0 (zero)

Definition at line 288 of file lin.h.

17.94.2.6.3 `lin_tl_queue_t tl_queue_data`

Data used in case of diagnostic or configuration frame

Definition at line 290 of file lin.h.

17.94.2.7 `struct lin_schedule_t`

Schedule table description Implements : `lin_schedule_t_Class`.

Definition at line 297 of file lin.h.

Data Fields

- `I_u8` [num_slots](#)
- [lin_sch_tbl_type_t](#) [sch_tbl_type](#)
- `const` [lin_schedule_data_t](#) * [ptr_sch_data_ptr](#)

Field Documentation

17.94.2.7.1 `I_u8 num_slots`

Number of frame slots in the schedule table

Definition at line 299 of file lin.h.

17.94.2.7.2 `const lin_schedule_data_t* ptr_sch_data_ptr`

Address of the schedule table

Definition at line 301 of file lin.h.

17.94.2.7.3 `lin_sch_tbl_type_t` `sch_tbl_type`

Schedule table type

Definition at line 300 of file `lin.h`.

17.94.2.8 `struct lin_transport_layer_queue_t`

Transport layer queue Implements : `lin_transport_layer_queue_t_Class`.

Definition at line 435 of file `lin.h`.

Data Fields

- `I_u16 queue_header`
- `I_u16 queue_tail`
- `Id_queue_status_t queue_status`
- `I_u16 queue_current_size`
- `I_u16 queue_max_size`
- `lin_tl_pdu_data_t * tl_pdu_ptr`

Field Documentation

17.94.2.8.1 `I_u16 queue_current_size`

Current size

Definition at line 440 of file `lin.h`.

17.94.2.8.2 `I_u16 queue_header`

The first element of queue

Definition at line 437 of file `lin.h`.

17.94.2.8.3 `I_u16 queue_max_size`

Maximum size

Definition at line 441 of file `lin.h`.

17.94.2.8.4 `Id_queue_status_t queue_status`

Status of queue

Definition at line 439 of file `lin.h`.

17.94.2.8.5 `I_u16 queue_tail`

The last element of queue

Definition at line 438 of file `lin.h`.

17.94.2.8.6 `lin_tl_pdu_data_t* tl_pdu_ptr`

PDU data

Definition at line 442 of file `lin.h`.

17.94.2.9 `struct lin_tl_descriptor_t`

Transport layer description Implements : `lin_tl_descriptor_t_Class`.

Definition at line 461 of file `lin.h`.

Data Fields

- [lin_transport_layer_queue_t tl_tx_queue](#)
- [lin_transport_layer_queue_t tl_rx_queue](#)
- [lin_message_status_t rx_msg_status](#)
- [l_u16 rx_msg_size](#)
- [lin_message_status_t tx_msg_status](#)
- [l_u16 tx_msg_size](#)
- [lin_last_cfg_result_t last_cfg_result](#)
- [l_u8 last_RSID](#)
- [l_u8 ld_error_code](#)
- [lin_message_timeout_type_t check_timeout_type](#)
- [l_u16 check_timeout](#)
- [lin_product_id_t * product_id_ptr](#)
- [l_u8 num_of_pdu](#)
- [l_u8 frame_counter](#)
- [lin_diagnostic_state_t diag_state](#)
- [diag_interleaved_state_t diag_interleave_state](#)
- [l_u16 interleave_timeout_counter](#)
- [l_u8 slave_resp_cnt](#)
- [lin_service_status_t service_status](#)
- [bool ld_return_data](#)
- [bool FF_pdu_received](#)
- [l_u8 * receive_message_ptr](#)
- [l_u8 * receive_NAD_ptr](#)
- [l_u16 * receive_message_length_ptr](#)

Field Documentation

17.94.2.9.1 [l_u16 check_timeout](#)

Timeout counter for N_As and N_Cr timeout

Definition at line 481 of file lin.h.

17.94.2.9.2 [lin_message_timeout_type_t check_timeout_type](#)

Timeout type

Definition at line 480 of file lin.h.

17.94.2.9.3 [diag_interleaved_state_t diag_interleave_state](#)

state of diagnostic interleaved mode

Definition at line 486 of file lin.h.

17.94.2.9.4 [lin_diagnostic_state_t diag_state](#)

Diagnostic state

Definition at line 485 of file lin.h.

17.94.2.9.5 [bool FF_pdu_received](#)

Status of FF pdu

Definition at line 492 of file lin.h.

17.94.2.9.6 I_u8 frame_counter

Frame counter in received message

Definition at line 484 of file lin.h.

17.94.2.9.7 I_u16 interleave_timeout_counter

Interleaved timeout counter

Definition at line 487 of file lin.h.

17.94.2.9.8 lin_last_cfg_result_t last_cfg_result

Status of the last configuration service

Definition at line 476 of file lin.h.

17.94.2.9.9 I_u8 last_RSID

RSID of the last node configuration service

Definition at line 477 of file lin.h.

17.94.2.9.10 I_u8 ld_error_code

Error code in case of positive response

Definition at line 478 of file lin.h.

17.94.2.9.11 bool ld_return_data

Decide return data of diagnostic frame to pointer of ld_receive_message function

Definition at line 491 of file lin.h.

17.94.2.9.12 I_u8 num_of_pdu

Number of received pdu

Definition at line 483 of file lin.h.

17.94.2.9.13 lin_product_id_t* product_id_ptr

To store address of RAM area contain response

Definition at line 482 of file lin.h.

17.94.2.9.14 I_u16* receive_message_length_ptr

Pointer to receive_message_length of user

Definition at line 497 of file lin.h.

17.94.2.9.15 I_u8* receive_message_ptr

Pointer to receive_message array of user

Definition at line 495 of file lin.h.

17.94.2.9.16 I_u8* receive_NAD_ptr

Pointer to receive_NAD of user

Definition at line 496 of file lin.h.

17.94.2.9.17 `l_u16 rx_msg_size`

Size of message in queue

Definition at line 470 of file lin.h.

17.94.2.9.18 `lin_message_status_t rx_msg_status`

Cooked rx status

Definition at line 469 of file lin.h.

17.94.2.9.19 `lin_service_status_t service_status`

Status of the last configuration service

Definition at line 489 of file lin.h.

17.94.2.9.20 `l_u8 slave_resp_cnt`

Slave Response data counter

Definition at line 488 of file lin.h.

17.94.2.9.21 `lin_transport_layer_queue_t tl_rx_queue`

Pointer to receive queue on TL

Definition at line 465 of file lin.h.

17.94.2.9.22 `lin_transport_layer_queue_t tl_tx_queue`

Pointer to transmit queue on TL

Definition at line 464 of file lin.h.

17.94.2.9.23 `l_u16 tx_msg_size`

Size of message in queue

Definition at line 474 of file lin.h.

17.94.2.9.24 `lin_message_status_t tx_msg_status`

Cooked tx status

Definition at line 473 of file lin.h.

17.94.2.10 `struct lin_protocol_user_config_t`

Configuration structure Implements : `lin_protocol_user_config_t_Class`.

Definition at line 507 of file lin.h.

Data Fields

- [lin_protocol_handle_t protocol_version](#)
- [lin_protocol_handle_t language_version](#)
- [lin_diagnostic_class_t diagnostic_class](#)
- [bool function](#)
- [l_u8 number_of_configurable_frames](#)
- [l_u8 frame_start](#)
- [const lin_frame_t * frame_tbl_ptr](#)
- [const l_u16 * list_identifiers_ROM_ptr](#)
- [l_u8 * list_identifiers_RAM_ptr](#)

- `I_u16 max_idle_timeout_cnt`
- `I_u8 num_of_schedules`
- `I_u8 schedule_start`
- `const lin_schedule_t * schedule_tbl`
- `I_ifc_slave_handle slave_ifc_handle`
- `I_ifc_master_handle master_ifc_handle`
- `lin_user_config_t * lin_user_config_ptr`
- `lin_tl_pdu_data_t * tl_tx_queue_data_ptr`
- `lin_tl_pdu_data_t * tl_rx_queue_data_ptr`
- `I_u16 max_message_length`

Field Documentation

17.94.2.10.1 `lin_diagnostic_class_t` `diagnostic_class`

Diagnostic class

Definition at line 511 of file `lin.h`.

17.94.2.10.2 `I_u8` `frame_start`

Start index of frame list

Definition at line 515 of file `lin.h`.

17.94.2.10.3 `const lin_frame_t*` `frame_tbl_ptr`

Frame list except diagnostic frames

Definition at line 516 of file `lin.h`.

17.94.2.10.4 `bool` `function`

Function `LIN_MASTER` or `LIN_SLAVE_`)

Definition at line 512 of file `lin.h`.

17.94.2.10.5 `lin_protocol_handle_t` `language_version`

Language version

Definition at line 510 of file `lin.h`.

17.94.2.10.6 `lin_user_config_t*` `lin_user_config_ptr`

Pointer to LIN driver user configuration structure

Definition at line 526 of file `lin.h`.

17.94.2.10.7 `I_u8*` `list_identifiers_RAM_ptr`

Configuration in RAM

Definition at line 519 of file `lin.h`.

17.94.2.10.8 `const I_u16*` `list_identifiers_ROM_ptr`

Configuration in ROM

Definition at line 518 of file `lin.h`.

17.94.2.10.9 `I_ifc_master_handle` `master_ifc_handle`

Interface handler of master node

Definition at line 525 of file lin.h.

17.94.2.10.10 `I_u16 max_idle_timeout_cnt`

Max Idle timeout counter

Definition at line 520 of file lin.h.

17.94.2.10.11 `I_u16 max_message_length`

Max message length

Definition at line 530 of file lin.h.

17.94.2.10.12 `I_u8 num_of_schedules`

Number of schedule table

Definition at line 521 of file lin.h.

17.94.2.10.13 `I_u8 number_of_configurable_frames`

Number of frame except diagnostic frames

Definition at line 514 of file lin.h.

17.94.2.10.14 `lin_protocol_handle_t protocol_version`

Protocol version

Definition at line 509 of file lin.h.

17.94.2.10.15 `I_u8 schedule_start`

Start index of schedule table list

Definition at line 522 of file lin.h.

17.94.2.10.16 `const lin_schedule_t* schedule_tbl`

Schedule table list

Definition at line 523 of file lin.h.

17.94.2.10.17 `I_ifc_slave_handle slave_ifc_handle`

Interface handler of slave node

Definition at line 524 of file lin.h.

17.94.2.10.18 `lin_tl_pdu_data_t* tl_rx_queue_data_ptr`

Rx queue data

Definition at line 529 of file lin.h.

17.94.2.10.19 `lin_tl_pdu_data_t* tl_tx_queue_data_ptr`

Tx queue data

Definition at line 528 of file lin.h.

17.94.2.11 `struct lin_master_data_t`

LIN master configuration structure Implements : `lin_master_data_t_Class`.

Definition at line 538 of file lin.h.

Data Fields

- `I_u8 active_schedule_id`
- `I_u8 previous_schedule_id`
- `I_u8 * schedule_start_entry_ptr`
- `I_bool event_trigger_collision_flg`
- `I_u8 master_data_buffer [8]`
- `I_u16 frm_offset`
- `I_u8 frm_size`
- `I_u16 flag_offset`
- `I_u8 flag_size`
- `I_bool send_slave_res_flg`
- `I_bool send_functional_request_flg`

Field Documentation

17.94.2.11.1 `I_u8 active_schedule_id`

Active schedule table id

Definition at line 540 of file lin.h.

17.94.2.11.2 `I_bool event_trigger_collision_flg`

Flag trigger collision event

Definition at line 543 of file lin.h.

17.94.2.11.3 `I_u16 flag_offset`

Flag offset

Definition at line 547 of file lin.h.

17.94.2.11.4 `I_u8 flag_size`

Flag size

Definition at line 548 of file lin.h.

17.94.2.11.5 `I_u16 frm_offset`

Frame offset

Definition at line 545 of file lin.h.

17.94.2.11.6 `I_u8 frm_size`

Size of frame

Definition at line 546 of file lin.h.

17.94.2.11.7 `I_u8 master_data_buffer[8]`

Master data buffer

Definition at line 544 of file lin.h.

17.94.2.11.8 `I_u8 previous_schedule_id`

Previous schedule table id

Definition at line 541 of file lin.h.

17.94.2.11.9 `I_u8* schedule_start_entry_ptr`

Start entry of each schedule table

Definition at line 542 of file lin.h.

17.94.2.11.10 `I_bool send_functional_request_flg`

Flag send Functional Request

Definition at line 550 of file lin.h.

17.94.2.11.11 `I_bool send_slave_res_flg`

Flag to send Slave Response Schedule

Definition at line 549 of file lin.h.

17.94.2.12 `struct lin_protocol_state_t`

LIN protocol status structure Implements : `lin_protocol_state_t_Class`.

Definition at line 557 of file lin.h.

Data Fields

- `I_u16 baud_rate`
- `I_u8 * response_buffer_ptr`
- `I_u8 response_length`
- `I_u8 successful_transfer`
- `I_u8 error_in_response`
- `I_bool go_to_sleep_flg`
- `I_u8 current_id`
- `I_u8 last_pid`
- `I_u8 num_of_processed_frame`
- `I_u8 overrun_flg`
- `lin_word_status_str_t word_status`
- `I_u8 next_transmit_tick`
- `I_bool save_config_flg`
- `I_diagnostic_mode_t diagnostic_mode`
- `I_u16 frame_timeout_cnt`
- `I_u16 idle_timeout_cnt`
- `I_bool transmit_error_resp_sig_flg`

Field Documentation**17.94.2.12.1 `I_u16 baud_rate`**

Adjusted baud rate

Definition at line 560 of file lin.h.

17.94.2.12.2 `I_u8 current_id`

Current PID

Definition at line 566 of file lin.h.

17.94.2.12.3 `I_diagnostic_mode_t diagnostic_mode`

Diagnostic mode

Definition at line 573 of file lin.h.

17.94.2.12.4 I_u8 error_in_response

Error response

Definition at line 564 of file lin.h.

17.94.2.12.5 I_u16 frame_timeout_cnt

Frame timeout counter for monitoring if timeout occurs during data transferring

Definition at line 574 of file lin.h.

17.94.2.12.6 I_bool go_to_sleep_flg

Go to sleep flag

Definition at line 565 of file lin.h.

17.94.2.12.7 I_u16 idle_timeout_cnt

Idle timeout counter

Definition at line 575 of file lin.h.

17.94.2.12.8 I_u8 last_pid

Last PID

Definition at line 567 of file lin.h.

17.94.2.12.9 I_u8 next_transmit_tick

Used to count the next transmit tick

Definition at line 571 of file lin.h.

17.94.2.12.10 I_u8 num_of_processed_frame

Number of processed frames

Definition at line 568 of file lin.h.

17.94.2.12.11 I_u8 overrun_flg

overrun flag

Definition at line 569 of file lin.h.

17.94.2.12.12 I_u8* response_buffer_ptr

Response buffer

Definition at line 561 of file lin.h.

17.94.2.12.13 I_u8 response_length

Response length

Definition at line 562 of file lin.h.

17.94.2.12.14 I_bool save_config_flg

Set when save configuration request has been received

Definition at line 572 of file lin.h.

17.94.2.12.15 `I_u8 successful_transfer`

Transfer flag

Definition at line 563 of file lin.h.

17.94.2.12.16 `I_bool transmit_error_resp_sig_flg`

Flag indicates that the error response signal is going to be sent

Definition at line 576 of file lin.h.

17.94.2.12.17 `lin_word_status_str_t word_status`

Word status

Definition at line 570 of file lin.h.

17.94.3 Macro Definition Documentation

17.94.3.1 `#define CALLBACK_HANDLER(iii, event_id, id) lin_pid_resp_callback_handler((iii), (event_id), (id))`

`CALLBACK_HANDLER`.

Note

call [lin_pid_resp_callback_handler\(\)](#) function in MASTER mode

Definition at line 684 of file lin.h.

17.94.3.2 `#define LD_NEGATIVE_RESPONSE 0x53U`

Negative response

Definition at line 84 of file lin.h.

17.94.3.3 `#define LD_POSITIVE_RESPONSE 0x54U`

Positive response

Definition at line 85 of file lin.h.

17.94.3.4 `#define LIN_LLD_ERROR 0xFFU`

Return value is ERROR

Definition at line 89 of file lin.h.

17.94.3.5 `#define LIN_LLD_OK 0x00U`

Return value is OK

Definition at line 88 of file lin.h.

17.94.3.6 `#define LIN_MASTER 1`

Master node

Definition at line 166 of file lin.h.

17.94.3.7 `#define LIN_READ_USR_DEF_MAX 63U`

Max user defined

Definition at line 81 of file lin.h.

17.94.3.8 #define LIN_READ_USR_DEF_MIN 32U

Min user defined

Definition at line 80 of file lin.h.

17.94.3.9 #define LIN_SLAVE 0

Mode of LIN node (master or slave)

Slave node

Definition at line 165 of file lin.h.

17.94.3.10 #define LIN_TL_CALLBACK_HANDLER(*iii*, *tl_event_id*, *id*) lin_tl_callback_handler((iii), (tl_event_id), (id))

Definition at line 372 of file lin.h.

17.94.3.11 #define PCI_RES_ASSIGN_FRAME_ID_RANGE 0x01U

PCI response value assign frame id range

Definition at line 77 of file lin.h.

17.94.3.12 #define PCI_RES_READ_BY_IDENTIFY 0x06U

PCI response value read by identify

Definition at line 75 of file lin.h.

17.94.3.13 #define PCI_RES_SAVE_CONFIGURATION 0x01U

PCI response value save configuration

Definition at line 76 of file lin.h.

17.94.3.14 #define PCI_SAVE_CONFIGURATION 0x01U

PCI value save configuration

Definition at line 72 of file lin.h.

17.94.3.15 #define SERVICE_FAULT_MEMORY_CLEAR 0x14U

Service fault memory clear

Definition at line 69 of file lin.h.

17.94.3.16 #define SERVICE_ASSIGN_FRAME_ID 0xB1U

Assign frame id service

Definition at line 58 of file lin.h.

17.94.3.17 #define SERVICE_ASSIGN_FRAME_ID_RANGE 0xB7U

Assign frame id range service

Definition at line 62 of file lin.h.

17.94.3.18 #define SERVICE_ASSIGN_NAD 0xB0U

Assign NAD service

Definition at line 57 of file lin.h.

17.94.3.19 #define SERVICE_CONDITIONAL_CHANGE_NAD 0xB3U

Conditional change NAD service

Definition at line 60 of file lin.h.

17.94.3.20 #define SERVICE_FAULT_MEMORY_READ 0x19U

Service fault memory read

Definition at line 68 of file lin.h.

17.94.3.21 #define SERVICE_IO_CONTROL_BY_IDENTIFY 0x2FU

Service I/O control

Definition at line 67 of file lin.h.

17.94.3.22 #define SERVICE_READ_BY_IDENTIFY 0xB2U

Read by identify service

Definition at line 59 of file lin.h.

17.94.3.23 #define SERVICE_READ_DATA_BY_IDENTIFY 0x22U

Service read data by identifier

Definition at line 64 of file lin.h.

17.94.3.24 #define SERVICE_SAVE_CONFIGURATION 0xB6U

Save configuration service

Definition at line 61 of file lin.h.

17.94.3.25 #define SERVICE_SESSION_CONTROL 0x10U

Service session control

Definition at line 66 of file lin.h.

17.94.3.26 #define SERVICE_WRITE_DATA_BY_IDENTIFY 0x2EU

Service write data by identifier

Definition at line 65 of file lin.h.

17.94.4 Typedef Documentation**17.94.4.1 typedef I_u8 lin_tl_pdu_data_t[8]**

PDU data. Implements : lin_tl_pdu_data_t_Class.

Definition at line 95 of file lin.h.

17.94.4.2 typedef I_u8 lin_tl_queue_t[8]

LIN transport layer queue Implements : lin_tl_queue_t_Class.

Definition at line 267 of file lin.h.

17.94.5 Enumeration Type Documentation

17.94.5.1 enum `diag_interleaved_state_t`

State of diagnostic interleaved mode Implements : `diag_interleaved_state_t_Class`.

Enumerator

DIAG_NOT_START Not into slave response schedule with interleaved mode

DIAG_NO_RESPONSE Master send 0x3D but slave does not response

DIAG_RESPONSE Response receive

Definition at line 450 of file `lin.h`.

17.94.5.2 enum `l_diagnostic_mode_t`

Diagnostic mode Implements : `l_diagnostic_mode_t_Class`.

Enumerator

DIAG_NONE None

DIAG_INTERLEAVE_MODE Interleave mode

DIAG_ONLY_MODE Diagnostic only mode

Definition at line 311 of file `lin.h`.

17.94.5.3 enum `ld_queue_status_t`

Status of queue Implements : `ld_queue_status_t_Class`.

Enumerator

LD_NO_DATA Rx Queue is empty, has no data

LD_DATA_AVAILABLE Data in queue is available

LD_RECEIVE_ERROR Receive data is error for LIN21 and above

LD_QUEUE_FULL The queue is full

LD_QUEUE_AVAILABLE Queue is available for insert data for LIN21 and above

LD_QUEUE_EMPTY Tx Queue is empty

LD_TRANSMIT_ERROR Error while transmitting for LIN21 and above

LD_TRANSFER_ERROR Error while transmitting/receiving for LIN20 and J2602

Definition at line 378 of file `lin.h`.

17.94.5.4 enum `lin_diagnostic_class_t`

List of diagnostic classes Implements : `lin_diagnostic_class_t_Class`.

Enumerator

LIN_DIAGNOSTIC_CLASS_I LIN Diagnostic Class 1

LIN_DIAGNOSTIC_CLASS_II LIN Diagnostic Class 2

LIN_DIAGNOSTIC_CLASS_III LIN Diagnostic Class 3

Definition at line 137 of file `lin.h`.

17.94.5.5 enum `lin_diagnostic_state_t`

LIN diagnostic state Implements : `lin_diagnostic_state_t_Class`.

Enumerator

`LD_DIAG_IDLE` IDLE
`LD_DIAG_TX_PHY` Diagnostic transmit physical
`LD_DIAG_TX_FUNCTIONAL` Diagnostic transmit active
`LD_DIAG_TX_INTERLEAVED` Diagnostic transmit in interleave mode
`LD_DIAG_RX_PHY` Diagnostic receive in physical
`LD_DIAG_RX_FUNCTIONAL` Diagnostic receive functional request
`LD_DIAG_RX_INTERLEAVED` Diagnostic receive in interleave mode

Definition at line 409 of file `lin.h`.

17.94.5.6 enum `lin_frame_response_t`

LIN frame response Implements : `lin_frame_response_t_Class`.

Enumerator

`LIN_RES_PUB` Publisher response
`LIN_RES_SUB` Subscriber response

Definition at line 228 of file `lin.h`.

17.94.5.7 enum `lin_frame_type_t`

Types of frame Implements : `lin_frame_type_t_Class`.

Enumerator

`LIN_FRM_UNCD` Unconditional frame
`LIN_FRM_EVNT` Event triggered frame
`LIN_FRM_SPRDC` Sporadic frame
`LIN_FRM_DIAG` Diagnostic frame

Definition at line 216 of file `lin.h`.

17.94.5.8 enum `lin_last_cfg_result_t`

Status of the last configuration call completed Implements : `lin_last_cfg_result_t_Class`.

Enumerator

`LD_SUCCESS` The service was successfully carried out
`LD_NEGATIVE` The service failed, more information can be found by parsing `error_code`
`LD_NO_RESPONSE` No response was received on the request
`LD_OVERWRITTEN` The slave response frame has been overwritten by another operation

Definition at line 334 of file `lin.h`.

17.94.5.9 enum lin_llc_event_id_t

Event id Implements : lin_llc_event_id_t_Class.

Enumerator

LIN_LLC_PID_OK LIN_LLC_PID_OK
LIN_LLC_TX_COMPLETED LIN_LLC_TX_COMPLETED
LIN_LLC_RX_COMPLETED LIN_LLC_RX_COMPLETED
LIN_LLC_PID_ERR LIN_LLC_PID_ERR
LIN_LLC_FRAME_ERR LIN_LLC_FRAME_ERR
LIN_LLC_CHECKSUM_ERR LIN_LLC_CHECKSUM_ERR
LIN_LLC_READBACK_ERR LIN_LLC_READBACK_ERR
LIN_LLC_NODATA_TIMEOUT No data timeout or received part of data but not completed
LIN_LLC_BUS_ACTIVITY_TIMEOUT LIN_LLC_BUS_ACTIVITY_TIMEOUT

Definition at line 105 of file lin.h.

17.94.5.10 enum lin_message_status_t

Status of LIN message Implements : lin_message_status_t_Class.

Enumerator

LD_NO_MSG No message
LD_IN_PROGRESS In progress
LD_COMPLETED Completed
LD_FAILED Failed
LD_N_AS_TIMEOUT N_As timeout
LD_N_CR_TIMEOUT N_Cr timeout
LD_WRONG_SN Wrong sequence number

Definition at line 394 of file lin.h.

17.94.5.11 enum lin_message_timeout_type_t

Types of message timeout Implements : lin_message_timeout_type_t_Class.

Enumerator

LD_NO_CHECK_TIMEOUT No check timeout
LD_CHECK_N_AS_TIMEOUT check N_As timeout
LD_CHECK_N_CR_TIMEOUT check N_Cr timeout

Definition at line 424 of file lin.h.

17.94.5.12 enum lin_protocol_handle_t

List of protocols Implements : lin_protocol_handle_t_Class.

Enumerator

LIN_PROTOCOL_21 LIN protocol version 2.1, 2.2
LIN_PROTOCOL_J2602 J2602 protocol
LIN_PROTOCOL_13 LIN protocol version 1.3
LIN_PROTOCOL_20 LIN protocol version 2.0

Definition at line 125 of file lin.h.

17.94.5.13 enum lin_sch_tbl_type_t

Types of schedule tables Implements : lin_sch_tbl_type_t_Class.

Enumerator

LIN_SCH_TBL_NULL Run nothing
LIN_SCH_TBL_NORM Normal schedule table
LIN_SCH_TBL_DIAG Diagnostic schedule table
LIN_SCH_TBL_GO_TO_SLEEP Goto sleep schedule table
LIN_SCH_TBL_COLL_RESOLV Collision resolving schedule table

Definition at line 273 of file lin.h.

17.94.5.14 enum lin_service_status_t

Status of the last configuration call for LIN 2.1 Implements : lin_service_status_t_Class.

Enumerator

LD_SERVICE_BUSY Service is ongoing
LD_REQUEST_FINISHED The configuration request has been completed
LD_SERVICE_IDLE The configuration request/response combination has been completed
LD_SERVICE_ERROR The configuration request or response experienced an error

Definition at line 322 of file lin.h.

17.94.5.15 enum lin_tl_callback_return_t

Transport layer event IDs Implements : lin_tl_callback_return_t_Class.

Enumerator

TL_ACTION_NONE Default return value of call back function
TL_ACTION_ID_IGNORE Ignore this ID

Definition at line 362 of file lin.h.

17.94.5.16 enum lin_tl_event_id_t

Transport layer event IDs Implements : lin_tl_event_id_t_Class.

Enumerator

TL_MAKE_RES_DATA Make master request data
TL_SLAVE_GET_ACTION Get slave action
TL_TX_COMPLETED Transmit completed
TL_RX_COMPLETED Receive completed
TL_ERROR Transport error
TL_TIMEOUT_SERVICE Transmit timeout
TL_HANDLER_INTERLEAVE_MODE Interleave mode
TL_RECEIVE_MESSAGE Return data for Id_receive_message function

Definition at line 346 of file lin.h.

17.94.6 Function Documentation

17.94.6.1 `I_u8 Id_read_by_id_callout (I_ifc_handle iii, I_u8 id, I_u8 * data)`

17.94.6.2 `static I_u16 lin_calc_max_header_timeout_cnt (I_u32 baudRate) [inline],[static]`

Computes maximum header timeout.

$T_{Header_Maximum} = 1.4 * T_{Header_Nominal}$, $T_{Header_Nominal} = 34 * T_{Bit}$, (13 nominal bits of break; 1 nominal bit of break delimiter; 10 bits for SYNC and 10 bits of PID) $TIME_OUT_UNIT_US$ is in micro second

Parameters

<code>in</code>	<code><i>baudRate</i></code>	LIN network baud rate
-----------------	------------------------------	-----------------------

Returns

maximum timeout for the selected baud rate

Implements : `lin_calc_max_header_timeout_cnt_Activity`

Definition at line 626 of file `lin.h`.

17.94.6.3 `static I_u16 lin_calc_max_res_timeout_cnt (I_u32 baudRate, I_u8 size) [inline],[static]`

Computes the maximum response timeout.

$T_{Response_Maximum} = 1.4 * T_{Response_Nominal}$, $T_{Response_Nominal} = 10 * (N_{Data} + 1) * T_{Bit}$

Parameters

<code>in</code>	<code><i>baudRate</i></code>	LIN network baud rate
<code>in</code>	<code><i>size</i></code>	frame size in bytes

Returns

maximum response timeout for the given baud rate and frame size

Implements : `lin_calc_max_res_timeout_cnt_Activity`

Definition at line 642 of file `lin.h`.

17.94.6.4 `void lin_lld_deinit (I_ifc_handle iii)`

This function disconnect the node from the cluster and free all hardware used.

Parameters

<code>in</code>	<code><i>iii</i></code>	LIN interface that is being handled
-----------------	-------------------------	-------------------------------------

Returns

Zero for success
void

Definition at line 153 of file `lin.c`.

17.94.6.5 `lin_node_state_t lin_lld_get_state (I_ifc_handle iii)`

This function gets current state of an interface.

Parameters

<i>in</i>	<i>iii</i>	LIN interface that is being handled
-----------	------------	-------------------------------------

Returns

current LIN node state

Definition at line 174 of file lin.c.

17.94.6.6 I_u8 lin_ild_ignore_response (I_ifc_handle *iii*)

This function terminates an on-going data transmission/reception.

Parameters

<i>in</i>	<i>iii</i>	LIN interface that is being handled
-----------	------------	-------------------------------------

Returns

Zero for success
Non-zero for error

Definition at line 294 of file lin.c.

17.94.6.7 I_bool lin_ild_init (I_ifc_handle *iii*)

This function initializes a LIN hardware instance for operation. This function will initialize the run-time state structure to keep track of the on-going transfers, initialize the module to user defined settings and default settings, configure the IRQ state structure and enable the module-level interrupt to the core, and enable the LIN hardware module transmitter and receiver.

Parameters

<i>in</i>	<i>iii</i>	LIN interface that is being handled
-----------	------------	-------------------------------------

Returns

zero if the initialization was successful and non-zero if failed

Definition at line 88 of file lin.c.

17.94.6.8 I_u8 lin_ild_int_disable (I_ifc_handle *iii*)

Disable the interrupt related to the interface.

Parameters

<i>in</i>	<i>iii</i>	LIN interface that is being handled
-----------	------------	-------------------------------------

Returns

Zero for success
Non-zero for error

Definition at line 271 of file lin.c.

17.94.6.9 I_u8 lin_ild_int_enable (I_ifc_handle *iii*)

Enable the interrupt related to the interface.

Parameters

<i>in</i>	<i>iii</i>	LIN interface that is being handled
-----------	------------	-------------------------------------

Returns

Zero for success
Non-zero for error

Definition at line 248 of file lin.c.

17.94.6.10 I_u8 lin_ild_rx_response (I_ifc_handle *iii*, I_u8 *response_length*)

This function receives frame data into the LIN_ild_response_buffer[*iii*] buffer.

This function will prepare LIN interface to receive data and then return. Data bytes will be received to the buffer in the interrupt handler of LIN interface. This function returns zero if preparation of receiving data was successful.

Parameters

<i>in</i>	<i>iii</i>	LIN interface that is being handled
<i>in</i>	<i>response_length</i>	Length of response

Returns

Zero for success
Non-zero for error

Definition at line 376 of file lin.c.

17.94.6.11 I_u8 lin_ild_set_low_power_mode (I_ifc_handle *iii*)

Let the low level driver go to low power mode.

Parameters

<i>in</i>	<i>iii</i>	LIN interface that is being handled
-----------	------------	-------------------------------------

Returns

Zero for success
Non-zero for error

Definition at line 317 of file lin.c.

17.94.6.12 I_u8 lin_ild_set_response (I_ifc_handle *iii*, I_u8 *response_length*)

This function sends frame data that is contained in LIN_ild_response_buffer[*iii*].

This function will send the first data byte in the buffer and then return. Next data bytes will be sent in the interrupt handler of LIN interface. This function returns zero if sending of first data byte was successful.

Parameters

<i>in</i>	<i>iii</i>	LIN interface that is being handled
<i>in</i>	<i>response_length</i>	Length of response

Returns

Zero for success
Non-zero for error

Definition at line 340 of file lin.c.

17.94.6.13 void lin_ild_timeout_service (I_ifc_handle *iii*)

Callback function for Timer Interrupt Handler In timer IRQ handler, call this function. Used to check if frame timeout has occurred during frame data transmission and reception, to check for N_As and N_Cr timeout for LIN 2.1 and above. This function also check if there is no LIN bus communication (no headers and no frame data transferring) for Idle timeout (s), then put LIN node to Sleep mode. Users may initialize a timer (for example FTM) with period of Timeout unit (default: 500 micro seconds) to call [lin_ild_timeout_service\(\)](#). For an interface *iii*, Idle timeout (s) = max_idle_timeout_cnt * Timeout unit (us) frame timeout (us) = frame_timeout_cnt * Timeout unit (us) N_As timeout (us) = N_As_timeout * Timeout unit (us) N_Cr timeout (us) = N_Cr_timeout * Timeout unit (us)

Parameters

<i>in</i>	<i>iii</i>	LIN interface that is being handled
-----------	------------	-------------------------------------

Returns

void

Definition at line 407 of file lin.c.

17.94.6.14 I_u8 lin_ild_tx_header (I_ifc_handle *iii*, I_u8 *id*)

This function sends frame header for the input PID.

This function only initializes the sending of break field and then return. Then the sync byte and PID will be sent in the interrupt handler of LIN interface.

Parameters

<i>in</i>	<i>iii</i>	LIN interface that is being handled
<i>in</i>	<i>id</i>	ID of the header to be sent

Returns

Zero for success
Non-zero for error

Definition at line 197 of file lin.c.

17.94.6.15 I_u8 lin_ild_tx_wake_up (I_ifc_handle *iii*)

This function send a wakeup signal.

Parameters

<i>in</i>	<i>iii</i>	LIN interface that is being handled
-----------	------------	-------------------------------------

Returns

Zero for success
Non-zero for error

Definition at line 225 of file lin.c.

17.94.6.16 void lin_pid_resp_callback_handler (I_ifc_handle *iii*, const lin_ild_event_id_t *event_id*, I_u8 *id*)

Callback handler for low level events.

This callback handler is being called from the LIN driver callback

Parameters

in	<i>iii</i>	LIN interface that is being handled
in	<i>event_id</i>	Low level event id lin_llc_event_id_t
in	<i>id</i>	Current protected identifier under processing by driver

Definition at line 74 of file `lin_common_proto.c`.

17.94.6.17 `I_u8 lin_process_parity (I_u8 pid, I_u8 typeAction)`

Makes or checks parity bits. If action is checking parity, the function returns ID value if parity bits are correct or 0xFF if parity bits are incorrect. If action is making parity bits, then from input value of ID, the function returns PID.

Parameters

<i>pid</i>	PID byte in case of checking parity bits or ID byte in case of making parity bits.
<i>typeAction</i>	TRUE for Checking parity bits, FALSE for making parity bits

Returns

0xFF if parity bits are incorrect, ID in case of checking parity bits and they are correct. Function returns PID in case of making parity bits.

Definition at line 71 of file `lin.c`.

17.94.6.18 `lin_tl_callback_return_t lin_tl_callback_handler (I_ifc_handle iii, lin_tl_event_id_t tl_event_id, I_u8 id)`

Definition at line 81 of file `lin_commonctl_proto.c`.

17.94.7 Variable Documentation

17.94.7.1 `volatile I_u8 g_buffer_backup_data[8]`

17.94.7.2 `volatile I_u8 g_lin_flag_handle_tbl[LIN_FLAG_BUF_SIZE]`

17.94.7.3 `volatile I_u8 g_lin_frame_data_buffer[LIN_FRAME_BUF_SIZE]`

17.94.7.4 `volatile I_bool g_lin_frame_flag_handle_tbl[LIN_NUM_OF_FRMS]`

17.94.7.5 `volatile I_u8 g_lin_frame_updating_flag_tbl[LIN_NUM_OF_FRMS]`

17.94.7.6 `const I_ifc_handle g_lin_hardware_ifc[HARDWARE_INSTANCE_COUNT]`

17.94.7.7 `lin_master_data_t g_lin_master_data_array[LIN_NUM_OF_MASTER_IFCS]`

Global array for storing the master interfaces configurations

Definition at line 49 of file `lin.c`.

17.94.7.8 `const lin_node_attribute_t g_lin_node_attribute_array[LIN_NUM_OF_SLAVE_IFCS]`

17.94.7.9 `lin_protocol_state_t g_lin_protocol_state_array[LIN_NUM_OF_IFCS]`

Global array for storing the protocol state for each interface

Definition at line 47 of file `lin.c`.

17.94.7.10 `const lin_protocol_user_config_t g_lin_protocol_user_cfg_array[LIN_NUM_OF_IFCS]`

17.94.7.11 `lin_tl_descriptor_t g_lin_tl_descriptor_array[LIN_NUM_OF_IFCS]`

Global array for storing transport configuration for each interface

Definition at line 46 of file lin.c.

17.94.7.12 `const l_u32 g_lin_virtual_ifc[LIN_NUM_OF_IFCS]`

17.94.7.13 `const lin_timer_get_time_interval_t timerGetTimeIntervalCallbackArr[LIN_NUM_OF_IFCS]`

17.95 MPU Driver

17.95.1 Detailed Description

Memory Protection Unit Peripheral Driver.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\drivers\src\mpu\mpu_driver.c
{S32SDK_PATH}\platform\drivers\src\mpu\mpu_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\drivers\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

No special dependencies are required for this component

Pre-Initialization information of MPU module

1. Before using the MPU driver the protocol clock of the module must be configured by the application using clock module.
2. Bus fault or Hard fault exception must be configured to handle MPU access violation.

To initialize the MPU module, call the [MPU_DRV_Init\(\)](#) function and provide the user configuration data structure. This function sets the configuration of the MPU module automatically and enables the MPU module. The default settings for the Region Descriptor 0 (RGD0):

- The access right for **CORE, DMA,..** can be **changed** except **DEBUGGER** master.
- The **start address, end address, process identifier** and **process identifier mask** are **ignored**.

This is example code to configure the MPU driver:

1. Define MPU instance

```
/* MPU 0 */
#define INST_MPU 0U

/* Status variable */
status_t status;
```

2. Configuration

User configuration

```
/* Region count */
#define REGION_CNT (1U)

/* Master access configuration
FEATURE_MPU_MASTER_COUNT macro has been already defined (number of masters supported by hardware)
*/
```

```

mpu_master_access_right_t masterAccRight[FEATURE_MPU_MASTER_COUNT] =
{
    /* CORE */
    {
        .masterNum    = FEATURE_MPU_MASTER_CORE,        /* Master number */
        .accessRight = MPU_SUPERVISOR_RWX_USER_RWX,    /* Access right */
        .processIdentifierEnable = false,              /* Process identifier enable */
    },
    /* The rest masters should be defined here */
    ...
}
/* User configuration */
mpu_user_config_t userConfig[REGION_CNT] =
{
    /* Region 0 */
    {
        .startAddr      = 0x00000000U,        /* Memory region start address */
        .endAddr        = 0xFFFFFFFFU,        /* Memory region end address */
        .masterAccRight  = masterAccRight,    /* Master access right */
        .processIdEnable = false,             /* Process identifier enable */
        .processIdentifier = 0x00U,           /* Process identifier */
        .processIdMask   = 0x00U             /* Process identifier mask */
    }
}

```

or get default configuration

```

/* Defines master access right structure */
mpu_master_access_right_t masterAccRight[FEATURE_MPU_MASTER_COUNT];

/* Gets default region configuration
   Cover entire memory
   Access right of all masters are allowed
*/
mpu_user_config_t regionConfig0 =
    MPU_DRV_GetDefaultRegionConfig(masterAccRight);
mpu_user_config_t userConfig[REGION_CNT] =
{
    regionConfig0
};

```

3. Initializes

```

/* Initializes the MPU instance */
status = MPU_DRV_Init(INST_MPU, REGION_CNT, userConfig);

```

4. De-initializes

```

/* De-initializes the MPU instance */
MPU_DRV_Deinit(INST_MPU);

```

After MPU initialization:

- The [MPU_DRV_SetRegionConfig\(\)](#) can be used to add/update the new/existing region descriptor.

```

/* Add the new region descriptor.
   Region 1 to be the same with region 0.
*/
status = MPU_DRV_SetRegionConfig(INST_MPU, 1U, &userConfig[0U]);

/* Updates the existing region descriptor.
   Updates PID mask value on region 1.
*/
userConfig[0U].processIdMask = 0xFFU;
status = MPU_DRV_SetRegionConfig(INST_MPU, 1U, &userConfig[0U]);

```

- The [MPU_DRV_SetRegionAddr\(\)](#) can be used to update the start and end address on an existing region descriptor.

```

/* Updates region 1 location (0x20000000 - 0x2FFFFFFF) */
MPU_DRV_SetRegionAddr(INST_MPU, 1U, 0x20000000U, 0x2FFFFFFFU);

```

- The [MPU_DRV_SetMasterAccessRights\(\)](#) can be used to update access permission of master in the region.

```

/* DMA can only operate on region 1 */
mpu_master_access_right_t DMA_AccRight;
DMA_AccRight.masterNum = FEATURE_MPU_MASTER_DMA;
/* Removes all access rights of DMA on region 0 */
DMA_AccRight.accessRight = MPU_SUPERVISOR_USER_NONE;
status = MPU_DRV_SetMasterAccessRights(INST_MPU, 0U, &DMA_AccRight);
/* Allows all access to region 1 from DMA */
DMA_AccRight.accessRight = MPU_SUPERVISOR_USER_RWX;
status = MPU_DRV_SetMasterAccessRights(INST_MPU, 1U, &DMA_AccRight);

```

- The `MPU_DRV_GetDetailErrorAccessInfo()` API can be used to get the status of a slave port and the detail when an error occurred.

```

/* DMA access to SRAML
- Access type: read
- Address: 0x1FFEFF00 (region 0)
*/
...
/* Checks and gets error status on slave port 1 (SRAML backdoor) */
bool errStatus = false;
mpu_access_err_info_t errReport;
errStatus = MPU_DRV_GetDetailErrorAccessInfo(INST_MPU,
    FEATURE_MPU_SLAVE_SRAM_BACKDOOR, &errReport);
/* Checks status:
- errStatus: true
- errReport:
- errReport.master: FEATURE_MPU_MASTER_DMA (DMA logical ID)
- errReport.attributes: MPU_DATA_ACCESS_IN_SUPERVISOR_MODE (Data access in supervisor mode)
- errReport.accessType: MPU_ERR_TYPE_READ (Read access)
- errReport.accessCtr: 0x8000 (Access violation occurs on region 0 - MSB is region 0 and so on)
- errReport.addr: 0x1FFEFF00 (Data access in supervisor mode)
- errReport.processorIdentification: 0U (Do not support for non-core processor)
*/
...

```

- The `MPU_DRV_EnableRegion()` can be used to enable or disable region descriptor.

```

/* Disables DMA - disable region 1 descriptor */
MPU_DRV_EnableRegion(INST_MPU, 1U, false);
/* Enables again */
MPU_DRV_EnableRegion(INST_MPU, 1U, true);

```

Power management:

- To minimizes power dissipation, disables MPU module or regions by using `MPU_DRV_Deinit()/MPU_DRV_↵_EnableRegion()` when they are unused anymore.

Data Structures

- struct `mpu_access_err_info_t`
MPU detail error access info Implements : `mpu_access_err_info_t_Class`. [More...](#)
- struct `mpu_master_access_right_t`
MPU master access rights. Implements : `mpu_master_access_right_t_Class`. [More...](#)
- struct `mpu_user_config_t`
MPU user region configuration structure. This structure is used when calling the `MPU_DRV_Init` function. Implements : `mpu_user_config_t_Class`. [More...](#)

Enumerations

- enum `mpu_err_access_type_t` { `MPU_ERR_TYPE_READ` = 0U, `MPU_ERR_TYPE_WRITE` = 1U }
MPU access error Implements : `mpu_err_access_type_t_Class`.
- enum `mpu_err_attributes_t` { `MPU_INSTRUCTION_ACCESS_IN_USER_MODE` = 0U, `MPU_DATA_ACCESS_IN_USER_MODE` = 1U, `MPU_INSTRUCTION_ACCESS_IN_SUPERVISOR_MODE` = 2U, `MPU_DATA_ACCESS_IN_SUPERVISOR_MODE` = 3U }
MPU access error attributes Implements : `mpu_err_attributes_t_Class`.

```

• enum mpu_access_rights_t {
    MPU_SUPERVISOR_RWX_USER_NONE = 0x00U, MPU_SUPERVISOR_RWX_USER_X = 0x01U, MPU_SUPERVISOR_RWX_USER_W = 0x02U, MPU_SUPERVISOR_RWX_USER_WX = 0x03U,
    MPU_SUPERVISOR_RWX_USER_R = 0x04U, MPU_SUPERVISOR_RWX_USER_RX = 0x05U, MPU_SUPERVISOR_RWX_USER_RW = 0x06U, MPU_SUPERVISOR_RWX_USER_RWX = 0x07U,
    MPU_SUPERVISOR_RX_USER_NONE = 0x08U, MPU_SUPERVISOR_RX_USER_X = 0x09U, MPU_SUPERVISOR_RX_USER_W = 0x0AU, MPU_SUPERVISOR_RX_USER_WX = 0x0BU,
    MPU_SUPERVISOR_RX_USER_R = 0x0CU, MPU_SUPERVISOR_RX_USER_RX = 0x0DU, MPU_SUPERVISOR_RX_USER_RW = 0x0EU, MPU_SUPERVISOR_RX_USER_RWX = 0x0FU,
    MPU_SUPERVISOR_RW_USER_NONE = 0x10U, MPU_SUPERVISOR_RW_USER_X = 0x11U, MPU_SUPERVISOR_RW_USER_W = 0x12U, MPU_SUPERVISOR_RW_USER_WX = 0x13U,
    MPU_SUPERVISOR_RW_USER_R = 0x14U, MPU_SUPERVISOR_RW_USER_RX = 0x15U, MPU_SUPERVISOR_RW_USER_RW = 0x16U, MPU_SUPERVISOR_RW_USER_RWX = 0x17U,
    MPU_SUPERVISOR_USER_NONE = 0x18U, MPU_SUPERVISOR_USER_X = 0x19U, MPU_SUPERVISOR_USER_W = 0x1AU, MPU_SUPERVISOR_USER_WX = 0x1BU,
    MPU_SUPERVISOR_USER_R = 0x1CU, MPU_SUPERVISOR_USER_RX = 0x1DU, MPU_SUPERVISOR_USER_RW = 0x1EU, MPU_SUPERVISOR_USER_RWX = 0x1FU,
    MPU_NONE = 0x80U, MPU_W = 0xA0U, MPU_R = 0xC0U, MPU_RW = 0xE0U }

```

MPU access rights.

Code	Supervisor	User	Description
MPU_SUPERVISOR_RWX_USER_NONE	r w x	- - -	Allow Read, write, execute in supervisor mode; no access in user mode
MPU_SUPERVISOR_RWX_USER_X	r w x	- - x	Allow Read, write, execute in supervisor mode; execute in user mode
MPU_SUPERVISOR_RWX_USER_W	r w x	- w -	Allow Read, write, execute in supervisor mode; write in user mode
MPU_SUPERVISOR_RWX_USER_WX	r w x	- w x	Allow Read, write, execute in supervisor mode; write and execute in user mode
MPU_SUPERVISOR_RWX_USER_R	r w x	r - -	Allow Read, write, execute in supervisor mode; read in user mode
MPU_SUPERVISOR_RWX_USER_RX	r w x	r - x	Allow Read, write, execute in supervisor mode; read and execute in user mode
MPU_SUPERVISOR_RWX_USER_RW	r w x	r w -	Allow Read, write, execute in supervisor mode; read and write in user mode
MPU_SUPERVISOR_RWX_USER_RWX	r w x	r w x	Allow Read, write, execute in supervisor mode; read, write and execute in user mode
MPU_SUPERVISOR_RX_USER_NONE	r - x	- - -	Allow Read, execute in supervisor mode; no access in user mode
MPU_SUPERVISOR_RX_USER_X	r - x	- - x	Allow Read, execute in supervisor mode; execute in user mode

<i>MPU_SUPERVISOR_↔ RX_USER_W</i>	<i>r - x</i>	<i>- w -</i>	<i>Allow Read, execute in supervisor mode; write in user mode</i>
<i>MPU_SUPERVISOR_↔ RX_USER_WX</i>	<i>r - x</i>	<i>- w x</i>	<i>Allow Read, execute in supervisor mode; write and execute in user mode</i>
<i>MPU_SUPERVISOR_↔ RX_USER_R</i>	<i>r - x</i>	<i>r - -</i>	<i>Allow Read, execute in supervisor mode; read in user mode</i>
<i>MPU_SUPERVISOR_↔ RX_USER_RX</i>	<i>r - x</i>	<i>r - x</i>	<i>Allow Read, execute in supervisor mode; read and execute in user mode</i>
<i>MPU_SUPERVISOR_↔ RX_USER_RW</i>	<i>r - x</i>	<i>r w -</i>	<i>Allow Read, execute in supervisor mode; read and write in user mode</i>
<i>MPU_SUPERVISOR_↔ RX_USER_RWX</i>	<i>r - x</i>	<i>r w x</i>	<i>Allow Read, execute in supervisor mode; read, write and execute in user mode</i>
<i>MPU_SUPERVISOR_↔ RW_USER_NONE</i>	<i>r w -</i>	<i>- - -</i>	<i>Allow Read, write in supervisor mode; no access in user mode</i>
<i>MPU_SUPERVISOR_↔ RW_USER_X</i>	<i>r w -</i>	<i>- - x</i>	<i>Allow Read, write in supervisor mode; execute in user mode</i>
<i>MPU_SUPERVISOR_↔ RW_USER_W</i>	<i>r w -</i>	<i>- w -</i>	<i>Allow Read, write in supervisor mode; write in user mode</i>
<i>MPU_SUPERVISOR_↔ RW_USER_WX</i>	<i>r w -</i>	<i>- w x</i>	<i>Allow Read, write in supervisor mode; write and execute in user mode</i>
<i>MPU_SUPERVISOR_↔ RW_USER_R</i>	<i>r w -</i>	<i>r - -</i>	<i>Allow Read, write in supervisor mode; read in user mode</i>
<i>MPU_SUPERVISOR_↔ RW_USER_RX</i>	<i>r w -</i>	<i>r - x</i>	<i>Allow Read, write in supervisor mode; read and execute in user mode</i>
<i>MPU_SUPERVISOR_↔ RW_USER_RW</i>	<i>r w -</i>	<i>r w -</i>	<i>Allow Read, write in supervisor mode; read and write in user mode</i>
<i>MPU_SUPERVISOR_↔ RW_USER_RWX</i>	<i>r w -</i>	<i>r w x</i>	<i>Allow Read, write in supervisor mode; read, write and execute in user mode</i>
<i>MPU_SUPERVISOR_↔ USER_NONE</i>	<i>- - -</i>	<i>- - -</i>	<i>No access allowed in user and supervisor modes</i>
<i>MPU_SUPERVISOR_↔ USER_X</i>	<i>- - x</i>	<i>- - x</i>	<i>Execute operation is allowed in user and supervisor modes</i>
<i>MPU_SUPERVISOR_↔ USER_W</i>	<i>- w -</i>	<i>- w -</i>	<i>Write operation is allowed in user and supervisor modes</i>

<code>MPU_SUPERVISOR_↔ USER_WX</code>	<code>- w x</code>	<code>- w x</code>	Write and execute operations are allowed in user and supervisor modes
<code>MPU_SUPERVISOR_↔ USER_R</code>	<code>r - -</code>	<code>r - -</code>	Read operation is allowed in user and supervisor modes
<code>MPU_SUPERVISOR_↔ USER_RX</code>	<code>r - x</code>	<code>r - x</code>	Read and execute operations are allowed in user and supervisor modes
<code>MPU_SUPERVISOR_↔ USER_RW</code>	<code>r w -</code>	<code>r w -</code>	Read and write operations are allowed in user and supervisor modes
<code>MPU_SUPERVISOR_↔ USER_RWX</code>	<code>r w x</code>	<code>r w x</code>	Read write and execute operations are allowed in user and supervisor modes

MPU Driver API

- `status_t MPU_DRV_Init` (uint32_t instance, uint8_t regionCnt, const `mpu_user_config_t` *userConfigArr)
The function initializes the memory protection unit by setting the access configurations of all available masters, process identifier and the memory location for the given regions; and activate module finally. Please note that access rights for region 0 will always be configured and regionCnt takes values between 1 and the maximum region count supported by the hardware. e.g. In S32K144 the number of supported regions is 8. The user must make sure that the clock is enabled.
- `void MPU_DRV_Deinit` (uint32_t instance)
De-initializes the memory protection unit by resetting all regions to default and disable module.
- `void MPU_DRV_SetRegionAddr` (uint32_t instance, uint8_t regionNum, uint32_t startAddr, uint32_t endAddr)
Sets the region start and end address.
- `status_t MPU_DRV_SetRegionConfig` (uint32_t instance, uint8_t regionNum, const `mpu_user_config_↔
t` *userConfigPtr)
Sets the region configuration. Updates the access configuration of all available masters, process identifier and memory location in a given region.
- `status_t MPU_DRV_SetMasterAccessRights` (uint32_t instance, uint8_t regionNum, const `mpu_master_↔
access_right_t` *accessRightsPtr)
Configures access permission for bus master in region.
- `bool MPU_DRV_GetDetailErrorAccessInfo` (uint32_t instance, uint8_t slavePortNum, `mpu_access_err_info_↔
_t` *errInfoPtr)
Checks and gets the MPU access error detail information for a slave port. Clears bus error flag if an error occurs.
- `mpu_user_config_t MPU_DRV_GetDefaultRegionConfig` (`mpu_master_access_right_t` *masterAccRight)
Gets default region configuration. Grants all access rights for masters and disables PID on entire memory.
- `void MPU_DRV_EnableRegion` (uint32_t instance, uint8_t regionNum, bool enable)
Enables/Disables region descriptor. Please note that region 0 should not be disabled.

17.95.2 Data Structure Documentation

17.95.2.1 struct `mpu_access_err_info_t`

MPU detail error access info Implements : `mpu_access_err_info_t_Class`.

Definition at line 63 of file `mpu_driver.h`.

Data Fields

- [uint8_t master](#)
- [mpu_err_attributes_t attributes](#)
- [mpu_err_access_type_t accessType](#)
- [uint16_t accessCtr](#)
- [uint32_t addr](#)

Field Documentation

17.95.2.1.1 [uint16_t accessCtr](#)

Access error control

Definition at line 68 of file `mpu_driver.h`.

17.95.2.1.2 [mpu_err_access_type_t accessType](#)

Access error type

Definition at line 67 of file `mpu_driver.h`.

17.95.2.1.3 [uint32_t addr](#)

Access error address

Definition at line 69 of file `mpu_driver.h`.

17.95.2.1.4 [mpu_err_attributes_t attributes](#)

Access error attributes

Definition at line 66 of file `mpu_driver.h`.

17.95.2.1.5 [uint8_t master](#)

Access error master

Definition at line 65 of file `mpu_driver.h`.

17.95.2.2 [struct mpu_master_access_right_t](#)

MPU master access rights. Implements : `mpu_master_access_right_t_Class`.

Definition at line 173 of file `mpu_driver.h`.

Data Fields

- [uint8_t masterNum](#)
- [mpu_access_rights_t accessRight](#)

Field Documentation

17.95.2.2.1 [mpu_access_rights_t accessRight](#)

Access right

Definition at line 176 of file `mpu_driver.h`.

17.95.2.2.2 [uint8_t masterNum](#)

Master number

Definition at line 175 of file `mpu_driver.h`.

17.95.2.3 struct mpu_user_config_t

MPU user region configuration structure. This structure is used when calling the MPU_DRV_Init function. Implements : mpu_user_config_t_Class.

Definition at line 187 of file mpu_driver.h.

Data Fields

- uint32_t [startAddr](#)
- uint32_t [endAddr](#)
- const [mpu_master_access_right_t](#) * [masterAccRight](#)

Field Documentation

17.95.2.3.1 uint32_t endAddr

Memory region end address

Definition at line 190 of file mpu_driver.h.

17.95.2.3.2 const mpu_master_access_right_t* masterAccRight

Access permission for masters

Definition at line 191 of file mpu_driver.h.

17.95.2.3.3 uint32_t startAddr

Memory region start address

Definition at line 189 of file mpu_driver.h.

17.95.3 Enumeration Type Documentation

17.95.3.1 enum mpu_access_rights_t

MPU access rights.

Code	Supervisor	User	Description
MPU_SUPERVISOR_↔ RWX_USER_NONE	r w x	- - -	Allow Read, write, execute in supervisor mode; no access in user mode
MPU_SUPERVISOR_↔ RWX_USER_X	r w x	- - x	Allow Read, write, execute in supervisor mode; execute in user mode
MPU_SUPERVISOR_↔ RWX_USER_W	r w x	- w -	Allow Read, write, execute in supervisor mode; write in user mode
MPU_SUPERVISOR_↔ RWX_USER_WX	r w x	- w x	Allow Read, write, execute in supervisor mode; write and execute in user mode

MPU_SUPERVISOR_↔ RWX_USER_R	r w x	r - -	Allow Read, write, execute in supervisor mode; read in user mode
MPU_SUPERVISOR_↔ RWX_USER_RX	r w x	r - x	Allow Read, write, execute in supervisor mode; read and execute in user mode
MPU_SUPERVISOR_↔ RWX_USER_RW	r w x	r w -	Allow Read, write, execute in supervisor mode; read and write in user mode
MPU_SUPERVISOR_↔ RWX_USER_RWX	r w x	r w x	Allow Read, write, execute in supervisor mode; read, write and execute in user mode
MPU_SUPERVISOR_↔ RX_USER_NONE	r - x	- - -	Allow Read, execute in supervisor mode; no access in user mode
MPU_SUPERVISOR_↔ RX_USER_X	r - x	- - x	Allow Read, execute in supervisor mode; execute in user mode
MPU_SUPERVISOR_↔ RX_USER_W	r - x	- w -	Allow Read, execute in supervisor mode; write in user mode
MPU_SUPERVISOR_↔ RX_USER_WX	r - x	- w x	Allow Read, execute in supervisor mode; write and execute in user mode
MPU_SUPERVISOR_↔ RX_USER_R	r - x	r - -	Allow Read, execute in supervisor mode; read in user mode
MPU_SUPERVISOR_↔ RX_USER_RX	r - x	r - x	Allow Read, execute in supervisor mode; read and execute in user mode
MPU_SUPERVISOR_↔ RX_USER_RW	r - x	r w -	Allow Read, execute in supervisor mode; read and write in user mode
MPU_SUPERVISOR_↔ RX_USER_RWX	r - x	r w x	Allow Read, execute in supervisor mode; read, write and execute in user mode
MPU_SUPERVISOR_↔ RW_USER_NONE	r w -	- - -	Allow Read, write in supervisor mode; no access in user mode
MPU_SUPERVISOR_↔ RW_USER_X	r w -	- - x	Allow Read, write in supervisor mode; execute in user mode
MPU_SUPERVISOR_↔ RW_USER_W	r w -	- w -	Allow Read, write in supervisor mode; write in user mode

MPU_SUPERVISOR_↔ RW_USER_WX	r w -	- w x	Allow Read, write in supervisor mode; write and execute in user mode
MPU_SUPERVISOR_↔ RW_USER_R	r w -	r - -	Allow Read, write in supervisor mode; read in user mode
MPU_SUPERVISOR_↔ RW_USER_RX	r w -	r - x	Allow Read, write in supervisor mode; read and execute in user mode
MPU_SUPERVISOR_↔ RW_USER_RW	r w -	r w -	Allow Read, write in supervisor mode; read and write in user mode
MPU_SUPERVISOR_↔ RW_USER_RWX	r w -	r w x	Allow Read, write in supervisor mode; read, write and execute in user mode
MPU_SUPERVISOR_↔ USER_NONE	- - -	- - -	No access allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_X	- - x	- - x	Execute operation is allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_W	- w -	- w -	Write operation is allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_WX	- w x	- w x	Write and execute operations are allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_R	r - -	r - -	Read operation is allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_RX	r - x	r - x	Read and execute operations are allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_RW	r w -	r w -	Read and write operations are allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_RWX	r w x	r w x	Read write and execute operations are allowed in user and supervisor modes

Code	Read/Write permission	Description
MPU_NONE	- -	No Read/Write access permission
MPU_W	- w	Write access permission
MPU_R	r -	Read access permission
MPU_RW	r w	Read/Write access permission

Implements : mpu_access_rights_t_Class

Enumerator

MPU_SUPERVISOR_RWX_USER_NONE 0b00000000U : rwx|—

MPU_SUPERVISOR_RWX_USER_X 0b00000001U : rwx|—x

MPU_SUPERVISOR_RWX_USER_W 0b00000010U : rwx|—w-

```

MPU_SUPERVISOR_RWX_USER_WX 0b00000011U : rwx|-wx
MPU_SUPERVISOR_RWX_USER_R 0b00000100U : rwx|r-
MPU_SUPERVISOR_RWX_USER_RX 0b00000101U : rwx|r-x
MPU_SUPERVISOR_RWX_USER_RW 0b00000110U : rwx|rw-
MPU_SUPERVISOR_RWX_USER_RWX 0b00000111U : rwx|rwx
MPU_SUPERVISOR_RX_USER_NONE 0b00001000U : r-x|—
MPU_SUPERVISOR_RX_USER_X 0b00001001U : r-x|-x
MPU_SUPERVISOR_RX_USER_W 0b00001010U : r-x|-w-
MPU_SUPERVISOR_RX_USER_WX 0b00001011U : r-x|-wx
MPU_SUPERVISOR_RX_USER_R 0b00001100U : r-x|r-
MPU_SUPERVISOR_RX_USER_RX 0b00001101U : r-x|r-x
MPU_SUPERVISOR_RX_USER_RW 0b00001110U : r-x|rw-
MPU_SUPERVISOR_RX_USER_RWX 0b00001111U : r-x|rwx
MPU_SUPERVISOR_RW_USER_NONE 0b00010000U : rw-|—
MPU_SUPERVISOR_RW_USER_X 0b00010001U : rw-|-x
MPU_SUPERVISOR_RW_USER_W 0b00010010U : rw-|-w-
MPU_SUPERVISOR_RW_USER_WX 0b00010011U : rw-|-wx
MPU_SUPERVISOR_RW_USER_R 0b00010100U : rw-|r-
MPU_SUPERVISOR_RW_USER_RX 0b00010101U : rw-|r-x
MPU_SUPERVISOR_RW_USER_RW 0b00010110U : rw-|rw-
MPU_SUPERVISOR_RW_USER_RWX 0b00010111U : rw-|rwx
MPU_SUPERVISOR_USER_NONE 0b00011000U : —|—
MPU_SUPERVISOR_USER_X 0b00011001U : -x|-x
MPU_SUPERVISOR_USER_W 0b00011010U : -w-|-w-
MPU_SUPERVISOR_USER_WX 0b00011011U : -wx|-wx
MPU_SUPERVISOR_USER_R 0b00011100U : r-|r-
MPU_SUPERVISOR_USER_RX 0b00011101U : r-x|r-x
MPU_SUPERVISOR_USER_RW 0b00011110U : rw-|rw-
MPU_SUPERVISOR_USER_RWX 0b00011111U : rwx|rwx
MPU_NONE 0b10000000U : -
MPU_W 0b10100000U : w-
MPU_R 0b11000000U : -r
MPU_RW 0b11100000U : wr

```

Definition at line 121 of file mpu_driver.h.

17.95.3.2 enum mpu_err_access_type_t

MPU access error Implements : mpu_err_access_type_t_Class.

Enumerator

```

MPU_ERR_TYPE_READ MPU error type: read
MPU_ERR_TYPE_WRITE MPU error type: write

```

Definition at line 41 of file mpu_driver.h.

17.95.3.3 enum mpu_err_attributes_t

MPU access error attributes Implements : mpu_err_attributes_t_Class.

Enumerator

MPU_INSTRUCTION_ACCESS_IN_USER_MODE Access instruction error in user mode

MPU_DATA_ACCESS_IN_USER_MODE Access data error in user mode

MPU_INSTRUCTION_ACCESS_IN_SUPERVISOR_MODE Access instruction error in supervisor mode

MPU_DATA_ACCESS_IN_SUPERVISOR_MODE Access data error in supervisor mode

Definition at line 51 of file mpu_driver.h.

17.95.4 Function Documentation

17.95.4.1 void MPU_DRV_Deinit (uint32_t instance)

De-initializes the memory protection unit by resetting all regions to default and disable module.

Parameters

in	<i>instance</i>	The MPU peripheral instance number.
----	-----------------	-------------------------------------

Definition at line 105 of file mpu_driver.c.

17.95.4.2 void MPU_DRV_EnableRegion (uint32_t instance, uint8_t regionNum, bool enable)

Enables/Disables region descriptor. Please note that region 0 should not be disabled.

Parameters

in	<i>instance</i>	The MPU peripheral instance number.
in	<i>regionNum</i>	The region number.
in	<i>enable</i>	Valid state <ul style="list-style-type: none"> • true : Enable region. • false : Disable region.

Definition at line 344 of file mpu_driver.c.

17.95.4.3 mpu_user_config_t MPU_DRV_GetDefaultRegionConfig (mpu_master_access_right_t * masterAccRight)

Gets default region configuration. Grants all access rights for masters and disables PID on entire memory.

Parameters

out	<i>masterAccRight</i>	The pointer to master configuration structure, see mpu_master_access_right_t . The length of array should be defined by number of masters supported by hardware.
-----	-----------------------	--

Returns

The default region configuration, see [mpu_user_config_t](#).

Definition at line 308 of file mpu_driver.c.

17.95.4.4 bool MPU_DRV_GetDetailErrorAccessInfo (uint32_t instance, uint8_t slavePortNum, mpu_access_err_info_t * errInfoPtr)

Checks and gets the MPU access error detail information for a slave port. Clears bus error flag if an error occurs.

Parameters

in	<i>instance</i>	The MPU peripheral instance number.
in	<i>slavePortNum</i>	The slave port number to get Error Detail.
out	<i>errInfoPtr</i>	The pointer to access error info structure, #see mpu_access_err_info_t .

Returns

operation status

- true : An error has occurred.
- false : No error has occurred.

Definition at line 256 of file mpu_driver.c.

17.95.4.5 `status_t MPU_DRV_Init (uint32_t instance, uint8_t regionCnt, const mpu_user_config_t * userConfigArr)`

The function initializes the memory protection unit by setting the access configurations of all available masters, process identifier and the memory location for the given regions; and activate module finally. Please note that access rights for region 0 will always be configured and regionCnt takes values between 1 and the maximum region count supported by the hardware. e.g. In S32K144 the number of supported regions is 8. The user must make sure that the clock is enabled.

Parameters

in	<i>instance</i>	The MPU peripheral instance number.
in	<i>regionCnt</i>	The number of configured regions.
in	<i>userConfigArr</i>	The pointer to the array of MPU user configure structure, see mpu_user_config_t .

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failed due to master number is out of range supported by hardware.

Definition at line 62 of file mpu_driver.c.

17.95.4.6 `status_t MPU_DRV_SetMasterAccessRights (uint32_t instance, uint8_t regionNum, const mpu_master_access_right_t * accessRightsPtr)`

Configures access permission for bus master in region.

Parameters

in	<i>instance</i>	The MPU peripheral instance number.
in	<i>regionNum</i>	The MPU region number.
in	<i>accessRightsPtr</i>	The pointer to access permission structure, #see mpu_master_access_right_t .

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failed due to master number is out of range supported by hardware.

Definition at line 224 of file mpu_driver.c.

17.95.4.7 `void MPU_DRV_SetRegionAddr (uint32_t instance, uint8_t regionNum, uint32_t startAddr, uint32_t endAddr)`

Sets the region start and end address.

Parameters

in	<i>instance</i>	The MPU peripheral instance number.
in	<i>regionNum</i>	The region number.
in	<i>startAddr</i>	The region start address.
in	<i>endAddr</i>	The region end address.

Definition at line 137 of file mpu_driver.c.

17.95.4.8 `status_t MPU_DRV_SetRegionConfig (uint32_t instance, uint8_t regionNum, const mpu_user_config_t * userConfigPtr)`

Sets the region configuration. Updates the access configuration of all available masters, process identifier and memory location in a given region.

Parameters

in	<i>instance</i>	The MPU peripheral instance number.
in	<i>regionNum</i>	The region number.
in	<i>userConfigPtr</i>	The region configuration structure pointer.

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failed due to master number is out of range supported by hardware.

Definition at line 164 of file mpu_driver.c.

17.96 MPU PAL

17.96.1 Detailed Description

Memory Protection Unit Peripheral Abstraction Layer.

Data Structures

- struct [mpu_error_info_t](#)
MPU detail error access info Implements : [mpu_error_info_t_Class](#). [More...](#)
- struct [mpu_master_access_permission_t](#)
MPU master access permission. Implements : [mpu_master_access_permission_t_Class](#). [More...](#)
- struct [mpu_region_config_t](#)
MPU region configuration structure. Implements : [mpu_region_config_t_Class](#). [More...](#)

Typedefs

- typedef [mpu_access_rights_t](#) [mpu_access_permission_t](#)

MPU detail access permission For specific master:

Code	Supervisor	User	Description
MPU_SUPERVISOR_↔ RWX_USER_NONE	<i>r w x</i>	- - -	Allow Read, write, execute in supervisor mode; no access in user mode
MPU_SUPERVISOR_↔ RWX_USER_X	<i>r w x</i>	- - x	Allow Read, write, execute in supervisor mode; execute in user mode
MPU_SUPERVISOR_↔ RWX_USER_W	<i>r w x</i>	- w -	Allow Read, write, execute in supervisor mode; write in user mode
MPU_SUPERVISOR_↔ RWX_USER_WX	<i>r w x</i>	- w x	Allow Read, write, execute in supervisor mode; write and execute in user mode
MPU_SUPERVISOR_↔ RWX_USER_R	<i>r w x</i>	r - -	Allow Read, write, execute in supervisor mode; read in user mode
MPU_SUPERVISOR_↔ RWX_USER_RX	<i>r w x</i>	r - x	Allow Read, write, execute in supervisor mode; read and execute in user mode
MPU_SUPERVISOR_↔ RWX_USER_RW	<i>r w x</i>	r w -	Allow Read, write, execute in supervisor mode; read and write in user mode
MPU_SUPERVISOR_↔ RWX_USER_RWX	<i>r w x</i>	r w x	Allow Read, write, execute in supervisor mode; read, write and execute in user mode

MPU_SUPERVISOR_↔ RX_USER_NONE	r - x	- - -	Allow Read, execute in supervisor mode; no access in user mode
MPU_SUPERVISOR_↔ RX_USER_X	r - x	- - x	Allow Read, execute in supervisor mode; execute in user mode
MPU_SUPERVISOR_↔ RX_USER_W	r - x	- w -	Allow Read, execute in supervisor mode; write in user mode
MPU_SUPERVISOR_↔ RX_USER_WX	r - x	- w x	Allow Read, execute in supervisor mode; write and execute in user mode
MPU_SUPERVISOR_↔ RX_USER_R	r - x	r - -	Allow Read, execute in supervisor mode; read in user mode
MPU_SUPERVISOR_↔ RX_USER_RX	r - x	r - x	Allow Read, execute in supervisor mode; read and execute in user mode
MPU_SUPERVISOR_↔ RX_USER_RW	r - x	r w -	Allow Read, execute in supervisor mode; read and write in user mode
MPU_SUPERVISOR_↔ RX_USER_RWX	r - x	r w x	Allow Read, execute in supervisor mode; read, write and execute in user mode
MPU_SUPERVISOR_↔ RW_USER_NONE	r w -	- - -	Allow Read, write in supervisor mode; no access in user mode
MPU_SUPERVISOR_↔ RW_USER_X	r w -	- - x	Allow Read, write in supervisor mode; execute in user mode
MPU_SUPERVISOR_↔ RW_USER_W	r w -	- w -	Allow Read, write in supervisor mode; write in user mode
MPU_SUPERVISOR_↔ RW_USER_WX	r w -	- w x	Allow Read, write in supervisor mode; write and execute in user mode
MPU_SUPERVISOR_↔ RW_USER_R	r w -	r - -	Allow Read, write in supervisor mode; read in user mode
MPU_SUPERVISOR_↔ RW_USER_RX	r w -	r - x	Allow Read, write in supervisor mode; read and execute in user mode
MPU_SUPERVISOR_↔ RW_USER_RW	r w -	r w -	Allow Read, write in supervisor mode; read and write in user mode
MPU_SUPERVISOR_↔ RW_USER_RWX	r w -	r w x	Allow Read, write in supervisor mode; read, write and execute in user mode

<code>MPU_SUPERVISOR_↔ USER_NONE</code>	- - -	- - -	No access allowed in user and supervisor modes
<code>MPU_SUPERVISOR_↔ USER_X</code>	- - x	- - x	Execute operation is allowed in user and supervisor modes
<code>MPU_SUPERVISOR_↔ USER_W</code>	- w -	- w -	Write operation is allowed in user and supervisor modes
<code>MPU_SUPERVISOR_↔ USER_WX</code>	- w x	- w x	Write and execute operations are allowed in user and supervisor modes
<code>MPU_SUPERVISOR_↔ USER_R</code>	r - -	r - -	Read operation is allowed in user and supervisor modes
<code>MPU_SUPERVISOR_↔ USER_RX</code>	r - x	r - x	Read and execute operations are allowed in user and supervisor modes
<code>MPU_SUPERVISOR_↔ USER_RW</code>	r w -	r w -	Read and write operations are allowed in user and supervisor modes
<code>MPU_SUPERVISOR_↔ USER_RWX</code>	r w x	r w x	Read write and execute operations are allowed in user and supervisor modes

Enumerations

- enum `mpu_error_access_type_t` { `MPU_ERROR_TYPE_READ` = 0U, `MPU_ERROR_TYPE_WRITE` = 1U }
MPU access error Implements : `mpu_error_access_type_t` Class.
- enum `mpu_error_attributes_t` { `MPU_ERROR_USER_MODE_INSTRUCTION_ACCESS` = 0U, `MPU_ERROR_USER_MODE_DATA_ACCESS` = 1U, `MPU_ERROR_SUPERVISOR_MODE_INSTRUCTION_ACCESS` = 2U, `MPU_ERROR_SUPERVISOR_MODE_DATA_ACCESS` = 3U }
MPU access error attributes Implements : `mpu_error_attributes_t` Class.

MPU PAL API

- status_t `MPU_Init` (const `mpu_instance_t` *const instance, uint8_t regionCnt, const `mpu_region_config_t` *configPtr)
Initializes memory protection unit by allocating regions and granting access rights for masters.
- status_t `MPU_Deinit` (const `mpu_instance_t` *const instance)
De-initializes memory protection unit by resetting all regions and masters to default and disable module.
- status_t `MPU_GetDefaultRegionConfig` (const `mpu_instance_t` *const instance, `mpu_master_access_permission_t` *masterAccRight, `mpu_region_config_t` *regionConfig)
Gets default region configuration. Grants all access rights for masters; disable PID and cache; unlock region descriptor.
- status_t `MPU_UpdateRegion` (const `mpu_instance_t` *const instance, uint8_t regionNum, const `mpu_region_config_t` *configPtr)
Updates region configuration.
- status_t `MPU_EnableRegion` (const `mpu_instance_t` *const instance, uint8_t regionNum, bool enable)
Enables or disables an exist region configuration.
- bool `MPU_GetError` (const `mpu_instance_t` *const instance, uint8_t channel, `mpu_error_info_t` *errPtr)
Checks and gets the access error detail information then clear error flag if the error caused by a master.

- enum [mpu_inst_type_t](#)

Enumeration with the types of peripherals supported by MPU PAL.

17.96.2 Data Structure Documentation

17.96.2.1 struct mpu_error_info_t

MPU detail error access info Implements : mpu_error_info_t_Class.

Definition at line 67 of file mpu_pal.h.

Data Fields

- uint8_t [master](#)
- bool [overrun](#)
- [mpu_error_attributes_t](#) [attributes](#)
- [mpu_error_access_type_t](#) [accessType](#)
- uint32_t [accessCtr](#)
- uint32_t [addr](#)
- uint8_t [processId](#)

Field Documentation

17.96.2.1.1 uint32_t accessCtr

Access error control

Definition at line 73 of file mpu_pal.h.

17.96.2.1.2 mpu_error_access_type_t accessType

Access error type

Definition at line 72 of file mpu_pal.h.

17.96.2.1.3 uint32_t addr

Access error address

Definition at line 74 of file mpu_pal.h.

17.96.2.1.4 mpu_error_attributes_t attributes

Access error attributes

Definition at line 71 of file mpu_pal.h.

17.96.2.1.5 uint8_t master

Access error master

Definition at line 69 of file mpu_pal.h.

17.96.2.1.6 bool overrun

Access error master overrun

Definition at line 70 of file mpu_pal.h.

17.96.2.1.7 uint8_t processId

Access error process identification

Definition at line 75 of file mpu_pal.h.

17.96.2.2 struct mpu_master_access_permission_t

MPU master access permission. Implements : `mpu_master_access_permission_t_Class`.

Definition at line 141 of file `mpu_pal.h`.

Data Fields

- `uint8_t masterNum`
- `mpu_access_permission_t accessRight`

Field Documentation**17.96.2.2.1 mpu_access_permission_t accessRight**

Privilege right

Definition at line 144 of file `mpu_pal.h`.

17.96.2.2.2 uint8_t masterNum

Master number

Definition at line 143 of file `mpu_pal.h`.

17.96.2.3 struct mpu_region_config_t

MPU region configuration structure. Implements : `mpu_region_config_t_Class`.

Definition at line 151 of file `mpu_pal.h`.

Data Fields

- `uint32_t startAddr`
- `uint32_t endAddr`
- `const mpu_master_access_permission_t * masterAccRight`
- `uint8_t processIdEnable`
- `uint8_t processIdentifier`
- `uint8_t processIdMask`
- `void * extension`

Field Documentation**17.96.2.3.1 uint32_t endAddr**

Memory region end address

Definition at line 154 of file `mpu_pal.h`.

17.96.2.3.2 void* extension

This field will be used to add extra settings to the basic region configuration

Definition at line 162 of file `mpu_pal.h`.

17.96.2.3.3 const mpu_master_access_permission_t* masterAccRight

Access permission for masters

Definition at line 155 of file `mpu_pal.h`.

17.96.2.3.4 uint8_t processIdEnable

Process identifier enable For MPU: the bit index corresponding with masters For SMPU: disable if equal zero, otherwise enable

Definition at line 156 of file mpu_pal.h.

17.96.2.3.5 uint8_t processIdentifier

Process identifier

Definition at line 159 of file mpu_pal.h.

17.96.2.3.6 uint8_t processIdMask

Process identifier mask. The setting bit will ignore the same bit in process identifier

Definition at line 160 of file mpu_pal.h.

17.96.2.3.7 uint32_t startAddr

Memory region start address

Definition at line 153 of file mpu_pal.h.

17.96.3 Typedef Documentation

17.96.3.1 typedef mpu_access_rights_t mpu_access_permission_t

MPU detail access permission For specific master:

Code	Supervisor	User	Description
MPU_SUPERVISOR_↔ RWX_USER_NONE	r w x	- - -	Allow Read, write, execute in supervisor mode; no access in user mode
MPU_SUPERVISOR_↔ RWX_USER_X	r w x	- - x	Allow Read, write, execute in supervisor mode; execute in user mode
MPU_SUPERVISOR_↔ RWX_USER_W	r w x	- w -	Allow Read, write, execute in supervisor mode; write in user mode
MPU_SUPERVISOR_↔ RWX_USER_WX	r w x	- w x	Allow Read, write, execute in supervisor mode; write and execute in user mode
MPU_SUPERVISOR_↔ RWX_USER_R	r w x	r - -	Allow Read, write, execute in supervisor mode; read in user mode
MPU_SUPERVISOR_↔ RWX_USER_RX	r w x	r - x	Allow Read, write, execute in supervisor mode; read and execute in user mode
MPU_SUPERVISOR_↔ RWX_USER_RW	r w x	r w -	Allow Read, write, execute in supervisor mode; read and write in user mode

MPU_SUPERVISOR_↔ RWX_USER_RWX	r w x	r w x	Allow Read, write, execute in supervisor mode; read, write and execute in user mode
MPU_SUPERVISOR_↔ RX_USER_NONE	r - x	- - -	Allow Read, execute in supervisor mode; no access in user mode
MPU_SUPERVISOR_↔ RX_USER_X	r - x	- - x	Allow Read, execute in supervisor mode; execute in user mode
MPU_SUPERVISOR_↔ RX_USER_W	r - x	- w -	Allow Read, execute in supervisor mode; write in user mode
MPU_SUPERVISOR_↔ RX_USER_WX	r - x	- w x	Allow Read, execute in supervisor mode; write and execute in user mode
MPU_SUPERVISOR_↔ RX_USER_R	r - x	r - -	Allow Read, execute in supervisor mode; read in user mode
MPU_SUPERVISOR_↔ RX_USER_RX	r - x	r - x	Allow Read, execute in supervisor mode; read and execute in user mode
MPU_SUPERVISOR_↔ RX_USER_RW	r - x	r w -	Allow Read, execute in supervisor mode; read and write in user mode
MPU_SUPERVISOR_↔ RX_USER_RWX	r - x	r w x	Allow Read, execute in supervisor mode; read, write and execute in user mode
MPU_SUPERVISOR_↔ RW_USER_NONE	r w -	- - -	Allow Read, write in supervisor mode; no access in user mode
MPU_SUPERVISOR_↔ RW_USER_X	r w -	- - x	Allow Read, write in supervisor mode; execute in user mode
MPU_SUPERVISOR_↔ RW_USER_W	r w -	- w -	Allow Read, write in supervisor mode; write in user mode
MPU_SUPERVISOR_↔ RW_USER_WX	r w -	- w x	Allow Read, write in supervisor mode; write and execute in user mode
MPU_SUPERVISOR_↔ RW_USER_R	r w -	r - -	Allow Read, write in supervisor mode; read in user mode
MPU_SUPERVISOR_↔ RW_USER_RX	r w -	r - x	Allow Read, write in supervisor mode; read and execute in user mode

MPU_SUPERVISOR_↔ RW_USER_RW	r w -	r w -	Allow Read, write in supervisor mode; read and write in user mode
MPU_SUPERVISOR_↔ RW_USER_RWX	r w -	r w x	Allow Read, write in supervisor mode; read, write and execute in user mode
MPU_SUPERVISOR_↔ USER_NONE	- - -	- - -	No access allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_X	- - x	- - x	Execute operation is allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_W	- w -	- w -	Write operation is allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_WX	- w x	- w x	Write and execute operations are allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_R	r - -	r - -	Read operation is allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_RX	r - x	r - x	Read and execute operations are allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_RW	r w -	r w -	Read and write operations are allowed in user and supervisor modes
MPU_SUPERVISOR_↔ USER_RWX	r w x	r w x	Read write and execute operations are allowed in user and supervisor modes

For normal master:

Code	Read/Write permission	Description
MPU_NONE	- -	No Read/Write access permission
MPU_W	- w	Write access permission
MPU_R	r -	Read access permission
MPU_RW	r w	Read/Write access permission

Implements : mpu_access_permission_t_Class

Definition at line 126 of file mpu_pal.h.

17.96.4 Enumeration Type Documentation

17.96.4.1 enum mpu_error_access_type_t

MPU access error Implements : mpu_error_access_type_t_Class.

Enumerator

MPU_ERROR_TYPE_READ Error type: read

MPU_ERROR_TYPE_WRITE Error type: write

Definition at line 45 of file mpu_pal.h.

17.96.4.2 enum mpu_error_attributes_t

MPU access error attributes Implements : mpu_error_attributes_t_Class.

Enumerator

- MPU_ERROR_USER_MODE_INSTRUCTION_ACCESS** Instruction access error in user mode
- MPU_ERROR_USER_MODE_DATA_ACCESS** Data access error in user mode
- MPU_ERROR_SUPERVISOR_MODE_INSTRUCTION_ACCESS** Instruction access error in supervisor mode
- MPU_ERROR_SUPERVISOR_MODE_DATA_ACCESS** Data access error in supervisor mode

Definition at line 55 of file mpu_pal.h.

17.96.4.3 enum mpu_inst_type_t

Enumeration with the types of peripherals supported by MPU PAL.

This enumeration contains the types of peripherals supported by MPU PAL. Implements : mpu_inst_type_t_Class

Definition at line 51 of file mpu_pal_mapping.h.

17.96.5 Function Documentation

17.96.5.1 status_t MPU_Deinit (const mpu_instance_t *const instance)

De-initializes memory protection unit by resetting all regions and masters to default and disable module.

Parameters

in	instance	The pointer to MPU instance number.
----	----------	-------------------------------------

Returns

operation status

- STATUS_SUCCESS : Operation was successful.
- STATUS_ERROR : Operation failed due to the region was locked by another master or all masters are locked.
- STATUS_UNSUPPORTED : Operation was unsupported.

Definition at line 276 of file mpu_pal.c.

17.96.5.2 status_t MPU_EnableRegion (const mpu_instance_t *const instance, uint8_t regionNum, bool enable)

Enables or disables an exist region configuration.

Parameters

in	instance	The pointer to MPU instance number.
in	regionNum	The region number.
in	enable	Valid state <ul style="list-style-type: none"> • true : Enable region. • false : Disable region.

Returns

operation status

- STATUS_SUCCESS : Operation was successful.
- STATUS_ERROR : Operation failed due to the region was locked by another master or all masters are locked.
- STATUS_UNSUPPORTED : Operation was unsupported.

Definition at line 425 of file mpu_pal.c.

17.96.5.3 `status_t MPU_GetDefaultRegionConfig (const mpu_instance_t *const instance, mpu_↔
master_access_permission_t * masterAccRight, mpu_region_config_t * regionConfig
)`

Gets default region configuration. Grants all access rights for masters; disable PID and cache; unlock region descriptor.

Parameters

in	<i>instance</i>	The pointer to MPU instance number.
out	<i>masterAccRight</i>	The pointer to master configuration structure, see mpu_master_access_↔ permission_t . The length of array should be defined by number of masters supported by hardware.
out	<i>regionConfig</i>	The pointer to default region configuration structure, see mpu_region_config_↔ _t .

Returns

operation status

- STATUS_SUCCESS : Operation was successful.
- STATUS_UNSUPPORTED : Operation was unsupported.

Definition at line 311 of file mpu_pal.c.

17.96.5.4 `bool MPU_GetError (const mpu_instance_t *const instance, uint8_t channel, mpu_error_info_t * errPtr)`

Checks and gets the access error detail information then clear error flag if the error caused by a master.

Parameters

in	<i>instance</i>	The pointer to MPU instance number.
in	<i>channel</i>	The error capture channel For MPU: corresponding with the slave port number For SMPU: corresponding with the the master number
out	<i>errPtr</i>	The pointer to access error info structure, see mpu_error_info_t .

Returns

operation status

- true : An error has occurred.
- false : No error has occurred or the operation was unsupported.

Definition at line 462 of file mpu_pal.c.

17.96.5.5 `status_t MPU_Init (const mpu_instance_t *const instance, uint8_t regionCnt, const mpu_region_config_t *
configPtr)`

Initializes memory protection unit by allocating regions and granting access rights for masters.

Parameters

in	<i>instance</i>	The pointer to MPU instance number.
in	<i>regionCnt</i>	The number of regions configured.
in	<i>configPtr</i>	The pointer to regions configuration structure, see mpu_region_config_t .

Returns

operation status

- STATUS_SUCCESS : Operation was successful.
- STATUS_ERROR : Operation failed due to invalid master number or the region was locked by another master or all masters are locked.
- STATUS_UNSUPPORTED : Operation was unsupported.

Definition at line 213 of file mpu_pal.c.

17.96.5.6 `status_t MPU_UpdateRegion (const mpu_instance_t *const instance, uint8_t regionNum, const mpu_region_config_t * configPtr)`

Updates region configuration.

Parameters

in	<i>instance</i>	The pointer to MPU instance number.
in	<i>regionNum</i>	The region number.
in	<i>configPtr</i>	The pointer to region configuration structure, see mpu_region_config_t .

Returns

operation status

- STATUS_SUCCESS : Operation was successful.
- STATUS_ERROR : Operation failed due to invalid master number or the region was locked by another master or all masters are locked.
- STATUS_UNSUPPORTED : Operation was unsupported.

Definition at line 380 of file mpu_pal.c.

17.97 MX25L6433F Serial Flash Driver

17.97.1 Detailed Description

Driver for the Macronix MX25L6433F Serial Flash.

The MX25L6433F Serial Flash Driver offers specific support for the Macronix MX25L6433F Serial Flash. It runs on top of the QuadSPI driver and adds device-specific features.

Functionality

Initialization

The QuadSPI driver must be initialized by the application prior to initializing the flash_mx25l6433f driver, by calling `QSPI_DRV_Init()`. Then the flash_mx25l6433f driver is initialized by calling `FLASH_MX25L6433F_DRV_Init()`. The `FLASH_MX25L6433F_DRV_Init()` function initializes the driver and ensures that the serial device is properly configured for operation, launching QuadSPI commands to change the device settings if necessary. After the call of this function the driver is available for read/write/erase operations on the serial flash device.

Read operations

Read operations are asynchronous, the function `FLASH_MX25L6433F_DRV_Read` starts the read operations and then immediately returns, leaving the QuadSPI module to handle the rest of the operation. The callback offered by the QuadSPI driver may be used to signal the end of the operation to the application, or `FLASH_MX25L6433F_DRV_GetStatus()` can be called to check the operation status.

The read operations can be performed in dma mode, if DMA was enabled at initialization time, or in interrupt mode.

Write operations

Write operations are asynchronous, the function `FLASH_MX25L6433F_DRV_Program` starts the write operation and then immediately returns, leaving the QuadSPI module to handle the rest of the operation. The callback offered by the QuadSPI driver may be used to signal the end of the QuadSpi command to the application, however the write operations is still not completed in the serial flash device and `FLASH_MX25L6433F_DRV_GetStatus()` must be called to check the operation status. Only when `FLASH_MX25L6433F_DRV_GetStatus()` returns a code other than `STATUS_BUSY` the operation is completed and the driver can accept other commands.

The write operations can be performed in dma mode, if DMA was enabled at initialization time, or in interrupt mode.

Due to device limitations write operations are possible only inside a 256 bytes data page, with the start address aligned to 256 bytes. Bytes that exceed the end of the page will wrap to the beginning of the page.

Erase operations

Erase operations are asynchronous, the erase functions start the erase operation and then immediately return, leaving the QuadSPI module to handle the rest of the operation. There are 4 erase functions, one for each erase command supported by the device: `FLASH_MX25L6433F_DRV_Erase4K()`, `FLASH_MX25L6433F_DRV_Erase32K()`, `FLASH_MX25L6433F_DRV_Erase64K()` and `FLASH_MX25L6433F_DRV_EraseAll()`.

After the completion of an erase function, `FLASH_MX25L6433F_DRV_GetStatus()` must be periodically called to check the operation status. Only when `FLASH_MX25L6433F_DRV_GetStatus()` returns a code other than `STATUS_BUSY` the operation is completed and the driver can accept other commands.

Program Verify and Blank Check operations

Program Verify and Blank Check operations are asynchronous, the functions `FLASH_MX25L6433F_DRV_EraseVerify()` and `FLASH_MX25L6433F_DRV_ProgramVerify()` start the operation and then immediately return, leaving the QuadSPI module to handle the rest of the operation. These functions internally use the QuadSPI read feature, and can only function in interrupt mode, even if the driver uses DMA. The callback offered by the QuadSPI driver may be used to signal the end of the operation to the application, or `FLASH_MX25L6433F_DRV_GetStatus()` can be called to check the operation status.

Other operations

The driver also offers other functionalities, mapping to the other features of the module, like setting the write protection or entering the special One Time Program or Deep Power Down modes. Please check the description of the respective functions for more information.

Important Notes

- This driver relies on the services of the QuadSPI driver, so please observe the restrictions from the Important Notes section in the QuadSPI driver documentation.
- The following QuadSPI initialization settings must be used when using this driver, or else the driver may not be able to communicate with the device:
 - dataRate = QSPI_DATE_RATE_SDR;
 - readMode = QSPI_READ_MODE_INTERNAL_SAMPLING;
 - memSize = 0x7FFFFFFU;
 - csHoldTime = 1U;
 - csSetupTime = 1U;
 - columnAddr = 0U;
 - wordAddressable = false;
 - sampleDelay = QSPI_SAMPLE_DELAY_1;
 - clockPhase = QSPI_SAMPLE_PHASE_NON_INVERTED;
 - endianness = QSPI_END_64BIT_LE;
 - io2IdleValue = 1U;
 - io3IdleValue = 1U; If the configuration tool is used these settings will be enforced by the tool.

Code example

```
status_t status;
#define INSTANCE 0
#define BUFFER_SIZE 10
#define SECTOR_ADDR 0x1000U
uint8_t txBuffer[BUFFER_SIZE] = {0, 1, 2, 3, 4, 5, 6, 7, 8, 9};
uint8_t rxBuffer[BUFFER_SIZE];
/* QuadSPI configuration and state structures */
qspi_user_config_t qspiConfig;
qspi_state_t qspiState;
/* Serial flash configuration and state structures */
flash_mx25l6433f_user_config_t flashConfig = {
    .dmaSupport = false,
    .outputDriverStrength = FLASH_MX25L6433F_DRV_STRENGTH_LOW,
};
flash_mx25l6433f_state_t flashState;

/* Initialize QuadSPI driver */
status = QSPI_DRV_GetDefaultConfig(&qspiConfig);
status = QSPI_DRV_Init(INSTANCE, &qspiConfig, &qspiState);
/* Initialize serial flash driver */
status = FLASH_MX25L6433F_DRV_Init(INSTANCE, &flashConfig, &flashState);

/* erase one sector */
status = FLASH_MX25L6433F_DRV_Erase4K(INSTANCE, SECTOR_ADDR);
while ((status = FLASH_MX25L6433F_DRV_GetStatus(INSTANCE)) == STATUS_BUSY);

/* program BUFFER_SIZE bytes */
FLASH_MX25L6433F_DRV_Program(INSTANCE, SECTOR_ADDR, txBuffer, BUFFER_SIZE);
while ((status = FLASH_MX25L6433F_DRV_GetStatus(INSTANCE)) == STATUS_BUSY);

/* read BUFFER_SIZE bytes */
FLASH_MX25L6433F_DRV_Read(INSTANCE, SECTOR_ADDR, rxBuffer, BUFFER_SIZE);
while ((status = FLASH_MX25L6433F_DRV_GetStatus(INSTANCE)) == STATUS_BUSY);

/* Deinit drivers */
status = FLASH_MX25L6433F_DRV_Deinit(INSTANCE);
status = QSPI_DRV_Deinit(INSTANCE);
```

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\drivers\src\flash_mx25l6433f\flash_mx25l6433f_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\drivers\inc
{S32SDK_PATH}\platform\drivers\src\flash_mx25l6433f
```

Compile symbols

No special symbols are required for this component

Dependencies

Quad Serial Peripheral Interface (QuadSPI)

Data Structures

- struct [flash_mx25l6433f_user_config_t](#)
Driver configuration structure. [More...](#)
- struct [flash_mx25l6433f_state_t](#)
Driver internal context structure. [More...](#)
- struct [flash_mx25l6433f_secure_lock_t](#)
Flash protection settings Implements : [flash_mx25l6433f_secure_lock_t](#) Class. [More...](#)

Enumerations

- enum [flash_mx25l6433f_prot_dir_t](#) { [FLASH_MX25L6433F_PROT_DIR_TOP](#) = 0x00U, [FLASH_MX25L6433F_PROT_DIR_BOTTOM](#) = 0x01U }
Flash protection direction Implements : [flash_mx25l6433f_prot_dir_t](#) Class.
- enum [flash_mx25l6433f_drv_strength_t](#) { [FLASH_MX25L6433F_DRV_STRENGTH_HIGH](#) = 0x00U, [FLASH_MX25L6433F_DRV_STRENGTH_LOW](#) = 0x01U }
Flash device drive strength Implements : [flash_mx25l6433f_drv_strength_t](#) Class.
- enum [flash_mx25l6433f_prot_size_t](#) {
[FLASH_MX25L6433F_PROT_SIZE_0](#) = 0x00U, [FLASH_MX25L6433F_PROT_SIZE_64K](#) = 0x01U, [FLASH_MX25L6433F_PROT_SIZE_128K](#) = 0x02U, [FLASH_MX25L6433F_PROT_SIZE_256K](#) = 0x03U,
[FLASH_MX25L6433F_PROT_SIZE_512K](#) = 0x04U, [FLASH_MX25L6433F_PROT_SIZE_1M](#) = 0x05U, [FLASH_MX25L6433F_PROT_SIZE_2M](#) = 0x06U, [FLASH_MX25L6433F_PROT_SIZE_4M](#) = 0x07U,
[FLASH_MX25L6433F_PROT_SIZE_8M](#) = 0x08U }
Size of flash protected area Implements : [flash_mx25l6433f_prot_size_t](#) Class.

FLASH_MX25L6433F Driver

- status_t [FLASH_MX25L6433F_DRV_Init](#) (uint32_t instance, const [flash_mx25l6433f_user_config_t](#) *userConfigPtr, [flash_mx25l6433f_state_t](#) *state)
Initializes the serial flash memory driver.
- status_t [FLASH_MX25L6433F_DRV_Deinit](#) (uint32_t instance)
De-initialize the MX25L6433F flash driver.

- status_t [FLASH_MX25L6433F_DRV_SetProtection](#) (uint32_t instance, [flash_mx25l6433f_prot_dir_t](#) direction, [flash_mx25l6433f_prot_size_t](#) size)
Configure protected area of the device.
- status_t [FLASH_MX25L6433F_DRV_GetProtection](#) (uint32_t instance, [flash_mx25l6433f_prot_dir_t](#) *direction, [flash_mx25l6433f_prot_size_t](#) *size)
Get protected area of the device.
- status_t [FLASH_MX25L6433F_DRV_SetSecureLock](#) (uint32_t instance)
Locks the customer sector of the secured OTP area.
- status_t [FLASH_MX25L6433F_DRV_GetSecureLock](#) (uint32_t instance, [flash_mx25l6433f_secure_lock_t](#) *lock)
Get lock status of the secured OTP area.
- status_t [FLASH_MX25L6433F_DRV_Read](#) (uint32_t instance, uint32_t address, uint8_t *data, uint32_t size)
Read data from serial flash.
- status_t [FLASH_MX25L6433F_DRV_Erase4K](#) (uint32_t instance, uint32_t address)
Erase a 4k sector in the serial flash.
- status_t [FLASH_MX25L6433F_DRV_Erase32K](#) (uint32_t instance, uint32_t address)
Erase a 32k block in the serial flash.
- status_t [FLASH_MX25L6433F_DRV_Erase64K](#) (uint32_t instance, uint32_t address)
Erase a 64k block in the serial flash.
- status_t [FLASH_MX25L6433F_DRV_EraseAll](#) (uint32_t instance)
Erases the entire serial flash.
- status_t [FLASH_MX25L6433F_DRV_EraseVerify](#) (uint32_t instance, uint32_t address, uint32_t size)
Checks whether or not an area in the serial flash is erased.
- status_t [FLASH_MX25L6433F_DRV_Program](#) (uint32_t instance, uint32_t address, const uint8_t *data, uint32_t size)
Writes data in serial flash.
- status_t [FLASH_MX25L6433F_DRV_ProgramVerify](#) (uint32_t instance, uint32_t address, const uint8_t *data, uint32_t size)
Verifies the correctness of the programmed data.
- status_t [FLASH_MX25L6433F_DRV_GetStatus](#) (uint32_t instance)
Get the status of the last operation.
- status_t [FLASH_MX25L6433F_DRV_Reset](#) (uint32_t instance)
Reset the serial flash device.
- status_t [FLASH_MX25L6433F_DRV_EnterOTP](#) (uint32_t instance)
Enters OTP mode.
- status_t [FLASH_MX25L6433F_DRV_ExitOTP](#) (uint32_t instance)
Exits OTP mode.
- status_t [FLASH_MX25L6433F_DRV_EnterDPD](#) (uint32_t instance)
Enters Deep Power Down mode.
- status_t [FLASH_MX25L6433F_DRV_ExitDPD](#) (uint32_t instance)
Exits Deep Power Down mode.
- status_t [FLASH_MX25L6433F_DRV_Suspend](#) (uint32_t instance)
Suspends current program or erase operation.
- status_t [FLASH_MX25L6433F_DRV_Resume](#) (uint32_t instance)
Resume a suspended program or erase operation.
- void [FLASH_MX25L6433F_DRV_GetDefaultConfig](#) ([flash_mx25l6433f_user_config_t](#) *userConfigPtr)
Returns default configuration structure for FLASH_MX25L6433F.

17.97.2 Data Structure Documentation

17.97.2.1 struct flash_mx25l6433f_user_config_t

Driver configuration structure.

This structure is used to provide configuration parameters for the mx25l6433f flash driver at initialization time.

Implements : flash_mx25l6433f_user_config_t_Class

Definition at line 82 of file flash_mx25l6433f_driver.h.

Data Fields

- bool [dmaSupport](#)
- [flash_mx25l6433f_drv_strength_t](#) outputDriverStrength

Field Documentation

17.97.2.1.1 bool dmaSupport

Enables DMA support in the driver

Definition at line 84 of file flash_mx25l6433f_driver.h.

17.97.2.1.2 flash_mx25l6433f_drv_strength_t outputDriverStrength

Output driver level of the device

Definition at line 85 of file flash_mx25l6433f_driver.h.

17.97.2.2 struct flash_mx25l6433f_state_t

Driver internal context structure.

This structure is used by the driver for its internal logic. It must be provided by the application through the [FLASH_MX25L6433F_DRV_Init\(\)](#) function, then it cannot be freed until the driver is de-initialized using [FLASH_MX25L6433F_DRV_Deinit\(\)](#). The application should make no assumptions about the content of this structure.

Definition at line 97 of file flash_mx25l6433f_driver.h.

17.97.2.3 struct flash_mx25l6433f_secure_lock_t

Flash protection settings Implements : flash_mx25l6433f_secure_lock_t_Class.

Definition at line 112 of file flash_mx25l6433f_driver.h.

Data Fields

- bool [userAreaLock](#)
- bool [factoryAreaLock](#)

Field Documentation

17.97.2.3.1 bool factoryAreaLock

Factory secured area (2nd 4KB region) is locked.

Definition at line 115 of file flash_mx25l6433f_driver.h.

17.97.2.3.2 bool userAreaLock

User secured area (1st 4KB region) is locked.

Definition at line 114 of file flash_mx25l6433f_driver.h.

17.97.3 Enumeration Type Documentation

17.97.3.1 enum flash_mx25l6433f_drv_strength_t

Flash device drive strength Implements : flash_mx25l6433f_drv_strength_t_Class.

Enumerator

FLASH_MX25L6433F_DRV_STRENGTH_HIGH Full driver strength.

FLASH_MX25L6433F_DRV_STRENGTH_LOW Low (1/4) driver strength.

Definition at line 47 of file flash_mx25l6433f_driver.h.

17.97.3.2 enum flash_mx25l6433f_prot_dir_t

Flash protection direction Implements : flash_mx25l6433f_prot_dir_t_Class.

Enumerator

FLASH_MX25L6433F_PROT_DIR_TOP Top flash area protected.

FLASH_MX25L6433F_PROT_DIR_BOTTOM Bottom flash area protected.

Definition at line 37 of file flash_mx25l6433f_driver.h.

17.97.3.3 enum flash_mx25l6433f_prot_size_t

Size of flash protected area Implements : flash_mx25l6433f_prot_size_t_Class.

Enumerator

FLASH_MX25L6433F_PROT_SIZE_0 Entire flash unprotected.

FLASH_MX25L6433F_PROT_SIZE_64K 64k flash area protected.

FLASH_MX25L6433F_PROT_SIZE_128K 128k flash area protected.

FLASH_MX25L6433F_PROT_SIZE_256K 256k flash area protected.

FLASH_MX25L6433F_PROT_SIZE_512K 512k flash area protected.

FLASH_MX25L6433F_PROT_SIZE_1M 1M flash area protected.

FLASH_MX25L6433F_PROT_SIZE_2M 2M flash area protected.

FLASH_MX25L6433F_PROT_SIZE_4M 4M flash area protected.

FLASH_MX25L6433F_PROT_SIZE_8M Entire flash area protected.

Definition at line 57 of file flash_mx25l6433f_driver.h.

17.97.4 Function Documentation

17.97.4.1 status_t FLASH_MX25L6433F_DRV_Deinit (uint32_t instance)

De-initialize the MX25L6433F flash driver.

This function de-initializes the MX25L6433F flash driver. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

Returns

Error or success status returned by API

Definition at line 500 of file flash_mx25l6433f_driver.c.

17.97.4.2 status_t FLASH_MX25L6433F_DRV_EnterDPD (uint32_t *instance*)

Enters Deep Power Down mode.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

Returns

Error or success status returned by API

Definition at line 1005 of file flash_mx25l6433f_driver.c.

17.97.4.3 status_t FLASH_MX25L6433F_DRV_EnterOTP (uint32_t *instance*)

Enters OTP mode.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

Returns

Error or success status returned by API

Definition at line 957 of file flash_mx25l6433f_driver.c.

17.97.4.4 status_t FLASH_MX25L6433F_DRV_Erase32K (uint32_t *instance*, uint32_t *address*)

Erase a 32k block in the serial flash.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
<i>address</i>	Address of block to be erased

Returns

Error or success status returned by API

Definition at line 712 of file flash_mx25l6433f_driver.c.

17.97.4.5 status_t FLASH_MX25L6433F_DRV_Erase4K (uint32_t *instance*, uint32_t *address*)

Erase a 4k sector in the serial flash.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

<i>address</i>	Address of sector to be erased
----------------	--------------------------------

Returns

Error or success status returned by API

Definition at line 685 of file flash_mx25l6433f_driver.c.

17.97.4.6 status_t FLASH_MX25L6433F_DRV_Erase64K (uint32_t *instance*, uint32_t *address*)

Erase a 64k block in the serial flash.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
<i>address</i>	Address of block to be erased

Returns

Error or success status returned by API

Definition at line 739 of file flash_mx25l6433f_driver.c.

17.97.4.7 status_t FLASH_MX25L6433F_DRV_EraseAll (uint32_t *instance*)

Erases the entire serial flash.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

Returns

Error or success status returned by API

Definition at line 766 of file flash_mx25l6433f_driver.c.

17.97.4.8 status_t FLASH_MX25L6433F_DRV_EraseVerify (uint32_t *instance*, uint32_t *address*, uint32_t *size*)

Checks whether or not an area in the serial flash is erased.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
<i>address</i>	Start address of area to be verified
<i>size</i>	Size of area to be verified

Returns

Error or success status returned by API

Definition at line 793 of file flash_mx25l6433f_driver.c.

17.97.4.9 status_t FLASH_MX25L6433F_DRV_ExitDPD (uint32_t *instance*)

Exits Deep Power Down mode.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

Returns

Error or success status returned by API

Definition at line 1029 of file flash_mx25l6433f_driver.c.

17.97.4.10 `status_t FLASH_MX25L6433F_DRV_ExitOTP (uint32_t instance)`

Exits OTP mode.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

Returns

Error or success status returned by API

Definition at line 981 of file flash_mx25l6433f_driver.c.

17.97.4.11 `void FLASH_MX25L6433F_DRV_GetDefaultConfig (flash_mx25l6433f_user_config_t * userConfigPtr)`

Returns default configuration structure for FLASH_MX25L6433F.

Parameters

<i>userConfigPtr</i>	Pointer to the FLASH_MX25L6433F user configuration structure.
----------------------	---

Definition at line 1103 of file flash_mx25l6433f_driver.c.

17.97.4.12 `status_t FLASH_MX25L6433F_DRV_GetProtection (uint32_t instance, flash_mx25l6433f_prot_dir_t * direction, flash_mx25l6433f_prot_size_t * size)`

Get protected area of the device.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
<i>direction</i>	Location of protected area (top or bottom)
<i>size</i>	Size of protected area

Returns

Error or success status returned by API

Definition at line 552 of file flash_mx25l6433f_driver.c.

17.97.4.13 `status_t FLASH_MX25L6433F_DRV_GetSecureLock (uint32_t instance, flash_mx25l6433f_secure_lock_t * lock)`

Get lock status of the secured OTP area.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

<i>lock</i>	Lock status of the secured OTP area
-------------	-------------------------------------

Returns

Error or success status returned by API

Definition at line 623 of file flash_mx25l6433f_driver.c.

17.97.4.14 `status_t FLASH_MX25L6433F_DRV_GetStatus (uint32_t instance)`

Get the status of the last operation.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

Returns

Error or success status returned by API

Definition at line 881 of file flash_mx25l6433f_driver.c.

17.97.4.15 `status_t FLASH_MX25L6433F_DRV_Init (uint32_t instance, const flash_mx25l6433f_user_config_t * userConfigPtr, flash_mx25l6433f_state_t * state)`

Initializes the serial flash memory driver.

This function initializes the MX25L6433F flash driver and prepares it for operation.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
<i>userConfigPtr</i>	Pointer to the MX25L6433F flash driver user configuration structure. The function reads configuration data from this structure and initializes the driver accordingly. The application may free this structure after the function returns.
<i>master</i>	Pointer to the MX25L6433F flash driver context structure. The driver uses this memory area for its internal logic. The application must make no assumptions about the content of this structure, and must not free this memory until the driver is de-initialized using FLASH_MX25L6433F_DRV_Deinit() .

Returns

Error or success status returned by API

Definition at line 460 of file flash_mx25l6433f_driver.c.

17.97.4.16 `status_t FLASH_MX25L6433F_DRV_Program (uint32_t instance, uint32_t address, const uint8_t * data, uint32_t size)`

Writes data in serial flash.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
<i>address</i>	Start address of area to be programmed
<i>data</i>	Data to be programmed in flash

<i>size</i>	Size of data buffer
-------------	---------------------

Returns

Error or success status returned by API

Definition at line 816 of file flash_mx25l6433f_driver.c.

17.97.4.17 `status_t FLASH_MX25L6433F_DRV_ProgramVerify (uint32_t instance, uint32_t address, const uint8_t * data, uint32_t size)`

Verifies the correctness of the programmed data.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
<i>address</i>	Start address of area to be verified
<i>data</i>	Data to be verified
<i>size</i>	Size of data buffer

Returns

Error or success status returned by API

Definition at line 855 of file flash_mx25l6433f_driver.c.

17.97.4.18 `status_t FLASH_MX25L6433F_DRV_Read (uint32_t instance, uint32_t address, uint8_t * data, uint32_t size)`

Read data from serial flash.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
<i>address</i>	Start address for read operation
<i>data</i>	Buffer where to store read data
<i>size</i>	Size of data buffer

Returns

Error or success status returned by API

Definition at line 653 of file flash_mx25l6433f_driver.c.

17.97.4.19 `status_t FLASH_MX25L6433F_DRV_Reset (uint32_t instance)`

Reset the serial flash device.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

Returns

Error or success status returned by API

Definition at line 925 of file flash_mx25l6433f_driver.c.

17.97.4.20 `status_t FLASH_MX25L6433F_DRV_Resume (uint32_t instance)`

Resume a suspended program or erase operation.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

Returns

Error or success status returned by API

Definition at line 1079 of file flash_mx25l6433f_driver.c.

17.97.4.21 `status_t FLASH_MX25L6433F_DRV_SetProtection (uint32_t instance, flash_mx25l6433f_prot_dir_t direction, flash_mx25l6433f_prot_size_t size)`

Configure protected area of the device.

This function configures the size and location (top or bottom) of protected area. Note that due to device limitations, once the protected area is set to BOTTOM it cannot be changed back (the setting is "one time program")

Parameters

<i>instance</i>	QuadSPI peripheral instance number
<i>direction</i>	Location of protected area (top or bottom)
<i>size</i>	Size of protected area

Returns

Error or success status returned by API

Definition at line 516 of file flash_mx25l6433f_driver.c.

17.97.4.22 `status_t FLASH_MX25L6433F_DRV_SetSecureLock (uint32_t instance)`

Locks the customer sector of the secured OTP area.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

Returns

Error or success status returned by API

Definition at line 594 of file flash_mx25l6433f_driver.c.

17.97.4.23 `status_t FLASH_MX25L6433F_DRV_Suspend (uint32_t instance)`

Suspends current program or erase operation.

Parameters

<i>instance</i>	QuadSPI peripheral instance number
-----------------	------------------------------------

Returns

Error or success status returned by API

Definition at line 1053 of file flash_mx25l6433f_driver.c.

17.98 Memory Protection Unit (MPU)

17.98.1 Detailed Description

The S32 SDK provides Peripheral Driver for the Memory Protection Unit (MPU) module of S32 SDK devices.

The memory protection unit (MPU) provides hardware access control for all memory references generated in the device.

Hardware background

The MPU concurrently monitors all system bus transactions and evaluates their appropriateness using pre-programmed region descriptors that define memory spaces and their access rights. Memory references that have sufficient access control rights are allowed to complete, while references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU implements a two-dimensional hardware array of memory region descriptors and the crossbar slave ports to continuously monitor the legality of every memory reference generated by each bus master in the system.

The feature set includes:

- 8(16 for S32K148) program-visible 128-bit region descriptors, accessible by four 32-bit words each
 - Each region descriptor defines a modulo-32 byte space, aligned anywhere in memory
 - * Region sizes can vary from 32 bytes to 4 Gbytes
 - Two access control permissions defined in a single descriptor word
 - * Masters 0–3: read, write, and execute attributes for supervisor and user accesses
 - * Masters 4–7: read and write attributes
 - Hardware-assisted maintenance of the descriptor valid bit minimizes coherency issues
 - Alternate programming model view of the access control permissions word
 - Priority given to granting permission over denying access for overlapping region descriptors
- Detects access protection errors if a memory reference does not hit in any memory region, or if the reference is illegal in all hit memory regions. If an access error occurs, the reference is terminated with an error response, and the MPU inhibits the bus cycle being sent to the targeted slave device.
- Error registers, per slave port, capture the last faulting address, attributes, and other information
- Global MPU enable/disable control bit

Logical Bus Master Assignments and Possible Access Types

ID	Master	User	Super-visor	Data	Instruc-tion	Read	Write	Exe-cute	PID
0	Core	x	x	x	x	x	x	x	x
1	Debug-ger	x	x	x	x	x	x	x	x
2	DMA		x	x		x	x		
3	ENET	x		x		x	x		

ID	S32K1xx	S32MTV	S32K1xxW
0	x	x	x
1	x	x	x
2	x	x	x
3	x(1)		x(1)

1: S32K148 only.

Logical Slave Port Assignments

Port	Source	Destination
0	Crossbar slave port 0	Flash Controller
1	Crossbar slave port 1	SRAM backdoor
2	Code Bus	SRAM_L frontdoor
3	System Bus	SRAM_U frontdoor
4	Crossbar slave port 3	QuadSPI

Port	S32K11x	S32K14x	S32MTV	S32K1xxW
0	x	x	x	x
1	x(1)	x	x	x
2		x	x	x
3		x	x	x
4		x(2)		x(2)

1: Destination: SRAM controller/MTB/DWT/MCM. 2: S32K148 only.

AHB-AP

AHB-AP provides the debugger access to all memory and registers in the system.

The MPU includes default settings and protections for the Region Descriptor 0 (RGD0) such that the Debugger always has access to the entire address space and those rights cannot be changed by the core or any other bus master.

ERRATA

- S32K148:
 - E11109: The MPU requires a special programming sequence to protect the QSPI space as it is unable to see the two MSB bits of the QSPI address on slave port 4.
This programming sequence requires 2 Region Descriptors [RGDx]:
 - * One will cover the region 0x280x_xxxx and the other one will cover region 0x680x_xxxx.
 - * When any master without permissions tries to access region 0x680x_xxxx, an error will be captured in both, EDR3 and EDR4 registers. Moreover, the address of the failed access is captured on EAR3 and EAR4 registers. However, EAR3 will capture the address 0x680x_xxxx, which is the one that belongs to the QSPI space. While EAR4 will capture the 0x280x_xxxx address.

Note

- S32K14x, S32K14xW:
 - In order to protect cache data, AHB LMEM will distribute all transactions to MPU slave port 2 for any access to the whole cacheable code bus memory domain.
 - * If there is a Pflash access protection error by CM4, both slave port 0 & slave port 2 will report the same error.

Modules

- [MPU Driver](#)
Memory Protection Unit Peripheral Driver.

17.99 Memory Protection Unit Peripheral Abstraction Layer (MPU PAL)

17.99.1 Detailed Description

The S32 SDK provides a Peripheral Abstraction Layer for Memory Protection Unit (MPU) modules of S32 SDK devices.

The MPU PAL driver provides memory protection functionality via allocate regions and restrict access rights of all masters on the region. It was designed to be portable across all platforms and IPs which support Memory Protection Unit.

Integration guideline

Unlike the other drivers, MPU PAL modules need to include a configuration file named `mpu_pal_cfg.h`, which allows the user to specify which IPs are used and how many resources are allocated for each of them (state structures). The following code example shows how to configure one instance for each available MPU IPs.

```
#ifndef MPU_PAL_CFG_H
#define MPU_PAL_CFG_H

/* Define which IP instance which supported on this device */
#define MPU_OVER_MPU
#define MPU_OVER_SMPU

#endif /* MPU_PAL_CFG_H */
```

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\pal\src\mpu\mpu_pal.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\pal\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Memory Protection Unit \(MPU\)](#) smpu

IPs specification

The following tables contains IPs specification on platforms:

- Available

IP/MCU	S32K1xx	MPC574x	S32Rx7x
MPU	x		
SMPU		x	x

- Number of supported instances

IP/MCU	S32K1xx	MPC574x	S32Rx7x
MPU	1	–	–
SMPU	–	1(1)	2

1: 2 instances with MPC5747C, MPC5748C, MPC5746G, MPC5747G and MPC5748G.

SMPU instance	MPC574x	S32Rx7x
0	Flash and peripherals	Data XBAR (XBAR_0)
1	RAM	instruction XBAR (XBAR_1)

MPC574x: The cores on the device treats the following memory region as guarded by default:

- Guarded Region0: Address 0xFC00_0000 to 0xFFFF_FFFF
- Guarded Region1: Address 0xF800_0000 to 0xFBFF_FFFF

- Number of supported regions

IP/MCU	S32K1xx	MPC574x	S32Rx7x
MPU	8(1)	–	–
SMPU	–	16	16

1: 16 regions with S32K148.

Note

- S32K14x, S32K14xW:
 - In order to protect cache data, AHB LMEM will distribute all transactions to MPU slave port 2 for any access to the whole cacheable code bus memory domain.
 - * If there is a Pflash access protection error by CM4, both slave port 0 & slave port 2 will report the same error.

Initialization & De-initialization

- In order to use the MPU PAL driver it must be first initialized, using [MPU_Init\(\)](#) function to initialize or re-initialize module.
- Example:

1. Definitions for MPU IP (MPU_OVER_MPU)

```

/* Define MPU PAL instance */
mpu_instance_t mpu_pal_Instance =
{
    .instType = MPU_INST_TYPE_MPU, /* MPU PAL over MPU */
    .instIdx  = 0U                 /* MPU instance 0 */
}

/* Define number of masters supported by platform */
#define MPU_PAL_MASTER_COUNT (16U)

/* Define number of used regions (should be in range supported by platform) */
#define MPU_PAL_REGION_COUNT (1U)

/* Status variable */
status_t status;

```

2. Region configuration

```

/* Master configuration */
mpu_master_access_permission_t mpu_pal_masterAccRight[MPU_PAL_MASTER_COUNT] =
{
    /* Master */
    {
        .masterNum = FEATURE_MPU_MASTER_CORE, /* Core */
        .accessRight = MPU_ACCESS_SUPERVISOR_RWX_USER_RWX /* Access right: read, write and execute
                                                             for both supervisor and user mode */
    },
    /* Define the rest masters here */
    ...
};

/* Region configuration */
mpu_region_config_t mpu_pal_regionConfigs[MPU_PAL_REGION_COUNT] =
{
    /* Region 0 */
    {
        .startAddr = 0U, /* Start address */
        .endAddr = 0xFFFFFFFU, /* End address */
    }
}

```

```

        .masterAccRight = mpu_pal_masterAccRight, /* Pointer to access right of all masters */
/* If support PID */
        .processIdEnable = 0x01U, /* 8'b00000001 Enable PID for logical master 0 (Core) */
        .processIdentifier = 0x00U, /* Process identifier */
        .processIdMask = 0xFFU, /* Process identifier mask */
/* End if */
/* Extension */
        .extension = NULL /* This field will be used to add extra settings
                           to the basic region configuration */
/* End extension */
    }
};

```

Or using MPU_GetDefaultConfig()

```

/* Master configuration */
mpu_master_access_permission_t mpu_pal_masterAccRight[MPU_PAL_MASTER_COUNT];
/* Region configuration */
mpu_region_config_t regionConfig0;

/* Get default region configuration */
status = MPU_GetDefaultConfig(&mpu_pal_Instance, mpu_pal_masterAccRight, &regionConfig0);
mpu_region_config_t mpu_pal_regionConfigs[MPU_PAL_REGION_COUNT] =
{
    regionConfig0
};

```

3. Initialization

```

/* Initializes MPU PAL */
status = MPU_Init(&mpu_pal_Instance, MPU_PAL_REGION_COUNT, mpu_pal_regionConfigs);

```

4. De-initialization

```

/* De-initializes MPU PAL */
status = MPU_Deinit(&mpu_pal_Instance);

```

Updates region configuration

- The MPU PAL driver provides a function named [MPU_UpdateRegion\(\)](#) to update a region configuration (address, access rights of all masters, process identifier,...).
- In order to remove unused region or add again, [MPU_EnableRegion\(\)](#) can be used.
- Please note the region will be unlocked if the update succeed.
- Example:

1. Modify (or add new) region after initialization

```

/* Disables process identifier functionality on region 0 */
regionConfig0.processIdEnable = 0x00U;

/* Updates region 0 */
status = MPU_UpdateRegion(&mpu_pal_Instance, 0U, &regionConfig0);

```

2. Enables/Disables an exist region configuration

```

/* Enables region 1 */
status = MPU_EnableRegion(&mpu_pal_Instance, 1U, true);

/* Disables region 2 */
status = MPU_EnableRegion(&mpu_pal_Instance, 2U, false);

```

Detects access protection errors

- The MPU PAL driver provides a function named [MPU_GetError\(\)](#) to detect an access protection error on error capture channel. The channel can be different among IPs.
- Example:

```

/* Define error variable */
mpu_error_info_t mpu_pal_errVal;

/* Gets information on channel 0 */
bool errStatus = MPU_GetError(&mpu_pal_Instance, 0U, &mpu_pal_errVal)

```

Other IP specific details

• **MPU** (MPU_OVER_MPU)

- Support PID for specific masters corresponding with the processIdEnable bit index.
- Detects an access error on slave ports:

Source	Slave port	Destination	S32K11x	S32K14x	S32MTV
Crossbar slave port 0	0	Flash Controller	x	x	x
Crossbar slave port 1	1	SRAM backdoor	x(1)	x	x
Code Bus	2	SRAM_L frontdoor		x	x
System Bus	3	SRAM_U frontdoor		x	x
Crossbar slave port 2	4	QuadSPI		x(2)	

1: Destination: SRAM controller/MTB/DWT/MCM.

2: S32K148 only.

• **SMPU** (MPU_OVER_SMPU)

- Support PID for for all specific masters (processIdEnable same as bool)
- Detects an access error on bus masters.
- Supports lock and cache inhibit features in region extension.
 - * An address range specified in an MPU region descriptor for a cacheable space (that is, CI = 0) must be defined with a starting address aligned on a 0-modulo-32 byte address and with a multiple of the 32 byte cache line size factoring into the end address.
- MPU_UpdateRegionLock() can be used to update lock configuration on a region.
- MPU_GetRegionLockInfo() can be used to get lock status on a region.
- Example:

1. Extension

```

/* E.g. MPC5748G */
/* SMPU region extension with normal access rights */
mpu_over_smpu_extension mpu_pal_extension =
{
    /* If specific access supported */
    .specAccessEnable = false, /* Use normal access rights */
    .specAccessSet = NULL, /* Specific access configuration
                             Only use when specific access enabled */

    /* End if */
    .cacheInhibitEnable = true, /* The region cannot be cached */
    .lockConfig = MPU_UNLOCK /* The region is unlocked */
}

/* Use specific access rights */
#define MPU_PAL_REGION_ACCESS_SET_COUNT 3U /* Support 3 configurations on each region */
mpu_specific_access_permission_t mpu_pal_specificAccessConfig[MPU_PAL_REGION_ACCESS_SET_COUNT] =
{
    /* Set 1 */
    MPU_SUPERVISOR_RWX_USER_RWX, /* Allow read, write and execute for both
                                   supervisor and user mode */
    /* Set 2 */
    MPU_SUPERVISOR_RWX_USER_RWX, /* Allow read, write and execute for both
                                   supervisor and user mode */
    /* Set 3 */
    MPU_SUPERVISOR_RWX_USER_RWX /* Allow read, write and execute for both supervisor and user mode */
}

mpu_pal_extension.specAccessEnable = true;
mpu_pal_extension.specAccessSet = true;

/* SMPU Master configuration /
#define MPU_PAL_MASTER_COUNT 15U
mpu_master_access_permission_t mpu_pal_masterAccRight[MPU_PAL_MASTER_COUNT] =
{
    /* Master */
    {

```

```

        .masterNum    = FEATURE_SMPU_MASTER_CORE_Z4A, /* Core Z4A */
        .accessRight = MPU_RW_OR_SET_3                /* Normal access rights: read, write and execute for both
                                                         supervisor and user mode
                                                         Specific access: use set 3 in region configuration */
    },
    /* Define the rest masters here */
    ...
};

/* SMPU region configuration */
#define MPU_PAL_REGION_COUNT 1U
mpu_region_config_t mpu_pal_regionConfigs[MPU_PAL_REGION_COUNT] =
{
    /* Region 0 */
    {
        .startAddr = 0U,                                /* Start address */
        .endAddr = 0xFFFFFFFFFU,                        /* End address */
        .masterAccRight = mpu_pal_masterAccRight, /* Pointer to access right of all masters */
        /* If support PID */
        .processIdEnable = true,                        /* Enable process identifier for all masters */
        .processIdentifier = 0x00U,                    /* Process identifier */
        .processIdMask = 0xFFU,                        /* Process identifier mask */
        /* End if */
        /* Extension */
        .extension = &mpu_pal_extension                /* This field will be used to add extra settings
                                                         to the basic region configuration */
    }
}

/* Initialization */
...

```

2. Update lock configuration and get lock status on region

```

/* All masters cannot write to region descriptor 0 (cannot modify region 0 configuration) */
status = MPU_UpdateRegionLock(&mpu_pal_Instance, 0U, MPU_ALL_LOCK);

/* Gets lock status on region 0 */
mpu_region_lock_t lockStatus;
status = MPU_GetRegionLockInfo(&mpu_pal_Instance, 0U, &lockStatus);

```

Modules

- **MPU PAL**

Memory Protection Unit Peripheral Abstraction Layer.

17.100 Node configuration

17.100.1 Detailed Description

This group contains APIs that used for node configuration purpose.

With protocol lin2.1 in slave node, some service like (Data dump, Conditional change nad with id from 2 to 255) are not supported by LinStack but user can implement it in application by use function `Id_receive_message` and `Id_send_message` in transport layer.

With protocol J2602 in slave node, some service like (Data dump, Assign NAD, Conditional change NAD) are not supported by LinStack but user can implement it in application by choosing these services in supported_sid in PEX GUI and use function `Id_receive_message` and `Id_send_message` in transport layer. When received target reset master request slave node just update `status_byte` and send response positive message.

Functions

- `I_u8 Id_is_ready (I_ifc_handle iii)`
This call returns the status of the last requested configuration service.
- `void Id_check_response (I_ifc_handle iii, I_u8 *const RSID, I_u8 *const error_code)`
This call returns the result of the last node configuration service, in the parameters RSID and error_code. A value in RSID is always returned but not always in the error_code. Default values for RSID and error_code is 0 (zero).
- `void Id_assign_frame_id_range (I_ifc_handle iii, I_u8 NAD, I_u8 start_index, const I_u8 *const PIDs)`
This function assigns the protected identifier of up to four frames.
- `void Id_save_configuration (I_ifc_handle iii, I_u8 NAD)`
This function to issue a save configuration request to a slave node.
- `I_u8 Id_read_configuration (I_ifc_handle iii, I_u8 *const data, I_u8 *const length)`
This function copies current configuration in a reserved area.
- `I_u8 Id_set_configuration (I_ifc_handle iii, const I_u8 *const data, I_u16 length)`
This function configures slave node according to data.
- `void Id_assign_NAD (I_ifc_handle iii, I_u8 initial_NAD, I_u16 supplier_id, I_u16 function_id, I_u8 new_NAD)`
This call assigns the NAD (node diagnostic address) of all slave nodes that matches the initial_NAD, the supplier ID and the function ID. Master node only.
- `void Id_conditional_change_NAD (I_ifc_handle iii, I_u8 NAD, I_u8 id, I_u8 byte_data, I_u8 mask, I_u8 invert, I_u8 new_NAD)`
This call changes the NAD if the node properties fulfill the test specified by id, byte, mask and invert. Master node only.

17.100.2 Function Documentation

17.100.2.1 void Id_assign_frame_id_range (I_ifc_handle iii, I_u8 NAD, I_u8 start_index, const I_u8 *const PIDs)

This function assigns the protected identifier of up to four frames.

Parameters

in	<i>iii</i>	lin interface handle
in	<i>NAD</i>	Node address value of the target node
in	<i>start_index</i>	specifies which is the first frame to assign a PID
in	<i>PIDs</i>	list of protected identifier

Returns

void

This API is available for master interfaces only

Definition at line 149 of file `lin_diagnostic_service.c`.

17.100.2.2 `void Id_assign_NAD (I_ifc_handle iii, I_u8 initial_NAD, I_u16 supplier_id, I_u16 function_id, I_u8 new_NAD)`

This call assigns the NAD (node diagnostic address) of all slave nodes that matches the `initial_NAD`, the supplier ID and the function ID. Master node only.

Parameters

in	<i>iii</i>	LIN interface handle
in	<i>initial_NAD</i>	Initial node address of the target node
in	<i>supplier_id</i>	Supplier ID of the target node
in	<i>function_id</i>	Function identifier of the target node
in	<i>new_NAD</i>	New node address

Returns

void

This call assigns the NAD (node diagnostic address) of all slave nodes that matches the initial_NAD, the supplier ID and the function ID. The new NAD of the slave node will be new_NAD. This function is used for master node only.

Definition at line 845 of file lin_diagnostic_service.c.

17.100.2.3 void Id_check_response (I_ifc_handle *iii*, I_u8 *const *RSID*, I_u8 *const *error_code*)

This call returns the result of the last node configuration service, in the parameters RSID and error_code. A value in RSID is always returned but not always in the error_code. Default values for RSID and error_code is 0 (zero).

For slave interfaces Id_check_response shall do nothing

Parameters

in	<i>iii</i>	lin interface handle
out	<i>RSID</i>	buffer for saving the response ID
out	<i>error_code</i>	buffer for saving the error code

This API is available for master interfaces only

Definition at line 118 of file lin_diagnostic_service.c.

17.100.2.4 void Id_conditional_change_NAD (I_ifc_handle *iii*, I_u8 *NAD*, I_u8 *id*, I_u8 *byte_data*, I_u8 *mask*, I_u8 *invert*, I_u8 *new_NAD*)

This call changes the NAD if the node properties fulfill the test specified by id, byte, mask and invert. Master node only.

Parameters

in	<i>iii</i>	:LIN interface handle
in	<i>NAD</i>	Current NAD value of the target node
in	<i>id</i>	Property ID of the target node
in	<i>byte</i>	Byte location of property value to be read from the target node
in	<i>mask</i>	Value for masking the read property byte
in	<i>invert</i>	Value for excluding the read property byte
in	<i>new_NAD</i>	New NAD value to be assigned when the condition is met

Returns

void

This call changes the NAD if the node properties fulfill the test specified by id, byte, mask and invert.

Definition at line 886 of file lin_diagnostic_service.c.

17.100.2.5 I_u8 Id_is_ready (I_ifc_handle *iii*)

This call returns the status of the last requested configuration service.

Parameters

<i>in</i>	<i>iii</i>	lin interface handle
-----------	------------	----------------------

Returns

LD_SERVICE_BUSY Service is ongoing.

LD_REQUEST_FINISHED The configuration request has been completed. This is a intermediate status between the configuration request and configuration response.

LD_SERVICE_IDLE The configuration request/response combination has been completed, i.e. the response is valid and may be analyzed. Also, this value is returned if no request has yet been called.

LD_SERVICE_ERROR The configuration request or response experienced an error. Error here means error on the bus, and not a negative configuration response from the slave node.

Definition at line 92 of file lin_diagnostic_service.c.

17.100.2.6 `I_u8 Id_read_configuration (I_ifc_handle iii, I_u8 *const data, I_u8 *const length)`

This function copies current configuration in a reserved area.

Parameters

<i>in</i>	<i>iii</i>	Lin interface handle
<i>out</i>	<i>data</i>	Data area to save configuration,
<i>out</i>	<i>length</i>	Length of data area (1 + n, NAD + PIDs)

Returns

LD_READ_OK If the service was successful.

LD_LENGTH_TOO_SHORT If the configuration size is greater than the length. It means that the data area does not contain a valid configuration.

This function is implemented Slave Only. Set the expected length value to EXP = NN + NF, where : NN = the number of NAD. NF = the number of configurable frames; Moreover: Not taken PID's diagnostics frame: 3C, 3D

Definition at line 446 of file lin_diagnostic_service.c.

17.100.2.7 `void Id_save_configuration (I_ifc_handle iii, I_u8 NAD)`

This function to issue a save configuration request to a slave node.

Parameters

<i>in</i>	<i>iii</i>	Interface name
<i>in</i>	<i>NAD</i>	Node address of target

Returns

void

This function is available for master nodes only. This function is available for all diagnostic classes and only for LIN2.1 and above. This function is called to send a save configuration request to a specific slave node with the given NAD, or to all slave nodes if NAD is set to broadcast This function is implemented for Master Only.

Definition at line 191 of file lin_diagnostic_service.c.

17.100.2.8 `I_u8 Id_set_configuration (I_ifc_handle iii, const I_u8 *const data, I_u16 length)`

This function configures slave node according to data.

Parameters

<i>in</i>	<i>iii</i>	Lin interface handle
<i>in</i>	<i>data</i>	Structure containing the NAD and all the n PIDs for the frames of the specified NAD,
<i>in</i>	<i>length</i>	Length of data area (1 + n, NAD + PIDs)

Returns

LD_SET_OK If the service was successful

LD_LENGTH_NOT_CORRECT If the required size of the configuration is not equal to the given length.

LD_DATA_ERROR The set of configuration could not be made.

This function is implemented Slave Only. Set the expected length value to $EXP = NN + NF$, where : NN = the number of NAD. NF = the number of configurable frames; Moreover: Not taken PID's diagnostics frame: 3C, 3D

Definition at line 511 of file lin_diagnostic_service.c.

17.101 Node configuration

17.101.1 Detailed Description

This group contains APIs that used for node configuration purpose.

Functions

- `I_bool Id_is_ready_j2602 (I_ifc_handle iii)`
Verifies a state of node setting (using for J2602 and LIN 2.0).
- `I_u8 Id_check_response_j2602 (I_ifc_handle iii, I_u8 *const RSID, I_u8 *const error_code)`
Verifies the state of response (using for J2602 and LIN 2.0) Master node only.
- `I_bool Id_reconfig_msg_ID (I_ifc_handle iii, I_u8 dnn)`
This function reconfigures frame identifiers of a J2602 slave node based on input dnn.
- `I_bool Id_assign_NAD_j2602 (I_ifc_handle iii, I_u8 dnn)`
This function assigns NAD of a J2602 slave device based on input DNN that is Device Node Number. NAD is (0x60+ DNN).

17.101.2 Function Documentation

17.101.2.1 I_bool Id_assign_NAD_j2602 (I_ifc_handle iii, I_u8 dnn)

This function assigns NAD of a J2602 slave device based on input DNN that is Device Node Number. NAD is (0x60+ DNN).

Parameters

<code>in</code>	<code>iii</code>	LIN interface handle
<code>in</code>	<code>dnn</code>	DNN of the device

Returns

- `I_bool`: 0: successful: New Configured NAD is 0x60 + DNN
`I_bool`: 1: Unsuccessful: for either one of the following reasons:
- The protocol of this interface is not J2602
 - This device is a Master node in this interface
 - The input DNN is greater than 0xD that is invalid

Definition at line 1740 of file `lin_diagnostic_service.c`.

17.101.2.2 I_u8 Id_check_response_j2602 (I_ifc_handle iii, I_u8 *const RSID, I_u8 *const error_code)

Verifies the state of response (using for J2602 and LIN 2.0) Master node only.

Parameters

<code>in</code>	<code>iii</code>	LIN interface handle
<code>out</code>	<code>RSID</code>	buffer for saving the response ID
<code>out</code>	<code>error_code</code>	buffer for saving the error code

Returns

`I_u8` status of the last service

Definition at line 1528 of file `lin_diagnostic_service.c`.

17.101.2.3 I_bool Id_is_ready_j2602 (I_ifc_handle iii)

Verifies a state of node setting (using for J2602 and LIN 2.0).

Parameters

<i>in</i>	<i>iii</i>	LIN interface handle
-----------	------------	----------------------

Returns

I_bool

Definition at line 1502 of file `lin_diagnostic_service.c`.

17.101.2.4 I_bool Id_reconfig_msg_ID (I_ifc_handle *iii*, I_u8 *dnn*)

This function reconfigures frame identifiers of a J2602 slave node based on input *dnn*.

Parameters

<i>in</i>	<i>iii</i>	LIN interface handle
<i>in</i>	<i>dnn</i>	DNN of the device

Returns

I_bool: 0: successful: Frame Identifiers were reconfigured based on input DNN according to NAD Message ID mapping table.

I_bool: 1: Unsuccessful: for either one of the following reasons:

- The protocol of this interface is not J2602
- This device is a Master node in this interface
- The input DNN is greater than 0xD that is invalid
- The slave has more than 16 configurable frames
- The slave has 9-16 configurable frames, and *dnn* is 0xC or 0xD
- The slave has 5-8 configurable frames, and *dnn* is not 0x00, 0x2, 0x4, 0x6, 0x8, 0xA, 0xC.

Definition at line 1622 of file `lin_diagnostic_service.c`.

17.102 Node identification

17.102.1 Detailed Description

This group contains API that used for node identification purpose.

Read by identifier service just support id 0 and 1. User can implement for other id by modify function `Id_read_by_id` in generated file `lin_cfg.c`.

Functions

- void `Id_read_by_id` (`I_ifc_handle` *iii*, `I_u8` *NAD*, `I_u16` *supplier_id*, `I_u16` *function_id*, `I_u8` *id*, `lin_product_id_t` **const data*)

The call requests the slave node selected with the NAD to return the property associated with the id parameter. Master node only.

17.102.2 Function Documentation

17.102.2.1 void `Id_read_by_id` (`I_ifc_handle` *iii*, `I_u8` *NAD*, `I_u16` *supplier_id*, `I_u16` *function_id*, `I_u8` *id*, `lin_product_id_t` **const data*)

The call requests the slave node selected with the NAD to return the property associated with the id parameter. Master node only.

Parameters

in	<i>iii</i>	LIN interface handle
in	<i>NAD</i>	Value of the target node
in	<i>supplier_id</i>	Supplier ID of the target node
in	<i>function_id</i>	Function ID of the target node
in	<i>id</i>	ID of the target node
out	<i>data</i>	Buffer for saving the data read from the node

Returns

void

The call requests the slave node selected with the NAD to return the property associated with the id parameter.

Definition at line 933 of file `lin_diagnostic_service.c`.

17.103 Notification

This group contains APIs that let users know when a signal's value changed.

17.104 OS Interface (OSIF)

17.104.1 Detailed Description

OS Interface Layer (OSIF)

The OSIF layer is a minimal wrapper layer for common RTOS services, intended to be used by SDK drivers and middlewares. It can be used by the user application, but it is not recommended. The operations supported by OSIF:

- mutex lock/unlock
- semaphore post/wait
- time delay and get time elapsed

OSIF currently comes in two variants: bare-metal and FreeRTOS. Steps to use each one are described below.

FreeRTOS

To integrate the FreeRTOS OSIF variant, two steps are necessary:

- compile and link the [osif_freertos.c](#) file
- define a project-wide compile symbol:

```
USING_OS_FREERTOS
```

FreeRTOSConfig.h dependencies

FreeRTOS configuration file needs to have these options activated (set to 1 in FreeRTOSConfig.h):

- INCLUDE_xQueueGetMutexHolder
- INCLUDE_xTaskGetCurrentTaskHandle

Hardware resources

FreeRTOS OSIF uses the FreeRTOS API and services, does not use any additional hardware or software resources.

FreeRTOS supported platforms

The SDK platforms supported by FreeRTOS can be found in the following table. If a platform is supported by FreeRTOS, both osif variants, bare-metal and freertos, are supported. If the platform is not supported by FreeRTOS, only osif bare-metal variant is applicable:

Platform	FreeRTOS support
S32K11x	Yes
S32K14x	Yes
S32K14xW	Yes
MPC5746C	Yes
MPC5748G	Yes
MPC5744P	Yes
S32R274	Yes
S32R372	Yes

FreeRTOS static vs dynamic memory allocation

OSIF objects will use static memory allocation schemes (FreeRTOS 9.0.0 and above) if the feature is enabled.

This should be transparent for the upper layer which uses OSIF.

The FreeRTOS configuration option is

```
configSUPPORT_STATIC_ALLOCATION
```

If it's set to 1, the OSIF will use static memory allocation.

Bare-metal

To integrate the bare-metal OSIF variant:

- compile and link the [osif_baremetal.c](#) file

Mutex operations are dummy operations (always return success) and semaphore is implemented as a simple counter.

Hardware resources

Bare-metal OSIF uses a hardware timer to accurately measure time. The timer and channel used are platform-dependent, are chosen to be the same as the FreeRTOS implementation if possible.

The table below shows which timers and channels are used on each platform:

Platform	Timer	Channel
S32K11x	Systick	N/A
S32K14x	Systick	N/A
S32K14xW	Systick	N/A
MPC5746C	PIT	15
MPC5748G	PIT	15
MPC5744P	PIT	3
S32R274	PIT0	3
S32R372	PIT0	3

Bare-metal timing limitations

For bare-metal OSIF, the timer is initialized at the first call in OSIF that needs timing. That is either [OSIF_TimeDelay](#), [OSIF_MutexLock](#) or [OSIF_SemaWait](#) (functions with timeout). The timer configuration, but not the counter, is updated at each subsequent call to these functions.

Do not assume [OSIF_GetMilliseconds](#) will return a global value since system initialization. It will return the global value since the very first timer initialization, mentioned above.

Integration guideline

Compilation units

The following files need to be compiled in the project:

- for baremetal variant:

```
${S32SDK_PATH}\rtos\osif\osif_baremetal.c
```

- for FreeRTOS variant:

```
${S32SDK_PATH}\rtos\osif\osif_freertos.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\rtos\osif\
```

Compile symbols

- for baremetal variant: No special symbols are required for this component
- for FreeRTOS variant: The following symbol must be added to the compile symbols of the toolchain:

```
USING_OS_FREERTOS
```

Dependencies

- for baremetal variant:

Clock Manager

Interrupt Manager (Interrupt)

- for FreeRTOS variant:

FreeRTOS

Macros

- `#define OSIF_WAIT_FOREVER 0xFFFFFFFFu`

Functions

- void `OSIF_TimeDelay` (const uint32_t delay)
Delays execution for a number of milliseconds.
- uint32_t `OSIF_GetMilliseconds` (void)
Returns the number of milliseconds elapsed since starting the internal timer or starting the scheduler.
- status_t `OSIF_MutexLock` (const mutex_t *const pMutex, const uint32_t timeout)
Waits for a mutex and locks it.
- status_t `OSIF_MutexUnlock` (const mutex_t *const pMutex)
Unlocks a previously locked mutex.
- status_t `OSIF_MutexCreate` (mutex_t *const pMutex)
Create an unlocked mutex.
- status_t `OSIF_MutexDestroy` (const mutex_t *const pMutex)
Destroys a previously created mutex.
- status_t `OSIF_SemaWait` (semaphore_t *const pSem, const uint32_t timeout)
Decrement a semaphore with timeout.
- status_t `OSIF_SemaPost` (semaphore_t *const pSem)
Increment a semaphore.
- status_t `OSIF_SemaCreate` (semaphore_t *const pSem, const uint8_t initValue)
Creates a semaphore with a given value.
- status_t `OSIF_SemaDestroy` (const semaphore_t *const pSem)
Destroys a previously created semaphore.

17.104.2 Macro Definition Documentation

17.104.2.1 `#define OSIF_WAIT_FOREVER 0xFFFFFFFFu`

Definition at line 71 of file osif.h.

17.104.3 Function Documentation

17.104.3.1 uint32_t `OSIF_GetMilliseconds` (void)

Returns the number of milliseconds elapsed since starting the internal timer or starting the scheduler.

Returns

the number of milliseconds elapsed

Definition at line 233 of file osif_baremetal.c.

17.104.3.2 `status_t OSIF_MutexCreate (mutex_t *const pMutex)`

Create an unlocked mutex.

Parameters

<i>in</i>	<i>pMutex</i>	reference to the mutex object
-----------	---------------	-------------------------------

Returns

One of the possible status codes:

- STATUS_SUCCESS: mutex created
- STATUS_ERROR: mutex could not be created

Definition at line 281 of file osif_baremetal.c.

17.104.3.3 status_t OSIF_MutexDestroy (const mutex_t *const pMutex)

Destroys a previously created mutex.

Parameters

<i>in</i>	<i>pMutex</i>	reference to the mutex object
-----------	---------------	-------------------------------

Returns

One of the possible status codes:

- STATUS_SUCCESS: mutex destroyed

Definition at line 295 of file osif_baremetal.c.

17.104.3.4 status_t OSIF_MutexLock (const mutex_t *const pMutex, const uint32_t timeout)

Waits for a mutex and locks it.

Parameters

<i>in</i>	<i>pMutex</i>	reference to the mutex object
<i>in</i>	<i>timeout</i>	time-out value in milliseconds

Returns

One of the possible status codes:

- STATUS_SUCCESS: mutex lock operation success
- STATUS_ERROR: mutex already owned by current thread
- STATUS_TIMEOUT: mutex lock operation timed out

Definition at line 251 of file osif_baremetal.c.

17.104.3.5 status_t OSIF_MutexUnlock (const mutex_t *const pMutex)

Unlocks a previously locked mutex.

Parameters

<i>in</i>	<i>pMutex</i>	reference to the mutex object
-----------	---------------	-------------------------------

Returns

One of the possible status codes:

- STATUS_SUCCESS: mutex unlock operation success
- STATUS_ERROR: mutex unlock failed

Definition at line 267 of file osif_baremetal.c.

17.104.3.6 `status_t OSIF_SemaCreate (semaphore_t *const pSem, const uint8_t initValue)`

Creates a semaphore with a given value.

Parameters

in	<i>pSem</i>	reference to the semaphore object
in	<i>initValue</i>	initial value of the semaphore

Returns

One of the possible status codes:

- STATUS_SUCCESS: semaphore created
- STATUS_ERROR: semaphore could not be created

Definition at line 402 of file osif_baremetal.c.

17.104.3.7 `status_t OSIF_SemaDestroy (const semaphore_t *const pSem)`

Destroys a previously created semaphore.

Parameters

in	<i>pSem</i>	reference to the semaphore object
----	-------------	-----------------------------------

Returns

One of the possible status codes:

- STATUS_SUCCESS: semaphore destroyed

Definition at line 420 of file osif_baremetal.c.

17.104.3.8 `status_t OSIF_SemaPost (semaphore_t *const pSem)`

Increment a semaphore.

Parameters

in	<i>pSem</i>	reference to the semaphore object
----	-------------	-----------------------------------

Returns

One of the possible status codes:

- STATUS_SUCCESS: semaphore post operation success
- STATUS_ERROR: semaphore could not be incremented

Definition at line 375 of file osif_baremetal.c.

17.104.3.9 `status_t OSIF_SemaWait (semaphore_t *const pSem, const uint32_t timeout)`

Decrement a semaphore with timeout.

Parameters

in	<i>pSem</i>	reference to the semaphore object
in	<i>timeout</i>	time-out value in milliseconds

Returns

One of the possible status codes:

- STATUS_SUCCESS: semaphore wait operation success
- STATUS_TIMEOUT: semaphore wait timed out

Definition at line 311 of file osif_baremetal.c.

17.104.3.10 void OSIF_TimeDelay (const uint32_t *delay*)

Delays execution for a number of milliseconds.

Parameters

<code>in</code>	<code>delay</code>	Time delay in milliseconds.
-----------------	--------------------	-----------------------------

Definition at line 208 of file `osif_baremetal.c`.

17.105 Output Compare - Peripheral Abstraction Layer (OC PAL)

17.105.1 Detailed Description

The S32 SDK provides a Peripheral Abstraction Layer for the output compare mode of S32 SDK devices.

The OC PAL driver allows to set pin, clear pin or toggle pin. It was designed to be portable across all platforms and IPs which support FTM, eMIOS, FlexPWM and eTIMER.

How to integrate OC PAL in your application

Unlike the other drivers, OC PAL modules need to include a configuration file named `oc_pal_cfg.h`. This one allows the user to specify which IPs are used. The following code example shows how to configure one instance for each available OC IPs.

```
#ifndef OC_PAL_CFG_H
#define OC_PAL_CFG_H

/* Define which IP instance will be used in current project */
#define OC_PAL_OVER_EMIOS

#endif /* OC_PAL_CFG_H */
```

The following table contains the matching between platforms and available IPs

IP/ M↔ CU	S32↔ K116	S32↔ K118	S32↔ K142	S32↔ K142↔ W	S32↔ K144	S32↔ K144↔ W	S32↔ K146	S32↔ K148	M↔ P↔ C5748 G	M↔ P↔ C5746 C	M↔ P↔ C5744 P	S32↔ R274	S32↔ R372
FT↔ M↔ _↔ OC	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	NO	NO	NO	NO	NO
e↔ MI↔ O↔ S_↔ OC	NO	NO	NO	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES	NO	NO	NO
eT↔ IM↔ ER	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES	Y↔ ES
Flex↔ P↔ WM	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES	Y↔ ES

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\pal\src\oc\oc_pal.c
${S32SDK_PATH}\platform\pal\src\oc\oc_irq.c
${S32SDK_PATH}\platform\pal\src\oc\oc_irq.h
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\pal\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager](#) [Interrupt Manager \(Interrupt\)](#) [ftm_oc](#) [emios_oc](#) [etimer](#) [flexpwm](#)

Features

- Set the output signal can be set, cleared, or toggled pin
- Start/stop the channel in the output compare mode
- Force the channel output to high or low level

Functionality

Initialization

In order to use the OC PAL driver it must be first initialized, using [OC_Init\(\)](#) function. Once initialized, it should be de-initialized before initialized again for the same OC module instance, using [OC_Deinit\(\)](#). The initialization function does the following operations:

- sets the clock source, clock prescaler
- sets the number of channel output compare are used
- configures the channel output to set or clear or toggle pin

Example:

```
const oc_instance_t oc_pall_instance = { OC_INST_TYPE_ETIMER, 0U };

channel_extension_etimer_for_oc_t oc_pall_etimerChnExtension0 =
{
    .primaryInput =
    {
        .source = ETIMER_IN_SRC_CLK_DIV_128,
        .polarity = ETIMER_POLARITY_POSITIVE,
    },
    .outputPin =
    {
        .enable = true,
        .polarity = ETIMER_POLARITY_POSITIVE,
    },
};

oc_output_ch_param_t oc_pall_ChnConfig[1] =
{
    /* Channel configuration 0 */
    {
        .hwChannelId      = 4U,
        .chMode            = OC_TOGGLE_ON_MATCH,
        .comparedValue     = 62500,
        .channelExtension  = &oc_pall_etimerChnExtension0,
        .channelCallbackParams = NULL,
        .channelCallbacks  = oc_pall_channel_callBack0
    }
};

oc_config_t oc_pall_InitConfig =
{
    .numChannels      = 1U,
    .outputChConfig   = oc_pall_ChnConfig,
    .extension        = NULL
};

/* Initialize output compare mode */
OC_Init(&oc_pall_instance, &oc_pall_InitConfig);
```

De-initialize a output compare instance

This function will disable the output compare mode. The driver can't be used again until reinitialized. All register are reset to default value and counter is stopped.

Example:

```
/* De-initialize output compare mode */
OC_Deinit(&oc_pall_instance);
```

Start the channel in the output compare mode

This function will set the channel is in the output compare mode.

Example:

```
uint8_t hwChannel = oc_pall_InitConfig.outputChConfig->hwChannelId;

/* Start channel in the output compare mode */
OC_StartChannel(&oc_pall_instance, hwChannel);
```

Stop the channel in the output compare mode

This function will set the channel is used in GPIO mode or other peripheral.

Example:

```
uint8_t hwChannel = oc_pall_InitConfig.outputChConfig->hwChannelId;

/* Stop channel in the output compare mode */
OC_StopChannel(&oc_pall_instance, hwChannel);
```

Control the channel output by software

This function is used to forces the output pin to a specified value. It can be used to control the output pin value when the OC channel is disabled.

Example:

```
uint8_t hwChannel = oc_pall_InitConfig.outputChConfig->hwChannelId;

/* Force the channel output by software */
OC_SetOutputState(&oc_pall_instance, hwChannel, false);
```

Set the operation mode of channel output

This function will set the action executed on a compare match value to set output pin, clear output pin, toggle output pin.

Example:

```
uint8_t hwChannel = oc_pall_InitConfig.outputChConfig->hwChannelId;

/* Change the channel output to toggle pin */
OC_SetOutputAction(&oc_pall_instance, hwChannel,
    OC_TOGGLE_ON_MATCH);
```

Update the match value on the channel

This function will update the value of an output compare channel to the counter matches to this value.

Example:

```
uint8_t hwChannel = oc_pall_InitConfig.outputChConfig->hwChannelId;

/* Set the match counter to new value */
OC_SetCompareValue(&oc_pall_instance, hwChannel, 0x1000UL,
    OC_RELATIVE_VALUE);
```

Important Notes

- Before using the OC PAL driver the module clock must be configured. Refer to Clock Manager for clock configuration.

- The board specific configurations must be done prior to driver after that can call APIs.
- Some features are not available for all OC IPs and incorrect parameters will be handled by DEV_ASSERT.

Data Structures

- struct [oc_output_ch_param_t](#)
The configuration structure of output compare parameters for each channel. [More...](#)
- struct [oc_config_t](#)
Defines the configuration structures are used in the output compare mode. [More...](#)
- struct [extension_ftm_for_oc_t](#)
Defines the extension structure for the output compare mode over FTM. [More...](#)

Enumerations

- enum [oc_option_mode_t](#) { [OC_DISABLE_OUTPUT](#) = 0x00U, [OC_TOGGLE_ON_MATCH](#) = 0x01U, [OC_CLEAR_ON_MATCH](#) = 0x02U, [OC_SET_ON_MATCH](#) = 0x03U }
- The type of comparison for output compare mode Implements : [oc_option_mode_t](#) Class.*
- enum [oc_option_update_t](#) { [OC_RELATIVE_VALUE](#) = 0x00U, [OC_ABSOLUTE_VALUE](#) = 0x01U }
- The type of update on the channel match Implements : [oc_option_update_t](#) Class.*

Functions

- status_t [OC_Init](#) (const [oc_instance_t](#) *const instance, const [oc_config_t](#) *const configPtr)
Initializes the output compare mode.
- status_t [OC_Deinit](#) (const [oc_instance_t](#) *const instance)
De-initialize the output compare instance.
- void [OC_StartChannel](#) (const [oc_instance_t](#) *const instance, const uint8_t channel)
Start the counter.
- void [OC_StopChannel](#) (const [oc_instance_t](#) *const instance, const uint8_t channel)
Stop the counter.
- status_t [OC_SetOutputState](#) (const [oc_instance_t](#) *const instance, const uint8_t channel, bool outputValue)
Control the channel output by software.
- status_t [OC_SetOutputAction](#) (const [oc_instance_t](#) *const instance, const uint8_t channel, [oc_option_mode_t](#) channelMode)
Set the operation mode of channel output.
- status_t [OC_SetCompareValue](#) (const [oc_instance_t](#) *const instance, const uint8_t channel, uint32_t nextCompareMatchValue, [oc_option_update_t](#) typeOfupdate)
Update the match value on the channel.
- void [OC_EnableNotification](#) (const [oc_instance_t](#) *const instance, const uint8_t channel)
Enable channel notifications.
- void [OC_DisableNotification](#) (const [oc_instance_t](#) *const instance, const uint8_t channel)
Disable channel notifications.

17.105.2 Data Structure Documentation

17.105.2.1 struct oc_output_ch_param_t

The configuration structure of output compare parameters for each channel.

Implements : [oc_output_ch_param_t](#) Class

Definition at line 83 of file [oc_pal.h](#).

Data Fields

- uint8_t [hwChannelId](#)
- oc_option_mode_t [chMode](#)
- uint16_t [comparedValue](#)
- void * [channelExtension](#)
- void * [channelCallbackParams](#)
- oc_callback_t [channelCallbacks](#)

Field Documentation**17.105.2.1.1 void* channelCallbackParams**

The parameter of callback application for channels event

Definition at line 89 of file oc_pal.h.

17.105.2.1.2 oc_callback_t channelCallbacks

The callback function for channels event

Definition at line 90 of file oc_pal.h.

17.105.2.1.3 void* channelExtension

The IP specific configuration structure for channel

Definition at line 88 of file oc_pal.h.

17.105.2.1.4 oc_option_mode_t chMode

Channel output mode

Definition at line 86 of file oc_pal.h.

17.105.2.1.5 uint16_t comparedValue

The compared value

Definition at line 87 of file oc_pal.h.

17.105.2.1.6 uint8_t hwChannelId

Physical hardware channel ID

Definition at line 85 of file oc_pal.h.

17.105.2.2 struct oc_config_t

Defines the configuration structures are used in the output compare mode.

Implements : oc_config_t_Class

Definition at line 98 of file oc_pal.h.

Data Fields

- uint8_t [nNumChannels](#)
- const oc_output_ch_param_t * [outputChConfig](#)
- void * [extension](#)

Field Documentation**17.105.2.2.1 void* extension**

IP specific configuration structure

Definition at line 102 of file oc_pal.h.

17.105.2.2.2 uint8_t nNumChannels

Number of output compare channel used

Definition at line 100 of file oc_pal.h.

17.105.2.2.3 const oc_output_ch_param_t* outputChConfig

Output compare channels configuration

Definition at line 101 of file oc_pal.h.

17.105.2.3 struct extension_ftm_for_oc_t

Defines the extension structure for the output compare mode over FTM.

Part of FTM configuration structure Implements : extension_ftm_for_oc_t_Class

Definition at line 112 of file oc_pal.h.

Data Fields

- uint16_t maxCountValue
- ftm_clock_source_t ftmClockSource
- ftm_clock_ps_t ftmPrescaler

Field Documentation

17.105.2.3.1 ftm_clock_source_t ftmClockSource

Select clock source for FTM

Definition at line 115 of file oc_pal.h.

17.105.2.3.2 ftm_clock_ps_t ftmPrescaler

Register pre-scaler options available in the ftm_clock_ps_t enumeration

Definition at line 116 of file oc_pal.h.

17.105.2.3.3 uint16_t maxCountValue

Maximum count value in ticks

Definition at line 114 of file oc_pal.h.

17.105.3 Enumeration Type Documentation

17.105.3.1 enum oc_option_mode_t

The type of comparison for output compare mode Implements : oc_option_mode_t_Class.

Enumerator

- OC_DISABLE_OUTPUT** No action on output pin
- OC_TOGGLE_ON_MATCH** Toggle on match
- OC_CLEAR_ON_MATCH** Clear on match
- OC_SET_ON_MATCH** Set on match

Definition at line 60 of file oc_pal.h.

17.105.3.2 enum oc_option_update_t

The type of update on the channel match Implements : oc_option_update_t_Class.

Enumerator

OC_RELATIVE_VALUE Next compared value is relative to current value

OC_ABSOLUTE_VALUE Next compared value is absolute

Definition at line 72 of file oc_pal.h.

17.105.4 Function Documentation

17.105.4.1 status_t OC_Deinit (const oc_instance_t *const instance)

De-initialize the output compare instance.

This function will disable the output compare mode. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

in	instance	The output compare instance number.
----	----------	-------------------------------------

Returns

Operation status

- STATUS_SUCCESS: Operation was successful

Definition at line 1126 of file oc_pal.c.

17.105.4.2 void OC_DisableNotification (const oc_instance_t *const instance, const uint8_t channel)

Disable channel notifications.

This function disables channel notification.

Parameters

in	instance	The output compare instance number
in	channel	The channel number

Definition at line 1706 of file oc_pal.c.

17.105.4.3 void OC_EnableNotification (const oc_instance_t *const instance, const uint8_t channel)

Enable channel notifications.

This function enables channel notification.

Parameters

in	instance	The output compare instance number
in	channel	The channel number

Definition at line 1672 of file oc_pal.c.

17.105.4.4 status_t OC_Init (const oc_instance_t *const instance, const oc_config_t *const configPtr)

Initializes the output compare mode.

This function will initialize the OC PAL instance, including the other platform specific HW units used together in the output compare mode. This function configures a group of channels in instance to set, clear toggle the output signal.

Parameters

in	<i>instance</i>	The output compare instance number.
in	<i>configPtr</i>	The pointer to configuration structure.

Returns

Operation status

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 1062 of file oc_pal.c.

17.105.4.5 `status_t OC_SetCompareValue (const oc_instance_t *const instance, const uint8_t channel, uint32_t nextCompareMatchValue, oc_option_update_t typeOfupdate)`

Update the match value on the channel.

This function will update the value of an output compare channel to the counter matches to this value.

Parameters

in	<i>instance</i>	The output compare instance number.
in	<i>channel</i>	The channel number.
in	<i>nextCompareMatchValue</i>	The timer value in ticks until the next compare match event should be appeared.
in	<i>typeOfupdate</i>	The type of update: <ul style="list-style-type: none"> • OC_RELATIVE_VALUE : nextCompareMatchValue will be added to current counter value into the channel value register • OC_ABSOLUTE_VALUE : nextCompareMatchValue will be written into the channel value register

Returns

Operation status

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 1556 of file oc_pal.c.

17.105.4.6 `status_t OC_SetOutputAction (const oc_instance_t *const instance, const uint8_t channel, oc_option_mode_t channelMode)`

Set the operation mode of channel output.

This function will set the action executed on a compare match value to set output pin, clear output pin, toggle output pin.

Parameters

in	<i>instance</i>	The output compare instance number.
in	<i>channel</i>	The channel number.
in	<i>channelMode</i>	The channel mode in output compare: <ul style="list-style-type: none"> • OC_DISABLE_OUTPUT : No action on output pin • OC_TOGGLE_ON_MATCH : Toggle on match • OC_CLEAR_ON_MATCH : Clear on match • OC_SET_ON_MATCH : Set on match

Returns

Operation status

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 1463 of file oc_pal.c.

17.105.4.7 `status_t OC_SetOutputState (const oc_instance_t *const instance, const uint8_t channel, bool outputValue)`

Control the channel output by software.

This function is used to forces the output pin to a specified value.

Parameters

in	<i>instance</i>	The output compare instance number.
in	<i>channel</i>	The channel number.
in	<i>outputValue</i>	The output value: <ul style="list-style-type: none"> • false : The software output control forces 0 to the channel output. • true : The software output control forces 1 to the channel output.

Returns

Operation status

- STATUS_SUCCESS : Completed successfully.
- STATUS_ERROR : Error occurred.

Definition at line 1389 of file oc_pal.c.

17.105.4.8 `void OC_StartChannel (const oc_instance_t *const instance, const uint8_t channel)`

Start the counter.

This function start channel counting.

Parameters

in	<i>instance</i>	The output compare instance number.
in	<i>channel</i>	The channel number.

Definition at line 1240 of file oc_pal.c.

17.105.4.9 `void OC_StopChannel (const oc_instance_t *const instance, const uint8_t channel)`

Stop the counter.

This function stop channel output.

Parameters

<i>in</i>	<i>instance</i>	The output compare instance number.
<i>in</i>	<i>channel</i>	The channel number.

Definition at line 1323 of file oc_pal.c.

17.106 PDB Driver

17.106.1 Detailed Description

Programmable Delay Block Peripheral Driver.

Overview

This section describes the programming interface of the PDB Peripheral driver. The PDB peripheral driver configures the PDB (Programmable Delay Block). It handles the triggers for ADC and pulse out to the CMP and the PDB counter.

The PDB contains a counter whose output is compared to several different digital values. If the PDB is enabled, then a trigger input event will reset the counter and make it start to count. A trigger input event is defined as a rising edge being detected on a selected trigger input source, or if software trigger is selected and a software trigger is issued. Each PDB channel is associated with 1 ADC block, and each PDB channel contains 8 pre-triggers. A pre-trigger has a delay associated and is mapped to an ADC channel; when the PDB counter is equal to the delay value configured for a pre-trigger, the pre-trigger is activated and selects the ADC channel that starts the conversion. Inside a PDB channel, the pre-triggers can be configured to work as chains, meaning that a pre-trigger is enabled automatically when the ADC conversion selected by the previous pre-trigger, completes its execution. The pre-trigger delays and back-to-back operation must be configured, in such a way that at most one pre-trigger per PDB channel is activated at any given point - otherwise a PDB sequence error occurs. This feature is called back-to-back mode, and needs to be configured individually for each pre-trigger using [PDB_DRV_ConfigAdcPreTrigger\(\)](#). On some devices (depending on availability), chains can be configured between different PDB channels or PDB instances - this can be configured using `interchannelBackToBackEnable` or `instanceBackToBackEnable`.

PDB Initialization

For initializing the PDB counter, input triggers or general pre-trigger settings (instance or interchannel back-to-back modes) call [PDB_DRV_Init\(\)](#) Note that all pre-triggers share the same counter. * The basic timing/counting step is set when initializing the main PDB counter: The basic timing/counting step = $F_BusClkHz / \text{pdb_timer_config_t} \leftarrow \text{clkPreDiv} / \text{pdb_timer_config_t} \leftarrow \text{clkPreMultFactor}$

The `F_BusClkHz` is the frequency of bus clock in Hertz. The `clkPreDiv` and `clkPreMultFactor` are in the [pdb_↔ timer_config_t](#) structure. All pre-triggering delays use this frequency.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
* ${S32SDK_PATH}\platform\drivers\src\pdb\pdb_driver.c
* ${S32SDK_PATH}\platform\drivers\src\pdb\pdb_hw_access.c
*
```

Include path

The following paths need to be added to the include path of the toolchain:

```
* ${S32SDK_PATH}\platform\drivers\inc\
* ${S32SDK_PATH}\platform\drivers\src\pdb\
*
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager Interrupt Manager \(Interrupt\)](#)

PDB Call diagram

Three kinds of typical use cases are designed for the PDB module.

- Normal Timer/Counter - the basic use-case. The Timer/Counter starts after the PDB is initialized, when the input trigger (hardware or software) is asserted. When the counter reaches the compare value (set via modulus register), an interrupt or DMA transfer occur if enabled. In continuous mode, when the counter reaches the modulus compare value, it resets to zero and starts counting again.
- Triggering for ADC module. Depending on the number of ADC channels that need to be used, each pre-trigger must be configured using `PDB_DRV_ConfigAdcPreTrigger()`. The PDB counter starts counting when the input trigger (hardware or software) is asserted. If the pre-trigger is enabled in normal mode (back-to-back disabled), it will be activated (thus starting the corresponding ADC channel conversion) when the PDB counter is equal with the configured pre-trigger delay. If the pre-trigger is enabled in back-to-back mode, it will trigger the corresponding ADC channel conversion, when the ADC channel corresponding to the previous pre-trigger in the chain, completes the conversion (ADC COCO flag set).
- Generate pulse outputs of configurable width. The Pulse-Out is set to high/low when the PDB counter reaches the values set in `POyDLY[DLY1/2]`, configured via `PDB_DRV_SetCmpPulseOutDelayForHigh()` or `PDB_DRV_SetCmpPulseOutDelayForLow`. The Pulse-Out signal is connected to TRGMUX, which can route it to any other peripheral (e.g. can be used as a sample window for any CMP module).

These are the examples to initialize and configure the PDB driver for typical use cases.

Normal Timer/Counter:

```
#define PDB_INSTANCE    OUL

static volatile uint32_t gPdbIntCounter = 0U;
static volatile uint32_t gPdbInstance = 0U;
static void PDB_ISR_Counter(void);
void PDB_TEST_NormalTimer(uint32_t instance)
{
    pdb_timer_config_t PdbTimerConfig;
    PdbTimerConfig.loadValueMode      =
        PDB_LOAD_VAL_IMMEDIATELY;
    PdbTimerConfig.seqErrIntEnable     = false;
    PdbTimerConfig.clkPreDiv           = PDB_CLK_PREDIV_BY_8;
    PdbTimerConfig.clkPreMultFactor    =
        PDB_CLK_PREMULT_FACT_AS_40;
    PdbTimerConfig.triggerInput        = PDB_SOFTWARE_TRIGGER;
    PdbTimerConfig.continuousModeEnable = true;
    PdbTimerConfig.dmaEnable           = false;
    PdbTimerConfig.intEnable           = true;
    PdbTimerConfig.instanceBackToBackEnable = false;
    PdbTimerConfig.interchannelBackToBackEnable = false;
    PDB_DRV_Init(instance, &PdbTimerConfig);
    PDB_DRV_SetTimerModulusValue(instance, 0xFFFFU);
    PDB_DRV_SetValueForTimerInterrupt(instance, 0xFFU);
    PDB_DRV_LoadValuesCmd(instance);
    gPdbIntCounter = 0U;
    gPdbInstance = instance;
    PDB_DRV_SoftTriggerCmd(instance);
    while (gPdbIntCounter < 20U) {}
    PRINTF("PDB Timer's delay interrupt generated.\r\n");
    PDB_DRV_Deinit(instance);
    PRINTF("OK.\r\n");
}

void PDB_IRQHandler()
{
    PDB_DRV_ClearTimerIntFlag(PDB_INSTANCE);
    if (gPdbIntCounter >= 0xFFFFU)
    {
        gPdbIntCounter = 0U;
    }
    else
    {
        gPdbIntCounter++;
    }
}

#if PDB_INSTANCE < 1
void PDB0_IRQHandler(void)
{
    PDB_IRQHandler();
}
```

```

    }
    #elif PDB_INSTANCE < 2
        void PDB1_IRQHandler(void)
        {
            PDB_IRQHandler();
        }
    #endif

```

Trigger for ADC module:

```

void PDB_TEST_AdcPreTrigger(uint32_t instance)
{
    pdb_timer_config_t PdbTimerConfig;
    pdb_adc_pretrigger_config_t PdbAdcPreTriggerConfig;
    PdbTimerConfig.loadValueMode =
        PDB_LOAD_VAL_IMMEDIATELY;
    PdbTimerConfig.seqErrIntEnable = false;
    PdbTimerConfig.clkPreDiv = PDB_CLK_PREDIV_BY_8;
    PdbTimerConfig.clkPreMultFactor =
        PDB_CLK_PREMULT_FACT_AS_40;
    PdbTimerConfig.triggerInput = PDB_SOFTWARE_TRIGGER;
    PdbTimerConfig.continuousModeEnable = false;
    PdbTimerConfig.dmaEnable = false;
    PdbTimerConfig.intEnable = false;
    PdbTimerConfig.instanceBackToBackEnable = false;
    PdbTimerConfig.interchannelBackToBackEnable = false;
    PDB_DRV_Init(instance, &PdbTimerConfig);

    PdbAdcPreTriggerConfig.adcPreTriggerIdx = 0U;
    PdbAdcPreTriggerConfig.preTriggerEnable = true;
    PdbAdcPreTriggerConfig.preTriggerOutputEnable = true;
    PdbAdcPreTriggerConfig.preTriggerBackToBackEnable = false;
    PDB_DRV_ConfigAdcPreTrigger(instance, 0U, &PdbAdcPreTriggerConfig);

    PDB_DRV_SetTimerModulusValue(instance, 0xFFFFU);
    PDB_DRV_SetAdcPreTriggerDelayValue(instance, 0U, 0U, 0xFFFFU);
    PDB_DRV_LoadValuesCmd(instance);
    PDB_DRV_SoftTriggerCmd(instance);
    while (1U != PDB_DRV_GetAdcPreTriggerFlags(instance, 0U, 1U)) {}
    PDB_DRV_ClearAdcPreTriggerFlags(instance, 0U, 1U);
    PRINTF("PDB ADC PreTrigger generated.\r\n");
    PDB_DRV_Deinit(instance);
    PRINTF("OK.\r\n");
}

```

Data Structures

- struct [pdb_timer_config_t](#)
Defines the type of structure for basic timer in PDB. [More...](#)
- struct [pdb_adc_pretrigger_config_t](#)
Defines the type of structure for configuring ADC's pre_trigger. [More...](#)

Enumerations

- enum [pdb_load_value_mode_t](#) { PDB_LOAD_VAL_IMMEDIATELY = 0U, PDB_LOAD_VAL_AT_MODULE_COUNTER = 1U, PDB_LOAD_VAL_AT_NEXT_TRIGGER = 2U, PDB_LOAD_VAL_AT_MODULE_COUNTER_OR_NEXT_TRIGGER = 3U }
Defines the type of value load mode for the PDB module.
- enum [pdb_clk_prescaler_div_t](#) { PDB_CLK_PREDIV_BY_1 = 0U, PDB_CLK_PREDIV_BY_2 = 1U, PDB_CLK_PREDIV_BY_4 = 2U, PDB_CLK_PREDIV_BY_8 = 3U, PDB_CLK_PREDIV_BY_16 = 4U, PDB_CLK_PREDIV_BY_32 = 5U, PDB_CLK_PREDIV_BY_64 = 6U, PDB_CLK_PREDIV_BY_128 = 7U }
Defines the type of prescaler divider for the PDB counter clock. Implements : [pdb_clk_prescaler_div_t_Class](#).
- enum [pdb_trigger_src_t](#) { PDB_TRIGGER_IN0 = 0U, PDB_SOFTWARE_TRIGGER = 15U }
Defines the type of trigger source mode for the PDB.
- enum [pdb_clk_prescaler_mult_factor_t](#) { PDB_CLK_PREMULT_FACT_AS_1 = 0U, PDB_CLK_PREMULT_FACT_AS_10 = 1U, PDB_CLK_PREMULT_FACT_AS_20 = 2U, PDB_CLK_PREMULT_FACT_AS_40 = 3U }
Defines the type of the multiplication source mode for PDB.

Functions

- void [PDB_DRV_Init](#) (const uint32_t instance, const [pdb_timer_config_t](#) *userConfigPtr)
Initializes the PDB counter and triggers input.
- void [PDB_DRV_Deinit](#) (const uint32_t instance)
De-initializes the PDB module.
- void [PDB_DRV_GetDefaultConfig](#) ([pdb_timer_config_t](#) *const config)
Gets the default configuration structure of PDB with default settings.
- void [PDB_DRV_Enable](#) (const uint32_t instance)
Enables the PDB module.
- void [PDB_DRV_Disable](#) (const uint32_t instance)
Disables the PDB module.
- void [PDB_DRV_SoftTriggerCmd](#) (const uint32_t instance)
Triggers the PDB with a software trigger.
- uint32_t [PDB_DRV_GetTimerValue](#) (const uint32_t instance)
Gets the current value of the PDB counter.
- bool [PDB_DRV_GetTimerIntFlag](#) (const uint32_t instance)
Gets the PDB interrupt flag.
- void [PDB_DRV_ClearTimerIntFlag](#) (const uint32_t instance)
Clears the interrupt flag.
- void [PDB_DRV_LoadValuesCmd](#) (const uint32_t instance)
Executes the command of loading values.
- void [PDB_DRV_SetTimerModulusValue](#) (const uint32_t instance, const uint16_t value)
Sets the value of timer modulus.
- void [PDB_DRV_SetValueForTimerInterrupt](#) (const uint32_t instance, const uint16_t value)
Sets the value for the timer interrupt.
- void [PDB_DRV_ConfigAdcPreTrigger](#) (const uint32_t instance, const uint32_t chn, const [pdb_adc_pretrigger_config_t](#) *configPtr)
Configures the ADC pre_trigger in the PDB module.
- uint32_t [PDB_DRV_GetAdcPreTriggerFlags](#) (const uint32_t instance, const uint32_t chn, const uint32_t preChnMask)
Gets the ADC pre_trigger flag in the PDB module.
- void [PDB_DRV_ClearAdcPreTriggerFlags](#) (const uint32_t instance, const uint32_t chn, const uint32_t preChnMask)
Clears the ADC pre_trigger flag in the PDB module.
- uint32_t [PDB_DRV_GetAdcPreTriggerSeqErrFlags](#) (const uint32_t instance, const uint32_t chn, const uint32_t preChnMask)
Gets the ADC pre_trigger flag in the PDB module.
- void [PDB_DRV_ClearAdcPreTriggerSeqErrFlags](#) (const uint32_t instance, const uint32_t chn, const uint32_t preChnMask)
Clears the ADC pre_trigger flag in the PDB module.
- void [PDB_DRV_SetAdcPreTriggerDelayValue](#) (const uint32_t instance, const uint32_t chn, const uint32_t preChn, const uint32_t value)
Sets the ADC pre_trigger delay value in the PDB module.
- void [PDB_DRV_SetCmpPulseOutEnable](#) (const uint32_t instance, const uint32_t pulseChnMask, bool enable)
Switches on/off the CMP pulse out in the PDB module.
- void [PDB_DRV_SetCmpPulseOutDelayForHigh](#) (const uint32_t instance, const uint32_t pulseChn, const uint32_t value)
Sets the CMP pulse out delay value for high in the PDB module.
- void [PDB_DRV_SetCmpPulseOutDelayForLow](#) (const uint32_t instance, const uint32_t pulseChn, const uint32_t value)
Sets the CMP pulse out delay value for low in the PDB module.

17.106.2 Data Structure Documentation

17.106.2.1 struct pdb_timer_config_t

Defines the type of structure for basic timer in PDB.

Definition at line 103 of file pdb_driver.h.

Data Fields

- [pdb_load_value_mode_t](#) loadValueMode
- bool [seqErrIntEnable](#)
- [pdb_clk_prescaler_div_t](#) clkPreDiv
- [pdb_clk_prescaler_mult_factor_t](#) clkPreMultFactor
- [pdb_trigger_src_t](#) triggerInput
- bool [continuousModeEnable](#)
- bool [dmaEnable](#)
- bool [intEnable](#)

Field Documentation

17.106.2.1.1 [pdb_clk_prescaler_div_t](#) clkPreDiv

Select the prescaler divider.

Definition at line 107 of file pdb_driver.h.

17.106.2.1.2 [pdb_clk_prescaler_mult_factor_t](#) clkPreMultFactor

Select multiplication factor for prescaler.

Definition at line 108 of file pdb_driver.h.

17.106.2.1.3 bool [continuousModeEnable](#)

Enable the continuous mode.

Definition at line 110 of file pdb_driver.h.

17.106.2.1.4 bool [dmaEnable](#)

Enable the dma for timer.

Definition at line 111 of file pdb_driver.h.

17.106.2.1.5 bool [intEnable](#)

Enable the interrupt for timer. : interrupt is generated only if DMA is disabled.

Definition at line 112 of file pdb_driver.h.

17.106.2.1.6 [pdb_load_value_mode_t](#) loadValueMode

Select the load mode.

Definition at line 105 of file pdb_driver.h.

17.106.2.1.7 bool [seqErrIntEnable](#)

Enable PDB Sequence Error Interrupt.

Definition at line 106 of file pdb_driver.h.

17.106.2.1.8 pdb_trigger_src_t triggerInput

Select the trigger input source.

Definition at line 109 of file pdb_driver.h.

17.106.2.2 struct pdb_adc_pretrigger_config_t

Defines the type of structure for configuring ADC's pre_trigger.

Definition at line 132 of file pdb_driver.h.

Data Fields

- uint32_t [adcPreTriggerIdx](#)
- bool [preTriggerEnable](#)
- bool [preTriggerOutputEnable](#)
- bool [preTriggerBackToBackEnable](#)

Field Documentation

17.106.2.2.1 uint32_t adcPreTriggerIdx

Setting pre_trigger's index.

Definition at line 134 of file pdb_driver.h.

17.106.2.2.2 bool preTriggerBackToBackEnable

Enable the back to back mode for ADC pre_trigger. If enabled, the pretrigger will be activated automatically when the ADC COCO flag corresponding to the previous pretrigger in the chain, is set. The previous pretrigger for pretriggers with index 0, depend on features instanceBackToBackEnable and interchannelBackToBackEnable.

Definition at line 137 of file pdb_driver.h.

17.106.2.2.3 bool preTriggerEnable

Enable the pre_trigger.

Definition at line 135 of file pdb_driver.h.

17.106.2.2.4 bool preTriggerOutputEnable

Enable the pre_trigger output.

Definition at line 136 of file pdb_driver.h.

17.106.3 Enumeration Type Documentation

17.106.3.1 enum pdb_clk_prescaler_div_t

Defines the type of prescaler divider for the PDB counter clock. Implements : `pdb_clk_prescaler_div_t_Class`.

Enumerator

- PDB_CLK_PREDIV_BY_1** Counting divided by 1 x prescaler multiplication factor (selected by MULT).
- PDB_CLK_PREDIV_BY_2** Counting divided by 2 x prescaler multiplication factor (selected by MULT).
- PDB_CLK_PREDIV_BY_4** Counting divided by 4 x prescaler multiplication factor (selected by MULT).
- PDB_CLK_PREDIV_BY_8** Counting divided by 8 x prescaler multiplication factor (selected by MULT).
- PDB_CLK_PREDIV_BY_16** Counting divided by 16 x prescaler multiplication factor (selected by MULT).
- PDB_CLK_PREDIV_BY_32** Counting divided by 32 x prescaler multiplication factor (selected by MULT).

PDB_CLK_PREDIV_BY_64 Counting divided by 64 x prescaler multiplication factor (selected by MULT).

PDB_CLK_PREDIV_BY_128 Counting divided by 128 x prescaler multiplication factor (selected by MULT).

Definition at line 58 of file pdb_driver.h.

17.106.3.2 enum pdb_clk_prescaler_mult_factor_t

Defines the type of the multiplication source mode for PDB.

Selects the multiplication factor of the prescaler divider for the PDB counter clock. Implements : `pdb_clk_prescaler_mult_factor_t_Class`

Enumerator

PDB_CLK_PREMULT_FACT_AS_1 Multiplication factor is 1.

PDB_CLK_PREMULT_FACT_AS_10 Multiplication factor is 10.

PDB_CLK_PREMULT_FACT_AS_20 Multiplication factor is 20.

PDB_CLK_PREMULT_FACT_AS_40 Multiplication factor is 40.

Definition at line 89 of file pdb_driver.h.

17.106.3.3 enum pdb_load_value_mode_t

Defines the type of value load mode for the PDB module.

Some timing related registers, such as the MOD, IDLY, CHnDLYm, INTx and POyDLY, buffer the setting values. Only the load operation is triggered. The setting value is loaded from a buffer and takes effect. There are four loading modes to fit different applications. Implements : `pdb_load_value_mode_t_Class`

Enumerator

PDB_LOAD_VAL_IMMEDIATELY Loaded immediately after load operation.

PDB_LOAD_VAL_AT_MODULO_COUNTER Loaded when counter hits the modulo after load operation.

PDB_LOAD_VAL_AT_NEXT_TRIGGER Loaded when detecting an input trigger after load operation.

PDB_LOAD_VAL_AT_MODULO_COUNTER_OR_NEXT_TRIGGER Loaded when counter hits the modulo or detecting an input trigger after load operation.

Definition at line 42 of file pdb_driver.h.

17.106.3.4 enum pdb_trigger_src_t

Defines the type of trigger source mode for the PDB.

Selects the trigger input source for the PDB. The trigger input source can be internal or the software trigger. Implements : `pdb_trigger_src_t_Class`

Enumerator

PDB_TRIGGER_IN0 Source trigger comes from TRGMUX.

PDB_SOFTWARE_TRIGGER Select software trigger.

Definition at line 77 of file pdb_driver.h.

17.106.4 Function Documentation

17.106.4.1 void PDB_DRV_ClearAdcPreTriggerFlags (const uint32_t instance, const uint32_t chn, const uint32_t preChnMask)

Clears the ADC pre_trigger flag in the PDB module.

This function clears the ADC pre_trigger flags in the PDB module.

Parameters

in	<i>instance</i>	PDB instance ID.
in	<i>chn</i>	PDB channel.
in	<i>preChnMask</i>	ADC pre_trigger channels mask.

Definition at line 379 of file pdb_driver.c.

17.106.4.2 void PDB_DRV_ClearAdcPreTriggerSeqErrFlags (const uint32_t *instance*, const uint32_t *chn*, const uint32_t *preChnMask*)

Clears the ADC pre_trigger flag in the PDB module.

This function clears the ADC pre_trigger sequence error flags in the PDB module.

Parameters

in	<i>instance</i>	PDB instance ID.
in	<i>chn</i>	PDB channel.
in	<i>preChnMask</i>	ADC pre_trigger channels mask.

Definition at line 415 of file pdb_driver.c.

17.106.4.3 void PDB_DRV_ClearTimerIntFlag (const uint32_t *instance*)

Clears the interrupt flag.

This function clears the interrupt flag.

Parameters

in	<i>instance</i>	PDB instance ID.
----	-----------------	------------------

Definition at line 278 of file pdb_driver.c.

17.106.4.4 void PDB_DRV_ConfigAdcPreTrigger (const uint32_t *instance*, const uint32_t *chn*, const pdb_adc_pretrigger_config_t * *configPtr*)

Configures the ADC pre_trigger in the PDB module.

This function configures the ADC pre_trigger in the PDB module. Important note: any pretrigger which is enabled and has the trigger output enabled (preTriggerOutputEnable and preTriggerEnable both true) must have the corresponding delay value set to a non-zero value by calling [PDB_DRV_SetAdcPreTriggerDelayValue](#) function.

Parameters

in	<i>instance</i>	PDB instance ID.
in	<i>chn</i>	PDB channel.
in	<i>configPtr</i>	Pointer to the user configuration structure. See pdb_adc_pretrigger_config_t .

Definition at line 340 of file pdb_driver.c.

17.106.4.5 void PDB_DRV_Deinit (const uint32_t *instance*)

De-initializes the PDB module.

This function de-initializes the PDB module. Calling this function shuts down the PDB module and reduces the power consumption.

Parameters

in	<i>instance</i>	PDB instance ID.
----	-----------------	------------------

Definition at line 136 of file pdb_driver.c.

17.106.4.6 void PDB_DRV_Disable (const uint32_t *instance*)

Disables the PDB module.

This function disables the PDB module, counter is off also.

Parameters

in	<i>instance</i>	PDB instance ID.
----	-----------------	------------------

Definition at line 215 of file pdb_driver.c.

17.106.4.7 void PDB_DRV_Enable (const uint32_t *instance*)

Enables the PDB module.

This function enables the PDB module, counter is on.

Parameters

in	<i>instance</i>	PDB instance ID.
----	-----------------	------------------

Definition at line 200 of file pdb_driver.c.

17.106.4.8 uint32_t PDB_DRV_GetAdcPreTriggerFlags (const uint32_t *instance*, const uint32_t *chn*, const uint32_t *preChnMask*)

Gets the ADC pre_trigger flag in the PDB module.

This function gets the ADC pre_trigger flags in the PDB module.

Parameters

in	<i>instance</i>	PDB instance ID.
in	<i>chn</i>	PDB channel.
in	<i>preChnMask</i>	ADC pre_trigger channels mask.

Returns

Assertion of indicated flag.

Definition at line 361 of file pdb_driver.c.

17.106.4.9 uint32_t PDB_DRV_GetAdcPreTriggerSeqErrFlags (const uint32_t *instance*, const uint32_t *chn*, const uint32_t *preChnMask*)

Gets the ADC pre_trigger flag in the PDB module.

This function gets the ADC pre_trigger flags in the PDB module.

Parameters

in	<i>instance</i>	PDB instance ID.
in	<i>chn</i>	PDB channel.
in	<i>preChnMask</i>	ADC pre_trigger channels mask.

Returns

Assertion of indicated flag.

Definition at line 397 of file pdb_driver.c.

17.106.4.10 void PDB_DRV_GetDefaultConfig (pdb_timer_config_t *const *config*)

Gets the default configuration structure of PDB with default settings.

This function initializes the hardware configuration structure to default values (Reference Manual Resets). This function should be called before configuring the hardware feature by `PDB_DRV_Init()` function, otherwise all members be written by user. This function ensures that all members are written with safe values, but the user still can modify the desired members.

Parameters

<code>out</code>	<code>config</code>	Pointer to PDB configuration structure.
------------------	---------------------	---

Definition at line 164 of file `pdb_driver.c`.

17.106.4.11 `bool PDB_DRV_GetTimerIntFlag (const uint32_t instance)`

Gets the PDB interrupt flag.

This function gets the PDB interrupt flag. It is asserted if the PDB interrupt occurs.

Parameters

<code>in</code>	<code>instance</code>	PDB instance ID.
-----------------	-----------------------	------------------

Returns

Assertion of indicated event.

Definition at line 263 of file `pdb_driver.c`.

17.106.4.12 `uint32_t PDB_DRV_GetTimerValue (const uint32_t instance)`

Gets the current value of the PDB counter.

This function gets the current counter value.

Parameters

<code>in</code>	<code>instance</code>	PDB instance ID.
-----------------	-----------------------	------------------

Returns

Current PDB counter value.

Definition at line 247 of file `pdb_driver.c`.

17.106.4.13 `void PDB_DRV_Init (const uint32_t instance, const pdb_timer_config_t * userConfigPtr)`

Initializes the PDB counter and triggers input.

This function initializes the PDB counter, input triggers and general pre-trigger settings. It resets PDB registers and enables the PDB clock. Therefore, it should be called before any other operation. After it is initialized, the PDB can act as a triggered timer, which enables other features in PDB module.

Parameters

<code>in</code>	<code>instance</code>	PDB instance ID.
<code>in</code>	<code>userConfigPtr</code>	Pointer to the user configuration structure. See the " <code>pdb_user_config_t</code> ".

Definition at line 61 of file `pdb_driver.c`.

17.106.4.14 `void PDB_DRV_LoadValuesCmd (const uint32_t instance)`

Executes the command of loading values.

This function executes the command of loading values.

Parameters

<i>in</i>	<i>instance</i>	PDB instance ID.
-----------	-----------------	------------------

Definition at line 293 of file pdb_driver.c.

17.106.4.15 void PDB_DRV_SetAdcPreTriggerDelayValue (const uint32_t *instance*, const uint32_t *chn*, const uint32_t *preChn*, const uint32_t *value*)

Sets the ADC pre_trigger delay value in the PDB module.

This function sets the ADC pre_trigger delay value in the PDB module.

Parameters

<i>instance</i>	PDB instance ID.
<i>chn</i>	ADC channel.
<i>preChn</i>	ADC pre_channel.
<i>value</i>	Setting value.

Definition at line 433 of file pdb_driver.c.

17.106.4.16 void PDB_DRV_SetCmpPulseOutDelayForHigh (const uint32_t *instance*, const uint32_t *pulseChn*, const uint32_t *value*)

Sets the CMP pulse out delay value for high in the PDB module.

This function sets the CMP pulse out delay value for high in the PDB module.

Parameters

<i>in</i>	<i>instance</i>	PDB instance ID.
<i>in</i>	<i>pulseChn</i>	Pulse channel.
<i>in</i>	<i>value</i>	Setting value.

Definition at line 471 of file pdb_driver.c.

17.106.4.17 void PDB_DRV_SetCmpPulseOutDelayForLow (const uint32_t *instance*, const uint32_t *pulseChn*, const uint32_t *value*)

Sets the CMP pulse out delay value for low in the PDB module.

This function sets the CMP pulse out delay value for low in the PDB module.

Parameters

<i>in</i>	<i>instance</i>	PDB instance ID.
<i>in</i>	<i>pulseChn</i>	Pulse channel.
<i>in</i>	<i>value</i>	Setting value.

Definition at line 489 of file pdb_driver.c.

17.106.4.18 void PDB_DRV_SetCmpPulseOutEnable (const uint32_t *instance*, const uint32_t *pulseChnMask*, bool *enable*)

Switches on/off the CMP pulse out in the PDB module.

This function switches the CMP pulse on/off in the PDB module.

Parameters

<i>in</i>	<i>instance</i>	PDB instance ID.
<i>in</i>	<i>pulseChnMask</i>	Pulse channel mask.

<i>in</i>	<i>enable</i>	Switcher to assert the feature.
-----------	---------------	---------------------------------

Definition at line 454 of file pdb_driver.c.

17.106.4.19 void PDB_DRV_SetTimerModulusValue (const uint32_t *instance*, const uint16_t *value*)

Sets the value of timer modulus.

This function sets the value of timer modulus.

Parameters

<i>in</i>	<i>instance</i>	PDB instance ID.
<i>in</i>	<i>value</i>	Setting value.

Definition at line 308 of file pdb_driver.c.

17.106.4.20 void PDB_DRV_SetValueForTimerInterrupt (const uint32_t *instance*, const uint16_t *value*)

Sets the value for the timer interrupt.

This function sets the value for the timer interrupt.

Parameters

<i>in</i>	<i>instance</i>	PDB instance ID.
<i>in</i>	<i>value</i>	Setting value.

Definition at line 324 of file pdb_driver.c.

17.106.4.21 void PDB_DRV_SoftTriggerCmd (const uint32_t *instance*)

Triggers the PDB with a software trigger.

This function triggers the PDB with a software trigger. When the PDB is set to use the software trigger as input, calling this function triggers the PDB.

Parameters

<i>in</i>	<i>instance</i>	PDB instance ID.
-----------	-----------------	------------------

Definition at line 232 of file pdb_driver.c.

17.107 PHY Framework

17.107.1 Detailed Description

PHY Driver containing API for operating PHYs managed in the PHY framework.

How to use the PHY framework in your application

In order to use the PHY framework in your application, the framework needs to be initialized by calling the **PHY_F↔FrameworkInit()** function. The parameters of this function specify:

- an array of PHY configuration structures;
- an array of pointers to the PHY drivers used by the application.

The configuration of the PHY is specified through the **phy_config_t** structure and contains:

- the PHY driver type used by the current PHY - will refer to an index in the array of drivers (**phyDrivers**);
- the address of the PHY;
- the location (internal/external);
- the role (master/slave/auto);
- the link speed;
- for MDIO/SMI managed devices: clause 45/22 MDIO frames selection;
- the instance number of the ENET module connected to this PHY;
- the callbacks associated with different events (link up/down, autonegotiation complete, autonegotiation failed, sleep request);

extended configuration (PHY specific).

The driver structure (**phy_driver_t**) represents a set of functions used to control the module and must be compatible with the associated device. Currently, the following drivers are implemented:

- TJA110x (**PHY_driver_tja110x**);
- generic driver, supporting IEEE standardized registers (**PHY_driver_generic**).

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\phy\phy.c
${S32SDK_PATH}\platform\drivers\src\phy\phy_generic.c
${S32SDK_PATH}\platform\drivers\src\phy\phy_tja110x.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

Ethernet MAC (ENET)

Examples:

Initializing the framework

```

phy_driver_t* phyDrivers[N_PHY_DRIVERS] = {&PHY_driver_tja110x, &
    PHY_driver_generic};

phy_config_t phyConfig[N_PHY_DEVS] = {
    {
        .type = PHY_TYPE_TJA110X,
        .addr = 4,
        .speed = PHY_SPEED_100_MBPS,
        .location = PHY_LOCATION_EXTERNAL,
        .role = PHY_ROLE_MASTER,
        .enetInstance = 0,
        .linkUpEventCB = NULL,
        .linkDownEventCB = NULL,
        .sleepRequestCB = NULL,
        .autonegCompleteCB = NULL,
        .autonegFailedCB = NULL,
        .extendedConfig = NULL
    },
    {
        .type = PHY_TYPE_GENERIC,
        .addr = 1,
        .speed = PHY_SPEED_AUTONEG,
        .location = PHY_LOCATION_EXTERNAL,
        .role = PHY_ROLE_SLAVE,
        .enetInstance = 0,
        .linkUpEventCB = NULL,
        .linkDownEventCB = NULL,
        .sleepRequestCB = NULL,
        .autonegCompleteCB = NULL,
        .autonegFailedCB = NULL,
        .extendedConfig = NULL
    }
};

int main(void)
{
    /* ... */

    /* Initialize the module */
    PHY_FrameworkInit(phyConfig, phyDrivers);

    /* Initialize the TJA110x PHY */
    PHY_Init(0);
    /* Initialize the generic PHY */
    PHY_Init(1);

    /* ... */
}

```

Important Note

1. When PHY TJA1102 device is used in the application, User must add 2 configurations with PHY TJA110x type. The configurations must be arranged in order TJA1102_P0 then TJA1102_P1. Because TJA1102_P1 is always initialized after TJA1102_P0.
2. With TJA110x: Link down occurs when the link is lost or Phy device is turned off. No link down is reported when disabling link control manually.

Modules

- [Generic PHY](#)

Generic PHY driver for 10/100/1000 PHYs following IEEE 802.3-Clause 22.

- [TJA110x PHY](#)

PHY driver for TJA110x series.

Data Structures

- struct [phy_id_t](#)
PHY ID. [More...](#)
- struct [phy_delay_t](#)
PHY Delay. [More...](#)
- struct [phy_config_t](#)
PHY configuration structure. [More...](#)
- struct [phy_driver_t](#)
Structure containing the APIs of a driver compatible with this PHY framework. [More...](#)

Enumerations

- enum [phy_speed_t](#) {
PHY_SPEED_1_GBPS = 2, PHY_SPEED_100_MBPS = 1, PHY_SPEED_10_MBPS = 0, PHY_SPEED_↔
AUTONEG = -1,
PHY_SPEED_RESERVED = -2 }
Link speed.
- enum [phy_state_t](#) {
PHY_STATE_LINKTRAINING = 7, PHY_STATE_DISABLED = 6, PHY_STATE_SILENT = 5, PHY_STAT↔
E_SLEEPREQ = 4,
PHY_STATE_SLEEP = 3, PHY_STATE_ACTIVE = 2, PHY_STATE_OFF = 1, PHY_STATE_UNKNOWN =
0 }
PHY state.
- enum [phy_role_t](#) { PHY_ROLE_AUTO = 2, PHY_ROLE_MASTER = 1, PHY_ROLE_SLAVE = 0 }
PHY role.
- enum [phy_location_t](#) { PHY_LOCATION_EXTERNAL = 1, PHY_LOCATION_INTERNAL = 0 }
PHY location.
- enum [phy_loopback_t](#) { PHY_LOOPBACK_REMOTE = 3, PHY_LOOPBACK_EXTERNAL = 2, PHY_LOO↔
PBACK_INTERNAL = 1, PHY_LOOPBACK_NONE = 0 }
Loopback modes.

Variables

- [phy_config_t](#) * [g_phyConfig](#)
Pointer to the array of PHY configuration structures.

Driver initialization

- status_t [PHY_FrameworkInit](#) ([phy_config_t](#) *phyConfig, [phy_driver_t](#) **phyDrivers)
Initializes the PHY driver.

Basic PHY functionality

- status_t [PHY_Init](#) (uint8_t phy)
Initializes the specified PHY device.
- status_t [PHY_Reset](#) (uint8_t phy)
Resets the specified PHY device.
- status_t [PHY_MainFunction](#) (uint8_t phy)
Provides polling support, by handling specific events.
- status_t [PHY_GetId](#) (uint8_t phy, [phy_id_t](#) *id)
Gets the ID of the specified PHY device.

- status_t [PHY_GetState](#) (uint8_t phy, [phy_state_t](#) *state)
Gets the current state of the specified PHY device.
- status_t [PHY_GetLinkStatus](#) (uint8_t phy, bool *linkUp)
Gets the link status for the specified PHY device.
- status_t [PHY_GetLinkSpeed](#) (uint8_t phy, [phy_speed_t](#) *speed)
Gets the link speed for the specified PHY device.
- status_t [PHY_GetDelay](#) (uint8_t phy, [phy_delay_t](#) *delay)
Gets the propagation delay within the PHY.
- status_t [PHY_Suspend](#) (uint8_t phy)
Suspends the specified PHY device.
- status_t [PHY_Resume](#) (uint8_t phy)
Resumes the specified PHY device.
- status_t [PHY_SleepAbortReject](#) (uint8_t phy)
Aborts an initiated sleep request or rejects an received sleep request.
- status_t [PHY_Sleep](#) (uint8_t phy)
Sends a sleep request to the specified PHY device.
- status_t [PHY_Wakeup](#) (uint8_t phy)
Wakes up the specified PHY device.
- status_t [PHY_SetRole](#) (uint8_t phy, [phy_role_t](#) role)
Sets the role of the specified PHY device.
- status_t [PHY_SetLoopback](#) (uint8_t phy, [phy_loopback_t](#) loopbackMode)
Sets the loopback mode for the specified PHY device.
- status_t [PHY_SelectTestMode](#) (uint8_t phy, uint8_t testModeIndex)
Sets the test mode for the specified PHY device.
- status_t [PHY_EnableInterrupts](#) (uint8_t phy)
Enables interrupts for the specified PHY device.
- status_t [PHY_HandleInterrupt](#) (uint8_t phy)
Handles interrupts for the specified PHY device.

Auto-negotiation

- status_t [PHY_EnableAutoneg](#) (uint8_t phy)
Enables auto-negotiation for the specified PHY device.
- status_t [PHY_DisableAutoneg](#) (uint8_t phy)
Disables auto-negotiation for the specified PHY device.
- status_t [PHY_RestartAutoneg](#) (uint8_t phy)
Restarts auto-negotiation for the specified PHY device.

Register Access

- status_t [PHY_Write](#) (uint8_t phy, uint8_t registerAddr, uint16_t value)
Writes a register of the specified PHY device.
- status_t [PHY_Read](#) (uint8_t phy, uint8_t registerAddr, uint16_t *value)
Reads a register of the specified PHY device.
- status_t [PHY_RMWW](#) (uint8_t phy, uint8_t registerAddr, uint16_t value, uint16_t mask)
Reads and modifies a register of the specified PHY device.
- status_t [PHY_WriteMMD](#) (uint8_t phy, uint8_t mmd, uint16_t registerAddr, uint16_t value)
Writes a register of the specified PHY device.
- status_t [PHY_ReadMMD](#) (uint8_t phy, uint8_t mmd, uint16_t registerAddr, uint16_t *value)
Reads a register of the specified PHY device.
- status_t [PHY_RMWMMD](#) (uint8_t phy, uint8_t mmd, uint16_t registerAddr, uint16_t value, uint16_t mask)
Reads and modifies a register of the specified PHY device.

17.107.2 Data Structure Documentation

17.107.2.1 struct phy_id_t

PHY ID.

Implements : phy_id_t_Class

Definition at line 114 of file phy.h.

Data Fields

- uint32_t [oui](#)
- uint8_t [typeNo](#)
- uint8_t [revisionNo](#)

Field Documentation

17.107.2.1.1 uint32_t oui

24-bit Organizationally Unique Identifier (OUI)

Definition at line 116 of file phy.h.

17.107.2.1.2 uint8_t revisionNo

Four-bit manufacturer revision number

Definition at line 118 of file phy.h.

17.107.2.1.3 uint8_t typeNo

6-bit manufacturer type number

Definition at line 117 of file phy.h.

17.107.2.2 struct phy_delay_t

PHY Delay.

Implements : phy_delay_t_Class

Definition at line 126 of file phy.h.

Data Fields

- uint32_t [miiToMdiMax](#)
- uint32_t [miiToMdiMin](#)
- uint32_t [mdiToMiiMax](#)
- uint32_t [mdiToMiiMin](#)

Field Documentation

17.107.2.2.1 uint32_t mdiToMiiMax

Maximum propagation delay from MDI to MII

Definition at line 130 of file phy.h.

17.107.2.2.2 uint32_t mdiToMiiMin

Minimum propagation delay from MDI to MII

Definition at line 131 of file phy.h.

17.107.2.2.3 uint32_t miiToMdiMax

Maximum propagation delay from MII to MDI

Definition at line 128 of file phy.h.

17.107.2.2.4 uint32_t miiToMdiMin

Minimum propagation delay from MII to MDI

Definition at line 129 of file phy.h.

17.107.2.3 struct phy_config_t

PHY configuration structure.

Implements : phy_config_t_Class

Definition at line 139 of file phy.h.

Data Fields

- [uint8_t type](#)
- [uint32_t addr](#)
- [phy_location_t location](#)
- [bool clause45](#)
- [phy_speed_t speed](#)
- [phy_role_t role](#)
- [uint8_t enetInstance](#)
- [void\(* linkUpEventCB \)\(uint8_t phy\)](#)
- [void\(* linkDownEventCB \)\(uint8_t phy\)](#)
- [void\(* sleepRequestCB \)\(uint8_t phy\)](#)
- [void\(* autonegCompleteCB \)\(uint8_t p_phy\)](#)
- [void\(* autonegFailedCB \)\(uint8_t p_phy\)](#)
- [bool manualDelay](#)
- [phy_delay_t delay](#)
- [uint32_t privateData](#)
- [void * extendedConfig](#)

Field Documentation**17.107.2.3.1 uint32_t addr**

SMI/MDIO Address for external PHY, Base Address for integrated PHY

Definition at line 142 of file phy.h.

17.107.2.3.2 void(* autonegCompleteCB)(uint8_t p_phy)

Callback for the auto-negotiation complete event

Definition at line 151 of file phy.h.

17.107.2.3.3 void(* autonegFailedCB)(uint8_t p_phy)

Callback for the auto-negotiation failed event

Definition at line 152 of file phy.h.

17.107.2.3.4 bool clause45

For MDIO/SMI managed devices: If true, access is performed using IEEE 802.3 Clause 45 MDIO frames. If false, using IEEE 802.3 Clause 22 MDIO frames

Definition at line 144 of file phy.h.

17.107.2.3.5 phy_delay_t delay

Delay values

Definition at line 154 of file phy.h.

17.107.2.3.6 uint8_t enetInstance

The instance number of the ENET module connected to this PHY

Definition at line 147 of file phy.h.

17.107.2.3.7 void* extendedConfig

Extended configuration (PHY specific)

Definition at line 156 of file phy.h.

17.107.2.3.8 void(* linkDownEventCB) (uint8_t phy)

Callback for the link down event

Definition at line 149 of file phy.h.

17.107.2.3.9 void(* linkUpEventCB) (uint8_t phy)

Callback for the link up event

Definition at line 148 of file phy.h.

17.107.2.3.10 phy_location_t location

Internal: PHY integrated with host device and addressable via memory mapped IO. External: PHY outside of device and addressable via MDIO/SMI

Definition at line 143 of file phy.h.

17.107.2.3.11 bool manualDelay

Delay values are configured statically

Definition at line 153 of file phy.h.

17.107.2.3.12 uint32_t privateData

Private data which can be used by the driver

Definition at line 155 of file phy.h.

17.107.2.3.13 phy_role_t role

Role of the PHY, e.g. Master or Slave

Definition at line 146 of file phy.h.

17.107.2.3.14 void(* sleepRequestCB) (uint8_t phy)

Callback for the sleep request event

Definition at line 150 of file phy.h.

17.107.2.3.15 phy_speed_t speed

Initial speed setting for the PHY

Definition at line 145 of file phy.h.

17.107.2.3.16 uint8_t type

type of driver used for this PHY instance. Will refer to an index in ::gap_phyDrivers

Definition at line 141 of file phy.h.

17.107.2.4 struct phy_driver_t

Structure containing the APIs of a driver compatible with this PHY framework.

Implements : phy_driver_t_Class

Definition at line 164 of file phy.h.

Data Fields

- status_t(* [init](#))(uint8_t phy)
- status_t(* [reset](#))(uint8_t phy)
- status_t(* [mainFunction](#))(uint8_t phy)
- status_t(* [getId](#))(uint8_t phy, [phy_id_t](#) *id)
- status_t(* [getState](#))(uint8_t phy, [phy_state_t](#) *state)
- status_t(* [getLinkStatus](#))(uint8_t phy, bool *linkUp)
- status_t(* [getLinkSpeed](#))(uint8_t phy, [phy_speed_t](#) *speed)
- status_t(* [getDelay](#))(uint8_t phy, [phy_delay_t](#) *delay)
- status_t(* [suspend](#))(uint8_t phy)
- status_t(* [resume](#))(uint8_t phy)
- status_t(* [sleepAbortReject](#))(uint8_t phy)
- status_t(* [sleep](#))(uint8_t phy)
- status_t(* [wakeUp](#))(uint8_t phy)
- status_t(* [setRole](#))(uint8_t phy, [phy_role_t](#) role)
- status_t(* [setLoopback](#))(uint8_t phy, [phy_loopback_t](#) loopbackMode)
- status_t(* [selectTestMode](#))(uint8_t phy, uint8_t testModelIndex)
- status_t(* [enableInterrupts](#))(uint8_t phy)
- status_t(* [handleInterrupt](#))(uint8_t phy)
- status_t(* [enableAutoneg](#))(uint8_t phy)
- status_t(* [disableAutoneg](#))(uint8_t phy)
- status_t(* [restartAutoneg](#))(uint8_t phy)
- status_t(* [write](#))(uint8_t phy, uint8_t registerAddr, uint16_t value)
- status_t(* [read](#))(uint8_t phy, uint8_t registerAddr, uint16_t *value)
- status_t(* [rmw](#))(uint8_t phy, uint8_t registerAddr, uint16_t value, uint16_t mask)
- status_t(* [writeMMD](#))(uint8_t phy, uint8_t mmd, uint16_t registerAddr, uint16_t value)
- status_t(* [readMMD](#))(uint8_t phy, uint8_t mmd, uint16_t registerAddr, uint16_t *value)
- status_t(* [rmwMMD](#))(uint8_t phy, uint8_t mmd, uint16_t registerAddr, uint16_t value, uint16_t mask)

Field Documentation

17.107.2.4.1 status_t(* [disableAutoneg](#))(uint8_t phy)

Definition at line 185 of file phy.h.

17.107.2.4.2 status_t(* [enableAutoneg](#))(uint8_t phy)

Definition at line 184 of file phy.h.

17.107.2.4.3 status_t(* [enableInterrupts](#))(uint8_t phy)

Definition at line 182 of file phy.h.

17.107.2.4.4 status_t(* [getDelay](#))(uint8_t phy, [phy_delay_t](#) *delay)

Definition at line 173 of file phy.h.

17.107.2.4.5 `status_t(* getld) (uint8_t phy, phy_id_t *id)`

Definition at line 169 of file phy.h.

17.107.2.4.6 `status_t(* getLinkSpeed) (uint8_t phy, phy_speed_t *speed)`

Definition at line 172 of file phy.h.

17.107.2.4.7 `status_t(* getLinkStatus) (uint8_t phy, bool *linkUp)`

Definition at line 171 of file phy.h.

17.107.2.4.8 `status_t(* getState) (uint8_t phy, phy_state_t *state)`

Definition at line 170 of file phy.h.

17.107.2.4.9 `status_t(* handleInterrupt) (uint8_t phy)`

Definition at line 183 of file phy.h.

17.107.2.4.10 `status_t(* init) (uint8_t phy)`

Definition at line 166 of file phy.h.

17.107.2.4.11 `status_t(* mainFunction) (uint8_t phy)`

Definition at line 168 of file phy.h.

17.107.2.4.12 `status_t(* read) (uint8_t phy, uint8_t registerAddr, uint16_t *value)`

Definition at line 188 of file phy.h.

17.107.2.4.13 `status_t(* readMMD) (uint8_t phy, uint8_t mmd, uint16_t registerAddr, uint16_t *value)`

Definition at line 191 of file phy.h.

17.107.2.4.14 `status_t(* reset) (uint8_t phy)`

Definition at line 167 of file phy.h.

17.107.2.4.15 `status_t(* restartAutoneg) (uint8_t phy)`

Definition at line 186 of file phy.h.

17.107.2.4.16 `status_t(* resume) (uint8_t phy)`

Definition at line 175 of file phy.h.

17.107.2.4.17 `status_t(* rmw) (uint8_t phy, uint8_t registerAddr, uint16_t value, uint16_t mask)`

Definition at line 189 of file phy.h.

17.107.2.4.18 `status_t(* rmwMMD) (uint8_t phy, uint8_t mmd, uint16_t registerAddr, uint16_t value, uint16_t mask)`

Definition at line 192 of file phy.h.

17.107.2.4.19 `status_t(* selectTestMode) (uint8_t phy, uint8_t testModelIndex)`

Definition at line 181 of file phy.h.

17.107.2.4.20 `status_t(* setLoopback)(uint8_t phy, phy_loopback_t loopbackMode)`

Definition at line 180 of file phy.h.

17.107.2.4.21 `status_t(* setRole)(uint8_t phy, phy_role_t role)`

Definition at line 179 of file phy.h.

17.107.2.4.22 `status_t(* sleep)(uint8_t phy)`

Definition at line 177 of file phy.h.

17.107.2.4.23 `status_t(* sleepAbortReject)(uint8_t phy)`

Definition at line 176 of file phy.h.

17.107.2.4.24 `status_t(* suspend)(uint8_t phy)`

Definition at line 174 of file phy.h.

17.107.2.4.25 `status_t(* wakeup)(uint8_t phy)`

Definition at line 178 of file phy.h.

17.107.2.4.26 `status_t(* write)(uint8_t phy, uint8_t registerAddr, uint16_t value)`

Definition at line 187 of file phy.h.

17.107.2.4.27 `status_t(* writeMMD)(uint8_t phy, uint8_t mmd, uint16_t registerAddr, uint16_t value)`

Definition at line 190 of file phy.h.

17.107.3 Enumeration Type Documentation

17.107.3.1 `enum phy_location_t`

PHY location.

Implements : `phy_location_t_Class`

Enumerator

`PHY_LOCATION_EXTERNAL` External PHY

`PHY_LOCATION_INTERNAL` Internal PHY

Definition at line 90 of file phy.h.

17.107.3.2 `enum phy_loopback_t`

Loopback modes.

Implements : `phy_loopback_t_Class`

Enumerator

`PHY_LOOPBACK_REMOTE` Remote loopback

`PHY_LOOPBACK_EXTERNAL` External loopback

`PHY_LOOPBACK_INTERNAL` Internal loopback

`PHY_LOOPBACK_NONE` No loopback

Definition at line 101 of file phy.h.

17.107.3.3 enum phy_role_t

PHY role.

Implements : phy_role_t_Class

Enumerator

PHY_ROLE_AUTO Automatic configuration, i.e. use the default of the device. Could be pin strapping or auto-negotiation of master/slave parameter.

PHY_ROLE_MASTER Master

PHY_ROLE_SLAVE Slave

Definition at line 78 of file phy.h.

17.107.3.4 enum phy_speed_t

Link speed.

Implements : phy_speed_t_Class

Enumerator

PHY_SPEED_1_GBPS 1 Gbps

PHY_SPEED_100_MBPS 100 Mbps

PHY_SPEED_10_MBPS 10 Mbps

PHY_SPEED_AUTONEG Auto-negotiation

PHY_SPEED_RESERVED Reserved

Definition at line 46 of file phy.h.

17.107.3.5 enum phy_state_t

PHY state.

Implements : phy_state_t_Class

Enumerator

PHY_STATE_LINKTRAINING PHY is in link training mode

PHY_STATE_DISABLED PHY disabled

PHY_STATE_SILENT PHY in silent mode

PHY_STATE_SLEEPREQ PHY in sleep request state

PHY_STATE_SLEEP PHY in low power sleep mode

PHY_STATE_ACTIVE PHY active/normal mode

PHY_STATE_OFF PHY switched off/standby/power down

PHY_STATE_UNKNOWN PHY state unknown, e.g. during state transition

Definition at line 60 of file phy.h.

17.107.4 Function Documentation

17.107.4.1 status_t PHY_DisableAutoneg (uint8_t phy)

Disables auto-negotiation for the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
----	------------	---

Definition at line 349 of file phy.c.

17.107.4.2 status_t PHY_EnableAutoneg (uint8_t *phy*)

Enables auto-negotiation for the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
----	------------	---

Definition at line 337 of file phy.c.

17.107.4.3 status_t PHY_EnableInterrupts (uint8_t *phy*)

Enables interrupts for the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
----	------------	---

Definition at line 313 of file phy.c.

17.107.4.4 status_t PHY_FrameworkInit (phy_config_t * *phyConfig*, phy_driver_t ** *phyDrivers*)

Initializes the PHY driver.

This function initializes the internal state of the driver and enables the MDIO interface. Important: PHY_FrameworkInit must be invoked prior to using the rest of the API.

Parameters

in	<i>phyConfig</i>	Array of PHY configuration structures.
in	<i>phyDrivers</i>	Array of pointers to the PHY drivers used by the application.

Definition at line 105 of file phy.c.

17.107.4.5 status_t PHY_GetDelay (uint8_t *phy*, phy_delay_t * *delay*)

Gets the propagation delay within the PHY.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
out	<i>delay</i>	The PHY propagation delays

Definition at line 205 of file phy.c.

17.107.4.6 status_t PHY_GetId (uint8_t *phy*, phy_id_t * *id*)

Gets the ID of the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
out	<i>id</i>	The ID of the PHY.

Definition at line 157 of file phy.c.

17.107.4.7 status_t PHY_GetLinkSpeed (uint8_t *phy*, phy_speed_t * *speed*)

Gets the link speed for the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
out	<i>speed</i>	The link speed.

Definition at line 193 of file phy.c.

17.107.4.8 `status_t PHY_GetLinkStatus (uint8_t phy, bool * linkUp)`

Gets the link status for the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
out	<i>linkUp</i>	The link status.

Definition at line 181 of file phy.c.

17.107.4.9 `status_t PHY_GetState (uint8_t phy, phy_state_t * state)`

Gets the current state of the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
out	<i>state</i>	The current state of the PHY

Definition at line 169 of file phy.c.

17.107.4.10 `status_t PHY_HandleInterrupt (uint8_t phy)`

Handles interrupts for the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
----	------------	---

Definition at line 325 of file phy.c.

17.107.4.11 `status_t PHY_Init (uint8_t phy)`

Initializes the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
----	------------	---

Definition at line 121 of file phy.c.

17.107.4.12 `status_t PHY_MainFunction (uint8_t phy)`

Provides polling support, by handling specific events.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
----	------------	---

Definition at line 145 of file phy.c.

17.107.4.13 `status_t PHY_Read (uint8_t phy, uint8_t registerAddr, uint16_t * value)`

Reads a register of the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
in	<i>registerAddr</i>	The address of the register to be read.
out	<i>value</i>	The value of the register.

Definition at line 395 of file phy.c.

17.107.4.14 `status_t PHY_ReadMMD (uint8_t phy, uint8_t mmd, uint16_t registerAddr, uint16_t * value)`

Reads a register of the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
in	<i>mmd</i>	The MMD index of the target register.
in	<i>registerAddr</i>	The address of the register to be read.
out	<i>value</i>	The value of the register.

Definition at line 497 of file phy.c.

17.107.4.15 `status_t PHY_Reset (uint8_t phy)`

Resets the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
----	------------	---

Definition at line 133 of file phy.c.

17.107.4.16 `status_t PHY_RestartAutoneg (uint8_t phy)`

Restarts auto-negotiation for the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
----	------------	---

Definition at line 361 of file phy.c.

17.107.4.17 `status_t PHY_Resume (uint8_t phy)`

Resumes the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
----	------------	---

Definition at line 229 of file phy.c.

17.107.4.18 `status_t PHY_RMW (uint8_t phy, uint8_t registerAddr, uint16_t value, uint16_t mask)`

Reads and modifies a register of the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
in	<i>registerAddr</i>	The address of the register to be written.
in	<i>value</i>	The value to be written.
in	<i>mask</i>	The mask representing the bits which should be modified.

Definition at line 417 of file phy.c.

17.107.4.19 `status_t PHY_RMWMMD (uint8_t phy, uint8_t mmd, uint16_t registerAddr, uint16_t value, uint16_t mask)`

Reads and modifies a register of the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
in	<i>mmd</i>	The MMD index of the target register.
in	<i>registerAddr</i>	The address of the register to be written.
in	<i>value</i>	The value to be written.
in	<i>mask</i>	The mask representing the bits which should be modified.

Definition at line 542 of file phy.c.

17.107.4.20 `status_t PHY_SelectTestMode (uint8_t phy, uint8_t testModelIndex)`

Sets the test mode for the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
in	<i>testModelIndex</i>	Index of the test mode to be started. 0 means no test mode.

Definition at line 301 of file phy.c.

17.107.4.21 `status_t PHY_SetLoopback (uint8_t phy, phy_loopback_t loopbackMode)`

Sets the loopback mode for the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
in	<i>loopbackMode</i>	The loopback type to be configured.

Definition at line 289 of file phy.c.

17.107.4.22 `status_t PHY_SetRole (uint8_t phy, phy_role_t role)`

Sets the role of the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
in	<i>role</i>	The role to be selected for the PHY.

Definition at line 277 of file phy.c.

17.107.4.23 `status_t PHY_Sleep (uint8_t phy)`

Sends a sleep request to the specified PHY device.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
----	------------	---

Definition at line 253 of file phy.c.

17.107.4.24 `status_t PHY_SleepAbortReject (uint8_t phy)`

Aborts an initiated sleep request or rejects an received sleep request.

Parameters

in	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
----	------------	---

Definition at line 241 of file phy.c.

17.107.4.25 `status_t PHY_Suspend (uint8_t phy)`

Suspends the specified PHY device.

Parameters

<i>in</i>	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
-----------	------------	---

Definition at line 217 of file phy.c.

17.107.4.26 `status_t PHY_Wakeup (uint8_t phy)`

Wakes up the specified PHY device.

Parameters

<i>in</i>	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
-----------	------------	---

Definition at line 265 of file phy.c.

17.107.4.27 `status_t PHY_Write (uint8_t phy, uint8_t registerAddr, uint16_t value)`

Writes a register of the specified PHY device.

Parameters

<i>in</i>	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
<i>in</i>	<i>registerAddr</i>	The address of the register to be written.
<i>in</i>	<i>value</i>	The value to be written.

Definition at line 373 of file phy.c.

17.107.4.28 `status_t PHY_WriteMMD (uint8_t phy, uint8_t mmd, uint16_t registerAddr, uint16_t value)`

Writes a register of the specified PHY device.

Parameters

<i>in</i>	<i>phy</i>	The device number, representing the index in the array of PHY configurations.
<i>in</i>	<i>mmd</i>	The MMD index of the target register.
<i>in</i>	<i>registerAddr</i>	The address of the register to be written.
<i>in</i>	<i>value</i>	The value to be written.

Definition at line 451 of file phy.c.

17.107.5 Variable Documentation

17.107.5.1 `phy_config_t* g_phyConfig`

Pointer to the array of PHY configuration structures.

Pointer to the array of PHY configuration structures.

Definition at line 92 of file phy.c.

17.108 PINS Driver

17.108.1 Detailed Description

This section describes the programming interface of the PINS driver.

Data Structures

- struct [pin_settings_config_t](#)
Defines the converter configuration. [More...](#)

Typedefs

- typedef uint8_t [pins_level_type_t](#)
Type of a port levels representation. Implements : [pins_level_type_t_Class](#).

Enumerations

- enum [port_data_direction_t](#) { [GPIO_INPUT_DIRECTION](#) = 0x0U, [GPIO_OUTPUT_DIRECTION](#) = 0x1U, [GPIO_UNSPECIFIED_DIRECTION](#) = 0x2U }
Configures the port data direction Implements : [port_data_direction_t_Class](#).

PINS DRIVER API.

- status_t [PINS_DRV_Init](#) (uint32_t pinCount, const [pin_settings_config_t](#) config[])
Initializes the pins with the given configuration structure.
- void [PINS_DRV_WritePin](#) (GPIO_Type *const base, pins_channel_type_t pin, [pins_level_type_t](#) value)
Write a pin of a port with a given value.
- void [PINS_DRV_WritePins](#) (GPIO_Type *const base, pins_channel_type_t pins)
Write all pins of a port.
- pins_channel_type_t [PINS_DRV_GetPinsOutput](#) (const GPIO_Type *const base)
Get the current output from a port.
- void [PINS_DRV_SetPins](#) (GPIO_Type *const base, pins_channel_type_t pins)
Write pins with 'Set' value.
- void [PINS_DRV_ClearPins](#) (GPIO_Type *const base, pins_channel_type_t pins)
Write pins to 'Clear' value.
- void [PINS_DRV_TogglePins](#) (GPIO_Type *const base, pins_channel_type_t pins)
Toggle pins value.
- pins_channel_type_t [PINS_DRV_ReadPins](#) (const GPIO_Type *const base)
Read input pins.

17.108.2 Data Structure Documentation

17.108.2.1 struct pin_settings_config_t

Defines the converter configuration.

This structure is used to configure the pins Implements : [pin_settings_config_t_Class](#)

Definition at line 565 of file [pins_driver.h](#).

Data Fields

- uint32_t [pinPortIdx](#)
- port_mux_t [mux](#)
Pin (C55: Out) mux selection.
- GPIO_Type * [gpioBase](#)
- [port_data_direction_t](#) [direction](#)
- [pins_level_type_t](#) [initValue](#)

Field Documentation

17.108.2.1.1 [port_data_direction_t](#) [direction](#)

Configures the port data direction.

Definition at line 602 of file pins_driver.h.

17.108.2.1.2 [GPIO_Type*](#) [gpioBase](#)

GPIO base pointer.

Definition at line 601 of file pins_driver.h.

17.108.2.1.3 [pins_level_type_t](#) [initValue](#)

Initial value

Definition at line 638 of file pins_driver.h.

17.108.2.1.4 [port_mux_t](#) [mux](#)

Pin (C55: Out) mux selection.

Definition at line 588 of file pins_driver.h.

17.108.2.1.5 [uint32_t](#) [pinPortIdx](#)

Port pin number.

Definition at line 572 of file pins_driver.h.

17.108.3 Typedef Documentation

17.108.3.1 [typedef uint8_t](#) [pins_level_type_t](#)

Type of a port levels representation. Implements : [pins_level_type_t_Class](#).

Definition at line 53 of file pins_driver.h.

17.108.4 Enumeration Type Documentation

17.108.4.1 [enum](#) [port_data_direction_t](#)

Configures the port data direction Implements : [port_data_direction_t_Class](#).

Enumerator

[GPIO_INPUT_DIRECTION](#) General purpose input direction.

[GPIO_OUTPUT_DIRECTION](#) General purpose output direction.

[GPIO_UNSPECIFIED_DIRECTION](#) General purpose unspecified direction.

Definition at line 59 of file pins_driver.h.

17.108.5 Function Documentation

17.108.5.1 void PINS_DRV_ClearPins (GPIO_Type *const base, pins_channel_type_t pins)

Write pins to 'Clear' value.

This function configures output pins listed in parameter pins (bits that are '1') to have a 'cleared' value (LOW). Pins corresponding to '0' will be unaffected.

Parameters

in	base	GPIO base pointer (PTA, PTB, PTC, etc.)
in	pins	Pin mask of bits to be cleared. Each bit represents one pin (LSB is pin 0, MSB is pin 31). For each bit: <ul style="list-style-type: none"> • 0: corresponding pin is unaffected • 1: corresponding pin is cleared(set to LOW)

Definition at line 526 of file pins_driver.c.

17.108.5.2 pins_channel_type_t PINS_DRV_GetPinsOutput (const GPIO_Type *const base)

Get the current output from a port.

This function returns the current output that is written to a port. Only pins that are configured as output will have meaningful values.

Parameters

in	base	GPIO base pointer (PTA, PTB, PTC, etc.)
----	------	---

Returns

GPIO outputs. Each bit represents one pin (LSB is pin 0, MSB is pin 31). For each bit:

- 0: corresponding pin is set to LOW
- 1: corresponding pin is set to HIGH

Definition at line 497 of file pins_driver.c.

17.108.5.3 status_t PINS_DRV_Init (uint32_t pinCount, const pin_settings_config_t config[])

Initializes the pins with the given configuration structure.

This function configures the pins with the options provided in the provided structure.

Parameters

in	pinCount	The number of configured pins in structure
in	config	The configuration structure

Returns

The status of the operation

Definition at line 50 of file pins_driver.c.

17.108.5.4 pins_channel_type_t PINS_DRV_ReadPins (const GPIO_Type *const base)

Read input pins.

This function returns the current input values from a port. Only pins configured as input will have meaningful values.

Parameters

<i>in</i>	<i>base</i>	GPIO base pointer (PTA, PTB, PTC, etc.)
-----------	-------------	---

Returns

GPIO inputs. Each bit represents one pin (LSB is pin 0, MSB is pin 31). For each bit:

- 0: corresponding pin is read as LOW
- 1: corresponding pin is read as HIGH

Definition at line 554 of file pins_driver.c.

17.108.5.5 void PINS_DRV_SetPins (GPIO_Type *const *base*, pins_channel_type_t *pins*)

Write pins with 'Set' value.

This function configures output pins listed in parameter *pins* (bits that are '1') to have a value of 'set' (HIGH). Pins corresponding to '0' will be unaffected.

Parameters

<i>in</i>	<i>base</i>	GPIO base pointer (PTA, PTB, PTC, etc.)
<i>in</i>	<i>pins</i>	Pin mask of bits to be set. Each bit represents one pin (LSB is pin 0, MSB is pin 31). For each bit: <ul style="list-style-type: none"> • 0: corresponding pin is unaffected • 1: corresponding pin is set to HIGH

Definition at line 511 of file pins_driver.c.

17.108.5.6 void PINS_DRV_TogglePins (GPIO_Type *const *base*, pins_channel_type_t *pins*)

Toggle pins value.

This function toggles output pins listed in parameter *pins* (bits that are '1'). Pins corresponding to '0' will be unaffected.

Parameters

<i>in</i>	<i>base</i>	GPIO base pointer (PTA, PTB, PTC, etc.)
<i>in</i>	<i>pins</i>	Pin mask of bits to be toggled. Each bit represents one pin (LSB is pin 0, MSB is pin 31). For each bit: <ul style="list-style-type: none"> • 0: corresponding pin is unaffected • 1: corresponding pin is toggled

Definition at line 540 of file pins_driver.c.

17.108.5.7 void PINS_DRV_WritePin (GPIO_Type *const *base*, pins_channel_type_t *pin*, pins_level_type_t *value*)

Write a pin of a port with a given value.

This function writes the given pin from a port, with the given value ('0' represents LOW, '1' represents HIGH).

Parameters

<i>in</i>	<i>base</i>	GPIO base pointer (PTA, PTB, PTC, etc.)
-----------	-------------	---

in	<i>pin</i>	Pin number to be written
in	<i>value</i>	Pin value to be written <ul style="list-style-type: none">• 0: corresponding pin is set to LOW• 1: corresponding pin is set to HIGH

Definition at line 468 of file pins_driver.c.

17.108.5.8 void PINS_DRV_WritePins (GPIO_Type *const *base*, pins_channel_type_t *pins*)

Write all pins of a port.

This function writes all pins configured as output with the values given in the parameter pins. '0' represents LOW, '1' represents HIGH.

Parameters

in	<i>base</i>	GPIO base pointer (PTA, PTB, PTC, etc.)
in	<i>pins</i>	Pin mask to be written <ul style="list-style-type: none">• 0: corresponding pin is set to LOW• 1: corresponding pin is set to HIGH

Definition at line 483 of file pins_driver.c.

17.109 Peripheral access layer for S32K148

This module covers all memory mapped register available on SoC.

17.110 Pins Driver (PINS)

17.110.1 Detailed Description

The S32 SDK provides Peripheral Drivers for the PINS module of S32K1xx, S32MTV, S32V234, MPC574xx and S32Rx7x devices.

The module provides dedicated pad control to general-purpose pads that can be configured as either inputs or outputs. The PINS module provides registers that enable user software to read values from GPIO pads configured as inputs, and write values to GPIO pads configured as outputs:

- When configured as output, you can write to an internal register to control the state driven on the associated output pad.
- When configured as input, you can detect the state of the associated pad by reading the value from an internal register.
- When configured as input and output, the pad value can be read back, which can be used as a method of checking if the written value appeared on the pad.

The PINS supports these following features: For S32K1xx and S32MTV devices: Pins driver is based on PORT (Port Control and Interrupt) and GPIO (General-Purpose Input/Output) modules Pin interrupt

- Interrupt flag and enable registers for each pin
- Support for edge sensitive (rising, falling, both) or level sensitive (low, high) configured per pin
- Support for interrupt or DMA request configured per pin
- Asynchronous wake-up in low-power modes
- Pin interrupt is functional in all digital pin muxing modes
- Peripheral trigger output (active high, low) configured per pin Digital input filter
- Digital input filter for each pin, usable by any digital peripheral muxed onto the pin
- Individual enable or bypass control field per pin
- Selectable clock source for digital input filter with a five bit resolution on filter size
- Functional in all digital pin multiplexing modes Port control
- Individual pull control fields with pullup, pulldown, and pull-disable support
- Individual drive strength field supporting high and low drive strength
- Individual slew rate field supporting fast and slow slew rates
- Individual input passive filter field supporting enable and disable of the individual input passive filter
- Individual open drain field supporting enable and disable of the individual open drain output
- Individual over-current detect enable with over-current detect flag and associated interrupt
- Individual mux control field supporting analog or pin disabled, GPIO, and up to 6 chip-specific digital functions
- Pad configuration fields are functional in all digital pin muxing modes For S32V234, MPC574xx and S32Rx7x devices: Pins driver is based on SIUL2 (System Integration Unit Lite2) module The System Integration Unit Lite2 supports these distinctive features:
 - 1 to 32 GPIO ports with data control
 - Drive data to as many as 16 independent I/O channels
 - Sample data from as many as 16 independent I/O channels Two 16-bit registers can be read/written with one access for a 32-bit port, if needed. External interrupt/DMA request support with:

- 1 to 4 system interrupt vectors for 1 to 4 interrupt sources with independent interrupt masks. For 32 external interrupt sources (REQ pins), four groups have eight interrupt sources each, and each of the four groups is assigned one system interrupt vector.
- 1 to 32 programmable digital glitch filters, one for each REQ pin
- 1 to 4 system DMA request channels up to 32 REQ pins, depending on device using
- Edge detection Additionally the SIUL2 contains the Multiplexed Signal Configuration Registers (MSCR) that configure the electrical parameters and settings for as many as 512 functional pads. The number of these registers that is actually implemented varies by device. These registers configure the following pad features:
 - Drive strength
 - Output impedance control
 - Open drain/source output enable
 - Slew rate control
 - Hysteresis control
 - Inversion control
 - Internal pull control and pull selection
 - Pin function assignment
 - Control of analog path switches
 - Safe mode behavior configuration

Modules

- [PINS Driver](#)

17.111 Power Manager

17.111.1 Detailed Description

The S32 SDK Power Manager provides a set of API/services that enables applications to configure and select among various operational and low power modes.

Driver consideration

The Power Manager driver is developed on top of an appropriate hardware access layer. The Power Manager provides API to handle the device power modes. It also supports run-time switching between multiple power modes. Each power mode is described by configuration structures with multiple power-related options. The Power Manager provides a notification mechanism for registered callbacks and API for static and dynamic callback registration.

The Driver uses structures for configuration. The actual format of the structure is defined by the underlying device specific header file. There is a power mode and a callback configuration structure. These structures may be generated using Processor Expert. The user application can use the default for most settings, changing only what is necessary.

This driver provides functions for initializing power manager and changing the power mode.

All methods that access the hardware layer will return an error code to signal if the operation succeeded or failed. The values are defined by the `status_t` enumeration, and the possible values include: success, switch error, callback notification errors, wrong clock setup error.

Modules

- [Power Manager Driver](#)

This module covers the device-specific power_manager functionality implemented for S32K1xx, s32k14xW and S32MTV SOC.

- [Power_s32k1xx](#)

Data Structures

- struct [power_manager_notify_struct_t](#)
Power mode user configuration structure. [More...](#)
- struct [power_manager_callback_user_config_t](#)
callback configuration structure [More...](#)
- struct [power_manager_state_t](#)
Power manager internal state structure. [More...](#)

Typedefs

- typedef void [power_manager_callback_data_t](#)
Callback-specific data.
- typedef status_t(* [power_manager_callback_t](#)) ([power_manager_notify_struct_t](#) *notify, [power_manager_callback_data_t](#) *dataPtr)
Callback prototype.

Enumerations

- enum [power_manager_policy_t](#) { [POWER_MANAGER_POLICY_AGREEMENT](#), [POWER_MANAGER_POLICY_FORCIBLE](#) }
- enum [power_manager_notify_t](#) { [POWER_MANAGER_NOTIFY_RECOVER](#) = 0x00U, [POWER_MANAGER_NOTIFY_BEFORE](#) = 0x01U, [POWER_MANAGER_NOTIFY_AFTER](#) = 0x02U }

The PM notification type. Used to notify registered callbacks. Callback notifications can be invoked in following situations:

- enum `power_manager_callback_type_t` { `POWER_MANAGER_CALLBACK_BEFORE` = 0x01U, `POWER_MANAGER_CALLBACK_AFTER` = 0x02U, `POWER_MANAGER_CALLBACK_BEFORE_AFTER` = 0x03U }

The callback type indicates when a callback will be invoked.

Functions

- status_t `POWER_SYS_Init` (`power_manager_user_config_t` *(*powerConfigsPtr)[], uint8_t configsNumber, `power_manager_callback_user_config_t` *(*callbacksPtr)[], uint8_t callbacksNumber)
Power manager initialization for operation.
- status_t `POWER_SYS_Deinit` (void)
This function deinitializes the Power manager.
- status_t `POWER_SYS_SetMode` (uint8_t powerModelIndex, `power_manager_policy_t` policy)
This function configures the power mode.
- status_t `POWER_SYS_GetLastMode` (uint8_t *powerModelIndexPtr)
This function returns the last successfully set power mode.
- status_t `POWER_SYS_GetLastModeConfig` (`power_manager_user_config_t` **powerModePtr)
This function returns the user configuration structure of the last successfully set power mode.
- `power_manager_modes_t` `POWER_SYS_GetCurrentMode` (void)
This function returns currently running power mode.
- uint8_t `POWER_SYS_GetErrorCallbackIndex` (void)
This function returns the last failed notification callback.
- `power_manager_callback_user_config_t` * `POWER_SYS_GetErrorCallback` (void)
This function returns the callback configuration structure for the last failed notification.
- void `POWER_SYS_GetDefaultConfig` (`power_manager_user_config_t` *const config)
This function returns the default power_manager configuration structure.

Variables

- `power_manager_state_t` `gPowerManagerState`
Power manager internal structure.

17.111.2 Data Structure Documentation

17.111.2.1 struct power_manager_notify_struct_t

Power mode user configuration structure.

This structure defines power mode with additional power options. This structure is implementation-defiend. Please refer to actual definition based on the underlying HAL (SMC, MC_ME etc). Applications may define multiple power modes and switch between them. A list of all defined power modes is passed to the Power manager during initialization as an array of references to structures of this type (see `POWER_SYS_Init()`). Power modes can be switched by calling `POWER_SYS_SetMode()`, which takes as argument the index of the requested power mode in the list passed during manager initialization. The power mode currently in use can be retrieved by calling `POWER_SYS_GetLastMode()`, which provides the index of the current power mode, or by calling `POWER_SYS_GetLastModeConfig()`, which provides a pointer to the configuration structure of the current power mode. The members of the power mode configuration structure depend on power options available for a specific chip, and includes at least the power mode. The available power modes are chip-specific. See `power_manager_modes_t` defined in the underlying HAL for a list of all supported modes.

Power notification structure passed to registered callback function

Implements `power_manager_notify_struct_t_Class`

Definition at line 140 of file `power_manager.h`.

Data Fields

- [power_manager_user_config_t * targetPowerConfigPtr](#)
- [uint8_t targetPowerConfigIndex](#)
- [power_manager_policy_t policy](#)
- [power_manager_notify_t notifyType](#)

Field Documentation

17.111.2.1.1 power_manager_notify_t notifyType

Power mode notification type.

Definition at line 145 of file power_manager.h.

17.111.2.1.2 power_manager_policy_t policy

Power mode transition policy.

Definition at line 144 of file power_manager.h.

17.111.2.1.3 uint8_t targetPowerConfigIndex

Target power configuration index.

Definition at line 143 of file power_manager.h.

17.111.2.1.4 power_manager_user_config_t* targetPowerConfigPtr

Pointer to target power configuration

Definition at line 142 of file power_manager.h.

17.111.2.2 struct power_manager_callback_user_config_t

callback configuration structure

This structure holds configuration of callbacks passed to the Power manager during its initialization. Structures of this type are expected to be statically allocated. This structure contains following application-defined data: callback - pointer to the callback function callbackType - specifies when the callback is called callbackData - pointer to the data passed to the callback Implements power_manager_callback_user_config_t_Class

Definition at line 185 of file power_manager.h.

Data Fields

- [power_manager_callback_t callbackFunction](#)
- [power_manager_callback_type_t callbackType](#)
- [power_manager_callback_data_t * callbackData](#)

Field Documentation

17.111.2.2.1 power_manager_callback_data_t* callbackData

Definition at line 189 of file power_manager.h.

17.111.2.2.2 power_manager_callback_t callbackFunction

Definition at line 187 of file power_manager.h.

17.111.2.2.3 power_manager_callback_type_t callbackType

Definition at line 188 of file power_manager.h.

17.111.2.3 struct power_manager_state_t

Power manager internal state structure.

Power manager internal structure. Contains data necessary for Power manager proper functionality. Stores references to registered power mode configurations, callbacks, and other internal data. This structure is statically allocated and initialized by `POWER_SYS_Init()`. Implements `power_manager_state_t_Class`

Definition at line 201 of file `power_manager.h`.

Data Fields

- `power_manager_user_config_t` `*(* configs)[]`
- `uint8_t configsNumber`
- `power_manager_callback_user_config_t` `*(* staticCallbacks)[]`
- `uint8_t staticCallbacksNumber`
- `uint8_t errorCallbackIndex`
- `uint8_t currentConfig`

Field Documentation

17.111.2.3.1 power_manager_user_config_t*(* configs)[]

Pointer to power configure table.

Definition at line 203 of file `power_manager.h`.

17.111.2.3.2 uint8_t configsNumber

Number of power configurations

Definition at line 204 of file `power_manager.h`.

17.111.2.3.3 uint8_t currentConfig

Index of current configuration.

Definition at line 208 of file `power_manager.h`.

17.111.2.3.4 uint8_t errorCallbackIndex

Index of callback returns error.

Definition at line 207 of file `power_manager.h`.

17.111.2.3.5 power_manager_callback_user_config_t*(* staticCallbacks)[]

Pointer to callback table.

Definition at line 205 of file `power_manager.h`.

17.111.2.3.6 uint8_t staticCallbacksNumber

Max. number of callback configurations

Definition at line 206 of file `power_manager.h`.

17.111.3 Typedef Documentation

17.111.3.1 typedef void power_manager_callback_data_t

Callback-specific data.

Pointer to data of this type is passed during callback registration. The pointer is part of the [power_manager_callback_user_config_t](#) structure and is passed to the callback during power mode change notifications. Implements `power_manager_callback_data_t_Class`

Definition at line 115 of file `power_manager.h`.

```
17.111.3.2 typedef status_t(* power_manager_callback_t) (power_manager_notify_struct_t *notify,
               power_manager_callback_data_t *dataPtr)
```

Callback prototype.

Declaration of callback. It is common for all registered callbacks. Function pointer of this type is part of [power_manager_callback_user_config_t](#) callback configuration structure. Depending on the callback type, the callback function is invoked during power mode change (see [POWER_SYS_SetMode\(\)](#)) before the mode change, after it, or in both cases to notify about the change progress (see `power_manager_callback_type_t`). When called, the type of the notification is passed as parameter along with a pointer to power mode configuration structure (see [power_manager_notify_struct_t](#)) and any data passed during the callback registration (see `power_manager_callback_data_t`). When notified before a mode change, depending on the power mode change policy (see `power_manager_policy_t`) the callback may deny the mode change by returning any error code other than `STATUS_SUCCESS` (see [POWER_SYS_SetMode\(\)](#)).

Parameters

<i>notify</i>	Notification structure.
<i>dataPtr</i>	Callback data. Pointer to the data passed during callback registration. Intended to pass any driver or application data such as internal state information.

Returns

An error code or `STATUS_SUCCESS`. Implements `power_manager_callback_t_Class`

Definition at line 169 of file `power_manager.h`.

17.111.4 Enumeration Type Documentation

17.111.4.1 enum power_manager_callback_type_t

The callback type indicates when a callback will be invoked.

Used in the callback configuration structures ([power_manager_callback_user_config_t](#)) to specify when the registered callback will be called during power mode change initiated by [POWER_SYS_SetMode\(\)](#).

Implements `power_manager_callback_type_t_Class`

Enumerator

`POWER_MANAGER_CALLBACK_BEFORE` Before callback.
`POWER_MANAGER_CALLBACK_AFTER` After callback.
`POWER_MANAGER_CALLBACK_BEFORE_AFTER` Before-After callback.

Definition at line 100 of file `power_manager.h`.

17.111.4.2 enum power_manager_notify_t

The PM notification type. Used to notify registered callbacks. Callback notifications can be invoked in following situations:

- before a power mode change (Callback return value can affect [POWER_SYS_SetMode\(\)](#) execution. Refer to the [POWER_SYS_SetMode\(\)](#) and `power_manager_policy_t` documentation).
- after a successful change of the power mode.

- after an unsuccessful attempt to switch power mode, in order to recover to a working state. Implements `power_manager_notify_t_Class`

Enumerator

`POWER_MANAGER_NOTIFY_RECOVER` Notify IP to recover to previous work state.

`POWER_MANAGER_NOTIFY_BEFORE` Notify IP that the system will change the power setting.

`POWER_MANAGER_NOTIFY_AFTER` Notify IP that the system has changed to a new power setting.

Definition at line 84 of file `power_manager.h`.

17.111.4.3 `enum power_manager_policy_t`

Power manager policies.

Defines whether the mode switch initiated by the [POWER_SYS_SetMode\(\)](#) is agreed upon (depending on the result of notification callbacks), or forced. For `POWER_MANAGER_POLICY_FORCIBLE` the power mode is changed regardless of the callback results, while for `POWER_MANAGER_POLICY_AGREEMENT` policy any error code returned by one of the callbacks aborts the mode change. See also [POWER_SYS_SetMode\(\)](#) description. Implements `power_manager_policy_t_Class`

Enumerator

`POWER_MANAGER_POLICY_AGREEMENT` Power mode is changed if all of the callbacks return success.

`POWER_MANAGER_POLICY_FORCIBLE` Power mode is changed regardless of the result of callbacks.

Definition at line 69 of file `power_manager.h`.

17.111.5 Function Documentation

17.111.5.1 `status_t POWER_SYS_Deinit (void)`

This function deinitializes the Power manager.

Returns

An error code or `STATUS_SUCCESS`.

Definition at line 110 of file `power_manager.c`.

17.111.5.2 `power_manager_modes_t POWER_SYS_GetCurrentMode (void)`

This function returns currently running power mode.

This function reads hardware settings and returns currently running power mode.

Returns

Currently used run power mode.

Definition at line 244 of file `power_manager_S32K1xx.c`.

17.111.5.3 `void POWER_SYS_GetDefaultConfig (power_manager_user_config_t *const config)`

This function returns the default `power_manager` configuration structure.

This function returns a pointer of the `power_manager` configuration structure. All structure members have default value when CPU is default power mode.

Definition at line 406 of file `power_manager.c`.

17.111.5.4 `power_manager_callback_user_config_t*` `POWER_SYS_GetErrorCallback (void)`

This function returns the callback configuration structure for the last failed notification.

This function returns a pointer to configuration structure of the last callback that failed during the power mode switch when `POWER_SYS_SetMode()` was called. If the last `POWER_SYS_SetMode()` call ended successfully, a NULL value is returned.

Returns

Pointer to the callback configuration which returns error.

Definition at line 208 of file `power_manager.c`.

17.111.5.5 `uint8_t` `POWER_SYS_GetErrorCallbackIndex (void)`

This function returns the last failed notification callback.

This function returns the index of the last callback that failed during the power mode switch when `POWER_SYS_SetMode()` was called. The returned value represents the index in the array of registered callbacks. If the last `POWER_SYS_SetMode()` call ended successfully, a value equal to the number of registered callbacks is returned.

Returns

Callback index of last failed callback or value equal to callbacks count.

Definition at line 196 of file `power_manager.c`.

17.111.5.6 `status_t` `POWER_SYS_GetLastMode (uint8_t * powerModeIndexPtr)`

This function returns the last successfully set power mode.

This function returns index of power mode which was last set using `POWER_SYS_SetMode()`. If the power mode was entered even though some of the registered callbacks denied the mode change, or if any of the callbacks invoked after the entering/restoring run mode failed, then the return code of this function has `STATUS_ERROR` value.

Parameters

out	<i>powerModeIndexPtr</i>	Power mode which has been set represented as an index into array of power mode configurations passed to the <code>POWER_SYS_Init()</code> .
-----	--------------------------	---

Returns

An error code or `STATUS_SUCCESS`.

Definition at line 133 of file `power_manager.c`.

17.111.5.7 `status_t` `POWER_SYS_GetLastModeConfig (power_manager_user_config_t ** powerModePtr)`

This function returns the user configuration structure of the last successfully set power mode.

This function returns a pointer to configuration structure which was last set using `POWER_SYS_SetMode()`. If the current power mode was entered even though some of the registered callbacks denied the mode change, or if any of the callbacks invoked after the entering/restoring run mode failed, then the return code of this function has `STATUS_ERROR` value.

Parameters

out	<i>powerModePtr</i>	Pointer to power mode configuration structure of the last set power mode.
-----	---------------------	---

Returns

An error code or STATUS_SUCCESS.

Definition at line 165 of file power_manager.c.

17.111.5.8 `status_t POWER_SYS_Init (power_manager_user_config_t (*) powerConfigsPtr[], uint8_t configsNumber, power_manager_callback_user_config_t (*) callbacksPtr[], uint8_t callbacksNumber)`

Power manager initialization for operation.

This function initializes the Power manager and its run-time state structure. Pointer to an array of Power mode configuration structures needs to be passed as a parameter along with a parameter specifying its size. At least one power mode configuration is required. Optionally, pointer to the array of predefined callbacks can be passed with its corresponding size parameter. For details about callbacks, refer to the [power_manager_callback_user_config_t](#). As Power manager stores only pointers to arrays of these structures, they need to exist and be valid for the entire life cycle of Power manager.

Parameters

in	<i>powerConfigsPtr</i>	A pointer to an array of pointers to all power configurations which will be handled by Power manager.
in	<i>configsNumber</i>	Number of power configurations. Size of powerConfigsPtr array.
in	<i>callbacksPtr</i>	A pointer to an array of pointers to callback configurations. If there are no callbacks to register during Power manager initialization, use NULL value.
in	<i>callbacksNumber</i>	Number of registered callbacks. Size of callbacksPtr array.

Returns

An error code or STATUS_SUCCESS.

Definition at line 70 of file power_manager.c.

17.111.5.9 `status_t POWER_SYS_SetMode (uint8_t powerModelIndex, power_manager_policy_t policy)`

This function configures the power mode.

This function switches to one of the defined power modes. Requested mode number is passed as an input parameter. This function notifies all registered callback functions before the mode change (using POWER_MANAGER_CALLBACK_BEFORE set as callback type parameter), sets specific power options defined in the power mode configuration and enters the specified mode. In case of run modes (for example, Run, Very low power run, or High speed run), this function also invokes all registered callbacks after the mode change (using POWER_MANAGER_CALLBACK_AFTER). In case of sleep or deep sleep modes, if the requested mode is not exited through a reset, these notifications are sent after the core wakes up. Callbacks are invoked in the following order: All registered callbacks are notified ordered by index in the callbacks array (see callbacksPtr parameter of [POWER_SYS_Init\(\)](#)). The same order is used for before and after switch notifications. The notifications before the power mode switch can be used to obtain confirmation about the change from registered callbacks. If any registered callback denies the power mode change, further execution of this function depends on mode change policy: the mode change is either forced(POWER_MANAGER_POLICY_FORCIBLE) or aborted(POWER_MANAGER_POLICY_AGREEMENT). When mode change is forced, the results of the before switch notifications are ignored. If agreement is requested, in case any callback returns an error code then further before switch notifications are cancelled and all already notified callbacks are re-invoked with POWER_MANAGER_CALLBACK_AFTER set as callback type parameter. The index of the callback which returned error code during pre-switch notifications is stored and can be obtained by using [POWER_SYS_GetErrorCallback\(\)](#). Any error codes during callbacks re-invocation (recover phase) are ignored. [POWER_SYS_SetMode\(\)](#) returns an error code denoting the phase in which a callback failed. It is possible to enter any mode supported by the processor. Refer to the chip reference manual for the list of available power modes. If it is necessary to switch into an intermediate power mode prior to entering the requested

mode (for example, when switching from Run into Very low power wait through Very low power run mode), then the intermediate mode is entered without invoking the callback mechanism.

Parameters

in	<i>powerMode↔ Index</i>	Requested power mode represented as an index into array of user-defined power mode configurations passed to the POWER_SYS_Init() .
in	<i>policy</i>	Transaction policy

Returns

An error code or STATUS_SUCCESS.

Definition at line 323 of file power_manager.c.

17.111.6 Variable Documentation**17.111.6.1 power_manager_state_t gPowerManagerState**

Power manager internal structure.

Definition at line 52 of file power_manager_S32K1xx.c.

17.112 Power Manager Driver

This module covers the device-specific power_manager functionality implemented for S32K1xx, s32k14xW and S32MTV SOC.

Hardware background

System mode controller (SMC) is passing the system into and out of all low-power Stop and Run modes. Controls the power, clocks and memories of the system to achieve the power consumption and functionality of that mode.

Driver consideration

Power mode entry and sleep-on-exit-value are provided at initialization time through the power manager user configuration structure.

With platform is S32K14x, the available power mode entries are the following ones: HSRUN, RUN, VLPR, STOP1, STOP2 and VLPS.

With platform is S32MTV,S32K11x and S32K14xW. The available power mode entries are the following ones: RUN, VLPR, STOP1, STOP2 and VLPS.

This is an example of configuration:

```
power_manager_user_config_t pwrMan1_InitConfig0 = {
    .powerMode = POWER_MANAGER_RUN,
    .sleepOnExitValue = false,
};

power_manager_user_config_t *powerConfigsArr[] = {
    &pwrMan1_InitConfig0
};

power_manager_callback_user_config_t * powerCallbacksConfigsArr[] = {(
    void *)0};

if (STATUS_SUCCESS != POWER_SYS_Init(&powerConfigsArr,1,&powerCallbacksConfigsArr,0)) {
    ...
}
else {
    ...
}

if (STATUS_SUCCESS != POWER_SYS_SetMode(0,
    POWER_MANAGER_POLICY_AGREEMENT)) {
    ...
}
else {
    ...
}
```

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\power_manager.c
${S32SDK_PATH}\platform\drivers\src\S32K1xx\power_manager_S32K1xx.c
${S32SDK_PATH}\platform\drivers\src\S32K1xx\power_smc_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc\
${S32SDK_PATH}\platform\drivers\src\power\
${S32SDK_PATH}\platform\drivers\src\power\S32K1xx\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager](#)

Important Note

1. ERR01077: The SCG_RCCR[SCS] and SCG_HCCR[SCS] may have a corrupted status during the interval by the software to ensure when the system clock is switching.
This errata did workaround by the SCS field was read twice the system clock switch has completed.
The clock configuration is not immediately updated after MCU switched from very low power mode to run or high speed mode. It may be taking longer time than expected.
2. The power manager driver will disable SPLL, FIRC, SOSC source in RUN mode before MCU jumps from RUN,HSRUN to very low power mode.
SIRC is clock source when MCU enters very low power mode. Driver will update initialize system clock configuration when MCU jumps to RUN or HSRUN mode again.
It will enable all clock source again which is configured by clock configurations. This is executed when user calls the POWER_SYS_SetMode function for RUN or HSRUN.
3. When MCU switches from HSRUN to STOP or VLP mode, the driver code will auto switch RUN mode before MCU enters next mode.
4. Users need to take care peripherals clock frequency via SPLL DIVx_CLK, SIRC DIVx_CLK after MCU switched power mode.
Clock configuration can be re-initialized when MCU returns to RUN mode. This way will make sure the clock for all peripherals.

17.113 Power_s32k1xx

17.113.1 Detailed Description

Data Structures

- struct [power_manager_user_config_t](#)
Power mode user configuration structure. [More...](#)
- struct [smc_power_mode_protection_config_t](#)
Power mode protection configuration. [More...](#)
- struct [smc_power_mode_config_t](#)
Power mode control configuration used for calling the SMC_SYS_SetPowerMode API. [More...](#)

Enumerations

- enum [power_manager_modes_t](#) { [POWER_MANAGER_RUN](#), [POWER_MANAGER_VLPR](#), [POWER_MANAGER_VLPS](#), [POWER_MANAGER_MAX](#) }
Power modes enumeration.
- enum [power_mode_stat_t](#) {
[STAT_RUN](#) = 0x01, [STAT_STOP](#) = 0x02, [STAT_VLPR](#) = 0x04, [STAT_VLPW](#) = 0x08,
[STAT_VLPS](#) = 0x10, [STAT_HSRUN](#) = 0x80, [STAT_INVALID](#) = 0xFF }
Power Modes in PMSTAT.
- enum [smc_run_mode_t](#) { [SMC_RUN](#), [SMC_RESERVED_RUN](#), [SMC_VLPR](#), [SMC_HSRUN](#) }
Run mode definition.
- enum [smc_stop_mode_t](#) { [SMC_STOP](#) = 0U, [SMC_RESERVED_STOP1](#) = 1U, [SMC_VLPS](#) = 2U }
Stop mode definition.
- enum [smc_stop_option_t](#) { [SMC_STOP_RESERVED](#) = 0x00, [SMC_STOP1](#) = 0x01, [SMC_STOP2](#) = 0x02 }
STOP option.
- enum [rcm_source_names_t](#) {
[RCM_LOW_VOLT_DETECT](#) = 1U, [RCM_LOSS_OF_CLK](#) = 2U, [RCM_LOSS_OF_LOCK](#) = 3U, [RCM_WATCHDOG](#) = 5U,
[RCM_EXTERNAL_PIN](#) = 6U, [RCM_POWER_ON](#) = 7U, [RCM_SJTAG](#) = 8U, [RCM_CORE_LOCKUP](#) = 9U,
[RCM_SOFTWARE](#) = 10U, [RCM_SMDM_AP](#) = 11U, [RCM_STOP_MODE_ACK_ERR](#) = 13U, [RCM_SRC_NAME_MAX](#) }
System Reset Source Name definitions Implements rcm_source_names_t_Class.

Functions

- status_t [POWER_SYS_DoInit](#) (void)
This function implementation-specific configuration of power modes.
- status_t [POWER_SYS_DoDeinit](#) (void)
This function implementation-specific de-initialization of power manager.
- status_t [POWER_SYS_DoSetMode](#) (const [power_manager_user_config_t](#) *const configPtr)
This function configures the power mode.
- bool [POWER_SYS_GetResetSrcStatusCmd](#) (const RCM_Type *const baseAddr, const [rcm_source_names_t](#) srcName)
Gets the reset source status.
- static void [POWER_SYS_DoGetDefaultConfig](#) ([power_manager_user_config_t](#) *const defaultConfig)
Gets the default power_manager configuration structure.

17.113.2 Data Structure Documentation

17.113.2.1 struct power_manager_user_config_t

Power mode user configuration structure.

List of power mode configuration structure members depends on power options available for the specific chip. Complete list contains: mode - S32K power mode. List of available modes is chip-specific. See power_manager_modes_t list of modes. sleepOnExitOption - Controls whether the sleep-on-exit option value is used (when set to true) or ignored (when set to false). See sleepOnExitValue. sleepOnExitValue - When set to true, ARM core returns to sleep (S32K wait modes) or deep sleep state (S32K stop modes) after interrupt service finishes. When set to false, core stays woken-up. Implements power_manager_user_config_t_Class

Definition at line 95 of file power_manager_S32K1xx.h.

Data Fields

- [power_manager_modes_t powerMode](#)
- bool [sleepOnExitValue](#)

Field Documentation

17.113.2.1.1 power_manager_modes_t powerMode

Definition at line 97 of file power_manager_S32K1xx.h.

17.113.2.1.2 bool sleepOnExitValue

Definition at line 98 of file power_manager_S32K1xx.h.

17.113.2.2 struct smc_power_mode_protection_config_t

Power mode protection configuration.

Definition at line 153 of file power_manager_S32K1xx.h.

Data Fields

- bool [vlpProt](#)

Field Documentation

17.113.2.2.1 bool vlpProt

VLP protect

Definition at line 155 of file power_manager_S32K1xx.h.

17.113.2.3 struct smc_power_mode_config_t

Power mode control configuration used for calling the SMC_SYS_SetPowerMode API.

Definition at line 165 of file power_manager_S32K1xx.h.

Data Fields

- [power_manager_modes_t powerModeName](#)

Field Documentation

17.113.2.3.1 power_manager_modes_t powerModeName

Power mode(enum), see power_manager_modes_t

Definition at line 167 of file power_manager_S32K1xx.h.

17.113.3 Enumeration Type Documentation

17.113.3.1 enum power_manager_modes_t

Power modes enumeration.

Defines power modes. Used in the power mode configuration structure ([power_manager_user_config_t](#)). From ARM core perspective, Power modes can be generally divided into run modes (High speed run, Run and Very low power run), sleep (Wait and Very low power wait) and deep sleep modes (all Stop modes). List of power modes supported by specific chip along with requirements for entering and exiting of these modes can be found in chip documentation. List of all supported power modes:

- POWER_MANAGER_HSRUN - High speed run mode.
- POWER_MANAGER_RUN - Run mode.
- POWER_MANAGER_VLPR - Very low power run mode.
- POWER_MANAGER_WAIT - Wait mode.
- POWER_MANAGER_VLPW - Very low power wait mode.
- POWER_MANAGER_PSTOP1 - Partial stop 1 mode.
- POWER_MANAGER_PSTOP2 - Partial stop 2 mode.
- POWER_MANAGER_PSTOP1 - Stop 1 mode.
- POWER_MANAGER_PSTOP2 - Stop 2 mode.
- POWER_MANAGER_VLPS - Very low power stop mode. Implements power_manager_modes_t_Class

Enumerator

POWER_MANAGER_RUN Run mode.
POWER_MANAGER_VLPR Very low power run mode.
POWER_MANAGER_VLPS Very low power stop mode.
POWER_MANAGER_MAX

Definition at line 58 of file power_manager_S32K1xx.h.

17.113.3.2 enum power_mode_stat_t

Power Modes in PMSTAT.

Enumerator

STAT_RUN 0000_0001 - Current power mode is RUN
STAT_STOP 0000_0010 - Current power mode is STOP
STAT_VLPR 0000_0100 - Current power mode is VLPR
STAT_VLPW 0000_1000 - Current power mode is VLPW
STAT_VLPS 0001_0000 - Current power mode is VLPS
STAT_HSRUN 1000_0000 - Current power mode is HSRUN
STAT_INVALID 1111_1111 - Non-existing power mode

Definition at line 105 of file power_manager_S32K1xx.h.

17.113.3.3 enum **rcm_source_names_t**

System Reset Source Name definitions Implements **rcm_source_names_t** Class.

Enumerator

RCM_LOW_VOLT_DETECT Low voltage detect reset
RCM_LOSS_OF_CLK Loss of clock reset
RCM_LOSS_OF_LOCK Loss of lock reset
RCM_WATCH_DOG Watch dog reset
RCM_EXTERNAL_PIN External pin reset
RCM_POWER_ON Power on reset
RCM_SJTAG JTAG generated reset
RCM_CORE_LOCKUP core lockup reset
RCM_SOFTWARE Software reset
RCM_SMDM_AP MDM-AP system reset
RCM_STOP_MODE_ACK_ERR Stop mode ack error reset
RCM_SRC_NAME_MAX

Definition at line 181 of file **power_manager_S32K1xx.h**.

17.113.3.4 enum **smc_run_mode_t**

Run mode definition.

Enumerator

SMC_RUN normal RUN mode
SMC_RESERVED_RUN
SMC_VLPR Very-Low-Power RUN mode
SMC_HSRUN High Speed Run mode (HSRUN)

Definition at line 120 of file **power_manager_S32K1xx.h**.

17.113.3.5 enum **smc_stop_mode_t**

Stop mode definition.

Enumerator

SMC_STOP Normal STOP mode
SMC_RESERVED_STOP1 Reserved
SMC_VLPS Very-Low-Power STOP mode

Definition at line 131 of file **power_manager_S32K1xx.h**.

17.113.3.6 enum **smc_stop_option_t**

STOP option.

Enumerator

SMC_STOP_RESERVED Reserved stop mode
SMC_STOP1 Stop with both system and bus clocks disabled
SMC_STOP2 Stop with system clock disabled and bus clock enabled

Definition at line 142 of file **power_manager_S32K1xx.h**.

17.113.4 Function Documentation

17.113.4.1 `status_t POWER_SYS_DoDeinit (void)`

This function implementation-specific de-initialization of power manager.

This function performs the actual implementation-specific de-initialization.

Returns

Operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failed.

Definition at line 200 of file power_manager_S32K1xx.c.

17.113.4.2 `static void POWER_SYS_DoGetDefaultConfig (power_manager_user_config_t *const defaultConfig)`
[inline], [static]

Gets the default power_manager configuration structure.

This function gets the power_manager configuration structure of the default power mode.

Parameters

out	defaultConfig	: Pointer to power mode configuration structure of the default power mode.
-----	---------------	--

< Power manager mode

< Sleep on exit value

Definition at line 261 of file power_manager_S32K1xx.h.

17.113.4.3 `status_t POWER_SYS_DoInit (void)`

This function implementation-specific configuration of power modes.

This function performs the actual implementation-specific initialization based on the provided power mode configurations. In addition, This function get all clock source were enabled. This one was used for update init clock when CPU jump from very low power mode to run or high speed run mode.

Returns

Operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failed.

Definition at line 157 of file power_manager_S32K1xx.c.

17.113.4.4 `status_t POWER_SYS_DoSetMode (const power_manager_user_config_t *const configPtr)`

This function configures the power mode.

This function performs the actual implementation-specific logic to switch to one of the defined power modes.

Parameters

configPtr	Pointer to user configuration structure
-----------	---

Returns

Operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_MCU_TRANSITION_FAILED: Operation failed.

Definition at line 217 of file power_manager_S32K1xx.c.

17.113.4.5 `bool POWER_SYS_GetResetSrcStatusCmd (const RCM_Type *const baseAddr, const rcm_source_names_t srcName)`

Gets the reset source status.

This function gets the current reset source status for a specified source.

Parameters

in	<i>baseAddr</i>	Register base address of RCM
in	<i>srcName</i>	reset source name

Returns

status True or false for specified reset source

Definition at line 688 of file `power_manager_S32K1xx.c`.

17.114 Programmable Delay Block (PDB)

17.114.1 Detailed Description

The S32 SDK provides a peripheral driver for the Programmable Delay Block (PDB) module.

The PDB is a configurable counter that can generate events (triggers) that can be used by the ADC to start conversions or routed through TRGMUX to other modules in the device.

Modules

- [PDB Driver](#)

Programmable Delay Block Peripheral Driver.

17.115 Pulse-width modulation - Peripheral Abstraction Layer (PWM PAL)

17.115.1 Detailed Description

The S32 SDK provides a Peripheral Abstraction Layer for the PWM mode.

The PWM PAL driver allows to generate PWM signals. It was designed to be portable across all platforms and IPs which support PWM features.

How to integrate PWM in your application

Unlike the other drivers, PWM PAL modules need to include a configuration file named `pwm_pal_cfg.h`, which allows the user to specify which IPs are used and how many resources are allocated for each of them (state structures). The following code example shows how to configure one instance for each available PWM IP.

```
#ifndef PWM_PAL_cfg_H
#define PWM_PAL_cfg_H

/* Define which IP instance will be used in current project */
#define PWM_OVER_FTM
#define PWM_OVER_EMIOS
#define PWM_OVER_ETIMER

/* Define the resources necessary for current project */
#define NO_OF_FTM_INSTS_FOR_PWM 1U
#define NO_OF_EMIOS_INSTS_FOR_PWM 1U
#define NO_OF_ETIMER_INSTS_FOR_PWM 1U
#endif /* PWM_PAL_cfg_H */
```

The following table contains the matching between platforms and available IPs

IP/ M↔ CU	S32↔ K116	S32↔ K118	S32↔ K142	S32↔ K144	S32↔ K142↔ W	S32↔ K144↔ W	S32↔ K146	S32↔ K148	M↔ P↔ C5748 G	M↔ P↔ C5746 C	M↔ P↔ C5744 P	S32↔ R274	S32↔ R372
FTM	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	NO	NO	NO	NO	NO
e↔ MI↔ OS	NO	NO	NO	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES	NO	NO	NO
E↔ TI↔ M↔ ER	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES	Y↔ ES

In order to use the PWM PAL driver it must be first initialized it using function [PWM_Init\(\)](#). Once initialized, it cannot be initialized again for the same PWM module instance until it is de-initialized, using [PWM_Deinit\(\)](#). Different PWM module instances can work independently of each other.

After initialization the duty cycle and pwm period can be updated with these functions: [PWM_UpdateDuty\(\)](#) and [PWM_UpdatePeriod\(\)](#). The measurement unit for duty and period is clock ticks, so the application should be aware about the clock frequency of the timebase used by PWM channel.

Due to hardware limitation period changing for a specific channel can change the period for other channels if they share the same timebase. Also, for FTM all channels must have the same period and type.

Important Notes

- The driver enables the interrupts for the corresponding module, but any interrupt priority setting must be done by the application.
- Due to different hardware features is necessary to use different timebase configuration on each platform and some features are available only on some peripherals. To be sure that your applications doesn't try to use unsupported features check return status of called functions and activate `DEV_ERROR_DETECT`.

Basic code sequence

1. Initialize PWM_PAL instance

```
PWM_Init(&pwm_palInstance, &pwm_palConfig);
```

2. Update duty cycle

```
PWM_UpdateDuty(&pwm_palInstance, 0, dutyCycle);
```

3. Update period

```
PWM_UpdatePeriod(&pwm_palInstance, 0, period);
```

4. De-initialize PWM_PAL instance

```
PWM_Deinit(&pwm_palInstance);
```

Hardware Limitations**eTimer**

eTimer cannot generate 0% or 100% duty cycles. At least one clock tick will have inverted polarity.

Integration guideline**Compilation units**

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\pal\src\pwm\pwm_pal.c
```

Additionally, it is required to compile also the .c files from the dependencies listed for each ADC PAL type (please see Dependencies subsection below).

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\pal\inc\  
${S32SDK_PATH}\platform\drivers\inc\  

```

An additional file, named *pwm_pal_cfg.h*, must be created by the user and added to one of the include paths. The user has to add to the file the definitions of preprocessor symbols according to the PWM PAL type used. These symbols are specified in the next subsection.

When using the S32 SDK configuration tool the file is generated by the configurator.

The pal type PWM_OVER_FTM also requires:

```
${S32SDK_PATH}\platform\drivers\src\ftm\  

```

Compile symbols

Define for selecting one of the PWM PAL type to be used:

```
PWM_OVER_FTM  
PWM_OVER_EMIO  
PWM_OVER_ETIMER
```

Dependencies

- The pal type PWM_OVER_FTM also depends on:
[FlexTimer Pulse Width Modulation Driver \(FTM_PWM\)](#)
[FlexTimer \(FTM\)](#)
- The pal type PWM_OVER_EMIO also depends on:
[mc_emios_driver](#)
[pwm_emios_driver](#)
- The pal type PWM_OVER_ETIMER also depends on:
[etimer_drv](#)

Data Structures

- struct [pwm_ftm_timebase_t](#)
This structure is specific for platforms where FTM is available. Implements : [pwm_ftm_timebase_t_Class](#). [More...](#)
- struct [pwm_channel_t](#)
This structure includes the configuration for each channel Implements : [pwm_channel_t_Class](#). [More...](#)
- struct [pwm_global_config_t](#)
This structure is the configuration for initialization of PWM channels. Implements : [pwm_global_config_t_Class](#). [More...](#)

Enumerations

- enum [pwm_channel_type_t](#) { PWM_EDGE_ALIGNED = 0, PWM_CENTER_ALIGNED = 1 }
Defines the channel types Implements : [pwm_channel_type_t_Class](#).
- enum [pwm_polarity_t](#) { PWM_ACTIVE_HIGH = 0, PWM_ACTIVE_LOW = 1 }
Defines the polarity of pwm channels Implements : [pwm_polarity_t_Class](#).
- enum [pwm_complementary_mode_t](#) { PWM_DUPLICATED = 0, PWM_INVERTED = 1 }
Defines the polarity of complementary pwm channels relative to main channel Implements : [pwm_complementary_mode_t_Class](#).

Functions

- status_t [PWM_Init](#) (const [pwm_instance_t](#) *const instance, const [pwm_global_config_t](#) *config)
Initialize PWM channels based on config parameter.
- status_t [PWM_UpdateDuty](#) (const [pwm_instance_t](#) *const instance, uint8_t channel, uint32_t duty)
Update duty cycle. The measurement unit for duty is clock ticks.
- status_t [PWM_UpdatePeriod](#) (const [pwm_instance_t](#) *const instance, uint8_t channel, uint32_t period)
Update period for specific a specific channel. This function changes period for all channels which shares the timebase with targeted channel.
- status_t [PWM_OverwriteOutputChannels](#) (const [pwm_instance_t](#) *const instance, uint32_t channelsMask, uint32_t channelsValues)
This function change the output value for some channels. channelsMask select which channels will be overwrite, each bit filed representing one channel: 1 - channel is controlled by channelsValues, 0 - channel is controlled by pwm. channelsValues select output values to be write on corresponding channel. For PWM_PAL over FTM, when enable complementary channels, if this function is used to force output of complementary channels(n and n+1) with value is high, the output of channel n is going to be high and the output of channel n+1 is going to be low. Please refer to Software ouput control behavior table in the reference manual to get more detail.

- status_t [PWM_Deinit](#) (const [pwm_instance_t](#) *const instance)
De-Initialize PWM instance.

17.115.2 Data Structure Documentation

17.115.2.1 struct [pwm_ftm_timebase_t](#)

This structure is specific for platforms where FTM is available. Implements : [pwm_ftm_timebase_t_Class](#).

Definition at line 92 of file [pwm_pal.h](#).

Data Fields

- [ftm_clock_source_t](#) sourceClock
- [ftm_clock_ps_t](#) prescaler
- [ftm_deadtime_ps_t](#) deadtimePrescaler

Field Documentation

17.115.2.1.1 [ftm_deadtime_ps_t](#) deadtimePrescaler

Prescaler for FTM dead-time insertion

Definition at line 96 of file [pwm_pal.h](#).

17.115.2.1.2 [ftm_clock_ps_t](#) prescaler

Prescaler for FTM timebase

Definition at line 95 of file [pwm_pal.h](#).

17.115.2.1.3 [ftm_clock_source_t](#) sourceClock

Clock source for FTM timebase

Definition at line 94 of file [pwm_pal.h](#).

17.115.2.2 struct [pwm_channel_t](#)

This structure includes the configuration for each channel Implements : [pwm_channel_t_Class](#).

Definition at line 147 of file [pwm_pal.h](#).

Data Fields

- uint8_t [channel](#)
- [pwm_channel_type_t](#) channelType
- uint32_t [period](#)
- uint32_t [duty](#)
- [pwm_polarity_t](#) polarity
- bool [insertDeadtime](#)
- uint8_t [deadtime](#)
- bool [enableComplementaryChannel](#)
- [pwm_complementary_mode_t](#) complementaryChannelPolarity
- void * [timebase](#)

Field Documentation

17.115.2.2.1 [uint8_t](#) channel

Channel number

Definition at line 149 of file [pwm_pal.h](#).

17.115.2.2.2 `pwm_channel_type_t` channelType

Channel waveform type

Definition at line 150 of file `pwm_pal.h`.

17.115.2.2.3 `pwm_complementary_mode_t` complementaryChannelPolarity

Configure the polarity of the complementary channel relative to the main channel

Definition at line 157 of file `pwm_pal.h`.

17.115.2.2.4 `uint8_t` deadtime

Dead-time value in ticks

Definition at line 155 of file `pwm_pal.h`.

17.115.2.2.5 `uint32_t` duty

Duty cycle in ticks

Definition at line 152 of file `pwm_pal.h`.

17.115.2.2.6 `bool` enableComplementaryChannel

Enable a complementary channel. This option can take control over other channel than the channel configured in this structure.

Definition at line 156 of file `pwm_pal.h`.

17.115.2.2.7 `bool` insertDeadtime

Enable/disable dead-time insertion. This feature is available only if complementary mode is enabled

Definition at line 154 of file `pwm_pal.h`.

17.115.2.2.8 `uint32_t` period

Period of the PWM signal in ticks

Definition at line 151 of file `pwm_pal.h`.

17.115.2.2.9 `pwm_polarity_t` polarity

Channel polarity

Definition at line 153 of file `pwm_pal.h`.

17.115.2.2.10 `void*` timebase

This field is platform specific and it's used to configure the clocking tree for different time-bases. If FTM is use this field must be filled by a pointer to [pwm_ftm_timebase_t](#)

Definition at line 158 of file `pwm_pal.h`.

17.115.2.3 `struct pwm_global_config_t`

This structure is the configuration for initialization of PWM channels. Implements : `pwm_global_config_t_Class`.

Definition at line 166 of file `pwm_pal.h`.

Data Fields

- [pwm_channel_t](#) * `pwmChannels`
- `uint8_t` `numberOfPwmChannels`

Field Documentation

17.115.2.3.1 `uint8_t numberOfPwmChannels`

Number of channels which are configured

Definition at line 169 of file `pwm_pal.h`.

17.115.2.3.2 `pwm_channel_t* pwmChannels`

Pointer to channels configurations

Definition at line 168 of file `pwm_pal.h`.

17.115.3 Enumeration Type Documentation

17.115.3.1 `enum pwm_channel_type_t`

Defines the channel types Implements : `pwm_channel_type_t_Class`.

Enumerator

PWM_EDGE_ALIGNED Counter used by this type of channel is in up counting mode and the edge is aligned to PWM period

PWM_CENTER_ALIGNED Counter used by this type of channel is in up-down counting mode and the duty is inserted in center of PWM period

Definition at line 60 of file `pwm_pal.h`.

17.115.3.2 `enum pwm_complementary_mode_t`

Defines the polarity of complementary pwm channels relative to main channel Implements : `pwm_complementary_mode_t_Class`.

Enumerator

PWM_DUPLICATED Complementary channel is the same as main channel

PWM_INVERTED Complementary channel is inverted relative to main channel

Definition at line 80 of file `pwm_pal.h`.

17.115.3.3 `enum pwm_polarity_t`

Defines the polarity of pwm channels Implements : `pwm_polarity_t_Class`.

Enumerator

PWM_ACTIVE_HIGH Polarity is active high

PWM_ACTIVE_LOW Polarity is active low

Definition at line 70 of file `pwm_pal.h`.

17.115.4 Function Documentation

17.115.4.1 `status_t PWM_Deinit (const pwm_instance_t *const instance)`

De-Initialize PWM instance.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance
-----------	-----------------	--------------------------

Returns

Error or success status returned by API

Definition at line 819 of file pwm_pal.c.

17.115.4.2 `status_t PWM_Init (const pwm_instance_t *const instance, const pwm_global_config_t * config)`

Initialize PWM channels based on config parameter.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance
<i>in</i>	<i>config</i>	The configuration structure used to initialize PWM modules

Returns

Error or success status returned by API

Definition at line 133 of file pwm_pal.c.

17.115.4.3 `status_t PWM_OverwriteOutputChannels (const pwm_instance_t *const instance, uint32_t channelsMask, uint32_t channelsValues)`

This function change the output value for some channels. channelsMask select which channels will be overwrite, each bit filed representing one channel: 1 - channel is controlled by channelsValues, 0 - channel is controlled by pwm. channelsValues select output values to be write on corresponding channel. For PWM_PAL over FTM, when enable complementary channels, if this function is used to force output of complementary channels(n and n+1) with value is high, the output of channel n is going to be high and the output of channel n+1 is going to be low. Please refer to Software ouput control behavior table in the reference manual to get more detail.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance
<i>in</i>	<i>channelsMask</i>	The name mask used to select which channel is overwrite
<i>in</i>	<i>channelsValues</i>	The name overwrite values for all channels

Returns

Error or success status returned by API

Definition at line 775 of file pwm_pal.c.

17.115.4.4 `status_t PWM_UpdateDuty (const pwm_instance_t *const instance, uint8_t channel, uint32_t duty)`

Update duty cycle. The measurement unit for duty is clock ticks.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance
<i>in</i>	<i>channel</i>	The channel which is update
<i>in</i>	<i>duty</i>	The duty cycle measured in ticks

Returns

Error or success status returned by API

Definition at line 574 of file pwm_pal.c.

17.115.4.5 `status_t PWM_UpdatePeriod (const pwm_instance_t *const instance, uint8_t channel, uint32_t period)`

Update period for specific a specific channel. This function changes period for all channels which shares the timebase with targeted channel.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance
<i>in</i>	<i>channel</i>	The channel which is update
<i>in</i>	<i>period</i>	The period measured in ticks

Returns

Error or success status returned by API

Definition at line 669 of file pwm_pal.c.

17.116 Quad Serial Peripheral Interface (QuadSPI)

17.116.1 Detailed Description

The Quad Serial Peripheral Interface (QuadSPI) block acts as an interface to a single or two external serial flash devices, each with up to eight bidirectional data lines. Main features of the QuadSPI include:

- Flexible sequence engine to support various flash vendor devices.
- Supports single/double data rate.
- Supports single, dual, quad and octal modes of operation.
- Allows AHB accesses to flash devices, directly memory mapped to the chip system memory.
- Multi-master accesses with configurable priority.

Due to the variations between different flash vendors, a single driver cannot support any serial flash device. Instead, a two-layered approach is used: the QuadSPI driver provides generic support for the QuadSPI module, serving as a base for the device-specific flash drivers. Device-specific flash drivers are targeted for a particular serial flash device and offer full support for its particular features.

Modules

- [MX25L6433F Serial Flash Driver](#)
Driver for the Macronix MX25L6433F Serial Flash.
- [QuadSPI Driver](#)
Generic driver for the QuadSPI module.

17.117 QuadSPI Driver

17.117.1 Detailed Description

Generic driver for the QuadSPI module.

The QuadSPI driver offers support for QuadSPI features without making any assumptions about the type of serial flash which is used. Device-specific drivers can be developed on top of the QuadSPI driver to add support for device-specific features.

Functionality

Initialization

The QuadSPI driver must be initialized by the application prior to initializing any serial flash driver, by calling `QSPI_DRV_Init()`. The configuration of the AHB buffers can also be set from the application by calling `QSPI_DRV_AhbSetup()`.

Configuration

Other configuration functions are provided to be called from the serial flash driver, to customize the flash operations according to the particularities of a specific device. `QSPI_DRV_SetLut()` can be used to configure the QuadSPI look-up table with the structure of the commands accepted by the device. `QSPI_DRV_LockLut()` and `QSPI_DRV_UnlockLut()` can optionally be used to secure the look-up table for protection against accidental writes. `QSPI_DRV_ClearIpSeqPointer()` and `QSPI_DRV_ClearAHBSeqPointer()` can be useful for devices which support burst modes for enhancing performance, by accepting a reduced command format for subsequent read accesses. `QSPI_DRV_SetAhbSeqId()` is needed to enable AHB operation by setting the sequence number for the read command.

Flash Commands

The QuadSPI driver implements several types of flash commands:

- `QSPI_DRV_IpCommand()` implements simple commands which do not require additional parameters. Due to the fact that these commands are very short and they are sometime used by serial flash drivers inside bigger state machines, this function only offers synchronous functionality.
- `QSPI_DRV_IpErase()` implements an erase operation, which only requires an address parameter. Since these operations take a very long time, the function only offers asynchronous functionality. After calling this function the serial flash drivers have to poll the serial flash device in order to detect the end of the operation.
- `QSPI_DRV_IpRead()` implements a read operation. This function can work in 3 modes: normal read, program verify and blank check. Please see the function description for more details on the usage of these modes. The `QSPI_DRV_IpRead()` function can work in synchronous mode (recommended for short operations like reading a status or control register) or asynchronous mode (recommended for reading large amounts of data). Only normal reads can work in DMA mode, other read modes must use synchronous mode or asynchronous interrupt mode.
- `QSPI_DRV_IpWrite()` implements a write operation. This function can work in synchronous mode (recommended for short operations like writing a status or control register) or asynchronous mode (recommended for writing large amounts of data). Asynchronous transfer can be either in interrupt or DMA modes, depending on the driver initialization settings.

The status of the asynchronous commands can be determined by calling `QSPI_DRV_IpGetStatus()`. Please note that this does not necessarily mean that the command is completed. Write and erase operations may require additional time to complete in the serial flash device. The serial flash driver must poll the device to get the status of the operation.

Important Notes

- Some of the initialization settings must be configured according to the needs of serial flash driver being used. See the documentation of the serial flash driver for information about the configuration needs of each driver.

If the configuration tool is used, it will indicate required settings by making them read-only in the QuadSPI component.

- Due to the high speed of the communication interrupt mode only works for amounts of data which can fit in the module's Rx/Tx FIFOs. For S32K148 this size is 128 bytes. For larger data sizes DMA mode can be used.
- The driver should only be used with SPL as system clock source. This is a hardware restriction from the QSPI module.
- When switching the system modes between HSRUN and RUN, the driver should be de-initialized and re-initialized.
- Reading in DMA mode is restricted to buffer sizes multiple of 4
- All writes bigger than the Tx FIFO size are restricted to buffer sizes multiple of 16.
- In DMA mode the buffers used for read and write operations must be aligned to 4 bytes.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\quadspi\quadspi_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc  
${S32SDK_PATH}\platform\drivers\src\quadspi\
```

Compile symbols

No special symbols are required for this component

Dependencies

Clock Manager OS Interface (OSIF) Interrupt Manager (Interrupt) Enhanced Direct Memory Access (eDMA)

- #define **QSPI_AHB_BUFFERS** 4U
Number of AHB buffers in the device.
- #define **QSPI_LUT_LOCK_KEY** 0x5AF05AF0U
Key to lock/unlock LUT.
- enum **qspi_lut_commands_t** {
QSPI_LUT_CMD_STOP = 0U, **QSPI_LUT_CMD_CMD** = 1U, **QSPI_LUT_CMD_ADDR** = 2U, **QSPI_LUT_CMD_DUMMY** = 3U,
QSPI_LUT_CMD_MODE = 4U, **QSPI_LUT_CMD_MODE2** = 5U, **QSPI_LUT_CMD_MODE4** = 6U, **QSPI_LUT_CMD_READ** = 7U,
QSPI_LUT_CMD_WRITE = 8U, **QSPI_LUT_CMD_JMP_ON_CS** = 9U, **QSPI_LUT_CMD_ADDR_DDR** = 10U, **QSPI_LUT_CMD_MODE_DDR** = 11U,
QSPI_LUT_CMD_MODE2_DDR = 12U, **QSPI_LUT_CMD_MODE4_DDR** = 13U, **QSPI_LUT_CMD_READ_DDR** = 14U, **QSPI_LUT_CMD_WRITE_DDR** = 15U,
QSPI_LUT_CMD_CMD_DDR = 17U, **QSPI_LUT_CMD_CADDR** = 18U, **QSPI_LUT_CMD_CADDR_DDR** = 19U }
Lut commands Implements : qspi_lut_commands_t Class.
- enum **qspi_lut_pads_t** { **QSPI_LUT_PADS_1** = 0U, **QSPI_LUT_PADS_2** = 1U, **QSPI_LUT_PADS_4** = 2U, **QSPI_LUT_PADS_8** = 3U }

- Lut pad options Implements : `qspi_lut_pads_t` Class.*
- enum `qspi_transfer_type_t` { `QSPI_TRANSFER_TYPE_SYNC` = 0U, `QSPI_TRANSFER_TYPE_ASYNC` ↔ `INT` = 1U, `QSPI_TRANSFER_TYPE_ASYNC_DMA` = 2U }
- Driver type Implements : `qspi_transfer_type_t` Class.*
- enum `qspi_read_mode_t` { `QSPI_READ_MODE_INTERNAL_SAMPLING` = 0U, `QSPI_READ_MODE_IN` ↔ `TERNAL_DQS` = 1U, `QSPI_READ_MODE_LOOPBACK_DQS` = 2U, `QSPI_READ_MODE_EXTERNAL` ↔ `DQS` = 3U }
- Read mode Implements : `qspi_read_mode_t` Class.*
- enum `qspi_endianness_t` { `QSPI_END_64BIT_BE` = 0U, `QSPI_END_32BIT_LE` = 1U, `QSPI_END_32BIT_BE` = 2U, `QSPI_END_64BIT_LE` = 3U }
- Endianness options Implements : `qspi_endianness_t` Class.*
- enum `qspi_clock_src_t` { `QSPI_CLK_SRC_PLL_DIV1` = 0U, `QSPI_CLK_SRC_FIRC_DIV1` = 1U }
- Source of QuadSPI internal reference clock Implements : `qspi_clock_src_t` Class.*
- enum `qspi_date_rate_t` { `QSPI_DATE_RATE_SDR` = 0U, `QSPI_DATE_RATE_DDR` = 1U }
- Clock phase used for sampling Rx data Implements : `qspi_date_rate_t` Class.*
- enum `qspi_flash_side_t` { `QSPI_FLASH_SIDE_A` = 0U, `QSPI_FLASH_SIDE_B` = 1U }
- External flash connection options (side A/B) Implements : `qspi_flash_side_t` Class.*
- enum `qspi_sample_delay_t` { `QSPI_SAMPLE_DELAY_1` = 0U, `QSPI_SAMPLE_DELAY_2` = 1U }
- Delay used for sampling Rx data Implements : `qspi_sample_delay_t` Class.*
- enum `qspi_sample_phase_t` { `QSPI_SAMPLE_PHASE_NON_INVERTED` = 0U, `QSPI_SAMPLE_PHASE` ↔ `_INVERTED` = 1U }
- Clock phase used for sampling Rx data Implements : `qspi_sample_phase_t` Class.*
- typedef void(* `qspi_callback_t`) (uint32_t instance, void *param)
- QuadSPI callback function type.*
- QuadSPI_Type *const `g_qspiBase` [QuadSPI_INSTANCE_COUNT]
- Table of base addresses for QuadSPI instances.*

17.117.2 Macro Definition Documentation

17.117.2.1 #define QSPI_AHB_BUFFERS 4U

Number of AHB buffers in the device.

Definition at line 34 of file `quadspi_driver.h`.

17.117.2.2 #define QSPI_LUT_LOCK_KEY 0x5AF05AF0U

Key to lock/unlock LUT.

Definition at line 38 of file `quadspi_driver.h`.

17.117.3 Typedef Documentation

17.117.3.1 typedef void(* qspi_callback_t) (uint32_t instance, void *param)

QuadSPI callback function type.

Definition at line 164 of file `quadspi_driver.h`.

17.117.4 Enumeration Type Documentation

17.117.4.1 enum qspi_clock_src_t

Source of QuadSPI internal reference clock Implements : `qspi_clock_src_t` Class.

Definition at line 114 of file `quadspi_driver.h`.

17.117.4.2 enum qspi_date_rate_t

Clock phase used for sampling Rx data Implements : qspi_date_rate_t_Class.

Definition at line 123 of file quadspi_driver.h.

17.117.4.3 enum qspi_endianness_t

Endianness options Implements : qspi_endianness_t_Class.

Definition at line 103 of file quadspi_driver.h.

17.117.4.4 enum qspi_flash_side_t

External flash connection options (side A/B) Implements : qspi_flash_side_t_Class.

Definition at line 133 of file quadspi_driver.h.

17.117.4.5 enum qspi_lut_commands_t

Lut commands Implements : qspi_lut_commands_t_Class.

Definition at line 43 of file quadspi_driver.h.

17.117.4.6 enum qspi_lut_pads_t

Lut pad options Implements : qspi_lut_pads_t_Class.

Definition at line 69 of file quadspi_driver.h.

17.117.4.7 enum qspi_read_mode_t

Read mode Implements : qspi_read_mode_t_Class.

Definition at line 91 of file quadspi_driver.h.

17.117.4.8 enum qspi_sample_delay_t

Delay used for sampling Rx data Implements : qspi_sample_delay_t_Class.

Definition at line 143 of file quadspi_driver.h.

17.117.4.9 enum qspi_sample_phase_t

Clock phase used for sampling Rx data Implements : qspi_sample_phase_t_Class.

Definition at line 152 of file quadspi_driver.h.

17.117.4.10 enum qspi_transfer_type_t

Driver type Implements : qspi_transfer_type_t_Class.

Definition at line 80 of file quadspi_driver.h.

17.117.5 Variable Documentation**17.117.5.1 QuadSPI_Type* const g_qspiBase[QuadSPI_INSTANCE_COUNT]**

Table of base addresses for QuadSPI instances.

17.118 RTC Driver

17.118.1 Detailed Description

Real Time Clock Peripheral Driver.

This section describes the programming interface of the RTC driver.

Data Structures

- struct [rtc_timedate_t](#)
RTC Time Date structure Implements : [rtc_timedate_t_Class](#). [More...](#)
- struct [rtc_init_config_t](#)
RTC Initialization structure Implements : [rtc_init_config_t_Class](#). [More...](#)
- struct [rtc_alarm_config_t](#)
RTC alarm configuration Implements : [rtc_alarm_config_t_Class](#). [More...](#)
- struct [rtc_interrupt_config_t](#)
RTC interrupt configuration. It is used to configure interrupt other than Time Alarm and Time Seconds interrupt Implements : [rtc_interrupt_config_t_Class](#). [More...](#)
- struct [rtc_seconds_int_config_t](#)
RTC Seconds Interrupt Configuration Implements : [rtc_seconds_int_config_t_Class](#). [More...](#)
- struct [rtc_register_lock_config_t](#)
RTC Register Lock Configuration Implements : [rtc_register_lock_config_t_Class](#). [More...](#)

Macros

- #define [SECONDS_IN_A_DAY](#) (86400UL)
- #define [SECONDS_IN_A_HOUR](#) (3600U)
- #define [SECONDS_IN_A_MIN](#) (60U)
- #define [MINS_IN_A_HOUR](#) (60U)
- #define [HOURS_IN_A_DAY](#) (24U)
- #define [DAYS_IN_A_YEAR](#) (365U)
- #define [DAYS_IN_A_LEAP_YEAR](#) (366U)
- #define [YEAR_RANGE_START](#) (1970U)
- #define [YEAR_RANGE_END](#) (2099U)

Enumerations

- enum [rtc_second_int_cfg_t](#) {
[RTC_INT_1HZ](#) = 0x00U, [RTC_INT_2HZ](#) = 0x01U, [RTC_INT_4HZ](#) = 0x02U, [RTC_INT_8HZ](#) = 0x03U,
[RTC_INT_16HZ](#) = 0x04U, [RTC_INT_32HZ](#) = 0x05U, [RTC_INT_64HZ](#) = 0x06U, [RTC_INT_128HZ](#) = 0x07U }
RTC Seconds interrupt configuration Implements : [rtc_second_int_cfg_t_Class](#).
- enum [rtc_clk_out_config_t](#) { [RTC_CLKOUT_DISABLED](#) = 0x00U, [RTC_CLKOUT_SRC_TSIC](#) = 0x01U, [RTC_CLKOUT_SRC_32KHZ](#) = 0x02U }
RTC CLKOUT pin configuration Implements : [rtc_clk_out_config_t_Class](#).
- enum [rtc_clk_select_t](#) { [RTC_CLK_SRC_OSC_32KHZ](#) = 0x00U, [RTC_CLK_SRC_LPO_1KHZ](#) = 0x01U }
RTC clock select Implements : [rtc_clk_select_t_Class](#).
- enum [rtc_lock_register_select_t](#) { [RTC_LOCK_REG_LOCK](#) = 0x00U, [RTC_STATUS_REG_LOCK](#) = 0x01U,
[RTC_CTRL_REG_LOCK](#) = 0x02U, [RTC_TCL_REG_LOCK](#) = 0x03U }
RTC register lock Implements : [rtc_lock_register_select_t_Class](#).

Functions

- status_t [RTC_DRV_Init](#) (uint32_t instance, const [rtc_init_config_t](#) *const rtcUserCfg)

This function initializes the RTC instance with the settings provided by the user via the [rtcUserCfg](#) parameter. The user must ensure that clock is enabled for the RTC instance used. If the Control register is locked then this method returns [STATUS_ERROR](#). In order to clear the CR Lock the user must perform a power-on reset.
- status_t [RTC_DRV_Deinit](#) (uint32_t instance)

This function deinitializes the RTC instance. If the Control register is locked then this method returns [STATUS_ERROR](#).
- void [RTC_DRV_GetDefaultConfig](#) ([rtc_init_config_t](#) *const config)

This function will set the default configuration values into the structure passed as a parameter.
- status_t [RTC_DRV_StartCounter](#) (uint32_t instance)

Start RTC instance counter. Before calling this function the user should use [RTC_DRV_SetTimeDate](#) to configure the start time.
- status_t [RTC_DRV_StopCounter](#) (uint32_t instance)

Disable RTC instance counter.
- status_t [RTC_DRV_GetCurrentTimeDate](#) (uint32_t instance, [rtc_timedate_t](#) *const currentTime)

Get current time and date from RTC instance.
- status_t [RTC_DRV_SetTimeDate](#) (uint32_t instance, const [rtc_timedate_t](#) *const time)

Set time and date for RTC instance. The user must stop the counter before using this function. Otherwise it will return an error.
- status_t [RTC_DRV_ConfigureRegisterLock](#) (uint32_t instance, const [rtc_register_lock_config_t](#) *const lockConfig)

This method configures register lock for the corresponding RTC instance. Remember that all the registers are unlocked only by software reset or power on reset. (Except for CR that is unlocked only by POR).
- void [RTC_DRV_GetRegisterLock](#) (uint32_t instance, [rtc_register_lock_config_t](#) *const lockConfig)

Get which registers are locked for RTC instance.
- status_t [RTC_DRV_ConfigureTimeCompensation](#) (uint32_t instance, uint8_t complInterval, int8_t compensation)

This method configures time compensation. Data is passed by the [complInterval](#) and [compensation](#) parameters. For more details regarding coefficient calculation see the Reference Manual.
- void [RTC_DRV_GetTimeCompensation](#) (uint32_t instance, uint8_t *complInterval, int8_t *compensation)

This retrieves the time compensation coefficients and saves them on the variables referenced by the parameters.
- void [RTC_DRV_ConfigureFaultInt](#) (uint32_t instance, [rtc_interrupt_config_t](#) *const intConfig)

This method configures fault interrupts such as:
- void [RTC_DRV_ConfigureSecondsInt](#) (uint32_t instance, [rtc_seconds_int_config_t](#) *const intConfig)

This method configures the Time Seconds Interrupt with the configuration from the [intConfig](#) parameter.
- status_t [RTC_DRV_ConfigureAlarm](#) (uint32_t instance, [rtc_alarm_config_t](#) *const alarmConfig)

This method configures the alarm with the configuration from the [alarmConfig](#) parameter.
- void [RTC_DRV_GetAlarmConfig](#) (uint32_t instance, [rtc_alarm_config_t](#) *alarmConfig)

Get alarm configuration for RTC instance.
- bool [RTC_DRV_IsAlarmPending](#) (uint32_t instance)

Check if alarm is pending.
- void [RTC_DRV_ConvertSecondsToTimeDate](#) (const uint32_t *seconds, [rtc_timedate_t](#) *const timeDate)

Convert seconds to [rtc_timedate_t](#) structure.
- void [RTC_DRV_ConvertTimeDateToSeconds](#) (const [rtc_timedate_t](#) *const timeDate, uint32_t *const seconds)

Convert seconds to [rtc_timedate_t](#) structure.
- bool [RTC_DRV_IsYearLeap](#) (uint16_t year)

Check if the current year is leap.
- bool [RTC_DRV_IsTimeDateCorrectFormat](#) (const [rtc_timedate_t](#) *const timeDate)

Check if the date time struct is configured properly.
- status_t [RTC_DRV_GetNextAlarmTime](#) (uint32_t instance, [rtc_timedate_t](#) *const alarmTime)

Gets the next alarm time.

- void [RTC_DRV_IRQHandler](#) (uint32_t instance)

This method is the API's Interrupt handler for generic and alarm IRQ. It will handle the alarm repetition and calls the user callbacks if they are not NULL.

- void [RTC_DRV_SecondsIRQHandler](#) (uint32_t instance)

This method is the API's Interrupt handler for RTC Second interrupt. This ISR will call the user callback if defined.

17.118.2 Data Structure Documentation

17.118.2.1 struct rtc_timedate_t

RTC Time Date structure Implements : rtc_timedate_t_Class.

Definition at line 97 of file rtc_driver.h.

Data Fields

- uint16_t [year](#)
- uint16_t [month](#)
- uint16_t [day](#)
- uint16_t [hour](#)
- uint16_t [minutes](#)
- uint8_t [seconds](#)

Field Documentation

17.118.2.1.1 uint16_t day

Day

Definition at line 101 of file rtc_driver.h.

17.118.2.1.2 uint16_t hour

Hour

Definition at line 102 of file rtc_driver.h.

17.118.2.1.3 uint16_t minutes

Minutes

Definition at line 103 of file rtc_driver.h.

17.118.2.1.4 uint16_t month

Month

Definition at line 100 of file rtc_driver.h.

17.118.2.1.5 uint8_t seconds

Seconds

Definition at line 104 of file rtc_driver.h.

17.118.2.1.6 uint16_t year

Year

Definition at line 99 of file rtc_driver.h.

17.118.2.2 struct rtc_init_config_t

RTC Initialization structure Implements : rtc_init_config_t_Class.

Definition at line 111 of file rtc_driver.h.

Data Fields

- uint8_t [compensationInterval](#)
- int8_t [compensation](#)
- [rtc_clk_select_t](#) clockSelect
- [rtc_clk_out_config_t](#) clockOutConfig
- bool [updateEnable](#)
- bool [nonSupervisorAccessEnable](#)

Field Documentation

17.118.2.2.1 rtc_clk_out_config_t clockOutConfig

RTC Clock Out Source

Definition at line 116 of file rtc_driver.h.

17.118.2.2.2 rtc_clk_select_t clockSelect

RTC Clock Select

Definition at line 115 of file rtc_driver.h.

17.118.2.2.3 int8_t compensation

Compensation Value

Definition at line 114 of file rtc_driver.h.

17.118.2.2.4 uint8_t compensationInterval

Compensation Interval

Definition at line 113 of file rtc_driver.h.

17.118.2.2.5 bool nonSupervisorAccessEnable

Enable writes to the registers in non Supervisor Mode

Definition at line 118 of file rtc_driver.h.

17.118.2.2.6 bool updateEnable

Enable changing the Time Counter Enable bit even if the Status register is locked

Definition at line 117 of file rtc_driver.h.

17.118.2.3 struct rtc_alarm_config_t

RTC alarm configuration Implements : rtc_alarm_config_t_Class.

Definition at line 125 of file rtc_driver.h.

Data Fields

- [rtc_timedate_t](#) alarmTime
- uint32_t [repetitionInterval](#)
- uint32_t [numberOfRepeats](#)
- bool [repeatForever](#)

- bool [alarmIntEnable](#)
- void(* [alarmCallback](#))(void *callbackParam)
- void * [callbackParams](#)

Field Documentation

17.118.2.3.1 void(* alarmCallback) (void *callbackParam)

Pointer to the user callback method.

Definition at line 132 of file rtc_driver.h.

17.118.2.3.2 bool alarmIntEnable

Enable alarm interrupt

Definition at line 131 of file rtc_driver.h.

17.118.2.3.3 rtc_timedate_t alarmTime

Alarm time

Definition at line 127 of file rtc_driver.h.

17.118.2.3.4 void* callbackParams

Pointer to the callback parameters.

Definition at line 133 of file rtc_driver.h.

17.118.2.3.5 uint32_t numberOfRepeats

Number of alarm repeats

Definition at line 129 of file rtc_driver.h.

17.118.2.3.6 bool repeatForever

Repeat forever if set, discard number of repeats

Definition at line 130 of file rtc_driver.h.

17.118.2.3.7 uint32_t repetitionInterval

Interval of repetition in sec

Definition at line 128 of file rtc_driver.h.

17.118.2.4 struct rtc_interrupt_config_t

RTC interrupt configuration. It is used to configure interrupt other than Time Alarm and Time Seconds interrupt
Implements : rtc_interrupt_config_t_Class.

Definition at line 141 of file rtc_driver.h.

Data Fields

- bool [overflowIntEnable](#)
- bool [timeInvalidIntEnable](#)
- void(* [rtcCallback](#))(void *callbackParam)
- void * [callbackParams](#)

Field Documentation

17.118.2.4.1 void* callbackParams

Pointer to the callback parameters.

Definition at line 146 of file rtc_driver.h.

17.118.2.4.2 bool overflowIntEnable

Enable Time Overflow Interrupt

Definition at line 143 of file rtc_driver.h.

17.118.2.4.3 void(* rtcCallback)(void *callbackParam)

Pointer to the user callback method.

Definition at line 145 of file rtc_driver.h.

17.118.2.4.4 bool timeInvalidIntEnable

Enable Time Invalid Interrupt

Definition at line 144 of file rtc_driver.h.

17.118.2.5 struct rtc_seconds_int_config_t

RTC Seconds Interrupt Configuration Implements : rtc_seconds_int_config_t_Class.

Definition at line 153 of file rtc_driver.h.

Data Fields

- [rtc_second_int_cfg_t secondIntConfig](#)
- bool [secondIntEnable](#)
- void(* [rtcSecondsCallback](#))(void *callbackParam)
- void * [secondsCallbackParams](#)

Field Documentation**17.118.2.5.1 void(* rtcSecondsCallback)(void *callbackParam)**

Pointer to the user callback method.

Definition at line 157 of file rtc_driver.h.

17.118.2.5.2 rtc_second_int_cfg_t secondIntConfig

Seconds Interrupt frequency

Definition at line 155 of file rtc_driver.h.

17.118.2.5.3 bool secondIntEnable

Seconds Interrupt enable

Definition at line 156 of file rtc_driver.h.

17.118.2.5.4 void* secondsCallbackParams

Pointer to the callback parameters.

Definition at line 158 of file rtc_driver.h.

17.118.2.6 struct rtc_register_lock_config_t

RTC Register Lock Configuration Implements : rtc_register_lock_config_t_Class.

Definition at line 165 of file rtc_driver.h.

Data Fields

- bool [lockRegisterLock](#)
- bool [statusRegisterLock](#)
- bool [controlRegisterLock](#)
- bool [timeCompensationRegisterLock](#)

Field Documentation

17.118.2.6.1 bool controlRegisterLock

Lock state of the Control Register

Definition at line 169 of file rtc_driver.h.

17.118.2.6.2 bool lockRegisterLock

Lock state of the Lock Register

Definition at line 167 of file rtc_driver.h.

17.118.2.6.3 bool statusRegisterLock

Lock state of the Status Register

Definition at line 168 of file rtc_driver.h.

17.118.2.6.4 bool timeCompensationRegisterLock

Lock state of the Time Compensation Register

Definition at line 170 of file rtc_driver.h.

17.118.3 Macro Definition Documentation

17.118.3.1 #define DAYS_IN_A_LEAP_YEAR (366U)

Definition at line 40 of file rtc_driver.h.

17.118.3.2 #define DAYS_IN_A_YEAR (365U)

Definition at line 39 of file rtc_driver.h.

17.118.3.3 #define HOURS_IN_A_DAY (24U)

Definition at line 38 of file rtc_driver.h.

17.118.3.4 #define MINS_IN_A_HOUR (60U)

Definition at line 37 of file rtc_driver.h.

17.118.3.5 #define SECONDS_IN_A_DAY (86400UL)

Definition at line 34 of file rtc_driver.h.

17.118.3.6 #define SECONDS_IN_A_HOUR (3600U)

Definition at line 35 of file rtc_driver.h.

17.118.3.7 #define SECONDS_IN_A_MIN (60U)

Definition at line 36 of file rtc_driver.h.

17.118.3.8 #define YEAR_RANGE_END (2099U)

Definition at line 42 of file rtc_driver.h.

17.118.3.9 #define YEAR_RANGE_START (1970U)

Definition at line 41 of file rtc_driver.h.

17.118.4 Enumeration Type Documentation

17.118.4.1 enum rtc_clk_out_config_t

RTC CLKOUT pin configuration Implements : rtc_clk_out_config_t_Class.

Enumerator

- RTC_CLKOUT_DISABLED** Clock out pin is disabled
- RTC_CLKOUT_SRC_TSIC** Output on RTC_CLKOUT as configured on Time seconds interrupt
- RTC_CLKOUT_SRC_32KHZ** Output on RTC_CLKOUT of the 32KHz clock

Definition at line 64 of file rtc_driver.h.

17.118.4.2 enum rtc_clk_select_t

RTC clock select Implements : rtc_clk_select_t_Class.

Enumerator

- RTC_CLK_SRC_OSC_32KHZ** RTC Prescaler increments using 32 KHz crystal
- RTC_CLK_SRC_LPO_1KHZ** RTC Prescaler increments using 1KHz LPO

Definition at line 75 of file rtc_driver.h.

17.118.4.3 enum rtc_lock_register_select_t

RTC register lock Implements : rtc_lock_register_select_t_Class.

Enumerator

- RTC_LOCK_REG_LOCK** RTC Lock Register lock
- RTC_STATUS_REG_LOCK** RTC Status Register lock
- RTC_CTRL_REG_LOCK** RTC Control Register lock
- RTC_TCL_REG_LOCK** RTC Time Compensation Reg lock

Definition at line 85 of file rtc_driver.h.

17.118.4.4 enum rtc_second_int_cfg_t

RTC Seconds interrupt configuration Implements : rtc_second_int_cfg_t_Class.

Enumerator

- RTC_INT_1HZ** RTC seconds interrupt occurs at 1 Hz
- RTC_INT_2HZ** RTC seconds interrupt occurs at 2 Hz

RTC_INT_4HZ RTC seconds interrupt occurs at 4 Hz
RTC_INT_8HZ RTC seconds interrupt occurs at 8 Hz
RTC_INT_16HZ RTC seconds interrupt occurs at 16 Hz
RTC_INT_32HZ RTC seconds interrupt occurs at 32 Hz
RTC_INT_64HZ RTC seconds interrupt occurs at 64 Hz
RTC_INT_128HZ RTC seconds interrupt occurs at 128 Hz

Definition at line 48 of file rtc_driver.h.

17.118.5 Function Documentation

17.118.5.1 `status_t RTC_DRV_ConfigureAlarm (uint32_t instance, rtc_alarm_config_t *const alarmConfig)`

This method configures the alarm with the configuration from the alarmConfig parameter.

Parameters

in	<i>instance</i>	The number of the RTC instance used
in	<i>alarmConfig</i>	Pointer to the structure which holds the alarm configuration

Returns

STATUS_SUCCESS if the configuration is successful or STATUS_ERROR if the alarm time is invalid.

Definition at line 933 of file rtc_driver.c.

17.118.5.2 `void RTC_DRV_ConfigureFaultInt (uint32_t instance, rtc_interrupt_config_t *const intConfig)`

This method configures fault interrupts such as:

- Time Overflow Interrupt
- Time Invalid Interrupt with the user provided configuration struct intConfig.

Parameters

in	<i>instance</i>	The number of the RTC instance used
in	<i>intConfig</i>	Pointer to the structure which holds the configuration

Returns

None

Definition at line 876 of file rtc_driver.c.

17.118.5.3 `status_t RTC_DRV_ConfigureRegisterLock (uint32_t instance, const rtc_register_lock_config_t *const lockConfig)`

This method configures register lock for the corresponding RTC instance. Remember that all the registers are unlocked only by software reset or power on reset. (Except for CR that is unlocked only by POR).

Parameters

in	<i>instance</i>	The number of the RTC instance used
in	<i>lockConfig</i>	Pointer to the lock configuration structure

Returns

STATUS_SUCCESS if the operation was successful, STATUS_ERROR if the Lock Register is locked.

Definition at line 426 of file rtc_driver.c.

17.118.5.4 void RTC_DRV_ConfigureSecondsInt (uint32_t *instance*, rtc_seconds_int_config_t *const *intConfig*)

This method configures the Time Seconds Interrupt with the configuration from the intConfig parameter.

Parameters

in	<i>instance</i>	The number of the RTC instance used
in	<i>intConfig</i>	Pointer to the structure which holds the configuration

Returns

None

Definition at line 903 of file rtc_driver.c.

17.118.5.5 status_t RTC_DRV_ConfigureTimeCompensation (uint32_t *instance*, uint8_t *complInterval*, int8_t *compensation*)

This method configures time compensation. Data is passed by the complInterval and compensation parameters. For more details regarding coefficient calculation see the Reference Manual.

Parameters

in	<i>instance</i>	The number of the RTC instance used
in	<i>complInterval</i>	Compensation interval
in	<i>compensation</i>	Compensation value

Returns

STATUS_SUCCESS if the operation was successful, STATUS_ERROR if the TC Register is locked.

Definition at line 501 of file rtc_driver.c.

17.118.5.6 void RTC_DRV_ConvertSecondsToTimeDate (const uint32_t * *seconds*, rtc_timedate_t *const *timeDate*)

Convert seconds to [rtc_timedate_t](#) structure.

Parameters

in	<i>seconds</i>	Pointer to the seconds
out	<i>timeDate</i>	Pointer to the structure in which to store the result

Returns

None

Definition at line 551 of file rtc_driver.c.

17.118.5.7 void RTC_DRV_ConvertTimeDateToSeconds (const rtc_timedate_t *const *timeDate*, uint32_t *const *seconds*)

Convert seconds to [rtc_timedate_t](#) structure.

Parameters

in	<i>timeDate</i>	Pointer to the source struct
out	<i>seconds</i>	Pointer to the variable in which to store the result

Returns

None

Definition at line 645 of file rtc_driver.c.

17.118.5.8 status_t RTC_DRV_Deinit (uint32_t instance)

This function deinitializes the RTC instance. If the Control register is locked then this method returns STATUS_ERROR.

Parameters

in	<i>instance</i>	The number of the RTC instance used
----	-----------------	-------------------------------------

Returns

STATUS_SUCCESS if the operation was successful or STATUS_ERROR if Control register is locked.

Definition at line 158 of file rtc_driver.c.

17.118.5.9 void RTC_DRV_GetAlarmConfig (uint32_t instance, rtc_alarm_config_t * alarmConfig)

Get alarm configuration for RTC instance.

Parameters

in	<i>instance</i>	The number of the RTC instance used
out	<i>alarmConfig</i>	Pointer to the structure in which to store the alarm configuration

Returns

None

Definition at line 987 of file rtc_driver.c.

17.118.5.10 status_t RTC_DRV_GetCurrentTimeDate (uint32_t instance, rtc_timedate_t *const currentTime)

Get current time and date from RTC instance.

Parameters

in	<i>instance</i>	The number of the RTC instance used
out	<i>currentTime</i>	Pointer to the variable in which to store the result

Returns

STATUS_SUCCESS if the operation was successful, STATUS_ERROR if there was a problem.

Definition at line 327 of file rtc_driver.c.

17.118.5.11 void RTC_DRV_GetDefaultConfig (rtc_init_config_t *const config)

This function will set the default configuration values into the structure passed as a parameter.

Parameters

out	<i>config</i>	Pointer to the structure in which the configuration will be saved.
-----	---------------	--

Returns

None

Definition at line 194 of file rtc_driver.c.

17.118.5.12 `status_t RTC_DRV_GetNextAlarmTime (uint32_t instance, rtc_timedate_t *const alarmTime)`

Gets the next alarm time.

Parameters

in	<i>instance</i>	The number of the RTC instance used
out	<i>alarmTime</i>	Pointer to the variable in which to store the data

Returns

STATUS_SUCCESS if the next alarm time is valid, STATUS_ERROR if there is no new alarm or alarm configuration specified.

Definition at line 1019 of file rtc_driver.c.

17.118.5.13 `void RTC_DRV_GetRegisterLock (uint32_t instance, rtc_register_lock_config_t *const lockConfig)`

Get which registers are locked for RTC instance.

Parameters

in	<i>instance</i>	The number of the RTC instance used
out	<i>lockConfig</i>	Pointer to the lock configuration structure in which to save the data

Returns

None

Definition at line 473 of file rtc_driver.c.

17.118.5.14 `void RTC_DRV_GetTimeCompensation (uint32_t instance, uint8_t * complInterval, int8_t * compensation)`

This retrieves the time compensation coefficients and saves them on the variables referenced by the parameters.

Parameters

in	<i>instance</i>	The number of the RTC instance used
out	<i>complInterval</i>	Pointer to the variable in which to save the compensation interval
out	<i>compensation</i>	Pointer to the variable in which to save the compensation value

Returns

None

Definition at line 534 of file rtc_driver.c.

17.118.5.15 `status_t RTC_DRV_Init (uint32_t instance, const rtc_init_config_t *const rtcUserCfg)`

This function initializes the RTC instance with the settings provided by the user via the rtcUserCfg parameter. The user must ensure that clock is enabled for the RTC instance used. If the Control register is locked then this method returns STATUS_ERROR. In order to clear the CR Lock the user must perform a power-on reset.

Parameters

in	<i>instance</i>	The number of the RTC instance used
in	<i>rtcUserCfg</i>	Pointer to the user's configuration structure

Returns

STATUS_SUCCESS if the operation was successful, STATUS_ERROR if Control is locked.

Definition at line 97 of file rtc_driver.c.

17.118.5.16 void RTC_DRV_IRQHandler (uint32_t *instance*)

This method is the API's Interrupt handler for generic and alarm IRQ. It will handle the alarm repetition and calls the user callbacks if they are not NULL.

Parameters

in	<i>instance</i>	RTC instance used
----	-----------------	-------------------

Returns

None

Definition at line 773 of file rtc_driver.c.

17.118.5.17 bool RTC_DRV_IsAlarmPending (uint32_t *instance*)

Check if alarm is pending.

Parameters

in	<i>instance</i>	The number of the RTC instance used
----	-----------------	-------------------------------------

Returns

True if the alarm has occurred, false if not

Definition at line 1002 of file rtc_driver.c.

17.118.5.18 bool RTC_DRV_IsTimeDateCorrectFormat (const rtc_timedate_t *const *timeDate*)

Check if the date time struct is configured properly.

Parameters

in	<i>timeDate</i>	Structure to check to check
----	-----------------	-----------------------------

Returns

True if the time date is in the correct format, false if not

Definition at line 695 of file rtc_driver.c.

17.118.5.19 bool RTC_DRV_IsYearLeap (uint16_t *year*)

Check if the current year is leap.

Parameters

<i>in</i>	<i>year</i>	Year to check
-----------	-------------	---------------

Returns

True if the year is leap, false if not

Definition at line 737 of file rtc_driver.c.

17.118.5.20 void RTC_DRV_SecondsIRQHandler (uint32_t *instance*)

This method is the API's Interrupt handler for RTC Second interrupt. This ISR will call the user callback if defined.

Parameters

<i>in</i>	<i>instance</i>	RTC instance used
-----------	-----------------	-------------------

Returns

None

Definition at line 850 of file rtc_driver.c.

17.118.5.21 status_t RTC_DRV_SetTimeDate (uint32_t *instance*, const rtc_timedate_t *const *time*)

Set time and date for RTC instance. The user must stop the counter before using this function. Otherwise it will return an error.

Parameters

<i>in</i>	<i>instance</i>	The number of the RTC instance used
<i>in</i>	<i>time</i>	Pointer to the variable in which the time is stored

Returns

STATUS_SUCCESS if the operation was successful, STATUS_ERROR if the time provided was invalid or if the counter was not stopped.

Definition at line 382 of file rtc_driver.c.

17.118.5.22 status_t RTC_DRV_StartCounter (uint32_t *instance*)

Start RTC instance counter. Before calling this function the user should use RTC_DRV_SetTimeDate to configure the start time.

Parameters

<i>in</i>	<i>instance</i>	The number of the RTC instance used
-----------	-----------------	-------------------------------------

Returns

STATUS_SUCCESS if the operation was successful, STATUS_ERROR if the counter cannot be enabled or is already enabled.

Definition at line 265 of file rtc_driver.c.

17.118.5.23 status_t RTC_DRV_StopCounter (uint32_t *instance*)

Disable RTC instance counter.

Parameters

<code>in</code>	<code>instance</code>	The number of the RTC instance used
-----------------	-----------------------	-------------------------------------

Returns

STATUS_SUCCESS if the operation was successful, STATUS_ERROR if the counter could not be stopped.

Definition at line 296 of file rtc_driver.c.

17.119 Raw API

17.119.1 Detailed Description

The raw API is operating on PDU level and it is typically used to gateway PDUs between CAN and LIN.

Usually, a FIFO is used to buffer PDUs in order to handle the different bus speeds.

Functions

- void [ld_put_raw](#) (I_ifc_handle iii, const I_u8 *const data)
Queue the transmission of 8 bytes of data in one frame.
- void [ld_get_raw](#) (I_ifc_handle iii, I_u8 *const data)
Copy the oldest received diagnostic frame data to the memory specified by data.
- I_u8 [ld_raw_tx_status](#) (I_ifc_handle iii)
Get the status of the raw frame transmission function.
- I_u8 [ld_raw_rx_status](#) (I_ifc_handle iii)
Get the status of the raw frame receive function.

17.119.2 Function Documentation

17.119.2.1 void ld_get_raw (I_ifc_handle iii, I_u8 *const data)

Copy the oldest received diagnostic frame data to the memory specified by data.

Parameters

in	iii	Interface name
in	data	Buffer for the data to be transmitted

Returns

void

Copy the oldest received diagnostic frame data to the memory specified by data. The data returned is received from master request frame for slave node and the slave response frame for master node.

Definition at line 161 of file lin_commontl_api.c.

17.119.2.2 void ld_put_raw (I_ifc_handle iii, const I_u8 *const data)

Queue the transmission of 8 bytes of data in one frame.

Parameters

in	iii	Interface name
in	data	Buffer for the data to be transmitted

Returns

void

Queue the transmission of 8 bytes of data in one frame The data is sent in the next suitable frame.

Definition at line 129 of file lin_commontl_api.c.

17.119.2.3 I_u8 ld_raw_rx_status (I_ifc_handle iii)

Get the status of the raw frame receive function.

Parameters

<i>in</i>	<i>iii</i>	Interface name
-----------	------------	----------------

Returns

l_u8

Get the status of the raw frame receive function: LD_NO_DATA The receive queue is empty.(For LIN2.1 and above only) LD_DATA_AVAILABLE The receive queue contains data that can be read. LD_RECEIVE_ERROR LIN protocol errors occurred during the transfer; initialize and redo the transfer.(For LIN2.1 and above only). LD_TRANSFER_ERROR: (For LIN2.0 and J2602 only) LIN protocol errors occurred during the transfer; initialize and redo the transfer.

Definition at line 193 of file lin_commontl_api.c.

17.119.2.4 *l_u8* ld_raw_tx_status (*l_ifc_handle iii*)

Get the status of the raw frame transmission function.

Parameters

<i>in</i>	<i>iii</i>	Interface name
-----------	------------	----------------

Returns

l_u8

Get the status of the raw frame transmission function: This function is available for < br / > LD_QUEUE_EMPTY : The transmit queue is empty. In case previous calls to < br / > ld_put_raw, all frames in the queue have been < br / > transmitted. < br / > LD_QUEUE_AVAILABLE: The transmit queue contains entries, but is not full. < br / > (For LIN2.1 and above only). LD_QUEUE_FULL : The transmit queue is full and can not accept further < br / > frames. < br / > LD_TRANSMIT_ERROR : (For LIN2.1 and above only) LIN protocol errors occurred during the transfer; initialize and redo the transfer. LD_TRANSFER_ERROR: (For LIN2.0 and J2602 only) LIN protocol errors occurred during the transfer; initialize and redo the transfer.

Definition at line 178 of file lin_commontl_api.c.

17.120 Real Time Clock Driver (RTC)

17.120.1 Detailed Description

The S32 SDK provides the Peripheral Driver for the Real Time Clock (RTC) module of S32 SDK devices.

Hardware background

The Real Time Clock Module is a independent timer that keeps track of the exact date and time with no software overhead, with low power usage.

Features of the RTC module include:

- 32-bit seconds counter with roll-over protection and 32-bit alarm
- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Option to increment prescaler using the LPO (prescaler increments by 32 every clock edge)
- Register write protection
- Lock register requires POR or software reset to enable write access
- Configurable 1, 2, 4, 8, 16, 32, 64 or 128 Hz square wave output with optional interrupt
- Alarm interrupt configured by the driver automatically refreshes alarm time configured by the user
- User interrupt handlers can be configured for all interrupts

How to use the RTC driver in your application

In order to be able to use the RTC in your application, the first thing to do is initializing it with the desired configuration. This is done by calling the **RTC_DRV_Init** function. One of the arguments passed to this function is the configuration which will be used for the RTC instance, specified by the **rtc_init_config_t** structure.

The **rtc_init_config_t** structure allows you to configure the following:

- RTC clock source (32 KHz clock or 1 KHz LPO clock)
- Clock Out pin configuration (Clock OUT pin source)
- Compensation (Interval and value)
- Update enable - this allows updates to Time Counter Enable bit if the Status Register under limited conditions
- Enable non supervisor writes to the registers

The **rtc_seconds_int_config_t** structure configures the **time seconds interrupt**. To setup an interrupt every seconds you have to configure the structure mentioned with the following parameters:

- Frequency of the interrupt
- Interrupt Handler
- If needed - interrupt handler parameters

An alarm is configured with **rtc_alarm_config_t** structure, which is described by the following parameters:

- Alarm time in date-time format
- Interval of alarm repeat in seconds
- Number of alarm repeats (use 0 if the alarm is not recursive)
- Repeat forever field (if set, the number of repeats field will be ignored)

- Alarm interrupt enable
- Alarm interrupt handler
- Alarm interrupt handler parameters

Note

If the alarm interrupt is not enabled, the user must make the updates of the alarm time manually.

After the [RTC_DRV_Init\(\)](#) function call and, if needed, alarm and other configurations the RTC counter is started by calling [RTC_DRV_StartCounter\(\)](#).

To update desired time date use [RTC_DRV_SetTimeDate\(\)](#) function, this method uses a Time and Date structure [rtc_timedate_t](#) in a calendar format mode.

To get the current time and date you can call [RTC_DRV_GetCurrentTimeDate\(\)](#) function, this method will get the seconds from the Time Seconds Register and will convert into human readable format as [rtc_timedate_t](#).

To check if a structure [rtc_timedate_t](#) is properly configured use [RTC_DRV_IsTimeDateCorrectFormat\(\)](#) function that will return true if configuration is valid or false if configuration is invalid.

To set an alarm at a desired date and time use [RTC_DRV_ConfigureAlarm\(\)](#) function, this method uses a structure [rtc_alarm_config_t](#) with Time, Date and Alarm Handler and will trigger at set time an interrupt set by user.

To get the configured alarm use [RTC_DRV_GetAlarmConfig\(\)](#) function, this method will return the Time and Date for alarm in a structure [rtc_alarm_config_t](#).

To check if an alarm is pending use [RTC_DRV_IsAlarmPending\(\)](#) function, this method will return true if alarm is pending or false if no alarm pending.

To configure a seconds interrupt use [RTC_DRV_ConfigureSecondsInt\(\)](#) function, this method use structure [rtc_↵_seconds_int_config_t](#) to be configured with a callback function.

After driver configuration the user can use [RTC_DRV_StartCounter\(\)](#) function to start the timer and [RTC_DRV_↵StopCounter\(\)](#) function to stop it.

To lock access to RTC registers use [RTC_DRV_ConfigureRegisterLock\(\)](#) function, this method uses a structure [rtc_register_lock_config_t](#) that describes what registers will be locked. Attention all the registers are unlocked only by software reset or power on reset.

To check if RTC registers are locked use [RTC_DRV_GetRegisterLock\(\)](#) function, this will return a structure [rtc_↵register_lock_config_t](#) with locked registers.

To convert seconds to a human readable value use [RTC_DRV_ConvertSecondsToTimeDate\(\)](#) function, this will return a structure [rtc_timedate_t](#) based on the seconds value.

To convert a time date to seconds use [RTC_DRV_ConvertTimeDateToSeconds\(\)](#) function, this will return seconds value based on time date structure [rtc_timedate_t](#).

To get the time date for next alarm use [RTC_DRV_GetNextAlarmTime\(\)](#) function, this will return a structure [rtc_↵timedate_t](#).

To configure a fault handler for cases as Overflow and Invalid Time use [RTC_DRV_ConfigureFaultInt\(\)](#) function, this method will use a structure [rtc_interrupt_config_t](#) with a callback function.

Example

```
/* Time Seconds interrupt handler */
void secondsISR(void)
{
    /* Do Something */
}

void rtcAlarmCallback(void)
{
    rtc_timedate_t currentTime;
    RTC_DRV_GetCurrentTimeDate(0U, &currentTime);

    /* Do something with the time and date */
}
```

```

}

int main()
{
    rtc_seconds_int_config_t rtcTimer1_SecIntConfig0 =
    {
        .secondIntConfig          =    RTC_INT_1HZ,
        .secondIntEnable          =    true,
        .rtcSecondsCallback       =    secondsISR,
        .secondsCallbackParams    =    NULL
    };

    /* rtcTimer1 configuration structure */
    const rtc_init_config_t rtcTimer1_Config0 =
    {
        /* Time compensation interval */
        .compensationInterval     =    0U,
        /* Time compensation value */
        .compensation             =    0,
        /* RTC Clock Source is 32 KHz crystal */
        .clockSelect              =    RTC_CLK_SRC_OSC_32KHZ,
        /* RTC Clock Out is 32 KHz clock */
        .clockOutConfig           =    RTC_CLKOUT_SRC_32KHZ,
        /* Update of the TCE bit is not allowed */
        .updateEnable             =    false,
        /* Non-supervisor mode write accesses are not supported and generate
         * a bus error.
         */
        .nonSupervisorAccessEnable =    false
    };

    /* RTC Initial Time and Date */
    rtc_timedate_t    rtcStartTime =
    {
        /* Year */
        .year          =    2016U,
        /* Month */
        .month         =    01U,
        /* Day */
        .day           =    01U,
        /* Hour */
        .hour          =    00U,
        /* Minutes */
        .minutes       =    00U,
        /* Seconds */
        .seconds       =    00U
    };

    /* rtcTimer1 Alarm configuration 0 */
    rtc_alarm_config_t    alarmConfig0 =
    {
        /* Alarm Date */
        .alarmTime        =
        {
            /* Year */
            .year          =    2016U,
            /* Month */
            .month         =    01U,
            /* Day */
            .day           =    01U,
            /* Hour */
            .hour          =    00U,
            /* Minutes */
            .minutes       =    00U,
            /* Seconds */
            .seconds       =    03U,
        },

        /* Alarm repeat interval */
        .repetitionInterval =    3UL,

        /* Number of alarm repeats */
        .numberOfRepeats    =    0UL,

        /* Repeat alarm forever */
        .repeatForever      =    true,

        /* Alarm interrupt disabled */
        .alarmIntEnable     =    true,

        /* Alarm interrupt handler */
        .alarmCallback      =    (void *)rtcAlarmCallback,

        /* Alarm interrupt handler parameters */
        .callbackParams     =    (void *)NULL
    };
}

```

```

/* Call the init function */
RTC_DRV_Init(0UL, &rtcInitConfig);

/* Set the time and date */
RTC_DRV_SetTimeDate(0UL, &rtcStartTime);

/* Configure RTC Time Seconds Interrupt */
RTC_DRV_ConfigureSecondsInt(0UL, &rtcTimer1_SecIntConfig0);

/* Start RTC counter */
RTC_DRV_StartCounter(0UL);

/* Configure an alarm every 3 seconds */
RTC_DRV_ConfigureAlarm(0UL, &rtcAlarmConfig0);

while(1);
}

```

Important Notes

- Before using the RTC driver the module clock must be configured

Note

When using the on chip LPO clock as source input for the RTC, the user needs to make sure that the LPO generates the desired frequency by adjusting the LPO trimming value.

For more details about LPO trimming please consult the available documentation.

- The driver enables the interrupts for the corresponding RTC module, but any interrupt priority must be done by the application
- The board specific configurations must be done prior to driver calls; the driver has no influence on the functionality of the clockout pin - they must be configured by application
- If Non-supervisor mode write accesses are supported you need to set AIPS to allow usermode access to RTC Memory Space

Integration guideline

Compilation units

The following files need to be compiled in the project:

```

${S32SDK_PATH}\platform\drivers\src\rtc\rtc_driver.c
${S32SDK_PATH}\platform\drivers\src\rtc\rtc_hw_access.c
${S32SDK_PATH}\platform\drivers\src\rtc\rtc_irq.c

```

Include path

The following paths need to be added to the include path of the toolchain:

```

${S32SDK_PATH}\platform\drivers\inc\

```

Compile symbols

No special symbols are required for this component

Dependencies

1. [Clock Manager](#)
2. [Interrupt Manager \(Interrupt\)](#)

Modules

- [RTC Driver](#)
Real Time Clock Peripheral Driver.

17.121 Register address map

17.121.1 Detailed Description

The SPI protocol requires the first byte transmitted on MOSI line to be set to register address the user wants to access (write/read). The byte consists of ADDRESS[7:1] and READ_BIT[0]. This section lists all the register addresses available on UJA113x devices which can be used throughout the source code instead of fixed values. The defined addresses are already shifted.

The address is useful in [UJA113X_SbcTransfer\(\)](#) function, which allows generic read/write access.

Primary control registers (0x00 - 0x0F)

- #define [WTDC_ADDRESS](#) ((uint8_t) 0x00U << 1U)
Watchdog control register address.
- #define [MC_ADDRESS](#) ((uint8_t) 0x01U << 1U)
Mode control register address.
- #define [FSC_ADDRESS](#) ((uint8_t) 0x02U << 1U)
Fail-safe control register address.
- #define [MSBCS_ADDRESS](#) ((uint8_t) 0x03U << 1U)
Main SBC status register address.
- #define [SYSIE_ADDRESS](#) ((uint8_t) 0x04U << 1U)
System interrupt enable register address.
- #define [WTDS_ADDRESS](#) ((uint8_t) 0x05U << 1U)
Watchdog status register address.
- #define [MEM0_ADDRESS](#) ((uint8_t) 0x06U << 1U)
General purpose memory 0 address.
- #define [MEM1_ADDRESS](#) ((uint8_t) 0x07U << 1U)
General purpose memory 1 address.
- #define [MEM2_ADDRESS](#) ((uint8_t) 0x08U << 1U)
General purpose memory 2 address.
- #define [MEM3_ADDRESS](#) ((uint8_t) 0x09U << 1U)
General purpose memory 3 address.
- #define [LCKC_ADDRESS](#) ((uint8_t) 0x0AU << 1U)
Lock control register address.

Supply control registers (0x10 - 0x1F)

- #define [RC_ADDRESS](#) ((uint8_t) 0x10U << 1U)
Regulator control register address.
- #define [BMETSC_ADDRESS](#) ((uint8_t) 0x11U << 1U)
Battery monitor event trigger source control register address.
- #define [BMUTC_ADDRESS](#) ((uint8_t) 0x12U << 1U)
Battery monitor undervoltage threshold control register address.
- #define [BMOTC_ADDRESS](#) ((uint8_t) 0x13U << 1U)
Battery monitor overvoltage threshold control register address.
- #define [BMHC_ADDRESS](#) ((uint8_t) 0x14U << 1U)
Battery monitor hysteresis control register address.
- #define [VBADC1_ADDRESS](#) ((uint8_t) 0x15U << 1U)
ADC conversion results for Vbat register 1 address.
- #define [VBADC2_ADDRESS](#) ((uint8_t) 0x16U << 1U)
ADC conversion results for Vbat register 2 address.

- #define [BSADC1_ADDRESS](#) ((uint8_t) 0x17U << 1U)
ADC conversion results for Vbatsense register 1 address.
- #define [BSADC2_ADDRESS](#) ((uint8_t) 0x18U << 1U)
ADC conversion results for Vbatsense register 2 address.
- #define [SMPSC_ADDRESS](#) ((uint8_t) 0x19U << 1U)
SMPS control register address.
- #define [SMPSOVC_ADDRESS](#) ((uint8_t) 0x1AU << 1U)
SMPS out voltage control register address.
- #define [SUPVS_ADDRESS](#) ((uint8_t) 0x1BU << 1U)
Supply voltage status register address.
- #define [SUPIE_ADDRESS](#) ((uint8_t) 0x1CU << 1U)
Supply interrupt enable register address.

Transceiver control registers (0x20 - 0x2F)

- #define [CANC_ADDRESS](#) ((uint8_t) 0x20U << 1U)
CAN control register address.
- #define [LINC_ADDRESS](#) ((uint8_t) 0x21U << 1U)
LIN control register address.
- #define [TS_ADDRESS](#) ((uint8_t) 0x22U << 1U)
Transceiver status register address.
- #define [TIE_ADDRESS](#) ((uint8_t) 0x23U << 1U)
Transceiver interrupt enable register address.
- #define [DR_ADDRESS](#) ((uint8_t) 0x26U << 1U)
Data rate register address.
- #define [ID0_ADDRESS](#) ((uint8_t) 0x27U << 1U)
ID register 0 address.
- #define [ID1_ADDRESS](#) ((uint8_t) 0x28U << 1U)
ID register 1 address.
- #define [ID2_ADDRESS](#) ((uint8_t) 0x29U << 1U)
ID register 2 address.
- #define [ID3_ADDRESS](#) ((uint8_t) 0x2AU << 1U)
ID register 3 address.
- #define [IDM0_ADDRESS](#) ((uint8_t) 0x2BU << 1U)
ID mask register 0 address.
- #define [IDM1_ADDRESS](#) ((uint8_t) 0x2CU << 1U)
ID mask register 1 address.
- #define [IDM2_ADDRESS](#) ((uint8_t) 0x2DU << 1U)
ID mask register 2 address.
- #define [IDM3_ADDRESS](#) ((uint8_t) 0x2EU << 1U)
ID mask register 3 address.
- #define [FC_ADDRESS](#) ((uint8_t) 0x2FU << 1U)
Frame control register address.

HVIO control registers (0x30 - 0x4F)

- #define **HVIO1C_ADDRESS** ((uint8_t) 0x30U << 1U)
HVIO 1 control register address.
- #define **HVIO2C_ADDRESS** ((uint8_t) 0x31U << 1U)
HVIO 2 control register address.
- #define **HVIO3C_ADDRESS** ((uint8_t) 0x32U << 1U)
HVIO 3 control register address.
- #define **HVIO4C_ADDRESS** ((uint8_t) 0x33U << 1U)
HVIO 4 control register address.
- #define **B0WUPTHRC_ADDRESS** ((uint8_t) 0x34U << 1U)
Bank 0 (HVIO 1 - 4) wake-up threshold control register address.
- #define **B0WUPS_ADDRESS** ((uint8_t) 0x35U << 1U)
Bank 0 wake-up status register address.
- #define **B0DRVS_ADDRESS** ((uint8_t) 0x36U << 1U)
Bank 0 driver status register address.
- #define **B0WUPIE_ADDRESS** ((uint8_t) 0x37U << 1U)
Bank 0 wake-up interrupt enable register address.
- #define **B0FIE_ADDRESS** ((uint8_t) 0x38U << 1U)
Bank 0 fail interrupt enable register address.
- #define **B0SCDTC_ADDRESS** ((uint8_t) 0x39U << 1U)
Bank 0 short-circuit detection threshold control register address.
- #define **B0OLDTC_ADDRESS** ((uint8_t) 0x3AU << 1U)
Bank 0 open-laod detection threshold control register address.
- #define **HVIO5C_ADDRESS** ((uint8_t) 0x40U << 1U)
HVIO 5 control register address.
- #define **HVIO6C_ADDRESS** ((uint8_t) 0x41U << 1U)
HVIO 6 control register address.
- #define **HVIO7C_ADDRESS** ((uint8_t) 0x42U << 1U)
HVIO 7 control register address.
- #define **HVIO8C_ADDRESS** ((uint8_t) 0x43U << 1U)
HVIO 8 control register address.
- #define **B1WUPTHRC_ADDRESS** ((uint8_t) 0x44U << 1U)
Bank 1 (HVIO 5 - 8) wake-up threshold control register address.
- #define **B1WUPS_ADDRESS** ((uint8_t) 0x45U << 1U)
Bank 1 wake-up status register address.
- #define **B1DRVS_ADDRESS** ((uint8_t) 0x46U << 1U)
Bank 1 driver status register address.
- #define **B1WUPIE_ADDRESS** ((uint8_t) 0x47U << 1U)
Bank 1 wake-up interrupt enable register address.
- #define **B1FIE_ADDRESS** ((uint8_t) 0x48U << 1U)
Bank 1 fail interrupt enable register address.
- #define **B1SCDTC_ADDRESS** ((uint8_t) 0x49U << 1U)
Bank 1 short-circuit detection threshold control register address.
- #define **B1OLDTC_ADDRESS** ((uint8_t) 0x4AU << 1U)
Bank 1 open-laod detection threshold control register address.

Timer control registers (0x50 - 0x5F)

- #define [TIM1C_ADDRESS](#) ((uint8_t) 0x50U << 1U)
Timer 1 control register address.
- #define [TIM1DCC_ADDRESS](#) ((uint8_t) 0x51U << 1U)
Timer 1 duty cycle control register address.
- #define [TIM2C_ADDRESS](#) ((uint8_t) 0x52U << 1U)
Timer 2 control register address.
- #define [TIM2DCC_ADDRESS](#) ((uint8_t) 0x53U << 1U)
Timer 2 duty cycle control register address.
- #define [TIM3C_ADDRESS](#) ((uint8_t) 0x54U << 1U)
Timer 3 control register address.
- #define [TIM3DCC_ADDRESS](#) ((uint8_t) 0x55U << 1U)
Timer 3 duty cycle control register address.
- #define [TIM4C_ADDRESS](#) ((uint8_t) 0x56U << 1U)
Timer 4 control register address.
- #define [TIM4DCC_ADDRESS](#) ((uint8_t) 0x57U << 1U)
Timer 4 duty cycle control register address.

Interrupt status registers (0x60 - 0x6F)

- #define [GIS_ADDRESS](#) ((uint8_t) 0x60U << 1U)
Global interrupt status register address.
- #define [SYSIS_ADDRESS](#) ((uint8_t) 0x61U << 1U)
System interrupt status register address.
- #define [SUPIS_ADDRESS](#) ((uint8_t) 0x62U << 1U)
Supply interrupt status register address.
- #define [TIS_ADDRESS](#) ((uint8_t) 0x63U << 1U)
Transceiver interrupt status register address.
- #define [B0WUPIS_ADDRESS](#) ((uint8_t) 0x64U << 1U)
Bank 0 wake-up interrupt status register address.
- #define [B0FIS_ADDRESS](#) ((uint8_t) 0x65U << 1U)
Bank 0 fail interrupt status register address.
- #define [B1WUPIS_ADDRESS](#) ((uint8_t) 0x66U << 1U)
Bank 1 wake-up interrupt status register address.
- #define [B1FIS_ADDRESS](#) ((uint8_t) 0x67U << 1U)
Bank 1 fail interrupt status register address.
- #define [DM0_ADDRESS](#) ((uint8_t) 0x68U << 1U)
Data mask register 0 address.
- #define [DM1_ADDRESS](#) ((uint8_t) 0x69U << 1U)
Data mask register 1 address.
- #define [DM2_ADDRESS](#) ((uint8_t) 0x6AU << 1U)
Data mask register 2 address.
- #define [DM3_ADDRESS](#) ((uint8_t) 0x6BU << 1U)
Data mask register 3 address.
- #define [DM4_ADDRESS](#) ((uint8_t) 0x6CU << 1U)
Data mask register 4 address.
- #define [DM5_ADDRESS](#) ((uint8_t) 0x6DU << 1U)
Data mask register 5 address.
- #define [DM6_ADDRESS](#) ((uint8_t) 0x6EU << 1U)
Data mask register 6 address.
- #define [DM7_ADDRESS](#) ((uint8_t) 0x6FU << 1U)
Data mask register 7 address.

MTPNV and ID registers (0x70 - 0x7F)

- `#define MTPNVS_ADDRESS ((uint8_t) 0x70U << 1U)`
MTPNV status register address.
- `#define HVIOHSDRVC_ADDRESS ((uint8_t) 0x71U << 1U)`
HVIO high-side driver control register address.
- `#define HVIOLSDRVC_ADDRESS ((uint8_t) 0x72U << 1U)`
HVIO low-side driver control register address.
- `#define SUPC_ADDRESS ((uint8_t) 0x73U << 1U)`
Start-up control register address.
- `#define SBCCC_ADDRESS ((uint8_t) 0x74U << 1U)`
SBC configuration control register address.
- `#define MTPNVCRCC_ADDRESS ((uint8_t) 0x75U << 1U)`
MTPVN CRC control register address.
- `#define DID1_ADDRESS ((uint8_t) 0x7EU << 1U)`
Device identification register 1 address.
- `#define DID2_ADDRESS ((uint8_t) 0x7FU << 1U)`
Device identification register 2 address.

17.121.2 Macro Definition Documentation

17.121.2.1 `#define B0DRVS_ADDRESS ((uint8_t) 0x36U << 1U)`

Bank 0 driver status register address.

Definition at line 145 of file sbc_uja113x.h.

17.121.2.2 `#define B0FIE_ADDRESS ((uint8_t) 0x38U << 1U)`

Bank 0 fail interrupt enable register address.

Definition at line 147 of file sbc_uja113x.h.

17.121.2.3 `#define B0FIS_ADDRESS ((uint8_t) 0x65U << 1U)`

Bank 0 fail interrupt status register address.

Definition at line 186 of file sbc_uja113x.h.

17.121.2.4 `#define B0OLDTC_ADDRESS ((uint8_t) 0x3AU << 1U)`

Bank 0 open-laod detection threshold control register address.

Definition at line 149 of file sbc_uja113x.h.

17.121.2.5 `#define B0SCDTC_ADDRESS ((uint8_t) 0x39U << 1U)`

Bank 0 short-circuit detection threshold control register address.

Definition at line 148 of file sbc_uja113x.h.

17.121.2.6 `#define B0WUPIE_ADDRESS ((uint8_t) 0x37U << 1U)`

Bank 0 wake-up interrupt enable register address.

Definition at line 146 of file sbc_uja113x.h.

17.121.2.7 `#define B0WUPIS_ADDRESS ((uint8_t) 0x64U << 1U)`

Bank 0 wake-up interrupt status register address.

Definition at line 185 of file sbc_uja113x.h.

17.121.2.8 #define B0WUPS_ADDRESS ((uint8_t) 0x35U << 1U)

Bank 0 wake-up status register address.

Definition at line 144 of file sbc_uja113x.h.

17.121.2.9 #define B0WUPTHRC_ADDRESS ((uint8_t) 0x34U << 1U)

Bank 0 (HVIO 1 - 4) wake-up threshold control register address.

Definition at line 143 of file sbc_uja113x.h.

17.121.2.10 #define B1DRVS_ADDRESS ((uint8_t) 0x46U << 1U)

Bank 1 driver status register address.

Definition at line 156 of file sbc_uja113x.h.

17.121.2.11 #define B1FIE_ADDRESS ((uint8_t) 0x48U << 1U)

Bank 1 fail interrupt enable register address.

Definition at line 158 of file sbc_uja113x.h.

17.121.2.12 #define B1FIS_ADDRESS ((uint8_t) 0x67U << 1U)

Bank 1 fail interrupt status register address.

Definition at line 188 of file sbc_uja113x.h.

17.121.2.13 #define B1OLDTC_ADDRESS ((uint8_t) 0x4AU << 1U)

Bank 1 open-load detection threshold control register address.

Definition at line 160 of file sbc_uja113x.h.

17.121.2.14 #define B1SCDTC_ADDRESS ((uint8_t) 0x49U << 1U)

Bank 1 short-circuit detection threshold control register address.

Definition at line 159 of file sbc_uja113x.h.

17.121.2.15 #define B1WUPIE_ADDRESS ((uint8_t) 0x47U << 1U)

Bank 1 wake-up interrupt enable register address.

Definition at line 157 of file sbc_uja113x.h.

17.121.2.16 #define B1WUPIS_ADDRESS ((uint8_t) 0x66U << 1U)

Bank 1 wake-up interrupt status register address.

Definition at line 187 of file sbc_uja113x.h.

17.121.2.17 #define B1WUPS_ADDRESS ((uint8_t) 0x45U << 1U)

Bank 1 wake-up status register address.

Definition at line 155 of file sbc_uja113x.h.

17.121.2.18 #define B1WUPTHRC_ADDRESS ((uint8_t) 0x44U << 1U)

Bank 1 (HVIO 5 - 8) wake-up threshold control register address.

Definition at line 154 of file sbc_uja113x.h.

17.121.2.19 `#define BMETSC_ADDRESS ((uint8_t) 0x11U << 1U)`

Battery monitor event trigger source control register address.

Definition at line 101 of file sbc_uja113x.h.

17.121.2.20 `#define BMHC_ADDRESS ((uint8_t) 0x14U << 1U)`

Battery monitor hysteresis control register address.

Definition at line 104 of file sbc_uja113x.h.

17.121.2.21 `#define BMOTC_ADDRESS ((uint8_t) 0x13U << 1U)`

Battery monitor overvoltage threshold control register address.

Definition at line 103 of file sbc_uja113x.h.

17.121.2.22 `#define BMUTC_ADDRESS ((uint8_t) 0x12U << 1U)`

Battery monitor undervoltage threshold control register address.

Definition at line 102 of file sbc_uja113x.h.

17.121.2.23 `#define BSADC1_ADDRESS ((uint8_t) 0x17U << 1U)`

ADC conversion results for Vbatsense register 1 address.

Definition at line 107 of file sbc_uja113x.h.

17.121.2.24 `#define BSADC2_ADDRESS ((uint8_t) 0x18U << 1U)`

ADC conversion results for Vbatsense register 2 address.

Definition at line 108 of file sbc_uja113x.h.

17.121.2.25 `#define CANC_ADDRESS ((uint8_t) 0x20U << 1U)`

CAN control register address.

Definition at line 119 of file sbc_uja113x.h.

17.121.2.26 `#define DID1_ADDRESS ((uint8_t) 0x7EU << 1U)`

Device identification register 1 address.

Definition at line 209 of file sbc_uja113x.h.

17.121.2.27 `#define DID2_ADDRESS ((uint8_t) 0x7FU << 1U)`

Device identification register 2 address.

Definition at line 210 of file sbc_uja113x.h.

17.121.2.28 `#define DM0_ADDRESS ((uint8_t) 0x68U << 1U)`

Data mask register 0 address.

Definition at line 189 of file sbc_uja113x.h.

17.121.2.29 `#define DM1_ADDRESS ((uint8_t) 0x69U << 1U)`

Data mask register 1 address.

Definition at line 190 of file sbc_uja113x.h.

17.121.2.30 #define DM2_ADDRESS ((uint8_t) 0x6AU << 1U)

Data mask register 2 address.

Definition at line 191 of file sbc_uja113x.h.

17.121.2.31 #define DM3_ADDRESS ((uint8_t) 0x6BU << 1U)

Data mask register 3 address.

Definition at line 192 of file sbc_uja113x.h.

17.121.2.32 #define DM4_ADDRESS ((uint8_t) 0x6CU << 1U)

Data mask register 4 address.

Definition at line 193 of file sbc_uja113x.h.

17.121.2.33 #define DM5_ADDRESS ((uint8_t) 0x6DU << 1U)

Data mask register 5 address.

Definition at line 194 of file sbc_uja113x.h.

17.121.2.34 #define DM6_ADDRESS ((uint8_t) 0x6EU << 1U)

Data mask register 6 address.

Definition at line 195 of file sbc_uja113x.h.

17.121.2.35 #define DM7_ADDRESS ((uint8_t) 0x6FU << 1U)

Data mask register 7 address.

Definition at line 196 of file sbc_uja113x.h.

17.121.2.36 #define DR_ADDRESS ((uint8_t) 0x26U << 1U)

Data rate register address.

Definition at line 123 of file sbc_uja113x.h.

17.121.2.37 #define FC_ADDRESS ((uint8_t) 0x2FU << 1U)

Frame control register address.

Definition at line 132 of file sbc_uja113x.h.

17.121.2.38 #define FSC_ADDRESS ((uint8_t) 0x02U << 1U)

Fail-safe control register address.

Definition at line 85 of file sbc_uja113x.h.

17.121.2.39 #define GIS_ADDRESS ((uint8_t) 0x60U << 1U)

Global interrupt status register address.

Definition at line 181 of file sbc_uja113x.h.

17.121.2.40 #define HVIO1C_ADDRESS ((uint8_t) 0x30U << 1U)

HVIO 1 control register address.

Definition at line 139 of file sbc_uja113x.h.

17.121.2.41 `#define HVIO2C_ADDRESS ((uint8_t) 0x31U << 1U)`

HVIO 2 control register address.

Definition at line 140 of file sbc_uja113x.h.

17.121.2.42 `#define HVIO3C_ADDRESS ((uint8_t) 0x32U << 1U)`

HVIO 3 control register address.

Definition at line 141 of file sbc_uja113x.h.

17.121.2.43 `#define HVIO4C_ADDRESS ((uint8_t) 0x33U << 1U)`

HVIO 4 control register address.

Definition at line 142 of file sbc_uja113x.h.

17.121.2.44 `#define HVIO5C_ADDRESS ((uint8_t) 0x40U << 1U)`

HVIO 5 control register address.

Definition at line 150 of file sbc_uja113x.h.

17.121.2.45 `#define HVIO6C_ADDRESS ((uint8_t) 0x41U << 1U)`

HVIO 6 control register address.

Definition at line 151 of file sbc_uja113x.h.

17.121.2.46 `#define HVIO7C_ADDRESS ((uint8_t) 0x42U << 1U)`

HVIO 7 control register address.

Definition at line 152 of file sbc_uja113x.h.

17.121.2.47 `#define HVIO8C_ADDRESS ((uint8_t) 0x43U << 1U)`

HVIO 8 control register address.

Definition at line 153 of file sbc_uja113x.h.

17.121.2.48 `#define HVIOHSDRVC_ADDRESS ((uint8_t) 0x71U << 1U)`

HVIO high-side driver control register address.

Definition at line 204 of file sbc_uja113x.h.

17.121.2.49 `#define HVIOLSDRVC_ADDRESS ((uint8_t) 0x72U << 1U)`

HVIO low-side driver control register address.

Definition at line 205 of file sbc_uja113x.h.

17.121.2.50 `#define ID0_ADDRESS ((uint8_t) 0x27U << 1U)`

ID register 0 address.

Definition at line 124 of file sbc_uja113x.h.

17.121.2.51 `#define ID1_ADDRESS ((uint8_t) 0x28U << 1U)`

ID register 1 address.

Definition at line 125 of file sbc_uja113x.h.

17.121.2.52 `#define ID2_ADDRESS ((uint8_t) 0x29U << 1U)`

ID register 2 address.

Definition at line 126 of file sbc_uja113x.h.

17.121.2.53 `#define ID3_ADDRESS ((uint8_t) 0x2AU << 1U)`

ID register 3 address.

Definition at line 127 of file sbc_uja113x.h.

17.121.2.54 `#define IDM0_ADDRESS ((uint8_t) 0x2BU << 1U)`

ID mask register 0 address.

Definition at line 128 of file sbc_uja113x.h.

17.121.2.55 `#define IDM1_ADDRESS ((uint8_t) 0x2CU << 1U)`

ID mask register 1 address.

Definition at line 129 of file sbc_uja113x.h.

17.121.2.56 `#define IDM2_ADDRESS ((uint8_t) 0x2DU << 1U)`

ID mask register 2 address.

Definition at line 130 of file sbc_uja113x.h.

17.121.2.57 `#define IDM3_ADDRESS ((uint8_t) 0x2EU << 1U)`

ID mask register 3 address.

Definition at line 131 of file sbc_uja113x.h.

17.121.2.58 `#define LCKC_ADDRESS ((uint8_t) 0x0AU << 1U)`

Lock control register address.

Definition at line 93 of file sbc_uja113x.h.

17.121.2.59 `#define LINC_ADDRESS ((uint8_t) 0x21U << 1U)`

LIN control register address.

Definition at line 120 of file sbc_uja113x.h.

17.121.2.60 `#define MC_ADDRESS ((uint8_t) 0x01U << 1U)`

Mode control register address.

Definition at line 84 of file sbc_uja113x.h.

17.121.2.61 `#define MEM0_ADDRESS ((uint8_t) 0x06U << 1U)`

General purpose memory 0 address.

Definition at line 89 of file sbc_uja113x.h.

17.121.2.62 `#define MEM1_ADDRESS ((uint8_t) 0x07U << 1U)`

General purpose memory 1 address.

Definition at line 90 of file sbc_uja113x.h.

17.121.2.63 #define MEM2_ADDRESS ((uint8_t) 0x08U << 1U)

General purpose memory 2 address.

Definition at line 91 of file sbc_uja113x.h.

17.121.2.64 #define MEM3_ADDRESS ((uint8_t) 0x09U << 1U)

General purpose memory 3 address.

Definition at line 92 of file sbc_uja113x.h.

17.121.2.65 #define MSBCS_ADDRESS ((uint8_t) 0x03U << 1U)

Main SBC status register address.

Definition at line 86 of file sbc_uja113x.h.

17.121.2.66 #define MTPNVCRC_ADDRESS ((uint8_t) 0x75U << 1U)

MTPVN CRC control register address.

Definition at line 208 of file sbc_uja113x.h.

17.121.2.67 #define MTPNVS_ADDRESS ((uint8_t) 0x70U << 1U)

MTPNV status register address.

Definition at line 203 of file sbc_uja113x.h.

17.121.2.68 #define RC_ADDRESS ((uint8_t) 0x10U << 1U)

Regulator control register address.

Definition at line 100 of file sbc_uja113x.h.

17.121.2.69 #define SBCCC_ADDRESS ((uint8_t) 0x74U << 1U)

SBC configuration control register address.

Definition at line 207 of file sbc_uja113x.h.

17.121.2.70 #define SMPSC_ADDRESS ((uint8_t) 0x19U << 1U)

SMPS control register address.

Definition at line 109 of file sbc_uja113x.h.

17.121.2.71 #define SMPSOVC_ADDRESS ((uint8_t) 0x1AU << 1U)

SMPS out voltage control register address.

Definition at line 110 of file sbc_uja113x.h.

17.121.2.72 #define SUPC_ADDRESS ((uint8_t) 0x73U << 1U)

Start-up control register address.

Definition at line 206 of file sbc_uja113x.h.

17.121.2.73 #define SUPIE_ADDRESS ((uint8_t) 0x1CU << 1U)

Supply interrupt enable register address.

Definition at line 112 of file sbc_uja113x.h.

17.121.2.74 `#define SUPIS_ADDRESS ((uint8_t) 0x62U << 1U)`

Supply interrupt status register address.

Definition at line 183 of file sbc_uja113x.h.

17.121.2.75 `#define SUPVS_ADDRESS ((uint8_t) 0x1BU << 1U)`

Supply voltage status register address.

Definition at line 111 of file sbc_uja113x.h.

17.121.2.76 `#define SYSIE_ADDRESS ((uint8_t) 0x04U << 1U)`

System interrupt enable register address.

Definition at line 87 of file sbc_uja113x.h.

17.121.2.77 `#define SYSIS_ADDRESS ((uint8_t) 0x61U << 1U)`

System interrupt status register address.

Definition at line 182 of file sbc_uja113x.h.

17.121.2.78 `#define TIE_ADDRESS ((uint8_t) 0x23U << 1U)`

Transceiver interrupt enable register address.

Definition at line 122 of file sbc_uja113x.h.

17.121.2.79 `#define TIM1C_ADDRESS ((uint8_t) 0x50U << 1U)`

Timer 1 control register address.

Definition at line 167 of file sbc_uja113x.h.

17.121.2.80 `#define TIM1DCC_ADDRESS ((uint8_t) 0x51U << 1U)`

Timer 1 duty cycle control register address.

Definition at line 168 of file sbc_uja113x.h.

17.121.2.81 `#define TIM2C_ADDRESS ((uint8_t) 0x52U << 1U)`

Timer 2 control register address.

Definition at line 169 of file sbc_uja113x.h.

17.121.2.82 `#define TIM2DCC_ADDRESS ((uint8_t) 0x53U << 1U)`

Timer 2 duty cycle control register address.

Definition at line 170 of file sbc_uja113x.h.

17.121.2.83 `#define TIM3C_ADDRESS ((uint8_t) 0x54U << 1U)`

Timer 3 control register address.

Definition at line 171 of file sbc_uja113x.h.

17.121.2.84 `#define TIM3DCC_ADDRESS ((uint8_t) 0x55U << 1U)`

Timer 3 duty cycle control register address.

Definition at line 172 of file sbc_uja113x.h.

17.121.2.85 `#define TIM4C_ADDRESS ((uint8_t) 0x56U << 1U)`

Timer 4 control register address.

Definition at line 173 of file sbc_uja113x.h.

17.121.2.86 `#define TIM4DCC_ADDRESS ((uint8_t) 0x57U << 1U)`

Timer 4 duty cycle control register address.

Definition at line 174 of file sbc_uja113x.h.

17.121.2.87 `#define TIS_ADDRESS ((uint8_t) 0x63U << 1U)`

Transceiver interrupt status register address.

Definition at line 184 of file sbc_uja113x.h.

17.121.2.88 `#define TS_ADDRESS ((uint8_t) 0x22U << 1U)`

Transceiver status register address.

Definition at line 121 of file sbc_uja113x.h.

17.121.2.89 `#define VBADC1_ADDRESS ((uint8_t) 0x15U << 1U)`

ADC conversion results for Vbat register 1 address.

Definition at line 105 of file sbc_uja113x.h.

17.121.2.90 `#define VBADC2_ADDRESS ((uint8_t) 0x16U << 1U)`

ADC conversion results for Vbat register 2 address.

Definition at line 106 of file sbc_uja113x.h.

17.121.2.91 `#define WTDC_ADDRESS ((uint8_t) 0x00U << 1U)`

Watchdog control register address.

Definition at line 83 of file sbc_uja113x.h.

17.121.2.92 `#define WTDS_ADDRESS ((uint8_t) 0x05U << 1U)`

Watchdog status register address.

Definition at line 88 of file sbc_uja113x.h.

17.122 S32K148 SoC Header file

17.122.1 Detailed Description

This module covers the S32K148 SoC Header file.

Modules

- [Backward Compatibility Symbols for S32K148](#)
This module covers backward compatibility symbols.
- [Interrupt vector numbers for S32K148](#)
This module covers interrupt number allocation.
- [Peripheral access layer for S32K148](#)
This module covers all memory mapped register available on SoC.

17.123 S32K148 System Files

This module covers the SoC support file for S32K148.

SystemInit method is called automatically from start-up code to do the minimum setup of the SoC. It disables the watchdog, enables FPU and the power mode protection if the corresponding feature macro is enabled.

SystemCoreClockUpdate method can be used at any time to update SystemCoreClock. It evaluates the clock register settings and calculates the current core clock.

SystemSoftwareReset method initiates a system reset.

17.124 SAI Driver

17.124.1 Detailed Description

This module covers the functionality of the Synchronous Audio Interface (SAI) peripheral driver.

The SAI driver implements communication using the SAI module in the S32K148 processor.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\sai\sai_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc\  
${S32SDK_PATH}\platform\drivers\src\sai\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager OS Interface \(OSIF\)](#) [Interrupt Manager \(Interrupt\)](#) [Enhanced Direct Memory Access \(eDMA\)](#)

Features

- Transmitter with independent bit clock and frame sync, or sync with receiver
- Receiver with independent bit clock and frame sync, or sync with transmitter
- Maximum frame size of 16 words
- Word size of between 8-bits and 32-bits
- Word size configured separately for first word and remaining words in frame
- Mux channels into one dataline, or mux data lines into one memory block

How to integrate SAI in your application

In order to use the SAI driver it must be first initialized in either transmit or receive mode, using functions [SAI_DRV_TxInit\(\)](#) or [SAI_DRV_RxInit\(\)](#). Once initialized, it cannot be initialized again for the same SAI module instance until it is de-initialized, using [SAI_DRV_TxDeinit\(\)](#) or [SAI_DRV_RxDeinit\(\)](#). Different SAI module instances can function independently of each other.

In each mode (transmit/receive) are available two types of transfers: blocking and non-blocking. The functions which initiate blocking transfers will configure the time out for transmission. If time expires [SAI_DRV_SendBlocking\(\)](#)/[SAI_DRV_ReceiveBlocking\(\)](#) will return error and the transmission will be aborted.

Important Notes

- If transmitter is initialized with [SAI_SYNC_WITH_OTHER](#) option, transmitter must be initialized first and receiver must use [SAI_ASYNC](#) mode
- If receiver is initialized with [SAI_SYNC_WITH_OTHER](#) option, receiver must be initialized first and transmitter must use [SAI_ASYNC](#) mode

- DMA module has to be initialized prior to usage in DMA mode; also, DMA channels need to be allocated by the application (the driver only takes care of configuring the DMA channels received in the configuration structure)
- There is a difference in ChannelEnable field usage between interrupt and dma mode:
In interrupt mode, if mux line is enabled then user must turn on only one bit in ChannelEnable, which will be the data line to output data. Number of data buffers to be muxed is specified in ChannelCount field.
In DMA mode, if mux line is enabled then user must turn on number of bits equal to number of data buffers to be muxed. The data lines corresponding to these bits will output the same as each other.
Also in DMA mode, if a mux mode is selected, ChannelEnable must be turned on from bit 0, and immediately above (for example turning on bit 0 and bit 2 is not a correct configuration).
- When multiple SAI channel is enabled, number of DMA channels must be equal number of SAI channels. And in DMA component:
Channel arbitration must be set to "Fixed priority".
The first DMA channel must have the lowest DMA channel number and request source must be set properly (for example SAI0_TX). Other DMA channels must have request field set to "No request".

Example code

```
/* sai0 configuration structure */
sai_user_config_t sai0_InitConfig0;

/* Driver state structure */
sai_state_t SAI0TxState;

/* Fill configuration structure with I2S settings */
SAI_DRV_GetDefaultConfig(&sai0_InitConfig0);

/* Provide two data buffer for left and right channel */
uint16_t* sendData[2U] = {LeftData, RightData};

/* Initialize transmitter for SAI0 */
SAI_DRV_TxInit(0U, &sai0_InitConfig0, &SAI0TxState);

/* Send blocking, timeout is 10ms */
status_t ret = SAI_DRV_SendBlocking(0U, (uint8_t**) sendData, sendBufferSize, 10U);
```

Data Structures

- struct [sai_xfer_state_t](#)
Transmit or receive state. [More...](#)
- struct [sai_state_t](#)
Structure for internal use. This structure is used by the driver for its internal logic. It must be provided by the application through the initialize functions, then it cannot be freed until the driver is de-initialized using Deinit functions. The application should make no assumptions about the content of this structure. [More...](#)
- struct [sai_user_config_t](#)
User config structure.
Note: entries in this structure are affected by ::FEATURE_SAI_HAS_CHMOD, which is device dependent and controlled from feature header file of the used device. [More...](#)

Macros

- #define [SAI_CHANNEL_0](#) 0x1
- #define [SAI_CHANNEL_1](#) 0x2
- #define [SAI_CHANNEL_2](#) 0x4
- #define [SAI_CHANNEL_3](#) 0x8

Typedefs

- typedef void(* [sai_transfer_callback_t](#)) ([sai_report_type_t](#) event, void *userData)
Sai callback function type for nonblock transfer, also called to report events ([sai_report_type_t](#)).

Enumerations

- enum `sai_report_type_t` {
`SAI_RX_COMPLETE` = 0x00U, `SAI_TX_COMPLETE` = 0x01U, `SAI_ERROR` = 0x03U, `SAI_FRAME_STATUS_ERROR` = 0x05U,
`SAI_RUN_ERROR` = 0x06U, `SAI_SYNC_ERROR` = 0x07U }
Report to enable.
- enum `sai_transfer_type_t` { `SAI_INTERRUPT` = 0U, `SAI_DMA` }
Transfer type.
- enum `sai_mux_mode_t` { `SAI_MUX_DISABLED` = 0U, `SAI_MUX_LINE` = 1U, `SAI_MUX_MEM` = 2U }
Data mux line or mux memory.
- enum `sai_sync_mode_t` { `SAI_ASYNC` = 0U, `SAI_SYNC_WITH_OTHER` = 1U }
SAI run in sync or async mode.
Note: entries in this enum are affected by `::FEATURE_SAI_SYNC_WITH_OTHER_INST`, which is device dependent and controlled from feature header file of the used device.
- enum `sai_master_clk_source_t`
Select master clock.
Note: entries in this enum are affected by `::FEATURE_SAI_MSEL_BUS_CLK`, `::FEATURE_SAI_MSEL_MCLK_PIN`, `::FEATURE_SAI_MSEL_FCD`, `::FEATURE_SAI_MSEL_SOSC_CLK`, `::FEATURE_SAI_MSEL_OTHER_MCLK_PIN`, which is device dependent and controlled from feature header file of the used device.

SAI Driver

- void `SAI_DRV_SetMaster` (uint32_t instNum, bool tx)
Enable tx/rx and disable rx/tx to change to tx/rx transfer, only use this when driver is used in half duplex way.
- void `SAI_DRV_TxInit` (uint32_t instNum, const `sai_user_config_t` *saiUserConfig, `sai_state_t` *StateAlloc)
Initialize the transmitter of driver.
- void `SAI_DRV_RxInit` (uint32_t instNum, const `sai_user_config_t` *saiUserConfig, `sai_state_t` *StateAlloc)
Initialize the receiver of driver.
- void `SAI_DRV_TxDeinit` (uint32_t instNum)
De-initialize transmitter.
- void `SAI_DRV_RxDeinit` (uint32_t instNum)
De-initialize receiver.
- uint32_t `SAI_DRV_TxGetBitClockFreq` (uint32_t instNum)
Return true bit clock frequency of transmitter.
- uint32_t `SAI_DRV_RxGetBitClockFreq` (uint32_t instNum)
Return true bit clock frequency of receiver.
- uint32_t `SAI_DRV_TxGetBitClockDiv` (uint32_t instNum)
Return true bit clock divisor of transmitter.
- uint32_t `SAI_DRV_RxGetBitClockDiv` (uint32_t instNum)
Return true bit clock divisor of receiver.
- void `SAI_DRV_TxSetNextMaskWords` (uint32_t instNum, uint16_t Words)
Set masked word index of subsequent frames for transmitter.
- void `SAI_DRV_RxSetNextMaskWords` (uint32_t instNum, uint16_t Words)
Set masked word index of subsequent frames for receiver.
- status_t `SAI_DRV_SendBlocking` (uint32_t instNum, const uint8_t *data[], uint32_t count, uint32_t timeout)
Send a block of data, return when transfer complete.
- void `SAI_DRV_Send` (uint32_t instNum, const uint8_t *data[], uint32_t count)
Send a block of data, return immediately.
- status_t `SAI_DRV_GetSendingStatus` (uint32_t instNum, uint32_t *countRemain)
Get status of a non-blocking transfer.
- void `SAI_DRV_AbortSending` (uint32_t instNum)

Abort an ongoing transfer.

- status_t [SAI_DRV_ReceiveBlocking](#) (uint32_t instNum, uint8_t *data[], uint32_t count, uint32_t timeout)

Receive a block of data, return when transfer complete.

- void [SAI_DRV_Receive](#) (uint32_t instNum, uint8_t *data[], uint32_t count)

Receive a block of data, return immediately.

- status_t [SAI_DRV_GetReceivingStatus](#) (uint32_t instNum, uint32_t *countRemain)

Get status of a non-blocking transfer.

- void [SAI_DRV_AbortReceiving](#) (uint32_t instNum)

Abort an ongoing transfer.

- void [SAI_DRV_GetDefaultConfig](#) (sai_user_config_t *uc)

Get default config structure for I2S standard. Init config structure for I2S interface: Interrupt mode, internal generated bit clock, 44.1 kHz sample rate, 16 bit word, 2 channel, data line 0,.

17.124.2 Data Structure Documentation

17.124.2.1 struct sai_xfer_state_t

Transmit or receive state.

Definition at line 49 of file sai_driver.h.

17.124.2.2 struct sai_state_t

Structure for internal use. This structure is used by the driver for its internal logic. It must be provided by the application through the initialize functions, then it cannot be freed until the driver is de-initialized using Deinit functions. The application should make no assumptions about the content of this structure.

Definition at line 104 of file sai_driver.h.

17.124.2.3 struct sai_user_config_t

User config structure.

Note: entries in this structure are affected by ::FEATURE_SAI_HAS_CHMOD, which is device dependent and controlled from feature header file of the used device.

Implements : sai_user_config_t_Class

Definition at line 202 of file sai_driver.h.

Data Fields

- [sai_sync_mode_t](#) SyncMode
- [sai_master_clk_source_t](#) MasterClkSrc
- bool [BitClkNegPolar](#)
- bool [BitClkInternal](#)
- uint16_t [BitClkDiv](#)
- uint8_t [ChannelEnable](#)
- uint8_t [FrameSize](#)
- uint8_t [SyncWidth](#)
- bool [MsbFirst](#)
- bool [SyncEarly](#)
- bool [SyncNegPolar](#)
- bool [SyncInternal](#)
- uint8_t [Word0Width](#)
- uint8_t [WordNWidth](#)
- uint8_t [FirstBitIndex](#)
- uint32_t [BitClkFreq](#)
- bool [RunErrorReport](#)

- bool [SyncErrorReport](#)
- bool [FrameStartReport](#)
- [sai_mux_mode_t](#) MuxMode
- [sai_transfer_type_t](#) TransferType
- [uint8_t](#) DmaChannel [SAI_MAX_CHANNEL_COUNT]
- [uint8_t](#) ElementSize
- [uint8_t](#) ChannelCount
- [sai_transfer_callback_t](#) callback
- void * [callbackParam](#)

Field Documentation

17.124.2.3.1 [uint16_t](#) BitClkDiv

If bit clock is generated internally, it is divided from master clock by this. User need to init this if master clock is external. Real value is derived by: $\text{floor}(\text{BitClkDiv} / 2) * 2$ Value range is from 2 to 512. If out of range value is assigned, maximum or minimum value is used

Definition at line 208 of file [sai_driver.h](#).

17.124.2.3.2 [uint32_t](#) BitClkFreq

Desired bit clock frequency in hertz, only for internally generated master clock and bit clock. Real divisor is derived by: $\text{floor}(\text{floor}(\text{MasterClockFreq} / \text{BitClkFreq}) / 2) * 2$, value range is from 2 to 512. If out of range value is assigned, maximum or minimum value is used. Real closest BitClockFreq is derived by: $\text{MasterClockFreq} / \text{real_divisor}$

Definition at line 226 of file [sai_driver.h](#).

17.124.2.3.3 [bool](#) BitClkInternal

True if bit clock is generated internally.

Definition at line 207 of file [sai_driver.h](#).

17.124.2.3.4 [bool](#) BitClkNegPolar

True if bit clock is negative polar (active low with drive outputs on falling edge and sample inputs on rising edge), false otherwise.

Definition at line 206 of file [sai_driver.h](#).

17.124.2.3.5 [sai_transfer_callback_t](#) callback

User callback function, called when transfer complete or selected events occurred.

Definition at line 239 of file [sai_driver.h](#).

17.124.2.3.6 [void*](#) callbackParam

User callback param

Definition at line 240 of file [sai_driver.h](#).

17.124.2.3.7 [uint8_t](#) ChannelCount

Number of channels to enable, only used when both line mux mode and interrupt mode is selected.

Definition at line 238 of file [sai_driver.h](#).

17.124.2.3.8 [uint8_t](#) ChannelEnable

Turn on each bit to enable each channel. 4 bit for 4 channels.

Definition at line 212 of file [sai_driver.h](#).

17.124.2.3.9 uint8_t DmaChannel[SAI_MAX_CHANNEL_COUNT]

DMA channels to be used.

Definition at line 236 of file sai_driver.h.

17.124.2.3.10 uint8_t ElementSize

Size in bytes of each read/write from/to buffer.

Definition at line 237 of file sai_driver.h.

17.124.2.3.11 uint8_t FirstBitIndex

Index from LSB of first bit to be transmitted/received, valid range from 0-31.

Definition at line 224 of file sai_driver.h.

17.124.2.3.12 uint8_t FrameSize

Frame size in number of words. When in mux line mode, the number of unmasked word in a frame must be divisible by number of channels

Definition at line 213 of file sai_driver.h.

17.124.2.3.13 bool FrameStartReport

Enable frame start report.

Definition at line 233 of file sai_driver.h.

17.124.2.3.14 sai_master_clk_source_t MasterClkSrc

Select master clock source.

Definition at line 205 of file sai_driver.h.

17.124.2.3.15 bool MsbFirst

True if data is MSB first, false if LSB first.

Definition at line 218 of file sai_driver.h.

17.124.2.3.16 sai_mux_mode_t MuxMode

Enable line mux, memory mux or mux is disabled.

Definition at line 234 of file sai_driver.h.

17.124.2.3.17 bool RunErrorReport

Underrun/overflow error report.

Definition at line 231 of file sai_driver.h.

17.124.2.3.18 bool SyncEarly

True if frame sync is one bit clock early.

Definition at line 219 of file sai_driver.h.

17.124.2.3.19 bool SyncErrorReport

Enable sync error report.

Definition at line 232 of file sai_driver.h.

17.124.2.3.20 `bool SyncInternal`

True if frame sync is generated internally

Definition at line 221 of file `sai_driver.h`.

17.124.2.3.21 `sai_sync_mode_t SyncMode`

Sync mode.

Definition at line 204 of file `sai_driver.h`.

17.124.2.3.22 `bool SyncNegPolar`

True if frame sync is negative polar (active low), false otherwise.

Definition at line 220 of file `sai_driver.h`.

17.124.2.3.23 `uint8_t SyncWidth`

Active sync width in number of bit clocks (must not longer than first word width).

Definition at line 214 of file `sai_driver.h`.

17.124.2.3.24 `sai_transfer_type_t TransferType`

Transfer using dma or interrupt.

Definition at line 235 of file `sai_driver.h`.

17.124.2.3.25 `uint8_t Word0Width`

First word width in number of bit clocks.

Definition at line 222 of file `sai_driver.h`.

17.124.2.3.26 `uint8_t WordNWidth`

Other words width in number of bit clocks.

Definition at line 223 of file `sai_driver.h`.

17.124.3 Macro Definition Documentation

17.124.3.1 `#define SAI_CHANNEL_0 0x1`

Definition at line 42 of file `sai_driver.h`.

17.124.3.2 `#define SAI_CHANNEL_1 0x2`

Definition at line 43 of file `sai_driver.h`.

17.124.3.3 `#define SAI_CHANNEL_2 0x4`

Definition at line 44 of file `sai_driver.h`.

17.124.3.4 `#define SAI_CHANNEL_3 0x8`

Definition at line 45 of file `sai_driver.h`.

17.124.4 Typedef Documentation

17.124.4.1 `typedef void(* sai_transfer_callback_t)(sai_report_type_t event, void *userData)`

Sai callback function type for nonblock transfer, also called to report events (sai_report_type_t).

Definition at line 75 of file sai_driver.h.

17.124.5 Enumeration Type Documentation

17.124.5.1 `enum sai_master_clk_source_t`

Select master clock.

Note: entries in this enum are affected by ::FEATURE_SAI_MSEL_BUS_CLK, ::FEATURE_SAI_MSEL_MCLK_↔PIN, ::FEATURE_SAI_MSEL_FCD, ::FEATURE_SAI_MSEL_SOSC_CLK, ::FEATURE_SAI_MSEL_OTHER_M↔CLK_PIN, which is device dependent and controlled from feature header file of the used device.

Implements : sai_master_clk_source_t_Class

Definition at line 150 of file sai_driver.h.

17.124.5.2 `enum sai_mux_mode_t`

Data mux line or mux memory.

Implements : sai_mux_mode_t_Class

Enumerator

SAI_MUX_DISABLED Each data line is a channel, uses a separate memory block

SAI_MUX_LINE Only one data line (data line 0 for DMA mode) is used. Words on data line is alternated between channels, each channel data is a separate memory block

SAI_MUX_MEM Words in memory block is alternated between channels, each channel data is on a separate data line.

Definition at line 91 of file sai_driver.h.

17.124.5.3 `enum sai_report_type_t`

Report to enable.

Implements : sai_report_type_t_Class

Enumerator

SAI_RX_COMPLETE Rx transfer complete, user can start another transfer

SAI_TX_COMPLETE Tx transfer complete, user can start another transfer

SAI_ERROR DMA error while transfer

SAI_FRAME_START Indicate a frame start

SAI_RUN_ERROR Overrun/underrun error. This event is useful for tx when user want to know whether all data in tx fifo has been pushed out to line and tx deinit can be called, since tx complete event only indicates all data from buffer has been pushed to hardware fifo

SAI_SYNC_ERROR Frame sync error

Definition at line 61 of file sai_driver.h.

17.124.5.4 `enum sai_sync_mode_t`

SAI run in sync or async mode.

Note: entries in this enum are affected by ::FEATURE_SAI_SYNC_WITH_OTHER_INST, which is device dependent and controlled from feature header file of the used device.

Implements : sai_sync_mode_t_Class

Enumerator

SAI_ASYNC Independent clock

SAI_SYNC_WITH_OTHER Bit clock and frame sync signal is taken from transmitter/receiver

Definition at line 129 of file sai_driver.h.

17.124.5.5 enum sai_transfer_type_t

Transfer type.

Implements : sai_transfer_type_t_Class

Enumerator

SAI_INTERRUPT Transfer type is interrupt

SAI_DMA Transfer type is DMA

Definition at line 81 of file sai_driver.h.

17.124.6 Function Documentation

17.124.6.1 void SAI_DRV_AbortReceiving (uint32_t instNum)

Abort an ongoing transfer.

Parameters

in	instNum	Peripheral instance number
----	---------	----------------------------

17.124.6.2 void SAI_DRV_AbortSending (uint32_t instNum)

Abort an ongoing transfer.

Parameters

in	instNum	Peripheral instance number
----	---------	----------------------------

17.124.6.3 void SAI_DRV_GetDefaultConfig (sai_user_config_t * uc)

Get default config structure for I2S standard. Init config structure for I2S interface: Interrupt mode, internal generated bit clock, 44.1 kHz sample rate, 16 bit word, 2 channel, data line 0,.

Parameters

out	uc	Pointer to config structure to fill in
-----	----	--

17.124.6.4 status_t SAI_DRV_GetReceivingStatus (uint32_t instNum, uint32_t * countRemain)

Get status of a non-blocking transfer.

Parameters

in	instNum	Peripheral instance number
out	countRemain	Number of words remain for each channel. This parameter can be NULL

Returns

Status of the transfer, can be success, aborted, timeout or busy.

17.124.6.5 status_t SAI_DRV_GetSendingStatus (uint32_t instNum, uint32_t * countRemain)

Get status of a non-blocking transfer.

Parameters

in	<i>instNum</i>	Peripheral instance number
out	<i>countRemain</i>	Number of words remain for each channel. This parameter can be NULL

Returns

Status of the transfer, can be success, aborted, timeout or busy. Note that for tx, success status imply that all data has been pushed to hardware fifo and another transfer can be started.

17.124.6.6 void SAI_DRV_Receive (uint32_t *instNum*, uint8_t * *data*[], uint32_t *count*)

Receive a block of data, return immediately.

When transfer completed, the callback function will be executed. User should use this callback function to immediately start another transfer to avoid data overrun error.

Parameters

in	<i>instNum</i>	Peripheral instance number
out	<i>data</i>	Array of pointer to each data block to transfer, each data block corresponds to an enabled channels If mux memory is selected, only first data block is used
in	<i>count</i>	Number of words to transfer for each channel. In DMA mode, count number upper limit is limited by DMA BITER/CITER register length.

17.124.6.7 status_t SAI_DRV_ReceiveBlocking (uint32_t *instNum*, uint8_t * *data*[], uint32_t *count*, uint32_t *timeout*)

Receive a block of data, return when transfer complete.

Should be called immediately after a transfer complete to avoid data overrun error.

Parameters

in	<i>instNum</i>	Peripheral instance number
out	<i>data</i>	Array of pointer to each data block to transfer, each data block corresponds to an enabled channels If mux memory is selected, only first data block is used
in	<i>count</i>	Number of words to transfer for each channel. In DMA mode, count number upper limit is limited by DMA BITER/CITER register length.
in	<i>timeout</i>	Timeout to return when transfer take too long.

Returns

Success, error or timeout status.

17.124.6.8 void SAI_DRV_RxDeinit (uint32_t *instNum*)

De-initialize receiver.

This function de-initializes driver. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

in	<i>instNum</i>	Peripheral instance number
----	----------------	----------------------------

17.124.6.9 uint32_t SAI_DRV_RxGetBitClockDiv (uint32_t *instNum*)

Return true bit clock divisor of receiver.

Only used when bit clock is internal and master clock is external

Parameters

in	<i>instNum</i>	Peripheral instance number
----	----------------	----------------------------

Returns

Divisor factor

17.124.6.10 `uint32_t SAI_DRV_RxGetBitClockFreq (uint32_t instNum)`

Return true bit clock frequency of receiver.

Only used when master clock and bit clock is internal

Parameters

in	<i>instNum</i>	Peripheral instance number
----	----------------	----------------------------

Returns

Frequency in hertz

17.124.6.11 `void SAI_DRV_RxInit (uint32_t instNum, const sai_user_config_t * saiUserConfig, sai_state_t * StateAlloc)`

Initialize the receiver of driver.

Parameters

in	<i>instNum</i>	Peripheral instance number
in	<i>saiUserConfig</i>	Pointer to the user configuration structure. The function reads configuration data from this structure and initializes the driver accordingly. The application may free this structure after the function returns.
in	<i>StateAlloc</i>	Pointer to the state structure. The driver uses this memory area for its internal logic. The application must make no assumptions about the content of this structure, and must not free this memory until the driver is de-initialized.

17.124.6.12 `void SAI_DRV_RxSetNextMaskWords (uint32_t instNum, uint16_t Words)`

Set masked word index of subsequent frames for receiver.

Set masked words of subsequent frames. Each bit is a masked word. Should be called in frame start event callback or in four bit clock cycles after Rx init.

Parameters

in	<i>instNum</i>	Peripheral instance number
in	<i>WordIndex</i>	Word index to mask

17.124.6.13 `void SAI_DRV_Send (uint32_t instNum, const uint8_t * data[], uint32_t count)`

Send a block of data, return immediately.

When transfer completed, the callback function will be executed. User should use this callback function to immediately start an other transfer to avoid data underrun error.

Parameters

in	<i>instNum</i>	Peripheral instance number
in	<i>data</i>	Array of pointer to each data block to transfer, each data block corresponds to an enabled channels If mux memory is selected, only first data block is used
in	<i>count</i>	Number of words to transfer for each channel. In DMA mode, count number upper limit is limited by DMA BITER/CITER register length.

17.124.6.14 `status_t SAI_DRV_SendBlocking (uint32_t instNum, const uint8_t * data[], uint32_t count, uint32_t timeout)`

Send a block of data, return when transfer complete.

Should be called immediately after a transfer complete to avoid data underrun error.

Parameters

in	<i>instNum</i>	Peripheral instance number
in	<i>data</i>	Array of pointer to each data block to transfer, each data block corresponds to an enabled channels If mux memory is selected, only first data block is used
in	<i>count</i>	Number of words to transfer for each channel. In DMA mode, count number upper limit is limited by DMA BITER/CITER register length.
in	<i>timeout</i>	Timeout to return when transfer take too long.

Returns

Success, error or timeout status.

17.124.6.15 `void SAI_DRV_SetMaster (uint32_t instNum, bool tx)`

Enable tx/rx and disable rx/tx to change to tx/rx transfer, only use this when driver is used in half duplex way.

In master mode, if user want to alternate between tx and rx operation (half duplex), both tx and rx need to be initialized as ASYNC, and this function must be called when:

- Before calling the first tx/rx transfer
- After a tx/rx transfer end and before start another rx/tx transfer.

Parameters

in	<i>instNum</i>	Peripheral instance number
in	<i>tx</i>	True if next operation is tx, false otherwise

17.124.6.16 `void SAI_DRV_TxDeinit (uint32_t instNum)`

De-initialize transmitter.

This function de-initializes driver. The driver can't be used again until reinitialized. The context structure is no longer needed by the driver and can be freed after calling this function.

Parameters

in	<i>instNum</i>	Peripheral instance number
----	----------------	----------------------------

17.124.6.17 `uint32_t SAI_DRV_TxGetBitClockDiv (uint32_t instNum)`

Return true bit clock divisor of transmitter.

Only used when bit clock is internal and master clock is external

Parameters

<i>in</i>	<i>instNum</i>	Peripheral instance number
-----------	----------------	----------------------------

Returns

Frequency in hertz

17.124.6.18 `uint32_t SAI_DRV_TxGetBitClockFreq (uint32_t instNum)`

Return true bit clock frequency of transmitter.

Only used when master clock and bit clock is internal

Parameters

<i>in</i>	<i>instNum</i>	Peripheral instance number
-----------	----------------	----------------------------

17.124.6.19 `void SAI_DRV_TxInit (uint32_t instNum, const sai_user_config_t * saiUserConfig, sai_state_t * StateAlloc)`

Initialize the transmitter of driver.

Parameters

<i>in</i>	<i>instNum</i>	Peripheral instance number
<i>in</i>	<i>saiUserConfig</i>	Pointer to the user configuration structure. The function reads configuration data from this structure and initializes the driver accordingly. The application may free this structure after the function returns.
<i>in</i>	<i>StateAlloc</i>	Pointer to the state structure. The driver uses this memory area for its internal logic. The application must make no assumptions about the content of this structure, and must not free this memory until the driver is de-initialized.

17.124.6.20 `void SAI_DRV_TxSetNextMaskWords (uint32_t instNum, uint16_t Words)`

Set masked word index of subsequent frames for transmitter.

Each bit is a masked word. Should be called in frame start event callback or in four bit clock cycles after Tx init.

Parameters

<i>in</i>	<i>instNum</i>	Peripheral instance number
<i>in</i>	<i>WordIndex</i>	Word index to mask

Returns

Divisor factor

17.125 SBC FS45 Driver

17.125.1 Detailed Description

SBC FS45 driver.

Data Structures

- struct [fs45_rx_data_t](#)
Structure representing received data frame. [More...](#)
- struct [fs45_reg_config_value_t](#)
Structure representing configuration value of one register. [More...](#)
- struct [fs45_vreg_reg_t](#)
Initialization structure with INIT_VREG content. [More...](#)
- struct [fs45_wu1_reg_t](#)
Initialization structure with INIT_WU1 content. [More...](#)
- struct [fs45_wu2_reg_t](#)
Initialization structure with INIT_WU2 content. [More...](#)
- struct [fs45_int_reg_t](#)
Initialization structure with INIT_INT content. [More...](#)
- struct [fs45_inh_int_reg_t](#)
Initialization structure with INIT_INH_INT content. [More...](#)
- struct [fs45_fs1b_timing_reg_t](#)
Initialization structure with INIT_FS1B_TIMING content. [More...](#)
- struct [fs45_supervisor_reg_t](#)
Initialization structure with INIT_SUPERVISOR content. [More...](#)
- struct [fs45_fault_reg_t](#)
Initialization structure with INIT_FAULT content. [More...](#)
- struct [fs45_fssm_reg_t](#)
Initialization structure with INIT_FSSM content. [More...](#)
- struct [fs45_sf_impact_reg_t](#)
Initialization structure with INIT_SF_IMPACT content. [More...](#)
- struct [fs45_wd_cnt_reg_t](#)
Initialization structure with INIT_WD_CNT content. [More...](#)
- struct [fs45_vcore_ovuv_impact_reg_t](#)
Initialization structure with INIT_VCORE_OVUV_IMPACT content. [More...](#)
- struct [fs45_vcca_ovuv_impact_reg_t](#)
Initialization structure with INIT_VCCA_OVUV_IMPACT content. [More...](#)
- struct [fs45_vaux_ovuv_impact_reg_t](#)
Initialization structure with INIT_VAUX_OVUV_IMPACT content. [More...](#)
- struct [fs45_drv_config_t](#)
Structure for FS45 driver configuration. [More...](#)

Enumerations

- enum [fs45_fsxb_release_t](#) { [fs45ReleaseFs0b](#), [fs45ReleaseFs1b](#), [fs45ReleaseFs0bFs1b](#) }
FSxb pin release options.
- enum [fs45_prev_mode_t](#) { [fs45PrevModePOR](#), [fs45PrevModeDFS](#), [fs45PrevModeLPOFF](#) }
Previous SBC state.
- enum [fs45_current_mode_t](#) { [fs45ModeUnknown](#), [fs45ModeInit](#), [fs45ModeNormal](#) }
Actual SBC state.

- enum `fs45_reg_mode_t` {
`fs45VCan`, `fs45Aux`, `fs45Vcca`, `fs45Vcore`,
`fs45Vkam` }
Voltage outputs. Can be used with function `FS45_SetRegulatorState()`.
- enum `fs45_amux_selection_t` {
`fs45AmuxVref` = `FS45_RW_M_AMUX_VREF`, `fs45AmuxVsnsWide` = `FS45_RW_M_AMUX_VSNS_W`, `fs45AmuxIO_0Wide` = `FS45_RW_M_AMUX_IO_0_W`, `fs45AmuxIO_5Wide` = `FS45_RW_M_AMUX_IO_5_W`,
`fs45AmuxVsnsTight` = `FS45_RW_M_AMUX_VSNS_T`, `fs45AmuxIO_0Tight` = `FS45_RW_M_AMUX_IO_0_T`,
`fs45AmuxIO_5TightDivVkam` = `FS45_RW_M_AMUX_IO_5_T`, `fs45AmuxDieTempSensor` = `FS45_RW_M_AMUX_TEMP_SENSOR` }
AMUX channel selection. Can be used with function `FS45_SwitchAMUXchannel()`.
- enum `fs45_can_mode_t` { `fs45CanModeSleepNoWakeup` = `FS45_RW_M_CAN_MODE_SLN_WU`, `fs45CanModeListenOnly` = `FS45_RW_M_CAN_MODE_LISTEN_ONLY`, `fs45CanModeSleepWakeup` = `FS45_RW_M_CAN_MODE_SL_WU`, `fs45CanModeNormal` = `FS45_RW_M_CAN_MODE_NORMAL` }
CAN mode. Can be used with function `FS45_CAN_SetMode()`.
- enum `fs45_ldt_function_t` {
`fs45LdtFunc1` = `FS45_RW_M_F2_F0_FUNCTION1`, `fs45LdtFunc2` = `FS45_RW_M_F2_F0_FUNCTION2`,
`fs45LdtFunc3` = `FS45_RW_M_F2_F0_FUNCTION3`, `fs45LdtFunc4` = `FS45_RW_M_F2_F0_FUNCTION4`,
`fs45LdtFunc5` = `FS45_RW_M_F2_F0_FUNCTION5` }
LDT operating function. Can be used with function `FS45_LDT_SetTimerOperation()`.
- enum `fs45_ldt_mode_t` { `fs45LdtModeCalibration` = `FS45_RW_M_MODE_CALIBRATION`, `fs45LdtModeNormal` = `FS45_RW_M_MODE_NORMAL` }
LDT mode. Can be used with function `FS45_LDT_SetTimerMode()`.
- enum `fs45_ldt_wu_scr_t` { `fs45LdtWakeupProg` = `FS45_RW_M_REG_SE_PROGRAMMED_REG`, `fs45LdtWakeupRTC` = `FS45_RW_M_REG_SE_RTC_REG` }
Wake-up register source. Can be used with function `FS45_LDT_SetWakeUpRegSrc()`.
- enum `fs45_wd_window_t` {
`fs45WdWindowDisable` = `FS45_W_FS_WD_WINDOW_DISABLE`, `fs45WdWindow1ms` = `FS45_W_FS_WD_WINDOW_1MS`, `fs45WdWindow2ms` = `FS45_W_FS_WD_WINDOW_2MS`, `fs45WdWindow3ms` = `FS45_W_FS_WD_WINDOW_3MS`,
`fs45WdWindow4ms` = `FS45_W_FS_WD_WINDOW_4MS`, `fs45WdWindow6ms` = `FS45_W_FS_WD_WINDOW_6MS`, `fs45WdWindow8ms` = `FS45_W_FS_WD_WINDOW_8MS`, `fs45WdWindow12ms` = `FS45_W_FS_WD_WINDOW_12MS`,
`fs45WdWindow16ms` = `FS45_W_FS_WD_WINDOW_16MS`, `fs45WdWindow24ms` = `FS45_W_FS_WD_WINDOW_24MS`, `fs45WdWindow32ms` = `FS45_W_FS_WD_WINDOW_32MS`, `fs45WdWindow64ms` = `FS45_W_FS_WD_WINDOW_64MS`,
`fs45WdWindow128ms` = `FS45_W_FS_WD_WINDOW_128MS`, `fs45WdWindow256ms` = `FS45_W_FS_WD_WINDOW_256MS`, `fs45WdWindow512ms` = `FS45_W_FS_WD_WINDOW_512MS`, `fs45WdWindow1024ms` = `FS45_W_FS_WD_WINDOW_1024MS` }
Watchdog window duration. Duty cycle is set to 50 %. Can be used with function `FS45_WD_ChangeWindow()`.
- enum `fs45_fsx_req_type_t` { `fs45ReqFS0B` = `FS45_W_FS_FS0B_REQ_FS0B_REQ`, `fs45ReqFS1BDelay` = `FS45_W_FS_FS1B_DLY_REQ_FS1B_REQ`, `fs45ReqFS1B` = `FS45_W_FS_FS1B_REQ_FS1B_REQ` }
Fail-safe output selection for its low level request. Can be used with function `FS45_RequestFSxLow()`.

Functions

- status_t `FS45_Init` (const `fs45_drv_config_t` *drvConfig, uint32_t lpspiInstance, uint32_t lpspiTimeoutMs)
This function runs full initialization of the SBC device.
- void `FS45_GetDefaultInitRegsConfig` (`fs45_drv_config_t` *drvConfig)
This function fills the driver configuration structure with default values of INIT phase registers.
- void `FS45_GetDefaultNonInitRegsConfig` (`fs45_drv_config_t` *drvConfig, `fs45_reg_config_value_t` *nonInitRegs)
This function fills the driver configuration structure with default values of non-init registers.
- status_t `FS45_ReadRegister` (uint8_t address, `fs45_rx_data_t` *rxData)

- Performs a read from a single FS45 register.*
- status_t [FS45_WriteRegister](#) (uint8_t address, uint8_t writeData, [fs45_rx_data_t](#) *rxData)
Sends write command to the FS45.
- status_t [FS45_WD_ChangeSeed](#) (uint8_t wdSeed)
Changes seed of LFSR used for watchdog.
- status_t [FS45_SwitchAMUXchannel](#) ([fs45_amux_selection_t](#) channelSelection)
Switches a desired channel to the AMUX pin.
- status_t [FS45_SetRegulatorState](#) ([fs45_reg_mode_t](#) vreg, bool enable)
Sets state (enable/disable) of the selected voltage regulator.
- status_t [FS45_GetFaultErrorCounterValue](#) (uint8_t *faultErrorCounterValue)
Reads actual Fault Error Counter value.
- status_t [FS45_GetMode](#) ([fs45_current_mode_t](#) *currentMode, [fs45_prev_mode_t](#) *prevMode)
This function gets current and previous mode of the SBC.
- status_t [FS45_CheckVAUX](#) (void)
This function checks if VAUX is safety critical and optionally runs related diagnostics.
- status_t [FS45_CheckFS1B](#) (void)
This function checks if FS1B has expected low level during initialization and runs related diagnostics.
- status_t [FS45_ReleaseFSx](#) ([fs45_fsxb_release_t](#) fsOutput)
This function releases selected fail-safe output as a part of error recovery procedure.
- status_t [FS45_CheckLbistAbistOk](#) (void)
Checks if LBIST and ABIST1 diagnostics passed.
- status_t [FS45_SetLowPowerMode](#) (bool autoWU)
This function switches mode of the SBC to the LPOFF, optionally with automatic wake-up 1ms after transition.
- status_t [FS45_RequestInterrupt](#) (void)
This function requests an interrupt (pulse on the INT pin).
- status_t [FS45_CAN_SetMode](#) ([fs45_can_mode_t](#) mode, bool autoDis)
This function changes CAN mode and the automatic transition of the CAN transceiver to the low-power mode on specific events.
- status_t [FS45_LDT_SetTimerOperation](#) ([fs45_ldt_function_t](#) op)
This function sets operating function of the LDT.
- status_t [FS45_LDT_SetTimerMode](#) ([fs45_ldt_mode_t](#) mode)
This function sets mode of the LDT (normal/calibration).
- status_t [FS45_LDT_SetWakeUpRegSrc](#) ([fs45_ldt_wu_scr_t](#) source)
This function sets counter to read real-time counter or programmed value into wake-up register.
- status_t [FS45_LDT_RunCounter](#) (bool run)
This function starts or stops the LDT counter.
- status_t [FS45_LDT_SetAfterRunValue](#) (uint16_t value)
This function sets new after-run value for the LDT.
- status_t [FS45_LDT_SetWakeUpValue](#) (uint32_t value)
This function sets new wake-up value for the LDT.
- status_t [FS45_WD_ChangeWindow](#) ([fs45_wd_window_t](#) windowDuration)
This function changes duration of watchdog window.
- status_t [FS45_WD_Refresh](#) (void)
This function refreshes watchdog of the SBC device.
- status_t [FS45_RequestReset](#) (void)
This function requests a low pulse on the RSTB (MCU reset).
- status_t [FS45_RequestFSxLow](#) ([fs45_fsx_req_type_t](#) fsxSelection)
This function requests a low level on the selected fail-safe output.
- status_t [FS45_SetOUT4](#) (bool level)
This function sets level of the IO_4 when configured as an output.

17.125.2 Data Structure Documentation

17.125.2.1 struct fs45_rx_data_t

Structure representing received data frame.

Implements : fs45_rx_data_t_Class

Definition at line 226 of file sbc_fs45_driver.h.

Data Fields

- uint8_t [deviceStatus](#)
A device status is returned into this byte after a successful transfer.
- uint8_t [deviceStatusEx](#)
Extended diagnostics. Sent by Main or Fail-safe if secured register is accessed.
- uint8_t [readData](#)
Content of a read register.

Field Documentation

17.125.2.1.1 uint8_t deviceStatus

A device status is returned into this byte after a successful transfer.

Definition at line 229 of file sbc_fs45_driver.h.

17.125.2.1.2 uint8_t deviceStatusEx

Extended diagnostics. Sent by Main or Fail-safe if secured register is accessed.

Diagnostics content is saved in 4 highest bits.

Definition at line 233 of file sbc_fs45_driver.h.

17.125.2.1.3 uint8_t readData

Content of a read register.

Definition at line 235 of file sbc_fs45_driver.h.

17.125.2.2 struct fs45_reg_config_value_t

Structure representing configuration value of one register.

Definition at line 239 of file sbc_fs45_driver.h.

Data Fields

- uint8_t [address](#)
Register address.
- uint8_t [value](#)
Mask used for register read value check.
- uint8_t [readMask](#)

Field Documentation

17.125.2.2.1 uint8_t address

Register address.

<Value of the register.

Definition at line 242 of file sbc_fs45_driver.h.

17.125.2.2.2 uint8_t readMask

Definition at line 246 of file sbc_fs45_driver.h.

17.125.2.2.3 uint8_t value

Mask used for register read value check.

Definition at line 244 of file sbc_fs45_driver.h.

17.125.2.3 struct fs45_vreg_reg_t

Initialization structure with INIT_VREG content.

Definition at line 250 of file sbc_fs45_driver.h.

Data Fields

- uint8_t [iccaLim](#)
Current limitation threshold for VCCA.
- uint8_t [tccaLimOff](#)
Current limitation duration before VCCA is switched off.
- uint8_t [ipffDis](#)
Disable the input power feed forward function of VPFE.
- uint8_t [vcanOvMon](#)
CAN_5V overvoltage monitoring.
- uint8_t [tauxLimOff](#)
Current limitation duration before VAUX is switched off.
- uint8_t [vauxTrkEn](#)
Enable VAUX regulator as a tracker of VCCA.

Field Documentation

17.125.2.3.1 uint8_t iccaLim

Current limitation threshold for VCCA.

Definition at line 253 of file sbc_fs45_driver.h.

17.125.2.3.2 uint8_t ipffDis

Disable the input power feed forward function of VPFE.

Definition at line 257 of file sbc_fs45_driver.h.

17.125.2.3.3 uint8_t tauxLimOff

Current limitation duration before VAUX is switched off.

Definition at line 261 of file sbc_fs45_driver.h.

17.125.2.3.4 uint8_t tccaLimOff

Current limitation duration before VCCA is switched off.

Definition at line 255 of file sbc_fs45_driver.h.

17.125.2.3.5 uint8_t vauxTrkEn

Enable VAUX regulator as a tracker of VCCA.

Definition at line 263 of file sbc_fs45_driver.h.

17.125.2.3.6 uint8_t vcanOvMon

CAN_5V overvoltage monitoring.

Definition at line 259 of file sbc_fs45_driver.h.

17.125.2.4 struct fs45_wu1_reg_t

Initialization structure with INIT_WU1 content.

Definition at line 267 of file sbc_fs45_driver.h.

Data Fields

- uint8_t [wulo0](#)
IO_0 wake-up configuration.
- uint8_t [wulo2](#)
IO_2 wake-up configuration.
- uint8_t [wulo3](#)
IO_3 wake-up configuration.
- uint8_t [wulo4](#)
IO_4 wake-up configuration.

Field Documentation

17.125.2.4.1 uint8_t wulo0

IO_0 wake-up configuration.

Definition at line 270 of file sbc_fs45_driver.h.

17.125.2.4.2 uint8_t wulo2

IO_2 wake-up configuration.

Definition at line 272 of file sbc_fs45_driver.h.

17.125.2.4.3 uint8_t wulo3

IO_3 wake-up configuration.

Definition at line 274 of file sbc_fs45_driver.h.

17.125.2.4.4 uint8_t wulo4

IO_4 wake-up configuration.

Definition at line 276 of file sbc_fs45_driver.h.

17.125.2.5 struct fs45_wu2_reg_t

Initialization structure with INIT_WU2 content.

Definition at line 280 of file sbc_fs45_driver.h.

Data Fields

- uint8_t [wulo5](#)
IO_5 wake-up configuration.
- uint8_t [canDisCfg](#)
CAN behavior when FS1B is asserted low.
- uint8_t [canWuTo](#)
CAN wake-up timeout.

- uint8_t [linJ2602Dis](#)
Comply with J2602 standard. Recessive mode when VSUP < 7.0 V.
- uint8_t [linSr](#)
LIN slew rate.

Field Documentation

17.125.2.5.1 uint8_t canDisCfg

CAN behavior when FS1B is asserted low.

Definition at line 285 of file sbc_fs45_driver.h.

17.125.2.5.2 uint8_t canWuTo

CAN wake-up timeout.

Definition at line 287 of file sbc_fs45_driver.h.

17.125.2.5.3 uint8_t linJ2602Dis

Comply with J2602 standard. Recessive mode when VSUP < 7.0 V.

Definition at line 289 of file sbc_fs45_driver.h.

17.125.2.5.4 uint8_t linSr

LIN slew rate.

Definition at line 291 of file sbc_fs45_driver.h.

17.125.2.5.5 uint8_t wulo5

IO_5 wake-up configuration.

Definition at line 283 of file sbc_fs45_driver.h.

17.125.2.6 struct fs45_int_reg_t

Initialization structure with INIT_INT content.

Definition at line 295 of file sbc_fs45_driver.h.

Data Fields

- uint8_t [duration](#)
Duration of the interrupt pulse.
- uint8_t [inhLin](#)
Inhibit the interrupt for LIN error bits.
- uint8_t [inhAll](#)
Inhibit ALL the interrupt.
- uint8_t [inhVsns](#)
Inhibit the interrupt for VSNS_UV.
- uint8_t [inhVpre](#)
Inhibit the interrupt for VPRES status event.
- uint8_t [inhVcore](#)
Inhibit the interrupt for VCORE status event.
- uint8_t [inhVother](#)
Inhibit the interrupt for VCCA/VAUX and VCAN status event.
- uint8_t [inhCan](#)
Inhibit the interrupt for CAN error bits.

Field Documentation

17.125.2.6.1 uint8_t duration

Duration of the interrupt pulse.

Definition at line 298 of file sbc_fs45_driver.h.

17.125.2.6.2 uint8_t inhAll

Inhibit ALL the interrupt.

Definition at line 302 of file sbc_fs45_driver.h.

17.125.2.6.3 uint8_t inhCan

Inhibit the interrupt for CAN error bits.

Definition at line 312 of file sbc_fs45_driver.h.

17.125.2.6.4 uint8_t inhLin

Inhibit the interrupt for LIN error bits.

Definition at line 300 of file sbc_fs45_driver.h.

17.125.2.6.5 uint8_t inhVcore

Inhibit the interrupt for VCORE status event.

Definition at line 308 of file sbc_fs45_driver.h.

17.125.2.6.6 uint8_t inhVother

Inhibit the interrupt for VCCA/VAUX and VCAN status event.

Definition at line 310 of file sbc_fs45_driver.h.

17.125.2.6.7 uint8_t inhVpre

Inhibit the interrupt for VPRE status event.

Definition at line 306 of file sbc_fs45_driver.h.

17.125.2.6.8 uint8_t inhVsns

Inhibit the interrupt for VSNS_UV.

Definition at line 304 of file sbc_fs45_driver.h.

17.125.2.7 struct fs45_inh_int_reg_t

Initialization structure with INIT_INH_INT content.

Definition at line 316 of file sbc_fs45_driver.h.

Data Fields

- uint8_t [inh5](#)
Inhibit the interrupt pulse for IO_5 (masked in IO_G).
- uint8_t [inh4](#)
Inhibit the interrupt pulse for IO_4 (masked in IO_G).
- uint8_t [inh3](#)
Inhibit the interrupt pulse for IO_3 (masked in IO_G).
- uint8_t [inh2](#)

- `uint8_t inh0`
Inhibit the interrupt pulse for IO_0 (masked in IO_G).

Field Documentation

17.125.2.7.1 `uint8_t inh0`

Inhibit the interrupt pulse for IO_0 (masked in IO_G).

Definition at line 327 of file `sbc_fs45_driver.h`.

17.125.2.7.2 `uint8_t inh2`

Inhibit the interrupt pulse for IO_2 (masked in IO_G).

Definition at line 325 of file `sbc_fs45_driver.h`.

17.125.2.7.3 `uint8_t inh3`

Inhibit the interrupt pulse for IO_3 (masked in IO_G).

Definition at line 323 of file `sbc_fs45_driver.h`.

17.125.2.7.4 `uint8_t inh4`

Inhibit the interrupt pulse for IO_4 (masked in IO_G).

Definition at line 321 of file `sbc_fs45_driver.h`.

17.125.2.7.5 `uint8_t inh5`

Inhibit the interrupt pulse for IO_5 (masked in IO_G).

Definition at line 319 of file `sbc_fs45_driver.h`.

17.125.2.8 `struct fs45_fs1b_timing_reg_t`

Initialization structure with INIT_FS1B_TIMING content.

Definition at line 331 of file `sbc_fs45_driver.h`.

Data Fields

- `uint8_t fs1bTime`
Delay between FS0B and FS1B activation.

Field Documentation

17.125.2.8.1 `uint8_t fs1bTime`

Delay between FS0B and FS1B activation.

Definition at line 334 of file `sbc_fs45_driver.h`.

17.125.2.9 `struct fs45_supervisor_reg_t`

Initialization structure with INIT_SUPERVISOR content.

Definition at line 338 of file `sbc_fs45_driver.h`.

Data Fields

- `uint8_t vcore5d`
VCORE undervoltage in degraded mode. Only valid for 5.0 V.

- `uint8_t vcca5d`
VCCA undervoltage in degraded mode. Only valid for 5.0 V.
- `uint8_t vaux5d`
VAUX undervoltage in degraded mode. Only valid for 5.0 V.
- `uint8_t fs1bTimeRange`
FS1B timing range factor x1 or x8.

Field Documentation

17.125.2.9.1 `uint8_t fs1bTimeRange`

FS1B timing range factor x1 or x8.

Definition at line 347 of file `sbc_fs45_driver.h`.

17.125.2.9.2 `uint8_t vaux5d`

VAUX undervoltage in degraded mode. Only valid for 5.0 V.

Definition at line 345 of file `sbc_fs45_driver.h`.

17.125.2.9.3 `uint8_t vcca5d`

VCCA undervoltage in degraded mode. Only valid for 5.0 V.

Definition at line 343 of file `sbc_fs45_driver.h`.

17.125.2.9.4 `uint8_t vcore5d`

VCORE undervoltage in degraded mode. Only valid for 5.0 V.

Definition at line 341 of file `sbc_fs45_driver.h`.

17.125.2.10 `struct fs45_fault_reg_t`

Initialization structure with `INIT_FAULT` content.

Definition at line 351 of file `sbc_fs45_driver.h`.

Data Fields

- `uint8_t fltErrFs`
Values of the fault error counter.
- `uint8_t fs1bCanImpact`
CAN behavior when FS1B is asserted low.
- `uint8_t fltErrImp`
RSTB and FS0B behavior when fault error counter \geq intermediate value.

Field Documentation

17.125.2.10.1 `uint8_t fltErrFs`

Values of the fault error counter.

Definition at line 354 of file `sbc_fs45_driver.h`.

17.125.2.10.2 `uint8_t fltErrImp`

RSTB and FS0B behavior when fault error counter \geq intermediate value.

Definition at line 358 of file `sbc_fs45_driver.h`.

17.125.2.10.3 uint8_t fs1bCanImpact

CAN behavior when FS1B is asserted low.

Definition at line 356 of file sbc_fs45_driver.h.

17.125.2.11 struct fs45_fssm_reg_t

Initialization structure with INIT_FSSM content.

Definition at line 362 of file sbc_fs45_driver.h.

Data Fields

- uint8_t [io45Fs](#)
IO_4:5 as safety inputs for external IC error monitoring.
- uint8_t [io23Fs](#)
IO_3:2 as safety inputs for FCCU monitoring.
- uint8_t [ps](#)
FCCU polarity.
- uint8_t [rstbDuration](#)
RSTB low duration time.

Field Documentation

17.125.2.11.1 uint8_t io23Fs

IO_3:2 as safety inputs for FCCU monitoring.

Definition at line 367 of file sbc_fs45_driver.h.

17.125.2.11.2 uint8_t io45Fs

IO_4:5 as safety inputs for external IC error monitoring.

Definition at line 365 of file sbc_fs45_driver.h.

17.125.2.11.3 uint8_t ps

FCCU polarity.

Definition at line 369 of file sbc_fs45_driver.h.

17.125.2.11.4 uint8_t rstbDuration

RSTB low duration time.

Definition at line 371 of file sbc_fs45_driver.h.

17.125.2.12 struct fs45_sf_impact_reg_t

Initialization structure with INIT_SF_IMPACT content.

Definition at line 375 of file sbc_fs45_driver.h.

Data Fields

- uint8_t [tdlyTdur](#)
FS1B delay or FS1B duration mode selection.
- uint8_t [dis8s](#)
Disable the 8.0 s timer used to enter deep fail-safe mode.
- uint8_t [wdlImpact](#)
Watchdog impact on RSTB and/or FS0B assertion.

Field Documentation

17.125.2.12.1 `uint8_t dis8s`

Disable the 8.0 s timer used to enter deep fail-safe mode.

Definition at line 380 of file `sbc_fs45_driver.h`.

17.125.2.12.2 `uint8_t tdlyTdur`

FS1B delay or FS1B duration mode selection.

Definition at line 378 of file `sbc_fs45_driver.h`.

17.125.2.12.3 `uint8_t wdImpact`

Watchdog impact on RSTB and/or FS0B assertion.

Definition at line 382 of file `sbc_fs45_driver.h`.

17.125.2.13 `struct fs45_wd_cnt_reg_t`

Initialization structure with `INIT_WD_CNT` content.

Definition at line 386 of file `sbc_fs45_driver.h`.

Data Fields

- `uint8_t wdCntErr`
Maximum value of the WD error counter.
- `uint8_t wdCntRfr`
Maximum value of the WD refresh counter.

Field Documentation

17.125.2.13.1 `uint8_t wdCntErr`

Maximum value of the WD error counter.

Definition at line 389 of file `sbc_fs45_driver.h`.

17.125.2.13.2 `uint8_t wdCntRfr`

Maximum value of the WD refresh counter.

Definition at line 391 of file `sbc_fs45_driver.h`.

17.125.2.14 `struct fs45_vcore_ovuv_impact_reg_t`

Initialization structure with `INIT_VCORE_OVUV_IMPACT` content.

Definition at line 395 of file `sbc_fs45_driver.h`.

Data Fields

- `uint8_t vcoreFsOv`
VCORE_FB overvoltage safety impact.
- `uint8_t vcoreFsUv`
VCORE_FB undervoltage safety impact.

Field Documentation

17.125.2.14.1 `uint8_t vcoreFsOv`

VCORE_FB overvoltage safety impact.

Definition at line 398 of file sbc_fs45_driver.h.

17.125.2.14.2 uint8_t vcoreFsUv

VCORE_FB undervoltage safety impact.

Definition at line 400 of file sbc_fs45_driver.h.

17.125.2.15 struct fs45_vcca_ovuv_impact_reg_t

Initialization structure with INIT_VCCA_OVUV_IMPACT content.

Definition at line 404 of file sbc_fs45_driver.h.

Data Fields

- uint8_t [vccaFsOv](#)
VCCA overvoltage safety impact.
- uint8_t [vccaFsUv](#)
VCCA undervoltage safety impact.

Field Documentation

17.125.2.15.1 uint8_t vccaFsOv

VCCA overvoltage safety impact.

Definition at line 407 of file sbc_fs45_driver.h.

17.125.2.15.2 uint8_t vccaFsUv

VCCA undervoltage safety impact.

Definition at line 409 of file sbc_fs45_driver.h.

17.125.2.16 struct fs45_vaux_ovuv_impact_reg_t

Initialization structure with INIT_VAUX_OVUV_IMPACT content.

Definition at line 413 of file sbc_fs45_driver.h.

Data Fields

- uint8_t [vauxFsOv](#)
VAUX overvoltage safety impact.
- uint8_t [vauxFsUv](#)
VAUX undervoltage safety impact.

Field Documentation

17.125.2.16.1 uint8_t vauxFsOv

VAUX overvoltage safety impact.

Definition at line 416 of file sbc_fs45_driver.h.

17.125.2.16.2 uint8_t vauxFsUv

VAUX undervoltage safety impact.

Definition at line 418 of file sbc_fs45_driver.h.

17.125.2.17 struct fs45_drv_config_t

Structure for FS45 driver configuration.

This structure is used as a parameter for [FS45_Init\(\)](#) function.

Implements : [fs45_drv_config_t_Class](#)

Definition at line 428 of file [sbc_fs45_driver.h](#).

Data Fields

- [fs45_vreg_reg_t vregReg](#)
Main logic registers.
- [fs45_wu1_reg_t wu1Reg](#)
- [fs45_wu2_reg_t wu2Reg](#)
- [fs45_inh_int_reg_t inhIntReg](#)
- [fs45_fs1b_timing_reg_t fs1bTimingReg](#)
Fail-safe logic registers.
- [fs45_supervisor_reg_t supervisorReg](#)
- [fs45_fault_reg_t faultReg](#)
- [fs45_fssm_reg_t fssmReg](#)
- [fs45_sf_impact_reg_t sfImpactReg](#)
- [fs45_wd_cnt_reg_t wdCntReg](#)
- [fs45_vcore_ovuv_impact_reg_t vcoreOvuvImpactReg](#)
- [fs45_vcca_ovuv_impact_reg_t vccaOvuvImpactReg](#)
- [fs45_vaux_ovuv_impact_reg_t vauxOvuvImpactReg](#)
- [fs45_int_reg_t intReg](#)
INIT_INT register.
- [fs45_reg_config_value_t * nonInitRegs](#)
Non-init registers (both main and fails-safe logic).
- [uint8_t nonInitRegsCount](#)

Field Documentation**17.125.2.17.1 fs45_fault_reg_t faultReg**

Definition at line 468 of file [sbc_fs45_driver.h](#).

17.125.2.17.2 fs45_fs1b_timing_reg_t fs1bTimingReg

Fail-safe logic registers.

Configuration values for fail-safe logic registers written during INIT phase. Following registers can be configured:

- [INIT_FS1B_TIMING](#)
- [INIT_SUPERVISOR](#)
- [INIT_FAULT](#)
- [INIT_FSSM](#)
- [INIT_SF_IMPACT](#)
- [INIT_WD_CNT](#)
- [INIT_VCORE_OVUV_IMPACT](#)
- [INIT_VCCA_OVUV_IMPACT](#)
- [INIT_VAUX_OVUV_IMPACT](#)

These registers use secured SPI command, please use unshifted values (the same as when the register is read). The shift and addition of secure bits is done automatically by the Init function.

Definition at line 466 of file sbc_fs45_driver.h.

17.125.2.17.3 fs45_fssm_reg_t fssmReg

Definition at line 469 of file sbc_fs45_driver.h.

17.125.2.17.4 fs45_inh_int_reg_t inhIntReg

Definition at line 445 of file sbc_fs45_driver.h.

17.125.2.17.5 fs45_int_reg_t intReg

INIT_INT register.

Writing into this register causes transition from INIT MAIN to NORMAL MODE.

Definition at line 481 of file sbc_fs45_driver.h.

17.125.2.17.6 fs45_reg_config_value_t* nonInitRegs

Non-init registers (both main and fails-safe logic).

Array of register configurations of the rest of the registers (or just selection of them - based on address and nonInitRegsCount). If nonInitRegs is NULL, or nonInitRegsCount is 0, it will be skipped.

Some of these registers use secured SPI command, please use unshifted values (the same as when the register is read). The shift and addition of secure bits is done automatically by the Init function.

Definition at line 494 of file sbc_fs45_driver.h.

17.125.2.17.7 uint8_t nonInitRegsCount

Definition at line 495 of file sbc_fs45_driver.h.

17.125.2.17.8 fs45_sf_impact_reg_t sflImpactReg

Definition at line 470 of file sbc_fs45_driver.h.

17.125.2.17.9 fs45_supervisor_reg_t supervisorReg

Definition at line 467 of file sbc_fs45_driver.h.

17.125.2.17.10 fs45_vaux_ovuv_impact_reg_t vauxOvuvImpactReg

Definition at line 474 of file sbc_fs45_driver.h.

17.125.2.17.11 fs45_vcca_ovuv_impact_reg_t vccaOvuvImpactReg

Definition at line 473 of file sbc_fs45_driver.h.

17.125.2.17.12 fs45_vcore_ovuv_impact_reg_t vcoreOvuvImpactReg

Definition at line 472 of file sbc_fs45_driver.h.

17.125.2.17.13 fs45_vreg_reg_t vregReg

Main logic registers.

Configuration values for main logic registers written during INIT phase. Following registers can be configured:

- INIT_VREG
- INIT_WU1

- INIT_WU2
- INIT_INH_INT

Note

INIT_INT register is separate at the end of this structure.

Definition at line 442 of file sbc_fs45_driver.h.

17.125.2.17.14 fs45_wd_cnt_reg_t wdCntReg

Definition at line 471 of file sbc_fs45_driver.h.

17.125.2.17.15 fs45_wu1_reg_t wu1Reg

Definition at line 443 of file sbc_fs45_driver.h.

17.125.2.17.16 fs45_wu2_reg_t wu2Reg

Definition at line 444 of file sbc_fs45_driver.h.

17.125.3 Enumeration Type Documentation

17.125.3.1 enum fs45_amux_selection_t

AMUX channel selection. Can be used with function [FS45_SwitchAMUXchannel\(\)](#).

Implements : fs45_amux_selection_t_Enumeration

Enumerator

- fs45AmuxVref** V_REF.
- fs45AmuxVsnsWide** V_SNS wide range.
- fs45AmuxIO_0Wide** IO_0 wide range.
- fs45AmuxIO_5Wide** IO_5 wide range.
- fs45AmuxVsnsTight** V_SNS tight range.
- fs45AmuxIO_0Tight** IO_0 tight range.
- fs45AmuxIO_5TightDivVkam** IO_5 tight range/VKAM.
- fs45AmuxDieTempSensor** Die Temperature Sensor.

Definition at line 95 of file sbc_fs45_driver.h.

17.125.3.2 enum fs45_can_mode_t

CAN mode. Can be used with function [FS45_CAN_SetMode\(\)](#).

Implements : fs45_can_mode_t_Enumeration

Enumerator

- fs45CanModeSleepNoWakeup** Sleep/no wake-up capability.
- fs45CanModeListenOnly** Listen only.
- fs45CanModeSleepWakeup** Sleep/wake-up capability.
- fs45CanModeNormal** Normal operation mode.

Definition at line 112 of file sbc_fs45_driver.h.

17.125.3.3 enum **fs45_current_mode_t**

Actual SBC state.

Implements : fs45_current_mode_t_Enumeration

Enumerator

fs45ModeUnknown Current SBC mode is unknown.

fs45Modelnit Current SBC mode is INIT.

fs45ModeNormal Current SBC mode is NORMAL.

Definition at line 64 of file sbc_fs45_driver.h.

17.125.3.4 enum **fs45_fsx_req_type_t**

Fail-safe output selection for its low level request. Can be used with function [FS45_RequestFSxLow\(\)](#).

Implements : fs45_fsx_req_type_t_Enumeration

Enumerator

fs45ReqFS0B Request FS0B assertion.

fs45ReqFS1BDelay Request FS1B assertion with tDELAY controlled by the backup delay (open S1).

fs45ReqFS1B Request FS1B assertion with immediate assertion, no delay.

Definition at line 211 of file sbc_fs45_driver.h.

17.125.3.5 enum **fs45_fsxb_release_t**

FSxb pin release options.

Implements : fs45_fsxb_release_t_Enumeration

Enumerator

fs45ReleaseFs0b Release FS0b pin only.

fs45ReleaseFs1b Release FS1b pin only.

fs45ReleaseFs0bFs1b Release both FS0b and FS1b pins.

Definition at line 40 of file sbc_fs45_driver.h.

17.125.3.6 enum **fs45_ldt_function_t**

LDT operating function. Can be used with function [FS45_LDT_SetTimerOperation\(\)](#).

Implements : fs45_ldt_function_t_Enumeration

Enumerator

fs45LdtFunc1 In normal mode count and generate flag or INT when counter reaches the after run value.

fs45LdtFunc2 In normal mode count until after run value is reached, then enters in LPOFF.

fs45LdtFunc3 In normal mode count until after run value is reached, then enters in LPOFF. Once in LPOFF, count until wake-up value is reached and wake-up.

fs45LdtFunc4 In LPOFF, count until wake-up value is reached and wake-up.

fs45LdtFunc5 In LPOFF, count and do not wake-up. Counter value is stored in wake-up register.

Definition at line 140 of file sbc_fs45_driver.h.

17.125.3.7 enum **fs45_ldt_mode_t**

LDT mode. Can be used with function [FS45_LDT_SetTimerMode\(\)](#).

Implements : fs45_ldt_mode_t_Enumeration

Enumerator

fs45LdtModeCalibration Calibration mode (488 us resolution).

fs45LdtModeNormal Normal mode (1 s resolution).

Definition at line 160 of file sbc_fs45_driver.h.

17.125.3.8 enum **fs45_ldt_wu_scr_t**

Wake-up register source. Can be used with function [FS45_LDT_SetWakeUpRegSrc\(\)](#).

Implements : fs45_ldt_wu_scr_t_Enumeration

Enumerator

fs45LdtWakeupProg Read programmed wake-up register.

fs45LdtWakeupRTC Read real time counter into wake-up register (after counter is stopped with LDT_ENA↔ BLE bit).

Definition at line 171 of file sbc_fs45_driver.h.

17.125.3.9 enum **fs45_prev_mode_t**

Previous SBC state.

Implements : fs45_prev_mode_t_Enumeration

Enumerator

fs45PrevModePOR Previous SBC mode was POR (power on reset).

fs45PrevModeDFS Resume from deep fail-safe mode.

fs45PrevModeLPOFF Resume from LPOFF mode.

Definition at line 52 of file sbc_fs45_driver.h.

17.125.3.10 enum **fs45_reg_mode_t**

Voltage outputs. Can be used with function [FS45_SetRegulatorState\(\)](#).

Implements : fs45_reg_mode_t_Enumeration

Enumerator

fs45VCan VCAN control.

fs45Aux VAUX control (switch off not recommended if VAUX is safety critical).

fs45Vcca VCCA control (switch off not recommended if VCCA is safety critical).

fs45Vcore VCORE control (switch off not recommended if VCORE is safety critical).

fs45Vkam VKAM control.

Definition at line 76 of file sbc_fs45_driver.h.

17.125.3.11 enum **fs45_wd_window_t**

Watchdog window duration. Duty cycle is set to 50 %. Can be used with function [FS45_WD_ChangeWindow\(\)](#).

Implements : fs45_wd_window_t_Enumeration

Enumerator

fs45WdWindowDisable Disable (in INIT phase only).

fs45WdWindow1ms 1.0 ms.

fs45WdWindow2ms 2.0 ms.

fs45WdWindow3ms 3.0 ms.

fs45WdWindow4ms 4.0 ms.

fs45WdWindow6ms 6.0 ms.

fs45WdWindow8ms 8.0 ms.

fs45WdWindow12ms 12 ms.

fs45WdWindow16ms 16 ms.

fs45WdWindow24ms 24 ms.

fs45WdWindow32ms 32 ms.

fs45WdWindow64ms 64 ms.

fs45WdWindow128ms 128 ms.

fs45WdWindow256ms 256 ms.

fs45WdWindow512ms 512 ms.

fs45WdWindow1024ms 1024 ms.

Definition at line 185 of file sbc_fs45_driver.h.

17.125.4 Function Documentation

17.125.4.1 `status_t FS45_CAN_SetMode (fs45_can_mode_t mode, bool autoDis)`

This function changes CAN mode and the automatic transition of the CAN transceiver to the low-power mode on specific events.

Parameters

<i>mode</i>	CAN mode.
<i>autoDis</i>	Automatic transition to the LPOFF on (CAN OT/TXD dominant/RXD recessive).

Returns

`status_t` Status return code.

Remarks

The function returns STATUS_SUCCESS when used on device without CAN, but the register access does not affect the device behavior.

Definition at line 1368 of file sbc_fs45_driver.c.

17.125.4.2 `status_t FS45_CheckFS1B (void)`

This function checks if FS1B has expected low level during initialization and runs related diagnostics.

Returns

`status_t` Status return code.

Definition at line 1123 of file sbc_fs45_driver.c.

17.125.4.3 `status_t FS45_CheckLbistAbistOk (void)`

Checks if LBIST and ABIST1 diagnostics passed.

Returns

`status_t` Status return code.

Definition at line 1272 of file `sbc_fs45_driver.c`.

17.125.4.4 `status_t FS45_CheckVAUX (void)`

This function checks if VAUX is safety critical and optionally runs related diagnostics.

Returns

`status_t` Status return code.

Definition at line 1073 of file `sbc_fs45_driver.c`.

17.125.4.5 `void FS45_GetDefaultInitRegsConfig (fs45_drv_config_t * drvConfig)`

This function fills the driver configuration structure with default values of INIT phase registers.

The init registers configurations are filled with default datasheet values.

Remarks

Default value of FS1B_CAN_IMPACT bit (INIT_FAULT register) is different than the datasheet value for devices with FS1B.

Parameters

<i>drvConfig</i>	Configuration structure of the SW driver.
------------------	---

Definition at line 695 of file `sbc_fs45_driver.c`.

17.125.4.6 `void FS45_GetDefaultNonInitRegsConfig (fs45_drv_config_t * drvConfig, fs45_reg_config_value_t * nonInitRegs)`

This function fills the driver configuration structure with default values of non-init registers.

The configurations of all writable non-init registers are filled with default datasheet values.

Parameters

<i>drvConfig</i>	Configuration structure of the SW driver.
<i>nonInitRegs</i>	Pointer to store default values for all registers which can be configured after init. Application should guarantee space for 5 registers.

Definition at line 766 of file `sbc_fs45_driver.c`.

17.125.4.7 `status_t FS45_GetFaultErrorCounterValue (uint8_t * faultErrorCounterValue)`

Reads actual Fault Error Counter value.

Parameters

<i>faultErrorCounterValue</i>	Fault Error counter value storage.
-------------------------------	------------------------------------

Returns

`status_t` Status return code.

Definition at line 992 of file `sbc_fs45_driver.c`.

17.125.4.8 `status_t FS45_GetMode(fs45_current_mode_t * currentMode, fs45_prev_mode_t * prevMode)`

This function gets current and previous mode of the SBC.

Parameters

<i>currentMode</i>	Current mode of the SBC device.
<i>prevMode</i>	Previous mode of the SBC device.

Returns

`status_t` Status return code.

Definition at line 1019 of file `sbc_fs45_driver.c`.

17.125.4.9 `status_t FS45_Init (const fs45_drv_config_t * drvConfig, uint32_t lpspiInstance, uint32_t lpspiTimeoutMs)`

This function runs full initialization of the SBC device.

This function writes configuration values to selected SBC registers (i.e. content of the `drvConfig` structure), checks results of built-in self-test diagnostics and optionally runs additional procedures to ensure correct functionality of safety critical features. The first watchdog refresh is part of the initialization procedure, the SBC should be in NORMAL mode upon the function exit.

Parameters

<i>drvConfig</i>	Configuration structure of the SW driver.
<i>lpspiInstance</i>	SPI peripheral instance.
<i>lpspiTimeoutMs</i>	SPI timeout in ms.

Returns

`status_t` Status return code.

Remarks

Note that main register set is initialized only after power on reset. It retains its values after transition to low-power mode and back to normal. It is recommended to read-out wake-up sources and diagnostic statuses after initialization to clear all flags.

Definition at line 478 of file `sbc_fs45_driver.c`.

17.125.4.10 `status_t FS45_LDT_RunCounter (bool run)`

This function starts or stops the LDT counter.

Parameters

<i>run</i>	Use true for start or false for stop the LDT counter.
------------	---

Returns

`status_t` Status return code.

Definition at line 1603 of file `sbc_fs45_driver.c`.

17.125.4.11 `status_t FS45_LDT_SetAfterRunValue (uint16_t value)`

This function sets new after-run value for the LDT.

Parameters

<i>value</i>	After-run value.
--------------	------------------

Returns

`status_t` Status return code.

Definition at line 1649 of file `sbc_fs45_driver.c`.

17.125.4.12 `status_t FS45_LDT_SetTimerMode (fs45_ldt_mode_t mode)`

This function sets mode of the LDT (normal/calibration).

Parameters

<i>mode</i>	Mode of the LDT.
-------------	------------------

Returns

`status_t` Status return code.

Remarks

Resolution is 1s for normal mode and 488us for calibration mode.

Definition at line 1512 of file `sbc_fs45_driver.c`.

17.125.4.13 `status_t FS45_LDT_SetTimerOperation (fs45_ldt_function_t op)`

This function sets operating function of the LDT.

Parameters

<i>op</i>	Operating function of the LDT.
-----------	--------------------------------

Returns

`status_t` Status return code.

Definition at line 1467 of file `sbc_fs45_driver.c`.

17.125.4.14 `status_t FS45_LDT_SetWakeUpRegSrc (fs45_ldt_wu_scr_t source)`

This function sets counter to read real-time counter or programmed value into wake-up register.

Parameters

<i>source</i>	Source for the wake-up register.
---------------	----------------------------------

Returns

`status_t` Status return code.

Definition at line 1558 of file `sbc_fs45_driver.c`.

17.125.4.15 `status_t FS45_LDT_SetWakeUpValue (uint32_t value)`

This function sets new wake-up value for the LDT.

Parameters

<i>value</i>	Wake-up value (1 - 16777215).
--------------	-------------------------------

Returns

`status_t` Status return code.

Definition at line 1704 of file `sbcs45_driver.c`.

17.125.4.16 `status_t FS45_ReadRegister (uint8_t address, fs45_rx_data_t * rxData)`

Performs a read from a single FS45 register.

Performs a single read register based on provided address. The response is returned in `fs45_rx_data_t` structure.

Parameters

<i>address</i>	Register address.
<i>rxData</i>	Structure holding the response from SBC.

Returns

`status_t` Status return code.

Definition at line 803 of file `sbcs45_driver.c`.

17.125.4.17 `status_t FS45_ReleaseFSx (fs45_fsxb_release_t fsOutput)`

This function releases selected fail-safe output as a part of error recovery procedure.

Parameters

<i>fsOutput</i>	Selection of fail-safe output.
-----------------	--------------------------------

Returns

`status_t` Status return code.

Remarks

When a fault is removed and the fault error counter changes back to level '0', a right word must be filled in the `RELEASE_FSxB` register. The value depends on the current `WD_LFSR`. LSB, MSB must be swapped, and a negative operation per bit must be applied. The `RELEASE_FSxB` write command must be done after the `WD_LFSR` read command within the same `WD` period.

Definition at line 1194 of file `sbcs45_driver.c`.

17.125.4.18 `status_t FS45_RequestFSxLow (fs45_fsx_req_type_t fsxSelection)`

This function requests a low level on the selected fail-safe output.

Parameters

<i>fsxSelection</i>	Selection of fail-safe output.
---------------------	--------------------------------

Returns

`status_t` Status return code.

Definition at line 1872 of file `sbcs45_driver.c`.

17.125.4.19 status_t FS45_RequestInterrupt (void)

This function requests an interrupt (pulse on the INT pin).

Returns

status_t Status return code.

Definition at line 1339 of file sbc_fs45_driver.c.

17.125.4.20 status_t FS45_RequestReset (void)

This function requests a low pulse on the RSTB (MCU reset).

Returns

status_t Status return code.

Definition at line 1856 of file sbc_fs45_driver.c.

17.125.4.21 status_t FS45_SetLowPowerMode (bool autoWU)

This function switches mode of the SBC to the LPOFF, optionally with automatic wake-up 1 ms after transition.

Parameters

<i>autoWU</i>	Automatic wake-up 1 ms after transition.
---------------	--

Returns

status_t Status return code.

Definition at line 1307 of file sbc_fs45_driver.c.

17.125.4.22 status_t FS45_SetOUT4 (bool level)

This function sets level of the IO_4 when configured as an output.

Parameters

<i>level</i>	Level of IO_4 when configured as output. True for high level, false for low level.
--------------	--

Returns

status_t Status return code.

Remarks

Note that this function automatically enables IO_4 to be used as output.

Definition at line 1894 of file sbc_fs45_driver.c.

17.125.4.23 status_t FS45_SetRegulatorState (fs45_reg_mode_t vreg, bool enable)

Sets state (enable/disable) of the selected voltage regulator.

Parameters

<i>vreg</i>	Voltage regulator enum (VCAN, VAUX, VCCA, VCORE).
<i>enable</i>	State (enable = true / disable = false).

Returns

`status_t` Status return code.

Remarks

Disabling the regulators might result in loss of some functionality, based on the regulator type and your board design (for example loss of SPI communication, SPI MISO is powered by VDDIO internal regulator, which is usually supplied from VCORE or VCCA - depends on board connections).

Definition at line 893 of file `sbc_fs45_driver.c`.

17.125.4.24 `status_t FS45_SwitchAMUXchannel (fs45_amux_selection_t channelSelection)`

Switches a desired channel to the AMUX pin.

Parameters

<i>channelSelection</i>	Selected channel to be delivered to AMUX pin.
-------------------------	---

Returns

`status_t` Status return code.

Definition at line 879 of file `sbc_fs45_driver.c`.

17.125.4.25 `status_t FS45_WD_ChangeSeed (uint8_t wdSeed)`

Changes seed of LFSR used for watchdog.

The watchdog seed can be changed just during the INIT_FS phase (for challenger WD) or during the OPE↔N watchdog window (for simple WD). Timing is up to the application!

Parameters

<i>wdSeed</i>	Watchdog LFSR seed.
---------------	---------------------

Returns

`status_t` Status return code.

Definition at line 1817 of file `sbc_fs45_driver.c`.

17.125.4.26 `status_t FS45_WD_ChangeWindow (fs45_wd_window_t windowDuration)`

This function changes duration of watchdog window.

Parameters

<i>windowDuration</i>	Watchdog window duration.
-----------------------	---------------------------

Returns

`status_t` Status return code.

Definition at line 1782 of file `sbc_fs45_driver.c`.

17.125.4.27 `status_t FS45_WD_Refresh (void)`

This function refreshes watchdog of the SBC device.

Returns

`status_t` Status return code.

Remarks

MCU internally computes monitoring result based on a received challenge token (LFSR state) and sends it back as an answer.

Definition at line 846 of file `sbc_fs45_driver.c`.

17.125.4.28 `status_t FS45_WriteRegister (uint8_t address, uint8_t writeData, fs45_rx_data_t * rxData)`

Sends write command to the FS45.

Parameters

<i>address</i>	Register address.
<i>writeData</i>	Register write value.
<i>rxData</i>	Diagnostic data returned by the SBC.

Returns

`status_t` Status return code.

Remarks

The `rxData` pointer is not mandatory, if it's NULL, `writeData` are written to the register and received data is ignored.

Definition at line 825 of file `sbc_fs45_driver.c`.

17.126 SBC configuration control options (0x74)

17.126.1 Detailed Description

This section lists all the possible options of 0x74 register related to:

1. V1 reset threshold at start-up configuration
2. FNMC mode configuration
3. SDMC mode configuration
4. VEXT pin mode selection
5. Sleep mode support configuraion

See also

[UJA113X_SetMtpnv\(\)](#)

V1 reset threshold (defined by V1RTC) at start-up options (0x74:V1RTSUC[5:4])

- #define [V1RTSUC_90_NOM](#) 0x00U
V1 undervoltage detection at 90% of nominal value at start-up (V1RTC = 00)
- #define [V1RTSUC_80_NOM](#) 0x10U
V1 undervoltage detection at 80% of nominal value at start-up (V1RTC = 01)
- #define [V1RTSUC_70_NOM](#) 0x20U
V1 undervoltage detection at 70% of nominal value at start-up (V1RTC = 10)
- #define [V1RTSUC_60_NOM](#) 0x30U
V1 undervoltage detection at 60% of nominal value at start-up (V1RTC = 11)

Forced normal mode options (0x74:FNMC[3])

- #define [FNMC_DISABLE](#) 0x00U
Disable Forced Normal mode.
- #define [FNMC_ENABLE](#) 0x08U
Enabled Forced Normal mode.

Software Development mode options (0x74:SDMC[2])

- #define [SDMC_DISABLE](#) 0x00U
Disable Software Development mode.
- #define [SDMC_ENABLE](#) 0x04U
Enable Software Development mode.

V2 regulator configuration options (0x74:VEXTAC[1])

- #define [VEXTAC_SENSOR_SUPPLY](#) 0x00U
Regulator V2 can be used as a sensor supply via pin VEXT, provided pin V2 is left floating.
- #define [VEXTAC_NO_PROTECTION](#) 0x02U
Regulator V2 is not protected against shorts to higher voltages; pin V2 must be shorted to pin VEXT.

Sleep mode configuration options (0x74:SLPC[0])

- `#define SLPC_SLEEP_SUPPORTED 0x00U`
Sleep mode is supported.
- `#define SLPC_SLEEP_NOT_SUPPORTED 0x01U`
Sleep mode is not supported.

17.126.2 Macro Definition Documentation

17.126.2.1 `#define FNMC_DISABLE 0x00U`

Disable Forced Normal mode.

Definition at line 1341 of file `sbc_uja113x.h`.

17.126.2.2 `#define FNMC_ENABLE 0x08U`

Enabled Forced Normal mode.

Definition at line 1342 of file `sbc_uja113x.h`.

17.126.2.3 `#define SDMC_DISABLE 0x00U`

Disable Software Development mode.

Definition at line 1348 of file `sbc_uja113x.h`.

17.126.2.4 `#define SDMC_ENABLE 0x04U`

Enable Software Development mode.

Definition at line 1349 of file `sbc_uja113x.h`.

17.126.2.5 `#define SLPC_SLEEP_NOT_SUPPORTED 0x01U`

Sleep mode is not supported.

Definition at line 1363 of file `sbc_uja113x.h`.

17.126.2.6 `#define SLPC_SLEEP_SUPPORTED 0x00U`

Sleep mode is supported.

Definition at line 1362 of file `sbc_uja113x.h`.

17.126.2.7 `#define V1RTSUC_60_NOM 0x30U`

V1 undervoltage detection at 60% of nominal value at start-up (V1RTC = 11)

Definition at line 1335 of file `sbc_uja113x.h`.

17.126.2.8 `#define V1RTSUC_70_NOM 0x20U`

V1 undervoltage detection at 70% of nominal value at start-up (V1RTC = 10)

Definition at line 1334 of file `sbc_uja113x.h`.

17.126.2.9 `#define V1RTSUC_80_NOM 0x10U`

V1 undervoltage detection at 80% of nominal value at start-up (V1RTC = 01)

Definition at line 1333 of file `sbc_uja113x.h`.

17.126.2.10 #define V1RTSUC_90_NOM 0x00U

V1 undervoltage detection at 90% of nominal value at start-up (V1RTC = 00)

Definition at line 1332 of file sbc_uja113x.h.

17.126.2.11 #define VEXTAC_NO_PROTECTION 0x02U

Regulator V2 is not protected against shorts to higher voltages; pin V2 must be shorted to pin VEXT.

Definition at line 1356 of file sbc_uja113x.h.

17.126.2.12 #define VEXTAC_SENSOR_SUPPLY 0x00U

Regulator V2 can be used as a sensor supply via pin VEXT, provided pin V2 is left floating.

Definition at line 1355 of file sbc_uja113x.h.

17.127 Schedule management

17.127.1 Detailed Description

This group contains APIs that help users manage schedule tables in master node only.

Functions

- `I_u8 I_sch_tick (I_ifc_handle iii)`

This function follows a schedule. When a frame becomes due, its transmission is initiated. When the end of the current schedule is reached, this function starts again at the beginning of the schedule.

- `void I_sch_set (I_ifc_handle iii, I_schedule_handle schedule_iii, I_u8 entry)`

Set up the next schedule to be followed by the I_sch_tick function for a certain interface. The new schedule will be activated as soon as the current schedule reaches its next schedule entry point.

17.127.2 Function Documentation

17.127.2.1 void I_sch_set (I_ifc_handle iii, I_schedule_handle schedule_iii, I_u8 entry)

Set up the next schedule to be followed by the I_sch_tick function for a certain interface. The new schedule will be activated as soon as the current schedule reaches its next schedule entry point.

Parameters

in	iii	Interface name
in	schedule_iii	Schedule table for interface
in	entry	Entry to be set

Returns

void

Definition at line 73 of file lin_common_api.c.

17.127.2.2 I_u8 I_sch_tick (I_ifc_handle iii)

This function follows a schedule. When a frame becomes due, its transmission is initiated. When the end of the current schedule is reached, this function starts again at the beginning of the schedule.

Parameters

in	Interface	name
----	-----------	------

Returns

Operation status

- Zero: if the next call of I_sch_tick will not start transmission of a frame.
- Non-Zero: if the next call of I_sch_tick will start transmission of a frame. The return value will in this case be the next schedule table entry's number (counted from the beginning of the schedule table) in the schedule table. The return value will be in range 1 to N if the schedule table has N entries.

Definition at line 240 of file lin_common_api.c.

17.128 Security PAL

17.128.1 Detailed Description

Security Peripheral Abstraction Layer.

Data Structures

- struct [security_user_config_t](#)
Define user configuration Implements : [security_user_config_t_Class](#). [More...](#)

Enumerations

- enum [security_instance_t](#) { [SECURITY_INSTANCE0](#) = 0U }
Define instances for SECURITY PAL Implements : [security_instance_t_Class](#).
- enum [security_key_id_t](#) {
[SECURITY_SECRET_KEY](#) = 0x0U, [SECURITY_MASTER_ECU](#) = 0x1U, [SECURITY_BOOT_MAC_KEY](#) = 0x2U, [SECURITY_BOOT_MAC](#) = 0x3U,
[SECURITY_KEY_1](#), [SECURITY_KEY_2](#), [SECURITY_KEY_3](#), [SECURITY_KEY_4](#),
[SECURITY_KEY_5](#), [SECURITY_KEY_6](#), [SECURITY_KEY_7](#), [SECURITY_KEY_8](#),
[SECURITY_KEY_9](#), [SECURITY_KEY_10](#), [SECURITY_RAM_KEY](#) = 0xFU, [SECURITY_KEY_11](#) = 0x14U,
[SECURITY_KEY_12](#), [SECURITY_KEY_13](#), [SECURITY_KEY_14](#), [SECURITY_KEY_15](#),
[SECURITY_KEY_16](#), [SECURITY_KEY_17](#) }
Defines the security keys Implements : [security_key_id_t_Class](#).
- enum [security_boot_flavor_t](#) { [SECURITY_BOOT_STRICT](#) = 0U, [SECURITY_BOOT_SERIAL](#) = 1U, [SECURITY_BOOT_PARALLEL](#) = 2U, [SECURITY_BOOT_NOT_DEFINED](#) = 3U }
Defines the security boot flavor Implements : [security_boot_flavor_t_Class](#).
- enum [security_cmd_t](#) {
[SECURITY_CMD_ENC_ECB](#) = 1U, [SECURITY_CMD_ENC_CBC](#), [SECURITY_CMD_DEC_ECB](#), [SECURITY_CMD_DEC_CBC](#),
[SECURITY_CMD_GENERATE_MAC](#), [SECURITY_CMD_VERIFY_MAC](#), [SECURITY_CMD_LOAD_KEY](#),
[SECURITY_CMD_LOAD_PLAIN_KEY](#),
[SECURITY_CMD_EXPORT_RAM_KEY](#), [SECURITY_CMD_INIT_RNG](#), [SECURITY_CMD_EXTEND_SEED](#), [SECURITY_CMD_RND](#),
[SECURITY_CMD_RESERVED_1](#), [SECURITY_CMD_BOOT_FAILURE](#), [SECURITY_CMD_BOOT_OK](#), [SECURITY_CMD_GET_ID](#),
[SECURITY_CMD_BOOT_DEFINE](#), [SECURITY_CMD_DBG_CHAL](#), [SECURITY_CMD_DBG_AUTH](#), [SECURITY_CMD_RESERVED_2](#),
[SECURITY_CMD_RESERVED_3](#), [SECURITY_CMD_MP_COMPRESS](#) }
Defines the security command Implements : [security_cmd_t_Class](#).

Functions

- void [SECURITY_GetDefaultConfig](#) ([security_user_config_t](#) *config)
Initializes the configuration structure.
- status_t [SECURITY_Init](#) ([security_instance_t](#) instance, const [security_user_config_t](#) *config)
Initializes the SECURITY module.
- status_t [SECURITY_Deinit](#) ([security_instance_t](#) instance)
De-initializes the SECURITY module.
- status_t [SECURITY_EncryptEcbBlocking](#) ([security_instance_t](#) instance, [security_key_id_t](#) keyId, const uint8_t *plainText, uint32_t msgLen, uint8_t *cipherText, uint32_t timeout)
ECB Encryption.
- status_t [SECURITY_DecryptEcbBlocking](#) ([security_instance_t](#) instance, [security_key_id_t](#) keyId, const uint8_t *cipherText, uint32_t msgLen, uint8_t *plainText, uint32_t timeout)

ECB Decryption.

- status_t [SECURITY_EncryptCbcBlocking](#) (security_instance_t instance, security_key_id_t keyId, const uint8_t *plainText, uint32_t msgLen, const uint8_t *iv, uint8_t *cipherText, uint32_t timeout)

CBC Decryption.

- status_t [SECURITY_DecryptCbcBlocking](#) (security_instance_t instance, security_key_id_t keyId, const uint8_t *cipherText, uint32_t msgLen, const uint8_t *iv, uint8_t *plainText, uint32_t timeout)

CBC Decryption.

- status_t [SECURITY_GenerateMacBlocking](#) (security_instance_t instance, security_key_id_t keyId, const uint8_t *msg, uint64_t msgLen, uint8_t *cmac, uint32_t timeout)

MAC Generation.

- status_t [SECURITY_VerifyMacBlocking](#) (security_instance_t instance, security_key_id_t keyId, const uint8_t *msg, uint64_t msgLen, const uint8_t *mac, uint16_t macLen, bool *verifStatus, uint32_t timeout)

MAC Verification.

- status_t [SECURITY_LoadKey](#) (security_instance_t instance, security_key_id_t keyId, const uint8_t *m1, const uint8_t *m2, const uint8_t *m3, uint8_t *m4, uint8_t *m5, uint32_t timeout)

Load Key.

- status_t [SECURITY_LoadPlainKey](#) (security_instance_t instance, const uint8_t *plainKey, uint32_t timeout)

Load Plain Key.

- status_t [SECURITY_ExportRamKey](#) (security_instance_t instance, uint8_t *m1, uint8_t *m2, uint8_t *m3, uint8_t *m4, uint8_t *m5, uint32_t timeout)

Export RAM key.

- status_t [SECURITY_ExtendSeed](#) (security_instance_t instance, const uint8_t *entropy, uint32_t timeout)

Initialize Random Number Generator.

- status_t [SECURITY_InitRng](#) (security_instance_t instance, uint32_t timeout)

Initialize Random Number Generator.

- status_t [SECURITY_GenerateRnd](#) (security_instance_t instance, uint8_t *rnd, uint32_t timeout)

Generate RND.

- status_t [SECURITY_GetId](#) (security_instance_t instance, const uint8_t *challenge, uint8_t *uid, uint8_t *sreg, uint8_t *mac, uint32_t timeout)

Get ID.

- status_t [SECURITY_SecureBoot](#) (security_instance_t instance, uint32_t bootImageSize, const uint8_t *bootImagePtr, uint32_t timeout)

Secure boot.

- status_t [SECURITY_BootFailure](#) (security_instance_t instance, uint32_t timeout)

Boot Failure.

- status_t [SECURITY_BootOk](#) (security_instance_t instance, uint32_t timeout)

Boot Ok.

- status_t [SECURITY_BootDefine](#) (security_instance_t instance, uint32_t bootSize, security_boot_flavor_t bootFlavor, uint32_t timeout)

Boot Define.

- status_t [SECURITY_DbgChal](#) (security_instance_t instance, uint8_t *challenge, uint32_t timeout)

Debug Challenge.

- status_t [SECURITY_DbgAuth](#) (security_instance_t instance, const uint8_t *authorization, uint32_t timeout)

Debug Authentication.

- status_t [SECURITY_MPCompress](#) (security_instance_t instance, const uint8_t *msg, uint32_t msgLen, uint8_t *mpCompress, uint32_t timeout)

Miyaguchi-Prenell Compression.

- status_t [SECURITY_GenerateTrnd](#) (security_instance_t instance, uint8_t *trnd, uint32_t timeout)

Generate True Random Number.

- status_t [SECURITY_CancelCommand](#) (security_instance_t instance)

Cancel Command.

- status_t [SECURITY_GetAsyncCmdStatus](#) (security_instance_t instance)

Get asynchronous command status.

- status_t [SECURITY_EncryptEcb](#) ([security_instance_t](#) instance, [security_key_id_t](#) keyId, const uint8_t *plainText, uint32_t msgLen, uint8_t *cipherText)

Encrypt ECB.

- status_t [SECURITY_DecryptEcb](#) ([security_instance_t](#) instance, [security_key_id_t](#) keyId, const uint8_t *cipherText, uint32_t msgLen, uint8_t *plainText)

Decrypt ECB.

- status_t [SECURITY_EncryptCbc](#) ([security_instance_t](#) instance, [security_key_id_t](#) keyId, const uint8_t *plainText, uint32_t msgLen, const uint8_t *iv, uint8_t *cipherText)

Encrypt CBC.

- status_t [SECURITY_DecryptCbc](#) ([security_instance_t](#) instance, [security_key_id_t](#) keyId, const uint8_t *cipherText, uint32_t msgLen, const uint8_t *iv, uint8_t *plainText)

Decrypt CBC.

- status_t [SECURITY_GenerateMac](#) ([security_instance_t](#) instance, [security_key_id_t](#) keyId, const uint8_t *msg, uint64_t msgLen, uint8_t *cmac)

Generate MAC.

- status_t [SECURITY_VerifyMac](#) ([security_instance_t](#) instance, [security_key_id_t](#) keyId, const uint8_t *msg, uint64_t msgLen, const uint8_t *mac, uint16_t macLen, bool *verifStatus)

Verify MAC.

17.128.2 Data Structure Documentation

17.128.2.1 struct security_user_config_t

Define user configuration Implements : [security_user_config_t_Class](#).

Definition at line 155 of file [security_pal.h](#).

Data Fields

- security_callback_t [callback](#)
- void * [callbackParam](#)

Field Documentation

17.128.2.1.1 security_callback_t callback

The callback invoked when an asynchronous command is completed

Definition at line 157 of file [security_pal.h](#).

17.128.2.1.2 void* callbackParam

User parameter for the command completion callback

Definition at line 158 of file [security_pal.h](#).

17.128.3 Enumeration Type Documentation

17.128.3.1 enum security_boot_flavor_t

Defines the security boot flavor Implements : [security_boot_flavor_t_Class](#).

Enumerator

SECURITY_BOOT_STRICT

SECURITY_BOOT_SERIAL

SECURITY_BOOT_PARALLEL
SECURITY_BOOT_NOT_DEFINED

Definition at line 97 of file security_pal.h.

17.128.3.2 enum security_cmd_t

Defines the security command Implements : security_cmd_t_Class.

Enumerator

SECURITY_CMD_ENC_ECB
SECURITY_CMD_ENC_CBC
SECURITY_CMD_DEC_ECB
SECURITY_CMD_DEC_CBC
SECURITY_CMD_GENERATE_MAC
SECURITY_CMD_VERIFY_MAC
SECURITY_CMD_LOAD_KEY
SECURITY_CMD_LOAD_PLAIN_KEY
SECURITY_CMD_EXPORT_RAM_KEY
SECURITY_CMD_INIT_RNG
SECURITY_CMD_EXTEND_SEED
SECURITY_CMD_RND
SECURITY_CMD_RESERVED_1
SECURITY_CMD_BOOT_FAILURE
SECURITY_CMD_BOOT_OK
SECURITY_CMD_GET_ID
SECURITY_CMD_BOOT_DEFINE
SECURITY_CMD_DBG_CHAL
SECURITY_CMD_DBG_AUTH
SECURITY_CMD_RESERVED_2
SECURITY_CMD_RESERVED_3
SECURITY_CMD_MP_COMPRESS

Definition at line 109 of file security_pal.h.

17.128.3.3 enum security_instance_t

Define instances for SECURITY PAL Implements : security_instance_t_Class.

Enumerator

SECURITY_INSTANCE0

Definition at line 49 of file security_pal.h.

17.128.3.4 enum security_key_id_t

Defines the security keys Implements : security_key_id_t_Class.

Enumerator

SECURITY_SECRET_KEY

SECURITY_MASTER_ECU
SECURITY_BOOT_MAC_KEY
SECURITY_BOOT_MAC
SECURITY_KEY_1
SECURITY_KEY_2
SECURITY_KEY_3
SECURITY_KEY_4
SECURITY_KEY_5
SECURITY_KEY_6
SECURITY_KEY_7
SECURITY_KEY_8
SECURITY_KEY_9
SECURITY_KEY_10
SECURITY_RAM_KEY
SECURITY_KEY_11
SECURITY_KEY_12
SECURITY_KEY_13
SECURITY_KEY_14
SECURITY_KEY_15
SECURITY_KEY_16
SECURITY_KEY_17

Definition at line 58 of file security_pal.h.

17.128.4 Function Documentation

17.128.4.1 **status_t SECURITY_BootDefine (security_instance_t instance, uint32_t bootSize, security_boot_flavor_t bootFlavor, uint32_t timeout)**

Boot Define.

Implements an extension of the SHE standard to define both the user boot size and boot method.

Parameters

in	<i>instance</i>	security module instance
in	<i>bootSize</i>	Number of blocks of 128-bit data to check on boot. Maximum size is 512k↔ Bytes.
in	<i>bootFlavor</i>	The boot method.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS↔ S_TIMEOUT is returned.

Returns

Error Code after command execution. Unsupported code if function is not available.

Definition at line 695 of file security_pal.c.

17.128.4.2 **status_t SECURITY_BootFailure (security_instance_t instance, uint32_t timeout)**

Boot Failure.

Signals a failure detected during later stages of the boot process.

Parameters

in	<i>instance</i>	security module instance
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_TIMEOUT is returned.

Returns

Error Code after command execution.

Definition at line 641 of file security_pal.c.

17.128.4.3 status_t SECURITY_BootOk (security_instance_t instance, uint32_t timeout)

Boot Ok.

Marks a successful boot verification during later stages of the boot process.

Parameters

in	<i>instance</i>	security module instance
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_TIMEOUT is returned.

Returns

Error Code after command execution.

Definition at line 668 of file security_pal.c.

17.128.4.4 status_t SECURITY_CancelCommand (security_instance_t instance)

Cancel Command.

Cancels a previously initiated command.

Parameters

in	<i>instance</i>	security module instance
----	-----------------	--------------------------

Returns

STATUS_SUCCESS

Definition at line 844 of file security_pal.c.

17.128.4.5 status_t SECURITY_DbgAuth (security_instance_t instance, const uint8_t * authorization, uint32_t timeout)

Debug Authentication.

Erases all keys (actual and outdated) stored in NVM Memory if the authorization is confirmed.

Parameters

in	<i>instance</i>	security module instance
in	<i>authorization</i>	Pointer to the 128-bit buffer containing the authorization value.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_TIMEOUT is returned.

Returns

Error Code after command execution.

Definition at line 756 of file security_pal.c.

17.128.4.6 `status_t SECURITY_DbgChal (security_instance_t instance, uint8_t * challenge, uint32_t timeout)`

Debug Challenge.

Obtains a random number which the user shall use along with the MASTER_ECU_KEY and UID to return an authorization request.

Parameters

in	<i>instance</i>	security module instance
out	<i>challenge</i>	Pointer to the 128-bit buffer where the challenge data will be stored.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_↔S_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 728 of file security_pal.c.

17.128.4.7 `status_t SECURITY_DecryptCbc (security_instance_t instance, security_key_id_t keyId, const uint8_t * cipherText, uint32_t msgLen, const uint8_t * iv, uint8_t * plainText)`

Decrypt CBC.

Asynchronously performs the AES-128 decryption in CBC mode of the input cipher text buffer.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>cipherText</i>	Pointer to the cipher text buffer.
in	<i>msgLen</i>	Number of bytes of cipher text message to be decrypted. It should be multiple of 16 bytes.
in	<i>iv</i>	Pointer to the initialization vector buffer.
out	<i>plainText</i>	Pointer to the plain text buffer. The buffer shall have the same size as the cipher text buffer.

Returns

STATUS_BUSY if another command is in execution, otherwise STATUS_SUCCESS.

Definition at line 982 of file security_pal.c.

17.128.4.8 `status_t SECURITY_DecryptCbcBlocking (security_instance_t instance, security_key_id_t keyId, const uint8_t * cipherText, uint32_t msgLen, const uint8_t * iv, uint8_t * plainText, uint32_t timeout)`

CBC Decryption.

Perform AES-128 decryption in CBC mode of the input cipher text buffer.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID used to perform the cryptographic operation
in	<i>cipherText</i>	Pointer to the cipher text buffer.
in	<i>msgLen</i>	Number of bytes of plain text message to be encrypted. It is multiple of 16 bytes.

in	<i>iv</i>	Pointer to the initialization vector buffer.
out	<i>plainText</i>	Pointer to the plain text buffer. The buffer shall have the same size as the cipher text buffer.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_↵S_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 312 of file security_pal.c.

17.128.4.9 `status_t SECURITY_DecryptEcb (security_instance_t instance, security_key_id_t keyId, const uint8_t * cipherText, uint32_t msgLen, uint8_t * plainText)`

Decrypt ECB.

Asynchronously performs the AES-128 decryption in ECB mode of the input cipher text buffer.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>cipherText</i>	Pointer to the cipher text buffer.
in	<i>msgLen</i>	Number of bytes of cipher text message to be decrypted. It should be multiple of 16 bytes.
out	<i>plainText</i>	Pointer to the plain text buffer. The buffer shall have the same size as the cipher text buffer.

Returns

STATUS_BUSY if another command is in execution, otherwise STATUS_SUCCESS.

Definition at line 923 of file security_pal.c.

17.128.4.10 `status_t SECURITY_DecryptEcbBlocking (security_instance_t instance, security_key_id_t keyId, const uint8_t * cipherText, uint32_t msgLen, uint8_t * plainText, uint32_t timeout)`

ECB Decryption.

Perform AES-128 decryption in ECB mode of the input cipher text buffer.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID used to perform the cryptographic operation
in	<i>cipherText</i>	Pointer to the cipher text buffer.
in	<i>msgLen</i>	Number of bytes of plain text message to be encrypted. It is multiple of 16 bytes.
out	<i>plainText</i>	Pointer to the plain text buffer. The buffer shall have the same size as the cipher text buffer.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_↵S_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 251 of file security_pal.c.

17.128.4.11 `status_t SECURITY_Deinit (security_instance_t instance)`

De-initializes the SECURITY module.

This function de-initializes the requested SECURITY instance.

Parameters

in	<i>instance</i>	security module instance
----	-----------------	--------------------------

Returns

Error or success status returned by API

Definition at line 188 of file security_pal.c.

17.128.4.12 `status_t SECURITY_EncryptCbc (security_instance_t instance, security_key_id_t keyId, const uint8_t * plainText, uint32_t msgLen, const uint8_t * iv, uint8_t * cipherText)`

Encrypt CBC.

Asynchronously performs the AES-128 encryption in CBC mode of the input plain text buffer.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>plainText</i>	Pointer to the plain text buffer.
in	<i>msgLen</i>	Number of bytes of plain text message to be encrypted. It should be multiple of 16 bytes.
in	<i>iv</i>	Pointer to the initialization vector buffer.
out	<i>cipherText</i>	Pointer to the cipher text buffer. The buffer shall have the same size as the plain text buffer.

Returns

STATUS_BUSY if another command is in execution, otherwise STATUS_SUCCESS.

Definition at line 952 of file security_pal.c.

17.128.4.13 `status_t SECURITY_EncryptCbcBlocking (security_instance_t instance, security_key_id_t keyId, const uint8_t * plainText, uint32_t msgLen, const uint8_t * iv, uint8_t * cipherText, uint32_t timeout)`

CBC Decryption.

Perform AES-128 decryption in CBC mode of the input cipher text buffer.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID used to perform the cryptographic operation
in	<i>plainText</i>	Pointer to the plain text buffer. The buffer shall have the same size as the cipher text buffer.
in	<i>msgLen</i>	Number of bytes of plain text message to be encrypted. It is multiple of 16 bytes.
in	<i>iv</i>	Pointer to the initialization vector buffer.
out	<i>cipherText</i>	Pointer to the cipher text buffer.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 281 of file security_pal.c.

17.128.4.14 `status_t SECURITY_EncryptEcb (security_instance_t instance, security_key_id_t keyId, const uint8_t * plainText, uint32_t msgLen, uint8_t * cipherText)`

Encrypt ECB.

Asynchronously performs the AES-128 encryption in ECB mode of the input plain text buffer.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>plainText</i>	Pointer to the plain text buffer.
in	<i>msgLen</i>	Number of bytes of plain text message to be encrypted. It should be multiple of 16 bytes.
out	<i>cipherText</i>	Pointer to the cipher text buffer. The buffer shall have the same size as the plain text buffer.

Returns

STATUS_BUSY if another command is in execution, otherwise STATUS_SUCCESS.

Definition at line 894 of file security_pal.c.

17.128.4.15 `status_t SECURITY_EncryptEcbBlocking (security_instance_t instance, security_key_id_t keyId, const uint8_t * plainText, uint32_t msgLen, uint8_t * cipherText, uint32_t timeout)`

ECB Encryption.

Perform AES-128 encryption in ECB mode of the input plain text buffer.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID used to perform the cryptographic operation
in	<i>plainText</i>	Pointer to the plain text buffer
in	<i>msgLen</i>	Number of bytes of plain text message to be encrypted. It is multiple of 16 bytes.
out	<i>cipherText</i>	Pointer to the cipher text buffer. The buffer shall have the same size as the plain text buffer.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_S_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 221 of file security_pal.c.

17.128.4.16 `status_t SECURITY_ExportRamKey (security_instance_t instance, uint8_t * m1, uint8_t * m2, uint8_t * m3, uint8_t * m4, uint8_t * m5, uint32_t timeout)`

Export RAM key.

Exports the RAM_KEY into a format protected by SECRET_KEY.

Parameters

in	<i>instance</i>	security module instance
----	-----------------	--------------------------

out	<i>m1</i>	Pointer to a buffer where the M1 parameter will be exported.
out	<i>m2</i>	Pointer to a buffer where the M2 parameter will be exported.
out	<i>m3</i>	Pointer to a buffer where the M3 parameter will be exported.
out	<i>m4</i>	Pointer to a buffer where the M4 parameter will be exported.
out	<i>m5</i>	Pointer to a buffer where the M5 parameter will be exported.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_↵S_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 467 of file security_pal.c.

17.128.4.17 `status_t SECURITY_ExtendSeed (security_instance_t instance, const uint8_t * entropy, uint32_t timeout)`

Initialize Random Number Generator.

Extends the seed of the PRNG by compressing the former seed value and the supplied entropy into a new seed. This new seed is then to be used to generate a random number by invoking the CMD_RND command. The random number generator must be initialized by CMD_INIT_RNG before the seed may be extended.

Parameters

in	<i>instance</i>	security module instance
in	<i>entropy</i>	pointer to a 128-bit buffer containing the entropy.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_↵S_TIMEOUT is returned.

Returns

Error Code after command execution.

Definition at line 498 of file security_pal.c.

17.128.4.18 `status_t SECURITY_GenerateMac (security_instance_t instance, security_key_id_t keyId, const uint8_t * msg, uint64_t msgLen, uint8_t * cmac)`

Generate MAC.

Asynchronously calculates the MAC of a given message using CMAC with AES-128.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>msg</i>	Pointer to the message buffer.
in	<i>msgLen</i>	Number of bits of message on which CMAC will be computed.
out	<i>cmac</i>	Pointer to the buffer containing the result of the CMAC computation.

Returns

STATUS_BUSY if another command is in execution, otherwise STATUS_SUCCESS.

Definition at line 1012 of file security_pal.c.

17.128.4.19 `status_t SECURITY_GenerateMacBlocking (security_instance_t instance, security_key_id_t keyId, const uint8_t * msg, uint64_t msgLen, uint8_t * cmac, uint32_t timeout)`

MAC Generation.

Calculates MAC of a given message using CMAC with AES-128.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>msg</i>	Pointer to the message buffer.
in	<i>msgLen</i>	Number of bits of message on which CMAC will be computed.
out	<i>cmac</i>	Pointer to the buffer containing the result of the CMAC computation.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_↵S_TIMEOUT is returned.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_↵S_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 342 of file security_pal.c.

17.128.4.20 `status_t SECURITY_GenerateRnd (security_instance_t instance, uint8_t * rnd, uint32_t timeout)`

Generate RND.

Generates a vector of 128 random bits.

Parameters

in	<i>instance</i>	security module instance
out	<i>rnd</i>	Pointer to a 128-bit buffer where the generated random number has to be stored.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_↵S_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 551 of file security_pal.c.

17.128.4.21 `status_t SECURITY_GenerateTrnd (security_instance_t instance, uint8_t * trnd, uint32_t timeout)`

Generate True Random Number.

Generates a vector of 128 random bits using TRNG.

Parameters

in	<i>instance</i>	security module instance
out	<i>trnd</i>	Pointer to a 128-bit buffer where the generated random number is stored.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_↵S_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.
Unsupported code if function is not available.

Definition at line 816 of file security_pal.c.

17.128.4.22 `status_t SECURITY_GetAsyncCmdStatus (security_instance_t instance)`

Get asynchronous command status.

Checks the status of the execution of an asynchronous command.

Parameters

in	<i>instance</i>	security module instance
----	-----------------	--------------------------

Returns

Error Code after command execution; STATUS_BUSY if a command is still in progress.

Definition at line 869 of file security_pal.c.

17.128.4.23 void SECURITY_GetDefaultConfig (security_user_config_t * config)

Initializes the configuration structure.

This function initializes the configuration struct members to default values.

Parameters

out	<i>config</i>	configuration struct pointer
-----	---------------	------------------------------

Definition at line 126 of file security_pal.c.

17.128.4.24 status_t SECURITY_GetId (security_instance_t instance, const uint8_t * challenge, uint8_t * uid, uint8_t * sreg, uint8_t * mac, uint32_t timeout)

Get ID.

Returns the identity (UID) and the value of the status register protected by a MAC over a challenge and the data.

Parameters

in	<i>instance</i>	security module instance
in	<i>challenge</i>	Pointer to the 128-bit buffer containing Challenge data.
out	<i>uid</i>	Pointer to 120 bit buffer where the UID will be stored.
out	<i>sreg</i>	Value of the status register.
out	<i>mac</i>	Pointer to the 128 bit buffer where the MAC generated over challenge and UID and status will be stored.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_S_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 579 of file security_pal.c.

17.128.4.25 status_t SECURITY_Init (security_instance_t instance, const security_user_config_t * config)

Initializes the SECURITY module.

This function initializes and enables the requested SECURITY instance.

Parameters

in	<i>instance</i>	security module instance
in	<i>config</i>	pointer to security module configuration structure

Returns

Error or success status returned by API

Definition at line 141 of file security_pal.c.

17.128.4.26 `status_t SECURITY_InitRng (security_instance_t instance, uint32_t timeout)`

Initialize Random Number Generator.

Initializes the seed and derive a key for the PRNG.

Parameters

in	<i>instance</i>	security module instance
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_TIMEOUT is returned.

Returns

Error Code after command execution.

Definition at line 525 of file security_pal.c.

17.128.4.27 `status_t SECURITY_LoadKey (security_instance_t instance, security_key_id_t keyId, const uint8_t * m1, const uint8_t * m2, const uint8_t * m3, uint8_t * m4, uint8_t * m5, uint32_t timeout)`

Load Key.

Updates an internal key per the SHE specification.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID of the key to be updated.
in	<i>m1</i>	Pointer to the 128-bit M1 message containing the UID, Key ID and Authentication Key ID.
in	<i>m2</i>	Pointer to the 256-bit M2 message contains the new security flags, counter and the key value all encrypted using a derived key generated from the Authentication Key.
in	<i>m3</i>	Pointer to the 128-bit M3 message is a MAC generated over messages M1 and M2.
out	<i>m4</i>	Pointer to a 256 bits buffer where the computed M4 parameter is stored.
out	<i>m5</i>	Pointer to a 128 bits buffer where the computed M5 parameter is stored.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 408 of file security_pal.c.

17.128.4.28 `status_t SECURITY_LoadPlainKey (security_instance_t instance, const uint8_t * plainKey, uint32_t timeout)`

Load Plain Key.

Updates the RAM key memory slot with a 128-bit plaintext.

Parameters

in	<i>instance</i>	security module instance
in	<i>plainKey</i>	Pointer to the 128-bit buffer containing the key that needs to be copied in RAM_KEY slot.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_TIMEOUT is returned.

Returns

Error Code after command execution.

Definition at line 440 of file security_pal.c.

17.128.4.29 **status_t SECURITY_MPCompress (security_instance_t instance, const uint8_t * msg, uint32_t msgLen, uint8_t * mpCompress, uint32_t timeout)**

Miyaguchi-Prenell Compression.

Compresses the given messages by accessing the Miyaguchi-Prenell compression feature with in the CSEc feature set.

Parameters

in	<i>instance</i>	security module instance
in	<i>msg</i>	Pointer to the messages to be compressed. Messages must be pre-processed per SHE specification if they do not already meet the full 128-bit block size requirement.
in	<i>msgLen</i>	The number of 128 bit messages to be compressed.
out	<i>mpCompress</i>	Pointer to the 128 bit buffer storing the compressed data.
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_S_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 785 of file security_pal.c.

17.128.4.30 **status_t SECURITY_SecureBoot (security_instance_t instance, uint32_t bootImageSize, const uint8_t * bootImagePtr, uint32_t timeout)**

Secure boot.

The function loads the command processor firmware and memory slot data and then executes the SHE secure boot protocol.

Parameters

in	<i>instance</i>	security module instance
in	<i>bootImageSize</i>	Boot image size (in bytes).
in	<i>bootImagePtr</i>	Boot image start address.

Note

Address passed in this parameter must be 32 bit aligned.

Parameters

in	<i>timeout</i>	Timeout in ms; the function returns STATUS_TIMEOUT if the command is not finished in the allocated period.
----	----------------	--

Returns

Error Code after command execution.

Definition at line 610 of file security_pal.c.

17.128.4.31 **status_t SECURITY_VerifyMac (security_instance_t instance, security_key_id_t keyId, const uint8_t * msg, uint64_t msgLen, const uint8_t * mac, uint16_t macLen, bool * verifStatus)**

Verify MAC.

Asynchronously verifies the MAC of a given message using CMAC with AES-128.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>msg</i>	Pointer to the message buffer.
in	<i>msgLen</i>	Number of bits of message on which CMAC will be computed.
in	<i>mac</i>	Pointer to the buffer containing the CMAC to be verified.
in	<i>macLen</i>	Number of bits of the CMAC to be compared. A macLength value of zero indicates that all 128-bits are compared.
out	<i>verifStatus</i>	Status of MAC verification command (true: verification operation passed, false: verification operation failed).

Returns

STATUS_BUSY if another command is in execution, otherwise STATUS_SUCCESS.

Definition at line 1044 of file security_pal.c.

17.128.4.32 `status_t SECURITY_VerifyMacBlocking (security_instance_t instance, security_key_id_t keyId, const uint8_t * msg, uint64_t msgLen, const uint8_t * mac, uint16_t macLen, bool * verifStatus, uint32_t timeout)`

MAC Verification.

Verifies the MAC of a given message using CMAC with AES-128.

Parameters

in	<i>instance</i>	security module instance
in	<i>keyId</i>	KeyID used to perform the cryptographic operation.
in	<i>msg</i>	Pointer to the message buffer.
in	<i>msgLen</i>	Number of bits of message on which CMAC will be computed.
in	<i>mac</i>	Pointer to the buffer containing the CMAC to be verified.
in	<i>macLen</i>	Number of bits of the CMAC to be compared. A macLength value of zero indicates that all 128-bits are compared.
out	<i>verifStatus</i>	Status of MAC verification command (true: verification operation passed, false: verification operation failed).
in	<i>timeout</i>	Specifies the maximum time allowed for command completion, else STATUS_TIMEOUT is returned.

Returns

Error Code after command execution. Output parameters are valid if the error code is STATUS_SUCCESS.

Definition at line 374 of file security_pal.c.

17.129 Security Peripheral Abstraction Layer - SECURITY PAL

17.129.1 Detailed Description

The SECURITY PAL provides security features over specific modules like:

- > Cryptographic Services Engine (CSEc)
- > Hardware Security Module (HSM)

Features

- Secure cryptographic key storage
- AES-128 encryption and decryption
- AES-128 CMAC (Cipher-based Message Authentication Code) calculation and authentication
- ECB (Electronic Cypher Book) Mode - encryption and decryption
- CBC (Cipher Block Chaining) Mode - encryption and decryption
- True and Pseudo random number generation
- Miyaguchi-Prenell compression function
- Secure Boot Mode (user configurable)

How to use the SECURITY PAL in your application

The SECURITY PAL is designed to be used in conjunction with CSEc driver or HSM driver, based on hardware platform. The SECURITY PAL can't be used simultaneously over different driver types.

The following table contains the matching between platforms and available IPs:

IP/↔ MCU	S32↔ K116	S32↔ K118	S32↔ K142	S32↔ K144	S32↔ K142↔ W	S32↔ K144↔ W	S32↔ K146	S32↔ K148	S32↔ MTV	MP↔ C5746↔ C	MP↔ C5748↔ G
CS↔ EC	YES	YES	YES	YES	YES	YES	YES	YES	YES	NO	NO
HSM	NO	NO	NO	NO	NO	NO	NO	NO	NO	YES	YES

The SECURITY PAL includes file security_pal_cfg.h, which allows the user to specify which IP is used and how many resources are allocated (state structure). The following code example shows how to configure one instance for one available security module.

```
#ifndef SECURITY_PAL_CFG_H
#define SECURITY_PAL_CFG_H

/* Define which IP instance will be used in current project */
#define SECURITY_OVER_CSEC
#define NO_OF_CSEC_INSTS_FOR_SECURITY 1

#endif /* SECURITY_PAL_CFG_H */
```

In order to use the SECURITY modules, the initialization procedure must be completed. Using the [SECURITY_Init\(\)](#) function, the instance of the module is selected and configured using the user configuration structure.

The security features are available in two types: blocking and non-blocking. The blocking features have specified in their naming the 'blocking' attribute. All other functions are considered to be non-blocking. The blocking functions use the osif layer, providing timeout feature.

Important Notes

- For advanced usage, user must verify the specific drivers documentation for CSEc or HSM.
- The SECURITY PAL enables the interrupts for the corresponding module. The application must configure the interrupts priorities.

- The SECURITY PAL API offers a "timeout" parameter for a number of functions. If "timeout" value is set to value '0', the returned status shall not be assumed as "STATUS_TIMEOUT". This behaviour is given by the response time of the OS system tick and the execution time of the called function. Example: If OS system tick is set to 1ms, then the response time for a timeout set to '0', is between 0ms and 0.99ms. If the execution time of the function is 10us, then there is a high probability that the returned status shall be "STATUS_SUCCESS".

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\pal\src\security\security_pal.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc
${S32SDK_PATH}\platform\pal\inc
${S32SDK_PATH}\rtos\osif
```

Compile symbols

No special symbols are required for this component

Dependencies

Clock Manager Interrupt Manager (Interrupt) OS Interface (OSIF)

Example code

```
static security_user_config_t g_SecurityUserConfig;

void SecurityCallback(uint32_t completedCmd, void *callbackParam)
{
    security_cmd_t securityCmd = (security_cmd_t)completedCmd;
    switch (securityCmd)
    {
        case SECURITY_CMD_ENC_ECB:
            /* Do something... */
            break;
        default:
            /* Error... */
            break;
    }
}

void main()
{
    static status_t status = STATUS_SUCCESS;
    static uint8_t rndBuf[16];

    g_SecurityUserConfig.callback = SecurityCallback;

    status = SECURITY_Init(SECURITY_INSTANCE0, &g_SecurityUserConfig);
    if(status != STATUS_SUCCESS)
    {
        /* Error... */
    }
    status = SECURITY_InitRng(SECURITY_INSTANCE0, TIMEOUT);
    if(status != STATUS_SUCCESS)
    {
        /* Error... */
    }
    status = SECURITY_GenerateRnd(SECURITY_INSTANCE0, rndBuf, TIMEOUT);
    if(status != STATUS_SUCCESS)
    {
        /* Error... */
    }

    while(1);
}
```

Modules

- [Security PAL](#)

Security Peripheral Abstraction Layer.

17.130 Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL)

17.130.1 Detailed Description

Serial Peripheral Interface - Peripheral Abstraction Layer.

The SPI PAL driver allows communication on an SPI bus. It was designed to be portable across all platforms and IPs which support SPI communication.

How to integrate DSPI in your application

Unlike the other drivers, SPI PAL modules need to include a configuration file named `spi_pal_cfg.h`, which allows the user to specify which IPs are used and how many resources are allocated for each of them (state structures). The following code example shows how to configure one instance for each available SPI IPs.

```
#ifndef SPI_PAL_cfg_H
#define SPI_PAL_cfg_H

/* Define which IP instance will be used in current project */
#define SPI_OVER_LPSP
#define SPI_OVER_FLEXIO
#define SPI_OVER_DSPI

/* Define the resources necessary for current project */
#define NO_OF_LPSP_INSTS_FOR_SPI 1U
#define NO_OF_FLEXIO_INSTS_FOR_SPI 1U
#define NO_OF_DSPI_INSTS_FOR_SPI 1U
#endif /* SPI_PAL_cfg_H */
```

The following table contains the matching between platforms and available IPs

IP/ M CU	S32 K118	S32 K116	S32 K142	S32 K144	S32 K146	S32 K148	S32 K142 W	S32 K144 W	M P C5748 G	M P C5746 C	M P C5744 P	S32 R274	S32 R372
FL E XIO	Y ES	Y ES	Y ES	Y ES	Y ES	Y ES	Y ES	Y ES	NO	NO	NO	NO	NO
LP S PI	Y ES	Y ES	Y ES	Y ES	Y ES	Y ES	Y ES	Y ES	NO	NO	NO	NO	NO
D S PI/ S PI	NO	NO	NO	NO	NO	NO	NO	NO	Y ES	Y ES	Y ES	Y ES	Y ES

In order to use the SPI driver it must be first initialized in either master or slave mode, using functions [SPI_MasterInit\(\)](#) or [SPI_SlaveInit\(\)](#). Once initialized, it cannot be initialized again for the same SPI module instance until it is de-initialized, using [SPI_SlaveDeinit\(\)](#) or [SPI_MasterDeinit\(\)](#). Different SPI module instances can work independently of each other.

In each mode (master/slave) are available two types of transfers: blocking and non-blocking. The functions which initiate blocking transfers will configure the time out for transmission. If time expires [SPI_MasterTransferBlocking\(\)](#) or [SPI_SlaveTransferBlocking\(\)](#) will return error and the transmission will be aborted.

The configuration structure includes a special field named extension. It will be used only for SPI transfers over FLEXIO and should contain a pointer to [extension_flexio_for_spi_t](#) structure. The purpose of this structure is to configure which FLEXIO pins are used by the applications and their functionality (MISO, MOSI, SCK, SS). One FLEXIO hardware instance can implements spi, so if instType is SPI_INST_TYPE_FLEXIO instIdx can be 0 or 1.

If device name is from MPC574xP and S32Rx7x families it can't be used as master in DMA mode and PAL will automatically switch the functionality to interrupt mode. If DMA mode is mandatory please use DSPI driver.

Important Notes

- The driver enables the interrupts for the corresponding module, but any interrupt priority setting must be done by the application.

Example code

```

/* Configure SPI master */
spi_master_t spi0_MasterConfig0 =
{
    .baudRate      = 100000,
    .ssPolarity    = SPI_ACTIVE_HIGH,
    .frameSize     = 8,
    .clockPhase    = READ_ON_ODD_EDGE,
    .clockPolarity = SPI_ACTIVE_HIGH,
    .bitOrder      = SPI_TRANSFER_MSB_FIRST,
    .transferType  = SPI_USING_INTERRUPTS,
    .rxDMAChannel  = 255,
    .txDMAChannel  = 255,
    .callback      = NULL,
    .callbackParam = NULL,
    .ssPin         = 0,
    .extension     = NULL
};

/* Configure FLEXIO pins routing */
extension_flexio_for_spi_t extension;
extension.misoPin = 0;
extension.mosiPin = 1;
extension.sckPin = 2;
extension.ssPin = 3;
spi0_MasterConfig0.extension = &extension;

/* Configure instances used in this example */
spi_instance_t lpspiInstance, flexioInstance;
lpspiInstance.instIdx = 0U;
lpspiInstance.instType = SPI_INST_TYPE_LPSPI;
flexioInstance.instIdx = 1U;
lpspiInstance.instType = SPI_INST_TYPE_FLEXIO;

/* Buffers */
uint8_t tx[5] = {1,2,3,4,5};
uint8_t rx[5];

/* Initializes SPI master for LPSPI 0 and send 5 frames */
SPI_MasterInit(&lpspiInstance, &spi0_MasterConfig0);
SPI_MasterTransfer(&lpspiInstance, tx, rx, 5);
/* Initializes SPI master for FLEXIO 0 and send 5 frames */
SPI_MasterInit(&flexioInstance, &spi1_MasterConfig0);
SPI_MasterTransfer(&flexioInstance, tx, rx, 5);

```

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\pal\src\spi\spi_pal.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\pal\inc
spi_pal_cfg.h path
```

Compile symbols

No special symbols are required for this component

Dependencies

Low Power Serial Peripheral Interface (LPSPI) flexio_spi Clock Manager OS Interface (OSIF) Interrupt Manager (Interrupt) Enhanced Direct Memory Access (eDMA)

Data Structures

- struct [spi_master_t](#)
Defines the configuration structure for SPI master Implements : [spi_master_t_Class](#). [More...](#)
- struct [spi_slave_t](#)
Defines the configuration structure for SPI slave Implements : [spi_slave_t_Class](#). [More...](#)
- struct [extension_flexio_for_spi_t](#)
Defines the extension structure for the SPI over FLEXIO Implements : [extension_flexio_for_spi_t_Class](#). [More...](#)

Enumerations

- enum [spi_transfer_type_t](#) { [SPI_USING_DMA](#) = 0U, [SPI_USING_INTERRUPTS](#) = 1U }
Defines the mechanism to update the rx or tx buffers Implements : [spi_transfer_type_t_Class](#).
- enum [spi_polarity_t](#) { [SPI_ACTIVE_HIGH](#) = 0U, [SPI_ACTIVE_LOW](#) = 1U }
Defines the polarity of signals Implements : [spi_polarity_t_Class](#).
- enum [spi_clock_phase_t](#) { [READ_ON_ODD_EDGE](#) = 0U, [READ_ON_EVEN_EDGE](#) = 1U }
Defines the edges used for sampling and shifting Implements : [spi_clock_phase_t_Class](#).
- enum [spi_transfer_bit_order_t](#) { [SPI_TRANSFER_MSB_FIRST](#) = 0U, [SPI_TRANSFER_LSB_FIRST](#) = 1U }
Defines the bit order Implements : [spi_transfer_bit_order_t_Class](#).

Functions

- status_t [SPI_MasterInit](#) (const [spi_instance_t](#) *const instance, const [spi_master_t](#) *config)
Initializes the SPI module in master mode.
- status_t [SPI_Slavelnit](#) (const [spi_instance_t](#) *const instance, const [spi_slave_t](#) *config)
Initializes the SPI module in slave mode.
- status_t [SPI_SetSS](#) (const [spi_instance_t](#) *const instance, uint8_t ss)
Update the SS.
- status_t [SPI_MasterTransfer](#) (const [spi_instance_t](#) *const instance, const void *txBuffer, void *rxBuffer, uint16_t numberOfFrames)
Initializes a non-blocking master transfer.
- status_t [SPI_MasterTransferBlocking](#) (const [spi_instance_t](#) *const instance, const void *txBuffer, void *rxBuffer, uint16_t numberOfFrames, uint16_t timeout)
Initializes a blocking master transfer.
- status_t [SPI_SlaveTransfer](#) (const [spi_instance_t](#) *const instance, const void *txBuffer, void *rxBuffer, uint16_t numberOfFrames)
Initializes a non-blocking slave transfer.
- status_t [SPI_SlaveTransferBlocking](#) (const [spi_instance_t](#) *const instance, const void *txBuffer, void *rxBuffer, uint16_t numberOfFrames, uint16_t timeout)
Initializes a blocking slave transfer.
- status_t [SPI_GetStatus](#) (const [spi_instance_t](#) *const instance)
Gets the status of the last transfer.
- status_t [SPI_GetDefaultMasterConfig](#) ([spi_master_t](#) *config)
Gets the default configuration structure for master.
- status_t [SPI_GetDefaultSlaveConfig](#) ([spi_slave_t](#) *config)
Gets the default configuration structure for slave.
- status_t [SPI_MasterDeinit](#) (const [spi_instance_t](#) *const instance)
De-initializes the spi master module.
- status_t [SPI_SlaveDeinit](#) (const [spi_instance_t](#) *const instance)
De-initializes the spi slave module.
- status_t [SPI_MasterSetDelay](#) (const [spi_instance_t](#) *const instance, uint32_t delayBetweenTransfers, uint32_t delaySCKtoPCS, uint32_t delayPCStoSCK)
Configures the SPI_PAL master mode bus timing delay options.

17.130.2 Data Structure Documentation

17.130.2.1 struct spi_master_t

Defines the configuration structure for SPI master Implements : spi_master_t_Class.

Definition at line 82 of file spi_pal.h.

Data Fields

- uint32_t [baudRate](#)
- uint8_t [frameSize](#)
- [spi_transfer_bit_order_t](#) [bitOrder](#)
- [spi_polarity_t](#) [clockPolarity](#)
- [spi_polarity_t](#) [ssPolarity](#)
- [spi_clock_phase_t](#) [clockPhase](#)
- uint8_t [ssPin](#)
- [spi_transfer_type_t](#) [transferType](#)
- uint8_t [rxDMAChannel](#)
- uint8_t [txDMAChannel](#)
- [spi_callback_t](#) [callback](#)
- void * [callbackParam](#)
- void * [extension](#)

Field Documentation

17.130.2.1.1 uint32_t baudRate

Clock frequency

Definition at line 84 of file spi_pal.h.

17.130.2.1.2 spi_transfer_bit_order_t bitOrder

Select if first bit is MSB or LSB

Definition at line 86 of file spi_pal.h.

17.130.2.1.3 spi_callback_t callback

Select the callback to transfer complete

Definition at line 94 of file spi_pal.h.

17.130.2.1.4 void* callbackParam

Select additional callback parameters if it's necessary

Definition at line 95 of file spi_pal.h.

17.130.2.1.5 spi_clock_phase_t clockPhase

Select clock edges for sampling and shifting

Definition at line 89 of file spi_pal.h.

17.130.2.1.6 spi_polarity_t clockPolarity

Select polarity for Clock

Definition at line 87 of file spi_pal.h.

17.130.2.1.7 void* extension

This field will be used to add extra settings to the basic configuration like FlexIO pins

Definition at line 96 of file spi_pal.h.

17.130.2.1.8 uint8_t frameSize

Size of frame in bits

Definition at line 85 of file spi_pal.h.

17.130.2.1.9 uint8_t rxDMAChannel

Channel number for DMA rx channel

Definition at line 92 of file spi_pal.h.

17.130.2.1.10 uint8_t ssPin

Select which SS is used

Definition at line 90 of file spi_pal.h.

17.130.2.1.11 spi_polarity_t ssPolarity

Select polarity for SS

Definition at line 88 of file spi_pal.h.

17.130.2.1.12 spi_transfer_type_t transferType

Select if buffers are managed by internal interrupt handler or by DMA

Definition at line 91 of file spi_pal.h.

17.130.2.1.13 uint8_t txDMAChannel

Channel number for DMA tx channel

Definition at line 93 of file spi_pal.h.

17.130.2.2 struct spi_slave_t

Defines the configuration structure for SPI slave Implements : spi_slave_t_Class.

Definition at line 103 of file spi_pal.h.

Data Fields

- [uint8_t frameSize](#)
- [spi_transfer_bit_order_t bitOrder](#)
- [spi_polarity_t clockPolarity](#)
- [spi_polarity_t ssPolarity](#)
- [spi_clock_phase_t clockPhase](#)
- [spi_transfer_type_t transferType](#)
- [uint8_t rxDMAChannel](#)
- [uint8_t txDMAChannel](#)
- [spi_callback_t callback](#)
- void * [callbackParam](#)
- void * [extension](#)

Field Documentation

17.130.2.2.1 spi_transfer_bit_order_t bitOrder

Select if first bit is MSB or LSB

Definition at line 106 of file spi_pal.h.

17.130.2.2.2 spi_callback_t callback

Select the callback to transfer complete

Definition at line 113 of file spi_pal.h.

17.130.2.2.3 void* callbackParam

Select additional callback parameters if it's necessary

Definition at line 114 of file spi_pal.h.

17.130.2.2.4 spi_clock_phase_t clockPhase

Select clock edges for sampling and shifting

Definition at line 109 of file spi_pal.h.

17.130.2.2.5 spi_polarity_t clockPolarity

Select polarity for Clock

Definition at line 107 of file spi_pal.h.

17.130.2.2.6 void* extension

This field will be used to add extra settings to the basic configuration like FlexIO

Definition at line 115 of file spi_pal.h.

17.130.2.2.7 uint8_t frameSize

Size of frame in bits

Definition at line 105 of file spi_pal.h.

17.130.2.2.8 uint8_t rxDMAChannel

Channel number for DMA rx channel

Definition at line 111 of file spi_pal.h.

17.130.2.2.9 spi_polarity_t ssPolarity

Select polarity for SS

Definition at line 108 of file spi_pal.h.

17.130.2.2.10 spi_transfer_type_t transferType

Select if buffers are managed by internal interrupt handler or by DMA

Definition at line 110 of file spi_pal.h.

17.130.2.2.11 uint8_t txDMAChannel

Channel number for DMA tx channel

Definition at line 112 of file spi_pal.h.

17.130.2.3 struct extension_flexio_for_spi_t

Defines the extension structure for the SPI over FLEXIO Implements : extension_flexio_for_spi_t_Class.

Definition at line 123 of file spi_pal.h.

Data Fields

- uint8_t [mosiPin](#)
- uint8_t [misoPin](#)
- uint8_t [sckPin](#)
- uint8_t [ssPin](#)

Field Documentation

17.130.2.3.1 uint8_t misoPin

FlexIO pin for MISO

Definition at line 126 of file spi_pal.h.

17.130.2.3.2 uint8_t mosiPin

FlexIO pin for MOSI

Definition at line 125 of file spi_pal.h.

17.130.2.3.3 uint8_t sckPin

FlexIO pin for SCK

Definition at line 127 of file spi_pal.h.

17.130.2.3.4 uint8_t ssPin

FlexIO pin for SS

Definition at line 128 of file spi_pal.h.

17.130.3 Enumeration Type Documentation

17.130.3.1 enum spi_clock_phase_t

Defines the edges used for sampling and shifting Implements : spi_clock_phase_t_Class.

Enumerator

READ_ON_ODD_EDGE The SPI signal is read on odd edges of SCK and counting starts after SS activation

READ_ON_EVEN_EDGE The SPI signal is read on even edges of SCK and counting starts after SS activation

Definition at line 61 of file spi_pal.h.

17.130.3.2 enum spi_polarity_t

Defines the polarity of signals Implements : spi_polarity_t_Class.

Enumerator

SPI_ACTIVE_HIGH The signal is active high

SPI_ACTIVE_LOW The signal is active low

Definition at line 51 of file spi_pal.h.

17.130.3.3 enum spi_transfer_bit_order_t

Defines the bit order Implements : spi_transfer_bit_order_t_Class.

Enumerator

SPI_TRANSFER_MSB_FIRST Transmit data starting with most significant bit

SPI_TRANSFER_LSB_FIRST Transmit data starting with least significant bit

Definition at line 71 of file spi_pal.h.

17.130.3.4 enum spi_transfer_type_t

Defines the mechanism to update the rx or tx buffers Implements : spi_transfer_type_t_Class.

Enumerator

SPI_USING_DMA The driver will use DMA to perform SPI transfer

SPI_USING_INTERRUPTS The driver will use interrupts to perform SPI transfer

Definition at line 41 of file spi_pal.h.

17.130.4 Function Documentation

17.130.4.1 status_t SPI_GetDefaultMasterConfig (spi_master_t * config)

Gets the default configuration structure for master.

The default configuration structure is:

Parameters

out	config	Pointer to configuration structure
-----	--------	------------------------------------

Returns

Error or success status returned by API

Definition at line 734 of file spi_pal.c.

17.130.4.2 status_t SPI_GetDefaultSlaveConfig (spi_slave_t * config)

Gets the default configuration structure for slave.

The default configuration structure is:

Parameters

out	config	Pointer to configuration structure
-----	--------	------------------------------------

Returns

Error or success status returned by API

Definition at line 759 of file spi_pal.c.

17.130.4.3 status_t SPI_GetStatus (const spi_instance_t * const instance)

Gets the status of the last transfer.

This function return the status of the last transfer. Using this function the user can check if the transfer is still in progress or if time-out event occurred.

Parameters

in	<i>instance</i>	The name of the instance
in	<i>txBuffer</i>	Pointer to tx buffer.
in	<i>rxBuffer</i>	Pointer to rx buffer.
in	<i>numberOfFrames</i>	Number of frames sent/received
in	<i>timeout</i>	Transfer time-out in ms

Returns

Error or success status returned by API

Definition at line 946 of file spi_pal.c.

17.130.4.4 status_t SPI_MasterDeinit (const spi_instance_t *const instance)

De-initializes the spi master module.

This function de-initialized the spi master module.

Parameters

in	<i>instance</i>	The name of the instance
----	-----------------	--------------------------

Returns

Error or success status returned by API

Definition at line 782 of file spi_pal.c.

17.130.4.5 status_t SPI_MasterInit (const spi_instance_t *const instance, const spi_master_t * config)

Initializes the SPI module in master mode.

This function initializes and enables the requested SPI module in master mode, configuring the bus parameters.

Parameters

in	<i>instance</i>	The name of the instance
in	<i>config</i>	The configuration structure

Returns

Error or success status returned by API

Definition at line 248 of file spi_pal.c.

17.130.4.6 status_t SPI_MasterSetDelay (const spi_instance_t *const instance, uint32_t delayBetweenTransfers, uint32_t delaySCKtoPCS, uint32_t delayPCStoSCK)

Configures the SPI_PAL master mode bus timing delay options.

This function involves the DSPI module's delay options to "fine tune" some of the signal timings and match the timing needs of a slower peripheral device. This is an optional function that can be called after the SPI_PAL module has been initialized for master mode. The timings are adjusted in terms of microseconds. The bus timing delays that can be adjusted are listed below:

SCK to PCS Delay: Adjustable delay option between the last edge of SCK to the de-assertion of the PCS signal.

PCS to SCK Delay: Adjustable delay option between the assertion of the PCS signal to the first SCK edge.

Delay between Transfers: Adjustable delay option between the de-assertion of the PCS signal for a frame to the assertion of the PCS signal for the next frame.

Definition at line 1014 of file spi_pal.c.

17.130.4.7 `status_t SPI_MasterTransfer (const spi_instance_t *const instance, const void * txBuffer, void * rxBuffer, uint16_t numberOfFrames)`

Initializes a non-blocking master transfer.

This function initializes a non-blocking master transfer.

Parameters

in	<i>instance</i>	The name of the instance
in	<i>txBuffer</i>	Pointer to tx buffer.
in	<i>rxBuffer</i>	Pointer to rx buffer.
in	<i>numberOfFrames</i>	Number of frames sent/received

Returns

Error or success status returned by API

Definition at line 373 of file spi_pal.c.

17.130.4.8 `status_t SPI_MasterTransferBlocking (const spi_instance_t *const instance, const void * txBuffer, void * rxBuffer, uint16_t numberOfFrames, uint16_t timeout)`

Initializes a blocking master transfer.

This function initializes a blocking master transfer.

Parameters

in	<i>instance</i>	The name of the instance
in	<i>txBuffer</i>	Pointer to tx buffer.
in	<i>rxBuffer</i>	Pointer to rx buffer.
in	<i>numberOfFrames</i>	Number of frames sent/received
in	<i>timeout</i>	Transfer time-out in ms

Returns

Error or success status returned by API

Definition at line 436 of file spi_pal.c.

17.130.4.9 `status_t SPI_SetSS (const spi_instance_t *const instance, uint8_t ss)`

Update the SS.

This function changes the SS, if this feature is available.

Parameters

in	<i>instance</i>	The name of the instance
in	<i>ss</i>	The number of SS

Returns

Error or success status returned by API

Definition at line 900 of file spi_pal.c.

17.130.4.10 `status_t SPI_SlaveDeinit (const spi_instance_t *const instance)`

De-initializes the spi slave module.

This function de-initialized the spi slave module.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance
-----------	-----------------	--------------------------

Returns

Error or success status returned by API

Definition at line 844 of file spi_pal.c.

17.130.4.11 `status_t SPI_SlaveInit (const spi_instance_t *const instance, const spi_slave_t * config)`

Initializes the SPI module in slave mode.

This function initializes and enables the requested SPI module in slave mode, configuring the bus parameters.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance
<i>in</i>	<i>config</i>	The configuration structure

Returns

Error or success status returned by API

Definition at line 499 of file spi_pal.c.

17.130.4.12 `status_t SPI_SlaveTransfer (const spi_instance_t *const instance, const void * txBuffer, void * rxBuffer, uint16_t numberOfFrames)`

Initializes a non-blocking slave transfer.

This function initializes a non-blocking slave transfer.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance
<i>in</i>	<i>txBuffer</i>	Pointer to tx buffer.
<i>in</i>	<i>rxBuffer</i>	Pointer to rx buffer.
<i>in</i>	<i>numberOfFrames</i>	Number of frames sent/received

Returns

Error or success status returned by API

Definition at line 608 of file spi_pal.c.

17.130.4.13 `status_t SPI_SlaveTransferBlocking (const spi_instance_t *const instance, const void * txBuffer, void * rxBuffer, uint16_t numberOfFrames, uint16_t timeout)`

Initializes a blocking slave transfer.

This function initializes a blocking slave transfer.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance
-----------	-----------------	--------------------------

in	<i>txBuffer</i>	Pointer to tx buffer.
in	<i>rxBuffer</i>	Pointer to rx buffer.
in	<i>numberOf↔ Frames</i>	Number of frames sent/received
in	<i>timeout</i>	Transfer time-out in ms

Returns

Error or success status returned by API

Definition at line 671 of file spi_pal.c.

17.131 Signal interaction

This group contains APIs that help users interact with signals of LIN node.

17.132 SoC Header file (SoC Header)

17.132.1 Detailed Description

This module covers SoC Header file.

This section describes the functionality supported by the header file. For usage please see `soc_header_usage`

Modules

- [S32K148 SoC Header file](#)

This module covers the S32K148 SoC Header file.

17.133 SoC Support

17.133.1 Detailed Description

This module covers SoC support files.

This section describes the files that are used for supporting various SoCs.

The support files are:

1. Linker files
2. Start-up files
3. SVD file
4. Header files

Linker files

Linker files are used to control the linkage part of the project compilation and contain details regarding the following:

1. memory areas definition (type and ranges)
2. data and code segments definition and their mapping to the memory areas.

linker configuration files are provided for all supported linkers. Please see [Build Tools](#) for details.

Start-up files

Start-up files are used to control the SoC bring-up part and contain:

1. interrupt vector allocation
2. start-up code and routines

Start-up files are provided for all supported compilers. Please see [Build Tools](#) for details.

SVD file

SVD file contains details about registers and can be used with an IDE to allow mapping of memory location to the register definition and information.

Header file

For each SoC there are two header files provided in the SDK:

1. `<SoC_name>.h`
2. `<SoC_name>_features.h`

The `<SoC_name>.h` file contains information related to registers that is used by the SDK drivers and code. The `<SoC_name>_features.h` contains information related to the integration of modules in the SoC.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\devices\<SoC_name>\startup\system_<SoC_name>.c  
${S32SDK_PATH}\platform\devices\startup.c  
${S32SDK_PATH}\platform\devices\<SoC_name>\startup\<Toolchain>\startup_<SoC_name>.S
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\devices  
${S32SDK_PATH}\platform\devices\<SoC_name>\br/>${S32SDK_PATH}\platform\devices\startup\  
${S32SDK_PATH}\platform\devices\<SoC_name>\include\  
${S32SDK_PATH}\platform\devices\common
```

Compile symbols

```
CPU_S32K144HFT0VLLT for S32K144  
CPU_<SoC_name>
```

Dependencies

No special dependencies are required for this component

Limitations

IAR: Function alignment is not supported using `ALIGNED()` macro.

Modules

- [S32K148 System Files](#)

This module covers the SoC support file for S32K148.

17.134 Start-up control configuration options (0x73)

17.134.1 Detailed Description

This section lists all the possible options of 0x73 register related to:

- Reset pulse width on RSTN pin
- V2 start-up configuration
- HVIO 4 - 2 pin mode selection

See also

[UJA113X_SetMtpnv\(\)](#)

RSTN output reset pulse width configuration options (0x73:RLC[5:4])

- #define [RLC_PULSE_WIDTH_20_25_MS](#) 0x00U
tw(rst) = 20 ms to 25 ms
- #define [RLC_PULSE_WIDTH_10_12_MS](#) 0x10U
tw(rst) = 10 ms to 12.5 ms
- #define [RLC_PULSE_WIDTH_03_05_MS](#) 0x20U
tw(rst) = 3.6 ms to 5 ms
- #define [RLC_PULSE_WIDTH_01_MS](#) 0x30U
tw(rst) = 1 ms to 1.5 ms

V2 start-up control configuration options (0x73:V2SUC[3])

See also

[uja113x_rc_v2c_t](#)

- #define [V2SUC_ALWAYS_OFF](#) 0x00U
Bits V2C is set to [V2C_OFF](#) (00) at power-up.
- #define [V2SUC_ALWAYS_ON](#) 0x08U
Bits V2C is set to [V2C_ON_NSSRF](#) (11) at power-up.

HVIO4 configuration control options (0x73:IO4SFC[2])

- #define [IO4SFC_STD_IO](#) 0x00U
Configure pin HVIO4 as a standard I/O pin.
- #define [IO4SFC_LIMP_HOME](#) 0x04U
Enable HVIO4 limp home function.

HVIO3 configuration control options (0x73:IO3SFC[1])

- #define [IO3SFC_STD_IO](#) 0x00U
Configure pin HVIO3 as a standard I/O pin.
- #define [IO3SFC_LIMP_HOME](#) 0x02U
Enable HVIO3 limp home function.

HVIO2 configuration control options (0x73:IO2SFC[0])

- `#define IO2SFC_STD_IO 0x00U`
Configure pin HVIO2 as a standard I/O pin.
- `#define IO2SFC_LIMP_HOME 0x01U`
Enable HVIO2 limp home function.

17.134.2 Macro Definition Documentation

17.134.2.1 `#define IO2SFC_LIMP_HOME 0x01U`

Enable HVIO2 limp home function.

Definition at line 1309 of file sbc_uja113x.h.

17.134.2.2 `#define IO2SFC_STD_IO 0x00U`

Configure pin HVIO2 as a standard I/O pin.

Definition at line 1308 of file sbc_uja113x.h.

17.134.2.3 `#define IO3SFC_LIMP_HOME 0x02U`

Enable HVIO3 limp home function.

Definition at line 1302 of file sbc_uja113x.h.

17.134.2.4 `#define IO3SFC_STD_IO 0x00U`

Configure pin HVIO3 as a standard I/O pin.

Definition at line 1301 of file sbc_uja113x.h.

17.134.2.5 `#define IO4SFC_LIMP_HOME 0x04U`

Enable HVIO4 limp home function.

Definition at line 1295 of file sbc_uja113x.h.

17.134.2.6 `#define IO4SFC_STD_IO 0x00U`

Configure pin HVIO4 as a standard I/O pin.

Definition at line 1294 of file sbc_uja113x.h.

17.134.2.7 `#define RLC_PULSE_WIDTH_01_MS 0x30U`

$tw(rst) = 1 \text{ ms to } 1.5 \text{ ms}$

Definition at line 1280 of file sbc_uja113x.h.

17.134.2.8 `#define RLC_PULSE_WIDTH_03_05_MS 0x20U`

$tw(rst) = 3.6 \text{ ms to } 5 \text{ ms}$

Definition at line 1279 of file sbc_uja113x.h.

17.134.2.9 `#define RLC_PULSE_WIDTH_10_12_MS 0x10U`

$tw(rst) = 10 \text{ ms to } 12.5 \text{ ms}$

Definition at line 1278 of file sbc_uja113x.h.

17.134.2.10 `#define RLC_PULSE_WIDTH_20_25_MS 0x00U`

tw(rst) = 20 ms to 25 ms

Definition at line 1277 of file sbc_uja113x.h.

17.134.2.11 `#define V2SUC_ALWAYS_OFF 0x00U`

Bits V2C is set to [V2C_OFF](#) (00) at power-up.

Definition at line 1287 of file sbc_uja113x.h.

17.134.2.12 `#define V2SUC_ALWAYS_ON 0x08U`

Bits V2C is set to [V2C_ON_NSSRF](#) (11) at power-up.

Definition at line 1288 of file sbc_uja113x.h.

17.135 Structural Core Self Test

Structural Core Self Test integration with S32 SDK

General Information

- The SCST library provides tests to achieve the claimed diagnostic coverage (analytically estimated).
- The SCST library can be executed periodically at run time. This way, it contributes to a Single-Point Fault metric. The library preserves execution context of application and device configuration.
- The included tests cover most of the core instructions, as well as the tests targeting specific IP blocks of the core:
 - Core control logic (branch control, exception control);
 - Core data path including:
 - * Register file and register multiplexing;
 - * ALU, multiplier, divider, load/store, and other execution units;
 - * SIMDSAT;
 - * Instruction decoder, 16-Bit, 32-Bit;
- Interrupts can be enabled during execution of the most of the tests. SCST library provides its own interrupt vector table and wrappers for interrupt service routines, which in case of unexpected for the library interrupt, forwards it to the corresponding interrupt handler of the OS / user application. SCST library supports nested interrupts without any limitations.
- SCST library can be compiled and linked with other SCST libraries (e.g. SCST library for Cortex A5 core) within the same application for which a single .elf file is generated.

Note

This is just a brief description of the Structural Core Self Test Library, for more information please check the full library documentation found in [<SDK_Location>/lib/<CPU_Family>/SCST/User_Documentation/<CoreType>>_<CPU_Name>_SCST_User_Manual.pdf](#)
 The library is provided in binary format, compiled using GCC and for evaluation purposes only. Please consult license.txt file for more information found in [<SDK_Location>/lib/<CPU_Family>/SCST/license.txt](#)
 The library was built with FPU(hard) enabled, so it must be enabled also in the application which will use it.

How to use

To add SCST in your application you need to follow four steps:

- 1) Add sCST S32CT component into your project. The component will automatically add the required include paths and library files to the compilation.
- 2) Check that **_m4_scst** is added to Libraries under Linker build settings. If it is not present add a new entry with text **:lib_m4_scst.a**
- 3) Check that **"\${workspace_loc:\${ProjName}/SDK/lib/SCST/SCST/src/lib}"** is added to Library search paths under Linker build settings. If it is not present add a new entry with following text (include the quotes as well) **"\${workspace_loc:\${ProjName}/SDK/lib/SCST/SCST/src/lib}"** or add the path to the folder where the library is located.
- 4) Add sCST code and data section to the linker file
 - Example(for GCC linker file):

```
.m4_scst :
{
    *(.m4_scst_test_code)
    *(.m4_scst_test_code_unprivileged)
    *(.m4_scst_test_code1_unprivileged)
    *(.m4_scst_test_shell_code)
    *(.m4_scst_rom_data)
    . = ALIGN(4);
    *(.m4_scst_exception_wrappers)
    *(.m4_scst_vector_table)
    . = ALIGN(4);
} > m_text

.m4_scst2 :
{
    __SCST_DATA_ROM = .;
    __scst_data_start__ = .;
    *(.m4_scst_test_shell_data)
    . = ALIGN(4);
    *(.m4_scst_ram_data)
    . = ALIGN(4);
    *(.m4_scst_ram_data_target0)
    . = ALIGN(4);
    *(.m4_scst_ram_data_target1)
    . = ALIGN(4);
    *(.m4_scst_ram_test_code)
    . = ALIGN(4);
    __scst_data_end__ = .;
} > m_data
```

- 5) Use the library API to execute the required tests.

You can use the sCST example as a practical implementation of the steps described above. SCST can not be used with RAM debug configuration due to RAM memory being too small.

17.136 Supply interrupt enable configuration options (0x1C)

17.136.1 Detailed Description

This section lists all the possible options of 0x1C register related to:

- SMPS status interrupt
- Battery monitor overvoltage interrupt
- Battery monitor undervoltage interrupt
- VEXT overvoltage interrupt
- VEXT undervoltage interrupt
- V1 undervoltage interrupt

See also

[UJA113X_SetSupplyInterrupts\(\)](#)

SMPS status interrupt configuration options (0x1C:SMPSSIE[5])

- #define [SMPSSIE_DISABLE](#) 0x00U
Disable SMPS status interrupt.
- #define [SMPSSIE_ENABLE](#) 0x20U
Enable SMPS status interrupt.

Battery monitor overvoltage interrupt configuration options (0x1C:BMOIE[4])

- #define [BMOIE_DISABLE](#) 0x00U
Disable battery monitor overvoltage interrupt.
- #define [BMOIE_ENABLE](#) 0x10U
Enable battery monitor overvoltage interrupt.

Battery monitor undervoltage interrupt configuration options (0x1C:BMUIE[3])

- #define [BMUIE_DISABLE](#) 0x00U
Disable battery monitor undervoltage interrupt.
- #define [BMUIE_ENABLE](#) 0x08U
Enable battery monitor undervoltage interrupt.

VEXT overvoltage interrupt configuration options (0x1C:VEXTOIE[2])

- #define [VEXTOIE_DISABLE](#) 0x00U
Disable VEXT overvoltage interrupt.
- #define [VEXTOIE_ENABLE](#) 0x04U
Enable VEXT overvoltage interrupt.

VEXT undervoltage interrupt configuration options (0x1C:VEXTUIE[1])

- #define [VEXTUIE_DISABLE](#) 0x00U
Disable VEXT undervoltage interrupt.
- #define [VEXTUIE_ENABLE](#) 0x02U
Enable VEXT undervoltage interrupt.

V1UIE undervoltage interrupt configuration options (0x1C:V1UIE[0])

- #define **V1UIE_DISABLE** 0x00U
Disable V1 undervoltage interrupt.
- #define **V1UIE_ENABLE** 0x01U
Enable V1 undervoltage interrupt.

17.136.2 Macro Definition Documentation

17.136.2.1 #define **BMOIE_DISABLE** 0x00U

Disable battery monitor overvoltage interrupt.

Definition at line 541 of file sbc_uja113x.h.

17.136.2.2 #define **BMOIE_ENABLE** 0x10U

Enable battery monitor overvoltage interrupt.

Definition at line 542 of file sbc_uja113x.h.

17.136.2.3 #define **BMUIE_DISABLE** 0x00U

Disable battery monitor undervoltage interrupt.

Definition at line 548 of file sbc_uja113x.h.

17.136.2.4 #define **BMUIE_ENABLE** 0x08U

Enable battery monitor undervoltage interrupt.

Definition at line 549 of file sbc_uja113x.h.

17.136.2.5 #define **SMPSSIE_DISABLE** 0x00U

Disable SMPS status interrupt.

Definition at line 534 of file sbc_uja113x.h.

17.136.2.6 #define **SMPSSIE_ENABLE** 0x20U

Enable SMPS status interrupt.

Definition at line 535 of file sbc_uja113x.h.

17.136.2.7 #define **V1UIE_DISABLE** 0x00U

Disable V1 undervoltage interrupt.

Definition at line 569 of file sbc_uja113x.h.

17.136.2.8 #define **V1UIE_ENABLE** 0x01U

Enable V1 undervoltage interrupt.

Definition at line 570 of file sbc_uja113x.h.

17.136.2.9 #define **VEXTOIE_DISABLE** 0x00U

Disable VEXT overvoltage interrupt.

Definition at line 555 of file sbc_uja113x.h.

17.136.2.10 `#define VEXTOIE_ENABLE 0x04U`

Enable VEXT overvoltage interrupt.

Definition at line 556 of file sbc_uja113x.h.

17.136.2.11 `#define VEXTUIE_DISABLE 0x00U`

Disable VEXT undervoltage interrupt.

Definition at line 562 of file sbc_uja113x.h.

17.136.2.12 `#define VEXTUIE_ENABLE 0x02U`

Enable VEXT undervoltage interrupt.

Definition at line 563 of file sbc_uja113x.h.

17.137 Synchronous Audio Interface (SAI)

17.137.1 Detailed Description

The S32 SDK provides driver for Synchronous Audio Interface

SAI module support many digital audio transmission standards, for example: I2S, AC97. These sections describe the S32 SDK software modules APIs.

Modules

- [SAI Driver](#)

This module covers the functionality of the Synchronous Audio Interface (SAI) peripheral driver.

17.138 System Basis Chip Driver (SBC) - FS45xx Family

17.138.1 Detailed Description

System Basis Chip driver is a middleware driver for SBC settings and control.

Hardware background

The FS45xx system basis chip (SBC) family provides power to MCUs and optimizes energy consumption through DC/DC switching regulators, linear regulators, and ultra-low-power saving modes. Featuring advanced functional safety measures, serial peripheral interface (SPI) to allow control and diagnostics with the MCU, integration of CAN FD and LIN physical interfaces compliant with the ISO 11898-2,-5, LIN 2.2, 2.1/J2602-2 standards along with the latest automotive OEM standards for EMC and ESD, range of integrated safety features such as monitoring of critical analog parameters, a failsafe state machine, and an advanced watchdog reduce software complexity with dual-core lock-step MCUs.

How to use SBC driver in your application

In order to set up SBC device the user needs to configure `fs45_drv_config_t` structure in which structures corresponding to individual init (configurable during initialization) and non-init (configurable any time) registers are included. The `fs45_drv_config_t` structure is passed as a parameter to `Init` function to initialize SBC device. The rest of the functions are related to individual features and registers.

Initialization

The initialization function is responsible for setting up the FS45xx, according to user configuration data which is passed as parameter. The initialization function takes another parameters which are an instance of SPI used for communication with the SBC and SPI timeout in milliseconds. The initialization function configures all SBC init registers and selected non-init registers.

Writing to registers

In order to write to registers, there are several functions dedicated to some specific registers. These functions (with name containing the word Set) take a value or a pointer to structure containing values to be written to particular registers as a parameter. Besides these methods there is also a generic function `FS45_WriteRegister` which is for writing to any register. It takes three parameters. The first one is an address of a register to be written. Addresses of registers are defined in [sbc_fs45_map.h](#). The second argument is a value which should be sent to a register. The last argument is a pointer to structure for storing received diagnostics and data. NULL pointer can be used when received data should be ignored.

Reading from registers

Several methods to reading specific control and status register are available similarly to the register writing. Their names contain the word Get. Content of any register can be read by function `FS45_ReadRegister`. This function has two arguments. The first is an address of a register to be read from, the second is a pointer to a structure where the content of a register and diagnostic data will be stored. Addresses of registers are defined in [sbc_fs45_map.h](#).

Watchdog refresh

The function `FS45_WD_Refresh` should be called periodically depending on watchdog window set. The function reads watchdog seed from the device, calculates the answer and writes it back to `WD_ANSWER` register.

Low-power mode

The device has two low-power modes which can be entered using the `FS45_SetLowPowerMode` function. Before entering LPOFF Sleep mode make sure some wake-up sources are enabled. The device can be woken up by physical layer (CAN, LIN), timer (LDT), or IOs (`IO_0` is enabled as wake-up source by default). In LPOFF auto WU mode the device wakes up automatically after 1 ms, it allows restart of the state machine.

Setting regulator state

The function `FS45_SetRegulatorState` allows turning on and off of the device regulators. There are various voltage regulators for different purposes. `VCORE` is a high efficiency regulator for MCU. `VCCA` is used to provide accurate voltage output (5.0 or 3.3 V) to MCU IOs, mainly ADC. `VAUX` can be used to power other device in the ECU, or external sensors. `VCAN` is a power supply dedicated to CAN transceiver. `VKAM` provides keep alive memory supply in low-power mode. Note that disabling the regulators might result in loss of some functionality, based on the regulator type and your board design (for example loss of SPI communication, SPI MISO is powered by `VDDIO` internal regulator, which is usually supplied from `VCORE` or `VCCA` - depends on board connections).

CAN and LIN transceivers mode

The functions `FS45_CAN_SetMode` and `FS45_LIN_SetMode` allow transition of the CAN and LIN transceivers between various modes (normal, listen-only, sleep with/without wake-up capability) together with automatic transition to listen only mode when there is a fault. Transitions between the modes can alter the CAN/LIN frames currently being sent on the bus, a delay might need to be added to allow settling after the transition.

Reading diagnostics

There are various diagnostics registers containing status of the voltage regulators (`DIAG_VPRE`, `DIAG_VCORE`, `DIAG_VCCA`, `DIAG_VAUX`, `DIAG_VSUP_VCAN`), CAN/LIN (`DIAG_CAN_FD`, `DIAG_CAN_LIN`) and SPI (`DIAG_↔SPI`), as well as general diagnostics returned on MISO with every read and write command. `FS45_ReadRegister` can be used to gather the status.

Error tracking

If an error during the R/W operations to FS45xx registers occurs, the driver keeps track of it. If a function returns status different from `STATUS_SUCCESS` the status represents the type of error from `status_t` enum.

Example code snippets (for DEVKIT-MPC5744P board).

SBC initialization

This example source code snippet shows how to initialize the device. During initialization the device registers are written with values in the main configuration structure. The main register set is initialized only after power on reset. The first watchdog refresh is part of the initialization function, the SBC should be in `NORMAL` mode upon the function exit. After `FS45_Init` the watchdog refresh timer should be started with period set to 3/4 of the device watchdog period.

```
/* SPI timeout. */
#define SPI_COMM_TIMEOUT_MS 5

int main(void)
{
    /* Status return code. */
    status_t status = STATUS_SUCCESS;
    /* Pointer to store default values of non-init registers. */
    fs45_reg_config_value_t nonInitConfig[5];
    /* Device configuration - if PEx is not used, otherwise the config is generated. */
    fs45_drv_config_t sbc_fs45_InitConfig;

    /* MCU peripherals initialization. */
    ...

    /* Get default values of init registers - if PEx is not used, otherwise the config is generated. */
    FS45_GetDefaultInitRegsConfig(&sbc_fs45_InitConfig);

    /* Change default init register values if needed. */
    /* Change default configuration when FCCU is not used. */
    sbc_fs45_InitConfig.fssmReg.io23Fs = FS45_R_FS_IO_23_FS_NOT_SAFETY;

    /* Get default values of non-init registers - only a subset can be configured too. */
    FS45_GetDefaultNonInitRegsConfig(&sbc_fs45_InitConfig, nonInitConfig);

    /* Change default non-init register values if needed. */
    /* Set watchdog window to 512 ms. */
    sbc_fs45_InitConfig.nonInitRegs[3].value = FS45_R_FS_WD_WINDOW_512MS;

    /* Initialize the SBC. */
    status = FS45_Init(&sbc_fs45_InitConfig, INST_LPSPICOM1, SPI_COMM_TIMEOUT_MS);
}
```

```
if (status != STATUS_SUCCESS)
{
    /* Error. */
}

/* Start timer for watchdog refresh. */
WD_TIMER_START();

...
}
```

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\middleware\sbc\sbc_fs45\source\sbc_fs45_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\middleware\sbc\sbc_fs45\include
```

Compile symbols

No special symbols are required for this component

Dependencies

[Low Power Serial Peripheral Interface \(LPSP\) OS Interface \(OSIF\)](#)

Modules

- [SBC FS45 Driver](#)
SBC FS45 driver.

17.139 System Basis Chip Driver (SBC) - UJA116xA Family

17.139.1 Detailed Description

System Basis Chip driver is a middleware driver for SBC settings and control.

Hardware background

The UJA116xA is a mini high-speed CAN System Basis Chip (SBC) containing an ISO 11898-2:201x compliant HS-CAN transceiver and an integrated 5 V or 3.3 V 250 mA scalable supply (V1) for a microcontroller and/or other loads. It also features a watchdog and a Serial Peripheral Interface (SPI). The UJA116xA can be operated in very low-current Standby and Sleep modes with bus and local wake-up capability. The UJA1169A comes in six variants. The UJA1169ATK, UJA1169ATK/F, UJA1169ATK/X and UJA1169ATK/X/F contain a 5 V regulator (V1). V1 is a 3.3 V regulator in the UJA1169ATK/3 and the UJA1169ATK/F/3. The UJA1169ATK, UJA1169ATK/F, UJA1169ATK/3 and UJA1169ATK/F/3 variants feature a second on-board 5 V regulator (V2) that supplies the internal CAN transceiver and can also be used to supply additional on-board hardware. The UJA1169ATK/X and UJA1169ATK/X/F are equipped with a 5 V supply (VEXT) for off-board components. VEXT is short-circuit proof to the battery, ground and negative voltages. The integrated CAN transceiver is supplied internally via V1, in parallel with the microcontroller. The UJA1168 comes in four variants. The UJA1168ATK, UJA1168ATK/FD, UJA1168ATK/VX and UJA1168ATK/VX/FD contain a 5 V regulator (V1). The UJA1168ATK and UJA1168ATK/FD versions contain a battery-related high-voltage output (INH) for controlling an external voltage regulator, while the UJA1168ATK/VX and UJA1168ATK/VX/FD are equipped with a 5 V sensor supply (VEXT). The UJA1169xx/F and UJA1168xx/FD variants support ISO 11898 compliant CAN partial networking with a selective wake-up function incorporating CAN FD-passive. CAN FD-passive is a feature that allows CAN FD bus traffic to be ignored in Sleep/Standby mode. CAN FD-passive partial networking is the perfect fit for networks that support both CAN FD and classic CAN communications. It allows normal CAN controllers that do not need to communicate CAN FD messages to remain in partial networking Sleep/Standby mode during CAN FD communication without generating bus errors. The UJA116xA implements the standard CAN physical layer as defined in the current ISO11898 standard (-2:2003, -5:2007, -6:2013). A dedicated LIMP output pin is provided to flag system failures on UJA1169 variants. A number of configuration settings are stored in non-volatile memory. This arrangement makes it possible to configure the power-on and limp-home behavior of the UJA116xA to meet the requirements of different applications.

How to use SBC driver in your application

In order to set up SBC device the user needs to configure `sbc_int_config_t` structure in which are included following structures: `sbc_regulator_ctr_t`, `sbc_wtdog_ctr_t`, `sbc_mode_mc_t`, `sbc_fail_safe_lhc_t`, `sbc_sys_evnt_t`, `sbc_lock_t`, `sbc_can_conf_t`, `sbc_wake_t`. These nested structures correspond to individual registers. The `sbc_int_config_t` structure is passed as a parameter to `Init` function to initialize SBC device. The rest of the functions are related to individual registers.

Initialization

The `SBC_InitDriver` function takes a parameter which is an instance of SPI used for communication with UJA116xA. The `SBC_InitDevice` function is responsible for setting up the UJA116xA, according to user configuration data which is passed as parameter. The `SBC_InitDevice` function configures all SBC registers except factories configuration set up in non volatile memory, (Start up control and SBC configuration register.) The `SBC_InitDevice` function transitions the SBC to standby mode, where the configuration is performed, and then to a mode selected in the main configuration structure. Before the transition to standby mode all event capture registers are cleared. In order to read the pre-reset or wake-up events, use `SBC_GetEventsStatus` between `SBC_InitDriver` and `SBC_InitDevice`.

Mode transition

`SBC_SetMode` performs software transition from one mode to another. The transition is achieved by writing to mode control register. The event capture registers are cleared before device is moved to standby and sleep mode.

Writing to registers

In order to write to registers, there are several methods dedicated to some specific registers. These methods (names starting with `SBC_Set`) take a value or a pointer to structure containing values to be written to particular

registers as a parameter. Besides these methods there is also a method `SBC_DataTransfer` which is common to reading and writing to all registers. It takes three parameters. The first one is an address of a register to be written. Addresses of registers are defined in `sbc_register_t` enum. The second argument is pointer to a value which should be sent to a register. The last argument is used for register reading only and its value is unused in this case. NULL pointer is used when parameter is unused.

Reading from registers

Content of a register is read by method `SBC_DataTransfer`, which provides both reading and writing to all registers. This method has three arguments. The first one is an address of a register to be read from, the third one is a pointer to a variable where the content of a register will be stored. Second argument is used for the register writing only and it should be NULL in this case. Addresses of registers are defined in enum `sbc_register_t`. Several methods to reading specific control and status register are available similarly to the register writing. Their names start with `SBC_Get`.

Reading status registers

Content of status register can be read by method `SBC_DataTransfer` or using appropriate function which starts with `SBC_Get` and finishes with `Status`. Event capture registers must be cleared using `SBC_CleanEvents` by setting to 1 appropriate status. For clear all events set all statuses to 1 or reading all event capture statuses using `SBC_GetEventsStatus` before.

There are several functions which read status and store it to structure. The Table 3 summarize which function reads appropriate status register.

Function name	Status register
<code>SBC_GetMainStatus</code>	Main status, Watchdog status
<code>SBC_GetSupplyStatus</code>	V2/VEXT status, V1 status
<code>SBC_GetCanStatus</code>	CAN transceiver status, CAN partial networking error, CAN partial networking status, CAN oscillator status, CAN-bus silence status, VCAN status, CAN failure status
<code>SBC_GetWakeStatus</code>	WAKE pin status
<code>SBC_GetEventsStatus</code>	Global event status, System event status, Supply event status, Transceiver event status, WAKE pin event status
<code>SBC_GetAllStatus</code>	Read all statuses from this table

Reading and writing non-volatile SBC configuration

The UJA116xA contains Multiple Time Programmable Non-Volatile (MTPNV) memory cells that allow some of the default device settings to be reconfigured. This non-volatile memory has limited write access. Programming of the NVM registers is performed in two steps. First, the required values are written. In the second step, reprogramming is confirmed by writing the correct CRC value to the MTPNV CRC control register. This memory is accessed by `SBC_GetFactoriesSettings` and `SBC_ChangeFactoriesSettings` methods. The only parameter is a pointer to `sbc_factories_conf_t` data structure, which should be written to NTPNV or where should be stored data read out from the NTPNV. If the device has been programmed previously, the factory presets may need to be restored before reprogramming can begin. When the factory presets have been restored successfully, a system reset is generated automatically and UJA116xA switches back to Forced Normal mode. If `SBC_ChangeFactoriesSettings` method returns an error "SBC_UJA_NVN_ERROR" it means device was preconfigured from default settings and it is not possible to write to non-volatile memory. Restore factory preset values is needed. Factory preset values are restored if the following conditions apply continuously for at least `td(MTPNV)` during battery power-up: • pin RSTN is held LOW • CANH is pulled up to VBAT • CANL is pulled down to GND Now `SBC_ChangeFactoriesSettings` can be used for change factory preset values to custom configuration.

Error tracking

If an error during the R/W operations to UJA116xA registers occurs, the driver keeps track of it. If a method returns status different from `STATUS_SUCCESS` the status represents the type of error from `sbc_status_t` enum.

Example code snippets (for FRDM PK144-Q100 freedom board).

Initialization example

This example source code snippet shows how to initialize SPI and the SBC. The SPI instance used in this example is LPSPICOM1. The following structures are generated by the configuration tool or need to be created by the user: lpspiCom1_MasterConfig0, lpspiCom1State, sbc_uja116x_InitConfig0.

```
int main(void)
{
    ...

    sbc_status_t status = STATUS_SUCCESS;

    /* Initialization clocks. */
    ...

    /* Initialize pins. */
    ...

    /* Initialize LPSPI. */
    LPSPI_DRV_MasterInit(LPSPICOM1, &lpspiCom1State, &lpspiCom1_MasterConfig0);

    /* Initialize SBC. */
    status = SBC_InitDriver(LPSPICOM1);
    status |= SBC_InitDevice(&sbc_uja116x_InitConfig0);

    if(status != STATUS_SUCCESS)
    {
        /* Do something here. */
    }

    ...
}
```

Write to Regulator control registers example

This example source code snippet shows how to configure Regulator control register. Power distribution control (PDC), V2/VEXT configuration (V2C/ VETXT), V1 reset threshold can be configured by writing to Regulator Control register. Note: PDC can be set for UJA1169 variants (not UJA1168), V2 can be set for models UJA1169ATK, UJA1169ATK/3, UJA1169ATK/F and UJA1169ATK/F/3, VEXT can be set for models UJA1169ATK/X and UJA1169ATK/X/F. For more info read function description.

```
int main(void)
{
    ...

    sbc_status_t status = STATUS_SUCCESS;
    sbc_regulator_ctr_t regulator;
    regulator.regulator.pdc = SBC_UJA_REGULATOR_PDC_HV;
    regulator.regulator.v2c = SBC_UJA_REGULATOR_V2C_OFF;
    regulator.regulator.v1rtc = SBC_UJA_REGULATOR_V1RTC_80;

    regulator.supplyEvt.v2oe = SBC_UJA_SUPPLY_EVT_V2OE_EN;
    regulator.supplyEvt.v2ue = SBC_UJA_SUPPLY_EVT_V2UE_EN;
    regulator.supplyEvt.v1ue = SBC_UJA_SUPPLY_EVT_V1UE_DIS;

    status = SBC_SetVreg(&regulator);

    if(status != STATUS_SUCCESS)
    {
        /* Do something here. */
    }

    ...
}
```

Read from Regulator control registers example

This example source code snippet shows how to read from Regulator control registers. Reading Regulator control register gives information about Power distribution control (PDC), V2/VEXT configuration (V2C/ VETXT), V1 reset threshold current configuration. Using this method can be useful for check if the Regulator control register is configured correctly. For more info read function description.

```
int main(void)
{
```

```

...

sbc_status_t status = STATUS_SUCCESS;
sbc_regulator_ctr_t regulator;

status = SBC_GetVreg(&regulator);

if(status == STATUS_SUCCESS)
{
    if(regulator.supplyEvt.v2oe ==
        SBC_UJA_SUPPLY_EVT_V2OE_EN)
    {
        /* Do something here. */
    }
}

...
}

```

Reading all device status example

This example source code snippet shows how to read all SBC device statuses in one function. Variable allStatuses contains these registers: Main status register, Watchdog status register, Supply voltage status register, Transceiver status register, WAKE pin status register, Event capture registers. For more info read function description.

```

int main(void)
{
    ...

    sbc_status_t status = STATUS_SUCCESS;
    sbc_status_group_t allStatuses;

    while(1) {

        status = SBC_GetAllStatus(&allStatuses);

        if(status == STATUS_SUCCESS)
        {

            if(allStatuses.trans.cbss == SBC_UJA_TRANS_STAT_CBSS_ACT)
            {
                /* Do something here. */
            }

            if(allStatuses.supply.vls == SBC_UJA_SUPPLY_STAT_VLS_VAB)
            {
                /* Do something here. */
            }

            ...

            /* Periodically feed watchdog (anytime in watchdog period in case of timeout watchdog mode). */
            SBC_FeedWatchdog();
        }
    }
}

```

Reading Transceiver device status example

This example source code snippet shows how to read Transceiver device status from SBC. It contains CAN transceiver status, CAN partial networking error, CAN partial networking status, CAN oscillator status, CAN-bus silence status, VCAN status, CAN failure status. For more info read function description. Note similar approach can be used for reading other status using different SBC_Get*Status.

```

int main(void)
{
    ...

    sbc_status_t status = STATUS_SUCCESS;
    sbc_trans_stat_t transStatus;

    while(1) {

        status = SBC_GetCanStatus(&transStatus);

        if(status == STATUS_SUCCESS)
        {

            if(transStatus.cbss == SBC_UJA_TRANS_STAT_CBSS_ACT)

```

```

    {
        /* Do something here. */
    }

    ...

    /* Periodically feed watchdog (anytime in watchdog period in case of timeout watchdog mode). */
    SBC_FeedWatchdog();
}
}
}

```

Change factories settings

This example source code snippet shows how to change factory preset value of non-volatile memory. Device must be set to factory preset. For more info read function description.

```

int main(void)
{
    ...

    sbc_status_t status = STATUS_SUCCESS;
    sbc_factories_conf_t factories;

    status = SBC_GetFactoriesSettings(&factories);

    factories.control.fnmc = SBC_UJA_SBC_SDMC_EN;
    factories.control.sdmc = SBC_UJA_SBC_SDMC_DIS;
    factories.startUp.rlc = SBC_UJA_START_UP_RLC_20_25p0;

    if(status == STATUS_SUCCESS)
    {
        status = SBC_ChangeFactoriesSettings(&factories);
    }

    if(status != STATUS_SUCCESS)
    {
        /* Do something here. */
    }
}

```

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\middleware\sbc\sbc_uja116x\source\sbc_uja116x_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\middleware\sbc\sbc_uja116x\include
```

Compile symbols

No special symbols are required for this component

Dependencies

[Low Power Serial Peripheral Interface \(LPSPI\) OS Interface \(OSIF\)](#)

Modules

- [UJA116xA SBC Driver](#)

17.140 System Basis Chip library (SBC) - UJA113x Family

17.140.1 Detailed Description

System Basis Chip library for configuration and control.

17.140.2 Introduction

The SBC is quite complex device with many features (CAN/CAN FD & LIN transceivers, Buck/boost driver, watch-dog etc.), several modes (Normal, Standby, Sleep, Forced normal mode, Software Development mode etc.) and provides interrupt/polling based error reporting mechanism to the Host MCU. Different applications require different functionalities ranging from a single feature usage to a complete SBC functionality. From this perspective it's not possible to provide a driver, which would satisfy the needs of all the applications. The driver would become too complicated with a large code footprint and the user will use it as a guide how to create his own application at the end instead.

From the abovementioned reasons the library is not a driver and should not be understood that way. It's a library which in conjunction with the S32 SDK provides a low level API allowing the user fast product evaluation in the first step. After becoming familiar with the device, the API can be used as a basis for a more complex application, where the user determines, whether interrupt based error handling or polling is sufficient, which errors to handle, how and when to switch between modes etc.

From programming perspective the chip is divided into following register groups:

- [01. Primary control](#) registers
- [02. Supply control](#) registers
- [03. Transceiver control](#) registers
- [04. HVIO bank 0 & 1 control](#) registers
- [05. Timer control](#) registers
- [06. Interrupts](#)
- [07. MTPNV and ID](#) registers

Each group represents a set of registers for configuring different part/functionality of the SBC. For instance the Primary control registers can be used to configure the Watchdog, SBC mode, Fail-safe behavior, General-purpose user memory etc. The API is designed that way to facilitate the users chip configuration by allowing the user to configure the chip per functionality.

For library internals description and how to start using this library, proceed to [00. Library internals](#) section.

Modules

- [00. Library internals](#)
- [01. Primary control](#)
- [02. Supply control](#)
- [03. Transceiver control](#)
- [04. HVIO bank 0 & 1 control](#)
- [05. Timer control](#)
- [06. Interrupts](#)
- [07. MTPNV and ID](#)

17.141 System interrupt enable configuration options (0x04)

17.141.1 Detailed Description

This section lists all the possible options of 0x04 register related to:

- Overtemperature interrupt
- SPI failure interrupt

See also

[UJA113X_SetSystemInterrupts\(\)](#)

Overtemperature warning interrupt configuration options (0x04:OTWIE[2])

- #define [OTWIE_DISABLE](#) 0x00U
Disable overtemperature warning interrupt.
- #define [OTWIE_ENABLE](#) 0x04U
Enable overtemperature warning interrupt.

SPI failure interrupt configuration options (0x04:SPIFIE[1])

- #define [SPIFIE_DISABLE](#) 0x00U
Disable SPI failure interrupt.
- #define [SPIFIE_ENABLE](#) 0x02U
Enable SPI failure interrupt.

17.141.2 Macro Definition Documentation

17.141.2.1 #define OTWIE_DISABLE 0x00U

Disable overtemperature warning interrupt.

Definition at line 343 of file sbc_uja113x.h.

17.141.2.2 #define OTWIE_ENABLE 0x04U

Enable overtemperature warning interrupt.

Definition at line 344 of file sbc_uja113x.h.

17.141.2.3 #define SPIFIE_DISABLE 0x00U

Disable SPI failure interrupt.

Definition at line 350 of file sbc_uja113x.h.

17.141.2.4 #define SPIFIE_ENABLE 0x02U

Enable SPI failure interrupt.

Definition at line 351 of file sbc_uja113x.h.

17.142 TJA110x PHY

17.142.1 Detailed Description

PHY driver for TJA110x series.

Supported devices

This driver supports TJA1110, TJA1101, TJA1102, TJA1102S devices. It reuses functions of [Generic PHY](#)

Unsupported API

The following functions are not supported by this driver:

- PHY_EnableAutoneg
- PHY_DisableAutoneg
- PHY_RestartAutoneg

Note: Wakeup functionality is not supported on TJA1100

Device specific configuration options

Device specific configuration options are represented by the [phy_tja110x_config_t](#) structure and include:

- Local wake-up forwarding
- Remote wake-up forwarding
- MII output driver strength reduced
- CLK_IN_OUT output driver strength reduced
- XTAL and CLK_IN_OUT output remain active until device switched to Sleep mode via SMI
- Local wake configuration: ratiometric input threshold
- Local wake-up timer
- Clock mode

Note: Device specific configuration options are not available for TJA1100

Files

- file [phy_tja110x.c](#)

Data Structures

- struct [phy_tja110x_config_t](#)
TJA110x PHY extended configuration structure. [More...](#)

Macros

- #define [OUI](#) 0x0006ECU
- #define [TJA1102P0_TYPE_NO](#) 0x8U
- #define [TJA1100_TYPE_NO](#) 0x4U
- #define [BASIC_CTRL_ADDR](#) 0U

- #define EXTENDED_CTRL_ADDR 17U
- #define CONFIG1_ADDR 18U
- #define CONFIG2_ADDR 19U
- #define IRQ_STATUS_ADDR 21U
- #define IRQ_ENABLE_ADDR 22U
- #define COMM_STATUS_ADDR 23U
- #define GENERAL_STATUS_ADDR 24U
- #define COMMON_CONFIG_ADDR 27U
- #define BASIC_CTRL_LOOPBACK_FLAG 0x4000U
- #define EXTENDED_CTRL_LINK_CTRL_FLAG 0x8000U
- #define EXTENDED_CTRL_LOOPBACK_MODE_MASK 0x0018U
- #define EXTENDED_CTRL_LOOPBACK_MODE_INTERNAL 0x0000U
- #define EXTENDED_CTRL_LOOPBACK_MODE_EXTERNAL 0x0008U
- #define EXTENDED_CTRL_LOOPBACK_MODE_REMOTE 0x0018U
- #define EXTENDED_CTRL_POWER_MODE_MASK 0x7800U
- #define EXTENDED_CTRL_POWER_MODE_SLEEP_REQ 0x5800U
- #define EXTENDED_CTRL_POWER_MODE_NORMAL_REQ 0x1800U
- #define EXTENDED_CTRL_POWER_MODE_STANDBY 0x6000U
- #define EXTENDED_CTRL_POWER_MODE_SLEEP 0x5000U
- #define EXTENDED_CTRL_POWER_MODE_SILENT 0x4800U
- #define EXTENDED_CTRL_TEST_MODE_MASK 0x01C0U
- #define EXTENDED_CTRL_WAKE_REQ_FLAG 0x0001U
- #define EXTENDED_CTRL_CONFIG_EN_FLAG 0x0004U
- #define EXTENDED_CTRL_TEST_MODE_SHIFT 6U
- #define CONFIG1_MASTERSLAVE_FLAG 0x8000U
- #define CONFIG1_FWDPHYLOC_FLAG 0x4000U
- #define CONFIG1_REMWUPHY_FLAG 0x0800U
- #define CONFIG1_LOCWUPHY_FLAG 0x0400U
- #define CONFIG1_MII_MODE_MASK 0x0300U
- #define CONFIG1_MII_DRIVER_FLAG 0x0080U
- #define CONFIG1_SLEEPCONFIRM_FLAG 0x0040U
- #define CONFIG1_SLEEPACK_FLAG 0x0010U
- #define CONFIG1_FWDPHYREM_FLAG 0x0004U
- #define CONFIG1_MII_MODE_SHIFT 8U
- #define CONFIG2_SLEEPREQUESTTO_MASK 0x0003U
- #define CONFIG2_SLEEPREQUESTTO_16_8 0x0003U
- #define IRQ_PWON_FLAG 0x8000U
- #define IRQ_WAKEUP_FLAG 0x4000U
- #define IRQ_LPS_RECEIVED_FLAG 0x1000U
- #define IRQ_LINKUP_FLAG 0x0200U
- #define IRQ_LINKDOWN_FLAG 0x0400U
- #define COMM_STATUS_LINKUP_FLAG 0x8000U
- #define GENERAL_STATUS_INT_STATUS_FLAG 0x8000U
- #define GENERAL_STATUS_PLL_LOCKED_FLAG 0x4000U
- #define GENERAL_STATUS_ENSTATUS_FLAG 0x0400U
- #define GENERAL_STATUS_RSTSTATUS_FLAG 0x0200U
- #define COMMON_CONFIG_AUTO_OP_MASK 0x8000U
- #define COMMON_CONFIG_CLK_MODE_MASK 0x3000U
- #define COMMON_CONFIG_CLK_MODE_LSB 12U
- #define COMMON_CONFIG_CLK_DRIVER_FLAG 0x0400U
- #define COMMON_CONFIG_CLK_HOLD_FLAG 0x0200U
- #define COMMON_CONFIG_LOC_WU_TIM_MASK 0x0180U
- #define COMMON_CONFIG_LOC_WU_TIM_SHORTEST 0x0180U
- #define COMMON_CONFIG_LOC_WU_TIM_SHORT 0x0100U
- #define COMMON_CONFIG_LOC_WU_TIM_LONG 0x0080U
- #define COMMON_CONFIG_CONFIG_WAKE_FLAG 0x0040U

Enumerations

- enum [phy_tja110x_localWuTime_t](#) { PHY_TJA110X_LOCALWUTIME_SHORTEST = 3, PHY_TJA110X_LOCALWUTIME_SHORT = 2, PHY_TJA110X_LOCALWUTIME_LONG = 1, PHY_TJA110X_LOCALWUTIME_LONGEST = 0 }

TJA110x PHY local wakeup pin timer.

- enum [phy_tja110x_clkMode_t](#) { PHY_TJA110X_CLKMODE_50MHZ_EXT_REFCLK = 3, PHY_TJA110X_CLKMODE_25MHZ_EXT_CLK = 2, PHY_TJA110X_CLKMODE_XTAL_WITH_25MHZ_OUTPUT = 1, PHY_TJA110X_CLKMODE_XTAL_NO_OUTPUT = 0 }

TJA110x PHY clk mode.

Functions

- static status_t [init](#) (uint8_t phy)
- static status_t [getState](#) (uint8_t phy, [phy_state_t](#) *state)
- static status_t [sleepAbortReject](#) (uint8_t phy)
- static status_t [sleep](#) (uint8_t phy)
- static status_t [wakeup](#) (uint8_t phy)
- static status_t [setRole](#) (uint8_t phy, [phy_role_t](#) role)
- static status_t [setLoopback](#) (uint8_t phy, [phy_loopback_t](#) loopbackMode)
- static status_t [selectTestMode](#) (uint8_t phy, uint8_t testModelIndex)
- static status_t [enableInterrupts](#) (uint8_t phy)
- static status_t [handleInterrupt](#) (uint8_t phy)
- static status_t [resume](#) (uint8_t phy)
- static status_t [writeExtendedConfig](#) (uint8_t phy, bool config1, bool commonConfig)
- static status_t [handleInterruptPwon](#) (uint8_t phy)
- static status_t [handleInterruptLinkUp](#) (uint8_t phy)
- static void [handleInterruptLinkDown](#) (uint8_t phy)
- static status_t [handleInterruptWakeUp](#) (uint8_t phy)
- static void [handleInterruptSleep](#) (uint8_t phy)
- static status_t [goFromStandbyToNormalMode](#) (uint8_t phy)
- static status_t [setManagedOperation](#) (uint8_t phy)
- static status_t [enableLink](#) (uint8_t phy)
- static status_t [disableLink](#) (uint8_t phy)
- static status_t [enableConfig](#) (uint8_t phy)
- static status_t [disableConfig](#) (uint8_t phy)

Variables

- [phy_driver_t PHY_driver_tja110x](#)

TJA110x PHY driver structure.

- [phy_driver_t PHY_driver_tja110x](#)

TJA110x PHY driver structure.

17.142.2 Data Structure Documentation

17.142.2.1 struct [phy_tja110x_config_t](#)

TJA110x PHY extended configuration structure.

Definition at line 85 of file [phy_tja110x.h](#).

Data Fields

- bool [fwdPhyLocal](#)
- bool [fwdPhyRemote](#)
- bool [localWakeupPhy](#)
- bool [remoteWakeupPhy](#)
- bool [reducedMiiDriveStrength](#)
- bool [reducedClkDriveStrength](#)
- bool [clkHold](#)
- bool [wakeInRatiometricThreshold](#)
- [phy_tja110x_localWuTime_t](#) [localWuTimer](#)
- [phy_tja110x_clkMode_t](#) [clkMode](#)

Field Documentation

17.142.2.1.1 bool [clkHold](#)

XTAL and CLK_IN_OUT output remain active until device switched to Sleep mode via SMI

Definition at line 93 of file [phy_tja110x.h](#).

17.142.2.1.2 [phy_tja110x_clkMode_t](#) [clkMode](#)

clock mode

Definition at line 96 of file [phy_tja110x.h](#).

17.142.2.1.3 bool [fwdPhyLocal](#)

local wake-up forwarding

Definition at line 87 of file [phy_tja110x.h](#).

17.142.2.1.4 bool [fwdPhyRemote](#)

remote wake-up forwarding

Definition at line 88 of file [phy_tja110x.h](#).

17.142.2.1.5 bool [localWakeupPhy](#)

local wake-up

Definition at line 89 of file [phy_tja110x.h](#).

17.142.2.1.6 [phy_tja110x_localWuTime_t](#) [localWuTimer](#)

local wake-up timer

Definition at line 95 of file [phy_tja110x.h](#).

17.142.2.1.7 bool [reducedClkDriveStrength](#)

CLK_IN_OUT output driver strength reduced

Definition at line 92 of file [phy_tja110x.h](#).

17.142.2.1.8 bool [reducedMiiDriveStrength](#)

MII output driver strength reduced

Definition at line 91 of file [phy_tja110x.h](#).

17.142.2.1.9 bool remoteWakeupPhy

remote wake-up

Definition at line 90 of file phy_tja110x.h.

17.142.2.1.10 bool wakeInRatiometricThreshold

local wake configuration: ratiometric input threshold

Definition at line 94 of file phy_tja110x.h.

17.142.3 Macro Definition Documentation

17.142.3.1 #define BASIC_CTRL_ADDR 0U

Definition at line 72 of file phy_tja110x.c.

17.142.3.2 #define BASIC_CTRL_LOOPBACK_FLAG 0x4000U

Definition at line 82 of file phy_tja110x.c.

17.142.3.3 #define COMM_STATUS_ADDR 23U

Definition at line 78 of file phy_tja110x.c.

17.142.3.4 #define COMM_STATUS_LINKUP_FLAG 0x8000U

Definition at line 120 of file phy_tja110x.c.

17.142.3.5 #define COMMON_CONFIG_ADDR 27U

Definition at line 80 of file phy_tja110x.c.

17.142.3.6 #define COMMON_CONFIG_AUTO_OP_MASK 0x8000U

Definition at line 127 of file phy_tja110x.c.

17.142.3.7 #define COMMON_CONFIG_CLK_DRIVER_FLAG 0x0400U

Definition at line 130 of file phy_tja110x.c.

17.142.3.8 #define COMMON_CONFIG_CLK_HOLD_FLAG 0x0200U

Definition at line 131 of file phy_tja110x.c.

17.142.3.9 #define COMMON_CONFIG_CLK_MODE_LSB 12U

Definition at line 129 of file phy_tja110x.c.

17.142.3.10 #define COMMON_CONFIG_CLK_MODE_MASK 0x3000U

Definition at line 128 of file phy_tja110x.c.

17.142.3.11 #define COMMON_CONFIG_CONFIG_WAKE_FLAG 0x0040U

Definition at line 137 of file phy_tja110x.c.

17.142.3.12 #define COMMON_CONFIG_LOC_WU_TIM_LONG 0x0080U

Definition at line 135 of file phy_tja110x.c.

17.142.3.13 `#define COMMON_CONFIG_LOC_WU_TIM_MASK 0x0180U`

Definition at line 132 of file `phy_tja110x.c`.

17.142.3.14 `#define COMMON_CONFIG_LOC_WU_TIM_SHORT 0x0100U`

Definition at line 134 of file `phy_tja110x.c`.

17.142.3.15 `#define COMMON_CONFIG_LOC_WU_TIM_SHORTEST 0x0180U`

Definition at line 133 of file `phy_tja110x.c`.

17.142.3.16 `#define CONFIG1_ADDR 18U`

Definition at line 74 of file `phy_tja110x.c`.

17.142.3.17 `#define CONFIG1_FWDPHYLOC_FLAG 0x4000U`

Definition at line 101 of file `phy_tja110x.c`.

17.142.3.18 `#define CONFIG1_FWDPHYREM_FLAG 0x0004U`

Definition at line 108 of file `phy_tja110x.c`.

17.142.3.19 `#define CONFIG1_LOCWUPHY_FLAG 0x0400U`

Definition at line 103 of file `phy_tja110x.c`.

17.142.3.20 `#define CONFIG1_MASTERSLAVE_FLAG 0x8000U`

Definition at line 100 of file `phy_tja110x.c`.

17.142.3.21 `#define CONFIG1_MII_DRIVER_FLAG 0x0080U`

Definition at line 105 of file `phy_tja110x.c`.

17.142.3.22 `#define CONFIG1_MII_MODE_MASK 0x0300U`

Definition at line 104 of file `phy_tja110x.c`.

17.142.3.23 `#define CONFIG1_MII_MODE_SHIFT 8U`

Definition at line 109 of file `phy_tja110x.c`.

17.142.3.24 `#define CONFIG1_REMWUPHY_FLAG 0x0800U`

Definition at line 102 of file `phy_tja110x.c`.

17.142.3.25 `#define CONFIG1_SLEEPACK_FLAG 0x0010U`

Definition at line 107 of file `phy_tja110x.c`.

17.142.3.26 `#define CONFIG1_SLEEPCONFIRM_FLAG 0x0040U`

Definition at line 106 of file `phy_tja110x.c`.

17.142.3.27 `#define CONFIG2_ADDR 19U`

Definition at line 75 of file `phy_tja110x.c`.

17.142.3.28 **#define CONFIG2_SLEEPREQUESTTO_16_8 0x0003U**

Definition at line 112 of file phy_tja110x.c.

17.142.3.29 **#define CONFIG2_SLEEPREQUESTTO_MASK 0x0003U**

Definition at line 111 of file phy_tja110x.c.

17.142.3.30 **#define EXTENDED_CTRL_ADDR 17U**

Definition at line 73 of file phy_tja110x.c.

17.142.3.31 **#define EXTENDED_CTRL_CONFIG_EN_FLAG 0x0004U**

Definition at line 97 of file phy_tja110x.c.

17.142.3.32 **#define EXTENDED_CTRL_LINK_CTRL_FLAG 0x8000U**

Definition at line 84 of file phy_tja110x.c.

17.142.3.33 **#define EXTENDED_CTRL_LOOPBACK_MODE_EXTERNAL 0x0008U**

Definition at line 87 of file phy_tja110x.c.

17.142.3.34 **#define EXTENDED_CTRL_LOOPBACK_MODE_INTERNAL 0x0000U**

Definition at line 86 of file phy_tja110x.c.

17.142.3.35 **#define EXTENDED_CTRL_LOOPBACK_MODE_MASK 0x0018U**

Definition at line 85 of file phy_tja110x.c.

17.142.3.36 **#define EXTENDED_CTRL_LOOPBACK_MODE_REMOTE 0x0018U**

Definition at line 88 of file phy_tja110x.c.

17.142.3.37 **#define EXTENDED_CTRL_POWER_MODE_MASK 0x7800U**

Definition at line 89 of file phy_tja110x.c.

17.142.3.38 **#define EXTENDED_CTRL_POWER_MODE_NORMAL_REQ 0x1800U**

Definition at line 91 of file phy_tja110x.c.

17.142.3.39 **#define EXTENDED_CTRL_POWER_MODE_SILENT 0x4800U**

Definition at line 94 of file phy_tja110x.c.

17.142.3.40 **#define EXTENDED_CTRL_POWER_MODE_SLEEP 0x5000U**

Definition at line 93 of file phy_tja110x.c.

17.142.3.41 **#define EXTENDED_CTRL_POWER_MODE_SLEEP_REQ 0x5800U**

Definition at line 90 of file phy_tja110x.c.

17.142.3.42 **#define EXTENDED_CTRL_POWER_MODE_STANDBY 0x6000U**

Definition at line 92 of file phy_tja110x.c.

17.142.3.43 **#define EXTENDED_CTRL_TEST_MODE_MASK 0x01C0U**

Definition at line 95 of file phy_tja110x.c.

17.142.3.44 **#define EXTENDED_CTRL_TEST_MODE_SHIFT 6U**

Definition at line 98 of file phy_tja110x.c.

17.142.3.45 **#define EXTENDED_CTRL_WAKE_REQ_FLAG 0x0001U**

Definition at line 96 of file phy_tja110x.c.

17.142.3.46 **#define GENERAL_STATUS_ADDR 24U**

Definition at line 79 of file phy_tja110x.c.

17.142.3.47 **#define GENERAL_STATUS_ENSTATUS_FLAG 0x0400U**

Definition at line 124 of file phy_tja110x.c.

17.142.3.48 **#define GENERAL_STATUS_INT_STATUS_FLAG 0x8000U**

Definition at line 122 of file phy_tja110x.c.

17.142.3.49 **#define GENERAL_STATUS_PLL_LOCKED_FLAG 0x4000U**

Definition at line 123 of file phy_tja110x.c.

17.142.3.50 **#define GENERAL_STATUS_RSTSTATUS_FLAG 0x0200U**

Definition at line 125 of file phy_tja110x.c.

17.142.3.51 **#define IRQ_ENABLE_ADDR 22U**

Definition at line 77 of file phy_tja110x.c.

17.142.3.52 **#define IRQ_LINKDOWN_FLAG 0x0400U**

Definition at line 118 of file phy_tja110x.c.

17.142.3.53 **#define IRQ_LINKUP_FLAG 0x0200U**

Definition at line 117 of file phy_tja110x.c.

17.142.3.54 **#define IRQ_LPS_RECEIVED_FLAG 0x1000U**

Definition at line 116 of file phy_tja110x.c.

17.142.3.55 **#define IRQ_PWON_FLAG 0x8000U**

Definition at line 114 of file phy_tja110x.c.

17.142.3.56 **#define IRQ_STATUS_ADDR 21U**

Definition at line 76 of file phy_tja110x.c.

17.142.3.57 **#define IRQ_WAKEUP_FLAG 0x4000U**

Definition at line 115 of file phy_tja110x.c.

17.142.3.58 #define OUI 0x0006ECU

Expected OUI across all devices covered by this driver

Definition at line 68 of file phy_tja110x.c.

17.142.3.59 #define TJA1100_TYPE_NO 0x4U

Definition at line 70 of file phy_tja110x.c.

17.142.3.60 #define TJA1102P0_TYPE_NO 0x8U

Definition at line 69 of file phy_tja110x.c.

17.142.4 Enumeration Type Documentation

17.142.4.1 enum phy_tja110x_clkMode_t

TJA110x PHY clk mode.

Enumerator

PHY_TJA110X_CLKMODE_50MHZ_EXT_REFCLK shortest (10 us to 40 us)

PHY_TJA110X_CLKMODE_25MHZ_EXT_CLK short (100 us to 200 us)

PHY_TJA110X_CLKMODE_XTAL_WITH_25MHZ_OUTPUT long (250 us to 500 us)

PHY_TJA110X_CLKMODE_XTAL_NO_OUTPUT longest (10 ms to 20 ms)

Definition at line 74 of file phy_tja110x.h.

17.142.4.2 enum phy_tja110x_localWuTime_t

TJA110x PHY local wakeup pin timer.

Enumerator

PHY_TJA110X_LOCALWUTIME_SHORTEST shortest (10 us to 40 us)

PHY_TJA110X_LOCALWUTIME_SHORT short (100 us to 200 us)

PHY_TJA110X_LOCALWUTIME_LONG long (250 us to 500 us)

PHY_TJA110X_LOCALWUTIME_LONGEST longest (10 ms to 20 ms)

Definition at line 63 of file phy_tja110x.h.

17.142.5 Function Documentation

17.142.5.1 static status_t disableConfig (uint8_t phy) [inline], [static]

Definition at line 248 of file phy_tja110x.c.

17.142.5.2 static status_t disableLink (uint8_t phy) [inline], [static]

Definition at line 226 of file phy_tja110x.c.

17.142.5.3 static status_t enableConfig (uint8_t phy) [inline], [static]

Definition at line 237 of file phy_tja110x.c.

17.142.5.4 static status_t enableInterrupts (uint8_t phy) [static]

Definition at line 606 of file phy_tja110x.c.

17.142.5.5 `static status_t enableLink (uint8_t phy) [inline], [static]`

Definition at line 215 of file `phy_tja110x.c`.

17.142.5.6 `static status_t getState (uint8_t phy, phy_state_t * state) [static]`

Definition at line 346 of file `phy_tja110x.c`.

17.142.5.7 `static status_t goFromStandbyToNormalMode (uint8_t phy) [static]`

Definition at line 999 of file `phy_tja110x.c`.

17.142.5.8 `static status_t handleInterrupt (uint8_t phy) [static]`

Definition at line 621 of file `phy_tja110x.c`.

17.142.5.9 `static void handleInterruptLinkDown (uint8_t phy) [static]`

Definition at line 894 of file `phy_tja110x.c`.

17.142.5.10 `static status_t handleInterruptLinkUp (uint8_t phy) [static]`

Definition at line 908 of file `phy_tja110x.c`.

17.142.5.11 `static status_t handleInterruptPwon (uint8_t phy) [static]`

Definition at line 785 of file `phy_tja110x.c`.

17.142.5.12 `static void handleInterruptSleep (uint8_t phy) [static]`

Definition at line 960 of file `phy_tja110x.c`.

17.142.5.13 `static status_t handleInterruptWakeUp (uint8_t phy) [static]`

Definition at line 940 of file `phy_tja110x.c`.

17.142.5.14 `static status_t init (uint8_t phy) [static]`

Definition at line 259 of file `phy_tja110x.c`.

17.142.5.15 `static status_t resume (uint8_t phy) [static]`

Definition at line 974 of file `phy_tja110x.c`.

17.142.5.16 `static status_t selectTestMode (uint8_t phy, uint8_t testModelIndex) [static]`

Definition at line 566 of file `phy_tja110x.c`.

17.142.5.17 `static status_t setLoopback (uint8_t phy, phy_loopback_t loopbackMode) [static]`

Definition at line 503 of file `phy_tja110x.c`.

17.142.5.18 `static status_t setManagedOperation (uint8_t phy) [static]`

Definition at line 1036 of file `phy_tja110x.c`.

17.142.5.19 `static status_t setRole (uint8_t phy, phy_role_t role) [static]`

Definition at line 452 of file `phy_tja110x.c`.

17.142.5.20 `static status_t sleep (uint8_t phy)` `[static]`

Definition at line 400 of file `phy_tja110x.c`.

17.142.5.21 `static status_t sleepAbortReject (uint8_t phy)` `[static]`

Definition at line 389 of file `phy_tja110x.c`.

17.142.5.22 `static status_t wakeup (uint8_t phy)` `[static]`

Definition at line 411 of file `phy_tja110x.c`.

17.142.5.23 `static status_t writeExtendedConfig (uint8_t phy, bool config1, bool commonConfig)` `[static]`

Definition at line 702 of file `phy_tja110x.c`.

17.142.6 Variable Documentation

17.142.6.1 `phy_driver_t` `PHY_driver_tja110x`

TJA110x PHY driver structure.

Definition at line 174 of file `phy_tja110x.c`.

17.142.6.2 `phy_driver_t` `PHY_driver_tja110x`

Initial value:

```
=
{
    .init           = init,
    .reset          = NULL,
    .mainFunction   = handleInterrupt,
    .getId          = NULL,
    .getState       = getState,
    .getLinkStatus  = NULL,
    .getLinkSpeed   = NULL,
    .getDelay       = NULL,
    .suspend        = NULL,
    .resume         = resume,
    .sleepAbortReject = sleepAbortReject,
    .sleep          = sleep,
    .wakeup         = wakeup,
    .setRole        = setRole,
    .setLoopback    = setLoopback,
    .selectTestMode = selectTestMode,
    .enableInterrupts = enableInterrupts,
    .handleInterrupt = handleInterrupt,
    .enableAutoneg  = NULL,
    .disableAutoneg = NULL,
    .restartAutoneg  = NULL,
    .write          = NULL,
    .read           = NULL,
    .rmw            = NULL,
    .writeMMD       = NULL,
    .readMMD        = NULL,
    .rmwMMD         = NULL
}
```

TJA110x PHY driver structure.

Definition at line 174 of file `phy_tja110x.c`.

17.143 TRGMUX Driver

17.143.1 Detailed Description

Trigger MUX Control Peripheral Driver. The TRGMUX introduces an extremely flexible methodology for connecting various trigger sources to multiple pins/peripherals.

The S32 SDK provides Peripheral Drivers for the Trigger MUX Control (TRGMUX) module of S32 SDK devices.

Overview

This section describes the programming interface of the TRGMUX driver. The TRGMUX driver configures the TRGMUX (Trigger Mux Control). The Trigger MUX module allows software to configure the trigger inputs for various peripherals.

TRGMUX Driver model building

TRGMUX can be seen as a collection of muxes, each mux allowing to select one output from a list of input signals that are common to all muxes. The TRGMUX registers are identical as structure and all bitfields can be read/written using the TRGMUX driver API.

TRGMUX Initialization

The [TRGMUX_DRV_Init\(\)](#) function is used to initialize the TRGMUX IP. The function receives as parameter a pointer to the [trgmux_user_config_t](#) structure. This structure contains a variable number of mappings between a trgmux trigger source and a trgmux target modules.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\drivers\src\trgmux\trgmux_driver.c
${S32SDK_PATH}\platform\drivers\src\trgmux\trgmux_hw_access.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

There are no dependencies with other components

TRGMUX API

After initialization, the driver allows the reconfiguration of the source trigger for a given target module using [TRGMUX_DRV_SetTrigSourceForTargetModule\(\)](#). Also, by using [TRGMUX_DRV_SetLockForTargetModule\(\)](#), a given target module can be locked, such that it cannot be updated until a reset.

Data Structures

- struct [trgmux_inout_mapping_config_t](#)
Configuration structure for pairing source triggers with target modules. [More...](#)
- struct [trgmux_user_config_t](#)

User configuration structure for the TRGMUX driver. [More...](#)

Typedefs

- typedef enum trgmux_trigger_source_e [trgmux_trigger_source_t](#)
Enumeration for trigger source module of TRGMUX.
- typedef enum trgmux_target_module_e [trgmux_target_module_t](#)
Enumeration for target module of TRGMUX.

Functions

- status_t [TRGMUX_DRV_Init](#) (const uint32_t instance, const [trgmux_user_config_t](#) *const trgmuxUserConfig)
Initialize a TRGMUX instance for operation.
- status_t [TRGMUX_DRV_Deinit](#) (const uint32_t instance)
Reset to default values the source triggers corresponding to all target modules, if none of the target modules is locked.
- status_t [TRGMUX_DRV_SetTrigSourceForTargetModule](#) (const uint32_t instance, const [trgmux_trigger_source_t](#) triggerSource, const [trgmux_target_module_t](#) targetModule)
Configure a source trigger for a selected target module.
- [trgmux_trigger_source_t](#) [TRGMUX_DRV_GetTrigSourceForTargetModule](#) (const uint32_t instance, const [trgmux_target_module_t](#) targetModule)
Get the source trigger configured for a target module.
- void [TRGMUX_DRV_SetLockForTargetModule](#) (const uint32_t instance, const [trgmux_target_module_t](#) targetModule)
Locks the TRGMUX register of a target module.
- bool [TRGMUX_DRV_GetLockForTargetModule](#) (const uint32_t instance, const [trgmux_target_module_t](#) targetModule)
Get the Lock bit status of the TRGMUX register of a target module.
- void [TRGMUX_DRV_GenSWTrigger](#) (const uint32_t instance)
Generate software triggers.

17.143.2 Data Structure Documentation

17.143.2.1 struct trgmux_inout_mapping_config_t

Configuration structure for pairing source triggers with target modules.

Use an instance of this structure to define a TRGMUX link between a trigger source and a target module. This structure is used by the user configuration structure.

Implements : [trgmux_inout_mapping_config_t_Class](#)

Definition at line 88 of file [trgmux_driver.h](#).

Data Fields

- [trgmux_trigger_source_t](#) triggerSource
- [trgmux_target_module_t](#) targetModule
- bool lockTargetModuleReg

Field Documentation

17.143.2.1.1 bool lockTargetModuleReg

if true, the LOCK bit of the target module register will be set by [TRGMUX_DRV_INIT\(\)](#), after the current mapping is configured

Definition at line 92 of file [trgmux_driver.h](#).

17.143.2.1.2 trgmux_target_module_t targetModule

selects one of the TRGMUX target modules

Definition at line 91 of file trgmux_driver.h.

17.143.2.1.3 trgmux_trigger_source_t triggerSource

selects one of the TRGMUX trigger sources

Definition at line 90 of file trgmux_driver.h.

17.143.2.2 struct trgmux_user_config_t

User configuration structure for the TRGMUX driver.

Use an instance of this structure with the [TRGMUX_DRV_Init\(\)](#) function. This enables configuration of TRGMUX with the user defined mappings between inputs (source triggers) and outputs (target modules), via a single function call.

Implements : trgmux_user_config_t_Class

Definition at line 104 of file trgmux_driver.h.

Data Fields

- [uint8_t numInOutMappingConfigs](#)
- [const trgmux_inout_mapping_config_t * inOutMappingConfig](#)

Field Documentation**17.143.2.2.1 const trgmux_inout_mapping_config_t* inOutMappingConfig**

pointer to array of in-out mapping structures

Definition at line 107 of file trgmux_driver.h.

17.143.2.2.2 uint8_t numInOutMappingConfigs

number of in-out mappings defined in TRGMUX configuration

Definition at line 106 of file trgmux_driver.h.

17.143.3 Typedef Documentation**17.143.3.1 typedef enum trgmux_target_module_e trgmux_target_module_t**

Enumeration for target module of TRGMUX.

Describes all possible outputs (target modules) of the TRGMUX IP This enumeration depends on the supported instances in device

Implements : trgmux_target_module_t_Class

Definition at line 78 of file trgmux_driver.h.

17.143.3.2 typedef enum trgmux_trigger_source_e trgmux_trigger_source_t

Enumeration for trigger source module of TRGMUX.

Describes all possible inputs (trigger sources) of the TRGMUX IP This enumeration depends on the supported instances in device

Implements : trgmux_trigger_source_t_Class

Definition at line 68 of file trgmux_driver.h.

17.143.4 Function Documentation

17.143.4.1 `status_t TRGMUX_DRV_Deinit (const uint32_t instance)`

Reset to default values the source triggers corresponding to all target modules, if none of the target modules is locked.

Parameters

<code>in</code>	<code>instance</code>	The TRGMUX instance number.
-----------------	-----------------------	-----------------------------

Returns

Execution status:

STATUS_SUCCESS

STATUS_ERROR - if at least one of the target module register is locked.

Definition at line 114 of file `trgmux_driver.c`.

17.143.4.2 `void TRGMUX_DRV_GenSWTrigger (const uint32_t instance)`

Generate software triggers.

This function uses a SIM register in order to generate a software triggers to the target peripherals selected in TRGMUX

Parameters

<code>param[in]</code>	<code>instance</code>	The TRGMUX instance number.
------------------------	-----------------------	-----------------------------

Definition at line 221 of file `trgmux_driver.c`.

17.143.4.3 `bool TRGMUX_DRV_GetLockForTargetModule (const uint32_t instance, const trgmux_target_module_t targetModule)`

Get the Lock bit status of the TRGMUX register of a target module.

This function gets the value of the LK bit from the TRGMUX register corresponding to the selected target module.

Parameters

<code>in</code>	<code>instance</code>	The TRGMUX instance number.
<code>in</code>	<code>targetModule</code>	One of the values in the <code>trgmux_target_module_t</code> enumeration

Returns

true - if the selected targetModule register is locked

false - if the selected targetModule register is not locked

Definition at line 203 of file `trgmux_driver.c`.

17.143.4.4 `trgmux_trigger_source_t TRGMUX_DRV_GetTrigSourceForTargetModule (const uint32_t instance, const trgmux_target_module_t targetModule)`

Get the source trigger configured for a target module.

This function returns the TRGMUX source trigger linked to a selected target module.

Parameters

in	<i>instance</i>	The TRGMUX instance number.
in	<i>targetModule</i>	One of the values in the <code>trgmux_target_module_t</code> enumeration.

Returns

Enum value corresponding to the trigger source configured for the selected target module.

Definition at line 168 of file `trgmux_driver.c`.

17.143.4.5 `status_t TRGMUX_DRV_Init (const uint32_t instance, const trgmux_user_config_t *const trgmuxUserConfig)`

Initialize a TRGMUX instance for operation.

This function first resets the source triggers of all TRGMUX target modules to their default values, then configures the TRGMUX with all the user defined in-out mappings. If at least one of the target modules is locked, the function will not change any of the TRGMUX target modules and return error code. This example shows how to set up the `trgmux_user_config_t` parameters and how to call the `TRGMUX_DRV_Init()` function with the required parameters:

```
1 trgmux_user_config_t      trgmuxConfig;
2 trgmux_inout_mapping_config_t trgmuxInoutMappingConfig[] =
3 {
4     {TRGMUX_TRIG_SOURCE_TRGMUX_IN9,    TRGMUX_TARGET_MODULE_DMA_CH0,    false},
5     {TRGMUX_TRIG_SOURCE_FTM1_EXT_TRIG, TRGMUX_TARGET_MODULE_TRGMUX_OUT4, true}
6 };
7
8 trgmuxConfig.numInOutMappingConfigs = 2;
9 trgmuxConfig.inOutMappingConfig     = trgmuxInoutMappingConfig;
10
11 TRGMUX_DRV_Init(instance, &trgmuxConfig);
```

Parameters

in	<i>instance</i>	The TRGMUX instance number.
in	<i>trgmuxUserConfig</i>	Pointer to the user configuration structure.

Returns

Execution status:

`STATUS_SUCCESS`

`STATUS_ERROR` - if at least one of the target module register is locked.

Definition at line 71 of file `trgmux_driver.c`.

17.143.4.6 `void TRGMUX_DRV_SetLockForTargetModule (const uint32_t instance, const trgmux_target_module_t targetModule)`

Locks the TRGMUX register of a target module.

This function sets the LK bit of the TRGMUX register corresponding to the selected target module. Please note that some TRGMUX registers can contain up to 4 SEL bitfields, meaning that these registers can be used to configure up to 4 target modules independently. Because the LK bit is only one per register, the configuration of all target modules referred from that register will be locked.

Parameters

in	<i>instance</i>	The TRGMUX instance number.
in	<i>targetModule</i>	One of the values in the <code>trgmux_target_module_t</code> enumeration

Definition at line 185 of file `trgmux_driver.c`.

17.143.4.7 `status_t TRGMUX_DRV_SetTrigSourceForTargetModule (const uint32_t instance, const trgmux_trigger_source_t triggerSource, const trgmux_target_module_t targetModule)`

Configure a source trigger for a selected target module.

This function configures a TRGMUX link between a source trigger and a target module, if the requested target module is not locked.

Parameters

<i>in</i>	<i>instance</i>	The TRGMUX instance number.
<i>in</i>	<i>triggerSource</i>	One of the values in the <code>trgmux_trigger_source_t</code> enumeration
<i>in</i>	<i>targetModule</i>	One of the values in the <code>trgmux_target_module_t</code> enumeration

Returns

Execution status:
STATUS_SUCCESS
STATUS_ERROR - if requested target module is locked

Definition at line 135 of file `trgmux_driver.c`.

17.144 Timing - Peripheral Abstraction Layer (TIMING PAL)

17.144.1 Detailed Description

The S32 SDK provides a Peripheral Abstraction Layer for timer modules of S32 SDK devices.

The TIMING PAL driver allows to generate period event. It was designed to be portable across all platforms and IPs which support LPIT, PIT, LPTMR, FTM, STM.

How to integrate TIMING PAL in your application

Unlike the other drivers, TIMING PAL modules need to include a configuration file named `timing_pal_cfg.h`, which allows the user to specify which IPs are used. The following code example shows how to configure one instance for each available TIMING IPs.

```
#ifndef TIMING_PAL_CFG_H
#define TIMING_PAL_CFG_H

/* Define which IP instance will be used in current project */
#define TIMING_OVER_LPIT
#define TIMING_OVER_FTM
#define TIMING_OVER_LPTMR

#endif /* TIMING_PAL_CFG_H */
```

The following table contains the matching between platforms and available IPs

LPIT PIT M CU	S32 K116	S32 K118	S32 K142	S32 K144	S32 K146	S32 K148	S32 K142 W	S32 K144 W	S32 V234	S32 R274	S32 R372	M P C5748 G	M P C5746 C	M P C5744 P
LPIT PIT M CU	YES	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO	NO	NO	NO
LPIT PIT M CU	YES	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO	NO	NO	NO

F↔ T↔ M↔ _↔ TI↔ M↔ I↔ NG	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	NO	NO	NO	NO	NO
PI↔ T↔ _↔ TI↔ M↔ I↔ NG	NO	NO	NO	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES
S↔ T↔ M↔ _↔ TI↔ M↔ I↔ NG	NO	NO	NO	NO	NO	NO	NO	NO	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES	Y↔ ES

Features

- Start timer channel counting with period in ticks function
- Generate one-shot or continuous notification(Event)
- Get elapsed time and remaining time functions
- Get tick resolution in engineering units (nanosecond, microsecond or millisecond)

Functionality

Initialization

In order to use the TIMING PAL driver it must be first initialized, using [TIMING_Init\(\)](#) function. Once initialized, it should be de-initialized before initialized again for the same TIMING module instance, using [TIMING_Deinit\(\)](#). The initialization function does the following operations:

- sets the clock source, clock prescaler (except LPIT, PIT_TIMING)
- sets notification type and callback function of timer channel Different TIMING modules instances can function independently of each other.

Start/Stop a timer channel counting with new period

After initialization, a timer channel can be started by calling [TIMING_StartChannel](#) function. The input period unit is ticks, the max value of period depends on which timer is used for timing. The [TIMING_StartChannel](#) function can be called consecutively, it starts new period immediately but in case LPIT, PIT_TIMING when timer channel is running, to abort the current timer channel period and start a timer channel period with a new value, the timer channel must be stopped and started again. A timer channel can be stop by calling [TIMING_StopChannel](#) function.

Get elapsed and remaining time

When a timer channel is running, the elapsed and remaining timer can be got by calling [TIMING_GetElapsed](#) and [TIMING_GetRemaining](#) function. The elapsed and remaining time in nanosecond, microsecond or millisecond is the result of this function multiplies by the result of the [TIMING_GetResolution](#).

Important Notes

- Before using the TIMING PAL driver the module clock must be configured. Refer to Clock Manager for clock configuration.
- The driver enables the interrupts for the corresponding TIMING module, but any interrupt priority must be done by the application
- When the vector table is not in ram (**flash_vector_table** = 1):
 - INT_SYS_InstallHandler shall check if the function pointer provided as parameter for the new handler is already present in the vector table for the given IRQ number.
 - The user will be required to manually add the correct handlers in the startup files
- The board specific configurations must be done prior to driver calls
- Some features are not available for all TIMING IPs and incorrect parameters will be handled by DEV_ASSERT
- Because of the driver code limit, when use FTM_TIMING or STM_TIMING the executing time of interrupt handler is about 4 microseconds, so the erroneous period is about 4 microsecond, should configure period enough to skip this erroneous period.
- In MPC574xG and MPC574xC devices, STM module has Errata e10200. If STM clock source is configured to use the FXOSC clock for the case application software reads the STM Count register(STM_CNT) while the counter is running, the value returned may be incorrect. Note the default clock source for the STM is the FS80 (divided system clock) and this configuration is working properly. Consequently the value returned by the function STM_DRV_GetCounterValue() may be incorrect when clock source is set to FXOSC option. Thus, this issue impacts to the functions that call STM_DRV_GetCounterValue() function:
 - TIMING_GetElapsed
 - TIMING_GetRemaining
 - TIMING_StartChannel only in case the timer is already started This issue should be taken care when using TIMING over STM.

Example code

```

/* The timer channel number */
#define TIMER_CHANNEL 0U

/* The timer channel period by nanosecond */
#define TIMER_PERIOD_NANO 1000000000U

/* Counting variable */
uint32_t count = 0;

/* Callback function */
void My_Callback(void * data)
{
    (void) data;
    count = count + 1;
}

/* Configure timer channel */
timer_chan_config_t timing_pall_channelArray[] =
{
    {
        TIMER_CHANNEL,
        TIMER_CHAN_TYPE_CONTINUOUS,
        My_Callback,
        NULL
    }
};

/* Configure FTM clock source */
extension_ftm_for_timer_t timing_pall_ftmExtension =
{
    FTM_CLOCK_SOURCE_FIXEDCLK,
    FTM_CLOCK_DIVID_BY_1,
    0xFFFF
};

/* Configure TIMING instance */

```

```

timer_config_t timing_pall_InitConfig =
{
    timing_pall_channelArray,
    1,
    &timing_pall_ftmExtention
};

/* TIMING instance number structure */
timing_instance_t instance =
{
    TIMING_INST_TYPE_LPIT,
    0U
};

int main(void)
{
    uint64_t resolution;
    uint32_t elapsedTime;

    /* Initialize TIMING */
    TIMING_Init(&instance, &timing_pall_InitConfig);

    /* Get tick resolution in nanosecond */
    TIMING_GetResolution(&instance,
        TIMER_RESOLUTION_TYPE_NANOSECOND, &resolution);

    /* Start channel counting with period is 1 second */
    TIMING_StartChannel(&instance, TIMER_CHANNEL, (TIMER_PERIOD_NANO / resolution));
    ....
    /* Get elapsed time in ticks */
    elapsedTime = TIMING_GetElapsed(&instance, TIMER_CHANNEL);

    /* Get elapsed time in nanosecond */
    elapsedTime = elapsedTime * resolution;

    /* De-initialize TIMING */
    TIMING_Deinit(&instance);
}

```

Integration guideline

Compilation units

The following files need to be compiled in the project:

```

${S32SDK_PATH}\platform\pal\src\timing\timing_pal.c
${S32SDK_PATH}\platform\pal\src\timing\timing_irq.c

```

Include path

The following paths need to be added to the include path of the toolchain:

```

${S32SDK_PATH}\platform\pal\inc\

```

Compile symbols

No special symbols are required for this component

Dependencies

Common: [Clock Manager](#) [Interrupt Manager](#) ([Interrupt](#))

S32K1xx: [Low Power Interrupt Timer \(LPIT\)](#) [Low Power Timer \(LPTMR\)](#) [FlexTimer \(FTM\)](#)

MPC574x and **S32Rx7x:** [pit stm](#)

Data Structures

- struct [timer_chan_config_t](#)
Structure to configure the channel timer notification. [More...](#)
- struct [timer_config_t](#)
Timer configuration structure. [More...](#)

- struct [extension_lptmr_for_timer_t](#)
Defines the extension structure for the timer over LPTMR. [More...](#)
- struct [extension_ftm_for_timer_t](#)
Defines the extension structure for the timer over FTM. [More...](#)

Enumerations

- enum [timer_resolution_type_t](#) { [TIMER_RESOLUTION_TYPE_NANOSECOND](#), [TIMER_RESOLUTION_TYPE_MICROSECOND](#), [TIMER_RESOLUTION_TYPE_MILLISECOND](#) }
Type options available for tick resolution.
- enum [timer_chan_type_t](#) { [TIMER_CHAN_TYPE_CONTINUOUS](#), [TIMER_CHAN_TYPE_ONESHOT](#) }
Type options available for timer channel notification.

Functions

- status_t [TIMING_Init](#) (const [timing_instance_t](#) *const instance, const [timer_config_t](#) *const config)
Initialize the timer instance and timer channels with value from input configuration structure.
- void [TIMING_Deinit](#) (const [timing_instance_t](#) *const instance)
De-initialize a timer instance.
- void [TIMING_StartChannel](#) (const [timing_instance_t](#) *const instance, const uint8_t channel, const uint32_t periodTicks)
Starts the timer channel counting.
- void [TIMING_StopChannel](#) (const [timing_instance_t](#) *const instance, const uint8_t channel)
Stop the timer channel counting.
- uint32_t [TIMING_GetElapsed](#) (const [timing_instance_t](#) *const instance, const uint8_t channel)
Get elapsed ticks.
- uint32_t [TIMING_GetRemaining](#) (const [timing_instance_t](#) *const instance, const uint8_t channel)
Get remaining ticks.
- void [TIMING_EnableNotification](#) (const [timing_instance_t](#) *const instance, const uint8_t channel)
Enable channel notifications.
- void [TIMING_DisableNotification](#) (const [timing_instance_t](#) *const instance, const uint8_t channel)
Disable channel notifications.
- status_t [TIMING_GetResolution](#) (const [timing_instance_t](#) *const instance, const [timer_resolution_type_t](#) type, uint64_t *const resolution)
Get tick resolution.
- status_t [TIMING_GetMaxPeriod](#) (const [timing_instance_t](#) *const instance, const [timer_resolution_type_t](#) type, uint64_t *const maxPeriod)
Get max period in engineering units.
- void [TIMING_InstallCallback](#) (const [timing_instance_t](#) *const instance, const uint8_t channel, const [timer_callback_t](#) callback, void *const callbackParam)
Installs callback function for the timer channel.

17.144.2 Data Structure Documentation

17.144.2.1 struct [timer_chan_config_t](#)

Structure to configure the channel timer notification.

This structure holds the configuration settings for the timer channel notification Implements : [timer_chan_config_t_Class](#)

Definition at line 77 of file [timing_pal.h](#).

Data Fields

- [uint8_t channel](#)
- [timer_chan_type_t chanType](#)
- [timer_callback_t callback](#)
- [void * callbackParam](#)

Field Documentation**17.144.2.1.1 timer_callback_t callback**

Callback function called on notification

Definition at line 81 of file timing_pal.h.

17.144.2.1.2 void* callbackParam

Callback parameter pointer

Definition at line 82 of file timing_pal.h.

17.144.2.1.3 uint8_t channel

Channel number

Definition at line 79 of file timing_pal.h.

17.144.2.1.4 timer_chan_type_t chanType

Continuous or One-shot

Definition at line 80 of file timing_pal.h.

17.144.2.2 struct timer_config_t

Timer configuration structure.

This structure holds the configuration settings for the timer Implements : timer_config_t_Class

Definition at line 91 of file timing_pal.h.

Data Fields

- [const timer_chan_config_t * chanConfigArray](#)
- [uint8_t numChan](#)
- [void * extension](#)

Field Documentation**17.144.2.2.1 const timer_chan_config_t* chanConfigArray**

Channel configuration array

Definition at line 93 of file timing_pal.h.

17.144.2.2.2 void* extension

IP specific configuration structure

Definition at line 95 of file timing_pal.h.

17.144.2.2.3 uint8_t numChan

Number of elements in chanConfigArray

Definition at line 94 of file timing_pal.h.

17.144.2.3 struct extension_lptmr_for_timer_t

Defines the extension structure for the timer over LPTMR.

Part of LPTMR configuration structure Implements : `extension_lptmr_for_timer_t_Class`

Definition at line 114 of file `timing_pal.h`.

Data Fields

- [lptmr_clocksource_t clockSelect](#)
- [lptmr_prescaler_t prescaler](#)
- `bool` [bypassPrescaler](#)

Field Documentation**17.144.2.3.1 bool bypassPrescaler**

Enable/Disable prescaler bypass

Definition at line 118 of file `timing_pal.h`.

17.144.2.3.2 lptmr_clocksource_t clockSelect

LPTMR clock source selection

Definition at line 116 of file `timing_pal.h`.

17.144.2.3.3 lptmr_prescaler_t prescaler

Prescaler Selection

Definition at line 117 of file `timing_pal.h`.

17.144.2.4 struct extension_ftm_for_timer_t

Defines the extension structure for the timer over FTM.

Part of FTM configuration structure Implements : `extension_ftm_for_timer_t_Class`

Definition at line 129 of file `timing_pal.h`.

Data Fields

- [ftm_clock_source_t clockSelect](#)
- [ftm_clock_ps_t prescaler](#)
- `uint16_t` [finalValue](#)

Field Documentation**17.144.2.4.1 ftm_clock_source_t clockSelect**

FTM clock source selection

Definition at line 131 of file `timing_pal.h`.

17.144.2.4.2 uint16_t finalValue

The final value of FTM counter

Definition at line 133 of file `timing_pal.h`.

17.144.2.4.3 ftm_clock_ps_t prescaler

Prescaler Selection

Definition at line 132 of file `timing_pal.h`.

17.144.3 Enumeration Type Documentation

17.144.3.1 enum timer_chan_type_t

Type options available for timer channel notification.

Implements : timer_chan_type_t_Class

Enumerator

TIMER_CHAN_TYPE_CONTINUOUS Timer channel creates continuous notification

TIMER_CHAN_TYPE_ONESHOT Timer channel creates one-shot notification

Definition at line 65 of file timing_pal.h.

17.144.3.2 enum timer_resolution_type_t

Type options available for tick resolution.

Implements : timer_resolution_type_t_Class

Enumerator

TIMER_RESOLUTION_TYPE_NANOSECOND Tick resolution is nanosecond

TIMER_RESOLUTION_TYPE_MICROSECOND Tick resolution is microsecond

TIMER_RESOLUTION_TYPE_MILLISECOND Tick resolution is millisecond

Definition at line 53 of file timing_pal.h.

17.144.4 Function Documentation

17.144.4.1 void TIMING_Deinit (const timing_instance_t *const instance)

De-initialize a timer instance.

This function de-initializes timer instance. In order to use the timer instance again, TIMING_Init must be called.

Parameters

in	instance	The pointer to timer instance number structure
----	----------	--

Definition at line 604 of file timing_pal.c.

17.144.4.2 void TIMING_DisableNotification (const timing_instance_t *const instance, const uint8_t channel)

Disable channel notifications.

This function disables channel notification.

Parameters

in	instance	The pointer to timer instance number structure
in	channel	The channel number

Definition at line 1390 of file timing_pal.c.

17.144.4.3 void TIMING_EnableNotification (const timing_instance_t *const instance, const uint8_t channel)

Enable channel notifications.

This function enables channel notification.

Parameters

in	<i>instance</i>	The pointer to timer instance number structure
in	<i>channel</i>	The channel number

Definition at line 1292 of file timing_pal.c.

17.144.4.4 `uint32_t TIMING_GetElapsed (const timing_instance_t *const instance, const uint8_t channel)`

Get elapsed ticks.

This function gets elapsed time of the current period by ticks. The elapsed time by nanosecond, microsecond or millisecond is the result of this function multiplies by the result of the TIMING_GetResolution function. Note that: If the timer channel type is continuous, this function may not return value of the period at the moment period is timeout depending on timer frequency, optimizations, etc. The behavior occurs if the execution time of the function is significant relative to timer tick duration. If the timer channel type is one-shot, this function can be used to check whether the current period is timeout, in this case if the returned value is bigger or equal than the period, the current period is timeout or overflowed.

Parameters

in	<i>instance</i>	The pointer to timer instance number structure
in	<i>channel</i>	The channel number

Returns

Number of ticks elapsed of the current period

Definition at line 956 of file timing_pal.c.

17.144.4.5 `status_t TIMING_GetMaxPeriod (const timing_instance_t *const instance, const timer_resolution_type_t type, uint64_t *const maxPeriod)`

Get max period in engineering units.

This function gets max period in engineering units.

Parameters

in	<i>instance</i>	The pointer to timer instance number structure
in	<i>type</i>	Resolution type
out	<i>maxPeriod</i>	The pointer to max period in engineering units

Returns

Operation status

- STATUS_SUCCESS: Operation was successful
- STATUS_ERROR : The timer frequency is not fit to resolution type

Definition at line 1627 of file timing_pal.c.

17.144.4.6 `uint32_t TIMING_GetRemaining (const timing_instance_t *const instance, const uint8_t channel)`

Get remaining ticks.

This function gets remaining time of the current period by ticks. The remaining time by nanosecond, microsecond or millisecond is the result of this function multiplies by the result of the TIMING_GetResolution function. Note that: If the timer channel type is continuous, this function may not return 0 at the moment period is timeout depending on timer frequency, optimizations, etc. The behavior occurs if the execution time of the function is significant relative to timer tick duration. If the timer channel type is one-shot, this function can be used to check whether the current period is timeout, in this case if the returned value is 0, the current period is timeout or overflowed.

Parameters

in	<i>instance</i>	The pointer to timer instance number structure
in	<i>channel</i>	The channel number

Returns

Number of ticks remaining of the current period

Definition at line 1127 of file timing_pal.c.

17.144.4.7 `status_t TIMING_GetResolution (const timing_instance_t *const instance, const timer_resolution_type_t type, uint64_t *const resolution)`

Get tick resolution.

This function gets tick resolution in engineering units (nanosecond, microsecond or millisecond). The result of this function is used to calculate period, remaining time or elapsed time in engineering units.

Parameters

in	<i>instance</i>	The pointer to timer instance number structure
in	<i>type</i>	Resolution type
out	<i>resolution</i>	The pointer to resolution in engineering units

Returns

Operation status

- STATUS_SUCCESS: Operation was successful
- STATUS_ERROR : The timer frequency is not fit to resolution type

Definition at line 1481 of file timing_pal.c.

17.144.4.8 `status_t TIMING_Init (const timing_instance_t *const instance, const timer_config_t *const config)`

Initialize the timer instance and timer channels with value from input configuration structure.

This function initializes clock source, prescaler of the timer instance(except LPIT, PIT), the final value of counter (only FTM). This function also setups notification type and callback function of timer channel. The timer instance number and its configuration structure shall be passed as arguments. Timer channels do not start counting by default after calling this function. The function TIMING_StartChannel must be called to start the timer channel counting.

Parameters

in	<i>instance</i>	The pointer to timer instance number structure
in	<i>config</i>	The pointer to configuration structure

Returns

Operation status

- STATUS_SUCCESS: Operation was successful
- STATUS_ERROR : Operation was fail if the timer instance is out of range For example: Timing over LPIT but the instance is not LPIT instance(TIMING_OVER_LPIT0_INSTANCE)
- STATUS_ERROR : Operation was fail if the FTM instance has been initialized

Definition at line 526 of file timing_pal.c.

17.144.4.9 void TIMING_InstallCallback (const timing_instance_t *const *instance*, const uint8_t *channel*, const timer_callback_t *callback*, void *const *callbackParam*)

Installs callback function for the timer channel.

This function installs new callback function and callback parameter for the timer channel event. This function allows changing the callback function and parameter while the timer channel is running. If the provided callback function parameter is NULL, it is equivalent to removing the callback.

Parameters

in	<i>instance</i>	The pointer to timer instance number structure
in	<i>callback</i>	The new callback function for timer channel
in	<i>callbackParam</i>	The new callback parameter pointer

Definition at line 1785 of file timing_pal.c.

17.144.4.10 void TIMING_StartChannel (const timing_instance_t *const *instance*, const uint8_t *channel*, const uint32_t *periodTicks*)

Starts the timer channel counting.

This function starts channel counting with a new period in ticks. Note that:

- If the timer is PIT or LPIT, to abort the current timer channel period and start a timer channel period with a new value, the timer channel must be stopped and started again.
- If the timer is FTM, this function start channel by enable channel interrupt generation.
- LPTMR and FTM is 16 bit timer, so the input period must be smaller than 65535.
- LPTMR and FTM is 16 bit timer, so the input period must be smaller than 65535.

Parameters

in	<i>instance</i>	The pointer to timer instance number structure
in	<i>channel</i>	The channel number
in	<i>periodTicks</i>	The input period in ticks

Definition at line 678 of file timing_pal.c.

17.144.4.11 void TIMING_StopChannel (const timing_instance_t *const *instance*, const uint8_t *channel*)

Stop the timer channel counting.

This function stop channel counting. Note that if the timer is FTM, this function stop channel by disable channel interrupt generation.

Parameters

in	<i>instance</i>	The pointer to timer instance number structure
in	<i>channel</i>	The channel number

Definition at line 854 of file timing_pal.c.

17.145 Transceiver interrupt enable configuration options (0x23)

17.145.1 Detailed Description

This section lists all the possible options of 0x23 register related to:

- CAN bus silence interrupt
- LIN 2 wake-up interrupt
- LIN 1 wake-up interrupt
- CAN failure interrupt
- CAN wake-up interrupt

See also

[UJA113X_SetTransceiverInterrupts\(\)](#)

CAN bus silence interrupt configuration options (0x23:CBSIE[4])

- #define [CBSIE_DISABLE](#) 0x00U
Disable CAN bus silence interrupt.
- #define [CBSIE_ENABLE](#) 0x10U
Enable CAN bus silence interrupt.

LIN 2 wake-up interrupt configuration options (0x23:LWI2E[3])

- #define [L2WIE_DISABLE](#) 0x00U
Disable LIN 2 wake-up interrupt.
- #define [L2WIE_ENABLE](#) 0x08U
Enable LIN 2 wake-up interrupt.

LIN 1 wake-up interrupt configuration options (0x23:LWI1E[2])

- #define [L1WIE_DISABLE](#) 0x00U
Disable LIN 1 wake-up interrupt.
- #define [L1WIE_ENABLE](#) 0x04U
Enable LIN 1 wake-up interrupt.

CAN failure interrupt configuration options (0x23:CFIE[1])

- #define [CFIE_DISABLE](#) 0x00U
Disable CAN failure interrupt.
- #define [CFIE_ENABLE](#) 0x02U
Enable CAN failure interrupt.

CAN wake-up interrupt configuration options (0x23:CWIE[0])

- #define [CWIE_DISABLE](#) 0x00U
Disable CAN wake-up interrupt.
- #define [CWIE_ENABLE](#) 0x01U
Enable CAN wake-up interrupt.

17.145.2 Macro Definition Documentation

17.145.2.1 `#define CBSIE_DISABLE 0x00U`

Disable CAN bus silence interrupt.

Definition at line 718 of file `sbc_uja113x.h`.

17.145.2.2 `#define CBSIE_ENABLE 0x10U`

Enable CAN bus silence interrupt.

Definition at line 719 of file `sbc_uja113x.h`.

17.145.2.3 `#define CFIE_DISABLE 0x00U`

Disable CAN failure interrupt.

Definition at line 739 of file `sbc_uja113x.h`.

17.145.2.4 `#define CFIE_ENABLE 0x02U`

Enable CAN failure interrupt.

Definition at line 740 of file `sbc_uja113x.h`.

17.145.2.5 `#define CWIE_DISABLE 0x00U`

Disable CAN wake-up interrupt.

Definition at line 746 of file `sbc_uja113x.h`.

17.145.2.6 `#define CWIE_ENABLE 0x01U`

Enable CAN wake-up interrupt.

Definition at line 747 of file `sbc_uja113x.h`.

17.145.2.7 `#define L1WIE_DISABLE 0x00U`

Disable LIN 1 wake-up interrupt.

Definition at line 732 of file `sbc_uja113x.h`.

17.145.2.8 `#define L1WIE_ENABLE 0x04U`

Enable LIN 1 wake-up interrupt.

Definition at line 733 of file `sbc_uja113x.h`.

17.145.2.9 `#define L2WIE_DISABLE 0x00U`

Disable LIN 2 wake-up interrupt.

Definition at line 725 of file `sbc_uja113x.h`.

17.145.2.10 `#define L2WIE_ENABLE 0x08U`

Enable LIN 2 wake-up interrupt.

Definition at line 726 of file `sbc_uja113x.h`.

17.146 Transport layer API

17.146.1 Detailed Description

Transport layer stands between the application layer and the core API layer.

This layer consists the implementation of data transportation which contains one or more LIN frames. It is situated between the application layer and the core API layer including LIN2.1 TL API and LIN TL J2602. This layer provides APIs for the transport protocol, node configuration and diagnostic services. For LIN 2.1, all components will be extended from LIN 2.0 specification. The node configuration for J2602 implements only some functions of LIN 2.0 specification.

Modules

- [Common Transport Layer API](#)

Contains Transport Layer APIs that used for both protocols LIN 2.1 and J2602.

- [J2602 Transport Layer specific API](#)

Contains Transport Layer APIs that only used for J2602 protocol.

17.147 UJA116xA SBC Driver

17.147.1 Detailed Description

Data Structures

- struct [sbc_wdog_ctr_t](#)
Watchdog control register structure. Watchdog configuration structure. [More...](#)
- struct [sbc_sbc_t](#)
SBC configuration control register structure. Two operating modes have a major impact on the operation of the watchdog: Forced Normal mode and Software Development mode (Software Development mode is provided for test and development purposes only and is not a dedicated SBC operating mode; the UJA116xA can be in any functional operating mode with Software Development mode enabled). These modes are enabled and disabled via bits FNMC and SDMC respectively in the SBC configuration control register. Note that this register is located in the non-volatile memory area. The watchdog is disabled in Forced Normal mode (FNM). In Software Development mode (SDM), the watchdog can be disabled or activated for test and software debugging purposes. [More...](#)
- struct [sbc_start_up_t](#)
Start-up control register structure. This structure contains settings of RSTN output reset pulse width and V2/VEXT start-up control. [More...](#)
- struct [sbc_regulator_t](#)
Regulator control register structure. This structure set power distribution control, V2/VEXT configuration, set V1 reset threshold. [More...](#)
- struct [sbc_supply_evt_t](#)
Supply event capture enable register structure. This structure enables or disables detection of V2/VEXT overvoltage, undervoltage and V1 undervoltage enable. [More...](#)
- struct [sbc_sys_evt_t](#)
System event capture enable register structure. This structure enables or disables overtemperature warning, SPI failure enable. [More...](#)
- struct [sbc_can_ctr_t](#)
CAN control register structure. This structure configure CAN peripheral behavior. [More...](#)
- struct [sbc_trans_evt_t](#)
Transceiver event capture enable register structure. Can bus silence, Can failure and Can wake-up settings. [More...](#)
- struct [sbc_frame_t](#)
Frame control register structure. The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register. [More...](#)
- struct [sbc_can_conf_t](#)
CAN configuration group structure. This structure configure CAN peripheral behavior. [More...](#)
- struct [sbc_wake_t](#)
WAKE pin event capture enable register structure. Local wake-up is enabled via bits WPRE and WPFE in the WAKE pin event capture enable register. A wake-up event is triggered by a LOW-to-HIGH (if WPRE = 1) and/or a HIGH-to-LOW (if WPFE = 1) transition on the WAKE pin. This arrangement allows for maximum flexibility when designing a local wake-up circuit. In applications that do not use the local wake-up facility, local wake-up should be disabled and the WAKE pin connected to GND. [More...](#)
- struct [sbc_regulator_ctr_t](#)
Regulator control register group. This structure is group of regulator settings. [More...](#)
- struct [sbc_int_config_t](#)
Init configuration structure. This structure is used for initialization of sbc. [More...](#)
- struct [sbc_factories_conf_t](#)
Factory configuration structure. It contains Start-up control register and SBC configuration control register. This is non-volatile memory with limited write access. The MTPNV cells can be reprogrammed a maximum of 200 times (Ncy(W)MTP; Bit NVMPs in the MTPNV status register indicates whether the non-volatile cells can be reprogrammed. This register also contains a write counter, WRCNTS, that is incremented each time the MTPNV cells are reprogrammed (up to a maximum value of 111111; there is no overflow; performing a factory reset also increments the counter). This counter is provided for information purposes only; reprogramming will not be rejected when it reaches its maximum value. Factory preset values are restored if the following conditions apply continuously for at least td(MTPNV) during battery power-up: pin RSTN is held LOW, CANH is pulled up to VBAT, CANL is pulled down to

GND After the factory preset values have been restored, the SBC performs a system reset and enters Forced normal Mode. Since the CAN-bus is clamped dominant, pin RXDC is forced LOW. Pin RXD is forced HIGH during the factory preset restore process (td(MTPNV)). A falling edge on RXD caused by bit PO being set after power-on indicates that the factory preset process has been completed. Note that the write counter, WRCNTS, in the MTPNV status register is incremented every time the factory presets are restored. [More...](#)

- struct [sbc_main_status_t](#)

Main status register structure. The Main status register can be accessed to monitor the status of the overtemperature warning flag and to determine whether the UJA116xA has entered Normal mode after initial power-up. It also indicates the source of the most recent reset event. [More...](#)

- struct [sbc_wtdog_status_t](#)

Watchdog status register structure. Information on the status of the watchdog is available from the Watchdog status register. This register also indicates whether Forced Normal and Software Development modes are active. [More...](#)

- struct [sbc_supply_status_t](#)

Supply voltage status register structure. V2/VEXT and V1 undervoltage and overvoltage status. [More...](#)

- struct [sbc_trans_stat_t](#)

Transceiver status register structure. There are stored CAN transceiver statuses. [More...](#)

- struct [sbc_gl_evnt_stat_t](#)

Global event status register. The microcontroller can monitor events via the event status registers. An extra status register, the Global event status register, is provided to help speed up software polling routines. By polling the Global event status register, the microcontroller can quickly determine the type of event captured (system, supply, transceiver or WAKE pin) and then query the relevant event status register. [More...](#)

- struct [sbc_sys_evnt_stat_t](#)

System event status register. Wake-up and interrupt event diagnosis in the UJA116xA is intended to provide the microcontroller with information on the status of a range of features and functions. This information is stored in the event status registers and is signaled on pin RXD, if enabled. [More...](#)

- struct [sbc_sup_evnt_stat_t](#)

Supply event status register. [More...](#)

- struct [sbc_trans_evnt_stat_t](#)

Transceiver event status register. [More...](#)

- struct [sbc_wake_evnt_stat_t](#)

WAKE pin event status register. [More...](#)

- struct [sbc_evn_capt_t](#)

Event capture registers structure. This structure contains Global event status, System event status, Supply event status, Transceiver event status, WAKE pin event status. [More...](#)

- struct [sbc_mtpnv_stat_t](#)

MTPNV status register. The MTPNV cells can be reprogrammed a maximum of 200 times (Ncy(W)MTP). Bit N_{VMPS} in the MTPNV status register indicates whether the non-volatile cells can be reprogrammed. This register also contains a write counter, WRCNTS, that is incremented each time the MTPNV cells are reprogrammed (up to a maximum value of 111111; there is no overflow; performing a factory reset also increments the counter). This counter is provided for information purposes only; reprogramming will not be rejected when it reaches its maximum value. [More...](#)

- struct [sbc_status_group_t](#)

Status group structure. All statuses of SBC are stored in this structure. [More...](#)

Macros

- #define [SBC_UJA_TIMEOUT](#) 1000U
- #define [SBC_UJA_COUNT_ID_REG](#) 4U
- #define [SBC_UJA_COUNT_MASK](#) 4U
- #define [SBC_UJA_COUNT_DMASK](#) 8U

Typedefs

- typedef uint8_t [sbc_fail_safe_rcc_t](#)
Fail-safe control register, reset counter control (0x02). incremented every time the SBC enters Reset mode while FNMC = 0; RCC overflows from 11 to 00; default at power-on is 00.
- typedef uint8_t [sbc_identifier_t](#)
ID registers, identifier format (0x27 to 0x2A). A valid WUF identifier is defined and stored in the ID registers. An ID mask can be defined to allow a group of identifiers to be recognized as valid by an individual node.
- typedef uint8_t [sbc_identif_mask_t](#)
ID mask registers (0x2B to 0x2E). The identifier mask is defined in the ID mask registers, where a 1 means dont care.
- typedef uint8_t [sbc_frame_ctr_dlc_t](#)
Frame control register, number of data bytes expected in a CAN frame (0x2F).
- typedef uint8_t [sbc_data_mask_t](#)
Data mask registers. The data field indicates the nodes to be woken up. Within the data field, groups of nodes can be predefined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.
- typedef uint8_t [sbc_mtpnv_stat_wrnts_t](#)
MTPNV status register, write counter status (0x70). 6-bits - contains the number of times the MTPNV cells were reprogrammed.

Enumerations

- enum [sbc_register_t](#) {
[SBC_UJA_WTDOG_CTR](#) = 0x00U, [SBC_UJA_MODE](#) = 0x01U, [SBC_UJA_FAIL_SAFE](#) = 0x02U, [SBC_UJA_MAIN](#) = 0x03U,
[SBC_UJA_SYSTEM_EVNT](#) = 0x04U, [SBC_UJA_WTDOG_STAT](#) = 0x05U, [SBC_UJA_MEMORY_0](#) = 0x06U, [SBC_UJA_MEMORY_1](#) = 0x07U,
[SBC_UJA_MEMORY_2](#) = 0x08U, [SBC_UJA_MEMORY_3](#) = 0x09U, [SBC_UJA_LOCK](#) = 0x0AU, [SBC_UJA_REGULATOR](#) = 0x0BU,
[SBC_UJA_SUPPLY_STAT](#) = 0x0CU, [SBC_UJA_SUPPLY_EVNT](#) = 0x0DU, [SBC_UJA_CAN](#) = 0x0EU, [SBC_UJA_TRANS_STAT](#) = 0x0FU,
[SBC_UJA_TRANS_EVNT](#) = 0x10U, [SBC_UJA_DAT_RATE](#) = 0x11U, [SBC_UJA_IDENTIF_0](#) = 0x12U, [SBC_UJA_IDENTIF_1](#) = 0x13U,
[SBC_UJA_IDENTIF_2](#) = 0x14U, [SBC_UJA_IDENTIF_3](#) = 0x15U, [SBC_UJA_MASK_0](#) = 0x16U, [SBC_UJA_MASK_1](#) = 0x17U,
[SBC_UJA_MASK_2](#) = 0x18U, [SBC_UJA_MASK_3](#) = 0x19U, [SBC_UJA_FRAME_CTR](#) = 0x1AU, [SBC_UJA_DAT_MASK_0](#) = 0x1BU,
[SBC_UJA_DAT_MASK_1](#) = 0x1CU, [SBC_UJA_DAT_MASK_2](#) = 0x1DU, [SBC_UJA_DAT_MASK_3](#) = 0x1EU, [SBC_UJA_DAT_MASK_4](#) = 0x1FU,
[SBC_UJA_DAT_MASK_5](#) = 0x20U, [SBC_UJA_DAT_MASK_6](#) = 0x21U, [SBC_UJA_DAT_MASK_7](#) = 0x22U, [SBC_UJA_WAKE_STAT](#) = 0x23U,
[SBC_UJA_WAKE_EN](#) = 0x24U, [SBC_UJA_GL_EVNT_STAT](#) = 0x25U, [SBC_UJA_SYS_EVNT_STAT](#) = 0x26U, [SBC_UJA_SUP_EVNT_STAT](#) = 0x27U,
[SBC_UJA_TRANS_EVNT_STAT](#) = 0x28U, [SBC_UJA_WAKE_EVNT_STAT](#) = 0x29U, [SBC_UJA_MTPNV_STAT](#) = 0x2AU, [SBC_UJA_START_UP](#) = 0x2BU,
[SBC_UJA_SBC](#) = 0x2CU, [SBC_UJA_MTPNV_CRC](#) = 0x2DU, [SBC_UJA_IDENTIF](#) = 0x2EU }
Register map.
- enum [sbc_wtdog_ctr_wmc_t](#) { [SBC_UJA_WTDOG_CTR_WMC_AUTO](#) = [SBC_UJA_WTDOG_CTR_WMC_F\(1U\)](#), [SBC_UJA_WTDOG_CTR_WMC_TIME](#) = [SBC_UJA_WTDOG_CTR_WMC_F\(2U\)](#), [SBC_UJA_WTDOG_CTR_WMC_WIND](#) = [SBC_UJA_WTDOG_CTR_WMC_F\(4U\)](#) }
Watchdog control register, watchdog mode control (0x00). The UJA116xA contains a watchdog that supports three operating modes: Window, Timeout and Autonomous. In Window mode (available only in SBC Normal mode), a watchdog trigger event within a defined watchdog window triggers and resets the watchdog timer. In Timeout mode, the watchdog runs continuously and can be triggered and reset at any time within the watchdog period by a watchdog trigger. Watchdog time-out mode can also be used for cyclic wake-up of the microcontroller. In Autonomous mode, the watchdog can be off or autonomously in Timeout mode, depending on the selected SBC mode. The watchdog mode

is selected via bits WMC in the Watchdog control register. The SBC must be in Standby mode when the watchdog mode is changed.

- enum `sbc_wtdog_ctr_nwp_t` {
`SBC_UJA_WTD OG_CTR_NWP_8` = 0x08U, `SBC_UJA_WTD OG_CTR_NWP_16` = 0x01U, `SBC_UJA_WTD OG_CTR_NWP_32` = 0x02U, `SBC_UJA_WTD OG_CTR_NWP_64` = 0x0BU,
`SBC_UJA_WTD OG_CTR_NWP_128` = 0x04U, `SBC_UJA_WTD OG_CTR_NWP_256` = 0x0DU, `SBC_UJA_WTD OG_CTR_NWP_1024` = 0x0EU, `SBC_UJA_WTD OG_CTR_NWP_4096` = 0x07U }

Watchdog control register, nominal watchdog period (0x00). Eight watchdog periods are supported, from 8 ms to 4096 ms. The watchdog period is programmed via bits NWP. The selected period is valid for both Window and Timeout modes. The default watchdog period is 128 ms. A watchdog trigger event resets the watchdog timer. A watchdog trigger event is any valid write access to the Watchdog control register. If the watchdog mode or the watchdog period have changed as a result of the write access, the new values are immediately valid.

- enum `sbc_mode_mc_t` { `SBC_UJA_MODE_MC_SLEEP` = 0x01U, `SBC_UJA_MODE_MC_STANDBY` = 0x04U, `SBC_UJA_MODE_MC_NORMAL` = 0x07U }

Mode control register, mode control (0x01)

- enum `sbc_fail_safe_lhc_t` { `SBC_UJA_FAIL_SAFE_LHC_FLOAT` = `SBC_UJA_FAIL_SAFE_LHC_F(0U)`, `SBC_UJA_FAIL_SAFE_LHC_LOW` = `SBC_UJA_FAIL_SAFE_LHC_F(1U)` }

Fail-safe control register, LIMP home control (0x02). The dedicated LIMP pin can be used to enable so called limp home hardware in the event of a serious ECU failure. Detectable failure conditions include SBC overtemperature events, loss of watchdog service, short-circuits on pins RSTN or V1 and user-initiated or external reset events. The LIMP pin is a battery-robust, active-LOW, open-drain output. The LIMP pin can also be forced LOW by setting bit LHC in the Fail-safe control register.

- enum `sbc_main_otws_t` { `SBC_UJA_MAIN_OTWS_BELOW` = `SBC_UJA_MAIN_OTWS_F(0U)`, `SBC_UJA_MAIN_OTWS_ABOVE` = `SBC_UJA_MAIN_OTWS_F(1U)` }

Main status register, Overtemperature warning status (0x03).

- enum `sbc_main_nms_t` { `SBC_UJA_MAIN_NMS_NORMAL` = `SBC_UJA_MAIN_NMS_F(0U)`, `SBC_UJA_MAIN_NMS_PWR_UP` = `SBC_UJA_MAIN_NMS_F(1U)` }

Main status register, normal mode status (0x03).

- enum `sbc_main_rss_t` {
`SBC_UJA_MAIN_RSS_OFF_MODE` = 0x00U, `SBC_UJA_MAIN_RSS_CAN_WAKEUP` = 0x01U, `SBC_UJA_MAIN_RSS_SLP_WAKEUP` = 0x04U, `SBC_UJA_MAIN_RSS_OVF_SLP` = 0x0CU,
`SBC_UJA_MAIN_RSS_DIAG_WAKEUP` = 0x0DU, `SBC_UJA_MAIN_RSS_WATCH_TRIG` = 0x0EU, `SBC_UJA_MAIN_RSS_WATCH_OVF` = 0x0FU, `SBC_UJA_MAIN_RSS_ILLEG_WATCH` = 0x10U,
`SBC_UJA_MAIN_RSS_RSTN_PULDW` = 0x11U, `SBC_UJA_MAIN_RSS_LFT_OVERTM` = 0x12U, `SBC_UJA_MAIN_RSS_V1_UNDERV` = 0x13U, `SBC_UJA_MAIN_RSS_ILLEG_SLP` = 0x14U,
`SBC_UJA_MAIN_RSS_WAKE_SLP` = 0x16U }

Main status register, Reset source status (0x03).

- enum `sbc_sys_evnt_otwe_t` { `SBC_UJA_SYS_EVNT_OTWE_DIS` = `SBC_UJA_SYS_EVNT_OTWE_F(0U)`, `SBC_UJA_SYS_EVNT_OTWE_EN` = `SBC_UJA_SYS_EVNT_OTWE_F(1U)` }

System event capture enable, overtemperature warning enable (0x04).

- enum `sbc_sys_evnt_spipe_t` { `SBC_UJA_SYS_EVNT_SPIFE_DIS` = `SBC_UJA_SYS_EVNT_SPIFE_F(0U)`, `SBC_UJA_SYS_EVNT_SPIFE_EN` = `SBC_UJA_SYS_EVNT_SPIFE_F(1U)` }

System event capture enable, SPI failure enable (0x04).

- enum `sbc_wtdog_stat_fnms_t` { `SBC_UJA_WTD OG_STAT_FNMS_N_NORMAL` = `SBC_UJA_WTD OG_STAT_FNMS_F(0U)`, `SBC_UJA_WTD OG_STAT_FNMS_NORMAL` = `SBC_UJA_WTD OG_STAT_FNMS_F(1U)` }

Watchdog status register, forced Normal mode status (0x05).

- enum `sbc_wtdog_stat_sdms_t` { `SBC_UJA_WTD OG_STAT_SDMS_N_NORMAL` = `SBC_UJA_WTD OG_STAT_SDMS_F(0U)`, `SBC_UJA_WTD OG_STAT_SDMS_NORMAL` = `SBC_UJA_WTD OG_STAT_SDMS_F(1U)` }

Watchdog status register, Software Development mode status (0x05).

- enum `sbc_wtdog_stat_wds_t` { `SBC_UJA_WTD OG_STAT_WDS_OFF` = `SBC_UJA_WTD OG_STAT_WDS_F(0U)`, `SBC_UJA_WTD OG_STAT_WDS_FIH` = `SBC_UJA_WTD OG_STAT_WDS_F(1U)`, `SBC_UJA_WTD OG_STAT_WDS_SEH` = `SBC_UJA_WTD OG_STAT_WDS_F(2U)` }

Watchdog status register, watchdog status (0x05).

- enum `sbc_lock_t` {
`LK0C` = SBC_UJA_LOCK_LK0C_MASK, `LK1C` = SBC_UJA_LOCK_LK1C_MASK, `LK2C` = SBC_UJA_LOCK_LK2C_MASK, `LK3C` = SBC_UJA_LOCK_LK3C_MASK,
`LK4C` = SBC_UJA_LOCK_LK4C_MASK, `LK5C` = SBC_UJA_LOCK_LK5C_MASK, `LK6C` = SBC_UJA_LOCK_LK6C_MASK, `LKAC` = SBC_UJA_LOCK_LKNC_MASK }
Lock control(0x0A). Sections of the register address area can be write-protected to protect against unintended modifications. This facility only protects locked bits from being modified via the SPI and will not prevent the UJA116xA updating status registers etc.
- enum `sbc_regulator_pdc_t` { `SBC_UJA_REGULATOR_PDC_HV` = SBC_UJA_REGULATOR_PDC_F(0U),
`SBC_UJA_REGULATOR_PDC_LV` = SBC_UJA_REGULATOR_PDC_F(1U) }
Regulator control register, power distribution control (0x10). PDC is not available on UJA1168 device variants, use any of these two values, the value written to the device will be ignored.
- enum `sbc_regulator_v2c_t` { `SBC_UJA_REGULATOR_V2C_OFF` = SBC_UJA_REGULATOR_V2C_F(0U),
`SBC_UJA_REGULATOR_V2C_N` = SBC_UJA_REGULATOR_V2C_F(1U), `SBC_UJA_REGULATOR_V2C_N_S_S_R` = SBC_UJA_REGULATOR_V2C_F(2U), `SBC_UJA_REGULATOR_V2C_N_S_S_R` = SBC_UJA_REGULATOR_V2C_F(3U) }
Regulator control register, V2/VEXT configuration (0x10).
- enum `sbc_regulator_v1rtc_t` { `SBC_UJA_REGULATOR_V1RTC_90` = SBC_UJA_REGULATOR_V1RTC_F(0U), `SBC_UJA_REGULATOR_V1RTC_80` = SBC_UJA_REGULATOR_V1RTC_F(1U), `SBC_UJA_REGULATOR_V1RTC_70` = SBC_UJA_REGULATOR_V1RTC_F(2U), `SBC_UJA_REGULATOR_V1RTC_60` = SBC_UJA_REGULATOR_V1RTC_F(3U) }
Regulator control register, set V1 reset threshold (0x10).
- enum `sbc_supply_stat_v2s_t` { `SBC_UJA_SUPPLY_STAT_V2S_VOK` = SBC_UJA_SUPPLY_STAT_V2S_F(0U), `SBC_UJA_SUPPLY_STAT_V2S_VBE` = SBC_UJA_SUPPLY_STAT_V2S_F(1U), `SBC_UJA_SUPPLY_STAT_V2S_VAB` = SBC_UJA_SUPPLY_STAT_V2S_F(2U), `SBC_UJA_SUPPLY_STAT_V2S_DIS` = SBC_UJA_SUPPLY_STAT_V2S_F(3U) }
Supply voltage status register, V2/VEXT status (0x1B).
- enum `sbc_supply_stat_v1s_t` { `SBC_UJA_SUPPLY_STAT_V1S_VAB` = SBC_UJA_SUPPLY_STAT_V1S_F(0U), `SBC_UJA_SUPPLY_STAT_V1S_VBE` = SBC_UJA_SUPPLY_STAT_V1S_F(1U) }
Supply voltage status register, V1 status (0x1B).
- enum `sbc_supply_evnt_v2oe_t` { `SBC_UJA_SUPPLY_EVNT_V2OE_DIS` = SBC_UJA_SUPPLY_EVNT_V2OE_F(0U), `SBC_UJA_SUPPLY_EVNT_V2OE_EN` = SBC_UJA_SUPPLY_EVNT_V2OE_F(1U) }
Supply event capture enable register, V2/VEXT overvoltage enable (0x1C).
- enum `sbc_supply_evnt_v2ue_t` { `SBC_UJA_SUPPLY_EVNT_V2UE_DIS` = SBC_UJA_SUPPLY_EVNT_V2UE_F(0U), `SBC_UJA_SUPPLY_EVNT_V2UE_EN` = SBC_UJA_SUPPLY_EVNT_V2UE_F(1U) }
Supply event capture enable register, V2/VEXT undervoltage enable (0x1C).
- enum `sbc_supply_evnt_v1ue_t` { `SBC_UJA_SUPPLY_EVNT_V1UE_DIS` = SBC_UJA_SUPPLY_EVNT_V1UE_F(0U), `SBC_UJA_SUPPLY_EVNT_V1UE_EN` = SBC_UJA_SUPPLY_EVNT_V1UE_F(1U) }
Supply event capture enable register, V1 undervoltage enable (0x1C).
- enum `sbc_can_cfdc_t` { `SBC_UJA_CAN_CFDC_DIS` = SBC_UJA_CAN_CFDC_F(0U), `SBC_UJA_CAN_CFDC_EN` = SBC_UJA_CAN_CFDC_F(1U) }
CAN control register, CAN FD control (0x20).
- enum `sbc_can_pncok_t` { `SBC_UJA_CAN_PNCOK_DIS` = SBC_UJA_CAN_PNCOK_F(0U), `SBC_UJA_CAN_PNCOK_EN` = SBC_UJA_CAN_PNCOK_F(1U) }
CAN control register, CAN partial networking configuration OK (0x20).
- enum `sbc_can_cpnc_t` { `SBC_UJA_CAN_CPNC_DIS` = SBC_UJA_CAN_CPNC_F(0U), `SBC_UJA_CAN_CPNC_EN` = SBC_UJA_CAN_CPNC_F(1U) }
CAN control register, CAN partial networking control (0x20).
- enum `sbc_can_cmc_t` { `SBC_UJA_CAN_CMC_OFMODE` = SBC_UJA_CAN_CMC_F(0U), `SBC_UJA_CAN_CMC_ACMODE_DA` = SBC_UJA_CAN_CMC_F(1U), `SBC_UJA_CAN_CMC_ACMODE_DD` = SBC_UJA_CAN_CMC_F(2U), `SBC_UJA_CAN_CMC_LISTEN` = SBC_UJA_CAN_CMC_F(3U) }
CAN control register, CAN mode control (0x20).
- enum `sbc_trans_stat_cts_t` { `SBC_UJA_TRANS_STAT_CTS_INACT` = SBC_UJA_TRANS_STAT_CTS_F(0U), `SBC_UJA_TRANS_STAT_CTS_ACT` = SBC_UJA_TRANS_STAT_CTS_F(1U) }

Transceiver status register, CAN transceiver status (0x22).

- enum `sbc_trans_stat_cpnrerr_t` { `SBC_UJA_TRANS_STAT_CPNRERR_NO_DET` = `SBC_UJA_TRANS_STAT_CPNRERR_F(0U)`, `SBC_UJA_TRANS_STAT_CPNRERR_DET` = `SBC_UJA_TRANS_STAT_CPNRERR_F(1U)` }

Transceiver status register, CAN partial networking error (0x22).

- enum `sbc_trans_stat_cpns_t` { `SBC_UJA_TRANS_STAT_CPNS_ERR` = `SBC_UJA_TRANS_STAT_CPNS_F(0U)`, `SBC_UJA_TRANS_STAT_CPNS_OK` = `SBC_UJA_TRANS_STAT_CPNS_F(1U)` }

Transceiver status register, CAN partial networking status (0x22).

- enum `sbc_trans_stat_coscs_t` { `SBC_UJA_TRANS_STAT_COSCS_NRUN` = `SBC_UJA_TRANS_STAT_COSCS_F(0U)`, `SBC_UJA_TRANS_STAT_COSCS_RUN` = `SBC_UJA_TRANS_STAT_COSCS_F(1U)` }

Transceiver status register, CAN oscillator status (0x22).

- enum `sbc_trans_stat_cbss_t` { `SBC_UJA_TRANS_STAT_CBSS_ACT` = `SBC_UJA_TRANS_STAT_CBSS_F(0U)`, `SBC_UJA_TRANS_STAT_CBSS_INACT` = `SBC_UJA_TRANS_STAT_CBSS_F(1U)` }

Transceiver status register, CAN-bus silence status (0x22).

- enum `sbc_trans_stat_vcs_t` { `SBC_UJA_TRANS_STAT_VCS_AB` = `SBC_UJA_TRANS_STAT_VCS_F(0U)`, `SBC_UJA_TRANS_STAT_VCS_BE` = `SBC_UJA_TRANS_STAT_VCS_F(1U)` }

Transceiver status register, VCAN status (0x22).

- enum `sbc_trans_stat_cfs_t` { `SBC_UJA_TRANS_STAT_CFS_NO_TXD` = `SBC_UJA_TRANS_STAT_CFS_F(0U)`, `SBC_UJA_TRANS_STAT_CFS_TXD` = `SBC_UJA_TRANS_STAT_CFS_F(1U)` }

Transceiver status register, CAN failure status (0x22).

- enum `sbc_trans_evt_cbse_t` { `SBC_UJA_TRANS_EVT_CBSE_DIS` = `SBC_UJA_TRANS_EVT_CBSE_F(0U)`, `SBC_UJA_TRANS_EVT_CBSE_EN` = `SBC_UJA_TRANS_EVT_CBSE_F(1U)` }

Transceiver event capture enable register, CAN-bus silence enable (0x23).

- enum `sbc_trans_evt_cfe_t` { `SBC_UJA_TRANS_EVT_CFE_DIS` = `SBC_UJA_TRANS_EVT_CFE_F(0U)`, `SBC_UJA_TRANS_EVT_CFE_EN` = `SBC_UJA_TRANS_EVT_CFE_F(1U)` }

Transceiver event capture enable register, CAN failure enable (0x23).

- enum `sbc_trans_evt_cwe_t` { `SBC_UJA_TRANS_EVT_CWE_DIS` = `SBC_UJA_TRANS_EVT_CWE_F(0U)`, `SBC_UJA_TRANS_EVT_CWE_EN` = `SBC_UJA_TRANS_EVT_CWE_F(1U)` }

Transceiver event capture enable register, CAN wake-up enable (0x23).

- enum `sbc_dat_rate_t` { `SBC_UJA_DAT_RATE_CDR_50KB` = `SBC_UJA_DAT_RATE_CDR_F(0U)`, `SBC_UJA_DAT_RATE_CDR_100KB` = `SBC_UJA_DAT_RATE_CDR_F(1U)`, `SBC_UJA_DAT_RATE_CDR_125KB` = `SBC_UJA_DAT_RATE_CDR_F(2U)`, `SBC_UJA_DAT_RATE_CDR_250KB` = `SBC_UJA_DAT_RATE_CDR_F(3U)`, `SBC_UJA_DAT_RATE_CDR_500KB` = `SBC_UJA_DAT_RATE_CDR_F(5U)`, `SBC_UJA_DAT_RATE_CDR_1000KB` = `SBC_UJA_DAT_RATE_CDR_F(7U)` }

Data rate register, CAN data rate selection (0x26). CAN partial networking configuration registers. Dedicated registers are provided for configuring CAN partial networking.

- enum `sbc_frame_ctr_ide_t` { `SBC_UJA_FRAME_CTR_IDE_11B` = `SBC_UJA_FRAME_CTR_IDE_F(0U)`, `SBC_UJA_FRAME_CTR_IDE_29B` = `SBC_UJA_FRAME_CTR_IDE_F(1U)` }

Frame control register, identifier format (0x2F). The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register.

- enum `sbc_frame_ctr_pndm_t` { `SBC_UJA_FRAME_CTR_PNDM_DCARE` = `SBC_UJA_FRAME_CTR_PNDM_F(0U)`, `SBC_UJA_FRAME_CTR_PNDM_EVAL` = `SBC_UJA_FRAME_CTR_PNDM_F(1U)` }

Frame control register, partial networking data mask (0x2F).

- enum `sbc_wake_stat_wpvs_t` { `SBC_UJA_WAKE_STAT_WPVS_BE` = `SBC_UJA_WAKE_STAT_WPVS_F(0U)`, `SBC_UJA_WAKE_STAT_WPVS_AB` = `SBC_UJA_WAKE_STAT_WPVS_F(1U)` }

WAKE pin status register, WAKE pin status (0x4B).

- enum `sbc_wake_en_wpre_t` { `SBC_UJA_WAKE_EN_WPRE_DIS` = `SBC_UJA_WAKE_EN_WPRE_F(0U)`, `SBC_UJA_WAKE_EN_WPRE_EN` = `SBC_UJA_WAKE_EN_WPRE_F(1U)` }

WAKE pin event capture enable register, WAKE pin rising-edge enable (0x4C).

- enum `sbc_wake_en_wpfe_t` { `SBC_UJA_WAKE_EN_WPFE_DIS` = `SBC_UJA_WAKE_EN_WPFE_F(0U)`, `SBC_UJA_WAKE_EN_WPFE_EN` = `SBC_UJA_WAKE_EN_WPFE_F(1U)` }

WAKE pin event capture enable register, WAKE pin falling-edge enable (0x4C).

- enum `sbcb_gl_evnt_stat_wpe_t` { `SBC_UJA_GL_EVNT_STAT_WPE_NO` = `SBC_UJA_GL_EVNT_STAT_WPE_F(0U)`, `SBC_UJA_GL_EVNT_STAT_WPE` = `SBC_UJA_GL_EVNT_STAT_WPE_F(1U)` }
Global event status register, WAKE pin event (0x60).
- enum `sbcb_gl_evnt_stat_trxe_t` { `SBC_UJA_GL_EVNT_STAT_TRXE_NO` = `SBC_UJA_GL_EVNT_STAT_TRXE_F(0U)`, `SBC_UJA_GL_EVNT_STAT_TRXE` = `SBC_UJA_GL_EVNT_STAT_TRXE_F(1U)` }
Global event status register, transceiver event (0x60).
- enum `sbcb_gl_evnt_stat_supe_t` { `SBC_UJA_GL_EVNT_STAT_SUPE_NO` = `SBC_UJA_GL_EVNT_STAT_SUPE_F(0U)`, `SBC_UJA_GL_EVNT_STAT_SUPE` = `SBC_UJA_GL_EVNT_STAT_SUPE_F(1U)` }
Global event status register, supply event (0x60).
- enum `sbcb_gl_evnt_stat_syse_t` { `SBC_UJA_GL_EVNT_STAT_SYSE_NO` = `SBC_UJA_GL_EVNT_STAT_SYSE_F(0U)`, `SBC_UJA_GL_EVNT_STAT_SYSE` = `SBC_UJA_GL_EVNT_STAT_SYSE_F(1U)` }
Global event status register, system event (0x60).
- enum `sbcb_sys_evnt_stat_po_t` { `SBC_UJA_SYS_EVNT_STAT_PO_NO` = `SBC_UJA_SYS_EVNT_STAT_PO_F(0U)`, `SBC_UJA_SYS_EVNT_STAT_PO` = `SBC_UJA_SYS_EVNT_STAT_PO_F(1U)` }
System event status register, power-on (0x61).
- enum `sbcb_sys_evnt_stat_otw_t` { `SBC_UJA_SYS_EVNT_STAT_OTW_NO` = `SBC_UJA_SYS_EVNT_STAT_OTW_F(0U)`, `SBC_UJA_SYS_EVNT_STAT_OTW` = `SBC_UJA_SYS_EVNT_STAT_OTW_F(1U)` }
System event status register, overtemperature warning (0x61).
- enum `sbcb_sys_evnt_stat_spif_t` { `SBC_UJA_SYS_EVNT_STAT_SPIF_NO` = `SBC_UJA_SYS_EVNT_STAT_SPIF_F(0U)`, `SBC_UJA_SYS_EVNT_STAT_SPIF` = `SBC_UJA_SYS_EVNT_STAT_SPIF_F(1U)` }
System event status register, SPI failure (0x61).
- enum `sbcb_sys_evnt_stat_wdf_t` { `SBC_UJA_SYS_EVNT_STAT_WDF_NO` = `SBC_UJA_SYS_EVNT_STAT_WDF_F(0U)`, `SBC_UJA_SYS_EVNT_STAT_WDF` = `SBC_UJA_SYS_EVNT_STAT_WDF_F(1U)` }
System event status register, watchdog failure (0x61).
- enum `sbcb_sup_evnt_stat_v2o_t` { `SBC_UJA_SUP_EVNT_STAT_V2O_NO` = `SBC_UJA_SUP_EVNT_STAT_V2O_F(0U)`, `SBC_UJA_SUP_EVNT_STAT_V2O` = `SBC_UJA_SUP_EVNT_STAT_V2O_F(1U)` }
Supply event status register, V2/VEXT overvoltage (0x62).
- enum `sbcb_sup_evnt_stat_v2u_t` { `SBC_UJA_SUP_EVNT_STAT_V2U_NO` = `SBC_UJA_SUP_EVNT_STAT_V2U_F(0U)`, `SBC_UJA_SUP_EVNT_STAT_V2U` = `SBC_UJA_SUP_EVNT_STAT_V2U_F(1U)` }
Supply event status register, V2/VEXT undervoltage (0x62).
- enum `sbcb_sup_evnt_stat_v1u_t` { `SBC_UJA_SUP_EVNT_STAT_V1U_NO` = `SBC_UJA_SUP_EVNT_STAT_V1U_F(0U)`, `SBC_UJA_SUP_EVNT_STAT_V1U` = `SBC_UJA_SUP_EVNT_STAT_V1U_F(1U)` }
Supply event status register, V1 undervoltage (0x62).
- enum `sbcb_trans_evnt_stat_pnfde_t` { `SBC_UJA_TRANS_EVNT_STAT_PNFDE_NO` = `SBC_UJA_TRANS_EVNT_STAT_PNFDE_F(0U)`, `SBC_UJA_TRANS_EVNT_STAT_PNFDE` = `SBC_UJA_TRANS_EVNT_STAT_PNFDE_F(1U)` }
Transceiver event status register, partial networking frame detection error (0x63).
- enum `sbcb_trans_evnt_stat_cbs_t` { `SBC_UJA_TRANS_EVNT_STAT_CBS_NO` = `SBC_UJA_TRANS_EVNT_STAT_CBS_F(0U)`, `SBC_UJA_TRANS_EVNT_STAT_CBS` = `SBC_UJA_TRANS_EVNT_STAT_CBS_F(1U)` }
Transceiver event status register, CAN-bus status (0x63).
- enum `sbcb_trans_evnt_stat_cf_t` { `SBC_UJA_TRANS_EVNT_STAT_CF_NO` = `SBC_UJA_TRANS_EVNT_STAT_CF_F(0U)`, `SBC_UJA_TRANS_EVNT_STAT_CF` = `SBC_UJA_TRANS_EVNT_STAT_CF_F(1U)` }
Transceiver event status register, CAN failure (0x63).
- enum `sbcb_trans_evnt_stat_cw_t` { `SBC_UJA_TRANS_EVNT_STAT_CW_NO` = `SBC_UJA_TRANS_EVNT_STAT_CW_F(0U)`, `SBC_UJA_TRANS_EVNT_STAT_CW` = `SBC_UJA_TRANS_EVNT_STAT_CW_F(1U)` }
Transceiver event status register, CAN wake-up (0x63).
- enum `sbcb_wake_evnt_stat_wpr_t` { `SBC_UJA_WAKE_EVNT_STAT_WPR_NO` = `SBC_UJA_WAKE_EVNT_STAT_WPR_F(0U)`, `SBC_UJA_WAKE_EVNT_STAT_WPR` = `SBC_UJA_WAKE_EVNT_STAT_WPR_F(1U)` }
WAKE pin event status register, WAKE pin rising edge (0x64).

- enum [sbc_wake_evnt_stat_wpf_t](#) { [SBC_UJA_WAKE_EVNT_STAT_WPF_NO](#) = SBC_UJA_WAKE_EVNT_STAT_WPF_F(0U), [SBC_UJA_WAKE_EVNT_STAT_WPF](#) = SBC_UJA_WAKE_EVNT_STAT_WPF_F(1U) }
WAKE pin event status register, WAKE pin falling edge (0x64).
- enum [sbc_mtpnv_stat_eccs_t](#) { [SBC_UJA_MTPNV_STAT_ECCS_NO](#) = SBC_UJA_MTPNV_STAT_ECCS_F(0U), [SBC_UJA_MTPNV_STAT_ECCS](#) = SBC_UJA_MTPNV_STAT_ECCS_F(1U) }
MTPNV status register, error correction code status (0x70).
- enum [sbc_mtpnv_stat_nvmps_t](#) { [SBC_UJA_MTPNV_STAT_NVMP_NO](#) = SBC_UJA_MTPNV_STAT_NVMP_F(0U), [SBC_UJA_MTPNV_STAT_NVMP](#) = SBC_UJA_MTPNV_STAT_NVMP_F(1U) }
MTPNV status register, non-volatile memory programming status (0x70).
- enum [sbc_start_up_rlc_t](#) { [SBC_UJA_START_UP_RLC_20_25p0](#) = SBC_UJA_START_UP_RLC_F(0U), [SBC_UJA_START_UP_RLC_10_12p5](#) = SBC_UJA_START_UP_RLC_F(1U), [SBC_UJA_START_UP_RLC_03p6_05](#) = SBC_UJA_START_UP_RLC_F(2U), [SBC_UJA_START_UP_RLC_01_01p5](#) = SBC_UJA_START_UP_RLC_F(3U) }
Start-up control register, RSTN output reset pulse width macros (0x73).
- enum [sbc_start_up_v2suc_t](#) { [SBC_UJA_START_UP_V2SUC_00](#) = SBC_UJA_START_UP_V2SUC_F(0U), [SBC_UJA_START_UP_V2SUC_11](#) = SBC_UJA_START_UP_V2SUC_F(1U) }
Start-up control register, V2/VEXT start-up control (0x73).
- enum [sbc_sbc_v1rtsuc_t](#) { [SBC_UJA_SBC_V1RTSUC_90](#) = SBC_UJA_SBC_V1RTSUC_F(0U), [SBC_UJA_SBC_V1RTSUC_80](#) = SBC_UJA_SBC_V1RTSUC_F(1U), [SBC_UJA_SBC_V1RTSUC_70](#) = SBC_UJA_SBC_V1RTSUC_F(2U), [SBC_UJA_SBC_V1RTSUC_60](#) = SBC_UJA_SBC_V1RTSUC_F(3U) }
SBC configuration control register, V1 undervoltage threshold (defined by bit V1RTC) at start-up (0x74).
- enum [sbc_sbc_fnmc_t](#) { [SBC_UJA_SBC_FNMC_DIS](#) = SBC_UJA_SBC_FNMC_F(0U), [SBC_UJA_SBC_FNMC_EN](#) = SBC_UJA_SBC_FNMC_F(1U) }
SBC configuration control register, Forced Normal mode control (0x74).
- enum [sbc_sbc_sdmc_t](#) { [SBC_UJA_SBC_SDMC_DIS](#) = SBC_UJA_SBC_SDMC_F(0U), [SBC_UJA_SBC_SDMC_EN](#) = SBC_UJA_SBC_SDMC_F(1U) }
SBC configuration control register, Software Development mode control (0x74).
- enum [sbc_sbc_slpc_t](#) { [SBC_UJA_SBC_SLPC_AC](#) = SBC_UJA_SBC_SLPC_F(0U), [SBC_UJA_SBC_SLPC_IG](#) = SBC_UJA_SBC_SLPC_F(1U) }
SBC configuration control register, Sleep control (0x74).

17.147.2 Data Structure Documentation

17.147.2.1 struct [sbc_wtdog_ctr_t](#)

Watchdog control register structure. Watchdog configuration structure.

Implements : [sbc_wtdog_ctr_t_Class](#)

Definition at line 1086 of file [sbc_uja116x_driver.h](#).

Data Fields

- [sbc_wtdog_ctr_wmc_t](#) modeControl
- [sbc_wtdog_ctr_nwp_t](#) nominalPeriod

Field Documentation

17.147.2.1.1 [sbc_wtdog_ctr_wmc_t](#) modeControl

Watchdog mode control.

Definition at line 1087 of file [sbc_uja116x_driver.h](#).

17.147.2.1.2 **sbc_wtdog_ctr_nwp_t** nominalPeriod

Nominal watchdog period.

Definition at line 1088 of file sbc_uja116x_driver.h.

17.147.2.2 **struct sbc_sbc_t**

SBC configuration control register structure. Two operating modes have a major impact on the operation of the watchdog: Forced Normal mode and Software Development mode (Software Development mode is provided for test and development purposes only and is not a dedicated SBC operating mode; the UJA116xA can be in any functional operating mode with Software Development mode enabled). These modes are enabled and disabled via bits FNMC and SDMC respectively in the SBC configuration control register. Note that this register is located in the non-volatile memory area. The watchdog is disabled in Forced Normal mode (FNM). In Software Development mode (SDM), the watchdog can be disabled or activated for test and software debugging purposes.

Implements : `sbc_sbc_t_Class`

Definition at line 1107 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_sbc_v1rtsuc_t v1rtsuc](#)
- [sbc_sbc_fnmc_t fnmc](#)
- [sbc_sbc_sdmc_t sdmc](#)
- [sbc_sbc_slpc_t slpc](#)

Field Documentation

17.147.2.2.1 **sbc_sbc_fnmc_t** fnmc

Forced Normal mode control.

Definition at line 1110 of file sbc_uja116x_driver.h.

17.147.2.2.2 **sbc_sbc_sdmc_t** sdmc

Software Development mode control.

Definition at line 1111 of file sbc_uja116x_driver.h.

17.147.2.2.3 **sbc_sbc_slpc_t** slpc

Sleep control.

Definition at line 1113 of file sbc_uja116x_driver.h.

17.147.2.2.4 **sbc_sbc_v1rtsuc_t** v1rtsuc

V1 undervoltage threshold (defined by bit V1RTC) at start-up (0x74).

Definition at line 1108 of file sbc_uja116x_driver.h.

17.147.2.3 **struct sbc_start_up_t**

Start-up control register structure. This structure contains settings of RSTN output reset pulse width and V2/VEXT start-up control.

Implements : `sbc_start_up_t_Class`

Definition at line 1123 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_start_up_rlc_t rlc](#)
- [sbc_start_up_v2suc_t v2suc](#)

Field Documentation

17.147.2.3.1 `sbc_start_up_rlc_t rlc`

RSTN output reset pulse width macros.

Definition at line 1124 of file `sbc_uja116x_driver.h`.

17.147.2.3.2 `sbc_start_up_v2suc_t v2suc`

V2/VEXT start-up control.

Definition at line 1126 of file `sbc_uja116x_driver.h`.

17.147.2.4 `struct sbc_regulator_t`

Regulator control register structure. This structure set power distribution control, V2/VEXT configuration, set V1 reset threshold.

Implements : `sbc_regulator_t_Class`

Definition at line 1136 of file `sbc_uja116x_driver.h`.

Data Fields

- [sbc_regulator_pdc_t pdc](#)
- [sbc_regulator_v2c_t v2c](#)
- [sbc_regulator_v1rtc_t v1rtc](#)

Field Documentation

17.147.2.4.1 `sbc_regulator_pdc_t pdc`

Power distribution control.

Definition at line 1137 of file `sbc_uja116x_driver.h`.

17.147.2.4.2 `sbc_regulator_v1rtc_t v1rtc`

Set V1 reset threshold.

Definition at line 1139 of file `sbc_uja116x_driver.h`.

17.147.2.4.3 `sbc_regulator_v2c_t v2c`

V2/VEXT configuration.

Definition at line 1138 of file `sbc_uja116x_driver.h`.

17.147.2.5 `struct sbc_supply_evnt_t`

Supply event capture enable register structure. This structure enables or disables detection of V2/VEXT overvoltage, undervoltage and V1 undervoltage enable.

Implements : `sbc_supply_evnt_t_Class`

Definition at line 1149 of file `sbc_uja116x_driver.h`.

Data Fields

- [sbc_supply_evnt_v2oe_t v2oe](#)
- [sbc_supply_evnt_v2ue_t v2ue](#)
- [sbc_supply_evnt_v1ue_t v1ue](#)

Field Documentation

17.147.2.5.1 sbc_supply_evnt_v1ue_t v1ue

SV1 undervoltage enable.

Definition at line 1152 of file sbc_uja116x_driver.h.

17.147.2.5.2 sbc_supply_evnt_v2oe_t v2oe

V2/VEXT overvoltage enable.

Definition at line 1150 of file sbc_uja116x_driver.h.

17.147.2.5.3 sbc_supply_evnt_v2ue_t v2ue

V2/VEXT undervoltage enable.

Definition at line 1151 of file sbc_uja116x_driver.h.

17.147.2.6 struct sbc_sys_evnt_t

System event capture enable register structure. This structure enables or disables overtemperature warning, SPI failure enable.

Implements : sbc_sys_evnt_t_Class

Definition at line 1162 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_sys_evnt_otwe_t otwe](#)
- [sbc_sys_evnt_spife_t spife](#)

Field Documentation**17.147.2.6.1 sbc_sys_evnt_otwe_t otwe**

Overtemperature warning enable.

Definition at line 1163 of file sbc_uja116x_driver.h.

17.147.2.6.2 sbc_sys_evnt_spife_t spife

SPI failure enable.

Definition at line 1164 of file sbc_uja116x_driver.h.

17.147.2.7 struct sbc_can_ctr_t

CAN control register structure. This structure configure CAN peripheral behavior.

Implements : sbc_can_ctr_t_Class

Definition at line 1173 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_can_cfdc_t cfdc](#)
- [sbc_can_pncok_t pncok](#)
- [sbc_can_cpnc_t cpnc](#)
- [sbc_can_cmc_t cmc](#)

Field Documentation**17.147.2.7.1 sbc_can_cfdc_t cfdc**

CAN FD control.

Definition at line 1174 of file sbc_uja116x_driver.h.

17.147.2.7.2 `sbc_can_cmc_t cmc`

CAN mode control.

Definition at line 1179 of file sbc_uja116x_driver.h.

17.147.2.7.3 `sbc_can_cpnc_t cpnc`

CAN partial. networking control.

Definition at line 1177 of file sbc_uja116x_driver.h.

17.147.2.7.4 `sbc_can_pncok_t pncok`

CAN partial networking. configuration OK.

Definition at line 1175 of file sbc_uja116x_driver.h.

17.147.2.8 `struct sbc_trans_evnt_t`

Transceiver event capture enable register structure. Can bus silence, Can failure and Can wake-up settings.

Implements : `sbc_trans_evnt_t_Class`

Definition at line 1188 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_trans_evnt_cbse_t cbse](#)
- [sbc_trans_evnt_cfe_t cfe](#)
- [sbc_trans_evnt_cwe_t cwe](#)

Field Documentation

17.147.2.8.1 `sbc_trans_evnt_cbse_t cbse`

CAN-bus silence enable.

Definition at line 1189 of file sbc_uja116x_driver.h.

17.147.2.8.2 `sbc_trans_evnt_cfe_t cfe`

CAN failure enable.

Definition at line 1190 of file sbc_uja116x_driver.h.

17.147.2.8.3 `sbc_trans_evnt_cwe_t cwe`

CAN wake-up enable.

Definition at line 1191 of file sbc_uja116x_driver.h.

17.147.2.9 `struct sbc_frame_t`

Frame control register structure. The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register.

Implements : `sbc_frame_t_Class`

Definition at line 1201 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_frame_ctr_ide_t ide](#)

- [sbc_frame_ctr_pndm_t pndm](#)
- [sbc_frame_ctr_dlc_t dlc](#)

Field Documentation

17.147.2.9.1 [sbc_frame_ctr_dlc_t dlc](#)

Number of data bytes expected.

Definition at line 1204 of file sbc_uja116x_driver.h.

17.147.2.9.2 [sbc_frame_ctr_ide_t ide](#)

Identifier format.

Definition at line 1202 of file sbc_uja116x_driver.h.

17.147.2.9.3 [sbc_frame_ctr_pndm_t pndm](#)

Partial networking data mask.

Definition at line 1203 of file sbc_uja116x_driver.h.

17.147.2.10 [struct sbc_can_conf_t](#)

CAN configuration group structure. This structure configure CAN peripheral behavior.

Implements : [sbc_can_conf_t_Class](#)

Definition at line 1213 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_can_ctr_t canConf](#)
- [sbc_trans_evnt_t canTransEvt](#)
- [sbc_dat_rate_t datRate](#)
- [sbc_identifier_t identif](#) [SBC_UJA_COUNT_ID_REG]
- [sbc_identif_mask_t mask](#) [SBC_UJA_COUNT_MASK]
- [sbc_frame_t frame](#)
- [sbc_data_mask_t dataMask](#) [SBC_UJA_COUNT_DMASK]

Field Documentation

17.147.2.10.1 [sbc_can_ctr_t canConf](#)

CAN control register.

Definition at line 1214 of file sbc_uja116x_driver.h.

17.147.2.10.2 [sbc_trans_evnt_t canTransEvt](#)

Transceiver event capture enable register.

Definition at line 1215 of file sbc_uja116x_driver.h.

17.147.2.10.3 [sbc_data_mask_t dataMask](#)[SBC_UJA_COUNT_DMASK]

Data mask 0 - 7 configuration.

Definition at line 1221 of file sbc_uja116x_driver.h.

17.147.2.10.4 [sbc_dat_rate_t datRate](#)

CAN data rate selection.

Definition at line 1217 of file sbc_uja116x_driver.h.

17.147.2.10.5 sbc_frame_t frame

Frame control register.

Definition at line 1220 of file sbc_uja116x_driver.h.

17.147.2.10.6 sbc_identifier_t identif[SBC_UJA_COUNT_ID_REG]

ID registers.

Definition at line 1218 of file sbc_uja116x_driver.h.

17.147.2.10.7 sbc_identif_mask_t mask[SBC_UJA_COUNT_MASK]

ID mask registers.

Definition at line 1219 of file sbc_uja116x_driver.h.

17.147.2.11 struct sbc_wake_t

WAKE pin event capture enable register structure. Local wake-up is enabled via bits WPRE and WPFE in the WAKE pin event capture enable register. A wake-up event is triggered by a LOW-to-HIGH (if WPRE = 1) and/or a HIGH-to-LOW (if WPFE = 1) transition on the WAKE pin. This arrangement allows for maximum flexibility when designing a local wake-up circuit. In applications that do not use the local wake-up facility, local wake-up should be disabled and the WAKE pin connected to GND.

Implements : sbc_wake_t_Class

Definition at line 1236 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_wake_en_wpre_t wpre](#)
- [sbc_wake_en_wpfe_t wpfe](#)

Field Documentation**17.147.2.11.1 sbc_wake_en_wpfe_t wpfe**

WAKE pin falling-edge enable.

Definition at line 1238 of file sbc_uja116x_driver.h.

17.147.2.11.2 sbc_wake_en_wpre_t wpre

WAKE pin rising-edge enable.

Definition at line 1237 of file sbc_uja116x_driver.h.

17.147.2.12 struct sbc_regulator_ctr_t

Regulator control register group. This structure is group of regulator settings.

Implements : sbc_regulator_ctr_t_Class

Definition at line 1247 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_regulator_t regulator](#)
- [sbc_supply_evnt_t supplyEvnt](#)

Field Documentation

17.147.2.12.1 sbc_regulator_t regulator

Regulator control register.

Definition at line 1248 of file sbc_uja116x_driver.h.

17.147.2.12.2 sbc_supply_evnt_t supplyEvt

Supply event capture enable register.

Definition at line 1249 of file sbc_uja116x_driver.h.

17.147.2.13 struct sbc_int_config_t

Init configuration structure. This structure is used for initialization of sbc.

Implements : sbc_int_config_t_Class

Definition at line 1259 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_regulator_ctr_t regulatorCtr](#)
- [sbc_wtdog_ctr_t watchdog](#)
- [sbc_mode_mc_t mode](#)
- [sbc_fail_safe_lhc_t lhc](#)
- [sbc_sys_evnt_t sysEvt](#)
- [sbc_lock_t lockMask](#)
- [sbc_can_conf_t can](#)
- [sbc_wake_t wakePin](#)

Field Documentation**17.147.2.13.1 sbc_can_conf_t can**

CAN configuration group.

Definition at line 1267 of file sbc_uja116x_driver.h.

17.147.2.13.2 sbc_fail_safe_lhc_t lhc

LIMP home control.

Definition at line 1263 of file sbc_uja116x_driver.h.

17.147.2.13.3 sbc_lock_t lockMask

Lock control register.

Definition at line 1266 of file sbc_uja116x_driver.h.

17.147.2.13.4 sbc_mode_mc_t mode

Mode control register.

Definition at line 1262 of file sbc_uja116x_driver.h.

17.147.2.13.5 sbc_regulator_ctr_t regulatorCtr

Regulator control register group.

Definition at line 1260 of file sbc_uja116x_driver.h.

17.147.2.13.6 sbc_sys_evnt_t sysEvt

System event capture enable registers.

Definition at line 1264 of file sbc_uja116x_driver.h.

17.147.2.13.7 `sbc_wake_t` wakePin

WAKE pin event capture enable register.

Definition at line 1268 of file sbc_uja116x_driver.h.

17.147.2.13.8 `sbc_wtdog_ctr_t` watchdog

Watchdog control register.

Definition at line 1261 of file sbc_uja116x_driver.h.

17.147.2.14 `struct sbc_factories_conf_t`

Factory configuration structure. It contains Start-up control register and SBC configuration control register. This is non-volatile memory with limited write access. The MTPNV cells can be reprogrammed a maximum of 200 times (Ncy(W)MTP; Bit NVMPs in the MTPNV status register indicates whether the non-volatile cells can be reprogrammed. This register also contains a write counter, WRCNTS, that is incremented each time the MTPNV cells are reprogrammed (up to a maximum value of 111111; there is no overflow; performing a factory reset also increments the counter). This counter is provided for information purposes only; reprogramming will not be rejected when it reaches its maximum value. Factory preset values are restored if the following conditions apply continuously for at least td(MTPNV) during battery power-up: pin RSTN is held LOW, CANH is pulled up to VBAT, CANL is pulled down to GND. After the factory preset values have been restored, the SBC performs a system reset and enters Forced normal Mode. Since the CAN-bus is clamped dominant, pin RXDC is forced LOW. Pin RXD is forced HIGH during the factory preset restore process (td(MTPNV)). A falling edge on RXD caused by bit PO being set after power-on indicates that the factory preset process has been completed. Note that the write counter, WRCNTS, in the MTPNV status register is incremented every time the factory presets are restored.

Implements : `sbc_factories_conf_t` Class

Definition at line 1298 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_start_up_t](#) startUp
- [sbc_sbc_t](#) control

Field Documentation

17.147.2.14.1 `sbc_sbc_t` control

SBC configuration control register. Note that this register is located in the non-volatile memory area.

Definition at line 1300 of file sbc_uja116x_driver.h.

17.147.2.14.2 `sbc_start_up_t` startUp

Start-up control register.

Definition at line 1299 of file sbc_uja116x_driver.h.

17.147.2.15 `struct sbc_main_status_t`

Main status register structure. The Main status register can be accessed to monitor the status of the overtemperature warning flag and to determine whether the UJA116xA has entered Normal mode after initial power-up. It also indicates the source of the most recent reset event.

Implements : `sbc_main_status_t` Class

Definition at line 1314 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_main_otws_t otws](#)
- [sbc_main_nms_t nms](#)
- [sbc_main_rss_t rss](#)

Field Documentation**17.147.2.15.1 sbc_main_nms_t nms**

Normal mode status.

Definition at line 1316 of file sbc_uja116x_driver.h.

17.147.2.15.2 sbc_main_otws_t otws

Overtemperature warning status.

Definition at line 1315 of file sbc_uja116x_driver.h.

17.147.2.15.3 sbc_main_rss_t rss

Reset source status.

Definition at line 1317 of file sbc_uja116x_driver.h.

17.147.2.16 struct sbc_wtdog_status_t

Watchdog status register structure. Information on the status of the watchdog is available from the Watchdog status register. This register also indicates whether Forced Normal and Software Development modes are active.

Implements : [sbc_wtdog_status_t_Class](#)

Definition at line 1328 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_wtdog_stat_fnms_t fnms](#)
- [sbc_wtdog_stat_sdms_t sdms](#)
- [sbc_wtdog_stat_wds_t wds](#)

Field Documentation**17.147.2.16.1 sbc_wtdog_stat_fnms_t fnms**

Forced Normal mode status.

Definition at line 1329 of file sbc_uja116x_driver.h.

17.147.2.16.2 sbc_wtdog_stat_sdms_t sdms

Software Development mode status.

Definition at line 1330 of file sbc_uja116x_driver.h.

17.147.2.16.3 sbc_wtdog_stat_wds_t wds

Watchdog status.

Definition at line 1331 of file sbc_uja116x_driver.h.

17.147.2.17 struct sbc_supply_status_t

Supply voltage status register structure. V2/VEXT and V1 undervoltage and overvoltage status.

Implements : [sbc_supply_status_t_Class](#)

Definition at line 1340 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_supply_stat_v2s_t v2s](#)
- [sbc_supply_stat_v1s_t v1s](#)

Field Documentation

17.147.2.17.1 **sbc_supply_stat_v1s_t v1s**

V1 status.

Definition at line 1342 of file sbc_uja116x_driver.h.

17.147.2.17.2 **sbc_supply_stat_v2s_t v2s**

V2/VEXT status.

Definition at line 1341 of file sbc_uja116x_driver.h.

17.147.2.18 **struct sbc_trans_stat_t**

Transceiver status register structure. There are stored CAN transceiver statuses.

Implements : `sbc_trans_stat_t_Class`

Definition at line 1351 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_trans_stat_cts_t cts](#)
- [sbc_trans_stat_cpnerr_t cpnerr](#)
- [sbc_trans_stat_cpns_t cpns](#)
- [sbc_trans_stat_coscs_t coscs](#)
- [sbc_trans_stat_cbss_t cbss](#)
- [sbc_trans_stat_vcs_t vcs](#)
- [sbc_trans_stat_cfs_t cfs](#)

Field Documentation

17.147.2.18.1 **sbc_trans_stat_cbss_t cbss**

CAN-bus silence status.

Definition at line 1356 of file sbc_uja116x_driver.h.

17.147.2.18.2 **sbc_trans_stat_cfs_t cfs**

CAN failure status.

Definition at line 1358 of file sbc_uja116x_driver.h.

17.147.2.18.3 **sbc_trans_stat_coscs_t coscs**

CAN oscillator status.

Definition at line 1355 of file sbc_uja116x_driver.h.

17.147.2.18.4 **sbc_trans_stat_cpnerr_t cpnerr**

CAN partial networking error.

Definition at line 1353 of file sbc_uja116x_driver.h.

17.147.2.18.5 sbc_trans_stat_cpns_t cpns

CAN partial networking status.

Definition at line 1354 of file sbc_uja116x_driver.h.

17.147.2.18.6 sbc_trans_stat_cts_t cts

CAN transceiver status.

Definition at line 1352 of file sbc_uja116x_driver.h.

17.147.2.18.7 sbc_trans_stat_vcs_t vcs

VCAN status.

Definition at line 1357 of file sbc_uja116x_driver.h.

17.147.2.19 struct sbc_gl_evnt_stat_t

Global event status register. The microcontroller can monitor events via the event status registers. An extra status register, the Global event status register, is provided to help speed up software polling routines. By polling the Global event status register, the microcontroller can quickly determine the type of event captured (system, supply, transceiver or WAKE pin) and then query the relevant event status register.

Implements : sbc_gl_evnt_stat_t_Class

Definition at line 1372 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_gl_evnt_stat_wpe_t wpe](#)
- [sbc_gl_evnt_stat_trxe_t trxe](#)
- [sbc_gl_evnt_stat_supe_t supe](#)
- [sbc_gl_evnt_stat_syse_t syse](#)

Field Documentation**17.147.2.19.1 sbc_gl_evnt_stat_supe_t supe**

Supply event.

Definition at line 1375 of file sbc_uja116x_driver.h.

17.147.2.19.2 sbc_gl_evnt_stat_syse_t syse

System event.

Definition at line 1376 of file sbc_uja116x_driver.h.

17.147.2.19.3 sbc_gl_evnt_stat_trxe_t trxe

Transceiver event.

Definition at line 1374 of file sbc_uja116x_driver.h.

17.147.2.19.4 sbc_gl_evnt_stat_wpe_t wpe

WAKE pin event.

Definition at line 1373 of file sbc_uja116x_driver.h.

17.147.2.20 struct sbc_sys_evnt_stat_t

System event status register. Wake-up and interrupt event diagnosis in the UJA116xA is intended to provide the microcontroller with information on the status of a range of features and functions. This information is stored in the

event status registers and is signaled on pin RXD, if enabled.

Implements : `sbc_sys_evnt_stat_t_Class`

Definition at line 1388 of file `sbc_uja116x_driver.h`.

Data Fields

- [sbc_sys_evnt_stat_po_t po](#)
- [sbc_sys_evnt_stat_otw_t otw](#)
- [sbc_sys_evnt_stat_spif_t spif](#)
- [sbc_sys_evnt_stat_wdf_t wdf](#)

Field Documentation

17.147.2.20.1 `sbc_sys_evnt_stat_otw_t otw`

Transceiver event, overtemperature warning

Definition at line 1390 of file `sbc_uja116x_driver.h`.

17.147.2.20.2 `sbc_sys_evnt_stat_po_t po`

Power-on.

Definition at line 1389 of file `sbc_uja116x_driver.h`.

17.147.2.20.3 `sbc_sys_evnt_stat_spif_t spif`

SPI failure.

Definition at line 1392 of file `sbc_uja116x_driver.h`.

17.147.2.20.4 `sbc_sys_evnt_stat_wdf_t wdf`

Watchdog failure.

Definition at line 1393 of file `sbc_uja116x_driver.h`.

17.147.2.21 `struct sbc_sup_evnt_stat_t`

Supply event status register.

Implements : `sbc_sup_evnt_stat_t_Class`

Definition at line 1401 of file `sbc_uja116x_driver.h`.

Data Fields

- [sbc_sup_evnt_stat_v2o_t v2o](#)
- [sbc_sup_evnt_stat_v2u_t v2u](#)
- [sbc_sup_evnt_stat_v1u_t v1u](#)

Field Documentation

17.147.2.21.1 `sbc_sup_evnt_stat_v1u_t v1u`

V1 undervoltage.

Definition at line 1404 of file `sbc_uja116x_driver.h`.

17.147.2.21.2 `sbc_sup_evnt_stat_v2o_t v2o`

V2/VEXT overvoltage.

Definition at line 1402 of file `sbc_uja116x_driver.h`.

17.147.2.21.3 sbc_sup_evnt_stat_v2u_t v2u

V2/VEXT undervoltage.

Definition at line 1403 of file sbc_uja116x_driver.h.

17.147.2.22 struct sbc_trans_evnt_stat_t

Transceiver event status register.

Implements : sbc_trans_evnt_stat_t_Class

Definition at line 1412 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_trans_evnt_stat_pnfde_t pnfde](#)
- [sbc_trans_evnt_stat_cbs_t cbs](#)
- [sbc_trans_evnt_stat_cf_t cf](#)
- [sbc_trans_evnt_stat_cw_t cw](#)

Field Documentation**17.147.2.22.1 sbc_trans_evnt_stat_cbs_t cbs**

CAN-bus status.

Definition at line 1415 of file sbc_uja116x_driver.h.

17.147.2.22.2 sbc_trans_evnt_stat_cf_t cf

CAN failure.

Definition at line 1416 of file sbc_uja116x_driver.h.

17.147.2.22.3 sbc_trans_evnt_stat_cw_t cw

CAN wake-up.

Definition at line 1417 of file sbc_uja116x_driver.h.

17.147.2.22.4 sbc_trans_evnt_stat_pnfde_t pnfde

Partial networking frame detection error.

Definition at line 1413 of file sbc_uja116x_driver.h.

17.147.2.23 struct sbc_wake_evnt_stat_t

WAKE pin event status register.

Implements : sbc_wake_evnt_stat_t_Class

Definition at line 1425 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_wake_evnt_stat_wpr_t wpr](#)
- [sbc_wake_evnt_stat_wpf_t wpf](#)

Field Documentation**17.147.2.23.1 sbc_wake_evnt_stat_wpf_t wpf**

WAKE pin falling edge.

Definition at line 1427 of file sbc_uja116x_driver.h.

17.147.2.23.2 sbc_wake_evnt_stat_wpr_t wpr

WAKE pin rising edge.

Definition at line 1426 of file sbc_uja116x_driver.h.

17.147.2.24 struct sbc_evn_capt_t

Event capture registers structure. This structure contains Global event status, System event status, Supply event status, Transceiver event status, WAKE pin event status.

Implements : sbc_evn_capt_t_Class

Definition at line 1437 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_gl_evnt_stat_t glEvt](#)
- [sbc_sys_evnt_stat_t sysEvt](#)
- [sbc_sup_evnt_stat_t supEvt](#)
- [sbc_trans_evnt_stat_t transEvt](#)
- [sbc_wake_evnt_stat_t wakePinEvt](#)

Field Documentation**17.147.2.24.1 sbc_gl_evnt_stat_t glEvt**

Global event status.

Definition at line 1438 of file sbc_uja116x_driver.h.

17.147.2.24.2 sbc_sup_evnt_stat_t supEvt

Supply event status.

Definition at line 1440 of file sbc_uja116x_driver.h.

17.147.2.24.3 sbc_sys_evnt_stat_t sysEvt

System event status.

Definition at line 1439 of file sbc_uja116x_driver.h.

17.147.2.24.4 sbc_trans_evnt_stat_t transEvt

Transceiver event status.

Definition at line 1441 of file sbc_uja116x_driver.h.

17.147.2.24.5 sbc_wake_evnt_stat_t wakePinEvt

WAKE pin event status.

Definition at line 1442 of file sbc_uja116x_driver.h.

17.147.2.25 struct sbc_mtpnv_stat_t

MTPNV status register. The MTPNV cells can be reprogrammed a maximum of 200 times (Ncy(W)MTP). Bit N↔ VMPS in the MTPNV status register indicates whether the non-volatile cells can be reprogrammed. This register also contains a write counter, WRCNTS, that is incremented each time the MTPNV cells are reprogrammed (up to a maximum value of 111111; there is no overflow; performing a factory reset also increments the counter). This counter is provided for information purposes only; reprogramming will not be rejected when it reaches its maximum value.

Implements : sbc_mtpnv_stat_t_Class

Definition at line 1458 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_mtpnv_stat_wrcnts_t wrcnts](#)
- [sbc_mtpnv_stat_eccs_t eccs](#)
- [sbc_mtpnv_stat_nvmps_t nvmps](#)

Field Documentation

17.147.2.25.1 **sbc_mtpnv_stat_eccs_t eccs**

Error correction code status.

Definition at line 1460 of file sbc_uja116x_driver.h.

17.147.2.25.2 **sbc_mtpnv_stat_nvmps_t nvmps**

Non-volatile memory programming status.

Definition at line 1461 of file sbc_uja116x_driver.h.

17.147.2.25.3 **sbc_mtpnv_stat_wrcnts_t wrcnts**

Write counter status.

Definition at line 1459 of file sbc_uja116x_driver.h.

17.147.2.26 **struct sbc_status_group_t**

Status group structure. All statuses of SBC are stored in this structure.

Implements : [sbc_status_group_t_Class](#)

Definition at line 1472 of file sbc_uja116x_driver.h.

Data Fields

- [sbc_main_status_t mainS](#)
- [sbc_wtdog_status_t wtdog](#)
- [sbc_supply_status_t supply](#)
- [sbc_trans_stat_t trans](#)
- [sbc_wake_stat_wpvs_t wakePin](#)
- [sbc_evn_capt_t events](#)

Field Documentation

17.147.2.26.1 **sbc_evn_capt_t events**

Event capture registers.

Definition at line 1478 of file sbc_uja116x_driver.h.

17.147.2.26.2 **sbc_main_status_t mainS**

Main status.

Definition at line 1473 of file sbc_uja116x_driver.h.

17.147.2.26.3 **sbc_supply_status_t supply**

Supply voltage status.

Definition at line 1475 of file sbc_uja116x_driver.h.

17.147.2.26.4 sbc_trans_stat_t trans

Transceiver status.

Definition at line 1476 of file sbc_uja116x_driver.h.

17.147.2.26.5 sbc_wake_stat_wpvs_t wakePin

WAKE pin status.

Definition at line 1477 of file sbc_uja116x_driver.h.

17.147.2.26.6 sbc_wtdog_status_t wtdog

Watchdog status.

Definition at line 1474 of file sbc_uja116x_driver.h.

17.147.3 Macro Definition Documentation**17.147.3.1 #define SBC_UJA_COUNT_DMASK 8U**

Definition at line 41 of file sbc_uja116x_driver.h.

17.147.3.2 #define SBC_UJA_COUNT_ID_REG 4U

Definition at line 39 of file sbc_uja116x_driver.h.

17.147.3.3 #define SBC_UJA_COUNT_MASK 4U

Definition at line 40 of file sbc_uja116x_driver.h.

17.147.3.4 #define SBC_UJA_TIMEOUT 1000U

Timeout for the transfer in milliseconds. If the transfer takes longer than this time, the transfer is aborted and LPSPi_STATUS_SBC_UJA_TIMEOUT error is reported.

Definition at line 33 of file sbc_uja116x_driver.h.

17.147.4 Typedef Documentation**17.147.4.1 typedef uint8_t sbc_data_mask_t**

Data mask registers. The data field indicates the nodes to be woken up. Within the data field, groups of nodes can be predefined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.

Implements : sbc_data_mask_t_Class

Definition at line 706 of file sbc_uja116x_driver.h.

17.147.4.2 typedef uint8_t sbc_fail_safe_rcc_t

Fail-safe control register, reset counter control (0x02). incremented every time the SBC enters Reset mode while FNMC = 0; RCC overflows from 11 to 00; default at power-on is 00.

Implements : sbc_fail_safe_rcc_t_Class

Definition at line 195 of file sbc_uja116x_driver.h.

17.147.4.3 typedef uint8_t sbc_frame_ctr_dlc_t

Frame control register, number of data bytes expected in a CAN frame (0x2F).

Implements : `sbc_frame_ctr_dlc_t_Class`

Definition at line 695 of file `sbc_uja116x_driver.h`.

17.147.4.4 `typedef uint8_t sbc_identif_mask_t`

ID mask registers (0x2B to 0x2E). The identifier mask is defined in the ID mask registers, where a 1 means dont care.

Implements : `sbc_identif_mask_t_Class`

Definition at line 661 of file `sbc_uja116x_driver.h`.

17.147.4.5 `typedef uint8_t sbc_identifier_t`

ID registers, identifier format (0x27 to 0x2A). A valid WUF identifier is defined and stored in the ID registers. An ID mask can be defined to allow a group of identifiers to be recognized as valid by an individual node.

Implements : `sbc_identifier_t_Class`

Definition at line 652 of file `sbc_uja116x_driver.h`.

17.147.4.6 `typedef uint8_t sbc_mtpnv_stat_wrcnts_t`

MTPNV status register, write counter status (0x70). 6-bits - contains the number of times the MTPNV cells were reprogrammed.

Implements : `sbc_mtpnv_stat_wrcnts_t_Class`

Definition at line 967 of file `sbc_uja116x_driver.h`.

17.147.5 Enumeration Type Documentation

17.147.5.1 `enum sbc_can_cfdc_t`

CAN control register, CAN FD control (0x20).

Implements : `sbc_can_cfdc_t_Class`

Enumerator

`SBC_UJA_CAN_CFDC_DIS` CAN FD tolerance disabled.

`SBC_UJA_CAN_CFDC_EN` CAN FD tolerance enabled.

Definition at line 460 of file `sbc_uja116x_driver.h`.

17.147.5.2 `enum sbc_can_cmc_t`

CAN control register, CAN mode control (0x20).

Implements : `sbc_can_cmc_t_Class`

Enumerator

`SBC_UJA_CAN_CMC_OFMODE` Offline mode.

`SBC_UJA_CAN_CMC_ACMODE_DA` Active mode (when the SBC is in Normal mode); CAN supply under-voltage detection active.

`SBC_UJA_CAN_CMC_ACMODE_DD` Active mode (when the SBC is in Normal mode); CAN supply under-voltage detection disabled.

`SBC_UJA_CAN_CMC_LISTEN` Listen-only mode.

Definition at line 496 of file `sbc_uja116x_driver.h`.

17.147.5.3 enum **sbc_can_cpnc_t**

CAN control register, CAN partial networking control (0x20).

Implements : `sbc_can_cpnc_t_Class`

Enumerator

SBC_UJA_CAN_CPNC_DIS Disable CAN selective wake-up.

SBC_UJA_CAN_CPNC_EN Enable CAN selective wake-up.

Definition at line 484 of file `sbc_uja116x_driver.h`.

17.147.5.4 enum **sbc_can_pncok_t**

CAN control register, CAN partial networking configuration OK (0x20).

Implements : `sbc_can_pncok_t_Class`

Enumerator

SBC_UJA_CAN_PNCOK_DIS Partial networking register configuration invalid (wake-up via standard wake-up pattern only).

SBC_UJA_CAN_PNCOK_EN Partial networking registers configured successfully.

Definition at line 472 of file `sbc_uja116x_driver.h`.

17.147.5.5 enum **sbc_dat_rate_t**

Data rate register, CAN data rate selection (0x26). CAN partial networking configuration registers. Dedicated registers are provided for configuring CAN partial networking.

Implements : `sbc_dat_rate_t_Class`

Enumerator

SBC_UJA_DAT_RATE_CDR_50KB 50 kbit/s.

SBC_UJA_DAT_RATE_CDR_100KB 100 kbit/s.

SBC_UJA_DAT_RATE_CDR_125KB 125 kbit/s.

SBC_UJA_DAT_RATE_CDR_250KB 250 kbit/s.

SBC_UJA_DAT_RATE_CDR_500KB 500 kbit/s.

SBC_UJA_DAT_RATE_CDR_1000KB 1000 kbit/s.

Definition at line 635 of file `sbc_uja116x_driver.h`.

17.147.5.6 enum **sbc_fail_safe_lhc_t**

Fail-safe control register, LIMP home control (0x02). The dedicated LIMP pin can be used to enable so called limp home hardware in the event of a serious ECU failure. Detectable failure conditions include SBC overtemperature events, loss of watchdog service, short-circuits on pins RSTN or V1 and user-initiated or external reset events. The LIMP pin is a battery-robust, active-LOW, open-drain output. The LIMP pin can also be forced LOW by setting bit LHC in the Fail-safe control register.

Implements : `sbc_fail_safe_lhc_t_Class`

Enumerator

SBC_UJA_FAIL_SAFE_LHC_FLOAT LIMP pin is floating.

SBC_UJA_FAIL_SAFE_LHC_LOW LIMP pin is driven LOW.

Definition at line 183 of file `sbc_uja116x_driver.h`.

17.147.5.7 enum `sbc_frame_ctr_ide_t`

Frame control register, identifier format (0x2F). The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register.

Implements : `sbc_frame_ctr_ide_t_Class`

Enumerator

SBC_UJA_FRAME_CTR_IDE_11B Standard frame format (11-bit).

SBC_UJA_FRAME_CTR_IDE_29B Extended frame format (29-bit).

Definition at line 670 of file `sbc_uja116x_driver.h`.

17.147.5.8 enum `sbc_frame_ctr_pndm_t`

Frame control register, partial networking data mask (0x2F).

Implements : `sbc_frame_ctr_pndm_t_Class`

Enumerator

SBC_UJA_FRAME_CTR_PNDM_DCARE Data length code and data field are do not care for wake-up.

SBC_UJA_FRAME_CTR_PNDM_EVAL Data length code and data field are evaluated at wake-up.

Definition at line 682 of file `sbc_uja116x_driver.h`.

17.147.5.9 enum `sbc_gl_evnt_stat_supe_t`

Global event status register, supply event (0x60).

Implements : `sbc_gl_evnt_stat_supe_t_Class`

Enumerator

SBC_UJA_GL_EVNT_STAT_SUPE_NO No pending supply event.

SBC_UJA_GL_EVNT_STAT_SUPE Supply event pending at address 0x62 .

Definition at line 773 of file `sbc_uja116x_driver.h`.

17.147.5.10 enum `sbc_gl_evnt_stat_syse_t`

Global event status register, system event (0x60).

Implements : `sbc_gl_evnt_stat_syse_t_Class`

Enumerator

SBC_UJA_GL_EVNT_STAT_SYSE_NO No pending system event.

SBC_UJA_GL_EVNT_STAT_SYSE System event pending at address 0x61.

Definition at line 785 of file `sbc_uja116x_driver.h`.

17.147.5.11 enum `sbc_gl_evnt_stat_trxe_t`

Global event status register, transceiver event (0x60).

Implements : `sbc_gl_evnt_stat_trxe_t_Class`

Enumerator

SBC_UJA_GL_EVNT_STAT_TRXE_NO No pending transceiver event.

SBC_UJA_GL_EVNT_STAT_TRXE Transceiver event pending at address 0x63.

Definition at line 761 of file `sbc_uja116x_driver.h`.

17.147.5.12 enum `sbc_gl_evnt_stat_wpe_t`

Global event status register, WAKE pin event (0x60).

Implements : `sbc_gl_evnt_stat_wpe_t_Class`

Enumerator

SBC_UJA_GL_EVNT_STAT_WPE_NO No pending WAKE pin event.

SBC_UJA_GL_EVNT_STAT_WPE WAKE pin event pending at address 0x64.

Definition at line 749 of file `sbc_uja116x_driver.h`.

17.147.5.13 enum `sbc_lock_t`

Lock control(0x0A). Sections of the register address area can be write-protected to protect against unintended modifications. This facility only protects locked bits from being modified via the SPI and will not prevent the UJA116xA updating status registers etc.

Implements : `sbc_lock_t_Class`

Enumerator

LK0C Lock control 0: address area 0x06 to 0x09 - general-purpose memory macros. Lock control 1: address area 0x10 to 0x1F - regulator control macros.

LK1C Lock control 2: address area 0x20 to 0x2F - transceiver control macros.

LK2C Lock control 3: address area 0x30 to 0x3F - unused register range macros.

LK3C Lock control 4: address area 0x40 to 0x4F - WAKE pin control macros.

LK4C Lock control 5: address area 0x50 to 0x5F.

LK5C Lock control 6: address area 0x68 to 0x6F macros.

LK6C Lock control All: address area 0x10 to 0x6F macros.

LKAC

Definition at line 317 of file `sbc_uja116x_driver.h`.

17.147.5.14 enum `sbc_main_nms_t`

Main status register, normal mode status (0x03).

Implements : `sbc_main_nms_t_Class`

Enumerator

SBC_UJA_MAIN_NMS_NORMAL UJA116xA has entered Normal mode (after power-up)

SBC_UJA_MAIN_NMS_PWR_UP UJA116xA has powered up but has not yet switched to Normal mode.

Definition at line 214 of file `sbc_uja116x_driver.h`.

17.147.5.15 enum `sbc_main_otws_t`

Main status register, Overtemperature warning status (0x03).

Implements : `sbc_main_otws_t_Class`

Enumerator

SBC_UJA_MAIN_OTWS_BELOW IC temperature below overtemperature warning threshold.

SBC_UJA_MAIN_OTWS_ABOVE IC temperature above overtemperature warning threshold.

Definition at line 202 of file `sbc_uja116x_driver.h`.

17.147.5.16 enum sbc_main_rss_t

Main status register, Reset source status (0x03).

Implements : sbc_main_rss_t_Class

Enumerator

SBC_UJA_MAIN_RSS_OFF_MODE Left Off mode (power-on).
SBC_UJA_MAIN_RSS_CAN_WAKEUP CAN wake-up in Sleep mode.
SBC_UJA_MAIN_RSS_SLP_WAKEUP Wake-up via WAKE pin in Sleep mode.
SBC_UJA_MAIN_RSS_OVF_SLP Watchdog overflow in Sleep mode (Timeout mode).
SBC_UJA_MAIN_RSS_DIAG_WAKEUP Diagnostic wake-up in Sleep mode
SBC_UJA_MAIN_RSS_WATCH_TRIG Watchdog triggered too early (Window mode).
SBC_UJA_MAIN_RSS_WATCH_OVF Watchdog overflow (Window mode or Timeout mode with WDF = 1)
SBC_UJA_MAIN_RSS_ILLEG_WATCH Illegal watchdog mode control access.
SBC_UJA_MAIN_RSS_RSTN_PULDW RSTN pulled down externally.
SBC_UJA_MAIN_RSS_LFT_OVERTM Left Overtemp mode.
SBC_UJA_MAIN_RSS_V1_UNDERV V1 undervoltage.
SBC_UJA_MAIN_RSS_ILLEG_SLP Illegal Sleep mode command received.
SBC_UJA_MAIN_RSS_WAKE_SLP Wake-up from Sleep mode due to a frame detect error

Definition at line 226 of file sbc_uja116x_driver.h.

17.147.5.17 enum sbc_mode_mc_t

Mode control register, mode control (0x01)

Implements : sbc_mode_mc_t_Class

Enumerator

SBC_UJA_MODE_MC_SLEEP Sleep mode.
SBC_UJA_MODE_MC_STANDBY Standby mode.
SBC_UJA_MODE_MC_NORMAL Normal mode.

Definition at line 165 of file sbc_uja116x_driver.h.

17.147.5.18 enum sbc_mtpnv_stat_eccs_t

MTPNV status register, error correction code status (0x70).

Implements : sbc_mtpnv_stat_eccs_t_Class

Enumerator

SBC_UJA_MTPNV_STAT_ECCS_NO No bit failure detected in non-volatile memory.
SBC_UJA_MTPNV_STAT_ECCS Bit failure detected and corrected in non-volatile memory.

Definition at line 974 of file sbc_uja116x_driver.h.

17.147.5.19 enum sbc_mtpnv_stat_nvmps_t

MTPNV status register, non-volatile memory programming status (0x70).

Implements : sbc_mtpnv_stat_nvmps_t_Class

Enumerator

SBC_UJA_MTPNV_STAT_NVMPs_NO MTPNV memory cannot be overwritten.
SBC_UJA_MTPNV_STAT_NVMPs MTPNV memory is ready to be reprogrammed.

Definition at line 986 of file sbc_uja116x_driver.h.

17.147.5.20 enum sbc_register_t

Register map.

Implements : sbc_register_t_Class

Enumerator

SBC_UJA_WTDOG_CTR
SBC_UJA_MODE
SBC_UJA_FAIL_SAFE
SBC_UJA_MAIN
SBC_UJA_SYSTEM_EVNT
SBC_UJA_WTDOG_STAT
SBC_UJA_MEMORY_0
SBC_UJA_MEMORY_1
SBC_UJA_MEMORY_2
SBC_UJA_MEMORY_3
SBC_UJA_LOCK
SBC_UJA_REGULATOR
SBC_UJA_SUPPLY_STAT
SBC_UJA_SUPPLY_EVNT
SBC_UJA_CAN
SBC_UJA_TRANS_STAT
SBC_UJA_TRANS_EVNT
SBC_UJA_DAT_RATE
SBC_UJA_IDENTIF_0
SBC_UJA_IDENTIF_1
SBC_UJA_IDENTIF_2
SBC_UJA_IDENTIF_3
SBC_UJA_MASK_0
SBC_UJA_MASK_1
SBC_UJA_MASK_2
SBC_UJA_MASK_3
SBC_UJA_FRAME_CTR
SBC_UJA_DAT_MASK_0
SBC_UJA_DAT_MASK_1
SBC_UJA_DAT_MASK_2
SBC_UJA_DAT_MASK_3
SBC_UJA_DAT_MASK_4
SBC_UJA_DAT_MASK_5
SBC_UJA_DAT_MASK_6
SBC_UJA_DAT_MASK_7
SBC_UJA_WAKE_STAT
SBC_UJA_WAKE_EN
SBC_UJA_GL_EVNT_STAT
SBC_UJA_SYS_EVNT_STAT
SBC_UJA_SUP_EVNT_STAT

SBC_UJA_TRANS_EVNT_STAT

SBC_UJA_WAKE_EVNT_STAT

SBC_UJA_MTPNV_STAT

SBC_UJA_START_UP

SBC_UJA_SBC

SBC_UJA_MTPNV_CRC

SBC_UJA_IDENTIF

Definition at line 51 of file sbc_uja116x_driver.h.

17.147.5.21 enum sbc_regulator_pdc_t

Regulator control register, power distribution control (0x10). PDC is not available on UJA1168 device variants, use any of these two values, the value written to the device will be ignored.

Implements : sbc_regulator_pdc_t_Class

Enumerator

SBC_UJA_REGULATOR_PDC_HV V1 threshold current for activating the external PNP transistor, load current rising; lth(act)PNP (higher value) V1 threshold current for deactivating the external PNP transistor, load current falling; lth(deact)PNP (higher value).

SBC_UJA_REGULATOR_PDC_LV V1 threshold current for activating the external PNP transistor; load current rising; lth(act)PNP (lower value) V1 threshold current for deactivating the external PNP transistor; load current falling; lth(deact)PNP (lower value).

Definition at line 344 of file sbc_uja116x_driver.h.

17.147.5.22 enum sbc_regulator_v1rtc_t

Regulator control register, set V1 reset threshold (0x10).

Implements : sbc_regulator_v1rtc_t_Class

Enumerator

SBC_UJA_REGULATOR_V1RTC_90 Reset threshold set to 90 % of V1 nominal output voltage.

SBC_UJA_REGULATOR_V1RTC_80 Reset threshold set to 80 % of V1 nominal output voltage.

SBC_UJA_REGULATOR_V1RTC_70 Reset threshold set to 70 % of V1 nominal output voltage.

SBC_UJA_REGULATOR_V1RTC_60 Reset threshold set to 60 % of V1 nominal output voltage.

Definition at line 378 of file sbc_uja116x_driver.h.

17.147.5.23 enum sbc_regulator_v2c_t

Regulator control register, V2/VEXT configuration (0x10).

Implements : sbc_regulator_v2c_t_Class

Enumerator

SBC_UJA_REGULATOR_V2C_OFF V2/VEXT off in all modes.

SBC_UJA_REGULATOR_V2C_N V2/VEXT on in Normal mode.

SBC_UJA_REGULATOR_V2C_N_S_R V2/VEXT on in Normal, Standby and Reset modes.

SBC_UJA_REGULATOR_V2C_N_S_S_R V2/VEXT on in Normal, Standby, Sleep and Reset modes.

Definition at line 362 of file sbc_uja116x_driver.h.

17.147.5.24 enum **sbc_sbc_fnmc_t**

SBC configuration control register, Forced Normal mode control (0x74).

Implements : **sbc_sbc_fnmc_t_Class**

Enumerator

SBC_UJA_SBC_FNMC_DIS Forced Normal mode disabled.

SBC_UJA_SBC_FNMC_EN Forced Normal mode enabled.

Definition at line 1043 of file **sbc_uja116x_driver.h**.

17.147.5.25 enum **sbc_sbc_sdmc_t**

SBC configuration control register, Software Development mode control (0x74).

Implements : **sbc_sbc_sdmc_t_Class**

Enumerator

SBC_UJA_SBC_SDMC_DIS Software Development mode disabled.

SBC_UJA_SBC_SDMC_EN Software Development mode enabled.

Definition at line 1056 of file **sbc_uja116x_driver.h**.

17.147.5.26 enum **sbc_sbc_slpc_t**

SBC configuration control register, Sleep control (0x74).

Implements : **sbc_sbc_slpc_t_Class**

Enumerator

SBC_UJA_SBC_SLPC_AC Sleep mode commands accepted. Factory preset value.

SBC_UJA_SBC_SLPC_IG Sleep mode commands ignored.

Definition at line 1069 of file **sbc_uja116x_driver.h**.

17.147.5.27 enum **sbc_sbc_v1rtsuc_t**

SBC configuration control register, V1 undervoltage threshold (defined by bit V1RTC) at start-up (0x74).

Implements : **sbc_sbc_v1rtsuc_t_Class**

Enumerator

SBC_UJA_SBC_V1RTSUC_90 V1 undervoltage detection at 90 % of nominal value at start-up (V1RTC = 00).

SBC_UJA_SBC_V1RTSUC_80 V1 undervoltage detection at 80 % of nominal value at start-up (V1RTC = 01).

SBC_UJA_SBC_V1RTSUC_70 V1 undervoltage detection at 70 % of nominal value at start-up V1RTC = 10).

SBC_UJA_SBC_V1RTSUC_60 V1 undervoltage detection at 60 % of nominal value at start-up (V1RTC = 11).

Definition at line 1027 of file **sbc_uja116x_driver.h**.

17.147.5.28 enum **sbc_start_up_rlc_t**

Start-up control register, RSTN output reset pulse width macros (0x73).

Implements : **sbc_start_up_rlc_t_Class**

Enumerator

SBC_UJA_START_UP_RLC_20_25p0 Tw(rst) = 20 ms to 25 ms.
SBC_UJA_START_UP_RLC_10_12p5 Tw(rst) = 10 ms to 12.5 ms.
SBC_UJA_START_UP_RLC_03p6_05 Tw(rst) = 3.6 ms to 5 ms.
SBC_UJA_START_UP_RLC_01_01p5 Tw(rst) = 1 ms to 1.5 ms.

Definition at line 998 of file sbc_uja116x_driver.h.

17.147.5.29 enum sbc_start_up_v2suc_t

Start-up control register, V2/VEXT start-up control (0x73).

Implements : sbc_start_up_v2suc_t_Class

Enumerator

SBC_UJA_START_UP_V2SUC_00 bits V2C/VEXTC set to 00 at power-up.
SBC_UJA_START_UP_V2SUC_11 bits V2C/VEXTC set to 11 at power-up.

Definition at line 1014 of file sbc_uja116x_driver.h.

17.147.5.30 enum sbc_sup_evnt_stat_v1u_t

Supply event status register, V1 undervoltage (0x62).

Implements : sbc_sup_evnt_stat_v1u_t_Class

Enumerator

SBC_UJA_SUP_EVNT_STAT_V1U_NO no V1 undervoltage event captured.
SBC_UJA_SUP_EVNT_STAT_V1U voltage on V1 has dropped below the 90 % undervoltage threshold while V1 is active (event is not captured in Sleep mode because V1 is off); V1U event capture is independent of the setting of bits V1RTC.

Definition at line 876 of file sbc_uja116x_driver.h.

17.147.5.31 enum sbc_sup_evnt_stat_v2o_t

Supply event status register, V2/VEXT overvoltage (0x62).

Implements : sbc_sup_evnt_stat_v2o_t_Class

Enumerator

SBC_UJA_SUP_EVNT_STAT_V2O_NO No V2/VEXT overvoltage event captured.
SBC_UJA_SUP_EVNT_STAT_V2O V2/VEXT overvoltage event captured.

Definition at line 852 of file sbc_uja116x_driver.h.

17.147.5.32 enum sbc_sup_evnt_stat_v2u_t

Supply event status register, V2/VEXT undervoltage (0x62).

Implements : sbc_sup_evnt_stat_v2u_t_Class

Enumerator

SBC_UJA_SUP_EVNT_STAT_V2U_NO No V2/VEXT undervoltage event captured.
SBC_UJA_SUP_EVNT_STAT_V2U V2/VEXT undervoltage event captured.

Definition at line 864 of file sbc_uja116x_driver.h.

17.147.5.33 enum `sbc_supply_evnt_v1ue_t`

Supply event capture enable register, V1 undervoltage enable (0x1C).

Implements : `sbc_supply_evnt_v1ue_t_Class`

Enumerator

`SBC_UJA_SUPPLY_EVNT_V1UE_DIS` V1 undervoltage detection disabled.

`SBC_UJA_SUPPLY_EVNT_V1UE_EN` V1 undervoltage detection enabled.

Definition at line 448 of file `sbc_uja116x_driver.h`.

17.147.5.34 enum `sbc_supply_evnt_v2oe_t`

Supply event capture enable register, V2/VEXT overvoltage enable (0x1C).

Implements : `sbc_supply_evnt_v2oe_t_Class`

Enumerator

`SBC_UJA_SUPPLY_EVNT_V2OE_DIS` V2/VEXT overvoltage detection disabled.

`SBC_UJA_SUPPLY_EVNT_V2OE_EN` V2/VEXT overvoltage detection enabled.

Definition at line 423 of file `sbc_uja116x_driver.h`.

17.147.5.35 enum `sbc_supply_evnt_v2ue_t`

Supply event capture enable register, V2/VEXT undervoltage enable (0x1C).

Implements : `sbc_supply_evnt_v2ue_t_Class`

Enumerator

`SBC_UJA_SUPPLY_EVNT_V2UE_DIS` V2/VEXT undervoltage detection disabled.

`SBC_UJA_SUPPLY_EVNT_V2UE_EN` V2/VEXT undervoltage detection enabled.

Definition at line 436 of file `sbc_uja116x_driver.h`.

17.147.5.36 enum `sbc_supply_stat_v1s_t`

Supply voltage status register, V1 status (0x1B).

Implements : `sbc_supply_stat_v1s_t_Class`

Enumerator

`SBC_UJA_SUPPLY_STAT_V1S_VAB` V1 output voltage above 90 % undervoltage threshold.

`SBC_UJA_SUPPLY_STAT_V1S_VBE` V1 output voltage below 90 % undervoltage threshold.

Definition at line 410 of file `sbc_uja116x_driver.h`.

17.147.5.37 enum `sbc_supply_stat_v2s_t`

Supply voltage status register, V2/VEXT status (0x1B).

Implements : `sbc_supply_stat_v2s_t_Class`

Enumerator

`SBC_UJA_SUPPLY_STAT_V2S_VOK` V2/VEXT voltage ok.

`SBC_UJA_SUPPLY_STAT_V2S_VBE` V2/VEXT output voltage below undervoltage threshold

`SBC_UJA_SUPPLY_STAT_V2S_VAB` V2/VEXT output voltage above overvoltage threshold

`SBC_UJA_SUPPLY_STAT_V2S_DIS` V2/VEXT disabled

Definition at line 394 of file `sbc_uja116x_driver.h`.

17.147.5.38 enum `sbc_sys_evnt_otwe_t`

System event capture enable, overtemperature warning enable (0x04).

Implements : `sbc_sys_evnt_otwe_t_Class`

Enumerator

SBC_UJA_SYS_EVNT_OTWE_DIS Overtemperature warning disabled.

SBC_UJA_SYS_EVNT_OTWE_EN Overtemperature warning enabled.

Definition at line 251 of file `sbc_uja116x_driver.h`.

17.147.5.39 enum `sbc_sys_evnt_spife_t`

System event capture enable, SPI failure enable (0x04).

Implements : `sbc_sys_evnt_spife_t_Class`

Enumerator

SBC_UJA_SYS_EVNT_SPIFE_DIS SPI failure detection disabled.

SBC_UJA_SYS_EVNT_SPIFE_EN SPI failure detection enabled.

Definition at line 263 of file `sbc_uja116x_driver.h`.

17.147.5.40 enum `sbc_sys_evnt_stat_otw_t`

System event status register, overtemperature warning (0x61).

Implements : `sbc_sys_evnt_stat_otw_t_Class`

Enumerator

SBC_UJA_SYS_EVNT_STAT_OTW_NO Overtemperature not detected.

SBC_UJA_SYS_EVNT_STAT_OTW The global chip temperature has exceeded the overtemperature warning threshold, `Tth(warn)otp` (not in Sleep mode).

Definition at line 809 of file `sbc_uja116x_driver.h`.

17.147.5.41 enum `sbc_sys_evnt_stat_po_t`

System event status register, power-on (0x61).

Implements : `sbc_sys_evnt_stat_po_t_Class`

Enumerator

SBC_UJA_SYS_EVNT_STAT_PO_NO No recent battery power-on.

SBC_UJA_SYS_EVNT_STAT_PO The UJA116xA has left Off mode after battery power-on.

Definition at line 797 of file `sbc_uja116x_driver.h`.

17.147.5.42 enum `sbc_sys_evnt_stat_spif_t`

System event status register, SPI failure (0x61).

Implements : `sbc_sys_evnt_stat_spif_t_Class`

Enumerator

SBC_UJA_SYS_EVNT_STAT_SPIF_NO No SPI failure detected

SBC_UJA_SYS_EVNT_STAT_SPIF SPI clock count error (only 16-, 24- and 32-bit commands are valid), illegal WMC, NWP or MC code or attempted write access to locked register (not in Sleep mode)

Definition at line 822 of file `sbc_uja116x_driver.h`.

17.147.5.43 enum **sbc_sys_evnt_stat_wdf_t**

System event status register, watchdog failure (0x61).

Implements : **sbc_sys_evnt_stat_wdf_t_Class**

Enumerator

SBC_UJA_SYS_EVNT_STAT_WDF_NO No watchdog failure event captured

SBC_UJA_SYS_EVNT_STAT_WDF Watchdog overflow in Window or Timeout mode or watchdog triggered too early in Window mode; a system reset is triggered immediately in response to a watchdog failure in Window mode; when the watchdog overflows in Timeout mode, a system reset is only performed if a WDF is already pending (WDF = 1).

Definition at line 836 of file **sbc_uja116x_driver.h**.

17.147.5.44 enum **sbc_trans_evnt_cbse_t**

Transceiver event capture enable register, CAN-bus silence enable (0x23).

Implements : **sbc_trans_evnt_cbse_t_Class**

Enumerator

SBC_UJA_TRANS_EVNT_CBSE_DIS CAN-bus silence detection disabled.

SBC_UJA_TRANS_EVNT_CBSE_EN CAN-bus silence detection enabled.

Definition at line 597 of file **sbc_uja116x_driver.h**.

17.147.5.45 enum **sbc_trans_evnt_cfe_t**

Transceiver event capture enable register, CAN failure enable (0x23).

Implements : **sbc_trans_evnt_cfe_t_Class**

Enumerator

SBC_UJA_TRANS_EVNT_CFE_DIS CAN failure detection disabled.

SBC_UJA_TRANS_EVNT_CFE_EN CAN failure detection enabled.

Definition at line 609 of file **sbc_uja116x_driver.h**.

17.147.5.46 enum **sbc_trans_evnt_cwe_t**

Transceiver event capture enable register, CAN wake-up enable (0x23).

Implements : **sbc_trans_evnt_cwe_t_Class**

Enumerator

SBC_UJA_TRANS_EVNT_CWE_DIS CAN wake-up detection disabled.

SBC_UJA_TRANS_EVNT_CWE_EN CAN wake-up detection enabled.

Definition at line 621 of file **sbc_uja116x_driver.h**.

17.147.5.47 enum **sbc_trans_evnt_stat_cbs_t**

Transceiver event status register, CAN-bus status (0x63).

Implements : **sbc_trans_evnt_stat_cbs_t_Class**

Enumerator

SBC_UJA_TRANS_EVNT_STAT_CBS_NO CAN-bus active.

SBC_UJA_TRANS_EVT_STAT_CBS No activity on CAN-bus for tto(silence) (detected only when CBSE = 1 while bus active).

Definition at line 903 of file sbc_uja116x_driver.h.

17.147.5.48 enum **sbc_trans_evt_stat_cf_t**

Transceiver event status register, CAN failure (0x63).

Implements : sbc_trans_evt_stat_cf_t_Class

Enumerator

SBC_UJA_TRANS_EVT_STAT_CF_NO No CAN failure detected.

SBC_UJA_TRANS_EVT_STAT_CF CAN transceiver deactivated due to VCAN undervoltage OR dominant clamped TXD (not in Sleep mode)

Definition at line 916 of file sbc_uja116x_driver.h.

17.147.5.49 enum **sbc_trans_evt_stat_cw_t**

Transceiver event status register, CAN wake-up (0x63).

Implements : sbc_trans_evt_stat_cw_t_Class

Enumerator

SBC_UJA_TRANS_EVT_STAT_CW_NO No CAN wake-up event detected.

SBC_UJA_TRANS_EVT_STAT_CW CAN wake-up event detected while the transceiver is in CAN Offline Mode.

Definition at line 929 of file sbc_uja116x_driver.h.

17.147.5.50 enum **sbc_trans_evt_stat_pnfde_t**

Transceiver event status register, partial networking frame detection error (0x63).

Implements : sbc_trans_evt_stat_pnfde_t_Class

Enumerator

SBC_UJA_TRANS_EVT_STAT_PNFDE_NO No partial networking frame detection error detected.

SBC_UJA_TRANS_EVT_STAT_PNFDE Partial networking frame detection error detected.

Definition at line 891 of file sbc_uja116x_driver.h.

17.147.5.51 enum **sbc_trans_stat_cbss_t**

Transceiver status register, CAN-bus silence status (0x22).

Implements : sbc_trans_stat_cbss_t_Class

Enumerator

SBC_UJA_TRANS_STAT_CBSS_ACT CAN-bus active (communication detected on bus)

SBC_UJA_TRANS_STAT_CBSS_INACT CAN-bus inactive (for longer than t_to(silence)).

Definition at line 561 of file sbc_uja116x_driver.h.

17.147.5.52 enum **sbc_trans_stat_cfs_t**

Transceiver status register, CAN failure status (0x22).

Implements : sbc_trans_stat_cfs_t_Class

Enumerator

SBC_UJA_TRANS_STAT_CFS_NO_TXD No TXD dominant time-out event detected.

SBC_UJA_TRANS_STAT_CFS_TXD CAN transmitter disabled due to a TXD dominant time-out event.

Definition at line 585 of file sbc_uja116x_driver.h.

17.147.5.53 enum sbc_trans_stat_coscs_t

Transceiver status register, CAN oscillator status (0x22).

Implements : sbc_trans_stat_coscs_t_Class

Enumerator

SBC_UJA_TRANS_STAT_COSCS_NRUN CAN partial networking oscillator not running at target frequency.

SBC_UJA_TRANS_STAT_COSCS_RUN CAN partial networking oscillator running at target.

Definition at line 549 of file sbc_uja116x_driver.h.

17.147.5.54 enum sbc_trans_stat_cpnerr_t

Transceiver status register, CAN partial networking error (0x22).

Implements : sbc_trans_stat_cpnerr_t_Class

Enumerator

SBC_UJA_TRANS_STAT_CPNERR_NO_DET no CAN partial networking error detected (PNFDE = 0 AND PNCOK = 1).

SBC_UJA_TRANS_STAT_CPNERR_DET CAN partial networking error detected (PNFDE = 1 OR PNCOK = 0; wake-up via standard wake-up pattern only).

Definition at line 524 of file sbc_uja116x_driver.h.

17.147.5.55 enum sbc_trans_stat_cpns_t

Transceiver status register, CAN partial networking status (0x22).

Implements : sbc_trans_stat_cpns_t_Class

Enumerator

SBC_UJA_TRANS_STAT_CPNS_ERR CAN partial networking configuration error detected (PNCOK = 0).

SBC_UJA_TRANS_STAT_CPNS_OK CAN partial networking configuration ok (PNCOK = 1).

Definition at line 537 of file sbc_uja116x_driver.h.

17.147.5.56 enum sbc_trans_stat_cts_t

Transceiver status register, CAN transceiver status (0x22).

Implements : sbc_trans_stat_cts_t_Class

Enumerator

SBC_UJA_TRANS_STAT_CTS_INACT CAN transceiver not in Active mode.

SBC_UJA_TRANS_STAT_CTS_ACT CAN transceiver in Active mode.

Definition at line 512 of file sbc_uja116x_driver.h.

17.147.5.57 enum sbc_trans_stat_vcs_t

Transceiver status register, VCAN status (0x22).

Implements : sbc_trans_stat_vcs_t_Class

Enumerator

SBC_UJA_TRANS_STAT_VCS_AB CAN supply voltage is above the 90 % threshold.

SBC_UJA_TRANS_STAT_VCS_BE CAN supply voltage is below the 90 % threshold

Definition at line 573 of file sbc_uja116x_driver.h.

17.147.5.58 enum sbc_wake_en_wpfe_t

WAKE pin event capture enable register, WAKE pin falling-edge enable (0x4C).

Implements : sbc_wake_en_wpfe_t_Class

Enumerator

SBC_UJA_WAKE_EN_WPFE_DIS Falling-edge detection on WAKE pin disabled.

SBC_UJA_WAKE_EN_WPFE_EN Falling-edge detection on WAKE pin enabled.

Definition at line 737 of file sbc_uja116x_driver.h.

17.147.5.59 enum sbc_wake_en_wpre_t

WAKE pin event capture enable register, WAKE pin rising-edge enable (0x4C).

Implements : sbc_wake_en_wpre_t_Class

Enumerator

SBC_UJA_WAKE_EN_WPRE_DIS Rising-edge detection on WAKE pin disabled.

SBC_UJA_WAKE_EN_WPRE_EN Rising-edge detection on WAKE pin enabled.

Definition at line 725 of file sbc_uja116x_driver.h.

17.147.5.60 enum sbc_wake_evnt_stat_wpf_t

WAKE pin event status register, WAKE pin falling edge (0x64).

Implements : sbc_wake_evnt_stat_wpf_t_Class

Enumerator

SBC_UJA_WAKE_EVNT_STAT_WPF_NO No falling edge detected on WAKE pin.

SBC_UJA_WAKE_EVNT_STAT_WPF Falling edge detected on WAKE pin.

Definition at line 953 of file sbc_uja116x_driver.h.

17.147.5.61 enum sbc_wake_evnt_stat_wpr_t

WAKE pin event status register, WAKE pin rising edge (0x64).

Implements : sbc_wake_evnt_stat_wpr_t_Class

Enumerator

SBC_UJA_WAKE_EVNT_STAT_WPR_NO No rising edge detected on WAKE pin.

SBC_UJA_WAKE_EVNT_STAT_WPR Rising edge detected on WAKE pin.

Definition at line 941 of file sbc_uja116x_driver.h.

17.147.5.62 enum `sbc_wake_stat_wpvs_t`

WAKE pin status register, WAKE pin status (0x4B).

Implements : `sbc_wake_stat_wpvs_t_Class`

Enumerator

`SBC_UJA_WAKE_STAT_WPVS_BE` Voltage on WAKE pin below switching threshold ($V_{th}(sw)$).

`SBC_UJA_WAKE_STAT_WPVS_AB` voltage on WAKE pin above switching threshold ($V_{th}(sw)$).

Definition at line 713 of file `sbc_uja116x_driver.h`.

17.147.5.63 enum `sbc_wtdog_ctr_nwp_t`

Watchdog control register, nominal watchdog period (0x00). Eight watchdog periods are supported, from 8 ms to 4096 ms. The watchdog period is programmed via bits NWP. The selected period is valid for both Window and Timeout modes. The default watchdog period is 128 ms. A watchdog trigger event resets the watchdog timer. A watchdog trigger event is any valid write access to the Watchdog control register. If the watchdog mode or the watchdog period have changed as a result of the write access, the new values are immediately valid.

Implements : `sbc_wtdog_ctr_nwp_t_Class`

Enumerator

`SBC_UJA_WTD OG_CTR_NWP_8` 8 ms.

`SBC_UJA_WTD OG_CTR_NWP_16` 16 ms.

`SBC_UJA_WTD OG_CTR_NWP_32` 32 ms.

`SBC_UJA_WTD OG_CTR_NWP_64` 64 ms.

`SBC_UJA_WTD OG_CTR_NWP_128` 128 ms.

`SBC_UJA_WTD OG_CTR_NWP_256` 256 ms.

`SBC_UJA_WTD OG_CTR_NWP_1024` 1024 ms.

`SBC_UJA_WTD OG_CTR_NWP_4096` 4096 ms.

Definition at line 149 of file `sbc_uja116x_driver.h`.

17.147.5.64 enum `sbc_wtdog_ctr_wmc_t`

Watchdog control register, watchdog mode control (0x00). The UJA116xA contains a watchdog that supports three operating modes: Window, Timeout and Autonomous. In Window mode (available only in SBC Normal mode), a watchdog trigger event within a defined watchdog window triggers and resets the watchdog timer. In Timeout mode, the watchdog runs continuously and can be triggered and reset at any time within the watchdog period by a watchdog trigger. Watchdog time-out mode can also be used for cyclic wake-up of the microcontroller. In Autonomous mode, the watchdog can be off or autonomously in Timeout mode, depending on the selected SBC mode. The watchdog mode is selected via bits WMC in the Watchdog control register. The SBC must be in Standby mode when the watchdog mode is changed.

Implements : `sbc_wtdog_ctr_wmc_t_Class`

Enumerator

`SBC_UJA_WTD OG_CTR_WMC_AUTO` Autonomous mode.

`SBC_UJA_WTD OG_CTR_WMC_TIME` Timeout mode.

`SBC_UJA_WTD OG_CTR_WMC_WIND` Window mode (available only in SBC Normal mode).

Definition at line 128 of file `sbc_uja116x_driver.h`.

17.147.5.65 enum sbc_wtdog_stat_fnms_t

Watchdog status register, forced Normal mode status (0x05).

Implements : sbc_wtdog_stat_fnms_t_Class

Enumerator

SBC_UJA_WTD OG_STAT_FNMS_N_NORMAL SBC is not in Forced Normal mode.

SBC_UJA_WTD OG_STAT_FNMS_NORMAL SBC is in Forced Normal mode.

Definition at line 275 of file sbc_uja116x_driver.h.

17.147.5.66 enum sbc_wtdog_stat_sdms_t

Watchdog status register, Software Development mode status (0x05).

Implements : sbc_wtdog_stat_sdms_t_Class

Enumerator

SBC_UJA_WTD OG_STAT_SDMS_N_NORMAL SBC is not in Software Development mode.

SBC_UJA_WTD OG_STAT_SDMS_NORMAL SBC is in Software Development mode.

Definition at line 287 of file sbc_uja116x_driver.h.

17.147.5.67 enum sbc_wtdog_stat_wds_t

Watchdog status register, watchdog status (0x05).

Implements : sbc_wtdog_stat_wds_t_Class

Enumerator

SBC_UJA_WTD OG_STAT_WDS_OFF Watchdog is off.

SBC_UJA_WTD OG_STAT_WDS_FIH Watchdog is in first half of the nominal period.

SBC_UJA_WTD OG_STAT_WDS_SEH Watchdog is in second half of the nominal period.

Definition at line 299 of file sbc_uja116x_driver.h.

17.148 Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL)

17.148.1 Detailed Description

The S32 SDK provides a Peripheral Abstraction Layer for Universal Asynchronous Receiver-Transmitter (UART) modules of S32 SDK devices.

The UART PAL driver allows communication over a serial port. It was designed to be portable across all platforms and IPs which support UART communication.

How to integrate UART PAL in your application

Unlike the other drivers, UART PAL modules need to include a configuration file named `uart_pal_cfg.h`, which allows the user to specify which IPs are used and how many resources are allocated for each of them (state structures). The following code example shows how to configure one instance for each available UART IPs.

```
#ifndef uart_pal_cfg_H
#define uart_pal_cfg_H

/* Define which IP instance will be used in current project */
#define UART_OVER_LPUART
#define UART_OVER_FLEXIO
#define UART_OVER_LINFLEXD

/* Define the resources necessary for current project */
#define NO_OF_LPUART_INSTS_FOR_UART 1U
#define NO_OF_FLEXIO_INSTS_FOR_UART 1U
#define NO_OF_LINFLEXD_INSTS_FOR_UART 1U

#endif /* uart_pal_cfg_H */
```

The following table contains the matching between platforms and available IPs

IP	S32-K11	S32-K11	S32-K14	S32-K14	S32-K14	S32-K14	S32-V23	MPC577G	MPC577C	MPC577P	S32-R27	S32-R37	MPC577R	MPC577C	S32-R29	S32-G27A	S32-R45	S32-K144
LPURTS	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	No	No	No	No	No	No	Yes
FLEXIO	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	No	No	No	No	No	No	Yes

L← I← N← Flex← D← _← _← U← A← R← T	N← O	N← O	N← O	N← O	N← O	N← O	Y← E← S	Y← E← S	Y← E← S	Y← E← S	Y← E← S	Y← E← S	Y← E← S	N← O	Y← E← S	Y← E← S	Y← E← S	N← O
e← S← C← I← _← _← U← A← R← T	N← O	N← O	N← O	N← O	N← O	N← O	N← O	N← O	N← O	N← O	N← O	N← O	N← O	Y← E← S	N← O	N← O	N← O	N← O

Features

- Interrupt or DMA mode
- Provides blocking and non-blocking transmit and receive functions
- Configurable baud rate and number of bits per char

The following table contains the matching between IPs and available features

IP/FEATURE	Bits per char	Parity	Stop Bits
LPUART	8, 9, 10	Disabled, Even, Odd	1, 2
FLEXIO_UART	7, 8, 9, 10, 15, 16	Disabled	1
LINFlexD_UART	7, 8, 15, 16	Disabled, Even, Odd	1, 2

Functionality

Initialization

In order to use the UART PAL driver it must be first initialized, using [UART_Init\(\)](#) function. Once initialized, it cannot be initialized again for the same UART module instance until it is de-initialized, using [UART_Deinit\(\)](#). The initialization function does the following operations:

- sets the baud rate
- sets parity/bit count/stop bits count
- initializes the state structure for the current instance
- enables receiver/transmitter for the current instance Different UART modules instances can function independently of each other.

Interrupt-based communication

After initialization, a serial communication can be triggered by calling [UART_SendData](#) function. The driver interrupt handler takes care of transmitting all bytes in the TX buffer. Similarly, data reception is triggered by calling [UART_ReceiveData](#) function, passing the RX buffer as parameter. The driver interrupt handler reads the received byte

and saves them in the RX buffer. Non-blocking operations will initiate the transfer and return `STATUS_SUCCESS`, but the module is still busy with the transfer and another transfer can't be initiated until the current transfer is complete. The application can check the status of the current transfer by calling `UART_GetTransmitStatus()` / `UART_GetReceiveStatus()`.

The workflow applies to send/receive operations using blocking method (triggered by `UART_SendDataBlocking()` and `UART_ReceiveDataBlocking()`), with the single difference that the send/receive function will not return until the send/receive operation is complete (all bytes are successfully transferred or a timeout occurred). The timeout for the blocking method is passed as parameter by the user.

When configured to use the LPUART or LINFlexD peripherals, if a user callback is installed for RX/TX, the callback has to take care of data handling and aborting the transfer when complete; the driver interrupt handler does not manipulate the buffers in this case. When using the UART PAL over FLEXIO, when the driver completes the transmission or reception of the current buffer, it will invoke the user callback (if installed) with an appropriate event.

DMA-based communication

In DMA operation, both blocking and non-blocking transmission methods configure a DMA channel to copy data to/from the buffer. The driver assumes the DMA channel is already allocated. In case of LPUART and LINFlexD, the application also assumes that the proper requests are routed to it via DMAMUX. The FLEXIO driver will set the DMA request source. After configuring the DMA channel, the driver enables DMA requests for RX/TX, then the DMA engine takes care of moving data to/from the data buffer. In this scenario, the callback is only called when the full transmission is done, that is when the DMA channel finishes the number of loops configured in the transfer descriptor.

Important Notes

- Before using the UART PAL driver the module clock must be configured. Refer to Clock Manager for clock configuration.
- The driver enables the interrupts for the corresponding UART module, but any interrupt priority must be done by the application
- The board specific configurations must be done prior to driver calls; the driver has no influence on the functionality of the TX/RX pins - they must be configured by application
- DMA module has to be initialized prior to UART usage in DMA mode; also, DMA channels need to be allocated for UART usage by the application (the driver only takes care of configuring the DMA channels received in the configuration structure)
- Some features are not available for all UART IPs and incorrect parameters will be handled by `DEV_ASSERT`
- The `UART_SetBaudRate()` function attempts to configure the requested baud rate for the selected UART peripheral. Note that due to module limitation not any baud rate can be achieved. The driver will set a baud rate as close as possible to the requested baud rate, but there may still be substantial differences. The application should call `UART_GetBaudRate()` after `UART_SetBaudRate()` to check what baud rate was actually set.
- Due to different implementation of drivers, callback parameters in case of errors during reception may be different. LPUART and LINFLEXD_UART will pass `UART_EVENT_ERROR` as the event parameter for callbacks, whereas FLEXIO_UART will pass `UART_EVENT_END_TRANSFER`. In both cases, in order to retrieve the exact status of the latest reception, users can call the appropriate functions in the (`UART_GetReceiveStatus()`).
- Due to DMA mechanism, bit character length should be recommended multiple by 8. So, LPUART only supports 8 bit chars while FLEXIO_UART supports 8 and 16 bit chars in DMA module. Specially, LINFLEXD_UART can process with all character lengths currently because it takes care of parity bit handling internally.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\pal\src\uart\uart_pal.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\drivers\inc
${S32SDK_PATH}\platform\pal\inc
${S32SDK_PATH}\rtos\osif
```

Preprocessor symbols

No special symbols are required for this component

Dependencies

[Clock Manager Interrupt Manager \(Interrupt\) Enhanced Direct Memory Access \(eDMA\) OS Interface \(OSIF\)](#)

Example code

```
uint32_t bytesRemaining;

/* Instance information structure */
uart_instance_t uart_pall_instance = {
    .instType = UART_INST_TYPE_FLEXIO_UART,
    .instIdx = 0U
};

/* Configure UART */
uart_user_config_t uart_pall_Config0 = {
    .baudRate      = 600U,
    .bitCount      = UART_7_BITS_PER_CHAR,
    .parityMode     = UART_PARITY_DISABLED,
    .stopBitCount  = UART_ONE_STOP_BIT,
    .transferType   = UART_USING_INTERRUPTS,
    .rxDMAChannel  = 0U,
    .txDMAChannel  = 0U,
    .rxCallback     = NULL,
    .rxCallbackParam = NULL,
    .txCallback     = NULL,
    .txCallbackParam = NULL,
    .extension      = NULL
};

/* Configure FLEXIO pins routing */
extension_flexio_for_uart_t extension = {
    .dataPinTx = 0U,
    .dataPinRx = 1U,
};
uart_pall_Config0.extension = &extension;

/* Buffers */
uint8_t tx[8] = {0, 1, 2, 3, 4, 5, 6, 7};
uint8_t rx[8];

/* Initialize UART */
UART_Init(&uart_pall_instance, &uart_pall_Config0);

/* Send 8 frames */
UART_SendData(&uart_pall_instance, tx, 8U);
while(UART_GetTransmitStatus(&uart_pall_instance, &bytesRemaining) !=
    STATUS_SUCCESS);

/* Receive 8 frames */
UART_ReceiveData(&uart_pall_instance, rx, 8UL);
/* Wait for transfer to be completed */
while(UART_GetReceiveStatus(&uart_pall_instance, &bytesRemaining) != STATUS_SUCCESS)
;

/* De-initialize UART */
UART_Deinit(&uart_pall_instance);
```

Data Structures

- struct `uart_user_config_t`
Defines the UART configuration structure. [More...](#)

- struct [extension_flexio_for_uart_t](#)

Defines the extension structure for the UART over FLEXIO. [More...](#)

Enumerations

- enum [uart_bit_count_per_char_t](#) {
[UART_7_BITS_PER_CHAR](#) = 0x0U, [UART_8_BITS_PER_CHAR](#) = 0x1U, [UART_9_BITS_PER_CHAR](#) = 0x2U, [UART_10_BITS_PER_CHAR](#) = 0x3U,
[UART_15_BITS_PER_CHAR](#) = 0x4U, [UART_16_BITS_PER_CHAR](#) = 0x5U }
Defines the number of bits in a character.
- enum [uart_transfer_type_t](#) { [UART_USING_DMA](#) = 0U, [UART_USING_INTERRUPTS](#) = 1U }
Defines the transfer type.
- enum [uart_parity_mode_t](#) { [UART_PARITY_DISABLED](#) = 0x0U, [UART_PARITY_EVEN](#) = 0x2U, [UART_PARITY_ODD](#) = 0x3U }
Defines the parity mode.
- enum [uart_stop_bit_count_t](#) { [UART_ONE_STOP_BIT](#) = 0x0U, [UART_TWO_STOP_BIT](#) = 0x1U }
Defines the number of stop bits.

Functions

- void [UART_GetDefaultConfig](#) ([uart_user_config_t](#) *config)
Gets the default configuration structure.
- status_t [UART_Init](#) (const [uart_instance_t](#) *const instance, const [uart_user_config_t](#) *config)
Initializes the UART module.
- status_t [UART_Deinit](#) (const [uart_instance_t](#) *const instance)
De-initializes the UART module.
- status_t [UART_SetBaudRate](#) (const [uart_instance_t](#) *const instance, uint32_t desiredBaudRate)
Configures the UART baud rate.
- status_t [UART_GetBaudRate](#) (const [uart_instance_t](#) *const instance, uint32_t *configuredBaudRate)
Returns the UART baud rate.
- status_t [UART_SendDataBlocking](#) (const [uart_instance_t](#) *const instance, const uint8_t *txBuff, uint32_t txSize, uint32_t timeout)
Perform a blocking UART transmission.
- status_t [UART_SendData](#) (const [uart_instance_t](#) *const instance, const uint8_t *txBuff, uint32_t txSize)
Perform a non-blocking UART transmission.
- status_t [UART_AbortSendingData](#) (const [uart_instance_t](#) *const instance)
Terminates a non-blocking transmission early.
- status_t [UART_GetTransmitStatus](#) (const [uart_instance_t](#) *const instance, uint32_t *bytesRemaining)
Get the status of the current non-blocking UART transmission.
- status_t [UART_ReceiveDataBlocking](#) (const [uart_instance_t](#) *const instance, uint8_t *rxBuff, uint32_t rxSize, uint32_t timeout)
Perform a blocking UART reception.
- status_t [UART_ReceiveData](#) (const [uart_instance_t](#) *const instance, uint8_t *rxBuff, uint32_t rxSize)
Perform a non-blocking UART reception.
- status_t [UART_AbortReceivingData](#) (const [uart_instance_t](#) *const instance)
Terminates a non-blocking receive early.
- status_t [UART_GetReceiveStatus](#) (const [uart_instance_t](#) *const instance, uint32_t *bytesRemaining)
Get the status of the current non-blocking UART reception.
- status_t [UART_SetRxBuffer](#) (const [uart_instance_t](#) *const instance, uint8_t *rxBuff, uint32_t rxSize)
Provide a buffer for receiving data.
- status_t [UART_SetTxBuffer](#) (const [uart_instance_t](#) *const instance, const uint8_t *txBuff, uint32_t txSize)
Provide a buffer for transmitting data.

17.148.2 Data Structure Documentation

17.148.2.1 struct uart_user_config_t

Defines the UART configuration structure.

Implements : `uart_user_config_t_Class`

Definition at line 88 of file `uart_pal.h`.

Data Fields

- `uint32_t baudRate`
- `uart_bit_count_per_char_t bitCount`
- `uart_parity_mode_t parityMode`
- `uart_stop_bit_count_t stopBitCount`
- `uart_transfer_type_t transferType`
- `uint8_t rxDMAChannel`
- `uint8_t txDMAChannel`
- `uart_callback_t rxCallback`
- `void * rxCallbackParam`
- `uart_callback_t txCallback`
- `void * txCallbackParam`
- `void * extension`

Field Documentation

17.148.2.1.1 uint32_t baudRate

Baud rate

Definition at line 90 of file `uart_pal.h`.

17.148.2.1.2 uart_bit_count_per_char_t bitCount

Number of bits in a character

Definition at line 91 of file `uart_pal.h`.

17.148.2.1.3 void* extension

This field will be used to add extra settings to the basic configuration like FlexIO data pins

Definition at line 101 of file `uart_pal.h`.

17.148.2.1.4 uart_parity_mode_t parityMode

Parity mode, disabled (default), even, odd

Definition at line 92 of file `uart_pal.h`.

17.148.2.1.5 uart_callback_t rxCallback

Callback to invoke for data receive

Definition at line 97 of file `uart_pal.h`.

17.148.2.1.6 void* rxCallbackParam

Receive callback parameter

Definition at line 98 of file `uart_pal.h`.

17.148.2.1.7 uint8_t rxDMAChannel

Channel number for DMA rx channel.

Definition at line 95 of file uart_pal.h.

17.148.2.1.8 uart_stop_bit_count_t stopBitCount

number of stop bits, 1 stop bit (default) or 2 stop bits

Definition at line 93 of file uart_pal.h.

17.148.2.1.9 uart_transfer_type_t transferType

Type of the transfer (interrupt/dma based)

Definition at line 94 of file uart_pal.h.

17.148.2.1.10 uart_callback_t txCallback

Callback to invoke for data send

Definition at line 99 of file uart_pal.h.

17.148.2.1.11 void* txCallbackParam

Transmit callback parameter

Definition at line 100 of file uart_pal.h.

17.148.2.1.12 uint8_t txDMAChannel

Channel number for DMA tx channel.

Definition at line 96 of file uart_pal.h.

17.148.2.2 struct extension_flexio_for_uart_t

Defines the extension structure for the UART over FLEXIO.

Implements : extension_flexio_for_uart_t_Class

Definition at line 110 of file uart_pal.h.

Data Fields

- uint8_t [dataPinTx](#)
- uint8_t [dataPinRx](#)

Field Documentation**17.148.2.2.1 uint8_t dataPinRx**

Flexio pin to use as Rx pin

Definition at line 113 of file uart_pal.h.

17.148.2.2.2 uint8_t dataPinTx

Flexio pin to use as Tx pin

Definition at line 112 of file uart_pal.h.

17.148.3 Enumeration Type Documentation

17.148.3.1 enum `uart_bit_count_per_char_t`

Defines the number of bits in a character.

Implements : `uart_bit_count_per_char_t_Class`

Enumerator

`UART_7_BITS_PER_CHAR` 7-bit data characters
`UART_8_BITS_PER_CHAR` 8-bit data characters
`UART_9_BITS_PER_CHAR` 9-bit data characters
`UART_10_BITS_PER_CHAR` 10-bit data characters
`UART_15_BITS_PER_CHAR` 15-bit data characters
`UART_16_BITS_PER_CHAR` 16-bit data characters

Definition at line 39 of file `uart_pal.h`.

17.148.3.2 enum `uart_parity_mode_t`

Defines the parity mode.

Implements : `uart_parity_mode_t_Class`

Enumerator

`UART_PARITY_DISABLED` parity disabled
`UART_PARITY_EVEN` parity enabled, type even
`UART_PARITY_ODD` parity enabled, type odd

Definition at line 65 of file `uart_pal.h`.

17.148.3.3 enum `uart_stop_bit_count_t`

Defines the number of stop bits.

Implements : `uart_stop_bit_count_t_Class`

Enumerator

`UART_ONE_STOP_BIT` one stop bit
`UART_TWO_STOP_BIT` two stop bits

Definition at line 77 of file `uart_pal.h`.

17.148.3.4 enum `uart_transfer_type_t`

Defines the transfer type.

Implements : `uart_transfer_type_t_Class`

Enumerator

`UART_USING_DMA` Driver uses DMA for data transfers
`UART_USING_INTERRUPTS` Driver uses interrupts for data transfers

Definition at line 54 of file `uart_pal.h`.

17.148.4 Function Documentation

17.148.4.1 `status_t UART_AbortReceivingData (const uart_instance_t *const instance)`

Terminates a non-blocking receive early.

Parameters

<i>in</i>	<i>instance</i>	Pointer to the UART_PAL instance structure.
-----------	-----------------	---

Returns

STATUS_SUCCESS: if successful; STATUS_ERROR : if invalid instance type;

Definition at line 1018 of file uart_pal.c.

17.148.4.2 status_t UART_AbortSendingData (const uart_instance_t *const *instance*)

Terminates a non-blocking transmission early.

Parameters

<i>in</i>	<i>instance</i>	Pointer to the UART_PAL instance structure.
-----------	-----------------	---

Returns

STATUS_SUCCESS: if successful; STATUS_ERROR : if invalid instance type;

Definition at line 832 of file uart_pal.c.

17.148.4.3 status_t UART_Deinit (const uart_instance_t *const *instance*)

De-initializes the UART module.

This function de-initializes the UART module.

Parameters

<i>in</i>	<i>instance</i>	Pointer to the UART_PAL instance structure.
-----------	-----------------	---

Returns

STATUS_SUCCESS: if successful; STATUS_BUSY: if TX/RX line is busy; STATUS_ERROR : if invalid instance type;

Definition at line 556 of file uart_pal.c.

17.148.4.4 status_t UART_GetBaudRate (const uart_instance_t *const *instance*, uint32_t * *configuredBaudRate*)

Returns the UART baud rate.

This function returns the UART configured baud rate.

Parameters

<i>in</i>	<i>instance</i>	Pointer to the UART_PAL instance structure.
<i>out</i>	<i>configured↔ BaudRate</i>	Pointer to configured baud rate.

Returns

STATUS_SUCCESS: if successful; STATUS_ERROR : if invalid instance type;

Definition at line 687 of file uart_pal.c.

17.148.4.5 void UART_GetDefaultConfig (uart_user_config_t * *config*)

Gets the default configuration structure.

This function gets the default configuration structure, with the following settings:

- Baud rate: 9600
- Number of bits in a character: 8
- Parity mode: disable
- Number of stop bits: 1 stop bit
- Type of the transfer: interrupt
- Callback to invoke for data receive: NULL
- Receive callback parameter: NULL
- Callback to invoke for data send: NULL
- Transmit callback parameter: NULL
- Setup pins for FLEXIO: NULL

Parameters

out	config	Pointer to the UART_PAL user configuration structure.
-----	--------	---

Returns

NONE

Definition at line 396 of file uart_pal.c.

17.148.4.6 `status_t UART_GetReceiveStatus (const uart_instance_t *const instance, uint32_t * bytesRemaining)`

Get the status of the current non-blocking UART reception.

Parameters

in	instance	Pointer to the UART_PAL instance structure.
out	bytesRemaining	Pointer to value that is filled with the number of bytes that still need to be received in the active transfer

Note

In DMA mode, this parameter may not be accurate, in case the transfer completes right after calling this function; in this edge-case, the parameter will reflect the initial transfer size, due to automatic reloading of the major loop count in the DMA transfer descriptor.

return STATUS_SUCCESS : The reception has completed successfully; STATUS_BUSY : The reception is still in progress. *bytesReceived* will be filled with the number of bytes that have been received so far; STATUS_UART_RX_OVERFLOW : If an overrun error occurred during the reception; STATUS_UART_ABORTED : The reception was aborted; STATUS_TIMEOUT : A timeout was reached; STATUS_ERROR : An error occurred; return For LPUART used by UART_PAL: STATUS_UART_FRAMING_ERROR: If bit stop on frame is wrong; STATUS_UART_PARITY_ERROR : If bit parity on frame is wrong; STATUS_UART_NOISE_ERROR : If noise happens on bus;

Definition at line 1062 of file uart_pal.c.

17.148.4.7 `status_t UART_GetTransmitStatus (const uart_instance_t *const instance, uint32_t * bytesRemaining)`

Get the status of the current non-blocking UART transmission.

Parameters

in	<i>instance</i>	Pointer to the UART_PAL instance structure.
out	<i>bytesRemaining</i>	Pointer to value that is populated with the number of bytes that have been sent in the active transfer.

Note

In DMA mode, this parameter may not be accurate, in case the transfer completes right after calling this function; in this edge-case, the parameter will reflect the initial transfer size, due to automatic reloading of the major loop count in the DMA transfer descriptor.

Returns

STATUS_SUCCESS : The transmit has completed successfully; STATUS_BUSY : The transmit is still in progress. *bytesTransmitted* will be filled with the number of bytes that have been transmitted so far; STATUS_UART_ABORTED : The transmit was aborted; STATUS_TIMEOUT : A timeout was reached; STATUS_ERROR : An error occurred;

Definition at line 876 of file `uart_pal.c`.

17.148.4.8 `status_t UART_Init (const uart_instance_t *const instance, const uart_user_config_t * config)`

Initializes the UART module.

This function initializes and enables the requested UART module, configuring the bus parameters.

Parameters

in	<i>instance</i>	Pointer to the UART_PAL instance structure.
in	<i>config</i>	Pointer to the UART_PAL user configuration structure.

return STATUS_SUCCESS: if successful; STATUS_ERROR : if invalid instance type or init over supported hardware. return For LPUART, LINFLEXD_UART used by UART_PAL: STATUS_BUSY : if calling function while bus is busy;

Definition at line 419 of file `uart_pal.c`.

17.148.4.9 `status_t UART_ReceiveData (const uart_instance_t *const instance, uint8_t * rxBuff, uint32_t rxSize)`

Perform a non-blocking UART reception.

This function receives a block of data and returns immediately. The rest of the transmission is handled by the interrupt service routine (if the driver is initialized in interrupt mode).

Parameters

in	<i>instance</i>	Pointer to the UART_PAL instance structure.
out	<i>rxBuff</i>	Pointer to the data to be transferred.
in	<i>rxSize</i>	Length in bytes of the data to be transferred.

Returns

STATUS_BUSY : if bus is busy; STATUS_SUCCESS: if successful; STATUS_ERROR : An error occurred;

Definition at line 972 of file `uart_pal.c`.

17.148.4.10 `status_t UART_ReceiveDataBlocking (const uart_instance_t *const instance, uint8_t * rxBuff, uint32_t rxSize, uint32_t timeout)`

Perform a blocking UART reception.

This function receives a block of data and only returns when the transmission is complete.

Parameters

in	<i>instance</i>	Pointer to the UART_PAL instance structure.
out	<i>rxBuff</i>	Pointer to the receive buffer.
in	<i>rxSize</i>	Length in bytes of the data to be received.
in	<i>timeout</i>	Timeout for the transfer in milliseconds.

return STATUS_TIMEOUT : if waiting time for reception finished while receive data incompletely; STATUS_BUSY : if bus is busy; STATUS_SUCCESS : if successful; STATUS_UART_RX_OVERRUN : If an overrun error occurred during the reception; STATUS_ERROR : An error occurred; return For LPUART used by UART_PAL: STATUS_UART_FRAMING_ERROR: If bit stop on frame is wrong; STATUS_UART_PARITY_ERROR : If bit parity on frame is wrong; STATUS_UART_NOISE_ERROR : If noise happens on bus;

Definition at line 921 of file uart_pal.c.

17.148.4.11 `status_t UART_SendData (const uart_instance_t *const instance, const uint8_t * txBuff, uint32_t txSize)`

Perform a non-blocking UART transmission.

This function sends a block of data and returns immediately. The rest of the transmission is handled by the interrupt service routine (if the driver is initialized in interrupt mode).

Parameters

in	<i>instance</i>	Pointer to the UART_PAL instance structure.
in	<i>txBuffer</i>	Pointer to the data to be transferred.
in	<i>txSize</i>	Length in bytes of the data to be transferred.

Returns

STATUS_BUSY : if bus is busy; STATUS_SUCCESS: if successful; STATUS_ERROR : An error occurred;

Definition at line 785 of file uart_pal.c.

17.148.4.12 `status_t UART_SendDataBlocking (const uart_instance_t *const instance, const uint8_t * txBuff, uint32_t txSize, uint32_t timeout)`

Perform a blocking UART transmission.

This function sends a block of data and only returns when the transmission is complete.

Parameters

in	<i>instance</i>	Pointer to the UART_PAL instance structure.
in	<i>txBuffer</i>	Pointer to the data to be transferred.
in	<i>txSize</i>	Length in bytes of the data to be transferred.
in	<i>timeout</i>	Timeout value in milliseconds.

Returns

STATUS_TIMEOUT: if waiting time for transfer finished but transmit data incompletely; STATUS_BUSY : if bus is busy; STATUS_SUCCESS: if successful; STATUS_ERROR : An error occurred;

Definition at line 732 of file uart_pal.c.

17.148.4.13 `status_t UART_SetBaudRate (const uart_instance_t *const instance, uint32_t desiredBaudRate)`

Configures the UART baud rate.

This function configures the UART baud rate. Note that due to module limitation not any baud rate can be achieved. The driver will set a baud rate as close as possible to the requested baud rate, but there may still be substantial differences. The application should call [UART_GetBaudRate\(\)](#) after [UART_SetBaudRate\(\)](#) to check what baud rate was actually set.

Parameters

in	<i>instance</i>	Pointer to the UART_PAL instance structure.
in	<i>desiredBaudRate</i>	Desired baud rate.

Returns

STATUS_SUCCESS: if successful; STATUS_BUSY : if calling function while bus is busy; STATUS_ERROR : if invalid instance type;

Definition at line 633 of file uart_pal.c.

17.148.4.14 `status_t UART_SetRxBuffer (const uart_instance_t *const instance, uint8_t * rxBuff, uint32_t rxSize)`

Provide a buffer for receiving data.

The function can be used to provide a new buffer for receiving data to the driver. Beside, It can be called from rx callback to provide a new buffer for continuous reception.

Parameters

in	<i>instance</i>	Pointer to the UART_PAL instance structure.
in	<i>rxBuff</i>	Pointer to buffer containing received data.
in	<i>rxSize</i>	The number of bytes to receive.

Returns

STATUS_SUCCESS: Provide completed; STATUS_ERROR : if invalid instance type;

Definition at line 1107 of file uart_pal.c.

17.148.4.15 `status_t UART_SetTxBuffer (const uart_instance_t *const instance, const uint8_t * txBuff, uint32_t txSize)`

Provide a buffer for transmitting data.

The function can be used to provide a new buffer for transmitting data to the driver. Beside, It can be called from tx callback to provide a new buffer for continuous transmission.

Parameters

in	<i>instance</i>	Pointer to the UART_PAL instance structure.
in	<i>txBuff</i>	Pointer to buffer containing transmitted data.
in	<i>txSize</i>	The number of bytes to transmit.

Returns

STATUS_SUCCESS: Provide completed; STATUS_ERROR : if invalid instance type;

Definition at line 1151 of file uart_pal.c.

17.149 User provided call-outs

17.149.1 Detailed Description

This group contains APIs which may be called from within the LIN module in order to enable/disable LIN communication interrupts.

Functions

- `I_u16 I_sys_irq_disable (I_ifc_handle iii)`
Disable LIN related IRQ.
- `void I_sys_irq_restore (I_ifc_handle iii)`
Enable LIN related IRQ.

17.149.2 Function Documentation

17.149.2.1 I_u16 I_sys_irq_disable (I_ifc_handle iii)

Disable LIN related IRQ.

Parameters

<code>in</code>	<code>iii</code>	Interface name
-----------------	------------------	----------------

Returns

`I_u16`

Definition at line 543 of file `lin_common_api.c`.

17.149.2.2 void I_sys_irq_restore (I_ifc_handle iii)

Enable LIN related IRQ.

Parameters

<code>in</code>	<code>iii</code>	Interface name
-----------------	------------------	----------------

Returns

`void`

Definition at line 557 of file `lin_common_api.c`.

17.150 WDG PAL

17.150.1 Detailed Description

Watchdog Peripheral Abstraction Layer.

Data Structures

- struct [wdg_option_mode_t](#)
WDG PAL option mode configuration structure Implements : [wdg_option_mode_t_Class](#). [More...](#)
- struct [extension_ewm_for_wdg_t](#)
The extension structure for the EWM over WDOG peripheral Implements : [extension_ewm_for_wdg_t_Class](#). [More...](#)
- struct [wdg_config_t](#)
WDG PAL configuration structure Implements : [wdg_config_t_Class](#). [More...](#)

Enumerations

- enum [wdg_clock_source_t](#) { [WDG_PAL_BUS_CLOCK](#) = 0x00U, [WDG_PAL_LPO_CLOCK](#) = 0x01U, [WDG_PAL_SOSC_CLOCK](#) = 0x02U, [WDG_PAL_SIRC_CLOCK](#) = 0x03U }
 - enum [wdg_in_assert_logic_t](#) { [WDG_IN_ASSERT_DISABLED](#) = 0x00U, [WDG_IN_ASSERT_ON_LOGIC_ZERO](#) = 0x01U, [WDG_IN_ASSERT_ON_LOGIC_ONE](#) = 0x02U }
 - enum [wdg_inst_type_t](#)
- Enumeration with the types of peripherals supported by Watchdog PAL.*

WDG PAL API

- status_t [WDG_Init](#) (const [wdg_instance_t](#) *const instance, const [wdg_config_t](#) *configPtr)
Initializes the WDG PAL.
- void [WDG_GetDefaultConfig](#) ([wdg_config_t](#) *const config)
Gets default configuration of the WDG PAL.
- void [WDG_Refresh](#) (const [wdg_instance_t](#) *const instance)
Refreshes the WDG PAL counter.
- status_t [WDG_Deinit](#) (const [wdg_instance_t](#) *const instance)
De-initializes the WDG PAL.
- status_t [WDG_SetInt](#) (const [wdg_instance_t](#) *const instance, bool enable)
Set interrupt for WDG PAL.
- status_t [WDG_SetTimeout](#) (const [wdg_instance_t](#) *const instance, uint32_t value)
Sets the value of the WDG PAL timeout.
- status_t [WDG_SetWindow](#) (const [wdg_instance_t](#) *const instance, bool enable, uint32_t value)
Set window mode and window value of the WDG PAL.
- status_t [WDG_GetCounter](#) (const [wdg_instance_t](#) *const instance, uint32_t *value)
Gets the value of the WDG PAL counter.
- void [WDG_ClearIntFlag](#) (const [wdg_instance_t](#) *const instance)
Clears the Timeout Interrupt Flag.

17.150.2 Data Structure Documentation

17.150.2.1 struct wdg_option_mode_t

WDG PAL option mode configuration structure Implements : wdg_option_mode_t_Class.

Definition at line 64 of file wdg_pal.h.

Data Fields

- bool [wait](#)
- bool [stop](#)
- bool [debug](#)

Field Documentation

17.150.2.1.1 bool debug

Debug mode

Definition at line 68 of file wdg_pal.h.

17.150.2.1.2 bool stop

Stop mode

Definition at line 67 of file wdg_pal.h.

17.150.2.1.3 bool wait

Wait mode

Definition at line 66 of file wdg_pal.h.

17.150.2.2 struct extension_ewm_for_wdg_t

The extension structure for the EWM over WDOG peripheral Implements : extension_ewm_for_wdg_t_Class.

Definition at line 88 of file wdg_pal.h.

Data Fields

- [wdg_in_assert_logic_t](#) assertLogic
- [uint8_t](#) prescalerValue

Field Documentation

17.150.2.2.1 wdg_in_assert_logic_t assertLogic

Assert logic for EWM input pin

Definition at line 90 of file wdg_pal.h.

17.150.2.2.2 uint8_t prescalerValue

EWM clock prescaler

Definition at line 91 of file wdg_pal.h.

17.150.2.3 struct wdg_config_t

WDG PAL configuration structure Implements : wdg_config_t_Class.

Definition at line 99 of file wdg_pal.h.

Data Fields

- [wdg_clock_source_t](#) clkSource
- [wdg_option_mode_t](#) opMode
- [uint32_t](#) timeoutValue
- [uint8_t](#) percentWindow
- [bool](#) intEnable
- [bool](#) winEnable
- [bool](#) prescalerEnable
- [void *](#) extension

Field Documentation

17.150.2.3.1 [wdg_clock_source_t](#) clkSource

The clock source of the WDOG

Definition at line 101 of file [wdg_pal.h](#).

17.150.2.3.2 [void*](#) extension

This field will be add extra settings to EWM's configuration

Definition at line 109 of file [wdg_pal.h](#).

17.150.2.3.3 [bool](#) intEnable

If true, an interrupt request is generated before reset

Definition at line 105 of file [wdg_pal.h](#).

17.150.2.3.4 [wdg_option_mode_t](#) opMode

The modes in which the WDOG is functional

Definition at line 102 of file [wdg_pal.h](#).

17.150.2.3.5 [uint8_t](#) percentWindow

The window value compares to timeout value. Maximum value is 100

Definition at line 104 of file [wdg_pal.h](#).

17.150.2.3.6 [bool](#) prescalerEnable

If true, prescaler is enabled(default prescaler = 256)

Definition at line 107 of file [wdg_pal.h](#).

17.150.2.3.7 [uint32_t](#) timeoutValue

The timeout value

Definition at line 103 of file [wdg_pal.h](#).

17.150.2.3.8 [bool](#) winEnable

If true, window mode is enabled

Definition at line 106 of file [wdg_pal.h](#).

17.150.3 Enumeration Type Documentation

17.150.3.1 enum wdg_clock_source_t

Clock sources for the WDG PAL. Implements : wdg_clock_source_t_Class.

Enumerator

WDG_PAL_BUS_CLOCK Bus clock
WDG_PAL_LPO_CLOCK LPO clock
WDG_PAL_SOSC_CLOCK SOSC clock
WDG_PAL_SIRC_CLOCK SIRC clock

Definition at line 52 of file wdg_pal.h.

17.150.3.2 enum wdg_in_assert_logic_t

WDG PAL input pin configuration Configures if the input pin is enabled and when is asserted Implements : wdg_in_assert_logic_t_Class.

Enumerator

WDG_IN_ASSERT_DISABLED Input pin disabled
WDG_IN_ASSERT_ON_LOGIC_ZERO Input pin asserts EWM when on logic 0
WDG_IN_ASSERT_ON_LOGIC_ONE Input pin asserts EWM when on logic 1

Definition at line 77 of file wdg_pal.h.

17.150.3.3 enum wdg_inst_type_t

Enumeration with the types of peripherals supported by Watchdog PAL.

This enumeration contains the types of peripherals supported by Watchdog PAL. Implements : wdg_inst_type_t_Class

Definition at line 42 of file wdg_pal_mapping.h.

17.150.4 Function Documentation

17.150.4.1 void WDG_ClearIntFlag (const wdg_instance_t *const instance)

Clears the Timeout Interrupt Flag.

This function clears the Timeout Interrupt Flag.

Parameters

in	instance	The name of the instance.
----	----------	---------------------------

Definition at line 488 of file wdg_pal.c.

17.150.4.2 status_t WDG_Deinit (const wdg_instance_t *const instance)

De-initializes the WDG PAL.

This function resets all configuration to default and disable the WDG PAL instance.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance.
-----------	-----------------	---------------------------

Returns

operation status

- STATUS_SUCCESS : Operation was successful.
- STATUS_ERROR : Operation failed due to WDG PAL was locked.
- STATUS_UNSUPPORTED : Operation was unsupported.

Definition at line 282 of file wdg_pal.c.

17.150.4.3 status_t WDG_GetCounter (const wdg_instance_t *const instance, uint32_t * value)

Gets the value of the WDG PAL counter.

This function gets counter of WDG PAL module. Note that: Counter will be reset to timeout value if WDG PAL uses SWT. The counter will continue to run if WDG PAL uses WDOG.

Parameters

<i>in</i>	<i>instance</i>	The name of the instance.
<i>out</i>	<i>value</i>	Pointer to the counter value

Returns

operation status

- STATUS_SUCCESS : Operation was successful.
- STATUS_ERROR : Operation failed due to SWT was lock by hard lock.
- STATUS_UNSUPPORTED : Operation was unsupported.

Definition at line 440 of file wdg_pal.c.

17.150.4.4 void WDG_GetDefaultConfig (wdg_config_t *const config)

Gets default configuration of the WDG PAL.

This function gets the default configuration of the WDG PAL.

Parameters

<i>out</i>	<i>configures</i>	the default configuration
------------	-------------------	---------------------------

Definition at line 206 of file wdg_pal.c.

17.150.4.5 status_t WDG_Init (const wdg_instance_t *const instance, const wdg_config_t * configPtr)

Initializes the WDG PAL.

This function initializes the WDG instance by user configuration

Parameters

<i>in</i>	<i>instance</i>	The name of the instance.
<i>in</i>	<i>configPtr</i>	Pointer to the WDG PAL user configuration structure

Returns

operation status

- STATUS_SUCCESS : Operation was successful.
- STATUS_ERROR : Operation failed. Possible causes: previous clock source or the one specified in the configuration structure is disabled; WDG PAL configuration updates are not allowed.

- STATUS_UNSUPPORTED : Operation was unsupported.

Definition at line 80 of file wdg_pal.c.

17.150.4.6 void WDG_Refresh (const wdg_instance_t *const instance)

Refreshes the WDG PAL counter.

This function resets the WDG PAL counter

Parameters

in	instance	The name of the instance.
----	----------	---------------------------

Definition at line 243 of file wdg_pal.c.

17.150.4.7 status_t WDG_SetInt (const wdg_instance_t *const instance, bool enable)

Set interrupt for WDG PAL.

This function enables/disables the WDG PAL timeout interrupt and sets a function to be called when a timeout interrupt is received, before reset.

Parameters

in	instance	The name of the instance.
in	enable	<ul style="list-style-type: none"> • true : Enable interrupt • false : Disable interrupt

Returns

operation status

- STATUS_SUCCESS : Operation was successful.
- STATUS_ERROR : Operation failed. Possible causes: failed to WDG PAL configuration updates not allowed.
- STATUS_UNSUPPORTED: Operation was unsupported.

Definition at line 319 of file wdg_pal.c.

17.150.4.8 status_t WDG_SetTimeout (const wdg_instance_t *const instance, uint32_t value)

Sets the value of the WDG PAL timeout.

This function sets the value of the WDG PAL timeout.

Parameters

in	instance	The name of the instance.
in	value	The value of the WDG PAL timeout.

Returns

operation status

- STATUS_SUCCESS : Operation was successful.
- STATUS_ERROR : Operation failed due to WDG PAL was locked.
- STATUS_UNSUPPORTED : Operation was unsupported.

Definition at line 358 of file wdg_pal.c.

17.150.4.9 `status_t WDG_SetWindow (const wdg_instance_t *const instance, bool enable, uint32_t value)`

Set window mode and window value of the WDG PAL.

This function set window mode, window value is set when window mode enabled.

Parameters

in	<i>instance</i>	The name of the instance.
in	<i>enable</i>	<ul style="list-style-type: none">• true : Enable window mode• false : Disable window mode
in	<i>value</i>	The value of the WDG PAL window.

Returns

operation status

- STATUS_SUCCESS : Operation was successful.
- STATUS_ERROR : Operation failed due to WDG PAL was locked.
- STATUS_UNSUPPORTED : Operation was unsupported.

Definition at line 397 of file wdg_pal.c.

17.151 WDOG Driver

17.151.1 Detailed Description

Watchdog Timer Peripheral Driver.

How to use the WDOG driver in your application

In order to be able to use the Watchdog in your application, the first thing to do is initializing it with the desired configuration. This is done by calling the **WDOG_DRV_Init** function. One of the arguments passed to this function is the configuration which will be used for the Watchdog, specified by the **wdog_user_config_t** structure.

The **wdog_user_config_t** structure allows you to configure the following:

- the clock source of the Watchdog;
- the prescaler (a fixed 256 pre-scaling of the Watchdog counter reference clock may be enabled);
- the operation modes in which the Watchdog is functional (by default, the Watchdog is not functional in Debug mode, Wait mode or Stop mode);
- the timeout value to which the Watchdog counter is compared;
- the window mode option for the refresh mechanism (by default, the window mode is disabled, but it may be enabled and a window value may be set);
- the Watchdog timeout interrupt (if enabled, after a reset-triggering event, the Watchdog first generates an interrupt request; next, the Watchdog delays 128 bus clocks before forcing a reset, to allow the interrupt service routine to perform tasks (like analyzing the stack to debug code));
- the update mechanism (by default, the Watchdog reconfiguration is enabled, but updates can be disabled)

Please note that if the updates are disabled the Watchdog cannot be later modified without forcing a reset (this implies that further calls of the **WDOG_DRV_Init**, **WDOG_DRV_Deinit** or **WDOG_DRV_SetInt** functions will lead to a reset).

As mentioned before, a timeout interrupt may be enabled by specifying it at the module initialization. The **WDOG_DRV_Init** only allows enabling/disabling the interrupt, and it does not set up the ISR to be used for the interrupt request. In order to set up a function to be called after a reset-triggering event (and also enable/disable the interrupt), the **WDOG_DRV_SetInt** function may be used. **Please note** that, due to the 128 bus clocks delay before the reset, a limited amount of job can be done in the ISR.

Integration guideline

Compilation units

The following files need to be compiled in the project:

```
{S32SDK_PATH}\platform\drivers\src\wdog\wdog_driver.c
{S32SDK_PATH}\platform\drivers\src\wdog\wdog_hw_driver.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
{S32SDK_PATH}\platform\drivers\inc\
```

Compile symbols

No special symbols are required for this component

Dependencies

[Clock Manager Interrupt Manager \(Interrupt\)](#)

Basic Operations of WDOG

1. To initialize WDOG, call `WDOG_DRV_Init()` with an user configuration structure. In the following code, WDOG is initialized with default settings.

```
#define INST_WDOG1 (0U)

wdog_user_config_t userConfigPtr = {
    .WDOG_LPO_CLOCK,      /* Use the LPO clock as source */
    .opMode = {           /* WDOG not functional in Wait/Debug/Stop mode */
        false,
        false,
        false
    },
    .true,                /* Enable further updates of the WDOG configuration */
    .false,               /* Timeout interrupt disabled */
    .false,               /* Window mode disabled */
    .0U,                  /* Window value */
    .0x400,               /* Timeout value */
    .false                /* Prescaler disabled */
};

/* Initialize WDOG module */
WDOG_DRV_Init(INST_WDOG1, &userConfigPtr);
```

2. To get default configuration of WDOG module, just call the function `WDOG_DRV_GetDefaultConfig()`. Make sure that the operation before WDOG timeout executing.

```
wdog_user_config_t userConfigPtr;

/* Get default configuration of WDOG module */
WDOG_DRV_GetDefaultConfig(&userConfigPtr);
```

3. To refresh WDOG counter of WDOG module, just call the function `WDOG_DRV_Trigger()`. Make sure that the operation before WDOG timeout executing.

```
/* Refresh counter of WDOG counter */
WDOG_DRV_Trigger(INST_WDOG1);
```

4. To de-initialize WDOG module, just call the function `WDOG_DRV_Deinit()`. Make sure that the operation before WDOG timeout executing.

```
/* De-initialize WDOG module */
WDOG_DRV_Deinit(INST_WDOG1);
```

Example:

```
#define INST_WDOG1 (0U)

wdog_user_config_t userConfigPtr = {
    .WDOG_LPO_CLOCK,      /* Use the LPO clock as source */
    .opMode = {           /* WDOG not functional in Wait/Debug/Stop mode */
        false,
        false,
        false
    },
    .true,                /* Enable further updates of the WDOG configuration */
    .false,               /* Timeout interrupt disabled */
    .false,               /* Window mode disabled */
    .0U,                  /* Window value */
    .0x400,               /* Timeout value */
    .false                /* Prescaler disabled */
};

/* Initialize WDOG module */
WDOG_DRV_Init(INST_WDOG1, &userConfigPtr);

/* Enable the timeout interrupt and set the ISR */
WDOG_DRV_SetInt(INST_WDOG1, true);

while (1) {

    /* Do something that takes between 0x100 and 0x400 clock cycles */

    /* Refresh the counter */
    WDOG_DRV_Trigger(INST_WDOG1);
}

/* De-initialize WDOG module */
WDOG_DRV_Deinit(INST_WDOG1);
```

Data Structures

- struct [wdog_op_mode_t](#)
WDOG option mode configuration structure Implements : [wdog_op_mode_t_Class](#). [More...](#)
- struct [wdog_user_config_t](#)
WDOG user configuration structure Implements : [wdog_user_config_t_Class](#). [More...](#)

Enumerations

- enum [wdog_clk_source_t](#) { [WDOG_BUS_CLOCK](#) = 0x00U, [WDOG_LPO_CLOCK](#) = 0x01U, [WDOG_SOSC_CLOCK](#) = 0x02U, [WDOG_SIRC_CLOCK](#) = 0x03U }
Clock sources for the WDOG. Implements : [wdog_clk_source_t_Class](#).
- enum [wdog_test_mode_t](#) { [WDOG_TST_DISABLED](#) = 0x00U, [WDOG_TST_USER](#) = 0x01U, [WDOG_TST_LOW](#) = 0x02U, [WDOG_TST_HIGH](#) = 0x03U }
Test modes for the WDOG. Implements : [wdog_test_mode_t_Class](#).
- enum [wdog_set_mode_t](#) { [WDOG_DEBUG_MODE](#) = 0x00U, [WDOG_WAIT_MODE](#) = 0x01U, [WDOG_STOP_MODE](#) = 0x02U }
set modes for the WDOG. Implements : [wdog_set_mode_t_Class](#)

WDOG Driver API

- status_t [WDOG_DRV_Init](#) (uint32_t instance, const [wdog_user_config_t](#) *userConfigPtr)
Initializes the WDOG driver.
- status_t [WDOG_DRV_Deinit](#) (uint32_t instance)
De-initializes the WDOG driver.
- void [WDOG_DRV_GetConfig](#) (uint32_t instance, [wdog_user_config_t](#) *const config)
Gets the current configuration of the WDOG.
- void [WDOG_DRV_GetDefaultConfig](#) ([wdog_user_config_t](#) *const config)
Gets default configuration of the WDOG.
- status_t [WDOG_DRV_SetInt](#) (uint32_t instance, bool enable)
Enables/Disables the WDOG timeout interrupt and sets a function to be called when a timeout interrupt is received, before reset.
- void [WDOG_DRV_ClearIntFlag](#) (uint32_t instance)
Clear interrupt flag of the WDOG.
- void [WDOG_DRV_Trigger](#) (uint32_t instance)
Refreshes the WDOG counter.
- uint16_t [WDOG_DRV_GetCounter](#) (uint32_t instance)
Gets the value of the WDOG counter.
- status_t [WDOG_DRV_SetWindow](#) (uint32_t instance, bool enable, uint16_t windowvalue)
Set window mode and window value of the WDOG.
- status_t [WDOG_DRV_SetMode](#) (uint32_t instance, bool enable, [wdog_set_mode_t](#) Setmode)
Sets the mode operation of the WDOG.
- status_t [WDOG_DRV_SetTimeout](#) (uint32_t instance, uint16_t timeout)
Sets the value of the WDOG timeout.
- status_t [WDOG_DRV_SetTestMode](#) (uint32_t instance, [wdog_test_mode_t](#) testMode)
Changes the WDOG test mode.
- [wdog_test_mode_t](#) [WDOG_DRV_GetTestMode](#) (uint32_t instance)
Gets the WDOG test mode.

17.151.2 Data Structure Documentation

17.151.2.1 struct wdog_op_mode_t

WDOG option mode configuration structure Implements : wdog_op_mode_t_Class.

Definition at line 84 of file wdog_driver.h.

Data Fields

- bool [wait](#)
- bool [stop](#)
- bool [debug](#)

Field Documentation

17.151.2.1.1 bool debug

Debug mode

Definition at line 88 of file wdog_driver.h.

17.151.2.1.2 bool stop

Stop mode

Definition at line 87 of file wdog_driver.h.

17.151.2.1.3 bool wait

Wait mode

Definition at line 86 of file wdog_driver.h.

17.151.2.2 struct wdog_user_config_t

WDOG user configuration structure Implements : wdog_user_config_t_Class.

Definition at line 95 of file wdog_driver.h.

Data Fields

- [wdog_clk_source_t](#) clkSource
- [wdog_op_mode_t](#) opMode
- bool [updateEnable](#)
- bool [intEnable](#)
- bool [winEnable](#)
- [uint16_t](#) windowValue
- [uint16_t](#) timeoutValue
- bool [prescalerEnable](#)

Field Documentation

17.151.2.2.1 wdog_clk_source_t clkSource

The clock source of the WDOG

Definition at line 97 of file wdog_driver.h.

17.151.2.2.2 bool intEnable

If true, an interrupt request is generated before reset

Definition at line 100 of file wdog_driver.h.

17.151.2.2.3 `wdog_op_mode_t` `opMode`

The modes in which the WDOG is functional

Definition at line 98 of file `wdog_driver.h`.

17.151.2.2.4 `bool` `prescalerEnable`

If true, a fixed 256 prescaling of the counter reference clock is enabled

Definition at line 104 of file `wdog_driver.h`.

17.151.2.2.5 `uint16_t` `timeoutValue`

The timeout value

Definition at line 103 of file `wdog_driver.h`.

17.151.2.2.6 `bool` `updateEnable`

If true, further updates of the WDOG are enabled

Definition at line 99 of file `wdog_driver.h`.

17.151.2.2.7 `uint16_t` `windowValue`

The window value

Definition at line 102 of file `wdog_driver.h`.

17.151.2.2.8 `bool` `winEnable`

If true, window mode is enabled

Definition at line 101 of file `wdog_driver.h`.

17.151.3 Enumeration Type Documentation

17.151.3.1 `enum` `wdog_clk_source_t`

Clock sources for the WDOG. Implements : `wdog_clk_source_t_Class`.

Enumerator

`WDOG_BUS_CLOCK` Bus clock

`WDOG_LPO_CLOCK` LPO clock

`WDOG_SOSC_CLOCK` SOSC clock

`WDOG_SIRC_CLOCK` SIRC clock

Definition at line 49 of file `wdog_driver.h`.

17.151.3.2 `enum` `wdog_set_mode_t`

set modes for the WDOG. Implements : `wdog_set_mode_t_Class`

Enumerator

`WDOG_DEBUG_MODE` Debug mode

`WDOG_WAIT_MODE` Wait mode

`WDOG_STOP_MODE` Stop mode

Definition at line 73 of file `wdog_driver.h`.

17.151.3.3 enum wdog_test_mode_t

Test modes for the WDOG. Implements : wdog_test_mode_t_Class.

Enumerator

WDOG_TST_DISABLED Test mode disabled

WDOG_TST_USER User mode enabled. (Test mode disabled.)

WDOG_TST_LOW Test mode enabled, only the low byte is used.

WDOG_TST_HIGH Test mode enabled, only the high byte is used.

Definition at line 61 of file wdog_driver.h.

17.151.4 Function Documentation

17.151.4.1 void WDOG_DRV_ClearIntFlag (uint32_t instance)

Clear interrupt flag of the WDOG.

Parameters

in	instance	WDOG peripheral instance number
----	----------	---------------------------------

Definition at line 270 of file wdog_driver.c.

17.151.4.2 status_t WDOG_DRV_Deinit (uint32_t instance)

De-initializes the WDOG driver.

Parameters

in	instance	WDOG peripheral instance number
----	----------	---------------------------------

Returns

operation status

- STATUS_SUCCESS: if allowed reconfigures WDOG module and de-initializes successful.
- STATUS_ERROR: Operation failed. Possible causes: failed to WDOG configuration updates not allowed.

Definition at line 160 of file wdog_driver.c.

17.151.4.3 void WDOG_DRV_GetConfig (uint32_t instance, wdog_user_config_t *const config)

Gets the current configuration of the WDOG.

Parameters

in	instance	WDOG peripheral instance number
out	configures	the current configuration

Definition at line 195 of file wdog_driver.c.

17.151.4.4 uint16_t WDOG_DRV_GetCounter (uint32_t instance)

Gets the value of the WDOG counter.

Parameters

<i>in</i>	<i>instance</i>	WDOG peripheral instance number.
-----------	-----------------	----------------------------------

Returns

the value of the WDOG counter.

Definition at line 301 of file wdog_driver.c.

17.151.4.5 void WDOG_DRV_GetDefaultConfig (wdog_user_config_t *const config)

Gets default configuration of the WDOG.

Parameters

<i>out</i>	<i>configures</i>	the default configuration
------------	-------------------	---------------------------

Definition at line 212 of file wdog_driver.c.

17.151.4.6 wdog_test_mode_t WDOG_DRV_GetTestMode (uint32_t instance)

Gets the WDOG test mode.

This function verifies the test mode of the WDOG.

Parameters

<i>in</i>	<i>instance</i>	WDOG peripheral instance number
-----------	-----------------	---------------------------------

Returns

Test modes for the WDOG

Definition at line 459 of file wdog_driver.c.

17.151.4.7 status_t WDOG_DRV_Init (uint32_t instance, const wdog_user_config_t * userConfigPtr)

Initializes the WDOG driver.

Parameters

<i>in</i>	<i>instance</i>	WDOG peripheral instance number
<i>in</i>	<i>userConfigPtr</i>	pointer to the WDOG user configuration structure

Returns

operation status

- STATUS_SUCCESS: Operation was successful.
- STATUS_ERROR: Operation failed. Possible causes: previous clock source or the one specified in the configuration structure is disabled; WDOG configuration updates are not allowed; WDOG instance has been initialized before; If window mode enabled and window value greater than or equal to the timeout value.

Definition at line 102 of file wdog_driver.c.

17.151.4.8 status_t WDOG_DRV_SetInt (uint32_t instance, bool enable)

Enables/Disables the WDOG timeout interrupt and sets a function to be called when a timeout interrupt is received, before reset.

Parameters

in	<i>instance</i>	WDOG peripheral instance number
in	<i>enable</i>	enable/disable interrupt

Returns

operation status

- STATUS_SUCCESS: if allowed reconfigures WDOG timeout interrupt.
- STATUS_ERROR: Operation failed. Possible causes: failed to WDOG configuration updates not allowed.

Definition at line 238 of file wdog_driver.c.

17.151.4.9 `status_t WDOG_DRV_SetMode (uint32_t instance, bool enable, wdog_set_mode_t Setmode)`

Sets the mode operation of the WDOG.

This function changes the mode operation of the WDOG.

Parameters

in	<i>instance</i>	WDOG peripheral instance number.
in	<i>enable</i>	enable/disable mode of the WDOG.
in	<i>Setmode</i>	select mode of the WDOG.

Returns

operation status

- STATUS_SUCCESS: if allowed reconfigures mode operation of the WDOG.
- STATUS_ERROR: Operation failed. Possible causes: failed to WDOG configuration updates not allowed.

Definition at line 352 of file wdog_driver.c.

17.151.4.10 `status_t WDOG_DRV_SetTestMode (uint32_t instance, wdog_test_mode_t testMode)`

Changes the WDOG test mode.

This function changes the test mode of the WDOG. If the WDOG is tested in mode, software should set this field to 0x01U in order to indicate that the WDOG is functioning normally.

Parameters

in	<i>instance</i>	WDOG peripheral instance number
in	<i>testMode</i>	Test modes for the WDOG.

Returns

operation status

- STATUS_SUCCESS: if allowed reconfigures WDOG test mode.
- STATUS_ERROR: Operation failed. Possible causes: failed to WDOG configuration updates not allowed.

Definition at line 426 of file wdog_driver.c.

17.151.4.11 `status_t WDOG_DRV_SetTimeout (uint32_t instance, uint16_t timeout)`

Sets the value of the WDOG timeout.

This function sets the value of the WDOG timeout.

Parameters

in	<i>instance</i>	WDOG peripheral instance number.
in	<i>timeout</i>	the value of the WDOG timeout.

Returns

operation status

- STATUS_SUCCESS: if allowed reconfigures WDOG timeout.
- STATUS_ERROR: Operation failed. Possible causes: failed to WDOG configuration updates not allowed.

Definition at line 397 of file wdog_driver.c.

17.151.4.12 `status_t WDOG_DRV_SetWindow (uint32_t instance, bool enable, uint16_t windowvalue)`

Set window mode and window value of the WDOG.

This function set window mode, window value is set when window mode enabled.

Parameters

in	<i>instance</i>	WDOG peripheral instance number.
in	<i>enable</i>	enable/disable window mode and window value.
in	<i>windowvalue</i>	the value of the WDOG window.

Returns

operation status

- STATUS_SUCCESS: if allowed reconfigures window value success.
- STATUS_ERROR: Operation failed. Possible causes: failed to WDOG configuration updates not allowed.

Definition at line 316 of file wdog_driver.c.

17.151.4.13 `void WDOG_DRV_Trigger (uint32_t instance)`

Refreshes the WDOG counter.

Parameters

in	<i>instance</i>	WDOG peripheral instance number
----	-----------------	---------------------------------

Definition at line 286 of file wdog_driver.c.

17.152 Watchdog Peripheral Abstraction Layer (WDG PAL)

17.152.1 Detailed Description

The S32 SDK provides a Peripheral Abstraction Layer for Watchdog (WDG PAL) modules of S32 SDK devices.

The Watchdog PAL driver allows to generate interrupt event to reset CPU or external circuit. It was designed to be portable across all platforms and IPs which support Watchdog Timer.

Integration guideline

Define IPs specification

Unlike the other drivers, WDG PAL modules need to include a configuration file named `wdg_pal_cfg.h`, which allows the user to specify which IPs are used and how many resources are allocated for each of them (state structures). The following code example shows how to configure one instance for each available WDG IPs.

```
#ifndef WDG_PAL_CFG_H
#define WDG_PAL_CFG_H

/* Define which IP instance will be used in current project */
#define WDG_OVER_WDOG
#define WDG_OVER_EWM
#define WDG_OVER_SWT

/* Define the resources necessary for current project */
#define WDG_OVER_WDOG_INSTANCE_COUNT 1U
#define WDG_OVER_EWM_INSTANCE_COUNT 1U
#define WDG_OVER_SWT_INSTANCE_COUNT 0U

#endif /* WDG_PAL_CFG_H */
```

The following table contains the matching between platforms and available IPs

IP/MCU	S32K11x	S32K14x	MPC574x	S32Rx7x
WDOG	YES	YES	NO	NO
EWM	NO	YES	NO	NO
SWT	NO	NO	YES	YES

Compilation units

The following files need to be compiled in the project:

```
${S32SDK_PATH}\platform\pal\src\wdg\wdg_pal.c
```

Include path

The following paths need to be added to the include path of the toolchain:

```
${S32SDK_PATH}\platform\pal\inc
```

Compile symbols

No special symbols are required for this component

Dependencies

- [Clock Manager](#)
- [Interrupt Manager \(Interrupt\)](#)
- [External Watchdog Monitor \(EWM\)](#)

- [Watchdog timer \(WDOG\)](#)
- [swt](#)

Functionality

Initialization

In order to use the WDG PAL driver it must be first initialized, using [WDG_Init\(\)](#) function. Once initialized, it cannot be initialized again for the same WDG module instance until it is de-initialized, using [WDG_Deinit\(\)](#). Different WDG modules instances can function independently of each other.

Interrupt event

After initialization, WDG PAL counter will count to timeout value. In window mode, when WDG PAL counter is refreshed, it will reset count to default value and count again. If WDG PAL counter count to timeout value, CPU or the external circuit will be reseted or placed into safe mode.

The configuration structure includes a special field named extension. It will be used only for WDG PAL over EWM peripheral and should contain a pointer to [extension_ewm_for_wdg_t](#) structure. The purpose of this structure is to configure which EWM_OUT pins and clock prescaler are used by the applications.

WDG PAL internal counter

WDG PAL internal counter is

- 8 bit if WDG PAL uses EWM
- 16 bit if WDG PAL uses WDOG
- 32 bit if WDG PAL uses SWT

WDG PAL's counter over EWM and WDOG will start to count from 0 to timeout value. WDG PAL's counter over SWT will start to count from timeout value to 0.

Important Notes

- Before using the WDG PAL driver the module clock must be configured. Refer to Clock Manager for clock configuration.
- The driver enables the interrupts for the corresponding WDG PAL module, but any interrupt priority must be done by the application
- For WDG PAL over SWT, if the counter clock is slow, the software needs a wait time (inversely proportional to counter clock frequency) to synchronization completed.

Example code

```
const wdg_instance_t wdg_pal1_Instance =
{
    .instType = WDG_INST_TYPE_WDOG,
    .instIdx  = 0U
};

const wdg_instance_t wdg_pal2_Instance =
{
    .instType = WDG_INST_TYPE_EWM,
    .instIdx  = 0U
};

const wdg_instance_t wdg_pal3_Instance =
{
    .instType = WDG_INST_TYPE_SWT,
    .instIdx  = 0U
};
```

```

/* Serial User Configurations */

const wdg_config_t wdg_pal1_Config0 =
{
    .clkSource      = WDG_PAL_LPO_CLOCK,
    .opMode         =
    {
        .wait       = false,
        .stop       = false,
        .debug      = false
    },
    .timeoutValue   = 1024,
    .percentWindow  = 50,
    .intEnable      = true,
    .winEnable      = true,
    .prescalerEnable = true
};

const wdg_config_t wdg_pal2_Config0 =
{
    .clkSource      = WDG_PAL_LPO_CLOCK,
    .opMode         =
    {
        .wait       = false,
        .stop       = false,
        .debug      = false
    },
    .timeoutValue   = 254,
    .percentWindow  = 100,
    .intEnable      = true,
    .winEnable      = true,
    .prescalerEnable = true,
    .extension      = &wdg_pal2_Extension0
};

extension_ewm_for_wdg_t wdg_pal2_Extension0 =
{
    .assertLogic    = WDG_IN_ASSERT_ON_LOGIC_ZERO,
    .prescalerValue = 251
};

const wdg_config_t wdg_pal3_Config0 =
{
    .clkSource      = WDG_PAL_LPO_CLOCK,
    .opMode         =
    {
        .wait       = false,
        .stop       = false,
        .debug      = false
    },
    .timeoutValue   = 2560,
    .percentWindow  = 50,
    .intEnable      = true,
    .winEnable      = true,
    .prescalerEnable = false
};

int main()
{
    /* Init clocks, pins, led and other modules */
    ...

    /* Initialize WDG PAL */
    WDG_Init(&wdg_pal1_Instance, &wdg_pal1_Config0);

    /* Infinite loop*/
    while(1)
    {
        /* Do something until the counter needs to be refreshed */
        ...
        /* Reset WDG PAL counter */
        WDG_Refresh(&wdg_pal1_Instance);
    }
}

```

Modules

- [WDG PAL](#)

Watchdog Peripheral Abstraction Layer.

17.153 Watchdog timer (WDOG)

17.153.1 Detailed Description

The S32 SDK provides Peripheral Driver for the Watchdog timer (WDOG) module of S32 SDK devices.

Hardware background

The Watchdog Timer (WDOG) module is an independent timer that is available for system use. It provides a safety feature to ensure that software is executing as planned and that the CPU is not stuck in an infinite loop or executing unintended code. If the WDOG module is not serviced (refreshed) within a certain period, it resets the MCU.

Features of the WDOG module include:

- Configurable clock source inputs independent from the bus clock
- Programmable timeout period
 - Programmable 16-bit timeout value
 - Optional fixed 256 clock prescaler when longer timeout periods are needed
- Window mode option for the refresh mechanism
 - Programmable 16-bit window value
 - Provides robust check that program flow is faster than expected
 - Early refresh attempts trigger a reset
- Optional timeout interrupt to allow post-processing diagnostics
 - Interrupt request to CPU with interrupt vector for an interrupt service routine (ISR)
 - Forced reset occurs 128 bus clocks after the interrupt vector fetch
- Configuration bits are write-once-after-reset to ensure watchdog configuration cannot be mistakenly altered
- Robust write sequence for unlocking write-once configuration bits

Modules

- [WDOG Driver](#)
Watchdog Timer Peripheral Driver.

18 Data Structure Documentation

18.1 __blake2b_param Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/blake2-int.h>
```

Data Fields

- byte [digest_length](#)
- byte [key_length](#)
- byte [fanout](#)
- byte [depth](#)
- word32 [leaf_length](#)
- word64 [node_offset](#)
- byte [node_depth](#)
- byte [inner_length](#)
- byte [reserved](#) [14]
- byte [salt](#) [BLAKE2B_SALTBYTES]
- byte [personal](#) [BLAKE2B_PERSONALBYTES]

18.1.1 Detailed Description

Definition at line 100 of file blake2-int.h.

18.1.2 Field Documentation

18.1.2.1 byte depth

Definition at line 105 of file blake2-int.h.

18.1.2.2 byte digest_length

Definition at line 102 of file blake2-int.h.

18.1.2.3 byte fanout

Definition at line 104 of file blake2-int.h.

18.1.2.4 byte inner_length

Definition at line 109 of file blake2-int.h.

18.1.2.5 byte key_length

Definition at line 103 of file blake2-int.h.

18.1.2.6 word32 leaf_length

Definition at line 106 of file blake2-int.h.

18.1.2.7 byte node_depth

Definition at line 108 of file blake2-int.h.

18.1.2.8 word64 node_offset

Definition at line 107 of file blake2-int.h.

18.1.2.9 `byte personal[BLAKE2B_PERSONALBYTES]`

Definition at line 112 of file `blake2-int.h`.

18.1.2.10 `byte reserved[14]`

Definition at line 110 of file `blake2-int.h`.

18.1.2.11 `byte salt[BLAKE2B_SALTBYTES]`

Definition at line 111 of file `blake2-int.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/blake2-int.h`

18.2 `__blake2bp_state` Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/blake2-int.h>
```

Data Fields

- `blake2b_state S` [4][1]
- `blake2b_state R` [1]
- `byte buf` [4 *`BLAKE2B_BLOCKBYTES`]
- `word64 buflen`

18.2.1 Detailed Description

Definition at line 133 of file `blake2-int.h`.

18.2.2 Field Documentation

18.2.2.1 `byte buf[4 *BLAKE2B_BLOCKBYTES]`

Definition at line 137 of file `blake2-int.h`.

18.2.2.2 `word64 buflen`

Definition at line 138 of file `blake2-int.h`.

18.2.2.3 `blake2b_state R[1]`

Definition at line 136 of file `blake2-int.h`.

18.2.2.4 `blake2b_state S[4][1]`

Definition at line 135 of file `blake2-int.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/blake2-int.h`

18.3 `__blake2s_param` Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/blake2-int.h>
```

Data Fields

- byte [digest_length](#)
- byte [key_length](#)
- byte [fanout](#)
- byte [depth](#)
- word32 [leaf_length](#)
- byte [node_offset](#) [6]
- byte [node_depth](#)
- byte [inner_length](#)
- byte [salt](#) [BLAKE2B_SALTBYTES]
- byte [personal](#) [BLAKE2S_PERSONALBYTES]

18.3.1 Detailed Description

Definition at line 75 of file blake2-int.h.

18.3.2 Field Documentation

18.3.2.1 byte depth

Definition at line 80 of file blake2-int.h.

18.3.2.2 byte digest_length

Definition at line 77 of file blake2-int.h.

18.3.2.3 byte fanout

Definition at line 79 of file blake2-int.h.

18.3.2.4 byte inner_length

Definition at line 84 of file blake2-int.h.

18.3.2.5 byte key_length

Definition at line 78 of file blake2-int.h.

18.3.2.6 word32 leaf_length

Definition at line 81 of file blake2-int.h.

18.3.2.7 byte node_depth

Definition at line 83 of file blake2-int.h.

18.3.2.8 byte node_offset[6]

Definition at line 82 of file blake2-int.h.

18.3.2.9 byte personal[BLAKE2S_PERSONALBYTES]

Definition at line 87 of file blake2-int.h.

18.3.2.10 byte salt[BLAKE2B_SALTBYTES]

Definition at line 86 of file blake2-int.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/blake2-int.h`

18.4 `__blake2sp_state` Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/blake2-int.h>
```

Data Fields

- `blake2s_state` [S](#) [8][1]
- `blake2s_state` [R](#) [1]
- `byte` [buf](#) [8 *BLAKE2S_BLOCKBYTES]
- `word64` [buflen](#)

18.4.1 Detailed Description

Definition at line 125 of file `blake2-int.h`.

18.4.2 Field Documentation

18.4.2.1 `byte buf[8 *BLAKE2S_BLOCKBYTES]`

Definition at line 129 of file `blake2-int.h`.

18.4.2.2 `word64 buflen`

Definition at line 130 of file `blake2-int.h`.

18.4.2.3 `blake2s_state R[1]`

Definition at line 128 of file `blake2-int.h`.

18.4.2.4 `blake2s_state S[8][1]`

Definition at line 127 of file `blake2-int.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/blake2-int.h`

18.5 `adc_callback_info_t` Struct Reference

Defines a structure used to pass information to the ADC PAL callback.

```
#include <platform/devices/callbacks.h>
```

Data Fields

- `uint32_t` [groupIndex](#)
- `uint16_t` [resultBufferTail](#)

18.5.1 Detailed Description

Defines a structure used to pass information to the ADC PAL callback.

Implements : `adc_callback_info_t_Class`

Definition at line 108 of file `callbacks.h`.

18.5.2 Field Documentation

18.5.2.1 `uint32_t groupIndex`

Index of the group executing the callback.

Definition at line 110 of file `callbacks.h`.

18.5.2.2 `uint16_t resultBufferTail`

Offset of the most recent conversion result in the result buffer.

Definition at line 111 of file `callbacks.h`.

The documentation for this struct was generated from the following file:

- `platform/devices/callbacks.h`

18.6 `adc_instance_t` Struct Reference

Structure storing PAL instance information.

```
#include <platform/pal/inc/adc_pal_mapping.h>
```

Data Fields

- `adc_inst_type_t instType`
- `uint32_t instIdx`

18.6.1 Detailed Description

Structure storing PAL instance information.

This structure is used for storing PAL instance information. Implements : `adc_instance_t_Class`

Definition at line 74 of file `adc_pal_mapping.h`.

18.6.2 Field Documentation

18.6.2.1 `uint32_t instIdx`

Instance index of the peripheral (for ADC PAL the triggering peripheral) over which the PAL is used

Definition at line 77 of file `adc_pal_mapping.h`.

18.6.2.2 `adc_inst_type_t instType`

Peripheral over which the PAL is used

Definition at line 76 of file `adc_pal_mapping.h`.

The documentation for this struct was generated from the following file:

- `platform/pal/inc/adc_pal_mapping.h`

18.7 Aes Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/aes.h>
```

Data Fields

- ALIGN16 word32 [key](#) [60]
- word32 [rounds](#)
- int [keylen](#)
- ALIGN16 word32 [reg](#) [AES_BLOCK_SIZE/sizeof(word32)]
- ALIGN16 word32 [tmp](#) [AES_BLOCK_SIZE/sizeof(word32)]
- void * [heap](#)

18.7.1 Detailed Description

Definition at line 76 of file aes.h.

18.7.2 Field Documentation**18.7.2.1 void* heap**

Definition at line 113 of file aes.h.

18.7.2.2 ALIGN16 word32 key[60]

Definition at line 78 of file aes.h.

18.7.2.3 int keylen

Definition at line 80 of file aes.h.

18.7.2.4 ALIGN16 word32 reg[AES_BLOCK_SIZE/sizeof(word32)]

Definition at line 82 of file aes.h.

18.7.2.5 word32 rounds

Definition at line 79 of file aes.h.

18.7.2.6 ALIGN16 word32 tmp[AES_BLOCK_SIZE/sizeof(word32)]

Definition at line 83 of file aes.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/aes.h`

18.8 Arc4 Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/arc4.h>
```

Data Fields

- byte [x](#)
- byte [y](#)
- byte [state](#) [ARC4_STATE_SIZE]
- void * [heap](#)

18.8.1 Detailed Description

Definition at line 43 of file arc4.h.

18.8.2 Field Documentation

18.8.2.1 void* heap

Definition at line 50 of file arc4.h.

18.8.2.2 byte state[ARC4_STATE_SIZE]

Definition at line 46 of file arc4.h.

18.8.2.3 byte x

Definition at line 44 of file arc4.h.

18.8.2.4 byte y

Definition at line 45 of file arc4.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/arc4.h`

18.9 Arrays Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- byte * [pendingMsg](#)
- byte * [preMasterSecret](#)
- word32 [preMasterSz](#)
- word32 [pendingMsgSz](#)
- word32 [pendingMsgOffset](#)
- word32 [psk_keySz](#)
- char [client_identity](#) [MAX_PSK_ID_LEN+NULL_TERM_LEN]
- char [server_hint](#) [MAX_PSK_ID_LEN+NULL_TERM_LEN]
- byte [psk_key](#) [MAX_PSK_KEY_LEN]
- byte [clientRandom](#) [RAN_LEN]
- byte [serverRandom](#) [RAN_LEN]
- byte [sessionID](#) [ID_LEN]
- byte [sessionIDSz](#)
- byte [masterSecret](#) [SECRET_LEN]
- byte [pendingMsgType](#)

18.9.1 Detailed Description

Definition at line 2935 of file internal.h.

18.9.2 Field Documentation

18.9.2.1 char client_identity[MAX_PSK_ID_LEN+NULL_TERM_LEN]

Definition at line 2943 of file internal.h.

18.9.2.2 byte clientRandom[RAN_LEN]

Definition at line 2947 of file internal.h.

18.9.2.3 byte masterSecret[SECRET_LEN]

Definition at line 2956 of file internal.h.

18.9.2.4 byte* pendingMsg

Definition at line 2936 of file internal.h.

18.9.2.5 word32 pendingMsgOffset

Definition at line 2940 of file internal.h.

18.9.2.6 word32 pendingMsgSz

Definition at line 2939 of file internal.h.

18.9.2.7 byte pendingMsgType

Definition at line 2961 of file internal.h.

18.9.2.8 byte* preMasterSecret

Definition at line 2937 of file internal.h.

18.9.2.9 word32 preMasterSz

Definition at line 2938 of file internal.h.

18.9.2.10 byte psk_key[MAX_PSK_KEY_LEN]

Definition at line 2945 of file internal.h.

18.9.2.11 word32 psk_keySz

Definition at line 2942 of file internal.h.

18.9.2.12 char server_hint[MAX_PSK_ID_LEN+NULL_TERM_LEN]

Definition at line 2944 of file internal.h.

18.9.2.13 byte serverRandom[RAN_LEN]

Definition at line 2948 of file internal.h.

18.9.2.14 byte sessionID[ID_LEN]

Definition at line 2949 of file internal.h.

18.9.2.15 byte sessionIDSz

Definition at line 2950 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.10 Base_entry Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h>
```

Data Fields

- [Base_entry * next](#)
- `char * name`
- `int nameSz`
- `byte type`

18.10.1 Detailed Description

Definition at line 385 of file `asn.h`.

18.10.2 Field Documentation

18.10.2.1 `char* name`

Definition at line 387 of file `asn.h`.

18.10.2.2 `int nameSz`

Definition at line 388 of file `asn.h`.

18.10.2.3 `Base_entry* next`

Definition at line 386 of file `asn.h`.

18.10.2.4 `byte type`

Definition at line 389 of file `asn.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h`

18.11 Buffers Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- `bufferStatic inputBuffer`
- `bufferStatic outputBuffer`
- `buffer domainName`
- `buffer clearOutputBuffer`
- `buffer sig`
- `buffer digest`
- `int prevSent`
- `int plainSz`
- `byte weOwnCert`
- `byte weOwnCertChain`
- `byte weOwnKey`
- `byte weOwnDH`
- `buffer serverDH_P`
- `buffer serverDH_G`
- `buffer serverDH_Pub`
- `buffer serverDH_Priv`

- [DhKey * serverDH_Key](#)
- [DerBuffer * certificate](#)
- [DerBuffer * key](#)
- [byte keyType](#)
- [int keySz](#)
- [DerBuffer * certChain](#)

18.11.1 Detailed Description

Definition at line 2726 of file internal.h.

18.11.2 Field Documentation

18.11.2.1 **DerBuffer*** certChain

Definition at line 2753 of file internal.h.

18.11.2.2 **DerBuffer*** certificate

Definition at line 2749 of file internal.h.

18.11.2.3 **buffer** clearOutputBuffer

Definition at line 2730 of file internal.h.

18.11.2.4 **buffer** digest

Definition at line 2732 of file internal.h.

18.11.2.5 **buffer** domainName

Definition at line 2729 of file internal.h.

18.11.2.6 **bufferStatic** inputBuffer

Definition at line 2727 of file internal.h.

18.11.2.7 **DerBuffer*** key

Definition at line 2750 of file internal.h.

18.11.2.8 **int** keySz

Definition at line 2752 of file internal.h.

18.11.2.9 **byte** keyType

Definition at line 2751 of file internal.h.

18.11.2.10 **bufferStatic** outputBuffer

Definition at line 2728 of file internal.h.

18.11.2.11 **int** plainSz

Definition at line 2735 of file internal.h.

18.11.2.12 **int** prevSent

Definition at line 2733 of file internal.h.

18.11.2.13 buffer serverDH_G

Definition at line 2743 of file internal.h.

18.11.2.14 DhKey* serverDH_Key

Definition at line 2746 of file internal.h.

18.11.2.15 buffer serverDH_P

Definition at line 2742 of file internal.h.

18.11.2.16 buffer serverDH_Priv

Definition at line 2745 of file internal.h.

18.11.2.17 buffer serverDH_Pub

Definition at line 2744 of file internal.h.

18.11.2.18 buffer sig

Definition at line 2731 of file internal.h.

18.11.2.19 byte weOwnCert

Definition at line 2737 of file internal.h.

18.11.2.20 byte weOwnCertChain

Definition at line 2738 of file internal.h.

18.11.2.21 byte weOwnDH

Definition at line 2740 of file internal.h.

18.11.2.22 byte weOwnKey

Definition at line 2739 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.12 bufferStatic Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- ALIGN16 byte [staticBuffer](#) [STATIC_BUFFER_LEN]
- byte * [buffer](#)
- word32 [length](#)
- word32 [idx](#)
- word32 [bufferSize](#)
- byte [dynamicFlag](#)
- byte [offset](#)

18.12.1 Detailed Description

Definition at line 1517 of file internal.h.

18.12.2 Field Documentation

18.12.2.1 `byte* buffer`

Definition at line 1519 of file internal.h.

18.12.2.2 `word32 bufferSize`

Definition at line 1522 of file internal.h.

18.12.2.3 `byte dynamicFlag`

Definition at line 1523 of file internal.h.

18.12.2.4 `word32 idx`

Definition at line 1521 of file internal.h.

18.12.2.5 `word32 length`

Definition at line 1520 of file internal.h.

18.12.2.6 `byte offset`

Definition at line 1524 of file internal.h.

18.12.2.7 `ALIGN16 byte staticBuffer[STATIC_BUFFER_LEN]`

Definition at line 1518 of file internal.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/internal.h`

18.13 BuildMsgArgs Struct Reference

Data Fields

- `word32 digestSz`
- `word32 sz`
- `word32 pad`
- `word32 idx`
- `word32 headerSz`
- `word16 size`
- `word32 ivSz`
- `byte iv [AES_BLOCK_SIZE]`

18.13.1 Detailed Description

Definition at line 12581 of file internal.c.

18.13.2 Field Documentation

18.13.2.1 word32 digestSz

Definition at line 12582 of file internal.c.

18.13.2.2 word32 headerSz

Definition at line 12586 of file internal.c.

18.13.2.3 word32 idx

Definition at line 12585 of file internal.c.

18.13.2.4 byte iv[AES_BLOCK_SIZE]

Definition at line 12589 of file internal.c.

18.13.2.5 word32 ivSz

Definition at line 12588 of file internal.c.

18.13.2.6 word32 pad

Definition at line 12584 of file internal.c.

18.13.2.7 word16 size

Definition at line 12587 of file internal.c.

18.13.2.8 word32 sz

Definition at line 12583 of file internal.c.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/src/internal.c

18.14 callback_functions Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/test.h>
```

Data Fields

- method_provider [method](#)
- ctx_callback [ctx_ready](#)
- ssl_callback [ssl_ready](#)
- ssl_callback [on_result](#)

18.14.1 Detailed Description

Definition at line 333 of file test.h.

18.14.2 Field Documentation

18.14.2.1 ctx_callback ctx_ready

Definition at line 335 of file test.h.

18.14.2.2 `method_provider` method

Definition at line 334 of file `test.h`.

18.14.2.3 `ssl_callback` on_result

Definition at line 337 of file `test.h`.

18.14.2.4 `ssl_callback` ssl_ready

Definition at line 336 of file `test.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/test.h`

18.15 `can_instance_t` Struct Reference

Structure storing PAL instance information.

```
#include <platform/pal/inc/can_pal_mapping.h>
```

Data Fields

- `can_inst_type_t` [instType](#)
- `uint32_t` [instIdx](#)

18.15.1 Detailed Description

Structure storing PAL instance information.

This structure is used for storing PAL instance information. Implements : `can_instance_t_Class`

Definition at line 54 of file `can_pal_mapping.h`.

18.15.2 Field Documentation

18.15.2.1 `uint32_t` instIdx

Instance index of the peripheral over which the PAL is used

Definition at line 56 of file `can_pal_mapping.h`.

18.15.2.2 `can_inst_type_t` instType

Peripheral over which the PAL is used

Definition at line 55 of file `can_pal_mapping.h`.

The documentation for this struct was generated from the following file:

- `platform/pal/inc/can_pal_mapping.h`

18.16 `CertSignCtx` Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h>
```

Data Fields

- byte * [sig](#)
- byte * [digest](#)
- byte * [encSig](#)
- int [encSigSz](#)
- int [state](#)

18.16.1 Detailed Description

Definition at line 467 of file `asn.h`.

18.16.2 Field Documentation

18.16.2.1 byte* digest

Definition at line 469 of file `asn.h`.

18.16.2.2 byte* encSig

Definition at line 471 of file `asn.h`.

18.16.2.3 int encSigSz

Definition at line 472 of file `asn.h`.

18.16.2.4 byte* sig

Definition at line 468 of file `asn.h`.

18.16.2.5 int state

Definition at line 474 of file `asn.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h`

18.17 Ciphers Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [Arc4](#) * [arc4](#)
- [Des3](#) * [des3](#)
- [Aes](#) * [aes](#)
- byte [state](#)
- byte [setup](#)

18.17.1 Detailed Description

Definition at line 2534 of file `internal.h`.

18.17.2 Field Documentation

18.17.2.1 **Aes*** aes

Definition at line 2542 of file internal.h.

18.17.2.2 **Arc4*** arc4

Definition at line 2536 of file internal.h.

18.17.2.3 **Des3*** des3

Definition at line 2539 of file internal.h.

18.17.2.4 **byte** setup

Definition at line 2564 of file internal.h.

18.17.2.5 **byte** state

Definition at line 2563 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.18 CipherSpecs Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- word16 [key_size](#)
- word16 [iv_size](#)
- word16 [block_size](#)
- word16 [aead_mac_size](#)
- byte [bulk_cipher_algorithm](#)
- byte [cipher_type](#)
- byte [mac_algorithm](#)
- byte [kea](#)
- byte [sig_algo](#)
- byte [hash_size](#)
- byte [pad_size](#)
- byte [static_ecdh](#)

18.18.1 Detailed Description

Definition at line 2446 of file internal.h.

18.18.2 Field Documentation

18.18.2.1 **word16** aead_mac_size

Definition at line 2450 of file internal.h.

18.18.2.2 word16 block_size

Definition at line 2449 of file internal.h.

18.18.2.3 byte bulk_cipher_algorithm

Definition at line 2451 of file internal.h.

18.18.2.4 byte cipher_type

Definition at line 2452 of file internal.h.

18.18.2.5 byte hash_size

Definition at line 2456 of file internal.h.

18.18.2.6 word16 iv_size

Definition at line 2448 of file internal.h.

18.18.2.7 byte kea

Definition at line 2454 of file internal.h.

18.18.2.8 word16 key_size

Definition at line 2447 of file internal.h.

18.18.2.9 byte mac_algorithm

Definition at line 2453 of file internal.h.

18.18.2.10 byte pad_size

Definition at line 2457 of file internal.h.

18.18.2.11 byte sig_algo

Definition at line 2455 of file internal.h.

18.18.2.12 byte static_ecdh

Definition at line 2458 of file internal.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/internal.h`

18.19 ClientRow Struct Reference

Data Fields

- int [nextIdx](#)
- int [totalCount](#)
- [ClientSession](#) [Clients](#) [SESSIONS_PER_ROW]

18.19.1 Detailed Description

Definition at line 4160 of file ssl.c.

18.19.2 Field Documentation

18.19.2.1 ClientSession Clients[SESSIONS_PER_ROW]

Definition at line 4163 of file ssl.c.

18.19.2.2 int nextIdx

Definition at line 4161 of file ssl.c.

18.19.2.3 int totalCount

Definition at line 4162 of file ssl.c.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/src/ssl.c

18.20 ClientSession Struct Reference

Data Fields

- word16 [serverRow](#)
- word16 [serverIdx](#)

18.20.1 Detailed Description

Definition at line 4155 of file ssl.c.

18.20.2 Field Documentation

18.20.2.1 word16 serverIdx

Definition at line 4157 of file ssl.c.

18.20.2.2 word16 serverRow

Definition at line 4156 of file ssl.c.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/src/ssl.c

18.21 CRL_Entry Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [CRL_Entry](#) * [next](#)
- byte [issuerHash](#) [CRL_DIGEST_SIZE]
- byte [lastDate](#) [MAX_DATE_SIZE]
- byte [nextDate](#) [MAX_DATE_SIZE]
- byte [lastDateFormat](#)
- byte [nextDateFormat](#)
- RevokedCert * [certs](#)

- int [totalCerts](#)
- int [verified](#)
- byte * [toBeSigned](#)
- word32 [tbsSz](#)
- byte * [signature](#)
- word32 [signatureSz](#)
- word32 [signatureOID](#)

18.21.1 Detailed Description

Definition at line 1618 of file internal.h.

18.21.2 Field Documentation

18.21.2.1 RevokedCert* certs

Definition at line 1627 of file internal.h.

18.21.2.2 byte issuerHash[CRL_DIGEST_SIZE]

Definition at line 1620 of file internal.h.

18.21.2.3 byte lastDate[MAX_DATE_SIZE]

Definition at line 1623 of file internal.h.

18.21.2.4 byte lastDateFormat

Definition at line 1625 of file internal.h.

18.21.2.5 CRL_Entry* next

Definition at line 1619 of file internal.h.

18.21.2.6 byte nextDate[MAX_DATE_SIZE]

Definition at line 1624 of file internal.h.

18.21.2.7 byte nextDateFormat

Definition at line 1626 of file internal.h.

18.21.2.8 byte* signature

Definition at line 1632 of file internal.h.

18.21.2.9 word32 signatureOID

Definition at line 1634 of file internal.h.

18.21.2.10 word32 signatureSz

Definition at line 1633 of file internal.h.

18.21.2.11 word32 tbsSz

Definition at line 1631 of file internal.h.

18.21.2.12 byte* toBeSigned

Definition at line 1630 of file internal.h.

18.21.2.13 int totalCerts

Definition at line 1628 of file internal.h.

18.21.2.14 int verified

Definition at line 1629 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.22 CRL_Monitor Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- char * [path](#)
- int [type](#)

18.22.1 Detailed Description

Definition at line 1645 of file internal.h.

18.22.2 Field Documentation

18.22.2.1 char* path

Definition at line 1646 of file internal.h.

18.22.2.2 int type

Definition at line 1647 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.23 DckeArgs Struct Reference

Data Fields

- byte * [output](#)
- word32 [length](#)
- word32 [idx](#)
- word32 [begin](#)
- word32 [sigSz](#)
- int [lastErr](#)

18.23.1 Detailed Description

Definition at line 23492 of file internal.c.

18.23.2 Field Documentation

18.23.2.1 word32 begin

Definition at line 23496 of file internal.c.

18.23.2.2 word32 idx

Definition at line 23495 of file internal.c.

18.23.2.3 int lastErr

Definition at line 23499 of file internal.c.

18.23.2.4 word32 length

Definition at line 23494 of file internal.c.

18.23.2.5 byte* output

Definition at line 23493 of file internal.c.

18.23.2.6 word32 sigSz

Definition at line 23497 of file internal.c.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/src/internal.c

18.24 DcvArgs Struct Reference

Data Fields

- byte * [output](#)
- word32 [sendSz](#)
- word16 [sz](#)
- word32 [sigSz](#)
- word32 [idx](#)
- word32 [begin](#)
- byte [hashAlgo](#)
- byte [sigAlgo](#)

18.24.1 Detailed Description

Definition at line 22805 of file internal.c.

18.24.2 Field Documentation

18.24.2.1 word32 begin

Definition at line 22811 of file internal.c.

18.24.2.2 byte hashAlgo

Definition at line 22812 of file internal.c.

18.24.2.3 word32 idx

Definition at line 22810 of file internal.c.

18.24.2.4 byte* output

Definition at line 22806 of file internal.c.

18.24.2.5 word32 sendSz

Definition at line 22807 of file internal.c.

18.24.2.6 byte sigAlgo

Definition at line 22813 of file internal.c.

18.24.2.7 word32 sigSz

Definition at line 22809 of file internal.c.

18.24.2.8 word16 sz

Definition at line 22808 of file internal.c.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/src/internal.c

18.25 DecodedCert Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h>
```

Data Fields

- byte * [publicKey](#)
- word32 [pubKeySize](#)
- int [pubKeyStored](#)
- word32 [certBegin](#)
- word32 [sigIndex](#)
- word32 [sigLength](#)
- word32 [signatureOID](#)
- word32 [keyOID](#)
- int [version](#)
- [DNS_entry](#) * [altNames](#)
- [DNS_entry](#) * [altEmailNames](#)
- [Base_entry](#) * [permittedNames](#)
- [Base_entry](#) * [excludedNames](#)
- byte [subjectHash](#) [KEYID_SIZE]
- byte [issuerHash](#) [KEYID_SIZE]
- byte * [signature](#)
- char * [subjectCN](#)
- int [subjectCNLen](#)
- char [subjectCNEnc](#)

- int [subjectCNStored](#)
- char [issuer](#) [ASN_NAME_MAX]
- char [subject](#) [ASN_NAME_MAX]
- int [verify](#)
- byte * [source](#)
- word32 [srcIdx](#)
- word32 [maxIdx](#)
- void * [heap](#)
- byte [serial](#) [EXTERNAL_SERIAL_SIZE]
- int [serialSz](#)
- byte * [extensions](#)
- int [extensionsSz](#)
- word32 [extensionsIdx](#)
- byte * [extAuthInfo](#)
- int [extAuthInfoSz](#)
- byte * [extCrlInfo](#)
- int [extCrlInfoSz](#)
- byte [extSubjKeyId](#) [KEYID_SIZE]
- byte [extSubjKeyIdSet](#)
- byte [extAuthKeyId](#) [KEYID_SIZE]
- byte [extAuthKeyIdSet](#)
- byte [extNameConstraintSet](#)
- byte [isCA](#)
- byte [pathLengthSet](#)
- byte [pathLength](#)
- byte [weOwnAltNames](#)
- byte [extKeyUsageSet](#)
- word16 [extKeyUsage](#)
- byte [extExtKeyUsageSet](#)
- byte [extExtKeyUsage](#)
- byte * [beforeDate](#)
- int [beforeDateLen](#)
- byte * [afterDate](#)
- int [afterDateLen](#)
- byte * [subjectRaw](#)
- int [subjectRawLen](#)
- [Signer](#) * [ca](#)
- [SignatureCtx](#) [sigCtx](#)

18.25.1 Detailed Description

Definition at line 488 of file `asn.h`.

18.25.2 Field Documentation

18.25.2.1 byte* afterDate

Definition at line 574 of file `asn.h`.

18.25.2.2 int afterDateLen

Definition at line 575 of file `asn.h`.

18.25.2.3 DNS_entry* altEmailNames

Definition at line 500 of file asn.h.

18.25.2.4 DNS_entry* altNames

Definition at line 498 of file asn.h.

18.25.2.5 byte* beforeDate

Definition at line 572 of file asn.h.

18.25.2.6 int beforeDateLen

Definition at line 573 of file asn.h.

18.25.2.7 Signer* ca

Definition at line 628 of file asn.h.

18.25.2.8 word32 certBegin

Definition at line 492 of file asn.h.

18.25.2.9 Base_entry* excludedNames

Definition at line 502 of file asn.h.

18.25.2.10 byte* extAuthInfo

Definition at line 526 of file asn.h.

18.25.2.11 int extAuthInfoSz

Definition at line 527 of file asn.h.

18.25.2.12 byte extAuthKeyId[KEYID_SIZE]

Definition at line 532 of file asn.h.

18.25.2.13 byte extAuthKeyIdSet

Definition at line 533 of file asn.h.

18.25.2.14 byte* extCrlInfo

Definition at line 528 of file asn.h.

18.25.2.15 int extCrlInfoSz

Definition at line 529 of file asn.h.

18.25.2.16 byte* extensions

Definition at line 523 of file asn.h.

18.25.2.17 word32 extensionsIdx

Definition at line 525 of file asn.h.

18.25.2.18 int extensionsSz

Definition at line 524 of file asn.h.

18.25.2.19 byte extExtKeyUsage

Definition at line 544 of file asn.h.

18.25.2.20 byte extExtKeyUsageSet

Definition at line 543 of file asn.h.

18.25.2.21 word16 extKeyUsage

Definition at line 542 of file asn.h.

18.25.2.22 byte extKeyUsageSet

Definition at line 541 of file asn.h.

18.25.2.23 byte extNameConstraintSet

Definition at line 535 of file asn.h.

18.25.2.24 byte extSubjKeyId[KEYID_SIZE]

Definition at line 530 of file asn.h.

18.25.2.25 byte extSubjKeyIdSet

Definition at line 531 of file asn.h.

18.25.2.26 void* heap

Definition at line 520 of file asn.h.

18.25.2.27 byte isCA

Definition at line 537 of file asn.h.

18.25.2.28 char issuer[ASN_NAME_MAX]

Definition at line 514 of file asn.h.

18.25.2.29 byte issuerHash[KEYID_SIZE]

Definition at line 505 of file asn.h.

18.25.2.30 word32 keyOID

Definition at line 496 of file asn.h.

18.25.2.31 word32 maxIdx

Definition at line 519 of file asn.h.

18.25.2.32 byte pathLength

Definition at line 539 of file asn.h.

18.25.2.33 byte pathLengthSet

Definition at line 538 of file asn.h.

18.25.2.34 Base_entry* permittedNames

Definition at line 501 of file asn.h.

18.25.2.35 word32 pubKeySize

Definition at line 490 of file asn.h.

18.25.2.36 int pubKeyStored

Definition at line 491 of file asn.h.

18.25.2.37 byte* publicKey

Definition at line 489 of file asn.h.

18.25.2.38 byte serial[EXTERNAL_SERIAL_SIZE]

Definition at line 521 of file asn.h.

18.25.2.39 int serialSz

Definition at line 522 of file asn.h.

18.25.2.40 SignatureCtx sigCtx

Definition at line 629 of file asn.h.

18.25.2.41 word32 sigIndex

Definition at line 493 of file asn.h.

18.25.2.42 word32 sigLength

Definition at line 494 of file asn.h.

18.25.2.43 byte* signature

Definition at line 509 of file asn.h.

18.25.2.44 word32 signatureOID

Definition at line 495 of file asn.h.

18.25.2.45 byte* source

Definition at line 517 of file asn.h.

18.25.2.46 word32 srcldx

Definition at line 518 of file asn.h.

18.25.2.47 char subject[ASN_NAME_MAX]

Definition at line 515 of file asn.h.

18.25.2.48 char* subjectCN

Definition at line 510 of file asn.h.

18.25.2.49 char subjectCNEnc

Definition at line 512 of file asn.h.

18.25.2.50 int subjectCNLen

Definition at line 511 of file asn.h.

18.25.2.51 int subjectCNStored

Definition at line 513 of file asn.h.

18.25.2.52 byte subjectHash[KEYID_SIZE]

Definition at line 504 of file asn.h.

18.25.2.53 byte* subjectRaw

Definition at line 581 of file asn.h.

18.25.2.54 int subjectRawLen

Definition at line 582 of file asn.h.

18.25.2.55 int verify

Definition at line 516 of file asn.h.

18.25.2.56 int version

Definition at line 497 of file asn.h.

18.25.2.57 byte weOwnAltNames

Definition at line 540 of file asn.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h

18.26 DecodedName Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h>
```

Data Fields

- char * [fullName](#)
- int [fullNameLen](#)
- int [entryCount](#)
- int [cnIdx](#)
- int [cnLen](#)
- int [snIdx](#)
- int [snLen](#)
- int [cldx](#)
- int [cLen](#)

- int [lIdx](#)
- int [lLen](#)
- int [stIdx](#)
- int [stLen](#)
- int [oldx](#)
- int [oLen](#)
- int [ouldx](#)
- int [ouLen](#)
- int [emailIdx](#)
- int [emailLen](#)
- int [uidIdx](#)
- int [uidLen](#)
- int [serialIdx](#)
- int [serialLen](#)

18.26.1 Detailed Description

Definition at line 393 of file `asn.h`.

18.26.2 Field Documentation

18.26.2.1 int `cIdx`

Definition at line 401 of file `asn.h`.

18.26.2.2 int `cLen`

Definition at line 402 of file `asn.h`.

18.26.2.3 int `cnIdx`

Definition at line 397 of file `asn.h`.

18.26.2.4 int `cnLen`

Definition at line 398 of file `asn.h`.

18.26.2.5 int `emailIdx`

Definition at line 411 of file `asn.h`.

18.26.2.6 int `emailLen`

Definition at line 412 of file `asn.h`.

18.26.2.7 int `entryCount`

Definition at line 396 of file `asn.h`.

18.26.2.8 char* `fullName`

Definition at line 394 of file `asn.h`.

18.26.2.9 int `fullNameLen`

Definition at line 395 of file `asn.h`.

18.26.2.10 int lldx

Definition at line 403 of file asn.h.

18.26.2.11 int lLen

Definition at line 404 of file asn.h.

18.26.2.12 int oldx

Definition at line 407 of file asn.h.

18.26.2.13 int oLen

Definition at line 408 of file asn.h.

18.26.2.14 int ouldx

Definition at line 409 of file asn.h.

18.26.2.15 int ouLen

Definition at line 410 of file asn.h.

18.26.2.16 int serialldx

Definition at line 415 of file asn.h.

18.26.2.17 int serialLen

Definition at line 416 of file asn.h.

18.26.2.18 int snldx

Definition at line 399 of file asn.h.

18.26.2.19 int snLen

Definition at line 400 of file asn.h.

18.26.2.20 int stldx

Definition at line 405 of file asn.h.

18.26.2.21 int stLen

Definition at line 406 of file asn.h.

18.26.2.22 int uidldx

Definition at line 413 of file asn.h.

18.26.2.23 int uidLen

Definition at line 414 of file asn.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h`

18.27 DerBuffer Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- byte * [buffer](#)
- void * [heap](#)
- word32 [length](#)
- int [type](#)
- int [dynType](#)

18.27.1 Detailed Description

Definition at line 1441 of file internal.h.

18.27.2 Field Documentation

18.27.2.1 byte* [buffer](#)

Definition at line 1442 of file internal.h.

18.27.2.2 int [dynType](#)

Definition at line 1446 of file internal.h.

18.27.2.3 void* [heap](#)

Definition at line 1443 of file internal.h.

18.27.2.4 word32 [length](#)

Definition at line 1444 of file internal.h.

18.27.2.5 int [type](#)

Definition at line 1445 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.28 Des Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/des3.h>
```

Data Fields

- word32 [reg](#) [DES_BLOCK_SIZE/sizeof(word32)]
- word32 [tmp](#) [DES_BLOCK_SIZE/sizeof(word32)]
- word32 [key](#) [DES_KS_SIZE]

18.28.1 Detailed Description

Definition at line 70 of file des3.h.

18.28.2 Field Documentation

18.28.2.1 word32 key[DES_KS_SIZE]

Definition at line 73 of file des3.h.

18.28.2.2 word32 reg[DES_BLOCK_SIZE/sizeof(word32)]

Definition at line 71 of file des3.h.

18.28.2.3 word32 tmp[DES_BLOCK_SIZE/sizeof(word32)]

Definition at line 72 of file des3.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/des3.h

18.29 Des3 Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/des3.h>
```

Data Fields

- word32 [key](#) [3][DES_KS_SIZE]
- word32 [reg](#) [DES_BLOCK_SIZE/sizeof(word32)]
- word32 [tmp](#) [DES_BLOCK_SIZE/sizeof(word32)]
- void * [heap](#)

18.29.1 Detailed Description

Definition at line 78 of file des3.h.

18.29.2 Field Documentation

18.29.2.1 void* heap

Definition at line 87 of file des3.h.

18.29.2.2 word32 key[3][DES_KS_SIZE]

Definition at line 79 of file des3.h.

18.29.2.3 word32 reg[DES_BLOCK_SIZE/sizeof(word32)]

Definition at line 80 of file des3.h.

18.29.2.4 word32 tmp[DES_BLOCK_SIZE/sizeof(word32)]

Definition at line 81 of file des3.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/des3.h

18.30 DhKey Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/dh.h>
```

Data Fields

- [mp_int p](#)
- [mp_int g](#)
- void * [heap](#)

18.30.1 Detailed Description

Definition at line 48 of file dh.h.

18.30.2 Field Documentation

18.30.2.1 [mp_int g](#)

Definition at line 49 of file dh.h.

18.30.2.2 [void* heap](#)

Definition at line 50 of file dh.h.

18.30.2.3 [mp_int p](#)

Definition at line 49 of file dh.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/dh.h

18.31 DhParams Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/dh.h>
```

Data Fields

- const byte * [p](#)
- word32 [p_len](#)
- const byte * [g](#)
- word32 [g_len](#)

18.31.1 Detailed Description

Definition at line 40 of file dh.h.

18.31.2 Field Documentation

18.31.2.1 [const byte* g](#)

Definition at line 43 of file dh.h.

18.31.2.2 word32 g_len

Definition at line 44 of file dh.h.

18.31.2.3 const byte* p

Definition at line 41 of file dh.h.

18.31.2.4 word32 p_len

Definition at line 42 of file dh.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/dh.h

18.32 DNS_entry Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h>
```

Data Fields

- [DNS_entry * next](#)
- [char * name](#)

18.32.1 Detailed Description

Definition at line 377 of file asn.h.

18.32.2 Field Documentation

18.32.2.1 char* name

Definition at line 379 of file asn.h.

18.32.2.2 DNS_entry* next

Definition at line 378 of file asn.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h

18.33 drv_config_t Struct Reference

Data Fields

- [sbc_wtdog_ctr_t watchdogCtr](#)
- [uint32_t lpspiIntace](#)
- [bool isInit](#)

18.33.1 Detailed Description

Definition at line 58 of file sbc_uja116x_driver.c.

18.33.2 Field Documentation

18.33.2.1 bool isInit

Definition at line 61 of file sbc_uja116x_driver.c.

18.33.2.2 uint32_t lpspiIntace

Definition at line 60 of file sbc_uja116x_driver.c.

18.33.2.3 sbc_wtdog_ctr_t watchdogCtr

Definition at line 59 of file sbc_uja116x_driver.c.

The documentation for this struct was generated from the following file:

- middleware/sbc/sbc_uja116x/source/sbc_uja116x_driver.c

18.34 DsaKey Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/dsa.h>
```

Data Fields

- [mp_int p](#)
- [mp_int q](#)
- [mp_int g](#)
- [mp_int y](#)
- [mp_int x](#)
- [int type](#)
- [void * heap](#)

18.34.1 Detailed Description

Definition at line 53 of file dsa.h.

18.34.2 Field Documentation

18.34.2.1 mp_int g

Definition at line 54 of file dsa.h.

18.34.2.2 void* heap

Definition at line 56 of file dsa.h.

18.34.2.3 mp_int p

Definition at line 54 of file dsa.h.

18.34.2.4 mp_int q

Definition at line 54 of file dsa.h.

18.34.2.5 int type

Definition at line 55 of file dsa.h.

18.34.2.6 mp_int x

Definition at line 54 of file dsa.h.

18.34.2.7 mp_int y

Definition at line 54 of file dsa.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/dsa.h

18.35 DskeArgs Struct Reference

Data Fields

- byte * [output](#)
- byte * [verifySig](#)
- word32 [idx](#)
- word32 [begin](#)
- word16 [verifySigSz](#)
- word16 [sigSz](#)
- byte [sigAlgo](#)
- byte [hashAlgo](#)

18.35.1 Detailed Description

Definition at line 17146 of file internal.c.

18.35.2 Field Documentation

18.35.2.1 word32 begin

Definition at line 17152 of file internal.c.

18.35.2.2 byte hashAlgo

Definition at line 17158 of file internal.c.

18.35.2.3 word32 idx

Definition at line 17151 of file internal.c.

18.35.2.4 byte* output

Definition at line 17147 of file internal.c.

18.35.2.5 byte sigAlgo

Definition at line 17157 of file internal.c.

18.35.2.6 word16 sigSz

Definition at line 17156 of file internal.c.

18.35.2.7 byte* verifySig

Definition at line 17149 of file internal.c.

18.35.2.8 word16 verifySigSz

Definition at line 17154 of file internal.c.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/src/internal.c

18.36 DtlsFrag Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- word32 [begin](#)
- word32 [end](#)
- struct [DtlsFrag](#) * [next](#)

18.36.1 Detailed Description

Definition at line 3108 of file internal.h.

18.36.2 Field Documentation

18.36.2.1 word32 begin

Definition at line 3109 of file internal.h.

18.36.2.2 word32 end

Definition at line 3110 of file internal.h.

18.36.2.3 struct DtlsFrag* next

Definition at line 3111 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.37 DtlsHandShakeHeader Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- byte [type](#)
- word24 [length](#)
- byte [message_seq](#) [2]
- word24 [fragment_offset](#)
- word24 [fragment_length](#)

18.37.1 Detailed Description

Definition at line 3562 of file internal.h.

18.37.2 Field Documentation

18.37.2.1 word24 fragment_length

Definition at line 3567 of file internal.h.

18.37.2.2 word24 fragment_offset

Definition at line 3566 of file internal.h.

18.37.2.3 word24 length

Definition at line 3564 of file internal.h.

18.37.2.4 byte message_seq[2]

Definition at line 3565 of file internal.h.

18.37.2.5 byte type

Definition at line 3563 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.38 DtlsMsg Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- struct [DtlsMsg](#) * [next](#)
- byte * [buf](#)
- byte * [msg](#)
- [DtlsFrag](#) * [fragList](#)
- word32 [fragSz](#)
- word32 [seq](#)
- word32 [sz](#)
- byte [type](#)

18.38.1 Detailed Description

Definition at line 3115 of file internal.h.

18.38.2 Field Documentation

18.38.2.1 byte* buf

Definition at line 3117 of file internal.h.

18.38.2.2 DtlsFrag* fragList

Definition at line 3119 of file internal.h.

18.38.2.3 word32 fragSz

Definition at line 3120 of file internal.h.

18.38.2.4 `byte* msg`

Definition at line 3118 of file `internal.h`.

18.38.2.5 `struct DtIsMsg* next`

Definition at line 3116 of file `internal.h`.

18.38.2.6 `word32 seq`

Definition at line 3121 of file `internal.h`.

18.38.2.7 `word32 sz`

Definition at line 3122 of file `internal.h`.

18.38.2.8 `byte type`

Definition at line 3123 of file `internal.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/internal.h`

18.39 `DtIsRecordLayerHeader` Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- `byte type`
- `byte pvMajor`
- `byte pvMinor`
- `byte sequence_number` [8]
- `byte length` [2]

18.39.1 Detailed Description

Definition at line 3099 of file `internal.h`.

18.39.2 Field Documentation

18.39.2.1 `byte length`[2]

Definition at line 3104 of file `internal.h`.

18.39.2.2 `byte pvMajor`

Definition at line 3101 of file `internal.h`.

18.39.2.3 `byte pvMinor`

Definition at line 3102 of file `internal.h`.

18.39.2.4 `byte sequence_number`[8]

Definition at line 3103 of file `internal.h`.

18.39.2.5 byte type

Definition at line 3100 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.40 EncryptedInfo Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- char [name](#) [NAME_SZ]
- byte [iv](#) [IV_SZ]
- word32 [ivSz](#)
- long [consumed](#)
- byte [set](#)
- [WOLFSSL_CTX](#) * [ctx](#)

18.40.1 Detailed Description

Definition at line 3490 of file internal.h.

18.40.2 Field Documentation

18.40.2.1 long consumed

Definition at line 3494 of file internal.h.

18.40.2.2 WOLFSSL_CTX* ctx

Definition at line 3496 of file internal.h.

18.40.2.3 byte iv[IV_SZ]

Definition at line 3492 of file internal.h.

18.40.2.4 word32 ivSz

Definition at line 3493 of file internal.h.

18.40.2.5 char name[NAME_SZ]

Definition at line 3491 of file internal.h.

18.40.2.6 byte set

Definition at line 3495 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.41 fp_int Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/tfm.h>
```

Data Fields

- int [used](#)
- int [sign](#)
- fp_digit [dp](#) [FP_SIZE]

18.41.1 Detailed Description

Definition at line 299 of file tfm.h.

18.41.2 Field Documentation

18.41.2.1 fp_digit dp[FP_SIZE]

Definition at line 305 of file tfm.h.

18.41.2.2 int sign

Definition at line 301 of file tfm.h.

18.41.2.3 int used

Definition at line 300 of file tfm.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/tfm.h

18.42 fs45_tx_data_t Struct Reference

Structure representing transmit data frame.

Data Fields

- bool [isSecured](#)
true if the SPI command is secured.
- uint8_t [registerAddress](#)
Register address.
- fs45_command_t [commandType](#)
Command type (R/W).
- uint8_t [writeData](#)
Data to be written to the register. If commandType is "read", this value will be ignored.

18.42.1 Detailed Description

Structure representing transmit data frame.

Definition at line 105 of file sbc_fs45_driver.c.

18.42.2 Field Documentation

18.42.2.1 fs45_command_t commandType

Command type (R/W).

Definition at line 112 of file sbc_fs45_driver.c.

18.42.2.2 bool isSecured

true if the SPI command is secured.

Definition at line 108 of file sbc_fs45_driver.c.

18.42.2.3 uint8_t registerAddress

Register address.

Definition at line 110 of file sbc_fs45_driver.c.

18.42.2.4 uint8_t writeData

Data to be written to the register. If commandType is "read", this value will be ignored.

Definition at line 116 of file sbc_fs45_driver.c.

The documentation for this struct was generated from the following file:

- middleware/sbc/sbc_fs45/source/sbc_fs45_driver.c

18.43 func_args Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/test.h>
```

Data Fields

- int [argc](#)
- char ** [argv](#)
- int [return_code](#)
- [tcp_ready](#) * [signal](#)
- [callback_functions](#) * [callbacks](#)

18.43.1 Detailed Description

Definition at line 340 of file test.h.

18.43.2 Field Documentation

18.43.2.1 int argc

Definition at line 341 of file test.h.

18.43.2.2 char** argv

Definition at line 342 of file test.h.

18.43.2.3 callback_functions* callbacks

Definition at line 345 of file test.h.

18.43.2.4 int return_code

Definition at line 343 of file test.h.

18.43.2.5 tcp_ready* signal

Definition at line 344 of file test.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/test.h

18.44 HandShakeHeader Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- byte [type](#)
- word24 [length](#)

18.44.1 Detailed Description

Definition at line 3555 of file internal.h.

18.44.2 Field Documentation

18.44.2.1 word24 length

Definition at line 3557 of file internal.h.

18.44.2.2 byte type

Definition at line 3556 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.45 handShakeInfo_st Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/callbacks.h>
```

Data Fields

- struct [WOLFSSL](#) * [ssl](#)
- char [cipherName](#) [MAX_CIPHERNAME_SZ+1]
- char [packetNames](#) [MAX_PACKETS_HANDSHAKE][MAX_PACKETNAME_SZ+1]
- int [numberPackets](#)
- int [negotiationError](#)

18.45.1 Detailed Description

Definition at line 45 of file callbacks.h.

18.45.2 Field Documentation

18.45.2.1 char cipherName[MAX_CIPHERNAME_SZ+1]

Definition at line 47 of file callbacks.h.

18.45.2.2 int negotiationError

Definition at line 51 of file callbacks.h.

18.45.2.3 int numberPackets

Definition at line 50 of file callbacks.h.

18.45.2.4 char packetNames[MAX_PACKETS_HANDSHAKE][MAX_PACKETNAME_SZ+1]

Definition at line 48 of file callbacks.h.

18.45.2.5 struct WOLFSSL* ssl

Definition at line 46 of file callbacks.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/callbacks.h

18.46 Hash Union Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/hmac.h>
```

Data Fields

- [Md5 md5](#)
- [Sha sha](#)
- [Sha256 sha256](#)

18.46.1 Detailed Description

Definition at line 124 of file hmac.h.

18.46.2 Field Documentation

18.46.2.1 Md5 md5

Definition at line 126 of file hmac.h.

18.46.2.2 Sha sha

Definition at line 129 of file hmac.h.

18.46.2.3 Sha256 sha256

Definition at line 135 of file hmac.h.

The documentation for this union was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/hmac.h

18.47 Hashes Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- byte [md5](#) [MD5_DIGEST_SIZE]
- byte [sha](#) [SHA_DIGEST_SIZE]
- byte [sha256](#) [SHA256_DIGEST_SIZE]

18.47.1 Detailed Description

Definition at line 2585 of file internal.h.

18.47.2 Field Documentation

18.47.2.1 byte md5[MD5_DIGEST_SIZE]

Definition at line 2587 of file internal.h.

18.47.2.2 byte sha[SHA_DIGEST_SIZE]

Definition at line 2590 of file internal.h.

18.47.2.3 byte sha256[SHA256_DIGEST_SIZE]

Definition at line 2593 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.48 HC128 Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/hc128.h>
```

Data Fields

- word32 [T](#) [1024]
- word32 [X](#) [16]
- word32 [Y](#) [16]
- word32 [counter1024](#)
- word32 [key](#) [8]
- word32 [iv](#) [8]

18.48.1 Detailed Description

Definition at line 39 of file hc128.h.

18.48.2 Field Documentation

18.48.2.1 word32 counter1024

Definition at line 43 of file hc128.h.

18.48.2.2 word32 iv[8]

Definition at line 45 of file hc128.h.

18.48.2.3 word32 key[8]

Definition at line 44 of file hc128.h.

18.48.2.4 word32 T[1024]

Definition at line 40 of file hc128.h.

18.48.2.5 word32 X[16]

Definition at line 41 of file hc128.h.

18.48.2.6 word32 Y[16]

Definition at line 42 of file hc128.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/hc128.h`

18.49 Hmac Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/hmac.h>
```

Data Fields

- [Hash hash](#)
- word32 [ipad](#) [HMAC_BLOCK_SIZE/sizeof(word32)]
- word32 [opad](#) [HMAC_BLOCK_SIZE/sizeof(word32)]
- word32 [innerHash](#) [MAX_DIGEST_SIZE/sizeof(word32)]
- void * [heap](#)
- byte [macType](#)
- byte [innerHashKeyed](#)

18.49.1 Detailed Description

Definition at line 149 of file hmac.h.

18.49.2 Field Documentation

18.49.2.1 Hash hash

Definition at line 150 of file hmac.h.

18.49.2.2 void* heap

Definition at line 154 of file hmac.h.

18.49.2.3 word32 innerHash[MAX_DIGEST_SIZE/sizeof(word32)]

Definition at line 153 of file hmac.h.

18.49.2.4 byte innerHashKeyed

Definition at line 156 of file hmac.h.

18.49.2.5 word32 ipad[HMAC_BLOCK_SIZE /sizeof(word32)]

Definition at line 151 of file hmac.h.

18.49.2.6 byte macType

Definition at line 155 of file hmac.h.

18.49.2.7 word32 opad[HMAC_BLOCK_SIZE /sizeof(word32)]

Definition at line 152 of file hmac.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/hmac.h`

18.50 HS_Hashes Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [Hashes verifyHashes](#)
- [Hashes certHashes](#)
- [Sha hashSha](#)
- [Md5 hashMd5](#)
- [Sha256 hashSha256](#)

18.50.1 Detailed Description

Definition at line 3164 of file internal.h.

18.50.2 Field Documentation

18.50.2.1 Hashes certHashes

Definition at line 3166 of file internal.h.

18.50.2.2 Md5 hashMd5

Definition at line 3171 of file internal.h.

18.50.2.3 Sha hashSha

Definition at line 3168 of file internal.h.

18.50.2.4 Sha256 hashSha256

Definition at line 3174 of file internal.h.

18.50.2.5 Hashes verifyHashes

Definition at line 3165 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.51 i2c_instance_t Struct Reference

Structure storing PAL instance information.

```
#include <platform/pal/inc/i2c_pal_mapping.h>
```

Data Fields

- i2c_inst_type_t [instType](#)
- uint32_t [instIdx](#)

18.51.1 Detailed Description

Structure storing PAL instance information.

This structure is used for storing PAL instance information. Implements : i2c_instance_t_Class

Definition at line 81 of file i2c_pal_mapping.h.

18.51.2 Field Documentation

18.51.2.1 uint32_t instIdx

Instance index of the peripheral over which the PAL is used

Definition at line 83 of file i2c_pal_mapping.h.

18.51.2.2 i2c_inst_type_t instType

Peripheral over which the PAL is used

Definition at line 82 of file i2c_pal_mapping.h.

The documentation for this struct was generated from the following file:

- platform/pal/inc/i2c_pal_mapping.h

18.52 i2s_instance_t Struct Reference

Structure storing PAL instance information.

```
#include <platform/pal/inc/i2s_pal_mapping.h>
```

Data Fields

- i2s_inst_type_t [instType](#)
- uint32_t [instIdx](#)

18.52.1 Detailed Description

Structure storing PAL instance information.

This structure is used for storing PAL instance information.

Definition at line 60 of file i2s_pal_mapping.h.

18.52.2 Field Documentation

18.52.2.1 uint32_t instIdx

Instance index of the peripheral over which the PAL is used

Definition at line 62 of file i2s_pal_mapping.h.

18.52.2.2 i2s_inst_type_t instType

Peripheral over which the PAL is used

Definition at line 61 of file i2s_pal_mapping.h.

The documentation for this struct was generated from the following file:

- platform/pal/inc/i2s_pal_mapping.h

18.53 ic_instance_t Struct Reference

Structure storing PAL instance information.

```
#include <platform/pal/inc/ic_pal_mapping.h>
```

Data Fields

- ic_inst_type_t [instType](#)
- uint32_t [instIdx](#)

18.53.1 Detailed Description

Structure storing PAL instance information.

This structure is used for storing PAL instance information. Implements : ic_instance_t_Class

Definition at line 132 of file ic_pal_mapping.h.

18.53.2 Field Documentation

18.53.2.1 uint32_t instIdx

Instance index of the peripheral over which the PAL is used

Definition at line 134 of file ic_pal_mapping.h.

18.53.2.2 ic_inst_type_t instType

Peripheral over which the PAL is used

Definition at line 133 of file ic_pal_mapping.h.

The documentation for this struct was generated from the following file:

- platform/pal/inc/ic_pal_mapping.h

18.54 Keys Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- byte [client_write_MAC_secret](#) [MAX_DIGEST_SIZE]
- byte [server_write_MAC_secret](#) [MAX_DIGEST_SIZE]
- byte [client_write_key](#) [AES_256_KEY_SIZE]
- byte [server_write_key](#) [AES_256_KEY_SIZE]
- byte [client_write_IV](#) [MAX_WRITE_IV_SZ]
- byte [server_write_IV](#) [MAX_WRITE_IV_SZ]
- word32 [peer_sequence_number_hi](#)
- word32 [peer_sequence_number_lo](#)
- word32 [sequence_number_hi](#)
- word32 [sequence_number_lo](#)
- word32 [encryptSz](#)
- word32 [padSz](#)
- byte [encryptionOn](#)
- byte [decryptedCur](#)

18.54.1 Detailed Description

Definition at line 1768 of file internal.h.

18.54.2 Field Documentation

18.54.2.1 byte [client_write_IV](#)[MAX_WRITE_IV_SZ]

Definition at line 1773 of file internal.h.

18.54.2.2 byte [client_write_key](#)[AES_256_KEY_SIZE]

Definition at line 1771 of file internal.h.

18.54.2.3 byte [client_write_MAC_secret](#)[MAX_DIGEST_SIZE]

Definition at line 1769 of file internal.h.

18.54.2.4 byte [decryptedCur](#)

Definition at line 1809 of file internal.h.

18.54.2.5 byte [encryptionOn](#)

Definition at line 1808 of file internal.h.

18.54.2.6 word32 [encryptSz](#)

Definition at line 1806 of file internal.h.

18.54.2.7 word32 [padSz](#)

Definition at line 1807 of file internal.h.

18.54.2.8 word32 [peer_sequence_number_hi](#)

Definition at line 1781 of file internal.h.

18.54.2.9 word32 [peer_sequence_number_lo](#)

Definition at line 1782 of file internal.h.

18.54.2.10 word32 sequence_number_hi

Definition at line 1783 of file internal.h.

18.54.2.11 word32 sequence_number_lo

Definition at line 1784 of file internal.h.

18.54.2.12 byte server_write_IV[MAX_WRITE_IV_SZ]

Definition at line 1774 of file internal.h.

18.54.2.13 byte server_write_key[AES_256_KEY_SIZE]

Definition at line 1772 of file internal.h.

18.54.2.14 byte server_write_MAC_secret[MAX_DIGEST_SIZE]

Definition at line 1770 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.55 lin_product_id_t Struct Reference

Product id structure Implements : lin_product_id_t_Class.

```
#include <middleware/lin/include/lin_types.h>
```

Data Fields

- I_u16 [supplier_id](#)
- I_u16 [function_id](#)
- I_u8 [variant](#)

18.55.1 Detailed Description

Product id structure Implements : lin_product_id_t_Class.

Definition at line 54 of file lin_types.h.

18.55.2 Field Documentation**18.55.2.1 I_u16 function_id**

Function ID

Definition at line 57 of file lin_types.h.

18.55.2.2 I_u16 supplier_id

Supplier ID

Definition at line 56 of file lin_types.h.

18.55.2.3 I_u8 variant

Variant value

Definition at line 58 of file lin_types.h.

The documentation for this struct was generated from the following file:

- middleware/lin/include/lin_types.h

18.56 Md4 Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/md4.h>
```

Data Fields

- word32 [buffLen](#)
- word32 [loLen](#)
- word32 [hiLen](#)
- word32 [digest](#) [MD4_DIGEST_SIZE/sizeof(word32)]
- word32 [buffer](#) [MD4_BLOCK_SIZE/sizeof(word32)]

18.56.1 Detailed Description

Definition at line 43 of file md4.h.

18.56.2 Field Documentation

18.56.2.1 word32 [buffer](#)[MD4_BLOCK_SIZE /sizeof(word32)]

Definition at line 48 of file md4.h.

18.56.2.2 word32 [buffLen](#)

Definition at line 44 of file md4.h.

18.56.2.3 word32 [digest](#)[MD4_DIGEST_SIZE/sizeof(word32)]

Definition at line 47 of file md4.h.

18.56.2.4 word32 [hiLen](#)

Definition at line 46 of file md4.h.

18.56.2.5 word32 [loLen](#)

Definition at line 45 of file md4.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/md4.h

18.57 Md5 Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/md5.h>
```

Data Fields

- word32 [buffLen](#)

- word32 [loLen](#)
- word32 [hiLen](#)
- word32 [buffer](#) [MD5_BLOCK_SIZE/sizeof(word32)]
- word32 [digest](#) [MD5_DIGEST_SIZE/sizeof(word32)]
- void * [heap](#)

18.57.1 Detailed Description

Definition at line 64 of file md5.h.

18.57.2 Field Documentation

18.57.2.1 word32 [buffer](#)[MD5_BLOCK_SIZE /sizeof(word32)]

Definition at line 68 of file md5.h.

18.57.2.2 word32 [buffLen](#)

Definition at line 65 of file md5.h.

18.57.2.3 word32 [digest](#)[MD5_DIGEST_SIZE/sizeof(word32)]

Definition at line 72 of file md5.h.

18.57.2.4 void* [heap](#)

Definition at line 74 of file md5.h.

18.57.2.5 word32 [hiLen](#)

Definition at line 67 of file md5.h.

18.57.2.6 word32 [loLen](#)

Definition at line 66 of file md5.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/md5.h`

18.58 mp_int Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/integer.h>
```

Data Fields

- int [used](#)
- int [alloc](#)
- int [sign](#)
- mp_digit * [dp](#)

18.58.1 Detailed Description

Definition at line 196 of file integer.h.

18.58.2 Field Documentation

18.58.2.1 int alloc

Definition at line 197 of file integer.h.

18.58.2.2 mp_digit* dp

Definition at line 198 of file integer.h.

18.58.2.3 int sign

Definition at line 197 of file integer.h.

18.58.2.4 int used

Definition at line 197 of file integer.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/integer.h`

18.59 mpu_instance_t Struct Reference

Structure storing PAL instance information.

```
#include <platform/pal/inc/mpu_pal_mapping.h>
```

Data Fields

- [mpu_inst_type_t instType](#)
- [uint32_t instIdx](#)

18.59.1 Detailed Description

Structure storing PAL instance information.

This structure is used for storing PAL instance information. Implements : `mpu_instance_t_Class`

Definition at line 68 of file `mpu_pal_mapping.h`.

18.59.2 Field Documentation

18.59.2.1 uint32_t instIdx

Instance index of the peripheral over which the PAL is used

Definition at line 71 of file `mpu_pal_mapping.h`.

18.59.2.2 mpu_inst_type_t instType

Peripheral over which the PAL is used

Definition at line 70 of file `mpu_pal_mapping.h`.

The documentation for this struct was generated from the following file:

- `platform/pal/inc/mpu_pal_mapping.h`

18.60 MsgsReceived Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- word16 [got_hello_request](#):1
- word16 [got_client_hello](#):2
- word16 [got_server_hello](#):1
- word16 [got_hello_verify_request](#):1
- word16 [got_session_ticket](#):1
- word16 [got_end_of_early_data](#):1
- word16 [got_hello_retry_request](#):1
- word16 [got_encrypted_extensions](#):1
- word16 [got_certificate](#):1
- word16 [got_certificate_status](#):1
- word16 [got_server_key_exchange](#):1
- word16 [got_certificate_request](#):1
- word16 [got_server_hello_done](#):1
- word16 [got_certificate_verify](#):1
- word16 [got_client_key_exchange](#):1
- word16 [got_finished](#):1
- word16 [got_key_update](#):1
- word16 [got_change_cipher](#):1

18.60.1 Detailed Description

Definition at line 3141 of file internal.h.

18.60.2 Field Documentation

18.60.2.1 word16 got_certificate

Definition at line 3150 of file internal.h.

18.60.2.2 word16 got_certificate_request

Definition at line 3153 of file internal.h.

18.60.2.3 word16 got_certificate_status

Definition at line 3151 of file internal.h.

18.60.2.4 word16 got_certificate_verify

Definition at line 3155 of file internal.h.

18.60.2.5 word16 got_change_cipher

Definition at line 3159 of file internal.h.

18.60.2.6 word16 got_client_hello

Definition at line 3143 of file internal.h.

18.60.2.7 word16 got_client_key_exchange

Definition at line 3156 of file internal.h.

18.60.2.8 word16 got_encrypted_extensions

Definition at line 3149 of file internal.h.

18.60.2.9 word16 got_end_of_early_data

Definition at line 3147 of file internal.h.

18.60.2.10 word16 got_finished

Definition at line 3157 of file internal.h.

18.60.2.11 word16 got_hello_request

Definition at line 3142 of file internal.h.

18.60.2.12 word16 got_hello_retry_request

Definition at line 3148 of file internal.h.

18.60.2.13 word16 got_hello_verify_request

Definition at line 3145 of file internal.h.

18.60.2.14 word16 got_key_update

Definition at line 3158 of file internal.h.

18.60.2.15 word16 got_server_hello

Definition at line 3144 of file internal.h.

18.60.2.16 word16 got_server_hello_done

Definition at line 3154 of file internal.h.

18.60.2.17 word16 got_server_key_exchange

Definition at line 3152 of file internal.h.

18.60.2.18 word16 got_session_ticket

Definition at line 3146 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.61 oc_instance_t Struct Reference

Structure storing PAL instance information.

```
#include <platform/pal/inc/oc_pal_mapping.h>
```

Data Fields

- oc_inst_type_t [instType](#)

- uint32_t [instIdx](#)

18.61.1 Detailed Description

Structure storing PAL instance information.

This structure is used for storing PAL instance information. Implements : [oc_instance_t_Class](#)

Definition at line 110 of file [oc_pal_mapping.h](#).

18.61.2 Field Documentation

18.61.2.1 uint32_t instIdx

Instance index of the peripheral over which the PAL is used

Definition at line 112 of file [oc_pal_mapping.h](#).

18.61.2.2 oc_inst_type_t instType

Peripheral over which the PAL is used

Definition at line 111 of file [oc_pal_mapping.h](#).

The documentation for this struct was generated from the following file:

- [platform/pal/inc/oc_pal_mapping.h](#)

18.62 oc_pal_state_t Struct Reference

The internal context structure.

18.62.1 Detailed Description

The internal context structure.

This structure is used by the driver for its internal logic. It must be provided by the application through the [OC_Init\(\)](#) function, then it cannot be freed until the driver is de-initialized using [OC_Deinit\(\)](#). The application should make no assumptions about the content of this structure.

Definition at line 97 of file [oc_pal.c](#).

The documentation for this struct was generated from the following file:

- [platform/pal/src/oc/oc_pal.c](#)

18.63 OcspEntry Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [OcspEntry](#) * [next](#)
- byte [issuerHash](#) [OCSP_DIGEST_SIZE]
- byte [issuerKeyHash](#) [OCSP_DIGEST_SIZE]
- CertStatus * [status](#)
- int [totalStatus](#)

18.63.1 Detailed Description

Definition at line 1578 of file internal.h.

18.63.2 Field Documentation

18.63.2.1 byte issuerHash[OCSP_DIGEST_SIZE]

Definition at line 1580 of file internal.h.

18.63.2.2 byte issuerKeyHash[OCSP_DIGEST_SIZE]

Definition at line 1581 of file internal.h.

18.63.2.3 OcspNext* next

Definition at line 1579 of file internal.h.

18.63.2.4 CertStatus* status

Definition at line 1582 of file internal.h.

18.63.2.5 int totalStatus

Definition at line 1583 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.64 Options Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- wc_psk_client_callback [client_psk_cb](#)
- wc_psk_server_callback [server_psk_cb](#)
- word16 [havePSK](#):1
- word16 [sendVerify](#):2
- word16 [sessionCacheOff](#):1
- word16 [sessionCacheFlushOff](#):1
- word16 [side](#):1
- word16 [verifyPeer](#):1
- word16 [verifyNone](#):1
- word16 [failNoCert](#):1
- word16 [failNoCertxPSK](#):1
- word16 [downgrade](#):1
- word16 [resuming](#):1
- word16 [haveSessionId](#):1
- word16 [tls](#):1
- word16 [tls1_1](#):1
- word16 [tls1_3](#):1
- word16 [dtls](#):1
- word16 [connReset](#):1
- word16 [isClosed](#):1

- word16 [closeNotify](#):1
- word16 [sentNotify](#):1
- word16 [usingCompression](#):1
- word16 [haveRSA](#):1
- word16 [haveECC](#):1
- word16 [haveDH](#):1
- word16 [haveNTRU](#):1
- word16 [haveQSH](#):1
- word16 [haveECDSA](#)sig:1
- word16 [haveStaticECC](#):1
- word16 [havePeerCert](#):1
- word16 [havePeerVerify](#):1
- word16 [usingPSK_cipher](#):1
- word16 [usingAnon_cipher](#):1
- word16 [noPskDheKe](#):1
- word16 [sendAlertState](#):1
- word16 [partialWrite](#):1
- word16 [quietShutdown](#):1
- word16 [certOnly](#):1
- word16 [groupMessages](#):1
- word16 [usingNonblock](#):1
- word16 [saveArrays](#):1
- word16 [weOwnRng](#):1
- word16 [haveEMS](#):1
- word16 [keepResources](#):1
- word16 [useClientOrder](#):1
- byte [processReply](#)
- byte [cipherSuite0](#)
- byte [cipherSuite](#)
- byte [serverState](#)
- byte [clientState](#)
- byte [handShakeState](#)
- byte [handShakeDone](#)
- byte [minDowngrade](#)
- byte [connectState](#)
- byte [acceptState](#)
- byte [asyncState](#)
- byte [buildMsgState](#)
- byte [alertCount](#)
- word16 [minDhKeySz](#)
- word16 [dhKeySz](#)
- short [minRsaKeySz](#)

18.64.1 Detailed Description

Definition at line 2807 of file internal.h.

18.64.2 Field Documentation

18.64.2.1 byte acceptState

Definition at line 2909 of file internal.h.

18.64.2.2 byte alertCount

Definition at line 2912 of file internal.h.

18.64.2.3 byte asyncState

Definition at line 2910 of file internal.h.

18.64.2.4 byte buildMsgState

Definition at line 2911 of file internal.h.

18.64.2.5 word16 certOnly

Definition at line 2858 of file internal.h.

18.64.2.6 byte cipherSuite

Definition at line 2902 of file internal.h.

18.64.2.7 byte cipherSuite0

Definition at line 2901 of file internal.h.

18.64.2.8 wc_psk_client_callback client_psk_cb

Definition at line 2809 of file internal.h.

18.64.2.9 byte clientState

Definition at line 2904 of file internal.h.

18.64.2.10 word16 closeNotify

Definition at line 2840 of file internal.h.

18.64.2.11 byte connectState

Definition at line 2908 of file internal.h.

18.64.2.12 word16 connReset

Definition at line 2838 of file internal.h.

18.64.2.13 word16 dhKeySz

Definition at line 2918 of file internal.h.

18.64.2.14 word16 downgrade

Definition at line 2831 of file internal.h.

18.64.2.15 word16 dtls

Definition at line 2837 of file internal.h.

18.64.2.16 word16 failNoCert

Definition at line 2829 of file internal.h.

18.64.2.17 word16 failNoCertxPSK

Definition at line 2830 of file internal.h.

18.64.2.18 word16 groupMessages

Definition at line 2859 of file internal.h.

18.64.2.19 byte handShakeDone

Definition at line 2906 of file internal.h.

18.64.2.20 byte handShakeState

Definition at line 2905 of file internal.h.

18.64.2.21 word16 haveDH

Definition at line 2845 of file internal.h.

18.64.2.22 word16 haveECC

Definition at line 2844 of file internal.h.

18.64.2.23 word16 haveECDSAsig

Definition at line 2848 of file internal.h.

18.64.2.24 word16 haveEMS

Definition at line 2864 of file internal.h.

18.64.2.25 word16 haveNTRU

Definition at line 2846 of file internal.h.

18.64.2.26 word16 havePeerCert

Definition at line 2850 of file internal.h.

18.64.2.27 word16 havePeerVerify

Definition at line 2851 of file internal.h.

18.64.2.28 word16 havePSK

Definition at line 2813 of file internal.h.

18.64.2.29 word16 haveQSH

Definition at line 2847 of file internal.h.

18.64.2.30 word16 haveRSA

Definition at line 2843 of file internal.h.

18.64.2.31 word16 haveSessionId

Definition at line 2833 of file internal.h.

18.64.2.32 word16 haveStaticECC

Definition at line 2849 of file internal.h.

18.64.2.33 word16 isClosed

Definition at line 2839 of file internal.h.

18.64.2.34 word16 keepResources

Definition at line 2889 of file internal.h.

18.64.2.35 word16 minDhKeySz

Definition at line 2917 of file internal.h.

18.64.2.36 byte minDowngrade

Definition at line 2907 of file internal.h.

18.64.2.37 short minRsaKeySz

Definition at line 2921 of file internal.h.

18.64.2.38 word16 noPskDheKe

Definition at line 2854 of file internal.h.

18.64.2.39 word16 partialWrite

Definition at line 2856 of file internal.h.

18.64.2.40 byte processReply

Definition at line 2900 of file internal.h.

18.64.2.41 word16 quietShutdown

Definition at line 2857 of file internal.h.

18.64.2.42 word16 resuming

Definition at line 2832 of file internal.h.

18.64.2.43 word16 saveArrays

Definition at line 2861 of file internal.h.

18.64.2.44 word16 sendAlertState

Definition at line 2855 of file internal.h.

18.64.2.45 word16 sendVerify

Definition at line 2820 of file internal.h.

18.64.2.46 word16 sentNotify

Definition at line 2841 of file internal.h.

18.64.2.47 wc_psk_server_callback server_psk_cb

Definition at line 2810 of file internal.h.

18.64.2.48 byte serverState

Definition at line 2903 of file internal.h.

18.64.2.49 word16 sessionCacheFlushOff

Definition at line 2822 of file internal.h.

18.64.2.50 word16 sessionCacheOff

Definition at line 2821 of file internal.h.

18.64.2.51 word16 side

Definition at line 2826 of file internal.h.

18.64.2.52 word16 tls

Definition at line 2834 of file internal.h.

18.64.2.53 word16 tls1_1

Definition at line 2835 of file internal.h.

18.64.2.54 word16 tls1_3

Definition at line 2836 of file internal.h.

18.64.2.55 word16 useClientOrder

Definition at line 2890 of file internal.h.

18.64.2.56 word16 usingAnon_cipher

Definition at line 2853 of file internal.h.

18.64.2.57 word16 usingCompression

Definition at line 2842 of file internal.h.

18.64.2.58 word16 usingNonblock

Definition at line 2860 of file internal.h.

18.64.2.59 word16 usingPSK_cipher

Definition at line 2852 of file internal.h.

18.64.2.60 word16 verifyNone

Definition at line 2828 of file internal.h.

18.64.2.61 word16 verifyPeer

Definition at line 2827 of file internal.h.

18.64.2.62 word16 weOwnRng

Definition at line 2863 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.65 OS_Seed Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/random.h>
```

Data Fields

- int [fd](#)

18.65.1 Detailed Description

Definition at line 118 of file random.h.

18.65.2 Field Documentation

18.65.2.1 int fd

Definition at line 122 of file random.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/random.h

18.66 packetInfo_st Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/callbacks.h>
```

Data Fields

- char [packetName](#) [MAX_PACKETNAME_SZ+1]
- Timeval [timestamp](#)
- unsigned char [value](#) [MAX_VALUE_SZ]
- unsigned char * [bufferValue](#)
- int [valueSz](#)

18.66.1 Detailed Description

Definition at line 58 of file callbacks.h.

18.66.2 Field Documentation

18.66.2.1 unsigned char* bufferValue

Definition at line 62 of file callbacks.h.

18.66.2.2 char packetName[MAX_PACKETNAME_SZ+1]

Definition at line 59 of file callbacks.h.

18.66.2.3 Timeval timestamp

Definition at line 60 of file callbacks.h.

18.66.2.4 unsigned char value[MAX_VALUE_SZ]

Definition at line 61 of file callbacks.h.

18.66.2.5 int valueSz

Definition at line 63 of file callbacks.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/callbacks.h

18.67 phy_basicStatus_t Struct Reference

Structure containing the basic status information.

```
#include <platform/drivers/src/phy/phy_shared.h>
```

Data Fields

- bool [link](#)
- bool [autonegAbility](#)
- bool [extendedStatus](#)
- bool [baseT2Hd](#)
- bool [baseT2Fd](#)
- bool [autonegComplete](#)
- bool [remoteFault](#)

18.67.1 Detailed Description

Structure containing the basic status information.

Definition at line 57 of file phy_shared.h.

18.67.2 Field Documentation

18.67.2.1 bool autonegAbility

Auto-negotiation ability

Definition at line 60 of file phy_shared.h.

18.67.2.2 bool autonegComplete

Auto-negotiation complete

Definition at line 64 of file phy_shared.h.

18.67.2.3 bool baseT2Fd

100BASE-T2 Full-Duplex

Definition at line 63 of file phy_shared.h.

18.67.2.4 bool baseT2Hd

100BASE-T2 Half-Duplex

Definition at line 62 of file phy_shared.h.

18.67.2.5 bool extendedStatus

Extended Status

Definition at line 61 of file phy_shared.h.

18.67.2.6 bool link

Link Status

Definition at line 59 of file phy_shared.h.

18.67.2.7 bool remoteFault

Remote fault

Definition at line 65 of file phy_shared.h.

The documentation for this struct was generated from the following file:

- platform/drivers/src/phy/phy_shared.h

18.68 ProcPeerCertArgs Struct Reference

Data Fields

- [buffer](#) * [certs](#)
- [DecodedCert](#) * [dCert](#)
- char * [domain](#)
- word32 [idx](#)
- word32 [begin](#)
- int [totalCerts](#)
- int [count](#)
- int [dCertInit](#)
- int [certIdx](#)
- int [fatal](#)
- int [lastErr](#)

18.68.1 Detailed Description

Definition at line 7737 of file internal.c.

18.68.2 Field Documentation

18.68.2.1 word32 begin

Definition at line 7745 of file internal.c.

18.68.2.2 int certIdx

Definition at line 7749 of file internal.c.

18.68.2.3 buffer* certs

Definition at line 7738 of file internal.c.

18.68.2.4 int count

Definition at line 7747 of file internal.c.

18.68.2.5 DecodedCert* dCert

Definition at line 7742 of file internal.c.

18.68.2.6 int dCertInit

Definition at line 7748 of file internal.c.

18.68.2.7 char* domain

Definition at line 7743 of file internal.c.

18.68.2.8 int fatal

Definition at line 7750 of file internal.c.

18.68.2.9 word32 idx

Definition at line 7744 of file internal.c.

18.68.2.10 int lastErr

Definition at line 7751 of file internal.c.

18.68.2.11 int totalCerts

Definition at line 7746 of file internal.c.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/src/internal.c

18.69 ProtocolVersion Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- byte [major](#)
- byte [minor](#)

18.69.1 Detailed Description

Definition at line 1317 of file internal.h.

18.69.2 Field Documentation

18.69.2.1 byte major

Definition at line 1318 of file internal.h.

18.69.2.2 byte minor

Definition at line 1319 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.70 pwm_instance_t Struct Reference

Structure storing PAL instance information.

```
#include <platform/pal/inc/pwm_pal_mapping.h>
```

Data Fields

- pwm_inst_type_t [instType](#)
- uint32_t [instIdx](#)

18.70.1 Detailed Description

Structure storing PAL instance information.

This structure is used for storing PAL instance information. Implements : `pwm_instance_t_Class`

Definition at line 46 of file `pwm_pal_mapping.h`.

18.70.2 Field Documentation

18.70.2.1 uint32_t instIdx

Instance index of the peripheral over which the PAL is used

Definition at line 48 of file `pwm_pal_mapping.h`.

18.70.2.2 pwm_inst_type_t instType

Peripheral over which the PAL is used

Definition at line 47 of file `pwm_pal_mapping.h`.

The documentation for this struct was generated from the following file:

- platform/pal/inc/pwm_pal_mapping.h

18.71 qspi_ahb_config_t Struct Reference

AHB configuration structure.

```
#include <platform/drivers/inc/quadspi_driver.h>
```

Data Fields

- uint8_t [masters](#) [[QSPI_AHB_BUFFERS](#)]

- uint16_t sizes [QSPI_AHB_BUFFERS]
- bool allMasters
- bool highPriority

18.71.1 Detailed Description

AHB configuration structure.

This structure is used to provide configuration parameters for AHB access to the external flash Implements : qspi_ahb_config_t Class

Definition at line 208 of file quadspi_driver.h.

18.71.2 Field Documentation

18.71.2.1 bool allMasters

Indicates that any master may access the last buffer

Definition at line 212 of file quadspi_driver.h.

18.71.2.2 bool highPriority

Indicates that the first buffer has high priority

Definition at line 213 of file quadspi_driver.h.

18.71.2.3 uint8_t masters[QSPI_AHB_BUFFERS]

List of AHB masters assigned to each buffer

Definition at line 210 of file quadspi_driver.h.

18.71.2.4 uint16_t sizes[QSPI_AHB_BUFFERS]

List of buffer sizes

Definition at line 211 of file quadspi_driver.h.

The documentation for this struct was generated from the following file:

- platform/drivers/inc/quadspi_driver.h

18.72 qspi_state_t Struct Reference

Driver internal context structure.

```
#include <platform/drivers/inc/quadspi_driver.h>
```

18.72.1 Detailed Description

Driver internal context structure.

This structure is used by the driver for its internal logic. It must be provided by the application through the QSPI_DRV_Init() function, then it cannot be freed until the driver is de-initialized using QSPI_DRV_Deinit(). The application should make no assumptions about the content of this structure.

Definition at line 225 of file quadspi_driver.h.

The documentation for this struct was generated from the following file:

- platform/drivers/inc/quadspi_driver.h

18.73 qspi_user_config_t Struct Reference

Driver configuration structure.

```
#include <platform/drivers/inc/quadspi_driver.h>
```

Data Fields

- [qspi_data_rate_t dataRate](#)
- [bool dmaSupport](#)
- [uint8_t dmaChannel](#)
- [qspi_callback_t callback](#)
- [void * callbackParam](#)
- [qspi_flash_side_t side](#)
- [uint32_t memSize](#)
- [uint8_t csHoldTime](#)
- [uint8_t csSetupTime](#)
- [uint8_t columnAddr](#)
- [bool wordAddressable](#)
- [qspi_read_mode_t readMode](#)
- [qspi_sample_delay_t sampleDelay](#)
- [qspi_sample_phase_t samplePhase](#)
- [uint8_t dqsDelay](#)
- [bool dqsInvert](#)
- [qspi_endianness_t endianness](#)
- [qspi_clock_src_t clock_src](#)
- [uint8_t divider](#)
- [uint8_t io2IdleValue](#)
- [uint8_t io3IdleValue](#)
- [bool dozeMode](#)

18.73.1 Detailed Description

Driver configuration structure.

This structure is used to provide configuration parameters for the qspi driver at initialization time. Implements : [qspi_user_config_t_Class](#)

Definition at line 173 of file [quadspi_driver.h](#).

18.73.2 Field Documentation

18.73.2.1 qspi_callback_t callback

User callback for reporting asynchronous events

Definition at line 180 of file [quadspi_driver.h](#).

18.73.2.2 void* callbackParam

Parameter for user callback

Definition at line 181 of file [quadspi_driver.h](#).

18.73.2.3 qspi_clock_src_t clock_src

Clock source for QuadSPI device

Definition at line 194 of file [quadspi_driver.h](#).

18.73.2.4 uint8_t columnAddr

Width of the column address, 0 if not used

Definition at line 186 of file quadspi_driver.h.

18.73.2.5 uint8_t csHoldTime

CS hold time, expressed in serial clock cycles

Definition at line 184 of file quadspi_driver.h.

18.73.2.6 uint8_t csSetupTime

CS setup time, expressed in serial clock cycles

Definition at line 185 of file quadspi_driver.h.

18.73.2.7 qspi_data_rate_t dataRate

Single/double data rate

Definition at line 175 of file quadspi_driver.h.

18.73.2.8 uint8_t divider

(1 - 8) Divider value for input clock

Definition at line 195 of file quadspi_driver.h.

18.73.2.9 uint8_t dmaChannel

DMA channel number. Only used if dmaSupport is true

Definition at line 178 of file quadspi_driver.h.

18.73.2.10 bool dmaSupport

Enables DMA support in the driver

Definition at line 176 of file quadspi_driver.h.

18.73.2.11 bool dozeMode

Enable Doze Mode

Definition at line 198 of file quadspi_driver.h.

18.73.2.12 uint8_t dqsDelay

Fine delay for internal or loopback DQS mode

Definition at line 191 of file quadspi_driver.h.

18.73.2.13 bool dqsInvert

Use inverted clock for internal or loopback DQS mode

Definition at line 192 of file quadspi_driver.h.

18.73.2.14 qspi_endianness_t endianness

Endianness configuration

Definition at line 193 of file quadspi_driver.h.

18.73.2.15 uint8_t io2IdleValue

(0 / 1) Logic level of IO[2] signal when not used

Definition at line 196 of file quadspi_driver.h.

18.73.2.16 uint8_t io3IdleValue

(0 / 1) Logic level of IO[3] signal when not used

Definition at line 197 of file quadspi_driver.h.

18.73.2.17 uint32_t memSize

Size of serial flash

Definition at line 183 of file quadspi_driver.h.

18.73.2.18 qspi_read_mode_t readMode

Read mode for incoming data from serial flash

Definition at line 188 of file quadspi_driver.h.

18.73.2.19 qspi_sample_delay_t sampleDelay

Delay (in clock cycles) used for sampling Rx data

Definition at line 189 of file quadspi_driver.h.

18.73.2.20 qspi_sample_phase_t samplePhase

Clock phase used for sampling Rx data

Definition at line 190 of file quadspi_driver.h.

18.73.2.21 qspi_flash_side_t side

Side on which the serial flash is connected

Definition at line 182 of file quadspi_driver.h.

18.73.2.22 bool wordAddressable

True if serial flash is word addressable

Definition at line 187 of file quadspi_driver.h.

The documentation for this struct was generated from the following file:

- platform/drivers/inc/quadspi_driver.h

18.74 Rabbit Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/rabbit.h>
```

Data Fields

- [RabbitCtx masterCtx](#)
- [RabbitCtx workCtx](#)

18.74.1 Detailed Description

Definition at line 49 of file rabbit.h.

18.74.2 Field Documentation

18.74.2.1 RabbitCtx masterCtx

Definition at line 50 of file rabbit.h.

18.74.2.2 RabbitCtx workCtx

Definition at line 51 of file rabbit.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/rabbit.h

18.75 RabbitCtx Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/rabbit.h>
```

Data Fields

- word32 [x](#) [8]
- word32 [c](#) [8]
- word32 [carry](#)

18.75.1 Detailed Description

Definition at line 41 of file rabbit.h.

18.75.2 Field Documentation

18.75.2.1 word32 c[8]

Definition at line 43 of file rabbit.h.

18.75.2.2 word32 carry

Definition at line 44 of file rabbit.h.

18.75.2.3 word32 x[8]

Definition at line 42 of file rabbit.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/rabbit.h

18.76 ReadDirCtx Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/wc_port.h>
```

Data Fields

- struct dirent * [entry](#)
- DIR * [dir](#)
- struct stat [s](#)
- char [name](#) [MAX_FILENAME_SZ]

18.76.1 Detailed Description

Definition at line 292 of file wc_port.h.

18.76.2 Field Documentation

18.76.2.1 DIR* dir

Definition at line 298 of file wc_port.h.

18.76.2.2 struct dirent* entry

Definition at line 297 of file wc_port.h.

18.76.2.3 char name[MAX_FILENAME_SZ]

Definition at line 301 of file wc_port.h.

18.76.2.4 struct stat s

Definition at line 299 of file wc_port.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/wc_port.h

18.77 RecordLayerHeader Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- byte [type](#)
- byte [pvMajor](#)
- byte [pvMinor](#)
- byte [length](#) [2]

18.77.1 Detailed Description

Definition at line 3090 of file internal.h.

18.77.2 Field Documentation

18.77.2.1 byte length[2]

Definition at line 3094 of file internal.h.

18.77.2.2 byte pvMajor

Definition at line 3092 of file internal.h.

18.77.2.3 byte pvMinor

Definition at line 3093 of file internal.h.

18.77.2.4 byte type

Definition at line 3091 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.78 RsaKey Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/rsa.h>
```

Data Fields

- [mp_int n](#)
- [mp_int e](#)
- [mp_int d](#)
- [mp_int p](#)
- [mp_int q](#)
- [mp_int dP](#)
- [mp_int dQ](#)
- [mp_int u](#)
- void * [heap](#)
- byte * [data](#)
- int [type](#)
- int [state](#)
- word32 [dataLen](#)
- byte [datalsAlloc](#)

18.78.1 Detailed Description

Definition at line 90 of file rsa.h.

18.78.2 Field Documentation

18.78.2.1 mp_int d

Definition at line 91 of file rsa.h.

18.78.2.2 byte* data

Definition at line 93 of file rsa.h.

18.78.2.3 byte datalsAlloc

Definition at line 111 of file rsa.h.

18.78.2.4 word32 dataLen

Definition at line 96 of file rsa.h.

18.78.2.5 mp_int dP

Definition at line 91 of file rsa.h.

18.78.2.6 mp_int dQ

Definition at line 91 of file rsa.h.

18.78.2.7 mp_int e

Definition at line 91 of file rsa.h.

18.78.2.8 void* heap

Definition at line 92 of file rsa.h.

18.78.2.9 mp_int n

Definition at line 91 of file rsa.h.

18.78.2.10 mp_int p

Definition at line 91 of file rsa.h.

18.78.2.11 mp_int q

Definition at line 91 of file rsa.h.

18.78.2.12 int state

Definition at line 95 of file rsa.h.

18.78.2.13 int type

Definition at line 94 of file rsa.h.

18.78.2.14 mp_int u

Definition at line 91 of file rsa.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/rsa.h

18.79 SckeArgs Struct Reference

Data Fields

- byte * [output](#)
- byte * [encSecret](#)
- byte * [input](#)
- word32 [encSz](#)
- word32 [length](#)
- int [sendSz](#)
- int [inputSz](#)

18.79.1 Detailed Description

Definition at line 18497 of file internal.c.

18.79.2 Field Documentation

18.79.2.1 `byte* encSecret`

Definition at line 18499 of file internal.c.

18.79.2.2 `word32 encSz`

Definition at line 18501 of file internal.c.

18.79.2.3 `byte* input`

Definition at line 18500 of file internal.c.

18.79.2.4 `int inputSz`

Definition at line 18504 of file internal.c.

18.79.2.5 `word32 length`

Definition at line 18502 of file internal.c.

18.79.2.6 `byte* output`

Definition at line 18498 of file internal.c.

18.79.2.7 `int sendSz`

Definition at line 18503 of file internal.c.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/src/internal.c`

18.80 ScvArgs Struct Reference

Data Fields

- `byte * output`
- `byte * verifySig`
- `byte * verify`
- `byte * input`
- `word32 idx`
- `word32 extraSz`
- `word32 sigSz`
- `int sendSz`
- `int inputSz`
- `word16 length`
- `byte sigAlgo`

18.80.1 Detailed Description

Definition at line 19663 of file internal.c.

18.80.2 Field Documentation

18.80.2.1 word32 extraSz

Definition at line 19671 of file internal.c.

18.80.2.2 word32 idx

Definition at line 19670 of file internal.c.

18.80.2.3 byte* input

Definition at line 19669 of file internal.c.

18.80.2.4 int inputSz

Definition at line 19674 of file internal.c.

18.80.2.5 word16 length

Definition at line 19675 of file internal.c.

18.80.2.6 byte* output

Definition at line 19664 of file internal.c.

18.80.2.7 int sendSz

Definition at line 19673 of file internal.c.

18.80.2.8 byte sigAlgo

Definition at line 19676 of file internal.c.

18.80.2.9 word32 sigSz

Definition at line 19672 of file internal.c.

18.80.2.10 byte* verify

Definition at line 19668 of file internal.c.

18.80.2.11 byte* verifySig

Definition at line 19666 of file internal.c.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/src/internal.c`

18.81 SessionRow Struct Reference

Data Fields

- int [nextIdx](#)
- int [totalCount](#)
- [WOLFSSL_SESSION Sessions](#) [SESSIONS_PER_ROW]

18.81.1 Detailed Description

Definition at line 4139 of file ssl.c.

18.81.2 Field Documentation

18.81.2.1 int nextIdx

Definition at line 4140 of file ssl.c.

18.81.2.2 WOLFSSL_SESSION Sessions[SESSIONS_PER_ROW]

Definition at line 4142 of file ssl.c.

18.81.2.3 int totalCount

Definition at line 4141 of file ssl.c.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/src/ssl.c

18.82 Sha Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/sha.h>
```

Data Fields

- word32 [buffLen](#)
- word32 [loLen](#)
- word32 [hiLen](#)
- word32 [buffer](#) [SHA_BLOCK_SIZE/sizeof(word32)]
- word32 [digest](#) [SHA_DIGEST_SIZE/sizeof(word32)]
- void * [heap](#)

18.82.1 Detailed Description

Definition at line 66 of file sha.h.

18.82.2 Field Documentation

18.82.2.1 word32 buffer[SHA_BLOCK_SIZE /sizeof(word32)]

Definition at line 73 of file sha.h.

18.82.2.2 word32 buffLen

Definition at line 70 of file sha.h.

18.82.2.3 word32 digest[SHA_DIGEST_SIZE/sizeof(word32)]

Definition at line 77 of file sha.h.

18.82.2.4 void* heap

Definition at line 79 of file sha.h.

18.82.2.5 word32 hiLen

Definition at line 72 of file sha.h.

18.82.2.6 word32 loLen

Definition at line 71 of file sha.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/sha.h

18.83 Sha256 Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/sha256.h>
```

Data Fields

- ALIGN16 word32 [digest](#) [SHA256_DIGEST_SIZE/sizeof(word32)]
- ALIGN16 word32 [buffer](#) [SHA256_BLOCK_SIZE/sizeof(word32)]
- word32 [buffLen](#)
- word32 [loLen](#)
- word32 [hiLen](#)
- void * [heap](#)

18.83.1 Detailed Description

Definition at line 66 of file sha256.h.

18.83.2 Field Documentation

18.83.2.1 ALIGN16 word32 [buffer](#)[SHA256_BLOCK_SIZE /sizeof(word32)]

Definition at line 72 of file sha256.h.

18.83.2.2 word32 [buffLen](#)

Definition at line 73 of file sha256.h.

18.83.2.3 ALIGN16 word32 [digest](#)[SHA256_DIGEST_SIZE/sizeof(word32)]

Definition at line 71 of file sha256.h.

18.83.2.4 void* [heap](#)

Definition at line 76 of file sha256.h.

18.83.2.5 word32 [hiLen](#)

Definition at line 75 of file sha256.h.

18.83.2.6 word32 [loLen](#)

Definition at line 74 of file sha256.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/sha256.h

18.84 SignatureCtx Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h>
```

Data Fields

- void * [heap](#)
- byte * [digest](#)
- byte * [out](#)
- byte * [plain](#)
- union {
 - struct [RsaKey](#) * [rsa](#)
 - void * [ptr](#)
- } [key](#)
- int [devId](#)
- int [state](#)
- int [typeH](#)
- int [digestSz](#)
- word32 [keyOID](#)

18.84.1 Detailed Description

Definition at line 427 of file `asn.h`.

18.84.2 Field Documentation

18.84.2.1 int devId

Definition at line 449 of file `asn.h`.

18.84.2.2 byte* digest

Definition at line 429 of file `asn.h`.

18.84.2.3 int digestSz

Definition at line 452 of file `asn.h`.

18.84.2.4 void* heap

Definition at line 428 of file `asn.h`.

18.84.2.5 union { ... } key

18.84.2.6 word32 keyOID

Definition at line 453 of file `asn.h`.

18.84.2.7 byte* out

Definition at line 431 of file `asn.h`.

18.84.2.8 byte* plain

Definition at line 432 of file `asn.h`.

18.84.2.9 void* ptr

Definition at line 447 of file asn.h.

18.84.2.10 struct RsaKey* rsa

Definition at line 439 of file asn.h.

18.84.2.11 int state

Definition at line 450 of file asn.h.

18.84.2.12 int typeH

Definition at line 451 of file asn.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h

18.85 Signer Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h>
```

Data Fields

- word32 [pubKeySize](#)
- word32 [keyOID](#)
- word16 [keyUsage](#)
- byte [pathLength](#)
- byte [pathLengthSet](#)
- byte * [publicKey](#)
- int [nameLen](#)
- char * [name](#)
- [Base_entry](#) * [permittedNames](#)
- [Base_entry](#) * [excludedNames](#)
- byte [subjectNameHash](#) [SIGNER_DIGEST_SIZE]
- byte [subjectKeyIdHash](#) [SIGNER_DIGEST_SIZE]
- [Signer](#) * [next](#)

18.85.1 Detailed Description

Definition at line 675 of file asn.h.

18.85.2 Field Documentation

18.85.2.1 Base_entry* excludedNames

Definition at line 686 of file asn.h.

18.85.2.2 word32 keyOID

Definition at line 677 of file asn.h.

18.85.2.3 word16 keyUsage

Definition at line 678 of file asn.h.

18.85.2.4 char* name

Definition at line 683 of file asn.h.

18.85.2.5 int nameLen

Definition at line 682 of file asn.h.

18.85.2.6 Signer* next

Definition at line 694 of file asn.h.

18.85.2.7 byte pathLength

Definition at line 679 of file asn.h.

18.85.2.8 byte pathLengthSet

Definition at line 680 of file asn.h.

18.85.2.9 Base_entry* permittedNames

Definition at line 685 of file asn.h.

18.85.2.10 word32 pubKeySize

Definition at line 676 of file asn.h.

18.85.2.11 byte* publicKey

Definition at line 681 of file asn.h.

18.85.2.12 byte subjectKeyIdHash[SIGNER_DIGEST_SIZE]

Definition at line 691 of file asn.h.

18.85.2.13 byte subjectNameHash[SIGNER_DIGEST_SIZE]

Definition at line 688 of file asn.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h

18.86 smtp_send_request Struct Reference

```
#include <middleware/tcpip/tcpip_stack/apps/smtp/smtp.h>
```

Data Fields

- const char * [from](#)
- const char * [to](#)
- const char * [subject](#)
- const char * [body](#)
- smtp_result_fn [callback_fn](#)
- void * [callback_arg](#)
- u8_t [static_data](#)

18.86.1 Detailed Description

This structure is used as argument for `smtp_send_mail_int()`, which in turn can be used with `tcip_callback()` to send mail from interrupt context, e.g. like this: `struct smtp_send_request req; (to be filled) tcip_callback_with_block(smtp_send_mail_int, (void)req, 0);`

For member description, see parameter description of `smtp_send_mail()`. When using with `tcip_callback`, this structure has to stay allocated (e.g. using `mem_malloc/mem_free`) until its 'callback_fn' is called.

Definition at line 51 of file `smtp.h`.

18.86.2 Field Documentation

18.86.2.1 `const char* body`

Definition at line 55 of file `smtp.h`.

18.86.2.2 `void* callback_arg`

Definition at line 57 of file `smtp.h`.

18.86.2.3 `smtp_result_fn callback_fn`

Definition at line 56 of file `smtp.h`.

18.86.2.4 `const char* from`

Definition at line 52 of file `smtp.h`.

18.86.2.5 `u8_t static_data`

If this is `!= 0`, data is *not* copied into an extra buffer but used from the pointers supplied in this struct. This means less memory usage, but data must stay untouched until the callback function is called.

Definition at line 62 of file `smtp.h`.

18.86.2.6 `const char* subject`

Definition at line 54 of file `smtp.h`.

18.86.2.7 `const char* to`

Definition at line 53 of file `smtp.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcip/tcip_stack/apps/smtp/smtp.h`

18.87 spi_instance_t Struct Reference

Structure storing PAL instance information.

```
#include <platform/pal/inc/spi_pal_mapping.h>
```

Data Fields

- `spi_inst_type_t instType`
- `uint32_t instIdx`

18.87.1 Detailed Description

Structure storing PAL instance information.

This structure is used for storing PAL instance information. Implements : `spi_instance_t_Class`

Definition at line 50 of file `spi_pal_mapping.h`.

18.87.2 Field Documentation

18.87.2.1 `uint32_t instIdx`

Instance index of the peripheral over which the PAL is used

Definition at line 52 of file `spi_pal_mapping.h`.

18.87.2.2 `spi_inst_type_t instType`

Peripheral over which the PAL is used

Definition at line 51 of file `spi_pal_mapping.h`.

The documentation for this struct was generated from the following file:

- `platform/pal/inc/spi_pal_mapping.h`

18.88 SskeArgs Struct Reference

Data Fields

- `byte * output`
- `byte * sigDataBuf`
- `byte * verifySig`
- `word32 idx`
- `word32 tmpSigSz`
- `word32 length`
- `word32 sigSz`
- `word32 sigDataSz`
- `int sendSz`

18.88.1 Detailed Description

Definition at line 20477 of file `internal.c`.

18.88.2 Field Documentation

18.88.2.1 `word32 idx`

Definition at line 20488 of file `internal.c`.

18.88.2.2 `word32 length`

Definition at line 20490 of file `internal.c`.

18.88.2.3 `byte* output`

Definition at line 20478 of file `internal.c`.

18.88.2.4 int sendSz

Definition at line 20501 of file internal.c.

18.88.2.5 byte* sigDataBuf

Definition at line 20480 of file internal.c.

18.88.2.6 word32 sigDataSz

Definition at line 20493 of file internal.c.

18.88.2.7 word32 sigSz

Definition at line 20491 of file internal.c.

18.88.2.8 word32 tmpSigSz

Definition at line 20489 of file internal.c.

18.88.2.9 byte* verifySig

Definition at line 20486 of file internal.c.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/src/internal.c

18.89 Suites Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- word16 [suiteSz](#)
- word16 [hashSigAlgoSz](#)
- byte [suites](#) [WOLFSSL_MAX_SUITE_SZ]
- byte [hashSigAlgo](#) [HELLO_EXT_SIGALGO_MAX]
- byte [setSuites](#)
- byte [hashAlgo](#)
- byte [sigAlgo](#)

18.89.1 Detailed Description

Definition at line 1528 of file internal.h.

18.89.2 Field Documentation

18.89.2.1 byte hashAlgo

Definition at line 1534 of file internal.h.

18.89.2.2 byte hashSigAlgo[HELLO_EXT_SIGALGO_MAX]

Definition at line 1532 of file internal.h.

18.89.2.3 word16 hashSigAlgoSz

Definition at line 1530 of file internal.h.

18.89.2.4 byte setSuites

Definition at line 1533 of file internal.h.

18.89.2.5 byte sigAlgo

Definition at line 1535 of file internal.h.

18.89.2.6 byte suites[WOLFSSL_MAX_SUITE_SZ]

Definition at line 1531 of file internal.h.

18.89.2.7 word16 suiteSz

Definition at line 1529 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.90 t_atcert Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/port/atmel/atmel.h>
```

Data Fields

- uint32_t [signer_ca_size](#)
- uint8_t [signer_ca](#) [512]
- uint8_t [signer_ca_pubkey](#) [64]
- uint32_t [end_user_size](#)
- uint8_t [end_user](#) [512]
- uint8_t [end_user_pubkey](#) [64]

18.90.1 Detailed Description

Definition at line 46 of file atmel.h.

18.90.2 Field Documentation

18.90.2.1 uint8_t end_user[512]

Definition at line 51 of file atmel.h.

18.90.2.2 uint8_t end_user_pubkey[64]

Definition at line 52 of file atmel.h.

18.90.2.3 uint32_t end_user_size

Definition at line 50 of file atmel.h.

18.90.2.4 uint8_t signer_ca[512]

Definition at line 48 of file atmel.h.

18.90.2.5 uint8_t signer_ca_pubkey[64]

Definition at line 49 of file atmel.h.

18.90.2.6 uint32_t signer_ca_size

Definition at line 47 of file atmel.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/port/atmel/atmel.h

18.91 tcp_ready Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/test.h>
```

Data Fields

- word16 [ready](#)
- word16 [port](#)
- char * [srfName](#)

18.91.1 Detailed Description

Definition at line 293 of file test.h.

18.91.2 Field Documentation

18.91.2.1 word16 port

Definition at line 295 of file test.h.

18.91.2.2 word16 ready

Definition at line 294 of file test.h.

18.91.2.3 char* srfName

Definition at line 296 of file test.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/test.h

18.92 timeoutInfo_st Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/callbacks.h>
```

Data Fields

- char [timeoutName](#) [MAX_TIMEOUT_NAME_SZ+1]
- int [flags](#)
- int [numberPackets](#)
- [PacketInfo](#) [packets](#) [MAX_PACKETS_HANDSHAKE]
- Timeval [timeoutValue](#)

18.92.1 Detailed Description

Definition at line 67 of file callbacks.h.

18.92.2 Field Documentation

18.92.2.1 int flags

Definition at line 69 of file callbacks.h.

18.92.2.2 int numberPackets

Definition at line 70 of file callbacks.h.

18.92.2.3 PacketInfo packets[MAX_PACKETS_HANDSHAKE]

Definition at line 71 of file callbacks.h.

18.92.2.4 char timeoutName[MAX_TIMEOUT_NAME_SZ+1]

Definition at line 68 of file callbacks.h.

18.92.2.5 Timeval timeoutValue

Definition at line 72 of file callbacks.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/callbacks.h

18.93 timer_chan_state_t Struct Reference

Runtime state of the Timer channel.

18.93.1 Detailed Description

Runtime state of the Timer channel.

This structure is used by the driver for its internal logic The application should make no assumptions about the content of this structure

Definition at line 77 of file timing_pal.c.

The documentation for this struct was generated from the following file:

- platform/pal/src/timing/timing_pal.c

18.94 timing_instance_t Struct Reference

Structure storing PAL instance information.

```
#include <platform/pal/inc/timing_pal_mapping.h>
```

Data Fields

- timing_inst_type_t [instType](#)
- uint32_t [instIdx](#)

18.94.1 Detailed Description

Structure storing PAL instance information.

This structure is used for storing PAL instance information. Implements : `timing_instance_t_Class`

Definition at line 88 of file `timing_pal_mapping.h`.

18.94.2 Field Documentation

18.94.2.1 uint32_t instIdx

Instance index of the peripheral over which the PAL is used

Definition at line 90 of file `timing_pal_mapping.h`.

18.94.2.2 timing_inst_type_t instType

Peripheral over which the PAL is used

Definition at line 89 of file `timing_pal_mapping.h`.

The documentation for this struct was generated from the following file:

- `platform/pal/inc/timing_pal_mapping.h`

18.95 uart_instance_t Struct Reference

Structure storing PAL instance information.

```
#include <platform/pal/inc/uart_pal_mapping.h>
```

Data Fields

- `uart_inst_type_t instType`
- `uint32_t instIdx`

18.95.1 Detailed Description

Structure storing PAL instance information.

This structure is used for storing PAL instance information. Implements : `uart_instance_t_Class`

Definition at line 63 of file `uart_pal_mapping.h`.

18.95.2 Field Documentation

18.95.2.1 uint32_t instIdx

Instance index of the peripheral over which the PAL is used

Definition at line 66 of file `uart_pal_mapping.h`.

18.95.2.2 uart_inst_type_t instType

Peripheral over which the PAL is used

Definition at line 65 of file `uart_pal_mapping.h`.

The documentation for this struct was generated from the following file:

- `platform/pal/inc/uart_pal_mapping.h`

18.96 WC_DerCertList Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/pkcs12.h>
```

Data Fields

- `byte * buffer`
- `word32 bufferSz`
- `struct WC_DerCertList * next`

18.96.1 Detailed Description

Definition at line 36 of file pkcs12.h.

18.96.2 Field Documentation

18.96.2.1 `byte* buffer`

Definition at line 37 of file pkcs12.h.

18.96.2.2 `word32 bufferSz`

Definition at line 38 of file pkcs12.h.

18.96.2.3 `struct WC_DerCertList* next`

Definition at line 39 of file pkcs12.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/pkcs12.h`

18.97 wc_HashAlg Union Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/hash.h>
```

Data Fields

- `Md5 md5`
- `Sha sha`
- `Sha256 sha256`

18.97.1 Detailed Description

Definition at line 59 of file hash.h.

18.97.2 Field Documentation

18.97.2.1 `Md5 md5`

Definition at line 61 of file hash.h.

18.97.2.2 `Sha sha`

Definition at line 64 of file hash.h.

18.97.2.3 Sha256 sha256

Definition at line 70 of file hash.h.

The documentation for this union was generated from the following file:

- [middleware/tcpip/wolfssl/wolfssl/wolfcrypt/hash.h](#)

18.98 WC_RNG Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/random.h>
```

Data Fields

- [OS_Seed seed](#)
- void * [heap](#)
- struct DRBG * [drbg](#)
- byte [status](#)

18.98.1 Detailed Description

Definition at line 138 of file random.h.

18.98.2 Field Documentation

18.98.2.1 struct DRBG* drbg

Definition at line 143 of file random.h.

18.98.2.2 void* heap

Definition at line 140 of file random.h.

18.98.2.3 OS_Seed seed

Definition at line 139 of file random.h.

18.98.2.4 byte status

Definition at line 144 of file random.h.

The documentation for this struct was generated from the following file:

- [middleware/tcpip/wolfssl/wolfssl/wolfcrypt/random.h](#)

18.99 wdg_instance_t Struct Reference

Structure storing PAL instance information.

```
#include <platform/pal/inc/wdg_pal_mapping.h>
```

Data Fields

- [wdg_inst_type_t instType](#)
- uint32_t [instIdx](#)

18.99.1 Detailed Description

Structure storing PAL instance information.

This structure is used for storing PAL instance information. Implements : `wdg_instance_t_Class`

Definition at line 63 of file `wdg_pal_mapping.h`.

18.99.2 Field Documentation

18.99.2.1 `uint32_t instIdx`

Instance index of the peripheral over which the PAL is used

Definition at line 65 of file `wdg_pal_mapping.h`.

18.99.2.2 `wdg_inst_type_t instType`

Peripheral over which the PAL is used

Definition at line 64 of file `wdg_pal_mapping.h`.

The documentation for this struct was generated from the following file:

- `platform/pal/inc/wdg_pal_mapping.h`

18.100 WOLF_EVENT Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/wolfevent.h>
```

Data Fields

- `WOLF_EVENT * next`
- `WOLF_EVENT * prev`
- `void * context`
- union {
 - `void * ptr``} dev`
- `pthread_t threadId`
- `int ret`
- `unsigned int flags`
- `WOLF_EVENT_TYPE type`
- `WOLF_EVENT_STATE state`

18.100.1 Detailed Description

Definition at line 64 of file `wolfevent.h`.

18.100.2 Field Documentation

18.100.2.1 `void* context`

Definition at line 69 of file `wolfevent.h`.

18.100.2.2 union { ... } dev

18.100.2.3 unsigned int flags

Definition at line 83 of file wolfevent.h.

18.100.2.4 WOLF_EVENT* next

Definition at line 66 of file wolfevent.h.

18.100.2.5 WOLF_EVENT* prev

Definition at line 67 of file wolfevent.h.

18.100.2.6 void* ptr

Definition at line 71 of file wolfevent.h.

18.100.2.7 int ret

Definition at line 82 of file wolfevent.h.

18.100.2.8 WOLF_EVENT_STATE state

Definition at line 85 of file wolfevent.h.

18.100.2.9 pthread_t threadId

Definition at line 80 of file wolfevent.h.

18.100.2.10 WOLF_EVENT_TYPE type

Definition at line 84 of file wolfevent.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/wolfevent.h

18.101 WOLF_EVENT_QUEUE Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/wolfevent.h>
```

Data Fields

- [WOLF_EVENT * head](#)
- [WOLF_EVENT * tail](#)
- [wolfSSL_Mutex lock](#)
- [int count](#)

18.101.1 Detailed Description

Definition at line 92 of file wolfevent.h.

18.101.2 Field Documentation

18.101.2.1 int count

Definition at line 98 of file wolfevent.h.

18.101.2.2 WOLF_EVENT* head

Definition at line 93 of file wolfevent.h.

18.101.2.3 wolfSSL_Mutex lock

Definition at line 96 of file wolfevent.h.

18.101.2.4 WOLF_EVENT* tail

Definition at line 94 of file wolfevent.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/wolfevent.h

18.102 WOLFSSL Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [WOLFSSL_CTX](#) * ctx
- [Suites](#) * suites
- [Arrays](#) * arrays
- [HS_Hashes](#) * hsHashes
- void * [IOCB_ReadCtx](#)
- void * [IOCB_WriteCtx](#)
- [WC_RNG](#) * rng
- void * [verifyCbCtx](#)
- VerifyCallback [verifyCallback](#)
- void * [heap](#)
- HandShakeDoneCb [hsDoneCb](#)
- void * [hsDoneCtx](#)
- void * [hsKey](#)
- word32 [hsType](#)
- [WOLFSSL_CIPHER](#) cipher
- hmacfp [hmac](#)
- [Ciphers](#) encrypt
- [Ciphers](#) decrypt
- [Buffers](#) buffers
- [WOLFSSL_SESSION](#) session
- [WOLFSSL_ALERT_HISTORY](#) alert_history
- int [error](#)
- int [rfd](#)
- int [wfd](#)
- int [rflags](#)
- int [wflags](#)
- word32 [timeout](#)
- word32 [fragOffset](#)
- word16 [curSize](#)
- [RecordLayerHeader](#) curRL
- [MsgsReceived](#) msgsReceived
- [ProtocolVersion](#) version
- [ProtocolVersion](#) chVersion

- [CipherSpecs specs](#)
- [Keys keys](#)
- [Options options](#)
- [RsaKey * peerRsaKey](#)
- [byte peerRsaKeyPresent](#)
- [byte pssAlgo](#)
- [byte keepCert](#)
- [int devId](#)

18.102.1 Detailed Description

Definition at line 3222 of file internal.h.

18.102.2 Field Documentation

18.102.2.1 WOLFSSL_ALERT_HISTORY alert_history

Definition at line 3259 of file internal.h.

18.102.2.2 Arrays* arrays

Definition at line 3225 of file internal.h.

18.102.2.3 Buffers buffers

Definition at line 3254 of file internal.h.

18.102.2.4 ProtocolVersion chVersion

Definition at line 3271 of file internal.h.

18.102.2.5 WOLFSSL_CIPHER cipher

Definition at line 3250 of file internal.h.

18.102.2.6 WOLFSSL_CTX* ctx

Definition at line 3223 of file internal.h.

18.102.2.7 RecordLayerHeader curRL

Definition at line 3268 of file internal.h.

18.102.2.8 word16 curSize

Definition at line 3267 of file internal.h.

18.102.2.9 Ciphers decrypt

Definition at line 3253 of file internal.h.

18.102.2.10 int devId

Definition at line 3385 of file internal.h.

18.102.2.11 Ciphers encrypt

Definition at line 3252 of file internal.h.

18.102.2.12 int error

Definition at line 3260 of file internal.h.

18.102.2.13 word32 fragOffset

Definition at line 3266 of file internal.h.

18.102.2.14 void* heap

Definition at line 3232 of file internal.h.

18.102.2.15 hmacfp hmac

Definition at line 3251 of file internal.h.

18.102.2.16 HandShakeDoneCb hsDoneCb

Definition at line 3242 of file internal.h.

18.102.2.17 void* hsDoneCtx

Definition at line 3243 of file internal.h.

18.102.2.18 HS_Hashes* hsHashes

Definition at line 3226 of file internal.h.

18.102.2.19 void* hsKey

Definition at line 3248 of file internal.h.

18.102.2.20 word32 hsType

Definition at line 3249 of file internal.h.

18.102.2.21 void* IOCB_ReadCtx

Definition at line 3227 of file internal.h.

18.102.2.22 void* IOCB_WriteCtx

Definition at line 3228 of file internal.h.

18.102.2.23 byte keepCert

Definition at line 3381 of file internal.h.

18.102.2.24 Keys keys

Definition at line 3273 of file internal.h.

18.102.2.25 MsgsReceived msgsReceived

Definition at line 3269 of file internal.h.

18.102.2.26 Options options

Definition at line 3274 of file internal.h.

18.102.2.27 RsaKey* peerRsaKey

Definition at line 3285 of file internal.h.

18.102.2.28 byte peerRsaKeyPresent

Definition at line 3286 of file internal.h.

18.102.2.29 byte pssAlgo

Definition at line 3303 of file internal.h.

18.102.2.30 int rfd

Definition at line 3261 of file internal.h.

18.102.2.31 int rflags

Definition at line 3263 of file internal.h.

18.102.2.32 WC_RNG* rng

Definition at line 3229 of file internal.h.

18.102.2.33 WOLFSSL_SESSION session

Definition at line 3255 of file internal.h.

18.102.2.34 CipherSpecs specs

Definition at line 3272 of file internal.h.

18.102.2.35 Suites* suites

Definition at line 3224 of file internal.h.

18.102.2.36 word32 timeout

Definition at line 3265 of file internal.h.

18.102.2.37 VerifyCallback verifyCallback

Definition at line 3231 of file internal.h.

18.102.2.38 void* verifyCbCtx

Definition at line 3230 of file internal.h.

18.102.2.39 ProtocolVersion version

Definition at line 3270 of file internal.h.

18.102.2.40 int wfd

Definition at line 3262 of file internal.h.

18.102.2.41 int wflags

Definition at line 3264 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.103 WOLFSSL_ALERT Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- int [code](#)
- int [level](#)

18.103.1 Detailed Description

Definition at line 190 of file ssl.h.

18.103.2 Field Documentation

18.103.2.1 int code

Definition at line 191 of file ssl.h.

18.103.2.2 int level

Definition at line 192 of file ssl.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/ssl.h

18.104 WOLFSSL_ALERT_HISTORY Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- [WOLFSSL_ALERT last_rx](#)
- [WOLFSSL_ALERT last_tx](#)

18.104.1 Detailed Description

Definition at line 195 of file ssl.h.

18.104.2 Field Documentation

18.104.2.1 WOLFSSL_ALERT last_rx

Definition at line 196 of file ssl.h.

18.104.2.2 WOLFSSL_ALERT last_tx

Definition at line 197 of file ssl.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/ssl.h

18.105 WOLFSSL_ASN1_BIT_STRING Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/asn1.h>
```

Data Fields

- int [length](#)
- int [type](#)
- char * [data](#)
- long [flags](#)

18.105.1 Detailed Description

Definition at line 5 of file `asn1.h`.

18.105.2 Field Documentation

18.105.2.1 char* data

Definition at line 8 of file `asn1.h`.

18.105.2.2 long flags

Definition at line 9 of file `asn1.h`.

18.105.2.3 int length

Definition at line 6 of file `asn1.h`.

18.105.2.4 int type

Definition at line 7 of file `asn1.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/openssl/asn1.h`

18.106 WOLFSSL_ASN1_INTEGER Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- unsigned char [data](#) [20]

18.106.1 Detailed Description

Definition at line 146 of file `ssl.h`.

18.106.2 Field Documentation

18.106.2.1 unsigned char data[20]

Definition at line 149 of file `ssl.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/ssl.h`

18.107 WOLFSSL_ASN1_OBJECT Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h>
```

Data Fields

- void * [heap](#)
- byte * [obj](#)
- int [type](#)
- word32 [objSz](#)
- byte [dynamic](#)

18.107.1 Detailed Description

Definition at line 633 of file `asn.h`.

18.107.2 Field Documentation

18.107.2.1 byte dynamic

Definition at line 638 of file `asn.h`.

18.107.2.2 void* heap

Definition at line 634 of file `asn.h`.

18.107.2.3 byte* obj

Definition at line 635 of file `asn.h`.

18.107.2.4 word32 objSz

Definition at line 637 of file `asn.h`.

18.107.2.5 int type

Definition at line 636 of file `asn.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/wolfcrypt/asn.h`

18.108 WOLFSSL_ASN1_STRING Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/asn1.h>
```

Data Fields

- int [length](#)
- int [type](#)
- char * [data](#)
- long [flags](#)

18.108.1 Detailed Description

Definition at line 12 of file `asn1.h`.

18.108.2 Field Documentation

18.108.2.1 `char* data`

Definition at line 15 of file `asn1.h`.

18.108.2.2 `long flags`

Definition at line 16 of file `asn1.h`.

18.108.2.3 `int length`

Definition at line 13 of file `asn1.h`.

18.108.2.4 `int type`

Definition at line 14 of file `asn1.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/openssl/asn1.h`

18.109 WOLFSSL_ASN1_TIME Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- unsigned char `data` [32+2]

18.109.1 Detailed Description

Definition at line 153 of file `ssl.h`.

18.109.2 Field Documentation

18.109.2.1 `unsigned char data[32+2]`

Definition at line 155 of file `ssl.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/ssl.h`

18.110 WOLFSSL_BIGNUM Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/bn.h>
```

Data Fields

- int `neg`
- void * `internal`

18.110.1 Detailed Description

Definition at line 14 of file bn.h.

18.110.2 Field Documentation

18.110.2.1 void* internal

Definition at line 16 of file bn.h.

18.110.2.2 int neg

Definition at line 15 of file bn.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/bn.h

18.111 WOLFSSL_BIO Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [WOLFSSL * ssl](#)
- [XFILE file](#)
- [WOLFSSL_BIO * prev](#)
- [WOLFSSL_BIO * next](#)
- [WOLFSSL_BIO * pair](#)
- [void * heap](#)
- [byte * mem](#)
- [int wrSz](#)
- [int wrIdx](#)
- [int rdIdx](#)
- [int readRq](#)
- [int memLen](#)
- [int fd](#)
- [int eof](#)
- [byte type](#)
- [byte close](#)

18.111.1 Detailed Description

Definition at line 1360 of file internal.h.

18.111.2 Field Documentation

18.111.2.1 byte close

Definition at line 1378 of file internal.h.

18.111.2.2 int eof

Definition at line 1376 of file internal.h.

18.111.2.3 int fd

Definition at line 1375 of file internal.h.

18.111.2.4 XFILE file

Definition at line 1363 of file internal.h.

18.111.2.5 void* heap

Definition at line 1368 of file internal.h.

18.111.2.6 byte* mem

Definition at line 1369 of file internal.h.

18.111.2.7 int memLen

Definition at line 1374 of file internal.h.

18.111.2.8 WOLFSSL_BIO* next

Definition at line 1366 of file internal.h.

18.111.2.9 WOLFSSL_BIO* pair

Definition at line 1367 of file internal.h.

18.111.2.10 WOLFSSL_BIO* prev

Definition at line 1365 of file internal.h.

18.111.2.11 int rdIdx

Definition at line 1372 of file internal.h.

18.111.2.12 int readRq

Definition at line 1373 of file internal.h.

18.111.2.13 WOLFSSL* ssl

Definition at line 1361 of file internal.h.

18.111.2.14 byte type

Definition at line 1377 of file internal.h.

18.111.2.15 int wrIdx

Definition at line 1371 of file internal.h.

18.111.2.16 int wrSz

Definition at line 1370 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.112 WOLFSSL_BIO_METHOD Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- byte [type](#)

18.112.1 Detailed Description

Definition at line 1354 of file internal.h.

18.112.2 Field Documentation

18.112.2.1 byte type

Definition at line 1355 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.113 WOLFSSL_BUFFER_INFO Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- unsigned char * [buffer](#)
- unsigned int [length](#)

18.113.1 Detailed Description

Definition at line 213 of file ssl.h.

18.113.2 Field Documentation

18.113.2.1 unsigned char* buffer

Definition at line 214 of file ssl.h.

18.113.2.2 unsigned int length

Definition at line 215 of file ssl.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/ssl.h

18.114 WOLFSSL_CERT_MANAGER Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [Signer](#) * [caTable](#) [CA_TABLE_SIZE]
- void * [heap](#)
- [WOLFSSL_CRL](#) * [crl](#)
- [WOLFSSL_OCSP](#) * [ocsp](#)
- char * [ocspOverrideURL](#)
- void * [ocsplOCtx](#)
- CallbackCACache [caCacheCallback](#)
- CbMissingCRL [cbMissingCRL](#)
- CbOCSPIO [ocsplOCb](#)
- CbOCSPRespFree [ocspRespFreeCb](#)
- wolfSSL_Mutex [caLock](#)
- byte [crlEnabled](#)
- byte [crlCheckAll](#)
- byte [ocspEnabled](#)
- byte [ocspCheckAll](#)
- byte [ocspSendNonce](#)
- byte [ocspUseOverrideURL](#)
- byte [ocspStaplingEnabled](#)
- short [minRsaKeySz](#)

18.114.1 Detailed Description

Definition at line 1690 of file internal.h.

18.114.2 Field Documentation

18.114.2.1 CallbackCACache caCacheCallback

Definition at line 1705 of file internal.h.

18.114.2.2 wolfSSL_Mutex caLock

Definition at line 1709 of file internal.h.

18.114.2.3 Signer* caTable[CA_TABLE_SIZE]

Definition at line 1691 of file internal.h.

18.114.2.4 CbMissingCRL cbMissingCRL

Definition at line 1706 of file internal.h.

18.114.2.5 WOLFSSL_CRL* crl

Definition at line 1697 of file internal.h.

18.114.2.6 byte crlCheckAll

Definition at line 1711 of file internal.h.

18.114.2.7 byte crlEnabled

Definition at line 1710 of file internal.h.

18.114.2.8 void* heap

Definition at line 1692 of file internal.h.

18.114.2.9 short minRsaKeySz

Definition at line 1719 of file internal.h.

18.114.2.10 WOLFSSL_OCSP* ocsp

Definition at line 1698 of file internal.h.

18.114.2.11 byte ocspCheckAll

Definition at line 1713 of file internal.h.

18.114.2.12 byte ocspEnabled

Definition at line 1712 of file internal.h.

18.114.2.13 CbOCSPiO ocspIOCb

Definition at line 1707 of file internal.h.

18.114.2.14 void* ocspIOCtx

Definition at line 1704 of file internal.h.

18.114.2.15 char* ocspOverrideURL

Definition at line 1703 of file internal.h.

18.114.2.16 CbOCSPRespFree ocspRespFreeCb

Definition at line 1708 of file internal.h.

18.114.2.17 byte ocspSendNonce

Definition at line 1714 of file internal.h.

18.114.2.18 byte ocspStaplingEnabled

Definition at line 1716 of file internal.h.

18.114.2.19 byte ocspUseOverrideURL

Definition at line 1715 of file internal.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/internal.h`

18.115 WOLFSSL_Cipher Union Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/evp.h>
```

Data Fields

- [Aes aes](#)
- [Des des](#)

- [Des3 des3](#)
- [Arc4 arc4](#)

18.115.1 Detailed Description

Definition at line 116 of file evp.h.

18.115.2 Field Documentation

18.115.2.1 Aes aes

Definition at line 118 of file evp.h.

18.115.2.2 Arc4 arc4

Definition at line 124 of file evp.h.

18.115.2.3 Des des

Definition at line 121 of file evp.h.

18.115.2.4 Des3 des3

Definition at line 122 of file evp.h.

The documentation for this union was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/evp.h

18.116 WOLFSSL_CIPHER Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [WOLFSSL * ssl](#)

18.116.1 Detailed Description

Definition at line 1560 of file internal.h.

18.116.2 Field Documentation

18.116.2.1 WOLFSSL* ssl

Definition at line 1561 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.117 WOLFSSL_COMP_METHOD Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- [int type](#)

18.117.1 Detailed Description

Definition at line 169 of file ssl.h.

18.117.2 Field Documentation

18.117.2.1 int type

Definition at line 170 of file ssl.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/ssl.h

18.118 WOLFSSL_CRL Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [WOLFSSL_CERT_MANAGER * cm](#)
- [CRL_Entry * crlList](#)
- [wolfSSL_Mutex crlLock](#)
- [CRL_Monitor monitors](#) [2]
- [void * heap](#)

18.118.1 Detailed Description

Definition at line 1656 of file internal.h.

18.118.2 Field Documentation

18.118.2.1 WOLFSSL_CERT_MANAGER* cm

Definition at line 1657 of file internal.h.

18.118.2.2 CRL_Entry* crlList

Definition at line 1658 of file internal.h.

18.118.2.3 wolfSSL_Mutex crlLock

Definition at line 1662 of file internal.h.

18.118.2.4 void* heap

Definition at line 1670 of file internal.h.

18.118.2.5 CRL_Monitor monitors[2]

Definition at line 1663 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.119 WOLFSSL_CTX Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [WOLFSSL_METHOD](#) * [method](#)
- [wolfSSL_Mutex](#) [countMutex](#)
- int [refCount](#)
- int [err](#)
- [buffer](#) [serverDH_P](#)
- [buffer](#) [serverDH_G](#)
- [DerBuffer](#) * [certificate](#)
- [DerBuffer](#) * [certChain](#)
- [DerBuffer](#) * [privateKey](#)
- [byte](#) [privateKeyType](#)
- int [privateKeySz](#)
- [WOLFSSL_CERT_MANAGER](#) * [cm](#)
- [Suites](#) * [suites](#)
- [void](#) * [heap](#)
- [byte](#) [verifyPeer](#)
- [byte](#) [verifyNone](#)
- [byte](#) [failNoCert](#)
- [byte](#) [failNoCertxPSK](#)
- [byte](#) [sessionCacheOff](#)
- [byte](#) [sessionCacheFlushOff](#)
- [byte](#) [sendVerify](#)
- [byte](#) [haveRSA](#)
- [byte](#) [haveECC](#)
- [byte](#) [haveDH](#)
- [byte](#) [haveNTRU](#)
- [byte](#) [haveECDSAsig](#)
- [byte](#) [haveStaticECC](#)
- [byte](#) [partialWrite](#)
- [byte](#) [quietShutdown](#)
- [byte](#) [groupMessages](#)
- [byte](#) [minDowngrade](#)
- [byte](#) [haveEMS](#)
- [byte](#) [useClientOrder](#):1
- [word16](#) [minDhKeySz](#)
- [short](#) [minRsaKeySz](#)
- [CallbackIORecv](#) [CBIORecv](#)
- [CallbackIOSend](#) [CBIOSend](#)
- [VerifyCallback](#) [verifyCallback](#)
- [word32](#) [timeout](#)
- [byte](#) [havePSK](#)
- [wc_psk_client_callback](#) [client_psk_cb](#)
- [wc_psk_server_callback](#) [server_psk_cb](#)
- [char](#) [server_hint](#) [MAX_PSK_ID_LEN+NULL_TERM_LEN]
- int [devId](#)

18.119.1 Detailed Description

TLS Extensions - RFC 6066 Server Name Indication - RFC 6066 (session 3) Maximum Fragment Length Negotiation - RFC 6066 (session 4) Truncated HMAC - RFC 6066 (session 7) Certificate Status Request - RFC 6066 (session 8) Certificate Status Request v2 - RFC 6961 Supported Elliptic Curves - RFC 4492 (session 4) Renegotiation Indication - RFC 5746 Session Ticket - RFC 5077 (session 3.2) Quantum-Safe-Hybrid - draft-whyte-qsh-tls12-00

Definition at line 2208 of file internal.h.

18.119.2 Field Documentation

18.119.2.1 CallbackIORecv CBIORcv

Definition at line 2295 of file internal.h.

18.119.2.2 CallbackIOSend CBIOSend

Definition at line 2296 of file internal.h.

18.119.2.3 DerBuffer* certChain

Definition at line 2222 of file internal.h.

18.119.2.4 DerBuffer* certificate

Definition at line 2221 of file internal.h.

18.119.2.5 wc_psk_client_callback client_psk_cb

Definition at line 2316 of file internal.h.

18.119.2.6 WOLFSSL_CERT_MANAGER* cm

Definition at line 2236 of file internal.h.

18.119.2.7 wolfSSL_Mutex countMutex

Definition at line 2213 of file internal.h.

18.119.2.8 int devId

Definition at line 2353 of file internal.h.

18.119.2.9 int err

Definition at line 2215 of file internal.h.

18.119.2.10 byte failNoCert

Definition at line 2246 of file internal.h.

18.119.2.11 byte failNoCertxPSK

Definition at line 2247 of file internal.h.

18.119.2.12 byte groupMessages

Definition at line 2262 of file internal.h.

18.119.2.13 byte haveDH

Definition at line 2256 of file internal.h.

18.119.2.14 byte haveECC

Definition at line 2255 of file internal.h.

18.119.2.15 byte haveECDSAsig

Definition at line 2258 of file internal.h.

18.119.2.16 byte haveEMS

Definition at line 2264 of file internal.h.

18.119.2.17 byte haveNTRU

Definition at line 2257 of file internal.h.

18.119.2.18 byte havePSK

Definition at line 2315 of file internal.h.

18.119.2.19 byte haveRSA

Definition at line 2254 of file internal.h.

18.119.2.20 byte haveStaticECC

Definition at line 2259 of file internal.h.

18.119.2.21 void* heap

Definition at line 2243 of file internal.h.

18.119.2.22 WOLFSSL_METHOD* method

Definition at line 2209 of file internal.h.

18.119.2.23 word16 minDhKeySz

Definition at line 2282 of file internal.h.

18.119.2.24 byte minDowngrade

Definition at line 2263 of file internal.h.

18.119.2.25 short minRsaKeySz

Definition at line 2285 of file internal.h.

18.119.2.26 byte partialWrite

Definition at line 2260 of file internal.h.

18.119.2.27 DerBuffer* privateKey

Definition at line 2233 of file internal.h.

18.119.2.28 int privateKeySz

Definition at line 2235 of file internal.h.

18.119.2.29 byte privateKeyType

Definition at line 2234 of file internal.h.

18.119.2.30 byte quietShutdown

Definition at line 2261 of file internal.h.

18.119.2.31 int refCount

Definition at line 2214 of file internal.h.

18.119.2.32 byte sendVerify

Definition at line 2253 of file internal.h.

18.119.2.33 char server_hint[MAX_PSK_ID_LEN+NULL_TERM_LEN]

Definition at line 2318 of file internal.h.

18.119.2.34 wc_psk_server_callback server_psk_cb

Definition at line 2317 of file internal.h.

18.119.2.35 buffer serverDH_G

Definition at line 2218 of file internal.h.

18.119.2.36 buffer serverDH_P

Definition at line 2217 of file internal.h.

18.119.2.37 byte sessionCacheFlushOff

Definition at line 2249 of file internal.h.

18.119.2.38 byte sessionCacheOff

Definition at line 2248 of file internal.h.

18.119.2.39 Suites* suites

Definition at line 2242 of file internal.h.

18.119.2.40 word32 timeout

Definition at line 2306 of file internal.h.

18.119.2.41 byte useClientOrder

Definition at line 2265 of file internal.h.

18.119.2.42 VerifyCallback verifyCallback

Definition at line 2305 of file internal.h.

18.119.2.43 byte verifyNone

Definition at line 2245 of file internal.h.

18.119.2.44 byte verifyPeer

Definition at line 2244 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.120 WOLFSSL_DH Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/dh.h>
```

Data Fields

- [WOLFSSL_BIGNUM](#) * [p](#)
- [WOLFSSL_BIGNUM](#) * [g](#)
- [WOLFSSL_BIGNUM](#) * [q](#)
- [WOLFSSL_BIGNUM](#) * [pub_key](#)
- [WOLFSSL_BIGNUM](#) * [priv_key](#)
- void * [internal](#)
- char [inSet](#)
- char [exSet](#)
- int [length](#)

18.120.1 Detailed Description

Definition at line 14 of file dh.h.

18.120.2 Field Documentation**18.120.2.1 char exSet**

Definition at line 22 of file dh.h.

18.120.2.2 WOLFSSL_BIGNUM* g

Definition at line 16 of file dh.h.

18.120.2.3 char inSet

Definition at line 21 of file dh.h.

18.120.2.4 void* internal

Definition at line 20 of file dh.h.

18.120.2.5 int length

Definition at line 26 of file dh.h.

18.120.2.6 WOLFSSL_BIGNUM* p

Definition at line 15 of file dh.h.

18.120.2.7 WOLFSSL_BIGNUM* priv_key

Definition at line 19 of file dh.h.

18.120.2.8 WOLFSSL_BIGNUM* pub_key

Definition at line 18 of file dh.h.

18.120.2.9 WOLFSSL_BIGNUM* q

Definition at line 17 of file dh.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/dh.h

18.121 WOLFSSL_DSA Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/dsa.h>
```

Data Fields

- [WOLFSSL_BIGNUM](#) * [p](#)
- [WOLFSSL_BIGNUM](#) * [q](#)
- [WOLFSSL_BIGNUM](#) * [g](#)
- [WOLFSSL_BIGNUM](#) * [pub_key](#)
- [WOLFSSL_BIGNUM](#) * [priv_key](#)
- void * [internal](#)
- char [inSet](#)
- char [exSet](#)

18.121.1 Detailed Description

Definition at line 20 of file dsa.h.

18.121.2 Field Documentation**18.121.2.1 char exSet**

Definition at line 28 of file dsa.h.

18.121.2.2 WOLFSSL_BIGNUM* g

Definition at line 23 of file dsa.h.

18.121.2.3 char inSet

Definition at line 27 of file dsa.h.

18.121.2.4 void* internal

Definition at line 26 of file dsa.h.

18.121.2.5 WOLFSSL_BIGNUM* p

Definition at line 21 of file dsa.h.

18.121.2.6 WOLFSSL_BIGNUM* priv_key

Definition at line 25 of file dsa.h.

18.121.2.7 WOLFSSL_BIGNUM* pub_key

Definition at line 24 of file dsa.h.

18.121.2.8 WOLFSSL_BIGNUM* q

Definition at line 22 of file dsa.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/dsa.h

18.122 WOLFSSL_DTLS_CTX Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [WOLFSSL_SOCKADDR peer](#)
- int [rfd](#)
- int [wfd](#)

18.122.1 Detailed Description

Definition at line 1738 of file internal.h.

18.122.2 Field Documentation

18.122.2.1 WOLFSSL_SOCKADDR peer

Definition at line 1739 of file internal.h.

18.122.2.2 int rfd

Definition at line 1740 of file internal.h.

18.122.2.3 int wfd

Definition at line 1741 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.123 WOLFSSL_DTLS_PEERSEQ Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- word32 [window](#) [WOLFSSL_DTLS_WINDOW_WORDS]
- word16 [nextEpoch](#)

- word16 [nextSeq_hi](#)
- word32 [nextSeq_lo](#)
- word32 [prevWindow](#) [WOLFSSL_DTLS_WINDOW_WORDS]
- word32 [prevSeq_lo](#)
- word16 [prevSeq_hi](#)

18.123.1 Detailed Description

Definition at line 1745 of file internal.h.

18.123.2 Field Documentation

18.123.2.1 word16 nextEpoch

Definition at line 1748 of file internal.h.

18.123.2.2 word16 nextSeq_hi

Definition at line 1749 of file internal.h.

18.123.2.3 word32 nextSeq_lo

Definition at line 1750 of file internal.h.

18.123.2.4 word16 prevSeq_hi

Definition at line 1755 of file internal.h.

18.123.2.5 word32 prevSeq_lo

Definition at line 1754 of file internal.h.

18.123.2.6 word32 prevWindow[WOLFSSL_DTLS_WINDOW_WORDS]

Definition at line 1752 of file internal.h.

18.123.2.7 word32 window[WOLFSSL_DTLS_WINDOW_WORDS]

Definition at line 1746 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.124 WOLFSSL_EC_GROUP Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/ec.h>
```

Data Fields

- int [curve_idx](#)
- int [curve_nid](#)
- int [curve_oid](#)

18.124.1 Detailed Description

Definition at line 67 of file ec.h.

18.124.2 Field Documentation

18.124.2.1 int curve_idx

Definition at line 68 of file ec.h.

18.124.2.2 int curve_nid

Definition at line 69 of file ec.h.

18.124.2.3 int curve_oid

Definition at line 70 of file ec.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/ec.h

18.125 WOLFSSL_EC_KEY Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/ec.h>
```

Data Fields

- [WOLFSSL_EC_GROUP](#) * group
- [WOLFSSL_EC_POINT](#) * pub_key
- [WOLFSSL_BIGNUM](#) * priv_key
- void * internal
- char inSet
- char exSet

18.125.1 Detailed Description

Definition at line 73 of file ec.h.

18.125.2 Field Documentation

18.125.2.1 char exSet

Definition at line 80 of file ec.h.

18.125.2.2 WOLFSSL_EC_GROUP* group

Definition at line 74 of file ec.h.

18.125.2.3 char inSet

Definition at line 79 of file ec.h.

18.125.2.4 void* internal

Definition at line 78 of file ec.h.

18.125.2.5 WOLFSSL_BIGNUM* priv_key

Definition at line 76 of file ec.h.

18.125.2.6 WOLFSSL_EC_POINT* pub_key

Definition at line 75 of file ec.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/ec.h

18.126 WOLFSSL_EC_POINT Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/ec.h>
```

Data Fields

- [WOLFSSL_BIGNUM * X](#)
- [WOLFSSL_BIGNUM * Y](#)
- [WOLFSSL_BIGNUM * Z](#)
- void * [internal](#)
- char [inSet](#)
- char [exSet](#)

18.126.1 Detailed Description

Definition at line 57 of file ec.h.

18.126.2 Field Documentation

18.126.2.1 char exSet

Definition at line 64 of file ec.h.

18.126.2.2 char inSet

Definition at line 63 of file ec.h.

18.126.2.3 void* internal

Definition at line 62 of file ec.h.

18.126.2.4 WOLFSSL_BIGNUM* X

Definition at line 58 of file ec.h.

18.126.2.5 WOLFSSL_BIGNUM* Y

Definition at line 59 of file ec.h.

18.126.2.6 WOLFSSL_BIGNUM* Z

Definition at line 60 of file ec.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/ec.h

18.127 WOLFSSL_ECDSA_SIG Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/ecdsa.h>
```

Data Fields

- [WOLFSSL_BIGNUM](#) * *r*
- [WOLFSSL_BIGNUM](#) * *s*

18.127.1 Detailed Description

Definition at line 20 of file `ecdsa.h`.

18.127.2 Field Documentation

18.127.2.1 WOLFSSL_BIGNUM* *r*

Definition at line 21 of file `ecdsa.h`.

18.127.2.2 WOLFSSL_BIGNUM* *s*

Definition at line 22 of file `ecdsa.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/openssl/ecdsa.h`

18.128 WOLFSSL_EVP_CIPHER_CTX Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/evp.h>
```

Data Fields

- int [keyLen](#)
- int [block_size](#)
- unsigned long [flags](#)
- unsigned char [enc](#)
- unsigned char [cipherType](#)
- ALIGN16 unsigned char [iv](#) [AES_BLOCK_SIZE]
- [WOLFSSL_Cipher](#) [cipher](#)
- ALIGN16 byte [buf](#) [WOLFSSL_EVP_BUF_SIZE]
- int [bufUsed](#)
- ALIGN16 byte [lastBlock](#) [WOLFSSL_EVP_BUF_SIZE]
- int [lastUsed](#)

18.128.1 Detailed Description

Definition at line 157 of file `evp.h`.

18.128.2 Field Documentation

18.128.2.1 int [block_size](#)

Definition at line 159 of file `evp.h`.

18.128.2.2 ALIGN16 byte buf[WOLFSSL_EVP_BUF_SIZE]

Definition at line 171 of file evp.h.

18.128.2.3 int bufUsed

Definition at line 172 of file evp.h.

18.128.2.4 WOLFSSL_Cipher cipher

Definition at line 170 of file evp.h.

18.128.2.5 unsigned char cipherType

Definition at line 162 of file evp.h.

18.128.2.6 unsigned char enc

Definition at line 161 of file evp.h.

18.128.2.7 unsigned long flags

Definition at line 160 of file evp.h.

18.128.2.8 ALIGN16 unsigned char iv[AES_BLOCK_SIZE]

Definition at line 165 of file evp.h.

18.128.2.9 int keyLen

Definition at line 158 of file evp.h.

18.128.2.10 ALIGN16 byte lastBlock[WOLFSSL_EVP_BUF_SIZE]

Definition at line 173 of file evp.h.

18.128.2.11 int lastUsed

Definition at line 174 of file evp.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/openssl/evp.h`

18.129 WOLFSSL_EVP_MD_CTX Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/evp.h>
```

Data Fields

- [WOLFSSL_Hasher hash](#)
- unsigned char [macType](#)

18.129.1 Detailed Description

Definition at line 110 of file evp.h.

18.129.2 Field Documentation

18.129.2.1 WOLFSSL_Hasher hash

Definition at line 111 of file evp.h.

18.129.2.2 unsigned char macType

Definition at line 112 of file evp.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/evp.h

18.130 WOLFSSL_EVP_PKEY Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/evp.h>
```

Data Fields

- int [type](#)
- int [save_type](#)
- int [pkey_sz](#)
- union {
 char * [ptr](#)
} [pkey](#)

18.130.1 Detailed Description

Definition at line 183 of file evp.h.

18.130.2 Field Documentation

18.130.2.1 union { ... } pkey

18.130.2.2 int pkey_sz

Definition at line 186 of file evp.h.

18.130.2.3 char* ptr

Definition at line 188 of file evp.h.

18.130.2.4 int save_type

Definition at line 185 of file evp.h.

18.130.2.5 int type

Definition at line 184 of file evp.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/evp.h

18.131 WOLFSSL_Hasher Union Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/evp.h>
```

Data Fields

- [WOLFSSL_MD5_CTX md5](#)
- [WOLFSSL_SHA_CTX sha](#)
- [WOLFSSL_SHA256_CTX sha256](#)

18.131.1 Detailed Description

Definition at line 89 of file evp.h.

18.131.2 Field Documentation

18.131.2.1 WOLFSSL_MD5_CTX md5

Definition at line 91 of file evp.h.

18.131.2.2 WOLFSSL_SHA_CTX sha

Definition at line 93 of file evp.h.

18.131.2.3 WOLFSSL_SHA256_CTX sha256

Definition at line 97 of file evp.h.

The documentation for this union was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/openssl/evp.h`

18.132 WOLFSSL_HMAC_CTX Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/hmac.h>
```

Data Fields

- [Hmac hmac](#)
- [int type](#)

18.132.1 Detailed Description

Definition at line 52 of file hmac.h.

18.132.2 Field Documentation

18.132.2.1 Hmac hmac

Definition at line 53 of file hmac.h.

18.132.2.2 int type

Definition at line 54 of file hmac.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/openssl/hmac.h`

18.133 WOLFSSL_MD4_CTX Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- int [buffer](#) [32]

18.133.1 Detailed Description

Definition at line 164 of file ssl.h.

18.133.2 Field Documentation

18.133.2.1 int [buffer](#)[32]

Definition at line 165 of file ssl.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/ssl.h

18.134 WOLFSSL_MD5_CTX Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/md5.h>
```

Data Fields

- int [holder](#) [28+(WC_ASYNC_DEV_SIZE/sizeof(int))]

18.134.1 Detailed Description

Definition at line 20 of file md5.h.

18.134.2 Field Documentation

18.134.2.1 int [holder](#)[28+(WC_ASYNC_DEV_SIZE/sizeof(int))]

Definition at line 21 of file md5.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/md5.h

18.135 WOLFSSL_METHOD Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [ProtocolVersion](#) [version](#)
- byte [side](#)
- byte [downgrade](#)

18.135.1 Detailed Description

Definition at line 1383 of file internal.h.

18.135.2 Field Documentation

18.135.2.1 byte downgrade

Definition at line 1386 of file internal.h.

18.135.2.2 byte side

Definition at line 1385 of file internal.h.

18.135.2.3 ProtocolVersion version

Definition at line 1384 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.136 WOLFSSL_OCSP Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [WOLFSSL_CERT_MANAGER](#) * cm
- [OcsEntry](#) * ocsplist
- wolfSSL_Mutex [ocspLock](#)

18.136.1 Detailed Description

Definition at line 1592 of file internal.h.

18.136.2 Field Documentation

18.136.2.1 WOLFSSL_CERT_MANAGER* cm

Definition at line 1593 of file internal.h.

18.136.2.2 OcsEntry* ocsplist

Definition at line 1594 of file internal.h.

18.136.2.3 wolfSSL_Mutex ocspLock

Definition at line 1595 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.137 WOLFSSL_RIPEMD_CTX Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/ripemd.h>
```

Data Fields

- int [holder](#) [32]

18.137.1 Detailed Description

Definition at line 14 of file ripemd.h.

18.137.2 Field Documentation

18.137.2.1 int holder[32]

Definition at line 15 of file ripemd.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/ripemd.h

18.138 WOLFSSL_RSA Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/rsa.h>
```

Data Fields

- WOLFSSL_BIGNUM * [n](#)
- WOLFSSL_BIGNUM * [e](#)
- WOLFSSL_BIGNUM * [d](#)
- WOLFSSL_BIGNUM * [p](#)
- WOLFSSL_BIGNUM * [q](#)
- WOLFSSL_BIGNUM * [dmp1](#)
- WOLFSSL_BIGNUM * [dmq1](#)
- WOLFSSL_BIGNUM * [iqmp](#)
- void * [internal](#)
- char [inSet](#)
- char [exSet](#)

18.138.1 Detailed Description

Definition at line 33 of file rsa.h.

18.138.2 Field Documentation

18.138.2.1 WOLFSSL_BIGNUM* d

Definition at line 36 of file rsa.h.

18.138.2.2 WOLFSSL_BIGNUM* dmp1

Definition at line 39 of file rsa.h.

18.138.2.3 WOLFSSL_BIGNUM* dmq1

Definition at line 40 of file rsa.h.

18.138.2.4 WOLFSSL_BIGNUM* e

Definition at line 35 of file rsa.h.

18.138.2.5 char exSet

Definition at line 44 of file rsa.h.

18.138.2.6 char inSet

Definition at line 43 of file rsa.h.

18.138.2.7 void* internal

Definition at line 42 of file rsa.h.

18.138.2.8 WOLFSSL_BIGNUM* iqmp

Definition at line 41 of file rsa.h.

18.138.2.9 WOLFSSL_BIGNUM* n

Definition at line 34 of file rsa.h.

18.138.2.10 WOLFSSL_BIGNUM* p

Definition at line 37 of file rsa.h.

18.138.2.11 WOLFSSL_BIGNUM* q

Definition at line 38 of file rsa.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/rsa.h

18.139 WOLFSSL_SESSION Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- word32 [bornOn](#)
- word32 [timeout](#)
- byte [sessionID](#) [ID_LEN]
- byte [sessionIDSz](#)
- byte [masterSecret](#) [SECRET_LEN]
- word16 [haveEMS](#)
- word16 [idLen](#)
- byte [serverID](#) [SERVER_ID_LEN]
- byte * [ticket](#)
- word16 [ticketLen](#)
- byte [staticTicket](#) [SESSION_TICKET_LEN]
- byte [isDynamic](#)

18.139.1 Detailed Description

Definition at line 2634 of file internal.h.

18.139.2 Field Documentation

18.139.2.1 word32 bornOn

Definition at line 2635 of file internal.h.

18.139.2.2 word16 haveEMS

Definition at line 2640 of file internal.h.

18.139.2.3 word16 idLen

Definition at line 2651 of file internal.h.

18.139.2.4 byte isDynamic

Definition at line 2666 of file internal.h.

18.139.2.5 byte masterSecret[SECRET_LEN]

Definition at line 2639 of file internal.h.

18.139.2.6 byte serverID[SERVER_ID_LEN]

Definition at line 2652 of file internal.h.

18.139.2.7 byte sessionID[ID_LEN]

Definition at line 2637 of file internal.h.

18.139.2.8 byte sessionIDSz

Definition at line 2638 of file internal.h.

18.139.2.9 byte staticTicket[SESSION_TICKET_LEN]

Definition at line 2665 of file internal.h.

18.139.2.10 byte* ticket

Definition at line 2663 of file internal.h.

18.139.2.11 word16 ticketLen

Definition at line 2664 of file internal.h.

18.139.2.12 word32 timeout

Definition at line 2636 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.140 WOLFSSL_SHA256_CTX Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/sha.h>
```

Data Fields

- ALIGN16 int [holder](#) [34+(WC_ASYNC_DEV_SIZE/sizeof(int))]

18.140.1 Detailed Description

Definition at line 81 of file sha.h.

18.140.2 Field Documentation

18.140.2.1 ALIGN16 int holder[34+(WC_ASYNC_DEV_SIZE/sizeof(int))]

Definition at line 83 of file sha.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/sha.h

18.141 WOLFSSL_SHA_CTX Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/openssl/sha.h>
```

Data Fields

- int [holder](#) [28+(WC_ASYNC_DEV_SIZE/sizeof(int))]

18.141.1 Detailed Description

Definition at line 19 of file sha.h.

18.141.2 Field Documentation

18.141.2.1 int holder[28+(WC_ASYNC_DEV_SIZE/sizeof(int))]

Definition at line 21 of file sha.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/openssl/sha.h

18.142 WOLFSSL_SOCKETADDR Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- unsigned int [sz](#)
- void * [sa](#)

18.142.1 Detailed Description

Definition at line 1733 of file internal.h.

18.142.2 Field Documentation

18.142.2.1 void* sa

Definition at line 1735 of file internal.h.

18.142.2.2 unsigned int sz

Definition at line 1734 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.143 WOLFSSL_STACK Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- unsigned long [num](#)
- union {
 - [WOLFSSL_X509 * x509](#)
 - [WOLFSSL_X509_NAME * name](#)
 - [WOLFSSL_BIO * bio](#)
 - [WOLFSSL_ASN1_OBJECT * obj](#)
 - char * [string](#)
- [WOLFSSL_STACK * next](#)

18.143.1 Detailed Description

Definition at line 2972 of file internal.h.

18.143.2 Field Documentation

18.143.2.1 WOLFSSL_BIO* bio

Definition at line 2978 of file internal.h.

18.143.2.2 union { ... } data

18.143.2.3 WOLFSSL_X509_NAME* name

Definition at line 2977 of file internal.h.

18.143.2.4 WOLFSSL_STACK* next

Definition at line 2982 of file internal.h.

18.143.2.5 unsigned long num

Definition at line 2973 of file internal.h.

18.143.2.6 WOLFSSL_ASN1_OBJECT* obj

Definition at line 2979 of file internal.h.

18.143.2.7 char* string

Definition at line 2980 of file internal.h.

18.143.2.8 WOLFSSL_X509* x509

Definition at line 2976 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.144 wolfssl_TI_Hash Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/wolfcrypt/port/ti/ti-hash.h>
```

Data Fields

- byte * [msg](#)
- word32 [used](#)
- word32 [len](#)
- byte [hash](#) [WOLFSSL_MAX_HASH_SIZE]

18.144.1 Detailed Description

Definition at line 36 of file ti-hash.h.

18.144.2 Field Documentation

18.144.2.1 byte hash[WOLFSSL_MAX_HASH_SIZE]

Definition at line 40 of file ti-hash.h.

18.144.2.2 word32 len

Definition at line 39 of file ti-hash.h.

18.144.2.3 byte* msg

Definition at line 37 of file ti-hash.h.

18.144.2.4 word32 used

Definition at line 38 of file ti-hash.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/wolfcrypt/port/ti/ti-hash.h

18.145 WOLFSSL_X509 Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- int [version](#)
- [WOLFSSL_X509_NAME issuer](#)
- [WOLFSSL_X509_NAME subject](#)
- int [serialSz](#)
- byte [serial](#) [EXTERNAL_SERIAL_SIZE]
- char [subjectCN](#) [ASN_NAME_MAX]
- int [notBeforeSz](#)
- byte [notBefore](#) [MAX_DATE_SZ]
- int [notAfterSz](#)
- byte [notAfter](#) [MAX_DATE_SZ]
- int [sigOID](#)
- [buffer sig](#)
- int [pubKeyOID](#)
- [buffer pubKey](#)
- [DerBuffer * derCert](#)
- [DNS_entry * altNames](#)
- [DNS_entry * altNamesNext](#)
- void * [heap](#)
- byte [dynamicMemory](#)
- byte [isCa](#)

18.145.1 Detailed Description

Definition at line 3010 of file internal.h.

18.145.2 Field Documentation

18.145.2.1 [DNS_entry* altNames](#)

Definition at line 3043 of file internal.h.

18.145.2.2 [DNS_entry* altNamesNext](#)

Definition at line 3044 of file internal.h.

18.145.2.3 [DerBuffer* derCert](#)

Definition at line 3041 of file internal.h.

18.145.2.4 [byte dynamicMemory](#)

Definition at line 3046 of file internal.h.

18.145.2.5 [void* heap](#)

Definition at line 3045 of file internal.h.

18.145.2.6 [byte isCa](#)

Definition at line 3047 of file internal.h.

18.145.2.7 WOLFSSL_X509_NAME issuer

Definition at line 3012 of file internal.h.

18.145.2.8 byte notAfter[MAX_DATE_SZ]

Definition at line 3032 of file internal.h.

18.145.2.9 int notAfterSz

Definition at line 3031 of file internal.h.

18.145.2.10 byte notBefore[MAX_DATE_SZ]

Definition at line 3030 of file internal.h.

18.145.2.11 int notBeforeSz

Definition at line 3029 of file internal.h.

18.145.2.12 buffer pubKey

Definition at line 3036 of file internal.h.

18.145.2.13 int pubKeyOID

Definition at line 3035 of file internal.h.

18.145.2.14 byte serial[EXTERNAL_SERIAL_SIZE]

Definition at line 3015 of file internal.h.

18.145.2.15 int serialSz

Definition at line 3014 of file internal.h.

18.145.2.16 buffer sig

Definition at line 3034 of file internal.h.

18.145.2.17 int sigOID

Definition at line 3033 of file internal.h.

18.145.2.18 WOLFSSL_X509_NAME subject

Definition at line 3013 of file internal.h.

18.145.2.19 char subjectCN[ASN_NAME_MAX]

Definition at line 3016 of file internal.h.

18.145.2.20 int version

Definition at line 3011 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.146 WOLFSSL_X509_CHAIN Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- [int count](#)
- [x509_buffer certs](#) [MAX_CHAIN_DEPTH]

18.146.1 Detailed Description

Definition at line 2627 of file internal.h.

18.146.2 Field Documentation

18.146.2.1 [x509_buffer certs](#)[MAX_CHAIN_DEPTH]

Definition at line 2629 of file internal.h.

18.146.2.2 [int count](#)

Definition at line 2628 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.147 WOLFSSL_X509_LOOKUP Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- [WOLFSSL_X509_STORE](#) * store

18.147.1 Detailed Description

Definition at line 177 of file ssl.h.

18.147.2 Field Documentation

18.147.2.1 [WOLFSSL_X509_STORE](#)* store

Definition at line 178 of file ssl.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/ssl.h

18.148 WOLFSSL_X509_LOOKUP_METHOD Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- int [type](#)

18.148.1 Detailed Description

Definition at line 173 of file ssl.h.

18.148.2 Field Documentation

18.148.2.1 int type

Definition at line 174 of file ssl.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/ssl.h

18.149 WOLFSSL_X509_NAME Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- char * [name](#)
- char [staticName](#) [ASN_NAME_MAX]
- int [dynamicName](#)
- int [sz](#)

18.149.1 Detailed Description

Definition at line 2986 of file internal.h.

18.149.2 Field Documentation

18.149.2.1 int dynamicName

Definition at line 2989 of file internal.h.

18.149.2.2 char* name

Definition at line 2987 of file internal.h.

18.149.2.3 char staticName[ASN_NAME_MAX]

Definition at line 2988 of file internal.h.

18.149.2.4 int sz

Definition at line 2990 of file internal.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/internal.h

18.150 WOLFSSL_X509_OBJECT Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- union {
 - char * ptr
 - WOLFSSL_X509 * x509
 - WOLFSSL_X509_CRL * crl
- } data

18.150.1 Detailed Description

Definition at line 205 of file ssl.h.

18.150.2 Field Documentation

18.150.2.1 WOLFSSL_X509_CRL* crl

Definition at line 209 of file ssl.h.

18.150.2.2 union { ... } data

18.150.2.3 char* ptr

Definition at line 207 of file ssl.h.

18.150.2.4 WOLFSSL_X509* x509

Definition at line 208 of file ssl.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/ssl.h

18.151 WOLFSSL_X509_REVOKED Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- WOLFSSL_ASN1_INTEGER * serialNumber

18.151.1 Detailed Description

Definition at line 200 of file ssl.h.

18.151.2 Field Documentation

18.151.2.1 WOLFSSL_ASN1_INTEGER* serialNumber

Definition at line 201 of file ssl.h.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/ssl.h`

18.152 WOLFSSL_X509_STORE Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- `int` `cache`
- `WOLFSSL_CERT_MANAGER *` `cm`
- `WOLFSSL_X509_LOOKUP` `lookup`

18.152.1 Detailed Description

Definition at line 181 of file `ssl.h`.

18.152.2 Field Documentation

18.152.2.1 `int` `cache`

Definition at line 182 of file `ssl.h`.

18.152.2.2 `WOLFSSL_CERT_MANAGER *` `cm`

Definition at line 183 of file `ssl.h`.

18.152.2.3 `WOLFSSL_X509_LOOKUP` `lookup`

Definition at line 184 of file `ssl.h`.

The documentation for this struct was generated from the following file:

- `middleware/tcpip/wolfssl/wolfssl/ssl.h`

18.153 WOLFSSL_X509_STORE_CTX Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/ssl.h>
```

Data Fields

- `WOLFSSL_X509_STORE *` `store`
- `WOLFSSL_X509 *` `current_cert`
- `WOLFSSL_STACK *` `chain`
- `char *` `domain`
- `void *` `ex_data`
- `void *` `userCtx`
- `int` `error`
- `int` `error_depth`
- `int` `discardSessionCerts`
- `int` `totalCerts`
- `WOLFSSL_BUFFER_INFO *` `certs`

18.153.1 Detailed Description

Definition at line 218 of file ssl.h.

18.153.2 Field Documentation

18.153.2.1 WOLFSSL_BUFFER_INFO* certs

Definition at line 229 of file ssl.h.

18.153.2.2 WOLFSSL_STACK* chain

Definition at line 221 of file ssl.h.

18.153.2.3 WOLFSSL_X509* current_cert

Definition at line 220 of file ssl.h.

18.153.2.4 int discardSessionCerts

Definition at line 227 of file ssl.h.

18.153.2.5 char* domain

Definition at line 222 of file ssl.h.

18.153.2.6 int error

Definition at line 225 of file ssl.h.

18.153.2.7 int error_depth

Definition at line 226 of file ssl.h.

18.153.2.8 void* ex_data

Definition at line 223 of file ssl.h.

18.153.2.9 WOLFSSL_X509_STORE* store

Definition at line 219 of file ssl.h.

18.153.2.10 int totalCerts

Definition at line 228 of file ssl.h.

18.153.2.11 void* userCtx

Definition at line 224 of file ssl.h.

The documentation for this struct was generated from the following file:

- middleware/tcpip/wolfssl/wolfssl/ssl.h

18.154 x509_buffer Struct Reference

```
#include <middleware/tcpip/wolfssl/wolfssl/internal.h>
```

Data Fields

- int [length](#)
- byte [buffer](#) [MAX_X509_SIZE]

18.154.1 Detailed Description

Definition at line 2620 of file internal.h.

18.154.2 Field Documentation**18.154.2.1 byte [buffer](#)[MAX_X509_SIZE]**

Definition at line 2622 of file internal.h.

18.154.2.2 int [length](#)

Definition at line 2621 of file internal.h.

The documentation for this struct was generated from the following file:

- [middleware/tcpip/wolfssl/wolfssl/internal.h](#)

Index

- __blake2b_param, 1243
 - depth, 1243
 - digest_length, 1243
 - fanout, 1243
 - inner_length, 1243
 - key_length, 1243
 - leaf_length, 1243
 - node_depth, 1243
 - node_offset, 1243
 - personal, 1243
 - reserved, 1244
 - salt, 1244
- __blake2bp_state, 1244
 - buf, 1244
 - buflen, 1244
 - R, 1244
 - S, 1244
- __blake2s_param, 1244
 - depth, 1245
 - digest_length, 1245
 - fanout, 1245
 - inner_length, 1245
 - key_length, 1245
 - leaf_length, 1245
 - node_depth, 1245
 - node_offset, 1245
 - personal, 1245
 - salt, 1245
- __blake2sp_state, 1246
 - buf, 1246
 - buflen, 1246
 - R, 1246
 - S, 1246
- 00. Library internals, 178
 - g_drivers, 188
 - UJA1131HW3V3, 186
 - UJA1131HW5V0, 186
 - UJA1131HWFD3V0, 187
 - UJA1131HWFD3V4, 187
 - UJA1131HWFD5V0, 187
 - UJA1131HWFD5V4, 187
 - UJA1132HW3V3, 186
 - UJA1132HW5V0, 186
 - UJA1132HWFD3V0, 187
 - UJA1132HWFD3V4, 187
 - UJA1132HWFD5V0, 187
 - UJA1132HWFD5V4, 187
 - UJA1135HW3V3, 186
 - UJA1135HW5V0, 186
 - UJA1136HW3V3, 186
 - UJA1136HW5V0, 186
 - UJA113X_Init, 187
 - UJA113X_RegisterDevice, 187
 - UJA113X_SbcTransfer, 187
 - uja113x_chip_t, 186
- 01. CAN & CAN partial networking configuration, 189
 - CDR_DATA_RATE_100, 195
 - CDR_DATA_RATE_1000, 195
 - CDR_DATA_RATE_125, 195
 - CDR_DATA_RATE_250, 195
 - CDR_DATA_RATE_50, 195
 - CDR_DATA_RATE_500a, 195
 - CDR_DATA_RATE_500b, 195
 - CDR_DATA_RATE_500c, 195
 - CMC_TRANSCEIVER_ACTIVE, 194
 - CMC_TRANSCEIVER_ACTIVE2, 194
 - CMC_TRANSCEIVER_LISTEN, 194
 - CMC_TRANSCEIVER_OFF, 194
 - CSC_NONE, 194
 - CSC_OVERVOLTAGE, 194
 - CSC_UNDRV_OVERV, 194
 - CSC_UNDRVOLTAGE, 194
 - DLC_0, 195
 - DLC_1, 195
 - DLC_2, 195
 - DLC_3, 195
 - DLC_4, 195
 - DLC_5, 195
 - DLC_6, 195
 - DLC_7, 195
 - DLC_8, 195
 - UJA113X_SetCan, 195
 - UJA113X_SetCanPartNet, 196
 - UJA113X_SetDataMasks, 196
 - uja113x_canc_cfdc_t, 193
 - uja113x_canc_cmc_t, 194
 - uja113x_canc_cpnc_t, 193
 - uja113x_canc_csc_t, 194
 - uja113x_dr_cdr_t, 194
 - uja113x_fc_dlc_t, 195
 - uja113x_fc_ide_t, 193
 - uja113x_fc_pndm_t, 193
 - uja113x_id_id_t, 194
 - uja113x_idm_idm_t, 194
- 01. Mode handling, 198
 - MC_NORMAL, 198
 - MC_SLEEP, 198
 - MC_STANDBY, 198
 - UJA113X_SetMode, 199
 - uja113x_mc_mc_t, 198
- 01. Primary control, 200
- 01. Regulator configuration, 201
 - UJA113X_SetRegulator, 203
 - uja113x_rc_v1rtc_t, 202
 - uja113x_rc_v2c_t, 202
 - uja113x_rc_v2sc_t, 202
 - V1RTC_60_NOMINAL_OUT, 202
 - V1RTC_70_NOMINAL_OUT, 202
 - V1RTC_80_NOMINAL_OUT, 202
 - V1RTC_90_NOMINAL_OUT, 202

- V2C_OFF, [202](#)
- V2C_ON_N, [202](#)
- V2C_ON_NSR, [202](#)
- V2C_ON_NSSRF, [202](#)
- V2SC_FULL, [203](#)
- V2SC_NONE, [202](#)
- V2SC_OVERVOLTAGE, [202](#)
- V2SC_UNDRVOLTAGE, [202](#)
- 02. Battery monitor configuration, [204](#)
 - IONOLTC_10_MA, [207](#)
 - IONOLTC_20_MA, [207](#)
 - IONOLTC_2_MA, [206](#)
 - IONOLTC_5_MA, [206](#)
 - IONSCTC_30_MA, [207](#)
 - IONSCTC_45_MA, [207](#)
 - IONSCTC_60_MA, [207](#)
 - IONSCTC_90_MA, [207](#)
 - UJA113X_SetBatteryMonitor, [207](#)
 - uja113x_bmetsc_bmsc_t, [206](#)
 - uja113x_bmhc_bmhc_t, [206](#)
 - uja113x_bmhc_bmhc_t, [206](#)
 - uja113x_bmotc_bmotc_t, [206](#)
 - uja113x_bmutc_bmutc_t, [206](#)
 - uja113x_boldt_ionoltc_t, [206](#)
 - uja113x_bscdt_ionsctc_t, [207](#)
- 02. LIN configuration, [208](#)
 - LMC1_TRANSCEIVER_LISTEN, [209](#)
 - LMC1_TRANSCEIVER_OFF, [209](#)
 - LMC1_TRANSCEIVER_ON, [209](#)
 - LMC1_TRANSCEIVER_ON2, [209](#)
 - LMC2_TRANSCEIVER_LISTEN, [210](#)
 - LMC2_TRANSCEIVER_OFF, [210](#)
 - LMC2_TRANSCEIVER_ON, [210](#)
 - LMC2_TRANSCEIVER_ON2, [210](#)
 - LSC1_SLOPE_ACTIVE, [210](#)
 - LSC1_SLOPE_ACTIVE2, [210](#)
 - LSC1_SLOPE_ACTIVE_TXDL_TIMEOUT, [210](#)
 - LSC2_SLOPE_ACTIVE, [210](#)
 - LSC2_SLOPE_ACTIVE2, [210](#)
 - LSC2_SLOPE_ACTIVE_TXDL_TIMEOUT, [210](#)
 - UJA113X_SetLin, [210](#)
 - uja113x_linc_lmc1_t, [209](#)
 - uja113x_linc_lmc2_t, [209](#)
 - uja113x_linc_lsc1_t, [210](#)
 - uja113x_linc_lsc2_t, [210](#)
- 02. Supply control, [212](#)
- 02. Watchdog, [213](#)
 - NWP_PERIOD_1024, [215](#)
 - NWP_PERIOD_128, [215](#)
 - NWP_PERIOD_16, [215](#)
 - NWP_PERIOD_256, [215](#)
 - NWP_PERIOD_32, [215](#)
 - NWP_PERIOD_4096, [215](#)
 - NWP_PERIOD_64, [215](#)
 - NWP_PERIOD_8, [215](#)
 - UJA113X_SetWatchdog, [215](#)
 - uja113x_wtdc_nwp_t, [214](#)
 - uja113x_wtdc_wmc_t, [215](#)
 - WMC_AUTONOMOUS, [215](#)
 - WMC_TIMEOUT, [215](#)
 - WMC_WINDOW, [215](#)
- 03. Fail-safe configuration, [217](#)
 - ENC_HIGH_N, [219](#)
 - ENC_HIGH_NRS, [219](#)
 - ENC_LOW, [219](#)
 - ENC_TIMER, [219](#)
 - ENSC_FULL, [219](#)
 - ENSC_NONE, [219](#)
 - ENSC_OVERVOLTAGE, [219](#)
 - ENSC_UNDRVOLTAGE, [219](#)
 - UJA113X_SetFailSafe, [220](#)
 - uja113x_fsc_enc_t, [219](#)
 - uja113x_fsc_endc_t, [219](#)
 - uja113x_fsc_ensc_t, [219](#)
 - uja113x_fsc_lhc_t, [219](#)
 - uja113x_fsc_rcc_t, [219](#)
- 03. SMPS configuration, [221](#)
 - SMPSC_ON_NSR, [222](#)
 - SMPSC_ON_NSRS, [222](#)
 - SMPSC_PASS_THROUGH_NSS, [222](#)
 - SMPSOC_50V, [222](#)
 - SMPSOC_52V, [222](#)
 - SMPSOC_54V, [222](#)
 - SMPSOC_56V, [222](#)
 - SMPSOC_58V, [223](#)
 - SMPSOC_60V, [223](#)
 - SMPSOC_62V, [223](#)
 - SMPSOC_64V, [223](#)
 - SMPSOC_66V, [223](#)
 - SMPSOC_68V, [223](#)
 - SMPSOC_70V, [223](#)
 - SMPSOC_72V, [223](#)
 - SMPSOC_74V, [223](#)
 - SMPSOC_76V, [223](#)
 - SMPSOC_78V, [223](#)
 - SMPSOC_80V, [223](#)
 - UJA113X_SetSmpls, [223](#)
 - uja113x_smpsc_smpsc_t, [222](#)
 - uja113x_smpsc_smpsotc_t, [222](#)
 - uja113x_smpsovc_smpsoc_t, [222](#)
- 03. Transceiver control, [224](#)
- 04. HVIO bank 0 & 1 control, [225](#)
 - IONAC_DEACTIVATED, [229](#)
 - IONAC_ENABLED, [229](#)
 - IONAC_HVIO, [229](#)
 - IONAC_HVIO_INV, [229](#)
 - IONAC_TMR_1, [229](#)
 - IONAC_TMR_2, [229](#)
 - IONAC_TMR_3, [229](#)
 - IONAC_TMR_4, [229](#)
 - IONCC_HS, [229](#)
 - IONCC_HS_SLOPE, [229](#)
 - IONCC_HS_WUP, [229](#)
 - IONCC_HS_WUP_SLOPE, [229](#)
 - IONCC_LS, [229](#)
 - IONCC_LS_SLOPE, [229](#)

- IONCC_OFF, [229](#)
- IONCC_WUP, [229](#)
- IONSC_FULL, [229](#)
- IONSC_NONE, [229](#)
- IONSC_OVERVOLTAGE, [229](#)
- IONSC_UNDRVOLTAGE, [229](#)
- UJA113X_SetBankOpenLoadThr, [229](#)
- UJA113X_SetBankShortCircThr, [230](#)
- UJA113X_SetBankWupThr, [230](#)
- UJA113X_SetHvio, [231](#)
- uja113x_bwtc_bnwtc_t, [228](#)
- uja113x_hvion_ionac_t, [228](#)
- uja113x_hvion_ioncc_t, [229](#)
- uja113x_hvion_ionsc_t, [229](#)
- 04. Lock control, [232](#)
 - UJA113X_SetLock, [234](#)
 - uja113x_lkc_lkxc_t, [234](#)
- 05. Timer control, [235](#)
 - TXMC_PWM, [237](#)
 - TXMC_TIM, [237](#)
 - TXMC_TRIG_END, [237](#)
 - TXMC_TRIG_START, [237](#)
 - TXPC_1000MS_PERIOD, [237](#)
 - TXPC_100MS_PERIOD, [237](#)
 - TXPC_2000MS_PERIOD, [237](#)
 - TXPC_200MS_PERIOD, [237](#)
 - TXPC_20MS_PERIOD, [237](#)
 - TXPC_30MS_PERIOD, [237](#)
 - TXPC_4000MS_PERIOD, [237](#)
 - TXPC_400MS_PERIOD, [237](#)
 - TXPC_4MS_PERIOD, [237](#)
 - TXPC_50MS_PERIOD, [237](#)
 - TXPC_800MS_PERIOD, [237](#)
 - TXPC_8MS_PERIOD, [237](#)
 - UJA113X_SetTimer, [237](#)
 - uja113x_timxc_txmc_t, [236](#)
 - uja113x_timxc_txpc_t, [237](#)
 - uja113x_timxdcc_txdcc_t, [236](#)
- 06. Interrupts, [239](#)
 - UJA113X_SetBankFailInterrupts, [239](#)
 - UJA113X_SetBankWupInterrupts, [240](#)
 - UJA113X_SetSupplyInterrupts, [240](#)
 - UJA113X_SetSystemInterrupts, [241](#)
 - UJA113X_SetTransceiverInterrupts, [241](#)
- 07. MTPNV and ID, [243](#)
 - UJA113X_ComputeCrc8, [248](#)
 - UJA113X_SetMtpnv, [248](#)
- ADC Driver, [250](#)
 - ADC_AVERAGE_16, [259](#)
 - ADC_AVERAGE_32, [259](#)
 - ADC_AVERAGE_4, [259](#)
 - ADC_AVERAGE_8, [259](#)
 - ADC_CLK_ALT_1, [259](#)
 - ADC_CLK_ALT_2, [259](#)
 - ADC_CLK_ALT_3, [259](#)
 - ADC_CLK_ALT_4, [259](#)
 - ADC_CLK_DIVIDE_1, [259](#)
 - ADC_CLK_DIVIDE_2, [259](#)
 - ADC_CLK_DIVIDE_4, [259](#)
 - ADC_CLK_DIVIDE_8, [259](#)
 - ADC_DRV_AutoCalibration, [262](#)
 - ADC_DRV_ClearLatchedTriggers, [262](#)
 - ADC_DRV_ClearTriggerErrors, [262](#)
 - ADC_DRV_ConfigChan, [262](#)
 - ADC_DRV_ConfigConverter, [263](#)
 - ADC_DRV_ConfigHwAverage, [263](#)
 - ADC_DRV_ConfigHwCompare, [263](#)
 - ADC_DRV_ConfigUserCalibration, [263](#)
 - ADC_DRV_GetChanConfig, [263](#)
 - ADC_DRV_GetChanResult, [264](#)
 - ADC_DRV_GetConvCompleteFlag, [264](#)
 - ADC_DRV_GetConverterConfig, [264](#)
 - ADC_DRV_GetHwAverageConfig, [264](#)
 - ADC_DRV_GetHwCompareConfig, [265](#)
 - ADC_DRV_GetInterruptNumber, [265](#)
 - ADC_DRV_GetTriggerErrorFlags, [265](#)
 - ADC_DRV_GetUserCalibration, [265](#)
 - ADC_DRV_InitChanStruct, [265](#)
 - ADC_DRV_InitConverterStruct, [266](#)
 - ADC_DRV_InitHwAverageStruct, [266](#)
 - ADC_DRV_InitHwCompareStruct, [266](#)
 - ADC_DRV_InitUserCalibrationStruct, [266](#)
 - ADC_DRV_Reset, [267](#)
 - ADC_DRV_SetSwPretrigger, [267](#)
 - ADC_DRV_WaitConvDone, [267](#)
 - ADC_INPUTCHAN_BANDGAP, [260](#)
 - ADC_INPUTCHAN_DISABLED, [260](#)
 - ADC_INPUTCHAN_EXT0, [259](#)
 - ADC_INPUTCHAN_EXT1, [259](#)
 - ADC_INPUTCHAN_EXT10, [260](#)
 - ADC_INPUTCHAN_EXT11, [260](#)
 - ADC_INPUTCHAN_EXT12, [260](#)
 - ADC_INPUTCHAN_EXT13, [260](#)
 - ADC_INPUTCHAN_EXT14, [260](#)
 - ADC_INPUTCHAN_EXT3, [259](#)
 - ADC_INPUTCHAN_EXT4, [260](#)
 - ADC_INPUTCHAN_EXT5, [260](#)
 - ADC_INPUTCHAN_EXT6, [260](#)
 - ADC_INPUTCHAN_EXT7, [260](#)
 - ADC_INPUTCHAN_EXT9, [260](#)
 - ADC_INPUTCHAN_INT0, [260](#)
 - ADC_INPUTCHAN_INT1, [260](#)
 - ADC_INPUTCHAN_INT2, [260](#)
 - ADC_INPUTCHAN_INT3, [260](#)
 - ADC_INPUTCHAN_SUPPLY_VDD, [260](#)
 - ADC_INPUTCHAN_SUPPLY_VDD_3V, [260](#)
 - ADC_INPUTCHAN_SUPPLY_VDD_FLASH_3V, [260](#)
 - ADC_INPUTCHAN_SUPPLY_VDD_LV, [260](#)
 - ADC_INPUTCHAN_SUPPLY_VDDA, [260](#)
 - ADC_INPUTCHAN_SUPPLY_VREFH, [260](#)
 - ADC_INPUTCHAN_TEMP, [260](#)
 - ADC_INPUTCHAN_VREFSH, [260](#)
 - ADC_INPUTCHAN_VREFSL, [260](#)
 - ADC_LATCH_CLEAR_FORCE, [260](#)
 - ADC_LATCH_CLEAR_WAIT, [260](#)

- ADC_PRETRIGGER_SEL_PDB, [260](#)
- ADC_PRETRIGGER_SEL_SW, [260](#)
- ADC_PRETRIGGER_SEL_TRGMUX, [260](#)
- ADC_RESOLUTION_10BIT, [261](#)
- ADC_RESOLUTION_12BIT, [261](#)
- ADC_RESOLUTION_8BIT, [261](#)
- ADC_SW_PRETRIGGER_0, [261](#)
- ADC_SW_PRETRIGGER_1, [261](#)
- ADC_SW_PRETRIGGER_2, [261](#)
- ADC_SW_PRETRIGGER_3, [261](#)
- ADC_SW_PRETRIGGER_DISABLED, [261](#)
- ADC_TRIGGER_HARDWARE, [261](#)
- ADC_TRIGGER_SEL_PDB, [261](#)
- ADC_TRIGGER_SEL_TRGMUX, [261](#)
- ADC_TRIGGER_SOFTWARE, [261](#)
- ADC_VOLTAGEREF_VALT, [262](#)
- ADC_VOLTAGEREF_VREF, [262](#)
- adc_average_t, [258](#)
- adc_clk_divide_t, [259](#)
- adc_input_clock_t, [259](#)
- adc_inputchannel_t, [259](#)
- adc_latch_clear_t, [260](#)
- adc_pretrigger_sel_t, [260](#)
- adc_resolution_t, [260](#)
- adc_sw_pretrigger_t, [261](#)
- adc_trigger_sel_t, [261](#)
- adc_trigger_t, [261](#)
- adc_voltage_reference_t, [261](#)
- ADC_AVERAGE_16
 - ADC Driver, [259](#)
- ADC_AVERAGE_32
 - ADC Driver, [259](#)
- ADC_AVERAGE_4
 - ADC Driver, [259](#)
- ADC_AVERAGE_8
 - ADC Driver, [259](#)
- ADC_CLK_ALT_1
 - ADC Driver, [259](#)
- ADC_CLK_ALT_2
 - ADC Driver, [259](#)
- ADC_CLK_ALT_3
 - ADC Driver, [259](#)
- ADC_CLK_ALT_4
 - ADC Driver, [259](#)
- ADC_CLK_DIVIDE_1
 - ADC Driver, [259](#)
- ADC_CLK_DIVIDE_2
 - ADC Driver, [259](#)
- ADC_CLK_DIVIDE_4
 - ADC Driver, [259](#)
- ADC_CLK_DIVIDE_8
 - ADC Driver, [259](#)
- ADC_DELAY_TYPE_GROUP_DELAY
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [276](#)
- ADC_DELAY_TYPE_INDIVIDUAL_DELAY
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [276](#)
- ADC_DELAY_TYPE_NO_DELAY
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [276](#)
- ADC_DRV_AutoCalibration
 - ADC Driver, [262](#)
- ADC_DRV_ClearLatchedTriggers
 - ADC Driver, [262](#)
- ADC_DRV_ClearTriggerErrors
 - ADC Driver, [262](#)
- ADC_DRV_ConfigChan
 - ADC Driver, [262](#)
- ADC_DRV_ConfigConverter
 - ADC Driver, [263](#)
- ADC_DRV_ConfigHwAverage
 - ADC Driver, [263](#)
- ADC_DRV_ConfigHwCompare
 - ADC Driver, [263](#)
- ADC_DRV_ConfigUserCalibration
 - ADC Driver, [263](#)
- ADC_DRV_GetChanConfig
 - ADC Driver, [263](#)
- ADC_DRV_GetChanResult
 - ADC Driver, [264](#)
- ADC_DRV_GetConvCompleteFlag
 - ADC Driver, [264](#)
- ADC_DRV_GetConverterConfig
 - ADC Driver, [264](#)
- ADC_DRV_GetHwAverageConfig
 - ADC Driver, [264](#)
- ADC_DRV_GetHwCompareConfig
 - ADC Driver, [265](#)
- ADC_DRV_GetInterruptNumber
 - ADC Driver, [265](#)
- ADC_DRV_GetTriggerErrorFlags
 - ADC Driver, [265](#)
- ADC_DRV_GetUserCalibration
 - ADC Driver, [265](#)
- ADC_DRV_InitChanStruct
 - ADC Driver, [265](#)
- ADC_DRV_InitConverterStruct
 - ADC Driver, [266](#)
- ADC_DRV_InitHwAverageStruct
 - ADC Driver, [266](#)
- ADC_DRV_InitHwCompareStruct
 - ADC Driver, [266](#)
- ADC_DRV_InitUserCalibrationStruct
 - ADC Driver, [266](#)
- ADC_DRV_Reset
 - ADC Driver, [267](#)
- ADC_DRV_SetSwPretrigger
 - ADC Driver, [267](#)
- ADC_DRV_WaitConvDone
 - ADC Driver, [267](#)
- ADC_Deinit
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [276](#)
- ADC_DisableHardwareTrigger

- Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [278](#)
- ADC_DisableNotification
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [278](#)
- ADC_EnableHardwareTrigger
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [278](#)
- ADC_EnableNotification
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [279](#)
- ADC_INPUTCHAN_BANDGAP
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_DISABLED
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_EXT0
 - ADC Driver, [259](#)
- ADC_INPUTCHAN_EXT1
 - ADC Driver, [259](#)
- ADC_INPUTCHAN_EXT10
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_EXT11
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_EXT12
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_EXT13
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_EXT14
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_EXT3
 - ADC Driver, [259](#)
- ADC_INPUTCHAN_EXT4
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_EXT5
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_EXT6
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_EXT7
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_EXT9
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_INT0
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_INT1
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_INT2
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_INT3
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_SUPPLY_VDD
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_SUPPLY_VDD_3V
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_SUPPLY_VDD_FLASH_3V
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_SUPPLY_VDD_LV
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_SUPPLY_VDDA
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_SUPPLY_VREFH
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_TEMP
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_VREFSH
 - ADC Driver, [260](#)
- ADC_INPUTCHAN_VREFSL
 - ADC Driver, [260](#)
- ADC_Init
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [279](#)
- ADC_LATCH_CLEAR_FORCE
 - ADC Driver, [260](#)
- ADC_LATCH_CLEAR_WAIT
 - ADC Driver, [260](#)
- ADC_PRETRIGGER_SEL_PDB
 - ADC Driver, [260](#)
- ADC_PRETRIGGER_SEL_SW
 - ADC Driver, [260](#)
- ADC_PRETRIGGER_SEL_TRGMUX
 - ADC Driver, [260](#)
- ADC_RESOLUTION_10BIT
 - ADC Driver, [261](#)
- ADC_RESOLUTION_12BIT
 - ADC Driver, [261](#)
- ADC_RESOLUTION_8BIT
 - ADC Driver, [261](#)
- ADC_SW_PRETRIGGER_0
 - ADC Driver, [261](#)
- ADC_SW_PRETRIGGER_1
 - ADC Driver, [261](#)
- ADC_SW_PRETRIGGER_2
 - ADC Driver, [261](#)
- ADC_SW_PRETRIGGER_3
 - ADC Driver, [261](#)
- ADC_SW_PRETRIGGER_DISABLED
 - ADC Driver, [261](#)
- ADC_StartGroupConversion
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [279](#)
- ADC_StopGroupConversion
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [280](#)
- ADC_TRIGGER_HARDWARE
 - ADC Driver, [261](#)
- ADC_TRIGGER_SEL_PDB
 - ADC Driver, [261](#)
- ADC_TRIGGER_SEL_TRGMUX
 - ADC Driver, [261](#)
- ADC_TRIGGER_SOFTWARE
 - ADC Driver, [261](#)
- ADC_VOLTAGEREF_VALT
 - ADC Driver, [262](#)
- ADC_VOLTAGEREF_VREF
 - ADC Driver, [262](#)
- ALL_MODES
 - Clock Manager Driver, [344](#)

- ATTR
 - edma_software_tcd_t, [421](#)
- AUTONEG_1000BASETFD
 - Generic PHY, [663](#)
- AUTONEG_1000BASETHD
 - Generic PHY, [663](#)
- AUTONEG_100BASETXFD
 - Generic PHY, [663](#)
- AUTONEG_100BASETXHD
 - Generic PHY, [663](#)
- AUTONEG_10BASETFD
 - Generic PHY, [663](#)
- AUTONEG_10BASETHD
 - Generic PHY, [663](#)
- AUTONEG_ADVERT_ADDR
 - Generic PHY, [664](#)
- AUTONEG_LPABILITY_ADDR
 - Generic PHY, [664](#)
- acceptState
 - Options, [1300](#)
- accessCtr
 - mpu_access_err_info_t, [862](#)
 - mpu_error_info_t, [873](#)
- accessRight
 - mpu_master_access_permission_t, [874](#)
 - mpu_master_access_right_t, [862](#)
- accessType
 - mpu_access_err_info_t, [862](#)
 - mpu_error_info_t, [873](#)
- active_schedule_id
 - lin_master_data_t, [840](#)
- adc_average_config_t, [257](#)
 - hwAverage, [257](#)
 - hwAvgEnable, [257](#)
- adc_average_t
 - ADC Driver, [258](#)
- adc_calibration_t, [258](#)
 - userGain, [258](#)
 - userOffset, [258](#)
- adc_callback_info_t, [1246](#)
 - groupIndex, [1247](#)
 - resultBufferTail, [1247](#)
- adc_chan_config_t, [257](#)
 - channel, [258](#)
 - interruptEnable, [258](#)
- adc_clk_divide_t
 - ADC Driver, [259](#)
- adc_compare_config_t, [256](#)
 - compVal1, [257](#)
 - compVal2, [257](#)
 - compareEnable, [257](#)
 - compareGreaterThanEnable, [257](#)
 - compareRangeFuncEnable, [257](#)
- adc_config_t, [274](#)
 - extension, [275](#)
 - groupConfigArray, [275](#)
 - numGroups, [275](#)
 - sampleTicks, [275](#)
- adc_converter_config_t, [255](#)
 - clockDivide, [255](#)
 - continuousConvEnable, [255](#)
 - dmaEnable, [255](#)
 - inputClock, [256](#)
 - pretriggerSel, [256](#)
 - resolution, [256](#)
 - sampleTime, [256](#)
 - supplyMonitoringEnable, [256](#)
 - trigger, [256](#)
 - triggerSel, [256](#)
 - voltageRef, [256](#)
- adc_delay_type_t
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [276](#)
- adc_group_config_t, [273](#)
 - callback, [273](#)
 - callbackUserData, [273](#)
 - continuousConvEn, [273](#)
 - delayArray, [273](#)
 - delayType, [274](#)
 - hwTriggerSupport, [274](#)
 - inputChannelArray, [274](#)
 - numChannels, [274](#)
 - numSetsResultBuffer, [274](#)
 - resultBuffer, [274](#)
 - triggerSource, [274](#)
- adc_input_chan_t
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [276](#)
- adc_input_clock_t
 - ADC Driver, [259](#)
- adc_inputchannel_t
 - ADC Driver, [259](#)
- adc_instance_t, [1247](#)
 - instIdx, [1247](#)
 - instType, [1247](#)
- adc_latch_clear_t
 - ADC Driver, [260](#)
- adc_pretrigger_sel_t
 - ADC Driver, [260](#)
- adc_resolution_t
 - ADC Driver, [260](#)
- adc_sw_pretrigger_t
 - ADC Driver, [261](#)
- adc_trigger_sel_t
 - ADC Driver, [261](#)
- adc_trigger_source_t
 - Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), [276](#)
- adc_trigger_t
 - ADC Driver, [261](#)
- adc_voltage_reference_t
 - ADC Driver, [261](#)
- adcPreTriggerIdx
 - pdb_adc_pretrigger_config_t, [934](#)
- addr
 - mpu_access_err_info_t, [862](#)

- mpu_error_info_t, 873
- phy_config_t, 946
- address
 - edma_scatter_gather_list_t, 417
 - fs45_reg_config_value_t, 1051
- aead_mac_size
 - CipherSpecs, 1258
- Aes, 1247
 - heap, 1248
 - key, 1248
 - keylen, 1248
 - reg, 1248
 - rounds, 1248
 - tmp, 1248
- aes
 - Ciphers, 1258
 - WOLFSSL_Cipher, 1349
- afterDate
 - DecodedCert, 1265
- afterDateLen
 - DecodedCert, 1265
- alarmCallback
 - rtc_alarm_config_t, 1003
- alarmIntEnable
 - rtc_alarm_config_t, 1003
- alarmTime
 - rtc_alarm_config_t, 1003
- alert_history
 - WOLFSSL, 1337
- alertCount
 - Options, 1300
- allMasters
 - qspi_ahb_config_t, 1310
- alloc
 - mp_int, 1295
- altEmailNames
 - DecodedCert, 1265
- altNames
 - DecodedCert, 1266
 - WOLFSSL_X509, 1373
- altNamesNext
 - WOLFSSL_X509, 1373
- alternateClock
 - scg_clock_mode_config_t, 333
- Analog to Digital Converter - Peripheral Abstraction Layer (ADC PAL), 268
 - ADC_DELAY_TYPE_GROUP_DELAY, 276
 - ADC_DELAY_TYPE_INDIVIDUAL_DELAY, 276
 - ADC_DELAY_TYPE_NO_DELAY, 276
 - ADC_Deinit, 276
 - ADC_DisableHardwareTrigger, 278
 - ADC_DisableNotification, 278
 - ADC_EnableHardwareTrigger, 278
 - ADC_EnableNotification, 279
 - ADC_Init, 279
 - ADC_StartGroupConversion, 279
 - ADC_StopGroupConversion, 280
 - adc_delay_type_t, 276
 - adc_input_chan_t, 276
 - adc_trigger_source_t, 276
- Arc4, 1248
 - heap, 1249
 - state, 1249
 - x, 1249
 - y, 1249
- arc4
 - Ciphers, 1258
 - WOLFSSL_Cipher, 1349
- argc
 - func_args, 1283
- argv
 - func_args, 1283
- Arrays, 1249
 - client_identity, 1249
 - clientRandom, 1249
 - masterSecret, 1249
 - pendingMsg, 1250
 - pendingMsgOffset, 1250
 - pendingMsgSz, 1250
 - pendingMsgType, 1250
 - preMasterSecret, 1250
 - preMasterSz, 1250
 - psk_key, 1250
 - psk_keySz, 1250
 - server_hint, 1250
 - serverRandom, 1250
 - sessionID, 1250
 - sessionIDSz, 1250
- arrays
 - WOLFSSL, 1337
- assertLogic
 - ewm_init_config_t, 470
 - extension_ewm_for_wdg_t, 1224
- associated_uncond_frame_ptr
 - lin_associate_frame_t, 831
- asyncState
 - Options, 1301
- attributes
 - mpu_access_err_info_t, 862
 - mpu_error_info_t, 873
- autoClearTrigger
 - ftm_pwm_sync_t, 589
- autobaudEnable
 - lin_user_config_t, 725
- Automotive Math and Motor Control Library, 281
- autonegAbility
 - phy_basicStatus_t, 1306
- autonegComplete
 - phy_basicStatus_t, 1306
- autonegCompleteCB
 - phy_config_t, 946
- autonegFailedCB
 - phy_config_t, 946
- B0DRVS_ADDRESS
 - Register address map, 1024
- B0FIE_ADDRESS

- Register address map, [1024](#)
- B0FIS_ADDRESS
 - Register address map, [1024](#)
- B0OLDTC_ADDRESS
 - Register address map, [1024](#)
- B0SCDTC_ADDRESS
 - Register address map, [1024](#)
- B0WUPIE_ADDRESS
 - Register address map, [1024](#)
- B0WUPIS_ADDRESS
 - Register address map, [1024](#)
- B0WUPS_ADDRESS
 - Register address map, [1024](#)
- B0WUPTHRC_ADDRESS
 - Register address map, [1025](#)
- B1DRVS_ADDRESS
 - Register address map, [1025](#)
- B1FIE_ADDRESS
 - Register address map, [1025](#)
- B1FIS_ADDRESS
 - Register address map, [1025](#)
- B1OLDTC_ADDRESS
 - Register address map, [1025](#)
- B1SCDTC_ADDRESS
 - Register address map, [1025](#)
- B1WUPIE_ADDRESS
 - Register address map, [1025](#)
- B1WUPIS_ADDRESS
 - Register address map, [1025](#)
- B1WUPS_ADDRESS
 - Register address map, [1025](#)
- B1WUPTHRC_ADDRESS
 - Register address map, [1025](#)
- BASIC_CONTROL_ADDR
 - Generic PHY, [664](#)
- BASIC_CONTROL_AUTONEG_FLAG
 - Generic PHY, [664](#)
- BASIC_CONTROL_LOOPBACK_FLAG
 - Generic PHY, [664](#)
- BASIC_CONTROL_PDOWN_FLAG
 - Generic PHY, [664](#)
- BASIC_CONTROL_RESET_FLAG
 - Generic PHY, [664](#)
- BASIC_CONTROL_RESTART_AUTONEG_FLAG
 - Generic PHY, [664](#)
- BASIC_CONTROL_SPEED_LSB_FLAG
 - Generic PHY, [664](#)
- BASIC_CONTROL_SPEED_MSB_FLAG
 - Generic PHY, [664](#)
- BASIC_CTRL_ADDR
 - TJA110x PHY, [1140](#)
- BASIC_CTRL_LOOPBACK_FLAG
 - TJA110x PHY, [1140](#)
- BDMMode
 - ftm_user_config_t, [590](#)
- BITER
 - edma_software_tcd_t, [421](#)
- BMETSC_ADDRESS
 - Register address map, [1025](#)
- BMHC_ADDRESS
 - Register address map, [1026](#)
- BMOIE_DISABLE
 - Supply interrupt enable configuration options (0x1C), [1123](#)
- BMOIE_ENABLE
 - Supply interrupt enable configuration options (0x1C), [1123](#)
- BMOTC_ADDRESS
 - Register address map, [1026](#)
- BMUIE_DISABLE
 - Supply interrupt enable configuration options (0x1C), [1123](#)
- BMUIE_ENABLE
 - Supply interrupt enable configuration options (0x1C), [1123](#)
- BMUTC_ADDRESS
 - Register address map, [1026](#)
- BSADC1_ADDRESS
 - Register address map, [1026](#)
- BSADC2_ADDRESS
 - Register address map, [1026](#)
- BUS_ACTIVITY_SET
 - Common Core API., [355](#)
- BUS_CLK_INDEX
 - Clock Manager Driver, [341](#)
- Backward Compatibility Symbols for S32K148, [282](#)
- Bank N fail interrupt enable configuration options (0x38/0x48), [283](#)
 - IO15OLIE_DISABLE, [284](#)
 - IO15OLIE_ENABLE, [284](#)
 - IO15SCIE_DISABLE, [284](#)
 - IO15SCIE_ENABLE, [284](#)
 - IO26OLIE_DISABLE, [284](#)
 - IO26OLIE_ENABLE, [284](#)
 - IO26SCIE_DISABLE, [284](#)
 - IO26SCIE_ENABLE, [285](#)
 - IO37OLIE_DISABLE, [285](#)
 - IO37OLIE_ENABLE, [285](#)
 - IO37SCIE_DISABLE, [285](#)
 - IO37SCIE_ENABLE, [285](#)
 - IO48OLIE_DISABLE, [285](#)
 - IO48OLIE_ENABLE, [285](#)
 - IO48SCIE_DISABLE, [285](#)
 - IO48SCIE_ENABLE, [285](#)
- Bank N wake-up interrupt enable configuration options (0x37/0x47), [286](#)
 - IO15FEIE_DISABLE, [287](#)
 - IO15FEIE_ENABLE, [287](#)
 - IO15REIE_DISABLE, [287](#)
 - IO15REIE_ENABLE, [287](#)
 - IO26FEIE_DISABLE, [287](#)
 - IO26FEIE_ENABLE, [287](#)
 - IO26REIE_DISABLE, [288](#)
 - IO26REIE_ENABLE, [288](#)
 - IO37FEIE_DISABLE, [288](#)
 - IO37FEIE_ENABLE, [288](#)

- IO37REIE_DISABLE, 288
- IO37REIE_ENABLE, 288
- IO48FEIE_DISABLE, 288
- IO48FEIE_ENABLE, 288
- IO48REIE_DISABLE, 288
- IO48REIE_ENABLE, 288
- bankFailIntMask
 - uja113x_hvio_bank_cfg_t, 182
- bankWupIntMask
 - uja113x_hvio_bank_cfg_t, 182
- bankWupThr
 - uja113x_hvio_bank_cfg_t, 182
- Base_entry, 1250
 - name, 1251
 - nameSz, 1251
 - next, 1251
 - type, 1251
- baseT2Fd
 - phy_basicStatus_t, 1306
- baseT2Hd
 - phy_basicStatus_t, 1307
- baud_rate
 - lin_protocol_state_t, 841
- baudRate
 - flexio_i2c_master_user_config_t, 534
 - flexio_i2s_master_user_config_t, 544
 - flexio_spi_master_user_config_t, 561
 - flexio_uart_user_config_t, 575
 - i2c_master_t, 697
 - i2s_user_config_t, 676
 - lin_user_config_t, 725
 - lpi2c_baud_rate_params_t, 748
 - lpi2c_master_user_config_t, 746
 - lpuart_user_config_t, 807
 - spi_master_t, 1104
 - uart_user_config_t, 1214
- baudrateEvalEnable
 - lin_state_t, 727
- beforeDate
 - DecodedCert, 1266
- beforeDateLen
 - DecodedCert, 1266
- begin
 - DckeArgs, 1263
 - DcvArgs, 1263
 - DskeArgs, 1277
 - DtlsFrag, 1278
 - ProcPeerCertArgs, 1307
- bio
 - WOLFSSL_STACK, 1371
- BitClkDiv
 - sai_user_config_t, 1039
- BitClkFreq
 - sai_user_config_t, 1039
- BitClkInternal
 - sai_user_config_t, 1039
- BitClkNegPolar
 - sai_user_config_t, 1039
- bitCount
 - flexio_uart_user_config_t, 575
 - uart_user_config_t, 1214
- bitCountPerChar
 - lpuart_state_t, 805
 - lpuart_user_config_t, 807
- bitOrder
 - flexio_spi_master_user_config_t, 561
 - flexio_spi_slave_user_config_t, 563
 - spi_master_t, 1104
 - spi_slave_t, 1105
- bitcount
 - lpspi_master_config_t, 775
 - lpspi_slave_config_t, 780
- bitrate
 - flexcan_user_config_t, 517
- bitsPerFrame
 - lpspi_state_t, 777
- bitsPerSec
 - lpspi_master_config_t, 775
- bitsWidth
 - flexio_i2s_master_user_config_t, 544
 - flexio_i2s_slave_user_config_t, 545
- block_size
 - CipherSpecs, 1258
 - WOLFSSL_EVP_CIPHER_CTX, 1361
- bmOverVoltThr
 - uja113x_bmc_cfg_t, 205
- bmOverVoltThrRel
 - uja113x_bmc_cfg_t, 205
- bmSrcCtrl
 - uja113x_bmc_cfg_t, 205
- bmUndrVoltThr
 - uja113x_bmc_cfg_t, 205
- bmUndrVoltThrRel
 - uja113x_bmc_cfg_t, 205
- bmcBatMonitorCfg
 - uja113x_init_cfg_t, 184
- body
 - smtp_send_request, 1325
- boldtBankOpenLoad
 - uja113x_hvio_bank_cfg_t, 182
- bornOn
 - WOLFSSL_SESSION, 1369
- brownOutCode
 - Flash Memory (Flash), 500
- bscdtBankShortCirc
 - uja113x_hvio_bank_cfg_t, 182
- buf
 - __blake2bp_state, 1244
 - __blake2sp_state, 1246
 - DtlsMsg, 1279
 - WOLFSSL_EVP_CIPHER_CTX, 1361
- bufUsed
 - WOLFSSL_EVP_CIPHER_CTX, 1362
- buffLen
 - Md4, 1293
 - Md5, 1294

- Sha, [1320](#)
- Sha256, [1321](#)
- buffer
 - bufferStatic, [1254](#)
 - DerBuffer, [1272](#)
 - enet_buffer_descriptor_t, [446](#)
 - Md4, [1293](#)
 - Md5, [1294](#)
 - Sha, [1320](#)
 - Sha256, [1321](#)
 - WC_DerCertList, [1332](#)
 - WOLFSSL_BUFFER_INFO, [1346](#)
 - WOLFSSL_MD4_CTX, [1365](#)
 - x509_buffer, [1380](#)
- bufferSize
 - bufferStatic, [1254](#)
- bufferStatic, [1253](#)
 - buffer, [1254](#)
 - bufferSize, [1254](#)
 - dynamicFlag, [1254](#)
 - idx, [1254](#)
 - length, [1254](#)
 - offset, [1254](#)
 - staticBuffer, [1254](#)
- bufferSz
 - WC_DerCertList, [1332](#)
- bufferValue
 - packetInfo_st, [1305](#)
- Buffers, [1251](#)
 - certChain, [1252](#)
 - certificate, [1252](#)
 - clearOutputBuffer, [1252](#)
 - digest, [1252](#)
 - domainName, [1252](#)
 - inputBuffer, [1252](#)
 - key, [1252](#)
 - keySz, [1252](#)
 - keyType, [1252](#)
 - outputBuffer, [1252](#)
 - plainSz, [1252](#)
 - prevSent, [1252](#)
 - serverDH_G, [1252](#)
 - serverDH_Key, [1253](#)
 - serverDH_P, [1253](#)
 - serverDH_Priv, [1253](#)
 - serverDH_Pub, [1253](#)
 - sig, [1253](#)
 - weOwnCert, [1253](#)
 - weOwnCertChain, [1253](#)
 - weOwnDH, [1253](#)
 - weOwnKey, [1253](#)
- buffers
 - WOLFSSL, [1337](#)
- buflen
 - __blake2bp_state, [1244](#)
 - __blake2sp_state, [1246](#)
- BuildMsgArgs, [1254](#)
 - digestSz, [1255](#)
 - headerSz, [1255](#)
 - idx, [1255](#)
 - iv, [1255](#)
 - ivSz, [1255](#)
 - pad, [1255](#)
 - size, [1255](#)
 - sz, [1255](#)
- buildMsgState
 - Options, [1301](#)
- bulk_cipher_algorithm
 - CipherSpecs, [1259](#)
- bus_activity
 - lin_word_status_str_t, [828](#)
- bypassPrescaler
 - extension_lptmr_for_timer_t, [1160](#)
 - lptmr_config_t, [794](#)
- bytesPerFrame
 - lpspi_state_t, [777](#)
- c
 - RabbitCtx, [1314](#)
- CALLBACK_HANDLER
 - Low level API, [843](#)
- CAN_AbortTransfer
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [391](#)
- CAN_CLK_SOURCE_OSC
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [390](#)
- CAN_CLK_SOURCE_PERIPH
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [390](#)
- CAN_ConfigRemoteResponseBuff
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [391](#)
- CAN_ConfigRxBuff
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [392](#)
- CAN_ConfigTxBuff
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [392](#)
- CAN_DISABLE_MODE
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [391](#)
- CAN_Deinit
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [393](#)
- CAN_FD_DATA_BITRATE
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [390](#)
- CAN_GetBtrRate
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [393](#)
- CAN_GetDefaultConfig
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [393](#)
- CAN_GetTransferStatus
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [393](#)

- CAN_Init
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [394](#)
- CAN_InstallEventCallback
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [394](#)
- CAN_LOOPBACK_MODE
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [391](#)
- CAN_MSG_ID_EXT
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [391](#)
- CAN_MSG_ID_STD
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [391](#)
- CAN_NOMINAL_BITRATE
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [390](#)
- CAN_NORMAL_MODE
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [391](#)
- CAN_PAYLOAD_SIZE_16
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [390](#)
- CAN_PAYLOAD_SIZE_32
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [391](#)
- CAN_PAYLOAD_SIZE_64
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [391](#)
- CAN_PAYLOAD_SIZE_8
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [390](#)
- CAN_Receive
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [394](#)
- CAN_ReceiveBlocking
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [395](#)
- CAN_Send
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [395](#)
- CAN_SendBlocking
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [396](#)
- CAN_SetBtrRate
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [396](#)
- CAN_SetRxFilter
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [396](#)
- CANC_ADDRESS
 - Register address map, [1026](#)
- CBIORcv
 - WOLFSSL_CTX, [1352](#)
- CBIOSend
 - WOLFSSL_CTX, [1352](#)
- CBSIE_DISABLE
 - Transceiver interrupt enable configuration options (0x23), [1166](#)
- CBSIE_ENABLE
 - Transceiver interrupt enable configuration options (0x23), [1166](#)
- CDR_DATA_RATE_100
 - 01. CAN & CAN partial networking configuration, [195](#)
- CDR_DATA_RATE_1000
 - 01. CAN & CAN partial networking configuration, [195](#)
- CDR_DATA_RATE_125
 - 01. CAN & CAN partial networking configuration, [195](#)
- CDR_DATA_RATE_250
 - 01. CAN & CAN partial networking configuration, [195](#)
- CDR_DATA_RATE_50
 - 01. CAN & CAN partial networking configuration, [195](#)
- CDR_DATA_RATE_500a
 - 01. CAN & CAN partial networking configuration, [195](#)
- CDR_DATA_RATE_500b
 - 01. CAN & CAN partial networking configuration, [195](#)
- CDR_DATA_RATE_500c
 - 01. CAN & CAN partial networking configuration, [195](#)
- CFIE_DISABLE
 - Transceiver interrupt enable configuration options (0x23), [1166](#)
- CFIE_ENABLE
 - Transceiver interrupt enable configuration options (0x23), [1166](#)
- CHAN0_IDX
 - FlexTimer (FTM), [591](#)
- CHAN1_IDX
 - FlexTimer (FTM), [591](#)
- CHAN2_IDX
 - FlexTimer (FTM), [591](#)
- CHAN3_IDX
 - FlexTimer (FTM), [591](#)
- CHAN4_IDX
 - FlexTimer (FTM), [591](#)
- CHAN5_IDX
 - FlexTimer (FTM), [591](#)
- CHAN6_IDX
 - FlexTimer (FTM), [591](#)
- CHAN7_IDX
 - FlexTimer (FTM), [591](#)
- CHECK_PARITY
 - LIN Driver, [729](#)
- CITER
 - edma_software_tcd_t, [421](#)
- cldx
 - DecodedName, [1270](#)
- CLEAR_FTFx_FSTAT_ERROR_BITS

- Flash Memory (Flash), [487](#)
- CLK_SRC_FIRC
 - Clock Manager Driver, [341](#)
- CLK_SRC_FIRC_DIV1
 - Clock Manager Driver, [341](#)
- CLK_SRC_FIRC_DIV2
 - Clock Manager Driver, [341](#)
- CLK_SRC_OFF
 - Clock Manager Driver, [341](#)
- CLK_SRC_SIRC
 - Clock Manager Driver, [341](#)
- CLK_SRC_SIRC_DIV1
 - Clock Manager Driver, [341](#)
- CLK_SRC_SIRC_DIV2
 - Clock Manager Driver, [341](#)
- CLK_SRC_SOSC
 - Clock Manager Driver, [341](#)
- CLK_SRC_SOSC_DIV1
 - Clock Manager Driver, [341](#)
- CLK_SRC_SOSC_DIV2
 - Clock Manager Driver, [341](#)
- CLK_SRC_SPLL
 - Clock Manager Driver, [342](#)
- CLK_SRC_SPLL_DIV1
 - Clock Manager Driver, [342](#)
- CLK_SRC_SPLL_DIV2
 - Clock Manager Driver, [342](#)
- CLOCK_DRV_GetFreq
 - Clock, [315](#)
- CLOCK_DRV_GetSystemClockSource
 - Clock Manager Driver, [349](#)
- CLOCK_DRV_Init
 - Clock, [315](#)
- CLOCK_DRV_SetClockSource
 - Clock Manager Driver, [349](#)
- CLOCK_DRV_SetModuleClock
 - Clock Manager Driver, [349](#)
- CLOCK_DRV_SetSystemClock
 - Clock Manager Driver, [351](#)
- CLOCK_MANAGER_CALLBACK_AFTER
 - Clock Manager Driver, [343](#)
- CLOCK_MANAGER_CALLBACK_BEFORE
 - Clock Manager Driver, [343](#)
- CLOCK_MANAGER_CALLBACK_BEFORE_AFTER
 - Clock Manager Driver, [343](#)
- CLOCK_MANAGER_NOTIFY_AFTER
 - Clock Manager Driver, [343](#)
- CLOCK_MANAGER_NOTIFY_BEFORE
 - Clock Manager Driver, [343](#)
- CLOCK_MANAGER_NOTIFY_RECOVER
 - Clock Manager Driver, [343](#)
- CLOCK_MANAGER_POLICY_AGREEMENT
 - Clock Manager Driver, [343](#)
- CLOCK_MANAGER_POLICY_FORCIBLE
 - Clock Manager Driver, [343](#)
- CLOCK_SYS_GetCurrentConfiguration
 - Clock Manager Driver, [351](#)
- CLOCK_SYS_GetErrorCallback
 - Clock Manager Driver, [351](#)
- CLOCK_SYS_GetFreq
 - Clock Manager Driver, [351](#)
- CLOCK_SYS_Init
 - Clock Manager Driver, [351](#)
- CLOCK_SYS_SetConfiguration
 - Clock Manager Driver, [353](#)
- CLOCK_SYS_UpdateConfiguration
 - Clock Manager Driver, [353](#)
- CLOCK_TRACE_SRC_CORE_CLK
 - Clock Manager Driver, [343](#)
- cLen
 - DecodedName, [1270](#)
- CMC_TRANSCEIVER_ACTIVE
 - 01. CAN & CAN partial networking configuration, [194](#)
- CMC_TRANSCEIVER_ACTIVE2
 - 01. CAN & CAN partial networking configuration, [194](#)
- CMC_TRANSCEIVER_LISTEN
 - 01. CAN & CAN partial networking configuration, [194](#)
- CMC_TRANSCEIVER_OFF
 - 01. CAN & CAN partial networking configuration, [194](#)
- CMP_AVAILABLE
 - Comparator Driver, [372](#)
- CMP_BOTH_EDGES
 - Comparator Driver, [373](#)
- CMP_CONTINUOUS
 - Comparator Driver, [372](#)
- CMP_COUT
 - Comparator Driver, [373](#)
- CMP_COUTA
 - Comparator Driver, [373](#)
- CMP_DAC
 - Comparator Driver, [373](#)
- CMP_DISABLED
 - Comparator Driver, [372](#)
- CMP_DRV_ClearInputFlags
 - Comparator Driver, [374](#)
- CMP_DRV_ClearOutputFlags
 - Comparator Driver, [374](#)
- CMP_DRV_ConfigComparator
 - Comparator Driver, [374](#)
- CMP_DRV_ConfigDAC
 - Comparator Driver, [374](#)
- CMP_DRV_ConfigMUX
 - Comparator Driver, [375](#)
- CMP_DRV_ConfigTriggerMode
 - Comparator Driver, [375](#)
- CMP_DRV_GetComparatorConfig
 - Comparator Driver, [375](#)
- CMP_DRV_GetConfigAll
 - Comparator Driver, [376](#)
- CMP_DRV_GetDACConfig
 - Comparator Driver, [376](#)
- CMP_DRV_GetDefaultConfig

- Comparator Driver, [376](#)
- CMP_DRV_GetInitConfigAll
 - Comparator Driver, [376](#)
- CMP_DRV_GetInitConfigComparator
 - Comparator Driver, [377](#)
- CMP_DRV_GetInitConfigDAC
 - Comparator Driver, [377](#)
- CMP_DRV_GetInitConfigMUX
 - Comparator Driver, [377](#)
- CMP_DRV_GetInitTriggerMode
 - Comparator Driver, [378](#)
- CMP_DRV_GetInputFlags
 - Comparator Driver, [378](#)
- CMP_DRV_GetMUXConfig
 - Comparator Driver, [378](#)
- CMP_DRV_GetOutputFlags
 - Comparator Driver, [378](#)
- CMP_DRV_GetTriggerModeConfig
 - Comparator Driver, [379](#)
- CMP_DRV_Init
 - Comparator Driver, [379](#)
- CMP_DRV_Reset
 - Comparator Driver, [379](#)
- CMP_FALLING_EDGE
 - Comparator Driver, [373](#)
- CMP_HIGH_SPEED
 - Comparator Driver, [373](#)
- CMP_INPUT_FLAGS_MASK
 - Comparator Driver, [371](#)
- CMP_INPUT_FLAGS_SHIFT
 - Comparator Driver, [371](#)
- CMP_INVERT
 - Comparator Driver, [372](#)
- CMP_LEVEL_HYS_0
 - Comparator Driver, [372](#)
- CMP_LEVEL_HYS_1
 - Comparator Driver, [372](#)
- CMP_LEVEL_HYS_2
 - Comparator Driver, [372](#)
- CMP_LEVEL_HYS_3
 - Comparator Driver, [372](#)
- CMP_LOW_SPEED
 - Comparator Driver, [373](#)
- CMP_MINUS_FIXED
 - Comparator Driver, [371](#)
- CMP_MUX
 - Comparator Driver, [373](#)
- CMP_NO_EVENT
 - Comparator Driver, [373](#)
- CMP_NORMAL
 - Comparator Driver, [372](#)
- CMP_PLUS_FIXED
 - Comparator Driver, [371](#)
- CMP_RISING_EDGE
 - Comparator Driver, [373](#)
- CMP_ROUND_ROBIN_CHANNELS_MASK
 - Comparator Driver, [371](#)
- CMP_ROUND_ROBIN_CHANNELS_SHIFT
 - Comparator Driver, [371](#)
- Comparator Driver, [371](#)
- CMP_SAMPLED_FILTRED_EXT_CLK
 - Comparator Driver, [372](#)
- CMP_SAMPLED_FILTRED_INT_CLK
 - Comparator Driver, [372](#)
- CMP_SAMPLED_NONFILTRED_EXT_CLK
 - Comparator Driver, [372](#)
- CMP_SAMPLED_NONFILTRED_INT_CLK
 - Comparator Driver, [372](#)
- CMP_UNAVAILABLE
 - Comparator Driver, [372](#)
- CMP_VIN1
 - Comparator Driver, [373](#)
- CMP_VIN2
 - Comparator Driver, [373](#)
- CMP_WINDOWED
 - Comparator Driver, [372](#)
- CMP_WINDOWED_FILTRED
 - Comparator Driver, [372](#)
- CMP_WINDOWED_RESAMPLED
 - Comparator Driver, [372](#)
- COMM_STATUS_ADDR
 - TJA110x PHY, [1140](#)
- COMM_STATUS_LINKUP_FLAG
 - TJA110x PHY, [1140](#)
- COMMON_CONFIG_ADDR
 - TJA110x PHY, [1140](#)
- COMMON_CONFIG_AUTO_OP_MASK
 - TJA110x PHY, [1140](#)
- COMMON_CONFIG_CLK_DRIVER_FLAG
 - TJA110x PHY, [1140](#)
- COMMON_CONFIG_CLK_HOLD_FLAG
 - TJA110x PHY, [1140](#)
- COMMON_CONFIG_CLK_MODE_LSB
 - TJA110x PHY, [1140](#)
- COMMON_CONFIG_CLK_MODE_MASK
 - TJA110x PHY, [1140](#)
- COMMON_CONFIG_CONFIG_WAKE_FLAG
 - TJA110x PHY, [1140](#)
- COMMON_CONFIG_LOC_WU_TIM_LONG
 - TJA110x PHY, [1140](#)
- COMMON_CONFIG_LOC_WU_TIM_MASK
 - TJA110x PHY, [1140](#)
- COMMON_CONFIG_LOC_WU_TIM_SHORT
 - TJA110x PHY, [1141](#)
- COMMON_CONFIG_LOC_WU_TIM_SHORTEST
 - TJA110x PHY, [1141](#)
- CONFIG1_ADDR
 - TJA110x PHY, [1141](#)
- CONFIG1_FWDPHYLOC_FLAG
 - TJA110x PHY, [1141](#)
- CONFIG1_FWDPHYREM_FLAG
 - TJA110x PHY, [1141](#)
- CONFIG1_LOCWUPHY_FLAG
 - TJA110x PHY, [1141](#)
- CONFIG1_MASTERSLAVE_FLAG
 - TJA110x PHY, [1141](#)
- CONFIG1_MII_DRIVER_FLAG

- TJA110x PHY, [1141](#)
- CONFIG1_MII_MODE_MASK
 - TJA110x PHY, [1141](#)
- CONFIG1_MII_MODE_SHIFT
 - TJA110x PHY, [1141](#)
- CONFIG1_REMWUPHY_FLAG
 - TJA110x PHY, [1141](#)
- CONFIG1_SLEEPACK_FLAG
 - TJA110x PHY, [1141](#)
- CONFIG1_SLEEPCONFIRM_FLAG
 - TJA110x PHY, [1141](#)
- CONFIG2_ADDR
 - TJA110x PHY, [1141](#)
- CONFIG2_SLEEPREQUESTTO_16_8
 - TJA110x PHY, [1141](#)
- CONFIG2_SLEEPREQUESTTO_MASK
 - TJA110x PHY, [1142](#)
- CONTROL_1000BASET_ADDR
 - Generic PHY, [664](#)
- CONTROL_1000BASET_CONFIG_ENABLE_FLAG
 - Generic PHY, [664](#)
- CONTROL_1000BASET_CONFIG_VALUE_FLAG
 - Generic PHY, [664](#)
- CONTROL_STATUS_1000BASET_OFFSET
 - Generic PHY, [664](#)
- CORE_CLK_INDEX
 - Clock Manager Driver, [342](#)
- CRC Driver, [289](#)
 - CRC_DRV_Configure, [290](#)
 - CRC_DRV_Deinit, [290](#)
 - CRC_DRV_GetConfig, [291](#)
 - CRC_DRV_GetCrc16, [291](#)
 - CRC_DRV_GetCrc32, [291](#)
 - CRC_DRV_GetCrc8, [292](#)
 - CRC_DRV_GetCrcResult, [292](#)
 - CRC_DRV_GetDefaultConfig, [292](#)
 - CRC_DRV_Init, [293](#)
 - CRC_DRV_WriteData, [293](#)
 - CRC_TRANSPOSE_BITS, [290](#)
 - CRC_TRANSPOSE_BITS_AND_BYTES, [290](#)
 - CRC_TRANSPOSE_BYTES, [290](#)
 - CRC_TRANSPOSE_NONE, [290](#)
 - crc_transpose_t, [290](#)
- CRC_DRV_Configure
 - CRC Driver, [290](#)
- CRC_DRV_Deinit
 - CRC Driver, [290](#)
- CRC_DRV_GetConfig
 - CRC Driver, [291](#)
- CRC_DRV_GetCrc16
 - CRC Driver, [291](#)
- CRC_DRV_GetCrc32
 - CRC Driver, [291](#)
- CRC_DRV_GetCrc8
 - CRC Driver, [292](#)
- CRC_DRV_GetCrcResult
 - CRC Driver, [292](#)
- CRC_DRV_GetDefaultConfig
 - CRC Driver, [292](#)
- CRC_DRV_Init
 - CRC Driver, [293](#)
- CRC_DRV_WriteData
 - CRC Driver, [293](#)
- CRC_TRANSPOSE_BITS
 - CRC Driver, [290](#)
- CRC_TRANSPOSE_BITS_AND_BYTES
 - CRC Driver, [290](#)
- CRC_TRANSPOSE_BYTES
 - CRC Driver, [290](#)
- CRC_TRANSPOSE_NONE
 - CRC Driver, [290](#)
- CRL_Entry, [1260](#)
 - certs, [1261](#)
 - issuerHash, [1261](#)
 - lastDate, [1261](#)
 - lastDateFormat, [1261](#)
 - next, [1261](#)
 - nextDate, [1261](#)
 - nextDateFormat, [1261](#)
 - signature, [1261](#)
 - signatureOID, [1261](#)
 - signatureSz, [1261](#)
 - tbsSz, [1261](#)
 - toBeSigned, [1261](#)
 - totalCerts, [1262](#)
 - verified, [1262](#)
- CRL_Monitor, [1262](#)
 - path, [1262](#)
 - type, [1262](#)
- CSC_NONE
 - 01. CAN & CAN partial networking configuration, [194](#)
- CSC_OVERVOLTAGE
 - 01. CAN & CAN partial networking configuration, [194](#)
- CSC_UNDRV_OVERV
 - 01. CAN & CAN partial networking configuration, [194](#)
- CSC_UNDRVOLTAGE
 - 01. CAN & CAN partial networking configuration, [194](#)
- CSE_KEY_SIZE_CODE_MAX
 - Flash Memory (Flash), [487](#)
- CSEC_BOOT_MAC
 - CSEc Driver, [303](#)
- CSEC_BOOT_MAC_KEY
 - CSEc Driver, [303](#)
- CSEC_BOOT_NOT_DEFINED
 - CSEc Driver, [302](#)
- CSEC_BOOT_PARALLEL
 - CSEc Driver, [302](#)
- CSEC_BOOT_SERIAL
 - CSEc Driver, [302](#)
- CSEC_BOOT_STRICT
 - CSEc Driver, [302](#)
- CSEC_CALL_SEQ_FIRST

- CSEc Driver, [303](#)
- CSEC_CALL_SEQ_SUBSEQUENT
 - CSEc Driver, [303](#)
- CSEC_CMD_BOOT_DEFINE
 - CSEc Driver, [303](#)
- CSEC_CMD_BOOT_FAILURE
 - CSEc Driver, [303](#)
- CSEC_CMD_BOOT_OK
 - CSEc Driver, [303](#)
- CSEC_CMD_DBG_AUTH
 - CSEc Driver, [303](#)
- CSEC_CMD_DBG_CHAL
 - CSEc Driver, [303](#)
- CSEC_CMD_DEC_CBC
 - CSEc Driver, [303](#)
- CSEC_CMD_DEC_ECB
 - CSEc Driver, [303](#)
- CSEC_CMD_ENC_CBC
 - CSEc Driver, [303](#)
- CSEC_CMD_ENC_ECB
 - CSEc Driver, [303](#)
- CSEC_CMD_EXPORT_RAM_KEY
 - CSEc Driver, [303](#)
- CSEC_CMD_EXTEND_SEED
 - CSEc Driver, [303](#)
- CSEC_CMD_GENERATE_MAC
 - CSEc Driver, [303](#)
- CSEC_CMD_GET_ID
 - CSEc Driver, [303](#)
- CSEC_CMD_INIT_RNG
 - CSEc Driver, [303](#)
- CSEC_CMD_LOAD_KEY
 - CSEc Driver, [303](#)
- CSEC_CMD_LOAD_PLAIN_KEY
 - CSEc Driver, [303](#)
- CSEC_CMD_MP_COMPRESS
 - CSEc Driver, [303](#)
- CSEC_CMD_RESERVED_1
 - CSEc Driver, [303](#)
- CSEC_CMD_RESERVED_2
 - CSEc Driver, [303](#)
- CSEC_CMD_RESERVED_3
 - CSEc Driver, [303](#)
- CSEC_CMD_RND
 - CSEc Driver, [303](#)
- CSEC_CMD_VERIFY_MAC
 - CSEc Driver, [303](#)
- CSEC_DRV_BootDefine
 - CSEc Driver, [304](#)
- CSEC_DRV_BootFailure
 - CSEc Driver, [304](#)
- CSEC_DRV_BootOK
 - CSEc Driver, [304](#)
- CSEC_DRV_CancelCommand
 - CSEc Driver, [305](#)
- CSEC_DRV_DbgAuth
 - CSEc Driver, [305](#)
- CSEC_DRV_DbgChal
 - CSEc Driver, [305](#)
- CSEC_DRV_DecryptCBC
 - CSEc Driver, [305](#)
- CSEC_DRV_DecryptCBCAsync
 - CSEc Driver, [306](#)
- CSEC_DRV_DecryptECB
 - CSEc Driver, [306](#)
- CSEC_DRV_DecryptECBAsync
 - CSEc Driver, [307](#)
- CSEC_DRV_Deinit
 - CSEc Driver, [307](#)
- CSEC_DRV_EncryptCBC
 - CSEc Driver, [307](#)
- CSEC_DRV_EncryptCBCAsync
 - CSEc Driver, [307](#)
- CSEC_DRV_EncryptECB
 - CSEc Driver, [308](#)
- CSEC_DRV_EncryptECBAsync
 - CSEc Driver, [308](#)
- CSEC_DRV_ExportRAMKey
 - CSEc Driver, [309](#)
- CSEC_DRV_ExtendSeed
 - CSEc Driver, [309](#)
- CSEC_DRV_GenerateMAC
 - CSEc Driver, [309](#)
- CSEC_DRV_GenerateMACAddrMode
 - CSEc Driver, [309](#)
- CSEC_DRV_GenerateMACAsync
 - CSEc Driver, [310](#)
- CSEC_DRV_GenerateRND
 - CSEc Driver, [310](#)
- CSEC_DRV_GetAsyncCmdStatus
 - CSEc Driver, [310](#)
- CSEC_DRV_GetID
 - CSEc Driver, [311](#)
- CSEC_DRV_GetStatus
 - CSEc Driver, [311](#)
- CSEC_DRV_Init
 - CSEc Driver, [311](#)
- CSEC_DRV_InitRNG
 - CSEc Driver, [311](#)
- CSEC_DRV_InstallCallback
 - CSEc Driver, [311](#)
- CSEC_DRV_LoadKey
 - CSEc Driver, [312](#)
- CSEC_DRV_LoadPlainKey
 - CSEc Driver, [312](#)
- CSEC_DRV_MPCompress
 - CSEc Driver, [312](#)
- CSEC_DRV_VerifyMAC
 - CSEc Driver, [313](#)
- CSEC_DRV_VerifyMACAddrMode
 - CSEc Driver, [313](#)
- CSEC_DRV_VerifyMACAsync
 - CSEc Driver, [314](#)
- CSEC_KEY_1
 - CSEc Driver, [303](#)
- CSEC_KEY_10
 - CSEc Driver, [303](#)

- CSEc Driver, [304](#)
- CSEC_KEY_11
 - CSEc Driver, [304](#)
- CSEC_KEY_12
 - CSEc Driver, [304](#)
- CSEC_KEY_13
 - CSEc Driver, [304](#)
- CSEC_KEY_14
 - CSEc Driver, [304](#)
- CSEC_KEY_15
 - CSEc Driver, [304](#)
- CSEC_KEY_16
 - CSEc Driver, [304](#)
- CSEC_KEY_17
 - CSEc Driver, [304](#)
- CSEC_KEY_2
 - CSEc Driver, [303](#)
- CSEC_KEY_3
 - CSEc Driver, [304](#)
- CSEC_KEY_4
 - CSEc Driver, [304](#)
- CSEC_KEY_5
 - CSEc Driver, [304](#)
- CSEC_KEY_6
 - CSEc Driver, [304](#)
- CSEC_KEY_7
 - CSEc Driver, [304](#)
- CSEC_KEY_8
 - CSEc Driver, [304](#)
- CSEC_KEY_9
 - CSEc Driver, [304](#)
- CSEC_MASTER_ECU
 - CSEc Driver, [303](#)
- CSEC_RAM_KEY
 - CSEc Driver, [304](#)
- CSEC_SECRET_KEY
 - CSEc Driver, [303](#)
- CSEC_STATUS_BOOT_FINISHED
 - CSEc Driver, [301](#)
- CSEC_STATUS_BOOT_INIT
 - CSEc Driver, [301](#)
- CSEC_STATUS_BOOT_OK
 - CSEc Driver, [301](#)
- CSEC_STATUS_BUSY
 - CSEc Driver, [301](#)
- CSEC_STATUS_EXT_DEBUGGER
 - CSEc Driver, [302](#)
- CSEC_STATUS_INT_DEBUGGER
 - CSEc Driver, [302](#)
- CSEC_STATUS_RND_INIT
 - CSEc Driver, [302](#)
- CSEC_STATUS_SECURE_BOOT
 - CSEc Driver, [302](#)
- CSEc Driver, [294](#)
 - CSEC_BOOT_MAC, [303](#)
 - CSEC_BOOT_MAC_KEY, [303](#)
 - CSEC_BOOT_NOT_DEFINED, [302](#)
 - CSEC_BOOT_PARALLEL, [302](#)
 - CSEC_BOOT_SERIAL, [302](#)
 - CSEC_BOOT_STRICT, [302](#)
 - CSEC_CALL_SEQ_FIRST, [303](#)
 - CSEC_CALL_SEQ_SUBSEQUENT, [303](#)
 - CSEC_CMD_BOOT_DEFINE, [303](#)
 - CSEC_CMD_BOOT_FAILURE, [303](#)
 - CSEC_CMD_BOOT_OK, [303](#)
 - CSEC_CMD_DBG_AUTH, [303](#)
 - CSEC_CMD_DBG_CHAL, [303](#)
 - CSEC_CMD_DEC_CBC, [303](#)
 - CSEC_CMD_DEC_ECB, [303](#)
 - CSEC_CMD_ENC_CBC, [303](#)
 - CSEC_CMD_ENC_ECB, [303](#)
 - CSEC_CMD_EXPORT_RAM_KEY, [303](#)
 - CSEC_CMD_EXTEND_SEED, [303](#)
 - CSEC_CMD_GENERATE_MAC, [303](#)
 - CSEC_CMD_GET_ID, [303](#)
 - CSEC_CMD_INIT_RNG, [303](#)
 - CSEC_CMD_LOAD_KEY, [303](#)
 - CSEC_CMD_LOAD_PLAIN_KEY, [303](#)
 - CSEC_CMD_MP_COMPRESS, [303](#)
 - CSEC_CMD_RESERVED_1, [303](#)
 - CSEC_CMD_RESERVED_2, [303](#)
 - CSEC_CMD_RESERVED_3, [303](#)
 - CSEC_CMD_RND, [303](#)
 - CSEC_CMD_VERIFY_MAC, [303](#)
 - CSEC_DRV_BootDefine, [304](#)
 - CSEC_DRV_BootFailure, [304](#)
 - CSEC_DRV_BootOK, [304](#)
 - CSEC_DRV_CancelCommand, [305](#)
 - CSEC_DRV_DbgAuth, [305](#)
 - CSEC_DRV_DbgChal, [305](#)
 - CSEC_DRV_DecryptCBC, [305](#)
 - CSEC_DRV_DecryptCBCAsync, [306](#)
 - CSEC_DRV_DecryptECB, [306](#)
 - CSEC_DRV_DecryptECBAsync, [307](#)
 - CSEC_DRV_Deinit, [307](#)
 - CSEC_DRV_EncryptCBC, [307](#)
 - CSEC_DRV_EncryptCBCAsync, [307](#)
 - CSEC_DRV_EncryptECB, [308](#)
 - CSEC_DRV_EncryptECBAsync, [308](#)
 - CSEC_DRV_ExportRAMKey, [309](#)
 - CSEC_DRV_ExtendSeed, [309](#)
 - CSEC_DRV_GenerateMAC, [309](#)
 - CSEC_DRV_GenerateMACAddrMode, [309](#)
 - CSEC_DRV_GenerateMACAsync, [310](#)
 - CSEC_DRV_GenerateRND, [310](#)
 - CSEC_DRV_GetAsyncCmdStatus, [310](#)
 - CSEC_DRV_GetID, [311](#)
 - CSEC_DRV_GetStatus, [311](#)
 - CSEC_DRV_Init, [311](#)
 - CSEC_DRV_InitRNG, [311](#)
 - CSEC_DRV_InstallCallback, [311](#)
 - CSEC_DRV_LoadKey, [312](#)
 - CSEC_DRV_LoadPlainKey, [312](#)
 - CSEC_DRV_MPCompress, [312](#)
 - CSEC_DRV_VerifyMAC, [313](#)
 - CSEC_DRV_VerifyMACAddrMode, [313](#)

- CSEC_DRV_VerifyMACAsync, 314
- CSEC_KEY_1, 303
- CSEC_KEY_10, 304
- CSEC_KEY_11, 304
- CSEC_KEY_12, 304
- CSEC_KEY_13, 304
- CSEC_KEY_14, 304
- CSEC_KEY_15, 304
- CSEC_KEY_16, 304
- CSEC_KEY_17, 304
- CSEC_KEY_2, 303
- CSEC_KEY_3, 304
- CSEC_KEY_4, 304
- CSEC_KEY_5, 304
- CSEC_KEY_6, 304
- CSEC_KEY_7, 304
- CSEC_KEY_8, 304
- CSEC_KEY_9, 304
- CSEC_MASTER_ECU, 303
- CSEC_RAM_KEY, 304
- CSEC_SECRET_KEY, 303
- CSEC_STATUS_BOOT_FINISHED, 301
- CSEC_STATUS_BOOT_INIT, 301
- CSEC_STATUS_BOOT_OK, 301
- CSEC_STATUS_BUSY, 301
- CSEC_STATUS_EXT_DEBUGGER, 302
- CSEC_STATUS_INT_DEBUGGER, 302
- CSEC_STATUS_RND_INIT, 302
- CSEC_STATUS_SECURE_BOOT, 302
- csec_boot_flavor_t, 302
- csec_call_sequence_t, 302
- csec_cmd_t, 303
- csec_key_id_t, 303
- csec_status_t, 302
- CSR
 - edma_software_tcd_t, 421
- CWIE_DISABLE
 - Transceiver interrupt enable configuration options (0x23), 1166
- CWIE_ENABLE
 - Transceiver interrupt enable configuration options (0x23), 1166
- ca
 - DecodedCert, 1266
- caCacheCallback
 - WOLFSSL_CERT_MANAGER, 1347
- caLock
 - WOLFSSL_CERT_MANAGER, 1347
- caTable
 - WOLFSSL_CERT_MANAGER, 1347
- cache
 - WOLFSSL_X509_STORE, 1378
- CallBack
 - Flash Memory (Flash), 500
- Callback
 - lin_state_t, 727
- callback
 - adc_group_config_t, 273
 - clock_manager_callback_user_config_t, 340
 - csec_state_t, 300
 - edma_channel_config_t, 417
 - edma_chn_state_t, 416
 - enet_config_t, 448
 - enet_state_t, 448
 - FlexCANState, 514
 - flexio_i2c_master_user_config_t, 534
 - flexio_i2s_master_user_config_t, 544
 - flexio_i2s_slave_user_config_t, 545
 - flexio_spi_master_user_config_t, 561
 - flexio_spi_slave_user_config_t, 563
 - flexio_uart_user_config_t, 575
 - i2c_master_t, 697
 - i2c_slave_t, 698
 - i2s_user_config_t, 676
 - lpspi_master_config_t, 776
 - lpspi_slave_config_t, 780
 - lpspi_state_t, 777
 - qspi_user_config_t, 1311
 - sai_user_config_t, 1039
 - security_user_config_t, 1082
 - spi_master_t, 1104
 - spi_slave_t, 1106
 - timer_chan_config_t, 1159
- callback_arg
 - smtp_send_request, 1325
- callback_fn
 - smtp_send_request, 1325
- callback_functions, 1255
 - ctx_ready, 1255
 - method, 1255
 - on_result, 1256
 - ssl_ready, 1256
- callbackConfig
 - clock_manager_state_t, 340
- callbackData
 - clock_manager_callback_user_config_t, 340
 - power_manager_callback_user_config_t, 968
- callbackFunction
 - power_manager_callback_user_config_t, 968
- callbackNum
 - clock_manager_state_t, 340
- callbackParam
 - csec_state_t, 300
 - edma_channel_config_t, 417
 - FlexCANState, 514
 - flexio_i2c_master_user_config_t, 534
 - flexio_i2s_master_user_config_t, 544
 - flexio_i2s_slave_user_config_t, 545
 - flexio_spi_master_user_config_t, 562
 - flexio_spi_slave_user_config_t, 563
 - flexio_uart_user_config_t, 575
 - i2c_master_t, 697
 - i2c_slave_t, 698
 - i2s_user_config_t, 677
 - lpi2c_master_user_config_t, 746
 - lpi2c_slave_user_config_t, 747

- lpspi_master_config_t, 776
- lpspi_slave_config_t, 780
- lpspi_state_t, 778
- qspi_user_config_t, 1311
- sai_user_config_t, 1039
- security_user_config_t, 1082
- spi_master_t, 1104
- spi_slave_t, 1106
- timer_chan_config_t, 1159
- callbackParams
 - rtc_alarm_config_t, 1003
 - rtc_interrupt_config_t, 1003
- callbackType
 - clock_manager_callback_user_config_t, 340
 - power_manager_callback_user_config_t, 968
- callbackUserData
 - adc_group_config_t, 273
- callbacks
 - func_args, 1283
- can
 - sbc_int_config_t, 1182
- can_bitrate_phase_t
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), 390
- can_buff_config_t, 387
 - enableBRS, 387
 - enableFD, 387
 - fdPadding, 388
 - idType, 388
 - isRemote, 388
- can_clk_source_t
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), 390
- can_fd_payload_size_t
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), 390
- can_instance_t, 1256
 - instIdx, 1256
 - instType, 1256
- can_message_t, 388
 - cs, 388
 - data, 388
 - id, 388
 - length, 388
- can_msg_id_type_t
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), 391
- can_operation_modes_t
 - Controller Area Network - Peripheral Abstraction Layer (CAN PAL), 391
- can_time_segment_t, 386
 - phaseSeg1, 387
 - phaseSeg2, 387
 - preDivider, 387
 - propSeg, 387
 - rJumpwidth, 387
- can_user_config_t, 388
 - dataBitrate, 389
 - enableFD, 389
 - extension, 389
 - maxBuffNum, 389
 - mode, 389
 - nominalBitrate, 389
 - payloadSize, 389
 - peClkSrc, 389
- canConf
 - sbc_can_conf_t, 1180
- canDataRate
 - uja113x_cpnc_cfg_t, 191
- canDisCfg
 - fs45_wu2_reg_t, 1054
- canFDCtrl
 - uja113x_canc_cfg_t, 190
- canModeCtrl
 - uja113x_canc_cfg_t, 190
- canPartNetCtrl
 - uja113x_canc_cfg_t, 190
- canShutdownCtrl
 - uja113x_canc_cfg_t, 191
- canTransEvt
 - sbc_can_conf_t, 1180
- canWuTo
 - fs45_wu2_reg_t, 1054
- cancCanCfg
 - uja113x_init_cfg_t, 184
- carry
 - RabbitCtx, 1314
- cbMissingCRL
 - WOLFSSL_CERT_MANAGER, 1347
- cbs
 - sbc_trans_evt_stat_t, 1188
- cbse
 - sbc_trans_evt_t, 1179
- cbss
 - sbc_trans_stat_t, 1185
- certBegin
 - DecodedCert, 1266
- certChain
 - Buffers, 1252
 - WOLFSSL_CTX, 1352
- certHashes
 - HS_Hashes, 1288
- certIdx
 - ProcPeerCertArgs, 1307
- certOnly
 - Options, 1301
- CertSignCtx, 1256
 - digest, 1257
 - encSig, 1257
 - encSigSz, 1257
 - sig, 1257
 - state, 1257
- certificate
 - Buffers, 1252
 - WOLFSSL_CTX, 1352
- certs

- CRL_Entry, [1261](#)
- ProcPeerCertArgs, [1308](#)
- WOLFSSL_X509_CHAIN, [1375](#)
- WOLFSSL_X509_STORE_CTX, [1379](#)
- cf
 - sbc_trans_evnt_stat_t, [1188](#)
- cfdc
 - sbc_can_ctr_t, [1178](#)
- cfe
 - sbc_trans_evnt_t, [1179](#)
- cfs
 - sbc_trans_stat_t, [1185](#)
- chMode
 - ftm_output_cmp_ch_param_t, [633](#)
 - oc_output_ch_param_t, [922](#)
- chVersion
 - WOLFSSL, [1337](#)
- chain
 - WOLFSSL_X509_STORE_CTX, [1379](#)
- chainChannel
 - lpit_user_channel_config_t, [762](#)
- chanConfigArray
 - timer_config_t, [1159](#)
- chanType
 - timer_chan_config_t, [1159](#)
- channel
 - adc_chan_config_t, [258](#)
 - eim_user_channel_config_t, [437](#)
 - erm_user_config_t, [465](#)
 - pwm_channel_t, [988](#)
 - timer_chan_config_t, [1159](#)
- channel_extension_ftm_for_ic_t, [688](#)
 - continuousModeEn, [688](#)
- channelCallbackParams
 - ic_input_ch_param_t, [687](#)
 - oc_output_ch_param_t, [922](#)
- channelCallbacks
 - ic_input_ch_param_t, [687](#)
 - oc_output_ch_param_t, [922](#)
- ChannelCount
 - sai_user_config_t, [1039](#)
- ChannelEnable
 - sai_user_config_t, [1039](#)
- channelExtension
 - ic_input_ch_param_t, [687](#)
 - oc_output_ch_param_t, [922](#)
- channelPriority
 - edma_channel_config_t, [417](#)
- channelType
 - pwm_channel_t, [988](#)
- channelsCallbacks
 - ftm_input_ch_param_t, [621](#)
 - ftm_state_t, [588](#)
- channelsCallbacksParams
 - ftm_input_ch_param_t, [621](#)
 - ftm_state_t, [588](#)
- check_timeout
 - lin_tl_descriptor_t, [835](#)
- check_timeout_type
 - lin_tl_descriptor_t, [835](#)
- checkBitMask
 - eim_user_channel_config_t, [437](#)
- checkCapabilities
 - Generic PHY, [665](#)
- checksum
 - lin_state_t, [727](#)
- checksum
 - enet_rx_enh_info_t, [449](#)
- chipType
 - uja113x_driver_t, [186](#)
 - uja113x_drv_cfg_t, [181](#)
- chnArbitration
 - edma_user_config_t, [416](#)
- cipher
 - WOLFSSL, [1337](#)
 - WOLFSSL_EVP_CIPHER_CTX, [1362](#)
- cipher_type
 - CipherSpecs, [1259](#)
- cipherName
 - handShakeInfo_st, [1285](#)
- CipherSpecs, [1258](#)
 - aead_mac_size, [1258](#)
 - block_size, [1258](#)
 - bulk_cipher_algorithm, [1259](#)
 - cipher_type, [1259](#)
 - hash_size, [1259](#)
 - iv_size, [1259](#)
 - kea, [1259](#)
 - key_size, [1259](#)
 - mac_algorithm, [1259](#)
 - pad_size, [1259](#)
 - sig_algo, [1259](#)
 - static_ecdh, [1259](#)
- cipherSuite
 - Options, [1301](#)
- cipherSuite0
 - Options, [1301](#)
- cipherType
 - WOLFSSL_EVP_CIPHER_CTX, [1362](#)
- Ciphers, [1257](#)
 - aes, [1258](#)
 - arc4, [1258](#)
 - des3, [1258](#)
 - setup, [1258](#)
 - state, [1258](#)
- classicPID
 - lin_user_config_t, [725](#)
- clause45
 - phy_config_t, [946](#)
- clearOutputBuffer
 - Buffers, [1252](#)
- client_identity
 - Arrays, [1249](#)
- client_psk_cb
 - Options, [1301](#)
 - WOLFSSL_CTX, [1352](#)

- client_write_IV
 - Keys, [1291](#)
- client_write_MAC_secret
 - Keys, [1291](#)
- client_write_key
 - Keys, [1291](#)
- clientRandom
 - Arrays, [1249](#)
- ClientRow, [1259](#)
 - Clients, [1260](#)
 - nextIdx, [1260](#)
 - totalCount, [1260](#)
- ClientSession, [1260](#)
 - serverIdx, [1260](#)
 - serverRow, [1260](#)
- clientState
 - Options, [1301](#)
- Clients
 - ClientRow, [1260](#)
- clkGate
 - peripheral_clock_config_t, [335](#)
- clkHold
 - phy_tja110x_config_t, [1139](#)
- clkMode
 - phy_tja110x_config_t, [1139](#)
- clkPhase
 - lpspi_master_config_t, [776](#)
 - lpspi_slave_config_t, [780](#)
- clkPolarity
 - lpspi_master_config_t, [776](#)
 - lpspi_slave_config_t, [780](#)
- clkPreDiv
 - pdb_timer_config_t, [933](#)
- clkPreMultFactor
 - pdb_timer_config_t, [933](#)
- clkSource
 - wdg_config_t, [1225](#)
 - wdog_user_config_t, [1233](#)
- clkSrc
 - peripheral_clock_config_t, [335](#)
- Clock, [315](#)
 - CLOCK_DRV_GetFreq, [315](#)
 - CLOCK_DRV_Init, [315](#)
- Clock Manager, [316](#)
- Clock Manager Driver, [317](#)
 - ALL_MODES, [344](#)
 - BUS_CLK_INDEX, [341](#)
 - CLK_SRC_FIRC, [341](#)
 - CLK_SRC_FIRC_DIV1, [341](#)
 - CLK_SRC_FIRC_DIV2, [341](#)
 - CLK_SRC_OFF, [341](#)
 - CLK_SRC_SIRC, [341](#)
 - CLK_SRC_SIRC_DIV1, [341](#)
 - CLK_SRC_SIRC_DIV2, [341](#)
 - CLK_SRC_SOSC, [341](#)
 - CLK_SRC_SOSC_DIV1, [341](#)
 - CLK_SRC_SOSC_DIV2, [341](#)
 - CLK_SRC_SPLL, [342](#)
 - CLK_SRC_SPLL_DIV1, [342](#)
 - CLK_SRC_SPLL_DIV2, [342](#)
 - CLOCK_DRV_GetSystemClockSource, [349](#)
 - CLOCK_DRV_SetClockSource, [349](#)
 - CLOCK_DRV_SetModuleClock, [349](#)
 - CLOCK_DRV_SetSystemClock, [351](#)
 - CLOCK_MANAGER_CALLBACK_AFTER, [343](#)
 - CLOCK_MANAGER_CALLBACK_BEFORE, [343](#)
 - CLOCK_MANAGER_CALLBACK_BEFORE_AFTER, [343](#)
 - CLOCK_MANAGER_NOTIFY_AFTER, [343](#)
 - CLOCK_MANAGER_NOTIFY_BEFORE, [343](#)
 - CLOCK_MANAGER_NOTIFY_RECOVER, [343](#)
 - CLOCK_MANAGER_POLICY_AGREEMENT, [343](#)
 - CLOCK_MANAGER_POLICY_FORCIBLE, [343](#)
 - CLOCK_SYS_GetCurrentConfiguration, [351](#)
 - CLOCK_SYS_GetErrorCallback, [351](#)
 - CLOCK_SYS_GetFreq, [351](#)
 - CLOCK_SYS_Init, [351](#)
 - CLOCK_SYS_SetConfiguration, [353](#)
 - CLOCK_SYS_UpdateConfiguration, [353](#)
 - CLOCK_TRACE_SRC_CORE_CLK, [343](#)
 - CORE_CLK_INDEX, [342](#)
 - clock_manager_callback_t, [342](#)
 - clock_manager_callback_type_t, [342](#)
 - clock_manager_notify_t, [343](#)
 - clock_manager_policy_t, [343](#)
 - clock_trace_src_t, [343](#)
 - clock_user_config_t, [342](#)
 - DIVIDE_BY_EIGHTH, [343](#)
 - DIVIDE_BY_FIVE, [343](#)
 - DIVIDE_BY_FOUR, [343](#)
 - DIVIDE_BY_ONE, [343](#)
 - DIVIDE_BY_SEVEN, [343](#)
 - DIVIDE_BY_SIX, [343](#)
 - DIVIDE_BY_THREE, [343](#)
 - DIVIDE_BY_TWO, [343](#)
 - g_RtcClkInFreq, [354](#)
 - g_TClkFreq, [354](#)
 - g_xtal0ClkFreq, [354](#)
 - HSRUN_MODE, [344](#)
 - MULTIPLY_BY_ONE, [344](#)
 - MULTIPLY_BY_TWO, [344](#)
 - NO_MODE, [344](#)
 - NUMBER_OF_TCLK_INPUTS, [342](#)
 - peripheral_clock_divider_t, [343](#)
 - peripheral_clock_frac_t, [343](#)
 - peripheral_clock_source_t, [342](#)
 - peripheralFeaturesList, [354](#)
 - pwr_modes_t, [344](#)
 - RUN_MODE, [344](#)
 - SCG_ASYNC_CLOCK_DISABLE, [344](#)
 - SCG_ASYNC_CLOCK_DIV_BY_1, [344](#)
 - SCG_ASYNC_CLOCK_DIV_BY_16, [344](#)
 - SCG_ASYNC_CLOCK_DIV_BY_2, [344](#)
 - SCG_ASYNC_CLOCK_DIV_BY_32, [344](#)
 - SCG_ASYNC_CLOCK_DIV_BY_4, [344](#)
 - SCG_ASYNC_CLOCK_DIV_BY_64, [344](#)

SCG_ASYNC_CLOCK_DIV_BY_8, [344](#)
SCG_CLOCKOUT_SRC_FIRC, [344](#)
SCG_CLOCKOUT_SRC_SCG_SLOW, [344](#)
SCG_CLOCKOUT_SRC_SIRC, [344](#)
SCG_CLOCKOUT_SRC_SOSC, [344](#)
SCG_CLOCKOUT_SRC_SPLL, [344](#)
SCG_FIRC_RANGE_48M, [345](#)
SCG_SIRC_RANGE_HIGH, [345](#)
SCG_SOSC_GAIN_HIGH, [345](#)
SCG_SOSC_GAIN_LOW, [345](#)
SCG_SOSC_MONITOR_DISABLE, [345](#)
SCG_SOSC_MONITOR_INT, [345](#)
SCG_SOSC_MONITOR_RESET, [345](#)
SCG_SOSC_RANGE_HIGH, [345](#)
SCG_SOSC_RANGE_MID, [345](#)
SCG_SOSC_REF_EXT, [345](#)
SCG_SOSC_REF_OSC, [345](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_16, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_17, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_18, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_19, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_20, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_21, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_22, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_23, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_24, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_25, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_26, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_27, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_28, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_29, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_30, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_31, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_32, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_33, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_34, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_35, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_36, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_37, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_38, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_39, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_40, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_41, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_42, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_43, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_44, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_45, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_46, [346](#)
SCG_SPLL_CLOCK_MULTIPLY_BY_47, [346](#)
SCG_SPLL_CLOCK_PREDIV_BY_1, [346](#)
SCG_SPLL_CLOCK_PREDIV_BY_2, [346](#)
SCG_SPLL_CLOCK_PREDIV_BY_3, [346](#)
SCG_SPLL_CLOCK_PREDIV_BY_4, [347](#)
SCG_SPLL_CLOCK_PREDIV_BY_5, [347](#)
SCG_SPLL_CLOCK_PREDIV_BY_6, [347](#)
SCG_SPLL_CLOCK_PREDIV_BY_7, [347](#)
SCG_SPLL_CLOCK_PREDIV_BY_8, [347](#)
SCG_SPLL_MONITOR_DISABLE, [347](#)
SCG_SPLL_MONITOR_INT, [347](#)
SCG_SPLL_MONITOR_RESET, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_1, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_10, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_11, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_12, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_13, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_14, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_15, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_16, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_2, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_3, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_4, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_5, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_6, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_7, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_8, [347](#)
SCG_SYSTEM_CLOCK_DIV_BY_9, [347](#)
SCG_SYSTEM_CLOCK_SRC_FIRC, [347](#)
SCG_SYSTEM_CLOCK_SRC_NONE, [347](#)
SCG_SYSTEM_CLOCK_SRC_SIRC, [347](#)
SCG_SYSTEM_CLOCK_SRC_SYS_OSC, [347](#)
SIM_CLKOUT_DIV_BY_1, [348](#)
SIM_CLKOUT_DIV_BY_2, [348](#)
SIM_CLKOUT_DIV_BY_3, [348](#)
SIM_CLKOUT_DIV_BY_4, [348](#)
SIM_CLKOUT_DIV_BY_5, [348](#)
SIM_CLKOUT_DIV_BY_6, [348](#)
SIM_CLKOUT_DIV_BY_7, [348](#)
SIM_CLKOUT_DIV_BY_8, [348](#)
SIM_CLKOUT_SEL_SYSTEM_BUS_CLK, [348](#)
SIM_CLKOUT_SEL_SYSTEM_FIRC_DIV2_CLK, [348](#)
SIM_CLKOUT_SEL_SYSTEM_HCLK, [348](#)
SIM_CLKOUT_SEL_SYSTEM_LPO_128K_CLK, [348](#)
SIM_CLKOUT_SEL_SYSTEM_LPO_CLK, [348](#)
SIM_CLKOUT_SEL_SYSTEM_RTC_CLK, [348](#)
SIM_CLKOUT_SEL_SYSTEM_SCG_CLKOUT, [348](#)
SIM_CLKOUT_SEL_SYSTEM_SIRC_DIV2_CLK, [348](#)
SIM_CLKOUT_SEL_SYSTEM_SOSC_DIV2_CLK, [348](#)
SIM_CLKOUT_SEL_SYSTEM_SPLL_DIV2_CLK, [348](#)
SIM_LPO_CLK_SEL_LPO_128K, [348](#)
SIM_LPO_CLK_SEL_LPO_1K, [348](#)
SIM_LPO_CLK_SEL_LPO_32K, [348](#)
SIM_LPO_CLK_SEL_NO_CLOCK, [348](#)
SIM_RTCCLK_SEL_FIRCDIV1_CLK, [349](#)
SIM_RTCCLK_SEL_LPO_32K, [349](#)
SIM_RTCCLK_SEL_RTC_CLKIN, [349](#)
SIM_RTCCLK_SEL_SOSCDIV1_CLK, [349](#)
SLOW_CLK_INDEX, [342](#)
STOP_MODE, [344](#)
SYS_CLK_MAX_NO, [342](#)
scg_async_clock_div_t, [344](#)

- scg_clockout_src_t, [344](#)
- scg_firc_range_t, [344](#)
- scg_sirc_range_t, [345](#)
- scg_sosc_ext_ref_t, [345](#)
- scg_sosc_gain_t, [345](#)
- scg_sosc_monitor_mode_t, [345](#)
- scg_sosc_range_t, [345](#)
- scg_spill_clock_multiply_t, [345](#)
- scg_spill_clock_prediv_t, [346](#)
- scg_spill_monitor_mode_t, [347](#)
- scg_system_clock_div_t, [347](#)
- scg_system_clock_src_t, [347](#)
- sim_clkout_div_t, [347](#)
- sim_clkout_src_t, [348](#)
- sim_lpoclk_sel_src_t, [348](#)
- sim_rtc_clk_sel_src_t, [348](#)
- VLPR_MODE, [344](#)
- VLPS_MODE, [344](#)
- XOSC_EXT_REF, [349](#)
- XOSC_INT_OSC, [349](#)
- xosc_ref_t, [349](#)
- clock_manager_callback_t
 - Clock Manager Driver, [342](#)
- clock_manager_callback_type_t
 - Clock Manager Driver, [342](#)
- clock_manager_callback_user_config_t, [339](#)
 - callback, [340](#)
 - callbackData, [340](#)
 - callbackType, [340](#)
- clock_manager_notify_t
 - Clock Manager Driver, [343](#)
- clock_manager_policy_t
 - Clock Manager Driver, [343](#)
- clock_manager_state_t, [340](#)
 - callbackConfig, [340](#)
 - callbackNum, [340](#)
 - clockConfigNum, [340](#)
 - configTable, [340](#)
 - curConfigIndex, [340](#)
 - errorCallbackIndex, [340](#)
- clock_manager_user_config_t, [336](#)
 - pccConfig, [337](#)
 - pmcConfig, [337](#)
 - scgConfig, [337](#)
 - simConfig, [337](#)
- clock_notify_struct_t, [339](#)
 - notifyType, [339](#)
 - policy, [339](#)
 - targetClockConfigIndex, [339](#)
- clock_source_config_t, [338](#)
 - div, [338](#)
 - enable, [338](#)
 - mul, [338](#)
 - outputDiv1, [338](#)
 - outputDiv2, [339](#)
 - refClk, [339](#)
 - refFreq, [339](#)
- clock_src
 - qspi_user_config_t, [1311](#)
- clock_trace_src_t
 - Clock Manager Driver, [343](#)
- clock_user_config_t
 - Clock Manager Driver, [342](#)
- clockConfigNum
 - clock_manager_state_t, [340](#)
- clockDivide
 - adc_converter_config_t, [255](#)
 - extension_adc_s32k1xx_t, [275](#)
- clockModeConfig
 - scg_config_t, [334](#)
- clockName
 - peripheral_clock_config_t, [335](#)
- clockOutConfig
 - rtc_init_config_t, [1002](#)
 - scg_config_t, [334](#)
 - sim_clock_config_t, [327](#)
- clockPhase
 - flexio_spi_master_user_config_t, [562](#)
 - flexio_spi_slave_user_config_t, [563](#)
 - spi_master_t, [1104](#)
 - spi_slave_t, [1106](#)
- clockPolarity
 - flexio_spi_master_user_config_t, [562](#)
 - flexio_spi_slave_user_config_t, [563](#)
 - spi_master_t, [1104](#)
 - spi_slave_t, [1106](#)
- clockSelect
 - extension_ftm_for_timer_t, [1160](#)
 - extension_lptmr_for_timer_t, [1160](#)
 - lptmr_config_t, [794](#)
 - rtc_init_config_t, [1002](#)
- close
 - WOLFSSL_BIO, [1344](#)
- closeNotify
 - Options, [1301](#)
- cm
 - WOLFSSL_CRL, [1350](#)
 - WOLFSSL_CTX, [1352](#)
 - WOLFSSL_OCSP, [1366](#)
 - WOLFSSL_X509_STORE, [1378](#)
- cmc
 - sbc_can_ctr_t, [1179](#)
- cmd
 - csec_state_t, [300](#)
- cmdInProgress
 - csec_state_t, [300](#)
- cmp_anmux_t, [368](#)
 - negativeInputMux, [368](#)
 - negativePortMux, [368](#)
 - positiveInputMux, [369](#)
 - positivePortMux, [369](#)
- cmp_ch_list_t
 - Comparator Driver, [371](#)
- cmp_ch_number_t
 - Comparator Driver, [371](#)
- cmp_comparator_t, [367](#)

- dmaTriggerState, [367](#)
- filterSampleCount, [367](#)
- filterSamplePeriod, [367](#)
- hysteresisLevel, [367](#)
- inverterState, [367](#)
- mode, [368](#)
- outputInterruptTrigger, [368](#)
- outputSelect, [368](#)
- pinState, [368](#)
- powerMode, [368](#)
- cmp_dac_t, [369](#)
 - state, [369](#)
 - voltage, [369](#)
 - voltageReferenceSource, [369](#)
- cmp_fixed_port_t
 - Comparator Driver, [371](#)
- cmp_hysteresis_t
 - Comparator Driver, [371](#)
- cmp_inverter_t
 - Comparator Driver, [372](#)
- cmp_mode_t
 - Comparator Driver, [372](#)
- cmp_module_t, [370](#)
 - comparator, [370](#)
 - dac, [370](#)
 - mux, [371](#)
 - triggerMode, [371](#)
- cmp_output_enable_t
 - Comparator Driver, [372](#)
- cmp_output_select_t
 - Comparator Driver, [372](#)
- cmp_output_trigger_t
 - Comparator Driver, [373](#)
- cmp_port_mux_t
 - Comparator Driver, [373](#)
- cmp_power_mode_t
 - Comparator Driver, [373](#)
- cmp_trigger_mode_t, [369](#)
 - fixedChannel, [370](#)
 - fixedPort, [370](#)
 - programedState, [370](#)
 - roundRobinChannelsState, [370](#)
 - roundRobinInterruptState, [370](#)
 - roundRobinState, [370](#)
 - samples, [370](#)
- cmp_voltage_reference_t
 - Comparator Driver, [373](#)
- cnIdx
 - DecodedName, [1270](#)
- cnLen
 - DecodedName, [1270](#)
- cntByte
 - lin_state_t, [727](#)
- code
 - WOLFSSL_ALERT, [1340](#)
- coll_resolv_schd
 - lin_associate_frame_t, [831](#)
- columnAddr
 - qspi_user_config_t, [1311](#)
- commandType
 - fs45_tx_data_t, [1283](#)
- Common Core API., [355](#)
 - BUS_ACTIVITY_SET, [355](#)
 - ERROR_IN_RESPONSE, [355](#)
 - EVENT_TRIGGER_COLLISION_SET, [355](#)
 - GO_TO_SLEEP_SET, [355](#)
 - OVERRUN, [355](#)
 - SAVE_CONFIG_SET, [356](#)
 - SUCCESSFULL_TRANSFER, [356](#)
- Common Transport Layer API, [357](#)
 - DIAG_SERVICE_CALLBACK_HANDLER, [357](#)
 - GENERAL_REJECT, [357](#)
 - LD_ANY_FUNCTION, [358](#)
 - LD_ANY_MESSAGE, [358](#)
 - LD_ANY_SUPPLIER, [358](#)
 - LD_BROADCAST, [358](#)
 - LD_DATA_ERROR, [358](#)
 - LD_FUNCTIONAL_NAD, [358](#)
 - LD_LENGTH_NOT_CORRECT, [358](#)
 - LD_LENGTH_TOO_SHORT, [358](#)
 - LD_READ_OK, [358](#)
 - LD_SET_OK, [358](#)
 - LIN_PRODUCT_ID, [358](#)
 - LIN_SERIAL_NUMBER, [359](#)
 - lin_diag_service_callback, [360](#)
 - NEGATIVE, [359](#)
 - POSITIVE, [359](#)
 - RECEIVING, [359](#)
 - RES_NEGATIVE, [359](#)
 - RES_POSITIVE, [359](#)
 - SERVICE_NOT_SUPPORTED, [359](#)
 - SERVICE_TARGET_RESET, [359](#)
 - SUBFUNCTION_NOT_SUPPORTED, [359](#)
 - TRANSMITTING, [359](#)
- compVal1
 - adc_compare_config_t, [257](#)
- compVal2
 - adc_compare_config_t, [257](#)
- comparator
 - cmp_module_t, [370](#)
- Comparator (CMP), [361](#)
- Comparator Driver, [365](#)
 - CMP_AVAILABLE, [372](#)
 - CMP_BOTH_EDGES, [373](#)
 - CMP_CONTINUOUS, [372](#)
 - CMP_COUT, [373](#)
 - CMP_COUTA, [373](#)
 - CMP_DAC, [373](#)
 - CMP_DISABLED, [372](#)
 - CMP_DRV_ClearInputFlags, [374](#)
 - CMP_DRV_ClearOutputFlags, [374](#)
 - CMP_DRV_ConfigComparator, [374](#)
 - CMP_DRV_ConfigDAC, [374](#)
 - CMP_DRV_ConfigMUX, [375](#)
 - CMP_DRV_ConfigTriggerMode, [375](#)
 - CMP_DRV_GetComparatorConfig, [375](#)

- CMP_DRV_GetConfigAll, [376](#)
- CMP_DRV_GetDACConfig, [376](#)
- CMP_DRV_GetDefaultConfig, [376](#)
- CMP_DRV_GetInitConfigAll, [376](#)
- CMP_DRV_GetInitConfigComparator, [377](#)
- CMP_DRV_GetInitConfigDAC, [377](#)
- CMP_DRV_GetInitConfigMUX, [377](#)
- CMP_DRV_GetInitTriggerMode, [378](#)
- CMP_DRV_GetInputFlags, [378](#)
- CMP_DRV_GetMUXConfig, [378](#)
- CMP_DRV_GetOutputFlags, [378](#)
- CMP_DRV_GetTriggerModeConfig, [379](#)
- CMP_DRV_Init, [379](#)
- CMP_DRV_Reset, [379](#)
- CMP_FALLING_EDGE, [373](#)
- CMP_HIGH_SPEED, [373](#)
- CMP_INPUT_FLAGS_MASK, [371](#)
- CMP_INPUT_FLAGS_SHIFT, [371](#)
- CMP_INVERT, [372](#)
- CMP_LEVEL_HYS_0, [372](#)
- CMP_LEVEL_HYS_1, [372](#)
- CMP_LEVEL_HYS_2, [372](#)
- CMP_LEVEL_HYS_3, [372](#)
- CMP_LOW_SPEED, [373](#)
- CMP_MINUS_FIXED, [371](#)
- CMP_MUX, [373](#)
- CMP_NO_EVENT, [373](#)
- CMP_NORMAL, [372](#)
- CMP_PLUS_FIXED, [371](#)
- CMP_RISING_EDGE, [373](#)
- CMP_ROUND_ROBIN_CHANNELS_MASK, [371](#)
- CMP_ROUND_ROBIN_CHANNELS_SHIFT, [371](#)
- CMP_SAMPLED_FILTERED_EXT_CLK, [372](#)
- CMP_SAMPLED_FILTERED_INT_CLK, [372](#)
- CMP_SAMPLED_NONFILTERED_EXT_CLK, [372](#)
- CMP_SAMPLED_NONFILTERED_INT_CLK, [372](#)
- CMP_UNAVAILABLE, [372](#)
- CMP_VIN1, [373](#)
- CMP_VIN2, [373](#)
- CMP_WINDOWED, [372](#)
- CMP_WINDOWED_FILTERED, [372](#)
- CMP_WINDOWED_RESAMPLED, [372](#)
- cmp_ch_list_t, [371](#)
- cmp_ch_number_t, [371](#)
- cmp_fixed_port_t, [371](#)
- cmp_hysteresis_t, [371](#)
- cmp_inverter_t, [372](#)
- cmp_mode_t, [372](#)
- cmp_output_enable_t, [372](#)
- cmp_output_select_t, [372](#)
- cmp_output_trigger_t, [373](#)
- cmp_port_mux_t, [373](#)
- cmp_power_mode_t, [373](#)
- cmp_voltage_reference_t, [373](#)
- compareEnable
 - adc_compare_config_t, [257](#)
- compareGreaterThanEnable
 - adc_compare_config_t, [257](#)
- compareHigh
 - ewm_init_config_t, [470](#)
- compareLow
 - ewm_init_config_t, [470](#)
- compareRangeFuncEnable
 - adc_compare_config_t, [257](#)
- compareValue
 - lptmr_config_t, [794](#)
- comparedValue
 - ftm_output_cmp_ch_param_t, [633](#)
 - oc_output_ch_param_t, [922](#)
- compensation
 - rtc_init_config_t, [1002](#)
- compensationInterval
 - rtc_init_config_t, [1002](#)
- complementChecksum
 - crc_user_config_t, [290](#)
- complementaryChannelPolarity
 - pwm_channel_t, [989](#)
- configTable
 - clock_manager_state_t, [340](#)
- configs
 - power_manager_state_t, [969](#)
- configsNumber
 - power_manager_state_t, [969](#)
- configured_NAD_ptr
 - lin_node_attribute_t, [830](#)
- connReset
 - Options, [1301](#)
- connectState
 - Options, [1301](#)
- consumed
 - EncryptedInfo, [1281](#)
- context
 - WOLF_EVENT, [1334](#)
- continuousConvEn
 - adc_group_config_t, [273](#)
- continuousConvEnable
 - adc_converter_config_t, [255](#)
- continuousModeEn
 - channel_extension_ftm_for_ic_t, [688](#)
 - ftm_input_ch_param_t, [622](#)
- continuousModeEnable
 - pdb_timer_config_t, [933](#)
- control
 - enet_buffer_descriptor_t, [446](#)
 - sbc_factories_conf_t, [1183](#)
- controlRegisterLock
 - rtc_register_lock_config_t, [1005](#)
- Controller Area Network - Peripheral Abstraction Layer (CAN PAL), [381](#)
 - CAN_AbortTransfer, [391](#)
 - CAN_CLK_SOURCE_OSC, [390](#)
 - CAN_CLK_SOURCE_PERIPH, [390](#)
 - CAN_ConfigRemoteResponseBuff, [391](#)
 - CAN_ConfigRxBuff, [392](#)
 - CAN_ConfigTxBuff, [392](#)
 - CAN_DISABLE_MODE, [391](#)

- CAN_Deinit, [393](#)
- CAN_FD_DATA_BITRATE, [390](#)
- CAN_GetBitrate, [393](#)
- CAN_GetDefaultConfig, [393](#)
- CAN_GetTransferStatus, [393](#)
- CAN_Init, [394](#)
- CAN_InstallEventCallback, [394](#)
- CAN_LOOPBACK_MODE, [391](#)
- CAN_MSG_ID_EXT, [391](#)
- CAN_MSG_ID_STD, [391](#)
- CAN_NOMINAL_BITRATE, [390](#)
- CAN_NORMAL_MODE, [391](#)
- CAN_PAYLOAD_SIZE_16, [390](#)
- CAN_PAYLOAD_SIZE_32, [391](#)
- CAN_PAYLOAD_SIZE_64, [391](#)
- CAN_PAYLOAD_SIZE_8, [390](#)
- CAN_Receive, [394](#)
- CAN_ReceiveBlocking, [395](#)
- CAN_Send, [395](#)
- CAN_SendBlocking, [396](#)
- CAN_SetBitrate, [396](#)
- CAN_SetRxFilter, [396](#)
- can_bitrate_phase_t, [390](#)
- can_clk_source_t, [390](#)
- can_fd_payload_size_t, [390](#)
- can_msg_id_type_t, [391](#)
- can_operation_modes_t, [391](#)
- Controller Area Network with Flexible Data Rate (FlexCAN), [398](#)
- Cooked API, [400](#)
 - ld_receive_message, [400](#)
 - ld_rx_status, [400](#)
 - ld_send_message, [401](#)
 - ld_tx_status, [401](#)
- coscs
 - sbc_trans_stat_t, [1185](#)
- count
 - pcc_config_t, [335](#)
 - ProcPeerCertArgs, [1308](#)
 - WOLF_EVENT_QUEUE, [1335](#)
 - WOLFSSL_X509_CHAIN, [1375](#)
- countMutex
 - WOLFSSL_CTX, [1352](#)
- counter
 - ftm_quad_decoder_state_t, [657](#)
- counter1024
 - HC128, [1286](#)
- counterDirection
 - ftm_quad_decoder_state_t, [657](#)
- counterUnits
 - lptmr_config_t, [794](#)
- cpnc
 - sbc_can_ctr_t, [1179](#)
- cpncCanPartNetCfg
 - uja113x_init_cfg_t, [184](#)
- cpnerr
 - sbc_trans_stat_t, [1185](#)
- cpns
 - sbc_trans_stat_t, [1185](#)
- crc_spec_t, [247](#)
 - init, [247](#)
 - poly, [247](#)
 - refIn, [247](#)
 - refOut, [248](#)
 - xorOut, [248](#)
- crc_transpose_t
 - CRC Driver, [290](#)
- crc_user_config_t, [289](#)
 - complementChecksum, [290](#)
 - seed, [290](#)
 - writeTranspose, [290](#)
- crl
 - WOLFSSL_CERT_MANAGER, [1347](#)
 - WOLFSSL_X509_OBJECT, [1377](#)
- crlCheckAll
 - WOLFSSL_CERT_MANAGER, [1347](#)
- crlEnabled
 - WOLFSSL_CERT_MANAGER, [1347](#)
- crlList
 - WOLFSSL_CRL, [1350](#)
- crlLock
 - WOLFSSL_CRL, [1350](#)
- Cryptographic Services Engine (CSEc), [402](#)
- cs
 - can_message_t, [388](#)
 - flexcan_msgbuff_t, [513](#)
- csHoldTime
 - qspi_user_config_t, [1312](#)
- csSetupTime
 - qspi_user_config_t, [1312](#)
- csec_boot_flavor_t
 - CSEc Driver, [302](#)
- csec_call_sequence_t
 - CSEc Driver, [302](#)
- csec_cmd_t
 - CSEc Driver, [303](#)
- csec_key_id_t
 - CSEc Driver, [303](#)
- csec_state_t, [299](#)
 - callback, [300](#)
 - callbackParam, [300](#)
 - cmd, [300](#)
 - cmdInProgress, [300](#)
 - errCode, [300](#)
 - fullSize, [300](#)
 - index, [300](#)
 - inputBuff, [300](#)
 - iv, [300](#)
 - keyId, [300](#)
 - mac, [300](#)
 - macLen, [300](#)
 - macWritten, [301](#)
 - msgLen, [301](#)
 - outputBuff, [301](#)
 - partSize, [301](#)
 - seq, [301](#)

- verifStatus, [301](#)
- csec_status_t
 - CSEc Driver, [302](#)
- cts
 - sbc_trans_stat_t, [1186](#)
- ctx
 - EncryptedInfo, [1281](#)
 - WOLFSSL, [1337](#)
- ctx_ready
 - callback_functions, [1255](#)
- curConfigIndex
 - clock_manager_state_t, [340](#)
- curRL
 - WOLFSSL, [1337](#)
- curSize
 - WOLFSSL, [1337](#)
- current_cert
 - WOLFSSL_X509_STORE_CTX, [1379](#)
- current_id
 - lin_protocol_state_t, [841](#)
- currentConfig
 - power_manager_state_t, [969](#)
- currentEventId
 - lin_state_t, [727](#)
- currentId
 - lin_state_t, [727](#)
- currentNodeState
 - lin_state_t, [727](#)
- currentPid
 - lin_state_t, [727](#)
- curve_idx
 - WOLFSSL_EC_GROUP, [1359](#)
- curve_nid
 - WOLFSSL_EC_GROUP, [1359](#)
- curve_oid
 - WOLFSSL_EC_GROUP, [1359](#)
- cw
 - sbc_trans_evnt_stat_t, [1188](#)
- cwe
 - sbc_trans_evnt_t, [1179](#)
- Cyclic Redundancy Check (CRC), [403](#)
- d
 - RsaKey, [1316](#)
 - WOLFSSL_RSA, [1367](#)
- DADDR
 - edma_software_tcd_t, [421](#)
- DAYS_IN_A_LEAP_YEAR
 - RTC Driver, [1005](#)
- DAYS_IN_A_YEAR
 - RTC Driver, [1005](#)
- dCert
 - ProcPeerCertArgs, [1308](#)
- dCertInit
 - ProcPeerCertArgs, [1308](#)
- DFLASH_IFR_READRESOURCE_ADDRESS
 - Flash Memory (Flash), [487](#)
- DFlashBase
 - Flash Memory (Flash), [500](#), [501](#)
- DFlashSize
 - Flash Memory (Flash), [501](#)
- DIAG_INTERLEAVE_MODE
 - Low level API, [846](#)
- DIAG_NO_RESPONSE
 - Low level API, [846](#)
- DIAG_NONE
 - Low level API, [846](#)
- DIAG_NOT_START
 - Low level API, [846](#)
- DIAG_ONLY_MODE
 - Low level API, [846](#)
- DIAG_RESPONSE
 - Low level API, [846](#)
- DIAG_SERVICE_CALLBACK_HANDLER
 - Common Transport Layer API, [357](#)
- DID1_ADDRESS
 - Register address map, [1026](#)
- DID2_ADDRESS
 - Register address map, [1026](#)
- DIVIDE_BY_EIGHTH
 - Clock Manager Driver, [343](#)
- DIVIDE_BY_FIVE
 - Clock Manager Driver, [343](#)
- DIVIDE_BY_FOUR
 - Clock Manager Driver, [343](#)
- DIVIDE_BY_ONE
 - Clock Manager Driver, [343](#)
- DIVIDE_BY_SEVEN
 - Clock Manager Driver, [343](#)
- DIVIDE_BY_SIX
 - Clock Manager Driver, [343](#)
- DIVIDE_BY_THREE
 - Clock Manager Driver, [343](#)
- DIVIDE_BY_TWO
 - Clock Manager Driver, [343](#)
- DLAST_SGA
 - edma_software_tcd_t, [421](#)
- DLC_0
 - 01. CAN & CAN partial networking configuration, [195](#)
- DLC_1
 - 01. CAN & CAN partial networking configuration, [195](#)
- DLC_2
 - 01. CAN & CAN partial networking configuration, [195](#)
- DLC_3
 - 01. CAN & CAN partial networking configuration, [195](#)
- DLC_4
 - 01. CAN & CAN partial networking configuration, [195](#)
- DLC_5
 - 01. CAN & CAN partial networking configuration, [195](#)
- DLC_6

- 01. CAN & CAN partial networking configuration, [195](#)
- DLC_7
 - 01. CAN & CAN partial networking configuration, [195](#)
- DLC_8
 - 01. CAN & CAN partial networking configuration, [195](#)
- DM0_ADDRESS
 - Register address map, [1026](#)
- DM1_ADDRESS
 - Register address map, [1026](#)
- DM2_ADDRESS
 - Register address map, [1026](#)
- DM3_ADDRESS
 - Register address map, [1027](#)
- DM4_ADDRESS
 - Register address map, [1027](#)
- DM5_ADDRESS
 - Register address map, [1027](#)
- DM6_ADDRESS
 - Register address map, [1027](#)
- DM7_ADDRESS
 - Register address map, [1027](#)
- DNS_entry, [1275](#)
 - name, [1275](#)
 - next, [1275](#)
- DOFF
 - edma_software_tcd_t, [422](#)
- dP
 - RsaKey, [1317](#)
- dQ
 - RsaKey, [1317](#)
- DR_ADDRESS
 - Register address map, [1027](#)
- dac
 - cmp_module_t, [370](#)
- datRate
 - sbc_can_conf_t, [1180](#)
- data
 - can_message_t, [388](#)
 - enet_buffer_t, [446](#)
 - flexcan_msgbuff_t, [513](#)
 - RsaKey, [1316](#)
 - WOLFSSL_ASN1_BIT_STRING, [1341](#)
 - WOLFSSL_ASN1_INTEGER, [1341](#)
 - WOLFSSL_ASN1_STRING, [1343](#)
 - WOLFSSL_ASN1_TIME, [1343](#)
 - WOLFSSL_STACK, [1371](#)
 - WOLFSSL_X509_OBJECT, [1377](#)
- data_length
 - flexcan_data_info_t, [515](#)
- dataBitrate
 - can_user_config_t, [389](#)
- datalsAlloc
 - RsaKey, [1316](#)
- dataLen
 - flexcan_msgbuff_t, [513](#)
 - RsaKey, [1316](#)
- dataLenCode
 - uja113x_cpnc_cfg_t, [191](#)
- dataMask
 - eim_user_channel_config_t, [437](#)
 - sbc_can_conf_t, [1180](#)
- dataPin
 - flexio_uart_user_config_t, [575](#)
- dataPinRx
 - extension_flexio_for_uart_t, [1215](#)
- dataPinTx
 - extension_flexio_for_uart_t, [1215](#)
- dataRate
 - qspi_user_config_t, [1312](#)
- day
 - rtc_timedate_t, [1001](#)
- DckeArgs, [1262](#)
 - begin, [1263](#)
 - idx, [1263](#)
 - lastErr, [1263](#)
 - length, [1263](#)
 - output, [1263](#)
 - sigSz, [1263](#)
- DcvArgs, [1263](#)
 - begin, [1263](#)
 - hashAlgo, [1263](#)
 - idx, [1264](#)
 - output, [1264](#)
 - sendSz, [1264](#)
 - sigAlgo, [1264](#)
 - sigSz, [1264](#)
 - sz, [1264](#)
- deadTime
 - ftm_combined_ch_param_t, [646](#)
 - ftm_independent_ch_param_t, [645](#)
- deadTimePrescaler
 - ftm_pwm_param_t, [648](#)
- deadTimeValue
 - ftm_pwm_param_t, [648](#)
- deadtime
 - pwm_channel_t, [989](#)
- deadtimePrescaler
 - pwm_ftm_timebase_t, [988](#)
- debug
 - wdg_option_mode_t, [1224](#)
 - wdog_op_mode_t, [1233](#)
- DecodedCert, [1264](#)
 - afterDate, [1265](#)
 - afterDateLen, [1265](#)
 - altEmailNames, [1265](#)
 - altNames, [1266](#)
 - beforeDate, [1266](#)
 - beforeDateLen, [1266](#)
 - ca, [1266](#)
 - certBegin, [1266](#)
 - excludedNames, [1266](#)
 - extAuthInfo, [1266](#)
 - extAuthInfoSz, [1266](#)

- extAuthKeyId, [1266](#)
- extAuthKeyIdSet, [1266](#)
- extCrlInfo, [1266](#)
- extCrlInfoSz, [1266](#)
- extExtKeyUsage, [1267](#)
- extExtKeyUsageSet, [1267](#)
- extKeyUsage, [1267](#)
- extKeyUsageSet, [1267](#)
- extNameConstraintSet, [1267](#)
- extSubjKeyId, [1267](#)
- extSubjKeyIdSet, [1267](#)
- extensions, [1266](#)
- extensionsIdx, [1266](#)
- extensionsSz, [1266](#)
- heap, [1267](#)
- isCA, [1267](#)
- issuer, [1267](#)
- issuerHash, [1267](#)
- keyOID, [1267](#)
- maxIdx, [1267](#)
- pathLength, [1267](#)
- pathLengthSet, [1267](#)
- permittedNames, [1268](#)
- pubKeySize, [1268](#)
- pubKeyStored, [1268](#)
- publicKey, [1268](#)
- serial, [1268](#)
- serialSz, [1268](#)
- sigCtx, [1268](#)
- sigIndex, [1268](#)
- sigLength, [1268](#)
- signature, [1268](#)
- signatureOID, [1268](#)
- source, [1268](#)
- srclIdx, [1268](#)
- subject, [1268](#)
- subjectCN, [1268](#)
- subjectCNEnc, [1269](#)
- subjectCNLen, [1269](#)
- subjectCNStored, [1269](#)
- subjectHash, [1269](#)
- subjectRaw, [1269](#)
- subjectRawLen, [1269](#)
- verify, [1269](#)
- version, [1269](#)
- weOwnAltNames, [1269](#)
- DecodedName, [1269](#)
 - cldx, [1270](#)
 - cLen, [1270](#)
 - cnldx, [1270](#)
 - cnLen, [1270](#)
 - emailldx, [1270](#)
 - emailLen, [1270](#)
 - entryCount, [1270](#)
 - fullName, [1270](#)
 - fullNameLen, [1270](#)
 - lldx, [1270](#)
 - lLen, [1271](#)
 - oldx, [1271](#)
 - oLen, [1271](#)
 - ouldx, [1271](#)
 - ouLen, [1271](#)
 - serialldx, [1271](#)
 - serialLen, [1271](#)
 - snldx, [1271](#)
 - snLen, [1271](#)
 - stldx, [1271](#)
 - stLen, [1271](#)
 - uidldx, [1271](#)
 - uidLen, [1271](#)
- decrypt
 - WOLFSSL, [1337](#)
- decryptedCur
 - Keys, [1291](#)
- DefaultISR
 - Interrupt Manager (Interrupt), [710](#)
- delay
 - phy_config_t, [946](#)
- delay_integer
 - lin_schedule_data_t, [833](#)
- delayArray
 - adc_group_config_t, [273](#)
- delayType
 - adc_group_config_t, [274](#)
- depth
 - __blake2b_param, [1243](#)
 - __blake2s_param, [1245](#)
- DerBuffer, [1272](#)
 - buffer, [1272](#)
 - dynType, [1272](#)
 - heap, [1272](#)
 - length, [1272](#)
 - type, [1272](#)
- derCert
 - WOLFSSL_X509, [1373](#)
- Des, [1272](#)
 - key, [1273](#)
 - reg, [1273](#)
 - tmp, [1273](#)
- des
 - WOLFSSL_Cipher, [1349](#)
- Des3, [1273](#)
 - heap, [1273](#)
 - key, [1273](#)
 - reg, [1273](#)
 - tmp, [1273](#)
- des3
 - Ciphers, [1258](#)
 - WOLFSSL_Cipher, [1349](#)
- destAddr
 - edma_transfer_config_t, [419](#)
- destLastAddrAdjust
 - edma_transfer_config_t, [419](#)
- destModulo
 - edma_transfer_config_t, [420](#)
- destOffset

- edma_transfer_config_t, [420](#)
- destTransferSize
 - edma_transfer_config_t, [420](#)
- dev
 - WOLF_EVENT, [1334](#)
- devId
 - SignatureCtx, [1322](#)
 - WOLFSSL, [1337](#)
 - WOLFSSL_CTX, [1352](#)
- deviceStatus
 - fs45_rx_data_t, [1051](#)
- deviceStatusEx
 - fs45_rx_data_t, [1051](#)
- DhKey, [1274](#)
 - g, [1274](#)
 - heap, [1274](#)
 - p, [1274](#)
- dhKeySz
 - Options, [1301](#)
- DhParams, [1274](#)
 - g, [1274](#)
 - g_len, [1274](#)
 - p, [1275](#)
 - p_len, [1275](#)
- diag_IO_control
 - Diagnostic services, [407](#)
- diag_clear_flag
 - Diagnostic services, [406](#)
- diag_fault_memory_clear
 - Diagnostic services, [406](#)
- diag_fault_memory_read
 - Diagnostic services, [406](#)
- diag_get_flag
 - Diagnostic services, [407](#)
- diag_interleave_state
 - lin_tl_descriptor_t, [835](#)
- diag_interleaved_state_t
 - Low level API, [845](#)
- diag_read_data_by_identifier
 - Diagnostic services, [407](#)
- diag_session_control
 - Diagnostic services, [408](#)
- diag_state
 - lin_tl_descriptor_t, [835](#)
- diag_write_data_by_identifier
 - Diagnostic services, [408](#)
- Diagnostic services, [405](#)
 - diag_IO_control, [407](#)
 - diag_clear_flag, [406](#)
 - diag_fault_memory_clear, [406](#)
 - diag_fault_memory_read, [406](#)
 - diag_get_flag, [407](#)
 - diag_read_data_by_identifier, [407](#)
 - diag_session_control, [408](#)
 - diag_write_data_by_identifier, [408](#)
- diagnostic_class
 - lin_protocol_user_config_t, [838](#)
- diagnostic_mode
 - lin_protocol_state_t, [841](#)
- digest
 - Buffers, [1252](#)
 - CertSignCtx, [1257](#)
 - Md4, [1293](#)
 - Md5, [1294](#)
 - Sha, [1320](#)
 - Sha256, [1321](#)
 - SignatureCtx, [1322](#)
- digest_length
 - __blake2b_param, [1243](#)
 - __blake2s_param, [1245](#)
- digestSz
 - BuildMsgArgs, [1255](#)
 - SignatureCtx, [1322](#)
- dir
 - ReadDirCtx, [1315](#)
- direction
 - flexio_uart_user_config_t, [575](#)
 - pin_settings_config_t, [959](#)
- dis8s
 - fs45_sf_impact_reg_t, [1059](#)
- disableAutoneg
 - Generic PHY, [665](#)
 - phy_driver_t, [948](#)
- disableConfig
 - TJA110x PHY, [1144](#)
- disableLink
 - TJA110x PHY, [1144](#)
- discardSessionCerts
 - WOLFSSL_X509_STORE_CTX, [1379](#)
- div
 - clock_source_config_t, [338](#)
 - module_clk_config_t, [337](#)
- div1
 - scg_firc_config_t, [330](#)
 - scg_sirc_config_t, [329](#)
 - scg_sosc_config_t, [328](#)
 - scg_spill_config_t, [331](#)
- div2
 - scg_firc_config_t, [330](#)
 - scg_sirc_config_t, [329](#)
 - scg_sosc_config_t, [328](#)
 - scg_spill_config_t, [331](#)
- divBus
 - scg_system_clock_config_t, [327](#)
- divCore
 - scg_system_clock_config_t, [327](#)
- divEnable
 - sim_trace_clock_config_t, [326](#)
- divFraction
 - sim_trace_clock_config_t, [326](#)
- divSlow
 - scg_system_clock_config_t, [327](#)
- divider
 - peripheral_clock_config_t, [335](#)
 - qspi_user_config_t, [1312](#)
 - sim_clock_out_config_t, [323](#)

- sim_trace_clock_config_t, 326
- dividers
 - sys_clk_config_t, 338
- dlc
 - sbc_frame_t, 1180
- dm0
 - uja113x_dm_cfg_t, 192
- dm1
 - uja113x_dm_cfg_t, 192
- dm2
 - uja113x_dm_cfg_t, 192
- dm3
 - uja113x_dm_cfg_t, 192
- dm4
 - uja113x_dm_cfg_t, 193
- dm5
 - uja113x_dm_cfg_t, 193
- dm6
 - uja113x_dm_cfg_t, 193
- dm7
 - uja113x_dm_cfg_t, 193
- dmCanDataMaskCfg
 - uja113x_init_cfg_t, 184
- DmaChannel
 - sai_user_config_t, 1039
- dmaChannel
 - flexio_uart_user_config_t, 575
 - i2c_slave_t, 698
 - lpi2c_master_user_config_t, 746
 - lpi2c_slave_user_config_t, 747
 - qspi_user_config_t, 1312
- dmaChannel1
 - i2c_master_t, 697
- dmaChannel2
 - i2c_master_t, 697
- dmaEnable
 - adc_converter_config_t, 255
 - pdb_timer_config_t, 933
- dmaRequest
 - lptmr_config_t, 794
- dmaSupport
 - flash_mx25l6433f_user_config_t, 885
 - qspi_user_config_t, 1312
- dmaTriggerState
 - cmp_comparator_t, 367
- dmp1
 - WOLFSSL_RSA, 1367
- dmq1
 - WOLFSSL_RSA, 1367
- domain
 - ProcPeerCertArgs, 1308
 - WOLFSSL_X509_STORE_CTX, 1379
- domainName
 - Buffers, 1252
- downgrade
 - Options, 1301
 - WOLFSSL_METHOD, 1366
- dozeMode
 - qspi_user_config_t, 1312
- dp
 - fp_int, 1282
 - mp_int, 1295
- dqsDelay
 - qspi_user_config_t, 1312
- dqsInvert
 - qspi_user_config_t, 1312
- drbg
 - WC_RNG, 1333
- Driver and cluster management, 409
 - l_sys_init, 409
- driverType
 - flexio_i2c_master_user_config_t, 534
 - flexio_i2s_master_user_config_t, 544
 - flexio_i2s_slave_user_config_t, 545
 - flexio_spi_master_user_config_t, 562
 - flexio_spi_slave_user_config_t, 563
 - flexio_uart_user_config_t, 575
- drv_config_t, 1275
 - isInit, 1276
 - lpspiIntace, 1276
 - watchdogCtr, 1276
- DsaKey, 1276
 - g, 1276
 - heap, 1276
 - p, 1276
 - q, 1276
 - type, 1276
 - x, 1276
 - y, 1277
- DskeArgs, 1277
 - begin, 1277
 - hashAlgo, 1277
 - idx, 1277
 - output, 1277
 - sigAlgo, 1277
 - sigSz, 1277
 - verifySig, 1277
 - verifySigSz, 1277
- dstOffsetEnable
 - edma_loop_transfer_config_t, 418
- dtls
 - Options, 1301
- DtlsFrag, 1278
 - begin, 1278
 - end, 1278
 - next, 1278
- DtlsHandShakeHeader, 1278
 - fragment_length, 1279
 - fragment_offset, 1279
 - length, 1279
 - message_seq, 1279
 - type, 1279
- DtlsMsg, 1279
 - buf, 1279
 - fragList, 1279
 - fragSz, 1279

- msg, [1279](#)
- next, [1280](#)
- seq, [1280](#)
- sz, [1280](#)
- type, [1280](#)
- DtlsRecordLayerHeader, [1280](#)
 - length, [1280](#)
 - pvMajor, [1280](#)
 - pvMinor, [1280](#)
 - sequence_number, [1280](#)
 - type, [1280](#)
- dummy
 - lpspi_state_t, [778](#)
- duration
 - fs45_int_reg_t, [1055](#)
- duty
 - pwm_channel_t, [989](#)
- dynType
 - DerBuffer, [1272](#)
- dynamic
 - WOLFSSL_ASN1_OBJECT, [1342](#)
- dynamicFlag
 - bufferStatic, [1254](#)
- dynamicMemory
 - WOLFSSL_X509, [1373](#)
- dynamicName
 - WOLFSSL_X509_NAME, [1376](#)
- e
 - RsaKey, [1317](#)
 - WOLFSSL_RSA, [1368](#)
- EDMA Driver, [410](#)
 - EDMA_ARBITRATION_FIXED_PRIORITY, [423](#)
 - EDMA_ARBITRATION_ROUND_ROBIN, [423](#)
 - EDMA_CHN_DEFAULT_PRIORITY, [423](#)
 - EDMA_CHN_ERR_INT, [423](#)
 - EDMA_CHN_ERROR, [424](#)
 - EDMA_CHN_HALF_MAJOR_LOOP_INT, [423](#)
 - EDMA_CHN_MAJOR_LOOP_INT, [423](#)
 - EDMA_CHN_NORMAL, [424](#)
 - EDMA_CHN_PRIORITY_0, [423](#)
 - EDMA_CHN_PRIORITY_1, [423](#)
 - EDMA_CHN_PRIORITY_10, [423](#)
 - EDMA_CHN_PRIORITY_11, [423](#)
 - EDMA_CHN_PRIORITY_12, [423](#)
 - EDMA_CHN_PRIORITY_13, [423](#)
 - EDMA_CHN_PRIORITY_14, [423](#)
 - EDMA_CHN_PRIORITY_15, [423](#)
 - EDMA_CHN_PRIORITY_2, [423](#)
 - EDMA_CHN_PRIORITY_3, [423](#)
 - EDMA_CHN_PRIORITY_4, [423](#)
 - EDMA_CHN_PRIORITY_5, [423](#)
 - EDMA_CHN_PRIORITY_6, [423](#)
 - EDMA_CHN_PRIORITY_7, [423](#)
 - EDMA_CHN_PRIORITY_8, [423](#)
 - EDMA_CHN_PRIORITY_9, [423](#)
 - EDMA_DRV_CancelTransfer, [425](#)
 - EDMA_DRV_Channellnit, [425](#)
 - EDMA_DRV_ClearTCD, [426](#)
 - EDMA_DRV_ConfigLoopTransfer, [426](#)
 - EDMA_DRV_ConfigMultiBlockTransfer, [426](#)
 - EDMA_DRV_ConfigScatterGatherTransfer, [427](#)
 - EDMA_DRV_ConfigSingleBlockTransfer, [428](#)
 - EDMA_DRV_ConfigureInterrupt, [428](#)
 - EDMA_DRV_Deinit, [428](#)
 - EDMA_DRV_DisableRequestsOnTransfer↔
Complete, [428](#)
 - EDMA_DRV_GetChannelStatus, [429](#)
 - EDMA_DRV_GetRemainingMajorIterationsCount,
[429](#)
 - EDMA_DRV_Init, [429](#)
 - EDMA_DRV_InstallCallback, [430](#)
 - EDMA_DRV_PushConfigToReg, [430](#)
 - EDMA_DRV_PushConfigToSTCD, [430](#)
 - EDMA_DRV_ReleaseChannel, [431](#)
 - EDMA_DRV_SetChannelRequestAndTrigger, [431](#)
 - EDMA_DRV_SetDestAddr, [431](#)
 - EDMA_DRV_SetDestLastAddrAdjustment, [431](#)
 - EDMA_DRV_SetDestOffset, [432](#)
 - EDMA_DRV_SetDestWriteChunkSize, [432](#)
 - EDMA_DRV_SetMajorLoopIterationCount, [432](#)
 - EDMA_DRV_SetMinorLoopBlockSize, [432](#)
 - EDMA_DRV_SetScatterGatherLink, [432](#)
 - EDMA_DRV_SetSrcAddr, [433](#)
 - EDMA_DRV_SetSrcLastAddrAdjustment, [433](#)
 - EDMA_DRV_SetSrcOffset, [433](#)
 - EDMA_DRV_SetSrcReadChunkSize, [433](#)
 - EDMA_DRV_StartChannel, [433](#)
 - EDMA_DRV_StopChannel, [434](#)
 - EDMA_DRV_TriggerSwRequest, [434](#)
 - EDMA_ERR_LSB_MASK, [422](#)
 - EDMA_MODULO_128B, [424](#)
 - EDMA_MODULO_128KB, [424](#)
 - EDMA_MODULO_128MB, [424](#)
 - EDMA_MODULO_16B, [424](#)
 - EDMA_MODULO_16KB, [424](#)
 - EDMA_MODULO_16MB, [424](#)
 - EDMA_MODULO_1GB, [424](#)
 - EDMA_MODULO_1KB, [424](#)
 - EDMA_MODULO_1MB, [424](#)
 - EDMA_MODULO_256B, [424](#)
 - EDMA_MODULO_256KB, [424](#)
 - EDMA_MODULO_256MB, [424](#)
 - EDMA_MODULO_2B, [424](#)
 - EDMA_MODULO_2GB, [424](#)
 - EDMA_MODULO_2KB, [424](#)
 - EDMA_MODULO_2MB, [424](#)
 - EDMA_MODULO_32B, [424](#)
 - EDMA_MODULO_32KB, [424](#)
 - EDMA_MODULO_32MB, [424](#)
 - EDMA_MODULO_4B, [424](#)
 - EDMA_MODULO_4KB, [424](#)
 - EDMA_MODULO_4MB, [424](#)
 - EDMA_MODULO_512B, [424](#)
 - EDMA_MODULO_512KB, [424](#)
 - EDMA_MODULO_512MB, [424](#)
 - EDMA_MODULO_64B, [424](#)

- EDMA_MODULO_64KB, [424](#)
- EDMA_MODULO_64MB, [424](#)
- EDMA_MODULO_8B, [424](#)
- EDMA_MODULO_8KB, [424](#)
- EDMA_MODULO_8MB, [424](#)
- EDMA_MODULO_OFF, [424](#)
- EDMA_TRANSFER_MEM2MEM, [425](#)
- EDMA_TRANSFER_MEM2PERIPH, [425](#)
- EDMA_TRANSFER_PERIPH2MEM, [425](#)
- EDMA_TRANSFER_PERIPH2PERIPH, [425](#)
- EDMA_TRANSFER_SIZE_1B, [425](#)
- EDMA_TRANSFER_SIZE_2B, [425](#)
- EDMA_TRANSFER_SIZE_4B, [425](#)
- edma_arbitration_algorithm_t, [422](#)
- edma_callback_t, [422](#)
- edma_channel_interrupt_t, [423](#)
- edma_channel_priority_t, [423](#)
- edma_chn_status_t, [423](#)
- edma_modulo_t, [424](#)
- edma_transfer_size_t, [424](#)
- edma_transfer_type_t, [425](#)
- STCD_ADDR, [422](#)
- STCD_SIZE, [422](#)
- EDMA_ARBITRATION_FIXED_PRIORITY
 - EDMA Driver, [423](#)
- EDMA_ARBITRATION_ROUND_ROBIN
 - EDMA Driver, [423](#)
- EDMA_CHN_DEFAULT_PRIORITY
 - EDMA Driver, [423](#)
- EDMA_CHN_ERR_INT
 - EDMA Driver, [423](#)
- EDMA_CHN_ERROR
 - EDMA Driver, [424](#)
- EDMA_CHN_HALF_MAJOR_LOOP_INT
 - EDMA Driver, [423](#)
- EDMA_CHN_MAJOR_LOOP_INT
 - EDMA Driver, [423](#)
- EDMA_CHN_NORMAL
 - EDMA Driver, [424](#)
- EDMA_CHN_PRIORITY_0
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_1
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_10
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_11
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_12
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_13
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_14
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_15
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_2
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_3
 - EDMA Driver, [423](#)
- EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_4
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_5
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_6
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_7
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_8
 - EDMA Driver, [423](#)
- EDMA_CHN_PRIORITY_9
 - EDMA Driver, [423](#)
- EDMA_DRV_CancelTransfer
 - EDMA Driver, [425](#)
- EDMA_DRV_ChannelInit
 - EDMA Driver, [425](#)
- EDMA_DRV_ClearTCD
 - EDMA Driver, [426](#)
- EDMA_DRV_ConfigLoopTransfer
 - EDMA Driver, [426](#)
- EDMA_DRV_ConfigMultiBlockTransfer
 - EDMA Driver, [426](#)
- EDMA_DRV_ConfigScatterGatherTransfer
 - EDMA Driver, [427](#)
- EDMA_DRV_ConfigSingleBlockTransfer
 - EDMA Driver, [428](#)
- EDMA_DRV_ConfigureInterrupt
 - EDMA Driver, [428](#)
- EDMA_DRV_Deinit
 - EDMA Driver, [428](#)
- EDMA_DRV_DisableRequestsOnTransferComplete
 - EDMA Driver, [428](#)
- EDMA_DRV_GetChannelStatus
 - EDMA Driver, [429](#)
- EDMA_DRV_GetRemainingMajorIterationsCount
 - EDMA Driver, [429](#)
- EDMA_DRV_Init
 - EDMA Driver, [429](#)
- EDMA_DRV_InstallCallback
 - EDMA Driver, [430](#)
- EDMA_DRV_PushConfigToReg
 - EDMA Driver, [430](#)
- EDMA_DRV_PushConfigToSTCD
 - EDMA Driver, [430](#)
- EDMA_DRV_ReleaseChannel
 - EDMA Driver, [431](#)
- EDMA_DRV_SetChannelRequestAndTrigger
 - EDMA Driver, [431](#)
- EDMA_DRV_SetDestAddr
 - EDMA Driver, [431](#)
- EDMA_DRV_SetDestLastAddrAdjustment
 - EDMA Driver, [431](#)
- EDMA_DRV_SetDestOffset
 - EDMA Driver, [432](#)
- EDMA_DRV_SetDestWriteChunkSize
 - EDMA Driver, [432](#)
- EDMA_DRV_SetMajorLoopIterationCount

- EDMA Driver, [432](#)
- EDMA_DRV_SetMinorLoopBlockSize
 - EDMA Driver, [432](#)
- EDMA_DRV_SetScatterGatherLink
 - EDMA Driver, [432](#)
- EDMA_DRV_SetSrcAddr
 - EDMA Driver, [433](#)
- EDMA_DRV_SetSrcLastAddrAdjustment
 - EDMA Driver, [433](#)
- EDMA_DRV_SetSrcOffset
 - EDMA Driver, [433](#)
- EDMA_DRV_SetSrcReadChunkSize
 - EDMA Driver, [433](#)
- EDMA_DRV_StartChannel
 - EDMA Driver, [433](#)
- EDMA_DRV_StopChannel
 - EDMA Driver, [434](#)
- EDMA_DRV_TriggerSwRequest
 - EDMA Driver, [434](#)
- EDMA_ERR_LSB_MASK
 - EDMA Driver, [422](#)
- EDMA_MODULO_128B
 - EDMA Driver, [424](#)
- EDMA_MODULO_128KB
 - EDMA Driver, [424](#)
- EDMA_MODULO_128MB
 - EDMA Driver, [424](#)
- EDMA_MODULO_16B
 - EDMA Driver, [424](#)
- EDMA_MODULO_16KB
 - EDMA Driver, [424](#)
- EDMA_MODULO_16MB
 - EDMA Driver, [424](#)
- EDMA_MODULO_1GB
 - EDMA Driver, [424](#)
- EDMA_MODULO_1KB
 - EDMA Driver, [424](#)
- EDMA_MODULO_1MB
 - EDMA Driver, [424](#)
- EDMA_MODULO_256B
 - EDMA Driver, [424](#)
- EDMA_MODULO_256KB
 - EDMA Driver, [424](#)
- EDMA_MODULO_256MB
 - EDMA Driver, [424](#)
- EDMA_MODULO_2B
 - EDMA Driver, [424](#)
- EDMA_MODULO_2GB
 - EDMA Driver, [424](#)
- EDMA_MODULO_2KB
 - EDMA Driver, [424](#)
- EDMA_MODULO_2MB
 - EDMA Driver, [424](#)
- EDMA_MODULO_32B
 - EDMA Driver, [424](#)
- EDMA_MODULO_32KB
 - EDMA Driver, [424](#)
- EDMA_MODULO_32MB
 - EDMA Driver, [424](#)
- EDMA Driver, [424](#)
- EDMA_MODULO_4B
 - EDMA Driver, [424](#)
- EDMA_MODULO_4KB
 - EDMA Driver, [424](#)
- EDMA_MODULO_4MB
 - EDMA Driver, [424](#)
- EDMA_MODULO_512B
 - EDMA Driver, [424](#)
- EDMA_MODULO_512KB
 - EDMA Driver, [424](#)
- EDMA_MODULO_512MB
 - EDMA Driver, [424](#)
- EDMA_MODULO_64B
 - EDMA Driver, [424](#)
- EDMA_MODULO_64KB
 - EDMA Driver, [424](#)
- EDMA_MODULO_64MB
 - EDMA Driver, [424](#)
- EDMA_MODULO_8B
 - EDMA Driver, [424](#)
- EDMA_MODULO_8KB
 - EDMA Driver, [424](#)
- EDMA_MODULO_8MB
 - EDMA Driver, [424](#)
- EDMA_MODULO_OFF
 - EDMA Driver, [424](#)
- EDMA_TRANSFER_MEM2MEM
 - EDMA Driver, [425](#)
- EDMA_TRANSFER_MEM2PERIPH
 - EDMA Driver, [425](#)
- EDMA_TRANSFER_PERIPH2MEM
 - EDMA Driver, [425](#)
- EDMA_TRANSFER_PERIPH2PERIPH
 - EDMA Driver, [425](#)
- EDMA_TRANSFER_SIZE_1B
 - EDMA Driver, [425](#)
- EDMA_TRANSFER_SIZE_2B
 - EDMA Driver, [425](#)
- EDMA_TRANSFER_SIZE_4B
 - EDMA Driver, [425](#)
- EEE_COMPLETE_INTERRUPT_QUICK_WRITE
 - Flash Memory (Flash), [491](#)
- EEE_DISABLE
 - Flash Memory (Flash), [491](#)
- EEE_ENABLE
 - Flash Memory (Flash), [491](#)
- EEE_QUICK_WRITE
 - Flash Memory (Flash), [491](#)
- EEE_STATUS_QUERY
 - Flash Memory (Flash), [491](#)
- EEESize
 - Flash Memory (Flash), [501](#)
- EERAMBase
 - Flash Memory (Flash), [501](#)
- EIM Driver, [435](#)
- EIM_CHECKBITMASK_DEFAULT, [437](#)
- EIM_DATAMASK_DEFAULT, [437](#)

- EIM_DRV_ConfigChannel, [438](#)
- EIM_DRV_Deinit, [438](#)
- EIM_DRV_GetChannelConfig, [438](#)
- EIM_DRV_GetDefaultConfig, [438](#)
- EIM_DRV_Init, [439](#)
- EIM_CHECKBITMASK_DEFAULT
 - EIM Driver, [437](#)
- EIM_DATAMASK_DEFAULT
 - EIM Driver, [437](#)
- EIM_DRV_ConfigChannel
 - EIM Driver, [438](#)
- EIM_DRV_Deinit
 - EIM Driver, [438](#)
- EIM_DRV_GetChannelConfig
 - EIM Driver, [438](#)
- EIM_DRV_GetDefaultConfig
 - EIM Driver, [438](#)
- EIM_DRV_Init
 - EIM Driver, [439](#)
- ENC_HIGH_N
 - 03. Fail-safe configuration, [219](#)
- ENC_HIGH_NRS
 - 03. Fail-safe configuration, [219](#)
- ENC_LOW
 - 03. Fail-safe configuration, [219](#)
- ENC_TIMER
 - 03. Fail-safe configuration, [219](#)
- ENET Driver, [440](#)
 - ENET_BABR_INTERRUPT, [455](#)
 - ENET_BABT_INTERRUPT, [455](#)
 - ENET_BUFF_ALIGN, [451](#)
 - ENET_BUFF_IS_ALIGNED, [451](#)
 - ENET_BUFFDESCR_ALIGN, [451](#)
 - ENET_BUFFDESCR_IS_ALIGNED, [451](#)
 - ENET_CTR_IEEE_R_ALIGN, [454](#)
 - ENET_CTR_IEEE_R_CRC, [454](#)
 - ENET_CTR_IEEE_R_DROP, [454](#)
 - ENET_CTR_IEEE_R_FDXFC, [454](#)
 - ENET_CTR_IEEE_R_FRAME_OK, [454](#)
 - ENET_CTR_IEEE_R_MACERR, [454](#)
 - ENET_CTR_IEEE_R_OCTETS_OK, [454](#)
 - ENET_CTR_IEEE_T_1COL, [453](#)
 - ENET_CTR_IEEE_T_CSERR, [454](#)
 - ENET_CTR_IEEE_T_DEF, [453](#)
 - ENET_CTR_IEEE_T_DROP, [453](#)
 - ENET_CTR_IEEE_T_EXCOL, [454](#)
 - ENET_CTR_IEEE_T_FDXFC, [454](#)
 - ENET_CTR_IEEE_T_FRAME_OK, [453](#)
 - ENET_CTR_IEEE_T_LCOL, [454](#)
 - ENET_CTR_IEEE_T_MACERR, [454](#)
 - ENET_CTR_IEEE_T_MCOL, [453](#)
 - ENET_CTR_IEEE_T_OCTETS_OK, [454](#)
 - ENET_CTR_IEEE_T_SQE, [454](#)
 - ENET_CTR_RMON_R_BC_PKT, [454](#)
 - ENET_CTR_RMON_R_CRC_ALIGN, [454](#)
 - ENET_CTR_RMON_R_FRAG, [454](#)
 - ENET_CTR_RMON_R_JAB, [454](#)
 - ENET_CTR_RMON_R_MC_PKT, [454](#)
 - ENET_CTR_RMON_R_OCTETS, [454](#)
 - ENET_CTR_RMON_R_OVERSIZE, [454](#)
 - ENET_CTR_RMON_R_P1024TO2047, [454](#)
 - ENET_CTR_RMON_R_P128TO255, [454](#)
 - ENET_CTR_RMON_R_P256TO511, [454](#)
 - ENET_CTR_RMON_R_P512TO1023, [454](#)
 - ENET_CTR_RMON_R_P64, [454](#)
 - ENET_CTR_RMON_R_P65TO127, [454](#)
 - ENET_CTR_RMON_R_P_GTE2048, [454](#)
 - ENET_CTR_RMON_R_PACKETS, [454](#)
 - ENET_CTR_RMON_R_RESVD_0, [454](#)
 - ENET_CTR_RMON_R_UNDERSIZE, [454](#)
 - ENET_CTR_RMON_T_BC_PKT, [453](#)
 - ENET_CTR_RMON_T_COL, [453](#)
 - ENET_CTR_RMON_T_CRC_ALIGN, [453](#)
 - ENET_CTR_RMON_T_DROP, [453](#)
 - ENET_CTR_RMON_T_FRAG, [453](#)
 - ENET_CTR_RMON_T_JAB, [453](#)
 - ENET_CTR_RMON_T_MC_PKT, [453](#)
 - ENET_CTR_RMON_T_OCTETS, [453](#)
 - ENET_CTR_RMON_T_OVERSIZE, [453](#)
 - ENET_CTR_RMON_T_P1024TO2047, [453](#)
 - ENET_CTR_RMON_T_P128TO255, [453](#)
 - ENET_CTR_RMON_T_P256TO511, [453](#)
 - ENET_CTR_RMON_T_P512TO1023, [453](#)
 - ENET_CTR_RMON_T_P64, [453](#)
 - ENET_CTR_RMON_T_P65TO127, [453](#)
 - ENET_CTR_RMON_T_P_GTE2048, [453](#)
 - ENET_CTR_RMON_T_PACKETS, [453](#)
 - ENET_CTR_RMON_T_UNDERSIZE, [453](#)
 - ENET_DRV_ConfigCounters, [456](#)
 - ENET_DRV_Deinit, [456](#)
 - ENET_DRV_EnableMDIO, [456](#)
 - ENET_DRV_GetCounter, [456](#)
 - ENET_DRV_GetDefaultConfig, [457](#)
 - ENET_DRV_GetInterruptFlags, [457](#)
 - ENET_DRV_GetMacAddr, [457](#)
 - ENET_DRV_GetTransmitStatus, [457](#)
 - ENET_DRV_Init, [458](#)
 - ENET_DRV_MDIORead, [458](#)
 - ENET_DRV_MDIOReadMMD, [458](#)
 - ENET_DRV_MDIOWrite, [459](#)
 - ENET_DRV_MDIOWriteMMD, [459](#)
 - ENET_DRV_ProvideRxBuff, [459](#)
 - ENET_DRV_ReadFrame, [460](#)
 - ENET_DRV_SendFrame, [460](#)
 - ENET_DRV_SetMacAddr, [461](#)
 - ENET_DRV_SetMulticastForward, [461](#)
 - ENET_DRV_SetMulticastForwardAll, [461](#)
 - ENET_DRV_SetSpeed, [461](#)
 - ENET_DRV_SetUnicastForward, [462](#)
 - ENET_EBERR_INTERRUPT, [455](#)
 - ENET_ERR_EVENT, [454](#)
 - ENET_FRAME_MAX_FRAMELEN, [451](#)
 - ENET_GRACE_STOP_INTERRUPT, [455](#)
 - ENET_LATE_COLLISION_INTERRUPT, [455](#)
 - ENET_MII_FULL_DUPLEX, [455](#)
 - ENET_MII_HALF_DUPLEX, [455](#)

- ENET_MII_INTERRUPT, [455](#)
- ENET_MII_MODE, [456](#)
- ENET_MII_SPEED_100M, [456](#)
- ENET_MII_SPEED_10M, [456](#)
- ENET_MIN_BUFFERSIZE, [451](#)
- ENET_PARSER_EVENT, [454](#)
- ENET_RETRY_LIMIT_INTERRUPT, [455](#)
- ENET_RMII_MODE, [456](#)
- ENET_RX_ALMOST_EMPTY, [455](#)
- ENET_RX_ALMOST_FULL, [455](#)
- ENET_RX_BUFFER_INTERRUPT, [455](#)
- ENET_RX_ENH_ERR_COLLISION, [452](#)
- ENET_RX_ENH_ERR_IPHDR_CHECKSUM, [452](#)
- ENET_RX_ENH_ERR_MAC, [452](#)
- ENET_RX_ENH_ERR_PHY, [452](#)
- ENET_RX_ENH_ERR_PROTO_CHECKSUM, [452](#)
- ENET_RX_EVENT, [454](#)
- ENET_RX_FRAME_INTERRUPT, [455](#)
- ENET_RX_SECTION_EMPTY, [455](#)
- ENET_RX_SECTION_FULL, [455](#)
- ENET_TX_ALMOST_EMPTY, [455](#)
- ENET_TX_ALMOST_FULL, [455](#)
- ENET_TX_BUFFER_INTERRUPT, [455](#)
- ENET_TX_ENH_ERR_EXCESS_COLLISION, [452](#)
- ENET_TX_ENH_ERR_FRAME, [452](#)
- ENET_TX_ENH_ERR_LATE_COLLISION, [452](#)
- ENET_TX_ENH_ERR_OVERFLOW, [452](#)
- ENET_TX_ENH_ERR_TIMESTAMP, [452](#)
- ENET_TX_ENH_ERR_UNDERFLOW, [452](#)
- ENET_TX_EVENT, [454](#)
- ENET_TX_FRAME_INTERRUPT, [455](#)
- ENET_TX_SECTION_EMPTY, [455](#)
- ENET_TX_WATERMARK_MASK, [453](#)
- ENET_TX_WATERMARK_SHIFT, [453](#)
- ENET_UNDERRUN_INTERRUPT, [455](#)
- ENET_WAKE_UP_EVENT, [454](#)
- enet_callback_t, [453](#)
- enet_counter_t, [453](#)
- enet_event_t, [454](#)
- enet_fifo_threshold_t, [454](#)
- enet_interrupt_t, [455](#)
- enet_mii_duplex_t, [455](#)
- enet_mii_mode_t, [455](#)
- enet_mii_speed_t, [456](#)
- ENET_BABR_INTERRUPT
 - ENET Driver, [455](#)
- ENET_BABT_INTERRUPT
 - ENET Driver, [455](#)
- ENET_BUFF_ALIGN
 - ENET Driver, [451](#)
- ENET_BUFF_IS_ALIGNED
 - ENET Driver, [451](#)
- ENET_BUFFDESCR_ALIGN
 - ENET Driver, [451](#)
- ENET_BUFFDESCR_IS_ALIGNED
 - ENET Driver, [451](#)
- ENET_CTR_IEEE_R_ALIGN
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_R_CRC
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_R_DROP
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_R_FDXFC
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_R_FRAME_OK
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_R_MACERR
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_R_OCTETS_OK
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_T_1COL
 - ENET Driver, [453](#)
- ENET_CTR_IEEE_T_CSERR
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_T_DEF
 - ENET Driver, [453](#)
- ENET_CTR_IEEE_T_DROP
 - ENET Driver, [453](#)
- ENET_CTR_IEEE_T_EXCOL
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_T_FDXFC
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_T_FRAME_OK
 - ENET Driver, [453](#)
- ENET_CTR_IEEE_T_LCOL
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_T_MACERR
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_T_MCOL
 - ENET Driver, [453](#)
- ENET_CTR_IEEE_T_OCTETS_OK
 - ENET Driver, [454](#)
- ENET_CTR_IEEE_T_SQE
 - ENET Driver, [454](#)
- ENET_CTR_RMON_R_BC_PKT
 - ENET Driver, [454](#)
- ENET_CTR_RMON_R_CRC_ALIGN
 - ENET Driver, [454](#)
- ENET_CTR_RMON_R_FRAG
 - ENET Driver, [454](#)
- ENET_CTR_RMON_R_JAB
 - ENET Driver, [454](#)
- ENET_CTR_RMON_R_MC_PKT
 - ENET Driver, [454](#)
- ENET_CTR_RMON_R_OCTETS
 - ENET Driver, [454](#)
- ENET_CTR_RMON_R_OVERSIZE
 - ENET Driver, [454](#)
- ENET_CTR_RMON_R_P1024TO2047
 - ENET Driver, [454](#)
- ENET_CTR_RMON_R_P128TO255
 - ENET Driver, [454](#)
- ENET_CTR_RMON_R_P256TO511
 - ENET Driver, [454](#)
- ENET_CTR_RMON_R_P512TO1023
 - ENET Driver, [454](#)

ENET_CTR_RMON_R_P64
ENET Driver, [454](#)

ENET_CTR_RMON_R_P65TO127
ENET Driver, [454](#)

ENET_CTR_RMON_R_P_GTE2048
ENET Driver, [454](#)

ENET_CTR_RMON_R_PACKETS
ENET Driver, [454](#)

ENET_CTR_RMON_R_RESVD_0
ENET Driver, [454](#)

ENET_CTR_RMON_R_UNDESIZE
ENET Driver, [454](#)

ENET_CTR_RMON_T_BC_PKT
ENET Driver, [453](#)

ENET_CTR_RMON_T_COL
ENET Driver, [453](#)

ENET_CTR_RMON_T_CRC_ALIGN
ENET Driver, [453](#)

ENET_CTR_RMON_T_DROP
ENET Driver, [453](#)

ENET_CTR_RMON_T_FRAG
ENET Driver, [453](#)

ENET_CTR_RMON_T_JAB
ENET Driver, [453](#)

ENET_CTR_RMON_T_MC_PKT
ENET Driver, [453](#)

ENET_CTR_RMON_T_OCTETS
ENET Driver, [453](#)

ENET_CTR_RMON_T_OVERSIZE
ENET Driver, [453](#)

ENET_CTR_RMON_T_P1024TO2047
ENET Driver, [453](#)

ENET_CTR_RMON_T_P128TO255
ENET Driver, [453](#)

ENET_CTR_RMON_T_P256TO511
ENET Driver, [453](#)

ENET_CTR_RMON_T_P512TO1023
ENET Driver, [453](#)

ENET_CTR_RMON_T_P64
ENET Driver, [453](#)

ENET_CTR_RMON_T_P65TO127
ENET Driver, [453](#)

ENET_CTR_RMON_T_P_GTE2048
ENET Driver, [453](#)

ENET_CTR_RMON_T_PACKETS
ENET Driver, [453](#)

ENET_CTR_RMON_T_UNDESIZE
ENET Driver, [453](#)

ENET_DRV_ConfigCounters
ENET Driver, [456](#)

ENET_DRV_Deinit
ENET Driver, [456](#)

ENET_DRV_EnableMDIO
ENET Driver, [456](#)

ENET_DRV_GetCounter
ENET Driver, [456](#)

ENET_DRV_GetDefaultConfig
ENET Driver, [457](#)

ENET_DRV_GetInterruptFlags
ENET Driver, [457](#)

ENET_DRV_GetMacAddr
ENET Driver, [457](#)

ENET_DRV_GetTransmitStatus
ENET Driver, [457](#)

ENET_DRV_Init
ENET Driver, [458](#)

ENET_DRV_MDIORead
ENET Driver, [458](#)

ENET_DRV_MDIOReadMMD
ENET Driver, [458](#)

ENET_DRV_MDIOWrite
ENET Driver, [459](#)

ENET_DRV_MDIOWriteMMD
ENET Driver, [459](#)

ENET_DRV_ProvideRxBuff
ENET Driver, [459](#)

ENET_DRV_ReadFrame
ENET Driver, [460](#)

ENET_DRV_SendFrame
ENET Driver, [460](#)

ENET_DRV_SetMacAddr
ENET Driver, [461](#)

ENET_DRV_SetMulticastForward
ENET Driver, [461](#)

ENET_DRV_SetMulticastForwardAll
ENET Driver, [461](#)

ENET_DRV_SetSpeed
ENET Driver, [461](#)

ENET_DRV_SetUnicastForward
ENET Driver, [462](#)

ENET_EBERR_INTERRUPT
ENET Driver, [455](#)

ENET_ERR_EVENT
ENET Driver, [454](#)

ENET_FRAME_MAX_FRAMELEN
ENET Driver, [451](#)

ENET_GRACE_STOP_INTERRUPT
ENET Driver, [455](#)

ENET_LATE_COLLISION_INTERRUPT
ENET Driver, [455](#)

ENET_MII_FULL_DUPLEX
ENET Driver, [455](#)

ENET_MII_HALF_DUPLEX
ENET Driver, [455](#)

ENET_MII_INTERRUPT
ENET Driver, [455](#)

ENET_MII_MODE
ENET Driver, [456](#)

ENET_MII_SPEED_100M
ENET Driver, [456](#)

ENET_MII_SPEED_10M
ENET Driver, [456](#)

ENET_MIN_BUFFERSIZE
ENET Driver, [451](#)

ENET_PARSER_EVENT
ENET Driver, [454](#)

- ENET_RETRY_LIMIT_INTERRUPT
 - ENET Driver, [455](#)
- ENET_RMII_MODE
 - ENET Driver, [456](#)
- ENET_RX_ALMOST_EMPTY
 - ENET Driver, [455](#)
- ENET_RX_ALMOST_FULL
 - ENET Driver, [455](#)
- ENET_RX_BUFFER_INTERRUPT
 - ENET Driver, [455](#)
- ENET_RX_ENH_ERR_COLLISION
 - ENET Driver, [452](#)
- ENET_RX_ENH_ERR_IPHDR_CHECKSUM
 - ENET Driver, [452](#)
- ENET_RX_ENH_ERR_MAC
 - ENET Driver, [452](#)
- ENET_RX_ENH_ERR_PHY
 - ENET Driver, [452](#)
- ENET_RX_ENH_ERR_PROTO_CHECKSUM
 - ENET Driver, [452](#)
- ENET_RX_EVENT
 - ENET Driver, [454](#)
- ENET_RX_FRAME_INTERRUPT
 - ENET Driver, [455](#)
- ENET_RX_SECTION_EMPTY
 - ENET Driver, [455](#)
- ENET_RX_SECTION_FULL
 - ENET Driver, [455](#)
- ENET_TX_ALMOST_EMPTY
 - ENET Driver, [455](#)
- ENET_TX_ALMOST_FULL
 - ENET Driver, [455](#)
- ENET_TX_BUFFER_INTERRUPT
 - ENET Driver, [455](#)
- ENET_TX_ENH_ERR_EXCESS_COLLISION
 - ENET Driver, [452](#)
- ENET_TX_ENH_ERR_FRAME
 - ENET Driver, [452](#)
- ENET_TX_ENH_ERR_LATE_COLLISION
 - ENET Driver, [452](#)
- ENET_TX_ENH_ERR_OVERFLOW
 - ENET Driver, [452](#)
- ENET_TX_ENH_ERR_TIMESTAMP
 - ENET Driver, [452](#)
- ENET_TX_ENH_ERR_UNDERFLOW
 - ENET Driver, [452](#)
- ENET_TX_EVENT
 - ENET Driver, [454](#)
- ENET_TX_FRAME_INTERRUPT
 - ENET Driver, [455](#)
- ENET_TX_SECTION_EMPTY
 - ENET Driver, [455](#)
- ENET_TX_WATERMARK_MASK
 - ENET Driver, [453](#)
- ENET_TX_WATERMARK_SHIFT
 - ENET Driver, [453](#)
- ENET_UNDERRUN_INTERRUPT
 - ENET Driver, [455](#)
- ENET_WAKE_UP_EVENT
 - ENET Driver, [454](#)
- ENSC_FULL
 - 03. Fail-safe configuration, [219](#)
- ENSC_NONE
 - 03. Fail-safe configuration, [219](#)
- ENSC_OVERVOLTAGE
 - 03. Fail-safe configuration, [219](#)
- ENSC_UNDRVOLTAGE
 - 03. Fail-safe configuration, [219](#)
- ERM Driver, [463](#)
 - ERM_DRV_ClearEvent, [466](#)
 - ERM_DRV_Deinit, [466](#)
 - ERM_DRV_GetErrorDetail, [466](#)
 - ERM_DRV_GetInterruptConfig, [466](#)
 - ERM_DRV_Init, [467](#)
 - ERM_DRV_SetInterruptConfig, [467](#)
 - ERM_EVENT_NON_CORRECTABLE, [466](#)
 - ERM_EVENT_NONE, [466](#)
 - ERM_EVENT_SINGLE_BIT, [466](#)
 - erm_ecc_event_t, [466](#)
- ERM_DRV_ClearEvent
 - ERM Driver, [466](#)
- ERM_DRV_Deinit
 - ERM Driver, [466](#)
- ERM_DRV_GetErrorDetail
 - ERM Driver, [466](#)
- ERM_DRV_GetInterruptConfig
 - ERM Driver, [466](#)
- ERM_DRV_Init
 - ERM Driver, [467](#)
- ERM_DRV_SetInterruptConfig
 - ERM Driver, [467](#)
- ERM_EVENT_NON_CORRECTABLE
 - ERM Driver, [466](#)
- ERM_EVENT_NONE
 - ERM Driver, [466](#)
- ERM_EVENT_SINGLE_BIT
 - ERM Driver, [466](#)
- ERROR_IN_RESPONSE
 - Common Core API., [355](#)
- EVENT_TRIGGER_COLLISION_SET
 - Common Core API., [355](#)
- EWM Driver, [468](#)
 - EWM_DRV_GetDefaultConfig, [471](#)
 - EWM_DRV_GetInputPinAssertLogic, [471](#)
 - EWM_DRV_Init, [471](#)
 - EWM_DRV_Refresh, [472](#)
 - EWM_IN_ASSERT_DISABLED, [471](#)
 - EWM_IN_ASSERT_ON_LOGIC_ONE, [471](#)
 - EWM_IN_ASSERT_ON_LOGIC_ZERO, [471](#)
 - ewm_in_assert_logic_t, [471](#)
- EWM_DRV_GetDefaultConfig
 - EWM Driver, [471](#)
- EWM_DRV_GetInputPinAssertLogic
 - EWM Driver, [471](#)
- EWM_DRV_Init
 - EWM Driver, [471](#)

EWM_DRV_Refresh
 EWM Driver, [472](#)
 EWM_IN_ASSERT_DISABLED
 EWM Driver, [471](#)
 EWM_IN_ASSERT_ON_LOGIC_ONE
 EWM Driver, [471](#)
 EWM_IN_ASSERT_ON_LOGIC_ZERO
 EWM Driver, [471](#)
 EXTENDED_CTRL_ADDR
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_CONFIG_EN_FLAG
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_LINK_CTRL_FLAG
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_LOOPBACK_MODE_EXTERNAL
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_LOOPBACK_MODE_INTERNAL
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_LOOPBACK_MODE_MASK
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_LOOPBACK_MODE_REMOTE
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_POWER_MODE_MASK
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_POWER_MODE_NORMAL_REQ
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_POWER_MODE_SILENT
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_POWER_MODE_SLEEP
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_POWER_MODE_SLEEP_REQ
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_POWER_MODE_STANDBY
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_TEST_MODE_MASK
 TJA110x PHY, [1142](#)
 EXTENDED_CTRL_TEST_MODE_SHIFT
 TJA110x PHY, [1143](#)
 EXTENDED_CTRL_WAKE_REQ_FLAG
 TJA110x PHY, [1143](#)
 EXTENDED_STATUS_1000BASETFD_FLAG
 Generic PHY, [664](#)
 EXTENDED_STATUS_1000BASETHD_FLAG
 Generic PHY, [665](#)
 EXTENDED_STATUS_ADDR
 Generic PHY, [665](#)
 eccs
 sbc_mtpnv_stat_t, [1190](#)
 edgeAlignement
 ftm_input_ch_param_t, [622](#)
 edma_arbitration_algorithm_t
 EDMA Driver, [422](#)
 edma_callback_t
 EDMA Driver, [422](#)
 edma_channel_config_t, [416](#)
 callback, [417](#)
 callbackParam, [417](#)
 channelPriority, [417](#)
 enableTrigger, [417](#)
 virtChnConfig, [417](#)
 edma_channel_interrupt_t
 EDMA Driver, [423](#)
 edma_channel_priority_t
 EDMA Driver, [423](#)
 edma_chn_state_t, [416](#)
 callback, [416](#)
 parameter, [416](#)
 status, [416](#)
 virtChn, [416](#)
 edma_chn_status_t
 EDMA Driver, [423](#)
 edma_loop_transfer_config_t, [418](#)
 dstOffsetEnable, [418](#)
 majorLoopChnLinkEnable, [418](#)
 majorLoopChnLinkNumber, [418](#)
 majorLoopIterationCount, [418](#)
 minorLoopChnLinkEnable, [419](#)
 minorLoopChnLinkNumber, [419](#)
 minorLoopOffset, [419](#)
 srcOffsetEnable, [419](#)
 edma_modulo_t
 EDMA Driver, [424](#)
 edma_scatter_gather_list_t, [417](#)
 address, [417](#)
 length, [417](#)
 type, [417](#)
 edma_software_tcd_t, [421](#)
 ATTR, [421](#)
 BITER, [421](#)
 CITER, [421](#)
 CSR, [421](#)
 DADDR, [421](#)
 DLAST_SGA, [421](#)
 DOFF, [422](#)
 NBYTES, [422](#)
 SADDR, [422](#)
 SLAST, [422](#)
 SOFF, [422](#)
 edma_state_t, [418](#)
 virtChnState, [418](#)
 edma_transfer_config_t, [419](#)
 destAddr, [419](#)
 destLastAddrAdjust, [419](#)
 destModulo, [420](#)
 destOffset, [420](#)
 destTransferSize, [420](#)
 interruptEnable, [420](#)
 loopTransferConfig, [420](#)
 minorByteTransferCount, [420](#)
 scatterGatherEnable, [420](#)
 scatterGatherNextDescAddr, [420](#)
 srcAddr, [420](#)
 srcLastAddrAdjust, [420](#)
 srcModulo, [421](#)
 srcOffset, [421](#)
 srcTransferSize, [421](#)

- edma_transfer_size_t
 - EDMA Driver, [424](#)
- edma_transfer_type_t
 - EDMA Driver, [425](#)
- edma_user_config_t, [415](#)
 - chnArbitration, [416](#)
 - haltOnError, [416](#)
- eim_user_channel_config_t, [437](#)
 - channel, [437](#)
 - checkBitMask, [437](#)
 - dataMask, [437](#)
 - enable, [437](#)
- ElementSize
 - sai_user_config_t, [1040](#)
- emailIdx
 - DecodedName, [1270](#)
- emailLen
 - DecodedName, [1270](#)
- enCtrl
 - uja113x_fsc_cfg_t, [218](#)
- enDriverCtrl
 - uja113x_fsc_cfg_t, [218](#)
- enShutdownCtrl
 - uja113x_fsc_cfg_t, [218](#)
- enable
 - clock_source_config_t, [338](#)
 - eim_user_channel_config_t, [437](#)
 - pmc_lpo_clock_config_t, [336](#)
 - sim_clock_out_config_t, [323](#)
- enableAutoneg
 - Generic PHY, [665](#)
 - phy_driver_t, [948](#)
- enableBRS
 - can_buff_config_t, [387](#)
- enableComplementaryChannel
 - pwm_channel_t, [989](#)
- enableConfig
 - TJA110x PHY, [1144](#)
- enableDma
 - sim_plat_gate_config_t, [325](#)
- enableEim
 - sim_plat_gate_config_t, [325](#)
- enableErm
 - sim_plat_gate_config_t, [325](#)
- enableExternalTrigger
 - ftm_combined_ch_param_t, [646](#)
 - ftm_independent_ch_param_t, [645](#)
 - ftm_output_cmp_ch_param_t, [633](#)
- enableExternalTriggerOnNextChn
 - ftm_combined_ch_param_t, [646](#)
- enableFD
 - can_buff_config_t, [387](#)
 - can_user_config_t, [389](#)
- enableInLowPower
 - scg_firc_config_t, [330](#)
 - scg_sirc_config_t, [329](#)
 - scg_sosc_config_t, [328](#)
- enableInStop
 - scg_firc_config_t, [330](#)
 - scg_sirc_config_t, [330](#)
 - scg_sosc_config_t, [328](#)
 - scg_spill_config_t, [331](#)
- enableInitializationTrigger
 - ftm_user_config_t, [590](#)
- enableInterrupts
 - phy_driver_t, [948](#)
 - TJA110x PHY, [1144](#)
- enableLink
 - TJA110x PHY, [1144](#)
- enableLpo1k
 - sim_lpo_clock_config_t, [324](#)
- enableLpo32k
 - sim_lpo_clock_config_t, [324](#)
- enableModifiedCombine
 - ftm_combined_ch_param_t, [646](#)
- enableMpu
 - sim_plat_gate_config_t, [325](#)
- enableMscm
 - sim_plat_gate_config_t, [325](#)
- enableNonCorrectable
 - erm_interrupt_config_t, [465](#)
- enableNotification
 - ftm_state_t, [588](#)
- enableQspiRefClk
 - sim_qspi_ref_clk_gating_t, [325](#)
- enableReloadOnTrigger
 - lpit_user_channel_config_t, [762](#)
- enableRunInDebug
 - lpit_user_config_t, [762](#)
- enableRunInDoze
 - lpit_user_config_t, [762](#)
- enableSecondChannelOutput
 - ftm_combined_ch_param_t, [647](#)
 - ftm_independent_ch_param_t, [645](#)
- enableSingleCorrection
 - erm_interrupt_config_t, [465](#)
- enableStartOnTrigger
 - lpit_user_channel_config_t, [762](#)
- enableStopOnInterrupt
 - lpit_user_channel_config_t, [763](#)
- enableTrigger
 - edma_channel_config_t, [417](#)
- enc
 - WOLFSSL_EVP_CIPHER_CTX, [1362](#)
- encSecret
 - SckeArgs, [1318](#)
- encSig
 - CertSignCtx, [1257](#)
- encSigSz
 - CertSignCtx, [1257](#)
- encSz
 - SckeArgs, [1318](#)
- encrypt
 - WOLFSSL, [1337](#)
- encryptSz
 - Keys, [1291](#)

- EncryptedInfo, 1281
 - consumed, 1281
 - ctx, 1281
 - iv, 1281
 - ivSz, 1281
 - name, 1281
 - set, 1281
- encryptionOn
 - Keys, 1291
- end
 - DtlsFrag, 1278
- end_user
 - t_atcert, 1328
- end_user_pubkey
 - t_atcert, 1328
- end_user_size
 - t_atcert, 1328
- endAddr
 - mpu_region_config_t, 874
 - mpu_user_config_t, 863
- endianess
 - qspi_user_config_t, 1312
- enet_buffer_config_t, 447
 - rxBufferAligned, 447
 - rxRingAligned, 447
 - rxRingSize, 447
 - txRingAligned, 447
 - txRingSize, 447
- enet_buffer_descriptor_t, 446
 - buffer, 446
 - control, 446
 - length, 446
- enet_buffer_t, 446
 - data, 446
 - length, 446
- enet_callback_t
 - ENET Driver, 453
- enet_config_t, 447
 - callback, 448
 - interrupts, 448
 - maxFrameLen, 448
 - miiDuplex, 448
 - miiMode, 448
 - miiSpeed, 448
 - ringCount, 448
- enet_counter_t
 - ENET Driver, 453
- enet_event_t
 - ENET Driver, 454
- enet_fifo_threshold_t
 - ENET Driver, 454
- enet_interrupt_t
 - ENET Driver, 455
- enet_mii_duplex_t
 - ENET Driver, 455
- enet_mii_mode_t
 - ENET Driver, 455
- enet_mii_speed_t
 - ENET Driver, 456
- enet_rx_enh_info_t, 449
 - checksum, 449
 - errMask, 450
 - headerLen, 450
 - ipv4Frag, 450
 - ipv6, 450
 - proto, 450
 - timestamp, 450
 - unicast, 450
 - vlanPrio, 450
- enet_state_t, 448
 - callback, 448
 - ringCount, 449
 - rxBdAlloc, 449
 - rxBdBase, 449
 - rxBdCurrent, 449
 - txBdBase, 449
 - txBdCurrent, 449
- enet_tx_enh_info_t, 450
 - errMask, 450
 - timestamp, 451
- enet_tx_options_t, 451
 - noCRC, 451
 - noInt, 451
- enetInstance
 - phy_config_t, 947
- Enhanced Direct Memory Access (eDMA), 473
- entry
 - ReadDirCtx, 1315
- entryCount
 - DecodedName, 1270
- eof
 - WOLFSSL_BIO, 1344
- erm_ecc_event_t
 - ERM Driver, 466
- erm_interrupt_config_t, 465
 - enableNonCorrectable, 465
 - enableSingleCorrection, 465
- erm_user_config_t, 465
 - channel, 465
 - interruptCfg, 465
- err
 - WOLFSSL_CTX, 1352
- errCode
 - csec_state_t, 300
- errMask
 - enet_rx_enh_info_t, 450
 - enet_tx_enh_info_t, 450
- error
 - WOLFSSL, 1337
 - WOLFSSL_X509_STORE_CTX, 1379
- Error Injection Module (EIM), 474
- Error Reporting Module (ERM), 476
- error_callback
 - FlexCANState, 514
- error_depth
 - WOLFSSL_X509_STORE_CTX, 1379

- error_in_res
 - lin_word_status_str_t, [828](#)
- error_in_response
 - lin_protocol_state_t, [841](#)
- errorCallbackIndex
 - clock_manager_state_t, [340](#)
 - power_manager_state_t, [969](#)
- errorCallbackParam
 - FlexCANState, [514](#)
- Ethernet MAC (ENET), [478](#)
- Ethernet Transceiver (PHY), [481](#)
- event_trigger_collision_flg
 - lin_master_data_t, [840](#)
 - lin_word_status_str_t, [828](#)
- events
 - sbc_status_group_t, [1190](#)
- ewm_in_assert_logic_t
 - EWM Driver, [471](#)
- ewm_init_config_t, [470](#)
 - assertLogic, [470](#)
 - compareHigh, [470](#)
 - compareLow, [470](#)
 - interruptEnable, [470](#)
 - prescaler, [470](#)
- ex_data
 - WOLFSSL_X509_STORE_CTX, [1379](#)
- exSet
 - WOLFSSL_DH, [1355](#)
 - WOLFSSL_DSA, [1356](#)
 - WOLFSSL_EC_KEY, [1359](#)
 - WOLFSSL_EC_POINT, [1360](#)
 - WOLFSSL_RSA, [1368](#)
- excludedNames
 - DecodedCert, [1266](#)
 - Signer, [1323](#)
- extAuthInfo
 - DecodedCert, [1266](#)
- extAuthInfoSz
 - DecodedCert, [1266](#)
- extAuthKeyId
 - DecodedCert, [1266](#)
- extAuthKeyIdSet
 - DecodedCert, [1266](#)
- extCrllInfo
 - DecodedCert, [1266](#)
- extCrllInfoSz
 - DecodedCert, [1266](#)
- extExtKeyUsage
 - DecodedCert, [1267](#)
- extExtKeyUsageSet
 - DecodedCert, [1267](#)
- extKeyUsage
 - DecodedCert, [1267](#)
- extKeyUsageSet
 - DecodedCert, [1267](#)
- extNameConstraintSet
 - DecodedCert, [1267](#)
- extPinSrc
 - sim_tclk_config_t, [324](#)
- extRef
 - scg_sosc_config_t, [328](#)
- extSubjKeyId
 - DecodedCert, [1267](#)
- extSubjKeyIdSet
 - DecodedCert, [1267](#)
- extendedConfig
 - phy_config_t, [947](#)
- extendedStatus
 - phy_basicStatus_t, [1307](#)
- extension
 - adc_config_t, [275](#)
 - can_user_config_t, [389](#)
 - i2c_master_t, [697](#)
 - i2s_user_config_t, [677](#)
 - ic_config_t, [688](#)
 - mpu_region_config_t, [874](#)
 - oc_config_t, [922](#)
 - spi_master_t, [1104](#)
 - spi_slave_t, [1106](#)
 - timer_config_t, [1159](#)
 - uart_user_config_t, [1214](#)
 - wdg_config_t, [1225](#)
- extension_adc_s32k1xx_t, [275](#)
 - clockDivide, [275](#)
 - inputClock, [275](#)
 - pdbPrescaler, [275](#)
 - resolution, [276](#)
 - supplyMonitoringEnable, [276](#)
 - voltageRef, [276](#)
- extension_ewm_for_wdg_t, [1224](#)
 - assertLogic, [1224](#)
 - prescalerValue, [1224](#)
- extension_flexcan_rx_fifo_t, [389](#)
 - idFilterTable, [390](#)
 - idFormat, [390](#)
 - numIdFilters, [390](#)
- extension_flexio_for_i2c_t, [696](#)
 - sclPin, [696](#)
 - sdaPin, [696](#)
- extension_flexio_for_i2s_t, [677](#)
 - rxPin, [677](#)
 - sckPin, [678](#)
 - txPin, [678](#)
 - wsPin, [678](#)
- extension_flexio_for_spi_t, [1106](#)
 - misoPin, [1107](#)
 - mosiPin, [1107](#)
 - sckPin, [1107](#)
 - ssPin, [1107](#)
- extension_flexio_for_uart_t, [1215](#)
 - dataPinRx, [1215](#)
 - dataPinTx, [1215](#)
- extension_ftm_for_ic_t, [688](#)
 - ftmClockSource, [689](#)
 - ftmPrescaler, [689](#)
- extension_ftm_for_oc_t, [923](#)

- ftmClockSource, [923](#)
- ftmPrescaler, [923](#)
- maxCountValue, [923](#)
- extension_ftm_for_timer_t, [1160](#)
 - clockSelect, [1160](#)
 - finalValue, [1160](#)
 - prescaler, [1160](#)
- extension_lptmr_for_timer_t, [1159](#)
 - bypassPrescaler, [1160](#)
 - clockSelect, [1160](#)
 - prescaler, [1160](#)
- extensions
 - DecodedCert, [1266](#)
- extensionsIdx
 - DecodedCert, [1266](#)
- extensionsSz
 - DecodedCert, [1266](#)
- External Watchdog Monitor (EWM), [482](#)
- extraSz
 - ScvArgs, [1319](#)
- FC_ADDRESS
 - Register address map, [1027](#)
- FF_pdu_received
 - lin_tl_descriptor_t, [835](#)
- FLASH_CALLBACK_CS
 - Flash Memory (Flash), [487](#)
- FLASH_DRV_CheckSum
 - Flash Memory (Flash), [491](#)
- FLASH_DRV_ClearReadColisionFlag
 - Flash Memory (Flash), [492](#)
- FLASH_DRV_DisableCmdCompleteInterupt
 - Flash Memory (Flash), [492](#)
- FLASH_DRV_DisableReadColisionInterupt
 - Flash Memory (Flash), [492](#)
- FLASH_DRV_EnableCmdCompleteInterupt
 - Flash Memory (Flash), [492](#)
- FLASH_DRV_EnableReadColisionInterupt
 - Flash Memory (Flash), [492](#)
- FLASH_DRV_EraseAllBlock
 - Flash Memory (Flash), [493](#)
- FLASH_DRV_EraseResume
 - Flash Memory (Flash), [493](#)
- FLASH_DRV_EraseSector
 - Flash Memory (Flash), [493](#)
- FLASH_DRV_EraseSuspend
 - Flash Memory (Flash), [494](#)
- FLASH_DRV_GetCmdCompleteFlag
 - Flash Memory (Flash), [494](#)
- FLASH_DRV_GetDefaultConfig
 - Flash Memory (Flash), [495](#)
- FLASH_DRV_GetPFlashProtection
 - Flash Memory (Flash), [495](#)
- FLASH_DRV_GetReadColisionFlag
 - Flash Memory (Flash), [495](#)
- FLASH_DRV_GetSecurityState
 - Flash Memory (Flash), [495](#)
- FLASH_DRV_Init
 - Flash Memory (Flash), [496](#)
- FLASH_DRV_Program
 - Flash Memory (Flash), [496](#)
- FLASH_DRV_ProgramCheck
 - Flash Memory (Flash), [496](#)
- FLASH_DRV_ProgramOnce
 - Flash Memory (Flash), [497](#)
- FLASH_DRV_ReadOnce
 - Flash Memory (Flash), [497](#)
- FLASH_DRV_SecurityBypass
 - Flash Memory (Flash), [498](#)
- FLASH_DRV_SetPFlashProtection
 - Flash Memory (Flash), [498](#)
- FLASH_DRV_VerifyAllBlock
 - Flash Memory (Flash), [499](#)
- FLASH_DRV_VerifySection
 - Flash Memory (Flash), [499](#)
- FLASH_MX25L6433F_DRV_Deinit
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_MX25L6433F_DRV_EnterDPD
 - MX25L6433F Serial Flash Driver, [887](#)
- FLASH_MX25L6433F_DRV_EnterOTP
 - MX25L6433F Serial Flash Driver, [887](#)
- FLASH_MX25L6433F_DRV_Erase32K
 - MX25L6433F Serial Flash Driver, [887](#)
- FLASH_MX25L6433F_DRV_Erase4K
 - MX25L6433F Serial Flash Driver, [887](#)
- FLASH_MX25L6433F_DRV_Erase64K
 - MX25L6433F Serial Flash Driver, [888](#)
- FLASH_MX25L6433F_DRV_EraseAll
 - MX25L6433F Serial Flash Driver, [888](#)
- FLASH_MX25L6433F_DRV_EraseVerify
 - MX25L6433F Serial Flash Driver, [888](#)
- FLASH_MX25L6433F_DRV_ExitDPD
 - MX25L6433F Serial Flash Driver, [888](#)
- FLASH_MX25L6433F_DRV_ExitOTP
 - MX25L6433F Serial Flash Driver, [889](#)
- FLASH_MX25L6433F_DRV_GetDefaultConfig
 - MX25L6433F Serial Flash Driver, [889](#)
- FLASH_MX25L6433F_DRV_GetProtection
 - MX25L6433F Serial Flash Driver, [889](#)
- FLASH_MX25L6433F_DRV_GetSecureLock
 - MX25L6433F Serial Flash Driver, [889](#)
- FLASH_MX25L6433F_DRV_GetStatus
 - MX25L6433F Serial Flash Driver, [890](#)
- FLASH_MX25L6433F_DRV_Init
 - MX25L6433F Serial Flash Driver, [890](#)
- FLASH_MX25L6433F_DRV_Program
 - MX25L6433F Serial Flash Driver, [890](#)
- FLASH_MX25L6433F_DRV_ProgramVerify
 - MX25L6433F Serial Flash Driver, [891](#)
- FLASH_MX25L6433F_DRV_Read
 - MX25L6433F Serial Flash Driver, [891](#)
- FLASH_MX25L6433F_DRV_Reset
 - MX25L6433F Serial Flash Driver, [891](#)
- FLASH_MX25L6433F_DRV_Resume
 - MX25L6433F Serial Flash Driver, [891](#)
- FLASH_MX25L6433F_DRV_STRENGTH_HIGH
 - MX25L6433F Serial Flash Driver, [886](#)

- FLASH_MX25L6433F_DRV_STRENGTH_LOW
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_MX25L6433F_DRV_SetProtection
 - MX25L6433F Serial Flash Driver, [892](#)
- FLASH_MX25L6433F_DRV_SetSecureLock
 - MX25L6433F Serial Flash Driver, [892](#)
- FLASH_MX25L6433F_DRV_Suspend
 - MX25L6433F Serial Flash Driver, [892](#)
- FLASH_MX25L6433F_PROT_DIR_BOTTOM
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_MX25L6433F_PROT_DIR_TOP
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_MX25L6433F_PROT_SIZE_0
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_MX25L6433F_PROT_SIZE_128K
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_MX25L6433F_PROT_SIZE_1M
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_MX25L6433F_PROT_SIZE_256K
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_MX25L6433F_PROT_SIZE_2M
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_MX25L6433F_PROT_SIZE_4M
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_MX25L6433F_PROT_SIZE_512K
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_MX25L6433F_PROT_SIZE_64K
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_MX25L6433F_PROT_SIZE_8M
 - MX25L6433F Serial Flash Driver, [886](#)
- FLASH_NOT_SECURE
 - Flash Memory (Flash), [487](#)
- FLASH_SECURE_BACKDOOR_DISABLED
 - Flash Memory (Flash), [488](#)
- FLASH_SECURE_BACKDOOR_ENABLED
 - Flash Memory (Flash), [488](#)
- FLASH_SECURITY_STATE_KEYEN
 - Flash Memory (Flash), [488](#)
- FLASH_SECURITY_STATE_UNSECURED
 - Flash Memory (Flash), [488](#)
- FLEXCAN_DISABLE_MODE
 - FlexCAN Driver, [518](#)
- FLEXCAN_DRV_AbortTransfer
 - FlexCAN Driver, [520](#)
- FLEXCAN_DRV_ConfigRemoteResponseMb
 - FlexCAN Driver, [520](#)
- FLEXCAN_DRV_ConfigRxFifo
 - FlexCAN Driver, [520](#)
- FLEXCAN_DRV_ConfigRxMb
 - FlexCAN Driver, [521](#)
- FLEXCAN_DRV_ConfigTxMb
 - FlexCAN Driver, [521](#)
- FLEXCAN_DRV_Deinit
 - FlexCAN Driver, [521](#)
- FLEXCAN_DRV_GetBitrate
 - FlexCAN Driver, [521](#)
- FLEXCAN_DRV_GetDefaultConfig
 - FlexCAN Driver, [522](#)
- FLEXCAN_DRV_GetErrorStatus
 - FlexCAN Driver, [522](#)
- FLEXCAN_DRV_GetTransferStatus
 - FlexCAN Driver, [522](#)
- FLEXCAN_DRV_Init
 - FlexCAN Driver, [523](#)
- FLEXCAN_DRV_InstallErrorCallback
 - FlexCAN Driver, [523](#)
- FLEXCAN_DRV_InstallEventCallback
 - FlexCAN Driver, [523](#)
- FLEXCAN_DRV_Receive
 - FlexCAN Driver, [523](#)
- FLEXCAN_DRV_ReceiveBlocking
 - FlexCAN Driver, [524](#)
- FLEXCAN_DRV_RxFifo
 - FlexCAN Driver, [524](#)
- FLEXCAN_DRV_RxFifoBlocking
 - FlexCAN Driver, [524](#)
- FLEXCAN_DRV_Send
 - FlexCAN Driver, [525](#)
- FLEXCAN_DRV_SendBlocking
 - FlexCAN Driver, [525](#)
- FLEXCAN_DRV_SetBitrate
 - FlexCAN Driver, [525](#)
- FLEXCAN_DRV_SetRxFifoGlobalMask
 - FlexCAN Driver, [526](#)
- FLEXCAN_DRV_SetRxIndividualMask
 - FlexCAN Driver, [526](#)
- FLEXCAN_DRV_SetRxMaskType
 - FlexCAN Driver, [526](#)
- FLEXCAN_DRV_SetRxMb14Mask
 - FlexCAN Driver, [526](#)
- FLEXCAN_DRV_SetRxMb15Mask
 - FlexCAN Driver, [527](#)
- FLEXCAN_DRV_SetRxMbGlobalMask
 - FlexCAN Driver, [527](#)
- FLEXCAN_EVENT_ERROR
 - FlexCAN Driver, [518](#)
- FLEXCAN_EVENT_RX_COMPLETE
 - FlexCAN Driver, [518](#)
- FLEXCAN_EVENT_RXFIFO_COMPLETE
 - FlexCAN Driver, [518](#)
- FLEXCAN_EVENT_RXFIFO_OVERFLOW
 - FlexCAN Driver, [518](#)
- FLEXCAN_EVENT_RXFIFO_WARNING
 - FlexCAN Driver, [518](#)
- FLEXCAN_EVENT_TX_COMPLETE
 - FlexCAN Driver, [518](#)
- FLEXCAN_FREEZE_MODE
 - FlexCAN Driver, [518](#)
- FLEXCAN_LISTEN_ONLY_MODE
 - FlexCAN Driver, [518](#)
- FLEXCAN_LOOPBACK_MODE
 - FlexCAN Driver, [518](#)
- FLEXCAN_MB_IDLE
 - FlexCAN Driver, [518](#)
- FLEXCAN_MB_RX_BUSY
 - FlexCAN Driver, [518](#)

- FLEXCAN_MB_TX_BUSY
 - FlexCAN Driver, [518](#)
- FLEXCAN_MSG_ID_EXT
 - FlexCAN Driver, [518](#)
- FLEXCAN_MSG_ID_STD
 - FlexCAN Driver, [518](#)
- FLEXCAN_NORMAL_MODE
 - FlexCAN Driver, [518](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_104
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_112
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_120
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_128
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_16
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_24
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_32
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_40
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_48
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_56
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_64
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_72
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_8
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_80
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_88
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FILTERS_96
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FORMAT_A
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FORMAT_B
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FORMAT_C
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_FIFO_ID_FORMAT_D
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_MASK_GLOBAL
 - FlexCAN Driver, [519](#)
- FLEXCAN_RX_MASK_INDIVIDUAL
 - FlexCAN Driver, [519](#)
- FLEXCAN_RXFIFO_USING_INTERRUPTS
 - FlexCAN Driver, [519](#)
- FLEXIO_DRIVER_TYPE_DMA
 - FlexIO Common Driver, [528](#)
- FLEXIO_DRIVER_TYPE_INTERRUPTS
 - FlexIO Common Driver, [528](#)
- FLEXIO_DRIVER_TYPE_POLLING
 - FlexIO Common Driver, [528](#)
- FLEXIO_DRV_DeinitDevice
 - FlexIO Common Driver, [528](#)
- FLEXIO_DRV_InitDevice
 - FlexIO Common Driver, [530](#)
- FLEXIO_DRV_Reset
 - FlexIO Common Driver, [530](#)
- FLEXIO_I2C_DRV_GenerateNineClock
 - FlexIO I2C Driver, [535](#)
- FLEXIO_I2C_DRV_GetBusStatus
 - FlexIO I2C Driver, [535](#)
- FLEXIO_I2C_DRV_GetDefaultConfig
 - FlexIO I2C Driver, [535](#)
- FLEXIO_I2C_DRV_MasterDeinit
 - FlexIO I2C Driver, [536](#)
- FLEXIO_I2C_DRV_MasterGetBaudRate
 - FlexIO I2C Driver, [536](#)
- FLEXIO_I2C_DRV_MasterGetStatus
 - FlexIO I2C Driver, [536](#)
- FLEXIO_I2C_DRV_MasterInit
 - FlexIO I2C Driver, [536](#)
- FLEXIO_I2C_DRV_MasterReceiveData
 - FlexIO I2C Driver, [537](#)
- FLEXIO_I2C_DRV_MasterReceiveDataBlocking
 - FlexIO I2C Driver, [537](#)
- FLEXIO_I2C_DRV_MasterSendData
 - FlexIO I2C Driver, [537](#)
- FLEXIO_I2C_DRV_MasterSendDataBlocking
 - FlexIO I2C Driver, [538](#)
- FLEXIO_I2C_DRV_MasterSetBaudRate
 - FlexIO I2C Driver, [538](#)
- FLEXIO_I2C_DRV_MasterSetSlaveAddr
 - FlexIO I2C Driver, [539](#)
- FLEXIO_I2C_DRV_MasterTransferAbort
 - FlexIO I2C Driver, [539](#)
- FLEXIO_I2C_DRV_StatusGenerateNineClock
 - FlexIO I2C Driver, [539](#)
- FLEXIO_I2S_DRV_MasterDeinit
 - FlexIO I2S Driver, [546](#)
- FLEXIO_I2S_DRV_MasterGetBaudRate
 - FlexIO I2S Driver, [546](#)
- FLEXIO_I2S_DRV_MasterGetDefaultConfig
 - FlexIO I2S Driver, [547](#)
- FLEXIO_I2S_DRV_MasterGetStatus
 - FlexIO I2S Driver, [547](#)
- FLEXIO_I2S_DRV_MasterInit
 - FlexIO I2S Driver, [547](#)
- FLEXIO_I2S_DRV_MasterReceiveData
 - FlexIO I2S Driver, [548](#)
- FLEXIO_I2S_DRV_MasterReceiveDataBlocking
 - FlexIO I2S Driver, [548](#)
- FLEXIO_I2S_DRV_MasterSendData
 - FlexIO I2S Driver, [548](#)
- FLEXIO_I2S_DRV_MasterSendDataBlocking
 - FlexIO I2S Driver, [549](#)
- FLEXIO_I2S_DRV_MasterSetConfig
 - FlexIO I2S Driver, [549](#)

- FLEXIO_I2S_DRV_MasterSetRxBuffer
FlexIO I2S Driver, [549](#)
- FLEXIO_I2S_DRV_MasterSetTxBuffer
FlexIO I2S Driver, [550](#)
- FLEXIO_I2S_DRV_MasterTransferAbort
FlexIO I2S Driver, [550](#)
- FLEXIO_I2S_DRV_SlaveDeinit
FlexIO I2S Driver, [550](#)
- FLEXIO_I2S_DRV_SlaveGetDefaultConfig
FlexIO I2S Driver, [551](#)
- FLEXIO_I2S_DRV_SlaveGetStatus
FlexIO I2S Driver, [551](#)
- FLEXIO_I2S_DRV_SlaveInit
FlexIO I2S Driver, [551](#)
- FLEXIO_I2S_DRV_SlaveReceiveData
FlexIO I2S Driver, [552](#)
- FLEXIO_I2S_DRV_SlaveReceiveDataBlocking
FlexIO I2S Driver, [552](#)
- FLEXIO_I2S_DRV_SlaveSendData
FlexIO I2S Driver, [553](#)
- FLEXIO_I2S_DRV_SlaveSendDataBlocking
FlexIO I2S Driver, [553](#)
- FLEXIO_I2S_DRV_SlaveSetConfig
FlexIO I2S Driver, [554](#)
- FLEXIO_I2S_DRV_SlaveSetRxBuffer
FlexIO I2S Driver, [554](#)
- FLEXIO_I2S_DRV_SlaveSetTxBuffer
FlexIO I2S Driver, [555](#)
- FLEXIO_I2S_DRV_SlaveTransferAbort
FlexIO I2S Driver, [555](#)
- FLEXIO_SPI_DRV_MasterDeinit
FlexIO SPI Driver, [565](#)
- FLEXIO_SPI_DRV_MasterGetBaudRate
FlexIO SPI Driver, [565](#)
- FLEXIO_SPI_DRV_MasterGetDefaultConfig
FlexIO SPI Driver, [566](#)
- FLEXIO_SPI_DRV_MasterGetStatus
FlexIO SPI Driver, [566](#)
- FLEXIO_SPI_DRV_MasterInit
FlexIO SPI Driver, [566](#)
- FLEXIO_SPI_DRV_MasterSetBaudRate
FlexIO SPI Driver, [566](#)
- FLEXIO_SPI_DRV_MasterTransfer
FlexIO SPI Driver, [567](#)
- FLEXIO_SPI_DRV_MasterTransferAbort
FlexIO SPI Driver, [567](#)
- FLEXIO_SPI_DRV_MasterTransferBlocking
FlexIO SPI Driver, [567](#)
- FLEXIO_SPI_DRV_SlaveDeinit
FlexIO SPI Driver, [568](#)
- FLEXIO_SPI_DRV_SlaveGetDefaultConfig
FlexIO SPI Driver, [568](#)
- FLEXIO_SPI_DRV_SlaveGetStatus
FlexIO SPI Driver, [568](#)
- FLEXIO_SPI_DRV_SlaveInit
FlexIO SPI Driver, [569](#)
- FLEXIO_SPI_DRV_SlaveTransfer
FlexIO SPI Driver, [569](#)
- FLEXIO_SPI_DRV_SlaveTransferAbort
FlexIO SPI Driver, [570](#)
- FLEXIO_SPI_DRV_SlaveTransferBlocking
FlexIO SPI Driver, [570](#)
- FLEXIO_SPI_TRANSFER_1BYTE
FlexIO SPI Driver, [565](#)
- FLEXIO_SPI_TRANSFER_2BYTE
FlexIO SPI Driver, [565](#)
- FLEXIO_SPI_TRANSFER_4BYTE
FlexIO SPI Driver, [565](#)
- FLEXIO_SPI_TRANSFER_LSB_FIRST
FlexIO SPI Driver, [565](#)
- FLEXIO_SPI_TRANSFER_MSB_FIRST
FlexIO SPI Driver, [565](#)
- FLEXIO_UART_DIRECTION_RX
FlexIO UART Driver, [576](#)
- FLEXIO_UART_DIRECTION_TX
FlexIO UART Driver, [576](#)
- FLEXIO_UART_DRV_Deinit
FlexIO UART Driver, [576](#)
- FLEXIO_UART_DRV_GetBaudRate
FlexIO UART Driver, [576](#)
- FLEXIO_UART_DRV_GetDefaultConfig
FlexIO UART Driver, [576](#)
- FLEXIO_UART_DRV_GetStatus
FlexIO UART Driver, [577](#)
- FLEXIO_UART_DRV_Init
FlexIO UART Driver, [577](#)
- FLEXIO_UART_DRV_ReceiveData
FlexIO UART Driver, [577](#)
- FLEXIO_UART_DRV_ReceiveDataBlocking
FlexIO UART Driver, [578](#)
- FLEXIO_UART_DRV_SendData
FlexIO UART Driver, [578](#)
- FLEXIO_UART_DRV_SendDataBlocking
FlexIO UART Driver, [578](#)
- FLEXIO_UART_DRV_SetConfig
FlexIO UART Driver, [579](#)
- FLEXIO_UART_DRV_SetRxBuffer
FlexIO UART Driver, [579](#)
- FLEXIO_UART_DRV_SetTxBuffer
FlexIO UART Driver, [579](#)
- FLEXIO_UART_DRV_TransferAbort
FlexIO UART Driver, [580](#)
- FNMC_DISABLE
SBC configuration control options (0x74), [1077](#)
- FNMC_ENABLE
SBC configuration control options (0x74), [1077](#)
- FS45_CAN_SetMode
SBC FS45 Driver, [1066](#)
- FS45_CheckFS1B
SBC FS45 Driver, [1066](#)
- FS45_CheckLbistAbistOk
SBC FS45 Driver, [1066](#)
- FS45_CheckVAUX
SBC FS45 Driver, [1067](#)
- FS45_GetDefaultInitRegsConfig
SBC FS45 Driver, [1067](#)

- FS45_GetDefaultNonInitRegsConfig
 - SBC FS45 Driver, [1067](#)
- FS45_GetFaultErrorCounterValue
 - SBC FS45 Driver, [1067](#)
- FS45_GetMode
 - SBC FS45 Driver, [1067](#)
- FS45_Init
 - SBC FS45 Driver, [1069](#)
- FS45_LDT_RunCounter
 - SBC FS45 Driver, [1069](#)
- FS45_LDT_SetAfterRunValue
 - SBC FS45 Driver, [1069](#)
- FS45_LDT_SetTimerMode
 - SBC FS45 Driver, [1069](#)
- FS45_LDT_SetTimerOperation
 - SBC FS45 Driver, [1071](#)
- FS45_LDT_SetWakeUpRegSrc
 - SBC FS45 Driver, [1071](#)
- FS45_LDT_SetWakeUpValue
 - SBC FS45 Driver, [1071](#)
- FS45_ReadRegister
 - SBC FS45 Driver, [1071](#)
- FS45_ReleaseFSx
 - SBC FS45 Driver, [1072](#)
- FS45_RequestFSxLow
 - SBC FS45 Driver, [1072](#)
- FS45_RequestInterrupt
 - SBC FS45 Driver, [1072](#)
- FS45_RequestReset
 - SBC FS45 Driver, [1072](#)
- FS45_SetLowPowerMode
 - SBC FS45 Driver, [1072](#)
- FS45_SetOUT4
 - SBC FS45 Driver, [1074](#)
- FS45_SetRegulatorState
 - SBC FS45 Driver, [1074](#)
- FS45_SwitchAMUXchannel
 - SBC FS45 Driver, [1074](#)
- FS45_WD_ChangeSeed
 - SBC FS45 Driver, [1074](#)
- FS45_WD_ChangeWindow
 - SBC FS45 Driver, [1075](#)
- FS45_WD_Refresh
 - SBC FS45 Driver, [1075](#)
- FS45_WriteRegister
 - SBC FS45 Driver, [1075](#)
- FSC_ADDRESS
 - Register address map, [1027](#)
- FTFx_DPHRASE_SIZE
 - Flash Memory (Flash), [488](#)
- FTFx_ERASE_ALL_BLOCK
 - Flash Memory (Flash), [488](#)
- FTFx_ERASE_ALL_BLOCK_UNSECURE
 - Flash Memory (Flash), [488](#)
- FTFx_ERASE_BLOCK
 - Flash Memory (Flash), [488](#)
- FTFx_ERASE_SECTOR
 - Flash Memory (Flash), [488](#)
- FTFx_FSTAT_ERROR_BITS
 - Flash Memory (Flash), [488](#)
- FTFx_LONGWORD_SIZE
 - Flash Memory (Flash), [488](#)
- FTFx_PFLASH_SWAP
 - Flash Memory (Flash), [488](#)
- FTFx_PHRASE_SIZE
 - Flash Memory (Flash), [488](#)
- FTFx_PROGRAM_CHECK
 - Flash Memory (Flash), [488](#)
- FTFx_PROGRAM_LONGWORD
 - Flash Memory (Flash), [489](#)
- FTFx_PROGRAM_ONCE
 - Flash Memory (Flash), [489](#)
- FTFx_PROGRAM_PARTITION
 - Flash Memory (Flash), [489](#)
- FTFx_PROGRAM_PHRASE
 - Flash Memory (Flash), [489](#)
- FTFx_PROGRAM_SECTION
 - Flash Memory (Flash), [489](#)
- FTFx_READ_ONCE
 - Flash Memory (Flash), [489](#)
- FTFx_READ_RESOURCE
 - Flash Memory (Flash), [489](#)
- FTFx_RSRC_CODE_REG
 - Flash Memory (Flash), [489](#)
- FTFx_SECURITY_BY_PASS
 - Flash Memory (Flash), [489](#)
- FTFx_SET_EERAM
 - Flash Memory (Flash), [489](#)
- FTFx_SWAP_COMPLETE
 - Flash Memory (Flash), [489](#)
- FTFx_SWAP_READY
 - Flash Memory (Flash), [489](#)
- FTFx_SWAP_REPORT_STATUS
 - Flash Memory (Flash), [489](#)
- FTFx_SWAP_SET_IN_COMPLETE
 - Flash Memory (Flash), [489](#)
- FTFx_SWAP_SET_IN_PREPARE
 - Flash Memory (Flash), [490](#)
- FTFx_SWAP_SET_INDICATOR_ADDR
 - Flash Memory (Flash), [490](#)
- FTFx_SWAP_UNINIT
 - Flash Memory (Flash), [490](#)
- FTFx_SWAP_UPDATE
 - Flash Memory (Flash), [490](#)
- FTFx_SWAP_UPDATE_ERASED
 - Flash Memory (Flash), [490](#)
- FTFx_VERIFY_ALL_BLOCK
 - Flash Memory (Flash), [490](#)
- FTFx_VERIFY_BLOCK
 - Flash Memory (Flash), [490](#)
- FTFx_VERIFY_SECTION
 - Flash Memory (Flash), [490](#)
- FTFx_WORD_SIZE
 - Flash Memory (Flash), [490](#)
- FTM_ABSOLUTE_VALUE
 - FlexTimer Output Compare Driver (FTM_OC), [634](#)

- FTM_BDM_MODE_00
 - FlexTimer (FTM), [594](#)
- FTM_BDM_MODE_01
 - FlexTimer (FTM), [594](#)
- FTM_BDM_MODE_10
 - FlexTimer (FTM), [594](#)
- FTM_BDM_MODE_11
 - FlexTimer (FTM), [594](#)
- FTM_BOTH_EDGES
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_CHANNEL0_FLAG
 - FlexTimer (FTM), [596](#)
- FTM_CHANNEL0_INT_ENABLE
 - FlexTimer (FTM), [595](#)
- FTM_CHANNEL1_FLAG
 - FlexTimer (FTM), [596](#)
- FTM_CHANNEL1_INT_ENABLE
 - FlexTimer (FTM), [595](#)
- FTM_CHANNEL2_FLAG
 - FlexTimer (FTM), [596](#)
- FTM_CHANNEL2_INT_ENABLE
 - FlexTimer (FTM), [595](#)
- FTM_CHANNEL3_FLAG
 - FlexTimer (FTM), [596](#)
- FTM_CHANNEL3_INT_ENABLE
 - FlexTimer (FTM), [595](#)
- FTM_CHANNEL4_FLAG
 - FlexTimer (FTM), [596](#)
- FTM_CHANNEL4_INT_ENABLE
 - FlexTimer (FTM), [595](#)
- FTM_CHANNEL5_FLAG
 - FlexTimer (FTM), [596](#)
- FTM_CHANNEL5_INT_ENABLE
 - FlexTimer (FTM), [595](#)
- FTM_CHANNEL6_FLAG
 - FlexTimer (FTM), [596](#)
- FTM_CHANNEL6_INT_ENABLE
 - FlexTimer (FTM), [595](#)
- FTM_CHANNEL7_FLAG
 - FlexTimer (FTM), [596](#)
- FTM_CHANNEL7_INT_ENABLE
 - FlexTimer (FTM), [595](#)
- FTM_CHANNEL_TRIGGER_FLAG
 - FlexTimer (FTM), [596](#)
- FTM_CLEAR_ON_MATCH
 - FlexTimer Output Compare Driver (FTM_OC), [634](#)
- FTM_CLOCK_DIVID_BY_1
 - FlexTimer (FTM), [594](#)
- FTM_CLOCK_DIVID_BY_128
 - FlexTimer (FTM), [594](#)
- FTM_CLOCK_DIVID_BY_16
 - FlexTimer (FTM), [594](#)
- FTM_CLOCK_DIVID_BY_2
 - FlexTimer (FTM), [594](#)
- FTM_CLOCK_DIVID_BY_32
 - FlexTimer (FTM), [594](#)
- FTM_CLOCK_DIVID_BY_4
 - FlexTimer (FTM), [594](#)
- FTM_CLOCK_DIVID_BY_64
 - FlexTimer (FTM), [594](#)
- FTM_CLOCK_DIVID_BY_8
 - FlexTimer (FTM), [594](#)
- FTM_CLOCK_SOURCE_EXTERNALCLK
 - FlexTimer (FTM), [594](#)
- FTM_CLOCK_SOURCE_FIXEDCLK
 - FlexTimer (FTM), [594](#)
- FTM_CLOCK_SOURCE_NONE
 - FlexTimer (FTM), [594](#)
- FTM_CLOCK_SOURCE_SYSTEMCLK
 - FlexTimer (FTM), [594](#)
- FTM_DEADTIME_DIVID_BY_1
 - FlexTimer (FTM), [595](#)
- FTM_DEADTIME_DIVID_BY_16
 - FlexTimer (FTM), [595](#)
- FTM_DEADTIME_DIVID_BY_4
 - FlexTimer (FTM), [595](#)
- FTM_DISABLE_OPERATION
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_DISABLE_OUTPUT
 - FlexTimer Output Compare Driver (FTM_OC), [634](#)
- FTM_DRV_ClearChSC
 - FlexTimer (FTM), [597](#)
- FTM_DRV_ClearChnEventStatus
 - FlexTimer (FTM), [596](#)
- FTM_DRV_ClearFaultFlagDetected
 - FlexTimer (FTM), [597](#)
- FTM_DRV_ClearStatusFlags
 - FlexTimer (FTM), [597](#)
- FTM_DRV_ControlChannelOutput
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [650](#)
- FTM_DRV_ConvertFreqToPeriodTicks
 - FlexTimer (FTM), [597](#)
- FTM_DRV_CounterRead
 - FlexTimer Module Counter Driver (FTM_MC), [629](#)
- FTM_DRV_CounterReset
 - FlexTimer (FTM), [597](#)
- FTM_DRV_CounterStart
 - FlexTimer Module Counter Driver (FTM_MC), [629](#)
- FTM_DRV_CounterStop
 - FlexTimer Module Counter Driver (FTM_MC), [629](#)
- FTM_DRV_Deinit
 - FlexTimer (FTM), [598](#)
- FTM_DRV_DeinitInputCapture
 - FlexTimer Input Capture Driver (FTM_IC), [624](#)
- FTM_DRV_DeinitOutputCompare
 - FlexTimer Output Compare Driver (FTM_OC), [634](#)
- FTM_DRV_DeinitPwm
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [650](#)
- FTM_DRV_DisableFaultInt
 - FlexTimer (FTM), [598](#)
- FTM_DRV_DisableInterrupts
 - FlexTimer (FTM), [598](#)
- FTM_DRV_EnableInterrupts
 - FlexTimer (FTM), [598](#)

- FTM_DRV_FastUpdatePwmChannels
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [650](#)
- FTM_DRV_GenerateHardwareTrigger
 - FlexTimer (FTM), [599](#)
- FTM_DRV_GetChInputState
 - FlexTimer (FTM), [599](#)
- FTM_DRV_GetChOutputValue
 - FlexTimer (FTM), [600](#)
- FTM_DRV_GetChnCountVal
 - FlexTimer (FTM), [599](#)
- FTM_DRV_GetChnEdgeLevel
 - FlexTimer (FTM), [599](#)
- FTM_DRV_GetChnEventStatus
 - FlexTimer (FTM), [600](#)
- FTM_DRV_GetClockFilterPs
 - FlexTimer (FTM), [600](#)
- FTM_DRV_GetCounter
 - FlexTimer (FTM), [601](#)
- FTM_DRV_GetCounterInitVal
 - FlexTimer (FTM), [601](#)
- FTM_DRV_GetDefaultConfig
 - FlexTimer (FTM), [601](#)
- FTM_DRV_GetEnabledInterrupts
 - FlexTimer (FTM), [601](#)
- FTM_DRV_GetEventStatus
 - FlexTimer (FTM), [602](#)
- FTM_DRV_GetFrequency
 - FlexTimer (FTM), [602](#)
- FTM_DRV_GetInputCaptureMeasurement
 - FlexTimer Input Capture Driver (FTM_IC), [624](#)
- FTM_DRV_GetMod
 - FlexTimer (FTM), [602](#)
- FTM_DRV_GetStatusFlags
 - FlexTimer (FTM), [602](#)
- FTM_DRV_GetTriggerControlled
 - FlexTimer (FTM), [603](#)
- FTM_DRV_Init
 - FlexTimer (FTM), [603](#)
- FTM_DRV_InitCounter
 - FlexTimer Module Counter Driver (FTM_MC), [629](#)
- FTM_DRV_InitInputCapture
 - FlexTimer Input Capture Driver (FTM_IC), [624](#)
- FTM_DRV_InitOutputCompare
 - FlexTimer Output Compare Driver (FTM_OC), [635](#)
- FTM_DRV_InitPwm
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [651](#)
- FTM_DRV_IsChnDma
 - FlexTimer (FTM), [603](#)
- FTM_DRV_IsChnLcrst
 - FlexTimer (FTM), [604](#)
- FTM_DRV_IsFaultFlagDetected
 - FlexTimer (FTM), [604](#)
- FTM_DRV_IsFaultInputEnabled
 - FlexTimer (FTM), [604](#)
- FTM_DRV_IsFtmEnable
 - FlexTimer (FTM), [605](#)
- FTM_DRV_IsWriteProtectionEnabled
 - FlexTimer (FTM), [605](#)
- FTM_DRV_MaskOutputChannels
 - FlexTimer (FTM), [605](#)
- FTM_DRV_QuadDecodeStart
 - FlexTimer Quadrature Decoder Driver (FTM_QD), [658](#)
- FTM_DRV_QuadDecodeStop
 - FlexTimer Quadrature Decoder Driver (FTM_QD), [658](#)
- FTM_DRV_QuadGetState
 - FlexTimer Quadrature Decoder Driver (FTM_QD), [658](#)
- FTM_DRV_SetAllChnSoftwareOutputControl
 - FlexTimer (FTM), [605](#)
- FTM_DRV_SetCaptureTestCmd
 - FlexTimer (FTM), [606](#)
- FTM_DRV_SetChnDmaCmd
 - FlexTimer (FTM), [606](#)
- FTM_DRV_SetChnLcrstCmd
 - FlexTimer (FTM), [607](#)
- FTM_DRV_SetChnOutputInitStateCmd
 - FlexTimer (FTM), [607](#)
- FTM_DRV_SetChnOutputMask
 - FlexTimer (FTM), [607](#)
- FTM_DRV_SetChnSoftwareCtrlCmd
 - FlexTimer (FTM), [607](#)
- FTM_DRV_SetChnSoftwareCtrlVal
 - FlexTimer (FTM), [608](#)
- FTM_DRV_SetClockFilterPs
 - FlexTimer (FTM), [608](#)
- FTM_DRV_SetCountReinitSyncCmd
 - FlexTimer (FTM), [608](#)
- FTM_DRV_SetDualChnInvertCmd
 - FlexTimer (FTM), [609](#)
- FTM_DRV_SetExtPairDeadtimeValue
 - FlexTimer (FTM), [609](#)
- FTM_DRV_SetGlobalLoadCmd
 - FlexTimer (FTM), [609](#)
- FTM_DRV_SetGlobalTimeBaseCmd
 - FlexTimer (FTM), [609](#)
- FTM_DRV_SetGlobalTimeBaseOutputCmd
 - FlexTimer (FTM), [609](#)
- FTM_DRV_SetHalfCycleCmd
 - FlexTimer (FTM), [611](#)
- FTM_DRV_SetHalfCycleReloadPoint
 - FlexTimer (FTM), [611](#)
- FTM_DRV_SetInitTrigOnReloadCmd
 - FlexTimer (FTM), [611](#)
- FTM_DRV_SetInitialCounterValue
 - FlexTimer (FTM), [611](#)
- FTM_DRV_SetInvertingControl
 - FlexTimer (FTM), [613](#)
- FTM_DRV_SetLoadCmd
 - FlexTimer (FTM), [613](#)
- FTM_DRV_SetLoadFreq
 - FlexTimer (FTM), [613](#)
- FTM_DRV_SetModuloCounterValue

- FlexTimer (FTM), [613](#)
- FTM_DRV_SetOutputlevel
 - FlexTimer (FTM), [614](#)
- FTM_DRV_SetPairDeadtimeCount
 - FlexTimer (FTM), [614](#)
- FTM_DRV_SetPairDeadtimePrescale
 - FlexTimer (FTM), [614](#)
- FTM_DRV_SetPwmLoadChnSelCmd
 - FlexTimer (FTM), [615](#)
- FTM_DRV_SetPwmLoadCmd
 - FlexTimer (FTM), [615](#)
- FTM_DRV_SetSoftOutChnValue
 - FlexTimer (FTM), [615](#)
- FTM_DRV_SetSoftwareOutputChannelControl
 - FlexTimer (FTM), [616](#)
- FTM_DRV_SetSync
 - FlexTimer (FTM), [616](#)
- FTM_DRV_SetTrigModeControlCmd
 - FlexTimer (FTM), [616](#)
- FTM_DRV_StartNewSignalMeasurement
 - FlexTimer Input Capture Driver (FTM_IC), [625](#)
- FTM_DRV_UpdateOutputCompareChannel
 - FlexTimer Output Compare Driver (FTM_OC), [635](#)
- FTM_DRV_UpdatePwmChannel
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [651](#)
- FTM_DRV_UpdatePwmPeriod
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [652](#)
- FTM_DUTY_TO_TICKS_SHIFT
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [649](#)
- FTM_EDGE_DETECT
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_FALLING_EDGE
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_FALLING_EDGE_PERIOD_MEASUREMENT
 - FlexTimer Input Capture Driver (FTM_IC), [624](#)
- FTM_FAULT_CONTROL_AUTO_ALL
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [649](#)
- FTM_FAULT_CONTROL_DISABLED
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [649](#)
- FTM_FAULT_CONTROL_MAN_ALL
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [649](#)
- FTM_FAULT_CONTROL_MAN_EVEN
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [649](#)
- FTM_FAULT_FLAG
 - FlexTimer (FTM), [596](#)
- FTM_FAULT_INT_ENABLE
 - FlexTimer (FTM), [595](#)
- FTM_HIGH_STATE
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [650](#)
- FTM_IC_DRV_SetChannelMode
 - FlexTimer Input Capture Driver (FTM_IC), [625](#)
- FTM_LOW_STATE
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [650](#)
- FTM_MAIN_DUPLICATED
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [650](#)
- FTM_MAIN_INVERTED
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [650](#)
- FTM_MAX_DUTY_CYCLE
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [649](#)
- FTM_MC_DRV_GetDefaultConfig
 - FlexTimer Module Counter Driver (FTM_MC), [630](#)
- FTM_MEASURE_FALLING_EDGE_PERIOD
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_MEASURE_PULSE_HIGH
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_MEASURE_PULSE_LOW
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_MEASURE_RISING_EDGE_PERIOD
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_MODE_CEN_ALIGNED_PWM
 - FlexTimer (FTM), [595](#)
- FTM_MODE_EDGE_ALIGNED_PWM
 - FlexTimer (FTM), [595](#)
- FTM_MODE_EDGE_ALIGNED_PWM_AND_INPUT_↔CAPTURE
 - FlexTimer (FTM), [595](#)
- FTM_MODE_INPUT_CAPTURE
 - FlexTimer (FTM), [595](#)
- FTM_MODE_NOT_INITIALIZED
 - FlexTimer (FTM), [595](#)
- FTM_MODE_OUTPUT_COMPARE
 - FlexTimer (FTM), [595](#)
- FTM_MODE_QUADRATURE_DECODER
 - FlexTimer (FTM), [595](#)
- FTM_MODE_UP_DOWN_TIMER
 - FlexTimer (FTM), [595](#)
- FTM_MODE_UP_TIMER
 - FlexTimer (FTM), [595](#)
- FTM_NO_MEASUREMENT
 - FlexTimer Input Capture Driver (FTM_IC), [624](#)
- FTM_NO_OPERATION
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_NO_PIN_CONTROL
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_PERIOD_OFF_MEASUREMENT
 - FlexTimer Input Capture Driver (FTM_IC), [624](#)
- FTM_PERIOD_ON_MEASUREMENT
 - FlexTimer Input Capture Driver (FTM_IC), [624](#)
- FTM_POLARITY_HIGH
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [649](#)
- FTM_POLARITY_LOW
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [649](#)

- FTM_PWM_SYNC
 - FlexTimer (FTM), [596](#)
- FTM_PWM_UPDATE_IN_DUTY_CYCLE
 - FlexTimer Pulse Width Modulation Driver (FTM_PWM), [649](#)
- FTM_PWM_UPDATE_IN_TICKS
 - FlexTimer Pulse Width Modulation Driver (FTM_PWM), [649](#)
- FTM_QD_DRV_GetDefaultConfig
 - FlexTimer Quadrature Decoder Driver (FTM_QD), [659](#)
- FTM_QUAD_COUNT_AND_DIR
 - FlexTimer Quadrature Decoder Driver (FTM_QD), [658](#)
- FTM_QUAD_PHASE_ENCODE
 - FlexTimer Quadrature Decoder Driver (FTM_QD), [658](#)
- FTM_QUAD_PHASE_INVERT
 - FlexTimer Quadrature Decoder Driver (FTM_QD), [658](#)
- FTM_QUAD_PHASE_NORMAL
 - FlexTimer Quadrature Decoder Driver (FTM_QD), [658](#)
- FTM_RELATIVE_VALUE
 - FlexTimer Output Compare Driver (FTM_OC), [634](#)
- FTM_RELOAD_FLAG
 - FlexTimer (FTM), [596](#)
- FTM_RELOAD_INT_ENABLE
 - FlexTimer (FTM), [595](#)
- FTM_RISING_EDGE
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_RISING_EDGE_PERIOD_MEASUREMENT
 - FlexTimer Input Capture Driver (FTM_IC), [624](#)
- FTM_RM_W_CNT
 - FlexTimer (FTM), [592](#)
- FTM_RM_W_CNTIN
 - FlexTimer (FTM), [592](#)
- FTM_RM_W_CONF
 - FlexTimer (FTM), [592](#)
- FTM_RM_W_CnSCV_REG
 - FlexTimer (FTM), [591](#)
- FTM_RM_W_DEADTIME
 - FlexTimer (FTM), [592](#)
- FTM_RM_W_EXTTRIG_REG
 - FlexTimer (FTM), [592](#)
- FTM_RM_W_FILTER
 - FlexTimer (FTM), [592](#)
- FTM_RM_W_FLTCTRL
 - FlexTimer (FTM), [592](#)
- FTM_RM_W_FMS
 - FlexTimer (FTM), [592](#)
- FTM_RM_W_MOD
 - FlexTimer (FTM), [592](#)
- FTM_RM_W_MODE
 - FlexTimer (FTM), [592](#)
- FTM_RM_W_PAIR0DEADTIME
 - FlexTimer (FTM), [593](#)
- FTM_RM_W_PAIR1DEADTIME
 - FlexTimer (FTM), [593](#)
- FTM_RM_W_PAIR2DEADTIME
 - FlexTimer (FTM), [593](#)
- FTM_RM_W_PAIR3DEADTIME
 - FlexTimer (FTM), [593](#)
- FTM_RM_W_POL
 - FlexTimer (FTM), [593](#)
- FTM_RM_W_QDCTRL
 - FlexTimer (FTM), [593](#)
- FTM_RM_W_SC
 - FlexTimer (FTM), [593](#)
- FTM_RM_W_STATUS
 - FlexTimer (FTM), [593](#)
- FTM_RM_W_SYNC
 - FlexTimer (FTM), [593](#)
- FTM_SET_ON_MATCH
 - FlexTimer Output Compare Driver (FTM_OC), [634](#)
- FTM_SIGNAL_MEASUREMENT
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_SYSTEM_CLOCK
 - FlexTimer (FTM), [596](#)
- FTM_TIME_OVER_FLOW_FLAG
 - FlexTimer (FTM), [596](#)
- FTM_TIME_OVER_FLOW_INT_ENABLE
 - FlexTimer (FTM), [595](#)
- FTM_TIMESTAMP_BOTH_EDGES
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_TIMESTAMP_FALLING_EDGE
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_TIMESTAMP_RISING_EDGE
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- FTM_TOGGLED_ON_MATCH
 - FlexTimer Output Compare Driver (FTM_OC), [634](#)
- FTM_UPDATE_NOW
 - FlexTimer (FTM), [596](#)
- FTM_WAIT_LOADING_POINTS
 - FlexTimer (FTM), [596](#)
- factoryAreaLock
 - flash_mx25l6433f_secure_lock_t, [885](#)
- failNoCert
 - Options, [1301](#)
 - WOLFSSL_CTX, [1352](#)
- failNoCertxPSK
 - Options, [1301](#)
 - WOLFSSL_CTX, [1352](#)
- fallingEdgeInterruptCount
 - lin_state_t, [727](#)
- fanout
 - __blake2b_param, [1243](#)
 - __blake2s_param, [1245](#)
- fatal
 - ProcPeerCertArgs, [1308](#)
- fault_state_signal_ptr
 - lin_node_attribute_t, [830](#)
- faultChannelEnabled
 - ftm_pwm_ch_fault_param_t, [644](#)
- faultConfig
 - ftm_pwm_param_t, [648](#)

faultFilterEnabled
 ftm_pwm_ch_fault_param_t, 644
 faultFilterValue
 ftm_pwm_fault_param_t, 644
 faultMode
 ftm_pwm_fault_param_t, 644
 faultReg
 fs45_drv_config_t, 1061
 fd
 OS_Seed, 1305
 WOLFSSL_BIO, 1344
 fdPadding
 can_buff_config_t, 388
 fifoSize
 lpspi_state_t, 778
 file
 WOLFSSL_BIO, 1345
 filterEn
 ftm_input_ch_param_t, 622
 ic_input_ch_param_t, 687
 filterSampleCount
 cmp_comparator_t, 367
 filterSamplePeriod
 cmp_comparator_t, 367
 filterValue
 ftm_input_ch_param_t, 622
 ic_input_ch_param_t, 687
 finalValue
 extension_ftm_for_timer_t, 1160
 ftm_timer_param_t, 628
 fircConfig
 scg_config_t, 334
 FirstBitIndex
 sai_user_config_t, 1040
 firstEdge
 ftm_combined_ch_param_t, 647
 fixedChannel
 cmp_trigger_mode_t, 370
 fixedPort
 cmp_trigger_mode_t, 370
 flag_offset
 lin_frame_t, 832
 lin_master_data_t, 840
 flag_size
 lin_frame_t, 832
 lin_master_data_t, 840
 flags
 timeoutInfo_st, 1330
 WOLF_EVENT, 1335
 WOLFSSL_ASN1_BIT_STRING, 1341
 WOLFSSL_ASN1_STRING, 1343
 WOLFSSL_EVP_CIPHER_CTX, 1362
 Flash Memory (Flash), 483, 503
 brownOutCode, 500
 CLEAR_FTFx_FSTAT_ERROR_BITS, 487
 CSE_KEY_SIZE_CODE_MAX, 487
 CallBack, 500
 DFLASH_IFR_READRESOURCE_ADDRESS, 487
 DFlashBase, 500, 501
 DFlashSize, 501
 EEE_COMPLETE_INTERRUPT_QUICK_WRITE, 491
 EEE_DISABLE, 491
 EEE_ENABLE, 491
 EEE_QUICK_WRITE, 491
 EEE_STATUS_QUERY, 491
 EEESize, 501
 EERAMBase, 501
 FLASH_CALLBACK_CS, 487
 FLASH_DRV_CheckSum, 491
 FLASH_DRV_ClearReadColisionFlag, 492
 FLASH_DRV_DisableCmdCompleteInterupt, 492
 FLASH_DRV_DisableReadColisionInterupt, 492
 FLASH_DRV_EnableCmdCompleteInterupt, 492
 FLASH_DRV_EnableReadColisionInterupt, 492
 FLASH_DRV_EraseAllBlock, 493
 FLASH_DRV_EraseResume, 493
 FLASH_DRV_EraseSector, 493
 FLASH_DRV_EraseSuspend, 494
 FLASH_DRV_GetCmdCompleteFlag, 494
 FLASH_DRV_GetDefaultConfig, 495
 FLASH_DRV_GetPFlashProtection, 495
 FLASH_DRV_GetReadColisionFlag, 495
 FLASH_DRV_GetSecurityState, 495
 FLASH_DRV_Init, 496
 FLASH_DRV_Program, 496
 FLASH_DRV_ProgramCheck, 496
 FLASH_DRV_ProgramOnce, 497
 FLASH_DRV_ReadOnce, 497
 FLASH_DRV_SecurityBypass, 498
 FLASH_DRV_SetPFlashProtection, 498
 FLASH_DRV_VerifyAllBlock, 499
 FLASH_DRV_VerifySection, 499
 FLASH_NOT_SECURE, 487
 FLASH_SECURE_BACKDOOR_DISABLED, 488
 FLASH_SECURE_BACKDOOR_ENABLED, 488
 FLASH_SECURITY_STATE_KEYEN, 488
 FLASH_SECURITY_STATE_UNSECURED, 488
 FTFx_DPHRASE_SIZE, 488
 FTFx_ERASE_ALL_BLOCK, 488
 FTFx_ERASE_ALL_BLOCK_UNSECURE, 488
 FTFx_ERASE_BLOCK, 488
 FTFx_ERASE_SECTOR, 488
 FTFx_FSTAT_ERROR_BITS, 488
 FTFx_LONGWORD_SIZE, 488
 FTFx_PFLASH_SWAP, 488
 FTFx_PHRASE_SIZE, 488
 FTFx_PROGRAM_CHECK, 488
 FTFx_PROGRAM_LONGWORD, 489
 FTFx_PROGRAM_ONCE, 489
 FTFx_PROGRAM_PARTITION, 489
 FTFx_PROGRAM_PHRASE, 489
 FTFx_PROGRAM_SECTION, 489
 FTFx_READ_ONCE, 489

- FTF_x_READ_RESOURCE, 489
- FTF_x_RSRC_CODE_REG, 489
- FTF_x_SECURITY_BY_PASS, 489
- FTF_x_SET_EERAM, 489
- FTF_x_SWAP_COMPLETE, 489
- FTF_x_SWAP_READY, 489
- FTF_x_SWAP_REPORT_STATUS, 489
- FTF_x_SWAP_SET_IN_COMPLETE, 489
- FTF_x_SWAP_SET_IN_PREPARE, 490
- FTF_x_SWAP_SET_INDICATOR_ADDR, 490
- FTF_x_SWAP_UNINIT, 490
- FTF_x_SWAP_UPDATE, 490
- FTF_x_SWAP_UPDATE_ERASED, 490
- FTF_x_VERIFY_ALL_BLOCK, 490
- FTF_x_VERIFY_BLOCK, 490
- FTF_x_VERIFY_SECTION, 490
- FTF_x_WORD_SIZE, 490
- flash_callback_t, 491
- flash_flexRam_function_control_code_t, 491
- GET_BIT_0_7, 490
- GET_BIT_16_23, 490
- GET_BIT_24_31, 490
- GET_BIT_8_15, 490
- NULL_CALLBACK, 491
- numOfRecordReqMaintain, 501
- PFlashBase, 501
- PFlashSize, 501
- RESUME_WAIT_CNT, 491
- SUSPEND_WAIT_CNT, 491
- sectorEraseCount, 502
- flash_callback_t
 - Flash Memory (Flash), 491
- flash_eeprom_status_t, 487
- flash_flexRam_function_control_code_t
 - Flash Memory (Flash), 491
- flash_mx25l6433f_drv_strength_t
 - MX25L6433F Serial Flash Driver, 886
- flash_mx25l6433f_prot_dir_t
 - MX25L6433F Serial Flash Driver, 886
- flash_mx25l6433f_prot_size_t
 - MX25L6433F Serial Flash Driver, 886
- flash_mx25l6433f_secure_lock_t, 885
 - factoryAreaLock, 885
 - userAreaLock, 885
- flash_mx25l6433f_state_t, 885
- flash_mx25l6433f_user_config_t, 885
 - dmaSupport, 885
 - outputDriverStrength, 885
- flash_ssd_config_t, 486
- flash_user_config_t, 486
- FlexCAN Driver, 506
 - FLEXCAN_DISABLE_MODE, 518
 - FLEXCAN_DRV_AbortTransfer, 520
 - FLEXCAN_DRV_ConfigRemoteResponseMb, 520
 - FLEXCAN_DRV_ConfigRxFifo, 520
 - FLEXCAN_DRV_ConfigRxMb, 521
 - FLEXCAN_DRV_ConfigTxMb, 521
 - FLEXCAN_DRV_Deinit, 521
 - FLEXCAN_DRV_GetBitrate, 521
 - FLEXCAN_DRV_GetDefaultConfig, 522
 - FLEXCAN_DRV_GetErrorStatus, 522
 - FLEXCAN_DRV_GetTransferStatus, 522
 - FLEXCAN_DRV_Init, 523
 - FLEXCAN_DRV_InstallErrorCallback, 523
 - FLEXCAN_DRV_InstallEventCallback, 523
 - FLEXCAN_DRV_Receive, 523
 - FLEXCAN_DRV_ReceiveBlocking, 524
 - FLEXCAN_DRV_RxFifo, 524
 - FLEXCAN_DRV_RxFifoBlocking, 524
 - FLEXCAN_DRV_Send, 525
 - FLEXCAN_DRV_SendBlocking, 525
 - FLEXCAN_DRV_SetBitrate, 525
 - FLEXCAN_DRV_SetRxFifoGlobalMask, 526
 - FLEXCAN_DRV_SetRxIndividualMask, 526
 - FLEXCAN_DRV_SetRxMaskType, 526
 - FLEXCAN_DRV_SetRxMb14Mask, 526
 - FLEXCAN_DRV_SetRxMb15Mask, 527
 - FLEXCAN_DRV_SetRxMbGlobalMask, 527
 - FLEXCAN_EVENT_ERROR, 518
 - FLEXCAN_EVENT_RX_COMPLETE, 518
 - FLEXCAN_EVENT_RXFIFO_COMPLETE, 518
 - FLEXCAN_EVENT_RXFIFO_OVERFLOW, 518
 - FLEXCAN_EVENT_RXFIFO_WARNING, 518
 - FLEXCAN_EVENT_TX_COMPLETE, 518
 - FLEXCAN_FREEZE_MODE, 518
 - FLEXCAN_LISTEN_ONLY_MODE, 518
 - FLEXCAN_LOOPBACK_MODE, 518
 - FLEXCAN_MB_IDLE, 518
 - FLEXCAN_MB_RX_BUSY, 518
 - FLEXCAN_MB_TX_BUSY, 518
 - FLEXCAN_MSG_ID_EXT, 518
 - FLEXCAN_MSG_ID_STD, 518
 - FLEXCAN_NORMAL_MODE, 518
 - FLEXCAN_RX_FIFO_ID_FILTERS_104, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_112, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_120, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_128, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_16, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_24, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_32, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_40, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_48, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_56, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_64, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_72, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_8, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_80, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_88, 519
 - FLEXCAN_RX_FIFO_ID_FILTERS_96, 519
 - FLEXCAN_RX_FIFO_ID_FORMAT_A, 519
 - FLEXCAN_RX_FIFO_ID_FORMAT_B, 519
 - FLEXCAN_RX_FIFO_ID_FORMAT_C, 519
 - FLEXCAN_RX_FIFO_ID_FORMAT_D, 519
 - FLEXCAN_RX_MASK_GLOBAL, 519
 - FLEXCAN_RX_MASK_INDIVIDUAL, 519
 - FLEXCAN_RXFIFO_USING_INTERRUPTS, 519

- flexcan_callback_t, 517
 - flexcan_error_callback_t, 517
 - flexcan_event_type_t, 517
 - flexcan_mb_state_t, 518
 - flexcan_msgbuff_id_type_t, 518
 - flexcan_operation_modes_t, 518
 - flexcan_rx_fifo_id_element_format_t, 518
 - flexcan_rx_fifo_id_filter_num_t, 519
 - flexcan_rx_mask_type_t, 519
 - flexcan_rxfifo_transfer_type_t, 519
 - flexcan_state_t, 517
 - FlexCANState, 514
 - callback, 514
 - callbackParam, 514
 - error_callback, 514
 - errorCallbackParam, 514
 - mbs, 514
 - transferType, 514
 - FlexIO Common Driver, 528
 - FLEXIO_DRIVER_TYPE_DMA, 528
 - FLEXIO_DRIVER_TYPE_INTERRUPTS, 528
 - FLEXIO_DRIVER_TYPE_POLLING, 528
 - FLEXIO_DRV_DeinitDevice, 528
 - FLEXIO_DRV_InitDevice, 530
 - FLEXIO_DRV_Reset, 530
 - flexio_driver_type_t, 528
 - FlexIO I2C Driver, 531
 - FLEXIO_I2C_DRV_GenerateNineClock, 535
 - FLEXIO_I2C_DRV_GetBusStatus, 535
 - FLEXIO_I2C_DRV_GetDefaultConfig, 535
 - FLEXIO_I2C_DRV_MasterDeinit, 536
 - FLEXIO_I2C_DRV_MasterGetBaudRate, 536
 - FLEXIO_I2C_DRV_MasterGetStatus, 536
 - FLEXIO_I2C_DRV_MasterInit, 536
 - FLEXIO_I2C_DRV_MasterReceiveData, 537
 - FLEXIO_I2C_DRV_MasterReceiveDataBlocking, 537
 - FLEXIO_I2C_DRV_MasterSendData, 537
 - FLEXIO_I2C_DRV_MasterSendDataBlocking, 538
 - FLEXIO_I2C_DRV_MasterSetBaudRate, 538
 - FLEXIO_I2C_DRV_MasterSetSlaveAddr, 539
 - FLEXIO_I2C_DRV_MasterTransferAbort, 539
 - FLEXIO_I2C_DRV_StatusGenerateNineClock, 539
 - FlexIO I2S Driver, 540
 - FLEXIO_I2S_DRV_MasterDeinit, 546
 - FLEXIO_I2S_DRV_MasterGetBaudRate, 546
 - FLEXIO_I2S_DRV_MasterGetDefaultConfig, 547
 - FLEXIO_I2S_DRV_MasterGetStatus, 547
 - FLEXIO_I2S_DRV_MasterInit, 547
 - FLEXIO_I2S_DRV_MasterReceiveData, 548
 - FLEXIO_I2S_DRV_MasterReceiveDataBlocking, 548
 - FLEXIO_I2S_DRV_MasterSendData, 548
 - FLEXIO_I2S_DRV_MasterSendDataBlocking, 549
 - FLEXIO_I2S_DRV_MasterSetConfig, 549
 - FLEXIO_I2S_DRV_MasterSetRxBuffer, 549
 - FLEXIO_I2S_DRV_MasterSetTxBuffer, 550
 - FLEXIO_I2S_DRV_MasterTransferAbort, 550
 - FLEXIO_I2S_DRV_SlaveDeinit, 550
 - FLEXIO_I2S_DRV_SlaveGetDefaultConfig, 551
 - FLEXIO_I2S_DRV_SlaveGetStatus, 551
 - FLEXIO_I2S_DRV_SlaveInit, 551
 - FLEXIO_I2S_DRV_SlaveReceiveData, 552
 - FLEXIO_I2S_DRV_SlaveReceiveDataBlocking, 552
 - FLEXIO_I2S_DRV_SlaveSendData, 553
 - FLEXIO_I2S_DRV_SlaveSendDataBlocking, 553
 - FLEXIO_I2S_DRV_SlaveSetConfig, 554
 - FLEXIO_I2S_DRV_SlaveSetRxBuffer, 554
 - FLEXIO_I2S_DRV_SlaveSetTxBuffer, 555
 - FLEXIO_I2S_DRV_SlaveTransferAbort, 555
 - flexio_i2s_slave_state_t, 546
- FlexIO SPI Driver, 558
 - FLEXIO_SPI_DRV_MasterDeinit, 565
 - FLEXIO_SPI_DRV_MasterGetBaudRate, 565
 - FLEXIO_SPI_DRV_MasterGetDefaultConfig, 566
 - FLEXIO_SPI_DRV_MasterGetStatus, 566
 - FLEXIO_SPI_DRV_MasterInit, 566
 - FLEXIO_SPI_DRV_MasterSetBaudRate, 566
 - FLEXIO_SPI_DRV_MasterTransfer, 567
 - FLEXIO_SPI_DRV_MasterTransferAbort, 567
 - FLEXIO_SPI_DRV_MasterTransferBlocking, 567
 - FLEXIO_SPI_DRV_SlaveDeinit, 568
 - FLEXIO_SPI_DRV_SlaveGetDefaultConfig, 568
 - FLEXIO_SPI_DRV_SlaveGetStatus, 568
 - FLEXIO_SPI_DRV_SlaveInit, 569
 - FLEXIO_SPI_DRV_SlaveTransfer, 569
 - FLEXIO_SPI_DRV_SlaveTransferAbort, 570
 - FLEXIO_SPI_DRV_SlaveTransferBlocking, 570
 - FLEXIO_SPI_TRANSFER_1BYTE, 565
 - FLEXIO_SPI_TRANSFER_2BYTE, 565
 - FLEXIO_SPI_TRANSFER_4BYTE, 565
 - FLEXIO_SPI_TRANSFER_LSB_FIRST, 565
 - FLEXIO_SPI_TRANSFER_MSB_FIRST, 565
 - flexio_spi_slave_state_t, 564
 - flexio_spi_transfer_bit_order_t, 565
 - flexio_spi_transfer_size_t, 565
 - FlexIO UART Driver, 572
 - FLEXIO_UART_DIRECTION_RX, 576
 - FLEXIO_UART_DIRECTION_TX, 576
 - FLEXIO_UART_DRV_Deinit, 576
 - FLEXIO_UART_DRV_GetBaudRate, 576
 - FLEXIO_UART_DRV_GetDefaultConfig, 576
 - FLEXIO_UART_DRV_GetStatus, 577
 - FLEXIO_UART_DRV_Init, 577
 - FLEXIO_UART_DRV_ReceiveData, 577
 - FLEXIO_UART_DRV_ReceiveDataBlocking, 578
 - FLEXIO_UART_DRV_SendData, 578
 - FLEXIO_UART_DRV_SendDataBlocking, 578
 - FLEXIO_UART_DRV_SetConfig, 579
 - FLEXIO_UART_DRV_SetRxBuffer, 579
 - FLEXIO_UART_DRV_SetTxBuffer, 579
 - FLEXIO_UART_DRV_TransferAbort, 580
 - flexio_uart_driver_direction_t, 576
 - FlexTimer (FTM), 581

CHAN0_IDX, [591](#)
 CHAN1_IDX, [591](#)
 CHAN2_IDX, [591](#)
 CHAN3_IDX, [591](#)
 CHAN4_IDX, [591](#)
 CHAN5_IDX, [591](#)
 CHAN6_IDX, [591](#)
 CHAN7_IDX, [591](#)
 FTM_BDM_MODE_00, [594](#)
 FTM_BDM_MODE_01, [594](#)
 FTM_BDM_MODE_10, [594](#)
 FTM_BDM_MODE_11, [594](#)
 FTM_CHANNEL0_FLAG, [596](#)
 FTM_CHANNEL0_INT_ENABLE, [595](#)
 FTM_CHANNEL1_FLAG, [596](#)
 FTM_CHANNEL1_INT_ENABLE, [595](#)
 FTM_CHANNEL2_FLAG, [596](#)
 FTM_CHANNEL2_INT_ENABLE, [595](#)
 FTM_CHANNEL3_FLAG, [596](#)
 FTM_CHANNEL3_INT_ENABLE, [595](#)
 FTM_CHANNEL4_FLAG, [596](#)
 FTM_CHANNEL4_INT_ENABLE, [595](#)
 FTM_CHANNEL5_FLAG, [596](#)
 FTM_CHANNEL5_INT_ENABLE, [595](#)
 FTM_CHANNEL6_FLAG, [596](#)
 FTM_CHANNEL6_INT_ENABLE, [595](#)
 FTM_CHANNEL7_FLAG, [596](#)
 FTM_CHANNEL7_INT_ENABLE, [595](#)
 FTM_CHANNEL_TRIGGER_FLAG, [596](#)
 FTM_CLOCK_DIVID_BY_1, [594](#)
 FTM_CLOCK_DIVID_BY_128, [594](#)
 FTM_CLOCK_DIVID_BY_16, [594](#)
 FTM_CLOCK_DIVID_BY_2, [594](#)
 FTM_CLOCK_DIVID_BY_32, [594](#)
 FTM_CLOCK_DIVID_BY_4, [594](#)
 FTM_CLOCK_DIVID_BY_64, [594](#)
 FTM_CLOCK_DIVID_BY_8, [594](#)
 FTM_CLOCK_SOURCE_EXTERNALCLK, [594](#)
 FTM_CLOCK_SOURCE_FIXEDCLK, [594](#)
 FTM_CLOCK_SOURCE_NONE, [594](#)
 FTM_CLOCK_SOURCE_SYSTEMCLK, [594](#)
 FTM_DEADTIME_DIVID_BY_1, [595](#)
 FTM_DEADTIME_DIVID_BY_16, [595](#)
 FTM_DEADTIME_DIVID_BY_4, [595](#)
 FTM_DRV_ClearChSC, [597](#)
 FTM_DRV_ClearChnEventStatus, [596](#)
 FTM_DRV_ClearFaultFlagDetected, [597](#)
 FTM_DRV_ClearStatusFlags, [597](#)
 FTM_DRV_ConvertFreqToPeriodTicks, [597](#)
 FTM_DRV_CounterReset, [597](#)
 FTM_DRV_Deinit, [598](#)
 FTM_DRV_DisableFaultInt, [598](#)
 FTM_DRV_DisableInterrupts, [598](#)
 FTM_DRV_EnableInterrupts, [598](#)
 FTM_DRV_GenerateHardwareTrigger, [599](#)
 FTM_DRV_GetChnInputState, [599](#)
 FTM_DRV_GetChnOutputValue, [600](#)
 FTM_DRV_GetChnCountVal, [599](#)
 FTM_DRV_GetChnEdgeLevel, [599](#)
 FTM_DRV_GetChnEventStatus, [600](#)
 FTM_DRV_GetClockFilterPs, [600](#)
 FTM_DRV_GetCounter, [601](#)
 FTM_DRV_GetCounterInitVal, [601](#)
 FTM_DRV_GetDefaultConfig, [601](#)
 FTM_DRV_GetEnabledInterrupts, [601](#)
 FTM_DRV_GetEventStatus, [602](#)
 FTM_DRV_GetFrequency, [602](#)
 FTM_DRV_GetMod, [602](#)
 FTM_DRV_GetStatusFlags, [602](#)
 FTM_DRV_GetTriggerControlled, [603](#)
 FTM_DRV_Init, [603](#)
 FTM_DRV_IsChnDma, [603](#)
 FTM_DRV_IsChnIcrst, [604](#)
 FTM_DRV_IsFaultFlagDetected, [604](#)
 FTM_DRV_IsFaultInputEnabled, [604](#)
 FTM_DRV_IsFtmEnable, [605](#)
 FTM_DRV_IsWriteProtectionEnabled, [605](#)
 FTM_DRV_MaskOutputChannels, [605](#)
 FTM_DRV_SetAllChnSoftwareOutputControl, [605](#)
 FTM_DRV_SetCaptureTestCmd, [606](#)
 FTM_DRV_SetChnDmaCmd, [606](#)
 FTM_DRV_SetChnIcrstCmd, [607](#)
 FTM_DRV_SetChnOutputInitStateCmd, [607](#)
 FTM_DRV_SetChnOutputMask, [607](#)
 FTM_DRV_SetChnSoftwareCtrlCmd, [607](#)
 FTM_DRV_SetChnSoftwareCtrlVal, [608](#)
 FTM_DRV_SetClockFilterPs, [608](#)
 FTM_DRV_SetCountReinitSyncCmd, [608](#)
 FTM_DRV_SetDualChnInvertCmd, [609](#)
 FTM_DRV_SetExtPairDeadtimeValue, [609](#)
 FTM_DRV_SetGlobalLoadCmd, [609](#)
 FTM_DRV_SetGlobalTimeBaseCmd, [609](#)
 FTM_DRV_SetGlobalTimeBaseOutputCmd, [609](#)
 FTM_DRV_SetHalfCycleCmd, [611](#)
 FTM_DRV_SetHalfCycleReloadPoint, [611](#)
 FTM_DRV_SetInitTrigOnReloadCmd, [611](#)
 FTM_DRV_SetInitialCounterValue, [611](#)
 FTM_DRV_SetInvertingControl, [613](#)
 FTM_DRV_SetLoadCmd, [613](#)
 FTM_DRV_SetLoadFreq, [613](#)
 FTM_DRV_SetModuloCounterValue, [613](#)
 FTM_DRV_SetOutputlevel, [614](#)
 FTM_DRV_SetPairDeadtimeCount, [614](#)
 FTM_DRV_SetPairDeadtimePrescale, [614](#)
 FTM_DRV_SetPwmLoadChnSelCmd, [615](#)
 FTM_DRV_SetPwmLoadCmd, [615](#)
 FTM_DRV_SetSoftOutChnValue, [615](#)
 FTM_DRV_SetSoftwareOutputChannelControl, [616](#)
 FTM_DRV_SetSync, [616](#)
 FTM_DRV_SetTrigModeControlCmd, [616](#)
 FTM_FAULT_FLAG, [596](#)
 FTM_FAULT_INT_ENABLE, [595](#)
 FTM_MODE_CEN_ALIGNED_PWM, [595](#)
 FTM_MODE_EDGE_ALIGNED_PWM, [595](#)

- FTM_MODE_EDGE_ALIGNED_PWM_AND_INPUT_CAPTURE, 595
- FTM_MODE_INPUT_CAPTURE, 595
- FTM_MODE_NOT_INITIALIZED, 595
- FTM_MODE_OUTPUT_COMPARE, 595
- FTM_MODE_QUADRATURE_DECODER, 595
- FTM_MODE_UP_DOWN_TIMER, 595
- FTM_MODE_UP_TIMER, 595
- FTM_PWM_SYNC, 596
- FTM_RELOAD_FLAG, 596
- FTM_RELOAD_INT_ENABLE, 595
- FTM_RMW_CNT, 592
- FTM_RMW_CNTIN, 592
- FTM_RMW_CONF, 592
- FTM_RMW_CnSCV_REG, 591
- FTM_RMW_DEADTIME, 592
- FTM_RMW_EXTTTRIG_REG, 592
- FTM_RMW_FILTER, 592
- FTM_RMW_FLTCTRL, 592
- FTM_RMW_FMS, 592
- FTM_RMW_MOD, 592
- FTM_RMW_MODE, 592
- FTM_RMW_PAIR0DEADTIME, 593
- FTM_RMW_PAIR1DEADTIME, 593
- FTM_RMW_PAIR2DEADTIME, 593
- FTM_RMW_PAIR3DEADTIME, 593
- FTM_RMW_POL, 593
- FTM_RMW_QDCTRL, 593
- FTM_RMW_SC, 593
- FTM_RMW_STATUS, 593
- FTM_RMW_SYNC, 593
- FTM_SYSTEM_CLOCK, 596
- FTM_TIME_OVER_FLOW_FLAG, 596
- FTM_TIME_OVER_FLOW_INT_ENABLE, 595
- FTM_UPDATE_NOW, 596
- FTM_WAIT_LOADING_POINTS, 596
- ftm_bdm_mode_t, 594
- ftm_clock_ps_t, 594
- ftm_clock_source_t, 594
- ftm_config_mode_t, 594
- ftm_deadtime_ps_t, 595
- ftm_interrupt_option_t, 595
- ftm_pwm_sync_mode_t, 595
- ftm_reg_update_t, 596
- ftm_status_flag_t, 596
- ftmStatePtr, 618
- g_ftmBase, 618
- g_ftmFaultIrqlId, 618
- g_ftmIrqlId, 618
- g_ftmOverflowIrqlId, 618
- g_ftmReloadIrqlId, 618
- FlexTimer Input Capture Driver (FTM_IC), 619
 - FTM_BOTH_EDGES, 623
 - FTM_DISABLE_OPERATION, 623
 - FTM_DRV_DeinitInputCapture, 624
 - FTM_DRV_GetInputCaptureMeasurement, 624
 - FTM_DRV_InitInputCapture, 624
 - FTM_DRV_StartNewSignalMeasurement, 625
 - FTM_EDGE_DETECT, 623
 - FTM_FALLING_EDGE, 623
 - FTM_FALLING_EDGE_PERIOD_MEASUREMENT, 624
 - FTM_IC_DRV_SetChannelMode, 625
 - FTM_MEASURE_FALLING_EDGE_PERIOD, 623
 - FTM_MEASURE_PULSE_HIGH, 623
 - FTM_MEASURE_PULSE_LOW, 623
 - FTM_MEASURE_RISING_EDGE_PERIOD, 623
 - FTM_NO_MEASUREMENT, 624
 - FTM_NO_OPERATION, 623
 - FTM_NO_PIN_CONTROL, 623
 - FTM_PERIOD_OFF_MEASUREMENT, 624
 - FTM_PERIOD_ON_MEASUREMENT, 624
 - FTM_RISING_EDGE, 623
 - FTM_RISING_EDGE_PERIOD_MEASUREMENT, 624
 - FTM_SIGNAL_MEASUREMENT, 623
 - FTM_TIMESTAMP_BOTH_EDGES, 623
 - FTM_TIMESTAMP_FALLING_EDGE, 623
 - FTM_TIMESTAMP_RISING_EDGE, 623
 - ftm_edge_alignment_mode_t, 623
 - ftm_ic_op_mode_t, 623
 - ftm_input_op_mode_t, 623
 - ftm_signal_measurement_mode_t, 623
- FlexTimer Module Counter Driver (FTM_MC), 627
 - FTM_DRV_CounterRead, 629
 - FTM_DRV_CounterStart, 629
 - FTM_DRV_CounterStop, 629
 - FTM_DRV_InitCounter, 629
 - FTM_MC_DRV_GetDefaultConfig, 630
- FlexTimer Output Compare Driver (FTM_OC), 631
 - FTM_ABSOLUTE_VALUE, 634
 - FTM_CLEAR_ON_MATCH, 634
 - FTM_DISABLE_OUTPUT, 634
 - FTM_DRV_DeinitOutputCompare, 634
 - FTM_DRV_InitOutputCompare, 635
 - FTM_DRV_UpdateOutputCompareChannel, 635
 - FTM_RELATIVE_VALUE, 634
 - FTM_SET_ON_MATCH, 634
 - FTM_TOGGLE_ON_MATCH, 634
 - ftm_output_compare_mode_t, 634
 - ftm_output_compare_update_t, 634
- FlexTimer Pulse Width Modulation Driver (FTM_PWM), 637
 - FTM_DRV_ControlChannelOutput, 650
 - FTM_DRV_DeinitPwm, 650
 - FTM_DRV_FastUpdatePwmChannels, 650
 - FTM_DRV_InitPwm, 651
 - FTM_DRV_UpdatePwmChannel, 651
 - FTM_DRV_UpdatePwmPeriod, 652
 - FTM_DUTY_TO_TICKS_SHIFT, 649
 - FTM_FAULT_CONTROL_AUTO_ALL, 649
 - FTM_FAULT_CONTROL_DISABLED, 649
 - FTM_FAULT_CONTROL_MAN_ALL, 649
 - FTM_FAULT_CONTROL_MAN_EVEN, 649
 - FTM_HIGH_STATE, 650
 - FTM_LOW_STATE, 650

- FTM_MAIN_DUPLICATED, 650
- FTM_MAIN_INVERTED, 650
- FTM_MAX_DUTY_CYCLE, 649
- FTM_POLARITY_HIGH, 649
- FTM_POLARITY_LOW, 649
- FTM_PWM_UPDATE_IN_DUTY_CYCLE, 649
- FTM_PWM_UPDATE_IN_TICKS, 649
- ftm_fault_mode_t, 649
- ftm_polarity_t, 649
- ftm_pwm_update_option_t, 649
- ftm_safe_state_polarity_t, 649
- ftm_second_channel_polarity_t, 650
- FlexTimer Quadrature Decoder Driver (FTM_QD), 654
 - FTM_DRV_QuadDecodeStart, 658
 - FTM_DRV_QuadDecodeStop, 658
 - FTM_DRV_QuadGetState, 658
 - FTM_QD_DRV_GetDefaultConfig, 659
 - FTM_QUAD_COUNT_AND_DIR, 658
 - FTM_QUAD_PHASE_ENCODE, 658
 - FTM_QUAD_PHASE_INVERT, 658
 - FTM_QUAD_PHASE_NORMAL, 658
 - ftm_quad_decode_mode_t, 657
 - ftm_quad_phase_polarity_t, 658
- flexcan_callback_t
 - FlexCAN Driver, 517
- flexcan_data_info_t, 515
 - data_length, 515
 - is_remote, 515
 - msg_id_type, 515
- flexcan_error_callback_t
 - FlexCAN Driver, 517
- flexcan_event_type_t
 - FlexCAN Driver, 517
- flexcan_id_table_t, 515
 - id, 515
 - isExtendedFrame, 515
 - isRemoteFrame, 515
- flexcan_mb_handle_t, 513
 - isBlocking, 513
 - isRemote, 513
 - mb_message, 513
 - mbSema, 513
 - state, 514
- flexcan_mb_state_t
 - FlexCAN Driver, 518
- flexcan_msgbuff_id_type_t
 - FlexCAN Driver, 518
- flexcan_msgbuff_t, 512
 - cs, 513
 - data, 513
 - dataLen, 513
 - msgId, 513
- flexcan_operation_modes_t
 - FlexCAN Driver, 518
- flexcan_rx_fifo_id_element_format_t
 - FlexCAN Driver, 518
- flexcan_rx_fifo_id_filter_num_t
 - FlexCAN Driver, 519
- flexcan_rx_mask_type_t
 - FlexCAN Driver, 519
- flexcan_rxfifo_transfer_type_t
 - FlexCAN Driver, 519
- flexcan_state_t
 - FlexCAN Driver, 517
- flexcan_time_segment_t, 516
 - phaseSeg1, 516
 - phaseSeg2, 516
 - preDivider, 516
 - propSeg, 516
 - rJumpwidth, 516
- flexcan_user_config_t, 516
 - bitrate, 517
 - flexcanMode, 517
 - is_rx_fifo_needed, 517
 - max_num_mb, 517
 - num_id_filters, 517
 - transfer_type, 517
- flexcanMode
 - flexcan_user_config_t, 517
- Flexible I/O (FlexIO), 660
- flexio_driver_type_t
 - FlexIO Common Driver, 528
- flexio_i2c_master_state_t, 535
- flexio_i2c_master_user_config_t, 534
 - baudRate, 534
 - callback, 534
 - callbackParam, 534
 - driverType, 534
 - rxDMACHannel, 534
 - sclPin, 534
 - sdaPin, 534
 - slaveAddress, 535
 - txDMACHannel, 535
- flexio_i2s_master_state_t, 546
- flexio_i2s_master_user_config_t, 543
 - baudRate, 544
 - bitsWidth, 544
 - callback, 544
 - callbackParam, 544
 - driverType, 544
 - rxDMACHannel, 544
 - rxPin, 544
 - sckPin, 544
 - txDMACHannel, 544
 - txPin, 544
 - wsPin, 544
- flexio_i2s_slave_state_t
 - FlexIO I2S Driver, 546
- flexio_i2s_slave_user_config_t, 545
 - bitsWidth, 545
 - callback, 545
 - callbackParam, 545
 - driverType, 545
 - rxDMACHannel, 545
 - rxPin, 545
 - sckPin, 545

- txDMAChannel, [546](#)
- txPin, [546](#)
- wsPin, [546](#)
- flexio_spi_master_state_t, [564](#)
- flexio_spi_master_user_config_t, [561](#)
 - baudRate, [561](#)
 - bitOrder, [561](#)
 - callback, [561](#)
 - callbackParam, [562](#)
 - clockPhase, [562](#)
 - clockPolarity, [562](#)
 - driverType, [562](#)
 - misoPin, [562](#)
 - mosiPin, [562](#)
 - rxDMAChannel, [562](#)
 - sckPin, [562](#)
 - ssPin, [562](#)
 - transferSize, [562](#)
 - txDMAChannel, [562](#)
- flexio_spi_slave_state_t
 - FlexIO SPI Driver, [564](#)
- flexio_spi_slave_user_config_t, [563](#)
 - bitOrder, [563](#)
 - callback, [563](#)
 - callbackParam, [563](#)
 - clockPhase, [563](#)
 - clockPolarity, [563](#)
 - driverType, [563](#)
 - misoPin, [564](#)
 - mosiPin, [564](#)
 - rxDMAChannel, [564](#)
 - sckPin, [564](#)
 - ssPin, [564](#)
 - transferSize, [564](#)
 - txDMAChannel, [564](#)
- flexio_spi_transfer_bit_order_t
 - FlexIO SPI Driver, [565](#)
- flexio_spi_transfer_size_t
 - FlexIO SPI Driver, [565](#)
- flexio_uart_driver_direction_t
 - FlexIO UART Driver, [576](#)
- flexio_uart_state_t, [575](#)
- flexio_uart_user_config_t, [574](#)
 - baudRate, [575](#)
 - bitCount, [575](#)
 - callback, [575](#)
 - callbackParam, [575](#)
 - dataPin, [575](#)
 - direction, [575](#)
 - dmaChannel, [575](#)
 - driverType, [575](#)
- fltErrFs
 - fs45_fault_reg_t, [1057](#)
- fltErrImp
 - fs45_fault_reg_t, [1057](#)
- fnmc
 - sbc_sbc_t, [1176](#)
- fnms
 - sbc_wdog_status_t, [1184](#)
- fp_int, [1282](#)
 - dp, [1282](#)
 - sign, [1282](#)
 - used, [1282](#)
- frac
 - peripheral_clock_config_t, [335](#)
- fragList
 - DtlsMsg, [1279](#)
- fragOffset
 - WOLFSSL, [1338](#)
- fragSz
 - DtlsMsg, [1279](#)
- fragment_length
 - DtlsHandShakeHeader, [1279](#)
- fragment_offset
 - DtlsHandShakeHeader, [1279](#)
- frame
 - sbc_can_conf_t, [1180](#)
- frame_counter
 - lin_tl_descriptor_t, [835](#)
- frame_data_ptr
 - lin_frame_t, [832](#)
- frame_start
 - lin_protocol_user_config_t, [838](#)
- frame_tbl_ptr
 - lin_protocol_user_config_t, [838](#)
- frame_timeout_cnt
 - lin_protocol_state_t, [842](#)
- FrameSize
 - sai_user_config_t, [1040](#)
- frameSize
 - spi_master_t, [1105](#)
 - spi_slave_t, [1106](#)
- FrameStartReport
 - sai_user_config_t, [1040](#)
- FreeRTOS, [661](#)
- freeRun
 - lptmr_config_t, [794](#)
- freq
 - scg_sosc_config_t, [328](#)
- frm_id
 - lin_schedule_data_t, [833](#)
- frm_len
 - lin_frame_t, [832](#)
- frm_offset
 - lin_frame_t, [832](#)
 - lin_master_data_t, [840](#)
- frm_response
 - lin_frame_t, [832](#)
- frm_size
 - lin_master_data_t, [840](#)
- frm_type
 - lin_frame_t, [832](#)
- from
 - smtp_send_request, [1325](#)
- fs1bCanImpact
 - fs45_fault_reg_t, [1057](#)

- fs1bTime
 - fs45_fs1b_timing_reg_t, [1056](#)
- fs1bTimeRange
 - fs45_supervisor_reg_t, [1057](#)
- fs1bTimingReg
 - fs45_drv_config_t, [1061](#)
- fs45_amux_selection_t
 - SBC FS45 Driver, [1063](#)
- fs45_can_mode_t
 - SBC FS45 Driver, [1063](#)
- fs45_current_mode_t
 - SBC FS45 Driver, [1063](#)
- fs45_drv_config_t, [1060](#)
 - faultReg, [1061](#)
 - fs1bTimingReg, [1061](#)
 - fssmReg, [1062](#)
 - inhIntReg, [1062](#)
 - intReg, [1062](#)
 - nonInitRegs, [1062](#)
 - nonInitRegsCount, [1062](#)
 - sflImpactReg, [1062](#)
 - supervisorReg, [1062](#)
 - vauxOvuvImpactReg, [1062](#)
 - vccaOvuvImpactReg, [1062](#)
 - vcoreOvuvImpactReg, [1062](#)
 - vregReg, [1062](#)
 - wdCntReg, [1063](#)
 - wu1Reg, [1063](#)
 - wu2Reg, [1063](#)
- fs45_fault_reg_t, [1057](#)
 - fltErrFs, [1057](#)
 - fltErrImp, [1057](#)
 - fs1bCanImpact, [1057](#)
- fs45_fs1b_timing_reg_t, [1056](#)
 - fs1bTime, [1056](#)
- fs45_fssm_reg_t, [1058](#)
 - io23Fs, [1058](#)
 - io45Fs, [1058](#)
 - ps, [1058](#)
 - rstbDuration, [1058](#)
- fs45_fsx_req_type_t
 - SBC FS45 Driver, [1064](#)
- fs45_fsxb_release_t
 - SBC FS45 Driver, [1064](#)
- fs45_inh_int_reg_t, [1055](#)
 - inh0, [1056](#)
 - inh2, [1056](#)
 - inh3, [1056](#)
 - inh4, [1056](#)
 - inh5, [1056](#)
- fs45_int_reg_t, [1054](#)
 - duration, [1055](#)
 - inhAll, [1055](#)
 - inhCan, [1055](#)
 - inhLin, [1055](#)
 - inhVcore, [1055](#)
 - inhVother, [1055](#)
 - inhVpre, [1055](#)
 - inhVsns, [1055](#)
- fs45_ldt_function_t
 - SBC FS45 Driver, [1064](#)
- fs45_ldt_mode_t
 - SBC FS45 Driver, [1064](#)
- fs45_ldt_wu_scr_t
 - SBC FS45 Driver, [1065](#)
- fs45_prev_mode_t
 - SBC FS45 Driver, [1065](#)
- fs45_reg_config_value_t, [1051](#)
 - address, [1051](#)
 - readMask, [1051](#)
 - value, [1052](#)
- fs45_reg_mode_t
 - SBC FS45 Driver, [1065](#)
- fs45_rx_data_t, [1051](#)
 - deviceStatus, [1051](#)
 - deviceStatusEx, [1051](#)
 - readData, [1051](#)
- fs45_sf_impact_reg_t, [1058](#)
 - dis8s, [1059](#)
 - tdlyTdur, [1059](#)
 - wdImpact, [1059](#)
- fs45_supervisor_reg_t, [1056](#)
 - fs1bTimeRange, [1057](#)
 - vaux5d, [1057](#)
 - vcca5d, [1057](#)
 - vcore5d, [1057](#)
- fs45_tx_data_t, [1282](#)
 - commandType, [1283](#)
 - isSecured, [1283](#)
 - registerAddress, [1283](#)
 - writeData, [1283](#)
- fs45_vaux_ovuv_impact_reg_t, [1060](#)
 - vauxFsOv, [1060](#)
 - vauxFsUv, [1060](#)
- fs45_vcca_ovuv_impact_reg_t, [1060](#)
 - vccaFsOv, [1060](#)
 - vccaFsUv, [1060](#)
- fs45_vcore_ovuv_impact_reg_t, [1059](#)
 - vcoreFsOv, [1059](#)
 - vcoreFsUv, [1060](#)
- fs45_vreg_reg_t, [1052](#)
 - iccaLim, [1052](#)
 - ipffDis, [1052](#)
 - tauxLimOff, [1052](#)
 - tccaLimOff, [1052](#)
 - vauxTrkEn, [1052](#)
 - vcanOvMon, [1052](#)
- fs45_wd_cnt_reg_t, [1059](#)
 - wdCntErr, [1059](#)
 - wdCntRfr, [1059](#)
- fs45_wd_window_t
 - SBC FS45 Driver, [1065](#)
- fs45_wu1_reg_t, [1053](#)
 - wulo0, [1053](#)
 - wulo2, [1053](#)
 - wulo3, [1053](#)

- wulo4, [1053](#)
- fs45_wu2_reg_t, [1053](#)
 - canDisCfg, [1054](#)
 - canWuTo, [1054](#)
 - linJ2602Dis, [1054](#)
 - linSr, [1054](#)
 - wulo5, [1054](#)
- fs45AmuxDieTempSensor
 - SBC FS45 Driver, [1063](#)
- fs45AmuxIO_0Tight
 - SBC FS45 Driver, [1063](#)
- fs45AmuxIO_0Wide
 - SBC FS45 Driver, [1063](#)
- fs45AmuxIO_5TightDivVkam
 - SBC FS45 Driver, [1063](#)
- fs45AmuxIO_5Wide
 - SBC FS45 Driver, [1063](#)
- fs45AmuxVref
 - SBC FS45 Driver, [1063](#)
- fs45AmuxVsnsTight
 - SBC FS45 Driver, [1063](#)
- fs45AmuxVsnsWide
 - SBC FS45 Driver, [1063](#)
- fs45Aux
 - SBC FS45 Driver, [1065](#)
- fs45CanModeListenOnly
 - SBC FS45 Driver, [1063](#)
- fs45CanModeNormal
 - SBC FS45 Driver, [1063](#)
- fs45CanModeSleepNoWakeup
 - SBC FS45 Driver, [1063](#)
- fs45CanModeSleepWakeup
 - SBC FS45 Driver, [1063](#)
- fs45LdtFunc1
 - SBC FS45 Driver, [1064](#)
- fs45LdtFunc2
 - SBC FS45 Driver, [1064](#)
- fs45LdtFunc3
 - SBC FS45 Driver, [1064](#)
- fs45LdtFunc4
 - SBC FS45 Driver, [1064](#)
- fs45LdtFunc5
 - SBC FS45 Driver, [1064](#)
- fs45LdtModeCalibration
 - SBC FS45 Driver, [1065](#)
- fs45LdtModeNormal
 - SBC FS45 Driver, [1065](#)
- fs45LdtWakeupProg
 - SBC FS45 Driver, [1065](#)
- fs45LdtWakeupRTC
 - SBC FS45 Driver, [1065](#)
- fs45Modelnit
 - SBC FS45 Driver, [1064](#)
- fs45ModeNormal
 - SBC FS45 Driver, [1064](#)
- fs45ModeUnknown
 - SBC FS45 Driver, [1064](#)
- fs45PrevModeDFS
 - SBC FS45 Driver, [1065](#)
- fs45PrevModeLPOFF
 - SBC FS45 Driver, [1065](#)
- fs45PrevModePOR
 - SBC FS45 Driver, [1065](#)
- fs45ReleaseFs0b
 - SBC FS45 Driver, [1064](#)
- fs45ReleaseFs0bFs1b
 - SBC FS45 Driver, [1064](#)
- fs45ReleaseFs1b
 - SBC FS45 Driver, [1064](#)
- fs45ReqFS0B
 - SBC FS45 Driver, [1064](#)
- fs45ReqFS1B
 - SBC FS45 Driver, [1064](#)
- fs45ReqFS1BDelay
 - SBC FS45 Driver, [1064](#)
- fs45VCan
 - SBC FS45 Driver, [1065](#)
- fs45Vcca
 - SBC FS45 Driver, [1065](#)
- fs45Vcore
 - SBC FS45 Driver, [1065](#)
- fs45Vkam
 - SBC FS45 Driver, [1065](#)
- fs45WdWindow1024ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow128ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow12ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow16ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow1ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow24ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow256ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow2ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow32ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow3ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow4ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow512ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow64ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow6ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindow8ms
 - SBC FS45 Driver, [1066](#)
- fs45WdWindowDisable
 - SBC FS45 Driver, [1066](#)
- fscCfg

- uja113x_init_cfg_t, [184](#)
- fsMReg
 - fs45_drv_config_t, [1062](#)
- ftm_bdm_mode_t
 - FlexTimer (FTM), [594](#)
- ftm_clock_ps_t
 - FlexTimer (FTM), [594](#)
- ftm_clock_source_t
 - FlexTimer (FTM), [594](#)
- ftm_combined_ch_param_t, [646](#)
 - deadTime, [646](#)
 - enableExternalTrigger, [646](#)
 - enableExternalTriggerOnNextChn, [646](#)
 - enableModifiedCombine, [646](#)
 - enableSecondChannelOutput, [647](#)
 - firstEdge, [647](#)
 - hwChannelId, [647](#)
 - mainChannelPolarity, [647](#)
 - mainChannelSafeState, [647](#)
 - secondChannelPolarity, [647](#)
 - secondChannelSafeState, [647](#)
 - secondEdge, [647](#)
- ftm_config_mode_t
 - FlexTimer (FTM), [594](#)
- ftm_deadtime_ps_t
 - FlexTimer (FTM), [595](#)
- ftm_edge_alignment_mode_t
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- ftm_fault_mode_t
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [649](#)
- ftm_ic_op_mode_t
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- ftm_independent_ch_param_t, [645](#)
 - deadTime, [645](#)
 - enableExternalTrigger, [645](#)
 - enableSecondChannelOutput, [645](#)
 - hwChannelId, [645](#)
 - polarity, [645](#)
 - safeState, [646](#)
 - secondChannelPolarity, [646](#)
 - uDutyCyclePercent, [646](#)
- ftm_input_ch_param_t, [621](#)
 - channelsCallbacks, [621](#)
 - channelsCallbacksParams, [621](#)
 - continuousModeEn, [622](#)
 - edgeAlignment, [622](#)
 - filterEn, [622](#)
 - filterValue, [622](#)
 - hwChannelId, [622](#)
 - inputMode, [622](#)
 - measurementType, [622](#)
- ftm_input_op_mode_t
 - FlexTimer Input Capture Driver (FTM_IC), [623](#)
- ftm_input_param_t, [622](#)
 - inputChConfig, [622](#)
 - nMaxCountValue, [623](#)
 - numChannels, [623](#)
- ftm_interrupt_option_t
 - FlexTimer (FTM), [595](#)
- ftm_output_cmp_ch_param_t, [633](#)
 - chMode, [633](#)
 - comparedValue, [633](#)
 - enableExternalTrigger, [633](#)
 - hwChannelId, [633](#)
- ftm_output_cmp_param_t, [633](#)
 - maxCountValue, [633](#)
 - mode, [633](#)
 - nNumOutputChannels, [634](#)
 - outputChannelConfig, [634](#)
- ftm_output_compare_mode_t
 - FlexTimer Output Compare Driver (FTM_OC), [634](#)
- ftm_output_compare_update_t
 - FlexTimer Output Compare Driver (FTM_OC), [634](#)
- ftm_phase_params_t, [656](#)
 - phaseFilterVal, [656](#)
 - phaseInputFilter, [656](#)
 - phasePolarity, [656](#)
- ftm_polarity_t
 - FlexTimer Pulse Width Modulation Driver (FTM_↔PWM), [649](#)
- ftm_pwm_ch_fault_param_t, [644](#)
 - faultChannelEnabled, [644](#)
 - faultFilterEnabled, [644](#)
 - ftmFaultPinPolarity, [644](#)
- ftm_pwm_fault_param_t, [644](#)
 - faultFilterValue, [644](#)
 - faultMode, [644](#)
 - ftmFaultChannelParam, [644](#)
 - pwmFaultInterrupt, [645](#)
 - pwmOutputStateOnFault, [645](#)
- ftm_pwm_param_t, [647](#)
 - deadTimePrescaler, [648](#)
 - deadTimeValue, [648](#)
 - faultConfig, [648](#)
 - mode, [648](#)
 - nNumCombinedPwmChannels, [648](#)
 - nNumIndependentPwmChannels, [648](#)
 - pwmCombinedChannelConfig, [648](#)
 - pwmIndependentChannelConfig, [648](#)
 - uFrequencyHZ, [648](#)
- ftm_pwm_sync_mode_t
 - FlexTimer (FTM), [595](#)
- ftm_pwm_sync_t, [588](#)
 - autoClearTrigger, [589](#)
 - hardwareSync0, [589](#)
 - hardwareSync1, [589](#)
 - hardwareSync2, [589](#)
 - initCounterSync, [589](#)
 - inverterSync, [589](#)
 - maskRegSync, [589](#)
 - maxLoadingPoint, [589](#)
 - minLoadingPoint, [589](#)
 - outRegSync, [590](#)
 - softwareSync, [590](#)
 - syncPoint, [590](#)

- ftm_pwm_update_option_t
 - FlexTimer Pulse Width Modulation Driver (FTM_↔ PWM), 649
- ftm_quad_decode_config_t, 656
 - initialVal, 656
 - maxVal, 656
 - mode, 656
 - phaseAConfig, 657
 - phaseBConfig, 657
- ftm_quad_decode_mode_t
 - FlexTimer Quadrature Decoder Driver (FTM_QD), 657
- ftm_quad_decoder_state_t, 657
 - counter, 657
 - counterDirection, 657
 - overflowDirection, 657
 - overflowFlag, 657
- ftm_quad_phase_polarity_t
 - FlexTimer Quadrature Decoder Driver (FTM_QD), 658
- ftm_reg_update_t
 - FlexTimer (FTM), 596
- ftm_safe_state_polarity_t
 - FlexTimer Pulse Width Modulation Driver (FTM_↔ PWM), 649
- ftm_second_channel_polarity_t
 - FlexTimer Pulse Width Modulation Driver (FTM_↔ PWM), 650
- ftm_signal_measurement_mode_t
 - FlexTimer Input Capture Driver (FTM_IC), 623
- ftm_state_t, 587
 - channelsCallbacks, 588
 - channelsCallbacksParams, 588
 - enableNotification, 588
 - ftmClockSource, 588
 - ftmModValue, 588
 - ftmMode, 588
 - ftmPeriod, 588
 - ftmSourceClockFrequency, 588
 - measurementResults, 588
- ftm_status_flag_t
 - FlexTimer (FTM), 596
- ftm_timer_param_t, 628
 - finalValue, 628
 - initialValue, 628
 - mode, 629
- ftm_user_config_t, 590
 - BDMMode, 590
 - enableInitializationTrigger, 590
 - ftmClockSource, 590
 - ftmMode, 590
 - ftmPrescaler, 590
 - isTofIsrEnabled, 591
 - syncMethod, 591
- ftmClockSource
 - extension_ftm_for_ic_t, 689
 - extension_ftm_for_oc_t, 923
 - ftm_state_t, 588
- ftm_user_config_t, 590
- ftmFaultChannelParam
 - ftm_pwm_fault_param_t, 644
- ftmFaultPinPolarity
 - ftm_pwm_ch_fault_param_t, 644
- ftmModValue
 - ftm_state_t, 588
- ftmMode
 - ftm_state_t, 588
 - ftm_user_config_t, 590
- ftmPeriod
 - ftm_state_t, 588
- ftmPrescaler
 - extension_ftm_for_ic_t, 689
 - extension_ftm_for_oc_t, 923
 - ftm_user_config_t, 590
- ftmSourceClockFrequency
 - ftm_state_t, 588
- ftmStatePtr
 - FlexTimer (FTM), 618
- fullName
 - DecodedName, 1270
- fullNameLen
 - DecodedName, 1270
- fullSize
 - csec_state_t, 300
- func_args, 1283
 - argc, 1283
 - argv, 1283
 - callbacks, 1283
 - return_code, 1283
 - signal, 1284
- function
 - lin_protocol_user_config_t, 838
- function_id
 - lin_product_id_t, 1292
- fwdPhyLocal
 - phy_tja110x_config_t, 1139
- fwdPhyRemote
 - phy_tja110x_config_t, 1139
- g
 - DhKey, 1274
 - DhParams, 1274
 - DsaKey, 1276
 - WOLFSSL_DH, 1355
 - WOLFSSL_DSA, 1356
- g_RtcClkInFreq
 - Clock Manager Driver, 354
- g_TClkFreq
 - Clock Manager Driver, 354
- g_buffer_backup_data
 - Low level API, 854
- g_drivers
 - 00. Library internals, 188
- g_ftmBase
 - FlexTimer (FTM), 618
- g_ftmFaultIrqId
 - FlexTimer (FTM), 618

- g_ftmIrqId
 - FlexTimer (FTM), [618](#)
- g_ftmOverflowIrqId
 - FlexTimer (FTM), [618](#)
- g_ftmReloadIrqId
 - FlexTimer (FTM), [618](#)
- g_len
 - DhParams, [1274](#)
- g_lin_flag_handle_tbl
 - Low level API, [854](#)
- g_lin_frame_data_buffer
 - Low level API, [854](#)
- g_lin_frame_flag_handle_tbl
 - Low level API, [854](#)
- g_lin_frame_updating_flag_tbl
 - Low level API, [854](#)
- g_lin_hardware_ifc
 - Low level API, [854](#)
- g_lin_master_data_array
 - Low level API, [854](#)
- g_lin_node_attribute_array
 - Low level API, [854](#)
- g_lin_protocol_state_array
 - Low level API, [854](#)
- g_lin_protocol_user_cfg_array
 - Low level API, [854](#)
- g_lin_tl_descriptor_array
 - Low level API, [854](#)
- g_lin_virtual_ifc
 - Low level API, [855](#)
- g_linLpuartIsrs
 - LIN Driver, [738](#)
- g_lpspiBase
 - LPSPi Driver, [790](#)
- g_lpspiIrqId
 - LPSPi Driver, [790](#)
- g_lpspiStatePtr
 - LPSPi Driver, [790](#)
- g_phyConfig
 - PHY Framework, [957](#)
- g_qspiBase
 - QuadSPi Driver, [998](#)
- g_xtal0ClkFreq
 - Clock Manager Driver, [354](#)
- GENERAL_REJECT
 - Common Transport Layer API, [357](#)
- GENERAL_STATUS_ADDR
 - TJA110x PHY, [1143](#)
- GENERAL_STATUS_ENSTATUS_FLAG
 - TJA110x PHY, [1143](#)
- GENERAL_STATUS_INT_STATUS_FLAG
 - TJA110x PHY, [1143](#)
- GENERAL_STATUS_PLL_LOCKED_FLAG
 - TJA110x PHY, [1143](#)
- GENERAL_STATUS_RSTSTATUS_FLAG
 - TJA110x PHY, [1143](#)
- GET_BIT_0_7
 - Flash Memory (Flash), [490](#)
- GET_BIT_16_23
 - Flash Memory (Flash), [490](#)
- GET_BIT_24_31
 - Flash Memory (Flash), [490](#)
- GET_BIT_8_15
 - Flash Memory (Flash), [490](#)
- GIS_ADDRESS
 - Register address map, [1027](#)
- GO_TO_SLEEP_SET
 - Common Core API., [355](#)
- GPIO_INPUT_DIRECTION
 - PINS Driver, [959](#)
- GPIO_OUTPUT_DIRECTION
 - PINS Driver, [959](#)
- GPIO_UNSPECIFIED_DIRECTION
 - PINS Driver, [959](#)
- gPowerManagerState
 - Power Manager, [975](#)
- gain
 - scg_sosc_config_t, [329](#)
- gating
 - module_clk_config_t, [337](#)
- Generic PHY, [662](#)
 - AUTONEG_1000BASETFD, [663](#)
 - AUTONEG_1000BASETHD, [663](#)
 - AUTONEG_100BASETXFD, [663](#)
 - AUTONEG_100BASETXHD, [663](#)
 - AUTONEG_10BASETFD, [663](#)
 - AUTONEG_10BASETHD, [663](#)
 - AUTONEG_ADVERT_ADDR, [664](#)
 - AUTONEG_LPABILITY_ADDR, [664](#)
 - BASIC_CONTROL_ADDR, [664](#)
 - BASIC_CONTROL_AUTONEG_FLAG, [664](#)
 - BASIC_CONTROL_LOOPBACK_FLAG, [664](#)
 - BASIC_CONTROL_PDOWN_FLAG, [664](#)
 - BASIC_CONTROL_RESET_FLAG, [664](#)
 - BASIC_CONTROL_RESTART_AUTONEG_FLAG, [664](#)
 - BASIC_CONTROL_SPEED_LSB_FLAG, [664](#)
 - BASIC_CONTROL_SPEED_MSB_FLAG, [664](#)
 - CONTROL_1000BASET_ADDR, [664](#)
 - CONTROL_1000BASET_CONFIG_ENABLE_FLAG, [664](#)
 - CONTROL_1000BASET_CONFIG_VALUE_FLAG, [664](#)
 - CONTROL_STATUS_1000BASET_OFFSET, [664](#)
 - checkCapabilities, [665](#)
 - disableAutoneg, [665](#)
 - EXTENDED_STATUS_1000BASETFD_FLAG, [664](#)
 - EXTENDED_STATUS_1000BASETHD_FLAG, [665](#)
 - EXTENDED_STATUS_ADDR, [665](#)
 - enableAutoneg, [665](#)
 - getDelay, [665](#)
 - getId, [665](#)
 - getLinkSpeed, [665](#)
 - getLinkStatus, [665](#)

- getState, 665
- ID_1_ADDR, 665
- ID_2_ADDR, 665
- init, 666
- mainFunction, 666
- PHY_driver_generic, 666
- reset, 666
- restartAutoneg, 666
- resume, 666
- returnNotSupportUint8Param, 666
- STATUS_1000BASET_ADDR, 665
- setLoopback, 666
- setRole, 666
- suspend, 666
- T_RST_MAX, 665
- getDelay
 - Generic PHY, 665
 - phy_driver_t, 948
- getId
 - Generic PHY, 665
 - phy_driver_t, 948
- getLinkSpeed
 - Generic PHY, 665
 - phy_driver_t, 949
- getLinkStatus
 - Generic PHY, 665
 - phy_driver_t, 949
- getState
 - Generic PHY, 665
 - phy_driver_t, 949
 - TJA110x PHY, 1145
- glEvt
 - sbc_evt_capt_t, 1189
- go_to_sleep_flg
 - lin_protocol_state_t, 842
 - lin_word_status_str_t, 828
- goFromStandbyToNormalMode
 - TJA110x PHY, 1145
- got_certificate
 - MsgsReceived, 1296
- got_certificate_request
 - MsgsReceived, 1296
- got_certificate_status
 - MsgsReceived, 1296
- got_certificate_verify
 - MsgsReceived, 1296
- got_change_cipher
 - MsgsReceived, 1296
- got_client_hello
 - MsgsReceived, 1296
- got_client_key_exchange
 - MsgsReceived, 1296
- got_encrypted_extensions
 - MsgsReceived, 1297
- got_end_of_early_data
 - MsgsReceived, 1297
- got_finished
 - MsgsReceived, 1297
- got_hello_request
 - MsgsReceived, 1297
- got_hello_retry_request
 - MsgsReceived, 1297
- got_hello_verify_request
 - MsgsReceived, 1297
- got_key_update
 - MsgsReceived, 1297
- got_server_hello
 - MsgsReceived, 1297
- got_server_hello_done
 - MsgsReceived, 1297
- got_server_key_exchange
 - MsgsReceived, 1297
- got_session_ticket
 - MsgsReceived, 1297
- gpioBase
 - pin_settings_config_t, 959
- group
 - WOLFSSL_EC_KEY, 1359
- groupConfigArray
 - adc_config_t, 275
- groupIndex
 - adc_callback_info_t, 1247
- groupMessages
 - Options, 1302
 - WOLFSSL_CTX, 1352
- HC128, 1286
 - counter1024, 1286
 - iv, 1286
 - key, 1287
 - T, 1287
 - X, 1287
 - Y, 1287
- HHSDC_IO1HOC_DISABLED
 - HVIO high-side configuration options (0x71), 669
- HHSDC_IO1HOC_ENABLED
 - HVIO high-side configuration options (0x71), 669
- HHSDC_IO2HOC_DISABLED
 - HVIO high-side configuration options (0x71), 669
- HHSDC_IO2HOC_ENABLED
 - HVIO high-side configuration options (0x71), 669
- HHSDC_IO3HOC_DISABLED
 - HVIO high-side configuration options (0x71), 669
- HHSDC_IO3HOC_ENABLED
 - HVIO high-side configuration options (0x71), 669
- HHSDC_IO4HOC_DISABLED
 - HVIO high-side configuration options (0x71), 669
- HHSDC_IO4HOC_ENABLED
 - HVIO high-side configuration options (0x71), 669
- HHSDC_IO5HOC_DISABLED
 - HVIO high-side configuration options (0x71), 669
- HHSDC_IO5HOC_ENABLED
 - HVIO high-side configuration options (0x71), 670
- HHSDC_IO6HOC_DISABLED
 - HVIO high-side configuration options (0x71), 670
- HHSDC_IO6HOC_ENABLED
 - HVIO high-side configuration options (0x71), 670

- HHSDC_IO7HOC_DISABLED
 - HVIO high-side configuration options (0x71), [670](#)
- HHSDC_IO7HOC_ENABLED
 - HVIO high-side configuration options (0x71), [670](#)
- HHSDC_IO8HOC_DISABLED
 - HVIO high-side configuration options (0x71), [670](#)
- HHSDC_IO8HOC_ENABLED
 - HVIO high-side configuration options (0x71), [670](#)
- HLSDC_IO1LOC_DISABLED
 - HVIO low-side configuration options (0x72), [672](#)
- HLSDC_IO1LOC_ENABLED
 - HVIO low-side configuration options (0x72), [672](#)
- HLSDC_IO2LOC_DISABLED
 - HVIO low-side configuration options (0x72), [672](#)
- HLSDC_IO2LOC_ENABLED
 - HVIO low-side configuration options (0x72), [672](#)
- HLSDC_IO3LOC_DISABLED
 - HVIO low-side configuration options (0x72), [672](#)
- HLSDC_IO3LOC_ENABLED
 - HVIO low-side configuration options (0x72), [672](#)
- HLSDC_IO4LOC_DISABLED
 - HVIO low-side configuration options (0x72), [672](#)
- HLSDC_IO4LOC_ENABLED
 - HVIO low-side configuration options (0x72), [672](#)
- HLSDC_IO5LOC_DISABLED
 - HVIO low-side configuration options (0x72), [672](#)
- HLSDC_IO5LOC_ENABLED
 - HVIO low-side configuration options (0x72), [673](#)
- HLSDC_IO6LOC_DISABLED
 - HVIO low-side configuration options (0x72), [673](#)
- HLSDC_IO6LOC_ENABLED
 - HVIO low-side configuration options (0x72), [673](#)
- HLSDC_IO7LOC_DISABLED
 - HVIO low-side configuration options (0x72), [673](#)
- HLSDC_IO7LOC_ENABLED
 - HVIO low-side configuration options (0x72), [673](#)
- HLSDC_IO8LOC_DISABLED
 - HVIO low-side configuration options (0x72), [673](#)
- HLSDC_IO8LOC_ENABLED
 - HVIO low-side configuration options (0x72), [673](#)
- HOURS_IN_A_DAY
 - RTC Driver, [1005](#)
- HS_Hashes, [1288](#)
 - certHashes, [1288](#)
 - hashMd5, [1288](#)
 - hashSha, [1288](#)
 - hashSha256, [1288](#)
 - verifyHashes, [1288](#)
- HSRUN_MODE
 - Clock Manager Driver, [344](#)
- HVIO high-side configuration options (0x71), [668](#)
 - HHSDC_IO1HOC_DISABLED, [669](#)
 - HHSDC_IO1HOC_ENABLED, [669](#)
 - HHSDC_IO2HOC_DISABLED, [669](#)
 - HHSDC_IO2HOC_ENABLED, [669](#)
 - HHSDC_IO3HOC_DISABLED, [669](#)
 - HHSDC_IO3HOC_ENABLED, [669](#)
 - HHSDC_IO4HOC_DISABLED, [669](#)
 - HHSDC_IO4HOC_ENABLED, [669](#)
 - HHSDC_IO5HOC_DISABLED, [669](#)
 - HHSDC_IO5HOC_ENABLED, [670](#)
 - HHSDC_IO6HOC_DISABLED, [670](#)
 - HHSDC_IO6HOC_ENABLED, [670](#)
 - HHSDC_IO7HOC_DISABLED, [670](#)
 - HHSDC_IO7HOC_ENABLED, [670](#)
 - HHSDC_IO8HOC_DISABLED, [670](#)
 - HHSDC_IO8HOC_ENABLED, [670](#)
- HVIO low-side configuration options (0x72), [671](#)
 - HLSDC_IO1LOC_DISABLED, [672](#)
 - HLSDC_IO1LOC_ENABLED, [672](#)
 - HLSDC_IO2LOC_DISABLED, [672](#)
 - HLSDC_IO2LOC_ENABLED, [672](#)
 - HLSDC_IO3LOC_DISABLED, [672](#)
 - HLSDC_IO3LOC_ENABLED, [672](#)
 - HLSDC_IO4LOC_DISABLED, [672](#)
 - HLSDC_IO4LOC_ENABLED, [672](#)
 - HLSDC_IO5LOC_DISABLED, [672](#)
 - HLSDC_IO5LOC_ENABLED, [673](#)
 - HLSDC_IO6LOC_DISABLED, [673](#)
 - HLSDC_IO6LOC_ENABLED, [673](#)
 - HLSDC_IO7LOC_DISABLED, [673](#)
 - HLSDC_IO7LOC_ENABLED, [673](#)
 - HLSDC_IO8LOC_DISABLED, [673](#)
 - HLSDC_IO8LOC_ENABLED, [673](#)
- HVIO1C_ADDRESS
 - Register address map, [1027](#)
- HVIO2C_ADDRESS
 - Register address map, [1027](#)
- HVIO3C_ADDRESS
 - Register address map, [1028](#)
- HVIO4C_ADDRESS
 - Register address map, [1028](#)
- HVIO5C_ADDRESS
 - Register address map, [1028](#)
- HVIO6C_ADDRESS
 - Register address map, [1028](#)
- HVIO7C_ADDRESS
 - Register address map, [1028](#)
- HVIO8C_ADDRESS
 - Register address map, [1028](#)
- HVIOHSDRVC_ADDRESS
 - Register address map, [1028](#)
- HVIOLSDRVC_ADDRESS
 - Register address map, [1028](#)
- haltOnError
 - edma_user_config_t, [416](#)
- handShakeDone
 - Options, [1302](#)
- HandShakeHeader, [1284](#)
 - length, [1284](#)
 - type, [1284](#)
- handShakeInfo_st, [1284](#)
 - cipherName, [1285](#)
 - negotiationError, [1285](#)
 - numberPackets, [1285](#)
 - packetNames, [1285](#)

- ssl, [1285](#)
- handShakeState
 - Options, [1302](#)
- handleInterrupt
 - phy_driver_t, [949](#)
 - TJA110x PHY, [1145](#)
- handleInterruptLinkDown
 - TJA110x PHY, [1145](#)
- handleInterruptLinkUp
 - TJA110x PHY, [1145](#)
- handleInterruptPwon
 - TJA110x PHY, [1145](#)
- handleInterruptSleep
 - TJA110x PHY, [1145](#)
- handleInterruptWakeUp
 - TJA110x PHY, [1145](#)
- hardwareSync0
 - ftm_pwm_sync_t, [589](#)
- hardwareSync1
 - ftm_pwm_sync_t, [589](#)
- hardwareSync2
 - ftm_pwm_sync_t, [589](#)
- Hash, [1285](#)
 - md5, [1285](#)
 - sha, [1285](#)
 - sha256, [1285](#)
- hash
 - Hmac, [1287](#)
 - WOLFSSL_EVP_MD_CTX, [1362](#)
 - wolfssl_TI_Hash, [1372](#)
- hash_size
 - CipherSpecs, [1259](#)
- hashAlgo
 - DcvArgs, [1263](#)
 - DskeArgs, [1277](#)
 - Suites, [1327](#)
- hashMd5
 - HS_Hashes, [1288](#)
- hashSha
 - HS_Hashes, [1288](#)
- hashSha256
 - HS_Hashes, [1288](#)
- hashSigAlgo
 - Suites, [1327](#)
- hashSigAlgoSz
 - Suites, [1327](#)
- Hashes, [1286](#)
 - md5, [1286](#)
 - sha, [1286](#)
 - sha256, [1286](#)
- haveDH
 - Options, [1302](#)
 - WOLFSSL_CTX, [1352](#)
- haveECC
 - Options, [1302](#)
 - WOLFSSL_CTX, [1353](#)
- haveECDSAsig
 - Options, [1302](#)
- WOLFSSL_CTX, [1353](#)
- haveEMS
 - Options, [1302](#)
 - WOLFSSL_CTX, [1353](#)
 - WOLFSSL_SESSION, [1369](#)
- haveNTRU
 - Options, [1302](#)
 - WOLFSSL_CTX, [1353](#)
- havePSK
 - Options, [1302](#)
 - WOLFSSL_CTX, [1353](#)
- havePeerCert
 - Options, [1302](#)
- havePeerVerify
 - Options, [1302](#)
- haveQSH
 - Options, [1302](#)
- haveRSA
 - Options, [1302](#)
 - WOLFSSL_CTX, [1353](#)
- haveSessionId
 - Options, [1302](#)
- haveStaticECC
 - Options, [1302](#)
 - WOLFSSL_CTX, [1353](#)
- hccrConfig
 - scg_clock_mode_config_t, [333](#)
- head
 - WOLF_EVENT_QUEUE, [1335](#)
- headerLen
 - enet_rx_enh_info_t, [450](#)
- headerSz
 - BuildMsgArgs, [1255](#)
- heap
 - Aes, [1248](#)
 - Arc4, [1249](#)
 - DecodedCert, [1267](#)
 - DerBuffer, [1272](#)
 - Des3, [1273](#)
 - DhKey, [1274](#)
 - DsaKey, [1276](#)
 - Hmac, [1287](#)
 - Md5, [1294](#)
 - RsaKey, [1317](#)
 - Sha, [1320](#)
 - Sha256, [1321](#)
 - SignatureCtx, [1322](#)
 - WC_RNG, [1333](#)
 - WOLFSSL, [1338](#)
 - WOLFSSL_ASN1_OBJECT, [1342](#)
 - WOLFSSL_BIO, [1345](#)
 - WOLFSSL_CERT_MANAGER, [1347](#)
 - WOLFSSL_CRL, [1350](#)
 - WOLFSSL_CTX, [1353](#)
 - WOLFSSL_X509, [1373](#)
- hiLen
 - Md4, [1293](#)
 - Md5, [1294](#)

- Sha, [1320](#)
- Sha256, [1321](#)
- highPriority
 - qspi_ahb_config_t, [1310](#)
- highSideCtrl
 - uja113x_mtpnv_cfg_t, [247](#)
- Hmac, [1287](#)
 - hash, [1287](#)
 - heap, [1287](#)
 - innerHash, [1287](#)
 - innerHashKeyed, [1287](#)
 - ipad, [1288](#)
 - macType, [1288](#)
 - opad, [1288](#)
- hmac
 - WOLFSSL, [1338](#)
 - WOLFSSL_HMAC_CTX, [1364](#)
- holder
 - WOLFSSL_MD5_CTX, [1365](#)
 - WOLFSSL_RIPEMD_CTX, [1367](#)
 - WOLFSSL_SHA256_CTX, [1370](#)
 - WOLFSSL_SHA_CTX, [1370](#)
- hour
 - rtc_timedate_t, [1001](#)
- hsDoneCb
 - WOLFSSL, [1338](#)
- hsDoneCtx
 - WOLFSSL, [1338](#)
- hsHashes
 - WOLFSSL, [1338](#)
- hsKey
 - WOLFSSL, [1338](#)
- hsType
 - WOLFSSL, [1338](#)
- hvioBank0Cfg
 - uja113x_init_cfg_t, [184](#)
- hvioBank1Cfg
 - uja113x_init_cfg_t, [184](#)
- hvioConfig
 - uja113x_hvio_bank_cfg_t, [182](#)
- hwAverage
 - adc_average_config_t, [257](#)
- hwAvgEnable
 - adc_average_config_t, [257](#)
- hwChannelId
 - ftm_combined_ch_param_t, [647](#)
 - ftm_independent_ch_param_t, [645](#)
 - ftm_input_ch_param_t, [622](#)
 - ftm_output_cmp_ch_param_t, [633](#)
 - ic_input_ch_param_t, [687](#)
 - oc_output_ch_param_t, [922](#)
- hwTriggerSupport
 - adc_group_config_t, [274](#)
- hysteresisLevel
 - cmp_comparator_t, [367](#)
- I2C_GetDefaultMasterConfig
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [699](#)
- I2C_GetDefaultSlaveConfig
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [699](#)
- I2C_MasterAbortTransfer
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [700](#)
- I2C_MasterDeinit
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [700](#)
- I2C_MasterGetBaudRate
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [700](#)
- I2C_MasterGetTransferStatus
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [700](#)
- I2C_MasterInit
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [701](#)
- I2C_MasterReceiveData
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [701](#)
- I2C_MasterReceiveDataBlocking
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [701](#)
- I2C_MasterSendData
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [702](#)
- I2C_MasterSendDataBlocking
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [702](#)
- I2C_MasterSetBaudRate
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [702](#)
- I2C_MasterSetSlaveAddress
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [703](#)
- I2C_PAL_FAST_MODE
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [699](#)
- I2C_PAL_FASTPLUS_MODE
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [699](#)
- I2C_PAL_HIGHSPEED_MODE
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [699](#)
- I2C_PAL_STANDARD_MODE
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [699](#)
- I2C_PAL_ULTRAFast_MODE
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [699](#)
- I2C_PAL_USING_DMA
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [699](#)
- I2C_PAL_USING_INTERRUPTS
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [699](#)
- I2C_SlaveAbortTransfer

- Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [703](#)
- I2C_SlaveDeinit
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [703](#)
- I2C_SlaveGetTransferStatus
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [703](#)
- I2C_SlaveInit
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [703](#)
- I2C_SlaveReceiveData
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [704](#)
- I2C_SlaveReceiveDataBlocking
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [704](#)
- I2C_SlaveSendData
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [704](#)
- I2C_SlaveSendDataBlocking
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [705](#)
- I2C_SlaveSetRxBuffer
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [705](#)
- I2C_SlaveSetTxBuffer
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [705](#)
- I2S - Peripheral Abstraction Layer (I2S PAL), [674](#)
 - I2S_Abort, [678](#)
 - I2S_Deinit, [679](#)
 - I2S_GetBaudRate, [679](#)
 - I2S_GetDefaultConfig, [679](#)
 - I2S_GetStatus, [679](#)
 - I2S_Init, [680](#)
 - I2S_MASTER, [678](#)
 - I2S_ReceiveData, [680](#)
 - I2S_ReceiveDataBlocking, [680](#)
 - I2S_SLAVE, [678](#)
 - I2S_SendData, [680](#)
 - I2S_SendDataBlocking, [681](#)
 - I2S_SetRxBuffer, [681](#)
 - I2S_SetTxBuffer, [681](#)
 - I2S_USING_DMA, [678](#)
 - I2S_USING_INTERRUPT, [678](#)
 - i2s_mode_t, [678](#)
 - i2s_transfer_type_t, [678](#)
- I2S_Abort
 - I2S - Peripheral Abstraction Layer (I2S PAL), [678](#)
- I2S_Deinit
 - I2S - Peripheral Abstraction Layer (I2S PAL), [679](#)
- I2S_GetBaudRate
 - I2S - Peripheral Abstraction Layer (I2S PAL), [679](#)
- I2S_GetDefaultConfig
 - I2S - Peripheral Abstraction Layer (I2S PAL), [679](#)
- I2S_GetStatus
 - I2S - Peripheral Abstraction Layer (I2S PAL), [679](#)
- I2S_Init
 - I2S - Peripheral Abstraction Layer (I2S PAL), [680](#)
- I2S_MASTER
 - I2S - Peripheral Abstraction Layer (I2S PAL), [678](#)
- I2S_ReceiveData
 - I2S - Peripheral Abstraction Layer (I2S PAL), [680](#)
- I2S_ReceiveDataBlocking
 - I2S - Peripheral Abstraction Layer (I2S PAL), [680](#)
- I2S_SLAVE
 - I2S - Peripheral Abstraction Layer (I2S PAL), [678](#)
- I2S_SendData
 - I2S - Peripheral Abstraction Layer (I2S PAL), [680](#)
- I2S_SendDataBlocking
 - I2S - Peripheral Abstraction Layer (I2S PAL), [681](#)
- I2S_SetRxBuffer
 - I2S - Peripheral Abstraction Layer (I2S PAL), [681](#)
- I2S_SetTxBuffer
 - I2S - Peripheral Abstraction Layer (I2S PAL), [681](#)
- I2S_USING_DMA
 - I2S - Peripheral Abstraction Layer (I2S PAL), [678](#)
- I2S_USING_INTERRUPT
 - I2S - Peripheral Abstraction Layer (I2S PAL), [678](#)
- i2c_instance_t, [1289](#)
 - instIdx, [1289](#)
 - instType, [1289](#)
- i2c_master_t, [696](#)
 - baudRate, [697](#)
 - callback, [697](#)
 - callbackParam, [697](#)
 - dmaChannel1, [697](#)
 - dmaChannel2, [697](#)
 - extension, [697](#)
 - is10bitAddr, [697](#)
 - operatingMode, [697](#)
 - slaveAddress, [697](#)
 - transferType, [697](#)
- i2c_operating_mode_t
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [699](#)
- i2c_pal_transfer_type_t
 - Inter Integrated Circuit - Peripheral Abstraction Layer(I2C PAL), [699](#)
- i2c_slave_t, [698](#)
 - callback, [698](#)
 - callbackParam, [698](#)
 - dmaChannel, [698](#)
 - is10bitAddr, [698](#)
 - operatingMode, [698](#)
 - slaveAddress, [698](#)
 - slaveListening, [698](#)
 - transferType, [698](#)
- i2s_instance_t, [1289](#)
 - instIdx, [1290](#)
 - instType, [1290](#)
- i2s_mode_t
 - I2S - Peripheral Abstraction Layer (I2S PAL), [678](#)
- i2s_transfer_type_t
 - I2S - Peripheral Abstraction Layer (I2S PAL), [678](#)

- i2s_user_config_t, [676](#)
 - baudRate, [676](#)
 - callback, [676](#)
 - callbackParam, [677](#)
 - extension, [677](#)
 - mode, [677](#)
 - rxDMACChannel, [677](#)
 - transferType, [677](#)
 - txDMACChannel, [677](#)
 - wordWidth, [677](#)
- IC_DISABLE_OPERATION
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [689](#)
- IC_Deinit
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [689](#)
- IC_DisableNotification
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [690](#)
- IC_EnableNotification
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [690](#)
- IC_GetMeasurement
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [690](#)
- IC_Init
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [690](#)
- IC_MEASURE_FALLING_EDGE_PERIOD
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [689](#)
- IC_MEASURE_PULSE_HIGH
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [689](#)
- IC_MEASURE_PULSE_LOW
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [689](#)
- IC_MEASURE_RISING_EDGE_PERIOD
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [689](#)
- IC_SetChannelMode
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [691](#)
- IC_StartChannel
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [691](#)
- IC_StopChannel
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [691](#)
- IC_TIMESTAMP_BOTH_EDGES
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [689](#)
- IC_TIMESTAMP_FALLING_EDGE
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [689](#)
- IC_TIMESTAMP_RISING_EDGE
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [689](#)
- ID0_ADDRESS
 - Register address map, [1028](#)
- ID1_ADDRESS
 - Register address map, [1028](#)
- ID2_ADDRESS
 - Register address map, [1028](#)
- ID3_ADDRESS
 - Register address map, [1029](#)
- ID_1_ADDR
 - Generic PHY, [665](#)
- ID_2_ADDR
 - Generic PHY, [665](#)
- IDM0_ADDRESS
 - Register address map, [1029](#)
- IDM1_ADDRESS
 - Register address map, [1029](#)
- IDM2_ADDRESS
 - Register address map, [1029](#)
- IDM3_ADDRESS
 - Register address map, [1029](#)
- INT_SYS_DisableIRQ
 - Interrupt Manager (Interrupt), [710](#)
- INT_SYS_DisableIRQGlobal
 - Interrupt Manager (Interrupt), [710](#)
- INT_SYS_EnableIRQ
 - Interrupt Manager (Interrupt), [711](#)
- INT_SYS_EnableIRQGlobal
 - Interrupt Manager (Interrupt), [711](#)
- INT_SYS_GetPriority
 - Interrupt Manager (Interrupt), [711](#)
- INT_SYS_InstallHandler
 - Interrupt Manager (Interrupt), [711](#)
- INT_SYS_SetPriority
 - Interrupt Manager (Interrupt), [711](#)
- IO15FEIE_DISABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [287](#)
- IO15FEIE_ENABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [287](#)
- IO15OLIE_DISABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [284](#)
- IO15OLIE_ENABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [284](#)
- IO15REIE_DISABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [287](#)
- IO15REIE_ENABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [287](#)
- IO15SCIE_DISABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [284](#)
- IO15SCIE_ENABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [284](#)

- IO26FEIE_DISABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [287](#)
- IO26FEIE_ENABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [287](#)
- IO26OLIE_DISABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [284](#)
- IO26OLIE_ENABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [284](#)
- IO26REIE_DISABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [287](#)
- IO26REIE_ENABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [288](#)
- IO26SCIE_DISABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [284](#)
- IO26SCIE_ENABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [285](#)
- IO2SFC_LIMP_HOME
 - Start-up control configuration options (0x73), [1118](#)
- IO2SFC_STD_IO
 - Start-up control configuration options (0x73), [1118](#)
- IO37FEIE_DISABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [288](#)
- IO37FEIE_ENABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [288](#)
- IO37OLIE_DISABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [285](#)
- IO37OLIE_ENABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [285](#)
- IO37REIE_DISABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [288](#)
- IO37REIE_ENABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [288](#)
- IO37SCIE_DISABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [285](#)
- IO37SCIE_ENABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [285](#)
- IO3SFC_LIMP_HOME
 - Start-up control configuration options (0x73), [1118](#)
- IO3SFC_STD_IO
 - Start-up control configuration options (0x73), [1118](#)
- IO48FEIE_DISABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [288](#)
- IO48FEIE_ENABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [288](#)
- IO48OLIE_DISABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [285](#)
- IO48OLIE_ENABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [285](#)
- IO48REIE_DISABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [288](#)
- IO48REIE_ENABLE
 - Bank N wake-up interrupt enable configuration options (0x37/0x47), [288](#)
- IO48SCIE_DISABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [285](#)
- IO48SCIE_ENABLE
 - Bank N fail interrupt enable configuration options (0x38/0x48), [285](#)
- IO4SFC_LIMP_HOME
 - Start-up control configuration options (0x73), [1118](#)
- IO4SFC_STD_IO
 - Start-up control configuration options (0x73), [1118](#)
- IOCB_ReadCtx
 - WOLFSSL, [1338](#)
- IOCB_WriteCtx
 - WOLFSSL, [1338](#)
- IONAC_DEACTIVATED
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONAC_ENABLED
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONAC_HVIO
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONAC_HVIO_INV
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONAC_TMR_1
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONAC_TMR_2
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONAC_TMR_3
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONAC_TMR_4
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONCC_HS
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONCC_HS_SLOPE
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONCC_HS_WUP
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONCC_HS_WUP_SLOPE
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONCC_LS
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONCC_LS_SLOPE
 - 04. HVIO bank 0 & 1 control, [229](#)

- IONCC_OFF
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONCC_WUP
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONOLTC_10_MA
 - 02. Battery monitor configuration, [207](#)
- IONOLTC_20_MA
 - 02. Battery monitor configuration, [207](#)
- IONOLTC_2_MA
 - 02. Battery monitor configuration, [206](#)
- IONOLTC_5_MA
 - 02. Battery monitor configuration, [206](#)
- IONSC_FULLL
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONSC_NONE
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONSC_OVERVOLTAGE
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONSC_UNDRVOLTAGE
 - 04. HVIO bank 0 & 1 control, [229](#)
- IONSCTC_30_MA
 - 02. Battery monitor configuration, [207](#)
- IONSCTC_45_MA
 - 02. Battery monitor configuration, [207](#)
- IONSCTC_60_MA
 - 02. Battery monitor configuration, [207](#)
- IONSCTC_90_MA
 - 02. Battery monitor configuration, [207](#)
- IRQ_ENABLE_ADDR
 - TJA110x PHY, [1143](#)
- IRQ_LINKDOWN_FLAG
 - TJA110x PHY, [1143](#)
- IRQ_LINKUP_FLAG
 - TJA110x PHY, [1143](#)
- IRQ_LPS_RECEIVED_FLAG
 - TJA110x PHY, [1143](#)
- IRQ_PWON_FLAG
 - TJA110x PHY, [1143](#)
- IRQ_STATUS_ADDR
 - TJA110x PHY, [1143](#)
- IRQ_WAKEUP_FLAG
 - TJA110x PHY, [1143](#)
- ic_config_t, [687](#)
 - extension, [688](#)
 - inputChConfig, [688](#)
 - nNumChannels, [688](#)
- ic_input_ch_param_t, [687](#)
 - channelCallbackParams, [687](#)
 - channelCallbacks, [687](#)
 - channelExtension, [687](#)
 - filterEn, [687](#)
 - filterValue, [687](#)
 - hwChannelId, [687](#)
 - inputCaptureMode, [687](#)
- ic_instance_t, [1290](#)
 - instIdx, [1290](#)
 - instType, [1290](#)
- ic_option_mode_t
 - Input Capture - Peripheral Abstraction Layer (I↔C PAL), [689](#)
- ic_pal_state_t, [689](#)
- iccaLim
 - fs45_vreg_reg_t, [1052](#)
- id
 - can_message_t, [388](#)
 - flexcan_id_table_t, [515](#)
 - uja113x_cpnc_cfg_t, [191](#)
- idFilterTable
 - extension_flexcan_rx_fifo_t, [390](#)
- idFormat
 - extension_flexcan_rx_fifo_t, [390](#)
- idLen
 - WOLFSSL_SESSION, [1369](#)
- idMask
 - uja113x_cpnc_cfg_t, [191](#)
- idType
 - can_buff_config_t, [388](#)
- ide
 - sbc_frame_t, [1180](#)
 - uja113x_cpnc_cfg_t, [191](#)
- identif
 - sbc_can_conf_t, [1181](#)
- idle_timeout_cnt
 - lin_protocol_state_t, [842](#)
- idx
 - bufferStatic, [1254](#)
 - BuildMsgArgs, [1255](#)
 - DckeArgs, [1263](#)
 - DcvArgs, [1264](#)
 - DskeArgs, [1277](#)
 - ProcPeerCertArgs, [1308](#)
 - ScvArgs, [1319](#)
 - SskeArgs, [1326](#)
- inOutMappingConfig
 - trgmux_user_config_t, [1149](#)
- inSet
 - WOLFSSL_DH, [1355](#)
 - WOLFSSL_DSA, [1356](#)
 - WOLFSSL_EC_KEY, [1359](#)
 - WOLFSSL_EC_POINT, [1360](#)
 - WOLFSSL_RSA, [1368](#)
- index
 - csec_state_t, [300](#)
- inh0
 - fs45_inh_int_reg_t, [1056](#)
- inh2
 - fs45_inh_int_reg_t, [1056](#)
- inh3
 - fs45_inh_int_reg_t, [1056](#)
- inh4
 - fs45_inh_int_reg_t, [1056](#)
- inh5
 - fs45_inh_int_reg_t, [1056](#)
- inhAll
 - fs45_int_reg_t, [1055](#)
- inhCan

- fs45_int_reg_t, [1055](#)
- inhIntReg
 - fs45_drv_config_t, [1062](#)
- inhLin
 - fs45_int_reg_t, [1055](#)
- inhVcore
 - fs45_int_reg_t, [1055](#)
- inhVother
 - fs45_int_reg_t, [1055](#)
- inhVpre
 - fs45_int_reg_t, [1055](#)
- inhVsns
 - fs45_int_reg_t, [1055](#)
- init
 - crc_spec_t, [247](#)
 - Generic PHY, [666](#)
 - phy_driver_t, [949](#)
 - TJA110x PHY, [1145](#)
- initCounterSync
 - ftm_pwm_sync_t, [589](#)
- initValue
 - pin_settings_config_t, [959](#)
- initial_NAD
 - lin_node_attribute_t, [830](#)
- initialVal
 - ftm_quad_decode_config_t, [656](#)
- initialValue
 - ftm_timer_param_t, [628](#)
- Initialization, [682](#)
 - ld_init, [682](#)
- initialize
 - pmc_lpo_clock_config_t, [336](#)
 - scg_clock_mode_config_t, [333](#)
 - scg_clockout_config_t, [333](#)
 - scg_firc_config_t, [331](#)
 - scg_rtc_config_t, [332](#)
 - scg_sirc_config_t, [330](#)
 - scg_sosc_config_t, [329](#)
 - scg_spill_config_t, [332](#)
 - sim_clock_out_config_t, [323](#)
 - sim_lpo_clock_config_t, [324](#)
 - sim_plat_gate_config_t, [325](#)
 - sim_tclk_config_t, [324](#)
 - sim_trace_clock_config_t, [326](#)
- inner_length
 - __blake2b_param, [1243](#)
 - __blake2s_param, [1245](#)
- innerHash
 - Hmac, [1287](#)
- innerHashKeyed
 - Hmac, [1287](#)
- input
 - SckeArgs, [1318](#)
 - ScvArgs, [1319](#)
- Input Capture - Peripheral Abstraction Layer (IC PAL), [683](#)
 - IC_DISABLE_OPERATION, [689](#)
 - IC_Deinit, [689](#)
 - IC_DisableNotification, [690](#)
 - IC_EnableNotification, [690](#)
 - IC_GetMeasurement, [690](#)
 - IC_Init, [690](#)
 - IC_MEASURE_FALLING_EDGE_PERIOD, [689](#)
 - IC_MEASURE_PULSE_HIGH, [689](#)
 - IC_MEASURE_PULSE_LOW, [689](#)
 - IC_MEASURE_RISING_EDGE_PERIOD, [689](#)
 - IC_SetChannelMode, [691](#)
 - IC_StartChannel, [691](#)
 - IC_StopChannel, [691](#)
 - IC_TIMESTAMP_BOTH_EDGES, [689](#)
 - IC_TIMESTAMP_FALLING_EDGE, [689](#)
 - IC_TIMESTAMP_RISING_EDGE, [689](#)
 - ic_option_mode_t, [689](#)
- inputBuff
 - csec_state_t, [300](#)
- inputBuffer
 - Buffers, [1252](#)
- inputCaptureMode
 - ic_input_ch_param_t, [687](#)
- inputChConfig
 - ftm_input_param_t, [622](#)
 - ic_config_t, [688](#)
- inputChannelArray
 - adc_group_config_t, [274](#)
- inputClock
 - adc_converter_config_t, [256](#)
 - extension_adc_s32k1xx_t, [275](#)
- inputMode
 - ftm_input_ch_param_t, [622](#)
- inputSz
 - SckeArgs, [1318](#)
 - ScvArgs, [1319](#)
- insertDeadtime
 - pwm_channel_t, [989](#)
- instIdx
 - adc_instance_t, [1247](#)
 - can_instance_t, [1256](#)
 - i2c_instance_t, [1289](#)
 - i2s_instance_t, [1290](#)
 - ic_instance_t, [1290](#)
 - mpu_instance_t, [1295](#)
 - oc_instance_t, [1298](#)
 - pwm_instance_t, [1309](#)
 - spi_instance_t, [1326](#)
 - timing_instance_t, [1331](#)
 - uart_instance_t, [1331](#)
 - wdg_instance_t, [1334](#)
- instType
 - adc_instance_t, [1247](#)
 - can_instance_t, [1256](#)
 - i2c_instance_t, [1289](#)
 - i2s_instance_t, [1290](#)
 - ic_instance_t, [1290](#)
 - mpu_instance_t, [1295](#)
 - oc_instance_t, [1298](#)
 - pwm_instance_t, [1309](#)

- spi_instance_t, [1326](#)
- timing_instance_t, [1331](#)
- uart_instance_t, [1331](#)
- wdg_instance_t, [1334](#)
- intEnable
 - pdb_timer_config_t, [933](#)
 - wdg_config_t, [1225](#)
 - wdog_user_config_t, [1233](#)
- intReg
 - fs45_drv_config_t, [1062](#)
- Inter Integrated Circuit - Peripheral Abstraction Layer(↔ I2C PAL), [692](#)
 - I2C_GetDefaultMasterConfig, [699](#)
 - I2C_GetDefaultSlaveConfig, [699](#)
 - I2C_MasterAbortTransfer, [700](#)
 - I2C_MasterDeinit, [700](#)
 - I2C_MasterGetBaudRate, [700](#)
 - I2C_MasterGetTransferStatus, [700](#)
 - I2C_MasterInit, [701](#)
 - I2C_MasterReceiveData, [701](#)
 - I2C_MasterReceiveDataBlocking, [701](#)
 - I2C_MasterSendData, [702](#)
 - I2C_MasterSendDataBlocking, [702](#)
 - I2C_MasterSetBaudRate, [702](#)
 - I2C_MasterSetSlaveAddress, [703](#)
 - I2C_PAL_FAST_MODE, [699](#)
 - I2C_PAL_FASTPLUS_MODE, [699](#)
 - I2C_PAL_HIGHSPEED_MODE, [699](#)
 - I2C_PAL_STANDARD_MODE, [699](#)
 - I2C_PAL_ULTRAFAST_MODE, [699](#)
 - I2C_PAL_USING_DMA, [699](#)
 - I2C_PAL_USING_INTERRUPTS, [699](#)
 - I2C_SlaveAbortTransfer, [703](#)
 - I2C_SlaveDeinit, [703](#)
 - I2C_SlaveGetTransferStatus, [703](#)
 - I2C_SlaveInit, [703](#)
 - I2C_SlaveReceiveData, [704](#)
 - I2C_SlaveReceiveDataBlocking, [704](#)
 - I2C_SlaveSendData, [704](#)
 - I2C_SlaveSendDataBlocking, [705](#)
 - I2C_SlaveSetRxBuffer, [705](#)
 - I2C_SlaveSetTxBuffer, [705](#)
 - i2c_operating_mode_t, [699](#)
 - i2c_pal_transfer_type_t, [699](#)
- Interface management, [707](#)
 - l_ifc_goto_sleep, [707](#)
 - l_ifc_init, [707](#)
 - l_ifc_read_status, [708](#)
 - l_ifc_wake_up, [708](#)
- interleave_timeout_counter
 - lin_tl_descriptor_t, [836](#)
- internal
 - WOLFSSL_BIGNUM, [1344](#)
 - WOLFSSL_DH, [1355](#)
 - WOLFSSL_DSA, [1356](#)
 - WOLFSSL_EC_KEY, [1359](#)
 - WOLFSSL_EC_POINT, [1360](#)
 - WOLFSSL_RSA, [1368](#)
- Interrupt Manager (Interrupt), [709](#)
 - DefaultISR, [710](#)
 - INT_SYS_DisableIRQ, [710](#)
 - INT_SYS_DisableIRQGlobal, [710](#)
 - INT_SYS_EnableIRQ, [711](#)
 - INT_SYS_EnableIRQGlobal, [711](#)
 - INT_SYS_GetPriority, [711](#)
 - INT_SYS_InstallHandler, [711](#)
 - INT_SYS_SetPriority, [711](#)
 - isr_t, [710](#)
- Interrupt vector numbers for S32K148, [714](#)
- interruptCfg
 - erm_user_config_t, [465](#)
- interruptEnable
 - adc_chan_config_t, [258](#)
 - edma_transfer_config_t, [420](#)
 - ewm_init_config_t, [470](#)
 - lptmr_config_t, [795](#)
- interrupts
 - enet_config_t, [448](#)
- inverterState
 - cmp_comparator_t, [367](#)
- inverterSync
 - ftm_pwm_sync_t, [589](#)
- io15OpenLoadThrCtrl
 - uja113x_boldt_cfg_t, [228](#)
- io15ShortCircuitThrCtrl
 - uja113x_bscdt_cfg_t, [227](#)
- io23Fs
 - fs45_fssm_reg_t, [1058](#)
- io26OpenLoadThrCtrl
 - uja113x_boldt_cfg_t, [228](#)
- io26ShortCircuitThrCtrl
 - uja113x_bscdt_cfg_t, [227](#)
- io2IdleValue
 - qspi_user_config_t, [1312](#)
- io37OpenLoadThrCtrl
 - uja113x_boldt_cfg_t, [228](#)
- io37ShortCircuitThrCtrl
 - uja113x_bscdt_cfg_t, [227](#)
- io3IdleValue
 - qspi_user_config_t, [1313](#)
- io45Fs
 - fs45_fssm_reg_t, [1058](#)
- io48OpenLoadThrCtrl
 - uja113x_boldt_cfg_t, [228](#)
- io48ShortCircuitThrCtrl
 - uja113x_bscdt_cfg_t, [227](#)
- ionActivateCtrl
 - uja113x_hvio_cfg_t, [227](#)
- ionConfCtrl
 - uja113x_hvio_cfg_t, [227](#)
- ionShutdownCtrl
 - uja113x_hvio_cfg_t, [227](#)
- ipad
 - Hmac, [1288](#)
- ipffDis
 - fs45_vreg_reg_t, [1052](#)

- ipv4Frag
 - enet_rx_enh_info_t, [450](#)
- ipv6
 - enet_rx_enh_info_t, [450](#)
- iqmp
 - WOLFSSL_RSA, [1368](#)
- is10bitAddr
 - i2c_master_t, [697](#)
 - i2c_slave_t, [698](#)
 - lpi2c_master_user_config_t, [746](#)
 - lpi2c_slave_user_config_t, [747](#)
- is_remote
 - flexcan_data_info_t, [515](#)
- is_rx_fifo_needed
 - flexcan_user_config_t, [517](#)
- isBlocking
 - flexcan_mb_handle_t, [513](#)
 - lpspi_state_t, [778](#)
- isBusBusy
 - lin_state_t, [727](#)
- isCA
 - DecodedCert, [1267](#)
- isCa
 - WOLFSSL_X509, [1373](#)
- isClosed
 - Options, [1303](#)
- isDynamic
 - WOLFSSL_SESSION, [1369](#)
- isExtendedFrame
 - flexcan_id_table_t, [515](#)
- isInit
 - drv_config_t, [1276](#)
- isInterruptEnabled
 - lpit_user_channel_config_t, [763](#)
- isPcsContinuous
 - lpspi_master_config_t, [776](#)
 - lpspi_state_t, [778](#)
- isRemote
 - can_buff_config_t, [388](#)
 - flexcan_mb_handle_t, [513](#)
- isRemoteFrame
 - flexcan_id_table_t, [515](#)
- isRxBlocking
 - lin_state_t, [727](#)
 - lpuart_state_t, [805](#)
- isRxBusy
 - lin_state_t, [727](#)
 - lpuart_state_t, [805](#)
- isSecured
 - fs45_tx_data_t, [1283](#)
- isToflsrEnabled
 - ftm_user_config_t, [591](#)
- isTransferInProgress
 - lpspi_state_t, [778](#)
- isTxBlocking
 - lin_state_t, [728](#)
 - lpuart_state_t, [805](#)
- isTxBusy
 - lin_state_t, [728](#)
 - lpuart_state_t, [805](#)
- isr_t
 - Interrupt Manager (Interrupt), [710](#)
- issuer
 - DecodedCert, [1267](#)
 - WOLFSSL_X509, [1373](#)
- issuerHash
 - CRL_Entry, [1261](#)
 - DecodedCert, [1267](#)
 - OcspEntry, [1299](#)
- issuerKeyHash
 - OcspEntry, [1299](#)
- iv
 - BuildMsgArgs, [1255](#)
 - csec_state_t, [300](#)
 - EncryptedInfo, [1281](#)
 - HC128, [1286](#)
 - WOLFSSL_EVP_CIPHER_CTX, [1362](#)
- iv_size
 - CipherSpecs, [1259](#)
- ivSz
 - BuildMsgArgs, [1255](#)
 - EncryptedInfo, [1281](#)
- J2602 Specific API, [715](#)
- J2602 Transport Layer specific API, [716](#)
- kea
 - CipherSpecs, [1259](#)
- keepCert
 - WOLFSSL, [1338](#)
- keepResources
 - Options, [1303](#)
- key
 - Aes, [1248](#)
 - Buffers, [1252](#)
 - Des, [1273](#)
 - Des3, [1273](#)
 - HC128, [1287](#)
 - SignatureCtx, [1322](#)
- key_length
 - __blake2b_param, [1243](#)
 - __blake2s_param, [1245](#)
- key_size
 - CipherSpecs, [1259](#)
- keyId
 - csec_state_t, [300](#)
- keyLen
 - WOLFSSL_EVP_CIPHER_CTX, [1362](#)
- keyOID
 - DecodedCert, [1267](#)
 - SignatureCtx, [1322](#)
 - Signer, [1323](#)
- keySz
 - Buffers, [1252](#)
- keyType
 - Buffers, [1252](#)
- keyUsage

- Signer, [1323](#)
- keylen
 - Aes, [1248](#)
- Keys, [1290](#)
 - client_write_IV, [1291](#)
 - client_write_MAC_secret, [1291](#)
 - client_write_key, [1291](#)
 - decryptedCur, [1291](#)
 - encryptSz, [1291](#)
 - encryptionOn, [1291](#)
 - padSz, [1291](#)
 - peer_sequence_number_hi, [1291](#)
 - peer_sequence_number_lo, [1291](#)
 - sequence_number_hi, [1291](#)
 - sequence_number_lo, [1292](#)
 - server_write_IV, [1292](#)
 - server_write_MAC_secret, [1292](#)
 - server_write_key, [1292](#)
- keys
 - WOLFSSL, [1338](#)
- L1WIE_DISABLE
 - Transceiver interrupt enable configuration options (0x23), [1166](#)
- L1WIE_ENABLE
 - Transceiver interrupt enable configuration options (0x23), [1166](#)
- L2WIE_DISABLE
 - Transceiver interrupt enable configuration options (0x23), [1166](#)
- L2WIE_ENABLE
 - Transceiver interrupt enable configuration options (0x23), [1166](#)
- l_diagnostic_mode_t
 - Low level API, [846](#)
- l_ifc_goto_sleep
 - Interface management, [707](#)
- l_ifc_init
 - Interface management, [707](#)
- l_ifc_read_status
 - Interface management, [708](#)
- l_ifc_wake_up
 - Interface management, [708](#)
- l_sch_set
 - Schedule management, [1079](#)
- l_sch_tick
 - Schedule management, [1079](#)
- l_sys_init
 - Driver and cluster management, [409](#)
- l_sys_irq_disable
 - User provided call-outs, [1222](#)
- l_sys_irq_restore
 - User provided call-outs, [1222](#)
- LCKC_ADDRESS
 - Register address map, [1029](#)
- LD_ANY_FUNCTION
 - Common Transport Layer API, [358](#)
- LD_ANY_MESSAGE
 - Common Transport Layer API, [358](#)
- LD_ANY_SUPPLIER
 - Common Transport Layer API, [358](#)
- LD_BROADCAST
 - Common Transport Layer API, [358](#)
- LD_CHECK_N_AS_TIMEOUT
 - Low level API, [848](#)
- LD_CHECK_N_CR_TIMEOUT
 - Low level API, [848](#)
- LD_COMPLETED
 - Low level API, [848](#)
- LD_DATA_AVAILABLE
 - Low level API, [846](#)
- LD_DATA_ERROR
 - Common Transport Layer API, [358](#)
- LD_DIAG_IDLE
 - Low level API, [847](#)
- LD_DIAG_RX_FUNCTIONAL
 - Low level API, [847](#)
- LD_DIAG_RX_INTERLEAVED
 - Low level API, [847](#)
- LD_DIAG_RX_PHY
 - Low level API, [847](#)
- LD_DIAG_TX_FUNCTIONAL
 - Low level API, [847](#)
- LD_DIAG_TX_INTERLEAVED
 - Low level API, [847](#)
- LD_DIAG_TX_PHY
 - Low level API, [847](#)
- LD_FAILED
 - Low level API, [848](#)
- LD_FUNCTIONAL_NAD
 - Common Transport Layer API, [358](#)
- LD_IN_PROGRESS
 - Low level API, [848](#)
- LD_LENGTH_NOT_CORRECT
 - Common Transport Layer API, [358](#)
- LD_LENGTH_TOO_SHORT
 - Common Transport Layer API, [358](#)
- LD_N_AS_TIMEOUT
 - Low level API, [848](#)
- LD_N_CR_TIMEOUT
 - Low level API, [848](#)
- LD_NEGATIVE
 - Low level API, [847](#)
- LD_NEGATIVE_RESPONSE
 - Low level API, [843](#)
- LD_NO_CHECK_TIMEOUT
 - Low level API, [848](#)
- LD_NO_DATA
 - Low level API, [846](#)
- LD_NO_MSG
 - Low level API, [848](#)
- LD_NO_RESPONSE
 - Low level API, [847](#)
- LD_OVERWRITTEN
 - Low level API, [847](#)
- LD_POSITIVE_RESPONSE
 - Low level API, [843](#)

- LD_QUEUE_AVAILABLE
 - Low level API, [846](#)
- LD_QUEUE_EMPTY
 - Low level API, [846](#)
- LD_QUEUE_FULL
 - Low level API, [846](#)
- LD_READ_OK
 - Common Transport Layer API, [358](#)
- LD_RECEIVE_ERROR
 - Low level API, [846](#)
- LD_REQUEST_FINISHED
 - Low level API, [849](#)
- LD_SERVICE_BUSY
 - Low level API, [849](#)
- LD_SERVICE_ERROR
 - Low level API, [849](#)
- LD_SERVICE_IDLE
 - Low level API, [849](#)
- LD_SET_OK
 - Common Transport Layer API, [358](#)
- LD_SUCCESS
 - Low level API, [847](#)
- LD_TRANSFER_ERROR
 - Low level API, [846](#)
- LD_TRANSMIT_ERROR
 - Low level API, [846](#)
- LD_WRONG_SN
 - Low level API, [848](#)
- LIN 2.1 Specific API, [717](#)
 - lin_collision_resolve, [717](#)
 - lin_make_res_evnt_frame, [717](#)
 - lin_update_err_signal, [718](#)
 - lin_update_rx_evnt_frame, [718](#)
 - lin_update_word_status_lin21, [718](#)
- LIN Core API, [719](#)
- LIN Driver, [720](#)
 - CHECK_PARITY, [729](#)
 - g_linLpuartIsrs, [738](#)
 - LIN_BAUDRATE_ADJUSTED, [729](#)
 - LIN_CHECKSUM_ERROR, [729](#)
 - LIN_DRV_AbortTransferData, [730](#)
 - LIN_DRV_AutoBaudCapture, [730](#)
 - LIN_DRV_Deinit, [731](#)
 - LIN_DRV_DisableIRQ, [731](#)
 - LIN_DRV_EnableIRQ, [731](#)
 - LIN_DRV_GetCurrentNodeState, [731](#)
 - LIN_DRV_GetDefaultConfig, [732](#)
 - LIN_DRV_GetReceiveStatus, [732](#)
 - LIN_DRV_GetTransmitStatus, [732](#)
 - LIN_DRV_GoToSleepMode, [733](#)
 - LIN_DRV_GotoldState, [733](#)
 - LIN_DRV_IRQHandler, [734](#)
 - LIN_DRV_Init, [733](#)
 - LIN_DRV_InstallCallback, [733](#)
 - LIN_DRV_MakeChecksumByte, [734](#)
 - LIN_DRV_MasterSendHeader, [734](#)
 - LIN_DRV_ProcessParity, [735](#)
 - LIN_DRV_ReceiveFrameData, [735](#)
 - LIN_DRV_ReceiveFrameDataBlocking, [736](#)
 - LIN_DRV_SendFrameData, [736](#)
 - LIN_DRV_SendFrameDataBlocking, [737](#)
 - LIN_DRV_SendWakeupSignal, [737](#)
 - LIN_DRV_SetTimeoutCounter, [738](#)
 - LIN_DRV_TimeoutService, [738](#)
 - LIN_FRAME_ERROR, [729](#)
 - LIN_NO_EVENT, [729](#)
 - LIN_NODE_STATE_IDLE, [730](#)
 - LIN_NODE_STATE_RECV_DATA, [730](#)
 - LIN_NODE_STATE_RECV_DATA_COMPLETED, [730](#)
 - LIN_NODE_STATE_RECV_PID, [730](#)
 - LIN_NODE_STATE_RECV_SYNC, [730](#)
 - LIN_NODE_STATE_SEND_BREAK_FIELD, [730](#)
 - LIN_NODE_STATE_SEND_DATA, [730](#)
 - LIN_NODE_STATE_SEND_DATA_COMPLETED, [730](#)
 - LIN_NODE_STATE_SEND_PID, [730](#)
 - LIN_NODE_STATE_SLEEP_MODE, [730](#)
 - LIN_NODE_STATE_UNINIT, [730](#)
 - LIN_PID_ERROR, [729](#)
 - LIN_PID_OK, [729](#)
 - LIN_READBACK_ERROR, [729](#)
 - LIN_RECV_BREAK_FIELD_OK, [729](#)
 - LIN_RX_COMPLETED, [730](#)
 - LIN_RX_OVERRUN, [730](#)
 - LIN_SYNC_ERROR, [729](#)
 - LIN_SYNC_OK, [729](#)
 - LIN_TX_COMPLETED, [729](#)
 - LIN_WAKEUP_SIGNAL, [729](#)
 - lin_callback_t, [729](#)
 - lin_event_id_t, [729](#)
 - lin_node_state_t, [730](#)
 - lin_timer_get_time_interval_t, [729](#)
 - MAKE_PARITY, [729](#)
 - MASTER, [729](#)
 - SLAVE, [729](#)
- LIN Stack, [739](#)
- LIN_BAUDRATE_ADJUSTED
 - LIN Driver, [729](#)
- LIN_CHECKSUM_ERROR
 - LIN Driver, [729](#)
- LIN_DIAGNOSTIC_CLASS_I
 - Low level API, [846](#)
- LIN_DIAGNOSTIC_CLASS_II
 - Low level API, [846](#)
- LIN_DIAGNOSTIC_CLASS_III
 - Low level API, [846](#)
- LIN_DRV_AbortTransferData
 - LIN Driver, [730](#)
- LIN_DRV_AutoBaudCapture
 - LIN Driver, [730](#)
- LIN_DRV_Deinit
 - LIN Driver, [731](#)
- LIN_DRV_DisableIRQ
 - LIN Driver, [731](#)
- LIN_DRV_EnableIRQ

- LIN Driver, [731](#)
- LIN_DRV_GetCurrentNodeState
 - LIN Driver, [731](#)
- LIN_DRV_GetDefaultConfig
 - LIN Driver, [732](#)
- LIN_DRV_GetReceiveStatus
 - LIN Driver, [732](#)
- LIN_DRV_GetTransmitStatus
 - LIN Driver, [732](#)
- LIN_DRV_GoToSleepMode
 - LIN Driver, [733](#)
- LIN_DRV_GotIdleState
 - LIN Driver, [733](#)
- LIN_DRV_IRQHandler
 - LIN Driver, [734](#)
- LIN_DRV_Init
 - LIN Driver, [733](#)
- LIN_DRV_InstallCallback
 - LIN Driver, [733](#)
- LIN_DRV_MakeChecksumByte
 - LIN Driver, [734](#)
- LIN_DRV_MasterSendHeader
 - LIN Driver, [734](#)
- LIN_DRV_ProcessParity
 - LIN Driver, [735](#)
- LIN_DRV_ReceiveFrameData
 - LIN Driver, [735](#)
- LIN_DRV_ReceiveFrameDataBlocking
 - LIN Driver, [736](#)
- LIN_DRV_SendFrameData
 - LIN Driver, [736](#)
- LIN_DRV_SendFrameDataBlocking
 - LIN Driver, [737](#)
- LIN_DRV_SendWakeupSignal
 - LIN Driver, [737](#)
- LIN_DRV_SetTimeoutCounter
 - LIN Driver, [738](#)
- LIN_DRV_TimeoutService
 - LIN Driver, [738](#)
- LIN_FRAME_ERROR
 - LIN Driver, [729](#)
- LIN_FRM_DIAG
 - Low level API, [847](#)
- LIN_FRM_EVNT
 - Low level API, [847](#)
- LIN_FRM_SPRDC
 - Low level API, [847](#)
- LIN_FRM_UNCD
 - Low level API, [847](#)
- LIN_LLD_BUS_ACTIVITY_TIMEOUT
 - Low level API, [848](#)
- LIN_LLD_CHECKSUM_ERR
 - Low level API, [848](#)
- LIN_LLD_ERROR
 - Low level API, [843](#)
- LIN_LLD_FRAME_ERR
 - Low level API, [848](#)
- LIN_LLD_NODATA_TIMEOUT
 - Low level API, [848](#)
- Low level API, [848](#)
- LIN_LLD_OK
 - Low level API, [843](#)
- LIN_LLD_PID_ERR
 - Low level API, [848](#)
- LIN_LLD_PID_OK
 - Low level API, [848](#)
- LIN_LLD_READBACK_ERR
 - Low level API, [848](#)
- LIN_LLD_RX_COMPLETED
 - Low level API, [848](#)
- LIN_LLD_TX_COMPLETED
 - Low level API, [848](#)
- LIN_MASTER
 - Low level API, [843](#)
- LIN_NO_EVENT
 - LIN Driver, [729](#)
- LIN_NODE_STATE_IDLE
 - LIN Driver, [730](#)
- LIN_NODE_STATE_RECV_DATA
 - LIN Driver, [730](#)
- LIN_NODE_STATE_RECV_DATA_COMPLETED
 - LIN Driver, [730](#)
- LIN_NODE_STATE_RECV_PID
 - LIN Driver, [730](#)
- LIN_NODE_STATE_RECV_SYNC
 - LIN Driver, [730](#)
- LIN_NODE_STATE_SEND_BREAK_FIELD
 - LIN Driver, [730](#)
- LIN_NODE_STATE_SEND_DATA
 - LIN Driver, [730](#)
- LIN_NODE_STATE_SEND_DATA_COMPLETED
 - LIN Driver, [730](#)
- LIN_NODE_STATE_SEND_PID
 - LIN Driver, [730](#)
- LIN_NODE_STATE_SLEEP_MODE
 - LIN Driver, [730](#)
- LIN_NODE_STATE_UNINIT
 - LIN Driver, [730](#)
- LIN_PID_ERROR
 - LIN Driver, [729](#)
- LIN_PID_OK
 - LIN Driver, [729](#)
- LIN_PRODUCT_ID
 - Common Transport Layer API, [358](#)
- LIN_PROTOCOL_13
 - Low level API, [848](#)
- LIN_PROTOCOL_20
 - Low level API, [848](#)
- LIN_PROTOCOL_21
 - Low level API, [848](#)
- LIN_PROTOCOL_J2602
 - Low level API, [848](#)
- LIN_READ_USR_DEF_MAX
 - Low level API, [843](#)
- LIN_READ_USR_DEF_MIN
 - Low level API, [843](#)
- LIN_READBACK_ERROR

- LIN Driver, [729](#)
- LIN_RECV_BREAK_FIELD_OK
 - LIN Driver, [729](#)
- LIN_RES_PUB
 - Low level API, [847](#)
- LIN_RES_SUB
 - Low level API, [847](#)
- LIN_RX_COMPLETED
 - LIN Driver, [730](#)
- LIN_RX_OVERRUN
 - LIN Driver, [730](#)
- LIN_SCH_TBL_COLL_RESOLV
 - Low level API, [849](#)
- LIN_SCH_TBL_DIAG
 - Low level API, [849](#)
- LIN_SCH_TBL_GO_TO_SLEEP
 - Low level API, [849](#)
- LIN_SCH_TBL_NORM
 - Low level API, [849](#)
- LIN_SCH_TBL_NULL
 - Low level API, [849](#)
- LIN_SERIAL_NUMBER
 - Common Transport Layer API, [359](#)
- LIN_SLAVE
 - Low level API, [844](#)
- LIN_SYNC_ERROR
 - LIN Driver, [729](#)
- LIN_SYNC_OK
 - LIN Driver, [729](#)
- LIN_TL_CALLBACK_HANDLER
 - Low level API, [844](#)
- LIN_TX_COMPLETED
 - LIN Driver, [729](#)
- LIN_WAKEUP_SIGNAL
 - LIN Driver, [729](#)
- LINC_ADDRESS
 - Register address map, [1029](#)
- lIdx
 - DecodedName, [1270](#)
- LK0C
 - UJA116xA SBC Driver, [1195](#)
- LK1C
 - UJA116xA SBC Driver, [1195](#)
- LK2C
 - UJA116xA SBC Driver, [1195](#)
- LK3C
 - UJA116xA SBC Driver, [1195](#)
- LK4C
 - UJA116xA SBC Driver, [1195](#)
- LK5C
 - UJA116xA SBC Driver, [1195](#)
- LK6C
 - UJA116xA SBC Driver, [1195](#)
- LKAC
 - UJA116xA SBC Driver, [1195](#)
- lLen
 - DecodedName, [1271](#)
- LMC1_TRANSCEIVER_LISTEN
 - 02. LIN configuration, [209](#)
- LMC1_TRANSCEIVER_OFF
 - 02. LIN configuration, [209](#)
- LMC1_TRANSCEIVER_ON
 - 02. LIN configuration, [209](#)
- LMC1_TRANSCEIVER_ON2
 - 02. LIN configuration, [209](#)
- LMC2_TRANSCEIVER_LISTEN
 - 02. LIN configuration, [210](#)
- LMC2_TRANSCEIVER_OFF
 - 02. LIN configuration, [210](#)
- LMC2_TRANSCEIVER_ON
 - 02. LIN configuration, [210](#)
- LMC2_TRANSCEIVER_ON2
 - 02. LIN configuration, [210](#)
- LPI2C Driver, [742](#)
 - LPI2C_DRV_MasterAbortTransferData, [748](#)
 - LPI2C_DRV_MasterDeinit, [749](#)
 - LPI2C_DRV_MasterGetBaudRate, [749](#)
 - LPI2C_DRV_MasterGetDefaultConfig, [749](#)
 - LPI2C_DRV_MasterGetTransferStatus, [749](#)
 - LPI2C_DRV_MasterIRQHandler, [750](#)
 - LPI2C_DRV_MasterInit, [750](#)
 - LPI2C_DRV_MasterReceiveData, [750](#)
 - LPI2C_DRV_MasterReceiveDataBlocking, [751](#)
 - LPI2C_DRV_MasterSendData, [751](#)
 - LPI2C_DRV_MasterSendDataBlocking, [751](#)
 - LPI2C_DRV_MasterSetBaudRate, [752](#)
 - LPI2C_DRV_MasterSetSlaveAddr, [752](#)
 - LPI2C_DRV_SetMasterBusIdleTimeout, [752](#)
 - LPI2C_DRV_SlaveAbortTransferData, [753](#)
 - LPI2C_DRV_SlaveDeinit, [753](#)
 - LPI2C_DRV_SlaveGetDefaultConfig, [753](#)
 - LPI2C_DRV_SlaveGetTransferStatus, [753](#)
 - LPI2C_DRV_SlaveIRQHandler, [755](#)
 - LPI2C_DRV_SlaveInit, [753](#)
 - LPI2C_DRV_SlaveReceiveData, [755](#)
 - LPI2C_DRV_SlaveReceiveDataBlocking, [755](#)
 - LPI2C_DRV_SlaveSendData, [756](#)
 - LPI2C_DRV_SlaveSendDataBlocking, [756](#)
 - LPI2C_DRV_SlaveSetRxBuffer, [756](#)
 - LPI2C_DRV_SlaveSetTxBuffer, [757](#)
 - LPI2C_FAST_MODE, [748](#)
 - LPI2C_STANDARD_MODE, [748](#)
 - LPI2C_USING_DMA, [748](#)
 - LPI2C_USING_INTERRUPTS, [748](#)
 - lpi2c_mode_t, [748](#)
 - lpi2c_transfer_type_t, [748](#)
- LPI2C_DRV_MasterAbortTransferData
 - LPI2C Driver, [748](#)
- LPI2C_DRV_MasterDeinit
 - LPI2C Driver, [749](#)
- LPI2C_DRV_MasterGetBaudRate
 - LPI2C Driver, [749](#)
- LPI2C_DRV_MasterGetDefaultConfig
 - LPI2C Driver, [749](#)
- LPI2C_DRV_MasterGetTransferStatus
 - LPI2C Driver, [749](#)

- LPI2C_DRV_MasterIRQHandler
 - LPI2C Driver, [750](#)
- LPI2C_DRV_MasterInit
 - LPI2C Driver, [750](#)
- LPI2C_DRV_MasterReceiveData
 - LPI2C Driver, [750](#)
- LPI2C_DRV_MasterReceiveDataBlocking
 - LPI2C Driver, [751](#)
- LPI2C_DRV_MasterSendData
 - LPI2C Driver, [751](#)
- LPI2C_DRV_MasterSendDataBlocking
 - LPI2C Driver, [751](#)
- LPI2C_DRV_MasterSetBaudRate
 - LPI2C Driver, [752](#)
- LPI2C_DRV_MasterSetSlaveAddr
 - LPI2C Driver, [752](#)
- LPI2C_DRV_SetMasterBusIdleTimeout
 - LPI2C Driver, [752](#)
- LPI2C_DRV_SlaveAbortTransferData
 - LPI2C Driver, [753](#)
- LPI2C_DRV_SlaveDeinit
 - LPI2C Driver, [753](#)
- LPI2C_DRV_SlaveGetDefaultConfig
 - LPI2C Driver, [753](#)
- LPI2C_DRV_SlaveGetTransferStatus
 - LPI2C Driver, [753](#)
- LPI2C_DRV_SlaveIRQHandler
 - LPI2C Driver, [755](#)
- LPI2C_DRV_SlaveInit
 - LPI2C Driver, [753](#)
- LPI2C_DRV_SlaveReceiveData
 - LPI2C Driver, [755](#)
- LPI2C_DRV_SlaveReceiveDataBlocking
 - LPI2C Driver, [755](#)
- LPI2C_DRV_SlaveSendData
 - LPI2C Driver, [756](#)
- LPI2C_DRV_SlaveSendDataBlocking
 - LPI2C Driver, [756](#)
- LPI2C_DRV_SlaveSetRxBuffer
 - LPI2C Driver, [756](#)
- LPI2C_DRV_SlaveSetTxBuffer
 - LPI2C Driver, [757](#)
- LPI2C_FAST_MODE
 - LPI2C Driver, [748](#)
- LPI2C_STANDARD_MODE
 - LPI2C Driver, [748](#)
- LPI2C_USING_DMA
 - LPI2C Driver, [748](#)
- LPI2C_USING_INTERRUPTS
 - LPI2C Driver, [748](#)
- LPIT Driver, [758](#)
 - LPIT_DRV_ClearInterruptFlagTimerChannels, [764](#)
 - LPIT_DRV_Deinit, [765](#)
 - LPIT_DRV_DisableTimerChannelInterrupt, [765](#)
 - LPIT_DRV_EnableTimerChannelInterrupt, [765](#)
 - LPIT_DRV_GetCurrentTimerCount, [766](#)
 - LPIT_DRV_GetCurrentTimerUs, [766](#)
 - LPIT_DRV_GetDefaultChanConfig, [766](#)
 - LPIT_DRV_GetDefaultConfig, [767](#)
 - LPIT_DRV_GetInterruptFlagTimerChannels, [767](#)
 - LPIT_DRV_GetTimerPeriodByCount, [767](#)
 - LPIT_DRV_GetTimerPeriodByUs, [769](#)
 - LPIT_DRV_Init, [769](#)
 - LPIT_DRV_InitChannel, [769](#)
 - LPIT_DRV_SetTimerPeriodByCount, [770](#)
 - LPIT_DRV_SetTimerPeriodByUs, [770](#)
 - LPIT_DRV_SetTimerPeriodInDual16ModeByCount, [771](#)
 - LPIT_DRV_SetTimerPeriodInDual16ModeByUs, [771](#)
 - LPIT_DRV_StartTimerChannels, [771](#)
 - LPIT_DRV_StopTimerChannels, [772](#)
 - LPIT_DUAL_PERIODIC_COUNTER, [764](#)
 - LPIT_INPUT_CAPTURE, [764](#)
 - LPIT_PERIOD_UNITS_COUNTS, [764](#)
 - LPIT_PERIOD_UNITS_MICROSECONDS, [764](#)
 - LPIT_PERIODIC_COUNTER, [764](#)
 - LPIT_TRIGGER_ACCUMULATOR, [764](#)
 - LPIT_TRIGGER_SOURCE_EXTERNAL, [764](#)
 - LPIT_TRIGGER_SOURCE_INTERNAL, [764](#)
 - lpit_period_units_t, [764](#)
 - lpit_timer_modes_t, [764](#)
 - lpit_trigger_source_t, [764](#)
 - MAX_PERIOD_COUNT, [763](#)
 - MAX_PERIOD_COUNT_16_BIT, [763](#)
 - MAX_PERIOD_COUNT_IN_DUAL_16BIT_MODE, [763](#)
- LPIT_DRV_ClearInterruptFlagTimerChannels
 - LPIT Driver, [764](#)
- LPIT_DRV_Deinit
 - LPIT Driver, [765](#)
- LPIT_DRV_DisableTimerChannelInterrupt
 - LPIT Driver, [765](#)
- LPIT_DRV_EnableTimerChannelInterrupt
 - LPIT Driver, [765](#)
- LPIT_DRV_GetCurrentTimerCount
 - LPIT Driver, [766](#)
- LPIT_DRV_GetCurrentTimerUs
 - LPIT Driver, [766](#)
- LPIT_DRV_GetDefaultChanConfig
 - LPIT Driver, [766](#)
- LPIT_DRV_GetDefaultConfig
 - LPIT Driver, [767](#)
- LPIT_DRV_GetInterruptFlagTimerChannels
 - LPIT Driver, [767](#)
- LPIT_DRV_GetTimerPeriodByCount
 - LPIT Driver, [767](#)
- LPIT_DRV_GetTimerPeriodByUs
 - LPIT Driver, [769](#)
- LPIT_DRV_Init
 - LPIT Driver, [769](#)
- LPIT_DRV_InitChannel
 - LPIT Driver, [769](#)
- LPIT_DRV_SetTimerPeriodByCount
 - LPIT Driver, [770](#)
- LPIT_DRV_SetTimerPeriodByUs
 - LPIT Driver, [770](#)

- LPIT Driver, [770](#)
- LPIT_DRV_SetTimerPeriodInDual16ModeByCount
 - LPIT Driver, [771](#)
- LPIT_DRV_SetTimerPeriodInDual16ModeByUs
 - LPIT Driver, [771](#)
- LPIT_DRV_StartTimerChannels
 - LPIT Driver, [771](#)
- LPIT_DRV_StopTimerChannels
 - LPIT Driver, [772](#)
- LPIT_DUAL_PERIODIC_COUNTER
 - LPIT Driver, [764](#)
- LPIT_INPUT_CAPTURE
 - LPIT Driver, [764](#)
- LPIT_PERIOD_UNITS_COUNTS
 - LPIT Driver, [764](#)
- LPIT_PERIOD_UNITS_MICROSECONDS
 - LPIT Driver, [764](#)
- LPIT_PERIODIC_COUNTER
 - LPIT Driver, [764](#)
- LPIT_TRIGGER_ACCUMULATOR
 - LPIT Driver, [764](#)
- LPIT_TRIGGER_SOURCE_EXTERNAL
 - LPIT Driver, [764](#)
- LPIT_TRIGGER_SOURCE_INTERNAL
 - LPIT Driver, [764](#)
- LPSPI Driver, [773](#)
 - g_lpspiBase, [790](#)
 - g_lpspiIrqId, [790](#)
 - g_lpspiStatePtr, [790](#)
 - LPSPi0_IRQHandler, [782](#)
 - LPSPi1_IRQHandler, [782](#)
 - LPSPi2_IRQHandler, [782](#)
 - LPSPI_ACTIVE_HIGH, [781](#)
 - LPSPI_ACTIVE_LOW, [781](#)
 - LPSPI_CLOCK_PHASE_1ST_EDGE, [781](#)
 - LPSPI_CLOCK_PHASE_2ND_EDGE, [781](#)
 - LPSPI_DRV_DisableTEIEInterrupts, [782](#)
 - LPSPI_DRV_FillupTxBuffer, [782](#)
 - LPSPI_DRV_IRQHandler, [782](#)
 - LPSPI_DRV_MasterAbortTransfer, [783](#)
 - LPSPI_DRV_MasterConfigureBus, [783](#)
 - LPSPI_DRV_MasterDeinit, [784](#)
 - LPSPI_DRV_MasterGetDefaultConfig, [784](#)
 - LPSPI_DRV_MasterGetTransferStatus, [784](#)
 - LPSPI_DRV_MasterIRQHandler, [785](#)
 - LPSPI_DRV_MasterInit, [784](#)
 - LPSPI_DRV_MasterSetDelay, [785](#)
 - LPSPI_DRV_MasterTransfer, [786](#)
 - LPSPI_DRV_MasterTransferBlocking, [786](#)
 - LPSPI_DRV_ReadRXBuffer, [787](#)
 - LPSPI_DRV_SetPcs, [787](#)
 - LPSPI_DRV_SlaveAbortTransfer, [787](#)
 - LPSPI_DRV_SlaveDeinit, [788](#)
 - LPSPI_DRV_SlaveGetDefaultConfig, [788](#)
 - LPSPI_DRV_SlaveGetTransferStatus, [788](#)
 - LPSPI_DRV_SlaveIRQHandler, [789](#)
 - LPSPI_DRV_SlaveInit, [788](#)
 - LPSPI_DRV_SlaveTransfer, [789](#)
 - LPSPI_DRV_SlaveTransferBlocking, [789](#)
 - LPSPI_PCS0, [781](#)
 - LPSPI_PCS1, [781](#)
 - LPSPI_PCS2, [782](#)
 - LPSPI_PCS3, [782](#)
 - LPSPI_RECEIVE_FAIL, [782](#)
 - LPSPI_SCK_ACTIVE_HIGH, [781](#)
 - LPSPI_SCK_ACTIVE_LOW, [781](#)
 - LPSPI_TRANSFER_OK, [782](#)
 - LPSPI_TRANSMIT_FAIL, [782](#)
 - LPSPI_USING_DMA, [781](#)
 - LPSPI_USING_INTERRUPTS, [781](#)
 - lpspi_clock_phase_t, [781](#)
 - lpspi_sck_polarity_t, [781](#)
 - lpspi_signal_polarity_t, [781](#)
 - lpspi_transfer_type, [781](#)
 - lpspi_which_pcs_t, [781](#)
 - transfer_status_t, [782](#)
- LPSPi0_IRQHandler
 - LPSPI Driver, [782](#)
- LPSPi1_IRQHandler
 - LPSPI Driver, [782](#)
- LPSPi2_IRQHandler
 - LPSPI Driver, [782](#)
- LPSPI_ACTIVE_HIGH
 - LPSPI Driver, [781](#)
- LPSPI_ACTIVE_LOW
 - LPSPI Driver, [781](#)
- LPSPI_CLOCK_PHASE_1ST_EDGE
 - LPSPI Driver, [781](#)
- LPSPI_CLOCK_PHASE_2ND_EDGE
 - LPSPI Driver, [781](#)
- LPSPI_DRV_DisableTEIEInterrupts
 - LPSPI Driver, [782](#)
- LPSPI_DRV_FillupTxBuffer
 - LPSPI Driver, [782](#)
- LPSPI_DRV_IRQHandler
 - LPSPI Driver, [782](#)
- LPSPI_DRV_MasterAbortTransfer
 - LPSPI Driver, [783](#)
- LPSPI_DRV_MasterConfigureBus
 - LPSPI Driver, [783](#)
- LPSPI_DRV_MasterDeinit
 - LPSPI Driver, [784](#)
- LPSPI_DRV_MasterGetDefaultConfig
 - LPSPI Driver, [784](#)
- LPSPI_DRV_MasterGetTransferStatus
 - LPSPI Driver, [784](#)
- LPSPI_DRV_MasterIRQHandler
 - LPSPI Driver, [785](#)
- LPSPI_DRV_MasterInit
 - LPSPI Driver, [784](#)
- LPSPI_DRV_MasterSetDelay
 - LPSPI Driver, [785](#)
- LPSPI_DRV_MasterTransfer
 - LPSPI Driver, [786](#)
- LPSPI_DRV_MasterTransferBlocking
 - LPSPI Driver, [786](#)

- LPSPi_DRV_ReadRXBuffer
 - LPSPi Driver, [787](#)
- LPSPi_DRV_SetPcs
 - LPSPi Driver, [787](#)
- LPSPi_DRV_SlaveAbortTransfer
 - LPSPi Driver, [787](#)
- LPSPi_DRV_SlaveDeinit
 - LPSPi Driver, [788](#)
- LPSPi_DRV_SlaveGetDefaultConfig
 - LPSPi Driver, [788](#)
- LPSPi_DRV_SlaveGetTransferStatus
 - LPSPi Driver, [788](#)
- LPSPi_DRV_SlaveIRQHandler
 - LPSPi Driver, [789](#)
- LPSPi_DRV_SlaveInit
 - LPSPi Driver, [788](#)
- LPSPi_DRV_SlaveTransfer
 - LPSPi Driver, [789](#)
- LPSPi_DRV_SlaveTransferBlocking
 - LPSPi Driver, [789](#)
- LPSPi_PCS0
 - LPSPi Driver, [781](#)
- LPSPi_PCS1
 - LPSPi Driver, [781](#)
- LPSPi_PCS2
 - LPSPi Driver, [782](#)
- LPSPi_PCS3
 - LPSPi Driver, [782](#)
- LPSPi_RECEIVE_FAIL
 - LPSPi Driver, [782](#)
- LPSPi_SCK_ACTIVE_HIGH
 - LPSPi Driver, [781](#)
- LPSPi_SCK_ACTIVE_LOW
 - LPSPi Driver, [781](#)
- LPSPi_TRANSFER_OK
 - LPSPi Driver, [782](#)
- LPSPi_TRANSMIT_FAIL
 - LPSPi Driver, [782](#)
- LPSPi_USING_DMA
 - LPSPi Driver, [781](#)
- LPSPi_USING_INTERRUPTS
 - LPSPi Driver, [781](#)
- LPTMR Driver, [791](#)
 - LPTMR_CLOCKSOURCE_1KHZ_LPO, [795](#)
 - LPTMR_CLOCKSOURCE_PCC, [795](#)
 - LPTMR_CLOCKSOURCE_RTC, [795](#)
 - LPTMR_CLOCKSOURCE_SIRCDIV2, [795](#)
 - LPTMR_COUNTER_UNITS_MICROSECONDS, [795](#)
 - LPTMR_COUNTER_UNITS_TICKS, [795](#)
 - LPTMR_DRV_ClearCompareFlag, [797](#)
 - LPTMR_DRV_Deinit, [797](#)
 - LPTMR_DRV_GetCompareFlag, [797](#)
 - LPTMR_DRV_GetCompareValueByCount, [797](#)
 - LPTMR_DRV_GetCompareValueByUs, [797](#)
 - LPTMR_DRV_GetConfig, [798](#)
 - LPTMR_DRV_GetCounterValueByCount, [798](#)
 - LPTMR_DRV_Init, [798](#)
 - LPTMR_DRV_InitConfigStruct, [798](#)
 - LPTMR_DRV_IsRunning, [798](#)
 - LPTMR_DRV_SetCompareValueByCount, [799](#)
 - LPTMR_DRV_SetCompareValueByUs, [799](#)
 - LPTMR_DRV_SetConfig, [799](#)
 - LPTMR_DRV_SetInterrupt, [800](#)
 - LPTMR_DRV_SetPinConfiguration, [800](#)
 - LPTMR_DRV_StartCounter, [800](#)
 - LPTMR_DRV_StopCounter, [800](#)
 - LPTMR_PINPOLARITY_FALLING, [796](#)
 - LPTMR_PINPOLARITY_RISING, [796](#)
 - LPTMR_PINSELECT_ALT2, [796](#)
 - LPTMR_PINSELECT_ALT3, [796](#)
 - LPTMR_PINSELECT_TRGMUX, [796](#)
 - LPTMR_PRESCALE_1024_GLITCHFILTER_512, [796](#)
 - LPTMR_PRESCALE_128_GLITCHFILTER_64, [796](#)
 - LPTMR_PRESCALE_16384_GLITCHFILTER_↵
8192, [796](#)
 - LPTMR_PRESCALE_16_GLITCHFILTER_8, [796](#)
 - LPTMR_PRESCALE_2, [796](#)
 - LPTMR_PRESCALE_2048_GLITCHFILTER_↵
1024, [796](#)
 - LPTMR_PRESCALE_256_GLITCHFILTER_128, [796](#)
 - LPTMR_PRESCALE_32768_GLITCHFILTER_↵
16384, [796](#)
 - LPTMR_PRESCALE_32_GLITCHFILTER_16, [796](#)
 - LPTMR_PRESCALE_4096_GLITCHFILTER_↵
2048, [796](#)
 - LPTMR_PRESCALE_4_GLITCHFILTER_2, [796](#)
 - LPTMR_PRESCALE_512_GLITCHFILTER_256, [796](#)
 - LPTMR_PRESCALE_64_GLITCHFILTER_32, [796](#)
 - LPTMR_PRESCALE_65536_GLITCHFILTER_↵
32768, [796](#)
 - LPTMR_PRESCALE_8192_GLITCHFILTER_↵
4096, [796](#)
 - LPTMR_PRESCALE_8_GLITCHFILTER_4, [796](#)
 - LPTMR_WORKMODE_PULSECOUNTER, [797](#)
 - LPTMR_WORKMODE_TIMER, [797](#)
 - lptmr_clocksource_t, [795](#)
 - lptmr_counter_units_t, [795](#)
 - lptmr_pinpolarity_t, [795](#)
 - lptmr_pinselect_t, [796](#)
 - lptmr_prescaler_t, [796](#)
 - lptmr_workmode_t, [796](#)
 - LPTMR_CLOCKSOURCE_1KHZ_LPO
 - LPTMR Driver, [795](#)
 - LPTMR_CLOCKSOURCE_PCC
 - LPTMR Driver, [795](#)
 - LPTMR_CLOCKSOURCE_RTC
 - LPTMR Driver, [795](#)
 - LPTMR_CLOCKSOURCE_SIRCDIV2
 - LPTMR Driver, [795](#)
 - LPTMR_COUNTER_UNITS_MICROSECONDS
 - LPTMR Driver, [795](#)

- LPTMR_COUNTER_UNITS_TICKS
 - LPTMR Driver, [795](#)
- LPTMR_DRV_ClearCompareFlag
 - LPTMR Driver, [797](#)
- LPTMR_DRV_Deinit
 - LPTMR Driver, [797](#)
- LPTMR_DRV_GetCompareFlag
 - LPTMR Driver, [797](#)
- LPTMR_DRV_GetCompareValueByCount
 - LPTMR Driver, [797](#)
- LPTMR_DRV_GetCompareValueByUs
 - LPTMR Driver, [797](#)
- LPTMR_DRV_GetConfig
 - LPTMR Driver, [798](#)
- LPTMR_DRV_GetCounterValueByCount
 - LPTMR Driver, [798](#)
- LPTMR_DRV_Init
 - LPTMR Driver, [798](#)
- LPTMR_DRV_InitConfigStruct
 - LPTMR Driver, [798](#)
- LPTMR_DRV_IsRunning
 - LPTMR Driver, [798](#)
- LPTMR_DRV_SetCompareValueByCount
 - LPTMR Driver, [799](#)
- LPTMR_DRV_SetCompareValueByUs
 - LPTMR Driver, [799](#)
- LPTMR_DRV_SetConfig
 - LPTMR Driver, [799](#)
- LPTMR_DRV_SetInterrupt
 - LPTMR Driver, [800](#)
- LPTMR_DRV_SetPinConfiguration
 - LPTMR Driver, [800](#)
- LPTMR_DRV_StartCounter
 - LPTMR Driver, [800](#)
- LPTMR_DRV_StopCounter
 - LPTMR Driver, [800](#)
- LPTMR_PINPOLARITY_FALLING
 - LPTMR Driver, [796](#)
- LPTMR_PINPOLARITY_RISING
 - LPTMR Driver, [796](#)
- LPTMR_PINSELECT_ALT2
 - LPTMR Driver, [796](#)
- LPTMR_PINSELECT_ALT3
 - LPTMR Driver, [796](#)
- LPTMR_PINSELECT_TRGMUX
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_1024_GLITCHFILTER_512
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_128_GLITCHFILTER_64
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_16384_GLITCHFILTER_8192
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_16_GLITCHFILTER_8
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_2
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_2048_GLITCHFILTER_1024
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_256_GLITCHFILTER_128
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_32768_GLITCHFILTER_16384
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_32_GLITCHFILTER_16
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_4096_GLITCHFILTER_2048
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_4_GLITCHFILTER_2
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_512_GLITCHFILTER_256
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_64_GLITCHFILTER_32
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_65536_GLITCHFILTER_32768
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_8192_GLITCHFILTER_4096
 - LPTMR Driver, [796](#)
- LPTMR_PRESCALE_8_GLITCHFILTER_4
 - LPTMR Driver, [796](#)
- LPTMR_WORKMODE_PULSECOUNTER
 - LPTMR Driver, [797](#)
- LPTMR_WORKMODE_TIMER
 - LPTMR Driver, [797](#)
- LPUART Driver, [801](#)
 - LPUART_10_BITS_PER_CHAR, [808](#)
 - LPUART_8_BITS_PER_CHAR, [808](#)
 - LPUART_9_BITS_PER_CHAR, [808](#)
 - LPUART_DRV_AbortReceivingData, [808](#)
 - LPUART_DRV_AbortSendingData, [809](#)
 - LPUART_DRV_Deinit, [809](#)
 - LPUART_DRV_GetBaudRate, [809](#)
 - LPUART_DRV_GetDefaultConfig, [809](#)
 - LPUART_DRV_GetReceiveStatus, [810](#)
 - LPUART_DRV_GetTransmitStatus, [810](#)
 - LPUART_DRV_Init, [811](#)
 - LPUART_DRV_InstallRxCallback, [811](#)
 - LPUART_DRV_InstallTxCallback, [811](#)
 - LPUART_DRV_ReceiveData, [812](#)
 - LPUART_DRV_ReceiveDataBlocking, [812](#)
 - LPUART_DRV_ReceiveDataPolling, [812](#)
 - LPUART_DRV_SendData, [813](#)
 - LPUART_DRV_SendDataBlocking, [813](#)
 - LPUART_DRV_SendDataPolling, [813](#)
 - LPUART_DRV_SetBaudRate, [814](#)
 - LPUART_DRV_SetRxBuffer, [814](#)
 - LPUART_DRV_SetTxBuffer, [814](#)
 - LPUART_ONE_STOP_BIT, [808](#)
 - LPUART_PARITY_DISABLED, [808](#)
 - LPUART_PARITY_EVEN, [808](#)
 - LPUART_PARITY_ODD, [808](#)
 - LPUART_TWO_STOP_BIT, [808](#)
 - LPUART_USING_DMA, [808](#)
 - LPUART_USING_INTERRUPTS, [808](#)
 - lpuart_bit_count_per_char_t, [808](#)
 - lpuart_parity_mode_t, [808](#)
 - lpuart_stop_bit_count_t, [808](#)
 - lpuart_transfer_type_t, [808](#)

LPUART_10_BITS_PER_CHAR
 LPUART Driver, [808](#)
 LPUART_8_BITS_PER_CHAR
 LPUART Driver, [808](#)
 LPUART_9_BITS_PER_CHAR
 LPUART Driver, [808](#)
 LPUART_DRV_AbortReceivingData
 LPUART Driver, [808](#)
 LPUART_DRV_AbortSendingData
 LPUART Driver, [809](#)
 LPUART_DRV_Deinit
 LPUART Driver, [809](#)
 LPUART_DRV_GetBaudRate
 LPUART Driver, [809](#)
 LPUART_DRV_GetDefaultConfig
 LPUART Driver, [809](#)
 LPUART_DRV_GetReceiveStatus
 LPUART Driver, [810](#)
 LPUART_DRV_GetTransmitStatus
 LPUART Driver, [810](#)
 LPUART_DRV_Init
 LPUART Driver, [811](#)
 LPUART_DRV_InstallRxCallback
 LPUART Driver, [811](#)
 LPUART_DRV_InstallTxCallback
 LPUART Driver, [811](#)
 LPUART_DRV_ReceiveData
 LPUART Driver, [812](#)
 LPUART_DRV_ReceiveDataBlocking
 LPUART Driver, [812](#)
 LPUART_DRV_ReceiveDataPolling
 LPUART Driver, [812](#)
 LPUART_DRV_SendData
 LPUART Driver, [813](#)
 LPUART_DRV_SendDataBlocking
 LPUART Driver, [813](#)
 LPUART_DRV_SendDataPolling
 LPUART Driver, [813](#)
 LPUART_DRV_SetBaudRate
 LPUART Driver, [814](#)
 LPUART_DRV_SetRxBuffer
 LPUART Driver, [814](#)
 LPUART_DRV_SetTxBuffer
 LPUART Driver, [814](#)
 LPUART_ONE_STOP_BIT
 LPUART Driver, [808](#)
 LPUART_PARITY_DISABLED
 LPUART Driver, [808](#)
 LPUART_PARITY_EVEN
 LPUART Driver, [808](#)
 LPUART_PARITY_ODD
 LPUART Driver, [808](#)
 LPUART_TWO_STOP_BIT
 LPUART Driver, [808](#)
 LPUART_USING_DMA
 LPUART Driver, [808](#)
 LPUART_USING_INTERRUPTS
 LPUART Driver, [808](#)

LSC1_SLOPE_ACTIVE
 02. LIN configuration, [210](#)
 LSC1_SLOPE_ACTIVE2
 02. LIN configuration, [210](#)
 LSC1_SLOPE_ACTIVE_TXDL_TIMEOUT
 02. LIN configuration, [210](#)
 LSC2_SLOPE_ACTIVE
 02. LIN configuration, [210](#)
 LSC2_SLOPE_ACTIVE2
 02. LIN configuration, [210](#)
 LSC2_SLOPE_ACTIVE_TXDL_TIMEOUT
 02. LIN configuration, [210](#)
 language_version
 lin_protocol_user_config_t, [838](#)
 last_RSID
 lin_tl_descriptor_t, [836](#)
 last_cfg_result
 lin_tl_descriptor_t, [836](#)
 last_pid
 lin_protocol_state_t, [842](#)
 lin_word_status_str_t, [828](#)
 last_rx
 WOLFSSL_ALERT_HISTORY, [1340](#)
 last_tx
 WOLFSSL_ALERT_HISTORY, [1340](#)
 lastBlock
 WOLFSSL_EVP_CIPHER_CTX, [1362](#)
 lastDate
 CRL_Entry, [1261](#)
 lastDateFormat
 CRL_Entry, [1261](#)
 lastErr
 DckeArgs, [1263](#)
 ProcPeerCertArgs, [1308](#)
 lastUsed
 WOLFSSL_EVP_CIPHER_CTX, [1362](#)
 lckcLockRegCfg
 uja113x_init_cfg_t, [184](#)
 Id_assign_NAD
 Node configuration, [900](#)
 Id_assign_NAD_j2602
 Node configuration, [905](#)
 Id_assign_frame_id_range
 Node configuration, [900](#)
 Id_check_response
 Node configuration, [902](#)
 Id_check_response_j2602
 Node configuration, [905](#)
 Id_conditional_change_NAD
 Node configuration, [902](#)
 Id_error_code
 lin_tl_descriptor_t, [836](#)
 Id_get_raw
 Raw API, [1014](#)
 Id_init
 Initialization, [682](#)
 Id_is_ready
 Node configuration, [902](#)

- ld_is_ready_j2602
 - Node configuration, [905](#)
- ld_put_raw
 - Raw API, [1014](#)
- ld_queue_status_t
 - Low level API, [846](#)
- ld_raw_rx_status
 - Raw API, [1014](#)
- ld_raw_tx_status
 - Raw API, [1015](#)
- ld_read_by_id
 - Node identification, [907](#)
- ld_read_by_id_callout
 - Low level API, [850](#)
- ld_read_configuration
 - Node configuration, [903](#)
- ld_receive_message
 - Cooked API, [400](#)
- ld_reconfig_msg_ID
 - Node configuration, [906](#)
- ld_return_data
 - lin_tl_descriptor_t, [836](#)
- ld_rx_status
 - Cooked API, [400](#)
- ld_save_configuration
 - Node configuration, [903](#)
- ld_send_message
 - Cooked API, [401](#)
- ld_set_configuration
 - Node configuration, [903](#)
- ld_tx_status
 - Cooked API, [401](#)
- leaf_length
 - __blake2b_param, [1243](#)
 - __blake2s_param, [1245](#)
- len
 - wolfssl_TI_Hash, [1372](#)
- length
 - bufferStatic, [1254](#)
 - can_message_t, [388](#)
 - DckeArgs, [1263](#)
 - DerBuffer, [1272](#)
 - DtlsHandShakeHeader, [1279](#)
 - DtlsRecordLayerHeader, [1280](#)
 - edma_scatter_gather_list_t, [417](#)
 - enet_buffer_descriptor_t, [446](#)
 - enet_buffer_t, [446](#)
 - HandShakeHeader, [1284](#)
 - RecordLayerHeader, [1315](#)
 - SckeArgs, [1318](#)
 - ScvArgs, [1319](#)
 - SskeArgs, [1326](#)
 - WOLFSSL_ASN1_BIT_STRING, [1341](#)
 - WOLFSSL_ASN1_STRING, [1343](#)
 - WOLFSSL_BUFFER_INFO, [1346](#)
 - WOLFSSL_DH, [1355](#)
 - x509_buffer, [1380](#)
- level
 - WOLFSSL_ALERT, [1340](#)
- lhc
 - sbc_int_config_t, [1182](#)
- limpHomeCtrl
 - uja113x_fsc_cfg_t, [218](#)
- lin1ModeCtrl
 - uja113x_linc_cfg_t, [209](#)
- lin1SlopeCtrl
 - uja113x_linc_cfg_t, [209](#)
- lin2ModeCtrl
 - uja113x_linc_cfg_t, [209](#)
- lin2SlopeCtrl
 - uja113x_linc_cfg_t, [209](#)
- lin_associate_frame_t, [831](#)
 - associated_uncond_frame_ptr, [831](#)
 - coll_resolv_schd, [831](#)
 - num_of_associated_uncond_frames, [832](#)
- lin_calc_max_header_timeout_cnt
 - Low level API, [850](#)
- lin_calc_max_res_timeout_cnt
 - Low level API, [850](#)
- lin_callback_t
 - LIN Driver, [729](#)
- lin_collision_resolve
 - LIN 2.1 Specific API, [717](#)
- lin_diag_service_callback
 - Common Transport Layer API, [360](#)
- lin_diagnostic_class_t
 - Low level API, [846](#)
- lin_diagnostic_state_t
 - Low level API, [846](#)
- lin_event_id_t
 - LIN Driver, [729](#)
- lin_frame_response_t
 - Low level API, [847](#)
- lin_frame_t, [832](#)
 - flag_offset, [832](#)
 - flag_size, [832](#)
 - frame_data_ptr, [832](#)
 - frm_len, [832](#)
 - frm_offset, [832](#)
 - frm_response, [832](#)
 - frm_type, [832](#)
- lin_frame_type_t
 - Low level API, [847](#)
- lin_last_cfg_result_t
 - Low level API, [847](#)
- lin_llid_deinit
 - Low level API, [850](#)
- lin_llid_event_id_t
 - Low level API, [847](#)
- lin_llid_get_state
 - Low level API, [850](#)
- lin_llid_ignore_response
 - Low level API, [851](#)
- lin_llid_init
 - Low level API, [851](#)
- lin_llid_int_disable

- Low level API, [851](#)
- lin_ild_int_enable
 - Low level API, [851](#)
- lin_ild_rx_response
 - Low level API, [852](#)
- lin_ild_set_low_power_mode
 - Low level API, [852](#)
- lin_ild_set_response
 - Low level API, [852](#)
- lin_ild_timeout_service
 - Low level API, [852](#)
- lin_ild_tx_header
 - Low level API, [853](#)
- lin_ild_tx_wake_up
 - Low level API, [853](#)
- lin_make_res_evt_frame
 - LIN 2.1 Specific API, [717](#)
- lin_master_data_t, [839](#)
 - active_schedule_id, [840](#)
 - event_trigger_collision_flg, [840](#)
 - flag_offset, [840](#)
 - flag_size, [840](#)
 - frm_offset, [840](#)
 - frm_size, [840](#)
 - master_data_buffer, [840](#)
 - previous_schedule_id, [840](#)
 - schedule_start_entry_ptr, [840](#)
 - send_functional_request_flg, [841](#)
 - send_slave_res_flg, [841](#)
- lin_message_status_t
 - Low level API, [848](#)
- lin_message_timeout_type_t
 - Low level API, [848](#)
- lin_node_attribute_t, [829](#)
 - configured_NAD_ptr, [830](#)
 - fault_state_signal_ptr, [830](#)
 - initial_NAD, [830](#)
 - N_As_timeout, [830](#)
 - N_Cr_timeout, [830](#)
 - num_frame_have_esignal, [830](#)
 - num_of_fault_state_signal, [830](#)
 - number_support_sid, [830](#)
 - P2_min, [830](#)
 - product_id, [830](#)
 - resp_err_frm_id_ptr, [830](#)
 - response_error, [831](#)
 - response_error_bit_offset_ptr, [831](#)
 - response_error_byte_offset_ptr, [831](#)
 - ST_min, [831](#)
 - serial_number, [831](#)
 - service_flags_ptr, [831](#)
 - service_supported_ptr, [831](#)
- lin_node_state_t
 - LIN Driver, [730](#)
- lin_pid_resp_callback_handler
 - Low level API, [853](#)
- lin_process_parity
 - Low level API, [854](#)
- lin_product_id_t, [1292](#)
 - function_id, [1292](#)
 - supplier_id, [1292](#)
 - variant, [1292](#)
- lin_protocol_handle_t
 - Low level API, [848](#)
- lin_protocol_state_t, [841](#)
 - baud_rate, [841](#)
 - current_id, [841](#)
 - diagnostic_mode, [841](#)
 - error_in_response, [841](#)
 - frame_timeout_cnt, [842](#)
 - go_to_sleep_flg, [842](#)
 - idle_timeout_cnt, [842](#)
 - last_pid, [842](#)
 - next_transmit_tick, [842](#)
 - num_of_processed_frame, [842](#)
 - overrun_flg, [842](#)
 - response_buffer_ptr, [842](#)
 - response_length, [842](#)
 - save_config_flg, [842](#)
 - successful_transfer, [842](#)
 - transmit_error_resp_sig_flg, [843](#)
 - word_status, [843](#)
- lin_protocol_user_config_t, [837](#)
 - diagnostic_class, [838](#)
 - frame_start, [838](#)
 - frame_tbl_ptr, [838](#)
 - function, [838](#)
 - language_version, [838](#)
 - lin_user_config_ptr, [838](#)
 - list_identifiers_RAM_ptr, [838](#)
 - list_identifiers_ROM_ptr, [838](#)
 - master_ifc_handle, [838](#)
 - max_idle_timeout_cnt, [839](#)
 - max_message_length, [839](#)
 - num_of_schedules, [839](#)
 - number_of_configurable_frames, [839](#)
 - protocol_version, [839](#)
 - schedule_start, [839](#)
 - schedule_tbl, [839](#)
 - slave_ifc_handle, [839](#)
 - tl_rx_queue_data_ptr, [839](#)
 - tl_tx_queue_data_ptr, [839](#)
- lin_sch_tbl_type_t
 - Low level API, [848](#)
- lin_schedule_data_t, [833](#)
 - delay_integer, [833](#)
 - frm_id, [833](#)
 - tl_queue_data, [833](#)
- lin_schedule_t, [833](#)
 - num_slots, [833](#)
 - ptr_sch_data_ptr, [833](#)
 - sch_tbl_type, [833](#)
- lin_serial_number_t, [829](#)
 - serial_0, [829](#)
 - serial_1, [829](#)
 - serial_2, [829](#)

- serial_3, [829](#)
- lin_service_status_t
 - Low level API, [849](#)
- lin_state_t, [726](#)
 - baudrateEvalEnable, [727](#)
 - Callback, [727](#)
 - checksum, [727](#)
 - cntByte, [727](#)
 - currentEventId, [727](#)
 - currentId, [727](#)
 - currentNodeState, [727](#)
 - currentPid, [727](#)
 - fallingEdgeInterruptCount, [727](#)
 - isBusBusy, [727](#)
 - isRxBlocking, [727](#)
 - isRxBusy, [727](#)
 - isTxBlocking, [728](#)
 - isTxBusy, [728](#)
 - linSourceClockFreq, [728](#)
 - rxBuff, [728](#)
 - rxCompleted, [728](#)
 - rxSize, [728](#)
 - timeoutCounter, [728](#)
 - timeoutCounterFlag, [728](#)
 - txBuff, [728](#)
 - txCompleted, [728](#)
 - txSize, [728](#)
- lin_timer_get_time_interval_t
 - LIN Driver, [729](#)
- lin_tl_callback_handler
 - Low level API, [854](#)
- lin_tl_callback_return_t
 - Low level API, [849](#)
- lin_tl_descriptor_t, [834](#)
 - check_timeout, [835](#)
 - check_timeout_type, [835](#)
 - diag_interleave_state, [835](#)
 - diag_state, [835](#)
 - FF_pdu_received, [835](#)
 - frame_counter, [835](#)
 - interleave_timeout_counter, [836](#)
 - last_RSID, [836](#)
 - last_cfg_result, [836](#)
 - ld_error_code, [836](#)
 - ld_return_data, [836](#)
 - num_of_pdu, [836](#)
 - product_id_ptr, [836](#)
 - receive_NAD_ptr, [836](#)
 - receive_message_length_ptr, [836](#)
 - receive_message_ptr, [836](#)
 - rx_msg_size, [836](#)
 - rx_msg_status, [837](#)
 - service_status, [837](#)
 - slave_resp_cnt, [837](#)
 - tl_rx_queue, [837](#)
 - tl_tx_queue, [837](#)
 - tx_msg_size, [837](#)
 - tx_msg_status, [837](#)
- lin_tl_event_id_t
 - Low level API, [849](#)
- lin_tl_pdu_data_t
 - Low level API, [845](#)
- lin_tl_queue_t
 - Low level API, [845](#)
- lin_transport_layer_queue_t, [834](#)
 - queue_current_size, [834](#)
 - queue_header, [834](#)
 - queue_max_size, [834](#)
 - queue_status, [834](#)
 - queue_tail, [834](#)
 - tl_pdu_ptr, [834](#)
- lin_update_err_signal
 - LIN 2.1 Specific API, [718](#)
- lin_update_rx_evnt_frame
 - LIN 2.1 Specific API, [718](#)
- lin_update_word_status_lin21
 - LIN 2.1 Specific API, [718](#)
- lin_user_config_ptr
 - lin_protocol_user_config_t, [838](#)
- lin_user_config_t, [725](#)
 - autobaudEnable, [725](#)
 - baudRate, [725](#)
 - classicPID, [725](#)
 - nodeFunction, [726](#)
 - numOfClassicPID, [726](#)
 - timerGetTimeIntervalCallback, [726](#)
- lin_word_status_str_t, [827](#)
 - bus_activity, [828](#)
 - error_in_res, [828](#)
 - event_trigger_collision_flg, [828](#)
 - go_to_sleep_flg, [828](#)
 - last_pid, [828](#)
 - overrun, [828](#)
 - reserved, [828](#)
 - save_config_flg, [828](#)
 - successful_transfer, [828](#)
- linJ2602Dis
 - fs45_wu2_reg_t, [1054](#)
- linSourceClockFreq
 - lin_state_t, [728](#)
- linSr
 - fs45_wu2_reg_t, [1054](#)
- link
 - phy_basicStatus_t, [1307](#)
- linkDownEventCB
 - phy_config_t, [947](#)
- linkUpEventCB
 - phy_config_t, [947](#)
- linxLinCtrl
 - uja113x_init_cfg_t, [184](#)
- list_identifiers_RAM_ptr
 - lin_protocol_user_config_t, [838](#)
- list_identifiers_ROM_ptr
 - lin_protocol_user_config_t, [838](#)
- loLen
 - Md4, [1293](#)

- Md5, [1294](#)
- Sha, [1321](#)
- Sha256, [1321](#)
- loadValueMode
 - pdb_timer_config_t, [933](#)
- Local Interconnect Network (LIN), [816](#)
- localWakeupPhy
 - phy_tja110x_config_t, [1139](#)
- localWuTimer
 - phy_tja110x_config_t, [1139](#)
- location
 - phy_config_t, [947](#)
- lock
 - WOLF_EVENT_QUEUE, [1336](#)
- lock0
 - uja113x_lckc_cfg_t, [233](#)
- lock1
 - uja113x_lckc_cfg_t, [233](#)
- lock2
 - uja113x_lckc_cfg_t, [233](#)
- lock3
 - uja113x_lckc_cfg_t, [233](#)
- lock4
 - uja113x_lckc_cfg_t, [233](#)
- lock5
 - uja113x_lckc_cfg_t, [233](#)
- lock6
 - uja113x_lckc_cfg_t, [233](#)
- lockMask
 - sbc_int_config_t, [1182](#)
- lockRegisterLock
 - rtc_register_lock_config_t, [1005](#)
- lockTargetModuleReg
 - trgmux_inout_mapping_config_t, [1148](#)
- locked
 - scg_firc_config_t, [331](#)
 - scg_sirc_config_t, [330](#)
 - scg_sosc_config_t, [329](#)
 - scg_spill_config_t, [332](#)
- lookup
 - WOLFSSL_X509_STORE, [1378](#)
- loopTransferConfig
 - edma_transfer_config_t, [420](#)
- Low level API, [824](#)
 - CALLBACK_HANDLER, [843](#)
 - DIAG_INTERLEAVE_MODE, [846](#)
 - DIAG_NO_RESPONSE, [846](#)
 - DIAG_NONE, [846](#)
 - DIAG_NOT_START, [846](#)
 - DIAG_ONLY_MODE, [846](#)
 - DIAG_RESPONSE, [846](#)
 - diag_interleaved_state_t, [845](#)
 - g_buffer_backup_data, [854](#)
 - g_lin_flag_handle_tbl, [854](#)
 - g_lin_frame_data_buffer, [854](#)
 - g_lin_frame_flag_handle_tbl, [854](#)
 - g_lin_frame_updating_flag_tbl, [854](#)
 - g_lin_hardware_ifc, [854](#)
 - g_lin_master_data_array, [854](#)
 - g_lin_node_attribute_array, [854](#)
 - g_lin_protocol_state_array, [854](#)
 - g_lin_protocol_user_cfg_array, [854](#)
 - g_lin_tl_descriptor_array, [854](#)
 - g_lin_virtual_ifc, [855](#)
 - l_diagnostic_mode_t, [846](#)
 - LD_CHECK_N_AS_TIMEOUT, [848](#)
 - LD_CHECK_N_CR_TIMEOUT, [848](#)
 - LD_COMPLETED, [848](#)
 - LD_DATA_AVAILABLE, [846](#)
 - LD_DIAG_IDLE, [847](#)
 - LD_DIAG_RX_FUNCTIONAL, [847](#)
 - LD_DIAG_RX_INTERLEAVED, [847](#)
 - LD_DIAG_RX_PHY, [847](#)
 - LD_DIAG_TX_FUNCTIONAL, [847](#)
 - LD_DIAG_TX_INTERLEAVED, [847](#)
 - LD_DIAG_TX_PHY, [847](#)
 - LD_FAILED, [848](#)
 - LD_IN_PROGRESS, [848](#)
 - LD_N_AS_TIMEOUT, [848](#)
 - LD_N_CR_TIMEOUT, [848](#)
 - LD_NEGATIVE, [847](#)
 - LD_NEGATIVE_RESPONSE, [843](#)
 - LD_NO_CHECK_TIMEOUT, [848](#)
 - LD_NO_DATA, [846](#)
 - LD_NO_MSG, [848](#)
 - LD_NO_RESPONSE, [847](#)
 - LD_OVERWRITTEN, [847](#)
 - LD_POSITIVE_RESPONSE, [843](#)
 - LD_QUEUE_AVAILABLE, [846](#)
 - LD_QUEUE_EMPTY, [846](#)
 - LD_QUEUE_FULL, [846](#)
 - LD_RECEIVE_ERROR, [846](#)
 - LD_REQUEST_FINISHED, [849](#)
 - LD_SERVICE_BUSY, [849](#)
 - LD_SERVICE_ERROR, [849](#)
 - LD_SERVICE_IDLE, [849](#)
 - LD_SUCCESS, [847](#)
 - LD_TRANSFER_ERROR, [846](#)
 - LD_TRANSMIT_ERROR, [846](#)
 - LD_WRONG_SN, [848](#)
 - LIN_DIAGNOSTIC_CLASS_I, [846](#)
 - LIN_DIAGNOSTIC_CLASS_II, [846](#)
 - LIN_DIAGNOSTIC_CLASS_III, [846](#)
 - LIN_FRM_DIAG, [847](#)
 - LIN_FRM_EVTNT, [847](#)
 - LIN_FRM_SPRDC, [847](#)
 - LIN_FRM_UNCD, [847](#)
 - LIN_LLD_BUS_ACTIVITY_TIMEOUT, [848](#)
 - LIN_LLD_CHECKSUM_ERR, [848](#)
 - LIN_LLD_ERROR, [843](#)
 - LIN_LLD_FRAME_ERR, [848](#)
 - LIN_LLD_NODATA_TIMEOUT, [848](#)
 - LIN_LLD_OK, [843](#)
 - LIN_LLD_PID_ERR, [848](#)
 - LIN_LLD_PID_OK, [848](#)
 - LIN_LLD_READBACK_ERR, [848](#)

- LIN_LLD_RX_COMPLETED, 848
- LIN_LLD_TX_COMPLETED, 848
- LIN_MASTER, 843
- LIN_PROTOCOL_13, 848
- LIN_PROTOCOL_20, 848
- LIN_PROTOCOL_21, 848
- LIN_PROTOCOL_J2602, 848
- LIN_READ_USR_DEF_MAX, 843
- LIN_READ_USR_DEF_MIN, 843
- LIN_RES_PUB, 847
- LIN_RES_SUB, 847
- LIN_SCH_TBL_COLL_RESOLV, 849
- LIN_SCH_TBL_DIAG, 849
- LIN_SCH_TBL_GO_TO_SLEEP, 849
- LIN_SCH_TBL_NORM, 849
- LIN_SCH_TBL_NULL, 849
- LIN_SLAVE, 844
- LIN_TL_CALLBACK_HANDLER, 844
- ld_queue_status_t, 846
- ld_read_by_id_callout, 850
- lin_calc_max_header_timeout_cnt, 850
- lin_calc_max_res_timeout_cnt, 850
- lin_diagnostic_class_t, 846
- lin_diagnostic_state_t, 846
- lin_frame_response_t, 847
- lin_frame_type_t, 847
- lin_last_cfg_result_t, 847
- lin_llid_deinit, 850
- lin_llid_event_id_t, 847
- lin_llid_get_state, 850
- lin_llid_ignore_response, 851
- lin_llid_init, 851
- lin_llid_int_disable, 851
- lin_llid_int_enable, 851
- lin_llid_rx_response, 852
- lin_llid_set_low_power_mode, 852
- lin_llid_set_response, 852
- lin_llid_timeout_service, 852
- lin_llid_tx_header, 853
- lin_llid_tx_wake_up, 853
- lin_message_status_t, 848
- lin_message_timeout_type_t, 848
- lin_pid_resp_callback_handler, 853
- lin_process_parity, 854
- lin_protocol_handle_t, 848
- lin_sch_tbl_type_t, 848
- lin_service_status_t, 849
- lin_tl_callback_handler, 854
- lin_tl_callback_return_t, 849
- lin_tl_event_id_t, 849
- lin_tl_pdu_data_t, 845
- lin_tl_queue_t, 845
- PCI_RES_ASSIGN_FRAME_ID_RANGE, 844
- PCI_RES_READ_BY_IDENTIFY, 844
- PCI_RES_SAVE_CONFIGURATION, 844
- PCI_SAVE_CONFIGURATION, 844
- SERVICE_FAULT_MEMORY_CLEAR, 844
- SERVICE_ASSIGN_FRAME_ID, 844
- SERVICE_ASSIGN_FRAME_ID_RANGE, 844
- SERVICE_ASSIGN_NAD, 844
- SERVICE_CONDITIONAL_CHANGE_NAD, 844
- SERVICE_FAULT_MEMORY_READ, 845
- SERVICE_IO_CONTROL_BY_IDENTIFY, 845
- SERVICE_READ_BY_IDENTIFY, 845
- SERVICE_READ_DATA_BY_IDENTIFY, 845
- SERVICE_SAVE_CONFIGURATION, 845
- SERVICE_SESSION_CONTROL, 845
- SERVICE_WRITE_DATA_BY_IDENTIFY, 845
- TL_ACTION_ID_IGNORE, 849
- TL_ACTION_NONE, 849
- TL_ERROR, 849
- TL_HANDLER_INTERLEAVE_MODE, 849
- TL_MAKE_RES_DATA, 849
- TL_RECEIVE_MESSAGE, 849
- TL_RX_COMPLETED, 849
- TL_SLAVE_GET_ACTION, 849
- TL_TIMEOUT_SERVICE, 849
- TL_TX_COMPLETED, 849
- timerGetTimeIntervalCallbackArr, 855
- Low Power Inter-Integrated Circuit (LPI2C), 817
- Low Power Interrupt Timer (LPIT), 818
- Low Power Serial Peripheral Interface (LPSPi), 819
- Low Power Timer (LPTMR), 822
- Low Power Universal Asynchronous Receiver-Transmitter (LPUART), 823
- lowSideCtrl
 - uja113x_mtpnv_cfg_t, 247
- lpi2c_baud_rate_params_t, 747
 - baudRate, 748
- lpi2c_master_state_t, 748
- lpi2c_master_user_config_t, 745
 - baudRate, 746
 - callbackParam, 746
 - dmaChannel, 746
 - is10bitAddr, 746
 - masterCallback, 746
 - operatingMode, 746
 - slaveAddress, 746
 - transferType, 746
- lpi2c_mode_t
 - LPI2C Driver, 748
- lpi2c_slave_state_t, 748
- lpi2c_slave_user_config_t, 746
 - callbackParam, 747
 - dmaChannel, 747
 - is10bitAddr, 747
 - operatingMode, 747
 - slaveAddress, 747
 - slaveCallback, 747
 - slaveListening, 747
 - transferType, 747
- lpi2c_transfer_type_t
 - LPI2C Driver, 748
- lpit_period_units_t
 - LPIT Driver, 764
- lpit_timer_modes_t

- LPIT Driver, [764](#)
- lpit_trigger_source_t
 - LPIT Driver, [764](#)
- lpit_user_channel_config_t, [762](#)
 - chainChannel, [762](#)
 - enableReloadOnTrigger, [762](#)
 - enableStartOnTrigger, [762](#)
 - enableStopOnInterrupt, [763](#)
 - isInterruptEnabled, [763](#)
 - period, [763](#)
 - periodUnits, [763](#)
 - timerMode, [763](#)
 - triggerSelect, [763](#)
 - triggerSource, [763](#)
- lpit_user_config_t, [762](#)
 - enableRunInDebug, [762](#)
 - enableRunInDoze, [762](#)
- lpoClockConfig
 - pmc_config_t, [336](#)
 - sim_clock_config_t, [327](#)
- lpspi_clock_phase_t
 - LPSPi Driver, [781](#)
- lpspi_master_config_t, [775](#)
 - bitcount, [775](#)
 - bitsPerSec, [775](#)
 - callback, [776](#)
 - callbackParam, [776](#)
 - clkPhase, [776](#)
 - clkPolarity, [776](#)
 - isPcsContinuous, [776](#)
 - lpspiSrcClk, [776](#)
 - lsbFirst, [776](#)
 - pcsPolarity, [776](#)
 - rxDMACHannel, [776](#)
 - transferType, [776](#)
 - txDMACHannel, [776](#)
 - whichPcs, [777](#)
- lpspi_sck_polarity_t
 - LPSPi Driver, [781](#)
- lpspi_signal_polarity_t
 - LPSPi Driver, [781](#)
- lpspi_slave_config_t, [779](#)
 - bitcount, [780](#)
 - callback, [780](#)
 - callbackParam, [780](#)
 - clkPhase, [780](#)
 - clkPolarity, [780](#)
 - lsbFirst, [780](#)
 - pcsPolarity, [780](#)
 - rxDMACHannel, [780](#)
 - transferType, [780](#)
 - txDMACHannel, [780](#)
 - whichPcs, [781](#)
- lpspi_state_t, [777](#)
 - bitsPerFrame, [777](#)
 - bytesPerFrame, [777](#)
 - callback, [777](#)
 - callbackParam, [778](#)
 - dummy, [778](#)
 - fifoSize, [778](#)
 - isBlocking, [778](#)
 - isPcsContinuous, [778](#)
 - isTransferInProgress, [778](#)
 - lpspiSemaphore, [778](#)
 - lpspiSrcClk, [778](#)
 - lsb, [778](#)
 - rxBuff, [778](#)
 - rxCount, [778](#)
 - rxDMACHannel, [779](#)
 - rxFrameCnt, [779](#)
 - status, [779](#)
 - transferType, [779](#)
 - txBuff, [779](#)
 - txCount, [779](#)
 - txDMACHannel, [779](#)
 - txFrameCnt, [779](#)
- lpspi_transfer_type
 - LPSPi Driver, [781](#)
- lpspi_which_pcs_t
 - LPSPi Driver, [781](#)
- lpspiInstance
 - uja113x_driver_t, [186](#)
 - uja113x_drv_cfg_t, [181](#)
- lpspiIntace
 - drv_config_t, [1276](#)
- lpspiSemaphore
 - lpspi_state_t, [778](#)
- lpspiSrcClk
 - lpspi_master_config_t, [776](#)
 - lpspi_state_t, [778](#)
- lptmr_clocksource_t
 - LPTMR Driver, [795](#)
- lptmr_config_t, [794](#)
 - bypassPrescaler, [794](#)
 - clockSelect, [794](#)
 - compareValue, [794](#)
 - counterUnits, [794](#)
 - dmaRequest, [794](#)
 - freeRun, [794](#)
 - interruptEnable, [795](#)
 - pinPolarity, [795](#)
 - pinSelect, [795](#)
 - prescaler, [795](#)
 - workMode, [795](#)
- lptmr_counter_units_t
 - LPTMR Driver, [795](#)
- lptmr_pinpolarity_t
 - LPTMR Driver, [795](#)
- lptmr_pinselect_t
 - LPTMR Driver, [796](#)
- lptmr_prescaler_t
 - LPTMR Driver, [796](#)
- lptmr_workmode_t
 - LPTMR Driver, [796](#)
- lpuart_bit_count_per_char_t
 - LPUART Driver, [808](#)

- lpuart_parity_mode_t
 - LPUART Driver, [808](#)
- lpuart_state_t, [804](#)
 - bitCountPerChar, [805](#)
 - isRxBlocking, [805](#)
 - isRxBusy, [805](#)
 - isTxBlocking, [805](#)
 - isTxBusy, [805](#)
 - receiveStatus, [805](#)
 - rxBuff, [805](#)
 - rxCallback, [805](#)
 - rxCallbackParam, [806](#)
 - rxComplete, [806](#)
 - rxSize, [806](#)
 - transferType, [806](#)
 - transmitStatus, [806](#)
 - txBuff, [806](#)
 - txCallback, [806](#)
 - txCallbackParam, [806](#)
 - txComplete, [806](#)
 - txSize, [806](#)
- lpuart_stop_bit_count_t
 - LPUART Driver, [808](#)
- lpuart_transfer_type_t
 - LPUART Driver, [808](#)
- lpuart_user_config_t, [807](#)
 - baudRate, [807](#)
 - bitCountPerChar, [807](#)
 - parityMode, [807](#)
 - rxDMACHannel, [807](#)
 - stopBitCount, [807](#)
 - transferType, [807](#)
 - txDMACHannel, [807](#)
- lsb
 - lpspi_state_t, [778](#)
- lsbFirst
 - lpspi_master_config_t, [776](#)
 - lpspi_slave_config_t, [780](#)
- MAKE_PARITY
 - LIN Driver, [729](#)
- MASTER
 - LIN Driver, [729](#)
- MAX_PERIOD_COUNT
 - LPIT Driver, [763](#)
- MAX_PERIOD_COUNT_16_BIT
 - LPIT Driver, [763](#)
- MAX_PERIOD_COUNT_IN_DUAL_16BIT_MODE
 - LPIT Driver, [763](#)
- MC_ADDRESS
 - Register address map, [1029](#)
- MC_NORMAL
 - 01. Mode handling, [198](#)
- MC_SLEEP
 - 01. Mode handling, [198](#)
- MC_STANDBY
 - 01. Mode handling, [198](#)
- MEM0_ADDRESS
 - Register address map, [1029](#)
- MEM1_ADDRESS
 - Register address map, [1029](#)
- MEM2_ADDRESS
 - Register address map, [1029](#)
- MEM3_ADDRESS
 - Register address map, [1030](#)
- MINS_IN_A_HOUR
 - RTC Driver, [1005](#)
- MPU Driver, [856](#)
 - MPU_DATA_ACCESS_IN_SUPERVISOR_MODE, [867](#)
 - MPU_DATA_ACCESS_IN_USER_MODE, [867](#)
 - MPU_DRV_Deinit, [867](#)
 - MPU_DRV_EnableRegion, [867](#)
 - MPU_DRV_GetDefaultRegionConfig, [867](#)
 - MPU_DRV_GetDetailErrorAccessInfo, [867](#)
 - MPU_DRV_Init, [868](#)
 - MPU_DRV_SetMasterAccessRights, [868](#)
 - MPU_DRV_SetRegionAddr, [868](#)
 - MPU_DRV_SetRegionConfig, [869](#)
 - MPU_ERR_TYPE_READ, [866](#)
 - MPU_ERR_TYPE_WRITE, [866](#)
 - MPU_INSTRUCTION_ACCESS_IN_SUPERVISOR_MODE, [867](#)
 - MPU_INSTRUCTION_ACCESS_IN_USER_MODE, [867](#)
 - MPU_NONE, [866](#)
 - MPU_R, [866](#)
 - MPU_RW, [866](#)
 - MPU_SUPERVISOR_RW_USER_NONE, [866](#)
 - MPU_SUPERVISOR_RW_USER_R, [866](#)
 - MPU_SUPERVISOR_RW_USER_RW, [866](#)
 - MPU_SUPERVISOR_RW_USER_RWX, [866](#)
 - MPU_SUPERVISOR_RW_USER_RX, [866](#)
 - MPU_SUPERVISOR_RW_USER_W, [866](#)
 - MPU_SUPERVISOR_RW_USER_WX, [866](#)
 - MPU_SUPERVISOR_RW_USER_X, [866](#)
 - MPU_SUPERVISOR_RWX_USER_NONE, [865](#)
 - MPU_SUPERVISOR_RWX_USER_R, [866](#)
 - MPU_SUPERVISOR_RWX_USER_RW, [866](#)
 - MPU_SUPERVISOR_RWX_USER_RWX, [866](#)
 - MPU_SUPERVISOR_RWX_USER_RX, [866](#)
 - MPU_SUPERVISOR_RWX_USER_W, [865](#)
 - MPU_SUPERVISOR_RWX_USER_WX, [865](#)
 - MPU_SUPERVISOR_RWX_USER_X, [865](#)
 - MPU_SUPERVISOR_RX_USER_NONE, [866](#)
 - MPU_SUPERVISOR_RX_USER_R, [866](#)
 - MPU_SUPERVISOR_RX_USER_RW, [866](#)
 - MPU_SUPERVISOR_RX_USER_RWX, [866](#)
 - MPU_SUPERVISOR_RX_USER_RX, [866](#)
 - MPU_SUPERVISOR_RX_USER_W, [866](#)
 - MPU_SUPERVISOR_RX_USER_WX, [866](#)
 - MPU_SUPERVISOR_RX_USER_X, [866](#)
 - MPU_SUPERVISOR_USER_NONE, [866](#)
 - MPU_SUPERVISOR_USER_R, [866](#)
 - MPU_SUPERVISOR_USER_RW, [866](#)
 - MPU_SUPERVISOR_USER_RWX, [866](#)
 - MPU_SUPERVISOR_USER_RX, [866](#)

- MPU_SUPERVISOR_USER_W, [866](#)
- MPU_SUPERVISOR_USER_WX, [866](#)
- MPU_SUPERVISOR_USER_X, [866](#)
- MPU_W, [866](#)
- mpu_access_rights_t, [863](#)
- mpu_err_access_type_t, [866](#)
- mpu_err_attributes_t, [866](#)
- MPU_PAL, [870](#)
 - MPU_Deinit, [878](#)
 - MPU_ERROR_SUPERVISOR_MODE_DATA_ACCESS, [878](#)
 - MPU_ERROR_SUPERVISOR_MODE_INSTRUCTION_ACCESS, [878](#)
 - MPU_ERROR_TYPE_READ, [877](#)
 - MPU_ERROR_TYPE_WRITE, [877](#)
 - MPU_ERROR_USER_MODE_DATA_ACCESS, [878](#)
 - MPU_ERROR_USER_MODE_INSTRUCTION_ACCESS, [878](#)
 - MPU_EnableRegion, [878](#)
 - MPU_GetDefaultRegionConfig, [879](#)
 - MPU_GetError, [879](#)
 - MPU_Init, [879](#)
 - MPU_UpdateRegion, [880](#)
 - mpu_access_permission_t, [875](#)
 - mpu_error_access_type_t, [877](#)
 - mpu_error_attributes_t, [877](#)
 - mpu_inst_type_t, [878](#)
- MPU_DATA_ACCESS_IN_SUPERVISOR_MODE
 - MPU Driver, [867](#)
- MPU_DATA_ACCESS_IN_USER_MODE
 - MPU Driver, [867](#)
- MPU_DRV_Deinit
 - MPU Driver, [867](#)
- MPU_DRV_EnableRegion
 - MPU Driver, [867](#)
- MPU_DRV_GetDefaultRegionConfig
 - MPU Driver, [867](#)
- MPU_DRV_GetDetailErrorAccessInfo
 - MPU Driver, [867](#)
- MPU_DRV_Init
 - MPU Driver, [868](#)
- MPU_DRV_SetMasterAccessRights
 - MPU Driver, [868](#)
- MPU_DRV_SetRegionAddr
 - MPU Driver, [868](#)
- MPU_DRV_SetRegionConfig
 - MPU Driver, [869](#)
- MPU_Deinit
 - MPU PAL, [878](#)
- MPU_ERR_TYPE_READ
 - MPU Driver, [866](#)
- MPU_ERR_TYPE_WRITE
 - MPU Driver, [866](#)
- MPU_ERROR_SUPERVISOR_MODE_DATA_ACCESS
 - MPU PAL, [878](#)
- MPU_ERROR_SUPERVISOR_MODE_INSTRUCTION_ACCESS
 - MPU PAL, [878](#)
- MPU_ENABLE_REGION
 - MPU PAL, [878](#)
- MPU_GET_DEFAULT_REGION_CONFIG
 - MPU PAL, [879](#)
- MPU_GET_ERROR
 - MPU PAL, [879](#)
- MPU_INSTRUCTION_ACCESS_IN_SUPERVISOR_MODE
 - MPU Driver, [867](#)
- MPU_INSTRUCTION_ACCESS_IN_USER_MODE
 - MPU Driver, [867](#)
- MPU_INIT
 - MPU PAL, [879](#)
- MPU_NONE
 - MPU Driver, [866](#)
- MPU_R
 - MPU Driver, [866](#)
- MPU_RW
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RW_USER_NONE
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RW_USER_R
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RW_USER_RW
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RW_USER_RWX
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RW_USER_RX
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RW_USER_W
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RW_USER_WX
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RW_USER_X
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RWX_USER_NONE
 - MPU Driver, [865](#)
- MPU_SUPERVISOR_RWX_USER_R
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RWX_USER_RW
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RWX_USER_RWX
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RWX_USER_RX
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RWX_USER_W
 - MPU Driver, [866](#)

- MPU Driver, [865](#)
- MPU_SUPERVISOR_RWX_USER_WX
 - MPU Driver, [865](#)
- MPU_SUPERVISOR_RWX_USER_X
 - MPU Driver, [865](#)
- MPU_SUPERVISOR_RX_USER_NONE
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RX_USER_R
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RX_USER_RW
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RX_USER_RWX
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RX_USER_RX
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RX_USER_W
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RX_USER_WX
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_RX_USER_X
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_USER_NONE
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_USER_R
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_USER_RW
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_USER_RWX
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_USER_RX
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_USER_W
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_USER_WX
 - MPU Driver, [866](#)
- MPU_SUPERVISOR_USER_X
 - MPU Driver, [866](#)
- MPU_UpdateRegion
 - MPU PAL, [880](#)
- MPU_W
 - MPU Driver, [866](#)
- MSBCS_ADDRESS
 - Register address map, [1030](#)
- MTPNVCRCC_ADDRESS
 - Register address map, [1030](#)
- MTPNVS_ADDRESS
 - Register address map, [1030](#)
- MULTIPLY_BY_ONE
 - Clock Manager Driver, [344](#)
- MULTIPLY_BY_TWO
 - Clock Manager Driver, [344](#)
- MX25L6433F Serial Flash Driver, [881](#)
 - FLASH_MX25L6433F_DRV_Deinit, [886](#)
 - FLASH_MX25L6433F_DRV_EnterDPD, [887](#)
 - FLASH_MX25L6433F_DRV_EnterOTP, [887](#)
 - FLASH_MX25L6433F_DRV_Erase32K, [887](#)
 - FLASH_MX25L6433F_DRV_Erase4K, [887](#)
 - FLASH_MX25L6433F_DRV_Erase64K, [888](#)
 - FLASH_MX25L6433F_DRV_EraseAll, [888](#)
 - FLASH_MX25L6433F_DRV_EraseVerify, [888](#)
 - FLASH_MX25L6433F_DRV_ExitDPD, [888](#)
 - FLASH_MX25L6433F_DRV_ExitOTP, [889](#)
 - FLASH_MX25L6433F_DRV_GetDefaultConfig, [889](#)
 - FLASH_MX25L6433F_DRV_GetProtection, [889](#)
 - FLASH_MX25L6433F_DRV_GetSecureLock, [889](#)
 - FLASH_MX25L6433F_DRV_GetStatus, [890](#)
 - FLASH_MX25L6433F_DRV_Init, [890](#)
 - FLASH_MX25L6433F_DRV_Program, [890](#)
 - FLASH_MX25L6433F_DRV_ProgramVerify, [891](#)
 - FLASH_MX25L6433F_DRV_Read, [891](#)
 - FLASH_MX25L6433F_DRV_Reset, [891](#)
 - FLASH_MX25L6433F_DRV_Resume, [891](#)
 - FLASH_MX25L6433F_DRV_STRENGTH_HIGH, [886](#)
 - FLASH_MX25L6433F_DRV_STRENGTH_LOW, [886](#)
 - FLASH_MX25L6433F_DRV_SetProtection, [892](#)
 - FLASH_MX25L6433F_DRV_SetSecureLock, [892](#)
 - FLASH_MX25L6433F_DRV_Suspend, [892](#)
 - FLASH_MX25L6433F_PROT_DIR_BOTTOM, [886](#)
 - FLASH_MX25L6433F_PROT_DIR_TOP, [886](#)
 - FLASH_MX25L6433F_PROT_SIZE_0, [886](#)
 - FLASH_MX25L6433F_PROT_SIZE_128K, [886](#)
 - FLASH_MX25L6433F_PROT_SIZE_1M, [886](#)
 - FLASH_MX25L6433F_PROT_SIZE_256K, [886](#)
 - FLASH_MX25L6433F_PROT_SIZE_2M, [886](#)
 - FLASH_MX25L6433F_PROT_SIZE_4M, [886](#)
 - FLASH_MX25L6433F_PROT_SIZE_512K, [886](#)
 - FLASH_MX25L6433F_PROT_SIZE_64K, [886](#)
 - FLASH_MX25L6433F_PROT_SIZE_8M, [886](#)
 - flash_mx25l6433f_drv_strength_t, [886](#)
 - flash_mx25l6433f_prot_dir_t, [886](#)
 - flash_mx25l6433f_prot_size_t, [886](#)
- mac
 - csec_state_t, [300](#)
- mac_algorithm
 - CipherSpecs, [1259](#)
- macLen
 - csec_state_t, [300](#)
- macType
 - Hmac, [1288](#)
 - WOLFSSL_EVP_MD_CTX, [1363](#)
- macWritten
 - csec_state_t, [301](#)
- mainChannelPolarity
 - ftm_combined_ch_param_t, [647](#)
- mainChannelSafeState
 - ftm_combined_ch_param_t, [647](#)
- mainFunction
 - Generic PHY, [666](#)
 - phy_driver_t, [949](#)
- mainS
 - sbc_status_group_t, [1190](#)
- major
 - ProtocolVersion, [1308](#)

- majorLoopChnLinkEnable
 - edma_loop_transfer_config_t, [418](#)
- majorLoopChnLinkNumber
 - edma_loop_transfer_config_t, [418](#)
- majorLoopIterationCount
 - edma_loop_transfer_config_t, [418](#)
- manualDelay
 - phy_config_t, [947](#)
- mask
 - sbc_can_conf_t, [1181](#)
- maskRegSync
 - ftm_pwm_sync_t, [589](#)
- master
 - mpu_access_err_info_t, [862](#)
 - mpu_error_info_t, [873](#)
- master_data_buffer
 - lin_master_data_t, [840](#)
- master_ifc_handle
 - lin_protocol_user_config_t, [838](#)
- masterAccRight
 - mpu_region_config_t, [874](#)
 - mpu_user_config_t, [863](#)
- masterCallback
 - lpi2c_master_user_config_t, [746](#)
- MasterClkSrc
 - sai_user_config_t, [1040](#)
- masterCtx
 - Rabbit, [1314](#)
- masterNum
 - mpu_master_access_permission_t, [874](#)
 - mpu_master_access_right_t, [862](#)
- masterSecret
 - Arrays, [1249](#)
 - WOLFSSL_SESSION, [1369](#)
- masters
 - qspi_ahb_config_t, [1310](#)
- max_idle_timeout_cnt
 - lin_protocol_user_config_t, [839](#)
- max_message_length
 - lin_protocol_user_config_t, [839](#)
- max_num_mb
 - flexcan_user_config_t, [517](#)
- maxBuffNum
 - can_user_config_t, [389](#)
- maxCountValue
 - extension_ftm_for_oc_t, [923](#)
 - ftm_output_cmp_param_t, [633](#)
- maxFrameLen
 - enet_config_t, [448](#)
- maxIdx
 - DecodedCert, [1267](#)
- maxLoadingPoint
 - ftm_pwm_sync_t, [589](#)
- maxVal
 - ftm_quad_decode_config_t, [656](#)
- mb_message
 - flexcan_mb_handle_t, [513](#)
- mbSema
 - flexcan_mb_handle_t, [513](#)
- mbs
 - FlexCANState, [514](#)
- mcSbcMode
 - uja113x_init_cfg_t, [184](#)
- Md4, [1293](#)
 - buffLen, [1293](#)
 - buffer, [1293](#)
 - digest, [1293](#)
 - hiLen, [1293](#)
 - loLen, [1293](#)
- Md5, [1293](#)
 - buffLen, [1294](#)
 - buffer, [1294](#)
 - digest, [1294](#)
 - heap, [1294](#)
 - hiLen, [1294](#)
 - loLen, [1294](#)
- md5
 - Hash, [1285](#)
 - Hashes, [1286](#)
 - WOLFSSL_Hasher, [1364](#)
 - wc_HashAlg, [1332](#)
- mdiToMiiMax
 - phy_delay_t, [945](#)
- mdiToMiiMin
 - phy_delay_t, [945](#)
- measurementResults
 - ftm_state_t, [588](#)
- measurementType
 - ftm_input_ch_param_t, [622](#)
- mem
 - WOLFSSL_BIO, [1345](#)
- memLen
 - WOLFSSL_BIO, [1345](#)
- memSize
 - qspi_user_config_t, [1313](#)
- Memory Protection Unit (MPU), [893](#)
- Memory Protection Unit Peripheral Abstraction Layer (↔ MPU PAL), [895](#)
- memory0
 - uja113x_init_cfg_t, [184](#)
- memory1
 - uja113x_init_cfg_t, [184](#)
- memory2
 - uja113x_init_cfg_t, [185](#)
- memory3
 - uja113x_init_cfg_t, [185](#)
- message_seq
 - DtlsHandShakeHeader, [1279](#)
- method
 - callback_functions, [1255](#)
 - WOLFSSL_CTX, [1353](#)
- miiDuplex
 - enet_config_t, [448](#)
- miiMode
 - enet_config_t, [448](#)
- miiSpeed

- enet_config_t, 448
- miiToMdiMax
 - phy_delay_t, 945
- miiToMdiMin
 - phy_delay_t, 946
- minDhKeySz
 - Options, 1303
 - WOLFSSL_CTX, 1353
- minDowngrade
 - Options, 1303
 - WOLFSSL_CTX, 1353
- minLoadingPoint
 - ftm_pwm_sync_t, 589
- minRsaKeySz
 - Options, 1303
 - WOLFSSL_CERT_MANAGER, 1348
 - WOLFSSL_CTX, 1353
- minor
 - ProtocolVersion, 1309
- minorByteTransferCount
 - edma_transfer_config_t, 420
- minorLoopChnLinkEnable
 - edma_loop_transfer_config_t, 419
- minorLoopChnLinkNumber
 - edma_loop_transfer_config_t, 419
- minorLoopOffset
 - edma_loop_transfer_config_t, 419
- minutes
 - rtc_timedate_t, 1001
- misoPin
 - extension_flexio_for_spi_t, 1107
 - flexio_spi_master_user_config_t, 562
 - flexio_spi_slave_user_config_t, 564
- mode
 - can_user_config_t, 389
 - cmp_comparator_t, 368
 - ftm_output_cmp_param_t, 633
 - ftm_pwm_param_t, 648
 - ftm_quad_decode_config_t, 656
 - ftm_timer_param_t, 629
 - i2s_user_config_t, 677
 - sbc_int_config_t, 1182
- modeControl
 - sbc_wtdog_ctr_t, 1175
- module_clk_config_t, 337
 - div, 337
 - gating, 337
 - mul, 337
 - source, 337
- monitorMode
 - scg_sosc_config_t, 329
 - scg_spill_config_t, 332
- monitors
 - WOLFSSL_CRL, 1350
- month
 - rtc_timedate_t, 1001
- mosiPin
 - extension_flexio_for_spi_t, 1107
- flexio_spi_master_user_config_t, 562
- flexio_spi_slave_user_config_t, 564
- mp_int, 1294
 - alloc, 1295
 - dp, 1295
 - sign, 1295
 - used, 1295
- mpu_access_err_info_t, 861
 - accessCtr, 862
 - accessType, 862
 - addr, 862
 - attributes, 862
 - master, 862
- mpu_access_permission_t
 - MPU PAL, 875
- mpu_access_rights_t
 - MPU Driver, 863
- mpu_err_access_type_t
 - MPU Driver, 866
- mpu_err_attributes_t
 - MPU Driver, 866
- mpu_error_access_type_t
 - MPU PAL, 877
- mpu_error_attributes_t
 - MPU PAL, 877
- mpu_error_info_t, 873
 - accessCtr, 873
 - accessType, 873
 - addr, 873
 - attributes, 873
 - master, 873
 - overflow, 873
 - processId, 873
- mpu_inst_type_t
 - MPU PAL, 878
- mpu_instance_t, 1295
 - instIdx, 1295
 - instType, 1295
- mpu_master_access_permission_t, 873
 - accessRight, 874
 - masterNum, 874
- mpu_master_access_right_t, 862
 - accessRight, 862
 - masterNum, 862
- mpu_region_config_t, 874
 - endAddr, 874
 - extension, 874
 - masterAccRight, 874
 - processIdEnable, 874
 - processIdMask, 875
 - processIdentifier, 875
 - startAddr, 875
- mpu_user_config_t, 862
 - endAddr, 863
 - masterAccRight, 863
 - startAddr, 863
- MsbFirst
 - sai_user_config_t, 1040

- msg
 - DtlsMsg, [1279](#)
 - wolfssl_TI_Hash, [1372](#)
- msg_id_type
 - flexcan_data_info_t, [515](#)
- msgId
 - flexcan_msgbuff_t, [513](#)
- msgLen
 - csec_state_t, [301](#)
- MsgsReceived, [1296](#)
 - got_certificate, [1296](#)
 - got_certificate_request, [1296](#)
 - got_certificate_status, [1296](#)
 - got_certificate_verify, [1296](#)
 - got_change_cipher, [1296](#)
 - got_client_hello, [1296](#)
 - got_client_key_exchange, [1296](#)
 - got_encrypted_extensions, [1297](#)
 - got_end_of_early_data, [1297](#)
 - got_finished, [1297](#)
 - got_hello_request, [1297](#)
 - got_hello_retry_request, [1297](#)
 - got_hello_verify_request, [1297](#)
 - got_key_update, [1297](#)
 - got_server_hello, [1297](#)
 - got_server_hello_done, [1297](#)
 - got_server_key_exchange, [1297](#)
 - got_session_ticket, [1297](#)
- msgsReceived
 - WOLFSSL, [1338](#)
- mul
 - clock_source_config_t, [338](#)
 - module_clk_config_t, [337](#)
- mult
 - scg_spill_config_t, [332](#)
- mux
 - cmp_module_t, [371](#)
 - pin_settings_config_t, [959](#)
- MuxMode
 - sai_user_config_t, [1040](#)
- n
 - RsaKey, [1317](#)
 - WOLFSSL_RSA, [1368](#)
- N_As_timeout
 - lin_node_attribute_t, [830](#)
- N_Cr_timeout
 - lin_node_attribute_t, [830](#)
- NBYTES
 - edma_software_tcd_t, [422](#)
- NEGATIVE
 - Common Transport Layer API, [359](#)
- nMaxCountValue
 - ftm_input_param_t, [623](#)
- nNumChannels
 - ftm_input_param_t, [623](#)
 - ic_config_t, [688](#)
 - oc_config_t, [923](#)
- nNumCombinedPwmChannels
 - ftm_pwm_param_t, [648](#)
- nNumIndependentPwmChannels
 - ftm_pwm_param_t, [648](#)
- nNumOutputChannels
 - ftm_output_cmp_param_t, [634](#)
- NO_MODE
 - Clock Manager Driver, [344](#)
- nTimer
 - uja113x_timsc_cfg_t, [236](#)
- NULL_CALLBACK
 - Flash Memory (Flash), [491](#)
- NUMBER_OF_TCLK_INPUTS
 - Clock Manager Driver, [342](#)
- NWP_PERIOD_1024
 - 02. Watchdog, [215](#)
- NWP_PERIOD_128
 - 02. Watchdog, [215](#)
- NWP_PERIOD_16
 - 02. Watchdog, [215](#)
- NWP_PERIOD_256
 - 02. Watchdog, [215](#)
- NWP_PERIOD_32
 - 02. Watchdog, [215](#)
- NWP_PERIOD_4096
 - 02. Watchdog, [215](#)
- NWP_PERIOD_64
 - 02. Watchdog, [215](#)
- NWP_PERIOD_8
 - 02. Watchdog, [215](#)
- name
 - Base_entry, [1251](#)
 - DNS_entry, [1275](#)
 - EncryptedInfo, [1281](#)
 - ReadDirCtx, [1315](#)
 - Signer, [1323](#)
 - WOLFSSL_STACK, [1371](#)
 - WOLFSSL_X509_NAME, [1376](#)
- nameLen
 - Signer, [1324](#)
- nameSz
 - Base_entry, [1251](#)
- neg
 - WOLFSSL_BIGNUM, [1344](#)
- negativeInputMux
 - cmp_anmux_t, [368](#)
- negativePortMux
 - cmp_anmux_t, [368](#)
- negotiationError
 - handShakeInfo_st, [1285](#)
- next
 - Base_entry, [1251](#)
 - CRL_Entry, [1261](#)
 - DNS_entry, [1275](#)
 - DtlsFrag, [1278](#)
 - DtlsMsg, [1280](#)
 - OcspEntry, [1299](#)
 - Signer, [1324](#)
 - WC_DerCertList, [1332](#)

- WOLF_EVENT, [1335](#)
- WOLFSSL_BIO, [1345](#)
- WOLFSSL_STACK, [1371](#)
- next_transmit_tick
 - lin_protocol_state_t, [842](#)
- nextDate
 - CRL_Entry, [1261](#)
- nextDateFormat
 - CRL_Entry, [1261](#)
- nextEpoch
 - WOLFSSL_DTLS_PEERSEQ, [1358](#)
- nextIdx
 - ClientRow, [1260](#)
 - SessionRow, [1320](#)
- nextSeq_hi
 - WOLFSSL_DTLS_PEERSEQ, [1358](#)
- nextSeq_lo
 - WOLFSSL_DTLS_PEERSEQ, [1358](#)
- nms
 - sbc_main_status_t, [1184](#)
- noCRC
 - enet_tx_options_t, [451](#)
- noInt
 - enet_tx_options_t, [451](#)
- noPskDheKe
 - Options, [1303](#)
- Node configuration, [900](#), [905](#)
 - ld_assign_NAD, [900](#)
 - ld_assign_NAD_j2602, [905](#)
 - ld_assign_frame_id_range, [900](#)
 - ld_check_response, [902](#)
 - ld_check_response_j2602, [905](#)
 - ld_conditional_change_NAD, [902](#)
 - ld_is_ready, [902](#)
 - ld_is_ready_j2602, [905](#)
 - ld_read_configuration, [903](#)
 - ld_reconfig_msg_ID, [906](#)
 - ld_save_configuration, [903](#)
 - ld_set_configuration, [903](#)
- Node identification, [907](#)
 - ld_read_by_id, [907](#)
- node_depth
 - __blake2b_param, [1243](#)
 - __blake2s_param, [1245](#)
- node_offset
 - __blake2b_param, [1243](#)
 - __blake2s_param, [1245](#)
- nodeFunction
 - lin_user_config_t, [726](#)
- nomWtdPeriod
 - uja113x_wtdc_cfg_t, [214](#)
- nominalBitrate
 - can_user_config_t, [389](#)
- nominalPeriod
 - sbc_wtdog_ctr_t, [1175](#)
- nonInitRegs
 - fs45_drv_config_t, [1062](#)
- nonInitRegsCount
 - fs45_drv_config_t, [1062](#)
- nonSupervisorAccessEnable
 - rtc_init_config_t, [1002](#)
- notAfter
 - WOLFSSL_X509, [1374](#)
- notAfterSz
 - WOLFSSL_X509, [1374](#)
- notBefore
 - WOLFSSL_X509, [1374](#)
- notBeforeSz
 - WOLFSSL_X509, [1374](#)
- Notification, [908](#)
- notifyType
 - clock_notify_struct_t, [339](#)
 - power_manager_notify_struct_t, [968](#)
- num
 - WOLFSSL_STACK, [1371](#)
- num_frame_have_esignal
 - lin_node_attribute_t, [830](#)
- num_id_filters
 - flexcan_user_config_t, [517](#)
- num_of_associated_uncond_frames
 - lin_associate_frame_t, [832](#)
- num_of_fault_state_signal
 - lin_node_attribute_t, [830](#)
- num_of_pdu
 - lin_tl_descriptor_t, [836](#)
- num_of_processed_frame
 - lin_protocol_state_t, [842](#)
- num_of_schedules
 - lin_protocol_user_config_t, [839](#)
- num_slots
 - lin_schedule_t, [833](#)
- numChan
 - timer_config_t, [1159](#)
- numChannels
 - adc_group_config_t, [274](#)
- numGroups
 - adc_config_t, [275](#)
- numIdFilters
 - extension_flexcan_rx_fifo_t, [390](#)
- numInOutMappingConfigs
 - trgmux_user_config_t, [1149](#)
- numOfClassicPID
 - lin_user_config_t, [726](#)
- numOfRecordReqMaintain
 - Flash Memory (Flash), [501](#)
- numSetsResultBuffer
 - adc_group_config_t, [274](#)
- number_of_configurable_frames
 - lin_protocol_user_config_t, [839](#)
- number_support_sid
 - lin_node_attribute_t, [830](#)
- numberOfPwmChannels
 - pwm_global_config_t, [990](#)
- numberOfRepeats
 - rtc_alarm_config_t, [1003](#)
- numberPackets

- handShakeInfo_st, [1285](#)
- timeoutInfo_st, [1330](#)
- nvmps
 - sbc_mtpnv_stat_t, [1190](#)
- OC_ABSOLUTE_VALUE
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [924](#)
- OC_CLEAR_ON_MATCH
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [923](#)
- OC_DISABLE_OUTPUT
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [923](#)
- OC_Deinit
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [924](#)
- OC_DisableNotification
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [924](#)
- OC_EnableNotification
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [924](#)
- OC_Init
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [924](#)
- OC_RELATIVE_VALUE
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [924](#)
- OC_SET_ON_MATCH
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [923](#)
- OC_SetCompareValue
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [925](#)
- OC_SetOutputAction
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [925](#)
- OC_SetOutputState
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [926](#)
- OC_StartChannel
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [926](#)
- OC_StopChannel
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [926](#)
- OC_TOGGLE_ON_MATCH
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [923](#)
- oldx
 - DecodedName, [1271](#)
- oLen
 - DecodedName, [1271](#)
- OS Interface (OSIF), [909](#)
 - OSIF_GetMilliseconds, [911](#)
 - OSIF_MutexCreate, [911](#)
 - OSIF_MutexDestroy, [913](#)
 - OSIF_MutexLock, [913](#)
 - OSIF_MutexUnlock, [913](#)
 - OSIF_SemaCreate, [913](#)
 - OSIF_SemaDestroy, [915](#)
 - OSIF_SemaPost, [915](#)
 - OSIF_SemaWait, [915](#)
 - OSIF_TimeDelay, [915](#)
 - OSIF_WAIT_FOREVER, [911](#)
- OS_Seed, [1305](#)
 - fd, [1305](#)
- OSIF_GetMilliseconds
 - OS Interface (OSIF), [911](#)
- OSIF_MutexCreate
 - OS Interface (OSIF), [911](#)
- OSIF_MutexDestroy
 - OS Interface (OSIF), [913](#)
- OSIF_MutexLock
 - OS Interface (OSIF), [913](#)
- OSIF_MutexUnlock
 - OS Interface (OSIF), [913](#)
- OSIF_SemaCreate
 - OS Interface (OSIF), [913](#)
- OSIF_SemaDestroy
 - OS Interface (OSIF), [915](#)
- OSIF_SemaPost
 - OS Interface (OSIF), [915](#)
- OSIF_SemaWait
 - OS Interface (OSIF), [915](#)
- OSIF_TimeDelay
 - OS Interface (OSIF), [915](#)
- OSIF_WAIT_FOREVER
 - OS Interface (OSIF), [911](#)
- OTWIE_DISABLE
 - System interrupt enable configuration options (0x04), [1135](#)
- OTWIE_ENABLE
 - System interrupt enable configuration options (0x04), [1135](#)
- OUI
 - TJA110x PHY, [1143](#)
- OVERRUN
 - Common Core API., [355](#)
- obj
 - WOLFSSL_ASN1_OBJECT, [1342](#)
 - WOLFSSL_STACK, [1372](#)
- objSz
 - WOLFSSL_ASN1_OBJECT, [1342](#)
- oc_config_t, [922](#)
 - extension, [922](#)
 - nNumChannels, [923](#)
 - outputChConfig, [923](#)
- oc_instance_t, [1297](#)
 - instIdx, [1298](#)
 - instType, [1298](#)
- oc_option_mode_t
 - Output Compare - Peripheral Abstraction Layer (↔ OC PAL), [923](#)
- oc_option_update_t

- Output Compare - Peripheral Abstraction Layer (↔ OC PAL), 923
- oc_output_ch_param_t, 921
 - chMode, 922
 - channelCallbackParams, 922
 - channelCallbacks, 922
 - channelExtension, 922
 - comparedValue, 922
 - hwChannelId, 922
- oc_pal_state_t, 1298
- ocsp
 - WOLFSSL_CERT_MANAGER, 1348
- ocspCheckAll
 - WOLFSSL_CERT_MANAGER, 1348
- ocspEnabled
 - WOLFSSL_CERT_MANAGER, 1348
- OcspEntry, 1298
 - issuerHash, 1299
 - issuerKeyHash, 1299
 - next, 1299
 - status, 1299
 - totalStatus, 1299
- ocspIOCb
 - WOLFSSL_CERT_MANAGER, 1348
- ocspIOCtx
 - WOLFSSL_CERT_MANAGER, 1348
- ocspList
 - WOLFSSL_OCSP, 1366
- ocspLock
 - WOLFSSL_OCSP, 1366
- ocspOverrideURL
 - WOLFSSL_CERT_MANAGER, 1348
- ocspRespFreeCb
 - WOLFSSL_CERT_MANAGER, 1348
- ocspSendNonce
 - WOLFSSL_CERT_MANAGER, 1348
- ocspStaplingEnabled
 - WOLFSSL_CERT_MANAGER, 1348
- ocspUseOverrideURL
 - WOLFSSL_CERT_MANAGER, 1348
- offset
 - bufferStatic, 1254
- on_result
 - callback_functions, 1256
- opMode
 - wdg_config_t, 1225
 - wdog_user_config_t, 1233
- opad
 - Hmac, 1288
- operatingMode
 - i2c_master_t, 697
 - i2c_slave_t, 698
 - lpi2c_master_user_config_t, 746
 - lpi2c_slave_user_config_t, 747
- Options, 1299
 - acceptState, 1300
 - alertCount, 1300
 - asyncState, 1301
 - buildMsgState, 1301
 - certOnly, 1301
 - cipherSuite, 1301
 - cipherSuite0, 1301
 - client_psk_cb, 1301
 - clientState, 1301
 - closeNotify, 1301
 - connReset, 1301
 - connectState, 1301
 - dhKeySz, 1301
 - downgrade, 1301
 - dtls, 1301
 - failNoCert, 1301
 - failNoCertxPSK, 1301
 - groupMessages, 1302
 - handShakeDone, 1302
 - handShakeState, 1302
 - haveDH, 1302
 - haveECC, 1302
 - haveECDSAsig, 1302
 - haveEMS, 1302
 - haveNTRU, 1302
 - havePSK, 1302
 - havePeerCert, 1302
 - havePeerVerify, 1302
 - haveQSH, 1302
 - haveRSA, 1302
 - haveSessionId, 1302
 - haveStaticECC, 1302
 - isClosed, 1303
 - keepResources, 1303
 - minDhKeySz, 1303
 - minDowngrade, 1303
 - minRsaKeySz, 1303
 - noPskDheKe, 1303
 - partialWrite, 1303
 - processReply, 1303
 - quietShutdown, 1303
 - resuming, 1303
 - saveArrays, 1303
 - sendAlertState, 1303
 - sendVerify, 1303
 - sentNotify, 1303
 - server_psk_cb, 1303
 - serverState, 1304
 - sessionCacheFlushOff, 1304
 - sessionCacheOff, 1304
 - side, 1304
 - tls, 1304
 - tls1_1, 1304
 - tls1_3, 1304
 - useClientOrder, 1304
 - usingAnon_cipher, 1304
 - usingCompression, 1304
 - usingNonblock, 1304
 - usingPSK_cipher, 1304
 - verifyNone, 1304
 - verifyPeer, 1304

- weOwnRng, [1304](#)
- options
 - WOLFSSL, [1338](#)
- otw
 - sbc_sys_evt_stat_t, [1187](#)
- otws
 - sbc_main_status_t, [1184](#)
- ouldx
 - DecodedName, [1271](#)
- ouLen
 - DecodedName, [1271](#)
- oui
 - phy_id_t, [945](#)
- out
 - SignatureCtx, [1322](#)
- outRegSync
 - ftm_pwm_sync_t, [590](#)
- output
 - DckeArgs, [1263](#)
 - DcvArgs, [1264](#)
 - DskeArgs, [1277](#)
 - SckeArgs, [1318](#)
 - ScvArgs, [1319](#)
 - SskeArgs, [1326](#)
- Output Compare - Peripheral Abstraction Layer (OC P↔AL), [918](#)
 - OC_ABSOLUTE_VALUE, [924](#)
 - OC_CLEAR_ON_MATCH, [923](#)
 - OC_DISABLE_OUTPUT, [923](#)
 - OC_Deinit, [924](#)
 - OC_DisableNotification, [924](#)
 - OC_EnableNotification, [924](#)
 - OC_Init, [924](#)
 - OC_RELATIVE_VALUE, [924](#)
 - OC_SET_ON_MATCH, [923](#)
 - OC_SetCompareValue, [925](#)
 - OC_SetOutputAction, [925](#)
 - OC_SetOutputState, [926](#)
 - OC_StartChannel, [926](#)
 - OC_StopChannel, [926](#)
 - OC_TOGGLE_ON_MATCH, [923](#)
 - oc_option_mode_t, [923](#)
 - oc_option_update_t, [923](#)
- outputBuff
 - csec_state_t, [301](#)
- outputBuffer
 - Buffers, [1252](#)
- outputChConfig
 - oc_config_t, [923](#)
- outputChannelConfig
 - ftm_output_cmp_param_t, [634](#)
- outputDiv1
 - clock_source_config_t, [338](#)
- outputDiv2
 - clock_source_config_t, [339](#)
- outputDriverStrength
 - flash_mx25l6433f_user_config_t, [885](#)
- outputInterruptTrigger
 - cmp_comparator_t, [368](#)
- outputSelect
 - cmp_comparator_t, [368](#)
- overflowDirection
 - ftm_quad_decoder_state_t, [657](#)
- overflowFlag
 - ftm_quad_decoder_state_t, [657](#)
- overflowIntEnable
 - rtc_interrupt_config_t, [1004](#)
- overrun
 - lin_word_status_str_t, [828](#)
 - mpu_error_info_t, [873](#)
- overrun_flg
 - lin_protocol_state_t, [842](#)
- owte
 - sbc_sys_evt_t, [1178](#)
- p
 - DhKey, [1274](#)
 - DhParams, [1275](#)
 - DsaKey, [1276](#)
 - RsaKey, [1317](#)
 - WOLFSSL_DH, [1355](#)
 - WOLFSSL_DSA, [1356](#)
 - WOLFSSL_RSA, [1368](#)
- P2_min
 - lin_node_attribute_t, [830](#)
- p_len
 - DhParams, [1275](#)
- PCI_RES_ASSIGN_FRAME_ID_RANGE
 - Low level API, [844](#)
- PCI_RES_READ_BY_IDENTIFY
 - Low level API, [844](#)
- PCI_RES_SAVE_CONFIGURATION
 - Low level API, [844](#)
- PCI_SAVE_CONFIGURATION
 - Low level API, [844](#)
- PDB Driver, [929](#)
 - PDB_CLK_PREDIV_BY_1, [934](#)
 - PDB_CLK_PREDIV_BY_128, [935](#)
 - PDB_CLK_PREDIV_BY_16, [934](#)
 - PDB_CLK_PREDIV_BY_2, [934](#)
 - PDB_CLK_PREDIV_BY_32, [934](#)
 - PDB_CLK_PREDIV_BY_4, [934](#)
 - PDB_CLK_PREDIV_BY_64, [934](#)
 - PDB_CLK_PREDIV_BY_8, [934](#)
 - PDB_CLK_PREMULT_FACT_AS_1, [935](#)
 - PDB_CLK_PREMULT_FACT_AS_10, [935](#)
 - PDB_CLK_PREMULT_FACT_AS_20, [935](#)
 - PDB_CLK_PREMULT_FACT_AS_40, [935](#)
 - PDB_DRV_ClearAdcPreTriggerFlags, [935](#)
 - PDB_DRV_ClearAdcPreTriggerSeqErrFlags, [936](#)
 - PDB_DRV_ClearTimerIntFlag, [936](#)
 - PDB_DRV_ConfigAdcPreTrigger, [936](#)
 - PDB_DRV_Deinit, [936](#)
 - PDB_DRV_Disable, [936](#)
 - PDB_DRV_Enable, [937](#)
 - PDB_DRV_GetAdcPreTriggerFlags, [937](#)
 - PDB_DRV_GetAdcPreTriggerSeqErrFlags, [937](#)

- PDB_DRV_GetDefaultConfig, [937](#)
- PDB_DRV_GetTimerIntFlag, [938](#)
- PDB_DRV_GetTimerValue, [938](#)
- PDB_DRV_Init, [938](#)
- PDB_DRV_LoadValuesCmd, [938](#)
- PDB_DRV_SetAdcPreTriggerDelayValue, [939](#)
- PDB_DRV_SetCmpPulseOutDelayForHigh, [939](#)
- PDB_DRV_SetCmpPulseOutDelayForLow, [939](#)
- PDB_DRV_SetCmpPulseOutEnable, [939](#)
- PDB_DRV_SetTimerModulusValue, [940](#)
- PDB_DRV_SetValueForTimerInterrupt, [940](#)
- PDB_DRV_SoftTriggerCmd, [940](#)
- PDB_LOAD_VAL_AT_MODULO_COUNTER, [935](#)
- PDB_LOAD_VAL_AT_MODULO_COUNTER_OR_N←
R_NEXT_TRIGGER, [935](#)
- PDB_LOAD_VAL_AT_NEXT_TRIGGER, [935](#)
- PDB_LOAD_VAL_IMMEDIATELY, [935](#)
- PDB_SOFTWARE_TRIGGER, [935](#)
- PDB_TRIGGER_IN0, [935](#)
- pdb_clk_prescaler_div_t, [934](#)
- pdb_clk_prescaler_mult_factor_t, [935](#)
- pdb_load_value_mode_t, [935](#)
- pdb_trigger_src_t, [935](#)
- PDB_CLK_PREDIV_BY_1
 - PDB Driver, [934](#)
- PDB_CLK_PREDIV_BY_128
 - PDB Driver, [935](#)
- PDB_CLK_PREDIV_BY_16
 - PDB Driver, [934](#)
- PDB_CLK_PREDIV_BY_2
 - PDB Driver, [934](#)
- PDB_CLK_PREDIV_BY_32
 - PDB Driver, [934](#)
- PDB_CLK_PREDIV_BY_4
 - PDB Driver, [934](#)
- PDB_CLK_PREDIV_BY_64
 - PDB Driver, [934](#)
- PDB_CLK_PREDIV_BY_8
 - PDB Driver, [934](#)
- PDB_CLK_PREMULT_FACT_AS_1
 - PDB Driver, [935](#)
- PDB_CLK_PREMULT_FACT_AS_10
 - PDB Driver, [935](#)
- PDB_CLK_PREMULT_FACT_AS_20
 - PDB Driver, [935](#)
- PDB_CLK_PREMULT_FACT_AS_40
 - PDB Driver, [935](#)
- PDB_DRV_ClearAdcPreTriggerFlags
 - PDB Driver, [935](#)
- PDB_DRV_ClearAdcPreTriggerSeqErrFlags
 - PDB Driver, [936](#)
- PDB_DRV_ClearTimerIntFlag
 - PDB Driver, [936](#)
- PDB_DRV_ConfigAdcPreTrigger
 - PDB Driver, [936](#)
- PDB_DRV_Deinit
 - PDB Driver, [936](#)
- PDB_DRV_Disable
 - PDB Driver, [936](#)
- PDB_DRV_Enable
 - PDB Driver, [937](#)
- PDB_DRV_GetAdcPreTriggerFlags
 - PDB Driver, [937](#)
- PDB_DRV_GetAdcPreTriggerSeqErrFlags
 - PDB Driver, [937](#)
- PDB_DRV_GetDefaultConfig
 - PDB Driver, [937](#)
- PDB_DRV_GetTimerIntFlag
 - PDB Driver, [938](#)
- PDB_DRV_GetTimerValue
 - PDB Driver, [938](#)
- PDB_DRV_Init
 - PDB Driver, [938](#)
- PDB_DRV_LoadValuesCmd
 - PDB Driver, [938](#)
- PDB_DRV_SetAdcPreTriggerDelayValue
 - PDB Driver, [939](#)
- PDB_DRV_SetCmpPulseOutDelayForHigh
 - PDB Driver, [939](#)
- PDB_DRV_SetCmpPulseOutDelayForLow
 - PDB Driver, [939](#)
- PDB_DRV_SetCmpPulseOutEnable
 - PDB Driver, [939](#)
- PDB_DRV_SetTimerModulusValue
 - PDB Driver, [940](#)
- PDB_DRV_SetValueForTimerInterrupt
 - PDB Driver, [940](#)
- PDB_DRV_SoftTriggerCmd
 - PDB Driver, [940](#)
- PDB_LOAD_VAL_AT_MODULO_COUNTER
 - PDB Driver, [935](#)
- PDB_LOAD_VAL_AT_MODULO_COUNTER_OR_N←
EXT_TRIGGER
 - PDB Driver, [935](#)
- PDB_LOAD_VAL_AT_NEXT_TRIGGER
 - PDB Driver, [935](#)
- PDB_LOAD_VAL_IMMEDIATELY
 - PDB Driver, [935](#)
- PDB_SOFTWARE_TRIGGER
 - PDB Driver, [935](#)
- PDB_TRIGGER_IN0
 - PDB Driver, [935](#)
- PFlashBase
 - Flash Memory (Flash), [501](#)
- PFlashSize
 - Flash Memory (Flash), [501](#)
- PHY Framework, [941](#)
 - g_phyConfig, [957](#)
 - PHY_DisableAutoneg, [951](#)
 - PHY_EnableAutoneg, [952](#)
 - PHY_EnableInterrupts, [952](#)
 - PHY_FrameworkInit, [952](#)
 - PHY_GetDelay, [952](#)
 - PHY_GetId, [952](#)
 - PHY_GetLinkSpeed, [952](#)
 - PHY_GetLinkStatus, [953](#)

- PHY_GetState, [953](#)
- PHY_HandleInterrupt, [953](#)
- PHY_Init, [953](#)
- PHY_LOCATION_EXTERNAL, [950](#)
- PHY_LOCATION_INTERNAL, [950](#)
- PHY_LOOPBACK_EXTERNAL, [950](#)
- PHY_LOOPBACK_INTERNAL, [950](#)
- PHY_LOOPBACK_NONE, [950](#)
- PHY_LOOPBACK_REMOTE, [950](#)
- PHY_MainFunction, [953](#)
- PHY_RMW, [954](#)
- PHY_RMWMMD, [954](#)
- PHY_ROLE_AUTO, [951](#)
- PHY_ROLE_MASTER, [951](#)
- PHY_ROLE_SLAVE, [951](#)
- PHY_Read, [953](#)
- PHY_ReadMMD, [954](#)
- PHY_Reset, [954](#)
- PHY_RestartAutoneg, [954](#)
- PHY_Resume, [954](#)
- PHY_SPEED_100_MBPS, [951](#)
- PHY_SPEED_10_MBPS, [951](#)
- PHY_SPEED_1_GBPS, [951](#)
- PHY_SPEED_AUTONEG, [951](#)
- PHY_SPEED_RESERVED, [951](#)
- PHY_STATE_ACTIVE, [951](#)
- PHY_STATE_DISABLED, [951](#)
- PHY_STATE_LINKTRAINING, [951](#)
- PHY_STATE_OFF, [951](#)
- PHY_STATE_SILENT, [951](#)
- PHY_STATE_SLEEP, [951](#)
- PHY_STATE_SLEEPREQ, [951](#)
- PHY_STATE_UNKNOWN, [951](#)
- PHY_SelectTestMode, [956](#)
- PHY_SetLoopback, [956](#)
- PHY_SetRole, [956](#)
- PHY_Sleep, [956](#)
- PHY_SleepAbortReject, [956](#)
- PHY_Suspend, [956](#)
- PHY_Wakeup, [957](#)
- PHY_Write, [957](#)
- PHY_WriteMMD, [957](#)
- phy_location_t, [950](#)
- phy_loopback_t, [950](#)
- phy_role_t, [950](#)
- phy_speed_t, [951](#)
- phy_state_t, [951](#)
- PHY_DisableAutoneg
 - PHY Framework, [951](#)
- PHY_EnableAutoneg
 - PHY Framework, [952](#)
- PHY_EnableInterrupts
 - PHY Framework, [952](#)
- PHY_FrameworkInit
 - PHY Framework, [952](#)
- PHY_GetDelay
 - PHY Framework, [952](#)
- PHY_GetId
 - PHY Framework, [952](#)
- PHY_GetLinkSpeed
 - PHY Framework, [952](#)
- PHY_GetLinkStatus
 - PHY Framework, [953](#)
- PHY_GetState
 - PHY Framework, [953](#)
- PHY_HandleInterrupt
 - PHY Framework, [953](#)
- PHY_Init
 - PHY Framework, [953](#)
- PHY_LOCATION_EXTERNAL
 - PHY Framework, [950](#)
- PHY_LOCATION_INTERNAL
 - PHY Framework, [950](#)
- PHY_LOOPBACK_EXTERNAL
 - PHY Framework, [950](#)
- PHY_LOOPBACK_INTERNAL
 - PHY Framework, [950](#)
- PHY_LOOPBACK_NONE
 - PHY Framework, [950](#)
- PHY_LOOPBACK_REMOTE
 - PHY Framework, [950](#)
- PHY_MainFunction
 - PHY Framework, [953](#)
- PHY_RMW
 - PHY Framework, [954](#)
- PHY_RMWMMD
 - PHY Framework, [954](#)
- PHY_ROLE_AUTO
 - PHY Framework, [951](#)
- PHY_ROLE_MASTER
 - PHY Framework, [951](#)
- PHY_ROLE_SLAVE
 - PHY Framework, [951](#)
- PHY_Read
 - PHY Framework, [953](#)
- PHY_ReadMMD
 - PHY Framework, [954](#)
- PHY_Reset
 - PHY Framework, [954](#)
- PHY_RestartAutoneg
 - PHY Framework, [954](#)
- PHY_Resume
 - PHY Framework, [954](#)
- PHY_SPEED_100_MBPS
 - PHY Framework, [951](#)
- PHY_SPEED_10_MBPS
 - PHY Framework, [951](#)
- PHY_SPEED_1_GBPS
 - PHY Framework, [951](#)
- PHY_SPEED_AUTONEG
 - PHY Framework, [951](#)
- PHY_SPEED_RESERVED
 - PHY Framework, [951](#)
- PHY_STATE_ACTIVE
 - PHY Framework, [951](#)
- PHY_STATE_DISABLED

- PHY Framework, [951](#)
- PHY_STATE_LINKTRAINING
 - PHY Framework, [951](#)
- PHY_STATE_OFF
 - PHY Framework, [951](#)
- PHY_STATE_SILENT
 - PHY Framework, [951](#)
- PHY_STATE_SLEEP
 - PHY Framework, [951](#)
- PHY_STATE_SLEEPREQ
 - PHY Framework, [951](#)
- PHY_STATE_UNKNOWN
 - PHY Framework, [951](#)
- PHY_SelectTestMode
 - PHY Framework, [956](#)
- PHY_SetLoopback
 - PHY Framework, [956](#)
- PHY_SetRole
 - PHY Framework, [956](#)
- PHY_Sleep
 - PHY Framework, [956](#)
- PHY_SleepAbortReject
 - PHY Framework, [956](#)
- PHY_Suspend
 - PHY Framework, [956](#)
- PHY_TJA110X_CLKMODE_25MHZ_EXT_CLK
 - TJA110x PHY, [1144](#)
- PHY_TJA110X_CLKMODE_50MHZ_EXT_REFCLK
 - TJA110x PHY, [1144](#)
- PHY_TJA110X_CLKMODE_XTAL_NO_OUTPUT
 - TJA110x PHY, [1144](#)
- PHY_TJA110X_CLKMODE_XTAL_WITH_25MHZ_OUT
 - UTPUT
 - TJA110x PHY, [1144](#)
- PHY_TJA110X_LOCALWUTIME_LONG
 - TJA110x PHY, [1144](#)
- PHY_TJA110X_LOCALWUTIME_LONGEST
 - TJA110x PHY, [1144](#)
- PHY_TJA110X_LOCALWUTIME_SHORT
 - TJA110x PHY, [1144](#)
- PHY_TJA110X_LOCALWUTIME_SHORTEST
 - TJA110x PHY, [1144](#)
- PHY_Wakeup
 - PHY Framework, [957](#)
- PHY_Write
 - PHY Framework, [957](#)
- PHY_WriteMMD
 - PHY Framework, [957](#)
- PHY_driver_generic
 - Generic PHY, [666](#)
- PHY_driver_tja110x
 - TJA110x PHY, [1146](#)
- PINS_Driver, [958](#)
 - GPIO_INPUT_DIRECTION, [959](#)
 - GPIO_OUTPUT_DIRECTION, [959](#)
 - GPIO_UNSPECIFIED_DIRECTION, [959](#)
 - PINS_DRV_ClearPins, [960](#)
 - PINS_DRV_GetPinsOutput, [960](#)
 - PINS_DRV_Init, [960](#)
 - PINS_DRV_ReadPins, [960](#)
 - PINS_DRV_SetPins, [961](#)
 - PINS_DRV_TogglePins, [961](#)
 - PINS_DRV_WritePin, [961](#)
 - PINS_DRV_WritePins, [962](#)
 - pins_level_type_t, [959](#)
 - port_data_direction_t, [959](#)
- PINS_DRV_ClearPins
 - PINS_Driver, [960](#)
- PINS_DRV_GetPinsOutput
 - PINS_Driver, [960](#)
- PINS_DRV_Init
 - PINS_Driver, [960](#)
- PINS_DRV_ReadPins
 - PINS_Driver, [960](#)
- PINS_DRV_SetPins
 - PINS_Driver, [961](#)
- PINS_DRV_TogglePins
 - PINS_Driver, [961](#)
- PINS_DRV_WritePin
 - PINS_Driver, [961](#)
- PINS_DRV_WritePins
 - PINS_Driver, [962](#)
- POSITIVE
 - Common Transport Layer API, [359](#)
- POWER_MANAGER_CALLBACK_AFTER
 - Power Manager, [970](#)
- POWER_MANAGER_CALLBACK_BEFORE
 - Power Manager, [970](#)
- POWER_MANAGER_CALLBACK_BEFORE_AFTER
 - Power Manager, [970](#)
- POWER_MANAGER_MAX
 - Power_s32k1xx, [980](#)
- POWER_MANAGER_NOTIFY_AFTER
 - Power Manager, [971](#)
- POWER_MANAGER_NOTIFY_BEFORE
 - Power Manager, [971](#)
- POWER_MANAGER_NOTIFY_RECOVER
 - Power Manager, [971](#)
- POWER_MANAGER_POLICY_AGREEMENT
 - Power Manager, [971](#)
- POWER_MANAGER_POLICY_FORCIBLE
 - Power Manager, [971](#)
- POWER_MANAGER_RUN
 - Power_s32k1xx, [980](#)
- POWER_MANAGER_VLPR
 - Power_s32k1xx, [980](#)
- POWER_MANAGER_VLPS
 - Power_s32k1xx, [980](#)
- POWER_SYS_Deinit
 - Power Manager, [971](#)
- POWER_SYS_DoDeinit
 - Power_s32k1xx, [982](#)
- POWER_SYS_DoGetDefaultConfig
 - Power_s32k1xx, [982](#)
- POWER_SYS_DoInit
 - Power_s32k1xx, [982](#)

POWER_SYS_DoSetMode
 Power_s32k1xx, [982](#)
 POWER_SYS_GetCurrentMode
 Power Manager, [971](#)
 POWER_SYS_GetDefaultConfig
 Power Manager, [971](#)
 POWER_SYS_GetErrorCallback
 Power Manager, [971](#)
 POWER_SYS_GetErrorCallbackIndex
 Power Manager, [972](#)
 POWER_SYS_GetLastMode
 Power Manager, [972](#)
 POWER_SYS_GetLastModeConfig
 Power Manager, [972](#)
 POWER_SYS_GetResetSrcStatusCmd
 Power_s32k1xx, [982](#)
 POWER_SYS_Init
 Power Manager, [973](#)
 POWER_SYS_SetMode
 Power Manager, [973](#)
 PWM_ACTIVE_HIGH
 Pulse-width modulation - Peripheral Abstraction
 Layer (PWM PAL), [990](#)
 PWM_ACTIVE_LOW
 Pulse-width modulation - Peripheral Abstraction
 Layer (PWM PAL), [990](#)
 PWM_CENTER_ALIGNED
 Pulse-width modulation - Peripheral Abstraction
 Layer (PWM PAL), [990](#)
 PWM_DUPLICATED
 Pulse-width modulation - Peripheral Abstraction
 Layer (PWM PAL), [990](#)
 PWM_Deinit
 Pulse-width modulation - Peripheral Abstraction
 Layer (PWM PAL), [990](#)
 PWM_EDGE_ALIGNED
 Pulse-width modulation - Peripheral Abstraction
 Layer (PWM PAL), [990](#)
 PWM_INVERTED
 Pulse-width modulation - Peripheral Abstraction
 Layer (PWM PAL), [990](#)
 PWM_Init
 Pulse-width modulation - Peripheral Abstraction
 Layer (PWM PAL), [991](#)
 PWM_OverwriteOutputChannels
 Pulse-width modulation - Peripheral Abstraction
 Layer (PWM PAL), [991](#)
 PWM_UpdateDuty
 Pulse-width modulation - Peripheral Abstraction
 Layer (PWM PAL), [991](#)
 PWM_UpdatePeriod
 Pulse-width modulation - Peripheral Abstraction
 Layer (PWM PAL), [991](#)
 packetInfo_st, [1305](#)
 bufferValue, [1305](#)
 packetName, [1305](#)
 timestamp, [1306](#)
 value, [1306](#)
 valueSz, [1306](#)
 packetName
 packetInfo_st, [1305](#)
 packetNames
 handShakeInfo_st, [1285](#)
 packets
 timeoutInfo_st, [1330](#)
 pad
 BuildMsgArgs, [1255](#)
 pad_size
 CipherSpecs, [1259](#)
 padSz
 Keys, [1291](#)
 pair
 WOLFSSL_BIO, [1345](#)
 parameter
 edma_chn_state_t, [416](#)
 parityMode
 lpuart_user_config_t, [807](#)
 uart_user_config_t, [1214](#)
 partNetDataMask
 uja113x_cpnc_cfg_t, [192](#)
 partSize
 csec_state_t, [301](#)
 partialWrite
 Options, [1303](#)
 WOLFSSL_CTX, [1353](#)
 path
 CRL_Monitor, [1262](#)
 pathLength
 DecodedCert, [1267](#)
 Signer, [1324](#)
 pathLengthSet
 DecodedCert, [1267](#)
 Signer, [1324](#)
 payloadSize
 can_user_config_t, [389](#)
 pcc_config_t, [335](#)
 count, [335](#)
 peripheralClocks, [335](#)
 pccConfig
 clock_manager_user_config_t, [337](#)
 pcsPolarity
 lpspi_master_config_t, [776](#)
 lpspi_slave_config_t, [780](#)
 pdb_adc_pretrigger_config_t, [934](#)
 adcPreTriggerIdx, [934](#)
 preTriggerBackToBackEnable, [934](#)
 preTriggerEnable, [934](#)
 preTriggerOutputEnable, [934](#)
 pdb_clk_prescaler_div_t
 PDB Driver, [934](#)
 pdb_clk_prescaler_mult_factor_t
 PDB Driver, [935](#)
 pdb_load_value_mode_t
 PDB Driver, [935](#)
 pdb_timer_config_t, [933](#)
 clkPreDiv, [933](#)

- clkPreMultFactor, [933](#)
- continuousModeEnable, [933](#)
- dmaEnable, [933](#)
- intEnable, [933](#)
- loadValueMode, [933](#)
- seqErrIntEnable, [933](#)
- triggerInput, [933](#)
- pdb_trigger_src_t
 - PDB Driver, [935](#)
- pdbPrescaler
 - extension_adc_s32k1xx_t, [275](#)
- pdc
 - sbc_regulator_t, [1177](#)
- peClkSrc
 - can_user_config_t, [389](#)
- peer
 - WOLFSSL_DTLS_CTX, [1357](#)
- peer_sequence_number_hi
 - Keys, [1291](#)
- peer_sequence_number_lo
 - Keys, [1291](#)
- peerRsaKey
 - WOLFSSL, [1338](#)
- peerRsaKeyPresent
 - WOLFSSL, [1339](#)
- pendingMsg
 - Arrays, [1250](#)
- pendingMsgOffset
 - Arrays, [1250](#)
- pendingMsgSz
 - Arrays, [1250](#)
- pendingMsgType
 - Arrays, [1250](#)
- percentWindow
 - wdg_config_t, [1225](#)
- period
 - lpit_user_channel_config_t, [763](#)
 - pwm_channel_t, [989](#)
- periodUnits
 - lpit_user_channel_config_t, [763](#)
- Peripheral access layer for S32K148, [963](#)
- peripheral_clock_config_t, [334](#)
 - clkGate, [335](#)
 - clkSrc, [335](#)
 - clockName, [335](#)
 - divider, [335](#)
 - frac, [335](#)
- peripheral_clock_divider_t
 - Clock Manager Driver, [343](#)
- peripheral_clock_frac_t
 - Clock Manager Driver, [343](#)
- peripheral_clock_source_t
 - Clock Manager Driver, [342](#)
- peripheralClocks
 - pcc_config_t, [335](#)
- peripheralFeaturesList
 - Clock Manager Driver, [354](#)
- permittedNames
 - DecodedCert, [1268](#)
 - Signer, [1324](#)
- personal
 - __blake2b_param, [1243](#)
 - __blake2s_param, [1245](#)
- phaseAConfig
 - ftm_quad_decode_config_t, [657](#)
- phaseBConfig
 - ftm_quad_decode_config_t, [657](#)
- phaseFilterVal
 - ftm_phase_params_t, [656](#)
- phaseInputFilter
 - ftm_phase_params_t, [656](#)
- phasePolarity
 - ftm_phase_params_t, [656](#)
- phaseSeg1
 - can_time_segment_t, [387](#)
 - flexcan_time_segment_t, [516](#)
- phaseSeg2
 - can_time_segment_t, [387](#)
 - flexcan_time_segment_t, [516](#)
- phy_basicStatus_t, [1306](#)
 - autonegAbility, [1306](#)
 - autonegComplete, [1306](#)
 - baseT2Fd, [1306](#)
 - baseT2Hd, [1307](#)
 - extendedStatus, [1307](#)
 - link, [1307](#)
 - remoteFault, [1307](#)
- phy_config_t, [946](#)
 - addr, [946](#)
 - autonegCompleteCB, [946](#)
 - autonegFailedCB, [946](#)
 - clause45, [946](#)
 - delay, [946](#)
 - enetInstance, [947](#)
 - extendedConfig, [947](#)
 - linkDownEventCB, [947](#)
 - linkUpEventCB, [947](#)
 - location, [947](#)
 - manualDelay, [947](#)
 - privateData, [947](#)
 - role, [947](#)
 - sleepRequestCB, [947](#)
 - speed, [947](#)
 - type, [947](#)
- phy_delay_t, [945](#)
 - mdiToMiiMax, [945](#)
 - mdiToMiiMin, [945](#)
 - miiToMdiMax, [945](#)
 - miiToMdiMin, [946](#)
- phy_driver_t, [948](#)
 - disableAutoneg, [948](#)
 - enableAutoneg, [948](#)
 - enableInterrupts, [948](#)
 - getDelay, [948](#)
 - getId, [948](#)
 - getLinkSpeed, [949](#)

- getLinkStatus, 949
- getState, 949
- handleInterrupt, 949
- init, 949
- mainFunction, 949
- read, 949
- readMMD, 949
- reset, 949
- restartAutoneg, 949
- resume, 949
- rmw, 949
- rmwMMD, 949
- selectTestMode, 949
- setLoopback, 949
- setRole, 950
- sleep, 950
- sleepAbortReject, 950
- suspend, 950
- wakeup, 950
- write, 950
- writeMMD, 950
- phy_id_t, 945
 - oui, 945
 - revisionNo, 945
 - typeNo, 945
- phy_location_t
 - PHY Framework, 950
- phy_loopback_t
 - PHY Framework, 950
- phy_role_t
 - PHY Framework, 950
- phy_speed_t
 - PHY Framework, 951
- phy_state_t
 - PHY Framework, 951
- phy_tja110x_clkMode_t
 - TJA110x PHY, 1144
- phy_tja110x_config_t, 1138
 - clkHold, 1139
 - clkMode, 1139
 - fwdPhyLocal, 1139
 - fwdPhyRemote, 1139
 - localWakeupPhy, 1139
 - localWuTimer, 1139
 - reducedClkDriveStrength, 1139
 - reducedMiiDriveStrength, 1139
 - remoteWakeupPhy, 1139
 - wakeInRatiometricThreshold, 1140
- phy_tja110x_localWuTime_t
 - TJA110x PHY, 1144
- pin_settings_config_t, 958
 - direction, 959
 - gpioBase, 959
 - initValue, 959
 - mux, 959
 - pinPortIdx, 959
- pinPolarity
 - lptmr_config_t, 795
- pinPortIdx
 - pin_settings_config_t, 959
- pinSelect
 - lptmr_config_t, 795
- pinState
 - cmp_comparator_t, 368
- Pins Driver (PINS), 964
- pins_level_type_t
 - PINS Driver, 959
- pkey
 - WOLFSSL_EVP_PKEY, 1363
- pkey_sz
 - WOLFSSL_EVP_PKEY, 1363
- plain
 - SignatureCtx, 1322
- plainSz
 - Buffers, 1252
- platGateConfig
 - sim_clock_config_t, 327
- pmc_config_t, 336
 - lpoClockConfig, 336
- pmc_lpo_clock_config_t, 335
 - enable, 336
 - initialize, 336
 - trimValue, 336
- pmcConfig
 - clock_manager_user_config_t, 337
- pncok
 - sbc_can_ctr_t, 1179
- pndm
 - sbc_frame_t, 1180
- pnfde
 - sbc_trans_evnt_stat_t, 1188
- po
 - sbc_sys_evnt_stat_t, 1187
- polarity
 - ftm_independent_ch_param_t, 645
 - pwm_channel_t, 989
- policy
 - clock_notify_struct_t, 339
 - power_manager_notify_struct_t, 968
- poly
 - crc_spec_t, 247
- port
 - tcp_ready, 1329
- port_data_direction_t
 - PINS Driver, 959
- positiveInputMux
 - cmp_anmux_t, 369
- positivePortMux
 - cmp_anmux_t, 369
- Power Manager, 966
 - gPowerManagerState, 975
 - POWER_MANAGER_CALLBACK_AFTER, 970
 - POWER_MANAGER_CALLBACK_BEFORE, 970
 - POWER_MANAGER_CALLBACK_BEFORE_AFTER, 970
 - POWER_MANAGER_NOTIFY_AFTER, 971

- POWER_MANAGER_NOTIFY_BEFORE, 971
- POWER_MANAGER_NOTIFY_RECOVER, 971
- POWER_MANAGER_POLICY_AGREEMENT, 971
- POWER_MANAGER_POLICY_FORCIBLE, 971
- POWER_SYS_Deinit, 971
- POWER_SYS_GetCurrentMode, 971
- POWER_SYS_GetDefaultConfig, 971
- POWER_SYS_GetErrorCallback, 971
- POWER_SYS_GetErrorCallbackIndex, 972
- POWER_SYS_GetLastMode, 972
- POWER_SYS_GetLastModeConfig, 972
- POWER_SYS_Init, 973
- POWER_SYS_SetMode, 973
- power_manager_callback_data_t, 969
- power_manager_callback_t, 970
- power_manager_callback_type_t, 970
- power_manager_notify_t, 970
- power_manager_policy_t, 971
- Power Manager Driver, 976
- power_manager_callback_data_t
 - Power Manager, 969
- power_manager_callback_t
 - Power Manager, 970
- power_manager_callback_type_t
 - Power Manager, 970
- power_manager_callback_user_config_t, 968
 - callbackData, 968
 - callbackFunction, 968
 - callbackType, 968
- power_manager_modes_t
 - Power_s32k1xx, 980
- power_manager_notify_struct_t, 967
 - notifyType, 968
 - policy, 968
 - targetPowerConfigIndex, 968
 - targetPowerConfigPtr, 968
- power_manager_notify_t
 - Power Manager, 970
- power_manager_policy_t
 - Power Manager, 971
- power_manager_state_t, 968
 - configs, 969
 - configsNumber, 969
 - currentConfig, 969
 - errorCallbackIndex, 969
 - staticCallbacks, 969
 - staticCallbacksNumber, 969
- power_manager_user_config_t, 979
 - powerMode, 979
 - sleepOnExitValue, 979
- power_mode_stat_t
 - Power_s32k1xx, 980
- Power_s32k1xx, 978
 - POWER_MANAGER_MAX, 980
 - POWER_MANAGER_RUN, 980
 - POWER_MANAGER_VLPR, 980
 - POWER_MANAGER_VLPS, 980
- POWER_SYS_DoDeinit, 982
- POWER_SYS_DoGetDefaultConfig, 982
- POWER_SYS_DoInit, 982
- POWER_SYS_DoSetMode, 982
- POWER_SYS_GetResetSrcStatusCmd, 982
- power_manager_modes_t, 980
- power_mode_stat_t, 980
- RCM_CORE_LOCKUP, 981
- RCM_EXTERNAL_PIN, 981
- RCM_LOSS_OF_CLK, 981
- RCM_LOSS_OF_LOCK, 981
- RCM_LOW_VOLT_DETECT, 981
- RCM_POWER_ON, 981
- RCM_SJTAG, 981
- RCM_SMDM_AP, 981
- RCM_SOFTWARE, 981
- RCM_SRC_NAME_MAX, 981
- RCM_STOP_MODE_ACK_ERR, 981
- RCM_WATCH_DOG, 981
- rcm_source_names_t, 980
- SMC_HSRUN, 981
- SMC_RESERVED_RUN, 981
- SMC_RESERVED_STOP1, 981
- SMC_RUN, 981
- SMC_STOP, 981
- SMC_STOP1, 981
- SMC_STOP2, 981
- SMC_STOP_RESERVED, 981
- SMC_VLPR, 981
- SMC_VLPS, 981
- STAT_HSRUN, 980
- STAT_INVALID, 980
- STAT_RUN, 980
- STAT_STOP, 980
- STAT_VLPR, 980
- STAT_VLPS, 980
- STAT_VLPW, 980
- smc_run_mode_t, 981
- smc_stop_mode_t, 981
- smc_stop_option_t, 981
- powerMode
 - cmp_comparator_t, 368
 - power_manager_user_config_t, 979
- powerModeName
 - smc_power_mode_config_t, 979
- preDivider
 - can_time_segment_t, 387
 - flexcan_time_segment_t, 516
- preMasterSecret
 - Arrays, 1250
- preMasterSz
 - Arrays, 1250
- preTriggerBackToBackEnable
 - pdb_adc_pretrigger_config_t, 934
- preTriggerEnable
 - pdb_adc_pretrigger_config_t, 934
- preTriggerOutputEnable
 - pdb_adc_pretrigger_config_t, 934

- prediv
 - scg_spll_config_t, 332
- prescaler
 - ewm_init_config_t, 470
 - extension_ftm_for_timer_t, 1160
 - extension_lptmr_for_timer_t, 1160
 - lptmr_config_t, 795
 - pwm_ftm_timebase_t, 988
- prescalerEnable
 - wdg_config_t, 1225
 - wdog_user_config_t, 1234
- prescalerValue
 - extension_ewm_for_wdg_t, 1224
- pretriggerSel
 - adc_converter_config_t, 256
- prev
 - WOLF_EVENT, 1335
 - WOLFSSL_BIO, 1345
- prevSent
 - Buffers, 1252
- prevSeq_hi
 - WOLFSSL_DTLS_PEERSEQ, 1358
- prevSeq_lo
 - WOLFSSL_DTLS_PEERSEQ, 1358
- prevWindow
 - WOLFSSL_DTLS_PEERSEQ, 1358
- previous_schedule_id
 - lin_master_data_t, 840
- priv_key
 - WOLFSSL_DH, 1355
 - WOLFSSL_DSA, 1356
 - WOLFSSL_EC_KEY, 1359
- privateData
 - phy_config_t, 947
- privateKey
 - WOLFSSL_CTX, 1353
- privateKeySz
 - WOLFSSL_CTX, 1353
- privateKeyType
 - WOLFSSL_CTX, 1354
- ProcPeerCertArgs, 1307
 - begin, 1307
 - certIdx, 1307
 - certs, 1308
 - count, 1308
 - dCert, 1308
 - dCertInit, 1308
 - domain, 1308
 - fatal, 1308
 - idx, 1308
 - lastErr, 1308
 - totalCerts, 1308
- processId
 - mpu_error_info_t, 873
- processIdEnable
 - mpu_region_config_t, 874
- processIdMask
 - mpu_region_config_t, 875
- processIdentifier
 - mpu_region_config_t, 875
- processReply
 - Options, 1303
- product_id
 - lin_node_attribute_t, 830
- product_id_ptr
 - lin_tl_descriptor_t, 836
- programedState
 - cmp_trigger_mode_t, 370
- Programmable Delay Block (PDB), 984
- propSeg
 - can_time_segment_t, 387
 - flexcan_time_segment_t, 516
- proto
 - enet_rx_enh_info_t, 450
- protocol_version
 - lin_protocol_user_config_t, 839
- ProtocolVersion, 1308
 - major, 1308
 - minor, 1309
- ps
 - fs45_fssm_reg_t, 1058
- psk_key
 - Arrays, 1250
- psk_keySz
 - Arrays, 1250
- pssAlgo
 - WOLFSSL, 1339
- ptr
 - SignatureCtx, 1322
 - WOLF_EVENT, 1335
 - WOLFSSL_EVP_PKEY, 1363
 - WOLFSSL_X509_OBJECT, 1377
- ptr_sch_data_ptr
 - lin_schedule_t, 833
- pub_key
 - WOLFSSL_DH, 1356
 - WOLFSSL_DSA, 1357
 - WOLFSSL_EC_KEY, 1359
- pubKey
 - WOLFSSL_X509, 1374
- pubKeyOID
 - WOLFSSL_X509, 1374
- pubKeySize
 - DecodedCert, 1268
 - Signer, 1324
- pubKeyStored
 - DecodedCert, 1268
- publicKey
 - DecodedCert, 1268
 - Signer, 1324
- Pulse-width modulation - Peripheral Abstraction Layer (PWM PAL), 985
 - PWM_ACTIVE_HIGH, 990
 - PWM_ACTIVE_LOW, 990
 - PWM_CENTER_ALIGNED, 990
 - PWM_DUPLICATED, 990

- PWM_Deinit, [990](#)
- PWM_EDGE_ALIGNED, [990](#)
- PWM_INVERTED, [990](#)
- PWM_Init, [991](#)
- PWM_OverwriteOutputChannels, [991](#)
- PWM_UpdateDuty, [991](#)
- PWM_UpdatePeriod, [991](#)
- pwm_channel_type_t, [990](#)
- pwm_complementary_mode_t, [990](#)
- pwm_polarity_t, [990](#)
- pvMajor
 - DtlsRecordLayerHeader, [1280](#)
 - RecordLayerHeader, [1315](#)
- pvMinor
 - DtlsRecordLayerHeader, [1280](#)
 - RecordLayerHeader, [1316](#)
- pwm_channel_t, [988](#)
 - channel, [988](#)
 - channelType, [988](#)
 - complementaryChannelPolarity, [989](#)
 - deadtime, [989](#)
 - duty, [989](#)
 - enableComplementaryChannel, [989](#)
 - insertDeadtime, [989](#)
 - period, [989](#)
 - polarity, [989](#)
 - timebase, [989](#)
- pwm_channel_type_t
 - Pulse-width modulation - Peripheral Abstraction Layer (PWM PAL), [990](#)
- pwm_complementary_mode_t
 - Pulse-width modulation - Peripheral Abstraction Layer (PWM PAL), [990](#)
- pwm_ftm_timebase_t, [988](#)
 - deadtimePrescaler, [988](#)
 - prescaler, [988](#)
 - sourceClock, [988](#)
- pwm_global_config_t, [989](#)
 - numberOfPwmChannels, [990](#)
 - pwmChannels, [990](#)
- pwm_instance_t, [1309](#)
 - instIdx, [1309](#)
 - instType, [1309](#)
- pwm_polarity_t
 - Pulse-width modulation - Peripheral Abstraction Layer (PWM PAL), [990](#)
- pwmChannels
 - pwm_global_config_t, [990](#)
- pwmCombinedChannelConfig
 - ftm_pwm_param_t, [648](#)
- pwmFaultInterrupt
 - ftm_pwm_fault_param_t, [645](#)
- pwmIndependentChannelConfig
 - ftm_pwm_param_t, [648](#)
- pwmOutputStateOnFault
 - ftm_pwm_fault_param_t, [645](#)
- pwr_modes_t
 - Clock Manager Driver, [344](#)
- q
 - DsaKey, [1276](#)
 - RsaKey, [1317](#)
 - WOLFSSL_DH, [1356](#)
 - WOLFSSL_DSA, [1357](#)
 - WOLFSSL_RSA, [1368](#)
 - QSPI_AHB_BUFFERS
 - QuadSPI Driver, [997](#)
 - QSPI_LUT_LOCK_KEY
 - QuadSPI Driver, [997](#)
 - qspi_ahb_config_t, [1309](#)
 - allMasters, [1310](#)
 - highPriority, [1310](#)
 - masters, [1310](#)
 - sizes, [1310](#)
 - qspi_callback_t
 - QuadSPI Driver, [997](#)
 - qspi_clock_src_t
 - QuadSPI Driver, [997](#)
 - qspi_data_rate_t
 - QuadSPI Driver, [997](#)
 - qspi_endianess_t
 - QuadSPI Driver, [998](#)
 - qspi_flash_side_t
 - QuadSPI Driver, [998](#)
 - qspi_lut_commands_t
 - QuadSPI Driver, [998](#)
 - qspi_lut_pads_t
 - QuadSPI Driver, [998](#)
 - qspi_read_mode_t
 - QuadSPI Driver, [998](#)
 - qspi_sample_delay_t
 - QuadSPI Driver, [998](#)
 - qspi_sample_phase_t
 - QuadSPI Driver, [998](#)
 - qspi_state_t, [1310](#)
 - qspi_transfer_type_t
 - QuadSPI Driver, [998](#)
 - qspi_user_config_t, [1311](#)
 - callback, [1311](#)
 - callbackParam, [1311](#)
 - clock_src, [1311](#)
 - columnAddr, [1311](#)
 - csHoldTime, [1312](#)
 - csSetupTime, [1312](#)
 - dataRate, [1312](#)
 - divider, [1312](#)
 - dmaChannel, [1312](#)
 - dmaSupport, [1312](#)
 - dozeMode, [1312](#)
 - dqsDelay, [1312](#)
 - dqsInvert, [1312](#)
 - endianess, [1312](#)
 - io2IdleValue, [1312](#)
 - io3IdleValue, [1313](#)
 - memSize, [1313](#)
 - readMode, [1313](#)
 - sampleDelay, [1313](#)

- samplePhase, [1313](#)
- side, [1313](#)
- wordAddressable, [1313](#)
- qspiRefClkGating
 - sim_clock_config_t, [327](#)
- Quad Serial Peripheral Interface (QuadSPI), [994](#)
- QuadSPI Driver, [995](#)
 - g_qspiBase, [998](#)
 - QSPI_AHB_BUFFERS, [997](#)
 - QSPI_LUT_LOCK_KEY, [997](#)
 - qspi_callback_t, [997](#)
 - qspi_clock_src_t, [997](#)
 - qspi_date_rate_t, [997](#)
 - qspi_endianess_t, [998](#)
 - qspi_flash_side_t, [998](#)
 - qspi_lut_commands_t, [998](#)
 - qspi_lut_pads_t, [998](#)
 - qspi_read_mode_t, [998](#)
 - qspi_sample_delay_t, [998](#)
 - qspi_sample_phase_t, [998](#)
 - qspi_transfer_type_t, [998](#)
- queue_current_size
 - lin_transport_layer_queue_t, [834](#)
- queue_header
 - lin_transport_layer_queue_t, [834](#)
- queue_max_size
 - lin_transport_layer_queue_t, [834](#)
- queue_status
 - lin_transport_layer_queue_t, [834](#)
- queue_tail
 - lin_transport_layer_queue_t, [834](#)
- quietShutdown
 - Options, [1303](#)
 - WOLFSSL_CTX, [1354](#)
- R
 - __blake2bp_state, [1244](#)
 - __blake2sp_state, [1246](#)
- r
 - WOLFSSL_ECDSA_SIG, [1361](#)
- RC_ADDRESS
 - Register address map, [1030](#)
- RCM_CORE_LOCKUP
 - Power_s32k1xx, [981](#)
- RCM_EXTERNAL_PIN
 - Power_s32k1xx, [981](#)
- RCM_LOSS_OF_CLK
 - Power_s32k1xx, [981](#)
- RCM_LOSS_OF_LOCK
 - Power_s32k1xx, [981](#)
- RCM_LOW_VOLT_DETECT
 - Power_s32k1xx, [981](#)
- RCM_POWER_ON
 - Power_s32k1xx, [981](#)
- RCM_SJTAG
 - Power_s32k1xx, [981](#)
- RCM_SMDM_AP
 - Power_s32k1xx, [981](#)
- RCM_SOFTWARE
 - Power_s32k1xx, [981](#)
- RCM_SRC_NAME_MAX
 - Power_s32k1xx, [981](#)
- RCM_STOP_MODE_ACK_ERR
 - Power_s32k1xx, [981](#)
- RCM_WATCH_DOG
 - Power_s32k1xx, [981](#)
- READ_ON_EVEN_EDGE
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1107](#)
- READ_ON_ODD_EDGE
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1107](#)
- RECEIVING
 - Common Transport Layer API, [359](#)
- RES_NEGATIVE
 - Common Transport Layer API, [359](#)
- RES_POSITIVE
 - Common Transport Layer API, [359](#)
- RESUME_WAIT_CNT
 - Flash Memory (Flash), [491](#)
- rJumpwidth
 - can_time_segment_t, [387](#)
 - flexcan_time_segment_t, [516](#)
- RLC_PULSE_WIDTH_01_MS
 - Start-up control configuration options (0x73), [1118](#)
- RLC_PULSE_WIDTH_03_05_MS
 - Start-up control configuration options (0x73), [1118](#)
- RLC_PULSE_WIDTH_10_12_MS
 - Start-up control configuration options (0x73), [1118](#)
- RLC_PULSE_WIDTH_20_25_MS
 - Start-up control configuration options (0x73), [1118](#)
- RTC Driver, [999](#)
 - DAYS_IN_A_LEAP_YEAR, [1005](#)
 - DAYS_IN_A_YEAR, [1005](#)
 - HOURS_IN_A_DAY, [1005](#)
 - MINS_IN_A_HOUR, [1005](#)
 - RTC_CLK_SRC_LPO_1KHZ, [1006](#)
 - RTC_CLK_SRC_OSC_32KHZ, [1006](#)
 - RTC_CLKOUT_DISABLED, [1006](#)
 - RTC_CLKOUT_SRC_32KHZ, [1006](#)
 - RTC_CLKOUT_SRC_TSIC, [1006](#)
 - RTC_CTRL_REG_LOCK, [1006](#)
 - RTC_DRV_ConfigureAlarm, [1007](#)
 - RTC_DRV_ConfigureFaultInt, [1007](#)
 - RTC_DRV_ConfigureRegisterLock, [1007](#)
 - RTC_DRV_ConfigureSecondsInt, [1008](#)
 - RTC_DRV_ConfigureTimeCompensation, [1008](#)
 - RTC_DRV_ConvertSecondsToTimeDate, [1008](#)
 - RTC_DRV_ConvertTimeDateToSeconds, [1008](#)
 - RTC_DRV_Deinit, [1009](#)
 - RTC_DRV_GetAlarmConfig, [1009](#)
 - RTC_DRV_GetCurrentTimeDate, [1009](#)
 - RTC_DRV_GetDefaultConfig, [1009](#)
 - RTC_DRV_GetNextAlarmTime, [1010](#)
 - RTC_DRV_GetRegisterLock, [1010](#)
 - RTC_DRV_GetTimeCompensation, [1010](#)
 - RTC_DRV_IRQHandler, [1011](#)

- RTC_DRV_Init, [1010](#)
- RTC_DRV_IsAlarmPending, [1011](#)
- RTC_DRV_IsTimeDateCorrectFormat, [1011](#)
- RTC_DRV_IsYearLeap, [1011](#)
- RTC_DRV_SecondsIRQHandler, [1012](#)
- RTC_DRV_SetTimeDate, [1012](#)
- RTC_DRV_StartCounter, [1012](#)
- RTC_DRV_StopCounter, [1012](#)
- RTC_INT_128HZ, [1007](#)
- RTC_INT_16HZ, [1007](#)
- RTC_INT_1HZ, [1006](#)
- RTC_INT_2HZ, [1006](#)
- RTC_INT_32HZ, [1007](#)
- RTC_INT_4HZ, [1006](#)
- RTC_INT_64HZ, [1007](#)
- RTC_INT_8HZ, [1007](#)
- RTC_LOCK_REG_LOCK, [1006](#)
- RTC_STATUS_REG_LOCK, [1006](#)
- RTC_TCL_REG_LOCK, [1006](#)
- rtc_clk_out_config_t, [1006](#)
- rtc_clk_select_t, [1006](#)
- rtc_lock_register_select_t, [1006](#)
- rtc_second_int_cfg_t, [1006](#)
- SECONDS_IN_A_DAY, [1005](#)
- SECONDS_IN_A_HOUR, [1005](#)
- SECONDS_IN_A_MIN, [1005](#)
- YEAR_RANGE_END, [1006](#)
- YEAR_RANGE_START, [1006](#)
- RTC_CLK_SRC_LPO_1KHZ
 - RTC Driver, [1006](#)
- RTC_CLK_SRC_OSC_32KHZ
 - RTC Driver, [1006](#)
- RTC_CLKOUT_DISABLED
 - RTC Driver, [1006](#)
- RTC_CLKOUT_SRC_32KHZ
 - RTC Driver, [1006](#)
- RTC_CLKOUT_SRC_TSIC
 - RTC Driver, [1006](#)
- RTC_CTRL_REG_LOCK
 - RTC Driver, [1006](#)
- RTC_DRV_ConfigureAlarm
 - RTC Driver, [1007](#)
- RTC_DRV_ConfigureFaultInt
 - RTC Driver, [1007](#)
- RTC_DRV_ConfigureRegisterLock
 - RTC Driver, [1007](#)
- RTC_DRV_ConfigureSecondsInt
 - RTC Driver, [1008](#)
- RTC_DRV_ConfigureTimeCompensation
 - RTC Driver, [1008](#)
- RTC_DRV_ConvertSecondsToTimeDate
 - RTC Driver, [1008](#)
- RTC_DRV_ConvertTimeDateToSeconds
 - RTC Driver, [1008](#)
- RTC_DRV_Deinit
 - RTC Driver, [1009](#)
- RTC_DRV_GetAlarmConfig
 - RTC Driver, [1009](#)
- RTC_DRV_GetCurrentTimeDate
 - RTC Driver, [1009](#)
- RTC_DRV_GetDefaultConfig
 - RTC Driver, [1009](#)
- RTC_DRV_GetNextAlarmTime
 - RTC Driver, [1010](#)
- RTC_DRV_GetRegisterLock
 - RTC Driver, [1010](#)
- RTC_DRV_GetTimeCompensation
 - RTC Driver, [1010](#)
- RTC_DRV_IRQHandler
 - RTC Driver, [1011](#)
- RTC_DRV_Init
 - RTC Driver, [1010](#)
- RTC_DRV_IsAlarmPending
 - RTC Driver, [1011](#)
- RTC_DRV_IsTimeDateCorrectFormat
 - RTC Driver, [1011](#)
- RTC_DRV_IsYearLeap
 - RTC Driver, [1011](#)
- RTC_DRV_SecondsIRQHandler
 - RTC Driver, [1012](#)
- RTC_DRV_SetTimeDate
 - RTC Driver, [1012](#)
- RTC_DRV_StartCounter
 - RTC Driver, [1012](#)
- RTC_DRV_StopCounter
 - RTC Driver, [1012](#)
- RTC_INT_128HZ
 - RTC Driver, [1007](#)
- RTC_INT_16HZ
 - RTC Driver, [1007](#)
- RTC_INT_1HZ
 - RTC Driver, [1006](#)
- RTC_INT_2HZ
 - RTC Driver, [1006](#)
- RTC_INT_32HZ
 - RTC Driver, [1007](#)
- RTC_INT_4HZ
 - RTC Driver, [1006](#)
- RTC_INT_64HZ
 - RTC Driver, [1007](#)
- RTC_INT_8HZ
 - RTC Driver, [1007](#)
- RTC_LOCK_REG_LOCK
 - RTC Driver, [1006](#)
- RTC_STATUS_REG_LOCK
 - RTC Driver, [1006](#)
- RTC_TCL_REG_LOCK
 - RTC Driver, [1006](#)
- RUN_MODE
 - Clock Manager Driver, [344](#)
- Rabbit, [1313](#)
 - masterCtx, [1314](#)
 - workCtx, [1314](#)
- RabbitCtx, [1314](#)
 - c, [1314](#)
 - carry, [1314](#)

- x, [1314](#)
- range
 - scg_firc_config_t, [331](#)
 - scg_sirc_config_t, [330](#)
 - scg_sosc_config_t, [329](#)
- Raw API, [1014](#)
 - ld_get_raw, [1014](#)
 - ld_put_raw, [1014](#)
 - ld_raw_rx_status, [1014](#)
 - ld_raw_tx_status, [1015](#)
- rcRegulatorCfg
 - uja113x_init_cfg_t, [185](#)
- rccrConfig
 - scg_clock_mode_config_t, [333](#)
- rcm_source_names_t
 - Power_s32k1xx, [980](#)
- rdldx
 - WOLFSSL_BIO, [1345](#)
- read
 - phy_driver_t, [949](#)
- readData
 - fs45_rx_data_t, [1051](#)
- ReadDirCtx, [1314](#)
 - dir, [1315](#)
 - entry, [1315](#)
 - name, [1315](#)
 - s, [1315](#)
- readMMD
 - phy_driver_t, [949](#)
- readMask
 - fs45_reg_config_value_t, [1051](#)
- readMode
 - qspi_user_config_t, [1313](#)
- readRq
 - WOLFSSL_BIO, [1345](#)
- ready
 - tcp_ready, [1329](#)
- Real Time Clock Driver (RTC), [1016](#)
- receive_NAD_ptr
 - lin_tl_descriptor_t, [836](#)
- receive_message_length_ptr
 - lin_tl_descriptor_t, [836](#)
- receive_message_ptr
 - lin_tl_descriptor_t, [836](#)
- receiveStatus
 - lpuart_state_t, [805](#)
- RecordLayerHeader, [1315](#)
 - length, [1315](#)
 - pvMajor, [1315](#)
 - pvMinor, [1316](#)
 - type, [1316](#)
- reducedClkDriveStrength
 - phy_tja110x_config_t, [1139](#)
- reducedMiiDriveStrength
 - phy_tja110x_config_t, [1139](#)
- refClk
 - clock_source_config_t, [339](#)
- refCount
 - WOLFSSL_CTX, [1354](#)
- refFreq
 - clock_source_config_t, [339](#)
- refIn
 - crc_spec_t, [247](#)
- refOut
 - crc_spec_t, [248](#)
- reg
 - Aes, [1248](#)
 - Des, [1273](#)
 - Des3, [1273](#)
- Register address map, [1020](#)
 - B0DRVS_ADDRESS, [1024](#)
 - B0FIE_ADDRESS, [1024](#)
 - B0FIS_ADDRESS, [1024](#)
 - B0OLDTC_ADDRESS, [1024](#)
 - B0SCDTC_ADDRESS, [1024](#)
 - B0WUPIE_ADDRESS, [1024](#)
 - B0WUPIS_ADDRESS, [1024](#)
 - B0WUPS_ADDRESS, [1024](#)
 - B0WUPTHRC_ADDRESS, [1025](#)
 - B1DRVS_ADDRESS, [1025](#)
 - B1FIE_ADDRESS, [1025](#)
 - B1FIS_ADDRESS, [1025](#)
 - B1OLDTC_ADDRESS, [1025](#)
 - B1SCDTC_ADDRESS, [1025](#)
 - B1WUPIE_ADDRESS, [1025](#)
 - B1WUPIS_ADDRESS, [1025](#)
 - B1WUPS_ADDRESS, [1025](#)
 - B1WUPTHRC_ADDRESS, [1025](#)
 - BMETSC_ADDRESS, [1025](#)
 - BMHC_ADDRESS, [1026](#)
 - BMOTC_ADDRESS, [1026](#)
 - BMUTC_ADDRESS, [1026](#)
 - BSADC1_ADDRESS, [1026](#)
 - BSADC2_ADDRESS, [1026](#)
 - CANC_ADDRESS, [1026](#)
 - DID1_ADDRESS, [1026](#)
 - DID2_ADDRESS, [1026](#)
 - DM0_ADDRESS, [1026](#)
 - DM1_ADDRESS, [1026](#)
 - DM2_ADDRESS, [1026](#)
 - DM3_ADDRESS, [1027](#)
 - DM4_ADDRESS, [1027](#)
 - DM5_ADDRESS, [1027](#)
 - DM6_ADDRESS, [1027](#)
 - DM7_ADDRESS, [1027](#)
 - DR_ADDRESS, [1027](#)
 - FC_ADDRESS, [1027](#)
 - FSC_ADDRESS, [1027](#)
 - GIS_ADDRESS, [1027](#)
 - HVIO1C_ADDRESS, [1027](#)
 - HVIO2C_ADDRESS, [1027](#)
 - HVIO3C_ADDRESS, [1028](#)
 - HVIO4C_ADDRESS, [1028](#)
 - HVIO5C_ADDRESS, [1028](#)
 - HVIO6C_ADDRESS, [1028](#)
 - HVIO7C_ADDRESS, [1028](#)

- HVIO8C_ADDRESS, [1028](#)
- HVIOHSDRVC_ADDRESS, [1028](#)
- HVIOLSDRVC_ADDRESS, [1028](#)
- ID0_ADDRESS, [1028](#)
- ID1_ADDRESS, [1028](#)
- ID2_ADDRESS, [1028](#)
- ID3_ADDRESS, [1029](#)
- IDM0_ADDRESS, [1029](#)
- IDM1_ADDRESS, [1029](#)
- IDM2_ADDRESS, [1029](#)
- IDM3_ADDRESS, [1029](#)
- LCKC_ADDRESS, [1029](#)
- LINC_ADDRESS, [1029](#)
- MC_ADDRESS, [1029](#)
- MEM0_ADDRESS, [1029](#)
- MEM1_ADDRESS, [1029](#)
- MEM2_ADDRESS, [1029](#)
- MEM3_ADDRESS, [1030](#)
- MSBCS_ADDRESS, [1030](#)
- MTPNVCRCC_ADDRESS, [1030](#)
- MTPNVS_ADDRESS, [1030](#)
- RC_ADDRESS, [1030](#)
- SBCCC_ADDRESS, [1030](#)
- SMPSC_ADDRESS, [1030](#)
- SMPSOVC_ADDRESS, [1030](#)
- SUPC_ADDRESS, [1030](#)
- SUPIE_ADDRESS, [1030](#)
- SUPIS_ADDRESS, [1030](#)
- SUPVS_ADDRESS, [1031](#)
- SYSIE_ADDRESS, [1031](#)
- SYSIS_ADDRESS, [1031](#)
- TIE_ADDRESS, [1031](#)
- TIM1C_ADDRESS, [1031](#)
- TIM1DCC_ADDRESS, [1031](#)
- TIM2C_ADDRESS, [1031](#)
- TIM2DCC_ADDRESS, [1031](#)
- TIM3C_ADDRESS, [1031](#)
- TIM3DCC_ADDRESS, [1031](#)
- TIM4C_ADDRESS, [1031](#)
- TIM4DCC_ADDRESS, [1032](#)
- TIS_ADDRESS, [1032](#)
- TS_ADDRESS, [1032](#)
- VBADC1_ADDRESS, [1032](#)
- VBADC2_ADDRESS, [1032](#)
- WTDC_ADDRESS, [1032](#)
- WTDS_ADDRESS, [1032](#)
- registerAddress
 - fs45_tx_data_t, [1283](#)
- regulator
 - sbc_regulator_ctr_t, [1181](#)
 - scg_firc_config_t, [331](#)
- regulatorCtr
 - sbc_int_config_t, [1182](#)
- remoteFault
 - phy_basicStatus_t, [1307](#)
- remoteWakeupPhy
 - phy_tja110x_config_t, [1139](#)
- repeatForever
 - rtc_alarm_config_t, [1003](#)
- repetitionInterval
 - rtc_alarm_config_t, [1003](#)
- reserved
 - __blake2b_param, [1244](#)
 - lin_word_status_str_t, [828](#)
- reset
 - Generic PHY, [666](#)
 - phy_driver_t, [949](#)
- resetCntCtrl
 - uja113x_fsc_cfg_t, [218](#)
- resolution
 - adc_converter_config_t, [256](#)
 - extension_adc_s32k1xx_t, [276](#)
- resp_err_frm_id_ptr
 - lin_node_attribute_t, [830](#)
- response_buffer_ptr
 - lin_protocol_state_t, [842](#)
- response_error
 - lin_node_attribute_t, [831](#)
- response_error_bit_offset_ptr
 - lin_node_attribute_t, [831](#)
- response_error_byte_offset_ptr
 - lin_node_attribute_t, [831](#)
- response_length
 - lin_protocol_state_t, [842](#)
- restartAutoneg
 - Generic PHY, [666](#)
 - phy_driver_t, [949](#)
- resultBuffer
 - adc_group_config_t, [274](#)
- resultBufferTail
 - adc_callback_info_t, [1247](#)
- resume
 - Generic PHY, [666](#)
 - phy_driver_t, [949](#)
 - TJA110x PHY, [1145](#)
- resuming
 - Options, [1303](#)
- ret
 - WOLF_EVENT, [1335](#)
- return_code
 - func_args, [1283](#)
- returnNotSupportUint8Param
 - Generic PHY, [666](#)
- revisionNo
 - phy_id_t, [945](#)
- rfd
 - WOLFSSL, [1339](#)
 - WOLFSSL_DTLS_CTX, [1357](#)
- rflags
 - WOLFSSL, [1339](#)
- ringCount
 - enet_config_t, [448](#)
 - enet_state_t, [449](#)
- rlc
 - sbc_start_up_t, [1177](#)
- rmw

- phy_driver_t, [949](#)
- rmwMMD
 - phy_driver_t, [949](#)
- rng
 - WOLFSSL, [1339](#)
- role
 - phy_config_t, [947](#)
- roundRobinChannelsState
 - cmp_trigger_mode_t, [370](#)
- roundRobinInterruptState
 - cmp_trigger_mode_t, [370](#)
- roundRobinState
 - cmp_trigger_mode_t, [370](#)
- rounds
 - Aes, [1248](#)
- rsa
 - SignatureCtx, [1323](#)
- RsaKey, [1316](#)
 - d, [1316](#)
 - dP, [1317](#)
 - dQ, [1317](#)
 - data, [1316](#)
 - dataIsAlloc, [1316](#)
 - dataLen, [1316](#)
 - e, [1317](#)
 - heap, [1317](#)
 - n, [1317](#)
 - p, [1317](#)
 - q, [1317](#)
 - state, [1317](#)
 - type, [1317](#)
 - u, [1317](#)
- rss
 - sbc_main_status_t, [1184](#)
- rstbDuration
 - fs45_fssm_reg_t, [1058](#)
- rtc_alarm_config_t, [1002](#)
 - alarmCallback, [1003](#)
 - alarmIntEnable, [1003](#)
 - alarmTime, [1003](#)
 - callbackParams, [1003](#)
 - numberOfRepeats, [1003](#)
 - repeatForever, [1003](#)
 - repetitionInterval, [1003](#)
- rtc_clk_out_config_t
 - RTC Driver, [1006](#)
- rtc_clk_select_t
 - RTC Driver, [1006](#)
- rtc_init_config_t, [1001](#)
 - clockOutConfig, [1002](#)
 - clockSelect, [1002](#)
 - compensation, [1002](#)
 - compensationInterval, [1002](#)
 - nonSupervisorAccessEnable, [1002](#)
 - updateEnable, [1002](#)
- rtc_interrupt_config_t, [1003](#)
 - callbackParams, [1003](#)
 - overflowIntEnable, [1004](#)
 - rtcCallback, [1004](#)
 - timeInvalidIntEnable, [1004](#)
- rtc_lock_register_select_t
 - RTC Driver, [1006](#)
- rtc_register_lock_config_t, [1004](#)
 - controlRegisterLock, [1005](#)
 - lockRegisterLock, [1005](#)
 - statusRegisterLock, [1005](#)
 - timeCompensationRegisterLock, [1005](#)
- rtc_second_int_cfg_t
 - RTC Driver, [1006](#)
- rtc_seconds_int_config_t, [1004](#)
 - rtcSecondsCallback, [1004](#)
 - secondIntConfig, [1004](#)
 - secondIntEnable, [1004](#)
 - secondsCallbackParams, [1004](#)
- rtc_timedate_t, [1001](#)
 - day, [1001](#)
 - hour, [1001](#)
 - minutes, [1001](#)
 - month, [1001](#)
 - seconds, [1001](#)
 - year, [1001](#)
- rtcCallback
 - rtc_interrupt_config_t, [1004](#)
- rtcClkInFreq
 - scg_rtc_config_t, [332](#)
- rtcConfig
 - scg_config_t, [334](#)
- rtcSecondsCallback
 - rtc_seconds_int_config_t, [1004](#)
- RunErrorReport
 - sai_user_config_t, [1040](#)
- rx_msg_size
 - lin_tl_descriptor_t, [836](#)
- rx_msg_status
 - lin_tl_descriptor_t, [837](#)
- rxBdAlloc
 - enet_state_t, [449](#)
- rxBdBase
 - enet_state_t, [449](#)
- rxBdCurrent
 - enet_state_t, [449](#)
- rxBuff
 - lin_state_t, [728](#)
 - lpspi_state_t, [778](#)
 - lpuart_state_t, [805](#)
- rxBufferAligned
 - enet_buffer_config_t, [447](#)
- rxCallback
 - lpuart_state_t, [805](#)
 - uart_user_config_t, [1214](#)
- rxCallbackParam
 - lpuart_state_t, [806](#)
 - uart_user_config_t, [1214](#)
- rxComplete
 - lpuart_state_t, [806](#)
- rxCompleted

- lin_state_t, 728
- rxCount
 - lpspi_state_t, 778
- rxDMAChannel
 - flexio_i2c_master_user_config_t, 534
 - flexio_i2s_master_user_config_t, 544
 - flexio_i2s_slave_user_config_t, 545
 - flexio_spi_master_user_config_t, 562
 - flexio_spi_slave_user_config_t, 564
 - i2s_user_config_t, 677
 - lpspi_master_config_t, 776
 - lpspi_slave_config_t, 780
 - lpspi_state_t, 779
 - lpuart_user_config_t, 807
 - spi_master_t, 1105
 - spi_slave_t, 1106
 - uart_user_config_t, 1214
- rxFrameCnt
 - lpspi_state_t, 779
- rxPin
 - extension_flexio_for_i2s_t, 677
 - flexio_i2s_master_user_config_t, 544
 - flexio_i2s_slave_user_config_t, 545
- rxRingAligned
 - enet_buffer_config_t, 447
- rxRingSize
 - enet_buffer_config_t, 447
- rxSize
 - lin_state_t, 728
 - lpuart_state_t, 806
- S
 - __blake2bp_state, 1244
 - __blake2sp_state, 1246
- s
 - ReadDirCtx, 1315
 - WOLFSSL_ECDSA_SIG, 1361
- S32K148 SoC Header file, 1033
- S32K148 System Files, 1034
- SADDR
 - edma_software_tcd_t, 422
- SAI Driver, 1035
 - SAI_ASYNC, 1043
 - SAI_CHANNEL_0, 1041
 - SAI_CHANNEL_1, 1041
 - SAI_CHANNEL_2, 1041
 - SAI_CHANNEL_3, 1041
 - SAI_DMA, 1043
 - SAI_DRV_AbortReceiving, 1043
 - SAI_DRV_AbortSending, 1043
 - SAI_DRV_GetDefaultConfig, 1043
 - SAI_DRV_GetReceivingStatus, 1043
 - SAI_DRV_GetSendingStatus, 1043
 - SAI_DRV_Receive, 1044
 - SAI_DRV_ReceiveBlocking, 1044
 - SAI_DRV_RxDeinit, 1044
 - SAI_DRV_RxGetBitClockDiv, 1044
 - SAI_DRV_RxGetBitClockFreq, 1045
 - SAI_DRV_RxInit, 1045
 - SAI_DRV_RxSetNextMaskWords, 1045
 - SAI_DRV_Send, 1045
 - SAI_DRV_SendBlocking, 1046
 - SAI_DRV_SetMaster, 1046
 - SAI_DRV_TxDeinit, 1046
 - SAI_DRV_TxGetBitClockDiv, 1046
 - SAI_DRV_TxGetBitClockFreq, 1047
 - SAI_DRV_TxInit, 1047
 - SAI_DRV_TxSetNextMaskWords, 1047
 - SAI_ERROR, 1042
 - SAI_FRAME_START, 1042
 - SAI_INTERRUPT, 1043
 - SAI_MUX_DISABLED, 1042
 - SAI_MUX_LINE, 1042
 - SAI_MUX_MEM, 1042
 - SAI_RUN_ERROR, 1042
 - SAI_RX_COMPLETE, 1042
 - SAI_SYNC_ERROR, 1042
 - SAI_SYNC_WITH_OTHER, 1043
 - SAI_TX_COMPLETE, 1042
 - sai_master_clk_source_t, 1042
 - sai_mux_mode_t, 1042
 - sai_report_type_t, 1042
 - sai_sync_mode_t, 1042
 - sai_transfer_callback_t, 1041
 - sai_transfer_type_t, 1043
- SAI_ASYNC
 - SAI Driver, 1043
- SAI_CHANNEL_0
 - SAI Driver, 1041
- SAI_CHANNEL_1
 - SAI Driver, 1041
- SAI_CHANNEL_2
 - SAI Driver, 1041
- SAI_CHANNEL_3
 - SAI Driver, 1041
- SAI_DMA
 - SAI Driver, 1043
- SAI_DRV_AbortReceiving
 - SAI Driver, 1043
- SAI_DRV_AbortSending
 - SAI Driver, 1043
- SAI_DRV_GetDefaultConfig
 - SAI Driver, 1043
- SAI_DRV_GetReceivingStatus
 - SAI Driver, 1043
- SAI_DRV_GetSendingStatus
 - SAI Driver, 1043
- SAI_DRV_Receive
 - SAI Driver, 1044
- SAI_DRV_ReceiveBlocking
 - SAI Driver, 1044
- SAI_DRV_RxDeinit
 - SAI Driver, 1044
- SAI_DRV_RxGetBitClockDiv
 - SAI Driver, 1044
- SAI_DRV_RxGetBitClockFreq
 - SAI Driver, 1045

- SAI_DRV_RxInit
 - SAI Driver, [1045](#)
- SAI_DRV_RxSetNextMaskWords
 - SAI Driver, [1045](#)
- SAI_DRV_Send
 - SAI Driver, [1045](#)
- SAI_DRV_SendBlocking
 - SAI Driver, [1046](#)
- SAI_DRV_SetMaster
 - SAI Driver, [1046](#)
- SAI_DRV_TxDeinit
 - SAI Driver, [1046](#)
- SAI_DRV_TxGetBitClockDiv
 - SAI Driver, [1046](#)
- SAI_DRV_TxGetBitClockFreq
 - SAI Driver, [1047](#)
- SAI_DRV_TxInit
 - SAI Driver, [1047](#)
- SAI_DRV_TxSetNextMaskWords
 - SAI Driver, [1047](#)
- SAI_ERROR
 - SAI Driver, [1042](#)
- SAI_FRAME_START
 - SAI Driver, [1042](#)
- SAI_INTERRUPT
 - SAI Driver, [1043](#)
- SAI_MUX_DISABLED
 - SAI Driver, [1042](#)
- SAI_MUX_LINE
 - SAI Driver, [1042](#)
- SAI_MUX_MEM
 - SAI Driver, [1042](#)
- SAI_RUN_ERROR
 - SAI Driver, [1042](#)
- SAI_RX_COMPLETE
 - SAI Driver, [1042](#)
- SAI_SYNC_ERROR
 - SAI Driver, [1042](#)
- SAI_SYNC_WITH_OTHER
 - SAI Driver, [1043](#)
- SAI_TX_COMPLETE
 - SAI Driver, [1042](#)
- SAVE_CONFIG_SET
 - Common Core API., [356](#)
- SBC configuration control options (0x74), [1076](#)
 - FNMC_DISABLE, [1077](#)
 - FNMC_ENABLE, [1077](#)
 - SDMC_DISABLE, [1077](#)
 - SDMC_ENABLE, [1077](#)
 - SLPC_SLEEP_NOT_SUPPORTED, [1077](#)
 - SLPC_SLEEP_SUPPORTED, [1077](#)
 - V1RTSUC_60_NOM, [1077](#)
 - V1RTSUC_70_NOM, [1077](#)
 - V1RTSUC_80_NOM, [1077](#)
 - V1RTSUC_90_NOM, [1077](#)
 - VEXTAC_NO_PROTECTION, [1078](#)
 - VEXTAC_SENSOR_SUPPLY, [1078](#)
- SBC FS45 Driver, [1048](#)
- FS45_CAN_SetMode, [1066](#)
- FS45_CheckFS1B, [1066](#)
- FS45_CheckLbistAbistOk, [1066](#)
- FS45_CheckVAUX, [1067](#)
- FS45_GetDefaultInitRegsConfig, [1067](#)
- FS45_GetDefaultNonInitRegsConfig, [1067](#)
- FS45_GetFaultErrorCounterValue, [1067](#)
- FS45_GetMode, [1067](#)
- FS45_Init, [1069](#)
- FS45_LDT_RunCounter, [1069](#)
- FS45_LDT_SetAfterRunValue, [1069](#)
- FS45_LDT_SetTimerMode, [1069](#)
- FS45_LDT_SetTimerOperation, [1071](#)
- FS45_LDT_SetWakeUpRegSrc, [1071](#)
- FS45_LDT_SetWakeUpValue, [1071](#)
- FS45_ReadRegister, [1071](#)
- FS45_ReleaseFSx, [1072](#)
- FS45_RequestFSxLow, [1072](#)
- FS45_RequestInterrupt, [1072](#)
- FS45_RequestReset, [1072](#)
- FS45_SetLowPowerMode, [1072](#)
- FS45_SetOUT4, [1074](#)
- FS45_SetRegulatorState, [1074](#)
- FS45_SwitchAMUXchannel, [1074](#)
- FS45_WD_ChangeSeed, [1074](#)
- FS45_WD_ChangeWindow, [1075](#)
- FS45_WD_Refresh, [1075](#)
- FS45_WriteRegister, [1075](#)
- fs45_amux_selection_t, [1063](#)
- fs45_can_mode_t, [1063](#)
- fs45_current_mode_t, [1063](#)
- fs45_fsx_req_type_t, [1064](#)
- fs45_fsxb_release_t, [1064](#)
- fs45_ldt_function_t, [1064](#)
- fs45_ldt_mode_t, [1064](#)
- fs45_ldt_wu_scr_t, [1065](#)
- fs45_prev_mode_t, [1065](#)
- fs45_reg_mode_t, [1065](#)
- fs45_wd_window_t, [1065](#)
- fs45AmuxDieTempSensor, [1063](#)
- fs45AmuxIO_0Tight, [1063](#)
- fs45AmuxIO_0Wide, [1063](#)
- fs45AmuxIO_5TightDivVkam, [1063](#)
- fs45AmuxIO_5Wide, [1063](#)
- fs45AmuxVref, [1063](#)
- fs45AmuxVsnsTight, [1063](#)
- fs45AmuxVsnsWide, [1063](#)
- fs45Aux, [1065](#)
- fs45CanModeListenOnly, [1063](#)
- fs45CanModeNormal, [1063](#)
- fs45CanModeSleepNoWakeup, [1063](#)
- fs45CanModeSleepWakeup, [1063](#)
- fs45LdtFunc1, [1064](#)
- fs45LdtFunc2, [1064](#)
- fs45LdtFunc3, [1064](#)
- fs45LdtFunc4, [1064](#)
- fs45LdtFunc5, [1064](#)
- fs45LdtModeCalibration, [1065](#)

- fs45LdtModeNormal, [1065](#)
- fs45LdtWakeupProg, [1065](#)
- fs45LdtWakeupRTC, [1065](#)
- fs45ModelInit, [1064](#)
- fs45ModeNormal, [1064](#)
- fs45ModeUnknown, [1064](#)
- fs45PrevModeDFS, [1065](#)
- fs45PrevModeLPOFF, [1065](#)
- fs45PrevModePOR, [1065](#)
- fs45ReleaseFs0b, [1064](#)
- fs45ReleaseFs0bFs1b, [1064](#)
- fs45ReleaseFs1b, [1064](#)
- fs45ReqFS0B, [1064](#)
- fs45ReqFS1B, [1064](#)
- fs45ReqFS1BDelay, [1064](#)
- fs45VCan, [1065](#)
- fs45Vcca, [1065](#)
- fs45Vcore, [1065](#)
- fs45Vkam, [1065](#)
- fs45WdWindow1024ms, [1066](#)
- fs45WdWindow128ms, [1066](#)
- fs45WdWindow12ms, [1066](#)
- fs45WdWindow16ms, [1066](#)
- fs45WdWindow1ms, [1066](#)
- fs45WdWindow24ms, [1066](#)
- fs45WdWindow256ms, [1066](#)
- fs45WdWindow2ms, [1066](#)
- fs45WdWindow32ms, [1066](#)
- fs45WdWindow3ms, [1066](#)
- fs45WdWindow4ms, [1066](#)
- fs45WdWindow512ms, [1066](#)
- fs45WdWindow64ms, [1066](#)
- fs45WdWindow6ms, [1066](#)
- fs45WdWindow8ms, [1066](#)
- fs45WdWindowDisable, [1066](#)
- SBC_UJA_CAN
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_CAN_CFDC_DIS
 - UJA116xA SBC Driver, [1192](#)
- SBC_UJA_CAN_CFDC_EN
 - UJA116xA SBC Driver, [1192](#)
- SBC_UJA_CAN_CMC_ACMODE_DA
 - UJA116xA SBC Driver, [1192](#)
- SBC_UJA_CAN_CMC_ACMODE_DD
 - UJA116xA SBC Driver, [1192](#)
- SBC_UJA_CAN_CMC_LISTEN
 - UJA116xA SBC Driver, [1192](#)
- SBC_UJA_CAN_CMC_OFMODE
 - UJA116xA SBC Driver, [1192](#)
- SBC_UJA_CAN_CPNC_DIS
 - UJA116xA SBC Driver, [1193](#)
- SBC_UJA_CAN_CPNC_EN
 - UJA116xA SBC Driver, [1193](#)
- SBC_UJA_CAN_PNCOK_DIS
 - UJA116xA SBC Driver, [1193](#)
- SBC_UJA_CAN_PNCOK_EN
 - UJA116xA SBC Driver, [1193](#)
- SBC_UJA_COUNT_DMASK
 - UJA116xA SBC Driver, [1191](#)
- SBC_UJA_COUNT_ID_REG
 - UJA116xA SBC Driver, [1191](#)
- SBC_UJA_COUNT_MASK
 - UJA116xA SBC Driver, [1191](#)
- SBC_UJA_DAT_MASK_0
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_DAT_MASK_1
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_DAT_MASK_2
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_DAT_MASK_3
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_DAT_MASK_4
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_DAT_MASK_5
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_DAT_MASK_6
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_DAT_MASK_7
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_DAT_RATE
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_DAT_RATE_CDR_1000KB
 - UJA116xA SBC Driver, [1193](#)
- SBC_UJA_DAT_RATE_CDR_100KB
 - UJA116xA SBC Driver, [1193](#)
- SBC_UJA_DAT_RATE_CDR_125KB
 - UJA116xA SBC Driver, [1193](#)
- SBC_UJA_DAT_RATE_CDR_250KB
 - UJA116xA SBC Driver, [1193](#)
- SBC_UJA_DAT_RATE_CDR_500KB
 - UJA116xA SBC Driver, [1193](#)
- SBC_UJA_DAT_RATE_CDR_50KB
 - UJA116xA SBC Driver, [1193](#)
- SBC_UJA_FAIL_SAFE
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_FAIL_SAFE_LHC_FLOAT
 - UJA116xA SBC Driver, [1193](#)
- SBC_UJA_FAIL_SAFE_LHC_LOW
 - UJA116xA SBC Driver, [1193](#)
- SBC_UJA_FRAME_CTR
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_FRAME_CTR_IDE_11B
 - UJA116xA SBC Driver, [1194](#)
- SBC_UJA_FRAME_CTR_IDE_29B
 - UJA116xA SBC Driver, [1194](#)
- SBC_UJA_FRAME_CTR_PNDM_DCARE
 - UJA116xA SBC Driver, [1194](#)
- SBC_UJA_FRAME_CTR_PNDM_EVAL
 - UJA116xA SBC Driver, [1194](#)
- SBC_UJA_GL_EVTN_STAT
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_GL_EVTN_STAT_SUPE
 - UJA116xA SBC Driver, [1194](#)
- SBC_UJA_GL_EVTN_STAT_SUPE_NO
 - UJA116xA SBC Driver, [1194](#)
- SBC_UJA_GL_EVTN_STAT_SYSE
 - UJA116xA SBC Driver, [1194](#)

- UJA116xA SBC Driver, [1194](#)
- SBC_UJA_GL_EVNT_STAT_SYSE_NO
 - UJA116xA SBC Driver, [1194](#)
- SBC_UJA_GL_EVNT_STAT_TRXE
 - UJA116xA SBC Driver, [1194](#)
- SBC_UJA_GL_EVNT_STAT_TRXE_NO
 - UJA116xA SBC Driver, [1194](#)
- SBC_UJA_GL_EVNT_STAT_WPE
 - UJA116xA SBC Driver, [1195](#)
- SBC_UJA_GL_EVNT_STAT_WPE_NO
 - UJA116xA SBC Driver, [1195](#)
- SBC_UJA_IDENTIF
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_IDENTIF_0
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_IDENTIF_1
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_IDENTIF_2
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_IDENTIF_3
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_LOCK
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_MAIN
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_MAIN_NMS_NORMAL
 - UJA116xA SBC Driver, [1195](#)
- SBC_UJA_MAIN_NMS_PWR_UP
 - UJA116xA SBC Driver, [1195](#)
- SBC_UJA_MAIN_OTWS_ABOVE
 - UJA116xA SBC Driver, [1195](#)
- SBC_UJA_MAIN_OTWS_BELOW
 - UJA116xA SBC Driver, [1195](#)
- SBC_UJA_MAIN_RSS_CAN_WAKEUP
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MAIN_RSS_DIAG_WAKEUP
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MAIN_RSS_ILLEG_SLP
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MAIN_RSS_ILLEG_WATCH
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MAIN_RSS_LFT_OVERTM
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MAIN_RSS_OFF_MODE
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MAIN_RSS_OVF_SLP
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MAIN_RSS_RSTN_PULDW
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MAIN_RSS_SLP_WAKEUP
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MAIN_RSS_V1_UNDERV
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MAIN_RSS_WAKE_SLP
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MAIN_RSS_WATCH_OVF
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MAIN_RSS_WATCH_TRIG
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MASK_0
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_MASK_1
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_MASK_2
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_MASK_3
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_MEMORY_0
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_MEMORY_1
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_MEMORY_2
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_MEMORY_3
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_MODE
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_MODE_MC_NORMAL
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MODE_MC_SLEEP
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MODE_MC_STANDBY
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MTPNV_CRC
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_MTPNV_STAT
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_MTPNV_STAT_ECCS
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MTPNV_STAT_ECCS_NO
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MTPNV_STAT_NVMPs
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_MTPNV_STAT_NVMPs_NO
 - UJA116xA SBC Driver, [1196](#)
- SBC_UJA_REGULATOR
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_REGULATOR_PDC_HV
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_REGULATOR_PDC_LV
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_REGULATOR_V1RTC_60
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_REGULATOR_V1RTC_70
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_REGULATOR_V1RTC_80
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_REGULATOR_V1RTC_90
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_REGULATOR_V2C_N
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_REGULATOR_V2C_N_S_R
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_REGULATOR_V2C_N_S_S_R
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_REGULATOR_V2C_OFF

- UJA116xA SBC Driver, [1198](#)
- SBC_UJA_SBC
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_SBC_FNMC_DIS
 - UJA116xA SBC Driver, [1199](#)
- SBC_UJA_SBC_FNMC_EN
 - UJA116xA SBC Driver, [1199](#)
- SBC_UJA_SBC_SDMC_DIS
 - UJA116xA SBC Driver, [1199](#)
- SBC_UJA_SBC_SDMC_EN
 - UJA116xA SBC Driver, [1199](#)
- SBC_UJA_SBC_SLPC_AC
 - UJA116xA SBC Driver, [1199](#)
- SBC_UJA_SBC_SLPC_IG
 - UJA116xA SBC Driver, [1199](#)
- SBC_UJA_SBC_V1RTSUC_60
 - UJA116xA SBC Driver, [1199](#)
- SBC_UJA_SBC_V1RTSUC_70
 - UJA116xA SBC Driver, [1199](#)
- SBC_UJA_SBC_V1RTSUC_80
 - UJA116xA SBC Driver, [1199](#)
- SBC_UJA_SBC_V1RTSUC_90
 - UJA116xA SBC Driver, [1199](#)
- SBC_UJA_START_UP
 - UJA116xA SBC Driver, [1198](#)
- SBC_UJA_START_UP_RLC_01_01p5
 - UJA116xA SBC Driver, [1200](#)
- SBC_UJA_START_UP_RLC_03p6_05
 - UJA116xA SBC Driver, [1200](#)
- SBC_UJA_START_UP_RLC_10_12p5
 - UJA116xA SBC Driver, [1200](#)
- SBC_UJA_START_UP_RLC_20_25p0
 - UJA116xA SBC Driver, [1200](#)
- SBC_UJA_START_UP_V2SUC_00
 - UJA116xA SBC Driver, [1200](#)
- SBC_UJA_START_UP_V2SUC_11
 - UJA116xA SBC Driver, [1200](#)
- SBC_UJA_SUP_EVNT_STAT
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_SUP_EVNT_STAT_V1U
 - UJA116xA SBC Driver, [1200](#)
- SBC_UJA_SUP_EVNT_STAT_V1U_NO
 - UJA116xA SBC Driver, [1200](#)
- SBC_UJA_SUP_EVNT_STAT_V2O
 - UJA116xA SBC Driver, [1200](#)
- SBC_UJA_SUP_EVNT_STAT_V2O_NO
 - UJA116xA SBC Driver, [1200](#)
- SBC_UJA_SUP_EVNT_STAT_V2U
 - UJA116xA SBC Driver, [1200](#)
- SBC_UJA_SUP_EVNT_STAT_V2U_NO
 - UJA116xA SBC Driver, [1200](#)
- SBC_UJA_SUPPLY_EVNT
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_SUPPLY_EVNT_V1UE_DIS
 - UJA116xA SBC Driver, [1201](#)
- SBC_UJA_SUPPLY_EVNT_V1UE_EN
 - UJA116xA SBC Driver, [1201](#)
- SBC_UJA_SUPPLY_EVNT_V2OE_DIS
 - UJA116xA SBC Driver, [1201](#)
- SBC_UJA_SUPPLY_EVNT_V2OE_EN
 - UJA116xA SBC Driver, [1201](#)
- SBC_UJA_SUPPLY_EVNT_V2UE_DIS
 - UJA116xA SBC Driver, [1201](#)
- SBC_UJA_SUPPLY_EVNT_V2UE_EN
 - UJA116xA SBC Driver, [1201](#)
- SBC_UJA_SUPPLY_STAT
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_SUPPLY_STAT_V1S_VAB
 - UJA116xA SBC Driver, [1201](#)
- SBC_UJA_SUPPLY_STAT_V1S_VBE
 - UJA116xA SBC Driver, [1201](#)
- SBC_UJA_SUPPLY_STAT_V2S_DIS
 - UJA116xA SBC Driver, [1201](#)
- SBC_UJA_SUPPLY_STAT_V2S_VAB
 - UJA116xA SBC Driver, [1201](#)
- SBC_UJA_SUPPLY_STAT_V2S_VBE
 - UJA116xA SBC Driver, [1201](#)
- SBC_UJA_SUPPLY_STAT_V2S_VOK
 - UJA116xA SBC Driver, [1201](#)
- SBC_UJA_SYS_EVNT_OTWE_DIS
 - UJA116xA SBC Driver, [1202](#)
- SBC_UJA_SYS_EVNT_OTWE_EN
 - UJA116xA SBC Driver, [1202](#)
- SBC_UJA_SYS_EVNT_SPIFE_DIS
 - UJA116xA SBC Driver, [1202](#)
- SBC_UJA_SYS_EVNT_SPIFE_EN
 - UJA116xA SBC Driver, [1202](#)
- SBC_UJA_SYS_EVNT_STAT
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_SYS_EVNT_STAT_OTW
 - UJA116xA SBC Driver, [1202](#)
- SBC_UJA_SYS_EVNT_STAT_OTW_NO
 - UJA116xA SBC Driver, [1202](#)
- SBC_UJA_SYS_EVNT_STAT_PO
 - UJA116xA SBC Driver, [1202](#)
- SBC_UJA_SYS_EVNT_STAT_PO_NO
 - UJA116xA SBC Driver, [1202](#)
- SBC_UJA_SYS_EVNT_STAT_SPIF
 - UJA116xA SBC Driver, [1202](#)
- SBC_UJA_SYS_EVNT_STAT_SPIF_NO
 - UJA116xA SBC Driver, [1202](#)
- SBC_UJA_SYS_EVNT_STAT_WDF
 - UJA116xA SBC Driver, [1203](#)
- SBC_UJA_SYS_EVNT_STAT_WDF_NO
 - UJA116xA SBC Driver, [1203](#)
- SBC_UJA_SYSTEM_EVNT
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_TIMEOUT
 - UJA116xA SBC Driver, [1191](#)
- SBC_UJA_TRANS_EVNT
 - UJA116xA SBC Driver, [1197](#)
- SBC_UJA_TRANS_EVNT_CBSE_DIS
 - UJA116xA SBC Driver, [1203](#)
- SBC_UJA_TRANS_EVNT_CBSE_EN
 - UJA116xA SBC Driver, [1203](#)
- SBC_UJA_TRANS_EVNT_CFE_DIS

UJA116xA SBC Driver, [1203](#)
 SBC_UJA_TRANS_EVT_CFE_EN
 UJA116xA SBC Driver, [1203](#)
 SBC_UJA_TRANS_EVT_CWE_DIS
 UJA116xA SBC Driver, [1203](#)
 SBC_UJA_TRANS_EVT_CWE_EN
 UJA116xA SBC Driver, [1203](#)
 SBC_UJA_TRANS_EVT_STAT
 UJA116xA SBC Driver, [1197](#)
 SBC_UJA_TRANS_EVT_STAT_CBS
 UJA116xA SBC Driver, [1203](#)
 SBC_UJA_TRANS_EVT_STAT_CBS_NO
 UJA116xA SBC Driver, [1203](#)
 SBC_UJA_TRANS_EVT_STAT_CF
 UJA116xA SBC Driver, [1204](#)
 SBC_UJA_TRANS_EVT_STAT_CF_NO
 UJA116xA SBC Driver, [1204](#)
 SBC_UJA_TRANS_EVT_STAT_CW
 UJA116xA SBC Driver, [1204](#)
 SBC_UJA_TRANS_EVT_STAT_CW_NO
 UJA116xA SBC Driver, [1204](#)
 SBC_UJA_TRANS_EVT_STAT_PNFDE
 UJA116xA SBC Driver, [1204](#)
 SBC_UJA_TRANS_EVT_STAT_PNFDE_NO
 UJA116xA SBC Driver, [1204](#)
 SBC_UJA_TRANS_STAT
 UJA116xA SBC Driver, [1197](#)
 SBC_UJA_TRANS_STAT_CBSS_ACT
 UJA116xA SBC Driver, [1204](#)
 SBC_UJA_TRANS_STAT_CBSS_INACT
 UJA116xA SBC Driver, [1204](#)
 SBC_UJA_TRANS_STAT_CFS_NO_TXD
 UJA116xA SBC Driver, [1205](#)
 SBC_UJA_TRANS_STAT_CFS_TXD
 UJA116xA SBC Driver, [1205](#)
 SBC_UJA_TRANS_STAT_COSCS_NRUN
 UJA116xA SBC Driver, [1205](#)
 SBC_UJA_TRANS_STAT_COSCS_RUN
 UJA116xA SBC Driver, [1205](#)
 SBC_UJA_TRANS_STAT_CPNERR_DET
 UJA116xA SBC Driver, [1205](#)
 SBC_UJA_TRANS_STAT_CPNERR_NO_DET
 UJA116xA SBC Driver, [1205](#)
 SBC_UJA_TRANS_STAT_CPNS_ERR
 UJA116xA SBC Driver, [1205](#)
 SBC_UJA_TRANS_STAT_CPNS_OK
 UJA116xA SBC Driver, [1205](#)
 SBC_UJA_TRANS_STAT_CTS_ACT
 UJA116xA SBC Driver, [1205](#)
 SBC_UJA_TRANS_STAT_CTS_INACT
 UJA116xA SBC Driver, [1205](#)
 SBC_UJA_TRANS_STAT_VCS_AB
 UJA116xA SBC Driver, [1206](#)
 SBC_UJA_TRANS_STAT_VCS_BE
 UJA116xA SBC Driver, [1206](#)
 SBC_UJA_WAKE_EN
 UJA116xA SBC Driver, [1197](#)
 SBC_UJA_WAKE_EN_WPFE_DIS
 UJA116xA SBC Driver, [1206](#)
 SBC_UJA_WAKE_EN_WPFE_EN
 UJA116xA SBC Driver, [1206](#)
 SBC_UJA_WAKE_EN_WPRE_DIS
 UJA116xA SBC Driver, [1206](#)
 SBC_UJA_WAKE_EN_WPRE_EN
 UJA116xA SBC Driver, [1206](#)
 SBC_UJA_WAKE_EVT_STAT
 UJA116xA SBC Driver, [1198](#)
 SBC_UJA_WAKE_EVT_STAT_WPF
 UJA116xA SBC Driver, [1206](#)
 SBC_UJA_WAKE_EVT_STAT_WPF_NO
 UJA116xA SBC Driver, [1206](#)
 SBC_UJA_WAKE_EVT_STAT_WPR
 UJA116xA SBC Driver, [1206](#)
 SBC_UJA_WAKE_EVT_STAT_WPR_NO
 UJA116xA SBC Driver, [1206](#)
 SBC_UJA_WAKE_STAT
 UJA116xA SBC Driver, [1197](#)
 SBC_UJA_WAKE_STAT_WPVS_AB
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WAKE_STAT_WPVS_BE
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WTDOG_CTR
 UJA116xA SBC Driver, [1197](#)
 SBC_UJA_WTDOG_CTR_NWP_1024
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WTDOG_CTR_NWP_128
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WTDOG_CTR_NWP_16
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WTDOG_CTR_NWP_256
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WTDOG_CTR_NWP_32
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WTDOG_CTR_NWP_4096
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WTDOG_CTR_NWP_64
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WTDOG_CTR_NWP_8
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WTDOG_CTR_WMC_AUTO
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WTDOG_CTR_WMC_TIME
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WTDOG_CTR_WMC_WIND
 UJA116xA SBC Driver, [1207](#)
 SBC_UJA_WTDOG_STAT
 UJA116xA SBC Driver, [1197](#)
 SBC_UJA_WTDOG_STAT_FNMS_N_NORMAL
 UJA116xA SBC Driver, [1208](#)
 SBC_UJA_WTDOG_STAT_FNMS_NORMAL
 UJA116xA SBC Driver, [1208](#)
 SBC_UJA_WTDOG_STAT_SDMS_N_NORMAL
 UJA116xA SBC Driver, [1208](#)
 SBC_UJA_WTDOG_STAT_SDMS_NORMAL
 UJA116xA SBC Driver, [1208](#)
 SBC_UJA_WTDOG_STAT_WDS_FIH

- UJA116xA SBC Driver, [1208](#)
- SBC_UJA_WTDOG_STAT_WDS_OFF
 - UJA116xA SBC Driver, [1208](#)
- SBC_UJA_WTDOG_STAT_WDS_SEH
 - UJA116xA SBC Driver, [1208](#)
- SBCCC_ADDRESS
 - Register address map, [1030](#)
- SCG_ASYNC_CLOCK_DISABLE
 - Clock Manager Driver, [344](#)
- SCG_ASYNC_CLOCK_DIV_BY_1
 - Clock Manager Driver, [344](#)
- SCG_ASYNC_CLOCK_DIV_BY_16
 - Clock Manager Driver, [344](#)
- SCG_ASYNC_CLOCK_DIV_BY_2
 - Clock Manager Driver, [344](#)
- SCG_ASYNC_CLOCK_DIV_BY_32
 - Clock Manager Driver, [344](#)
- SCG_ASYNC_CLOCK_DIV_BY_4
 - Clock Manager Driver, [344](#)
- SCG_ASYNC_CLOCK_DIV_BY_64
 - Clock Manager Driver, [344](#)
- SCG_ASYNC_CLOCK_DIV_BY_8
 - Clock Manager Driver, [344](#)
- SCG_CLOCKOUT_SRC_FIRC
 - Clock Manager Driver, [344](#)
- SCG_CLOCKOUT_SRC_SCG_SLOW
 - Clock Manager Driver, [344](#)
- SCG_CLOCKOUT_SRC_SIRC
 - Clock Manager Driver, [344](#)
- SCG_CLOCKOUT_SRC_SOSC
 - Clock Manager Driver, [344](#)
- SCG_CLOCKOUT_SRC_SPLL
 - Clock Manager Driver, [344](#)
- SCG_FIRC_RANGE_48M
 - Clock Manager Driver, [345](#)
- SCG_SIRC_RANGE_HIGH
 - Clock Manager Driver, [345](#)
- SCG_SOSC_GAIN_HIGH
 - Clock Manager Driver, [345](#)
- SCG_SOSC_GAIN_LOW
 - Clock Manager Driver, [345](#)
- SCG_SOSC_MONITOR_DISABLE
 - Clock Manager Driver, [345](#)
- SCG_SOSC_MONITOR_INT
 - Clock Manager Driver, [345](#)
- SCG_SOSC_MONITOR_RESET
 - Clock Manager Driver, [345](#)
- SCG_SOSC_RANGE_HIGH
 - Clock Manager Driver, [345](#)
- SCG_SOSC_RANGE_MID
 - Clock Manager Driver, [345](#)
- SCG_SOSC_REF_EXT
 - Clock Manager Driver, [345](#)
- SCG_SOSC_REF_OSC
 - Clock Manager Driver, [345](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_16
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_17
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_18
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_19
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_20
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_21
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_22
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_23
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_24
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_25
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_26
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_27
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_28
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_29
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_30
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_31
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_32
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_33
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_34
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_35
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_36
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_37
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_38
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_39
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_40
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_41
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_42
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_43
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_44
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_45
 - Clock Manager Driver, [346](#)
- SCG_SPLL_CLOCK_MULTIPLY_BY_46
 - Clock Manager Driver, [346](#)

Clock Manager Driver, [346](#)
 SCG_SPLL_CLOCK_MULTIPLY_BY_47
 Clock Manager Driver, [346](#)
 SCG_SPLL_CLOCK_PREDIV_BY_1
 Clock Manager Driver, [346](#)
 SCG_SPLL_CLOCK_PREDIV_BY_2
 Clock Manager Driver, [346](#)
 SCG_SPLL_CLOCK_PREDIV_BY_3
 Clock Manager Driver, [346](#)
 SCG_SPLL_CLOCK_PREDIV_BY_4
 Clock Manager Driver, [347](#)
 SCG_SPLL_CLOCK_PREDIV_BY_5
 Clock Manager Driver, [347](#)
 SCG_SPLL_CLOCK_PREDIV_BY_6
 Clock Manager Driver, [347](#)
 SCG_SPLL_CLOCK_PREDIV_BY_7
 Clock Manager Driver, [347](#)
 SCG_SPLL_CLOCK_PREDIV_BY_8
 Clock Manager Driver, [347](#)
 SCG_SPLL_MONITOR_DISABLE
 Clock Manager Driver, [347](#)
 SCG_SPLL_MONITOR_INT
 Clock Manager Driver, [347](#)
 SCG_SPLL_MONITOR_RESET
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_1
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_10
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_11
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_12
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_13
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_14
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_15
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_16
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_2
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_3
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_4
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_5
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_6
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_7
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_8
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_DIV_BY_9
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_SRC_FIRC

Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_SRC_NONE
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_SRC_SIRC
 Clock Manager Driver, [347](#)
 SCG_SYSTEM_CLOCK_SRC_SYS_OSC
 Clock Manager Driver, [347](#)
 SDMC_DISABLE
 SBC configuration control options (0x74), [1077](#)
 SDMC_ENABLE
 SBC configuration control options (0x74), [1077](#)
 SECONDS_IN_A_DAY
 RTC Driver, [1005](#)
 SECONDS_IN_A_HOUR
 RTC Driver, [1005](#)
 SECONDS_IN_A_MIN
 RTC Driver, [1005](#)
 SECURITY_BOOT_MAC
 Security PAL, [1084](#)
 SECURITY_BOOT_MAC_KEY
 Security PAL, [1084](#)
 SECURITY_BOOT_NOT_DEFINED
 Security PAL, [1083](#)
 SECURITY_BOOT_PARALLEL
 Security PAL, [1082](#)
 SECURITY_BOOT_SERIAL
 Security PAL, [1082](#)
 SECURITY_BOOT_STRICT
 Security PAL, [1082](#)
 SECURITY_BootDefine
 Security PAL, [1084](#)
 SECURITY_BootFailure
 Security PAL, [1084](#)
 SECURITY_BootOk
 Security PAL, [1085](#)
 SECURITY_CMD_BOOT_DEFINE
 Security PAL, [1083](#)
 SECURITY_CMD_BOOT_FAILURE
 Security PAL, [1083](#)
 SECURITY_CMD_BOOT_OK
 Security PAL, [1083](#)
 SECURITY_CMD_DBG_AUTH
 Security PAL, [1083](#)
 SECURITY_CMD_DBG_CHAL
 Security PAL, [1083](#)
 SECURITY_CMD_DEC_CBC
 Security PAL, [1083](#)
 SECURITY_CMD_DEC_ECB
 Security PAL, [1083](#)
 SECURITY_CMD_ENC_CBC
 Security PAL, [1083](#)
 SECURITY_CMD_ENC_ECB
 Security PAL, [1083](#)
 SECURITY_CMD_EXPORT_RAM_KEY
 Security PAL, [1083](#)
 SECURITY_CMD_EXTEND_SEED
 Security PAL, [1083](#)
 SECURITY_CMD_GENERATE_MAC

- Security PAL, [1083](#)
- SECURITY_CMD_GET_ID
 - Security PAL, [1083](#)
- SECURITY_CMD_INIT_RNG
 - Security PAL, [1083](#)
- SECURITY_CMD_LOAD_KEY
 - Security PAL, [1083](#)
- SECURITY_CMD_LOAD_PLAIN_KEY
 - Security PAL, [1083](#)
- SECURITY_CMD_MP_COMPRESS
 - Security PAL, [1083](#)
- SECURITY_CMD_RESERVED_1
 - Security PAL, [1083](#)
- SECURITY_CMD_RESERVED_2
 - Security PAL, [1083](#)
- SECURITY_CMD_RESERVED_3
 - Security PAL, [1083](#)
- SECURITY_CMD_RND
 - Security PAL, [1083](#)
- SECURITY_CMD_VERIFY_MAC
 - Security PAL, [1083](#)
- SECURITY_CancelCommand
 - Security PAL, [1085](#)
- SECURITY_DbgAuth
 - Security PAL, [1085](#)
- SECURITY_DbgChal
 - Security PAL, [1085](#)
- SECURITY_DecryptCbc
 - Security PAL, [1086](#)
- SECURITY_DecryptCbcBlocking
 - Security PAL, [1086](#)
- SECURITY_DecryptEcb
 - Security PAL, [1087](#)
- SECURITY_DecryptEcbBlocking
 - Security PAL, [1087](#)
- SECURITY_Deinit
 - Security PAL, [1087](#)
- SECURITY_EncryptCbc
 - Security PAL, [1088](#)
- SECURITY_EncryptCbcBlocking
 - Security PAL, [1088](#)
- SECURITY_EncryptEcb
 - Security PAL, [1088](#)
- SECURITY_EncryptEcbBlocking
 - Security PAL, [1089](#)
- SECURITY_ExportRamKey
 - Security PAL, [1089](#)
- SECURITY_ExtendSeed
 - Security PAL, [1090](#)
- SECURITY_GenerateMac
 - Security PAL, [1090](#)
- SECURITY_GenerateMacBlocking
 - Security PAL, [1090](#)
- SECURITY_GenerateRnd
 - Security PAL, [1092](#)
- SECURITY_GenerateTrnd
 - Security PAL, [1092](#)
- SECURITY_GetAsyncCmdStatus
 - Security PAL, [1092](#)
- SECURITY_GetDefaultConfig
 - Security PAL, [1093](#)
- SECURITY_GetId
 - Security PAL, [1093](#)
- SECURITY_INSTANCE0
 - Security PAL, [1083](#)
- SECURITY_Init
 - Security PAL, [1093](#)
- SECURITY_InitRng
 - Security PAL, [1093](#)
- SECURITY_KEY_1
 - Security PAL, [1084](#)
- SECURITY_KEY_10
 - Security PAL, [1084](#)
- SECURITY_KEY_11
 - Security PAL, [1084](#)
- SECURITY_KEY_12
 - Security PAL, [1084](#)
- SECURITY_KEY_13
 - Security PAL, [1084](#)
- SECURITY_KEY_14
 - Security PAL, [1084](#)
- SECURITY_KEY_15
 - Security PAL, [1084](#)
- SECURITY_KEY_16
 - Security PAL, [1084](#)
- SECURITY_KEY_17
 - Security PAL, [1084](#)
- SECURITY_KEY_2
 - Security PAL, [1084](#)
- SECURITY_KEY_3
 - Security PAL, [1084](#)
- SECURITY_KEY_4
 - Security PAL, [1084](#)
- SECURITY_KEY_5
 - Security PAL, [1084](#)
- SECURITY_KEY_6
 - Security PAL, [1084](#)
- SECURITY_KEY_7
 - Security PAL, [1084](#)
- SECURITY_KEY_8
 - Security PAL, [1084](#)
- SECURITY_KEY_9
 - Security PAL, [1084](#)
- SECURITY_LoadKey
 - Security PAL, [1095](#)
- SECURITY_LoadPlainKey
 - Security PAL, [1095](#)
- SECURITY_MASTER_ECU
 - Security PAL, [1083](#)
- SECURITY_MPCompress
 - Security PAL, [1095](#)
- SECURITY_RAM_KEY
 - Security PAL, [1084](#)
- SECURITY_SECRET_KEY
 - Security PAL, [1083](#)
- SECURITY_SecureBoot

- Security PAL, [1096](#)
- SECURITY_VerifyMac
 - Security PAL, [1096](#)
- SECURITY_VerifyMacBlocking
 - Security PAL, [1097](#)
- SERVICE_FAULT_MEMORY_CLEAR
 - Low level API, [844](#)
- SERVICE_ASSIGN_FRAME_ID
 - Low level API, [844](#)
- SERVICE_ASSIGN_FRAME_ID_RANGE
 - Low level API, [844](#)
- SERVICE_ASSIGN_NAD
 - Low level API, [844](#)
- SERVICE_CONDITIONAL_CHANGE_NAD
 - Low level API, [844](#)
- SERVICE_FAULT_MEMORY_READ
 - Low level API, [845](#)
- SERVICE_IO_CONTROL_BY_IDENTIFY
 - Low level API, [845](#)
- SERVICE_NOT_SUPPORTED
 - Common Transport Layer API, [359](#)
- SERVICE_READ_BY_IDENTIFY
 - Low level API, [845](#)
- SERVICE_READ_DATA_BY_IDENTIFY
 - Low level API, [845](#)
- SERVICE_SAVE_CONFIGURATION
 - Low level API, [845](#)
- SERVICE_SESSION_CONTROL
 - Low level API, [845](#)
- SERVICE_TARGET_RESET
 - Common Transport Layer API, [359](#)
- SERVICE_WRITE_DATA_BY_IDENTIFY
 - Low level API, [845](#)
- SIM_CLKOUT_DIV_BY_1
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_DIV_BY_2
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_DIV_BY_3
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_DIV_BY_4
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_DIV_BY_5
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_DIV_BY_6
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_DIV_BY_7
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_DIV_BY_8
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_SEL_SYSTEM_BUS_CLK
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_SEL_SYSTEM_FIRC_DIV2_CLK
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_SEL_SYSTEM_HCLK
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_SEL_SYSTEM_LPO_128K_CLK
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_SEL_SYSTEM_LPO_CLK
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_SEL_SYSTEM_RTC_CLK
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_SEL_SYSTEM_SCG_CLKOUT
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_SEL_SYSTEM_SIRC_DIV2_CLK
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_SEL_SYSTEM_SOSC_DIV2_CLK
 - Clock Manager Driver, [348](#)
- SIM_CLKOUT_SEL_SYSTEM_SPLL_DIV2_CLK
 - Clock Manager Driver, [348](#)
- SIM_LPO_CLK_SEL_LPO_128K
 - Clock Manager Driver, [348](#)
- SIM_LPO_CLK_SEL_LPO_1K
 - Clock Manager Driver, [348](#)
- SIM_LPO_CLK_SEL_LPO_32K
 - Clock Manager Driver, [348](#)
- SIM_LPO_CLK_SEL_NO_CLOCK
 - Clock Manager Driver, [348](#)
- SIM_RTCCLK_SEL_FIRCDIV1_CLK
 - Clock Manager Driver, [349](#)
- SIM_RTCCLK_SEL_LPO_32K
 - Clock Manager Driver, [349](#)
- SIM_RTCCLK_SEL_RTC_CLKIN
 - Clock Manager Driver, [349](#)
- SIM_RTCCLK_SEL_SOSCDIV1_CLK
 - Clock Manager Driver, [349](#)
- SLAST
 - edma_software_tcd_t, [422](#)
- SLAVE
 - LIN Driver, [729](#)
- SLOW_CLK_INDEX
 - Clock Manager Driver, [342](#)
- SLPC_SLEEP_NOT_SUPPORTED
 - SBC configuration control options (0x74), [1077](#)
- SLPC_SLEEP_SUPPORTED
 - SBC configuration control options (0x74), [1077](#)
- SMC_HSRUN
 - Power_s32k1xx, [981](#)
- SMC_RESERVED_RUN
 - Power_s32k1xx, [981](#)
- SMC_RESERVED_STOP1
 - Power_s32k1xx, [981](#)
- SMC_RUN
 - Power_s32k1xx, [981](#)
- SMC_STOP
 - Power_s32k1xx, [981](#)
- SMC_STOP1
 - Power_s32k1xx, [981](#)
- SMC_STOP2
 - Power_s32k1xx, [981](#)
- SMC_STOP_RESERVED
 - Power_s32k1xx, [981](#)
- SMC_VLPR
 - Power_s32k1xx, [981](#)
- SMC_VLPS
 - Power_s32k1xx, [981](#)
- SMPSC_ADDRESS

- Register address map, [1030](#)
- SMPSC_ON_NSR
 - 03. SMPS configuration, [222](#)
- SMPSC_ON_NSRS
 - 03. SMPS configuration, [222](#)
- SMPSC_PASS_THROUGH_NSS
 - 03. SMPS configuration, [222](#)
- SMPSOC_50V
 - 03. SMPS configuration, [222](#)
- SMPSOC_52V
 - 03. SMPS configuration, [222](#)
- SMPSOC_54V
 - 03. SMPS configuration, [222](#)
- SMPSOC_56V
 - 03. SMPS configuration, [222](#)
- SMPSOC_58V
 - 03. SMPS configuration, [223](#)
- SMPSOC_60V
 - 03. SMPS configuration, [223](#)
- SMPSOC_62V
 - 03. SMPS configuration, [223](#)
- SMPSOC_64V
 - 03. SMPS configuration, [223](#)
- SMPSOC_66V
 - 03. SMPS configuration, [223](#)
- SMPSOC_68V
 - 03. SMPS configuration, [223](#)
- SMPSOC_70V
 - 03. SMPS configuration, [223](#)
- SMPSOC_72V
 - 03. SMPS configuration, [223](#)
- SMPSOC_74V
 - 03. SMPS configuration, [223](#)
- SMPSOC_76V
 - 03. SMPS configuration, [223](#)
- SMPSOC_78V
 - 03. SMPS configuration, [223](#)
- SMPSOC_80V
 - 03. SMPS configuration, [223](#)
- SMPSOVC_ADDRESS
 - Register address map, [1030](#)
- SMPSSIE_DISABLE
 - Supply interrupt enable configuration options (0x1C), [1123](#)
- SMPSSIE_ENABLE
 - Supply interrupt enable configuration options (0x1C), [1123](#)
- SOFF
 - edma_software_tcd_t, [422](#)
- SPI_ACTIVE_HIGH
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1107](#)
- SPI_ACTIVE_LOW
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1107](#)
- SPI_GetDefaultMasterConfig
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1108](#)
- SPI_GetDefaultSlaveConfig
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1108](#)
- SPI_GetStatus
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1108](#)
- SPI_MasterDeinit
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1109](#)
- SPI_MasterInit
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1109](#)
- SPI_MasterSetDelay
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1109](#)
- SPI_MasterTransfer
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1109](#)
- SPI_MasterTransferBlocking
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1110](#)
- SPI_SetSS
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1110](#)
- SPI_SlaveDeinit
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1110](#)
- SPI_SlaveInit
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1111](#)
- SPI_SlaveTransfer
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1111](#)
- SPI_SlaveTransferBlocking
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1111](#)
- SPI_TRANSFER_LSB_FIRST
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1108](#)
- SPI_TRANSFER_MSB_FIRST
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1108](#)
- SPI_USING_DMA
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1108](#)
- SPI_USING_INTERRUPTS
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1108](#)
- SPIFIE_DISABLE
 - System interrupt enable configuration options (0x04), [1135](#)
- SPIFIE_ENABLE
 - System interrupt enable configuration options (0x04), [1135](#)
- ST_min
 - lin_node_attribute_t, [831](#)
- STAT_HSRUN
 - Power_s32k1xx, [980](#)

- STAT_INVALID
 - Power_s32k1xx, [980](#)
- STAT_RUN
 - Power_s32k1xx, [980](#)
- STAT_STOP
 - Power_s32k1xx, [980](#)
- STAT_VLPR
 - Power_s32k1xx, [980](#)
- STAT_VLPS
 - Power_s32k1xx, [980](#)
- STAT_VLPW
 - Power_s32k1xx, [980](#)
- STATUS_1000BASET_ADDR
 - Generic PHY, [665](#)
- STCD_ADDR
 - EDMA Driver, [422](#)
- STCD_SIZE
 - EDMA Driver, [422](#)
- STOP_MODE
 - Clock Manager Driver, [344](#)
- SUBFUNCTION_NOT_SUPPORTED
 - Common Transport Layer API, [359](#)
- SUCCESSFULL_TRANSFER
 - Common Core API., [356](#)
- SUPC_ADDRESS
 - Register address map, [1030](#)
- SUPIE_ADDRESS
 - Register address map, [1030](#)
- SUPIS_ADDRESS
 - Register address map, [1030](#)
- SUPVS_ADDRESS
 - Register address map, [1031](#)
- SUSPEND_WAIT_CNT
 - Flash Memory (Flash), [491](#)
- SYS_CLK_MAX_NO
 - Clock Manager Driver, [342](#)
- SYSIE_ADDRESS
 - Register address map, [1031](#)
- SYSIS_ADDRESS
 - Register address map, [1031](#)
- sa
 - WOLFSSL_SOCKADDR, [1371](#)
- safeState
 - ftm_independent_ch_param_t, [646](#)
- sai_master_clk_source_t
 - SAI Driver, [1042](#)
- sai_mux_mode_t
 - SAI Driver, [1042](#)
- sai_report_type_t
 - SAI Driver, [1042](#)
- sai_state_t, [1038](#)
- sai_sync_mode_t
 - SAI Driver, [1042](#)
- sai_transfer_callback_t
 - SAI Driver, [1041](#)
- sai_transfer_type_t
 - SAI Driver, [1043](#)
- sai_user_config_t, [1038](#)
- BitClkDiv, [1039](#)
- BitClkFreq, [1039](#)
- BitClkInternal, [1039](#)
- BitClkNegPolar, [1039](#)
- callback, [1039](#)
- callbackParam, [1039](#)
- ChannelCount, [1039](#)
- ChannelEnable, [1039](#)
- DmaChannel, [1039](#)
- ElementSize, [1040](#)
- FirstBitIndex, [1040](#)
- FrameSize, [1040](#)
- FrameStartReport, [1040](#)
- MasterClkSrc, [1040](#)
- MsbFirst, [1040](#)
- MuxMode, [1040](#)
- RunErrorReport, [1040](#)
- SyncEarly, [1040](#)
- SyncErrorReport, [1040](#)
- SyncInternal, [1040](#)
- SyncMode, [1041](#)
- SyncNegPolar, [1041](#)
- SyncWidth, [1041](#)
- TransferType, [1041](#)
- Word0Width, [1041](#)
- WordNWidth, [1041](#)
- sai_xfer_state_t, [1038](#)
- salt
 - __blake2b_param, [1244](#)
 - __blake2s_param, [1245](#)
- sampleDelay
 - qspi_user_config_t, [1313](#)
- samplePhase
 - qspi_user_config_t, [1313](#)
- sampleTicks
 - adc_config_t, [275](#)
- sampleTime
 - adc_converter_config_t, [256](#)
- samples
 - cmp_trigger_mode_t, [370](#)
- save_config_flg
 - lin_protocol_state_t, [842](#)
 - lin_word_status_str_t, [828](#)
- save_type
 - WOLFSSL_EVP_PKEY, [1363](#)
- saveArrays
 - Options, [1303](#)
- sbc_can_cfdc_t
 - UJA116xA SBC Driver, [1192](#)
- sbc_can_cmc_t
 - UJA116xA SBC Driver, [1192](#)
- sbc_can_conf_t, [1180](#)
 - canConf, [1180](#)
 - canTransEvtnt, [1180](#)
 - datRate, [1180](#)
 - dataMask, [1180](#)
 - frame, [1180](#)
 - identif, [1181](#)

- mask, [1181](#)
- sbc_can_cpnc_t
 - UJA116xA SBC Driver, [1192](#)
- sbc_can_ctr_t, [1178](#)
 - cfdc, [1178](#)
 - cmc, [1179](#)
 - cpnc, [1179](#)
 - pncok, [1179](#)
- sbc_can_pncok_t
 - UJA116xA SBC Driver, [1193](#)
- sbc_dat_rate_t
 - UJA116xA SBC Driver, [1193](#)
- sbc_data_mask_t
 - UJA116xA SBC Driver, [1191](#)
- sbc_evn_capt_t, [1189](#)
 - glEvt, [1189](#)
 - supEvt, [1189](#)
 - sysEvt, [1189](#)
 - transEvt, [1189](#)
 - wakePinEvt, [1189](#)
- sbc_factories_conf_t, [1183](#)
 - control, [1183](#)
 - startUp, [1183](#)
- sbc_fail_safe_lhc_t
 - UJA116xA SBC Driver, [1193](#)
- sbc_fail_safe_rcc_t
 - UJA116xA SBC Driver, [1191](#)
- sbc_frame_ctr_dlc_t
 - UJA116xA SBC Driver, [1191](#)
- sbc_frame_ctr_ide_t
 - UJA116xA SBC Driver, [1193](#)
- sbc_frame_ctr_pndm_t
 - UJA116xA SBC Driver, [1194](#)
- sbc_frame_t, [1179](#)
 - dlc, [1180](#)
 - ide, [1180](#)
 - pndm, [1180](#)
- sbc_gl_evt_stat_supe_t
 - UJA116xA SBC Driver, [1194](#)
- sbc_gl_evt_stat_syse_t
 - UJA116xA SBC Driver, [1194](#)
- sbc_gl_evt_stat_t, [1186](#)
 - supe, [1186](#)
 - syse, [1186](#)
 - trxe, [1186](#)
 - wpe, [1186](#)
- sbc_gl_evt_stat_trxe_t
 - UJA116xA SBC Driver, [1194](#)
- sbc_gl_evt_stat_wpe_t
 - UJA116xA SBC Driver, [1194](#)
- sbc_identif_mask_t
 - UJA116xA SBC Driver, [1192](#)
- sbc_identifier_t
 - UJA116xA SBC Driver, [1192](#)
- sbc_int_config_t, [1182](#)
 - can, [1182](#)
 - lhc, [1182](#)
 - lockMask, [1182](#)
 - mode, [1182](#)
 - regulatorCtr, [1182](#)
 - sysEvt, [1182](#)
 - wakePin, [1183](#)
 - watchdog, [1183](#)
- sbc_lock_t
 - UJA116xA SBC Driver, [1195](#)
- sbc_main_nms_t
 - UJA116xA SBC Driver, [1195](#)
- sbc_main_otws_t
 - UJA116xA SBC Driver, [1195](#)
- sbc_main_rss_t
 - UJA116xA SBC Driver, [1195](#)
- sbc_main_status_t, [1183](#)
 - nms, [1184](#)
 - otws, [1184](#)
 - rss, [1184](#)
- sbc_mode_mc_t
 - UJA116xA SBC Driver, [1196](#)
- sbc_mtpnv_stat_eccs_t
 - UJA116xA SBC Driver, [1196](#)
- sbc_mtpnv_stat_nvmps_t
 - UJA116xA SBC Driver, [1196](#)
- sbc_mtpnv_stat_t, [1189](#)
 - eccs, [1190](#)
 - nvmps, [1190](#)
 - wrcnts, [1190](#)
- sbc_mtpnv_stat_wrcnts_t
 - UJA116xA SBC Driver, [1192](#)
- sbc_register_t
 - UJA116xA SBC Driver, [1196](#)
- sbc_regulator_ctr_t, [1181](#)
 - regulator, [1181](#)
 - supplyEvt, [1182](#)
- sbc_regulator_pdc_t
 - UJA116xA SBC Driver, [1198](#)
- sbc_regulator_t, [1177](#)
 - pdc, [1177](#)
 - v1rtc, [1177](#)
 - v2c, [1177](#)
- sbc_regulator_v1rtc_t
 - UJA116xA SBC Driver, [1198](#)
- sbc_regulator_v2c_t
 - UJA116xA SBC Driver, [1198](#)
- sbc_sbc_fnmc_t
 - UJA116xA SBC Driver, [1198](#)
- sbc_sbc_sdmc_t
 - UJA116xA SBC Driver, [1199](#)
- sbc_sbc_slpc_t
 - UJA116xA SBC Driver, [1199](#)
- sbc_sbc_t, [1176](#)
 - fnmc, [1176](#)
 - sdmc, [1176](#)
 - slpc, [1176](#)
 - v1rtsuc, [1176](#)
- sbc_sbc_v1rtsuc_t
 - UJA116xA SBC Driver, [1199](#)
- sbc_start_up_rlc_t

- UJA116xA SBC Driver, [1199](#)
- sbc_start_up_t, [1176](#)
 - rlc, [1177](#)
 - v2suc, [1177](#)
- sbc_start_up_v2suc_t
 - UJA116xA SBC Driver, [1200](#)
- sbc_status_group_t, [1190](#)
 - events, [1190](#)
 - mainS, [1190](#)
 - supply, [1190](#)
 - trans, [1190](#)
 - wakePin, [1191](#)
 - wtdog, [1191](#)
- sbc_sup_evnt_stat_t, [1187](#)
 - v1u, [1187](#)
 - v2o, [1187](#)
 - v2u, [1187](#)
- sbc_sup_evnt_stat_v1u_t
 - UJA116xA SBC Driver, [1200](#)
- sbc_sup_evnt_stat_v2o_t
 - UJA116xA SBC Driver, [1200](#)
- sbc_sup_evnt_stat_v2u_t
 - UJA116xA SBC Driver, [1200](#)
- sbc_supply_evnt_t, [1177](#)
 - v1ue, [1177](#)
 - v2oe, [1178](#)
 - v2ue, [1178](#)
- sbc_supply_evnt_v1ue_t
 - UJA116xA SBC Driver, [1200](#)
- sbc_supply_evnt_v2oe_t
 - UJA116xA SBC Driver, [1201](#)
- sbc_supply_evnt_v2ue_t
 - UJA116xA SBC Driver, [1201](#)
- sbc_supply_stat_v1s_t
 - UJA116xA SBC Driver, [1201](#)
- sbc_supply_stat_v2s_t
 - UJA116xA SBC Driver, [1201](#)
- sbc_supply_status_t, [1184](#)
 - v1s, [1185](#)
 - v2s, [1185](#)
- sbc_sys_evnt_otwe_t
 - UJA116xA SBC Driver, [1201](#)
- sbc_sys_evnt_spife_t
 - UJA116xA SBC Driver, [1202](#)
- sbc_sys_evnt_stat_otw_t
 - UJA116xA SBC Driver, [1202](#)
- sbc_sys_evnt_stat_po_t
 - UJA116xA SBC Driver, [1202](#)
- sbc_sys_evnt_stat_spif_t
 - UJA116xA SBC Driver, [1202](#)
- sbc_sys_evnt_stat_t, [1186](#)
 - otw, [1187](#)
 - po, [1187](#)
 - spif, [1187](#)
 - wdf, [1187](#)
- sbc_sys_evnt_stat_wdf_t
 - UJA116xA SBC Driver, [1202](#)
- sbc_sys_evnt_t, [1178](#)
 - owte, [1178](#)
 - spife, [1178](#)
- sbc_trans_evnt_cbse_t
 - UJA116xA SBC Driver, [1203](#)
- sbc_trans_evnt_cfe_t
 - UJA116xA SBC Driver, [1203](#)
- sbc_trans_evnt_cwe_t
 - UJA116xA SBC Driver, [1203](#)
- sbc_trans_evnt_stat_cbs_t
 - UJA116xA SBC Driver, [1203](#)
- sbc_trans_evnt_stat_cf_t
 - UJA116xA SBC Driver, [1204](#)
- sbc_trans_evnt_stat_cw_t
 - UJA116xA SBC Driver, [1204](#)
- sbc_trans_evnt_stat_pnfde_t
 - UJA116xA SBC Driver, [1204](#)
- sbc_trans_evnt_stat_t, [1188](#)
 - cbs, [1188](#)
 - cf, [1188](#)
 - cw, [1188](#)
 - pnfde, [1188](#)
- sbc_trans_evnt_t, [1179](#)
 - cbse, [1179](#)
 - cfe, [1179](#)
 - cwe, [1179](#)
- sbc_trans_stat_cbss_t
 - UJA116xA SBC Driver, [1204](#)
- sbc_trans_stat_cfs_t
 - UJA116xA SBC Driver, [1204](#)
- sbc_trans_stat_coscs_t
 - UJA116xA SBC Driver, [1205](#)
- sbc_trans_stat_cpnerr_t
 - UJA116xA SBC Driver, [1205](#)
- sbc_trans_stat_cpns_t
 - UJA116xA SBC Driver, [1205](#)
- sbc_trans_stat_cts_t
 - UJA116xA SBC Driver, [1205](#)
- sbc_trans_stat_t, [1185](#)
 - cbss, [1185](#)
 - cfs, [1185](#)
 - coscs, [1185](#)
 - cpnerr, [1185](#)
 - cpns, [1185](#)
 - cts, [1186](#)
 - vcs, [1186](#)
- sbc_trans_stat_vcs_t
 - UJA116xA SBC Driver, [1205](#)
- sbc_wake_en_wpfe_t
 - UJA116xA SBC Driver, [1206](#)
- sbc_wake_en_wpre_t
 - UJA116xA SBC Driver, [1206](#)
- sbc_wake_evnt_stat_t, [1188](#)
 - wpf, [1188](#)
 - wpr, [1188](#)
- sbc_wake_evnt_stat_wpf_t
 - UJA116xA SBC Driver, [1206](#)
- sbc_wake_evnt_stat_wpr_t
 - UJA116xA SBC Driver, [1206](#)

- sbc_wake_stat_wpvs_t
 - UJA116xA SBC Driver, [1206](#)
- sbc_wake_t, [1181](#)
 - wpfe, [1181](#)
 - wpre, [1181](#)
- sbc_wtdog_ctr_nwp_t
 - UJA116xA SBC Driver, [1207](#)
- sbc_wtdog_ctr_t, [1175](#)
 - modeControl, [1175](#)
 - nominalPeriod, [1175](#)
- sbc_wtdog_ctr_wmc_t
 - UJA116xA SBC Driver, [1207](#)
- sbc_wtdog_stat_fnms_t
 - UJA116xA SBC Driver, [1207](#)
- sbc_wtdog_stat_sdms_t
 - UJA116xA SBC Driver, [1208](#)
- sbc_wtdog_stat_wds_t
 - UJA116xA SBC Driver, [1208](#)
- sbc_wtdog_status_t, [1184](#)
 - fnms, [1184](#)
 - sdms, [1184](#)
 - wds, [1184](#)
- sbcConfigCtrl
 - uja113x_mtpnv_cfg_t, [247](#)
- scatterGatherEnable
 - edma_transfer_config_t, [420](#)
- scatterGatherNextDescAddr
 - edma_transfer_config_t, [420](#)
- scg_async_clock_div_t
 - Clock Manager Driver, [344](#)
- scg_clock_mode_config_t, [332](#)
 - alternateClock, [333](#)
 - hccrConfig, [333](#)
 - initialize, [333](#)
 - rccrConfig, [333](#)
 - vccrConfig, [333](#)
- scg_clockout_config_t, [333](#)
 - initialize, [333](#)
 - source, [333](#)
- scg_clockout_src_t
 - Clock Manager Driver, [344](#)
- scg_config_t, [333](#)
 - clockModeConfig, [334](#)
 - clockOutConfig, [334](#)
 - fircConfig, [334](#)
 - rtcConfig, [334](#)
 - sircConfig, [334](#)
 - soscConfig, [334](#)
 - spllConfig, [334](#)
- scg_firc_config_t, [330](#)
 - div1, [330](#)
 - div2, [330](#)
 - enableInLowPower, [330](#)
 - enableInStop, [330](#)
 - initialize, [331](#)
 - locked, [331](#)
 - range, [331](#)
 - regulator, [331](#)
- scg_firc_range_t
 - Clock Manager Driver, [344](#)
- scg_rtc_config_t, [332](#)
 - initialize, [332](#)
 - rtcClkInFreq, [332](#)
- scg_sirc_config_t, [329](#)
 - div1, [329](#)
 - div2, [329](#)
 - enableInLowPower, [329](#)
 - enableInStop, [330](#)
 - initialize, [330](#)
 - locked, [330](#)
 - range, [330](#)
- scg_sirc_range_t
 - Clock Manager Driver, [345](#)
- scg_sosc_config_t, [328](#)
 - div1, [328](#)
 - div2, [328](#)
 - enableInLowPower, [328](#)
 - enableInStop, [328](#)
 - extRef, [328](#)
 - freq, [328](#)
 - gain, [329](#)
 - initialize, [329](#)
 - locked, [329](#)
 - monitorMode, [329](#)
 - range, [329](#)
- scg_sosc_ext_ref_t
 - Clock Manager Driver, [345](#)
- scg_sosc_gain_t
 - Clock Manager Driver, [345](#)
- scg_sosc_monitor_mode_t
 - Clock Manager Driver, [345](#)
- scg_sosc_range_t
 - Clock Manager Driver, [345](#)
- scg_spill_clock_multiply_t
 - Clock Manager Driver, [345](#)
- scg_spill_clock_prediv_t
 - Clock Manager Driver, [346](#)
- scg_spill_config_t, [331](#)
 - div1, [331](#)
 - div2, [331](#)
 - enableInStop, [331](#)
 - initialize, [332](#)
 - locked, [332](#)
 - monitorMode, [332](#)
 - mult, [332](#)
 - prediv, [332](#)
 - src, [332](#)
- scg_spill_monitor_mode_t
 - Clock Manager Driver, [347](#)
- scg_system_clock_config_t, [327](#)
 - divBus, [327](#)
 - divCore, [327](#)
 - divSlow, [327](#)
 - src, [328](#)
- scg_system_clock_div_t
 - Clock Manager Driver, [347](#)

scg_system_clock_src_t
 Clock Manager Driver, 347
 scgConfig
 clock_manager_user_config_t, 337
 sch_tbl_type
 lin_schedule_t, 833
 Schedule management, 1079
 l_sch_set, 1079
 l_sch_tick, 1079
 schedule_start
 lin_protocol_user_config_t, 839
 schedule_start_entry_ptr
 lin_master_data_t, 840
 schedule_tbl
 lin_protocol_user_config_t, 839
 sckPin
 extension_flexio_for_i2s_t, 678
 extension_flexio_for_spi_t, 1107
 flexio_i2s_master_user_config_t, 544
 flexio_i2s_slave_user_config_t, 545
 flexio_spi_master_user_config_t, 562
 flexio_spi_slave_user_config_t, 564
 SckeArgs, 1317
 encSecret, 1318
 encSz, 1318
 input, 1318
 inputSz, 1318
 length, 1318
 output, 1318
 sendSz, 1318
 sclPin
 extension_flexio_for_i2c_t, 696
 flexio_i2c_master_user_config_t, 534
 ScvArgs, 1318
 extraSz, 1319
 idx, 1319
 input, 1319
 inputSz, 1319
 length, 1319
 output, 1319
 sendSz, 1319
 sigAlgo, 1319
 sigSz, 1319
 verify, 1319
 verifySig, 1319
 sdaPin
 extension_flexio_for_i2c_t, 696
 flexio_i2c_master_user_config_t, 534
 sdmc
 sbc_sbc_t, 1176
 sdms
 sbc_wtdog_status_t, 1184
 secondChannelPolarity
 ftm_combined_ch_param_t, 647
 ftm_independent_ch_param_t, 646
 secondChannelSafeState
 ftm_combined_ch_param_t, 647
 secondEdge
 ftm_combined_ch_param_t, 647
 secondIntConfig
 rtc_seconds_int_config_t, 1004
 secondIntEnable
 rtc_seconds_int_config_t, 1004
 seconds
 rtc_timedate_t, 1001
 secondsCallbackParams
 rtc_seconds_int_config_t, 1004
 sectorEraseCount
 Flash Memory (Flash), 502
 Security PAL, 1080
 SECURITY_BOOT_MAC, 1084
 SECURITY_BOOT_MAC_KEY, 1084
 SECURITY_BOOT_NOT_DEFINED, 1083
 SECURITY_BOOT_PARALLEL, 1082
 SECURITY_BOOT_SERIAL, 1082
 SECURITY_BOOT_STRICT, 1082
 SECURITY_BootDefine, 1084
 SECURITY_BootFailure, 1084
 SECURITY_BootOk, 1085
 SECURITY_CMD_BOOT_DEFINE, 1083
 SECURITY_CMD_BOOT_FAILURE, 1083
 SECURITY_CMD_BOOT_OK, 1083
 SECURITY_CMD_DBG_AUTH, 1083
 SECURITY_CMD_DBG_CHAL, 1083
 SECURITY_CMD_DEC_CBC, 1083
 SECURITY_CMD_DEC_ECB, 1083
 SECURITY_CMD_ENC_CBC, 1083
 SECURITY_CMD_ENC_ECB, 1083
 SECURITY_CMD_EXPORT_RAM_KEY, 1083
 SECURITY_CMD_EXTEND_SEED, 1083
 SECURITY_CMD_GENERATE_MAC, 1083
 SECURITY_CMD_GET_ID, 1083
 SECURITY_CMD_INIT_RNG, 1083
 SECURITY_CMD_LOAD_KEY, 1083
 SECURITY_CMD_LOAD_PLAIN_KEY, 1083
 SECURITY_CMD_MP_COMPRESS, 1083
 SECURITY_CMD_RESERVED_1, 1083
 SECURITY_CMD_RESERVED_2, 1083
 SECURITY_CMD_RESERVED_3, 1083
 SECURITY_CMD_RND, 1083
 SECURITY_CMD_VERIFY_MAC, 1083
 SECURITY_CancelCommand, 1085
 SECURITY_DbgAuth, 1085
 SECURITY_DbgChal, 1085
 SECURITY_DecryptCbc, 1086
 SECURITY_DecryptCbcBlocking, 1086
 SECURITY_DecryptEcb, 1087
 SECURITY_DecryptEcbBlocking, 1087
 SECURITY_Deinit, 1087
 SECURITY_EncryptCbc, 1088
 SECURITY_EncryptCbcBlocking, 1088
 SECURITY_EncryptEcb, 1088
 SECURITY_EncryptEcbBlocking, 1089
 SECURITY_ExportRamKey, 1089
 SECURITY_ExtendSeed, 1090
 SECURITY_GenerateMac, 1090

- SECURITY_GenerateMacBlocking, [1090](#)
- SECURITY_GenerateRnd, [1092](#)
- SECURITY_GenerateTrnd, [1092](#)
- SECURITY_GetAsyncCmdStatus, [1092](#)
- SECURITY_GetDefaultConfig, [1093](#)
- SECURITY_GetId, [1093](#)
- SECURITY_INSTANCE0, [1083](#)
- SECURITY_Init, [1093](#)
- SECURITY_InitRng, [1093](#)
- SECURITY_KEY_1, [1084](#)
- SECURITY_KEY_10, [1084](#)
- SECURITY_KEY_11, [1084](#)
- SECURITY_KEY_12, [1084](#)
- SECURITY_KEY_13, [1084](#)
- SECURITY_KEY_14, [1084](#)
- SECURITY_KEY_15, [1084](#)
- SECURITY_KEY_16, [1084](#)
- SECURITY_KEY_17, [1084](#)
- SECURITY_KEY_2, [1084](#)
- SECURITY_KEY_3, [1084](#)
- SECURITY_KEY_4, [1084](#)
- SECURITY_KEY_5, [1084](#)
- SECURITY_KEY_6, [1084](#)
- SECURITY_KEY_7, [1084](#)
- SECURITY_KEY_8, [1084](#)
- SECURITY_KEY_9, [1084](#)
- SECURITY_LoadKey, [1095](#)
- SECURITY_LoadPlainKey, [1095](#)
- SECURITY_MASTER_ECU, [1083](#)
- SECURITY_MPCompress, [1095](#)
- SECURITY_RAM_KEY, [1084](#)
- SECURITY_SECRET_KEY, [1083](#)
- SECURITY_SecureBoot, [1096](#)
- SECURITY_VerifyMac, [1096](#)
- SECURITY_VerifyMacBlocking, [1097](#)
- security_boot_flavor_t, [1082](#)
- security_cmd_t, [1083](#)
- security_instance_t, [1083](#)
- security_key_id_t, [1083](#)
- Security Peripheral Abstraction Layer - SECURITY PAL, [1098](#)
- security_boot_flavor_t
 - Security PAL, [1082](#)
- security_cmd_t
 - Security PAL, [1083](#)
- security_instance_t
 - Security PAL, [1083](#)
- security_key_id_t
 - Security PAL, [1083](#)
- security_user_config_t, [1082](#)
 - callback, [1082](#)
 - callbackParam, [1082](#)
- seed
 - crc_user_config_t, [290](#)
 - WC_RNG, [1333](#)
- selectTestMode
 - phy_driver_t, [949](#)
 - TJA110x PHY, [1145](#)
- send_functional_request_flg
 - lin_master_data_t, [841](#)
- send_slave_res_flg
 - lin_master_data_t, [841](#)
- sendAlertState
 - Options, [1303](#)
- sendSz
 - DcvArgs, [1264](#)
 - SckeArgs, [1318](#)
 - ScvArgs, [1319](#)
 - SskeArgs, [1326](#)
- sendVerify
 - Options, [1303](#)
 - WOLFSSL_CTX, [1354](#)
- sentNotify
 - Options, [1303](#)
- seq
 - csec_state_t, [301](#)
 - DtlsMsg, [1280](#)
- seqErrIntEnable
 - pdb_timer_config_t, [933](#)
- sequence_number
 - DtlsRecordLayerHeader, [1280](#)
- sequence_number_hi
 - Keys, [1291](#)
- sequence_number_lo
 - Keys, [1292](#)
- serial
 - DecodedCert, [1268](#)
 - WOLFSSL_X509, [1374](#)
- Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1101](#)
 - READ_ON_EVEN_EDGE, [1107](#)
 - READ_ON_ODD_EDGE, [1107](#)
 - SPI_ACTIVE_HIGH, [1107](#)
 - SPI_ACTIVE_LOW, [1107](#)
 - SPI_GetDefaultMasterConfig, [1108](#)
 - SPI_GetDefaultSlaveConfig, [1108](#)
 - SPI_GetStatus, [1108](#)
 - SPI_MasterDeinit, [1109](#)
 - SPI_MasterInit, [1109](#)
 - SPI_MasterSetDelay, [1109](#)
 - SPI_MasterTransfer, [1109](#)
 - SPI_MasterTransferBlocking, [1110](#)
 - SPI_SetSS, [1110](#)
 - SPI_SlaveDeinit, [1110](#)
 - SPI_SlaveInit, [1111](#)
 - SPI_SlaveTransfer, [1111](#)
 - SPI_SlaveTransferBlocking, [1111](#)
 - SPI_TRANSFER_LSB_FIRST, [1108](#)
 - SPI_TRANSFER_MSB_FIRST, [1108](#)
 - SPI_USING_DMA, [1108](#)
 - SPI_USING_INTERRUPTS, [1108](#)
 - spi_clock_phase_t, [1107](#)
 - spi_polarity_t, [1107](#)
 - spi_transfer_bit_order_t, [1107](#)
 - spi_transfer_type_t, [1108](#)
- serial_0

- lin_serial_number_t, [829](#)
- serial_1
 - lin_serial_number_t, [829](#)
- serial_2
 - lin_serial_number_t, [829](#)
- serial_3
 - lin_serial_number_t, [829](#)
- serial_number
 - lin_node_attribute_t, [831](#)
- serialIdx
 - DecodedName, [1271](#)
- serialLen
 - DecodedName, [1271](#)
- serialNumber
 - WOLFSSL_X509_REVOKED, [1377](#)
- serialSz
 - DecodedCert, [1268](#)
 - WOLFSSL_X509, [1374](#)
- server_hint
 - Arrays, [1250](#)
 - WOLFSSL_CTX, [1354](#)
- server_psk_cb
 - Options, [1303](#)
 - WOLFSSL_CTX, [1354](#)
- server_write_IV
 - Keys, [1292](#)
- server_write_MAC_secret
 - Keys, [1292](#)
- server_write_key
 - Keys, [1292](#)
- serverDH_G
 - Buffers, [1252](#)
 - WOLFSSL_CTX, [1354](#)
- serverDH_Key
 - Buffers, [1253](#)
- serverDH_P
 - Buffers, [1253](#)
 - WOLFSSL_CTX, [1354](#)
- serverDH_Priv
 - Buffers, [1253](#)
- serverDH_Pub
 - Buffers, [1253](#)
- serverID
 - WOLFSSL_SESSION, [1369](#)
- serverIdx
 - ClientSession, [1260](#)
- serverRandom
 - Arrays, [1250](#)
- serverRow
 - ClientSession, [1260](#)
- serverState
 - Options, [1304](#)
- service_flags_ptr
 - lin_node_attribute_t, [831](#)
- service_status
 - lin_tl_descriptor_t, [837](#)
- service_supported_ptr
 - lin_node_attribute_t, [831](#)
- session
 - WOLFSSL, [1339](#)
- sessionCacheFlushOff
 - Options, [1304](#)
 - WOLFSSL_CTX, [1354](#)
- sessionCacheOff
 - Options, [1304](#)
 - WOLFSSL_CTX, [1354](#)
- sessionID
 - Arrays, [1250](#)
 - WOLFSSL_SESSION, [1369](#)
- sessionIDSz
 - Arrays, [1250](#)
 - WOLFSSL_SESSION, [1369](#)
- SessionRow, [1319](#)
 - nextIdx, [1320](#)
 - Sessions, [1320](#)
 - totalCount, [1320](#)
- Sessions
 - SessionRow, [1320](#)
- set
 - EncryptedInfo, [1281](#)
- setLoopback
 - Generic PHY, [666](#)
 - phy_driver_t, [949](#)
 - TJA110x PHY, [1145](#)
- setManagedOperation
 - TJA110x PHY, [1145](#)
- setRole
 - Generic PHY, [666](#)
 - phy_driver_t, [950](#)
 - TJA110x PHY, [1145](#)
- setSuites
 - Suites, [1328](#)
- setup
 - Ciphers, [1258](#)
- sflImpactReg
 - fs45_drv_config_t, [1062](#)
- Sha, [1320](#)
 - buffLen, [1320](#)
 - buffer, [1320](#)
 - digest, [1320](#)
 - heap, [1320](#)
 - hiLen, [1320](#)
 - loLen, [1321](#)
- sha
 - Hash, [1285](#)
 - Hashes, [1286](#)
 - WOLFSSL_Hasher, [1364](#)
 - wc_HashAlg, [1332](#)
- Sha256, [1321](#)
 - buffLen, [1321](#)
 - buffer, [1321](#)
 - digest, [1321](#)
 - heap, [1321](#)
 - hiLen, [1321](#)
 - loLen, [1321](#)
- sha256

- Hash, [1285](#)
- Hashes, [1286](#)
- WOLFSSL_Hasher, [1364](#)
- wc_HashAlg, [1332](#)
- side
 - Options, [1304](#)
 - qspi_user_config_t, [1313](#)
 - WOLFSSL_METHOD, [1366](#)
- sig
 - Buffers, [1253](#)
 - CertSignCtx, [1257](#)
 - WOLFSSL_X509, [1374](#)
- sig_algo
 - CipherSpecs, [1259](#)
- sigAlgo
 - DcvArgs, [1264](#)
 - DskeArgs, [1277](#)
 - ScvArgs, [1319](#)
 - Suites, [1328](#)
- sigCtx
 - DecodedCert, [1268](#)
- sigDataBuf
 - SskeArgs, [1327](#)
- sigDataSz
 - SskeArgs, [1327](#)
- sigIndex
 - DecodedCert, [1268](#)
- sigLength
 - DecodedCert, [1268](#)
- sigOID
 - WOLFSSL_X509, [1374](#)
- sigSz
 - DckeArgs, [1263](#)
 - DcvArgs, [1264](#)
 - DskeArgs, [1277](#)
 - ScvArgs, [1319](#)
 - SskeArgs, [1327](#)
- sign
 - fp_int, [1282](#)
 - mp_int, [1295](#)
- signal
 - func_args, [1284](#)
- Signal interaction, [1113](#)
- signature
 - CRL_Entry, [1261](#)
 - DecodedCert, [1268](#)
- SignatureCtx, [1322](#)
 - devId, [1322](#)
 - digest, [1322](#)
 - digestSz, [1322](#)
 - heap, [1322](#)
 - key, [1322](#)
 - keyOID, [1322](#)
 - out, [1322](#)
 - plain, [1322](#)
 - ptr, [1322](#)
 - rsa, [1323](#)
 - state, [1323](#)
 - typeH, [1323](#)
 - signatureOID
 - CRL_Entry, [1261](#)
 - DecodedCert, [1268](#)
 - signatureSz
 - CRL_Entry, [1261](#)
 - Signer, [1323](#)
 - excludedNames, [1323](#)
 - keyOID, [1323](#)
 - keyUsage, [1323](#)
 - name, [1323](#)
 - nameLen, [1324](#)
 - next, [1324](#)
 - pathLength, [1324](#)
 - pathLengthSet, [1324](#)
 - permittedNames, [1324](#)
 - pubKeySize, [1324](#)
 - publicKey, [1324](#)
 - subjectKeyIdHash, [1324](#)
 - subjectNameHash, [1324](#)
 - signer_ca
 - t_atcert, [1328](#)
 - signer_ca_pubkey
 - t_atcert, [1328](#)
 - signer_ca_size
 - t_atcert, [1329](#)
- sim_clkout_div_t
 - Clock Manager Driver, [347](#)
- sim_clkout_src_t
 - Clock Manager Driver, [348](#)
- sim_clock_config_t, [326](#)
 - clockOutConfig, [327](#)
 - lpoClockConfig, [327](#)
 - platGateConfig, [327](#)
 - qspiRefClkGating, [327](#)
 - tlkConfig, [327](#)
 - traceClockConfig, [327](#)
- sim_clock_out_config_t, [323](#)
 - divider, [323](#)
 - enable, [323](#)
 - initialize, [323](#)
 - source, [323](#)
- sim_lpo_clock_config_t, [323](#)
 - enableLpo1k, [324](#)
 - enableLpo32k, [324](#)
 - initialize, [324](#)
 - sourceLpoClk, [324](#)
 - sourceRtcClk, [324](#)
- sim_lpclock_sel_src_t
 - Clock Manager Driver, [348](#)
- sim_plat_gate_config_t, [324](#)
 - enableDma, [325](#)
 - enableEim, [325](#)
 - enableErm, [325](#)
 - enableMpu, [325](#)
 - enableMscm, [325](#)
 - initialize, [325](#)
- sim_qspi_ref_clk_gating_t, [325](#)

- enableQspiRefClk, [325](#)
- sim_rtc_clk_sel_src_t
 - Clock Manager Driver, [348](#)
- sim_tclk_config_t, [324](#)
 - extPinSrc, [324](#)
 - initialize, [324](#)
 - tclkFreq, [324](#)
- sim_trace_clock_config_t, [326](#)
 - divEnable, [326](#)
 - divFraction, [326](#)
 - divider, [326](#)
 - initialize, [326](#)
 - source, [326](#)
- simConfig
 - clock_manager_user_config_t, [337](#)
- sircConfig
 - scg_config_t, [334](#)
- size
 - BuildMsgArgs, [1255](#)
- sizes
 - qspi_ahb_config_t, [1310](#)
- slave_ifc_handle
 - lin_protocol_user_config_t, [839](#)
- slave_resp_cnt
 - lin_tl_descriptor_t, [837](#)
- slaveAddress
 - flexio_i2c_master_user_config_t, [535](#)
 - i2c_master_t, [697](#)
 - i2c_slave_t, [698](#)
 - lpi2c_master_user_config_t, [746](#)
 - lpi2c_slave_user_config_t, [747](#)
- slaveCallback
 - lpi2c_slave_user_config_t, [747](#)
- slaveListening
 - i2c_slave_t, [698](#)
 - lpi2c_slave_user_config_t, [747](#)
- sleep
 - phy_driver_t, [950](#)
 - TJA110x PHY, [1145](#)
- sleepAbortReject
 - phy_driver_t, [950](#)
 - TJA110x PHY, [1146](#)
- sleepOnExitValue
 - power_manager_user_config_t, [979](#)
- sleepRequestCB
 - phy_config_t, [947](#)
- slpc
 - sbc_sbc_t, [1176](#)
- smc_power_mode_config_t, [979](#)
 - powerModeName, [979](#)
- smc_power_mode_protection_config_t, [979](#)
 - vlpProt, [979](#)
- smc_run_mode_t
 - Power_s32k1xx, [981](#)
- smc_stop_mode_t
 - Power_s32k1xx, [981](#)
- smc_stop_option_t
 - Power_s32k1xx, [981](#)
- smpsCtrl
 - uja113x_smpsc_cfg_t, [222](#)
- smpsOutVolt
 - uja113x_smpsc_cfg_t, [222](#)
- smpsOvertempCtrl
 - uja113x_smpsc_cfg_t, [222](#)
- smpscSmpsCfg
 - uja113x_init_cfg_t, [185](#)
- smtp_send_request, [1324](#)
 - body, [1325](#)
 - callback_arg, [1325](#)
 - callback_fn, [1325](#)
 - from, [1325](#)
 - static_data, [1325](#)
 - subject, [1325](#)
 - to, [1325](#)
- snIdx
 - DecodedName, [1271](#)
- snLen
 - DecodedName, [1271](#)
- SoC Header file (SoC Header), [1114](#)
- SoC Support, [1115](#)
- softwareSync
 - ftm_pwm_sync_t, [590](#)
- soscConfig
 - scg_config_t, [334](#)
- source
 - DecodedCert, [1268](#)
 - module_clk_config_t, [337](#)
 - scg_clockout_config_t, [333](#)
 - sim_clock_out_config_t, [323](#)
 - sim_trace_clock_config_t, [326](#)
- sourceClock
 - pwm_ftm_timebase_t, [988](#)
- sourceLpoClk
 - sim_lpo_clock_config_t, [324](#)
- sourceRtcClk
 - sim_lpo_clock_config_t, [324](#)
- specs
 - WOLFSSL, [1339](#)
- speed
 - phy_config_t, [947](#)
- spi_clock_phase_t
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1107](#)
- spi_instance_t, [1325](#)
 - instIdx, [1326](#)
 - instType, [1326](#)
- spi_master_t, [1104](#)
 - baudRate, [1104](#)
 - bitOrder, [1104](#)
 - callback, [1104](#)
 - callbackParam, [1104](#)
 - clockPhase, [1104](#)
 - clockPolarity, [1104](#)
 - extension, [1104](#)
 - frameSize, [1105](#)
 - rxDMAChannel, [1105](#)

- ssPin, [1105](#)
- ssPolarity, [1105](#)
- transferType, [1105](#)
- txDMAChannel, [1105](#)
- spi_polarity_t
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1107](#)
- spi_slave_t, [1105](#)
 - bitOrder, [1105](#)
 - callback, [1106](#)
 - callbackParam, [1106](#)
 - clockPhase, [1106](#)
 - clockPolarity, [1106](#)
 - extension, [1106](#)
 - frameSize, [1106](#)
 - rxDMAChannel, [1106](#)
 - ssPolarity, [1106](#)
 - transferType, [1106](#)
 - txDMAChannel, [1106](#)
- spi_transfer_bit_order_t
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1107](#)
- spi_transfer_type_t
 - Serial Peripheral Interface - Peripheral Abstraction Layer(SPI PAL), [1108](#)
- spif
 - sbc_sys_evt_stat_t, [1187](#)
- spife
 - sbc_sys_evt_t, [1178](#)
- spilConfig
 - scg_config_t, [334](#)
- src
 - scg_spil_config_t, [332](#)
 - scg_system_clock_config_t, [328](#)
 - sys_clk_config_t, [338](#)
- srcAddr
 - edma_transfer_config_t, [420](#)
- srcIdx
 - DecodedCert, [1268](#)
- srcLastAddrAdjust
 - edma_transfer_config_t, [420](#)
- srcModulo
 - edma_transfer_config_t, [421](#)
- srcOffset
 - edma_transfer_config_t, [421](#)
- srcOffsetEnable
 - edma_loop_transfer_config_t, [419](#)
- srcTransferSize
 - edma_transfer_config_t, [421](#)
- srfName
 - tcp_ready, [1329](#)
- ssPin
 - extension_flexio_for_spi_t, [1107](#)
 - flexio_spi_master_user_config_t, [562](#)
 - flexio_spi_slave_user_config_t, [564](#)
 - spi_master_t, [1105](#)
- ssPolarity
 - spi_master_t, [1105](#)
 - spi_slave_t, [1106](#)
- SskeArgs, [1326](#)
 - idx, [1326](#)
 - length, [1326](#)
 - output, [1326](#)
 - sendSz, [1326](#)
 - sigDataBuf, [1327](#)
 - sigDataSz, [1327](#)
 - sigSz, [1327](#)
 - tmpSigSz, [1327](#)
 - verifySig, [1327](#)
- ssl
 - handShakeInfo_st, [1285](#)
 - WOLFSSL_BIO, [1345](#)
 - WOLFSSL_CIPHER, [1349](#)
- ssl_ready
 - callback_functions, [1256](#)
- stIdx
 - DecodedName, [1271](#)
- stLen
 - DecodedName, [1271](#)
- Start-up control configuration options (0x73), [1117](#)
 - IO2SFC_LIMP_HOME, [1118](#)
 - IO2SFC_STD_IO, [1118](#)
 - IO3SFC_LIMP_HOME, [1118](#)
 - IO3SFC_STD_IO, [1118](#)
 - IO4SFC_LIMP_HOME, [1118](#)
 - IO4SFC_STD_IO, [1118](#)
 - RLC_PULSE_WIDTH_01_MS, [1118](#)
 - RLC_PULSE_WIDTH_03_05_MS, [1118](#)
 - RLC_PULSE_WIDTH_10_12_MS, [1118](#)
 - RLC_PULSE_WIDTH_20_25_MS, [1118](#)
 - V2SUC_ALWAYS_OFF, [1119](#)
 - V2SUC_ALWAYS_ON, [1119](#)
- startAddr
 - mpu_region_config_t, [875](#)
 - mpu_user_config_t, [863](#)
- startUp
 - sbc_factories_conf_t, [1183](#)
- startupCtrl
 - uja113x_mtpnv_cfg_t, [247](#)
- state
 - Arc4, [1249](#)
 - CertSignCtx, [1257](#)
 - Ciphers, [1258](#)
 - cmp_dac_t, [369](#)
 - flexcan_mb_handle_t, [514](#)
 - RsaKey, [1317](#)
 - SignatureCtx, [1323](#)
 - WOLF_EVENT, [1335](#)
- static_data
 - smtp_send_request, [1325](#)
- static_ecdh
 - CipherSpecs, [1259](#)
- staticBuffer
 - bufferStatic, [1254](#)
- staticCallbacks
 - power_manager_state_t, [969](#)

- staticCallbacksNumber
 - power_manager_state_t, 969
- staticName
 - WOLFSSL_X509_NAME, 1376
- staticTicket
 - WOLFSSL_SESSION, 1369
- status
 - edma_chn_state_t, 416
 - lpspi_state_t, 779
 - OcspEntry, 1299
 - WC_RNG, 1333
- statusRegisterLock
 - rtc_register_lock_config_t, 1005
- stop
 - wdg_option_mode_t, 1224
 - wdog_op_mode_t, 1233
- stopBitCount
 - lpuart_user_config_t, 807
 - uart_user_config_t, 1215
- store
 - WOLFSSL_X509_LOOKUP, 1375
 - WOLFSSL_X509_STORE_CTX, 1379
- string
 - WOLFSSL_STACK, 1372
- Structural Core Self Test, 1120
- subject
 - DecodedCert, 1268
 - smtp_send_request, 1325
 - WOLFSSL_X509, 1374
- subjectCN
 - DecodedCert, 1268
 - WOLFSSL_X509, 1374
- subjectCNEnc
 - DecodedCert, 1269
- subjectCNLen
 - DecodedCert, 1269
- subjectCNStored
 - DecodedCert, 1269
- subjectHash
 - DecodedCert, 1269
- subjectKeyIdHash
 - Signer, 1324
- subjectNameHash
 - Signer, 1324
- subjectRaw
 - DecodedCert, 1269
- subjectRawLen
 - DecodedCert, 1269
- successful_transfer
 - lin_protocol_state_t, 842
 - lin_word_status_str_t, 828
- suiteSz
 - Suites, 1328
- Suites, 1327
 - hashAlgo, 1327
 - hashSigAlgo, 1327
 - hashSigAlgoSz, 1327
 - setSuites, 1328
 - sigAlgo, 1328
 - suiteSz, 1328
 - suites, 1328
- suites
 - Suites, 1328
 - WOLFSSL, 1339
 - WOLFSSL_CTX, 1354
- supEvt
 - sbc_evn_capt_t, 1189
- supe
 - sbc_gl_evt_stat_t, 1186
- supervisorReg
 - fs45_drv_config_t, 1062
- supieMask
 - uja113x_init_cfg_t, 185
- supplier_id
 - lin_product_id_t, 1292
- supply
 - sbc_status_group_t, 1190
- Supply interrupt enable configuration options (0x1C), 1122
 - BMOIE_DISABLE, 1123
 - BMOIE_ENABLE, 1123
 - BMUIE_DISABLE, 1123
 - BMUIE_ENABLE, 1123
 - SMPSSIE_DISABLE, 1123
 - SMPSSIE_ENABLE, 1123
 - V1UIE_DISABLE, 1123
 - V1UIE_ENABLE, 1123
 - VEXTIOE_DISABLE, 1123
 - VEXTIOE_ENABLE, 1123
 - VEXTUIE_DISABLE, 1124
 - VEXTUIE_ENABLE, 1124
- supplyEvt
 - sbc_regulator_ctr_t, 1182
- supplyMonitoringEnable
 - adc_converter_config_t, 256
 - extension_adc_s32k1xx_t, 276
- suspend
 - Generic PHY, 666
 - phy_driver_t, 950
- SyncEarly
 - sai_user_config_t, 1040
- SyncErrorReport
 - sai_user_config_t, 1040
- SyncInternal
 - sai_user_config_t, 1040
- syncMethod
 - ftm_user_config_t, 591
- SyncMode
 - sai_user_config_t, 1041
- SyncNegPolar
 - sai_user_config_t, 1041
- syncPoint
 - ftm_pwm_sync_t, 590
- SyncWidth
 - sai_user_config_t, 1041
- Synchronous Audio Interface (SAI), 1125

- sys_clk_config_t, [337](#)
 - dividers, [338](#)
 - src, [338](#)
- sysEvt
 - sbc_evn_capt_t, [1189](#)
 - sbc_int_config_t, [1182](#)
- syse
 - sbc_gl_evnt_stat_t, [1186](#)
- sysieMask
 - uja113x_init_cfg_t, [185](#)
- System Basis Chip Driver (SBC) - FS45xx Family, [1126](#)
- System Basis Chip Driver (SBC) - UJA116xA Family, [1129](#)
- System Basis Chip library (SBC) - UJA113x Family, [1134](#)
- System interrupt enable configuration options (0x04), [1135](#)
 - OTWIE_DISABLE, [1135](#)
 - OTWIE_ENABLE, [1135](#)
 - SPIFIE_DISABLE, [1135](#)
 - SPIFIE_ENABLE, [1135](#)
- sz
 - BuildMsgArgs, [1255](#)
 - DcvArgs, [1264](#)
 - DtlsMsg, [1280](#)
 - WOLFSSL_SOCKADDR, [1371](#)
 - WOLFSSL_X509_NAME, [1376](#)
- T
 - HC128, [1287](#)
- T_RST_MAX
 - Generic PHY, [665](#)
- t_atcert, [1328](#)
 - end_user, [1328](#)
 - end_user_pubkey, [1328](#)
 - end_user_size, [1328](#)
 - signer_ca, [1328](#)
 - signer_ca_pubkey, [1328](#)
 - signer_ca_size, [1329](#)
- TIE_ADDRESS
 - Register address map, [1031](#)
- TIM1C_ADDRESS
 - Register address map, [1031](#)
- TIM1DCC_ADDRESS
 - Register address map, [1031](#)
- TIM2C_ADDRESS
 - Register address map, [1031](#)
- TIM2DCC_ADDRESS
 - Register address map, [1031](#)
- TIM3C_ADDRESS
 - Register address map, [1031](#)
- TIM3DCC_ADDRESS
 - Register address map, [1031](#)
- TIM4C_ADDRESS
 - Register address map, [1031](#)
- TIM4DCC_ADDRESS
 - Register address map, [1032](#)
- TIMER_CHAN_TYPE_CONTINUOUS
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1161](#)
- TIMER_CHAN_TYPE_ONESHOT
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1161](#)
- TIMER_RESOLUTION_TYPE_MICROSECOND
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1161](#)
- TIMER_RESOLUTION_TYPE_MILLISECOND
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1161](#)
- TIMER_RESOLUTION_TYPE_NANOSECOND
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1161](#)
- TIMING_Deinit
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1161](#)
- TIMING_DisableNotification
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1161](#)
- TIMING_EnableNotification
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1161](#)
- TIMING_GetElapsed
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1162](#)
- TIMING_GetMaxPeriod
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1162](#)
- TIMING_GetRemaining
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1162](#)
- TIMING_GetResolution
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1163](#)
- TIMING_Init
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1163](#)
- TIMING_InstallCallback
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1163](#)
- TIMING_StartChannel
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1164](#)
- TIMING_StopChannel
 - Timing - Peripheral Abstraction Layer (TIMING P↔AL), [1164](#)
- TIS_ADDRESS
 - Register address map, [1032](#)
- TJA1100_TYPE_NO
 - TJA110x PHY, [1144](#)
- TJA1102P0_TYPE_NO
 - TJA110x PHY, [1144](#)
- TJA110x PHY, [1136](#)
 - BASIC_CTRL_ADDR, [1140](#)
 - BASIC_CTRL_LOOPBACK_FLAG, [1140](#)
 - COMM_STATUS_ADDR, [1140](#)
 - COMM_STATUS_LINKUP_FLAG, [1140](#)
 - COMMON_CONFIG_ADDR, [1140](#)
 - COMMON_CONFIG_AUTO_OP_MASK, [1140](#)

COMMON_CONFIG_CLK_DRIVER_FLAG, 1140
 COMMON_CONFIG_CLK_HOLD_FLAG, 1140
 COMMON_CONFIG_CLK_MODE_LSB, 1140
 COMMON_CONFIG_CLK_MODE_MASK, 1140
 COMMON_CONFIG_CONFIG_WAKE_FLAG, 1140
 COMMON_CONFIG_LOC_WU_TIM_LONG, 1140
 COMMON_CONFIG_LOC_WU_TIM_MASK, 1140
 COMMON_CONFIG_LOC_WU_TIM_SHOR←T, 1141
 COMMON_CONFIG_LOC_WU_TIM_SHORTE←ST, 1141
 CONFIG1_ADDR, 1141
 CONFIG1_FWDPHYLOC_FLAG, 1141
 CONFIG1_FWDPHYREM_FLAG, 1141
 CONFIG1_LOCWUPHY_FLAG, 1141
 CONFIG1_MASTERSLAVE_FLAG, 1141
 CONFIG1_MII_DRIVER_FLAG, 1141
 CONFIG1_MII_MODE_MASK, 1141
 CONFIG1_MII_MODE_SHIFT, 1141
 CONFIG1_REMWUPHY_FLAG, 1141
 CONFIG1_SLEEPACK_FLAG, 1141
 CONFIG1_SLEEPCONFIRM_FLAG, 1141
 CONFIG2_ADDR, 1141
 CONFIG2_SLEEPREQUESTTO_16_8, 1141
 CONFIG2_SLEEPREQUESTTO_MASK, 1142
 disableConfig, 1144
 disableLink, 1144
 EXTENDED_CTRL_ADDR, 1142
 EXTENDED_CTRL_CONFIG_EN_FLAG, 1142
 EXTENDED_CTRL_LINK_CTRL_FLAG, 1142
 EXTENDED_CTRL_LOOPBACK_MODE_EXTE←RNAL, 1142
 EXTENDED_CTRL_LOOPBACK_MODE_INTE←RNAL, 1142
 EXTENDED_CTRL_LOOPBACK_MODE_MASK, 1142
 EXTENDED_CTRL_LOOPBACK_MODE_REM←OTE, 1142
 EXTENDED_CTRL_POWER_MODE_MAS←K, 1142
 EXTENDED_CTRL_POWER_MODE_NORMAL←_REQ, 1142
 EXTENDED_CTRL_POWER_MODE_SILEN←T, 1142
 EXTENDED_CTRL_POWER_MODE_SLEEP, 1142
 EXTENDED_CTRL_POWER_MODE_SLEEP_←REQ, 1142
 EXTENDED_CTRL_POWER_MODE_STANDBY, 1142
 EXTENDED_CTRL_TEST_MODE_MASK, 1142
 EXTENDED_CTRL_TEST_MODE_SHIFT, 1143
 EXTENDED_CTRL_WAKE_REQ_FLAG, 1143
 enableConfig, 1144
 enableInterrupts, 1144
 enableLink, 1144
 GENERAL_STATUS_ADDR, 1143
 GENERAL_STATUS_ENSTATUS_FLAG, 1143
 GENERAL_STATUS_INT_STATUS_FLAG, 1143
 GENERAL_STATUS_PLL_LOCKED_FLAG, 1143
 GENERAL_STATUS_RSTSTATUS_FLAG, 1143
 getState, 1145
 goFromStandbyToNormalMode, 1145
 handleInterrupt, 1145
 handleInterruptLinkDown, 1145
 handleInterruptLinkUp, 1145
 handleInterruptPwon, 1145
 handleInterruptSleep, 1145
 handleInterruptWakeUp, 1145
 IRQ_ENABLE_ADDR, 1143
 IRQ_LINKDOWN_FLAG, 1143
 IRQ_LINKUP_FLAG, 1143
 IRQ_LPS_RECEIVED_FLAG, 1143
 IRQ_PWON_FLAG, 1143
 IRQ_STATUS_ADDR, 1143
 IRQ_WAKEUP_FLAG, 1143
 init, 1145
 OUI, 1143
 PHY_TJA110X_CLKMODE_25MHZ_EXT_CLK, 1144
 PHY_TJA110X_CLKMODE_50MHZ_EXT_REF←CLK, 1144
 PHY_TJA110X_CLKMODE_XTAL_NO_OUTPUT, 1144
 PHY_TJA110X_CLKMODE_XTAL_WITH_25M←HZ_OUTPUT, 1144
 PHY_TJA110X_LOCALWUTIME_LONG, 1144
 PHY_TJA110X_LOCALWUTIME_LONGES←T, 1144
 PHY_TJA110X_LOCALWUTIME_SHORT, 1144
 PHY_TJA110X_LOCALWUTIME_SHORTEST, 1144
 PHY_driver_tja110x, 1146
 phy_tja110x_clkMode_t, 1144
 phy_tja110x_localWuTime_t, 1144
 resume, 1145
 selectTestMode, 1145
 setLoopback, 1145
 setManagedOperation, 1145
 setRole, 1145
 sleep, 1145
 sleepAbortReject, 1146
 TJA1100_TYPE_NO, 1144
 TJA1102P0_TYPE_NO, 1144
 wakeup, 1146
 writeExtendedConfig, 1146
 TL_ACTION_ID_IGNORE
 Low level API, 849
 TL_ACTION_NONE
 Low level API, 849
 TL_ERROR
 Low level API, 849
 TL_HANDLER_INTERLEAVE_MODE
 Low level API, 849
 TL_MAKE_RES_DATA

- Low level API, [849](#)
- TL_RECEIVE_MESSAGE
 - Low level API, [849](#)
- TL_RX_COMPLETED
 - Low level API, [849](#)
- TL_SLAVE_GET_ACTION
 - Low level API, [849](#)
- TL_TIMEOUT_SERVICE
 - Low level API, [849](#)
- TL_TX_COMPLETED
 - Low level API, [849](#)
- TRANSMITTING
 - Common Transport Layer API, [359](#)
- TRGMUX Driver, [1147](#)
 - TRGMUX_DRV_Deinit, [1150](#)
 - TRGMUX_DRV_GenSWTrigger, [1150](#)
 - TRGMUX_DRV_GetLockForTargetModule, [1150](#)
 - TRGMUX_DRV_GetTrigSourceForTargetModule, [1150](#)
 - TRGMUX_DRV_Init, [1151](#)
 - TRGMUX_DRV_SetLockForTargetModule, [1151](#)
 - TRGMUX_DRV_SetTrigSourceForTargetModule, [1151](#)
 - trgmux_target_module_t, [1149](#)
 - trgmux_trigger_source_t, [1149](#)
- TRGMUX_DRV_Deinit
 - TRGMUX Driver, [1150](#)
- TRGMUX_DRV_GenSWTrigger
 - TRGMUX Driver, [1150](#)
- TRGMUX_DRV_GetLockForTargetModule
 - TRGMUX Driver, [1150](#)
- TRGMUX_DRV_GetTrigSourceForTargetModule
 - TRGMUX Driver, [1150](#)
- TRGMUX_DRV_Init
 - TRGMUX Driver, [1151](#)
- TRGMUX_DRV_SetLockForTargetModule
 - TRGMUX Driver, [1151](#)
- TRGMUX_DRV_SetTrigSourceForTargetModule
 - TRGMUX Driver, [1151](#)
- TS_ADDRESS
 - Register address map, [1032](#)
- TXMC_PWM
 - 05. Timer control, [237](#)
- TXMC_TIM
 - 05. Timer control, [237](#)
- TXMC_TRIG_END
 - 05. Timer control, [237](#)
- TXMC_TRIG_START
 - 05. Timer control, [237](#)
- TXPC_1000MS_PERIOD
 - 05. Timer control, [237](#)
- TXPC_100MS_PERIOD
 - 05. Timer control, [237](#)
- TXPC_2000MS_PERIOD
 - 05. Timer control, [237](#)
- TXPC_200MS_PERIOD
 - 05. Timer control, [237](#)
- TXPC_20MS_PERIOD
 - 05. Timer control, [237](#)
- TXPC_30MS_PERIOD
 - 05. Timer control, [237](#)
- TXPC_4000MS_PERIOD
 - 05. Timer control, [237](#)
- TXPC_400MS_PERIOD
 - 05. Timer control, [237](#)
- TXPC_4MS_PERIOD
 - 05. Timer control, [237](#)
- TXPC_50MS_PERIOD
 - 05. Timer control, [237](#)
- TXPC_800MS_PERIOD
 - 05. Timer control, [237](#)
- TXPC_8MS_PERIOD
 - 05. Timer control, [237](#)
- tail
 - WOLF_EVENT_QUEUE, [1336](#)
- targetClockConfigIndex
 - clock_notify_struct_t, [339](#)
- targetModule
 - trgmux_inout_mapping_config_t, [1148](#)
- targetPowerConfigIndex
 - power_manager_notify_struct_t, [968](#)
- targetPowerConfigPtr
 - power_manager_notify_struct_t, [968](#)
- tauxLimOff
 - fs45_vreg_reg_t, [1052](#)
- tbsSz
 - CRL_Entry, [1261](#)
- tccaLimOff
 - fs45_vreg_reg_t, [1052](#)
- tlclkConfig
 - sim_clock_config_t, [327](#)
- tlclkFreq
 - sim_tclk_config_t, [324](#)
- tcp_ready, [1329](#)
 - port, [1329](#)
 - ready, [1329](#)
 - srfName, [1329](#)
- tdlyTdur
 - fs45_sf_impact_reg_t, [1059](#)
- threadId
 - WOLF_EVENT, [1335](#)
- ticket
 - WOLFSSL_SESSION, [1369](#)
- ticketLen
 - WOLFSSL_SESSION, [1369](#)
- tieMask
 - uja113x_init_cfg_t, [185](#)
- timXDutyCycleCtrl
 - uja113x_timsc_cfg_t, [236](#)
- timXModeCtrl
 - uja113x_timsc_cfg_t, [236](#)
- timXPeriodCtrl
 - uja113x_timsc_cfg_t, [236](#)
- timeCompensationRegisterLock
 - rtc_register_lock_config_t, [1005](#)
- timeInvalidIntEnable

- rtc_interrupt_config_t, [1004](#)
- timebase
 - pwm_channel_t, [989](#)
- timeout
 - uja113x_driver_t, [186](#)
 - uja113x_drv_cfg_t, [181](#)
 - WOLFSSL, [1339](#)
 - WOLFSSL_CTX, [1354](#)
 - WOLFSSL_SESSION, [1369](#)
- timeoutCounter
 - lin_state_t, [728](#)
- timeoutCounterFlag
 - lin_state_t, [728](#)
- timeoutInfo_st, [1329](#)
 - flags, [1330](#)
 - numberPackets, [1330](#)
 - packets, [1330](#)
 - timeoutName, [1330](#)
 - timeoutValue, [1330](#)
- timeoutName
 - timeoutInfo_st, [1330](#)
- timeoutValue
 - timeoutInfo_st, [1330](#)
 - wdg_config_t, [1225](#)
 - wdog_user_config_t, [1234](#)
- timer_chan_config_t, [1158](#)
 - callback, [1159](#)
 - callbackParam, [1159](#)
 - chanType, [1159](#)
 - channel, [1159](#)
- timer_chan_state_t, [1330](#)
- timer_chan_type_t
 - Timing - Peripheral Abstraction Layer (TIMING PAL), [1161](#)
- timer_config_t, [1159](#)
 - chanConfigArray, [1159](#)
 - extension, [1159](#)
 - numChan, [1159](#)
- timer_resolution_type_t
 - Timing - Peripheral Abstraction Layer (TIMING PAL), [1161](#)
- timerGetTimeIntervalCallback
 - lin_user_config_t, [726](#)
- timerGetTimeIntervalCallbackArr
 - Low level API, [855](#)
- timerMode
 - lpit_user_channel_config_t, [763](#)
- timestamp
 - enet_rx_enh_info_t, [450](#)
 - enet_tx_enh_info_t, [451](#)
 - packetInfo_st, [1306](#)
- Timing - Peripheral Abstraction Layer (TIMING PAL), [1154](#)
 - TIMER_CHAN_TYPE_CONTINUOUS, [1161](#)
 - TIMER_CHAN_TYPE_ONESHOT, [1161](#)
 - TIMER_RESOLUTION_TYPE_MICROSECOND, [1161](#)
 - TIMER_RESOLUTION_TYPE_MILLISECOND, [1161](#)
 - TIMER_RESOLUTION_TYPE_NANOSECOND, [1161](#)
 - TIMING_Deinit, [1161](#)
 - TIMING_DisableNotification, [1161](#)
 - TIMING_EnableNotification, [1161](#)
 - TIMING_GetElapsed, [1162](#)
 - TIMING_GetMaxPeriod, [1162](#)
 - TIMING_GetRemaining, [1162](#)
 - TIMING_GetResolution, [1163](#)
 - TIMING_Init, [1163](#)
 - TIMING_InstallCallback, [1163](#)
 - TIMING_StartChannel, [1164](#)
 - TIMING_StopChannel, [1164](#)
 - timer_chan_type_t, [1161](#)
 - timer_resolution_type_t, [1161](#)
- timing_instance_t, [1330](#)
 - instIdx, [1331](#)
 - instType, [1331](#)
- timscTimer1Cfg
 - uja113x_init_cfg_t, [185](#)
- timscTimer2Cfg
 - uja113x_init_cfg_t, [185](#)
- timscTimer3Cfg
 - uja113x_init_cfg_t, [185](#)
- timscTimer4Cfg
 - uja113x_init_cfg_t, [185](#)
- tl_pdu_ptr
 - lin_transport_layer_queue_t, [834](#)
- tl_queue_data
 - lin_schedule_data_t, [833](#)
- tl_rx_queue
 - lin_tl_descriptor_t, [837](#)
- tl_rx_queue_data_ptr
 - lin_protocol_user_config_t, [839](#)
- tl_tx_queue
 - lin_tl_descriptor_t, [837](#)
- tl_tx_queue_data_ptr
 - lin_protocol_user_config_t, [839](#)
- tls
 - Options, [1304](#)
- tls1_1
 - Options, [1304](#)
- tls1_3
 - Options, [1304](#)
- tmp
 - Aes, [1248](#)
 - Des, [1273](#)
 - Des3, [1273](#)
- tmpSigSz
 - SskeArgs, [1327](#)
- to
 - smtp_send_request, [1325](#)
- toBeSigned
 - CRL_Entry, [1261](#)
- totalCerts
 - CRL_Entry, [1262](#)

- ProcPeerCertArgs, [1308](#)
- WOLFSSL_X509_STORE_CTX, [1379](#)
- totalCount
 - ClientRow, [1260](#)
 - SessionRow, [1320](#)
- totalStatus
 - OcspEntry, [1299](#)
- traceClockConfig
 - sim_clock_config_t, [327](#)
- trans
 - sbc_status_group_t, [1190](#)
- transEvt
 - sbc_evn_capt_t, [1189](#)
- Transceiver interrupt enable configuration options
 - (0x23), [1165](#)
 - CBSIE_DISABLE, [1166](#)
 - CBSIE_ENABLE, [1166](#)
 - CFIE_DISABLE, [1166](#)
 - CFIE_ENABLE, [1166](#)
 - CWIE_DISABLE, [1166](#)
 - CWIE_ENABLE, [1166](#)
 - L1WIE_DISABLE, [1166](#)
 - L1WIE_ENABLE, [1166](#)
 - L2WIE_DISABLE, [1166](#)
 - L2WIE_ENABLE, [1166](#)
- transfer_status_t
 - LPSPi Driver, [782](#)
- transfer_type
 - flexcan_user_config_t, [517](#)
- transferSize
 - flexio_spi_master_user_config_t, [562](#)
 - flexio_spi_slave_user_config_t, [564](#)
- TransferType
 - sai_user_config_t, [1041](#)
- transferType
 - FlexCANState, [514](#)
 - i2c_master_t, [697](#)
 - i2c_slave_t, [698](#)
 - i2s_user_config_t, [677](#)
 - lpi2c_master_user_config_t, [746](#)
 - lpi2c_slave_user_config_t, [747](#)
 - lpspi_master_config_t, [776](#)
 - lpspi_slave_config_t, [780](#)
 - lpspi_state_t, [779](#)
 - lpuart_state_t, [806](#)
 - lpuart_user_config_t, [807](#)
 - spi_master_t, [1105](#)
 - spi_slave_t, [1106](#)
 - uart_user_config_t, [1215](#)
- transmit_error_resp_sig_flg
 - lin_protocol_state_t, [843](#)
- transmitStatus
 - lpuart_state_t, [806](#)
- Transport layer API, [1167](#)
- trgmux_inout_mapping_config_t, [1148](#)
 - lockTargetModuleReg, [1148](#)
 - targetModule, [1148](#)
 - triggerSource, [1149](#)
- trgmux_target_module_t
 - TRGMUX Driver, [1149](#)
- trgmux_trigger_source_t
 - TRGMUX Driver, [1149](#)
- trgmux_user_config_t, [1149](#)
 - inOutMappingConfig, [1149](#)
 - numInOutMappingConfigs, [1149](#)
- trigger
 - adc_converter_config_t, [256](#)
- triggerInput
 - pdb_timer_config_t, [933](#)
- triggerMode
 - cmp_module_t, [371](#)
- triggerSel
 - adc_converter_config_t, [256](#)
- triggerSelect
 - lpit_user_channel_config_t, [763](#)
- triggerSource
 - adc_group_config_t, [274](#)
 - lpit_user_channel_config_t, [763](#)
 - trgmux_inout_mapping_config_t, [1149](#)
- trimValue
 - pmc_lpo_clock_config_t, [336](#)
- trxe
 - sbc_gl_evt_stat_t, [1186](#)
- tx_msg_size
 - lin_tl_descriptor_t, [837](#)
- tx_msg_status
 - lin_tl_descriptor_t, [837](#)
- txBdBase
 - enet_state_t, [449](#)
- txBdCurrent
 - enet_state_t, [449](#)
- txBuff
 - lin_state_t, [728](#)
 - lpspi_state_t, [779](#)
 - lpuart_state_t, [806](#)
- txCallback
 - lpuart_state_t, [806](#)
 - uart_user_config_t, [1215](#)
- txCallbackParam
 - lpuart_state_t, [806](#)
 - uart_user_config_t, [1215](#)
- txComplete
 - lpuart_state_t, [806](#)
- txCompleted
 - lin_state_t, [728](#)
- txCount
 - lpspi_state_t, [779](#)
- txDMAChannel
 - flexio_i2c_master_user_config_t, [535](#)
 - flexio_i2s_master_user_config_t, [544](#)
 - flexio_i2s_slave_user_config_t, [546](#)
 - flexio_spi_master_user_config_t, [562](#)
 - flexio_spi_slave_user_config_t, [564](#)
 - i2s_user_config_t, [677](#)
 - lpspi_master_config_t, [776](#)
 - lpspi_slave_config_t, [780](#)

- lpspi_state_t, [779](#)
- lpuart_user_config_t, [807](#)
- spi_master_t, [1105](#)
- spi_slave_t, [1106](#)
- uart_user_config_t, [1215](#)
- txFrameCnt
 - lpspi_state_t, [779](#)
- txPin
 - extension_flexio_for_i2s_t, [678](#)
 - flexio_i2s_master_user_config_t, [544](#)
 - flexio_i2s_slave_user_config_t, [546](#)
- txRingAligned
 - enet_buffer_config_t, [447](#)
- txRingSize
 - enet_buffer_config_t, [447](#)
- txSize
 - lin_state_t, [728](#)
 - lpuart_state_t, [806](#)
- type
 - Base_entry, [1251](#)
 - CRL_Monitor, [1262](#)
 - DerBuffer, [1272](#)
 - DsaKey, [1276](#)
 - DtlsHandShakeHeader, [1279](#)
 - DtlsMsg, [1280](#)
 - DtlsRecordLayerHeader, [1280](#)
 - edma_scatter_gather_list_t, [417](#)
 - HandShakeHeader, [1284](#)
 - phy_config_t, [947](#)
 - RecordLayerHeader, [1316](#)
 - RsaKey, [1317](#)
 - WOLF_EVENT, [1335](#)
 - WOLFSSL_ASN1_BIT_STRING, [1341](#)
 - WOLFSSL_ASN1_OBJECT, [1342](#)
 - WOLFSSL_ASN1_STRING, [1343](#)
 - WOLFSSL_BIO, [1345](#)
 - WOLFSSL_BIO_METHOD, [1346](#)
 - WOLFSSL_COMP_METHOD, [1350](#)
 - WOLFSSL_EVP_PKEY, [1363](#)
 - WOLFSSL_HMAC_CTX, [1364](#)
 - WOLFSSL_X509_LOOKUP_METHOD, [1376](#)
- typeH
 - SignatureCtx, [1323](#)
- typeNo
 - phy_id_t, [945](#)
- u
 - RsaKey, [1317](#)
- UART_10_BITS_PER_CHAR
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_15_BITS_PER_CHAR
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_16_BITS_PER_CHAR
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_7_BITS_PER_CHAR
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_8_BITS_PER_CHAR
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_9_BITS_PER_CHAR
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_AbortReceivingData
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_AbortSendingData
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1217](#)
- UART_Deinit
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1217](#)
- UART_GetBaudRate
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1217](#)
- UART_GetDefaultConfig
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1217](#)
- UART_GetReceiveStatus
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1218](#)
- UART_GetTransmitStatus
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1218](#)
- UART_Init
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1219](#)
- UART_ONE_STOP_BIT
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_PARITY_DISABLED
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_PARITY_EVEN
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_PARITY_ODD
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_ReceiveData
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1219](#)
- UART_ReceiveDataBlocking
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1219](#)
- UART_SendData
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1220](#)
- UART_SendDataBlocking
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1220](#)
- UART_SetBaudRate
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)

- Peripheral Abstraction Layer (UART PAL), [1220](#)
- UART_SetRxBuffer
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1221](#)
- UART_SetTxBuffer
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1221](#)
- UART_TWO_STOP_BIT
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_USING_DMA
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- UART_USING_INTERRUPTS
 - Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- uDutyCyclePercent
 - ftm_independent_ch_param_t, [646](#)
- uFrequencyHZ
 - ftm_pwm_param_t, [648](#)
- UJA1131HW3V3
 - 00. Library internals, [186](#)
- UJA1131HW5V0
 - 00. Library internals, [186](#)
- UJA1131HWFD3V0
 - 00. Library internals, [187](#)
- UJA1131HWFD3V4
 - 00. Library internals, [187](#)
- UJA1131HWFD5V0
 - 00. Library internals, [187](#)
- UJA1131HWFD5V4
 - 00. Library internals, [187](#)
- UJA1132HW3V3
 - 00. Library internals, [186](#)
- UJA1132HW5V0
 - 00. Library internals, [186](#)
- UJA1132HWFD3V0
 - 00. Library internals, [187](#)
- UJA1132HWFD3V4
 - 00. Library internals, [187](#)
- UJA1132HWFD5V0
 - 00. Library internals, [187](#)
- UJA1132HWFD5V4
 - 00. Library internals, [187](#)
- UJA1135HW3V3
 - 00. Library internals, [186](#)
- UJA1135HW5V0
 - 00. Library internals, [186](#)
- UJA1136HW3V3
 - 00. Library internals, [186](#)
- UJA1136HW5V0
 - 00. Library internals, [186](#)
- UJA113X_ComputeCrc8
 - 07. MTPNV and ID, [248](#)
- UJA113X_Init
 - 00. Library internals, [187](#)
- UJA113X_RegisterDevice
 - 00. Library internals, [187](#)
- UJA113X_SbcTransfer
 - 00. Library internals, [187](#)
- UJA113X_SetBankFailInterrupts
 - 06. Interrupts, [239](#)
- UJA113X_SetBankOpenLoadThr
 - 04. HVIO bank 0 & 1 control, [229](#)
- UJA113X_SetBankShortCircThr
 - 04. HVIO bank 0 & 1 control, [230](#)
- UJA113X_SetBankWupInterrupts
 - 06. Interrupts, [240](#)
- UJA113X_SetBankWupThr
 - 04. HVIO bank 0 & 1 control, [230](#)
- UJA113X_SetBatteryMonitor
 - 02. Battery monitor configuration, [207](#)
- UJA113X_SetCan
 - 01. CAN & CAN partial networking configuration, [195](#)
- UJA113X_SetCanPartNet
 - 01. CAN & CAN partial networking configuration, [196](#)
- UJA113X_SetDataMasks
 - 01. CAN & CAN partial networking configuration, [196](#)
- UJA113X_SetFailSafe
 - 03. Fail-safe configuration, [220](#)
- UJA113X_SetHvio
 - 04. HVIO bank 0 & 1 control, [231](#)
- UJA113X_SetLin
 - 02. LIN configuration, [210](#)
- UJA113X_SetLock
 - 04. Lock control, [234](#)
- UJA113X_SetMode
 - 01. Mode handling, [199](#)
- UJA113X_SetMtpnv
 - 07. MTPNV and ID, [248](#)
- UJA113X_SetRegulator
 - 01. Regulator configuration, [203](#)
- UJA113X_SetSmps
 - 03. SMPS configuration, [223](#)
- UJA113X_SetSupplyInterrupts
 - 06. Interrupts, [240](#)
- UJA113X_SetSystemInterrupts
 - 06. Interrupts, [241](#)
- UJA113X_SetTimer
 - 05. Timer control, [237](#)
- UJA113X_SetTransceiverInterrupts
 - 06. Interrupts, [241](#)
- UJA113X_SetWatchdog
 - 02. Watchdog, [215](#)
- UJA116xA SBC Driver, [1168](#)
 - LK0C, [1195](#)
 - LK1C, [1195](#)
 - LK2C, [1195](#)
 - LK3C, [1195](#)
 - LK4C, [1195](#)
 - LK5C, [1195](#)
 - LK6C, [1195](#)
 - LKAC, [1195](#)

SBC_UJA_CAN, [1197](#)
 SBC_UJA_CAN_CFDC_DIS, [1192](#)
 SBC_UJA_CAN_CFDC_EN, [1192](#)
 SBC_UJA_CAN_CMC_ACMODE_DA, [1192](#)
 SBC_UJA_CAN_CMC_ACMODE_DD, [1192](#)
 SBC_UJA_CAN_CMC_LISTEN, [1192](#)
 SBC_UJA_CAN_CMC_OFMODE, [1192](#)
 SBC_UJA_CAN_CPNC_DIS, [1193](#)
 SBC_UJA_CAN_CPNC_EN, [1193](#)
 SBC_UJA_CAN_PNCOK_DIS, [1193](#)
 SBC_UJA_CAN_PNCOK_EN, [1193](#)
 SBC_UJA_COUNT_DMASK, [1191](#)
 SBC_UJA_COUNT_ID_REG, [1191](#)
 SBC_UJA_COUNT_MASK, [1191](#)
 SBC_UJA_DAT_MASK_0, [1197](#)
 SBC_UJA_DAT_MASK_1, [1197](#)
 SBC_UJA_DAT_MASK_2, [1197](#)
 SBC_UJA_DAT_MASK_3, [1197](#)
 SBC_UJA_DAT_MASK_4, [1197](#)
 SBC_UJA_DAT_MASK_5, [1197](#)
 SBC_UJA_DAT_MASK_6, [1197](#)
 SBC_UJA_DAT_MASK_7, [1197](#)
 SBC_UJA_DAT_RATE, [1197](#)
 SBC_UJA_DAT_RATE_CDR_1000KB, [1193](#)
 SBC_UJA_DAT_RATE_CDR_100KB, [1193](#)
 SBC_UJA_DAT_RATE_CDR_125KB, [1193](#)
 SBC_UJA_DAT_RATE_CDR_250KB, [1193](#)
 SBC_UJA_DAT_RATE_CDR_500KB, [1193](#)
 SBC_UJA_DAT_RATE_CDR_50KB, [1193](#)
 SBC_UJA_FAIL_SAFE, [1197](#)
 SBC_UJA_FAIL_SAFE_LHC_FLOAT, [1193](#)
 SBC_UJA_FAIL_SAFE_LHC_LOW, [1193](#)
 SBC_UJA_FRAME_CTR, [1197](#)
 SBC_UJA_FRAME_CTR_IDE_11B, [1194](#)
 SBC_UJA_FRAME_CTR_IDE_29B, [1194](#)
 SBC_UJA_FRAME_CTR_PNDM_DCARE, [1194](#)
 SBC_UJA_FRAME_CTR_PNDM_EVAL, [1194](#)
 SBC_UJA_GL_EVNT_STAT, [1197](#)
 SBC_UJA_GL_EVNT_STAT_SUPE, [1194](#)
 SBC_UJA_GL_EVNT_STAT_SUPE_NO, [1194](#)
 SBC_UJA_GL_EVNT_STAT_SYSE, [1194](#)
 SBC_UJA_GL_EVNT_STAT_SYSE_NO, [1194](#)
 SBC_UJA_GL_EVNT_STAT_TRXE, [1194](#)
 SBC_UJA_GL_EVNT_STAT_TRXE_NO, [1194](#)
 SBC_UJA_GL_EVNT_STAT_WPE, [1195](#)
 SBC_UJA_GL_EVNT_STAT_WPE_NO, [1195](#)
 SBC_UJA_IDENTIF, [1198](#)
 SBC_UJA_IDENTIF_0, [1197](#)
 SBC_UJA_IDENTIF_1, [1197](#)
 SBC_UJA_IDENTIF_2, [1197](#)
 SBC_UJA_IDENTIF_3, [1197](#)
 SBC_UJA_LOCK, [1197](#)
 SBC_UJA_MAIN, [1197](#)
 SBC_UJA_MAIN_NMS_NORMAL, [1195](#)
 SBC_UJA_MAIN_NMS_PWR_UP, [1195](#)
 SBC_UJA_MAIN_OTWS_ABOVE, [1195](#)
 SBC_UJA_MAIN_OTWS_BELOW, [1195](#)
 SBC_UJA_MAIN_RSS_CAN_WAKEUP, [1196](#)
 SBC_UJA_MAIN_RSS_DIAG_WAKEUP, [1196](#)
 SBC_UJA_MAIN_RSS_ILLEG_SLP, [1196](#)
 SBC_UJA_MAIN_RSS_ILLEG_WATCH, [1196](#)
 SBC_UJA_MAIN_RSS_LFT_OVERTM, [1196](#)
 SBC_UJA_MAIN_RSS_OFF_MODE, [1196](#)
 SBC_UJA_MAIN_RSS_OVF_SLP, [1196](#)
 SBC_UJA_MAIN_RSS_RSTN_PULDW, [1196](#)
 SBC_UJA_MAIN_RSS_SLP_WAKEUP, [1196](#)
 SBC_UJA_MAIN_RSS_V1_UNDERV, [1196](#)
 SBC_UJA_MAIN_RSS_WAKE_SLP, [1196](#)
 SBC_UJA_MAIN_RSS_WATCH_OVF, [1196](#)
 SBC_UJA_MAIN_RSS_WATCH_TRIG, [1196](#)
 SBC_UJA_MASK_0, [1197](#)
 SBC_UJA_MASK_1, [1197](#)
 SBC_UJA_MASK_2, [1197](#)
 SBC_UJA_MASK_3, [1197](#)
 SBC_UJA_MEMORY_0, [1197](#)
 SBC_UJA_MEMORY_1, [1197](#)
 SBC_UJA_MEMORY_2, [1197](#)
 SBC_UJA_MEMORY_3, [1197](#)
 SBC_UJA_MODE, [1197](#)
 SBC_UJA_MODE_MC_NORMAL, [1196](#)
 SBC_UJA_MODE_MC_SLEEP, [1196](#)
 SBC_UJA_MODE_MC_STANDBY, [1196](#)
 SBC_UJA_MTPNV_CRC, [1198](#)
 SBC_UJA_MTPNV_STAT, [1198](#)
 SBC_UJA_MTPNV_STAT_ECCS, [1196](#)
 SBC_UJA_MTPNV_STAT_ECCS_NO, [1196](#)
 SBC_UJA_MTPNV_STAT_NVMPs, [1196](#)
 SBC_UJA_MTPNV_STAT_NVMPs_NO, [1196](#)
 SBC_UJA_REGULATOR, [1197](#)
 SBC_UJA_REGULATOR_PDC_HV, [1198](#)
 SBC_UJA_REGULATOR_PDC_LV, [1198](#)
 SBC_UJA_REGULATOR_V1RTC_60, [1198](#)
 SBC_UJA_REGULATOR_V1RTC_70, [1198](#)
 SBC_UJA_REGULATOR_V1RTC_80, [1198](#)
 SBC_UJA_REGULATOR_V1RTC_90, [1198](#)
 SBC_UJA_REGULATOR_V2C_N, [1198](#)
 SBC_UJA_REGULATOR_V2C_N_S_R, [1198](#)
 SBC_UJA_REGULATOR_V2C_N_S_S_R, [1198](#)
 SBC_UJA_REGULATOR_V2C_OFF, [1198](#)
 SBC_UJA_SBC, [1198](#)
 SBC_UJA_SBC_FNMC_DIS, [1199](#)
 SBC_UJA_SBC_FNMC_EN, [1199](#)
 SBC_UJA_SBC_SDMC_DIS, [1199](#)
 SBC_UJA_SBC_SDMC_EN, [1199](#)
 SBC_UJA_SBC_SLPC_AC, [1199](#)
 SBC_UJA_SBC_SLPC_IG, [1199](#)
 SBC_UJA_SBC_V1RTSUC_60, [1199](#)
 SBC_UJA_SBC_V1RTSUC_70, [1199](#)
 SBC_UJA_SBC_V1RTSUC_80, [1199](#)
 SBC_UJA_SBC_V1RTSUC_90, [1199](#)
 SBC_UJA_START_UP, [1198](#)
 SBC_UJA_START_UP_RLC_01_01p5, [1200](#)
 SBC_UJA_START_UP_RLC_03p6_05, [1200](#)
 SBC_UJA_START_UP_RLC_10_12p5, [1200](#)
 SBC_UJA_START_UP_RLC_20_25p0, [1200](#)
 SBC_UJA_START_UP_V2SUC_00, [1200](#)

SBC_UJA_START_UP_V2SUC_11, 1200
 SBC_UJA_SUP_EVNT_STAT, 1197
 SBC_UJA_SUP_EVNT_STAT_V1U, 1200
 SBC_UJA_SUP_EVNT_STAT_V1U_NO, 1200
 SBC_UJA_SUP_EVNT_STAT_V2O, 1200
 SBC_UJA_SUP_EVNT_STAT_V2O_NO, 1200
 SBC_UJA_SUP_EVNT_STAT_V2U, 1200
 SBC_UJA_SUP_EVNT_STAT_V2U_NO, 1200
 SBC_UJA_SUPPLY_EVNT, 1197
 SBC_UJA_SUPPLY_EVNT_V1UE_DIS, 1201
 SBC_UJA_SUPPLY_EVNT_V1UE_EN, 1201
 SBC_UJA_SUPPLY_EVNT_V2OE_DIS, 1201
 SBC_UJA_SUPPLY_EVNT_V2OE_EN, 1201
 SBC_UJA_SUPPLY_EVNT_V2UE_DIS, 1201
 SBC_UJA_SUPPLY_EVNT_V2UE_EN, 1201
 SBC_UJA_SUPPLY_STAT, 1197
 SBC_UJA_SUPPLY_STAT_V1S_VAB, 1201
 SBC_UJA_SUPPLY_STAT_V1S_VBE, 1201
 SBC_UJA_SUPPLY_STAT_V2S_DIS, 1201
 SBC_UJA_SUPPLY_STAT_V2S_VAB, 1201
 SBC_UJA_SUPPLY_STAT_V2S_VBE, 1201
 SBC_UJA_SUPPLY_STAT_V2S_VOK, 1201
 SBC_UJA_SYS_EVNT_OTWE_DIS, 1202
 SBC_UJA_SYS_EVNT_OTWE_EN, 1202
 SBC_UJA_SYS_EVNT_SPIFE_DIS, 1202
 SBC_UJA_SYS_EVNT_SPIFE_EN, 1202
 SBC_UJA_SYS_EVNT_STAT, 1197
 SBC_UJA_SYS_EVNT_STAT_OTW, 1202
 SBC_UJA_SYS_EVNT_STAT_OTW_NO, 1202
 SBC_UJA_SYS_EVNT_STAT_PO, 1202
 SBC_UJA_SYS_EVNT_STAT_PO_NO, 1202
 SBC_UJA_SYS_EVNT_STAT_SPIF, 1202
 SBC_UJA_SYS_EVNT_STAT_SPIF_NO, 1202
 SBC_UJA_SYS_EVNT_STAT_WDF, 1203
 SBC_UJA_SYS_EVNT_STAT_WDF_NO, 1203
 SBC_UJA_SYSTEM_EVNT, 1197
 SBC_UJA_TIMEOUT, 1191
 SBC_UJA_TRANS_EVNT, 1197
 SBC_UJA_TRANS_EVNT_CBSE_DIS, 1203
 SBC_UJA_TRANS_EVNT_CBSE_EN, 1203
 SBC_UJA_TRANS_EVNT_CFE_DIS, 1203
 SBC_UJA_TRANS_EVNT_CFE_EN, 1203
 SBC_UJA_TRANS_EVNT_CWE_DIS, 1203
 SBC_UJA_TRANS_EVNT_CWE_EN, 1203
 SBC_UJA_TRANS_EVNT_STAT, 1197
 SBC_UJA_TRANS_EVNT_STAT_CBS, 1203
 SBC_UJA_TRANS_EVNT_STAT_CBS_NO, 1203
 SBC_UJA_TRANS_EVNT_STAT_CF, 1204
 SBC_UJA_TRANS_EVNT_STAT_CF_NO, 1204
 SBC_UJA_TRANS_EVNT_STAT_CW, 1204
 SBC_UJA_TRANS_EVNT_STAT_CW_NO, 1204
 SBC_UJA_TRANS_EVNT_STAT_PNFDE, 1204
 SBC_UJA_TRANS_EVNT_STAT_PNFDE_NO, 1204
 SBC_UJA_TRANS_STAT, 1197
 SBC_UJA_TRANS_STAT_CBSS_ACT, 1204
 SBC_UJA_TRANS_STAT_CBSS_INACT, 1204
 SBC_UJA_TRANS_STAT_CFS_NO_TXD, 1205
 SBC_UJA_TRANS_STAT_CFS_TXD, 1205
 SBC_UJA_TRANS_STAT_COSCS_NRUN, 1205
 SBC_UJA_TRANS_STAT_COSCS_RUN, 1205
 SBC_UJA_TRANS_STAT_CPNERR_DET, 1205
 SBC_UJA_TRANS_STAT_CPNERR_NO_DET, 1205
 SBC_UJA_TRANS_STAT_CPNS_ERR, 1205
 SBC_UJA_TRANS_STAT_CPNS_OK, 1205
 SBC_UJA_TRANS_STAT_CTS_ACT, 1205
 SBC_UJA_TRANS_STAT_CTS_INACT, 1205
 SBC_UJA_TRANS_STAT_VCS_AB, 1206
 SBC_UJA_TRANS_STAT_VCS_BE, 1206
 SBC_UJA_WAKE_EN, 1197
 SBC_UJA_WAKE_EN_WPFE_DIS, 1206
 SBC_UJA_WAKE_EN_WPFE_EN, 1206
 SBC_UJA_WAKE_EN_WPRE_DIS, 1206
 SBC_UJA_WAKE_EN_WPRE_EN, 1206
 SBC_UJA_WAKE_EVNT_STAT, 1198
 SBC_UJA_WAKE_EVNT_STAT_WPF, 1206
 SBC_UJA_WAKE_EVNT_STAT_WPF_NO, 1206
 SBC_UJA_WAKE_EVNT_STAT_WPR, 1206
 SBC_UJA_WAKE_EVNT_STAT_WPR_NO, 1206
 SBC_UJA_WAKE_STAT, 1197
 SBC_UJA_WAKE_STAT_WPVS_AB, 1207
 SBC_UJA_WAKE_STAT_WPVS_BE, 1207
 SBC_UJA_WTDOG_CTR, 1197
 SBC_UJA_WTDOG_CTR_NWP_1024, 1207
 SBC_UJA_WTDOG_CTR_NWP_128, 1207
 SBC_UJA_WTDOG_CTR_NWP_16, 1207
 SBC_UJA_WTDOG_CTR_NWP_256, 1207
 SBC_UJA_WTDOG_CTR_NWP_32, 1207
 SBC_UJA_WTDOG_CTR_NWP_4096, 1207
 SBC_UJA_WTDOG_CTR_NWP_64, 1207
 SBC_UJA_WTDOG_CTR_NWP_8, 1207
 SBC_UJA_WTDOG_CTR_WMC_AUTO, 1207
 SBC_UJA_WTDOG_CTR_WMC_TIME, 1207
 SBC_UJA_WTDOG_CTR_WMC_WIND, 1207
 SBC_UJA_WTDOG_STAT, 1197
 SBC_UJA_WTDOG_STAT_FNMS_N_NORMAL, 1208
 SBC_UJA_WTDOG_STAT_FNMS_NORMA↵L, 1208
 SBC_UJA_WTDOG_STAT_SDMS_N_NORMAL, 1208
 SBC_UJA_WTDOG_STAT_SDMS_NORMA↵L, 1208
 SBC_UJA_WTDOG_STAT_WDS_FIH, 1208
 SBC_UJA_WTDOG_STAT_WDS_OFF, 1208
 SBC_UJA_WTDOG_STAT_WDS_SEH, 1208
 sbc_can_cfdc_t, 1192
 sbc_can_cmc_t, 1192
 sbc_can_cpnc_t, 1192
 sbc_can_pncok_t, 1193
 sbc_dat_rate_t, 1193
 sbc_data_mask_t, 1191
 sbc_fail_safe_lhc_t, 1193
 sbc_fail_safe_rcc_t, 1191
 sbc_frame_ctr_dlc_t, 1191

- [sbc_frame_ctr_ide_t](#), [1193](#)
- [sbc_frame_ctr_pndm_t](#), [1194](#)
- [sbc_gl_evnt_stat_supe_t](#), [1194](#)
- [sbc_gl_evnt_stat_syse_t](#), [1194](#)
- [sbc_gl_evnt_stat_trxe_t](#), [1194](#)
- [sbc_gl_evnt_stat_wpe_t](#), [1194](#)
- [sbc_identif_mask_t](#), [1192](#)
- [sbc_identifier_t](#), [1192](#)
- [sbc_lock_t](#), [1195](#)
- [sbc_main_nms_t](#), [1195](#)
- [sbc_main_otws_t](#), [1195](#)
- [sbc_main_rss_t](#), [1195](#)
- [sbc_mode_mc_t](#), [1196](#)
- [sbc_mtpnv_stat_eccs_t](#), [1196](#)
- [sbc_mtpnv_stat_nvmps_t](#), [1196](#)
- [sbc_mtpnv_stat_wrcnts_t](#), [1192](#)
- [sbc_register_t](#), [1196](#)
- [sbc_regulator_pdc_t](#), [1198](#)
- [sbc_regulator_v1rtc_t](#), [1198](#)
- [sbc_regulator_v2c_t](#), [1198](#)
- [sbc_sbc_fnmc_t](#), [1198](#)
- [sbc_sbc_sdmc_t](#), [1199](#)
- [sbc_sbc_slpc_t](#), [1199](#)
- [sbc_sbc_v1rtsuc_t](#), [1199](#)
- [sbc_start_up_rlc_t](#), [1199](#)
- [sbc_start_up_v2suc_t](#), [1200](#)
- [sbc_sup_evnt_stat_v1u_t](#), [1200](#)
- [sbc_sup_evnt_stat_v2o_t](#), [1200](#)
- [sbc_sup_evnt_stat_v2u_t](#), [1200](#)
- [sbc_supply_evnt_v1ue_t](#), [1200](#)
- [sbc_supply_evnt_v2oe_t](#), [1201](#)
- [sbc_supply_evnt_v2ue_t](#), [1201](#)
- [sbc_supply_stat_v1s_t](#), [1201](#)
- [sbc_supply_stat_v2s_t](#), [1201](#)
- [sbc_sys_evnt_otwe_t](#), [1201](#)
- [sbc_sys_evnt_spife_t](#), [1202](#)
- [sbc_sys_evnt_stat_otw_t](#), [1202](#)
- [sbc_sys_evnt_stat_po_t](#), [1202](#)
- [sbc_sys_evnt_stat_spif_t](#), [1202](#)
- [sbc_sys_evnt_stat_wdf_t](#), [1202](#)
- [sbc_trans_evnt_cbse_t](#), [1203](#)
- [sbc_trans_evnt_cfe_t](#), [1203](#)
- [sbc_trans_evnt_cwe_t](#), [1203](#)
- [sbc_trans_evnt_stat_cbs_t](#), [1203](#)
- [sbc_trans_evnt_stat_cf_t](#), [1204](#)
- [sbc_trans_evnt_stat_cw_t](#), [1204](#)
- [sbc_trans_evnt_stat_pnfde_t](#), [1204](#)
- [sbc_trans_stat_cbss_t](#), [1204](#)
- [sbc_trans_stat_cfs_t](#), [1204](#)
- [sbc_trans_stat_coscs_t](#), [1205](#)
- [sbc_trans_stat_cpnrerr_t](#), [1205](#)
- [sbc_trans_stat_cpns_t](#), [1205](#)
- [sbc_trans_stat_cts_t](#), [1205](#)
- [sbc_trans_stat_vcs_t](#), [1205](#)
- [sbc_wake_en_wpfe_t](#), [1206](#)
- [sbc_wake_en_wpre_t](#), [1206](#)
- [sbc_wake_evnt_stat_wpf_t](#), [1206](#)
- [sbc_wake_evnt_stat_wpr_t](#), [1206](#)
- [sbc_wake_stat_wpvs_t](#), [1206](#)
- [sbc_wtdog_ctr_nwp_t](#), [1207](#)
- [sbc_wtdog_ctr_wmc_t](#), [1207](#)
- [sbc_wtdog_stat_fnms_t](#), [1207](#)
- [sbc_wtdog_stat_sdms_t](#), [1208](#)
- [sbc_wtdog_stat_wds_t](#), [1208](#)
- [uart_bit_count_per_char_t](#)
Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1215](#)
- [uart_instance_t](#), [1331](#)
instIdx, [1331](#)
instType, [1331](#)
- [uart_parity_mode_t](#)
Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- [uart_stop_bit_count_t](#)
Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- [uart_transfer_type_t](#)
Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1216](#)
- [uart_user_config_t](#), [1214](#)
baudRate, [1214](#)
bitCount, [1214](#)
extension, [1214](#)
parityMode, [1214](#)
rxCallback, [1214](#)
rxCallbackParam, [1214](#)
rxDMAChannel, [1214](#)
stopBitCount, [1215](#)
transferType, [1215](#)
txCallback, [1215](#)
txCallbackParam, [1215](#)
txDMAChannel, [1215](#)
- [uidIdx](#)
DecodedName, [1271](#)
- [uidLen](#)
DecodedName, [1271](#)
- [uja113x_bmc_cfg_t](#), [204](#)
bmOverVoltThr, [205](#)
bmOverVoltThrRel, [205](#)
bmSrcCtrl, [205](#)
bmUndrVoltThr, [205](#)
bmUndrVoltThrRel, [205](#)
- [uja113x_bmetsc_bmsc_t](#)
02. Battery monitor configuration, [206](#)
- [uja113x_bmhc_bmhoc_t](#)
02. Battery monitor configuration, [206](#)
- [uja113x_bmhc_bmhuc_t](#)
02. Battery monitor configuration, [206](#)
- [uja113x_bmotc_bmotc_t](#)
02. Battery monitor configuration, [206](#)
- [uja113x_bmutc_bmutc_t](#)
02. Battery monitor configuration, [206](#)
- [uja113x_boldt_cfg_t](#), [227](#)
io15OpenLoadThrCtrl, [228](#)
io26OpenLoadThrCtrl, [228](#)
io37OpenLoadThrCtrl, [228](#)

- io48OpenLoadThrCtrl, [228](#)
- uja113x_boldt_ionoltc_t
 - 02. Battery monitor configuration, [206](#)
- uja113x_bscdt_cfg_t, [227](#)
 - io15ShortCircuitThrCtrl, [227](#)
 - io26ShortCircuitThrCtrl, [227](#)
 - io37ShortCircuitThrCtrl, [227](#)
 - io48ShortCircuitThrCtrl, [227](#)
- uja113x_bscdt_ionsctc_t
 - 02. Battery monitor configuration, [207](#)
- uja113x_bwtc_bnwtc_t
 - 04. HVIO bank 0 & 1 control, [228](#)
- uja113x_canc_cfdc_t
 - 01. CAN & CAN partial networking configuration, [193](#)
- uja113x_canc_cfg_t, [190](#)
 - canFDCtrl, [190](#)
 - canModeCtrl, [190](#)
 - canPartNetCtrl, [190](#)
 - canShutdownCtrl, [191](#)
- uja113x_canc_cmc_t
 - 01. CAN & CAN partial networking configuration, [194](#)
- uja113x_canc_cpnc_t
 - 01. CAN & CAN partial networking configuration, [193](#)
- uja113x_canc_csc_t
 - 01. CAN & CAN partial networking configuration, [194](#)
- uja113x_chip_t
 - 00. Library internals, [186](#)
- uja113x_cpnc_cfg_t, [191](#)
 - canDataRate, [191](#)
 - dataLenCode, [191](#)
 - id, [191](#)
 - idMask, [191](#)
 - ide, [191](#)
 - partNetDataMask, [192](#)
- uja113x_dm_cfg_t, [192](#)
 - dm0, [192](#)
 - dm1, [192](#)
 - dm2, [192](#)
 - dm3, [192](#)
 - dm4, [193](#)
 - dm5, [193](#)
 - dm6, [193](#)
 - dm7, [193](#)
- uja113x_dr_cdr_t
 - 01. CAN & CAN partial networking configuration, [194](#)
- uja113x_driver_t, [186](#)
 - chipType, [186](#)
 - lpsplInstance, [186](#)
 - timeout, [186](#)
- uja113x_drv_cfg_t, [181](#)
 - chipType, [181](#)
 - lpsplInstance, [181](#)
 - timeout, [181](#)
- uja113x_fc_dlc_t
 - 01. CAN & CAN partial networking configuration, [195](#)
- uja113x_fc_ide_t
 - 01. CAN & CAN partial networking configuration, [193](#)
- uja113x_fc_pndm_t
 - 01. CAN & CAN partial networking configuration, [193](#)
- uja113x_fsc_cfg_t, [218](#)
 - enCtrl, [218](#)
 - enDriverCtrl, [218](#)
 - enShutdownCtrl, [218](#)
 - limpHomeCtrl, [218](#)
 - resetCntCtrl, [218](#)
- uja113x_fsc_enc_t
 - 03. Fail-safe configuration, [219](#)
- uja113x_fsc_endc_t
 - 03. Fail-safe configuration, [219](#)
- uja113x_fsc_ensc_t
 - 03. Fail-safe configuration, [219](#)
- uja113x_fsc_lhc_t
 - 03. Fail-safe configuration, [219](#)
- uja113x_fsc_rcc_t
 - 03. Fail-safe configuration, [219](#)
- uja113x_hvio_bank_cfg_t, [181](#)
 - bankFailIntMask, [182](#)
 - bankWupIntMask, [182](#)
 - bankWupThr, [182](#)
 - boldtBankOpenLoad, [182](#)
 - bscdtBankShortCirc, [182](#)
 - hvioConfig, [182](#)
- uja113x_hvio_cfg_t, [226](#)
 - ionActivateCtrl, [227](#)
 - ionConfCtrl, [227](#)
 - ionShutdownCtrl, [227](#)
- uja113x_hvion_ionac_t
 - 04. HVIO bank 0 & 1 control, [228](#)
- uja113x_hvion_ioncc_t
 - 04. HVIO bank 0 & 1 control, [229](#)
- uja113x_hvion_ionsc_t
 - 04. HVIO bank 0 & 1 control, [229](#)
- uja113x_id_id_t
 - 01. CAN & CAN partial networking configuration, [194](#)
- uja113x_idm_idm_t
 - 01. CAN & CAN partial networking configuration, [194](#)
- uja113x_init_cfg_t, [182](#)
 - bmcBatMonitorCfg, [184](#)
 - cancCanCfg, [184](#)
 - cpncCanPartNetCfg, [184](#)
 - dmCanDataMaskCfg, [184](#)
 - fscCfg, [184](#)
 - hvioBank0Cfg, [184](#)
 - hvioBank1Cfg, [184](#)
 - lckcLockRegCfg, [184](#)
 - linxLinCtrl, [184](#)

- mcSbcMode, [184](#)
- memory0, [184](#)
- memory1, [184](#)
- memory2, [185](#)
- memory3, [185](#)
- rcRegulatorCfg, [185](#)
- smpscSmpsCfg, [185](#)
- supieMask, [185](#)
- sysieMask, [185](#)
- tieMask, [185](#)
- timscTimer1Cfg, [185](#)
- timscTimer2Cfg, [185](#)
- timscTimer3Cfg, [185](#)
- timscTimer4Cfg, [185](#)
- wdcWatchdogCfg, [185](#)
- uja113x_lckc_cfg_t, [232](#)
 - lock0, [233](#)
 - lock1, [233](#)
 - lock2, [233](#)
 - lock3, [233](#)
 - lock4, [233](#)
 - lock5, [233](#)
 - lock6, [233](#)
- uja113x_lckc_lkxc_t
 - 04. Lock control, [234](#)
- uja113x_linc_cfg_t, [208](#)
 - lin1ModeCtrl, [209](#)
 - lin1SlopeCtrl, [209](#)
 - lin2ModeCtrl, [209](#)
 - lin2SlopeCtrl, [209](#)
- uja113x_linc_lmc1_t
 - 02. LIN configuration, [209](#)
- uja113x_linc_lmc2_t
 - 02. LIN configuration, [209](#)
- uja113x_linc_lsc1_t
 - 02. LIN configuration, [210](#)
- uja113x_linc_lsc2_t
 - 02. LIN configuration, [210](#)
- uja113x_mc_mc_t
 - 01. Mode handling, [198](#)
- uja113x_mtpnv_cfg_t, [246](#)
 - highSideCtrl, [247](#)
 - lowSideCtrl, [247](#)
 - sbcConfigCtrl, [247](#)
 - startupCtrl, [247](#)
- uja113x_rc_cfg_t, [201](#)
 - v1RstThrCtrl, [202](#)
 - v2Ctrl, [202](#)
 - v2ShutdownCtrl, [202](#)
- uja113x_rc_v1rtc_t
 - 01. Regulator configuration, [202](#)
- uja113x_rc_v2c_t
 - 01. Regulator configuration, [202](#)
- uja113x_rc_v2sc_t
 - 01. Regulator configuration, [202](#)
- uja113x_smpsc_cfg_t, [221](#)
 - smpsCtrl, [222](#)
 - smpsOutVolt, [222](#)
 - smpsOvertempCtrl, [222](#)
- uja113x_smpsc_smpsc_t
 - 03. SMPS configuration, [222](#)
- uja113x_smpsc_smpsotc_t
 - 03. SMPS configuration, [222](#)
- uja113x_smpsovc_smpsoc_t
 - 03. SMPS configuration, [222](#)
- uja113x_timsc_cfg_t, [235](#)
 - nTimer, [236](#)
 - timXDutyCycleCtrl, [236](#)
 - timXModeCtrl, [236](#)
 - timXPeriodCtrl, [236](#)
- uja113x_timxc_txmc_t
 - 05. Timer control, [236](#)
- uja113x_timxc_txpc_t
 - 05. Timer control, [237](#)
- uja113x_timxdcc_txdcc_t
 - 05. Timer control, [236](#)
- uja113x_wtdc_cfg_t, [214](#)
 - nomWtdPeriod, [214](#)
 - wtdModeCtrl, [214](#)
- uja113x_wtdc_nwp_t
 - 02. Watchdog, [214](#)
- uja113x_wtdc_wmc_t
 - 02. Watchdog, [215](#)
- unicast
 - enet_rx_enh_info_t, [450](#)
- Universal Asynchronous Receiver/Transmitter - Peripheral Abstraction Layer (UART PAL), [1209](#)
 - UART_10_BITS_PER_CHAR, [1216](#)
 - UART_15_BITS_PER_CHAR, [1216](#)
 - UART_16_BITS_PER_CHAR, [1216](#)
 - UART_7_BITS_PER_CHAR, [1216](#)
 - UART_8_BITS_PER_CHAR, [1216](#)
 - UART_9_BITS_PER_CHAR, [1216](#)
 - UART_AbortReceivingData, [1216](#)
 - UART_AbortSendingData, [1217](#)
 - UART_Deinit, [1217](#)
 - UART_GetBaudRate, [1217](#)
 - UART_GetDefaultConfig, [1217](#)
 - UART_GetReceiveStatus, [1218](#)
 - UART_GetTransmitStatus, [1218](#)
 - UART_Init, [1219](#)
 - UART_ONE_STOP_BIT, [1216](#)
 - UART_PARITY_DISABLED, [1216](#)
 - UART_PARITY_EVEN, [1216](#)
 - UART_PARITY_ODD, [1216](#)
 - UART_ReceiveData, [1219](#)
 - UART_ReceiveDataBlocking, [1219](#)
 - UART_SendData, [1220](#)
 - UART_SendDataBlocking, [1220](#)
 - UART_SetBaudRate, [1220](#)
 - UART_SetRxBuffer, [1221](#)
 - UART_SetTxBuffer, [1221](#)
 - UART_TWO_STOP_BIT, [1216](#)
 - UART_USING_DMA, [1216](#)
 - UART_USING_INTERRUPTS, [1216](#)
 - uart_bit_count_per_char_t, [1215](#)

- uart_parity_mode_t, [1216](#)
- uart_stop_bit_count_t, [1216](#)
- uart_transfer_type_t, [1216](#)
- updateEnable
 - rtc_init_config_t, [1002](#)
 - wdog_user_config_t, [1234](#)
- useClientOrder
 - Options, [1304](#)
 - WOLFSSL_CTX, [1354](#)
- used
 - fp_int, [1282](#)
 - mp_int, [1295](#)
 - wolfssl_TI_Hash, [1372](#)
- User provided call-outs, [1222](#)
 - l_sys_irq_disable, [1222](#)
 - l_sys_irq_restore, [1222](#)
- userAreaLock
 - flash_mx25l6433f_secure_lock_t, [885](#)
- userCtx
 - WOLFSSL_X509_STORE_CTX, [1379](#)
- userGain
 - adc_calibration_t, [258](#)
- userOffset
 - adc_calibration_t, [258](#)
- usingAnon_cipher
 - Options, [1304](#)
- usingCompression
 - Options, [1304](#)
- usingNonblock
 - Options, [1304](#)
- usingPSK_cipher
 - Options, [1304](#)
- V1RTC_60_NOMINAL_OUT
 - 01. Regulator configuration, [202](#)
- V1RTC_70_NOMINAL_OUT
 - 01. Regulator configuration, [202](#)
- V1RTC_80_NOMINAL_OUT
 - 01. Regulator configuration, [202](#)
- V1RTC_90_NOMINAL_OUT
 - 01. Regulator configuration, [202](#)
- V1RTSUC_60_NOM
 - SBC configuration control options (0x74), [1077](#)
- V1RTSUC_70_NOM
 - SBC configuration control options (0x74), [1077](#)
- V1RTSUC_80_NOM
 - SBC configuration control options (0x74), [1077](#)
- V1RTSUC_90_NOM
 - SBC configuration control options (0x74), [1077](#)
- v1RstThrCtrl
 - uja113x_rc_cfg_t, [202](#)
- V1UIE_DISABLE
 - Supply interrupt enable configuration options (0x1C), [1123](#)
- V1UIE_ENABLE
 - Supply interrupt enable configuration options (0x1C), [1123](#)
- v1rtc
 - sbc_regulator_t, [1177](#)
- v1rtsuc
 - sbc_sbc_t, [1176](#)
- v1s
 - sbc_supply_status_t, [1185](#)
- v1u
 - sbc_sup_evnt_stat_t, [1187](#)
- v1ue
 - sbc_supply_evnt_t, [1177](#)
- V2C_OFF
 - 01. Regulator configuration, [202](#)
- V2C_ON_N
 - 01. Regulator configuration, [202](#)
- V2C_ON_NSR
 - 01. Regulator configuration, [202](#)
- V2C_ON_NSSRF
 - 01. Regulator configuration, [202](#)
- v2Ctrl
 - uja113x_rc_cfg_t, [202](#)
- V2SC_FULL
 - 01. Regulator configuration, [203](#)
- V2SC_NONE
 - 01. Regulator configuration, [202](#)
- V2SC_OVERVOLTAGE
 - 01. Regulator configuration, [202](#)
- V2SC_UNDRVOLTAGE
 - 01. Regulator configuration, [202](#)
- V2SUC_ALWAYS_OFF
 - Start-up control configuration options (0x73), [1119](#)
- V2SUC_ALWAYS_ON
 - Start-up control configuration options (0x73), [1119](#)
- v2ShutdownCtrl
 - uja113x_rc_cfg_t, [202](#)
- v2c
 - sbc_regulator_t, [1177](#)
- v2o
 - sbc_sup_evnt_stat_t, [1187](#)
- v2oe
 - sbc_supply_evnt_t, [1178](#)
- v2s
 - sbc_supply_status_t, [1185](#)
- v2suc
 - sbc_start_up_t, [1177](#)
- v2u
 - sbc_sup_evnt_stat_t, [1187](#)
- v2ue
 - sbc_supply_evnt_t, [1178](#)
- VBADC1_ADDRESS
 - Register address map, [1032](#)
- VBADC2_ADDRESS
 - Register address map, [1032](#)
- VEXTAC_NO_PROTECTION
 - SBC configuration control options (0x74), [1078](#)
- VEXTAC_SENSOR_SUPPLY
 - SBC configuration control options (0x74), [1078](#)
- VEXTOIE_DISABLE
 - Supply interrupt enable configuration options (0x1C), [1123](#)
- VEXTOIE_ENABLE

- Supply interrupt enable configuration options (0x1C), [1123](#)
- VEXTUIE_DISABLE
 - Supply interrupt enable configuration options (0x1C), [1124](#)
- VEXTUIE_ENABLE
 - Supply interrupt enable configuration options (0x1C), [1124](#)
- VLPR_MODE
 - Clock Manager Driver, [344](#)
- VLPS_MODE
 - Clock Manager Driver, [344](#)
- value
 - fs45_reg_config_value_t, [1052](#)
 - packetInfo_st, [1306](#)
- valueSz
 - packetInfo_st, [1306](#)
- variant
 - lin_product_id_t, [1292](#)
- vaux5d
 - fs45_supervisor_reg_t, [1057](#)
- vauxFsOv
 - fs45_vaux_ovuv_impact_reg_t, [1060](#)
- vauxFsUv
 - fs45_vaux_ovuv_impact_reg_t, [1060](#)
- vauxOvuvImpactReg
 - fs45_drv_config_t, [1062](#)
- vauxTrkEn
 - fs45_vreg_reg_t, [1052](#)
- vcanOvMon
 - fs45_vreg_reg_t, [1052](#)
- vcca5d
 - fs45_supervisor_reg_t, [1057](#)
- vccaFsOv
 - fs45_vcca_ovuv_impact_reg_t, [1060](#)
- vccaFsUv
 - fs45_vcca_ovuv_impact_reg_t, [1060](#)
- vccaOvuvImpactReg
 - fs45_drv_config_t, [1062](#)
- vccrConfig
 - scg_clock_mode_config_t, [333](#)
- vcCore5d
 - fs45_supervisor_reg_t, [1057](#)
- vcCoreFsOv
 - fs45_vcore_ovuv_impact_reg_t, [1059](#)
- vcCoreFsUv
 - fs45_vcore_ovuv_impact_reg_t, [1060](#)
- vcCoreOvuvImpactReg
 - fs45_drv_config_t, [1062](#)
- vcs
 - sbc_trans_stat_t, [1186](#)
- verifStatus
 - csec_state_t, [301](#)
- verified
 - CRL_Entry, [1262](#)
- verify
 - DecodedCert, [1269](#)
 - ScvArgs, [1319](#)
- verifyCallback
 - WOLFSSL, [1339](#)
 - WOLFSSL_CTX, [1354](#)
- verifyCbCtx
 - WOLFSSL, [1339](#)
- verifyHashes
 - HS_Hashes, [1288](#)
- verifyNone
 - Options, [1304](#)
 - WOLFSSL_CTX, [1354](#)
- verifyPeer
 - Options, [1304](#)
 - WOLFSSL_CTX, [1355](#)
- verifySig
 - DskeArgs, [1277](#)
 - ScvArgs, [1319](#)
 - SskeArgs, [1327](#)
- verifySigSz
 - DskeArgs, [1277](#)
- version
 - DecodedCert, [1269](#)
 - WOLFSSL, [1339](#)
 - WOLFSSL_METHOD, [1366](#)
 - WOLFSSL_X509, [1374](#)
- virtChn
 - edma_chn_state_t, [416](#)
- virtChnConfig
 - edma_channel_config_t, [417](#)
- virtChnState
 - edma_state_t, [418](#)
- vlanPrio
 - enet_rx_enh_info_t, [450](#)
- vlpProt
 - smc_power_mode_protection_config_t, [979](#)
- voltage
 - cmp_dac_t, [369](#)
- voltageRef
 - adc_converter_config_t, [256](#)
 - extension_adc_s32k1xx_t, [276](#)
- voltageReferenceSource
 - cmp_dac_t, [369](#)
- vregReg
 - fs45_drv_config_t, [1062](#)
- WC_DerCertList, [1332](#)
 - buffer, [1332](#)
 - bufferSz, [1332](#)
 - next, [1332](#)
- WC_RNG, [1333](#)
 - drbg, [1333](#)
 - heap, [1333](#)
 - seed, [1333](#)
 - status, [1333](#)
- WDG_PAL, [1223](#)
 - WDG_ClearIntFlag, [1226](#)
 - WDG_Deinit, [1226](#)
 - WDG_GetCounter, [1227](#)
 - WDG_GetDefaultConfig, [1227](#)
 - WDG_IN_ASSERT_DISABLED, [1226](#)

- WDG_IN_ASSERT_ON_LOGIC_ONE, [1226](#)
- WDG_IN_ASSERT_ON_LOGIC_ZERO, [1226](#)
- WDG_Init, [1227](#)
- WDG_PAL_BUS_CLOCK, [1226](#)
- WDG_PAL_LPO_CLOCK, [1226](#)
- WDG_PAL_SIRC_CLOCK, [1226](#)
- WDG_PAL_SOSC_CLOCK, [1226](#)
- WDG_Refresh, [1228](#)
- WDG_SetInt, [1228](#)
- WDG_SetTimeout, [1228](#)
- WDG_SetWindow, [1228](#)
- wdg_clock_source_t, [1225](#)
- wdg_in_assert_logic_t, [1226](#)
- wdg_inst_type_t, [1226](#)
- WDG_ClearIntFlag
 - WDG PAL, [1226](#)
- WDG_Deinit
 - WDG PAL, [1226](#)
- WDG_GetCounter
 - WDG PAL, [1227](#)
- WDG_GetDefaultConfig
 - WDG PAL, [1227](#)
- WDG_IN_ASSERT_DISABLED
 - WDG PAL, [1226](#)
- WDG_IN_ASSERT_ON_LOGIC_ONE
 - WDG PAL, [1226](#)
- WDG_IN_ASSERT_ON_LOGIC_ZERO
 - WDG PAL, [1226](#)
- WDG_Init
 - WDG PAL, [1227](#)
- WDG_PAL_BUS_CLOCK
 - WDG PAL, [1226](#)
- WDG_PAL_LPO_CLOCK
 - WDG PAL, [1226](#)
- WDG_PAL_SIRC_CLOCK
 - WDG PAL, [1226](#)
- WDG_PAL_SOSC_CLOCK
 - WDG PAL, [1226](#)
- WDG_Refresh
 - WDG PAL, [1228](#)
- WDG_SetInt
 - WDG PAL, [1228](#)
- WDG_SetTimeout
 - WDG PAL, [1228](#)
- WDG_SetWindow
 - WDG PAL, [1228](#)
- WDOG Driver, [1230](#)
 - WDOG_BUS_CLOCK, [1234](#)
 - WDOG_DEBUG_MODE, [1234](#)
 - WDOG_DRV_ClearIntFlag, [1235](#)
 - WDOG_DRV_Deinit, [1235](#)
 - WDOG_DRV_GetConfig, [1235](#)
 - WDOG_DRV_GetCounter, [1235](#)
 - WDOG_DRV_GetDefaultConfig, [1236](#)
 - WDOG_DRV_GetTestMode, [1236](#)
 - WDOG_DRV_Init, [1236](#)
 - WDOG_DRV_SetInt, [1236](#)
 - WDOG_DRV_SetMode, [1237](#)
- WDOG_DRV_SetTestMode, [1237](#)
- WDOG_DRV_SetTimeout, [1237](#)
- WDOG_DRV_SetWindow, [1238](#)
- WDOG_DRV_Trigger, [1238](#)
- WDOG_LPO_CLOCK, [1234](#)
- WDOG_SIRC_CLOCK, [1234](#)
- WDOG_SOSC_CLOCK, [1234](#)
- WDOG_STOP_MODE, [1234](#)
- WDOG_TST_DISABLED, [1235](#)
- WDOG_TST_HIGH, [1235](#)
- WDOG_TST_LOW, [1235](#)
- WDOG_TST_USER, [1235](#)
- WDOG_WAIT_MODE, [1234](#)
- wdog_clk_source_t, [1234](#)
- wdog_set_mode_t, [1234](#)
- wdog_test_mode_t, [1234](#)
- WDOG_BUS_CLOCK
 - WDOG Driver, [1234](#)
- WDOG_DEBUG_MODE
 - WDOG Driver, [1234](#)
- WDOG_DRV_ClearIntFlag
 - WDOG Driver, [1235](#)
- WDOG_DRV_Deinit
 - WDOG Driver, [1235](#)
- WDOG_DRV_GetConfig
 - WDOG Driver, [1235](#)
- WDOG_DRV_GetCounter
 - WDOG Driver, [1235](#)
- WDOG_DRV_GetDefaultConfig
 - WDOG Driver, [1236](#)
- WDOG_DRV_GetTestMode
 - WDOG Driver, [1236](#)
- WDOG_DRV_Init
 - WDOG Driver, [1236](#)
- WDOG_DRV_SetInt
 - WDOG Driver, [1236](#)
- WDOG_DRV_SetMode
 - WDOG Driver, [1237](#)
- WDOG_DRV_SetTestMode
 - WDOG Driver, [1237](#)
- WDOG_DRV_SetTimeout
 - WDOG Driver, [1237](#)
- WDOG_DRV_SetWindow
 - WDOG Driver, [1238](#)
- WDOG_DRV_Trigger
 - WDOG Driver, [1238](#)
- WDOG_LPO_CLOCK
 - WDOG Driver, [1234](#)
- WDOG_SIRC_CLOCK
 - WDOG Driver, [1234](#)
- WDOG_SOSC_CLOCK
 - WDOG Driver, [1234](#)
- WDOG_STOP_MODE
 - WDOG Driver, [1234](#)
- WDOG_TST_DISABLED
 - WDOG Driver, [1235](#)
- WDOG_TST_HIGH
 - WDOG Driver, [1235](#)

- WDOG_TST_LOW
 - WDOG Driver, [1235](#)
- WDOG_TST_USER
 - WDOG Driver, [1235](#)
- WDOG_WAIT_MODE
 - WDOG Driver, [1234](#)
- WMC_AUTONOMOUS
 - 02. Watchdog, [215](#)
- WMC_TIMEOUT
 - 02. Watchdog, [215](#)
- WMC_WINDOW
 - 02. Watchdog, [215](#)
- WOLF_EVENT, [1334](#)
 - context, [1334](#)
 - dev, [1334](#)
 - flags, [1335](#)
 - next, [1335](#)
 - prev, [1335](#)
 - ptr, [1335](#)
 - ret, [1335](#)
 - state, [1335](#)
 - threadId, [1335](#)
 - type, [1335](#)
- WOLF_EVENT_QUEUE, [1335](#)
 - count, [1335](#)
 - head, [1335](#)
 - lock, [1336](#)
 - tail, [1336](#)
- WOLFSSL, [1336](#)
 - alert_history, [1337](#)
 - arrays, [1337](#)
 - buffers, [1337](#)
 - chVersion, [1337](#)
 - cipher, [1337](#)
 - ctx, [1337](#)
 - curRL, [1337](#)
 - curSize, [1337](#)
 - decrypt, [1337](#)
 - devId, [1337](#)
 - encrypt, [1337](#)
 - error, [1337](#)
 - fragOffset, [1338](#)
 - heap, [1338](#)
 - hmac, [1338](#)
 - hsDoneCb, [1338](#)
 - hsDoneCtx, [1338](#)
 - hsHashes, [1338](#)
 - hsKey, [1338](#)
 - hsType, [1338](#)
 - IOCB_ReadCtx, [1338](#)
 - IOCB_WriteCtx, [1338](#)
 - keepCert, [1338](#)
 - keys, [1338](#)
 - msgsReceived, [1338](#)
 - options, [1338](#)
 - peerRsaKey, [1338](#)
 - peerRsaKeyPresent, [1339](#)
 - pssAlgo, [1339](#)
 - rfd, [1339](#)
 - rflags, [1339](#)
 - rng, [1339](#)
 - session, [1339](#)
 - specs, [1339](#)
 - suites, [1339](#)
 - timeout, [1339](#)
 - verifyCallback, [1339](#)
 - verifyCbCtx, [1339](#)
 - version, [1339](#)
 - wfd, [1339](#)
 - wflags, [1339](#)
- WOLFSSL_ALERT, [1340](#)
 - code, [1340](#)
 - level, [1340](#)
- WOLFSSL_ALERT_HISTORY, [1340](#)
 - last_rx, [1340](#)
 - last_tx, [1340](#)
- WOLFSSL_ASN1_BIT_STRING, [1341](#)
 - data, [1341](#)
 - flags, [1341](#)
 - length, [1341](#)
 - type, [1341](#)
- WOLFSSL_ASN1_INTEGER, [1341](#)
 - data, [1341](#)
- WOLFSSL_ASN1_OBJECT, [1342](#)
 - dynamic, [1342](#)
 - heap, [1342](#)
 - obj, [1342](#)
 - objSz, [1342](#)
 - type, [1342](#)
- WOLFSSL_ASN1_STRING, [1342](#)
 - data, [1343](#)
 - flags, [1343](#)
 - length, [1343](#)
 - type, [1343](#)
- WOLFSSL_ASN1_TIME, [1343](#)
 - data, [1343](#)
- WOLFSSL_BIGNUM, [1343](#)
 - internal, [1344](#)
 - neg, [1344](#)
- WOLFSSL_BIO, [1344](#)
 - close, [1344](#)
 - eof, [1344](#)
 - fd, [1344](#)
 - file, [1345](#)
 - heap, [1345](#)
 - mem, [1345](#)
 - memLen, [1345](#)
 - next, [1345](#)
 - pair, [1345](#)
 - prev, [1345](#)
 - rdIdx, [1345](#)
 - readRq, [1345](#)
 - ssl, [1345](#)
 - type, [1345](#)
 - wrIdx, [1345](#)
 - wrSz, [1345](#)

- WOLFSSL_BIO_METHOD, [1346](#)
 - type, [1346](#)
- WOLFSSL_BUFFER_INFO, [1346](#)
 - buffer, [1346](#)
 - length, [1346](#)
- WOLFSSL_CERT_MANAGER, [1346](#)
 - caCacheCallback, [1347](#)
 - caLock, [1347](#)
 - caTable, [1347](#)
 - cbMissingCRL, [1347](#)
 - crl, [1347](#)
 - crlCheckAll, [1347](#)
 - crlEnabled, [1347](#)
 - heap, [1347](#)
 - minRsaKeySz, [1348](#)
 - ocsp, [1348](#)
 - ocspCheckAll, [1348](#)
 - ocspEnabled, [1348](#)
 - ocspIOCb, [1348](#)
 - ocspIOCtx, [1348](#)
 - ocspOverrideURL, [1348](#)
 - ocspRespFreeCb, [1348](#)
 - ocspSendNonce, [1348](#)
 - ocspStaplingEnabled, [1348](#)
 - ocspUseOverrideURL, [1348](#)
- WOLFSSL_CIPHER, [1349](#)
 - ssl, [1349](#)
- WOLFSSL_COMP_METHOD, [1349](#)
 - type, [1350](#)
- WOLFSSL_CRL, [1350](#)
 - cm, [1350](#)
 - crlList, [1350](#)
 - crlLock, [1350](#)
 - heap, [1350](#)
 - monitors, [1350](#)
- WOLFSSL_CTX, [1351](#)
 - CBIORcv, [1352](#)
 - CBIOSend, [1352](#)
 - certChain, [1352](#)
 - certificate, [1352](#)
 - client_psk_cb, [1352](#)
 - cm, [1352](#)
 - countMutex, [1352](#)
 - devId, [1352](#)
 - err, [1352](#)
 - failNoCert, [1352](#)
 - failNoCertxPSK, [1352](#)
 - groupMessages, [1352](#)
 - haveDH, [1352](#)
 - haveECC, [1353](#)
 - haveECDSAsig, [1353](#)
 - haveEMS, [1353](#)
 - haveNTRU, [1353](#)
 - havePSK, [1353](#)
 - haveRSA, [1353](#)
 - haveStaticECC, [1353](#)
 - heap, [1353](#)
 - method, [1353](#)
 - minDhKeySz, [1353](#)
 - minDowngrade, [1353](#)
 - minRsaKeySz, [1353](#)
 - partialWrite, [1353](#)
 - privateKey, [1353](#)
 - privateKeySz, [1353](#)
 - privateKeyType, [1354](#)
 - quietShutdown, [1354](#)
 - refCount, [1354](#)
 - sendVerify, [1354](#)
 - server_hint, [1354](#)
 - server_psk_cb, [1354](#)
 - serverDH_G, [1354](#)
 - serverDH_P, [1354](#)
 - sessionCacheFlushOff, [1354](#)
 - sessionCacheOff, [1354](#)
 - suites, [1354](#)
 - timeout, [1354](#)
 - useClientOrder, [1354](#)
 - verifyCallback, [1354](#)
 - verifyNone, [1354](#)
 - verifyPeer, [1355](#)
- WOLFSSL_Cipher, [1348](#)
 - aes, [1349](#)
 - arc4, [1349](#)
 - des, [1349](#)
 - des3, [1349](#)
- WOLFSSL_DH, [1355](#)
 - exSet, [1355](#)
 - g, [1355](#)
 - inSet, [1355](#)
 - internal, [1355](#)
 - length, [1355](#)
 - p, [1355](#)
 - priv_key, [1355](#)
 - pub_key, [1356](#)
 - q, [1356](#)
- WOLFSSL_DSA, [1356](#)
 - exSet, [1356](#)
 - g, [1356](#)
 - inSet, [1356](#)
 - internal, [1356](#)
 - p, [1356](#)
 - priv_key, [1356](#)
 - pub_key, [1357](#)
 - q, [1357](#)
- WOLFSSL_DTLS_CTX, [1357](#)
 - peer, [1357](#)
 - rfd, [1357](#)
 - wfd, [1357](#)
- WOLFSSL_DTLS_PEERSEQ, [1357](#)
 - nextEpoch, [1358](#)
 - nextSeq_hi, [1358](#)
 - nextSeq_lo, [1358](#)
 - prevSeq_hi, [1358](#)
 - prevSeq_lo, [1358](#)
 - prevWindow, [1358](#)
 - window, [1358](#)

- WOLFSSL_EC_GROUP, 1358
 - curve_idx, 1359
 - curve_nid, 1359
 - curve_oid, 1359
- WOLFSSL_EC_KEY, 1359
 - exSet, 1359
 - group, 1359
 - inSet, 1359
 - internal, 1359
 - priv_key, 1359
 - pub_key, 1359
- WOLFSSL_EC_POINT, 1360
 - exSet, 1360
 - inSet, 1360
 - internal, 1360
 - X, 1360
 - Y, 1360
 - Z, 1360
- WOLFSSL_ECDSA_SIG, 1361
 - r, 1361
 - s, 1361
- WOLFSSL_EVP_CIPHER_CTX, 1361
 - block_size, 1361
 - buf, 1361
 - bufUsed, 1362
 - cipher, 1362
 - cipherType, 1362
 - enc, 1362
 - flags, 1362
 - iv, 1362
 - keyLen, 1362
 - lastBlock, 1362
 - lastUsed, 1362
- WOLFSSL_EVP_MD_CTX, 1362
 - hash, 1362
 - macType, 1363
- WOLFSSL_EVP_PKEY, 1363
 - pkey, 1363
 - pkey_sz, 1363
 - ptr, 1363
 - save_type, 1363
 - type, 1363
- WOLFSSL_HMAC_CTX, 1364
 - hmac, 1364
 - type, 1364
- WOLFSSL_Hasher, 1363
 - md5, 1364
 - sha, 1364
 - sha256, 1364
- WOLFSSL_MD4_CTX, 1365
 - buffer, 1365
- WOLFSSL_MD5_CTX, 1365
 - holder, 1365
- WOLFSSL_METHOD, 1365
 - downgrade, 1366
 - side, 1366
 - version, 1366
- WOLFSSL_OCSP, 1366
 - cm, 1366
 - ocspList, 1366
 - ocspLock, 1366
- WOLFSSL_RIPEMD_CTX, 1367
 - holder, 1367
- WOLFSSL_RSA, 1367
 - d, 1367
 - dmp1, 1367
 - dmq1, 1367
 - e, 1368
 - exSet, 1368
 - inSet, 1368
 - internal, 1368
 - iqmp, 1368
 - n, 1368
 - p, 1368
 - q, 1368
- WOLFSSL_SESSION, 1368
 - bornOn, 1369
 - haveEMS, 1369
 - idLen, 1369
 - isDynamic, 1369
 - masterSecret, 1369
 - serverID, 1369
 - sessionID, 1369
 - sessionIDSz, 1369
 - staticTicket, 1369
 - ticket, 1369
 - ticketLen, 1369
 - timeout, 1369
- WOLFSSL_SHA256_CTX, 1370
 - holder, 1370
- WOLFSSL_SHA_CTX, 1370
 - holder, 1370
- WOLFSSL_SOCKADDR, 1370
 - sa, 1371
 - sz, 1371
- WOLFSSL_STACK, 1371
 - bio, 1371
 - data, 1371
 - name, 1371
 - next, 1371
 - num, 1371
 - obj, 1372
 - string, 1372
 - x509, 1372
- WOLFSSL_X509, 1373
 - altNames, 1373
 - altNamesNext, 1373
 - derCert, 1373
 - dynamicMemory, 1373
 - heap, 1373
 - isCa, 1373
 - issuer, 1373
 - notAfter, 1374
 - notAfterSz, 1374
 - notBefore, 1374
 - notBeforeSz, 1374

- pubKey, [1374](#)
- pubKeyOID, [1374](#)
- serial, [1374](#)
- serialSz, [1374](#)
- sig, [1374](#)
- sigOID, [1374](#)
- subject, [1374](#)
- subjectCN, [1374](#)
- version, [1374](#)
- WOLFSSL_X509_CHAIN, [1375](#)
 - certs, [1375](#)
 - count, [1375](#)
- WOLFSSL_X509_LOOKUP, [1375](#)
 - store, [1375](#)
- WOLFSSL_X509_LOOKUP_METHOD, [1375](#)
 - type, [1376](#)
- WOLFSSL_X509_NAME, [1376](#)
 - dynamicName, [1376](#)
 - name, [1376](#)
 - staticName, [1376](#)
 - sz, [1376](#)
- WOLFSSL_X509_OBJECT, [1377](#)
 - crl, [1377](#)
 - data, [1377](#)
 - ptr, [1377](#)
 - x509, [1377](#)
- WOLFSSL_X509_REVOKED, [1377](#)
 - serialNumber, [1377](#)
- WOLFSSL_X509_STORE, [1378](#)
 - cache, [1378](#)
 - cm, [1378](#)
 - lookup, [1378](#)
- WOLFSSL_X509_STORE_CTX, [1378](#)
 - certs, [1379](#)
 - chain, [1379](#)
 - current_cert, [1379](#)
 - discardSessionCerts, [1379](#)
 - domain, [1379](#)
 - error, [1379](#)
 - error_depth, [1379](#)
 - ex_data, [1379](#)
 - store, [1379](#)
 - totalCerts, [1379](#)
 - userCtx, [1379](#)
- WTDC_ADDRESS
 - Register address map, [1032](#)
- WTDS_ADDRESS
 - Register address map, [1032](#)
- wait
 - wdg_option_mode_t, [1224](#)
 - wdog_op_mode_t, [1233](#)
- wakeInRatiometricThreshold
 - phy_tja110x_config_t, [1140](#)
- wakePin
 - sbc_int_config_t, [1183](#)
 - sbc_status_group_t, [1191](#)
- wakePinEvt
 - sbc_evn_capt_t, [1189](#)
- wakeup
 - phy_driver_t, [950](#)
 - TJA110x PHY, [1146](#)
- watchdog
 - sbc_int_config_t, [1183](#)
- Watchdog Peripheral Abstraction Layer (WDG PAL), [1239](#)
- Watchdog timer (WDOG), [1242](#)
- watchdogCtr
 - drv_config_t, [1276](#)
- wc_HashAlg, [1332](#)
 - md5, [1332](#)
 - sha, [1332](#)
 - sha256, [1332](#)
- wdCntErr
 - fs45_wd_cnt_reg_t, [1059](#)
- wdCntReg
 - fs45_drv_config_t, [1063](#)
- wdCntRfr
 - fs45_wd_cnt_reg_t, [1059](#)
- wdlImpact
 - fs45_sf_impact_reg_t, [1059](#)
- wdcWatchdogCfg
 - uja113x_init_cfg_t, [185](#)
- wdf
 - sbc_sys_evnt_stat_t, [1187](#)
- wdg_clock_source_t
 - WDG PAL, [1225](#)
- wdg_config_t, [1224](#)
 - clkSource, [1225](#)
 - extension, [1225](#)
 - intEnable, [1225](#)
 - opMode, [1225](#)
 - percentWindow, [1225](#)
 - prescalerEnable, [1225](#)
 - timeoutValue, [1225](#)
 - winEnable, [1225](#)
- wdg_in_assert_logic_t
 - WDG PAL, [1226](#)
- wdg_inst_type_t
 - WDG PAL, [1226](#)
- wdg_instance_t, [1333](#)
 - instIdx, [1334](#)
 - instType, [1334](#)
- wdg_option_mode_t, [1224](#)
 - debug, [1224](#)
 - stop, [1224](#)
 - wait, [1224](#)
- wdog_clk_source_t
 - WDOG Driver, [1234](#)
- wdog_op_mode_t, [1233](#)
 - debug, [1233](#)
 - stop, [1233](#)
 - wait, [1233](#)
- wdog_set_mode_t
 - WDOG Driver, [1234](#)
- wdog_test_mode_t
 - WDOG Driver, [1234](#)

- wdog_user_config_t, [1233](#)
 - clkSource, [1233](#)
 - intEnable, [1233](#)
 - opMode, [1233](#)
 - prescalerEnable, [1234](#)
 - timeoutValue, [1234](#)
 - updateEnable, [1234](#)
 - winEnable, [1234](#)
 - windowValue, [1234](#)
- wds
 - sbc_wtdog_status_t, [1184](#)
- weOwnAltNames
 - DecodedCert, [1269](#)
- weOwnCert
 - Buffers, [1253](#)
- weOwnCertChain
 - Buffers, [1253](#)
- weOwnDH
 - Buffers, [1253](#)
- weOwnKey
 - Buffers, [1253](#)
- weOwnRng
 - Options, [1304](#)
- wfd
 - WOLFSSL, [1339](#)
 - WOLFSSL_DTLS_CTX, [1357](#)
- wflags
 - WOLFSSL, [1339](#)
- whichPcs
 - lpspi_master_config_t, [777](#)
 - lpspi_slave_config_t, [781](#)
- winEnable
 - wdg_config_t, [1225](#)
 - wdog_user_config_t, [1234](#)
- window
 - WOLFSSL_DTLS_PEERSEQ, [1358](#)
- windowValue
 - wdog_user_config_t, [1234](#)
- wolfssl_Tl_Hash, [1372](#)
 - hash, [1372](#)
 - len, [1372](#)
 - msg, [1372](#)
 - used, [1372](#)
- Word0Width
 - sai_user_config_t, [1041](#)
- word_status
 - lin_protocol_state_t, [843](#)
- wordAddressable
 - qspi_user_config_t, [1313](#)
- WordNWidth
 - sai_user_config_t, [1041](#)
- wordWidth
 - i2s_user_config_t, [677](#)
- workCtx
 - Rabbit, [1314](#)
- workMode
 - lptmr_config_t, [795](#)
- wpe
 - sbc_gl_evnt_stat_t, [1186](#)
- wpf
 - sbc_wake_evnt_stat_t, [1188](#)
- wpfe
 - sbc_wake_t, [1181](#)
- wpr
 - sbc_wake_evnt_stat_t, [1188](#)
- wpre
 - sbc_wake_t, [1181](#)
- wrIdx
 - WOLFSSL_BIO, [1345](#)
- wrSz
 - WOLFSSL_BIO, [1345](#)
- wrcnts
 - sbc_mtpnv_stat_t, [1190](#)
- write
 - phy_driver_t, [950](#)
- writeData
 - fs45_tx_data_t, [1283](#)
- writeExtendedConfig
 - TJA110x PHY, [1146](#)
- writeMMD
 - phy_driver_t, [950](#)
- writeTranspose
 - crc_user_config_t, [290](#)
- wsPin
 - extension_flexio_for_i2s_t, [678](#)
 - flexio_i2s_master_user_config_t, [544](#)
 - flexio_i2s_slave_user_config_t, [546](#)
- wtdModeCtrl
 - uja113x_wtdc_cfg_t, [214](#)
- wtdog
 - sbc_status_group_t, [1191](#)
- wu1Reg
 - fs45_drv_config_t, [1063](#)
- wu2Reg
 - fs45_drv_config_t, [1063](#)
- wulo0
 - fs45_wu1_reg_t, [1053](#)
- wulo2
 - fs45_wu1_reg_t, [1053](#)
- wulo3
 - fs45_wu1_reg_t, [1053](#)
- wulo4
 - fs45_wu1_reg_t, [1053](#)
- wulo5
 - fs45_wu2_reg_t, [1054](#)
- X
 - HC128, [1287](#)
 - WOLFSSL_EC_POINT, [1360](#)
- x
 - Arc4, [1249](#)
 - DsaKey, [1276](#)
 - RabbitCtx, [1314](#)
- x509
 - WOLFSSL_STACK, [1372](#)
 - WOLFSSL_X509_OBJECT, [1377](#)
 - x509_buffer, [1379](#)

- buffer, [1380](#)
- length, [1380](#)
- XOSC_EXT_REF
 - Clock Manager Driver, [349](#)
- XOSC_INT_OSC
 - Clock Manager Driver, [349](#)
- xorOut
 - crc_spec_t, [248](#)
- xosc_ref_t
 - Clock Manager Driver, [349](#)
- Y
 - HC128, [1287](#)
 - WOLFSSL_EC_POINT, [1360](#)
- y
 - Arc4, [1249](#)
 - DsaKey, [1277](#)
- YEAR_RANGE_END
 - RTC Driver, [1006](#)
- YEAR_RANGE_START
 - RTC Driver, [1006](#)
- year
 - rtc_timedate_t, [1001](#)
- Z
 - WOLFSSL_EC_POINT, [1360](#)