life.augmented

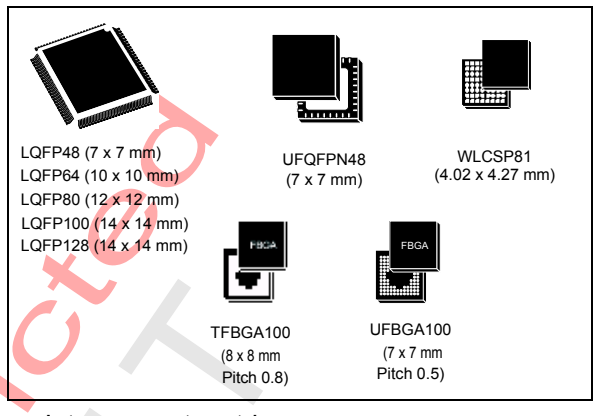
STM32G471xC
STM32G471xE

Arm® Cortex®-M4 32b MCU+FPU, up to 512 KB Flash, 170MHz / 213DMIPS, 128KB SRAM, Analog rich, Math accelerator

Datasheet - preliminary data

Features

- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 170 MHz with 213 DMIPS, MPU, DSP instructions
- Operating conditions:
  - VDD, VDDA voltage range: 1.71 V to 3.6 V
- Mathematical HW accelerator
  - CORDIC for trigonometric functions acceleration
  - FMAC: Filter mathematical accelerator
- Memories
  - 512 Kbytes of Flash memory with ECC support, two banks read-while-write, proprietary code readout protection (PCROP), Securable memory area
  - 96 Kbytes of SRAM, with HW parity check implemented on the first Kbytes
  - Routine booster: 32 Kbytes of SRAM on instruction and data bus, with HW parity check (CCM SRAM)
- Reset and supply management
  - Power-on/Power-down reset (POR/PDR/BOR)
  - Programmable voltage detector (PVD)
  - Low-power modes: sleep, stop, standby and shutdown
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 48 MHz crystal oscillator
  - 32 kHz oscillator with calibration
  - Internal 16 MHz RC with PLL option (± 1%)
  - Internal 32 kHz RC oscillator (± 5%)
- Up to 107 fast I/Os
  - All mappable on external interrupt vectors
  - Several I/Os with 5 V tolerant capability



- Interconnect matrix
- 16-channel DMA controller
- 3 x ADCs 0.20 µs up to 35 channels. Resolution up to 16-bit with hardware oversampling, 0 to 3.6 V conversion range
- 4 x 12-bit DAC channels
  - 2 x buffered external channels 1MSPS
  - 2 x unbuffered internal channels 15 MSPS
- 4 x ultra-fast rail-to-rail analog comparators
- 3 x operational amplifiers that can be used in PGA mode, all terminals accessible
- 15 timers:
  - 2 x 32-bit timer and 2 x 16-bit timers with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 2 x 16-bit 8-channel advanced motor control timers, with up to 8 x PWM channels, dead time generation and emergency stop
  - 1 x 16-bit timer with 2 x IC/OCs, one OCN/PWM, dead time generation and emergency stop
  - 2 x 16-bit timers with IC/OC/OCN/PWM, dead time generation and emergency stop
  - 2 x watchdog timers (independent, window)
  - 1 x SysTick timer: 24-bit downcounter
  - 2 x 16-bit basic timers

  - 1 x low-power timer
- Calendar RTC with alarm, periodic wakeup from stop/standby
- Communication interfaces
  - 2 x FDCAN controller supporting Flexible data rate
  - 4 x I^2C Fast mode plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from stop
  - 5 x USART/UARTs (ISO 7816 interface, LIN, IrDA, modem control)
  - 1 x LPUART
  - 4 x SPIs, 4 to 16 programmable bit frames, 2 x with multiplexed half duplex I^2S interface
  - 1 x SAI (serial audio interface)
  - USB 2.0 full-speed interface with LPM and BCD support
  - IRTIM (Infrared interface)
  - USB Type-C™ /USB power delivery controller (UCPD)
- True random number generator (RNG)
- CRC calculation unit, 96-bit unique ID
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™

Table 1. Device summary

Reference	Part number
STM32G471xC	STM32G471CC, STM32G471RC, STM32G471VC, STM32G471QC
STM32G471xE	STM32G471CE, STM32G471ME, STM32G471RE, STM32G471VE, STM32G471QE

Contents

List of tables

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32G471xx microcontrollers.

This document should be read in conjunction with the STM32G4xx reference manual (RM0440). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the Arm®(a) Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32G471xx devices are based on the high-performance Arm® Cortex®-M4 32-bit RISC core. They operate at a frequency of up to 170 MHz.

The Cortex-M4 core features a single-precision floating-point unit (FPU), which supports all the Arm single-precision data-processing instructions and all the data types. It also implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) which enhances the application's security.

These devices embed high-speed memories (512 Kbytes of Flash memory, 128 Kbytes of SRAM), an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The devices also embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, Securable memory area and proprietary code readout protection.

The devices embed peripherals allowing mathematical/arithmetic function acceleration (CORDIC for trigonometric functions and FMAC unit for Filter Functions).

They offer three fast 12-bit ADCs (5 Msps), four comparators, three operational amplifiers, four DAC channels (2 external and 2 internal), an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timers, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and one 16-bit low-power timer.

They also feature standard and advanced communication interfaces such as:

- Four I2Cs
- Four SPIs multiplexed with two half duplex I2Ss
- Three USARTs, two UARTs and one low-power UART.
- Two FDCANs
- One SAI (Serial Audio Interfaces)
- USB device
- UCPD

The devices operate in the -40 to +85 °C (+105 °C junction), -40 to +105 °C (+125 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported including an analog independent supply input for ADC, DAC, OPAMPs and comparators. A VBAT input allows backup of the RTC and the registers.

The STM32G471xx family offers 9 packages from 48-pin to 128-pin.

Table 2. STM32G471xx features and peripheral counts

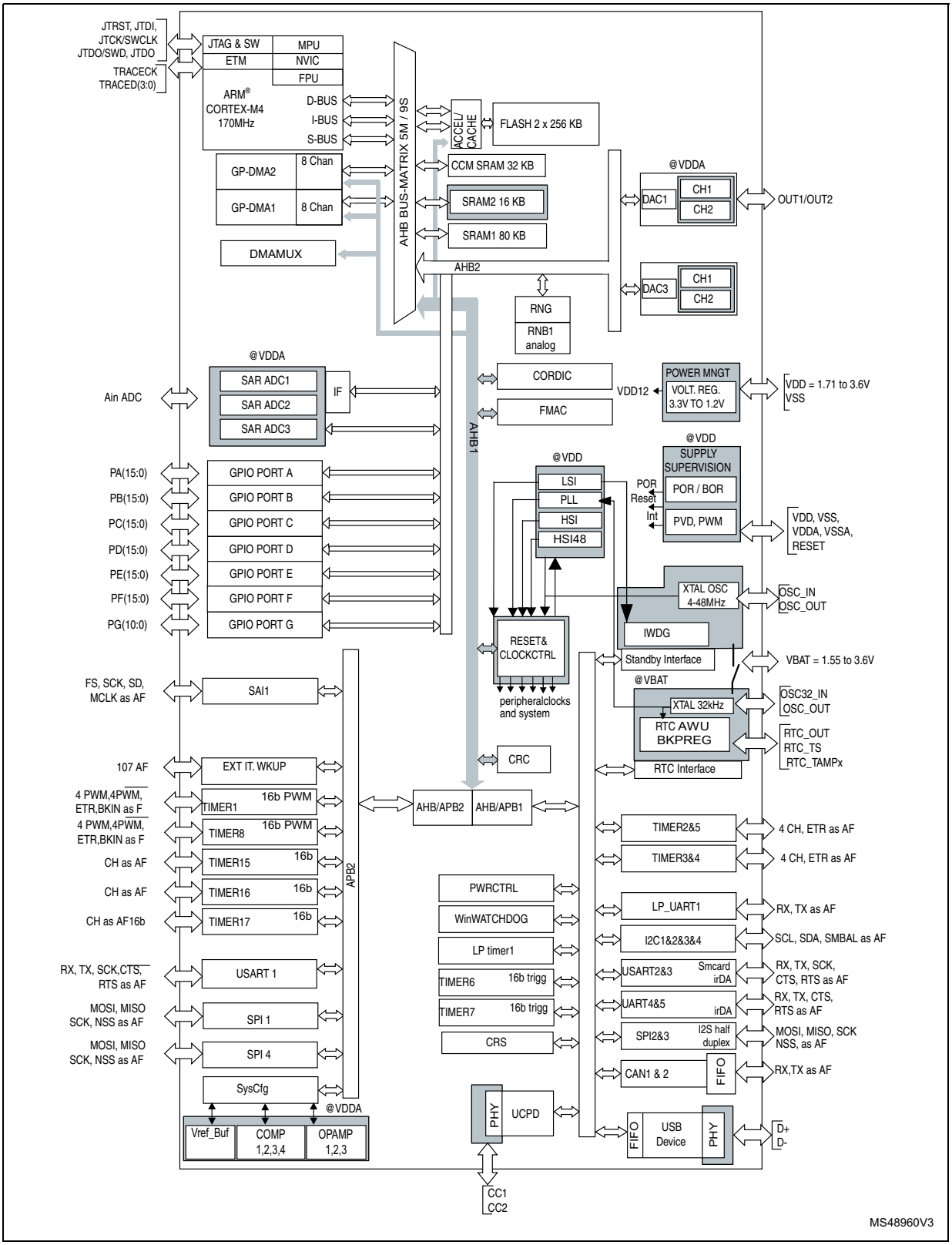
Peripheral		STM32G471 Cx		STM32G471 Rx		STM32G471 Mx		STM32G471 Vx		STM32G471 Qx	
Flash memory		256 KB	512 KB	256 KB	512 KB	256 KB	512 KB	256 KB	512 KB	256 KB	512 KB
SRAM		128 (80 + 16+ 32) KB									
Timers	Advanced motor control	2 (16-bit)									
	General purpose	5 (16-bit) 2 (32-bit)									
	Basic	2 (16-bit)									
	Low power	1 (16-bit)									
	SysTick timer	1									
	Watchdog timers (independent, window)	2									
	Total number of PWMs(1)	TBD		TBD		TBD		TBD		TBD	
Comm. interfaces	SPI(I2S)(2)	3 (2)				4 (2)					
	I^2C	4									
	USART	3									
	UART	0		2							
	LPUART	1									
	FDCANs	2									
	USB device	Yes									
	UCPD	Yes									
	SAI	Yes									
RTC		Yes									
Tamper pins		2				3					
Random number generator		Yes									
CORDIC		Yes									
FMAC		Yes									
GPIOs		38 in LQFP48 42 in UFQFPN48		52		67 in WLCSP81 66 in LQFP80		86		107	
Wakeup pins		3		4		4		5		5	
12-bit ADCs Number of channels		3									
		18 in LQFP48 19 in UFQFPN48		24		31 in LQFP80 32 in WLCSP81		35		35	
12-bit DAC Number of channels		2 4(2 external + 2internal)									
Internal voltage reference buffer		Yes									
Analog comparator		4									

Table 2. STM32G471xx features and peripheral counts (continued)

Peripheral	STM32G471 Cx	STM32G471 Rx	STM32G471 Mx	STM32G471 Vx	STM32G471 Qx
Operational amplifiers	3				
Max. CPU frequency	170 MHz				
Operating voltage	1.71 V to 3.6 V				
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C				
Packages	LQFP48/ UFQFPN48	LQFP64	LQFP80 WLCSP81	LQFP100/ TFBGA100	LQFP128

1. This corresponds to the total number of TIM1/8/20/2/3/4/5/15/16/17 PWMs, that could be used in parallel. It includes the number of complementary PWMs.
2. The SPI2/3 interfaces can work in an exclusive way in either the SPI mode or the I2S audio mode.

Figure 1. STM32G471xx block diagram



Note: AF: alternate function on I/O pins.

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of the MCU implementation, with a reduced pin count and with low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features an exceptional code-efficiency, delivering the expected high-performance from an Arm core in a memory size usually associated with 8-bit and 16-bit devices.

The processor supports a set of DSP instructions which allows an efficient signal processing and a complex algorithm execution. Its single precision FPU speeds up the software development by using metalanguage development tools to avoid saturation.

With its embedded Arm core, the STM32G471xx family is compatible with all Arm tools and software.

Figure 1 shows the general block diagram of the STM32G471xx devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator that is optimized for the STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to 8 protected areas, which can be divided in up into 8 subareas each. The protection area sizes range between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The STM32G471xx devices feature 512 kbytes of embedded Flash memory which is available for storing programs and data.

The Flash interface features:

- Single or dual bank operating modes
- Read-while-write (RWW) in dual bank mode

This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported.

Flexible protections can be configured thanks to the option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels of protection are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection; the Flash memory cannot be read from or written to if either the debug features are connected or the boot in RAM or bootloader are selected
  - Level 2: chip readout protection; the debug features (Cortex-M4 JTAG and serial wire), the boot in RAM and the bootloader selection are disabled (JTAG fuse). This selection is irreversible.
- Write protection (WRP): the protected area is protected against erasing and programming.
- Proprietary code readout protection (PCROP): a part of the Flash memory can be protected against read and write from third parties. The protected area is execute-only and it can only be reached by the STM32 CPU as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

- Securable memory area: a part of Flash memory can be configured by option bytes to be securable. After reset is this securable memory area not secured and it behaves like the remainder of MAin Flash memory (execute, read, write access). When secured (the SEC_PROTx bit is set FLASH_CR register), any access to this securable memory area generates corresponding read/write error (WRPERR flag or RDERR flag is set). Purpose of the Securable memory area is to protect sensitive code and data (secure keys storage) which can be executed only once at boot, and never again unless a new reset occurs.

The Flash memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- The address of the ECC fail can be read in the ECC register

3.5 Embedded SRAM

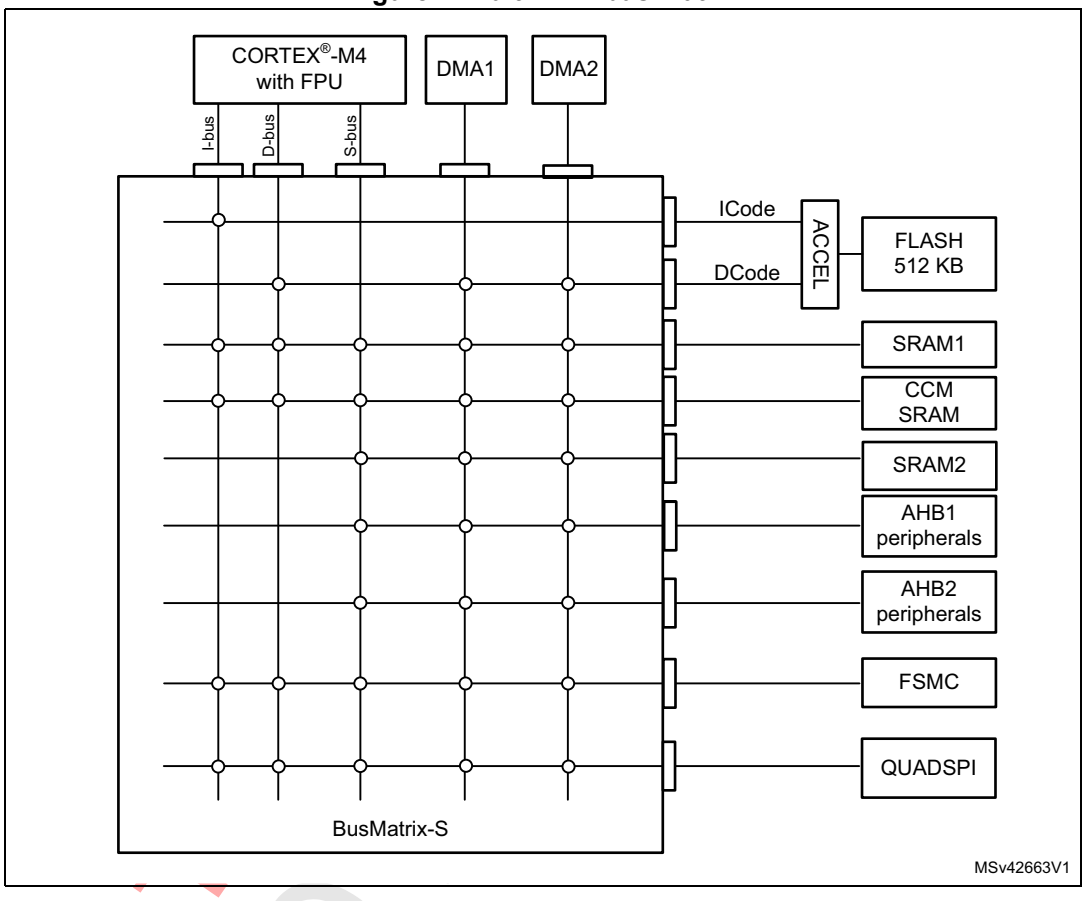
STM32G471xx devices feature 128 Kbyte of embedded SRAM. This SRAM is split into three blocks:

- 80 Kbyte mapped at address 0x2000 0000 (SRAM1). The CM4 can access the SRAM1 through the System Bus or through the I-Code/D-Code bus. The first 32 Kbyte of SRAM1 support hardware parity check.
- 16 Kbyte mapped at address 0x2001 4000 (SRAM2). The CM4 can access the SRAM2 through the System Bus or through the I-Code/D-Code bus. SRAM2 can be retained in standby modes.
- 32 Kbyte mapped at address 0x1000 0000 (CCM SRAM). It is accessed by the CPU through ICODE/DCODE bus for maximum performance.
  It is also aliased at 0x2001 8000 address to be accessed by all masters (CPU, DMA1, DMA2) through SBUS contiguously to SRAM1 and SRAM2. The CCM SRAM supports hardware parity check and can be write-protected with 1 Kbyte granularity.
- The memory can be accessed in read/write at max CPU clock speed with 0 wait states.

3.6 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, AHB and APB peripherals). It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 2. Multi-AHB bus matrix



3.7 Boot modes

At startup, a BOOT0 pin(or nBOOT0 option bit) and an nBOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The BOOT0 value may come from the PB8-BOOT0 pin or from an nBOOT0 option bit depending on the value of a user nBOOT_SEL option bit to free the GPIO pad if needed.

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, and USB through the DFU (device firmware upgrade).

3.8 CORDIC

The CORDIC provides hardware acceleration of certain mathematical functions, notably trigonometric, commonly used in motor control, metering, signal processing and many other applications.

It speeds up the calculation of these functions compared to a software implementation, allowing a lower operating frequency, or freeing up processor cycles in order to perform other tasks.

Cordic features

- 24-bit CORDIC rotation engine
- Circular and Hyperbolic modes
- Rotation and Vectoring modes
- Functions: Sine, Cosine, Sinh, Cosh, Atan, Atan2, Atanh, Modulus, Square root, Natural logarithm
- Programmable precision up to 20-bit
- Fast convergence: 4 bits per clock cycle
- Supports 16-bit and 32-bit fixed point input and output formats
- Low latency AHB slave interface
- Results can be read as soon as ready without polling or interrupt
- DMA read and write channels

3.9 Filter Mathematical ACcelerator (FMAC)

The filter mathematical accelerator unit performs arithmetic operations on vectors. It comprises a multiplier/accumulator (MAC) unit, together with address generation logic, which allows it to index vector elements held in local memory.

The unit includes support for circular buffers on input and output, which allows digital filters to be implemented. Both finite and infinite impulse response filters can be realized.

The unit allows frequent or lengthy filtering operations to be offloaded from the CPU, freeing up the processor for other tasks. In many cases it can accelerate such calculations compared to a software implementation, resulting in a speed-up of time critical tasks.

FMAC features

- 16 x 16-bit multiplier
- 24+2-bit accumulator with addition and subtraction
- 16-bit input and output data
- 256 x 16-bit local memory
- Up to three areas can be defined in memory for data buffers (two input, one output), defined by programmable base address pointers and associated size registers
- Input and output sample buffers can be circular
- Buffer “watermark” feature reduces overhead in interrupt mode
- Filter functions: FIR, IIR (direct form 1)
- AHB slave interface
- DMA read and write data channels

3.10 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the Flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and which can be stored at a given memory location.

3.11 Power supply management

3.11.1 Power supply schemes

The STM32G471xx devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies, can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V
  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
- V_{DDA} = 1.71 V (ADC) to 3.6 V.
  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is

independent from the V_{DD} voltage and should preferably be connected to V_{DD} when these peripherals are not used.

- V_{BAT} = 1.55 V to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

- V_{REF-}, V_{REF+}

  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

  When V_{DDA} < 2 V V_{REF+} must be equal to V_{DDA}.

  When V_{DDA} ≥ 2 V V_{REF+} must be between 2 V and V_{DDA}.

  The internal voltage reference buffer supports three output voltages, which are configured with VRS bits in the VREFBUF_CSR register:

  – V_{REF+} = 2.048 V
  – V_{REF+} = 2.5 V
  – V_{REF+} = 2.95 V

  V_{REF-} is double bonded with V_{SSA}.

3.11.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes (except for Shutdown mode). The BOR ensures proper operation of the devices after power-on and during power down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor which compares the independent supply voltages V_{DDA}, with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.11.3 Voltage regulator

Two embedded linear voltage regulators, main regulator (MR) and low-power regulator (LPR), supply most of digital circuitry in the device. The MR is used in Run and Sleep modes. The LPR is used in Low-power run, Low-power sleep and Stop modes. In Standby and Shutdown modes, both regulators are powered down and their outputs set in high-impedance state, such as to bring their current consumption close to zero.

The device supports dynamic voltage scaling to optimize its power consumption in Run mode. the voltage from the main regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

The main regulator (MR) operates in the following ranges:

- Range 1 boost mode with the CPU running at up to 170 MHz.
- Range 1 normal mode with CPU running at up to 150 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz.

3.11.4 Low-power modes

By default, the microcontroller is in Run mode after system or power Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep mode**: In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Low-power run mode:** This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.
- **Low-power sleep mode:** This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the Low power run mode.
- **Stop mode:** In Stop mode, the device achieves the lowest power consumption while retaining the SRAM and register contents. All clocks in the VCORE domain are stopped. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are disabled. The LSE or LSI keep running. The RTC can remain active (Stop mode with RTC, Stop mode without RTC). Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode, so as to get clock for processing the wakeup event.
- **Standby mode:** The Standby mode is used to achieve the lowest power consumption with brown-out reset, BOR. The internal regulator is switched off to power down the VCORE domain. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are also powered down. The RTC can remain active (Standby mode with RTC, Standby mode without RTC). The BOR always remains active in Standby mode. For each I/O, the software can determine whether a pull-up, a pull-down or no resistor shall be applied to that I/O during Standby mode. Upon entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and standby circuitry. The device exits Standby mode upon external reset event (NRST pin), IWDG reset event, wakeup event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wakeup, timestamp, tamper), or when a failure is detected on LSE (CSS on LSE).
- **Shutdown mode:** The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off to power down the VCORE domain. The PLL, as well as the HSI16 and LSI RC-oscillators and HSE crystal oscillator are also powered down. The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC). The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode. Therefore, switching to RTC domain is not supported. SRAM and register contents are lost except for registers in the RTC domain. The device exits Shutdown mode upon external reset event (NRST pin), IWDG reset event, wakeup event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wakeup, timestamp, tamper).

3.11.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.11.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when there is no external battery and when an external supercapacitor is present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

The VBAT operation is automatically activated when V_{DD} is not present. An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, neither external interrupts nor RTC alarm/events exit the microcontroller from the VBAT operation.

3.12 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep and Stop modes.

Table 3. STM32G471xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-
	ADCx DACx	Conversion triggers	Y	Y	Y	Y	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-
TIM16/TIM17	IRTIM	Infrared interface output generation	Y	Y	Y	Y	-
COMPx	TIM1, 8 TIM2, 3, 4	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-
	LPTIMER1	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y
ADCx	TIM1, 8	Timer triggered by analog watchdog	Y	Y	Y	Y	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-
	LPTIMER1	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y
All clocks sources (internal and external)	TIM15, 16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-

Table 3. STM32G471xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD	TIM1,8 TIM15,16,17	Timer break	Y	Y	Y	Y	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-
	LPTIMER1	External trigger	Y	Y	Y	Y	-
	ADCx DACx	Conversion external trigger	Y	Y	Y	Y	-

3.13 Clocks and startup

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** three different sources can deliver SYSCLK system clock:
  - 4 - 48 MHz high-speed oscillator with external crystal or ceramic resonator (HSE). It can supply clock to system PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software. It can supply clock to system PLL.
  - System PLL with maximum output frequency of 170 MHz. It can be fed with HSE or HSI16 clocks.
- **RC48 with clock recovery system (HSI48):** internal HSI48 MHz clock source can be used to drive the USB or the RNG peripherals.
- **Auxiliary clock source:** two ultra-low-power clock sources for the real-time clock (RTC):
  - 32.768 kHz low-speed oscillator with external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for using an external clock.
  - 32 kHz low-speed internal RC oscillator (LSI) with ±5% accuracy, also used to clock an independent watchdog.
- **Peripheral clock sources:** several peripherals (I2S, USART, I2C, LPTimer, ADC, SAI, RNG) have their own clock independent of the system clock.
- **Clock security system (CSS):** in the event of HSE clock failure, the system clock is automatically switched to HSI16 and, if enabled, a software interrupt is generated. LSE clock failure can also be detected and generate an interrupt.
- Clock-out capability:
  - **MCO:** microcontroller clock output: it outputs one of the internal clocks for external use by the application
  - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes.

Several prescalers allow to configure the AHB frequency, the High-speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 170 MHz.

3.14 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.15 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 4: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations.

The two DMA controllers have 16 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 16 independently configurable channels (requests)
  - Each channel is connected to a dedicated hardware DMA request, a software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are both software programmable (4 levels: very high, high, medium, low) or hardware programmable in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536.

Table 4. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	8	8

3.16 DMA request router (DMAMux)

When a peripheral indicates a request for DMA transfer by setting its DMA request line, the DMA request is pending until it is served and the corresponding DMA request line is reset. The DMA request router allows to route the DMA control lines between the peripherals and the DMA controllers of the product.

An embedded multi-channel DMA request generator can be considered as one of such peripherals. The routing function is ensured by a multi-channel DMA request line multiplexer. Each channel selects a unique set of DMA control lines, unconditionally or synchronously with events on synchronization inputs.

For simplicity, the functional description is limited to DMA request lines. The other DMA control lines are not shown in figures or described in the text. The DMA request generator produces DMA requests following events on DMA request trigger inputs.

3.17 Interrupts and events

3.17.1 Nested vectored interrupt controller (NVIC)

The STM32G471xx devices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and to handle up to TBD maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.17.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 44 edge detector lines used to generate interrupt/event requests and to wake-up the system from the Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently.

A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 107 GPIOs can be connected to the 16 external interrupt lines.

3.18 Analog-to-digital converter (ADC)

The device embeds three successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- One external reference pin is available on all packages, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into a data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching
  - Flexible sample time control
  - Hardware gain and offset compensation

3.18.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADCs input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 5. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA} = V_{REF+} = 3.0 V (± 10 mV)	TBD
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), V_{DDA} = V_{REF+} = 3.0 V (± 10 mV)	TBD

3.18.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and the comparators. The VREFINT is internally connected to the ADCx_IN18, x = 1,3 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.18.3 V_{BAT} battery voltage monitoring

This embedded hardware enables the application to measure the V_{BAT} battery voltage using the internal ADC1_IN17 channel. As the V_{BAT} voltage may be higher than the VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third of the V_{BAT} voltage.

3.19 Digital to analog converter (DAC)

Four 12 bit DAC channels (2 external buffered and 2 internal unbuffered) can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Saw tooth wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor
- Up to 1 Msps for external output and 15 Msps for internal output

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.20 Voltage reference buffer (V_{REFBUF})

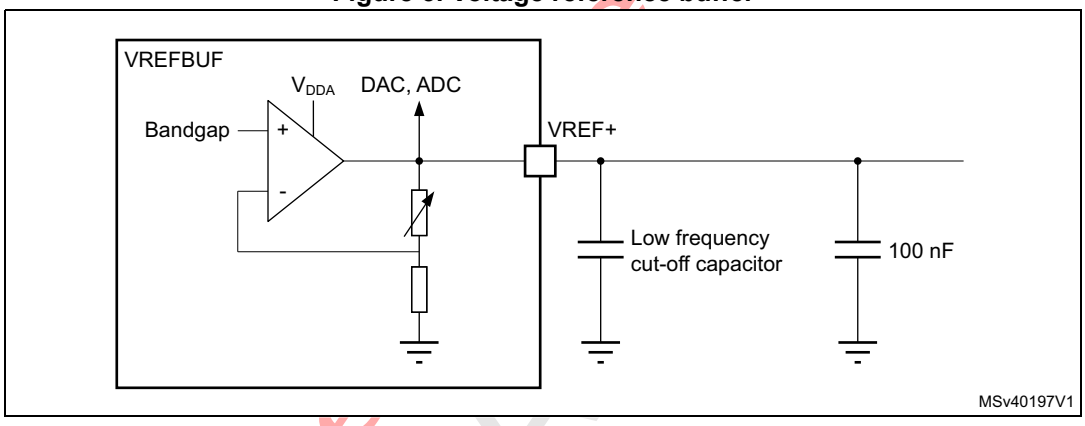
The STM32G471xx devices embed a voltage reference buffer which can be used as voltage reference for ADC, DACs and also as voltage reference for external components through the VREF+ pin.

The internal voltage reference buffer supports three voltages:

- 2.048 V
- 2.5 V
- 2.9 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

Figure 3. Voltage reference buffer



3.21 Comparators (COMP)

The STM32G471xx devices embed four rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers.

3.22 Operational amplifier (OPAMP)

The STM32G471xx devices embed three operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- 15 MHz bandwidth
- Rail-to-rail input/output
- PGA with a non-inverting gain ranging of 2, 4, 8, 16, 32 or 64 or inverting gain ranging of -1, -3, -7, -15, -31 or -63

3.23 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.24 Timers and watchdogs

The STM32G471xx devices include two advanced motor control timers, up to general-purpose timers, two basic timers, one low-power timer, two watchdog timers and a SysTick timer. The table below compares the features of the advanced motor control, general purpose and basic timers.

Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced motor control	TIM1, TIM8	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	4
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.24.1 Advanced motor control timer (TIM1, TIM8)

The advanced motor control timers can each be seen as a four-phase PWM multiplexed on 8 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced motor control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in *Section 3.24.2*) using the same architecture, so the advanced motor control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.24.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

There are up to seven synchronizable general-purpose timers embedded in the STM32G471xx devices (see *Table 6* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3, TIM4 and TIM5

  They are full-featured general-purpose timers:
  - TIM2 and TIM5 have a 32-bit auto-reload up/downcounter and 32-bit prescaler
  - TIM3 and TIM4 have 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.
- TIM15, 16 and 17

  They are general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.
  - TIM15 has 2 channels and 1 complementary channel
  - TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.24.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.24.4 Low-power timer (LPTIM1)

The devices embed a low-power timer. This timer has an independent clock and are running in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the system from Stop mode.

LPTIM1 is active in Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode

3.24.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.24.6 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.24.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.25 Real-time clock (RTC) and backup registers

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC is supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp) can generate an interrupt and wakeup the device from the low-power modes.

3.26 Tamper and backup registers (TAMP)

- 16 32-bit backup registers, retained in all low-power modes and also in VBAT mode. They can be used to store sensitive data as their content is protected by an tamper detection circuit. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.
- Up to three tamper pins for external tamper detection events. The external tamper pins can be configured for edge detection, edge and level, level detection with filtering.
- Five internal tampers events.
- Any tamper detection can generate a RTC timestamp event.
- Any tamper detection erases the backup registers.
- Any tamper detection can generate an interrupt and wake-up the device from all low-power modes.

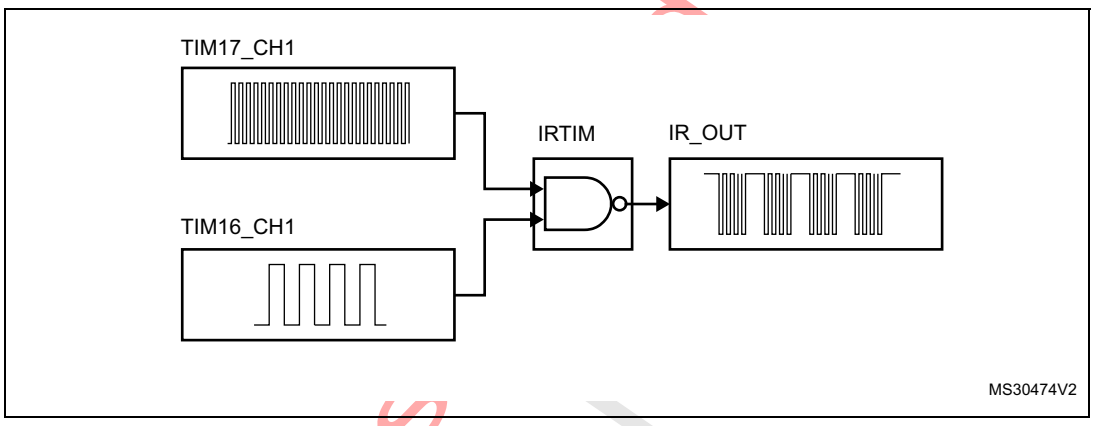
3.27 Infrared transmitter

The STM32G471xx devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 4. Infrared transmitter



3.28 Inter-integrated circuit interface (I^2C)

The device embeds four I2Cs. Refer to *Table 7: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 7. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Wakeup from Stop mode on address match	X	X	X	X

1. X: supported

3.29 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32G471xx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4, USART5).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN master/slave capability. They provide hardware management of the CTS and RTS signals, and RS485 driver enable.

The USART1, USART2 and USART3 also provide a Smartcard mode (ISO 7816 compliant) and an SPI-like communication capability.

The USART comes with a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3,4,5) to wake up the MCU from Stop mode. The wakeup from Stop mode can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Some specific TXFIFO/RXFIFO status interrupts when FIFO mode is enabled

All USART interfaces can be served by the DMA controller.

Table 8. USART/UART/LPUART features

USART modes/features(1)	USART1	USART2	USART3	UART4	UART5	LPUART1
Hardware flow control for modem	X	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X	X
Synchronous mode	X	X	X	-	-	-
Smartcard mode	X	X	X	-	-	-
Single-wire half-duplex communication	X	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X	-
LIN mode	X	X	X	X	X	-
Dual clock domain	X	X	X	X	X	X
Wakeup from Stop mode	X	X	X	X	X	X
Receiver timeout interrupt	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	-
Auto baud rate detection	X (4 modes)					-
Driver Enable	X	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits					

Table 8. USART/UART/LPUART features (continued)

USART modes/features(1)	USART1	USART2	USART3	UART4	UART5	LPUART1
Tx/Rx FIFO	X					
Tx/Rx FIFO size	8					

1. X = supported.

3.30 Low-power universal asynchronous receiver transmitter (LPUART)

The STM32G471xx devices embed one Low-Power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART comes with a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default. It has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode. The wake up from Stop mode can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Some specific TXFIFO/RXFIFO status interrupts when FIFO mode is enabled

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

3.31 Serial peripheral interface (SPI)

Four SPI interfaces allow communication up to TBD Mbits/s in master and up to TBD Mbits/s in slave, half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and hardware CRC calculation.

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

All SPI interfaces can be served by the DMA controller.

3.32 Serial audio interfaces (SAI)

The device embeds 1 SAI. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out.
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively. – Overrun and underrun detection. – Anticipated frame synchronization signal detection in slave mode. – Late frame synchronization signal detection in slave mode. – Codec not ready for the AC’97 mode in reception.
- Interruption sources when enabled: – Errors. – FIFO requests.
- DMA interface with 2 dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

Table 9. SAI implementation for the features implementation

SAI features	Support(1)
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97	X
Mute mode	X
Stereo/Mono audio frame capability	X
16 slots	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X
FIFO size	X (8 word)
SPDIF	X

1. X: supported.

3.33 Controller area network (FDCAN)

The controller area network (CAN) subsystem consists of two CAN modules and a shared message RAM memory.

The two CAN modules (FDCAN1 and FDCAN2) compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

A 2 Kbyte message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers.

3.34 Universal serial bus (USB)

The STM32G471xx devices embed a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

3.35 USB Type-C™ / USB Power Delivery controller (UCPD)

The device embeds one controller (UCPD) compliant with USB Type-C Rev. 1.2 and USB Power Delivery Rev. 3.0 specifications.

The controller uses specific I/Os supporting the USB Type-C and USB Power Delivery requirements, featuring:

- USB Type-C pull-up (Rp, all values) and pull-down (Rd) resistors
- “Dead battery” support
- USB Power Delivery message transmission and reception
- FRS (fast role swap) support

The digital controller handles notably:

- USB Type-C level detection with de-bounce, generating interrupts
- FRS detection, generating an interrupt
- Byte-level interface for USB Power Delivery payload, generating interrupts (DMA compatible)
- USB Power Delivery timing dividers (including a clock pre-scaler)
- CRC generation/checking
- 4b5b encode/decode
- Ordered sets (with a programmable ordered set mask at receive)
- Frequency recovery in receiver during preamble

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB Power Delivery messages and FRS signaling.

3.36 Clock recovery system (CRS)

The devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.37 Development support

3.37.1 Serial wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.37.2 Embedded Trace Macrocell™

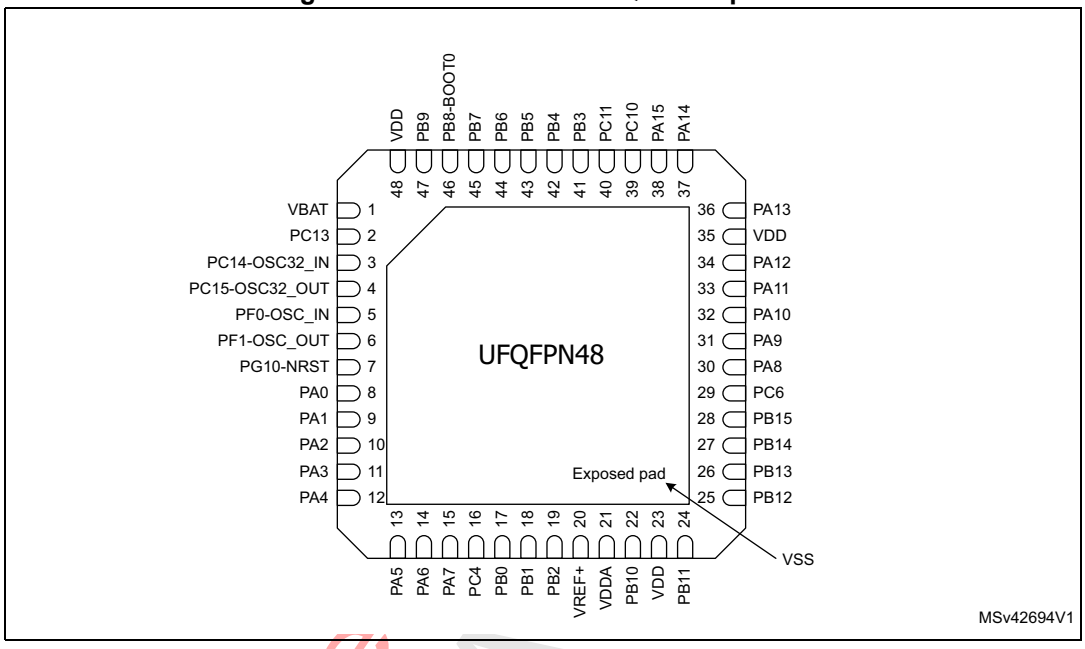
The Arm Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32G471xx devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

4 Pinouts and pin description

4.1 UFQFPN48 pinout description

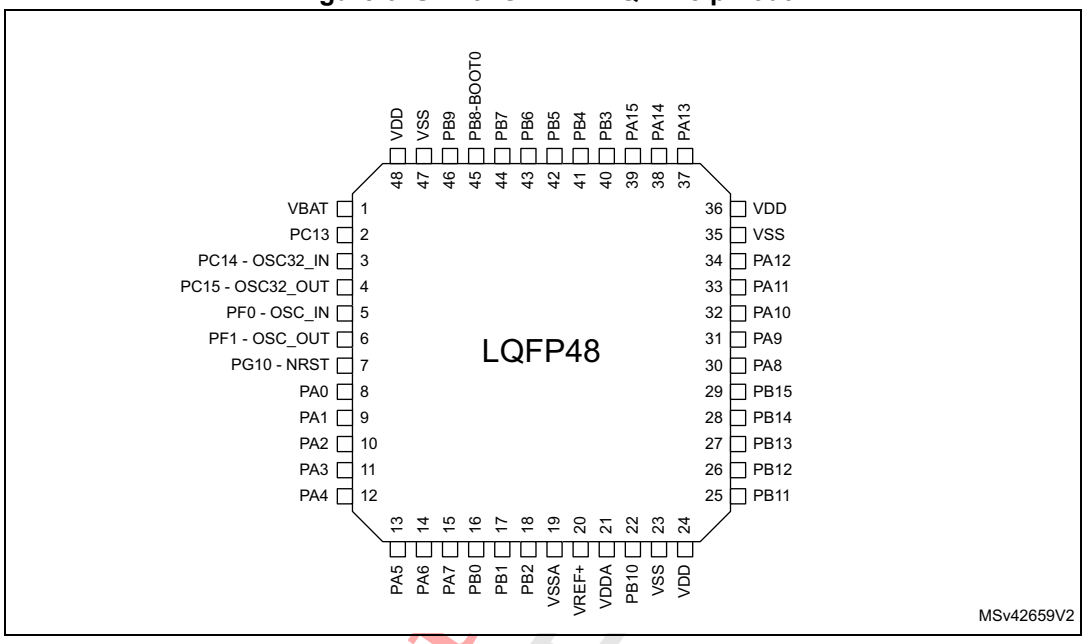
Figure 5. STM32G471xx UFQFPN48 pinout



1. The above figure shows the package top view
2. VSS pads are connected to the exposed pad.

4.2 LQFP48 pinout description

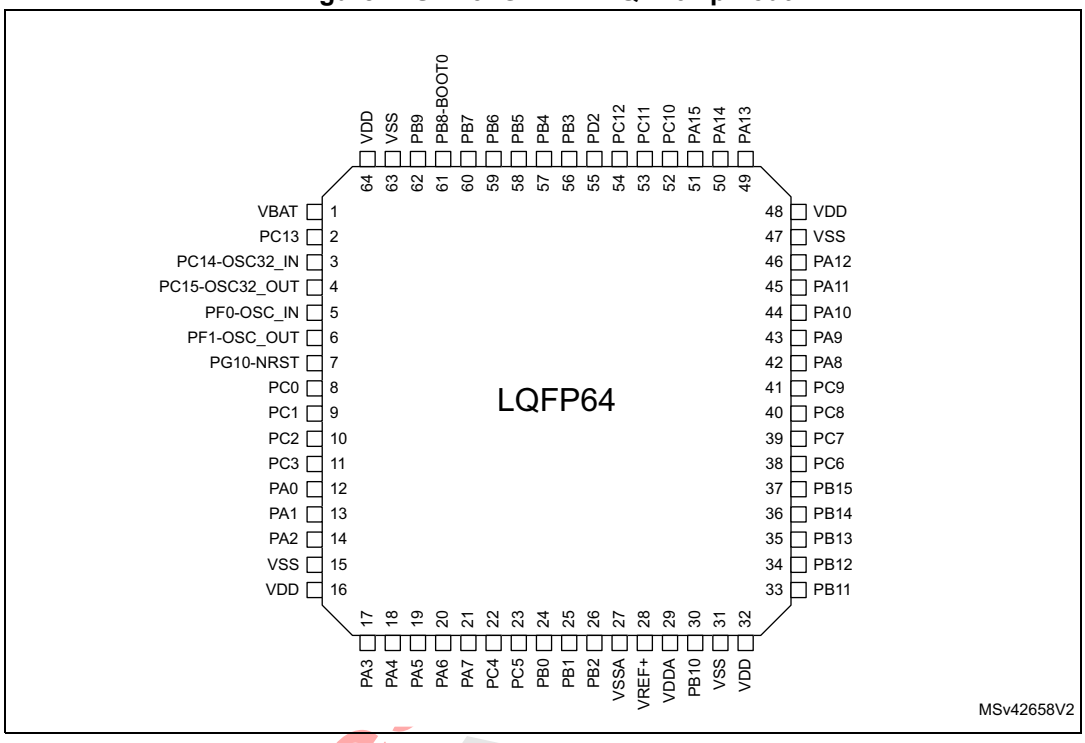
Figure 6. STM32G471xx LQFP48 pinout



1. The above figure shows the package top view

4.3 LQFP64 pinout description

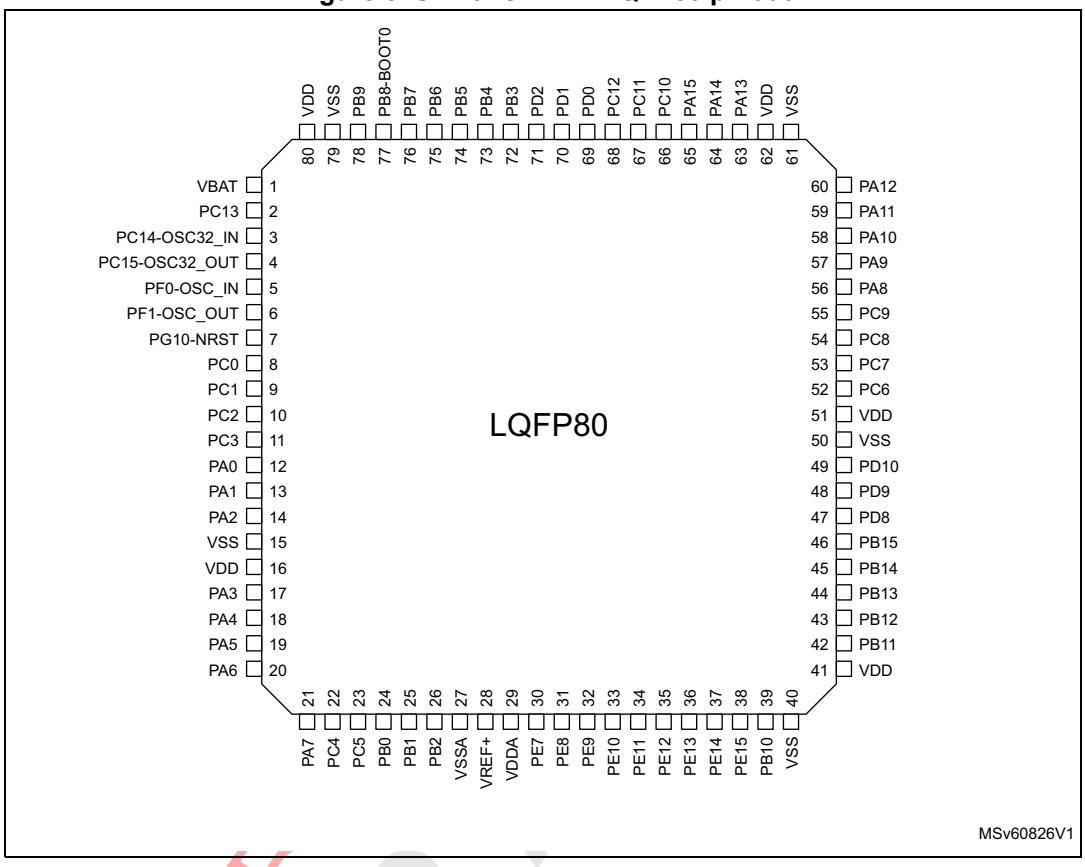
Figure 7. STM32G471xx LQFP64 pinout



1. The above figure shows the package top view.

4.4 LQFP80 pinout description

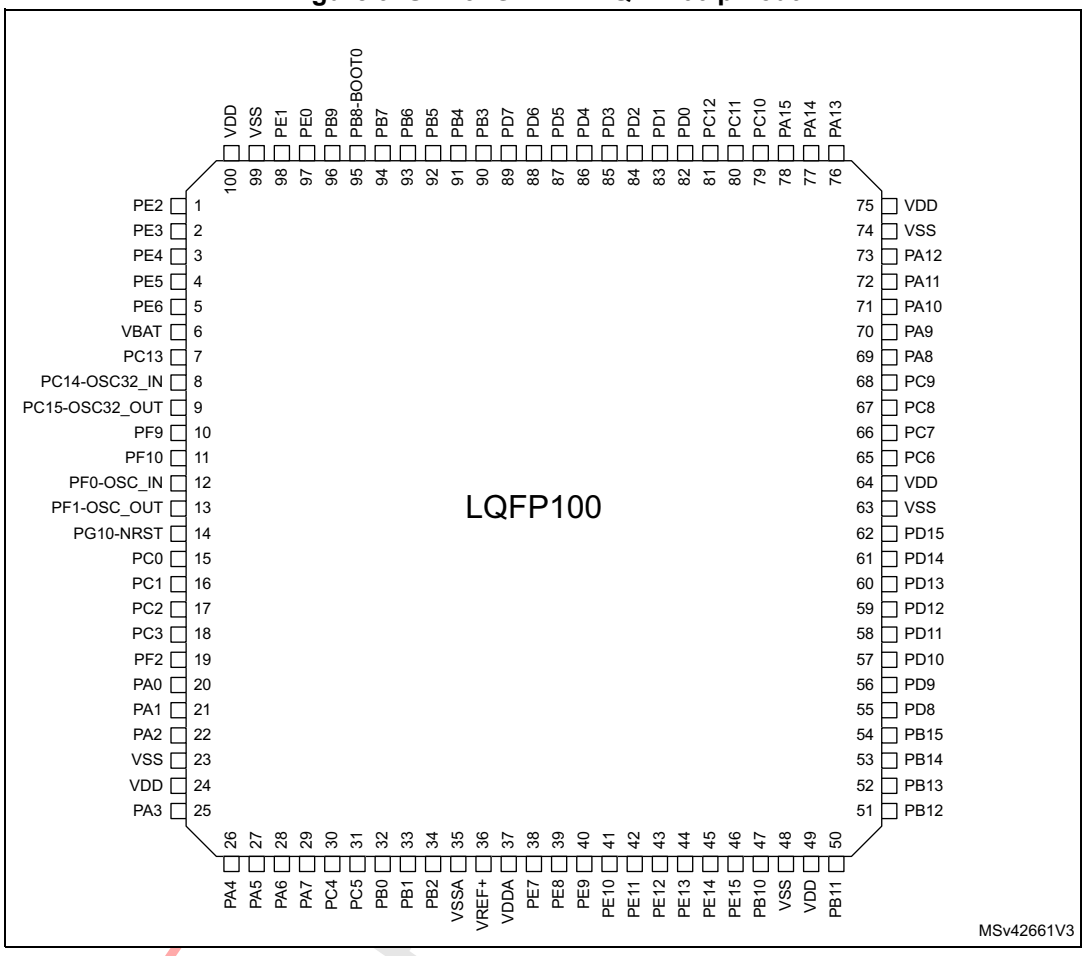
Figure 8. STM32G471xx LQFP80 pinout



1. The above figure shows the package top view.

4.5 LQFP100 pinout description

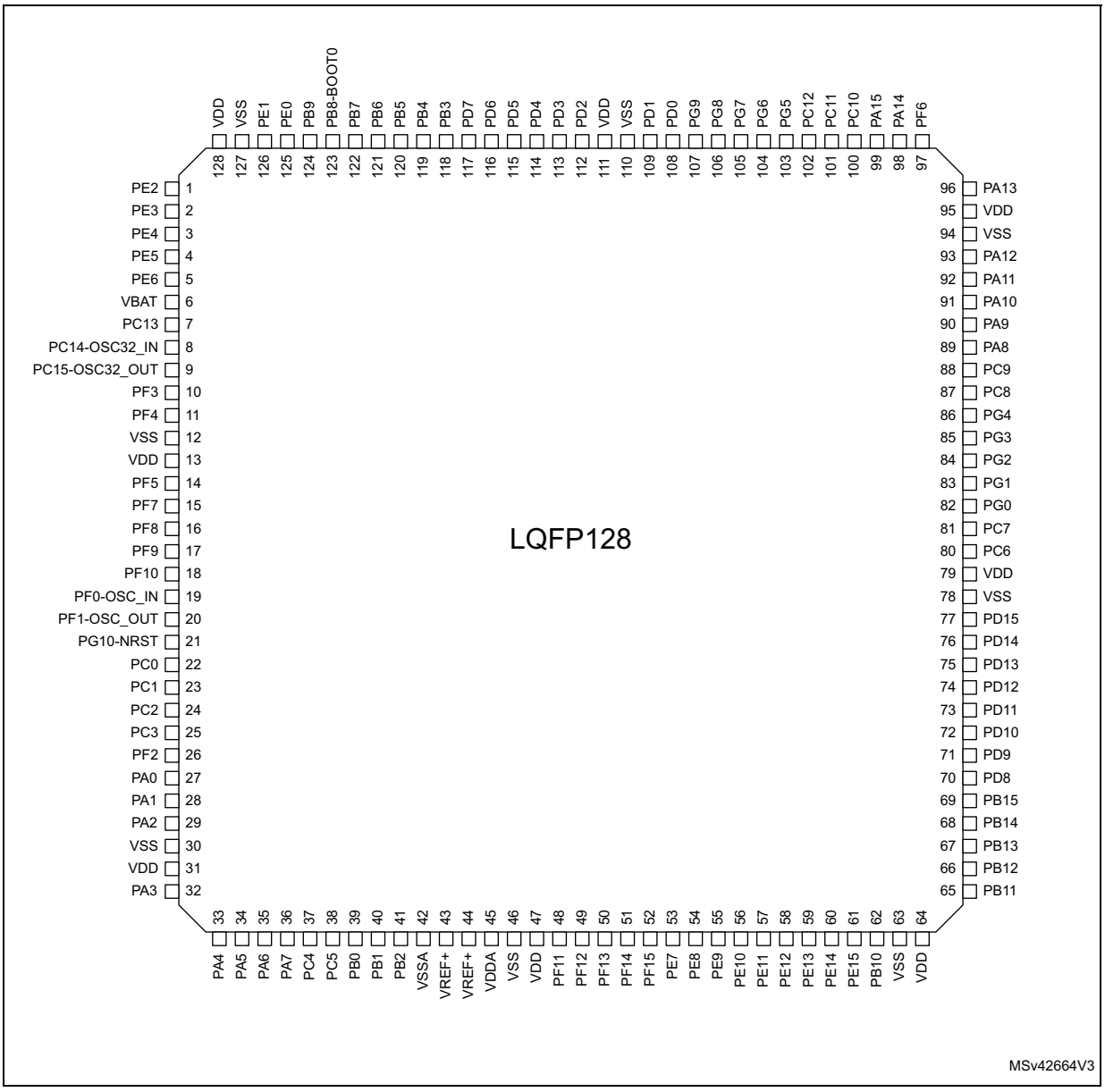
Figure 9. STM32G471xx LQFP100 pinout



1. The above figure shows the package top view.

4.6 LQFP128 pinout description

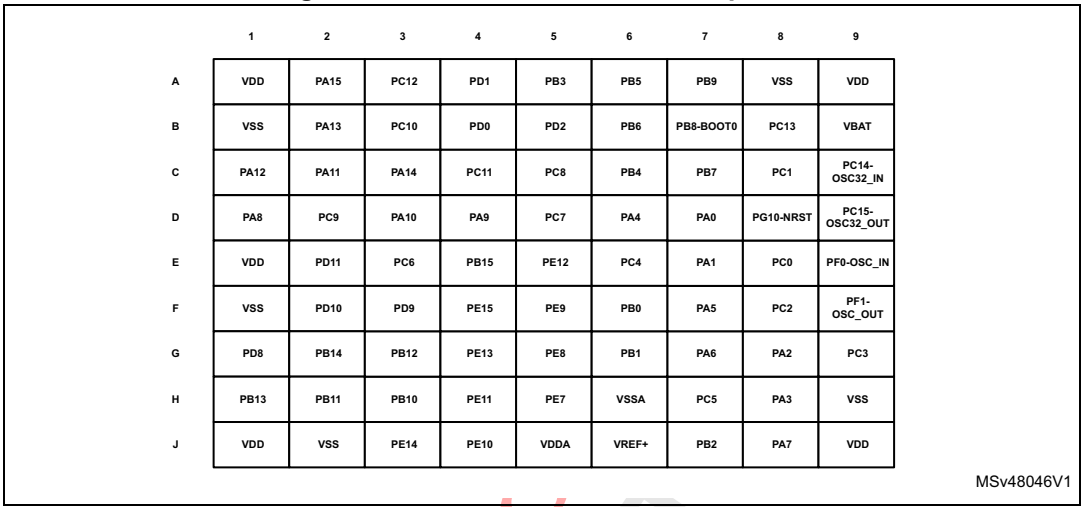
Figure 10. STM32G471xx LQFP128 pinout



1. The above figure shows the package top view.

4.7 WLCSP81 pinout description

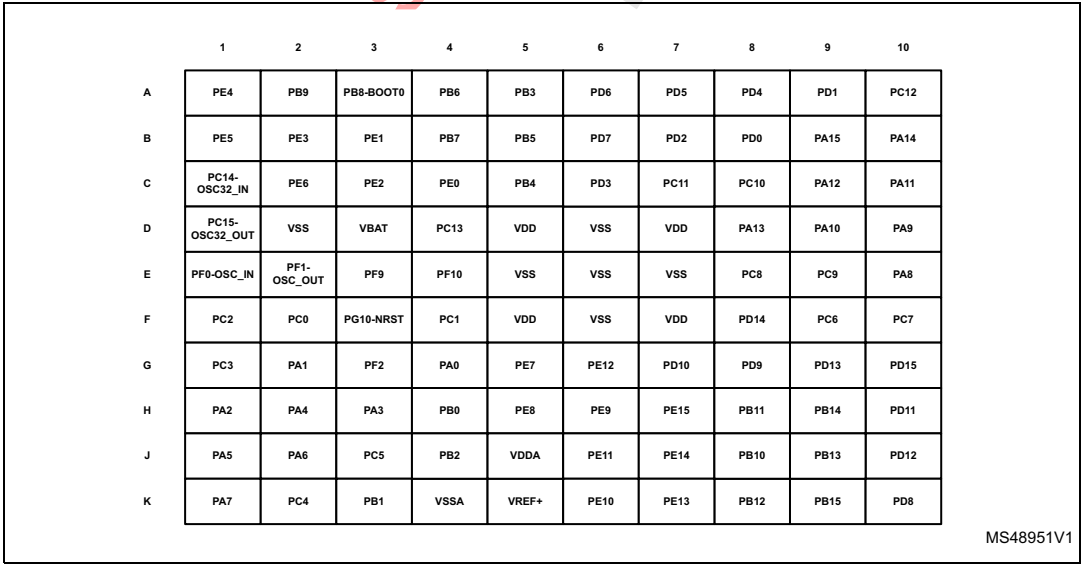
Figure 11. STM32G471xx WLCSP81 pinout



1. The above figure shows the package top view.

4.8 TFBGA100 pinout description

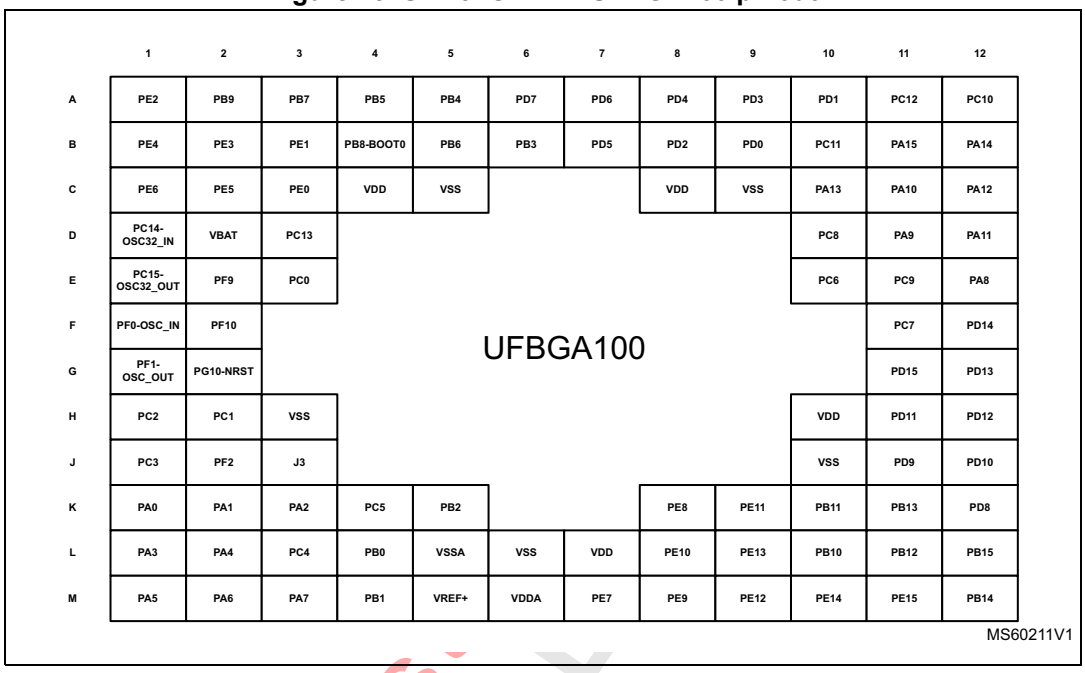
Figure 12. STM32G471xx TFBGA100 pinout



1. The above figure shows the package top view.

4.9 UFBGA100 pinout description

Figure 13. STM32G471xx UFBGA100 pinout



1. The above figure shows the package top view.

4.10 Pin definition

Table 10. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TT	3.6 V tolerant I/O
	B	Dedicated BOOT0 pin
	NRST	Bidirectional reset pin with embedded weak pull-up resistor
	Option for TT or FT I/Os	
	_a(1)	I/O, with Analog switch function supplied by V_{DDA}
	_c	I/O, USB Type-C PD capable
	_d	I/O, USB Type-C PD Dead Battery function
	_f(2)	I/O, Fm+ capable
	_u(3)	I/O, with USB function
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled through peripheral registers

1. The related I/O structures in *Table 11* are: FT_a, FT_fa, TT_a.
2. The related I/O structures in *Table 11* are: FT_f, FT_fa.
3. The related I/O structures in are FT_u.

Table 11. STM32G471xx pin definition

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LQFP80	LPQF100	LPQF128						
-	-	-	-	C3	-	1	1	PE2	I/O	FT	-	TRACECK, TIM3_CH1, SAI_CK1, SPI4_SCK, SAI_MCLK_A, EVENTOUT	-
-	-	-	-	B2	-	2	2	PE3	I/O	FT	-	TRACED0, TIM3_CH2, SPI4_NSS, SAI_SD_B, EVENTOUT	-
-	-	-	-	A1	-	3	3	PE4	I/O	FT	-	TRACED1, TIM3_CH3, SAI_D2, SPI4_NSS, SAI_FS_A, EVENTOUT	-
-	-	-	-	B1	-	4	4	PE5	I/O	FT	-	TRACED2, TIM3_CH4, SAI_CK2, SPI4_MISO, SAI_SCK_A, EVENTOUT	-
-	-	-	-	C2	-	5	5	PE6	I/O	FT	-	TRACED3, SAI_D1, SPI4_MOSI, SAI_SD_A, EVENTOUT	WKUP3, RTC_TAMP3
B9	1	1	1	D3	1	6	6	VBAT	S	-	-	-	-
B8	2	2	2	D4	2	7	7	PC13	I/O	FT	-	TIM1_BKIN, TIM1_CH1N, TIM8_CH4N, EVENTOUT	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT1
C9	3	3	3	C1	3	8	8	PC14-OSC32_IN	I/O	FT	-	EVENTOUT	OSC32_IN
D9	4	4	4	D1	4	9	9	PC15-OSC32_OUT	I/O	FT	-	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	-	10	PF3	I/O	FT_f	-	I2C3_SCL, EVENTOUT	-
-	-	-	-	-	-	-	11	PF4	I/O	FT_f	-	COMP1_OUT, I2C3_SDA, EVENTOUT	-
F1	-	-	-	-	-	-	12	VSS	S	-	-	-	-
A9	-	-	-	-	-	-	13	VDD	S	-	-	-	-
-	-	-	-	-	-	-	14	PF5	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	-	15	PF7	I/O	FT	-	TIM5_CH2, SAI_MCLK_B, EVENTOUT	-
-	-	-	-	-	-	-	16	PF8	I/O	FT	-	TIM5_CH3, SAI_SCK_B, EVENTOUT	-

Table 11. STM32G471xx pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LQFP80	LPQF100	LPQF128						
-	-	-	-	E3	-	10	17	PF9	I/O	FT	-	TIM15_CH1, SPI2_SCK, TIM5_CH4, SAI_FS_B, EVENTOUT	-
-	-	-	-	E4	-	11	18	PF10	I/O	FT	-	TIM15_CH2, SPI2_SCK, SAI_D3 EVENTOUT	-
E9	5	5	5	E1	5	12	19	PF0-OSC_IN	I	FT_fa	-	I2C2_SDA, SPI2_NSS/I2S2_WS, TIM1_CH3N, EVENTOUT	ADC1_IN10, OSC_IN
F9	6	6	6	E2	6	13	20	PF1-OSC_OUT	O	FT_a	-	SPI2_SCK/I2S2_CK, EVENTOUT	ADC2_IN10, COMP3_INM, OSC_OUT
D8	7	7	7	F3	7	14	21	PG10-NRST	I/O	FT	-	MCO, EVENTOUT	NRST
E8	-	-	8	F2	8	15	22	PC0	I/O	FT_a	-	LPTIM1_IN1, TIM1_CH1, LPUART1_RX, EVENTOUT	ADC12_IN6, COMP3_INM
C8	-	-	9	F4	9	16	23	PC1	I/O	TT_a	-	LPTIM1_OUT, TIM1_CH2, LPUART1_TX, SAI_SD_A, EVENTOUT	ADC12_IN7, COMP3_INP
F8	-	-	10	F1	10	17	24	PC2	I/O	FT_a	-	LPTIM1_IN2, TIM1_CH3, COMP3_OUT, EVENTOUT	ADC12_IN8
G9	-	-	11	G1	11	18	25	PC3	I/O	TT_a	-	LPTIM1_ETR, TIM1_CH4, SAI_D1, TIM1_BKIN2, SAI_SD_A, EVENTOUT	ADC12_IN9
-	-	-	-	G3	-	19	26	PF2	I/O	FT	-	I2C2_SMBA, EVENTOUT	-
D7	8	8	12	G4	12	20	27	PA0	I/O	TT_a	-	TIM2_CH1, TIM5_CH1, USART2_CTS, COMP1_OUT, TIM8_BKIN, TIM8_ETR, TIM2_ETR, EVENTOUT	ADC12_IN1, COMP1_INM, COMP3_INP, RTC_TAMP2,WKUP1

Table 11. STM32G471xx pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LQFP80	LPQF100	LPQF128						
E7	9	9	13	G2	13	21	28	PA1	I/O	TT_a	-	RTC_REFIN, TIM2_CH2, TIM5_CH2, USART2_RTS_DE, TIM15_CH1N, EVENTOUT	ADC12_IN2, COMP1_INP, OPAMP1_VINP, OPAMP3_VINP
G8	10	10	14	H1	14	22	29	PA2	I/O	FT_a	-	TIM2_CH3, TIM5_CH3, USART2_TX, COMP2_OUT, TIM15_CH1, LPUART1_TX, UCPD_FRSTX, EVENTOUT	ADC1_IN3, COMP2_INM, OPAMP1_VOUT, WKUP4/LSCO
H9	-	-	15	D2	15	23	30	VSS	S	-	-	-	-
J9	-	-	16	D5	16	24	31	VDD	S	-	-	-	-
H8	11	11	17	H3	17	25	32	PA3	I/O	TT_a	-	TIM2_CH4, TIM5_CH4, SAI_CK1, USART2_RX, TIM15_CH2, LPUART1_RX, SAI_MCLK_A, EVENTOUT	ADC1_IN4, COMP2_INP, OPAMP1_VINM/ OPAMP1_VINP
D6	12	12	18	H2	18	26	33	PA4	I/O	TT_a	-	TIM3_CH2, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, SAI_FS_B, EVENTOUT	ADC2_IN17, DAC1_OUT1, COMP1_INM
F7	13	13	19	J1	19	27	34	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, UCPD_FRSTX, EVENTOUT	ADC2_IN13, DAC1_OUT2, COMP2_INM, OPAMP2_VINM
G7	14	14	20	J2	20	28	35	PA6	I/O	TT_a	-	TIM16_CH1, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM1_BKIN, COMP1_OUT, LPUART1_CTS, EVENTOUT	ADC2_IN3, OPAMP2_VOUT

Table 11. STM32G471xx pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LQFP80	LPQF100	LPQF128						
J8	15	15	21	K1	21	29	36	PA7	I/O	TT_a	-	TIM17_CH1, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, TIM1_CH1N, COMP2_OUT, UCPD_FRSTX, EVENTOUT	ADC2_IN4, COMP2_INP, OPAMP1_VINP, OPAMP2_VINP
E6	16	-	22	K2	22	30	37	PC4	I/O	FT_fa	-	TIM1_ETR, I2C2_SCL, USART1_TX, EVENTOUT	ADC2_IN5
H7	-	-	23	J3	23	31	38	PC5	I/O	TT_a	-	TIM15_BKIN, SAI_D3, TIM1_CH4N, USART1_RX, EVENTOUT	ADC2_IN11, OPAMP1_VINM, OPAMP2_VINM, WKUP5
F6	17	16	24	H4	24	32	39	PB0	I/O	TT_a	-	TIM3_CH3, TIM8_CH2N, TIM1_CH2N, UCPD_FRSTX, EVENTOUT	ADC1_IN15, ADC3_IN12, COMP4_INP, OPAMP2_VINP, OPAMP3_VINP
G6	18	17	25	K3	25	33	40	PB1	I/O	TT_a	-	TIM3_CH4, TIM8_CH3N, TIM1_CH3N, COMP4_OUT, LPUART1_RTS_DE, EVENTOUT	ADC1_IN12, ADC3_IN1, COMP1_INP, OPAMP3_VOUT
J7	19	18	26	J4	26	34	41	PB2	I/O	TT_a	-	RTC_OUT2, LPTIM1_OUT, TIM5_CH1, I2C3_SMBA, EVENTOUT	ADC2_IN12, COMP4_INM, OPAMP3_VINM
H6	-	19	27	K4	27	35	42	VSSA	S	-	-	-	-
J6	20	20	28	K5	28	36	43	VREF+	S	-	-	-	VREFBUF_OUT
-	-	-	-	-	-	-	44	VREF+	S	-	-	-	VREFBUF_OUT
J5	21	21	29	J5	29	37	45	VDDA	S	-	-	-	-
H9	-	-	-		-	-	46	VSS	S	-	-	-	-
J1	-	-	-		-	-	47	VDD	S	-	-	-	-
-	-	-	-	-	-	-	48	PF11	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	-	49	PF12	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	-	50	PF13	I/O	FT	-	I2C4_SMBA, EVENTOUT	-

Table 11. STM32G471xx pin definition (continued)

Pin Number								Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LQFP80	LPQF100	LPQF128						
-	-	-	-	-	-	-	51	PF14	I/O	FT_f	-	I2C4_SCL, EVENTOUT	-
-	-	-	-	-	-	-	52	PF15	I/O	FT_f	-	I2C4_SDA, EVENTOUT	-
H5	-	-	-	G5	30	38	53	PE7	I/O	TT_a	-	TIM1_ETR, SAI_SD_B, EVENTOUT	ADC3_IN4, COMP4_INP
G5	-	-	-	H5	31	39	54	PE8	I/O	FT_a	-	TIM5_CH3, TIM1_CH1N, SAI_SCK_B, EVENTOUT	ADC3_IN6, COMP4_INM
F5	-	-	-	H6	32	40	55	PE9	I/O	FT_a	-	TIM5_CH4, TIM1_CH1, SAI_FS_B, EVENTOUT	-
J4	-	-	-	K6	33	41	56	PE10	I/O	FT_a	-	TIM1_CH2N, SAI_MCLK_B, EVENTOUT	ADC3_IN14
H4	-	-	-	J6	34	42	57	PE11	I/O	FT_a	-	TIM1_CH2, SPI4_NSS, EVENTOUT	ADC3_IN15
E5	-	-	-	G6	35	43	58	PE12	I/O	FT_a	-	TIM1_CH3N, SPI4_SCK, EVENTOUT	ADC3_IN16
G4	-	-	-	K7	36	44	59	PE13	I/O	FT_a	-	TIM1_CH3, SPI4_MISO, EVENTOUT	ADC3_IN3
J3	-	-	-	J7	37	45	60	PE14	I/O	FT_a	-	TIM1_CH4, SPI4_MOSI, TIM1_BKIN2, EVENTOUT	-
F4	-	-	-	H7	38	46	61	PE15	I/O	FT_a	-	TIM1_BKIN, TIM1_CH4N, USART3_RX, EVENTOUT	-
H3	22	22	30	J8	39	47	62	PB10	I/O	TT_a	-	TIM2_CH3, USART3_TX, LPUART1_RX, TIM1_BKIN, SAI_SCK_A, EVENTOUT	OPAMP3_VINM
J2	-	23	31	D6	40	48	63	VSS	S	-	-	-	-
J1	23	24	32	D7	41	49	64	VDD	S	-	-	-	-
H2	24	25	33	H8	42	50	65	PB11	I/O	TT_a	-	TIM2_CH4, USART3_RX, LPUART1_TX, EVENTOUT	ADC12_IN14

Table 11. STM32G471xx pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LQFP80	LPQF100	LPQF128						
G3	25	26	34	K8	43	51	66	PB12	I/O	TT_a	-	TIM5_ETR, I2C2_SMBA, SPI2_NSS/I2S2_WS, TIM1_BKIN, USART3_CK, LPUART1_RTS_DE, FDCAN2_RX, EVENTOUT	ADC1_IN11
H1	26	27	35	J9	44	52	67	PB13	I/O	TT_a	-	SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, LPUART1_CTS, FDCAN2_TX, EVENTOUT	ADC3_IN5. OPAMP3_VINP
G2	27	28	36	H9	45	53	68	PB14	I/O	TT_a	-	TIM15_CH1, SPI2_MISO, TIM1_CH2N, USART3_RTS_DE, COMP4_OUT, EVENTOUT	ADC1_IN5, OPAMP2_VINP
E4	28	29	37	K9	46	54	69	PB15	I/O	TT_a	-	RTC_REFIN, TIM15_CH2, TIM15_CH1N, COMP3_OUT, TIM1_CH3N, SPI2_MOSI/I2S2_SD, EVENTOUT	ADC2_IN15
G1	-	-	-	K10	47	55	70	PD8	I/O	TT_a	-	USART3_TX, EVENTOUT	-
F3	-	-	-	G8	48	56	71	PD9	I/O	TT_a	-	USART3_RX, FDCAN2_RXFD, EVENTOUT	-
F2	-	-	-	G7	49	57	72	PD10	I/O	FT_a	-	USART3_CK, FDCAN2_TXFD, EVENTOUT	ADC3_IN7
E2	-	-	-	H10	-	58	73	PD11	I/O	TT_a	-	TIM5_ETR, I2C4_SMBA, USART3_CTS, EVENTOUT	ADC3_IN8
-	-	-	-	J10	-	59	74	PD12	I/O	TT_a	-	TIM4_CH1, USART3_RTS_DE, EVENTOUT	ADC3_IN9

Table 11. STM32G471xx pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LQFP80	LPQF100	LPQF128						
-	-	-	-	G9	-	60	75	PD13	I/O	FT_a	-	TIM4_CH2, EVENTOUT	ADC3_IN10
-	-	-	-	F8	-	61	76	PD14	I/O	TT_a	-	TIM4_CH3, EVENTOUT	ADC3_IN11, OPAMP2_VINP
-	-	-	-	G10	-	62	77	PD15	I/O	FT_a	-	TIM4_CH4, SPI2_NSS, EVENTOUT	-
B1	-	-	-		50	63	78	VSS	S	-	-	-	-
E1	-	-	-		51	64	79	VDD	S	-	-	-	-
E3	29	-	38	F9	52	65	80	PC6	I/O	FT_f	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, I2C4_SCL, EVENTOUT	-
D5	-	-	39	F10	53	66	81	PC7	I/O	FT_f	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, I2C4_SDA, EVENTOUT	-
-	-	-	-	-	-	-	82	PG0	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	-	83	PG1	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	-	84	PG2	I/O	FT	-	SPI1_SCK, EVENTOUT	-
-	-	-	-	-	-	-	85	PG3	I/O	FT_f	-	I2C4_SCL, SPI1_MISO, EVENTOUT	-
-	-	-	-	-	-	-	86	PG4	I/O	FT_f	-	I2C4_SDA, SPI1_MOSI, EVENTOUT	-
C5	-	-	40	E8	54	67	87	PC8	I/O	FT_f	-	TIM3_CH3, TIM8_CH3, I2C3_SCL, EVENTOUT	-
D2	-	-	41	E9	55	68	88	PC9	I/O	FT_f	-	TIM3_CH4, RTIM1_CHE2, TIM8_CH4, I2SCKIN, TIM8_BKIN2, I2C3_SDA, EVENTOUT	-
D1	30	30	42	E10	56	69	89	PA8	I/O	FT_a	-	MCO, I2C3_SCL, I2C2_SDA, I2S2_MCK, TIM1_CH1, USART1_CK, TIM4_ETR, SAI_CK2, SAI_SCK_A, EVENTOUT	-

Table 11. STM32G471xx pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LQFP80	LPQF100	LPQF128						
D4	31	31	43	D10	57	70	90	PA9	I/O	FT_fd	-	I2C3_SMBA, I2C2_SCL, I2S3_MCK, TIM1_CH2, USART1_TX, OMP5_OUT, TIM15_BKIN, TIM2_CH3, FDCAN1_RXFD, SAI_FS_A, EVENTOUT	UCPD_DBCC1
D3	32	32	44	D9	58	71	91	PA10	I/O	FT_fd	-	TIM17_BKIN, USB_CRS_SYNC, I2C2_SMBA, SPI2_MISO, TIM1_CH3, USART1_RX, FDCAN1_TXFD, TIM2_CH4, TIM8_BKIN, SAI_D1, SAI_SD_A, EVENTOUT	UCPD_DBCC2
C2	33	33	45	C10	59	72	92	PA11	I/O	FT_u	-	SPI2_MOSI/I2S2_SD, TIM1_CH1N, USART1_CTS, COMP1_OUT, FDCAN1_RX, TIM4_CH1, TIM1_CH4, TIM1_BKIN2, EVENTOUT	USB_DM
C1	34	34	46	C9	60	73	93	PA12	I/O	FT_u	-	TIM16_CH1, I2SCKIN, TIM1_CH2N, USART1_RTS_DE, COMP2_OUT, FDCAN1_TX, TIM4_CH2, TIM1_ETR, EVENTOUT	USB_DP
A8	-	35	47	E6	61	74	94	VSS	S	-	-	-	-
A1	35	36	48	F7	62	75	95	VDD	S	-	-	-	-
B2	36	37	49	D8	63	76	96	PA13	I/O	FT_f	-	SWDIO-JTMS, TIM16_CH1N, I2C4_SCL, I2C1_SCL, IR_OUT, USART3_CTS, TIM4_CH3, SAI_SD_B, EVENTOUT	-

Table 11. STM32G471xx pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LQFP80	LPQF100	LPQF128						
-	-	-	-	-	-	-	97	PF6	I/O	FT_f	-	TIM5_ETR, TIM4_CH4, SAI_SD_B, I2C2_SCL, TIM5_CH1, USART3_RTS, EVENTOUT	-
C3	37	38	50	B10	64	77	98	PA14	I/O	FT_f	-	SWCLK-JTCK, LPTIM1_OUT, I2C4_SMBA, I2C1_SDA, TIM8_CH2, TIM1_BKIN, USART2_TX, SAI_FS_B, EVENTOUT	-
A2	38	39	51	B9	65	78	99	PA15	I/O	FT_f	-	JTDI, TIM2_CH1, TIM8_CH1, I2C1_SCL, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_RX, UART4_RTS_DE, TIM1_BKIN, TIM2_ETR, EVENTOUT	-
B3	39	-	52	C8	66	79	100	PC10	I/O	FT	-	TIM8_CH1N, UART4_TX, SPI3_SCK/I2S3_CK, USART3_TX, EVENTOUT	-
C4	40	-	53	C7	67	80	101	PC11	I/O	FT_f	-	TIM8_CH2N, UART4_RX, SPI3_MISO, USART3_RX, I2C3_SDA, EVENTOUT	-
A3	-	-	54	A10	68	81	102	PC12	I/O	FT	-	TIM5_CH2, TIM8_CH3N, UART5_TX, SPI3_MOSI/I2S3_SD, USART3_CK, UCPD_FRSTX, EVENTOUT	-
-	-	-	-	-	-	-	103	PG5	I/O	FT	-	SPI1_NSS, LPUART1_CTS, EVENTOUT	-
-	-	-	-	-	-	-	104	PG6	I/O	FT	-	I2C3_SMBA, LPUART1_RTS_DE, EVENTOUT	-

Table 11. STM32G471xx pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LQFP80	LPQF100	LPQF128						
-	-	-	-	-	-	-	105	PG7	I/O	FT_f	-	SAI_CK1, I2C3_SCL, LPUART1_TX, SAI_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	-	106	PG8	I/O	FT_f	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	-	-	-	-	-	107	PG9	I/O	FT	-	SPI3_SCK, USART1_TX, TIM15_CH1N, EVENTOUT	-
B4	-	-	-	B8	69	82	108	PD0	I/O	FT	-	TIM8_CH4N, FDCAN1_RX, EVENTOUT	-
A4	-	-	-	A9	70	83	109	PD1	I/O	FT	-	TIM8_CH4, TIM8_BKIN2, FDCAN1_TX, EVENTOUT	-
-	-	-	-	E7	-	-	110	VSS	S	-	-	-	-
A1	-	-	-	-	-	-	111	VDD	S	-	-	-	-
B5	-	-	55	B7	71	84	112	PD2	I/O	FT	-	TIM3_ETR, TIM8_BKIN, UART5_RX, EVENTOUT	-
-	-	-	-	C6	-	85	113	PD3	I/O	FT	-	TIM2_CH1/ TIM2_ETR, USART2_CTS, EVENTOUT	-
-	-	-	-	A8	-	86	114	PD4	I/O	FT	-	TIM2_CH2, USART2_RTS_DE, FDCAN1_RXFD, EVENTOUT	-
-	-	-	-	A7	-	87	115	PD5	I/O	FT	-	USART2_TX, FDCAN1_TXFD, EVENTOUT	-
-	-	-	-	A6	-	88	116	PD6	I/O	FT	-	TIM2_CH4, SAI_D1, USART2_RX, FDCAN2_RXFD, SAI_SD_A, EVENTOUT	-
-	-	-	-	B6	-	89	117	PD7	I/O	FT	-	TIM2_CH3, USART2_CK, EVENTOUT	-

Table 11. STM32G471xx pin definition (continued)

Pin Number								Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LQFP80	LPQF100	LPQF128						
A5	41	40	56	A5	72	90	118	PB3	I/O	FT	-	JTDO-TRACESWO, TIM2_CH2, TIM4_ETR, USB_CRS_SYNC, TIM8_CH1N, SPI1_SCK, SPI3_SCK/I2S3_CK, USART2_TX, TIM3_ETR, SAI_SCK_B, EVENTOUT	-
C6	42	41	57	C5	73	91	119	PB4	I/O	FT_c	-	JTRST, TIM16_CH1, TIM3_CH1, TIM8_CH2N, SPI1_MISO, SPI3_MISO, USART2_RX, UART5_RTS_DE, TIM17_BKIN, SAI_MCLK_B, EVENTOUT	UCPD_CC2
A6	43	42	58	B5	74	92	120	PB5	I/O	FT_f	-	TIM16_BKIN, TIM3_CH2, TIM8_CH3N, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI/I2S3_SD, USART2_CK, I2C3_SDA, FDCAN2_RX, TIM17_CH1, LPTIM1_IN1, SAI_SD_B, UART5_CTS, EVENTOUT	-
B6	44	43	59	A4	75	93	121	PB6	I/O	FT_c	-	TIM16_CH1N, TIM4_CH1, TIM8_CH1, TIM8_ETR, USART1_TX, COMP4_OUT, FDCAN2_TX, TIM8_BKIN2, LPTIM1_ETR, SAI_FS_B, EVENTOUT	UCPD_CC1

Table 11. STM32G471xx pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LQFP80	LPQF100	LPQF128						
C7	45	44	60	B4	76	94	122	PB7	I/O	FT_f	-	TIM17_CH1N, TIM4_CH2, I2C4_SDA, I2C1_SDA, TIM8_BKIN, USART1_RX, COMP3_OUT, FDCAN2_TXFD, TIM3_CH4, LPTIM1_IN2, UART4_CTS, EVENTOUT	PVD_IN
B7	46	45	61	A3	77	95	123	PB8-BOOT0	I/O	FT_f	-	TIM16_CH1, TIM4_CH3, SAI_CK1, I2C1_SCL, USART3_RX, COMP1_OUT, FDCAN1_RX, TIM8_CH2, TIM1_BKIN, SAI_MCLK_A, EVENTOUT	-
A7	47	46	62	A2	78	96	124	PB9	I/O	FT_f	-	TIM17_CH1, TIM4_CH4, SAI_D2, I2C1_SDA, IR_OUT, USART3_TX, COMP2_OUT, FDCAN1_TX, TIM8_CH3, TIM1_CH3N, SAI_FS_A, EVENTOUT	-
-	-	-	-	C4	-	97	125	PE0	I/O	FT	-	TIM4_ETR, TIM16_CH1, USART1_TX, FDCAN1_RXFD, EVENTOUT	-
-	-	-	-	B3	-	98	126	PE1	I/O	FT	-	TIM17_CH1, USART1_RX, FDCAN1_TXFD, EVENTOUT	-
-	-	47	63	F6	79	99	127	VSS	S	-	-	-	-
A9	48	48	64	-	80	100	128	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.

4.11 Alternate functions

Table 12. Alternate function

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/ 15/20/ GPCOMP1	I2C3/4/SAI/ USB/ TIM8/15/20/ GPCOMP3/ TSC	I2C1/2/3/ 4/ TIM1/8/1 6/17	SPI1/2/3/4/ I2S2/3/ I2C4/ UART4/5 /TIM8/ Infrared	SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3 /CAN	I2C3/4/ UART4/5/ LPUART1/ GPCOMP1/ 2/3/4	CAN/ TIM1/8/1 5/fdCAN 1/2	TIM2/3/4/8/1 7	LPTIM1/ TIM1/8/ FDCAN1/3	SDIO/ LPUART1/ SAI/ TIM1	SAI/ OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port A	PA0	-	TIM2_CH1	TIM5_CH1	-	-	-	-	USART2_ CTS	COMP1 _OUT	TIM8_ BKIN	TIM8_ETR	-	-	-	TIM2_ ETR	EVENT OUT
	PA1	RTC_ REFIN	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_ RTS_DE	-	TIM15_C H1N	-	-	-	-	-	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_ TX	COMP2 _OUT	TIM15_C H1	-	-	LPUART1_TX	-	UCPD_ FRSTX	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	SAI_CK1	-	-	-	USART2_ RX	-	TIM15_C H2	-	-	LPUART1_RX	SAI_MCLK_A	-	EVENT OUT
	PA4	-	-	TIM3_CH2	-	-	SPI1_NSS	SPI3_NSS/I2 S3_WS	USART2_ CK	-	-	-	-	-	SAI_FS_B	-	EVENT OUT
	PA5	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK	-	-	-	-	-	-	-	-	UCPD_ FRSTX	EVENT OUT
	PA6	-	TIM16_CH1	TIM3_CH1	-	TIM8_ BKIN	SPI1_MISO	TIM1_BKIN	-	COMP1 _OUT	-	-	-	LPUART1_ CTS	-	-	EVENT OUT
	PA7	-	TIM17_CH1	TIM3_CH2	-	TIM8_ CH1N	SPI1_MOSI	TIM1_CH1N	-	COMP2_ OUT	-	-	-	-	-	UCPD_ FRSTX	EVENT OUT
	PA8	MCO	-	-	-	I2C2_ SMBA	I2S2_MCK	TIM1_CH1	USART1_ CK	-	-	TIM4_ETR	-	SAI_CK2	-	SAI_SCK _A	EVENT OUT
	PA9	-	-	I2C3_SMBA	-	I2C2_ SCL	I2S3_MCK	TIM1_CH2	USART1_ TX	-	TIM15_B KIN	TIM2_CH3	FDCAN1_ RXFD	-	-	SAI_FS_ A	EVENT OUT
	PA10	-	TIM17_BKIN	I2C3_SCL	USB_CRS_ SYNC	I2C2_ SDA	SPI2_MISO	TIM1_CH3	USART1_ RX	-	CAN1_T XFD	TIM2_CH4	TIM8_ BKIN	SAI_D1	-	SAI_SD_ A	EVENT OUT
	PA11	-	-	-	-	-	SPI2_MOSI/I 2S2_SD	TIM1_CH1N	USART1_ CTS	COMP1 _OUT	CAN1_ RX	TIM4_CH1	TIM1_ CH4	TIM1_BKIN2	-	-	EVENT OUT
	PA12	-	TIM16_CH1	-	-	-	I2SCKIN	TIM1_CH2N	USART1_ RTS_DE	COMP2 _OUT	CAN1_ TX	TIM4_CH2	TIM1_ ETR	-	-	-	EVENT OUT
	PA13	SWDIO-JTMS	TIM16_CH1N	-	-	-	IR_OUT	-	USART3_ CTS	-	-	TIM4_CH3	-	-	SAI_SD_B	-	EVENT OUT
	PA14	SWCLK-JTCK	LPTIM1_OUT	-	I2C4_SMBA	I2C1_ SDA	TIM8_CH2	TIM1_ BKIN	USART2_ TX	-	-	-	-	-	SAI_FS_B	-	EVENT OUT
	PA15	JTDI	TIM2_CH1	TIM8_CH1	-	I2C1_ SCL	SPI1_NSS	SPI3_NSS/I2 S3_WS	USART2_ RX	UART4 _RTS_DE	TIM1_ BKIN	-	-	-		TIM2_ ETR	EVENT OUT

Table 12. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/ 15/20/ GPCOMP1	I2C3/4/SAI/ USB/ TIM8/15/20/ GPCOMP3/ TSC	I2C1/2/3/ 4/ TIM1/8/1 6/17	SPI1/2/3/4/ I2S2/3/ I2C4/ UART4/5 /TIM8/ Infrared	SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3 /CAN	I2C3/4/ UART4/5/ LPUART1/ GPCOMP1/ 2/3/4	CAN/ TIM1/8/1 5/fdCAN 1/2	TIM2/3/4/8/1 7	LPTIM1/ TIM1/8/ FDCAN1/3	SDIO/ LPUART1/ SAI/ TIM1	SAI/ OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port B	PB0	-	-	TIM3_CH3	-	TIM8_ CH2N	-	TIM1_CH2N	-	-	-	-	-	-	-	UCPD_ FRSTX	EVENT OUT
	PB1	-	-	TIM3_CH4	-	TIM8_ CH3N	-	TIM1_CH3N	-	COMP4_ OUT	-	-	-	LPUART1_RTS _DE	-	-	EVENT OUT
	PB2	-	LPTIM1_OUT	TIM5_CH1	-	I2C3_ SMBA	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PB3	JTDO-TRACESWO	TIM2_CH2	TIM4_ETR	USB_CRS_ SYNC	TIM8_ CH1N	SPI1_SCK	SPI3_SCK/I2 S3_CK	USART2_ TX	-	-	TIM3_ETR	-	-	-	SAI_SCK _B	EVENT OUT
	PB4	JTRST	TIM16_CH1	TIM3_CH1	-	TIM8_ CH2N	SPI1_MISO	SPI3_MISO	USART2_ RX	UART5_ RTS_DE	-	TIM17_BKIN	-	-	-	SAI_MCL K_B	EVENT OUT
	PB5	-	TIM16_BKIN	TIM3_CH2	TIM8_CH3N	I2C1_ SMBA	SPI1_MOSI	SPI3_MOSI/I 2S3_SD	USART2_ CK	I2C3_SDA	FDCAN2 _RX	TIM17_CH1	LPTIM1 _IN1	SAI_SD_B	-	UART5_ CTS	EVENT OUT
	PB6	-	TIM16_CH1N	TIM4_CH1	I2C4_SCL	I2C1_ SCL	TIM8_CH1	TIM8_ETR	USART1_ TX	COMP4_ OUT	FDCAN2 _TX	TIM8_BKIN2	LPTIM1 _ETR	-	-	SAI_FS_ B	EVENT OUT
	PB7	-	TIM17_CH1N	TIM4_CH2	I2C4_SDA	I2C1_ SDA	TIM8_BKIN	-	USART1_ RX	COMP3_ OUT	FDCAN2 _TXFD	TIM3_CH4	LPTIM1 _IN2	-	-	UART4_ CTS	EVENT OUT
	PB8	-	TIM16_CH1	TIM4_CH3	SAI_CK1	I2C1_ SCL	-	-	USART3_ RX	COMP1_ OUT	FDCAN1 _RX	TIM8_CH2	-	TIM1_BKIN	-	SAI_MCL K_A	EVENT OUT
	PB9	-	TIM17_CH1	TIM4_CH4	SAI_D2	I2C1_ SDA	-	IR_OUT	USART3_TX	COMP2_ OUT	FDCAN1 _TX	TIM8_CH3	-	TIM1_CH3N	-	SAI_FS_ A	EVENT OUT
	PB10	-	TIM2_CH3	-	-	-	-	-	USART3_ TX	LPUART1_ RX	-		-	TIM1_BKIN	-	SAI_SCK _A	EVENT OUT
	PB11	-	TIM2_CH4	-	-	-	-	-	USART3_ RX	LPUART1_ TX	-		-	-	-	-	EVENT OUT
	PB12	-	-	TIM5_ETR	-	I2C2_ SMBA	SPI2_NSS/I2 S2_WS	TIM1_BKIN	USART3_ CK	LPUART1_ RTS_DE	FDCAN2 _RX	-	-	-	-	-	EVENT OUT
	PB13	-	-	-	-	-	SPI2_SCK/I2 S2_CK	TIM1_CH1N	USART3_ CTS	LPUART1_ CTS	FDCAN2 _TX	-	-	-	-	-	EVENT OUT
	PB14	-	TIM15_CH1	-	-	-	SPI2_MISO	TIM1_CH2N	USART3_ RTS_DE	COMP4_ OUT	-	-	-	-	-	-	EVENT OUT
	PB15	RTC_REFIN	TIM15_CH2	TIM15_CH1N	COMP3_OUT	TIM1_ CH3N	SPI2_MOSI/I 2S2_SD	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 12. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/ 15/20/ GPCOMP1	I2C3/4/SAI/ USB/ TIM8/15/20/ GPCOMP3/ TSC	I2C1/2/3/ 4/ TIM1/8/1 6/17	SPI1/2/3/4/ I2S2/3/ I2C4/ UART4/5 /TIM8/ Infrared	SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3 /CAN	I2C3/4/ UART4/5/ LPUART1/ GPCOMP1/ 2/3/4	CAN/ TIM1/8/1 5/fdCAN 1/2	TIM2/3/4/8/1 7	LPTIM1/ TIM1/8/ FDCAN1/3	SDIO/ LPUART1/ SAI/ TIM1	SAI/ OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port C	PC0	-	LPTIM1_IN1	TIM1_CH1	-	-	-	-	-	LPUART1_ RX	-	-	-	-	-	-	EVENT OUT
	PC1	-	LPTIM1_OUT	TIM1_CH2	-	-	-	-	-	LPUART1_ TX	-	-	-	-	SAI_SD_A	-	EVENT OUT
	PC2	-	LPTIM1_IN2	TIM1_CH3	COMP3_OUT	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC3	-	LPTIM1_ETR	TIM1_CH4	SAI_D1	-	-	TIM1_BKIN2	-	-	-	-	-	-	SAI_SD_A	-	EVENT OUT
	PC4	-	-	TIM1_ETR	-	I2C2_ SCL	-	-	USART1_ TX	-	-	-	-	-	-	-	EVENT OUT
	PC5	-	-	TIM15_BKIN	SAI_D3	-	-	TIM1_CH4N	USART1_ RX	-	-	-	-	-	-	-	EVENT OUT
	PC6	-	-	TIM3_CH1	-	TIM8_ CH1	-	I2S2_MCK	-	I2C4_SCL	-	-	-	-	-	-	EVENT OUT
	PC7	-	-	TIM3_CH2	-	TIM8_ CH2	-	I2S3_MCK	-	I2C4_SDA	-	-	-	-	-	-	EVENT OUT
	PC8	-	-	TIM3_CH3	-	TIM8_ CH3	-	-	-	I2C3_SCL	-	-	-	-	-	-	EVENT OUT
	PC9	-	-	TIM3_CH4	-	TIM8_ CH4	I2SCKIN	TIM8_ BKIN2	-	I2C3_SDA	-	-	-	-	-	-	EVENT OUT
	PC10	-	-	-	-	TIM8_ CH1N	UART4_TX	SPI3_SCK/I2 S3_CK	USART3_ TX	-	-	-	-	-	-	-	EVENT OUT
	PC11	-	-	-	-	TIM8_ CH2N	UART4_RX	SPI3_MISO	USART3_ RX	I2C3_SDA	-	-	-	-	-	-	EVENT OUT
	PC12	-	TIM5_CH2	-	-	TIM8_C H3N	UART5_TX	SPI3_MOSI/I 2S3_SD	USART3_ CK	-	-	-	-	-	-	UCPD_ FRSTX	EVENT OUT
	PC13	-	-	TIM1_BKIN	-	TIM1_ CH1N	-	TIM8_CH4N	-	-	-	-	-	-	-	-	EVENT OUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 12. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/ 15/20/ GPCOMP1	I2C3/4/SAI/ USB/ TIM8/15/20/ GPCOMP3/ TSC	I2C1/2/3/ 4/ TIM1/8/1 6/17	SPI1/2/3/4/ I2S2/3/ I2C4/ UART4/5 /TIM8/ Infrared	SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3 /CAN	I2C3/4/ UART4/5/ LPUART1/ GPCOMP1/ 2/3/4	CAN/ TIM1/8/1 5/fdCAN 1/2	TIM2/3/4/8/1 7	LPTIM1/ TIM1/8/ FDCAN1/3	SDIO/ LPUART1/ SAI/ TIM1	SAI/ OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port D	PD0	-	-	-	-	-	-	TIM8_CH4N	-	-	FDCAN1 _RX	-	-	-	-	-	EVENT OUT
	PD1	-	-	-	-	TIM8_ CH4	-	TIM8_BKIN2	-	-	FDCAN1 _TX	-	-	-	-	-	EVENT OUT
	PD2	-	-	TIM3_ETR	-	TIM8_ BKIN	UART5_RX	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD3	-	-	TIM2_CH1/TIM2 _ETR	-	-	-	-	USART2_CT S	-	-	-	-	-	-	-	EVENT OUT
	PD4	-	-	TIM2_CH2	-	-	-	-	USART2_RT S_DE	-	FDCAN1 _RXFD	-	-	-	-	-	EVENT OUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	FDCAN1 _TXFD	-	-	-	-	-	EVENT OUT
	PD6	-	-	TIM2_CH4	SAI_D1	-	-	-	USART2_ RX	-	FDCAN2 _RXFD	-	-	-	SAI_SD_A	-	EVENT OUT
	PD7	-	-	TIM2_CH3	-	-	-	-	USART2_ CK	-	-	-	-	-	-	-	EVENT OUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	-	-	-	EVENT OUT
	PD9	-	-	-	-	-	-	-	USART3_ RX	-	FDCAN2 _RXFD	-	-	-	-	-	EVENT OUT
	PD10	-	-	-	-	-	-	-	USART3_ CK	-	FDCAN2 _TXFD	-	-	-	-	-	EVENT OUT
	PD11	-	TIM5_ETR	-	-	I2C4_ SMBA	-	-	USART3_ CTS	-	-	-	-	-	-	-	EVENT OUT
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_ RTS_DE	-	-	-	-	-	-	-	EVENT OUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD15	-	-	TIM4_CH4	-	-	-	SPI2_NSS	-	-	-	-	-	-	-	-	EVENT OUT

Table 12. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/ 15/20/ GPCOMP1	I2C3/4/SAI/ USB/ TIM8/15/20/ GPCOMP3/ TSC	I2C1/2/3/ 4/ TIM1/8/1 6/17	SPI1/2/3/4/ I2S2/3/ I2C4/ UART4/5 /TIM8/ Infrared	SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3 /CAN	I2C3/4/ UART4/5/ LPUART1/ GPCOMP1/ 2/3/4	CAN/ TIM1/8/1 5/fdCAN 1/2	TIM2/3/4/8/1 7	LPTIM1/ TIM1/8/ FDCAN1/3	SDIO/ LPUART1/ SAI/ TIM1	SAI/ OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port E	PE0	-	-	TIM4_ETR	-	TIM16_ CH1	-	-	USART1_ TX	-	CAN1_R XFD	-	-	-	-	-	EVENT OUT
	PE1	-	-	-	-	TIM17_ CH1	-	-	USART1_ RX	-	CAN1_T XFD	-	-	-	-	-	EVENT OUT
	PE2	TRACECK	-	TIM3_CH1	SAI_CK1	-	SPI4_SCK	-	-	-	-	-	-	-	SAI_MCLK_A	-	EVENT OUT
	PE3	TRACED0	-	TIM3_CH2	-	-	SPI4_NSS	-	-	-	-	-	-	-	SAI_SD_B	-	EVENT OUT
	PE4	TRACED1	-	TIM3_CH3	SAI_D2	-	SPI4_NSS	-	-	-	-	-	-	-	SAI_FS_A	-	EVENT OUT
	PE5	TRACED2	-	TIM3_CH4	SAI_CK2	-	SPI4_MISO	-	-	-	-	-	-	-	SAI_SCK_A	-	EVENT OUT
	PE6	TRACED3	-	-	SAI_D1	-	SPI4_MOSI	-	-	-	-	-	-	-	SAI_SD_A	-	EVENT OUT
	PE7	-	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	-	SAI_SD_B	-	EVENT OUT
	PE8	-	TIM5_CH3	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	SAI_SCK_B	-	EVENT OUT
	PE9	-	TIM5_CH4	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	SAI_FS_B	-	EVENT OUT
	PE10	-	-	TIM1_CH2N	-	-	-	-	-	-	-	-	-	-	SAI_MCLK_B	-	EVENT OUT
	PE11	-	-	TIM1_CH2	-	-	SPI4_NSS	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE12	-	-	TIM1_CH3N	-	-	SPI4_SCK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE13	-	-	TIM1_CH3	-	-	SPI4_MISO	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE14	-	-	TIM1_CH4	-	-	SPI4_MOSI	TIM1_ BKIN2	-	-	-	-	-	-	-	-	EVENT OUT
	PE15	-	-	TIM1_BKIN	-	-	-	TIM1_ CH4N	USART3_ RX	-	-	-	-	-	-	-	EVENT OUT

Table 12. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/ 15/20/ GPCOMP1	I2C3/4/SAI/ USB/ TIM8/15/20/ GPCOMP3/ TSC	I2C1/2/3/ 4/ TIM1/8/1 6/17	SPI1/2/3/4/ I2S2/3/ I2C4/ UART4/5 /TIM8/ Infrared	SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3 /CAN	I2C3/4/ UART4/5/ LPUART1/ GPCOMP1/ 2/3/4	CAN/ TIM1/8/1 5/fdCAN 1/2	TIM2/3/4/8/1 7	LPTIM1/ TIM1/8/ FDCAN1/3	SDIO/ LPUART1/ SAI/ TIM1	SAI/ OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port F	PF0	-	-	-	-	I2C2_ SDA	SPI2_NSS/I2 S2_WS	TIM1_CH3N	-	-	-	-	-	-	-	-	EVENT OUT
	PF1	-	-	-	-	-	SPI2_SCK/I2 S2_CK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF2	-	-	-	-	I2C2_ SMBA	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF3	-	-	-	-	I2C3_ SCL	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF4	-	-	COMP1_OUT	-	I2C3_ SDA	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF6	-	TIM5_ETR	TIM4_CH4	SAI_SD_B	I2C2_ SCL	-	TIM5_CH1	USART3_ RTS	-	-	-	-	-	-	-	EVENT OUT
	PF7	-	-	-	-	-	-	TIM5_CH2	-	-	-	-	-	-	SAI_MCLK_B	-	EVENT OUT
	PF8	-	-	-	-	-	-	TIM5_CH3	-	-	-	-	-	-	SAI_SCK_B	-	EVENT OUT
	PF9	-	-	-	TIM15_CH1	-	SPI2_SCK	TIM5_CH4	-	-	-	-	-	-	SAI_FS_B	-	EVENT OUT
	PF10	-	-	-	TIM15_CH2	-	SPI2_SCK	-	-	-	-	-	-	-	SAI_D3	-	EVENT OUT
	PF11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF13	-	-	-	-	I2C4_ SMBA	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF14	-	-	-	-	I2C4_ SCL	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF15	-	-	-	-	I2C4_ SDA	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 12. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/ 15/20/ GPCOMP1	I2C3/4/SAI/ USB/ TIM8/15/20/ GPCOMP3/ TSC	I2C1/2/3/ 4/ TIM1/8/1 6/17	SPI1/2/3/4/ I2S2/3/ I2C4/ UART4/5 /TIM8/ Infrared	SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3 /CAN	I2C3/4/ UART4/5/ LPUART1/ GPCOMP1/ 2/3/4	CAN/ TIM1/8/1 5/fdCAN 1/2	TIM2/3/4/8/1 7	LPTIM1/ TIM1/8/ FDCAN1/3	SDIO/ LPUART1/ SAI/ TIM1	SAI/ OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PG2	-	-	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PG3	-	-	-	-	I2C4_ SCL	SPI1_MISO	-	-	-	-	-	-	-	-	-	EVENT OUT
	PG4	-	-	-	-	I2C4_ SDA	SPI1_MOSI	-	-	-	-	-	-	-	-	-	EVENT OUT
	PG5	-	-	-	-	-	SPI1_NSS	-	-	LPUART1_ CTS	-	-	-	-	-	-	EVENT OUT
	PG6	-	-	-	-	I2C3_ SMBA	-	-	-	LPUART1_ RTS_DE	-	-	-	-	-	-	EVENT OUT
	PG7	-	-	-	SAI_CK1	I2C3_ SCL	-	-	-	LPUART1_ TX	-	-	-	-	SAI_MCLK_A	-	EVENT OUT
	PG8	-	-	-	-	I2C3_ SDA	-	-	-	LPUART1_ RX	-	-	-	-	-	-	EVENT OUT
	PG9	-	-	-	-	-	-	SPI3_SCK	USART1_TX	-	-	-	-	-	-	TIM15_C H1N	EVENT OUT
	PG10	MCO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 14*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 15*.

Figure 14. Pin loading conditions

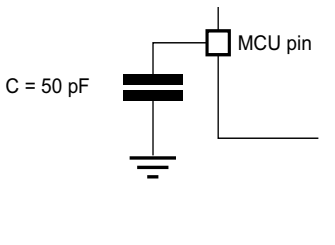
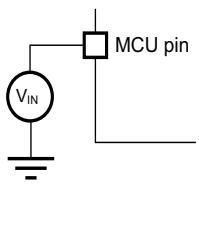
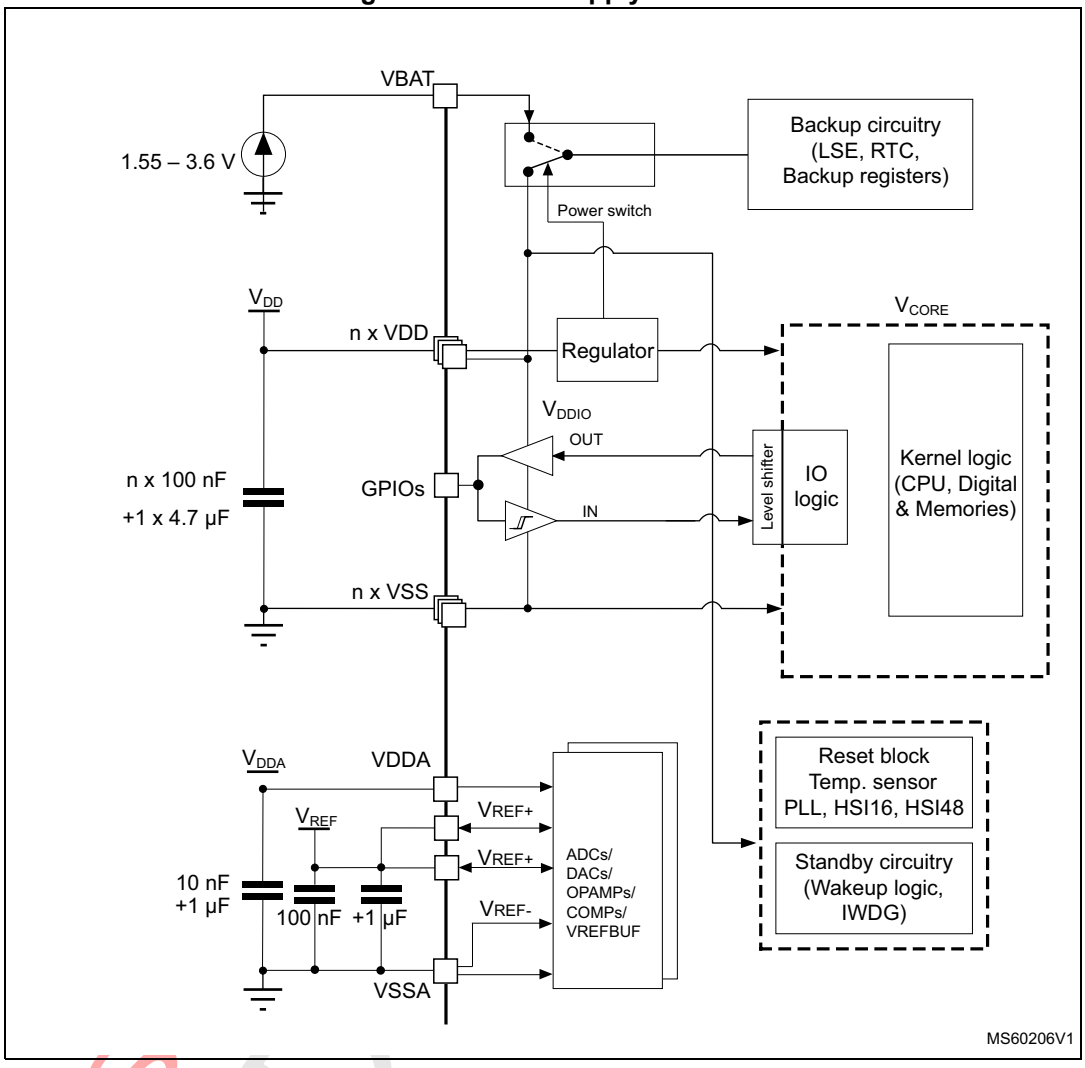


Figure 15. Pin input voltage



5.1.6 Power supply scheme

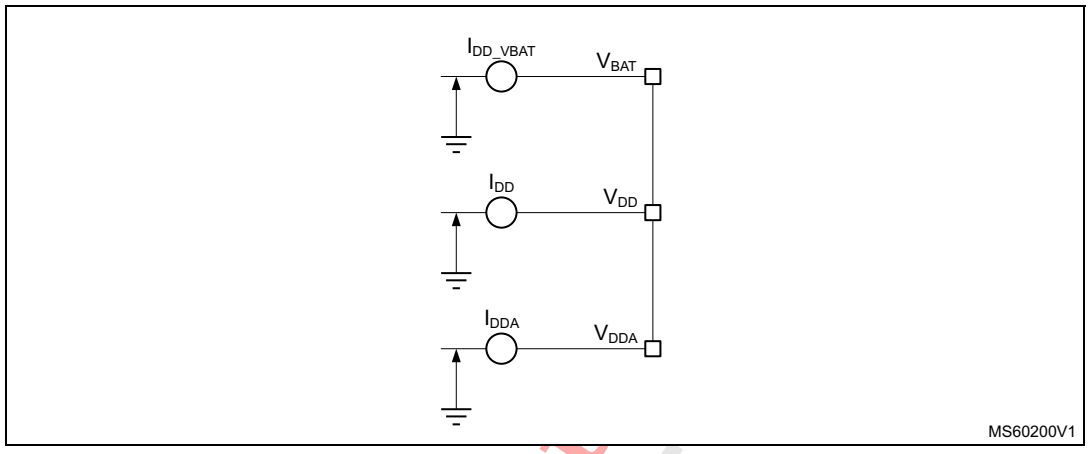
Figure 16. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

5.1.7 Current consumption measurement

Figure 17. Current consumption measurement



The I_{DD_ALL} parameters given in *Table 20* to *Table 27* represent the total MCU consumption including the current supplying V_{DD}, V_{DDA} and V_{BAT}.

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics* and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 13. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA} and V_{BAT})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins except FT_c pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}) + 4.0(3)(4)	
	Input voltage on FT_c pins	V_{SS}-0.3	5.0	
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins(5)	-	50	

1. All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 14: Current characteristics* for the maximum allowed injected current values.

3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 14. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1)	150	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	150	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xxx, TT_xx, NRST pins	-5/0(4)	
$\sum\|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection (when $V_{IN} > V_{DD}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by VIN < VSS. IINJ(PIN) must never be exceeded. Refer also to *Table 13: Voltage characteristics* for the minimum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 15. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-		0	170	MHz
f_{PCLK1}	Internal APB1 clock frequency	-		0	170	
f_{PCLK2}	Internal APB2 clock frequency	-		0	170	
V_{DD}	Standard operating voltage	-		1.71(1)	3.6	V
V_{DDA}	Analog supply voltage	ADC		1.62	3.6	V
		DAC 1 MSPS or OPAMP used		1.8		
		DAC 15MSPS or COMP used		TBD	3.6	
		VREFBUF used		2.4	3.6	
		ADC, DAC, OPAMP, COMP, VREFBUF not used		0		
V_{BAT}	Backup operating voltage	-		1.55	3.6	V
V_{IN}	I/O input voltage	TT_xx		-0.3	V_{DD}+0.3	V
		FT_c		-0.3	5	
		All I/O except TT_xx and FT_c		-0.3	MIN(MIN(V_{DD}, V_{DDA})+3.6 V, 5.5 V)(2)(3)	
P_D	Power dissipation at T_A = 80 °C for suffix 3(4)	LQFP128	-	-	TBD	mW
		LQFP100	-	-	TBD	
		LQFP80	-	-	TBD	
		LQFP64	-	-	TBD	
		LQFP48	-	-	TBD	
		UFQFPN48	-	-	TBD	
		UFBGA100	-	-	TBD	
		TFBGA100	-	-	TBD	
		WLCSP81	-	-	TBD	

Table 16. General operating conditions (continued)

Symbol	Parameter	Conditions		Min	Max	Unit
P_D	Power dissipation at T_A = 125 °C for suffix 3(4)	LQFP128	-	-	TBD	mW
		LQFP100	-	-	TBD	
		LQFP80	-	-	TBD	
		LQFP64	-	-	TBD	
		LQFP48	-	-	TBD	
		UFQFPN48	-	-	TBD	
		UFBGA100	-	-	TBD	
		TFBGA100	-	-	TBD	
		WLCSP81	-	-	TBD	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation		-40	85	°C
		Low-power dissipation(5)		-40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation		-40	125	
		Low-power dissipation(5)		-40	130	
T_J	Junction temperature range	Suffix 6 version		-40	105	°C
		Suffix 3 version		-40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB})+3.6 V and 5.5V.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If T_A is lower, higher PD values are allowed as long as TJ does not exceed T_{Jmax} (see *Section 6.10: Thermal characteristics*).
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 6.10: Thermal characteristics*).

5.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 17* are derived from tests performed under the ambient temperature condition summarized in *Table 16*.

Table 17. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	µs/V
	V_{DDA} fall time rate		10	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 18* are derived from tests performed under the ambient temperature conditions summarized in *Table 16: General operating conditions*.

Table 18. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	TBD	TBD	TBD	µs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVD1}	PVD threshold 1	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVD2}	PVD threshold 2	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVD3}	PVD threshold 3	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	

Table 18. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVD4}	PVD threshold 4	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVD5}	PVD threshold 5	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVD6}	PVD threshold 6	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	TBD	TBD	TBD	mV
		Hysteresis in other mode	TBD	TBD	TBD	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	TBD	TBD	TBD	mV
I_{DD} (BOR_PVD)[2]	BOR[3] (except BOR0) and PVD consumption from V_{DD}	-	TBD	TBD	TBD	µA
V_{PVM1}	V_{DDUSB} peripheral voltage monitoring	-	TBD	TBD	TBD	V
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{hyst_PVM3}	PVM3 hysteresis	-	TBD	TBD	TBD	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	TBD	TBD	TBD	mV
I_{DD} (PVM1/PVM2) (2)	PVM1 and PVM2 consumption from V_{DD}	-	TBD	TBD	TBD	µA
I_{DD} (PVM3/PVM4) (2)	PVM3 and PVM4 consumption from V_{DD}	-	TBD	TBD	TBD	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

5.3.4 Embedded voltage reference

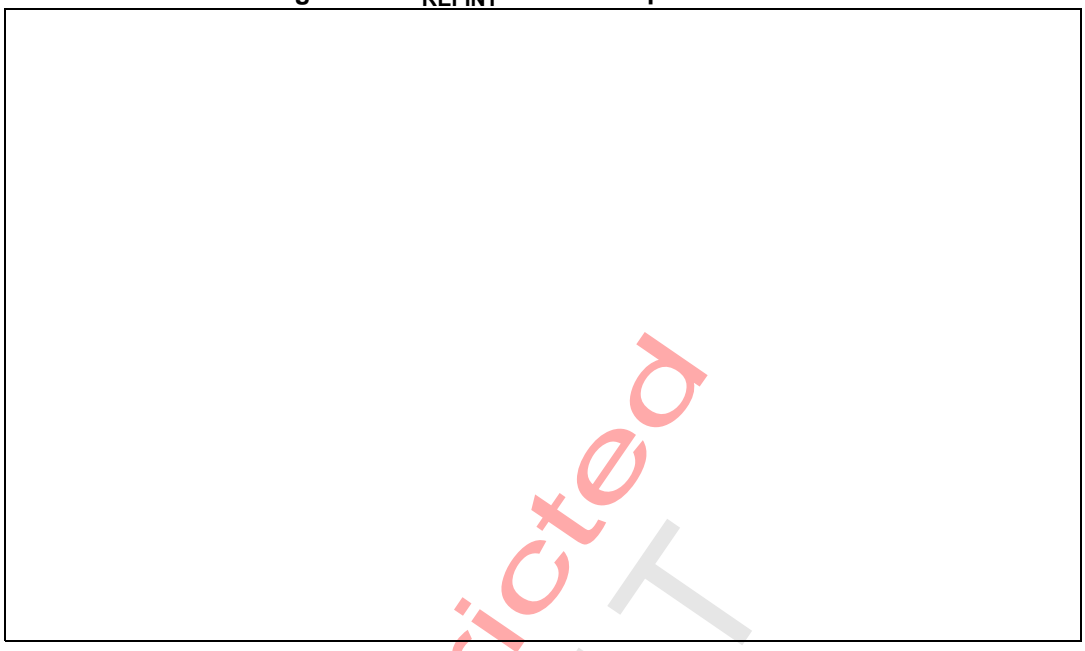
The parameters given in *Table 19* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 16: General operating conditions*.

Table 19. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	TBD	TBD	TBD	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	TBD (2)	TBD	TBD	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	TBD	TBD	TBD(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	TBD	TBD	TBD(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	TBD	TBD	TBD(2)	mV
T_{Coeff}	Average temperature coefficient	–40°C < T_A < +130°C	TBD	TBD	TBD(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	TBD	TBD	TBD(2)	ppm
$V_{DDCoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	TBD	TBD	TBD(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	TBD	TBD	TBD	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		TBD	TBD	TBD	
V_{REFINT_DIV3}	3/4 reference voltage		TBD	TBD	TBD	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Figure 18. V_{REFINT} versus temperature TBD



5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code

The current consumption is measured as described in *Figure 17: Current consumption measurement*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0440 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- The voltage scaling Range 1 is adjusted to f_{HCLK} frequency as follows:
  - Voltage Range 1 Boost mode for 150 MHz < $f_{HCLK} \leq$ 170 MHz
  - Voltage Range 1 Normal mode for 26 MHz < $f_{HCLK} \leq$ 150 MHz

The parameters given in *Table 20* to *Table 27* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 16: General operating conditions*.

Table 20. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ART enable (Cache ON Prefetch OFF

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.80	3.95	4.4	5.1	6.35	TBD	TBD	TBD	TBD	TBD	mA
				16 MHz	2.40	2.55	3	3.7	4.95	TBD	TBD	TBD	TBD	TBD	
				8 MHz	1.30	1.45	1.9	2.55	3.8	TBD	TBD	TBD	TBD	TBD	
				4 MHz	0.74	0.88	1.3	1.95	3.2	TBD	TBD	TBD	TBD	TBD	
				2 MHz	0.45	0.59	1	1.65	2.9	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.31	0.44	0.87	1.55	2.75	TBD	TBD	TBD	TBD	TBD	
				100 KHz	0.18	0.31	0.74	1.4	2.6	TBD	TBD	TBD	TBD	TBD	
			Range 1 Boost mode	170 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1	150 MHz	24.50	25	25.5	26.5	28	TBD	TBD	TBD	TBD	TBD	
				120 MHz	19.50	20	20.5	21.5	23	TBD	TBD	TBD	TBD	TBD	
				80 MHz	13.50	13.5	14	15	16.5	TBD	TBD	TBD	TBD	TBD	
				72 MHz	12.00	12	13	13.5	15	TBD	TBD	TBD	TBD	TBD	
				64 MHz	10.50	11	11.5	12.5	14	TBD	TBD	TBD	TBD	TBD	
				48 MHz	8.25	8.5	9.1	10	11.5	TBD	TBD	TBD	TBD	TBD	
				32 MHz	5.55	5.75	6.35	7.15	8.7	TBD	TBD	TBD	TBD	TBD	
				24 MHz	4.20	4.4	5	5.8	7.3	TBD	TBD	TBD	TBD	TBD	
				16 MHz	2.90	3.1	3.65	4.45	5.95	TBD	TBD	TBD	TBD	TBD	

Table 20. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ART enable (Cache ON Prefetch OFF (continued)

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPRun)	Supply current in Low-power run mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	395	575	1050	1800	3200	TBD	TBD	TBD	TBD	TBD	µA
				1 MHz	270	405	900	1650	3000	TBD	TBD	TBD	TBD	TBD	
				250 KHz	120	280	775	1500	2900	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	110	250	740	1500	2850	TBD	TBD	TBD	TBD	TBD	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	895	1050	1550	2250	3650	TBD	TBD	TBD	TBD	TBD	
				1_MHz	760	920	1400	2150	3500	TBD	TBD	TBD	TBD	TBD	
				250 KHz	630	805	1300	2050	3400	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	625	785	1250	2000	3400	TBD	TBD	TBD	TBD	TBD	

Table 21. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.80	3.95	4.4	5.1	6.35	TBD	TBD	TBD	TBD	TBD	mA
				16 MHz	2.40	2.55	3	3.7	4.9	TBD	TBD	TBD	TBD	TBD	
				8 MHz	1.30	1.45	1.9	2.55	3.75	TBD	TBD	TBD	TBD	TBD	
				4 MHz	0.75	0.88	1.3	1.95	3.2	TBD	TBD	TBD	TBD	TBD	
				2 MHz	0.45	0.59	1	1.65	2.9	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.31	0.44	0.865	1.5	2.75	TBD	TBD	TBD	TBD	TBD	
				100 KHz	0.18	0.31	0.73	1.4	2.6	TBD	TBD	TBD	TBD	TBD	
			Range 1 Boost mode	170 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1	150 MHz	24.50	25	25.5	26.5	28	TBD	TBD	TBD	TBD	TBD	
				120 MHz	19.50	20	20.5	21.5	23	TBD	TBD	TBD	TBD	TBD	
				80 MHz	13.50	13.5	14	15	16.5	TBD	TBD	TBD	TBD	TBD	
				72 MHz	12.00	12	13	13.5	15	TBD	TBD	TBD	TBD	TBD	
				64 MHz	10.50	11	11.5	12.5	14	TBD	TBD	TBD	TBD	TBD	
				48 MHz	8.30	8.5	9.15	10	11.5	TBD	TBD	TBD	TBD	TBD	
				32 MHz	5.55	5.75	6.35	7.2	8.7	TBD	TBD	TBD	TBD	TBD	
				24 MHz	4.25	4.45	5	5.8	7.3	TBD	TBD	TBD	TBD	TBD	
				16 MHz	2.90	3.1	3.65	4.45	5.9	TBD	TBD	TBD	TBD	TBD	

Table 21. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF) (continued)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPRun)	Supply current in Low-power run mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	415	575	1050	1800	3150	TBD	TBD	TBD	TBD	TBD	µA
				1_MHz	250	405	890	1650	3000	TBD	TBD	TBD	TBD	TBD	
				250 KHz	130	280	765	1500	2850	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	97	245	735	1450	2850	TBD	TBD	TBD	TBD	TBD	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	895	1050	1500	2250	3600	TBD	TBD	TBD	TBD	TBD	
				1_MHz	765	910	1400	2100	3500	TBD	TBD	TBD	TBD	TBD	
				250 KHz	665	810	1300	2000	3400	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	640	780	1250	2000	3350	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.

Table 22. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.65	3.85	4.3	5	6.25	TBD	TBD	TBD	TBD	TBD	mA
				16 MHz	2.75	2.9	3.35	4.05	5.3	TBD	TBD	TBD	TBD	TBD	
				8 MHz	1.45	1.6	2.05	2.75	3.95	TBD	TBD	TBD	TBD	TBD	
				4 MHz	0.83	0.97	1.4	2.05	3.3	TBD	TBD	TBD	TBD	TBD	
				2 MHz	0.50	0.635	1.05	1.7	2.95	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.33	0.46	0.895	1.55	2.8	TBD	TBD	TBD	TBD	TBD	
				100 KHz	0.18	0.315	0.74	1.4	2.65	TBD	TBD	TBD	TBD	TBD	
			Range 1 Boost mode	170 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1	150 MHz	18.50	19	19.5	20.5	22	TBD	TBD	TBD	TBD	TBD	
				120 MHz	16.50	17	17.5	18.5	20	TBD	TBD	TBD	TBD	TBD	
				80 MHz	13.00	13.5	14	15	16.5	TBD	TBD	TBD	TBD	TBD	
				72 MHz	12.00	12	12.5	13.5	15	TBD	TBD	TBD	TBD	TBD	
				64 MHz	10.50	10.5	11.5	12	14	TBD	TBD	TBD	TBD	TBD	
				48 MHz	8.10	8.4	9	9.8	11.5	TBD	TBD	TBD	TBD	TBD	
				32 MHz	6.45	6.65	7.3	8.15	9.65	TBD	TBD	TBD	TBD	TBD	
				24 MHz	4.90	5.1	5.7	6.55	8.05	TBD	TBD	TBD	TBD	TBD	
				16 MHz	3.35	3.55	4.1	4.95	6.45	TBD	TBD	TBD	TBD	TBD	

Table 22. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable (continued)

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPRun)	Supply current in Low-power run mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	440	640	1150	1850	3250	TBD	TBD	TBD	TBD	TBD	µA
				1_MHz	300	440	930	1650	3050	TBD	TBD	TBD	TBD	TBD	
				250 KHz	135	285	780	1500	2900	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	91	255	745	1500	2850	TBD	TBD	TBD	TBD	TBD	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	915	1100	1600	2350	3700	TBD	TBD	TBD	TBD	TBD	
				1 MHz	785	945	1400	2150	3550	TBD	TBD	TBD	TBD	TBD	
				250 KHz	700	825	1300	2050	3400	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	670	790	1250	2000	3400	TBD	TBD	TBD	TBD	TBD	

Table 23. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.35	3.5	3.95	4.65	5.9	TBD	TBD	TBD	TBD	TBD	mA
				16 MHz	2.65	2.8	3.25	3.95	5.15	TBD	TBD	TBD	TBD	TBD	
				8 MHz	1.40	1.55	2	2.65	3.9	TBD	TBD	TBD	TBD	TBD	
				4 MHz	0.80	0.935	1.35	2	3.25	TBD	TBD	TBD	TBD	TBD	
				2 MHz	0.48	0.615	1.05	1.7	2.9	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.33	0.45	0.88	1.55	2.75	TBD	TBD	TBD	TBD	TBD	
				100 KHz	0.18	0.31	0.735	1.4	2.6	TBD	TBD	TBD	TBD	TBD	
			Range 1 Boost mode	170 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1	150 MHz	16.00	16.5	17	18	19.5	TBD	TBD	TBD	TBD	TBD	
				120 MHz	14.50	15	15.5	16.5	18	TBD	TBD	TBD	TBD	TBD	
				80 MHz	12.00	12	12.5	13.5	15	TBD	TBD	TBD	TBD	TBD	
				72 MHz	10.50	11	11.5	12.5	14	TBD	TBD	TBD	TBD	TBD	
				64 MHz	9.45	9.7	10.5	11	12.5	TBD	TBD	TBD	TBD	TBD	
				48 MHz	7.35	7.6	8.15	9.05	10.5	TBD	TBD	TBD	TBD	TBD	
				32 MHz	6.15	6.4	7	7.85	9.35	TBD	TBD	TBD	TBD	TBD	
				24 MHz	4.70	4.9	5.5	6.3	7.8	TBD	TBD	TBD	TBD	TBD	
				16 MHz	3.20	3.4	3.95	4.8	6.25	TBD	TBD	TBD	TBD	TBD	

Table 23. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable (continued)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPRun)	Supply current in Low-power run mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	455	610	1100	1850	3200	TBD	TBD	TBD	TBD	TBD	µA
				1_MHz	270	420	910	1650	3000	TBD	TBD	TBD	TBD	TBD	
				250 KHz	130	280	770	1500	2850	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	99	250	735	1450	2850	TBD	TBD	TBD	TBD	TBD	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	935	1100	1550	2300	3650	TBD	TBD	TBD	TBD	TBD	
				1_MHz	785	930	1400	2150	3500	TBD	TBD	TBD	TBD	TBD	
				250 KHz	670	815	1300	2000	3350	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	640	785	1250	2000	3350	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.

Table 24. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.35	3.5	3.95	4.65	5.9	TBD	TBD	TBD	TBD	TBD	mA
				16 MHz	2.15	2.3	2.75	3.4	4.65	TBD	TBD	TBD	TBD	TBD	
				8 MHz	1.15	1.3	1.75	2.4	3.65	TBD	TBD	TBD	TBD	TBD	
				4 MHz	0.68	0.81	1.25	1.9	3.1	TBD	TBD	TBD	TBD	TBD	
				2 MHz	0.42	0.555	0.98	1.65	2.85	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.29	0.425	0.85	1.5	2.7	TBD	TBD	TBD	TBD	TBD	
				100 KHz	0.18	0.305	0.73	1.4	2.6	TBD	TBD	TBD	TBD	TBD	
			Range 1 Boost mode	170 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1	150 MHz	TBD	TBD	TBD	TBD	25	TBD	TBD	TBD	TBD	TBD	
				120 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				80 MHz	21.50	22	22.5	23.5	25	TBD	TBD	TBD	TBD	TBD	
				72 MHz	17.50	17.5	18.5	19	21	TBD	TBD	TBD	TBD	TBD	
				64 MHz	12.00	12	12.5	13.5	15	TBD	TBD	TBD	TBD	TBD	
				48 MHz	10.50	11	11.5	12.5	14	TBD	TBD	TBD	TBD	TBD	
				32 MHz	9.50	9.7	10.5	11	12.5	TBD	TBD	TBD	TBD	TBD	
				24 MHz	7.35	7.6	8.2	9.05	10.5	TBD	TBD	TBD	TBD	TBD	
				16 MHz	4.95	5.15	5.75	6.55	8.05	TBD	TBD	TBD	TBD	TBD	

Table 24. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1 (continued)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPRun)	Supply current in Low-power run mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	365	515	1000	1750	3100	TBD	TBD	TBD	TBD	TBD	µA
				1_MHz	220	365	860	1600	2950	TBD	TBD	TBD	TBD	TBD	
				250 KHz	110	255	750	1500	2850	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	84	230	720	1450	2800	TBD	TBD	TBD	TBD	TBD	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	850	1000	1450	2200	3550	TBD	TBD	TBD	TBD	TBD	
				1_MHz	735	880	1350	2100	3450	TBD	TBD	TBD	TBD	TBD	
				250 KHz	650	790	1250	2000	3350	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	630	765	1250	1950	3350	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.

Table 25. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
IDD (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26MHz	Reduced code(1)	3.80	3.8	mA	146	146	µA/MHz
				Coremark	3.75	3.8		144	146	
				Dhrystone2.1	3.75	3.8		144	146	
				Fibonacci	4.55	4.25		175	163	
				While(1)	3.25	4		125	154	
			Range 1 f_{HCLK}= 150 MHz	Reduced code(1)	24.5	24.5	mA	163	163	µA/MHz
				Coremark	24.50	24		163	160	
				Dhrystone2.1	24.50	24.5		163	163	
				Fibonacci	30.00	28.5		200	190	
				While(1)	21.00	26.5		140	177	
			Range 1 Boost mode f_{HCLK}= 170 MHz	Reduced code(1)	TBD	TBD	mA	TBD	TBD	µA/MHz
				Coremark	TBD	TBD		TBD	TBD	
				Dhrystone2.1	TBD	TBD		TBD	TBD	
				Fibonacci	TBD	TBD		TBD	TBD	
				While(1)	TBD	TBD		TBD	TBD	

Table 25. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) (continued)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (LPRun)	Supply current in Low-power run	SYSCLK source is HSI16 f_{HCLK} = 2 MHz all peripherals disable		Reduced code(1)	895	895	µA	448	448	µA/MHz
				Coremark	860	900		430	450	
				Dhrystone2.1	870	895		435	448	
				Fibonacci	960	950		480	475	
				While(1)	880	925		440	463	

1. Reduced code used for characterization results provided in *Table 20*, *Table 22*, *Table 24*.

Table 26. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK}= 26 MHz	Reduced code(1)	3.65	3.35	mA	140	129	µA/MHz
				Coremark	3.60	3.25		138	125	
				Dhrystone2.1	3.70	3.3		142	127	
				Fibonacci	3.45	2.95		133	113	
				While(1)	3.35	2.8		129	108	
			Range 1 f_{HCLK}= 150 MHz	Reduced code(1)	18.50	16.00	mA	123	107	µA/MHz
				Coremark	18.00	15.50		120	103	
				Dhrystone2.1	18.50	16.00		123	107	
				Fibonacci	16.00	14.00		107	93	
				While(1)	21.50	13.00		143	87	
			Range 1 Boost mode f_{HCLK}= 170 MHz	Reduced code(1)	TBD	TBD	mA	TBD	TBD	µA/MHz
				Coremark	TBD	TBD		TBD	TBD	
				Dhrystone2.1	TBD	TBD		TBD	TBD	
				Fibonacci	TBD	TBD		TBD	TBD	
				While(1)	TBD	TBD		TBD	TBD	

Table 26. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable (continued)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (LPRun)	Supply current in Low-power run	SYSCLK source is HSI16 f_{HCLK} = 2 MHz all peripherals disable		Reduced code(1)	915	935	µA	458	468	µA/MHz
				Coremark	975	940		488	470	
				Dhrystone2.1	980	935		490	468	
				Fibonacci	965	940		483	470	
				While(1)	915	935		458	468	

1. Reduced code used for characterization results provided in *Table 20*, *Table 22*, *Table 24*.

Table 27. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions		Code	TYP	Unit	TYP	Unit
		-	Voltage scaling		25°C		25°C	
IDD (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 MHz	Reduced code(1)	3.35	mA	129	µA/MHz
				Coremark	3.45		133	
				Dhrystone2.1	3.35		129	
				Fibonacci	3.35		129	
				While(1)	3.50		135	
			Range 1 f_{HCLK}= 150 MHz	Reduced code(1)	21.50	mA	143	µA/MHz
				Coremark	22.50		150	
				Dhrystone2.1	21.50		143	
				Fibonacci	22.50		150	
				While(1)	19.50		130	
			Range 1 Boost mode f_{HCLK}= 170 MHz	Reduced code(1)	TBD	mA	TBD	µA/MHz
				Coremark	TBD		TBD	
				Dhrystone2.1	TBD		TBD	
				Fibonacci	TBD		TBD	
				While(1)	TBD		TBD	
IDD (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{HSE} = 2 MHz all peripherals disable		Reduced code(1) Coremark	850	µA	425	µA/MHz
					870		435	
				Dhrystone2.1	850		425	
				Fibonacci	865		433	
				While(1)	825		413	

1. Reduced code used for characterization results provided in *Table 20*, *Table 22*, *Table 24*.

Table 28. Current consumption in Sleep and Low-power mode Flash ON

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Sleep)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	1.05	1.2	1.65	2.3	3.55	TBD	TBD	TBD	TBD	TBD	mA
				16 MHz	0.74	0.88	1.3	2	3.2	TBD	TBD	TBD	TBD	TBD	
				8 MHz	0.46	0.6	1.05	1.7	2.9	TBD	TBD	TBD	TBD	TBD	
				4 MHz	0.32	0.45	0.88	1.55	2.75	TBD	TBD	TBD	TBD	TBD	
				2 MHz	0.24	0.375	0.8	1.45	2.65	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.21	0.335	0.76	1.4	2.65	TBD	TBD	TBD	TBD	TBD	
				100 KHz	0.17	0.3	0.725	1.35	2.6	TBD	TBD	TBD	TBD	TBD	
			Range 1 Boost mode	170 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1	150 MHz	5.50	5.7	6.25	7.1	8.6	TBD	TBD	TBD	TBD	TBD	
				120 MHz	4.50	4.7	5.25	6.05	7.55	TBD	TBD	TBD	TBD	TBD	
				80 MHz	3.15	3.35	3.9	4.7	6.15	TBD	TBD	TBD	TBD	TBD	
				72 MHz	2.90	3.05	3.6	4.4	5.85	TBD	TBD	TBD	TBD	TBD	
				64 MHz	2.60	2.8	3.3	4.1	5.6	TBD	TBD	TBD	TBD	TBD	
				48 MHz	2.20	2.4	2.95	3.8	5.25	TBD	TBD	TBD	TBD	TBD	
				32 MHz	1.50	1.7	2.25	3.05	4.5	TBD	TBD	TBD	TBD	TBD	
				24 MHz	1.20	1.35	1.9	2.7	4.2	TBD	TBD	TBD	TBD	TBD	
				16 MHz	0.88	1.05	1.6	2.4	3.85	TBD	TBD	TBD	TBD	TBD	

Table 28. Current consumption in Sleep and Low-power mode Flash ON (continued)

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPRun)	Supply current in Low-power run mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	175	325	820	1550	2900	TBD	TBD	TBD	TBD	TBD	µA
				1_MHz	130	280	770	1500	2850	TBD	TBD	TBD	TBD	TBD	
				250 KHz	97	250	735	1500	2850	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	89	240	730	1450	2850	TBD	TBD	TBD	TBD	TBD	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	655	800	1300	2000	3350	TBD	TBD	TBD	TBD	TBD	µA
				1_MHz	645	790	1250	2000	3350	TBD	TBD	TBD	TBD	TBD	
				250 KHz	635	775	1250	2000	3350	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	635	775	1250	2000	3350	TBD	TBD	TBD	TBD	TBD	

Table 29. Current consumption in low-power sleep modes, Flash in power-down

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPSleep)	Supply current in power sleep mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	160	310	805	1550	2900	TBD	TBD	TBD	TBD	TBD	mA
				1_MHz	120	265	760	1500	2850	TBD	TBD	TBD	TBD	TBD	
				250 KHz	85	235	725	1450	2800	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	78	225	715	1450	2800	TBD	TBD	TBD	TBD	TBD	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	645	780	1250	2000	3350	TBD	TBD	TBD	TBD	TBD	
				1_MHz	630	770	1250	2000	3350	TBD	TBD	TBD	TBD	TBD	
				250 KHz	625	765	1250	1950	3350	TBD	TBD	TBD	TBD	TBD	
				62.5 KHz	620	760	1250	1950	3350	TBD	TBD	TBD	TBD	TBD	

Table 30. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Stop 1)	Supply current in Stop 1 mode, RTC disabled	RTC disabled	1.8 V	46	165	570	1200	2350	TBD	TBD	TBD	TBD	TBD	µA
			2.4 V	46	165	570	1200	2350	TBD	TBD	TBD	TBD	TBD	
			3.0 V	47	170	575	1200	2350	TBD	TBD	TBD	TBD	TBD	
			3.6 V	46.50	170	575	1200	2400	TBD	TBD	TBD	TBD	TBD	
IDD (Stop 1 with RTC)	Supply current in Stop 1 mode, RTC enabled	RTC clocked by LSI	1.8 V	46.50	165	570	1200	2350	TBD	TBD	TBD	TBD	TBD	
			2.4 V	47.50	165	570	1200	2350	TBD	TBD	TBD	TBD	TBD	
			3.0 V	48	170	575	1200	2350	TBD	TBD	TBD	TBD	TBD	
			3.6 V	47.50	170	580	1200	2400	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	47	160	545	1150	2300	TBD	TBD	TBD	TBD	TBD	
			2.4 V	47	160	545	1150	2300	TBD	TBD	TBD	TBD	TBD	
			3.0 V	47.50	160	545	1150	2300	TBD	TBD	TBD	TBD	TBD	
			3.6 V	48	160	550	1150	2300	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE quartz in low drive mode at 32768 Hz	1.8 V	47	160	555	1150	-	TBD	TBD	TBD	TBD	TBD	
			2.4 V	47	160	555	1150	-	TBD	TBD	TBD	TBD	TBD	
			3.0 V	47	160	555	1150	-	TBD	TBD	TBD	TBD	TBD	
			3.6 V	47.50	160	560	1150	-	TBD	TBD	TBD	TBD	TBD	
IDD (wakeup from Stop 1	Supply current during wakeup from Stop 1 mode	Wakeup clock is HSI6, voltage Range 1	3.0 V	TBD	-	-	-	-	TBD	TBD	TBD	TBD	TBD	mA
		Wakeup clock is HSI6 = 4 MHz, (HPRE = 4), voltage Range 2	3.0 V	TBD	-	-	-	-	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.

Table 31. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(Stop 0)	Supply current in Stop 0 mode, RTC disabled	-	1.8 V	155	280	690	1350	2550	TBD	TBD	TBD	TBD	TBD	µA
			2.4 V	155	280	695	1350	2550	TBD	TBD	TBD	TBD	TBD	
			3 V	155	280	695	1350	2550	TBD	TBD	TBD	TBD	TBD	
			3.6 V	160	285	695	1350	2550	TBD	TBD	TBD	TBD	TBD(2)	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 32. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	No independent watchdog	1.8 V	99	305	1600	4700	13000	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	110	355	1850	5500	15000	TBD	TBD	TBD	TBD	TBD	
			3 V	130	425	2200	6500	17500	TBD	TBD	TBD	TBD	TBD	
			3.6 V	195	585	2850	8050	21500	TBD	TBD	TBD	TBD	TBD	
		With independent watchdog	1.8 V	295	-	-	-	-	TBD	TBD	TBD	TBD	TBD	
			2.4 V	370	-	-	-	-	TBD	TBD	TBD	TBD	TBD	
			3 V	435	-	-	-	-	TBD	TBD	TBD	TBD	TBD	
			3.6 V	550	-	-	-	-	TBD	TBD	TBD	TBD	TBD	

Table 32. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	1.8 V	540	750	2050	5100	13000	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	700	945	2450	6050	15500	TBD	TBD	TBD	TBD	TBD	
			3 V	880	1200	2950	7200	18500	TBD	TBD	TBD	TBD	TBD	
			3.6 V	1150	1500	3750	8950	22500	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSI, with independent watchdog	1.8 V	575	-	-	-	-	TBD	TBD	TBD	TBD	TBD	
			2.4 V	760	-	-	-	-	TBD	TBD	TBD	TBD	TBD	
			3 V	955	-	-	-	-	TBD	TBD	TBD	TBD	TBD	
			3.6 V	1200	-	-	-	-	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	425	625	1900	4900	13000	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	575	820	2300	5850	15500	TBD	TBD	TBD	TBD	TBD	
			3 V	755	1050	2800	6950	18000	TBD	TBD	TBD	TBD	TBD	
			3.6 V	1000	1400	3550	8700	22000	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE quartz(2) in low drive mode	1.8 V	260	500	1800	4600	12500	TBD	TBD	TBD	TBD	TBD	
			2.4 V	335	625	2200	5300	14500	TBD	TBD	TBD	TBD	TBD	
			3 V	485	825	2700	6250	17000	TBD	TBD	TBD	TBD	TBD	
			3.6 V	730	1200	3600	7800	21000	TBD	TBD	TBD	TBD	TBD	
I_{DD} (SRAM2)(3)	Supply current to be added in Standby mode when SRAM2 is retained	-	1.8 V	266	645	2300	5300	12000	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	255	645	2300	5500	12000	TBD	TBD	TBD	TBD	TBD	
			3 V	260	675	2300	5500	12000	TBD	TBD	TBD	TBD	TBD	
			3.6 V	260	665	2300	5450	12000	TBD	TBD	TBD	TBD	TBD	

Table 32. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is HSI16 = 16 MHz(4)	3 V	TBD	-	-	-	-	TBD	TBD	TBD	TBD	TBD	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. The supply current in Standby with SRAM2 mode is: I_{DD_ALL}(Standby) + I_{DD_ALL}(SRAM2). The supply current in Standby with RTC with SRAM2 mode is: II_{DD_ALL}(Standby + RTC) + I_{DD_ALL}(SRAM2).
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 36: Low-power mode wakeup timings*.

Table 33. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	15	160	1100	3450	10500	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	23	195	1300	4050	12000	TBD	TBD	TBD	TBD	TBD	
			3 V	40	250	1550	4850	14500	TBD	TBD	TBD	TBD	TBD	
			3.6 V	94	395	2100	6250	18000	TBD	TBD	TBD	TBD	TBD	

Table 33. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	345	485	1400	3750	10500	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	490	660	1750	4450	12500	TBD	TBD	TBD	TBD	TBD	
			3 V	665	875	2150	5400	14500	TBD	TBD	TBD	TBD	TBD	
			3.6 V	900	1200	2900	6950	18500	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE quartz(2) in low drive mode	1.8 V	175	360	1300	3550	-	TBD	TBD	TBD	TBD	TBD	
			2.4 V	260	470	1650	4150	-	TBD	TBD	TBD	TBD	TBD	
			3 V	410	670	2100	4950	-	TBD	TBD	TBD	TBD	TBD	
			3.6 V	650	1000	2950	6450	-	TBD	TBD	TBD	TBD	TBD	
IDD(wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is HSI16 = 16 MHz(3)	3 V	TBD	-	-	-	-	TBD	TBD	TBD	TBD	TBD	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 36: Low-power mode wakeup timings*.

Table 34. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{BAT}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(VBAT)	Backup domain supply current	RTC disabled	1.8 V	4	20	125	385	1100	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	5	23	145	440	1250	TBD	TBD	TBD	TBD	TBD	
			3 V	7	28	170	515	1450	TBD	TBD	TBD	TBD	TBD	
			3.6 V	12	59	335	1000	2900	TBD	TBD	TBD	TBD	TBD	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	330	350	460	720	-	-	-	-	-	-	
			2.4 V	470	490	620	920	-	-	-	-	-	-	
			3 V	630	660	805	1150	-	-	-	-	-	-	
			3.6 V	815	860	1150	1850	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz(2)	1.8 V	150	235	380	565	1300	-	-	-	-	-	
			2.4 V	215	345	560	630	1450	-	-	-	-	-	
			3 V	330	485	760	760	1650	-	-	-	-	-	
			3.6 V	515	720	1250	1400	3200	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 54: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC, OPAMP, COMP input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 36: Low-power mode wakeup timings*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 36*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 13: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 36*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 35. Peripheral current consumption

Bus	Peripheral	Range 1	Range 2	Low-power run and sleep	Unit
-	Bus Matrix	5.70	4.70	6.00	uA/MHz
	AHB1 to APB1 bridge	0.26	0.19	0.10	
	AHB1 to APB2 bridge	0.39	0.32	0.10	
AHB1	CORDIC	1.20	1.00	1.00	uA/MHz
	CRC	0.71	0.60	0.50	
	DMA 1	2.66	2.19	2.50	
	DMA 2	2.92	2.40	2.50	
	DMAMUX	6.32	5.24	6.00	
	SRAM1	0.55	0.45	0.50	
	FLASH	6.03	4.97	6.00	
	FMAC	4.31	3.59	4.50	

Table 35. Peripheral current consumption (continued)

Bus	Peripheral	Range 1	Range 2	Low-power run and sleep	Unit
AHB2	ADC1/ADC2	5.82	4.81	5.50	uA/MHz
	ADC3	7.65	6.32	7.00	
	DAC1	4.42	3.66	4.50	
	DAC3	4.34	3.59	4.00	
	GPIOA	0.08	0.06	0.50	
	GPIOB	0.09	0.07	0.50	
	GPIOC	0.09	0.07	1.00	
	GPIOD	0.05	0.06	0.50	
	GPIOE	0.22	0.16	0.50	
	GPIOF	0.06	0.05	0.50	
	GPIOG	0.24	0.20	1.00	
	SRAM2	0.36	0.28	0.50	
	CCM SRAM	0.26	0.25	0.50	
	RNG	1.96	NA	NA	

Table 35. Peripheral current consumption (continued)

Bus	Peripheral	Range 1	Range 2	Low-power run and sleep	Unit
APB1	CRS	0.27	0.22	0.50	uA/MHz
	FDCAN1/FDCAN2	20.87	17.31	20.00	
	I2C1	1.22	1.01	1.50	
	I2C2	1.22	1.01	1.50	
	I2C3	1.19	0.98	1.50	
	I2C4	1.18	0.97	1.50	
	LPTIM1	1.04	0.89	1.00	
	LPUART1	1.80	1.49	2.00	
	PWR	0.66	0.55	1.00	
	RTC	2.50	2.14	3.50	
	SPI2/I2S2	3.78	3.18	4.00	
	SPI3/I2S3	3.82	3.16	4.00	
	TIM2	7.46	6.15	7.00	
	TIM3	5.99	4.90	6.00	
	TIM4	6.05	5.02	6.00	
	TIM5	7.76	6.43	7.50	
	TIM6	1.15	0.95	1.50	
	TIM7	1.20	1.00	1.50	
	UART4	2.35	1.96	2.50	
	UART5	2.62	2.18	3.00	
	USART2	2.59	2.15	3.00	
	USART3	2.55	2.13	3.00	
	USB	0.43	NA	NA	
	USB PD	1.19	5.55	NA	
	WWDG	0.40	0.34	1.00	

Table 35. Peripheral current consumption (continued)

Bus	Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB2	SAI1		2.49	2.04	2.50	uA/MHz
	SPI1		1.86	1.53	2.00	
	SPI4		1.86	1.53	2.00	
	TIM1		10.22	8.52	9.50	
	TIM8		10.05	8.36	9.50	
	TIM15		4.52	3.71	4.50	
	TIM16		3.48	2.92	3.50	
	TIM17		3.44	2.83	3.50	
	USART1		2.32	2.30	2.50	
	SYSCFG/COMP/OPAMP/VREFBUF		1.51	1.23	1.50	
Independent clock domain	ADC1/ADC2	independent clock domain	0.67	0.53	0.50	uA/MHz
	ADC3	independent clock domain	0.63	0.52	1.00	
	FDCAN1/FDCAN2	independent clock domain	10.95	9.07	10.50	
	I2C1	independent clock domain	3.79	3.17	3.50	
	I2C2	independent clock domain	3.56	2.98	3.50	
	I2C3	independent clock domain	2.58	2.19	2.50	
	I2C4	independent clock domain	3.70	3.14	3.50	
	I2S2	independent clock domain	1.38	1.21	1.50	
	I2S3	independent clock domain	1.43	1.16	1.50	
	LPTIM1	independent clock domain	9.39	7.76	9.50	
	LPUART1	independent clock domain	4.18	3.49	4.00	
	RNG	independent clock domain	0.89	NA	NA	
	USB	independent clock domain	1.18	NA	NA	
	SAI1	independent clock domain	3.14	2.59	3.00	
	UART4	independent clock domain	6.24	5.18	6.00	
	UART5	independent clock domain	6.22	5.16	6.00	
	USART1	independent clock domain	7.16	5.94	6.50	
	USART2	independent clock domain	6.94	5.79	6.50	
	USART3	independent clock domain	7.50	6.10	7.00	

5.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 36* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 36. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		TBD	TBD	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	-		TBD	TBD	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock HSI16 = 16 MHz	TBD	TBD	µs
		Range 2	Wakeup clock HSI16 = 16 MHz	TBD	TBD	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock HSI16 = 16 MHz	TBD	TBD	
		Range 2	Wakeup clock HSI16 = 16 MHz	TBD	TBD	
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in Flash	Range 1	Wakeup clock HSI16 = 16 MHz	TBD	TBD	
		Range 2	Wakeup clock HSI16 = 16 MHz	TBD	TBD	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock HSI16 = 16 MHz	TBD	TBD	
		Range 2	Wakeup clock HSI16 = 16 MHz	TBD	TBD	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock HSI16 = 16 MHz, with HPRE = 8	TBD	TBD	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			TBD	TBD	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock HSI16 = 16 MHz	TBD	TBD	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock HSI16 = 16 MHz	TBD	TBD	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock HSI16 = 16 MHz	TBD	TBD	

1. Guaranteed by characterization results.

Table 37. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low- power run mode to Run mode(2)	Wakeup clock HSI16 = 16 MHz with HPRE = 8	TBD	TBD	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Wakeup clock HSI16 = 16 MHz with HPRE = 8	TBD	TBD	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

Table 38. Wakeup time using USART/LPUART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wakeup up from stop mode when USART/LPUART clock source is HSI16	Stop 0 mode	-	1.7	µs
		Stop 1 mode	-	8.5	

1. Guaranteed by characterization results.

5.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

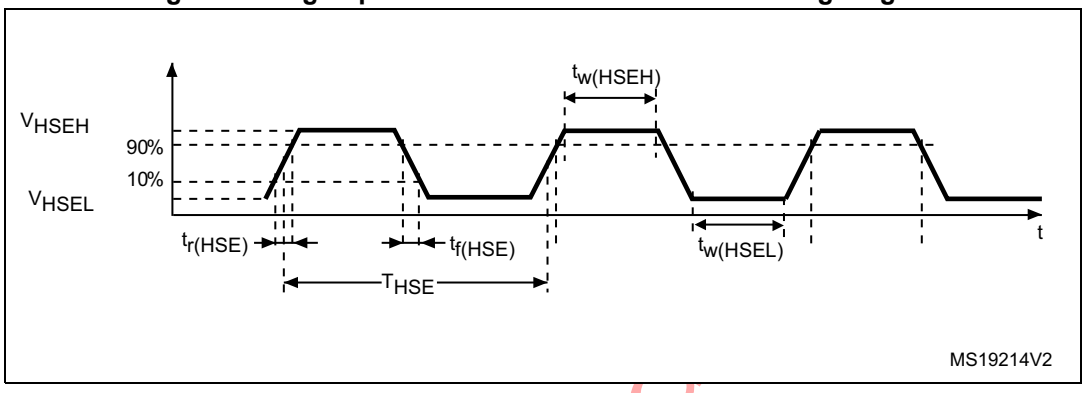
The external clock signal has to respect the I/O characteristics in *Section 5.3.14*. However, the recommended clock input waveform is shown in *Figure 19: High-speed external clock source AC timing diagram*.

Table 39. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DD}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

1. Guaranteed by design.

Figure 19. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

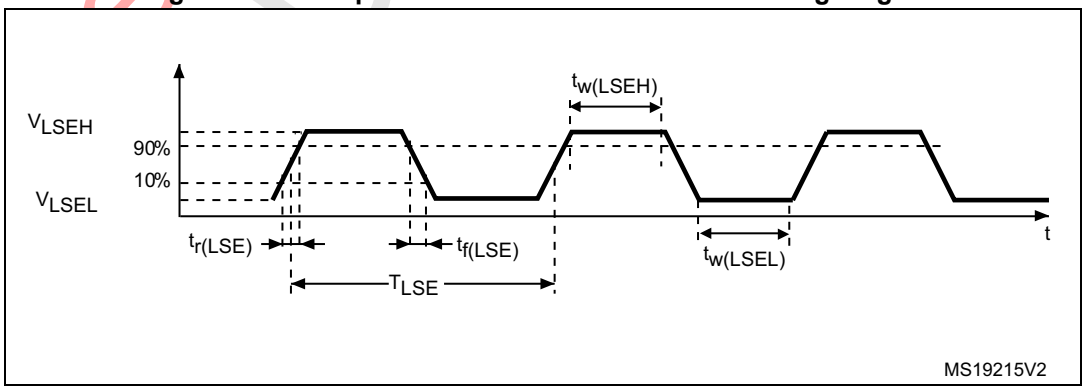
The external clock signal has to respect the I/O characteristics in *Section 5.3.14*. However, the recommended clock input waveform is shown in *Figure 20*.

Table 40. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DD}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 20. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 41. HSE oscillator characteristics(1)

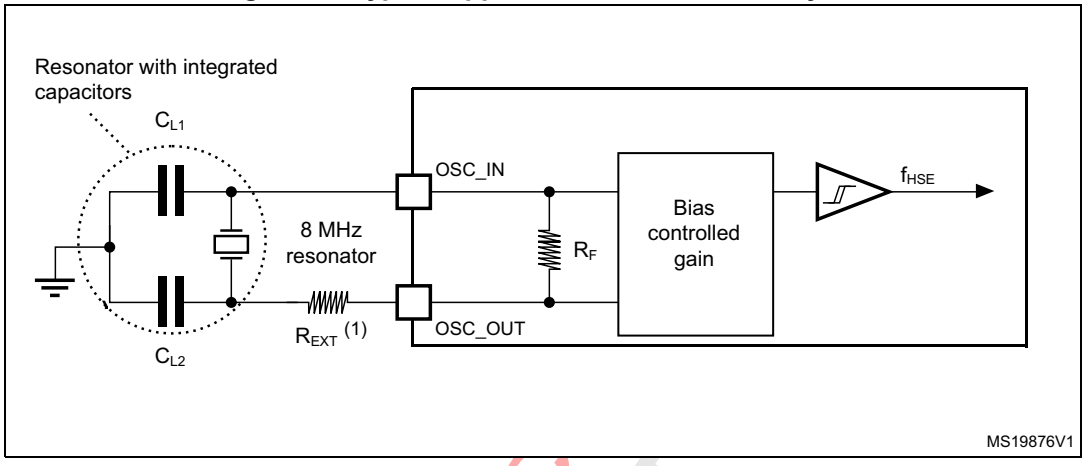
Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 21*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 21. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 42*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

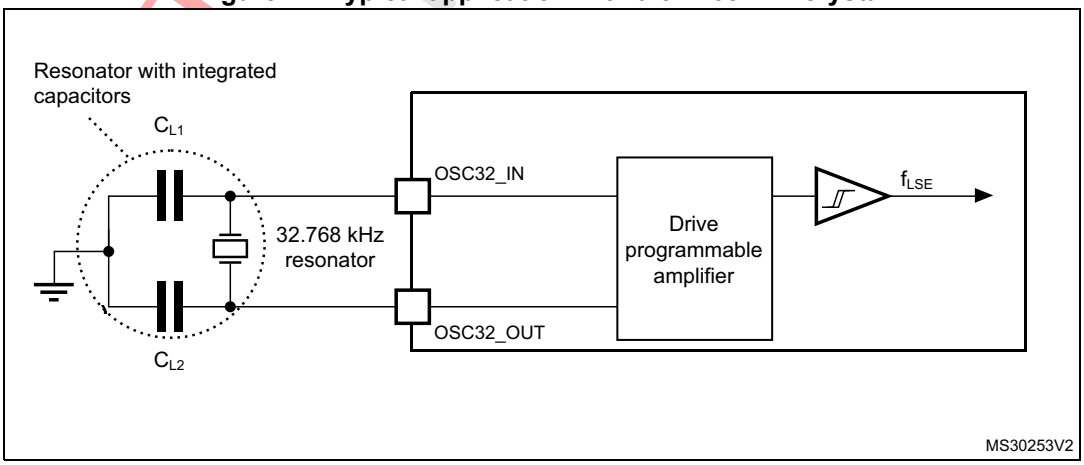
Table 42. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 22. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

5.3.8 Internal clock source characteristics

The parameters given in *Table 43* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 16: General operating conditions*. The provided curves are characterization results, not tested in production.

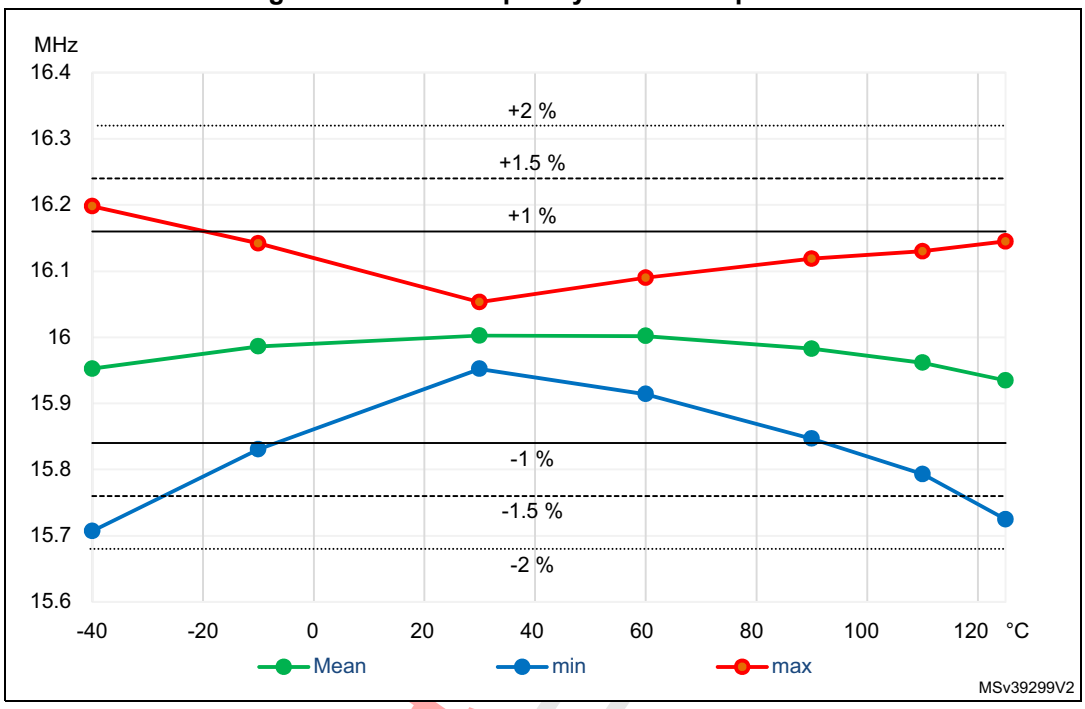
High-speed internal (HSI16) RC oscillator

Table 43. HSI16 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	TBD	-6	TBD	
DuCy(HSI16)(2)	Duty Cycle	-	45	-	55	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%
t_{su}(HSI16)(2)	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
t_{stab}(HSI16)(2)	HSI16 oscillator stabilization time	-	-	3	5	µs
I_{DD}(HSI16)(2)	HSI16 oscillator power consumption	-	-	155	190	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Figure 23. HSI16 frequency versus temperature



High-speed internal 48 MHz (HSI48) RC oscillator

Table 44. HSI48 oscillator characteristics(1)

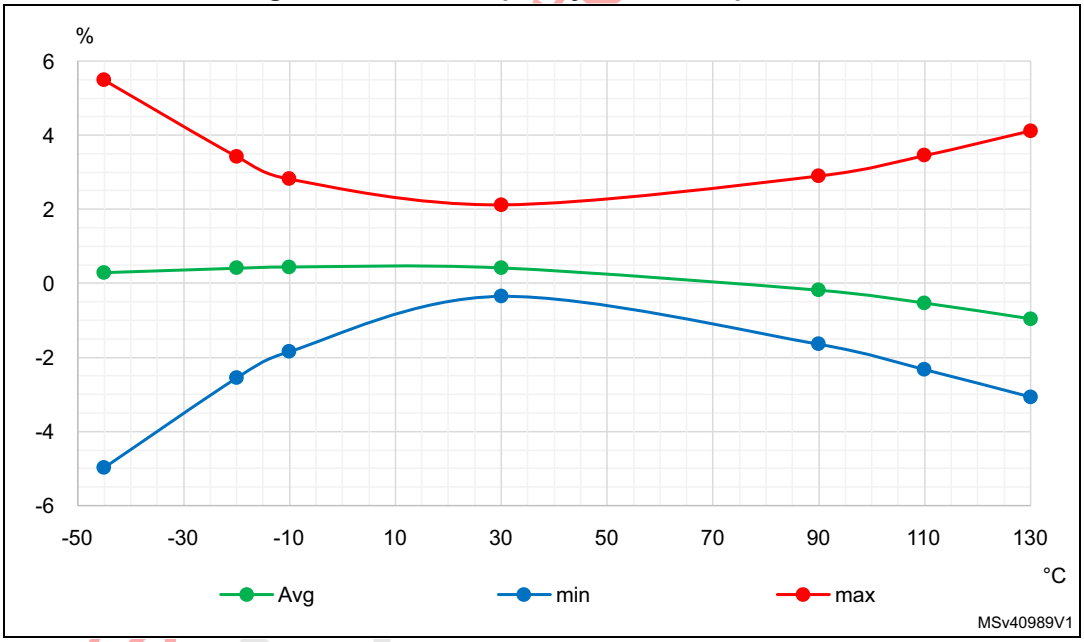
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD}=3.0V, T_A=30°C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	%
DuCy(HSI48)	Duty Cycle	-	45(2)	-	55(2)	%
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –15 to 85 °C	-	-	±3(3)	%
		V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 125 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	%
		V_{DD} = 1.65 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA

Table 44. HSI48 oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(4)	-	-	+/-0.15(2)	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(4)	-	-	+/-0.25(2)	-	ns

1. V_{DD} = 3 V, T_A = –40 to 125°C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

Figure 24. HSI48 frequency versus temperature



Low-speed internal (LSI) RC oscillator

Table 45. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, T_A = -40 to 125 °C	29.5	-	34	
$t_{SU}(LSI)$(2)	LSI oscillator start-up time	-	-	80	130	µs

Table 45. LSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{STAB}(LSI)^{(2)}$	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
$I_{DD}(LSI)^{(2)}$	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

5.3.9 PLL characteristics

The parameters given in *Table 46* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions*.

Table 46. PLL characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	TBD	-	TBD	MHz
	PLL input clock duty cycle	-	TBD	-	TBD	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1 Boost mode	TBD	-	TBD	MHz
		Voltage scaling Range 1	TBD	-	TBD	
		Voltage scaling Range 2	TBD	-	TBD	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1 Boost mode	TBD	-	TBD	
		Voltage scaling Range 1	TBD	-	TBD	
		Voltage scaling Range 2	TBD	-	TBD	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1 Boost mode	TBD	-	TBD	
		Voltage scaling Range 1	TBD	-	TBD	
		Voltage scaling Range 2	TBD	-	TBD	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1 Boost mode	TBD	-	TBD	
		Voltage scaling Range 1	TBD	-	TBD	
		Voltage scaling Range 2	TBD	-	TBD	
t_{LOCK}	PLL lock time	-	-	TBD	TBD	µs
Jitter	RMS cycle-to-cycle jitter	System clock 170 MHz	-	TBD	-	±ps
	RMS period jitter		-	TBD	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}(1)	VCO freq = 64 MHz	-	TBD	TBD	µA
		VCO freq = 96 MHz	-	TBD	TBD	
		VCO freq = 192 MHz	-	TBD	TBD	
		VCO freq = 344 MHz	-	TBD	TBD	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values.

5.3.10 Flash memory characteristics

Table 47. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	TBD	TBD	µs
t_{prog_row}	One row (32 double word) programming time	Normal programming	TBD	TBD	ms
		Fast programming	TBD	TBD	
t_{prog_page}	One page (2 Kbytes) programming time	Normal programming	TBD	TBD	
		Fast programming	TBD	TBD	
t_{ERASE}	Page (2 Kbytes) erase time	-	TBD	TBD	
t_{prog_bank}	One bank (256 Kbyte) programming time	Normal programming	TBD	TBD	s
		Fast programming	TBD	TBD	
t_{ME}	Mass erase time (one or two banks)	-	TBD	TBD	ms
I_{DD}	Average consumption from VDD	Write mode	TBD	-	mA
		Erase mode	TBD	-	
	Maximum current (peak)	Write mode	TBD	-	
		Erase mode	TBD	-	

1. Guaranteed by design.

Table 48. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 49*. They are based on the EMS levels and classes defined in application note AN1709.

Table 49. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 170 MHz, conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 170 MHz, conforming to IEC 61000-4-4	5B

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 50. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8 MHz / 170 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP128 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	4	dBµV
			30 MHz to 130 MHz	0	
			130 MHz to 1 GHz	16	
			1 GHz to 2 GHz	11	
			EMI Level	3.5	-

5.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 51. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	TBD	TBD	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS- 002	TBD	TBD	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on three parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78E IC latch-up standard.

Table 52. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	TA = +125 °C conforming to JESD78E	Class II level A

5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 53*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 53. I/O current injection susceptibility

Symbol	Description		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}(1)	Injected current on pin	All except TT_a, PF10, PB8-BOOT0, PC10	-5	NA	mA
		PF10, PB8-BOOT0, PC10	-0	NA	
		TT_a pins	-5	0	

1. Guaranteed by characterization.

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 54* are derived from tests performed under the conditions summarized in *Table 16: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

Table 54. I/O static characteristics

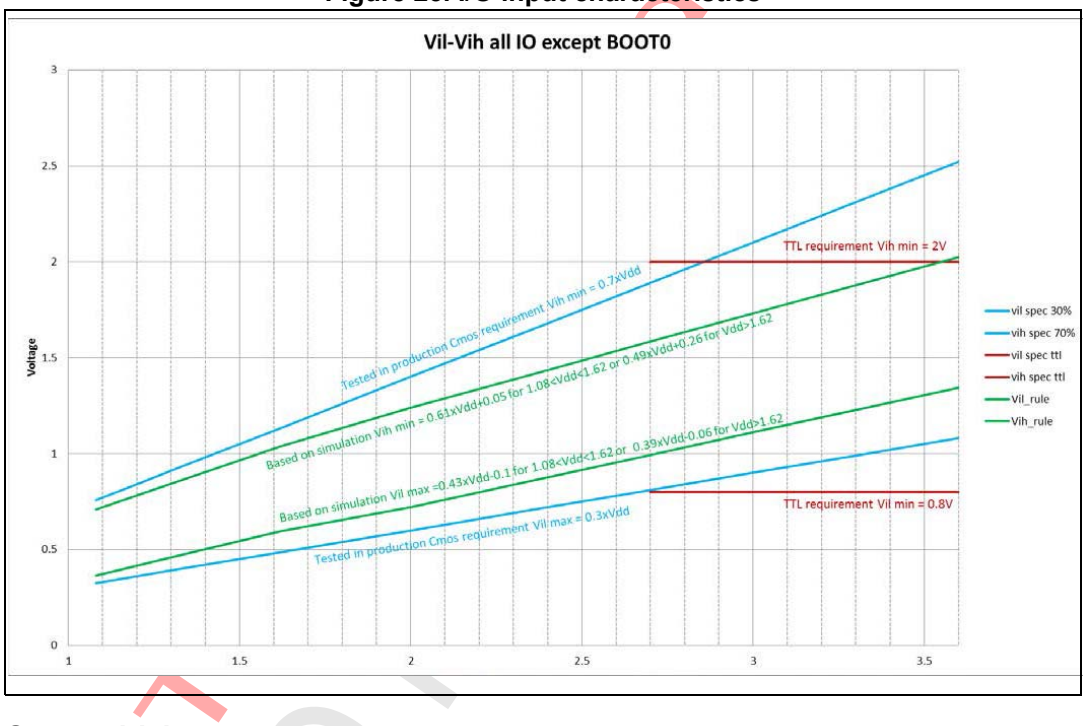
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage	All except FT_c	1.62 V<V_{DD}<3.6 V	--	--	0.3xV_{DD}	V
						0.39xV_{DD}-0.06(2)	
		FT_c	2 V<V_{DD}<2.7 V	-	-	0.3xV_{DD}	
			1.62 V<V_{DD}<2.7 V	-	-	0.2.5xV_{DD}	
V_{IH}(1)	I/O input high level voltage	All except FT_c	1.62 V<V_{DD}<3.6 V	0.7xV_{DD}	-	-	V
				0.49xV_{DD} +0.26(2)	-	-	
		FT_c	1.62 V<V_{DD}<3.6 V	0.7xV_{DD}	-	-	
V_{HYS}(2)	Input hysteresis	TT_xx, FT_xxx, NRST	1.62 V<V_{DD}<3.6 V	-	200	-	mV
I_{leak}	Input leakage current(2)	FT_xx except FT_c	0 < V_{IN} ≤ V_{DD}	-	-	±100	nA
			V_{DD} ≤ V_{IN} ≤ V_{DD}+1 V	-	-	650(3)	
			V_{DD}+1 V < V_{IN} ≤ 5.5 V	-	-	200(3)	
		FT_c	0< ≤ V_{IN} ≤ V_{DDMAX}	-	-	2000	
			V_{DD} ≤ V_{IN} <0.5 V	-	-	3000	
		FT_u, PC3	0 ≤ V_{IN} ≤ V_{DD}	-	-	±150	
			V_{DD} ≤ V_{IN} ≤ V_{DD}+ 1 V	-	-	±2500	
			V_{DD} ≤ V_{IN} ≤ 5.5 V	-	-	±250	
		FT_d	0 ≤ V_{IN} ≤ V_{DD}	-	-	±4500	
			V_{DD} + 1V ≤ V_{IN} ≤ 5.5 V	-	-	±9000	
		TT_xx	0 ≤ V_{IN} ≤ V_{DD}	-	-	±150	
			V_{DD} ≤ V_{IN} ≤ 3.6 V	-	-	2000	
R_{PU}	Weak pull-up equivalent resistor(4)	V_{IN} = V_{SS}		25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	V_{IN} = V_{DD}		25	40	55	
C_{IO}	I/O pin capacitance	I/O pin capacitance	-	-	5	-	pF

1. Refer to *Figure 25: I/O input characteristics*

2. Guaranteed by design.
3. This value represents the pad leakage of the I/O itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of I/Os where VIN is applied on the pad] x I_{lkg}(Max).
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 25* for standard I/Os, and in *Figure 25* for 5 V tolerant I/Os.

Figure 25. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 13: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 13: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 16: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 55. Output voltage characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(3)	Output low level voltage for an I/O pin	CMOS port $\|I_{IO}\|$ = 2 mA for FT_c I/Os = 8 mA for other I/Os V_{DD} ≥ 2.7 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port $\|I_{IO}\|$ = 2 mA for FT_c I/Os = 8 mA for other I/Os V_{DD} ≥ 2.7 V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	All I/Os except FT_c $\|I_{IO}\|$ = 20 mA V_{DD} ≥ 2.7 V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}-1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 1 mA for FT_c I/Os = 4 mA for other I/Os V_{DD} ≥ 1.62 V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}-0.45	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with “f” option)	$\|I_{IO}\|$ = 20 mA V_{DD} ≥ 2.7 V	-	0.4	
		$\|I_{IO}\|$ = 10 mA V_{DD} ≥ 1.62 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 13: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 26* and *Table 56*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 16: General operating conditions*.

Table 56. I/O (except FT_c) AC characteristics(1) (2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	1	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	1.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	52	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	37	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	16	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	9	
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	25	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	100(3)	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	37.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	11	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	5	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	120(3)	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	50	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	180(3)	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	75	
	Tr/Tf	Output rise and fall time(4)	C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	6	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	1.7	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	3.3	

Table 56. I/O (except FT_c) AC characteristics(1) (2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
FM+	Fmax(5)	Maximum frequency	C=50 pF, 1.6 V≤V_{DD}≤3.6 V	-	1	MHz
	Tr/TF(4)	Output high to low level fall time		-	5	ns

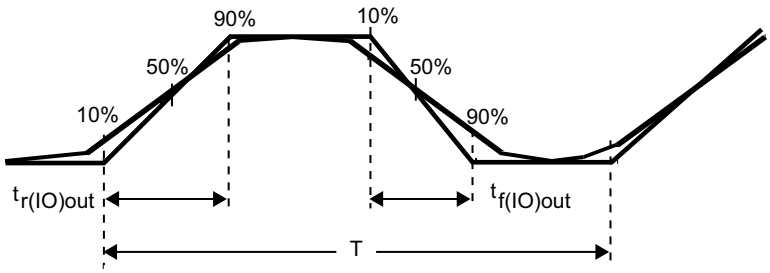
1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0440 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represented the I/O capability but maximum system frequency is 170 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I2C specification.
5. The maximum frequency is defined with the following conditions:
   - (Tr+ Tf) ≤ 2/3 T.
   - 45%<Duty cycle<55%

Table 57. I/O FT_c AC characteristics(1) (2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	2	MHz
			C=50 pF, 1.6 V≤V_{DD}≤2.7 V	-	1	
	Tr/Tf	Output H/L to L/H level fall time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	170	ns
			C=50 pF, 1.6 V≤V_{DD}≤2.7 V	-	330	
1	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	10	MHz
			C=50 pF, 1.6 V≤V_{DD}≤2.7 V	-	5	
	Tr/Tf	Output H/L to L/H level fall time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	35	ns
			C=50 pF, 1.6 V≤V_{DD}≤2.7 V	-	65	

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0440 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.

Figure 26. I/O AC characteristics definition(1)



Maximum frequency is achieved if (t_r + t_f (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

MS32132V2

1. Refer to *Table 56: I/O (except FT_c) AC characteristics*

5.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

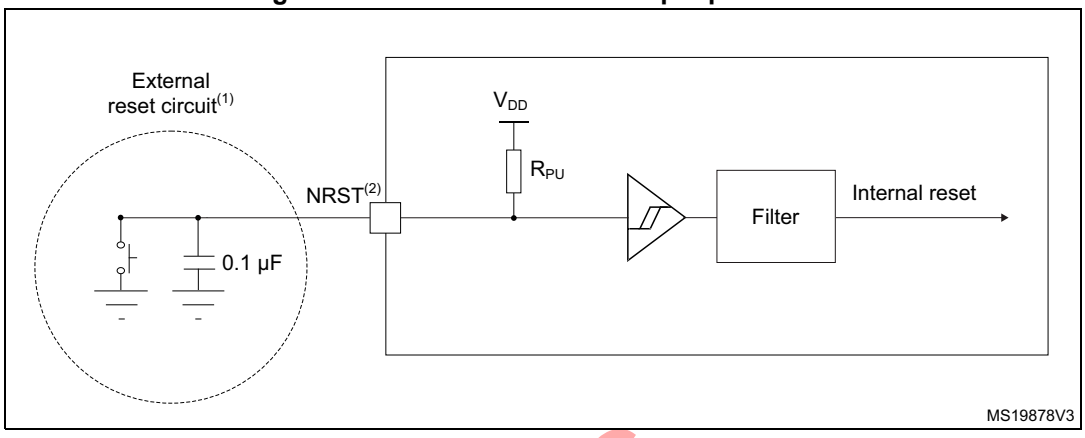
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 16: General operating conditions*.

Table 58. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3_x V_{DD}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7_x V_{DD}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 27. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 58: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

5.3.16 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 59. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	TBD	-	-	ns

1. Guaranteed by design.

5.3.17 Analog switches booster

Table 60. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

5.3.18 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in *Table 61* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 16: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 61. ADC characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 1	-	-	80	MHz
		Range 2	-	-	26	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	5.33	Msps
		Resolution = 10 bits	-	-	6.15	
		Resolution = 8 bits	-	-	7.27	
		Resolution = 6 bits	-	-	8.88	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	4.21	
		Resolution = 10 bits	-	-	4.71	
		Resolution = 8 bits	-	-	5.33	
		Resolution = 6 bits	-	-	6.15	
f_{TRIG}	External trigger frequency	f_{ADC} = 80 MHz Resolution = 12 bits	-	-	5.33	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{AIN} (3)	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			conversion cycle

Table 61. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CAL}	Calibration time	f_{ADC} = 80 MHz	1.45			µs
		-	116			$1/f_{ADC}$
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 80 MHz	0.03125	-	8.00625	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80 MHz Resolution = 12 bits	0.1875	-	8.1625	µs
		Resolution = 12 bits	ts + 12.5 cycles for successive approximation = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the VDDA supply	fs = 5 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 5 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 5 Msps	-	260	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package.
   Refer to *Section 4: Pinouts and pin description* for further details.

The maximum value of R_{AIN} can be found in *Table 62: Maximum ADC RAIN*.

Table 62. Maximum ADC R_{AIN}(1)(2)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	R_{AIN} max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

1. Guaranteed by design.
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. Fast channels are: TBD
4. Slow channels are: all ADC inputs except the fast channels.

Table 63. ADC accuracy - limited test conditions 1(1)(2)(3)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	TBD	TBD	LSB
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
EO	Offset error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
EG	Gain error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	TBD	TBD	-	bits
				Slow channel (max speed)	TBD	TBD	-	
			Differential	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	TBD	TBD	-	dB
				Slow channel (max speed)	TBD	TBD	-	
			Differential	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	
			Differential	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	

Table 63. ADC accuracy - limited test conditions 1(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA} = V_{REF+} = 3$ V, TA = 25 °C	Single ended	Fast channel (max speed)	-	-74	-73	dB
				Slow channel (max speed)	-	-74	-73	
			Differential	Fast channel (max speed)	-	-79	-76	
				Slow channel (max speed)	-	-79	-76	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 64. ADC accuracy - limited test conditions 2(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	TBD	TBD	LSB
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
EO	Offset error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
EG	Gain error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	TBD	TBD	-	bits
				Slow channel (max speed)	TBD	TBD	-	
			Differential	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	TBD	TBD	-	dB
				Slow channel (max speed)	TBD	TBD	-	
			Differential	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	
			Differential	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	

Table 64. ADC accuracy - limited test conditions 2(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	TBD	TBD	dB
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 65. ADC accuracy - limited test conditions 3(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.62 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	TBD	TBD	LSB
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
EO	Offset error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
EG	Gain error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	TBD	TBD	-	bits
				Slow channel (max speed)	TBD	TBD	-	
			Differential	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	TBD	TBD	-	dB
				Slow channel (max speed)	TBD	TBD	-	
			Differential	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	
			Differential	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	

Table 65. ADC accuracy - limited test conditions 3(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.62 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	TBD	TBD	dB
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 66. ADC accuracy - limited test conditions 4(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 26 MHz, 1.62 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	TBD	TBD	LSB
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
EO	Offset error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
EG	Gain error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	TBD	TBD	-	bits
				Slow channel (max speed)	TBD	TBD	-	
			Differential	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	TBD	TBD	-	dB
				Slow channel (max speed)	TBD	TBD	-	
			Differential	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	
			Differential	Fast channel (max speed)	TBD	TBD	-	
				Slow channel (max speed)	TBD	TBD	-	

Table 66. ADC accuracy - limited test conditions 4(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 26 MHz, 1.62 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	TBD	TBD	dB
				Slow channel (max speed)	-	TBD	TBD	
			Differential	Fast channel (max speed)	-	TBD	TBD	
				Slow channel (max speed)	-	TBD	TBD	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Figure 28. ADC accuracy characteristics

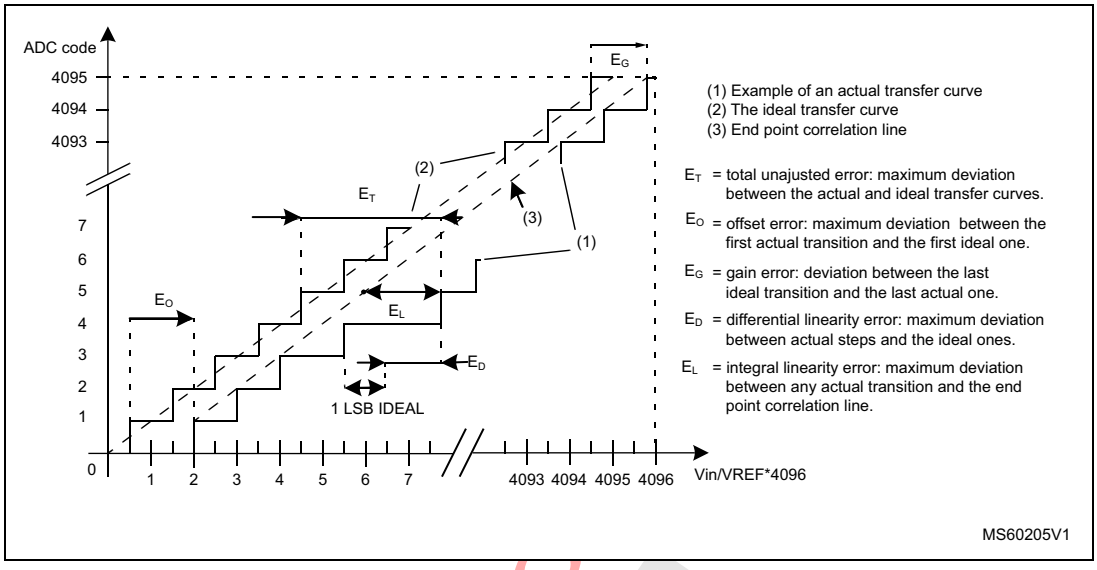
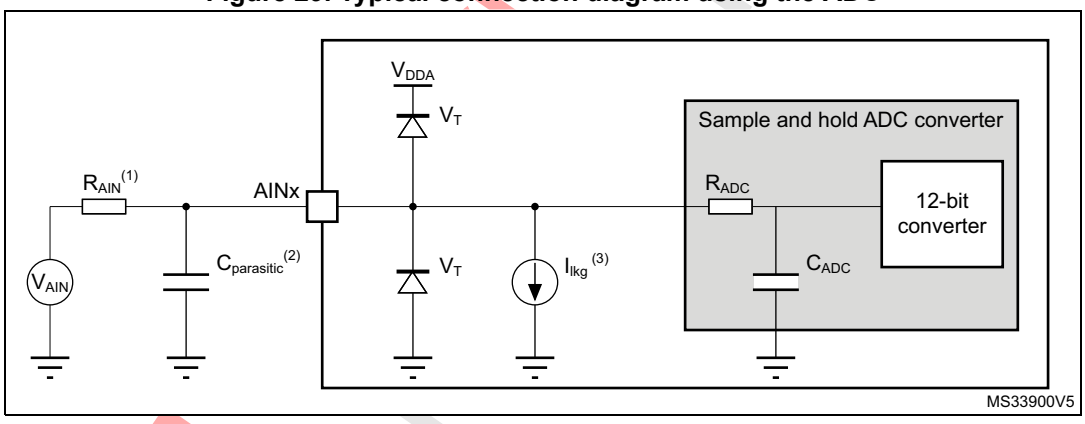


Figure 29. Typical connection diagram using the ADC



1. Refer to *Table 61: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 54: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 54: I/O static characteristics* for the values of I_{lkg}.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 16: Power supply scheme*. The decoupling capacitor on V_{DDA} should be ceramic (good quality) and it should be placed as close as possible to the chip.

5.3.19 Digital-to-Analog converter characteristics

Table 67. DAC 1MSPS characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	3.6	V
		Other modes		1.80	-		
V_{REF+}	Positive reference voltage	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	V_{DDA}	
		Other modes		1.80	-		
V_{REF-}	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} – 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

Table 67. DAC 1MSPS characteristics(1) (continued)

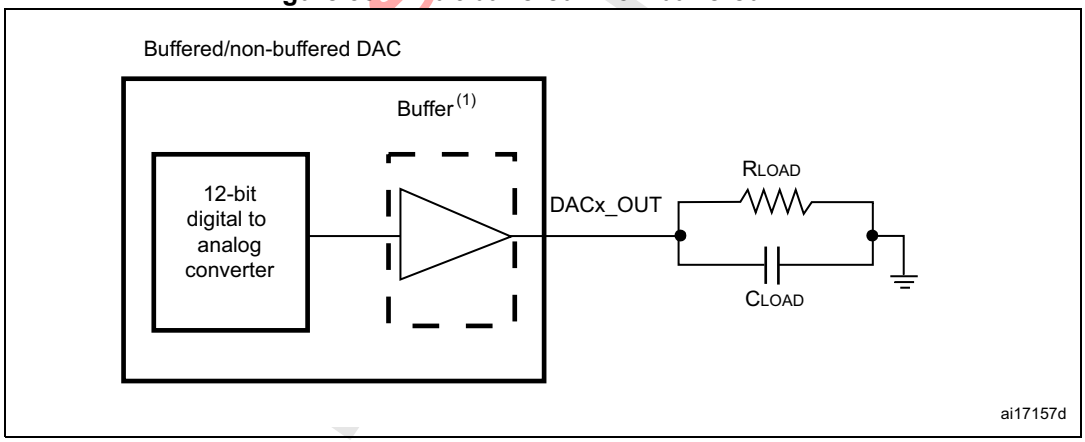
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W\_to\_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB) DAC_MCR:MODEx[2:0] = 000 or 001 DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 50 pF, RL ≥ 5 kΩ CL ≤ 10 pF		1 1.4	-	-	µs
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-(3)	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff) (4)	670 x Ton/(Ton +Toff) (4)	

Table 67. DAC 1MSPS characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x Ton/(Ton +Toff) (4)	400 x Ton/(Ton +Toff) (4)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x Ton/(Ton +Toff) (4)	205 x Ton/(Ton +Toff) (4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
3. Refer to *Table 54: I/O static characteristics*.
4. Ton is the Refresh phase duration. Toff is the Hold phase duration. Refer to RM0440 reference manual for more details.

Figure 30. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 68. DAC 1MSPS accuracy(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	DAC output buffer ON		TBD	TBD	TBD	LSB
		DAC output buffer OFF		TBD	TBD	TBD	
-	monotonicity	10 bits		TBD	TBD	TBD	
INL	Integral non linearity(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		TBD	TBD	TBD	
		DAC output buffer OFF CL ≤ 50 pF, no RL		TBD	TBD	TBD	
Offset	Offset error at code 0x800(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	TBD	TBD	TBD	
			V_{REF+} = 1.8 V	TBD	TBD	TBD	
		DAC output buffer OFF CL ≤ 50 pF, no RL		TBD	TBD	TBD	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF CL ≤ 50 pF, no RL		TBD	TBD	TBD	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	TBD	TBD	TBD	
			V_{REF+} = 1.8 V	TBD	TBD	TBD	
Gain	Gain error(5)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		TBD	TBD	TBD	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		TBD	TBD	TBD	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		TBD	TBD	TBD	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		TBD	TBD	TBD	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		TBD	TBD	TBD	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		TBD	TBD	TBD	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		TBD	TBD	TBD	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		TBD	TBD	TBD	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		TBD	TBD	TBD	

Table 68. DAC 1MSPS accuracy(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	TBD	TBD	TBD	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	TBD	TBD	TBD	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	TBD	TBD	TBD	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	TBD	TBD	TBD	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} – 0.2) V when buffer is ON.

Table 69. DAC 15MSPS characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	-	1.71	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.71	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}			
R_O	Output Impedance	-	TBD	TBD	TBD	kΩ
R_{BOFF}	Output impedance sample and hold mode	V_{DD} = 2.7 V	-	-	TBD	kΩ
		V_{DD} = 2.0 V	-	-	TBD	
C_L	Capacitive load	Sample and hold mode	-	TBD	TBD	µF
C_{SH}						
V_{DAC_OUT}	Voltage on DAC_OUT output	-	0	-	V_{REF+}	V
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode ±1LSB, CL = 10 pF	TBD	TBD	TBD	TBD
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode CL ≤ 10 pF	TBD	TBD	TBD	TBD
PSRR	V_{DDA} supply rejection ratio	Normal mode CL ≤ 50 pF, RL = 5 kΩ, DC	-	TBD	TBD	dB

Table 69. DAC 15MSPS characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{W\_to\_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB) DAC_MCR:MODEx[2:0] = 000 or 001 DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 50 pF, RL ≥ 5 kΩ CL ≤ 10 pF	TBD TBD	-	-	µs
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	-	-	TBD	TBD	µs
CI_{int}	Internal sample and hold capacitor	-	TBD	TBD	TBD	pF
t_{TRIM}	Middle code offset trim time	-	TBD	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V	-	TBD	-	µV
		V_{REF+} = 1.8 V	-	TBD	-	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	No load, middle code (0x800)	-	-	TBD	µA
		Sample and hold mode, C_{SH} = 100 nF	-	TBD	TBD	
I_{DDV}(DAC)	DAC consumption from V_{REF+}	No load, middle code (0x800)	-	TBD	TBD	
		Sample and hold mode, C_{SH} = 100 nF, worst case	-	TBD	TBD	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Table 70. DAC 15MSPS accuracy(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	-		TBD	TBD	TBD	LSB
-	monotonicity	10 bits		TBD	TBD	TBD	
INL	Integral non linearity(3)	CL ≤ 50 pF, no RL		TBD	TBD	TBD	
Offset	Offset error at code 0x800(3)	CL ≤ 50 pF, no RL		TBD	TBD	TBD	
Offset1	Offset error at code 0x001(4)	CL ≤ 50 pF, no RL		TBD	TBD	TBD	
OffsetCal	Offset Error at code 0x800 after calibration	CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	TBD	TBD	TBD	
			V_{REF+} = 1.8 V	TBD	TBD	TBD	
Gain	Gain error(5)	CL ≤ 50 pF, no RL		TBD	TBD	TBD	%
TUE	Total unadjusted error	CL ≤ 50 pF, no RL		TBD	TBD	TBD	LSB
TUECal	Total unadjusted error after calibration	CL ≤ 50 pF, RL ≥ 5 kΩ		TBD	TBD	TBD	LSB
SNR	Signal-to-noise ratio	CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		TBD	TBD	TBD	dB
THD	Total harmonic distortion	CL ≤ 50 pF, no RL, 1 kHz		TBD	TBD	TBD	dB
SINAD	Signal-to-noise and distortion ratio	CL ≤ 50 pF, no RL, 1 kHz		TBD	TBD	TBD	dB
ENOB	Effective number of bits	CL ≤ 50 pF, no RL, 1 kHz		TBD	TBD	TBD	bits

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF.

5.3.20 Voltage reference buffer characteristics

Table 71. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 00	TBD	TBD	TBD	V
			V_{RS} = 01	TBD	TBD	TBD	
			V_{RS} = 10	TBD	TBD	TBD	
		Degraded mode(2)	V_{RS} = 00	TBD	TBD	TBD	
			V_{RS} = 01	TBD	TBD	TBD	
			V_{RS} = 10	TBD	TBD	TBD	
V_{REFBUF_OUT}	Voltage reference output	Normal mode(3)	V_{RS} = 00	TBD	TBD	TBD	
			V_{RS} = 01	TBD	TBD	TBD	
			V_{RS} = 10	TBD	TBD	TBD	
		Degraded mode(2)	V_{RS} = 00	TBD	TBD	TBD	
			V_{RS} = 01	TBD	TBD	TBD	
			V_{RS} = 10	TBD	TBD	TBD	
V_{REFOUT_TEMP}(3)	Voltage reference output spread over the temperature range	V_{DDA} = 3V		-	-	TBD	mV
ΔV_{REFOUT_VDD}	Voltage reference output spread over the main supply VDD range	V_{DDA} = 3V		-	-	TBD	mV
TRIM	Trim step resolution	-	-	TBD	TBD	TBD	%
CL	Load capacitor	-	-	TBD	TBD	TBD	µF
esr	Equivalent Serial Resistor of Cload	-	-	TBD	TBD	TBD	Ω
I_{load}	Static load current	-	-	TBD	TBD	TBD	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	TBD	TBD	TBD	ppm/V
			I_{load} = 4 mA	TBD	TBD	TBD	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	TBD	TBD	TBD	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < TJ < +125 °C		TBD	TBD	TBD	ppm/ °C
		0 °C < TJ < +50 °C		TBD	TBD	TBD	
A_{Coeff}	Long-term stability	1000 hours, T= 25 °C		-	-	TBD	ppm
PSRR	Power supply rejection	DC		TBD	TBD	TBD	dB
		100 kHz		TBD	TBD	TBD	

Table 71. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{START}	Start-up time	CL = 0.5 µF(4)		TBD	TBD	TBD	µs
		CL = 1.1 µF(4)		TBD	TBD	TBD	
		CL = 1.5 µF(4)		TBD	TBD	TBD	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (5)	-	-	TBD	TBD	TBD	mA
I_{DDA}(VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA		TBD	TBD	TBD	µA
		I_{load} = 500 µA		TBD	TBD	TBD	
		I_{load} = 4 mA		TBD	TBD	TBD	
I_{VDD}	VREFBUF consumption from V_{DD}	I_{load} = 0 µA		TBD	TBD	TBD	µA
		I_{load} = 500 µA		TBD	TBD	TBD	
		I_{load} = 4 mA		TBD	TBD	TBD	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (VDDA - drop voltage).
3. Guaranteed by characterization results.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

5.3.21 Comparator characteristics

Table 72. COMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	TBD	TBD	TBD	V
V_{IN}	Comparator input voltage range	-	TBD	TBD	TBD	
V_{BG}(2)	Scaler input voltage	-	TBD	TBD	TBD	
V_{SC}	Scaler offset voltage	-	TBD	TBD	TBD	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)	TBD	TBD	TBD	nA
		BRG_EN=1 (bridge enable)	TBD	TBD	TBD	µA
t_{START_SCALER}	Scaler startup time	-	TBD	TBD	TBD	µs
t_{START}	Comparator startup time to reach propagation delay specification	V_{DDA} ≥ 2.7 V	TBD	TBD	TBD	µs
		V_{DDA} < 2.7 V	TBD	TBD	TBD	
t_D(3)	Propagation delay (From COMP input pin to COMP output pin) for 200 mV step with 100 mV overdrive	V_{DDA} ≥ 2.7 V (DEGLITCH = 0)	TBD	TBD	TBD	ns
		V_{DDA} ≥ 2.7 V (DEGLITCH = 1)	TBD	TBD	TBD	ns
		V_{DDA} < 2.7 V	TBD	TBD	TBD	
V_{offset}	Comparator offset error	Full common mode range	TBD	TBD	TBD	mV
V_{hys}	Comparator hysteresis	HYST[2:0] = 0	TBD	TBD	TBD	mV
		HYST[2:0] = 1	TBD	TBD	TBD	
		HYST[2:0] = 2	TBD	TBD	TBD	
		HYST[2:0] = 3	TBD	TBD	TBD	
		HYST[2:0] = 4	TBD	TBD	TBD	
		HYST[2:0] = 5	TBD	TBD	TBD	
		HYST[2:0] = 6	TBD	TBD	TBD	
		HYST[2:0] = 7	TBD	TBD	TBD	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Static	TBD	TBD	TBD	µA
		With 50 kHz ±100 mV overdrive square signal	TBD	TBD	TBD	
I_{bias}	Comparator input bias current	-	TBD	TBD	TBD (4)	nA

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 19: Embedded internal voltage reference*.
3. Guaranteed by characterization results.
4. Mostly I/O leakage when used in analog mode. Refer to I_{lkg} parameter in *Table 54: I/O static characteristics*.

5.3.22 Operational amplifiers characteristics

Table 73. OPAMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		TBD	TBD	TBD	V
CMIR	Common mode input range	-		TBD	TBD	TBD	V
VI_{OFFSET}(2)	Input offset voltage	25 °C, No Load on output.		TBD	TBD	TBD	mV
		All voltage/Temp.		TBD	TBD	TBD	
ΔVI_{OFFSET}	Input offset voltage drift	Normal mode		TBD	TBD	TBD	µV/°C
		High-speed mode		TBD	TBD	TBD	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1 x V_{DDA})	-		TBD	TBD	TBD	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9 x V_{DDA})	-		TBD	TBD	TBD	
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	TBD	TBD	TBD	µA
		High-speed mode		TBD	TBD	TBD	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	TBD	TBD	TBD	
		High-speed mode		TBD	TBD	TBD	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	TBD	TBD	TBD	kΩ
		High-speed mode		TBD	TBD	TBD	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	TBD	TBD	TBD	
		High-speed mode		TBD	TBD	TBD	
C_{LOAD}	Capacitive load	-		TBD	TBD	TBD	pF
CMRR	Common mode rejection ratio	Normal mode		TBD	TBD	TBD	dB
		High-speed mode		TBD	TBD	TBD	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	TBD	TBD	TBD	dB
		High-speed mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	TBD	TBD	TBD	

Table 73. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
GBW	Gain Bandwidth Product	Normal mode	V_{DDA} ≥ 2.4 V (OPA_RANGE = 1)	TBD	TBD	TBD	kHz
		High-speed mode		TBD	TBD	TBD	
		Normal mode	V_{DDA} < 2.4 V (OPA_RANGE = 0)	TBD	TBD	TBD	
		High-speed mode		TBD	TBD	TBD	
SR(2)	Slew rate (from 10 and 90% of output voltage)	Normal mode	V_{DDA} ≥ 2.4 V	TBD	TBD	TBD	V/ms
		High-speed mode		TBD	TBD	TBD	
		Normal mode	V_{DDA} < 2.4 V	TBD	TBD	TBD	
		High-speed mode		TBD	TBD	TBD	
AO	Open loop gain	Normal mode		TBD	TBD	TBD	dB
		High-speed mode		TBD	TBD	TBD	
V_{OHSAT}(2)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	TBD	TBD	TBD	mV
		High-speed mode		TBD	TBD	TBD	
V_{OLSAT}(2)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	TBD	TBD	TBD	
		High-speed mode		TBD	TBD	TBD	
φ_m	Phase margin	Normal mode		TBD	TBD	TBD	°
		High-speed mode		TBD	TBD	TBD	
GM	Gain margin	Normal mode		TBD	TBD	TBD	dB
		High-speed mode		TBD	TBD	TBD	
t_{WAKEUP}(2)	Wake up time from OFF state.	Normal mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ follower configuration	TBD	TBD	TBD	µs
		High-speed mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 20 kΩ follower configuration	TBD	TBD	TBD	
I_{bias}	OPAMP input bias current	-		TBD	TBD	TBD	nA

Table 73. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PGA gain(2)	Non inverting gain value	-	-	2	-	-
			-	4	-	
			-	8	-	
			-	16	-	
			-	32	-	
			-	64	-	
	Inverting gain value	-	-	-1	-	-
			-	-3	-	
			-	-7	-	
			-	-15	-	
			-	-31	-	
			-	-63	-	
$R_{network}$	R2/R1 internal resistance values in PGA mode(3)	PGA Gain = 2	TBD	TBD	TBD	kΩ/kΩ
		PGA Gain = 4	TBD	TBD	TBD	
		PGA Gain = 8	TBD	TBD	TBD	
		PGA Gain = 16	TBD	TBD	TBD	
		PGA Gain = 32	TBD	TBD	TBD	
		PGA Gain = 64	TBD	TBD	TBD	
		PGA Gain = -1	TBD	TBD	TBD	
		PGA Gain = -3	TBD	TBD	TBD	
		PGA Gain = -7	TBD	TBD	TBD	
		PGA Gain = -15	TBD	TBD	TBD	
		PGA Gain = -31	TBD	TBD	TBD	
		PGA Gain = -63	TBD	TBD	TBD	
Delta R	Resistance variation (R1 or R2)	-	TBD	TBD	TBD	%
PGA gain error	PGA gain error	-	TBD	TBD	TBD	%

Table 73. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	TBD	TBD	TBD	MHz
		Gain = 4	-	TBD	TBD	TBD	
		Gain = 8	-	TBD	TBD	TBD	
		Gain = 16	-	TBD	TBD	TBD	
		Gain = 32	-	TBD	TBD	TBD	
		Gain = 64	-	TBD	TBD	TBD	
	PGA bandwidth for different inverting gain	Gain = -1	-	TBD	TBD	TBD	MHz
		Gain = -3	-	TBD	TBD	TBD	
		Gain = -7	-	TBD	TBD	TBD	
		Gain = -15	-	TBD	TBD	TBD	
		Gain = -31	-	TBD	TBD	TBD	
		Gain = -63	-	TBD	TBD	TBD	
eN	Voltage noise density	Normal mode	at 1 kHz, Output loaded with 4 kΩ	TBD	TBD	TBD	nV/√Hz
		High-speed mode	at 1 kHz, Output loaded with 20 kΩ	TBD	TBD	TBD	
		Normal mode	at 10 kHz, Output loaded with 4 kΩ	TBD	TBD	TBD	
		High-speed mode	at 10 kHz, Output loaded with 20 kΩ	TBD	TBD	TBD	
I_{DDA}(OPAMP)(2)	OPAMP consumption from VDDA	Normal mode	no Load, quiescent mode	TBD	TBD	TBD	µA
		High-speed mode		TBD	TBD	TBD	

1. Guaranteed by design, unless otherwise specified.
2. Guaranteed by characterization results.
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain =1+R2/R1

5.3.23 Temperature sensor characteristics

Table 74. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	TBD	TBD	TBD	°C
Avg_Slope(2)	Average slope	TBD	TBD	TBD	mV/°C
V_{30}	Voltage at 30°C (±5 °C)(3)	TBD	TBD	TBD	V
t_{START} (TS_BUF)(1)	Sensor Buffer Start-up time in continuous mode(4)	TBD	TBD	TBD	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	TBD	TBD	TBD	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	TBD	TBD	TBD	µs
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by ADC	TBD	TBD	TBD	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 4: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

5.3.24 V_{BAT} monitoring characteristics

Table 75. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	TBD	TBD	TBD	kΩ
Q	Ratio on V_{BAT} measurement	TBD	3	TBD	-
Er(1)	Error on Q	TBD	TBD	TBD	%
t_{S_vbat}(1)	ADC sampling time when reading the VBAT	TBD	TBD	TBD	µs

1. Guaranteed by design.

Table 76. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	TBD	5	TBD	kΩ
		VBRS = 1	TBD	1.5	TBD	

5.3.25 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 5.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 77. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 170 MHz	6.66	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 170 MHz	0	75	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2 and TIM5)	-	16	bit
		TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 170 MHz	0.00666	436.9	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 170 MHz	-	28.63	s
f_{ENC}	Encoder frequency on TI1 and TI2 input pins	-	0	$f_{TIMxCLK}/4$	MHz
		$f_{TIMxCLK}$ = 170MHz	0	37.5	MHz
$t_{W(INDEX)}$	Index pulsewidth on ETR input	-	2	-	Tck
$t_{W(TI1, TI2)}$	Min pulsewidth on TI1 and TI2 inputs in all encoder modes except directional clock x1	-	2	-	Tck
	Min pulsewidth on TI1 and TI2 inputs in directional clock x1	-	3	-	Tck

1. TIMx is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16, 17 or 20.

Table 78. IWDG min/max timeout period at 32 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 79. WWDG min/max timeout value at 170 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0241	1.542	ms
2	1	0.0482	3.084	
4	2	0.0964	6.168	
8	3	0.1928	12.336	

5.3.26 Communication interfaces characteristics

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0440 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 5.3.14: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to *Table 80* below for the analog filter characteristics:

Table 80. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in *Table 81* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 16: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 81. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2.7 V < V_{DD} < 3.6 V Voltage Range V1	-	-	75	MHz
		Master mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1			50	
		Master transmitter mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1			50	
		Slave receiver mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1			50	
		Slave mode transmitter/full duplex 2.7 V < V_{DD} < 3.6 V Voltage Range V1			41	
		Slave mode transmitter/full duplex 1.71 V < V_{DD} < 3.6 V Voltage Range V1			27	
		1.71 V < V_{DD} < 3.6 V Voltage Range V2			13	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	4*T_{pclk}	-	-	-
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	2*T_{pclk}	-	-	-

Table 81. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{pclk}-1	T_{pclk}	T_{pclk}+1	-
$t_{su(MI)}$	Data input setup time	Master mode	4	-	-	ns
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	-	ns
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	ns
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V < V_{DD} < 3.6 V Voltage Range V1	-	9	12	ns
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1	-	9	18	
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range V2	-	13	22	
$t_{v(MO)}$		Master mode	-	3.5	4.5	
$t_{h(SO)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	6	-	-	
		Slave mode Range V2	9	-	-	
$t_{h(MO)}$		Master mode	2	-	-	

1. Guaranteed by characterization results.
2. The maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high-phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.

Figure 31. SPI timing diagram - slave mode and CPHA = 0

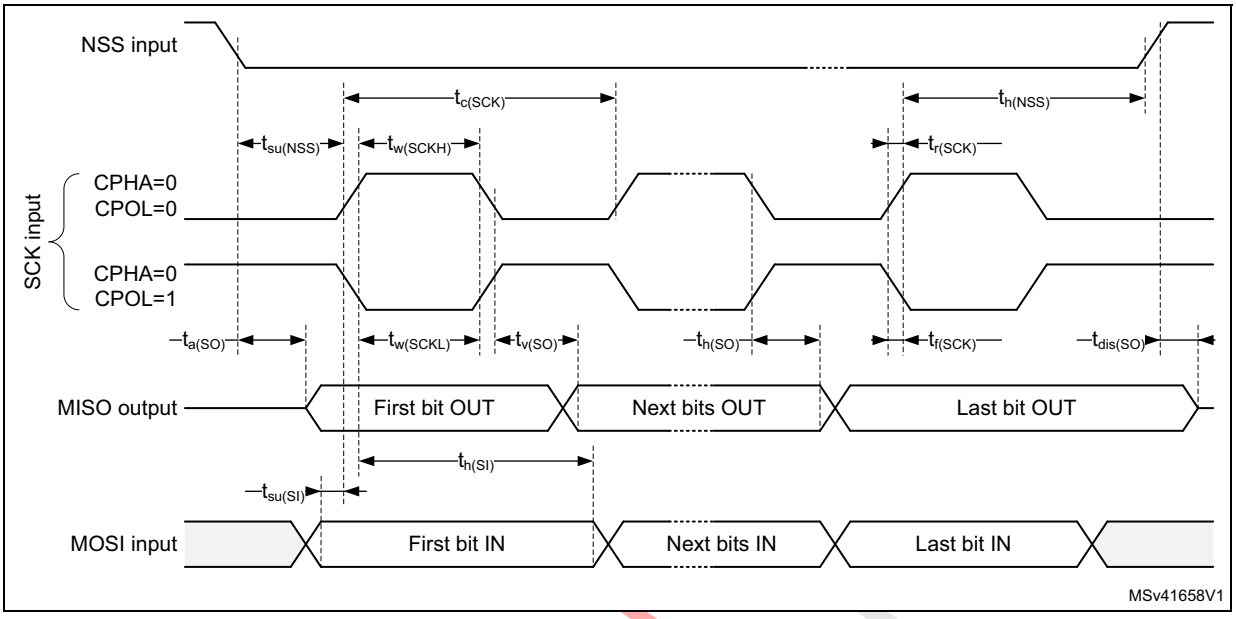
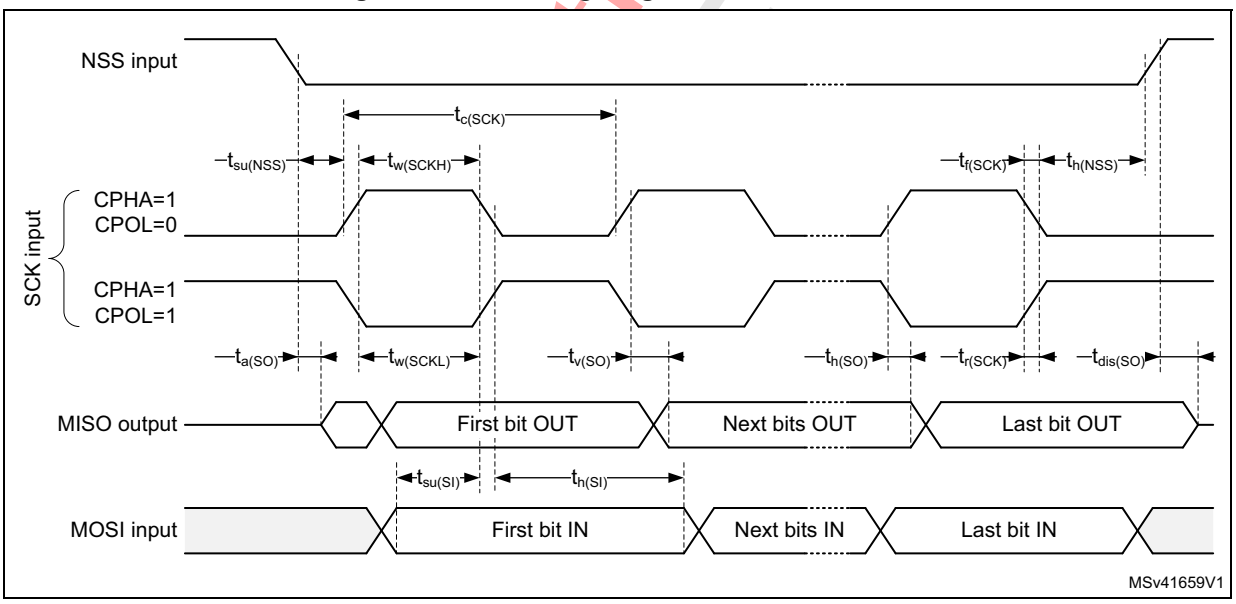
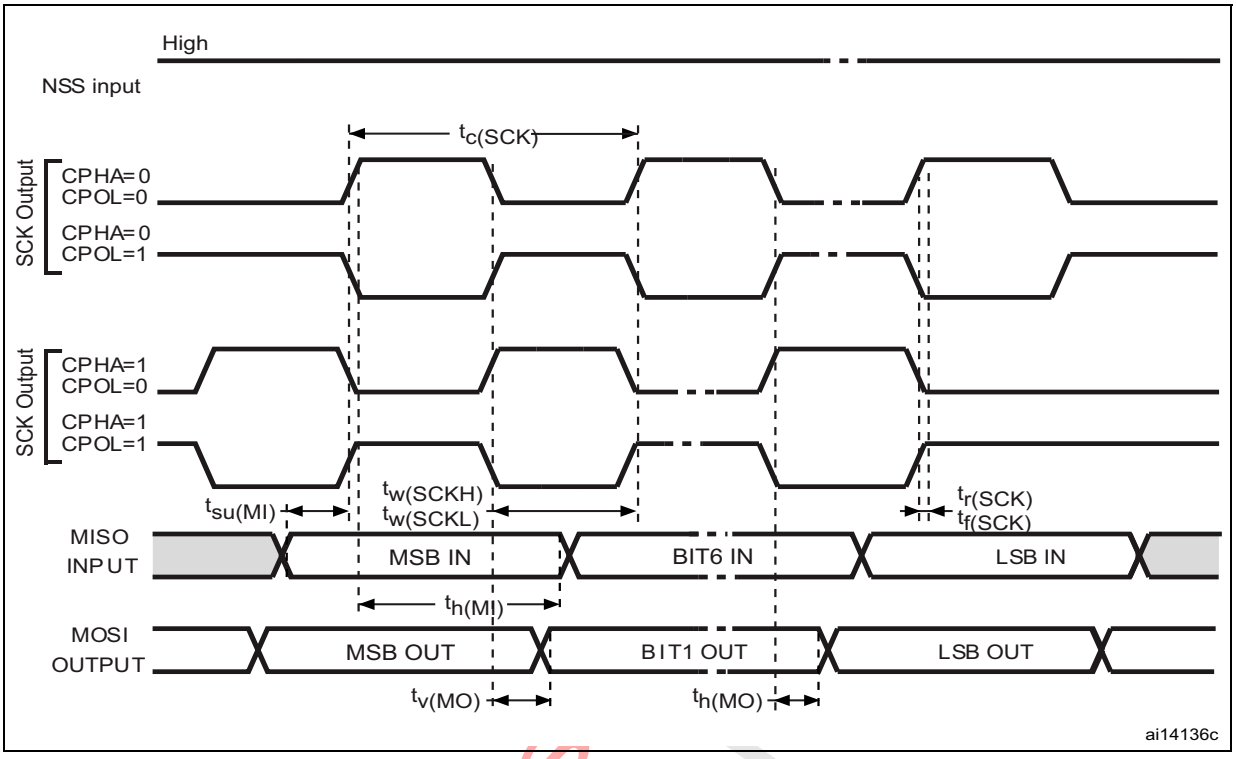


Figure 32. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 33. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 82* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 82. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	TBD	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	TBD	33	MHz
		Master transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	TBD	22	
		Master receiver Voltage Range 1	TBD	22	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	TBD	45	
		Slave transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	TBD	29	
		Slave receiver Voltage Range 1	TBD	50	
		Slave transmitter Voltage Range 2	TBD	13	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	TBD	15	ns
		Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V	TBD	22	
$t_{h(FS)}$	FS hold time	Master mode	10	TBD	ns
$t_{su(FS)}$	FS setup time	Slave mode	2	TBD	ns
$t_{h(FS)}$	FS hold time	Slave mode	1	TBD	ns
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	2.5	TBD	ns
$t_{su(SD\_B\_SR)}$		Slave receiver	1	TBD	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	5	TBD	ns
$t_{h(SD\_B\_SR)}$		Slave receiver	1	TBD	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	TBD	11	ns
		Slave transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	TBD	17	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	TBD	ns
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	TBD	14	ns
		Master transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	TBD	21	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	TBD	ns

1. Guaranteed by characterization results.

2. APB clock frequency must be at least twice SAI clock frequency.

Figure 34. SAI master timing waveforms

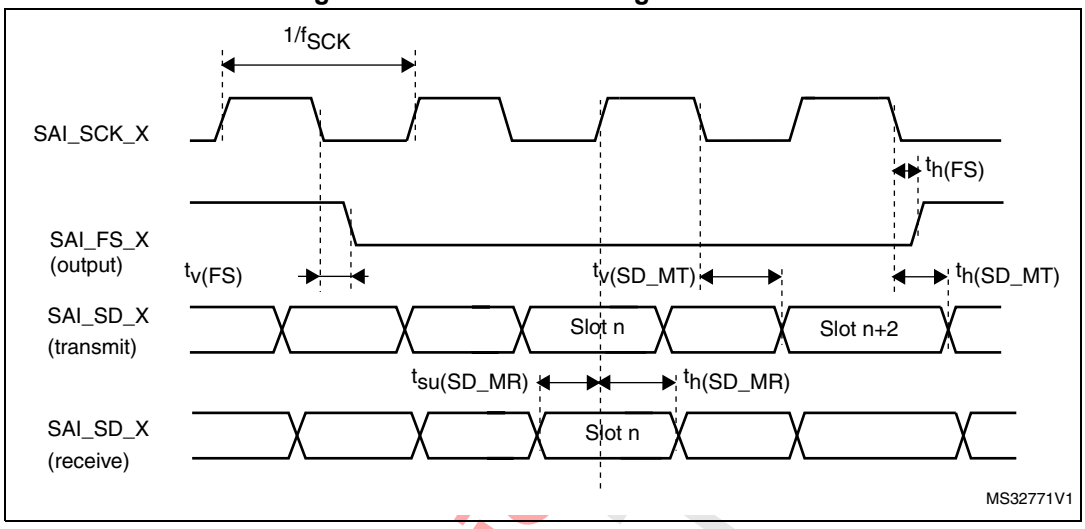
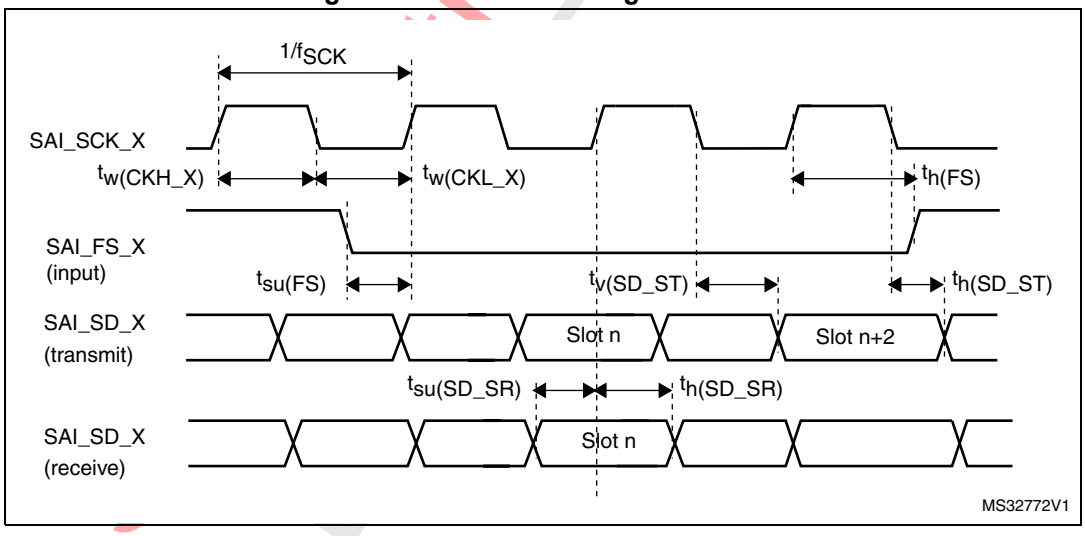


Figure 35. SAI slave timing waveforms



CAN (controller area network) interface

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (FDCANx_TX and FDCANx_RX).

USB characteristics

The device USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-sp[eed device operation).

Table 83. USB electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	USB transceiver operating voltage		3.0(2)	-	3.6	V
$t_{Crystal\_less}$	USB crystal less operation temperature		-15	-	85	°C
R_{PUI}	Embedded USB_DP pull-up value during idle		900	1250	1500	Ω
R_{PUR}	Embedded USB_PD pull-up value during reception		1400	2300	3200	
Z_{sDRV}(3)	Output driver impedance(4)	Driving high and low	28	36	44	Ω

1. TA = -40 to 125 °C unless otherwise specified.
2. The device USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics, which are degraded in the 2.7-to-3.0 V voltage range.
3. Guarantee by design..
4. No external termination series resistors are required on USB_PD (D+) and USB_DM (D-); the matching impedence is already included in the embedded driver.

5.3.27 UCPD characteristics

UCPD1 controller complies with USB Type-C Rev.1.2 and USB Power Delivery Rev. 3.0 specifications.

Table 84. UCPD characteristics

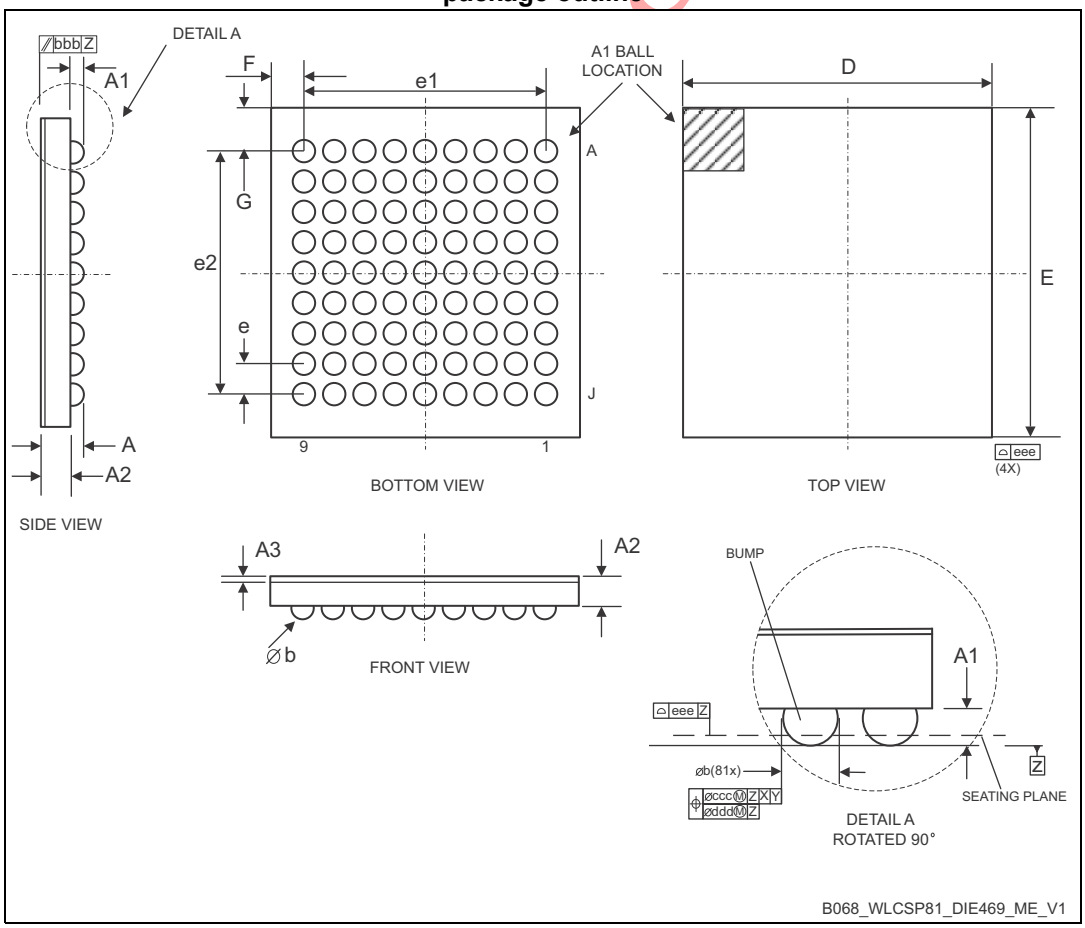
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	UCPD operating supply voltage	Sink mode only	TBD	TBD	TBD	V
		Sink and source mode	TBD	TBD	TBD	V

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 WLCSP81 package information

Figure 36. WLCSP - 81 balls, 4.02x4.27 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 85. WLCSP - 81 balls, 4.02x4.27 mm, 0.4 mm pitch wafer level chip scale mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025	-	-	0.001	-
b	0.22	0.25	0.28	0.009	0.010	0.011
D	4.00	4.02	4.04	0.157	0.158	0.159
E	4.25	4.27	4.29	0.167	0.168	0.169
e	-	0.40	-	-	0.016	-
e1	-	3.20	-	-	0.126	-
e2	-	3.20	-	-	0.126	-
F[3]	-	0.410	-	-	0.016	-
G[3]	-	0.535	-	-	0.021	-
aaa	-	-	0.10	-	-	0.004
bbb	-	-	0.10	-	-	0.004
ccc	-	-	0.10	-	-	0.004
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 3 decimal digits.
2. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal and tolerances values of A1 and A2.
3. Calculated dimensions are rounded to the 3rd decimal place

Figure 37. WLCSP - 81 balls, 4.02x4.27 mm, 0.4 mm pitch wafer level chip scale recommended footprint

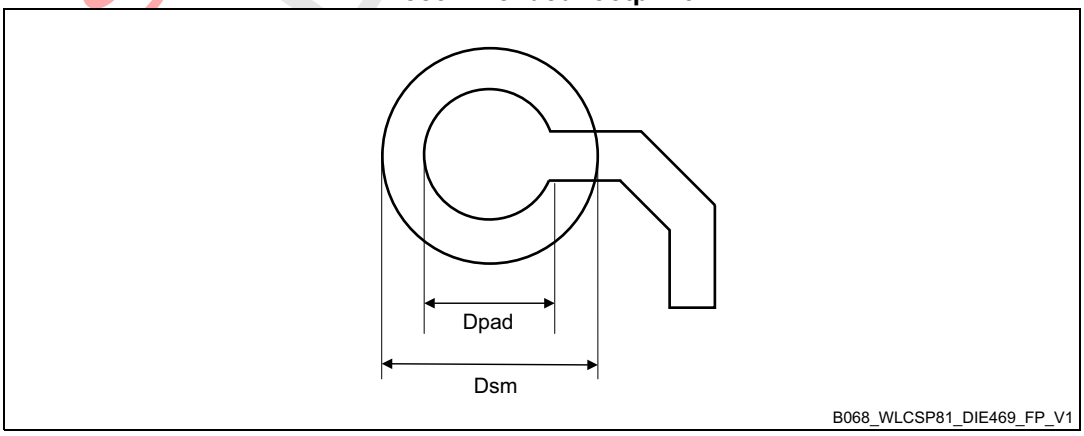
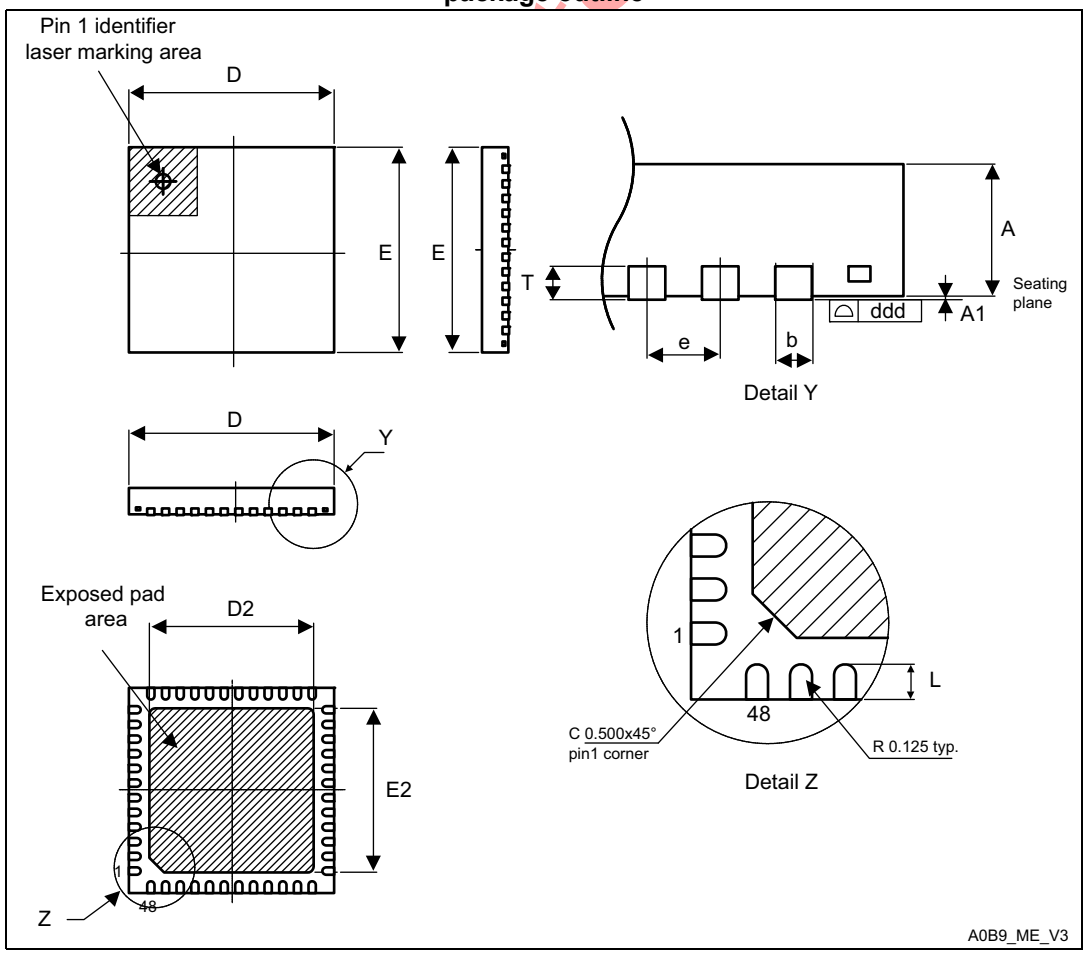


Table 86. WLCSP81 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0,225 mm
Dsm	0.290 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

6.2 UFQFPN48 package information

Figure 38. UFQFPN - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



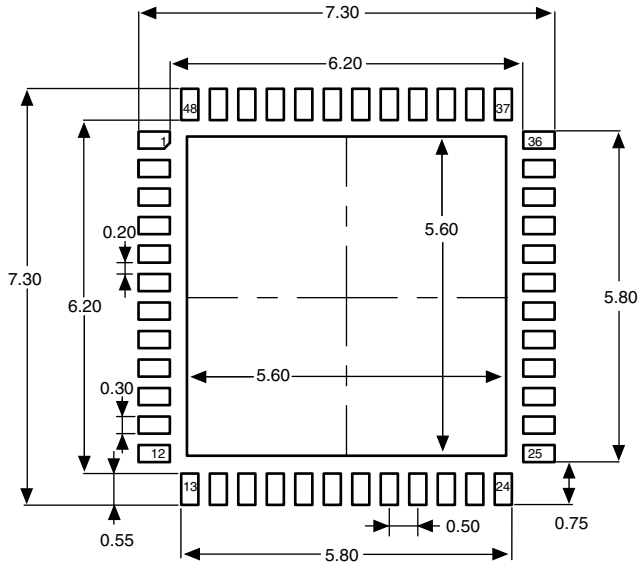
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 87. UFQFPN - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

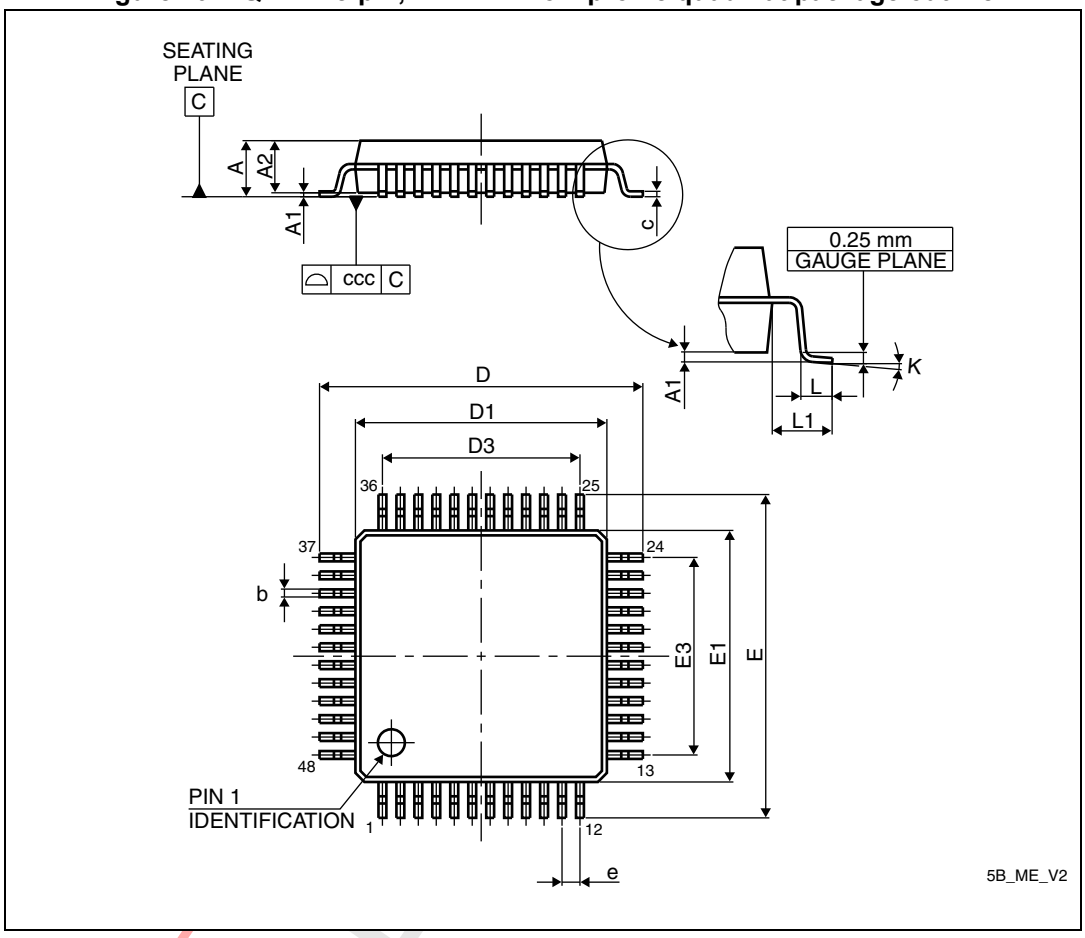
Figure 39. UFQFPN - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.3 LQFP48 package information

Figure 40. LQFP - 48-pin, 7 x 7 mm low-profile quad flat package outline



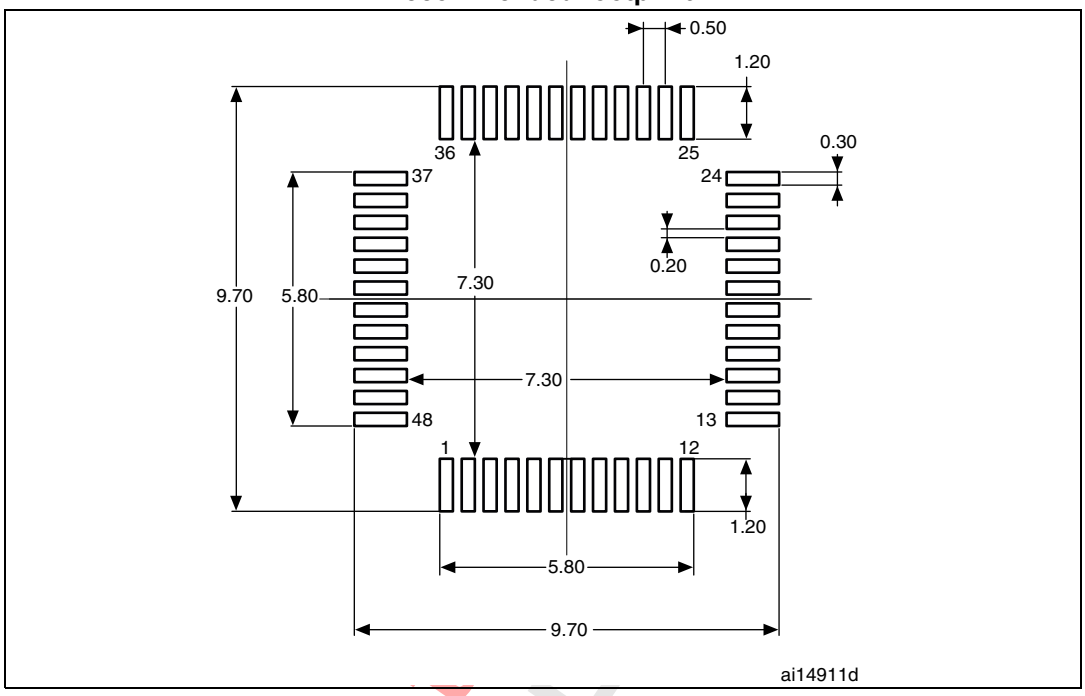
1. Drawing is not to scale.

Table 88. LQFP - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

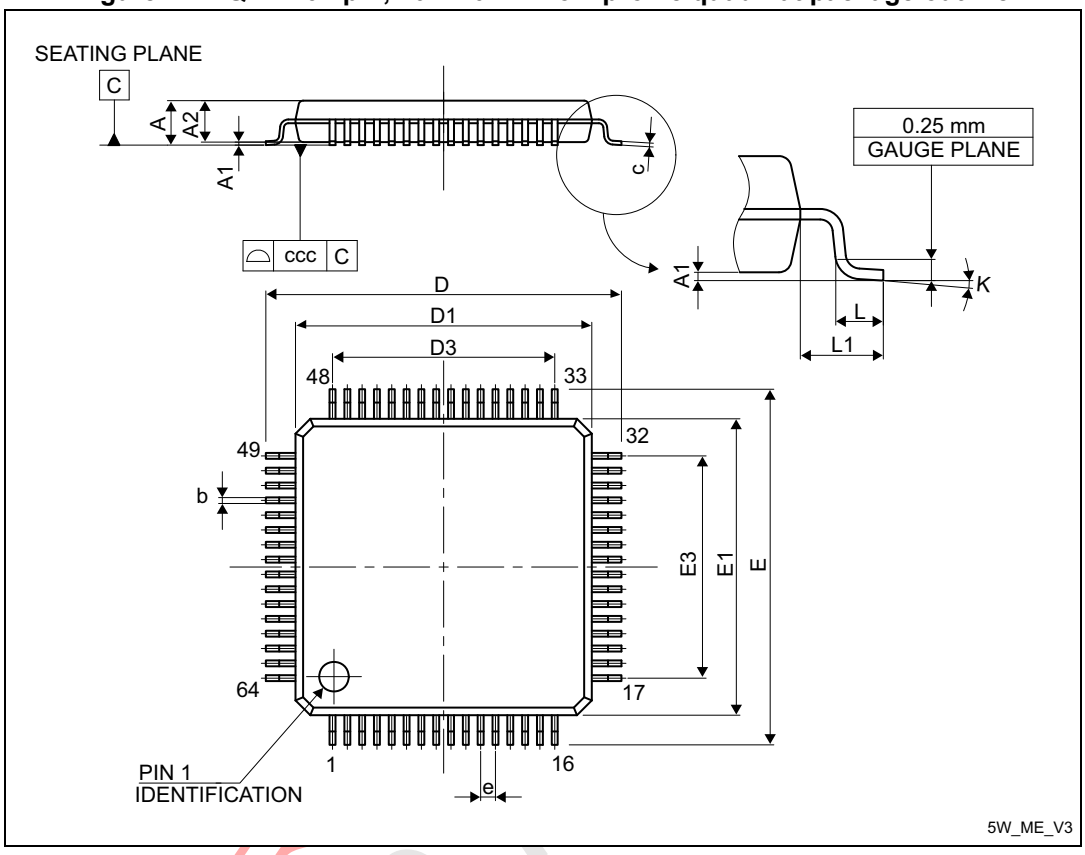
Figure 41. LQFP - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.4 LQFP64 package information

Figure 42. LQFP - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 89. LQFP - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

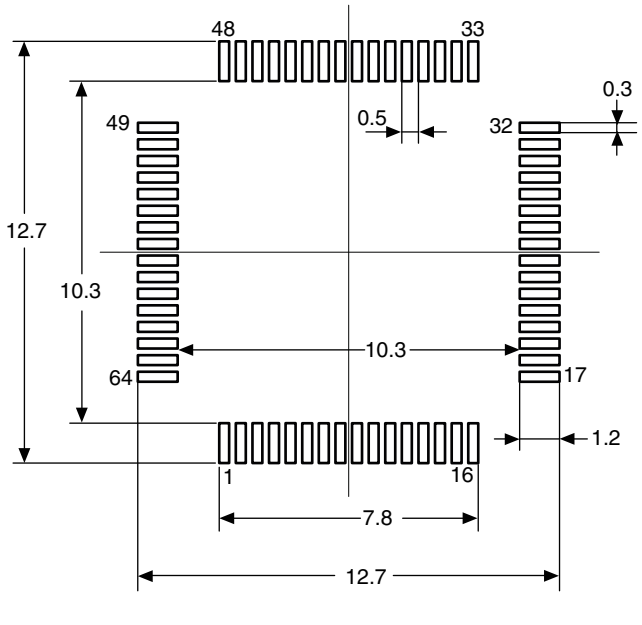
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 89. LQFP - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

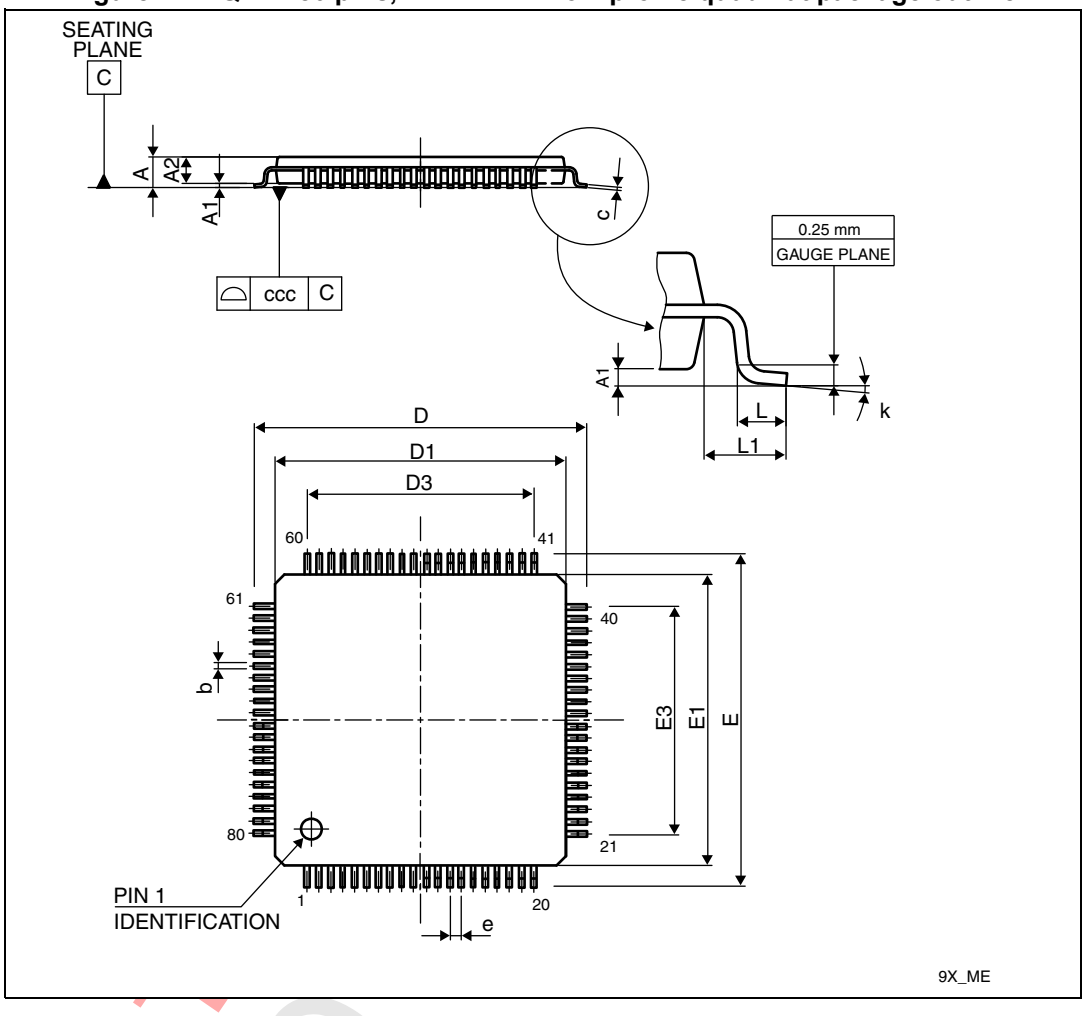
Figure 43. LQFP - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.5 LQFP80 package information

Figure 44. LQFP - 80 pins, 12 x 12 mm low-profile quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 90. LQFP - 80 pins, 12 x 12 mm low-profile quad flat package mechanical data

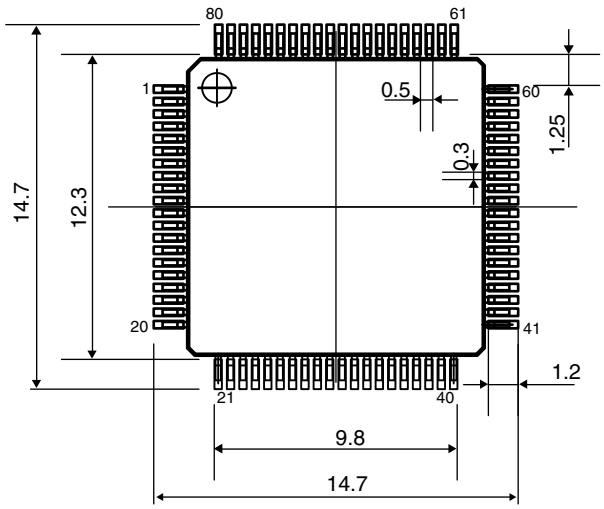
Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079

Table 90. LQFP - 80 pins, 12 x 12 mm low-profile quad flat package mechanical data (continued)

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	-	14.000	-	-	0.5512	-
D1	-	12.000	-	-	0.4724	-
D2	-	9.500	-	-	0.3740	-
E	-	14.000	-	-	0.5512	-
E1	-	12.000	-	-	0.4724	-
E3	-	9.500	-	-	0.3740	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031
k	0.0°	-	7.0°	0.0°	-	7.0°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45. LQFP - 80 pins, 12 x 12 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.6 TFBGA100 package information

Figure 46. TFBGA - 100 - ball, 8X8 mm, 0.8 mm pitch fine pitch ball grid array package outline

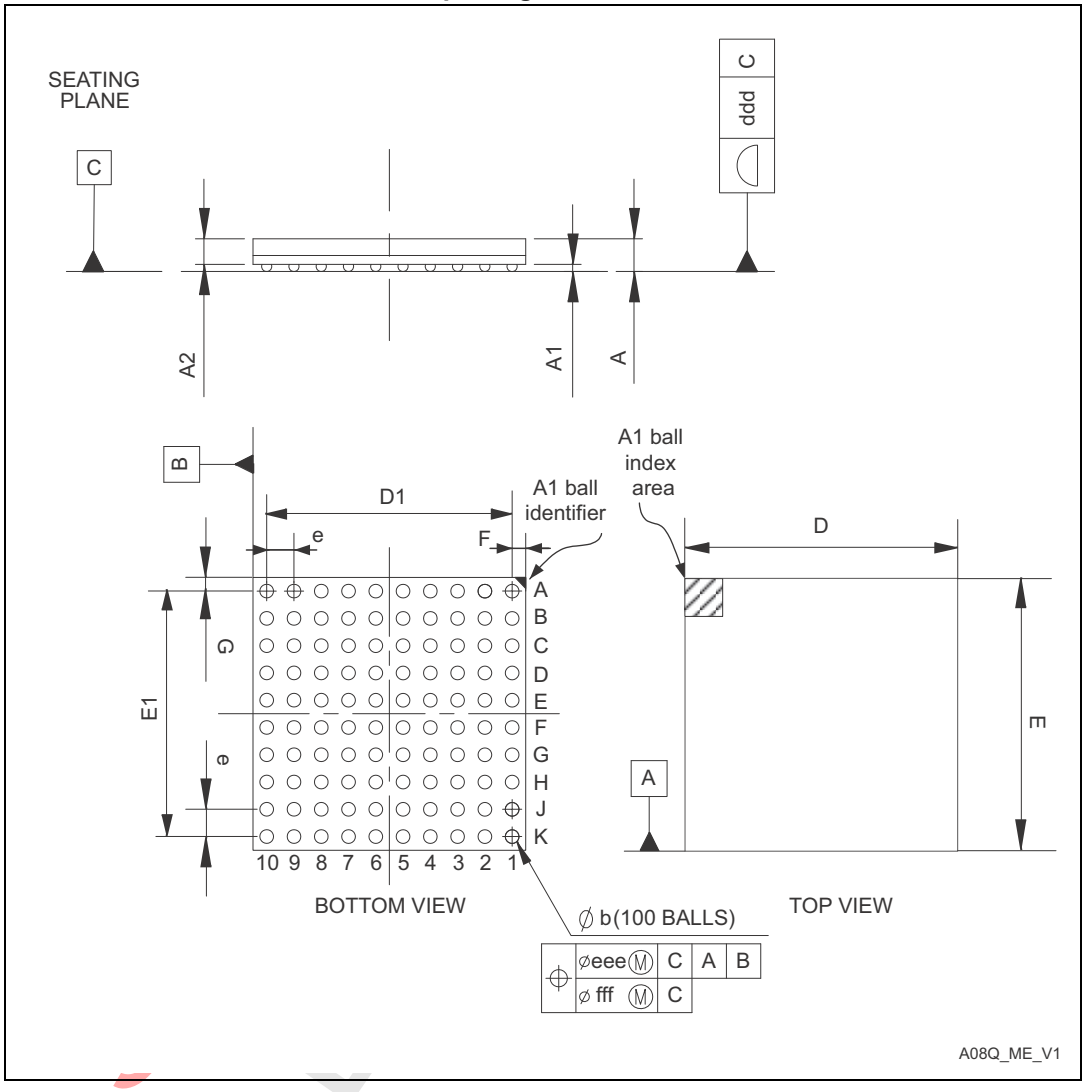
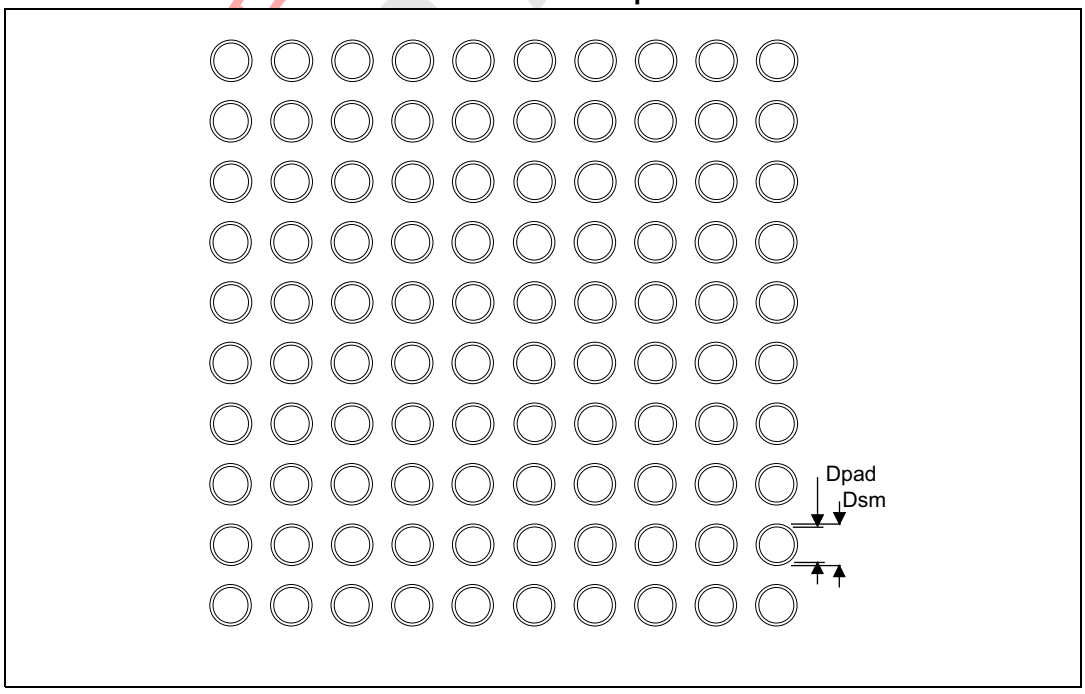


Table 91. TFBGA - 100 - ball, 8X8 mm, 0.8 mm pitch fine pitch ball grid array mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	7.850	8.000	8.150	0.3091	0.3150	0.3209
D1	-	7.200		-	0.2835	-
E	7.850	8.000	8.150	0.3091	0.3150	0.3209
E1	-	7.200	-	-	0.2835	-
e	-	0.800	-	-	0.0315	-
F	-	0.400	-	-	0.0157	-
G	-	0.400	-	-	0.0157	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47. TFBGA - 100 - ball, 8X8 mm, 0.8 mm pitch fine pitch ball grid array recommended footprint



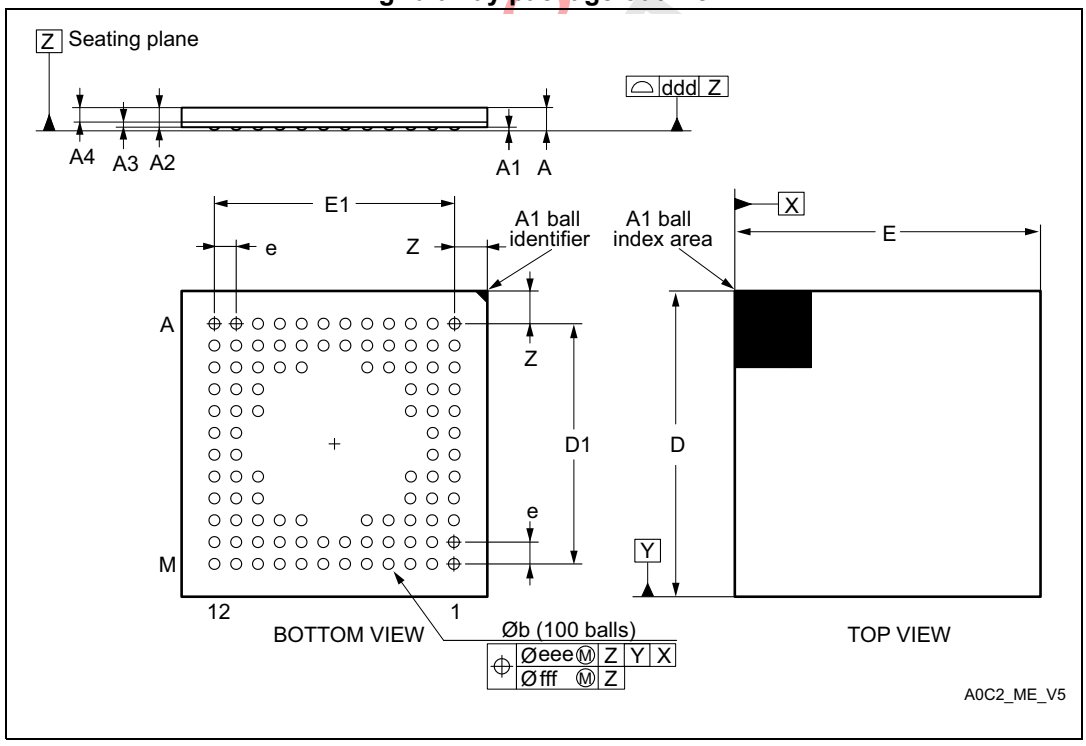
1. Dimensions are expressed in millimeters.

Table 92. TFBGA 100 recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

6.7 UFBGA100 package information

Figure 48. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 93. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043

Table 93. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

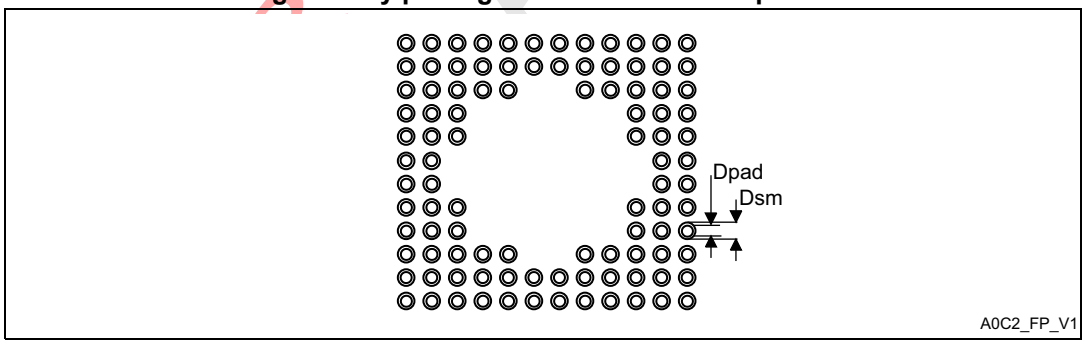
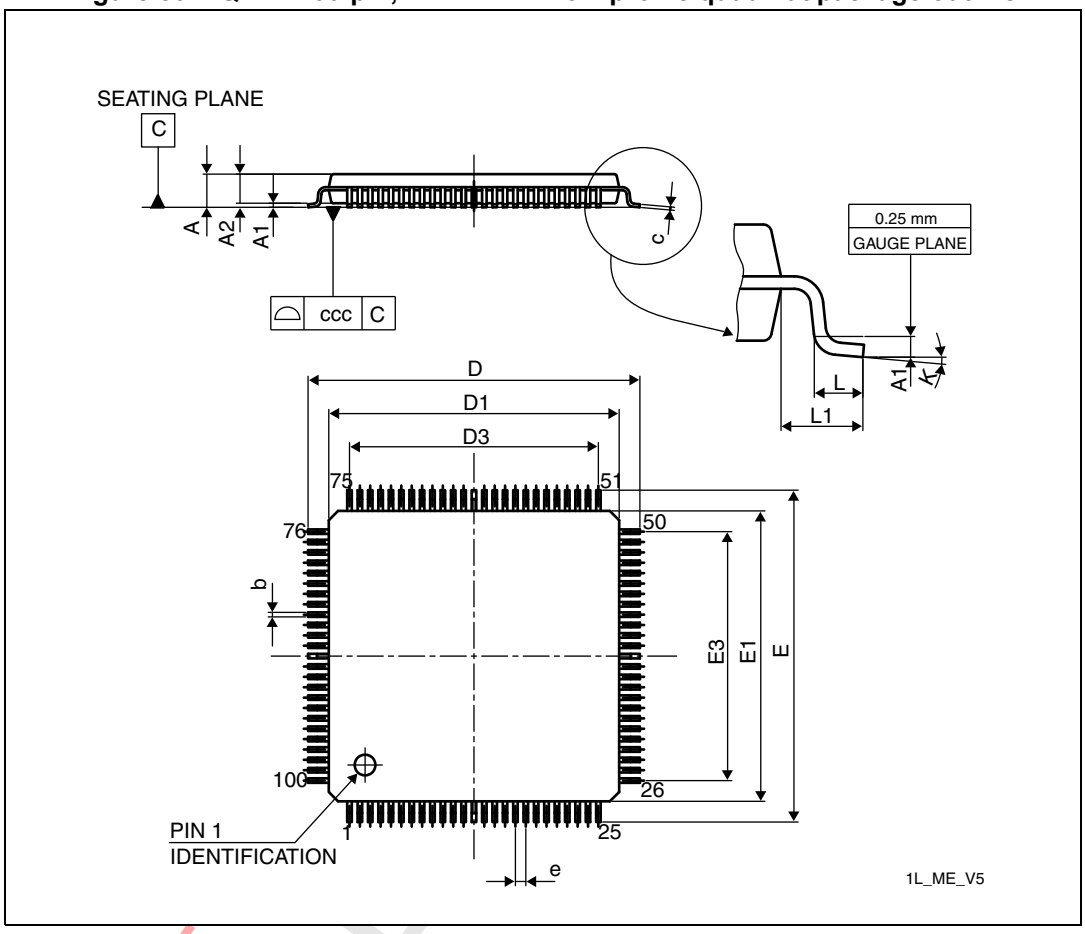


Table 94. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the solder mask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

6.8 LQFP100 package information

Figure 50. LQFP - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 95. LQPF - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

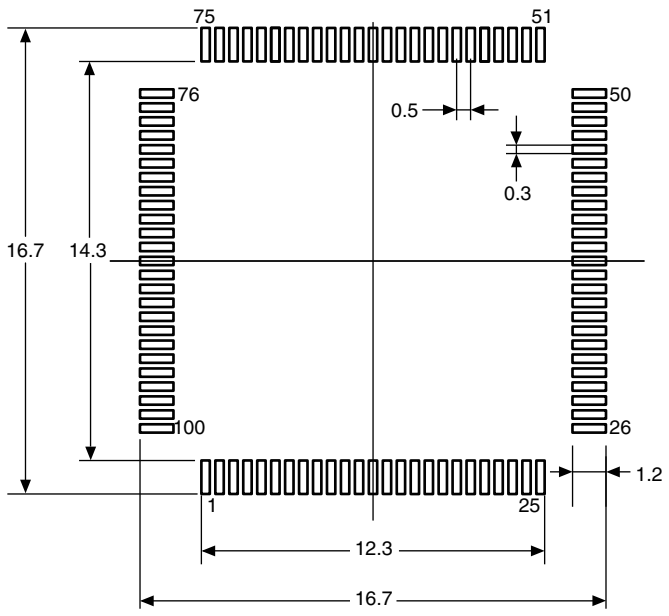
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 95. LQPF - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

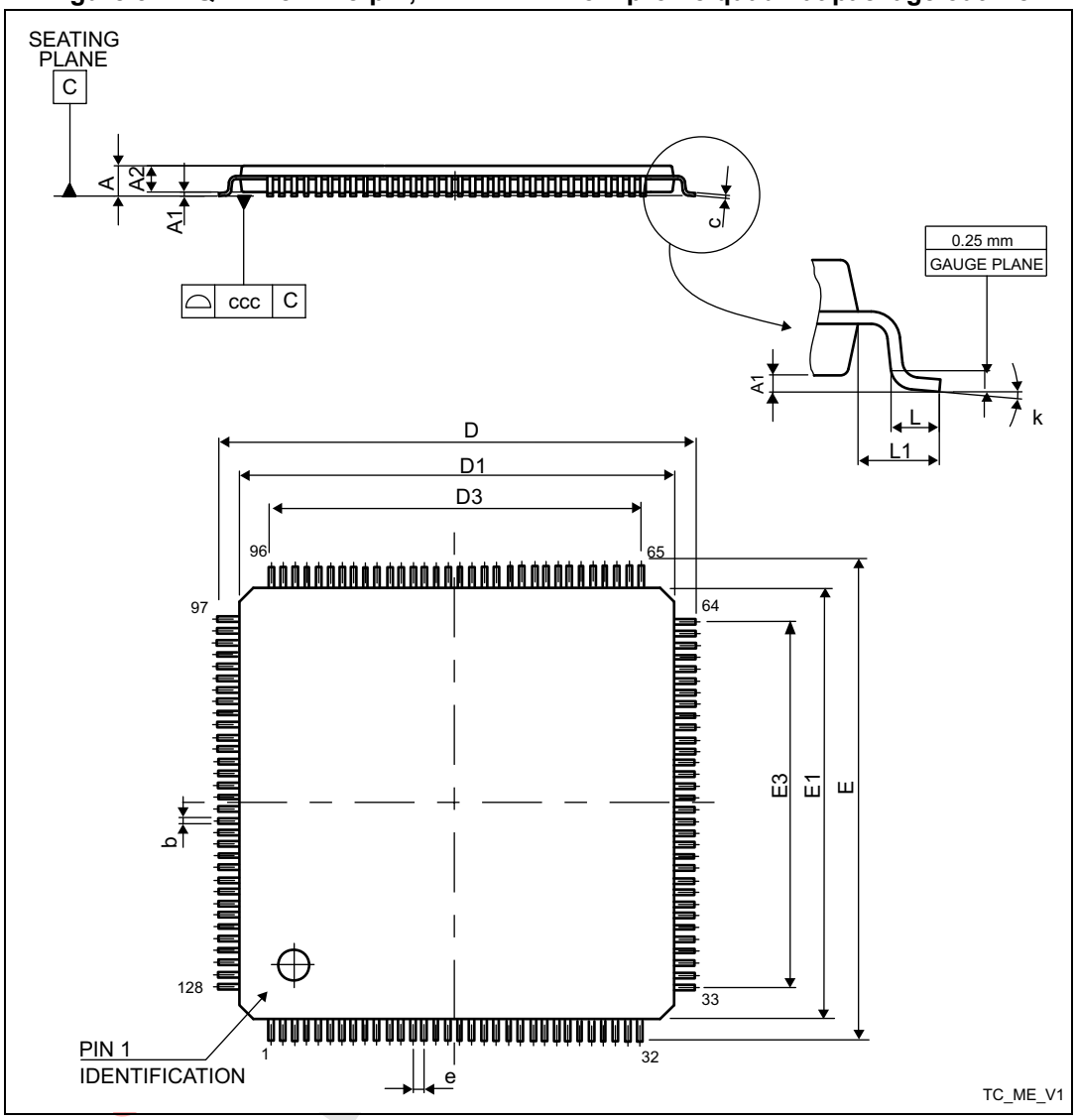
Figure 51. LQFP - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

6.9 LQFP128 package information

Figure 52. LQFP128 - 128-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 96. LQFP128 - 128-pin, 14 x 14 mm low-profile quad flat package mechanical data

Ref.	Dimensions					
	Millimeters			Inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 96. LQFP128 - 128-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b	0.130	0.180	0.230	0.0051	0.0071	0.0091
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.400	-	-	0.4882	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.400	-	-	0.4882	-
e	-	0.400	-	-	0.0157	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.10 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ ((V_{DDIOx} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 97. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP128 - 14 × 14 mm	TBD	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	TBD	
	Thermal resistance junction-ambient LQFP80 - 12 × 12 mm	TBD	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm	TBD	
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	TBD	
	Thermal resistance junction-ambient UFBGA100 - 7 × 7 mm	TBD	
	Thermal resistance junction-ambient TFBGA100 - 8 × 8 mm	TBD	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	TBD	
	Thermal resistance junction-ambient WLCSP81 - 4.02 X 4.27 mm	TBD	

6.10.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

6.10.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 7: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32G471xE at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 82 °C + (42 °C/W × 447 mW) = 82 °C + 18.774 °C = 100.774 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 7: Ordering information*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 7: Ordering information*).

Note: With this given P_{Dmax} we can find the TAmax allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 105-18.774 = 86.226 °C

Suffix 3: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 130-18.774 = 111.226 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 100 °C + (42 °C/W × 134 mW) = 100 °C + 5.628 °C = 105.628 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 3 (see *Section 7: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

7 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact the nearest ST sales office.

Table 98. Ordering information

Example: STM32 G 471 V E T 6 x

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

G = General-purpose

Sub-family

471 = STM32G471xx

Pin count

C = 48 pins
R = 64 pins
M = 80 pins, 81 pins
V = 100 pins
Q = 128 pins

Code size

C = 256 Kbyte
E = 512 Kbyte

Package

H = TFBGA
T = LQFP
U = UFQFPN
Y = WLCSP

Temperature range

6 = Industrial temperature range, - 40 to 85 °C (105 °C junction)
7 = Industrial temperature range, - 40 to 105 °C (125 °C junction)
3 = Industrial temperature range, - 40 to 125 °C (130 °C junction)

Options

xxx = programmed parts
TR = tape and reel

8 Revision history

Table 99. Document revision history

Date	Revision	Changes
08-Nov-2018	0.1	Initial release.