

Evaluation board with STM32L552E MCU

Introduction

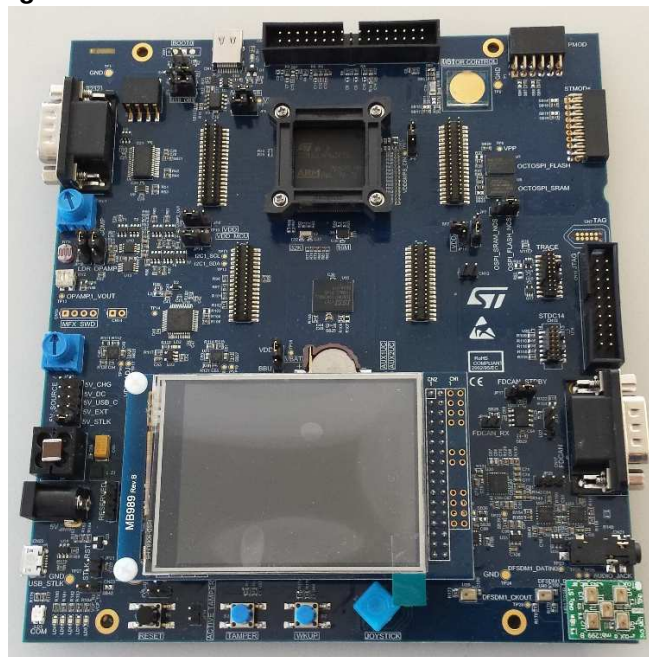
The STM32L552E-EVAL evaluation board is designed as complete demonstration and development platform for STMicroelectronics ARM® Cortex®-M4 core-based STM32L552ZET6Q microcontroller with 256-Kbytes internal SRAM and 512-Kbytes internal Flash memory, one Flexible memory controller (FMC) interface, one Octo SPI memory interface, one LCD-TFT controller, one RTC, up to 16 timers, one USB Type C Device FS port with UCPD controller, two SAI ports, four I²C buses, six USART ports, three SPI, one CANFD port, one SDMMC interface, 2x 12-bit ADC, 2x 12-bit DAC, 2 low power comparator, 4 digital filter for Sigma Delta modulator, up to 24 capacitive touch-sensing, an embedded step down converter, and JTAG and ETM debugging support.

STM32L552E-EVAL, shown in [Figure 1](#), is used as reference design for user application development, although it is not considered as final application.

The full range of hardware features on the board helps user to evaluate all the peripherals (USB, USART, digital microphones, ADC and DAC, TFT LCD, LDR, SRAM, Octo SPI Flash memory device, Octo SPI SRAM device, microSD card, sigma-delta modulators, CAN transceiver, EEPROM) and develop applications. Extension headers allow easy connection of a daughter board or wrapping board for a specific application.

An ST-LINK/V2-1 is integrated on the board, as embedded in-circuit debugger and programmer for the STM32 MCU and the USB virtual COM port bridge

Figure 1. STM32L552E-EVAL evaluation board



Contents

Contents	2
List of tables	5
List of figures	7
1 Overview	8
1.1 Demonstration software	9
1.2 Order code	9
1.3 Unpacking recommendations	9
1.4 Conventions	9
2 Hardware Layout and configuration	10
2.1 ST-LINK/V2-1	12
2.1.1 Drivers	13
2.1.2 ST-LINK/V2-1 firmware upgrade	13
2.2 ETM trace	14
2.2.1 IO restriction to other features	15
2.3 JTAG Connector	16
2.3.1 IO restriction to other features	17
2.4 STDC14 Connector	18
2.4.1 IO restriction to other features	19
2.5 TAG Footprint	19
2.5.1 IO restriction to other features	20
2.6 Power Supply	21
2.6.1 5V power supply general view.	21
2.6.2 5V_ST_LINK power source	22
2.6.3 5V_EXT power source	23
2.6.4 5V_USB_TYPE C power source	24
2.6.5 5V_DC power source	25
2.6.6 5V_USB_CHARGER power source	26
2.6.7 Programing/debugging when the power supply is not from ST-LINK (5V_STLK)	27
2.6.8 External power Supply Output	28
2.6.9 Internal Power supply	28
2.7 Clock references	31
2.8 Reset Source	32
2.9 Boot Option	32
2.10 Audio	33
2.10.1 Operating voltage.	33
2.10.2 Audio Codec interface	33
2.10.3 Digital microphones	33
2.10.4 Headphones outputs	34
2.10.5 Audio Jack connector	34
2.10.6 IO restriction to other features	35
2.11 USB TYPE C FS port	36
2.11.1 Operating voltage.	36
2.11.2 USB FS device	36
2.11.3 UCPD	36
2.11.4 USB TYPE C connector	37
2.11.5 IO restriction to other features	37
2.12 RS-232 port	39
2.12.1 Operating voltage.	39
2.12.2 RS-232 interface	39
2.12.3 IO restriction to other features	40
2.13 microSD card	41
2.13.1 Operating voltage.	41
2.13.2 SD card interface	41
2.13.3 IO restriction to other features	42
2.14 FDCAN	43
2.14.1 Operating voltage.	43

UMxxxx

2.14.2	FDCAN interface	43
2.14.3	IO restriction to other features	44
2.15	SMARTCARD	45
2.15.1	Operating voltage.	45
2.15.2	SmartCard interface.....	45
2.15.3	IO restriction to other features	46
2.16	User LEDs	47
2.16.1	Operating voltage.	47
2.16.2	LED interface.	47
2.16.3	IO restriction to other features	47
2.17	Physical input devices: BUTTONS	48
2.17.1	Operating voltage.	48
2.17.2	Physical input IO interface.....	48
2.17.3	Limitations.....	48
2.18	Operational amplifier and comparator	49
2.18.1	Operating voltage.	49
2.18.2	Operational amplifier.....	49
2.18.3	Comparator	50
2.18.4	Limitations.....	50
2.19	Analog input, output, VREF	51
2.19.1	ADC/DAC IO interface	51
2.19.2	Limitations.....	51
2.20	SRAM device	52
2.20.1	Operating voltage.	52
2.20.2	SRAM interface.....	52
2.20.3	Limitations.....	53
2.21	Octo-SPI memory device	54
2.21.1	Octo-SPI FLASH memory device	54
2.21.2	Octo-SPI SRAM device	54
2.21.3	Operating voltage	54
2.21.4	Octo-SPI IO interface.....	54
2.21.5	Limitations.....	55
2.22	EEPROM	56
2.22.1	Operating voltage	56
2.22.2	EEPROM IO interface.....	56
2.23	EXT_I2C connector	56
2.23.1	Operating voltage	56
2.23.2	EXT_I2C IO interface.....	56
2.24	Touch-sensing button	58
2.24.1	Touch-sensing button IO interface.	58
2.24.2	Limitations.....	58
2.25	MXF MCU	59
2.25.1	Operating voltage	59
2.25.2	MXF IO expander	59
2.25.3	IDD measurement.....	60
2.25.4	Limitations.....	60
2.26	Motor control.....	61
2.26.1	Motor-control IO interface.....	61
2.26.2	Board modifications to enable motor control	62
2.26.3	Limitations.....	63
2.27	Extension connectors CN5, CN6, CN8 and CN9	64
2.28	TFT LCD	67
2.28.1	Operating voltage	67
2.28.2	LCD interface.....	67
2.28.3	Limitations.....	68
2.29	PMOD connector	69
2.29.1	Limitations.....	70
2.30	STMOD+ connector.....	71
2.30.1	Limitations.....	72

UMxxxx

1	Appendix A STM32L552E-EVAL Jumper summary	73
2	Appendix B STM32L552E-EVAL IO Assignment	74
3	Appendix C Mechanical Dimensions	78
4	Appendix C Document Revision History.....	79
	Appendix A	80
	Appendix B: CISPR32	81

List of tables

Table 1. Jumper and SB ON/OFF convention	9
Table 2. STLINK USB μ B connector pinout CN22.	12
Table 3. HW configuration for the TRACE connector CN11	14
Table 4. TRACE connector pinout: CN11.	14
Table 5. HW configuration for the JTAG function on connector: CN10.....	16
Table 6. CN10 JTAG connector pinout.....	17
Table 7. HW configuration for the STDC14 connector CN15.....	18
Table 8. STDC14 connector pinout.....	18
Table 9. HW configuration for the TAG connector CN7.....	19
Table 10. TAG connector pinout: CN7.	20
Table 11. Power sources capability.....	21
Table 12. SB41 Bypass USB PWR protection.....	26
Table 13. LDO and the associated HW SB configuration.....	28
Table 14. HW configuration for the MCU power supply voltage.....	29
Table 15. HW configuration for the 32.768KHz.....	31
Table 16. HW configuration for the 16MHz.....	31
Table 17. HW configuration for the BOOT mode SW1.....	32
Table 18. HW configuration for the audio codec interface SAI and I2C.....	33
Table 19. HW configuration for the DFSDM interface.....	34
Table 20. Audio Jack connector pinout CN21.....	35
Table 21. HW configuration for the USB interface.....	36
Table 22. HW configuration for the UCPD feature.....	36
Table 23. USB_TYPE_C connector pinout CN1.....	37
Table 24. HW configuration for the RS-232 interface.....	39
Table 25. Audio Jack connector pinout CN3.....	40
Table 26. HW configuration for the SDIO interface.....	41
Table 27. SDCARD connector pinout CN25.....	42
Table 28. HW configuration between MCU and FDCAN transceiver.....	43
Table 29. FDCAN interface and connector pinout CN17.....	44
Table 30. HW configuration for the smartcard interface.....	45
Table 31. smartcard interface U26 and connector pinout CN26.....	46
Table 32. HW configuration for the LED interface.....	47
Table 33. HW configuration for the physical user interface.....	48
Table 34. HW configuration for the OPAMP interface.....	49
Table 35. Jumper configuration to enable the LDR or the potentiometer to OPAMP1 function.....	50
Table 36. HW configuration for the comparator interface.....	50
Table 37. Jumper configuration to enable the LDR or the potentiometer to COMP2 function.....	50
Table 38. HW configuration for the ADC/DAC interface.....	51
Table 39. ADC/DAC interface and connector pinout CN12.....	51
Table 40. HW configuration for the SRAM interface.....	52
Table 41. HW configuration for the OCTOSPI interface.....	54
Table 42. Octo-SPI jumper configuration.....	55
Table 43. HW configuration for the EEPROM interface.....	56
Table 44. HW configuration for the EXT_I2C interface.....	56
Table 45. EXT_I2C connector pinout CN4.....	57
Table 46. HW configuration for the Touch-sensing button interface.....	58
Table 47. HW configuration for the MFX interface.....	59
Table 48. IO signals driven by the MFX.....	59
Table 49. jumper associated with the IDD measurement on the board.....	60
Table 50. Motor control terminal and IO function assignment.....	61
Table 51. Motor Control connector pinout CN2.....	62
Table 52. CN5 connector pinout.....	64
Table 53. CN6 connector pinout.....	65
Table 54. CN8 connector pinout.....	66
Table 55. CN9 connector pinout.....	66
Table 56. HW configuration for the LCD interface.....	67

UMxxxx

Table 57. LCD connector pinout CN18.....	68
Table 58. HW configuration for the PMOD interface.	69
Table 59. PMOD connector pinout P1.....	70
Table 60. HW configuration for the STMOD+ interface.	71
Table 61. STMOD+ interface and connector pinout.	72

List of figures

Figure 1. STM32L552E-EVAL evaluation board	1
Figure 2. STM32L552E-EVAL hardware block diagram	10
Figure 3. STM32L552E-EVAL PCB layout: TOP side	11
Figure 4. STM32L552E-EVAL PCB layout: BOTTOM side	11
Figure 5. STLINK USB μ B connector pinout CN22	12
Figure 6. USB composite device	13
Figure 7. TRACE connector pinout: CN11	14
Figure 8. CN10 JTAG connector pinout	16
Figure 9. CN15 STDC14 connector pinout	18
Figure 10. TAG connector pinout: CN7	19
Figure 11. JP16[1-2]: 5V_STLK PWR SOURCE	22
Figure 12. JP16[3-4]: 5V_EXT PWR SOURCE	23
Figure 13. 5V power supply connector: CN19	23
Figure 14. JP16[5-6]: 5V_USB_TYPEC: CN1	24
Figure 15. JP16[7-8]: 5V_DC PWR SOURCE	25
Figure 16. JP16[9-10]: 5V_USB_CHG PWR SOURCE : CN22	26
Figure 17. Jumper and SB for power sources	29
Figure 18. Audio Jack connector pinout CN21	34
Figure 19. USB TYPE C connector pinout CN1	37
Figure 20. RS-232 connector pinout CN3	40
Figure 21. SDCARD connector pinout CN25	42
Figure 22. FDCAN connector pinout CN17	43
Figure 23. Smartcard connector pinout CN26	45
Figure 24. ADC/DAC connector pinout CN12	51
Figure 25. EXT_I2C connector pinout CN4 (front view)	57
Figure 26. Motor control connector pinout CN2	62
Figure 27. STM32L552E-EVAL Top side Motor control hardware update	63
Figure 28. STM32L552E-EVAL Top side Motor control hardware update	63
Figure 29. CN5/CN6 connector pinout	64
Figure 30. CN8/CN9 connector pinout	65
Figure 31. LCD connector pinout CN18	67
Figure 32. PMOD connector pinout P1	69
Figure 33. STMOD+ connector pinout	72
Figure 34. jumper default setting of the STM32L552E-EVAL	73

1 Overview

Features

- STM32L552ZET6Q microcontroller with 512-Kbytes Flash memory and 256-Kbytes RAM in LQFP144 Package and INT-SMPS (1)
- 2.8" TFT LCD, 240RGB x 320 pixels, 262K color, with touch control panel.
- 16-Mbit (1M x 16 bit) SRAM device
- 512-Mbit Octo SPI Flash memory device with double transfer rate (DTR) support
- 64-Mbit Octo SPI SRAM memory device with HyperBus interface support
- Low power Stereo Audio CODEC with Headphone amplifier
- Two MEMS digital microphones.
- 8-Gbyte microSD card bundled (To Be confirm if SD is include on BOX and capacity)
- 2 smart sensors with sigma-Delta modulator
- EEPROM supporting 1 MHz I²C-bus communication speed
- Joystick with four-way controller and selector
- Reset and Wake-up / tamper buttons
- One Touch-sensing button
- Light-dependent resistor (LDR)
- Potentiometer
- Coin battery cell for power backup
- Board connectors:
 - One jack outputs for stereo audio headphone with independent content
 - Extension connector for MEMS digital microphones.
 - Slot for microSD card supporting SD, SDHC, SDXC
 - TFT LCD standard connector
 - USB Type C Device FS supported UCPD controller
 - SmartCard interface 3V or 5V with smartcard reader
 - RS-232 port configurable for communication or MCU flashing
 - CAN-FD compliant port ISO-11898-2 and ISO-11898-5 standards
 - EXT_I2C connector supports I²C bus
 - Connector for ADC input and DAC output
 - JTAG/SWD, ETM trace debug support, user interface through USB virtual COM port, embedded ST-LINK/V2-1 debug and flashing facility
 - TAG connector
 - STDC14 connector
- Expansion connectors:
 - PMOD connector
 - STMOD+ connector
 - Motor Control connector
 - Extension connector for daughter board
- Flexible power-supply options: Power jack, ST-LINK/V2-1 USB connector, USB Type C FS connector, daughter board.
- Microcontroller supply voltage: 3.3 V or range from 1.71 V to 3.6 V
- MCU current consumption measurement circuit
- Access to comparator and operational amplifier of STM32L552ZET6Q

- Comprehensive free software libraries and examples available with the STM32Cube package.

Support of a wide choice of Integrated Development Environments (IDES) including IAR™, Keil®, GCC-based

(1). SMPS significantly reduces power consumption in Run mode, by generating Vcore logic supply from an internal DC/DC converter.

1.1 Demonstration software

The demonstration software, included in the STM32Cube package, is preloaded in the STM32 Flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from the www.st.com webpage.

1.2 Order code

To order the evaluation board based on the STM32L552ZET6Q MCU, use the order code STM32L552E-EVAL.

1.3 Unpacking recommendations

Before the first use, make sure that, no damage occurred to the board during shipment and no socketed components are loosen in their sockets or fallen into the plastic bag.

In particular, pay attention to the following components:

1. **microSD card in its CN8 receptacle**
2. Module LCD MB989 daughter board in its CN18 connector, and LCD screw, spacer and nut are in place.

For product information related with STM32L552ZET6Q microcontroller, visit www.st.com website.

1.4 Conventions

[Table 1](#) provides the definition of some conventions used in the present document.

Table 1. Jumper and SB ON/OFF convention

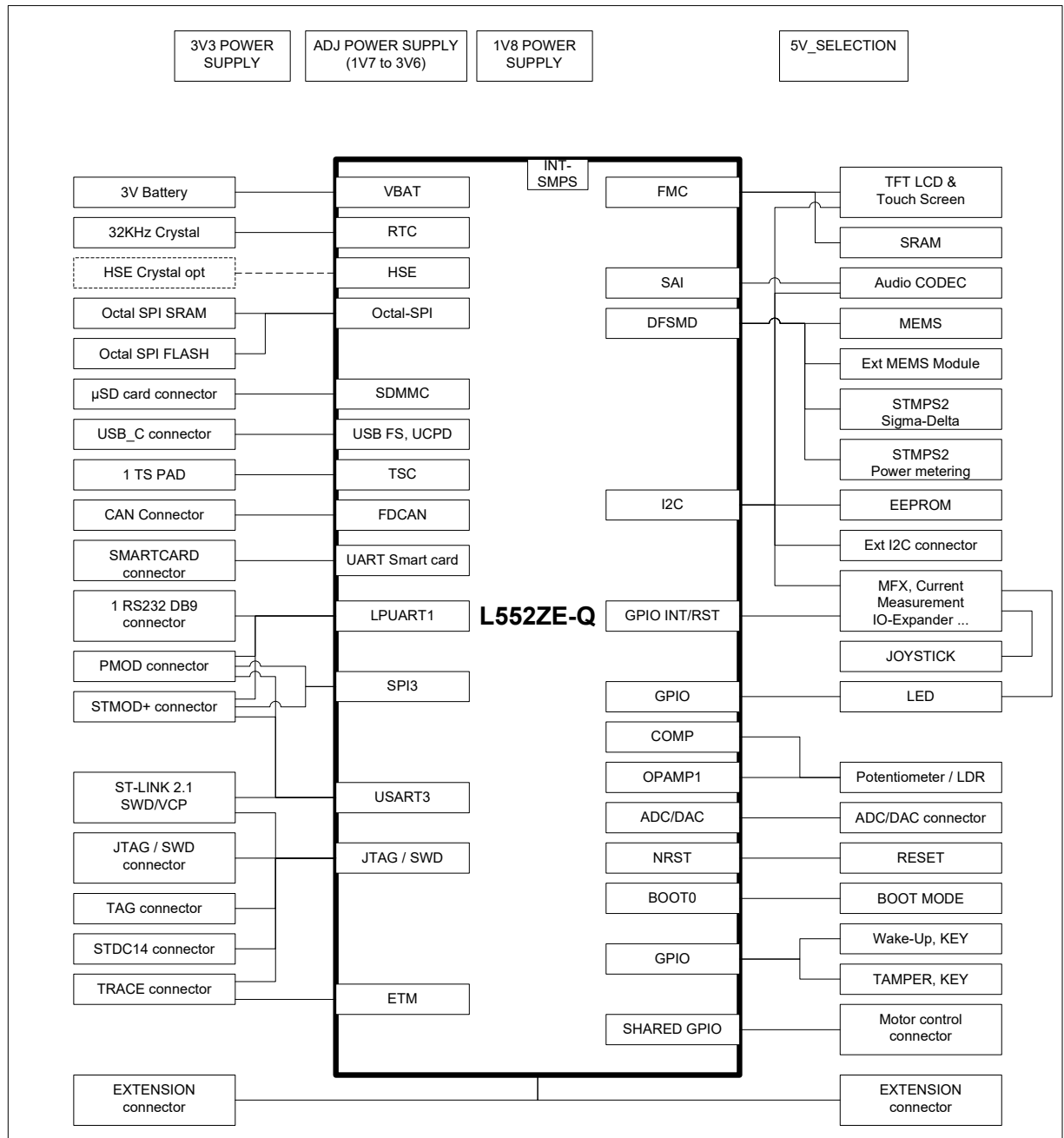
Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper should be fitted between Pin 1 and Pin 2
Solder bridge SBxxx ON	SBx connections closed by 0 ohm resistor
Solder bridge SBxxx OFF	SBx connections left open
Resistor Rxxx ON	Resistor soldered
Resistor Rxxx OFF	Resistor NOT soldered

In this document the references for all information that is common to all sale types, are “STM32 Nucleo-144 board” and “STM32 Nucleo-144 boards”.

2 Hardware Layout and configuration

The STM32L552E-EVAL evaluation board is designed around STM32L552ZET6Q target microcontroller in LQFP 144-pin package. Figure 2 illustrates STM32L552ZET6Q connections with peripheral components. Figure 3 shows the location of main components on the evaluation board on the TOP side and Figure 4 shows the location of main components on the evaluation board on the BOTTOM side.

Figure 2. STM32L552E-EVAL hardware block diagram



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Figure 3. STM32L552E-EVAL PCB layout: TOP side

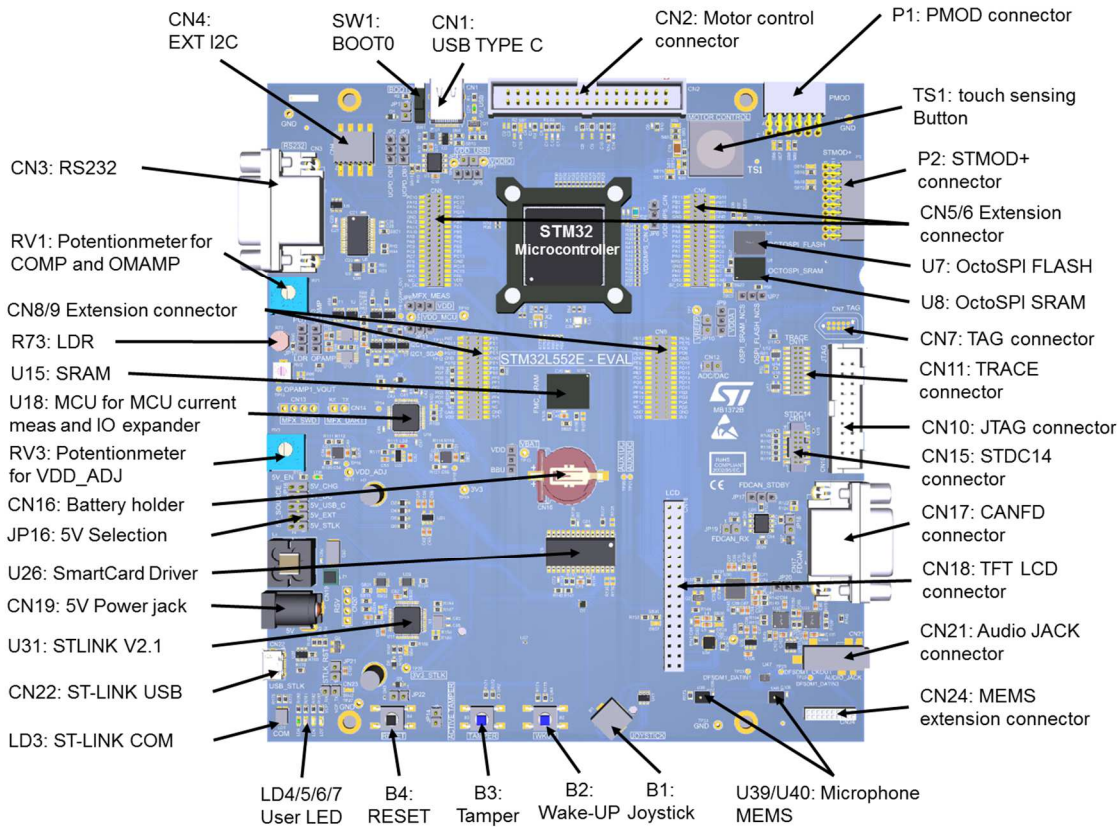
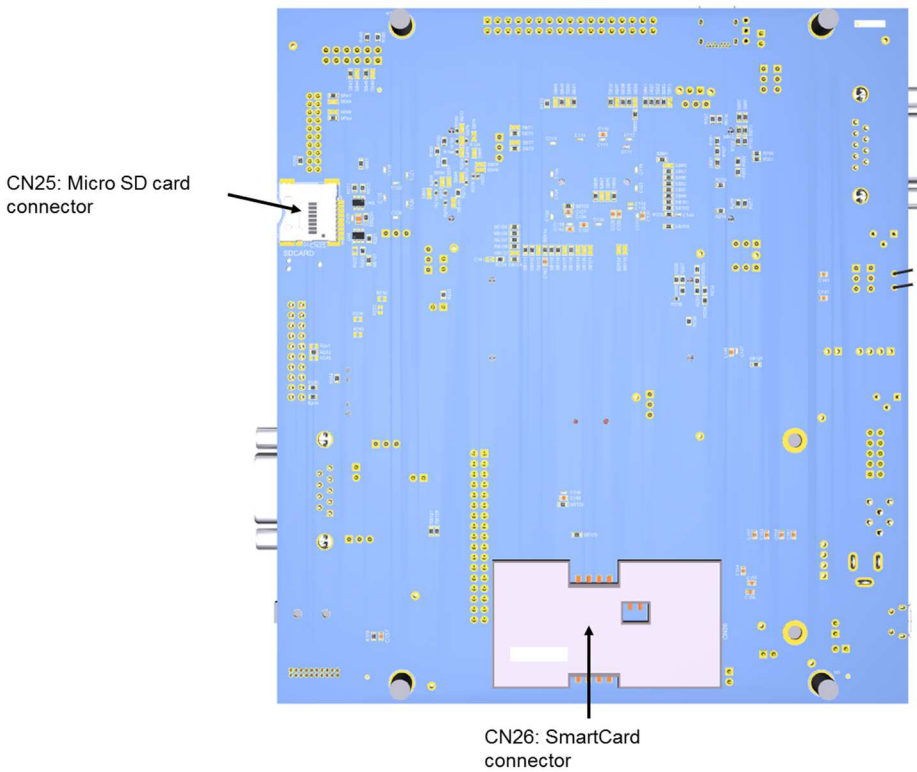


Figure 4. STM32L552E-EVAL PCB layout: BOTTOM side



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2.1 ST-LINK/V2-1

ST-LINK/V2-1 facility for debug and flashing of STM32L552ZET6Q, is integrated on the STM32L552E-EVAL evaluation board.

Compared to ST-LINK/V2 stand-alone tool available from STMicroelectronics, ST-LINK/V2-1 offers new features and drops some others.

New features:

- USB software re-enumeration
- Virtual COM port interface on USB
- Mass storage interface on USB
- USB power management request for more than 100mA power on USB

Features dropped:

- SWIM interface

The USB connector CN22 can be used to power STM32L552E-EVAL regardless of the ST-LINK/V2-1 facility use for debugging or for flashing STM32L552ZET6Q.

Figure 5 shows the STLINK USB μ B connector pinout CN22.

Figure 5. STLINK USB μ B connector pinout CN22.

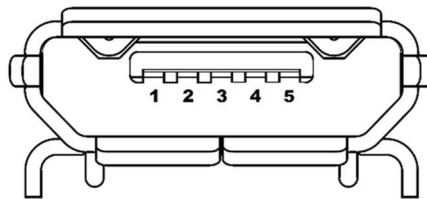


Table 2 describe STLINK USB μ B connector pinout CN22.

Table 2. STLINK USB μ B connector pinout CN22.

Pin	Board function	STLINK STM32 pin
1	VBUS Power	-
2	DM	PA11
3	DP	PA12
4	ID	GND
5	GND	GND

This holds also when ST-LINK/V2 stand-alone tool is connected to CN7: Tag connector, CN10: JTAG connector, CN11: Trace connector or CN15: STDC14 connector and used for debugging or flashing STM32L552ZET6Q. [Section 2.6: Power supply](#) provides more detail on powering STM32L552E-EVAL.

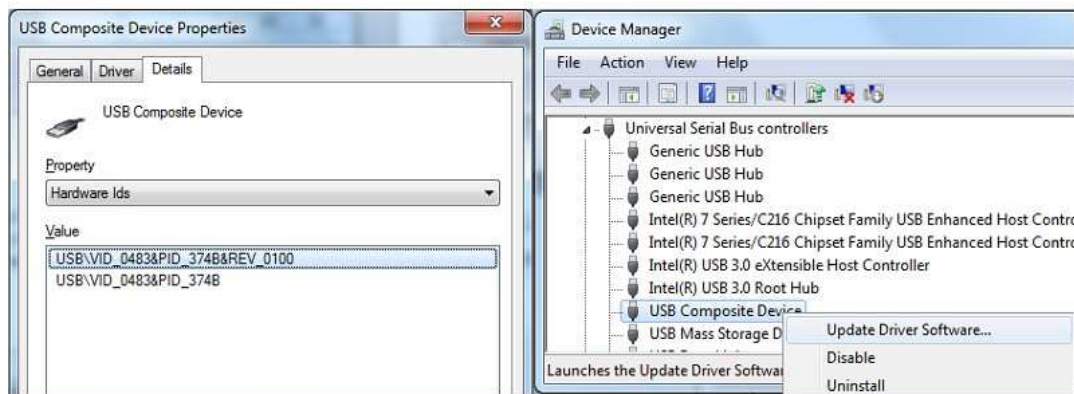
For full detail on both versions of the debug and flashing tool, the stand-alone ST-LINK/V2 and the embedded ST-LINK/V2-1, refer to www.st.com.

2.1.1 Drivers

Before connecting STM32L552E-EVAL to a Windows (XP, 7, 8 10) PC via USB, a driver for ST-LINK/V2-1 must be installed. It can be downloaded from www.st.com.

In case the STM32L552E-EVAL evaluation board is connected to the PC before installing the driver, the Windows device manager may report some USB devices found on STM32L552E-EVAL as “Unknown”. To recover from this situation, after installing the dedicated driver downloaded from www.st.com, the association of “Unknown” USB devices found on STM32L552E-EVAL to this dedicated driver must be updated in the device manager manually. It is recommended to proceed using USB Composite Device line, as shown in [Figure 6](#).

Figure 6. USB composite device



2.1.2 ST-LINK/V2-1 firmware upgrade

For its own operation, ST-LINK/V2-1 employs a dedicated MCU with Flash memory. Its firmware determines ST-LINK/V2-1 functionality and performance. The firmware may evolve during the life span of STM32L552E-EVAL to include new functionality, fix bugs or support new target microcontroller families. It is therefore recommended to keep ST-LINK/V2-1 firmware up to date. The latest version is available from www.st.com.

2.2 ETM trace

The connector CN11 can output trace signals used for debug.

Table 3 describe the HW configuration for the TRACE function.

Table 3. HW configuration for the TRACE connector CN11

IO	Bridge	Setting	comment
PC9	SB59	ON	PC9 can be used for the trace function TRACE D0
		OFF	PC9 is not connected to Trace PC9 can be used for SDIO
PC10	SB68	ON	PC10 can be used for the trace function TRACE D1
		OFF	PC10 is not connected to Trace PC10 can be used for SDIO
PC12	SB53	ON	PC12 can be used for the trace function TRACE D3
		OFF	PC12 is not connected to Trace PC12 can be used for SDIO
PE2	R230	ON	PE2 can be used for the trace function TRACE CLK
		OFF	PE2 is not connected to Trace No other muxing
PE5	R95	ON	PE5 can be used for the trace function TRACE D2
		OFF	PE5 is not connected to Trace No other muxing

(Default configuration is shown in bold.)

Figure 7 shows the TRACE connector pinout.

Figure 7. TRACE connector pinout: CN11.

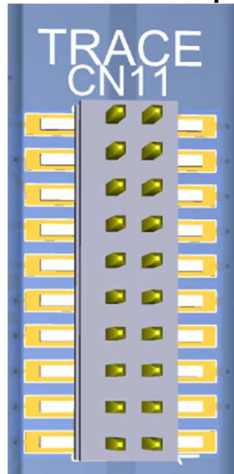


Table 4 describe the TRACE connector pinout

Table 4. TRACE connector pinout: CN11.

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
VDD	Power	1	2	TMS / SWDIO	PA13
GND	Power	3	4	TCK / SWCLK	PA14
GND	Power	5	6	TDO / SWO	PB3

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-	KEY	7	8	TDI	PA15
GND	Power	9	10	HOST NRST	NRST
GND	Power	11	12	TRACE CLK	PE2
GND	Power	13	14	TRACE D0	PC9
GND	Power	15	16	TRACE D1	PC10
GND	Power	17	18	TRACE D2	PE5
GND	Power	19	20	TRACE D3	PC12

2.2.1 IO restriction to other features

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the audio features:

The TRACE cannot be operated simultaneously with SDCARD function.

The TRACE cannot be operated simultaneously with STMOD+ function.

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2.3 JTAG Connector

The connector CN10 can output JTAG signals used for debug.

Table 5 describe the HW configuration for the JTAG function.

Table 5. HW configuration for the JTAG function on connector: CN10

IO	Bridge	Setting	comment
PB4	SB93	ON	PB4 is connected to JTAG JTRSTN
		OFF	PB4 is NOT connected to JTAG PB4 can be used for COMP or STMOD+
PA15	SB72	ON	PA15 is connected to JTAG JTDI
		OFF	PA15 is NOT connected to JTAG PA15 can be used for UCPB
PA13	R192	ON	PA13 is connected to JTAG as JTMS or SWD SWDIO
		OFF	PA13 is NOT connected to JTAG or SWD No other muxing
PA14	R193	ON	PA14 is connected to JTAG as JTCK or SWD SWCLK
		OFF	PA14 is NOT connected to JTAG or SWD No other muxing
PB3	R197	ON	PB3 is connected to JTAG as JTDO (SWO)
		OFF	PB3 is NOT connected to JTAG or SWD PA15 can be used for GREEN LED
NRST	-	-	NRST used to RESET target

(Default configuration is shown in bold.)

Figure 8 shows the CN10 JTAG connector pinout.

Figure 8. CN10 JTAG connector pinout.

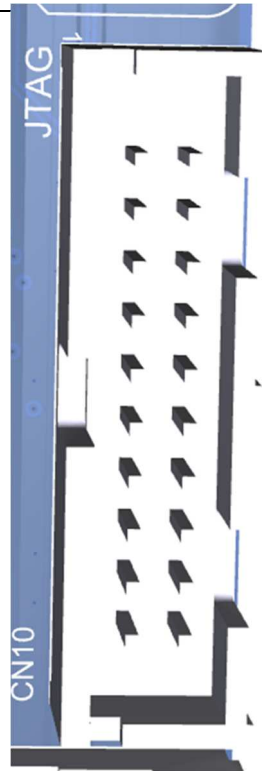


Table 6 describe the JTAG connector pinout

Table 6. CN10 JTAG connector pinout.

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
VDD	Power	1	2	Power	VDD
PB4	JTRSTN	3	4	Power	GND
PA15	TDI	5	6	Power	GND
PA13	TMS/SWDIO	7	8	Power	GND
PA14	TCK/SWCLK	9	10	Power	GND
-	Pull down	11	12	Power	GND
PB3	TDO/SWO	13	14	Power	GND
NRST	HOST NRST	15	16	Power	GND
-	TRGIN	17	18	Power	GND
-	TRGOUT	19	20	Power	GND

2.3.1 IO restriction to other features

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the audio features:

The JTAG is mainly limited to SWD function, TDI and TDO are optional.

The full JTAG cannot be operated simultaneously with COMP function.

The full JTAG cannot be operated simultaneously with STMOD+ function.

The full JTAG cannot be operated simultaneously with UCPD function.

The full JTAG cannot be operated simultaneously with Green LED function.

2.4 STDC14 Connector

The connector CN15 can output also JTAG signals used for debug compatible with STDC14.

Table 7 describe the HW configuration for the STDC14 function.

Table 7. HW configuration for the STDC14 connector CN15

IO	Bridge	Setting	comment
PA15	SB72	ON	PA15 is connected to JTAG JTDI
		OFF	PA15 is NOT connected to JTAG PA15 can be used for UCPB
PA13	R192	ON	PA13 is connected to JTAG JTMS or SWD SWDIO
		OFF	PA13 is NOT connected to JTAG or SWD No other muxing
PA14	R193	ON	PA14 is connected to JTAG JTCK or SWD SWCLK
		OFF	PA14 is NOT connected to JTAG or SWD No other muxing
PB3	R197	ON	PB3 is connected to JTAG JTDO or SWD SWO
		OFF	PB3 is NOT connected to JTAG or SWD PA15 can be used for GREEN LED
NRST	-	-	NRST used to RESET target
PB10	SB78	ON	PB10 USART3_TX is connected to T_VCP function SB48 and SB77 should be not fitted
		OFF	PB10 USART3_TX is NOT connected to T_VCP PB10 can be used for RS-232 or STMOD+
PB11	SB75	ON	PB11 USART3_RX is connected to T_VCP SB50 and SB71 should be not fitted
		OFF	PB11 USART3_RX is NOT connected to T_VCP PB11 can be used for RS-232 or STMOD+

(Default configuration is shown in bold.)

Figure 9 shows the CN15 STDC14 connector pinout.

Figure 9. CN15 STDC14 connector pinout.

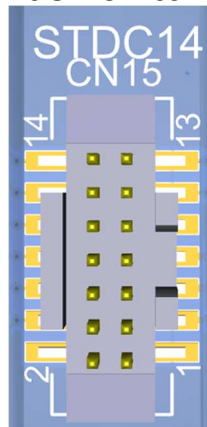


Table 8 describe the STDC14 connector pinout

Table 8. STDC14 connector pinout.

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
-	NC	1	2	NC	-
VDD	Power	3	4	TMS_SWDIO	PA13

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GND	Power	5	6	TCK_SWCLK	PA14
GND	Power	7	8	TDO_SWO	PB3
-	KEY	9	10	TDI	PA15
-	GNDDetect: Pull down	11	12	HOST NRST	NRST
PB11	T_VCP_RX	13	14	T_VCP_TX	PB10

2.4.1 IO restriction to other features

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the audio features:

The JTAG is mainly limited to SWD function, TDI and TDO are optional.

The full JTAG cannot be operated simultaneously with COMP function.

The full JTAG cannot be operated simultaneously with STMOD+ function.

The full JTAG cannot be operated simultaneously with UCPD function.

The full JTAG cannot be operated simultaneously with Green LED function.

2.5 TAG Footprint

The Footprint CN7 can output also Debug interface compatible with TAG probe TC2050-IDC-NL.

Table 9 describe the HW configuration for the TAG function.

Table 9. HW configuration for the TAG connector CN7

IO	Bridge	Setting	comment
PA15	SB72	ON	PA15 is connected to JTAG JTDI
		OFF	PA15 is NOT connected to JTAG PA15 can be used for UCPB
PA13	R192	ON	PA13 is connected to JTAG JTMS or SWD SWDIO
		OFF	PA13 is NOT connected to JTAG or SWD No other muxing
PA14	R193	ON	PA14 is connected to JTAG JTCK SWD SWCLK
		OFF	PA14 is NOT connected to JTAG or SWD No other muxing
PB3	R197	ON	PB3 is connected to JTAG JTDO or SWD SWO
		OFF	PB3 is NOT connected to JTAG or SWD PA15 can be used for GREEN LED
PB4	SB93	ON	PB4 is connected to JTAG JTRSTN
		OFF	PB4 is NOT connected to JTAG PB4 can be used for COMP or STMOD+
NRST	-	-	NRST used to RESET target

(Default configuration is shown in bold.)

Figure 10 shows the TAG connector pinout.

Figure 10. TAG connector pinout: CN7.

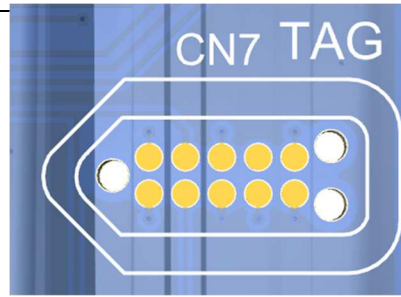


Table 10 describe the TAG connector pinnout

Table 10. TAG connector pinout: CN7.

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
VDD	Power	1	10	HOST NRST	NRST
PA13	TMS SWDIO	2	9	JTAG_TRST	PB4
GND	Power	3	8	TDI	PA15
PA14	TCK SWCLK	4	7	NC	-
GND	Power	5	6	TDO_SWO	PB3

2.5.1 IO restriction to other features

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the audio features:

The JTAG is mainly limited to SWD function, TDI and TDO are optional.

The full JTAG cannot be operated simultaneously with COMP function.

The full JTAG cannot be operated simultaneously with STMOD+ function.

The full JTAG cannot be operated simultaneously with UCPD function.

The full JTAG cannot be operated simultaneously with Green LED function.

2.6 Power Supply

2.6.1 5V power supply general view.

STM32L552E-EVAL evaluation board is designed to be powered from 5V DC power source. It incorporates a precise polymer Zener diode (Poly-Zen) protecting the board from damage due to wrong power supply. One of the following five 5V DC power inputs can be used, upon an appropriate board configuration:

- **5V_STLK from micro-B USB receptacle CN22 of ST-LINK/V2-1 (default).**
- 5V_EXT from power jack CN19, marked 5V on the board. The positive pole is on the center pin as illustrated in [Figure 13](#).
- 5V_USB_C from USB TYPE C receptacle CN1 of USB user interface.
- 5V_DC from pin 37 of CN5 or Pin 37 of CN6 extension connectors for custom daughter board.
- 5V_CHG from micro-B USB receptacle CN22 of ST-LINK/V2-1, in case of wall charger (no-enumeration).

No external power supply is provided with the board.

when 5V_EXT, 5V_DC is used to power the board, this power source must comply with the standard EN-60950-1: 2006+A11/2009 and must be Safety Extra Low Voltage (SELV) with limited power capability

LD8 Green LED turns on when the voltage on the power line marked as 5V is present. All supply lines required for the operation of the components on STM32L552E-EVAL are derived from that 5V line.

[Table 11](#) describe the 5V power supply capabilities.

Table 11. Power sources capability.

Input Power name	Connector Pins	Voltage range	Max current	Limitation
5V_STLK VBUS from STLINK USB	CN22 pin 1 JP16[1-2]	4.75V to 5.25V	500mA	Max current depend of the USB enumeration: <ul style="list-style-type: none"> • 100mA without enumeration • 500mA with enumeration OK.
5V_EXT	CN19 pin 1 JP16[3-4]	4.75V to 5.25V	-	Max current depending of the power source
5V_USB_TYPE -C	CN1 JP16[5-6]	4.75V to 5.25V	1A	Max current depend of the USB Host use to powered the EVAL board
5V_DC	CN5 pin 37 CN6 pin 37 JP16[7-8]	4.75V to 5.25V	-	Max current depending of the power source
5V_USB_CHG	CN22 pin 1 JP16[9-10]	4.75V to 5.25V	-	Max current depend of the USB wall charger use to powered the board

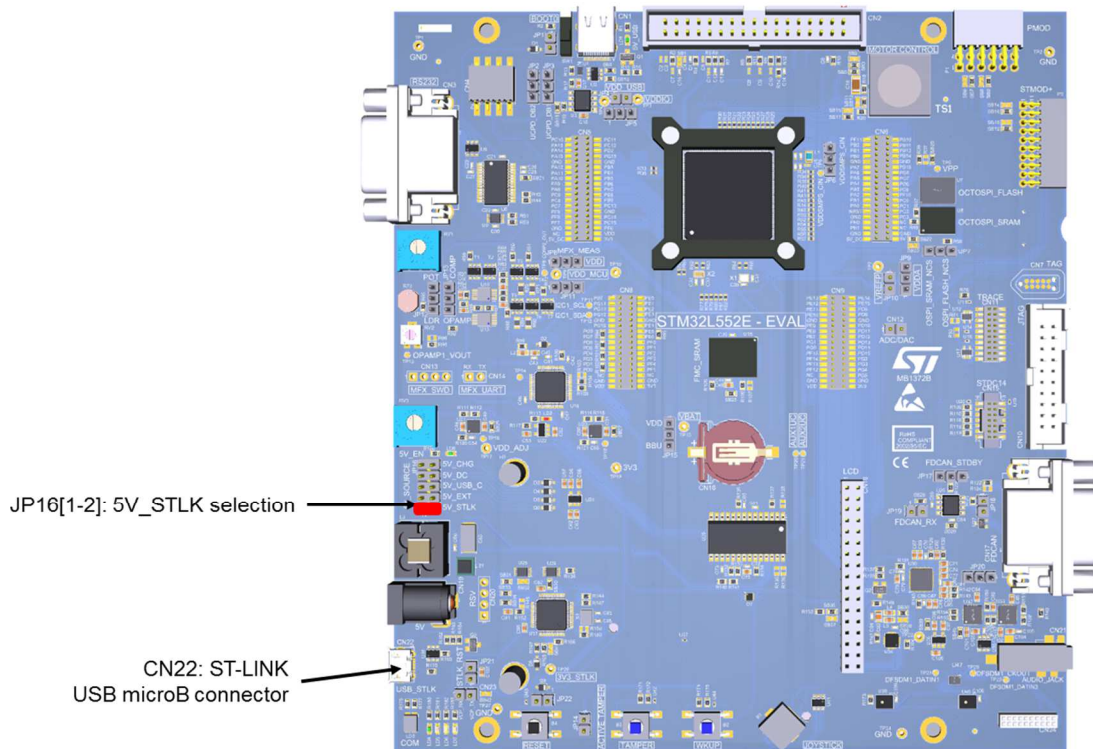
2.6.2 5V_ST_LINK power source

5V_ST_LINK is a DC power with limitation from ST-LINK USB connector (USB type micro-B connector of ST-LINK/V2-1). In this case JP16 jumper should be on pin [1-2] to select 5V_STLK power source on silkscreen of JP16. **This is the default setting.** If the USB enumeration succeeds, the 5V_STLK power is enabled, by asserting the PWR_ENn signal (from STM32F103CBT6). This pin is connected to a power switch STMP52141STR, which powers the board. This power switch features also a current limitation to protect the PC in case of a short-circuit on board (more than 500mA).

The EVAL board and its shield on it can be powered from ST-LINK USB connector CN22, but only ST-LINK circuit has the power before USB enumeration, because the host PC only provides 100mA to the board at that time. During the USB enumeration, the EVAL board asks for the 500mA power to the host PC. If the host is able to provide the required power, the enumeration finishes by a “SetConfiguration” command and then, the power switch is switched ON, the GREEN LED LD4 turned ON, thus the EVAL board and its shield on it can consume 500mA current, but no more. If the host is not able to provide the requested current, the enumeration fails. Therefore the power switch remains OFF and the MCU part including the extension board is not powered. As a consequence the GREEN LED LD4 remains turned OFF. In this case it is mandatory to use an external power supply.

5V_STLK power source configuration for jumper JP16[1-2] is describe on [figure 11](#)

Figure 11. JP16[1-2]: 5V_STLK PWR SOURCE.



2.6.3 5V_EXT power source

5V_EXT is the DC power coming from the power jack CN19. In this case JP16 jumper should be on pin [3-4] to select 5V_EXT power source on silkscreen of JP16. The positive pole is on the center pin as illustrated in [Figure 13](#)

5V_EXT power source configuration for jumper JP16[3-4] is describe on [figure 12](#)

Figure 12. JP16[3-4]: 5V_EXT PWR SOURCE.

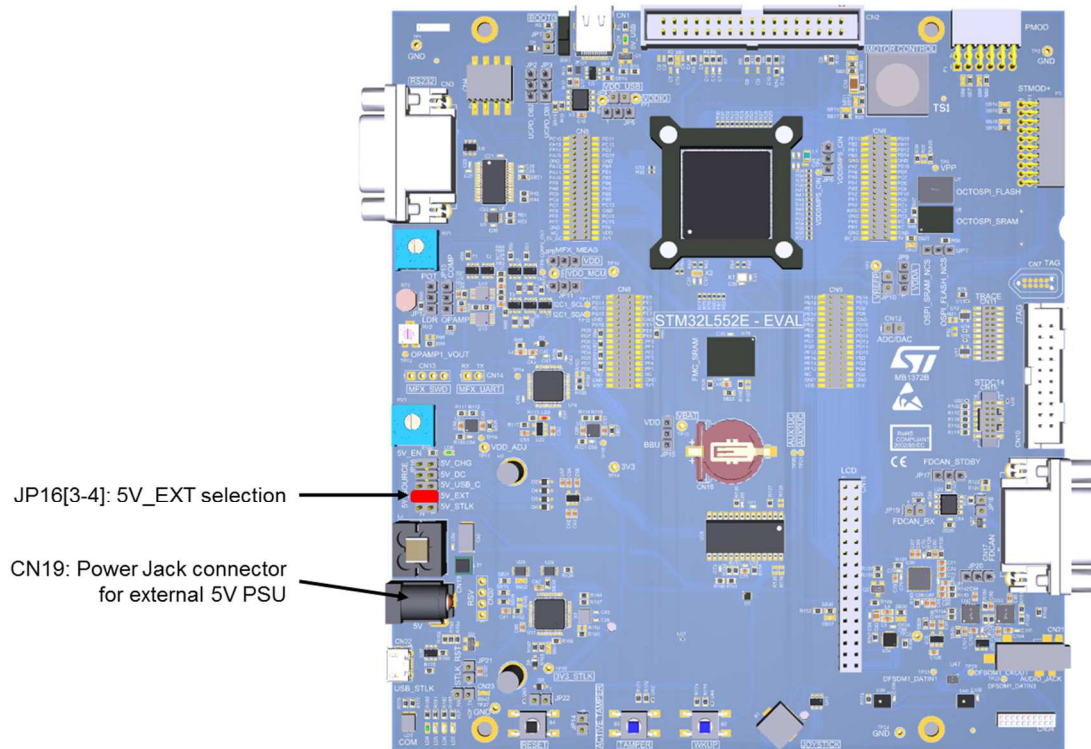
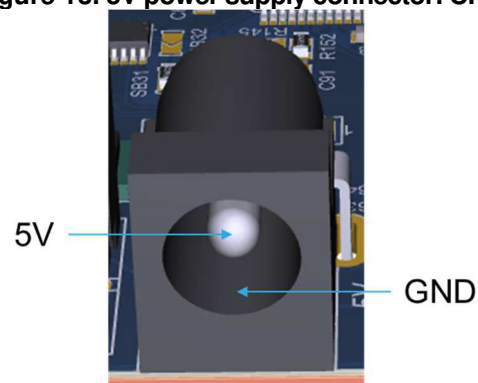


Figure 13. 5V power supply connector: CN19.

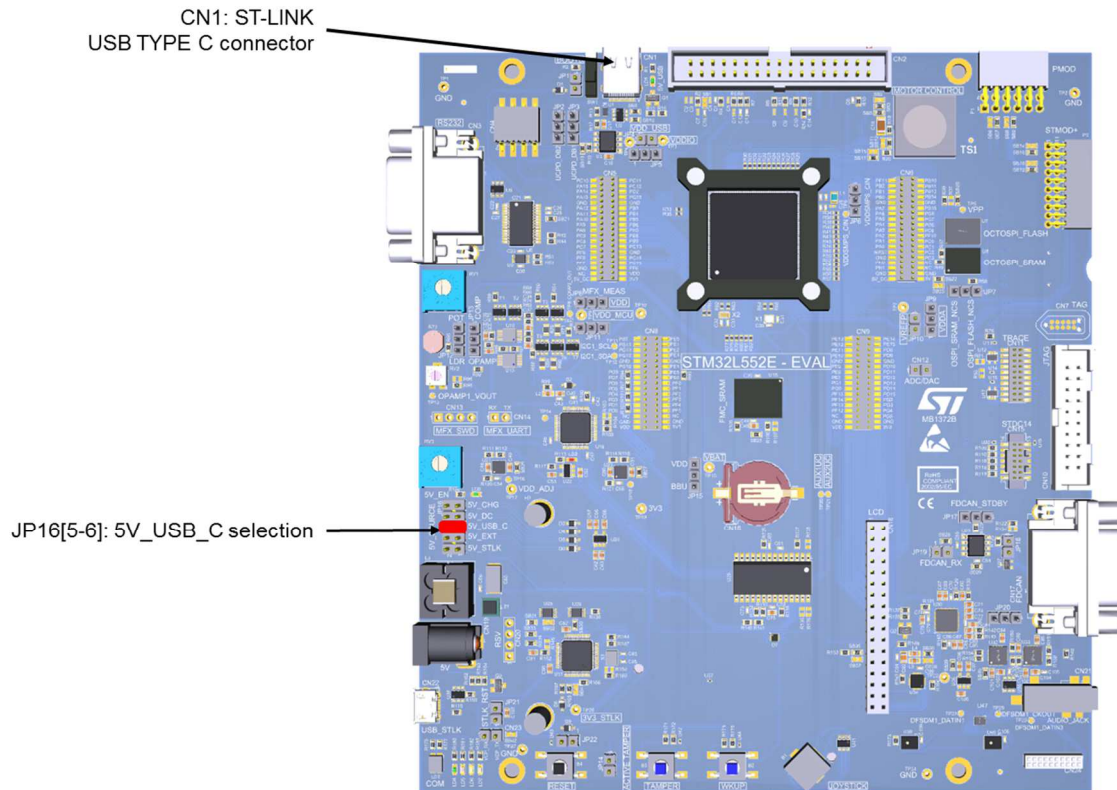


2.6.4 5V_USB_TYPE C power source

- **5V_USB_TYPE_C** is the DC power supply connected to the user USB TYPE C (CN1). To select the 5V_USB_TYPE_C power source on silkscreen of JP16, the jumper of JP16 should be on pins [5-6]. In this case.

5V_USB_TYPEC power source configuration for jumper JP16[5-6] is describe on [figure 14](#)

Figure 14. JP16[5-6]: 5V_USB_TYPEC: CN1

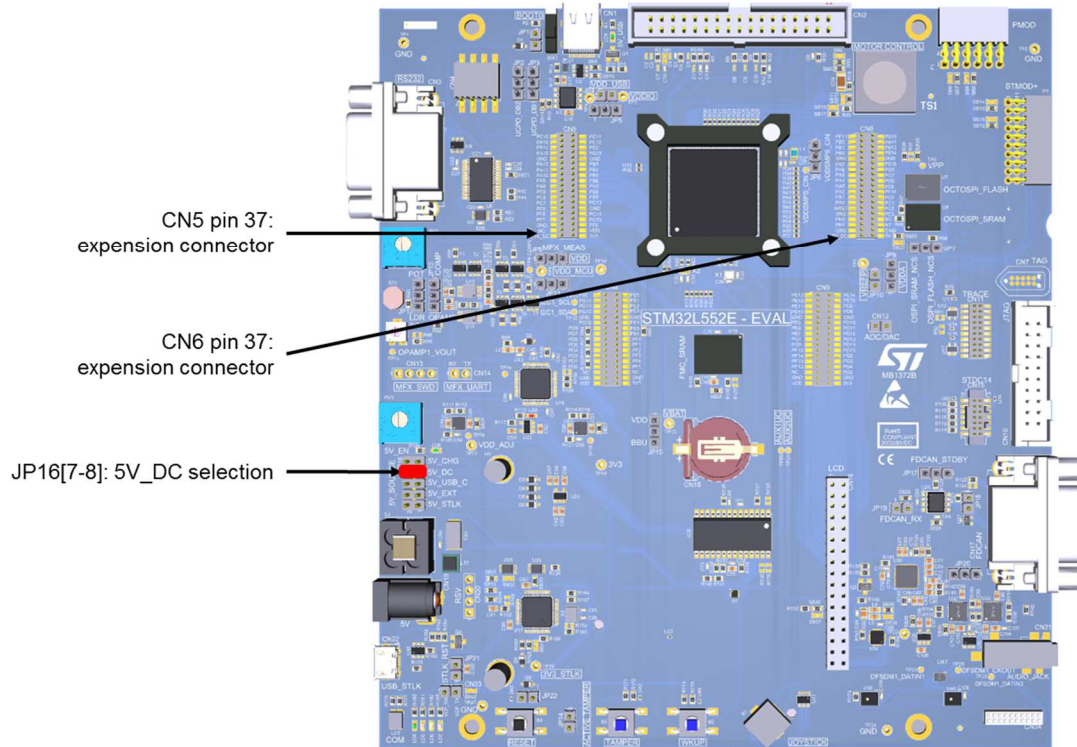


2.6.5 5V_DC power source

5V_DC is the DC power coming from external (5V DC power from extension connector CN5 pin 37 or CN6 pin 37. In this case JP16 jumper should be on pin [7-8] to select 5V_DC power source on silkscreen of JP16.

5V_DC power source configuration for jumper JP16[7-8] is describe on [figure 15](#)

Figure 15. JP16[7-8]: 5V_DC PWR SOURCE.

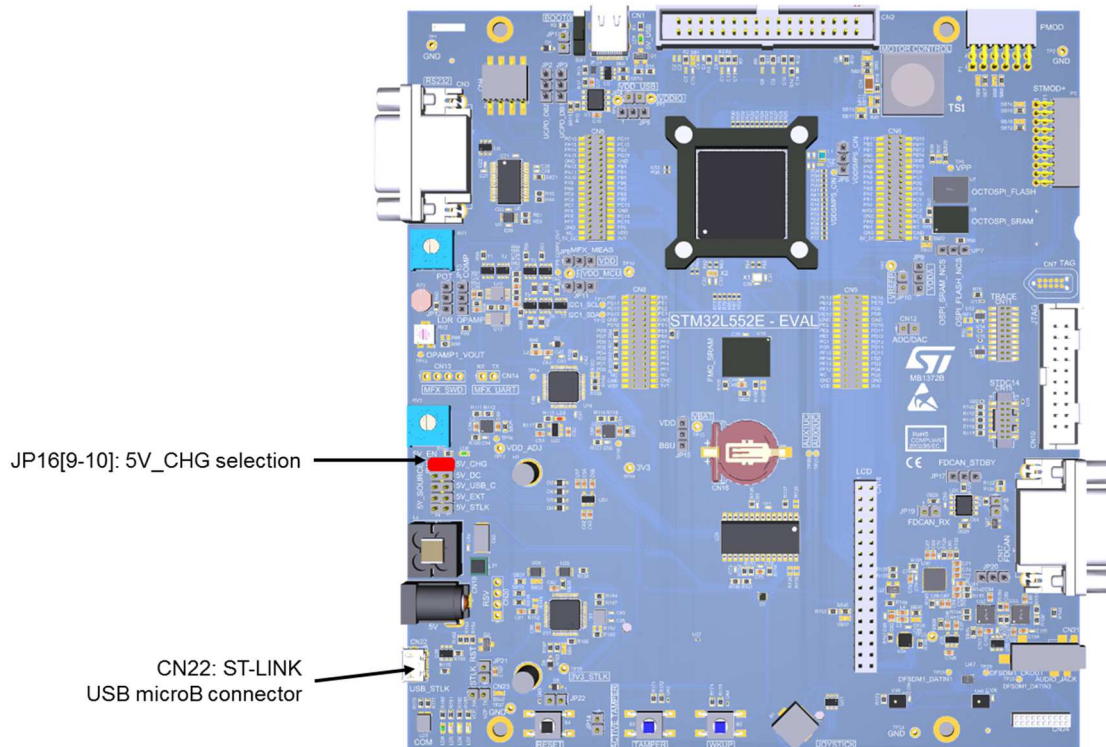


2.6.6 5V_USB_CHARGER power source

5V_USB_CHARGER is the DC power charger connected to USB STLINK (CN22). To select the 5V_USB_CHARGER power source on silkscreen of JP16, the jumper of JP16 should be on pins [9-10]. In this case, if the EVAL board is powered by an external USB charger then the debug is not available. If a computer is connected instead of the charger, the current limitation is no more effective, in this case the computer could be damaged, in this case it is recommended to select . **5V_ST_LINK** mode.

5V_USB_CHG power source configuration for jumper JP16[9-10] is describe on [figure 16](#)

Figure 16. JP16[9-10]: 5V_USB_CHG PWR SOURCE : CN22.



Note: With this JP16 configuration: 5V_USB_CHG, the USB_PWR protection is bypass. Never used this configuration with a computer connected instead of the charger, because as the USB_PWR_protection is bypass, the board can more than 500mA and this can damaged the computer.

Caution: A solder Bridge (SB41) can be used to by-pass the USB PWR protection switch. (This is not a ST recommended setting). SB41 can be set only in case of the board is powered by USB PC and maximum current consumption on 5V_STLINK **doesn't exceed 100mA** (including an eventual extension board or Arduino™ Shield). In such condition USB enumeration will always succeed since no more than 100mA is requested to the PC. Possible configurations of SB41 are summarized in [Table 12](#)

Table 12. SB41 Bypass USB PWR protection.

SB	Default Position	Power supply	Allow current
SB41	OFF (not soldered)	USB PWR through CN22	500mA max limited by Power switch
	ON (soldered)		100mA max

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	OFF (not soldered)	5V_EXT or 5V_DC PWR	Whatever current is: no limitation
	ON (soldered)		Forbidden configuration (1)

Warning: In case maximum current consumption of the EVAL board and its extension boards may exceed 500mA it is recommended to power the EVAL board using an external power supply connected to 5V_EXT or 5V_DC.

Note 1: SB41 must be removed when the board is powered by 5V_EXT (CN19) or by 5V_DC (CN5 pin 37 or CN6 pin37).

2.6.7 Programing/debugging when the power supply is not from ST-LINK (5V_STLK)

5V_EXT, 5V_DC or 5V_USB-TYPE-C can be used as external power supply in case current consumption of the EVAL and extensions boards exceeds allowed current on USB. In such condition it is still possible to use USB for communication for programming or debugging only.

In this case it is mandatory to power first using 5V_EXT, 5V_DC or 5V_USB-TYPE-C then connect the USB cable to the PC. Proceeding this way the enumeration succeed thanks to the external power source.

The following power sequence procedure must be respected:

- 1) Connect JP16 jumper according to the external 5V power source selected
- 2) Be sure that SB41 is removed
- 3) Connect the external power source according to JP16
- 4) Power ON the external power supply.
- 5) Check 5V GREEN LED LD8 is turned ON
- 6) Connect the PC to USB connector CN22

If this sequence is not respected, the board may be powered by V_{BUS} first from STLINK, and the following risk may be encountered:

- If more than 500mA current is needed by the board, the PC may be damaged or current can be limited by PC, As a consequence the board is not powered correctly.
- 500mA is requested at enumeration (since SB41 must be OFF) so there is risk that request is rejected and enumeration won't succeed if PC is not able to provide such current, consequently the board won't be powered (LED LD8 remains OFF).

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2.6.8 External power Supply Output

5V: When EVAL board is powered by USB, 5V_EXT or 5V_DC the 5V (CN6 pin 38) can be used as output power supply for an extension board plug on CN6. In this case, the maximum current of the power source specified in [Table 3: Power sources capability](#) needs to be respected.

3V3: CN5 pin 38, CN8 pin 38 or CN9 pin 38 can be used also as power supply output. The current is limited by the max current capability of the regulator U23 (ST1L05BPUR from STMicroelectronics) 1,3A max concerning EVAL board consumption + shield consumption..

2.6.9 Internal Power supply

For all general information concerning Design recommendations for STM32L5xx with internal SMPS, and design guide for ultra-low-power applications with performance, refer to ST-Design recommendation for L5SMPS application note (ANxxxx) at the www.st.com website

2.6.9.1 3V3

Regardless of the 5V power source a LDO U23 is used to deliver a fix 3V3 power supply with a current capability of 1.3A. This power source of 3V3 is shared betweenr EVAL board and expansion board.

2.6.9.2 VDD_ADJ

Regardless of the 5V power source a LDO U21 is used to deliver a adjust power voltage with a range of 1V7 to 3V6 and a current capability of 1.3A. This voltage is tune thanks to a potentiometer RV3. This adjustable voltage should be reserved for MCU debug capability.
Be careful to set and select the feature compatible with this adjustable voltage range before to update board accordingly.

2.6.9.3 1V8

Regardless of the 5V power source a LDO U35 is used to deliver a fix 1V8 voltage with a current capability of 150mA. This voltage source is mainly reserved for the Low power audio Codec. This one are not targeted to supply the MCU. To drive the MCU in low voltage, please to used the VDD_ADJ supply voltage.

The [table 13](#) detail the LDO and the associated HW SB configuration.

Table 13. LDO and the associated HW SB configuration.

Solder Bridge	Definition	Default Position	comment
SB27	LDO output for 3V3	ON	U23 able to provide main 3V3
		OFF	U23 disconnected, no 3V3 source
SB26	LDO output for VDD_ADJ	ON	U21 able to provide main VDD_ADJ: 1V7 to 3V6
		OFF	U23 disconnected, no 3V3 source
SB39	1V8	ON	U35 able to provide audio 1V8
		OFF	U35 disconnected, no audio 1V8 source

(Default configuration is shown in bold.)

The [table 14](#) detail the MCU power supplied configuration and the associated HW configuration.

Table 14. HW configuration for the MCU power supply voltage.

Jumper	Definition	Default Position	comment
JP11	VDD source selection Range 1V7<VDD<3V6	JP11[1-2]	VDD source is fix 3V3
		JP11[2-3]	VDD source is VDD_ADJ (1V7 to 3V6)
JP8	VDD_MCU selection: power measurement 1V7<VDD_MCU<3V6	JP8[1-2]	VDD_MCU power measurement selected
		JP8[2-3]	VDD_MCU directly connected to VDD, power measurement is bypass
JP4	VDDIO source selection Range 1V7<VDDIO<3V6	JP4[1-2]	VDDIO source is VDD_MCU
		JP4 OFF	VDDIO not supply or open for debug or current measurement
JP15	VBAT source selection Range 1V7<VBAT<3V6	JP15[1-2]	VBAT source is VDD
		JP15[2-3]	VBAT source is the external battery
JP9	VDDA source selection Range 1V7<VDDA<3V6	JP9[1-2]	VDDA source is VDD_MCU
		JP9[2-3]	VDDA source is fix 3V3
JP10	VREFP source selection Range 1V7<VREFP<3V6	JP10[1-2]	VREFP source is VDDA
		JP10 OFF	VREFP not supply or open for debug or current measurement
JP5	VDD_USB source selection Range 3V0<VDD_USB<3V6	JP5[1-2]	VDD_USB source is VDD_MCU (when USB is not used)
		JP11[2-3]	VDD_USB source is fix 3V3
JP6	VDD_SMPS source selection Range 2V0<VDDSMPS<3V6	JP6[1-2]	VDD_SMPS source is VDD_MCU
		JP11[2-3]	VDD_SMPS source is fix 3V3

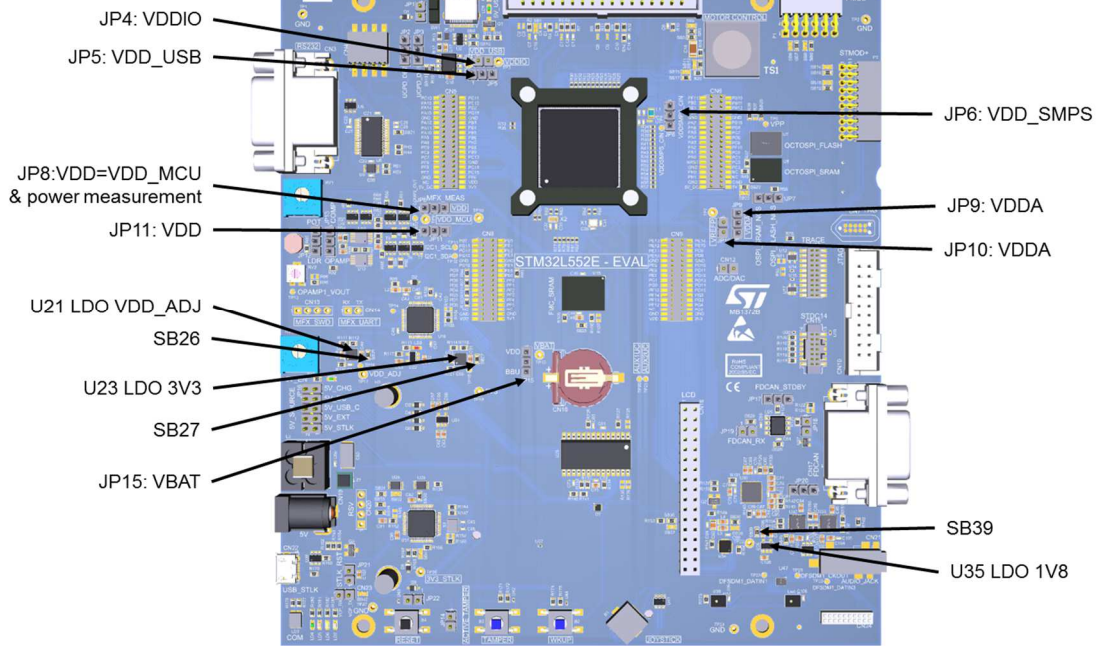
(Default configuration is shown in bold.)

The [figure 17](#) describe the MCU power supplied position on the EVAL board.

Figure 17. Jumper and SB for power sources.

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2.7 Clock references

Two clock references are available on STM32L552E-EVAL for STM32L552ZET6Q target microcontroller.

- 32.768KHz crystal X2, for embedded RTC
- 16MHz Crystal X1, for HSE clock generator. This one is optional

The main clock can also be generated using an internal RC oscillator.

The [table 15](#) describe the HW configuration for the 32.768KHz.

Table 15. HW configuration for the 32.768KHz.

IO	Solder bridge	Setting	Configuration
PC14	SB110	Open	PC14 OSC32_IN terminal is not routed to extension connector CN5. X2 is used as clock reference R62 connected.
		Closed	PC14 OSC32_IN is routed to extension connector CN5. R62 must be removed to X2 quartz circuit to not disturb clock reference or source from daughter board.
PC15	SB109	Open	PC15 OSC32_OUT terminal is not routed to extension connector CN5. X1 is used as clock reference. R63 connected
		Closed	PC15 OSC32_OUT is routed to extension connector CN5. R63 must be removed to X2 quartz circuit to not disturb clock reference or source from daughter board.

(Default configuration is shown in bold.)

The [table 16](#) describe the HW configuration for the 16MHz.

Table 16. HW configuration for the 16MHz.

IO	Solder bridge	Setting	Configuration
PH0	SB120	Open	PH0 OSC_IN terminal is not routed to extension connector CN6. X1 can be use as clock reference. SB121 should be open
		closed	PH0 OSC_IN is routed to extension connector CN6. R64 and SB121 must be removed, in order not to disturb clock reference or source on daughterboard.
	SB121	Open	PH0 OSC_IN terminal is not connected to STLINK MCO clock reference.
		closed	PH0 OSC_IN is connected to STLINK MCO clock reference. R64 and SB120 must be removed, in order not to disturb MCO clock reference
PH1	SB119	Open	PH1 OSC_OUT terminal is not routed to extension connector CN6. X1 can be use as clock reference.
		closed	PH1 OSC_OUT is routed to extension connector CN6. R65 must be removed, in order not to disturb clock reference or source on daughter board.

(Default configuration is shown in bold.)

2.8 Reset Source

The reset signal of STM32L552E-EVAL board is active low.

Sources of reset are:

- reset button B4 (BLACK button)
- JTAG/SWD connector CN10, ETM trace connector CN11, STDC14 connector CN15 and TAG connector CN7 (reset from debug tools)
- Through extension connector CN6 pin 27 (reset from daughter board)
- Embedded ST-LINK/V2-1
- Optional (JP22 not fitted) External RS232 interface.

2.9 Boot Option



At startup, a BOOT0 pin, nBOOT0 and NSBOOTADDx[24:0] / SECBOOTADD0(24:0) option bytes are used to select the boot memory address which includes:

- Boot from any address in user flash
- Boot from system memory bootloader
- Boot from any address in embedded SRAM
- Boot from Root security Service (RSS)

The BOOT0 value may come from the PH3_BOOT0 pin, connected to the BOOT switch SW1, or from an option bit depending on the value of a user option bit.

The [table 17](#) describe the HW configuration for the BOOT mode.

Table 17. HW configuration for the BOOT mode SW1.

IO	Switch	Setting	Description
PH3	SW1	0<->1 	BOOT0 line is tied low. STM32L552ZET6Q boots address define by user option bytes NSBOOTADD0 or SECBOOTADD0 according to Trustzone setting.
		0<->1 	BOOT0 line is tied high. STM32L552ZET6Q boots address define by user option bytes NSBOOTADD1 or RSS according to Trustzone setting.

(Default configuration is shown in bold.)

2.10 Audio

A codec CS42L51-CNZ is connected to SAI interface of STM32L552ZET6Q supports TDM feature of the SAI port. TDM feature offers to STM32L552ZET6Q the capability to stream stereo audio channels.

There are two digital microphones on board of STM32L552E-EVAL, and the STM32L552E-EVAL offer the possibility to connect a MEMS extension module.

2.10.1 Operating voltage.

The microphones are supply by VDD and are compatible with the VDD_MCU voltage range 1V71 to 3V6. The audio codec have two supplies:

- VDD_CODEC connected to VDD compatible with VDD_MCU low voltage 1V71 but limited to max 3V47 according to audio codec datasheet
- 1V8_CODEC dedicated 1V8 source provided by U35.

2.10.2 Audio Codec interface

The audio Codec interface is the MCU SAI1 and also a I2C1 interface

Table 18 describe the HW configuration for the audio codec interface SAI and I2C.

Table 18. HW configuration for the audio codec interface SAI and I2C.

IO	HW	Setting	Configuration
PF6	R219	ON	PF6 is used as SAI1_SD_B to interface the audio codec No other muxing
PF7	R216	ON	PF7 is used as SAI1_MCLK_B to interface the audio codec No other muxing
PF8	R217	ON	PF8 is used as SAI1_SCK_B to interface the audio codec No other muxing
PF9	SB98	ON	PF9 is used as SAI1_FS_B to interface the audio codec
		OFF	PF9 is not used for audio codec PF9 can be used for Motor control
PA10	R202	ON	PA10 is used as SAI1_SD_A to interface the audio codec No other muxing
PG13	R232	ON	PG13 is used as I2C1_SDA to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+
PG14	R228	ON	PG14 is used as I2C1_SCL to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+

2.10.3 Digital microphones

U39 and U40 on board of STM32L552E-EVAL are MP34DT01TR MEMS digital omnidirectional microphones providing PDM (pulse density modulation) outputs. To share the same data line, their outputs are interlaced. The combined data output of the microphones is routed to STM32L552ZET6Q terminals, thanks to the integrated input digital filters. The microphones are supply with programmable clock generated directly by STM32L552ZET6Q.

The STM32L552ZET6Q DFSDM interface is shared and exclusive between the embedded microphone U39 and U40, the extension module on connector CN24, the STMOD+ connector P2 and with the two Smart Sensor STPMS2 U32 and U33.

Table 19 describe the HW configuration for the DFSDM interface.

Table 19. HW configuration for the DFSDM interface.

IO	HW	Setting	Configuration
-	CN24	NO external module	The switch U47 connect directly the DFSDM interface to the on board MEMS U39 and U40 (signal DETECTn low)
		External module plug on CN24	The switch U47 disconnect DFSDM to the on board MEMS U39 and U40, and connect it to CN24 connector (signal DETECTn switch HIGH by the module)
-	P2	NO external module	The switch U47 connect directly the DFSDM interface to the on board MEMS U39 and U40 (signal DETECTn low)
		External module plug on P2	It is recommended to force signal DETECTn CN24 pin 10 to VDD CN24 pin2 to disconnect DFSDM to the on board MEMS U39 and U40, to use dit on P2 module
PD6	R155	ON	DFSDM1_DATIN1 connected to U32 STPMS2L for power metering
		OFF	DFSDM1_DATIN1 NOT connected to U32 STPMS2L for power metering.
PF10	R154	ON	DFSDM1_CKOUT connected to U32 STPMS2L for power metering and U33 STPMS2L for Sigma Delta measurement
		OFF	DFSDM1_CKOUT NOT connected to U32 STPMS2L for power metering and U33 STPMS2L for Sigma Delta measurement
PC7	R157	ON	DFSDM1_DATIN3 connected to U33 STPMS2L for Sigma Delta measurement
		OFF	DFSDM1_DATIN3 NOT connected to U33 STPMS2L for Sigma Delta measurement

(Default configuration is shown in bold.)

2.10.4 Headphones outputs

The STM32L552E-EVAL evaluation board can drive a stereo headphones. The STM32L552ZET6Q sends up stereo audio channels, via its SAI1 TDM port, to the codec device. The codec device converts the digital audio stream to stereo analog signals. It then boosts them for direct drive of headphones connecting to 3.5 mm stereo jack receptacles on the board, CN21.

The audio codec is set by an I²C-bus. The address is a 7 bits address: and a bit for read/write: (hight for read, low for write). The AD0 pin connected to GND give the least significant bit address: address of the audio codec is 0b1001010x: 0x94 for write, 0x95 to read.

2.10.5 Audio Jack connector

Figure 18 shows the Audio jack connector pinout CN21.

Figure 18. Audio Jack connector pinout CN21.

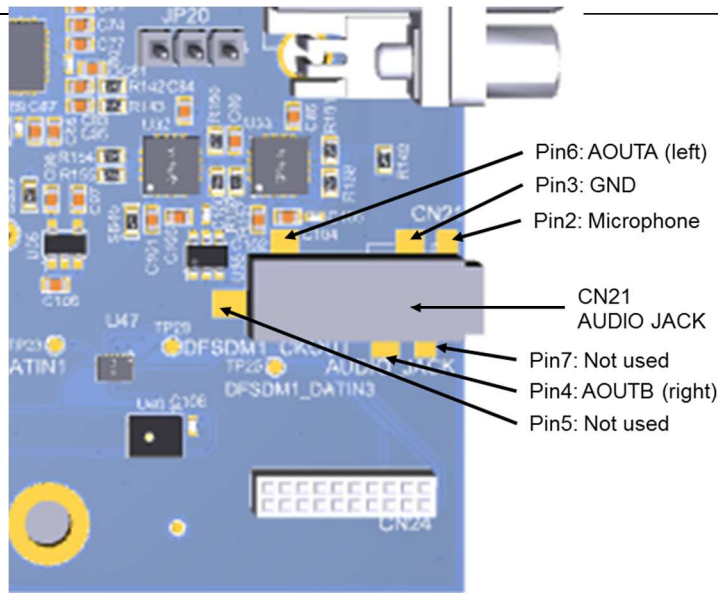


Table 20 describe the Audio jack connector pinout CN21

Table 20. Audio Jack connector pinout CN21.

Pin	Board function	Audio Codec Pin
2	MIC IN	MICIN1
3	GND	GND
4	AOUTB	AOUTB
5	NA	NA
6	AOUTA	AOUTA
7	NA	NA

2.10.6 IO restriction to other features

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the audio features:

The AUDIO CODEC cannot be operated simultaneously with motor control.

The MEMS DFSDM cannot be operated simultaneously with DFSDM of EXT MEMS module (CN24).

The MEMS DFSDM cannot be operated simultaneously with DFSDM of STMOD+.

The MEMS DFSDM cannot be operated simultaneously with DFSDM of STMPS2 U32, U33.

2.11 USB TYPE C FS port

The STM32L552E-EVAL board supports USB full-speed (FS) communication. The USB connector CN1 is a USB TYPE C connector.

The STM32L552E-EVAL board supports USB TYPE C SINK mode only.

A green LED LD1 lits up when VBUS is powered by an USB host when the STM32L552E-EVAL board works as a USB device.

2.11.1 Operating voltage.

The STM32L552E-EVAL board supports USB voltage 5V: 4.75V to 5.25V.

2.11.2 USB FS device

When a “USB host” connection to the CN1 TYPE C USB connector of STM32L552E-EVAL is detected, the STM32L552E-EVAL board starts behaving as “USB device”. Depending on the powering capability of the USB host, the board can take power from VBUS terminal of CN1. In the board schematic diagrams, the corresponding power voltage line is called 5V_VBUS_C.

[Section 2.6 Power Supply](#) provides information on how to used powering option.

[Table 21](#) describe the HW configuration for the USB interface.

Table 21. HW configuration for the USB interface.

IO	HW	Setting	Configuration
PA11	R201	ON	PA11 used as USB_FS_N diff pair interface No other muxing
PA12	R199	ON	PA12 used as USB_FS_P diff pair interface No other muxing

(Default configuration is shown in bold.)

2.11.3 UCPD

The USB TYPE C introduce the USB Power Delivery feature, the STM32L552E-EVAL support the FRS, the dead battery and SINK mode.

In addition to the IO directly connected to the USB TYPE connector, 5 IOs are also used for UCPD configuration: Configuration Channel (CCx), VBUS-SENSE and UCPD Dead Battery (DBCCx) feature.

- Configuration Channel IO: UCPD_CCx: These signals are connected to the associated CCx line of the USB TYPE C connector for the configuration channel lines (CCx) to select the USB TYPE C current mode. STM32L552E-EVAL support only SINK current mode.
- Dead Battery IO: UCPD_DBx: These signals are connected to the associated CCx line of the USB TYPE C connector to support the dead battery feature. If dead battery feature is not requested, these IO should be connected to GND.

[Table 22](#) describe the HW configuration for the UCPD feature.

Table 22. HW configuration for the UCPD feature.

IO	HW	Setting	Configuration
PA15	SB73	ON	PA15 used as USB_CC1 (SB10 ON)

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		OFF	PA15 NOT used for USB. PA15 can used for JTAG JTDI
PB15	R196	ON	PB15 used as USB_CC2 (SB4 ON) No other muxing
PA4	SB107	ON	PA4 used as VBUS_SENSE
		OFF	PA4 NOT used for USB. PA4 can used for STMOD+, ADC/DAC or Motor control
PB5	JP2	JP2[1-2]	IO USB_DB1 connected to USB_CC1 (PA15): Dead battery supported
		JP2[2-3]	IO USB_DB1 connected to GND: Dead battery not supported
PB14	JP3	JP3[1-2]	IO USB_DB2 connected to USB_CC2 (PB15): Dead battery supported
		JP3[2-3]	IO USB_DB2 connected to GND. Dead battery not supported

(Default configuration is shown in bold.)

2.11.4 USB TYPE C connector

Figure 19 shows the USB TYPE C connector pinout CN1.

Figure 19. USB TYPE C connector pinout CN1.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND

Table 23 describe the USB TYPE C connector pinout CN1

Table 23. USB_TYPE_C connector pinout CN1.

STM32 pin	Signal name	Pin	Pin	Signal name	STM32 pin
-	GND	A1	B12	GND	-
-	TX1+	A2	B11	RX1+	-
-	TX1-	A3	B10	RX1-	-
5V_VBUS_C	VBUS	A4	B9	VBUS	5V_VBUS_C
PA15	CC1	A5	B8	SBU2	-
PA12	D+	A6	B7	D-	PA11
PA11	D-	A7	B6	D+	PA12
--	SBU1	A8	B5	CC2	PB15
5V_VBUS_C	VBUS	A9	B4	VBUS	5V_VBUS_C
-	RX2-	A10	B3	TX2-	-
-	RX2+	A11	B2	TX2+	-
-	GND	A12	B1	GND	-

2.11.5 IO restriction to other features

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the USB features:

The USB UCPD cannot be operated simultaneously with full JTAG (JTDI).

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- If PA15 is used as USB_CC1 (USB peripheral), in this case JTDI cannot be used for JTAG peripheral.

The USB UCPD cannot be operated simultaneously with COMPARATOR.

The USB UCPD impose some restrictions to the STMOD+.

- If PB5 is used as USB_DB1 (USB peripheral), in this case COMP2_OUT cannot be used for COMPARATOR feature, and SPI3_MOSI2 cannot be used for STMOD+ feature.

2.12 RS-232 port

The STM32L552E-EVAL board offers one RS-232 communication port. The RS-232 communication port uses the DB9 male connector CN3.

2.12.1 Operating voltage.

The RS-232 transceiver U6 is supply by the fix 3V3 power voltage. To support MCU 1V8 IO configuration, a level shifter U9 is used for the MCU output IO to reach the transceiver Voltage Input high level (VIH).

In this configuration the RS-232 interface is fully compatible with the MCU range 1.71V to 3.6V

2.12.2 RS-232 interface.

The RS-232 interface can be connect to either

- MCU USART3 in 2 wires mode RX, TX
- MCU LPUART1 in 4 wires mode RX, TX, RTS, CTS.

Table 24 describe the HW configuration for the RS-232 interface.

Table 24. HW configuration for the RS-232 interface.

IO	Solder bridge	Setting	Configuration
PG7	SB49	ON	PG7 LPUART1_TX is connected to RS-232 transceiver SB48 and SB77 should be not fitted
		OFF	PG7 LPUART1_TX is NOT connected to RS-232 transceiver PG7 can be used for STLINK_VCP
PG8	SB51	ON	PG8 LPUART1_RX is connected to RS-232 transceiver SB50 and SB71 should be not fitted
		OFF	PG8 LPUART1_RX is NOT connected to RS-232 transceiver PG8 can be used for STLINK_VCP
PB10	SB77	ON	PB10 USART3_TX is connected to RS-232 transceiver SB49 and SB78 should be not fitted
		OFF	PB10 USART3_TX is NOT connected to RS-232 transceiver PB10 can be used for STLINK_VCP
PB11	SB71	ON	PB11 USART3_RX is connected to RS-232 transceiver SB51 and SB75 should be not fitted
		OFF	PB11 USART3_RX is NOT connected to RS-232 transceiver PB11 can be used for STLINK_VCP
PB13	R190 / R44	ON	PB13: LPUART1_CTS is connect to RS232 transceiver
PG6	R203	ON	PG6: LPUART1_RTS is connect to RS232 transceiver

(Default configuration is shown in bold.)

Figure 20 shows the RS-232 connector pinout CN3.

Figure 20. RS-232 connector pinout CN3.

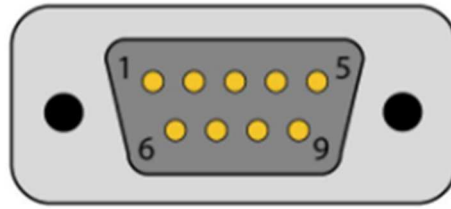


Table 25 describe the RS-232 connector pinout CN3

Table 25. Audio Jack connector pinout CN3.

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
NC	NC	1	6	NC	NC
PG8/PB11	LP or USART_RX	2	7	LPUART1_RTS	PG6
PG7/PB10	LP or USART_TX	3	8	LPUART1_CTS	PB13
NC	NC	4	9	NC	NC
GND	GND	5			

2.12.3 IO restriction to other features

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the RS-232 features:

The RS-232 cannot be operated simultaneously with the STLINK-VCP.

The RS-232 cannot be operated simultaneously with the STMOD+_UART.

2.13 microSD card

The CN25 slot for microSD card is routed to STM32L552ZET6Q SDIO port. This interface is compliance with SD Memory Card Specification Version 4.1: SDR104 SDMMC_CLK speed limited to maximum allowed IO speed. UHS-II mode is not supported.

2.13.1 Operating voltage.

The SDCARD interface is only compatible with 3V3 voltage range: 2V7 to 3V6.

The SDCARD interface not support the MCU low voltage1V8 range

2.13.2 SD card interface.

The SD card interface is used in 4 data line D[0:3] one CLK, one CDM and a card detection signal.

Table 26 describe the HW configuration for the SDIO interface.

Table 26. HW configuration for the SDIO interface.

IO	Solder bridge	Setting	Configuration
PG10	SB61	ON	PG10 is connected to SDCARD DETECT
		OFF	PG10 is connected to SDCARD DETECT PG10 can be used for STMOD+
PC8	SB56	ON	PC8 is connected to SDCARD SDIO1_D0
		OFF	PC8 is connected to SDCARD SDIO1_D0 PC8 can be used for Motor control
PC9	SB58	ON	PC9 is connected to SDCARD SDIO1_D1
		OFF	PC9 is connected to SDCARD SDIO1_D1 PC9 can be used for TRACE ETM
PC10	SB67	ON	PC10 is connected to SDCARD SDIO1_D2
		OFF	PC10 is connected to SDCARD SDIO1_D2 PC10 can be used for TRACE ETM
PC12	SB63	ON	PC12 is connected to SDCARD SDIO1_CLK
		OFF	PC12 is connected to SDCARD SDIO1_CLK PC12 can be used for TRACE ETM or STMOD+
PC11	R187	ON	PC11 is connected to SDCARD SDIO1_D3 No other muxing
PD2	R188	ON	PD2 is connected to SDCARD SDIO1_CMD No other muxing

(Default configuration is shown in bold.)

Figure 21 shows the SDCARD connector pinout CN25.

Figure 21. SDCARD connector pinout CN25.

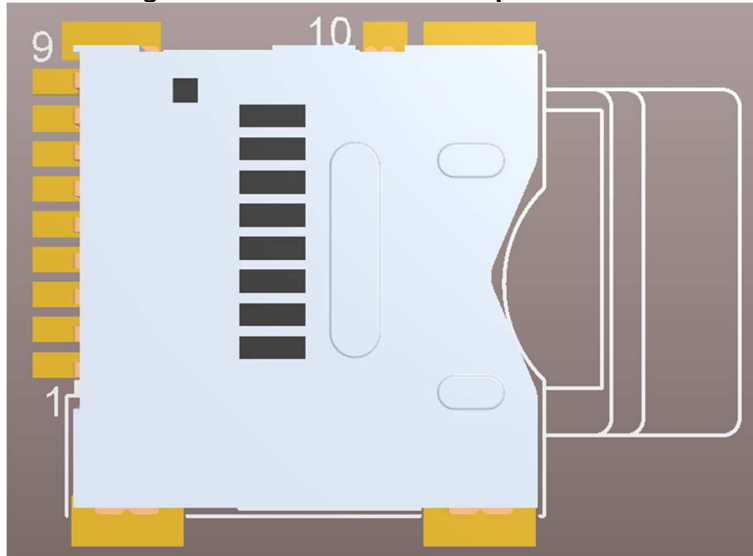


Table 27 describe the SDCARD connector pinout CN25

Table 27. SDCARD connector pinout CN25.

Pin	Board function	STM32 pin
1	SDIO1_D2	PC10
2	SDIO1_D3	PC11
3	SDIO1_CMD	PD2
4	VDD_SDCARD	-
5	SDIO1_CLK	PC12
6	GND	-
7	SDIO1_D0	PC8
8	SDIO1_D1	PC9
9	GND for DETECT pin	-
10	SDCARD_DETECT active LOW	PG10

2.13.3 IO restriction to other features

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the SDIO features:

The microSD card cannot be operated simultaneously with motor control.

The microSD card cannot be operated simultaneously with TRACE ETM 4bits

The microSD card cannot be operated simultaneously with STMOD+ SPI

2.14 FDCAN

The STM32L552E-EVAL board supports one FDCAN compliant with ISO-11898-1 version 2.0 part A,B. The CN17 DB9 male connector is available as FDCAN interface.

2.14.1 Operating voltage.

A 3V3 CAN transceiver is fitted between the CN17 connector and the CAN controller port of STM32L552ZET6Q.

In this configuration the RS-232 interface is compatible with the MCU range 1V8 to 3V6. (low voltage 1V71 not fit with the CAN transceiver specification).

2.14.2 FDCAN interface.

The JP17 jumper allows selecting one of high-speed, standby and slope control modes of the CAN transceiver. The JP18 jumper can fit a CAN termination resistor in. The JP19 is used to connected CAN transceiver avoiding unknown signals from CAN transceiver.

Table 28 describe the HW configuration for the FDCAN.

Table 28. HW configuration between MCU and FDCAN transceiver.

IO	HW	Setting	Configuration
-	JP17	JP17[1-2]	CAN transceiver operates in high-speed mode
		JP17[2-3]	CAN transceiver is in standby mode
-	JP18	ON	Termination resistor fitted on CAN physical link
		OFF	No termination resistor on CAN physical link
PB8	JP19	ON	PB8: CAN_RX is used from STM32L552ZET6Q terminal
		OFF	PB8 is not used for CAN transceiver. No other muxing
PB9	R210	ON	PB9: CAN_TX is used as CAN_TX
		OFF	PB9 is not used for CAN transceiver. No other muxing

(Default configuration is shown in bold.)

Figure 22 shows the FDCAN connector pinout CN17.

Figure 22. FDCAN connector pinout CN17.

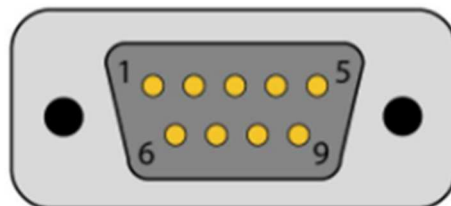


Table 29 describe the FDCAN interface and connector pinout CN17

Table 29. FDCAN interface and connector pinout CN17.

CAN transceiver	Board function	Pin	Pin	Board function	CAN transceiver
-	NC	1	6	GND	-
CANL	CANL	2	7	CANH	CANH
GND	GND	3	8	NC	-
-	NC	4	9	NC	-
-	NC	5			

2.14.3 IO restriction to other features

There are no limitation for the CAN interface link to the IO muxing.

2.15 SMARTCARD

The STM32L552E-EVAL board supports one smartcard interface. The CN26 smartcard connector is used as card reader.

2.15.1 Operating voltage.

A smartcard interface is used between the card reader connector CN26 and the smartcard controller port of STM32L552ZET6Q.

The smartcard interface is only compatible from 2V7 to 3V6 MCU range. Low power MCU 1V8 is not supported by the smartcard interface.

2.15.2 SmartCard interface.

The smartcard interface is connected for some IO to the STM32L552ZET6Q and for other IO to the MFX IO expander.

Table 30 describe the HW configuration for the smartcard interface.

Table 30. HW configuration for the smartcard interface.

IO	Solder bridge	Setting	Configuration
PA9	SB65	ON	PA9 is connected to Smarcard interface as SMARTCARD_IO
		OFF	PA9 is NOT connected to smartcard interface PA9 can be used for Motor control
PA8	R205	ON	PA8 is connected to Smarcard interface as SMARTCARD_CLK No other muxing
MFX_IO6	-	-	MFX_IO6 used as SMARTCARD_OFF No other muxing
MFX_IO7	-	-	MFX_IO7 used as SMARTCARD_RST No other muxing
MFX_IO9	-	-	MFX_IO9 used as SMARTCARD_CMDVCC No other muxing
MFX_IO10	-	-	MFX_IO10 used as SMARTCARD_3/5V No other muxing

(Default configuration is shown in bold.)

Figure 23 shows the smartcard connector pinout CN26.

Figure 23. Smartcard connector pinout CN26.

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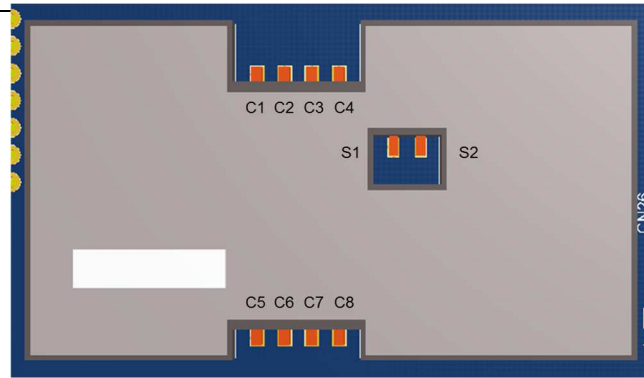


Table 31 describe the Smartcard interface U26 and connector pinout CN26

Table 31. smartcard interface U26 and connector pinout CN26.

Pin	Board function	U26 Smartcard interface pin
C1	VCC: Card supply	U26-17
C2	RST: Card Reset	U26-16
C3	CLK: Card CLK	U26-15
C4	NC	-
C5	GND: CARD GND	U26-14
C6	NC	-
C7	I/O CARD DATA	U26-11
C8	NC	-
S1	GND: CAR GND	GND
S2	DETECT: CARD-Detect (LOW)	U26-9

2.15.3 IO restriction to other features

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the Smartcard features:

The SmartCard card cannot be operated simultaneously with motor control.

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2.16 User LEDs

Four general-purpose color LEDs (LD4, LD5, LD6, LD7) are available as light indicators. Each LED is in light-emitting state with low level of the corresponding ports.

Two users LED, LD4 green LED and LD5 red LED are directly connected to the STM32L552ZET6Q.

The two other users LED LD6 yellow LED and LD7 orange LED are connected to the MFX IO expander.

2.16.1 Operating voltage.

As LEDs are drive by IO LOW level, LED are compatible with VDD_MCU 1V8.

2.16.2 LED interface.

Table 32 describe the HW configuration for the LED interface.

Table 32. HW configuration for the LED interface.

IO	Solder bridge	Setting	Configuration
PB3	SB82	ON	PB3 is connected to the GREEN LED LD4. Active Low
		OFF	PB3 is NOT connected to LED PB3 can be used for JTAG
PD3	R102	ON	PD3 is connected to the RED LED LD5: Active Low No other muxing
MFX_IO11	-	-	MFX_IO11 is connected to YELLOW LED: LD6. Active Low No other muxing
MFX_IO13	-	-	MFX_IO13 is connected to ORANGE LED LD7. Active Low No other muxing

(Default configuration is shown in bold.)

2.16.3 IO restriction to other features

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the LED features:

The GREEN LED IO cannot be operated simultaneously with JTAG SWO.

2.17 Physical input devices: BUTTONS

The STM32L552E-EVAL board provides a number of input devices for physical human control. These are:

- four-way joystick controller with select key (B1)
- wake-up button (B2)
- Tamper button (B3)
- Reset button (B4)

2.17.1 Operating voltage.

Input device for physical human control are connected to VDD or are reference to GND. So input device are compatible with VDD_MCU range 1V71 to 3V6 .

2.17.2 Physical input IO interface.

Table 33 describe the HW configuration for the physical user interface.

Table 33. HW configuration for the physical user interface.

IO	HW	Setting	Configuration
PA1	SB114	ON	PA1 is connected to TAMPER KEY button B3 as TAMPER function (active High)
		OFF	PA1 is NOT connected to TAMPER KEY PA1 can be used for OPAMP, STMOD+ or Motor control
PC13	JP14	OFF	PC13 connected to Wakeup button B2 (active High)
		ON	Active TAMPER function between PA1 and PC13
NRST	-	-	Button RESET source (active LOW)
MFX_IO2		-	JOY_LEFT: Joystick left direction connected to B1 pin1
MFX_IO0		-	JOY_SEL: Joystick selection connected to B1 pin2
MFX_IO1		-	JOY_DOWN: Joystick down direction connected to B1 pin3
MFX_IO4		-	JOY_UP: Joystick up direction connected to B1 pin4
MFX_IO3		-	JOY_RIGHT: Joystick right direction connected to B1 pin6

(Default configuration is shown in bold.)

2.17.3 Limitations

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the Physical interface features:

The TAMPER KEY function cannot be operated simultaneously with TAMPER LOOP, OPAMP, STMOD+ or motor control function, .

The WAKEUP Button function cannot be operated simultaneously with TAMPER LOOP function.

2.18 Operational amplifier and comparator

The STM32L552E-EVAL board provides a number of input devices for physical human control. These are:

- 10 kΩ potentiometer (RV1)
- light-dependent resistor, LDR (R73).

The potentiometer and the light-dependent resistor can be routed, mutually exclusively, to either PB4 or to PA0 port of STM32L552ZET6Q.

2.18.1 Operating voltage.

Input device for physical human control are connected to VDD or are reference to GND. So input device are compatible with VDD_MCU range 1V71 to 3V6 .

2.18.2 Operational amplifier

STM32L552ZET6Q provides two on-board operational amplifiers, one of which, OpAmp1, is made accessible on STM32L552E-EVAL. OpAmp1 has its inputs and its output routed to I/O ports.

Table 34 describe the HW configuration for the OPAMP interface

Table 34. HW configuration for the OPAMP interface.

IO	HW	Setting	Configuration
PA0	SB116	ON	PA0 is used as OPAMP1_INP and connected to JP13 pin3
		OFF	PA0 is NOT used as OPAMP PA0 can be used for MFX, STMOD+ or Motor control
PA1	SB111	ON	PA1 is used as OPAMP1_INM and connected to R98/RV2
		OFF	PA1 is NOT used as OPAMP PA1 can be used for MFX, STMOD+ or Motor control
PA3	SB84	ON	PA3 is used as OPAMP1_VOUT and connected to TP13
		OFF	PA3 is NOT used as OPAMP PA3 can be used for OCTOSPI , or Motor control

The non-inverting input PA0 is accessible on the pin 3 of the JP13 jumper header. On top of the possibility of routing either of the potentiometer or LDR to PA0, an external source can also be connected to it, using the terminal 3 of JP13.

The PA3 output of the operational amplifier can be accessed on test point TP13. Refer to the schematic of the STM32L552E_EVAL.

The gain of OpAmp1 is determined by the ratio of the variable resistor RV2 and the resistor R98, as shown in the following equation:

$$\text{Gain} = 1 + \text{RV2}/\text{R98}$$

With the RV2 ranging from 0 to 10 kΩ and R98 being 1 kΩ, the gain can vary from 1 to 11.

The R92 resistor in series with PA0 is beneficial for reducing the output offset.

Table 35 describe the Jumper configuration to enable the LDR or the potentiometer to OPAMP1 function.

Table 35. Jumper configuration to enable the LDR or the potentiometer to OPAMP1 function.

HW	Setting	Configuration
JP12/JP13	JP12[1-2] / JP13[2-3]	Potentiometer is routed to pin OPAMP1_INP PA0 of STM32L552ZET6Q
	JP12[2-3] / JP13[2-3]	LDR is routed to pin OPAMP1_INP PA0 of STM32L552ZET6Q

2.18.3 Comparator

STM32L552ZET6Q provides two on-board comparators, one of which, Comp2, is made accessible on STM32L552E-EVAL. Comp2 has its non-inverting input and its output.

Table 36 describe the HW configuration for the comparator interface

Table 36. HW configuration for the comparator interface.

IO	HW	Setting	Configuration
PB4	SB92	ON	PB4 is used as COMP2_INP and connected to JP13 pin1
		OFF	PB4 is NOT used as COMP PB4 can be used for JTAG or STMOD
PB5	SB103	ON	PB5 is used as COMP2_OUT and connected to TP8
		OFF	PB5 is NOT used as COMP PB5 can be used for USB or STMOD+

The input is accessible on the pin 1 of the JP13 jumper header. On top of the possibility of routing either the potentiometer or LDR to PB4, an external source can also be connected to it, using the terminal 1 of JP13.

The PB5 output of the comparator can be accessed on test point TP8. Refer to the schematic of the STM32L552E_EVAL.

Table 37 describe the Jumper configuration to enable the LDR or the potentiometer to COMP2 function.

Table 37. Jumper configuration to enable the LDR or the potentiometer to COMP2 function.

HW	Setting	Configuration
JP12/JP13	JP12[1-2] / JP13[1-2]	Potentiometer is routed to pin PB4 of STM32L552ZET6Q
	JP12[2-3] / JP13[1-2]	LDR is routed to pin PB4 of STM32L552ZET6Q

(Default configuration is shown in bold.)

2.18.4 Limitations

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the OPAMP and COMP features:

The OPAMP function cannot be operated simultaneously with TAMPER KEY, MFX, OCTOSPI, STMOD+ or Motor control function

The COMP function cannot be operate simultaneously with JTAG STMOD+ and USB UCPD function.

2.19 Analog input, output, VREF

STM32L552ZET6Q provides on-board analog-to-digital converter, ADC and digital-to-analog converter, DAC. The port PA4 can be configured to operate either as ADC input or as DAC output. PA4 is routed to the two-way header CN12 allowing to fetch signals to or from PA4 or to ground it by fitting a jumper into CN12.

2.19.1 ADC/DAC IO interface

Parameters of the ADC input low-pass filter formed with R233 and C141 can be modified by replacing these components according to application requirements.

Similarly, parameters of the DAC output low-pass filter formed with R224 and C141 can be modified by replacing these components according to application requirements.

The VREFP terminal of STM32L552ZET6Q is used as reference voltage for both ADC and DAC. By default, it is routed to VDDA through a jumper fitted into the two-way header JP10. The jumper can be removed and an external voltage applied to the terminal 2 of JP10, for specific purposes.

Table 38 describe the HW configuration for the ADC/DAC interface

Table 38. HW configuration for the ADC/DAC interface.

IO	HW	Setting	Configuration
PA4	SB124	ON	PA4 is used as ADC/DAC and connected to CN12 pin1
		OFF	PA4 is NOT used as ADC/DAC PA4 can be used for USB, STMOD+, or Motor control
VREFP	JP10	ON	VDDA used as ADC/DAC power supply
		OFF	ADC/DAC not powered

Figure 24 shows the ADC/DAC connector pinout CN12.

Figure 24. ADC/DAC connector pinout CN12.



Table 39 describe the ADC/DAC interface and connector pinout CN12

Table 39. ADC/DAC interface and connector pinout CN12.

STM32 pin	Signal name	Pin	Pin	Signal name	STM32 pin
PA4	ADC/DAC	1	2	GND	-

2.19.2 Limitations

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the PMOD Button features:

The ADC/DAC cannot be operated simultaneously with UCPD function

The ADC/DAC cannot be operated simultaneously with STMOD+ function

The ADC/DAC cannot be operated simultaneously with MotorControl function

2.20 SRAM device

IS61WV102416BLL, a 16-Mbit static RAM (SRAM), 1 M x16 bit, is fitted on the STM32L552E-EVAL main board, in U15 position.

2.20.1 Operating voltage.

The SRAM is only functional to the voltage range 2V4 to 3V6 (according to the SRAM datasheet).

In this case the SRAM not support the low voltage MCU 1V8 .

2.20.2 SRAM interface.

The STM32L552E-EVAL main board as well as the addressing capabilities of FMC allow hosting SRAM devices up to 32 Mbytes. This is the reason why the schematic of the STM32L552E-EVAL mentions several SRAM devices

The SRAM device is attached to the 16-bit data bus and accessed with FMC. The base address is 0x6000 0000, corresponding to NOR/SRAM1 bank1. The SRAM device is selected with FMC_NE1 chip select. FMC_NBL0 and FMC_NBL1 signals allow selecting 8-bit and 16-bit data word operating modes.

Table 40 describe the HW configuration for the SRAM interface

Table 40. HW configuration for the SRAM interface.

IO	HW	Setting	Configuration
PD7	R94	ON	PD7 is used as FMC_NE1 and connected to SRAM
PD5	R239	ON	PD5 is used as FMC_NWE and connected to SRAM and LCD
PD4	R101	ON	PD4 is used as FMC_NOE and connected to SRAM and LCD
PE0	R227	ON	PE0 is used as FMC_NBL0 and connected to SRAM
PE1	R226	ON	PD4 is used as FMC_NBL1 and connected to SRAM
PD14	R23	ON	PD14 is used as FMC_D0 and connected to SRAM and LCD
PD15	R22	ON	PD15 is used as FMC_D1 and connected to SRAM and LCD
PD0	R33	ON	PD0 is used as FMC_D2 and connected to SRAM and LCD
PD1	R35	ON	PD1 is used as FMC_D3 and connected to SRAM and LCD
PE7	R48	ON	PE7 is used as FMC_D4 and connected to SRAM and LCD
PE8	R46	ON	PE8 is used as FMC_D5 and connected to SRAM and LCD
PE9	R45	ON	PE9 is used as FMC_D6 and connected to SRAM and LCD
PE10	R43	ON	PE10 is used as FMC_D7 and connected to SRAM and LCD
PE11	R41	ON	PE11 is used as FMC_D8 and connected to SRAM and LCD
PE12	R40	ON	PE12 is used as FMC_D9 and connected to SRAM and LCD
PE13	R38	ON	PE13 is used as FMC_D10 and connected to SRAM and LCD
PE14	R36	ON	PE14 is used as FMC_D11 and connected to SRAM and LCD
PE15	R34	ON	PE15 is used as FMC_D12 and connected to SRAM and LCD
PD8	R29	ON	PD8 is used as FMC_D13 and connected to SRAM and LCD
PD9	R28	ON	PD9 is used as FMC_D14 and connected to SRAM and LCD
PD10	R27	ON	PD10 is used as FMC_D15 and connected to SRAM and LCD
PF0	R77	ON	PF0 is used as FMC_A0 and connected to SRAM
PF1	R78	ON	PF1 is used as FMC_A1 and connected to SRAM
PF2	R79	ON	PF2 is used as FMC_A2 and connected to SRAM
PF3	R80	ON	PF3 is used as FMC_A3 and connected to SRAM
PF4	R81	ON	PF4 is used as FMC_A4 and connected to SRAM
PF5	R82	ON	PF5 is used as FMC_A5 and connected to SRAM
PF12	R57	ON	PF12 is used as FMC_A6 and connected to SRAM
PF13	R56	ON	PF13 is used as FMC_A7 and connected to SRAM
PF14	R55	ON	PF14 is used as FMC_A8 and connected to SRAM
PF15	R54	ON	PF15 is used as FMC_A9 and connected to SRAM
PG0	R52	ON	PG0 is used as FMC_A10 and connected to SRAM

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PG1	R50	ON	PG1 is used as FMC_A11 and connected to SRAM
PG2	R21	ON	PG2 is used as FMC_A12 and connected to SRAM
PG3	R32	ON	PG3 is used as FMC_A13 and connected to SRAM
PG4	R31	ON	PG4 is used as FMC_A14 and connected to SRAM
PG5	R30	ON	PG5 is used as FMC_A15 and connected to SRAM
PD11	R26	ON	PD11 is used as FMC_A16 and connected to SRAM
PD12	R25	ON	PD12 is used as FMC_A17 and connected to SRAM
PD13	R24	ON	PD13 is used as FMC_A18 and connected to SRAM
PE3	R66	ON	PE3 is used as FMC_A19 and connected to SRAM
PE4	R67	ON	PE4 is used as FMC_A20 and connected to SRAM

(Default configuration is shown in bold.)

2.20.3 Limitations

By default, only a SRAM of 16Mbits is present on the STM32L552E_EVAL board. An update of the SRAM (footprint compatible) could be done to increase the memory up to 32Mbits A[0-20].

FMC interface is shared with LCD.

2.21 Octo-SPI memory device

2.21.1 Octo-SPI FLASH memory device

MX25LM51245GXDI00, a 512-Mbit Octo-SPI Flash memory device, is fitted on the STM32L552E-EVAL main board, in U7 position. It allows evaluating STM32L552ZET6Q Octo-SPI interface.

MX25LM51245GXDI00 can operate in single transfer rate (STR) and double transfer rate (DTR) modes

2.21.2 Octo-SPI SRAM device

IS66WVH8M8BLL-100BLI, a 64-Mbit self-refresh Static Random Access Memory (SRAM) device with a HyperBus interface, is fitted on the STM32L552E-EVAL main board, in U8 position. It allows evaluating STM32L552ZET6Q Octal-SPI interface with Hyper bus.

2.21.3 Operating voltage

Voltage of Octo-SPI Flash memory device MX25LM51245GXDI00 is in the range of 2.7 V to 3.6 V.

Voltage of Octo-SPI SRAM device IS66WVH8M8BLL-100BLI is in the range of 2.7 V to 3.6 V.

In this case the OCTO-SPI memory not support the low voltage MCU 1V8 .

2.21.4 Octo-SPI IO interface

Table 41 describe the HW configuration for the OCTOSPI interface

Table 41. HW configuration for the OCTOSPI interface.

IO	Resistor	Setting	Configuration
PA2	R208	ON	PA2 is connected to Octo-SPI FLASH as NCS
		OFF	PA2 is NOT connected to Octo-SPI FLASH PA2 can be used for Motor control
PA3	R206	ON	PA3 is connected to Octo-SPI FLASH as CLK
		OFF	PA3 is NOT connected to Octo-SPI FLASH PA3 can be used for OPAMP or Motor control
PA6	R204	ON	PA6 is connected to Octo-SPI FLASH as IO3
		OFF	PA6 is NOT connected to Octo-SPI FLASH PA6 can be used for Motor control
PA7	R198	ON	PA7 is connected to Octo-SPI FLASH as IO2
		OFF	PA7 is NOT connected to Octo-SPI FLASH PA7 can be used for Motor control
PB0	R195	ON	PB0 is connected to Octo-SPI FLASH as IO1
		OFF	PB0 is NOT connected to Octo-SPI FLASH PB0 can be used for Motor control
PB1	R194	ON	PB1 is connected to Octo-SPI FLASH as IO0
		OFF	PB1 is NOT connected to Octo-SPI FLASH PB1 can be used for Motor control
PB2	R189	ON	PB2 is connected to Octo-SPI FLASH as DQS

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		OFF	PB2 is NOT connected to Octo-SPI FLASH PB2 can be used for Motor control
PC0	R209	ON	PC0 is connected to Octo-SPI FLASH as IO7
		OFF	PC0 is NOT connected to Octo-SPI FLASH PC0 can be used for Motor control
PC1	R215	ON	PC1 is connected to Octo-SPI FLASH as IO4
		OFF	PC1 is NOT connected to Octo-SPI FLASH PC1 can be used for Motor control
PC2	R214	ON	PC2 is connected to Octo-SPI FLASH as IO5
		OFF	PC2 is NOT connected to Octo-SPI FLASH PC2 can be used for Motor control
PC3	R218	ON	PC3 is connected to Octo-SPI FLASH as IO6
		OFF	PC3 is NOT connected to Octo-SPI FLASH PC3 can be used for Motor control
PF11	SB22	ON	PF11 is connected to Octo-SPI SRAM CSn JP7 should be in [1-2] in this configuration
		OFF	PF11 is NOT connected to Octo-SPI SRAM NCS PF11 can be used for optional OctoSPI SRAM 1V8 for CLK-N
	SB23	ON	PF11 is connected to Octo-SPI SRAM NCS
		OFF	PF11 is NOT connected to Octo-SPI SRAM CSn

(Default configuration is shown in bold.)

Table 42 shows the Jumper configuration to allowing to access the Octo-SPI Flash memory device.

Table 42. Octo-SPI jumper configuration.

HW	Setting	Configuration
JP7	JP7[1-2]	PA2 for OCTOSPI CS is connected to the OCTOSPI FLASH CS pin
	JP7[2-3]	PA2 for OCTOSPI CS is NOT connected to the OCTOSPI FLASH CS pin, OCTOSPI SRAM can be used. In this configuration, SB22 should be removed.

(Default configuration is shown in bold.)

2.21.5 Limitations

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the OCTOSPI features:

The OCTOSPI function cannot be operated simultaneously with Motor control function

The OCTOSPI function cannot be operated simultaneously with OPAMP function

2.22 EEPROM

M24128-DFDW6TP, a 128-Kbit I²C-bus EEPROM device, is fitted on the main board of STM32L552E-EVAL, in U3 position. It is accessed with I²C-bus lines I2C1_SCL and I2C1_SDA of STM32L552ZET6Q. It supports all I²C-bus modes with speeds up to 1 MHz. The base I²C-bus address is 0xA0. Write-protecting the EEPROM is possible through opening the SB13 solder bridge. By default, SB13 is closed and writing into the EEPROM enabled.

2.22.1 Operating voltage

The M24128-DFDW6TP EEPROM device's operating voltage is fully compatible with the MCU voltage range 1V71 to 3V6.

2.22.2 EEPROM IO interface.

Table 43 describe the HW configuration for the EEPROM interface

Table 43. HW configuration for the EEPROM interface.

IO	Resistor	Setting	Configuration
PG13	R232	ON	PG13 is used as I2C1_SDA to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+
PG14	R228	ON	PG14 is used as I2C1_SCL to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+

2.23 EXT_I2C connector

EXT_I2C connector CN4 can be connected to I²C bus daughter board. MFX_GPIO8 of MFX MCU provide EXT_RESET.

2.23.1 Operating voltage

CN4 connector pin 4 is connected to VDD. So external module should be compliant with the VDD range used on the MCU: 2V7 to 3V3 or low voltage range 1V7 to 3V3

2.23.2 EXT_I2C IO interface.

Table 44 describe the HW configuration for the EXT_I2C interface

Table 44. HW configuration for the EXT_I2C interface.

IO	Resistor	Setting	Configuration
PG13	R232	ON	PG13 is used as I2C1_SDA to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+
PG14	R228	ON	PG14 is used as I2C1_SCL to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+
MFX_IO8	-	-	MFX_IO8 conencted to CN4 as EXT_RESET

Figure 25 shows the EXT_I2C connector pinout CN4.

Figure 25. EXT_I2C connector pinout CN4 (front view).

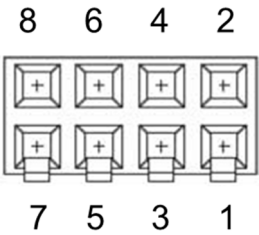


Table 45 describe the EXT_I2C connector pinout CN4

Table 45. EXT_I2C connector pinout CN4.

STM32 pin	Signal name	Pin	Pin	Signal name	STM32 pin
NC	NC	1	2	GND	GND
NC	NC	3	4	VDD	VDD
MFX_IO8	EXT_RESET	5	6	I2C1_SCL	PG14
NC	NC	7	8	I2C1_SDA	PG13

2.24 Touch-sensing button

The STM32L552E-EVAL evaluation board supports a touch sensing button based on either RC charging or on charge-transfer technique. This one is enabled by default.

2.24.1 Touch-sensing button IO interface.

The touch sensing button is connected to PC6 port of STM32L552ZET6Q and the related charge capacitor is connected to PC7.

An active shield is designed in the layer 2 of the main PCB, under the button footprint. It allows reducing disturbances from other circuits to prevent from false touch detections.

The active shield is connected to PB6 port of STM32L552ZET6Q through the resistor R20. The related charge capacitor is connected to PB7.

The SB configuration related with the touch sensing function enable or disable its operation. However, most of them serve to optimize the touch sensing performance, by isolating copper tracks to avoid disturbances due to their antenna effect.

Table 46 describe the HW configuration for the Touch-sensing button interface

Table 46. HW configuration for the Touch-sensing button interface.

IO	Resistor	Setting	Configuration
PC6	SB12	ON	PC6 is connected to Touch button TKEY
		OFF	PC6 is NOT connected to touch Button PC6 can be used for Motor control
PC7	SB5	ON	PC7 is connected to Touch button TKEY_CS
		OFF	PC7 is NOT connected to touch Button PC7 can be used for Motor control or Audio DFSDM or STMOD+
PB6	SB17	ON	PB6 is connected to Touch button SHIELD
		OFF	PB6 is NOT connected to touch Button PB6 can be used for Motor control
PB7	R229	ON	PB7 is connected to Touch button SHIELD_CS
		OFF	PB7 is NOT connected to touch Button No other muxing

2.24.2 Limitations

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the Touch Sensing Button features:

The Touch Sensing Button cannot be operated simultaneously with Motor control function

The Touch Sensing Button cannot be operated simultaneously with external MEMS module, the STMP52 for measurement using Sigma Delta interface the DFSDM Audio on STMOD+

2.25 MFX MCU

The MFX: Multi Function eXpander MCU is used as GPIO expander and IDD measurement: U18.

2.25.1 Operating voltage

The MFX MCU is connected to VDD and is fully compatible with the MCU voltage range 1V71 to 3V6.

2.25.2 MFX IO expander

MFX circuit on STM32L552E-EVAL board acts as IO-expander. The communication interface between MFX and STM32L552ZET6Q is I2C bus, a Wake-UP pin and an INT pin.

Table 47 describe the HW configuration for the MFX interface

Table 47. HW configuration for the MFX interface.

IO	SB	Setting	Configuration
PA0	SB118	ON	PA0 is connected to MFX as MFX_IRQ_OUT
		OFF	PA0 is NOT connected to MFX PA0 can be used for OPAMP, STMOD+ or Motor control
PG9	SB87	ON	PG9 is connected to MFX as MFX_WAKEUP
		OFF	PG9 is NOT connected to MFX PG9 can be used for STMOD+ or Motor control
PG13	R232	ON	PG13 is used as I2C1_SDA to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+
PG14	R228	ON	PG14 is used as I2C1_SCL to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+

(Default configuration is shown in bold.)

Table 48 describe the IO signals driven by the MFX

Table 48. IO signals driven by the MFX.

Pin number	Pin names	Signal name	Function
18	GPIO0	JOY_SEL	B1 Joystick selection
19	GPIO1	JOY_DOWN	B1 Joystick down direction
20	GPIO2	JOY_LEFT	B1 Joystick left direction
39	GPIO3	JOY_RIGHT	B1 Joystick right direction
40	GPIO4	JOY_UP	B1 Joystick up direction
15	GPIO5	MEMS_LED	CN24 LED for Ext audio Module
16	GPIO6	SMARTCARD_OFF	U26 Smart Card OFF
17	GPIO7	SMARTCARD_RST	U26 Smart Card RESET
29	GPIO8	EXT_RESET	Cn4 I2C module RESET
30	GPIO9	SMARTCARD_CMDVCC	U26 smartcard VCC cmd
31	GPIO10	SMARTCARD_3V/5V	U26 Smart card 3V 5V selection
32	GPIO11	LED_YELLOW	LD6 LED yellow

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33	GPIO12	LCD_RESET	CN18 LCD Reset
26	GPIO13	LED_ORANGE	LD7 LED Orange
27	GPIO14	STMOD+_RST	P2 STMOD+ Reset
28	GPIO15	AUDIO_RESETN	U30 Audio reset

2.25.3 IDD measurement

STM32L552ZET6Q has a built-in circuit allowing to measure its own current consumption (IDD) in Run and Low-power modes, except for Shutdown mode. It is strongly recommended that, the MCU supply voltage (VDD_MCU line) does not exceed 3.3V. This is because there are components on STM32L552E-EVAL supplied from 3.3 V that communicate with the MCU through I/O ports. Voltage exceeding 3.3 V on the MCU output port may inject current into 3.3 V-supplied peripheral I/Os and false the MCU current consumption measurement.

Table 49 shows settings of jumper associated with the IDD measurement on the board.

Table 49. jumper associated with the IDD measurement on the board.

HW	Setting	Configuration
JP8	JP8[1-2]	STM32L552ZET6Q has a built-in circuit allowing to measure its own current consumption
	JP8[2-3]	IDD measurement is not available, bypass mode only for STM32L552ZET6Q VDD_MCU power supply.

(Default configuration is shown in bold.)

2.25.4 Limitations

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the MFX features:

The MFX cannot be operated simultaneously with OPAMP and COMP function

The MFX cannot be operated simultaneously with STMOD+ function

The MFX cannot be operated simultaneously with Motor control function

2.26 Motor control

The CN2 connector is designed to receive a motor control (MC) module.

2.26.1 Motor-control IO interface.

The Motor control IO interface are not connected by default because to more IO consuming.

Table 50 describe the assignment of the CN2 Motor control interface and the IO function associated from the STM32L552ZET6Q.

Table 50. Motor control terminal and IO function assignment.

Motor Control connector CN2		STM32L552ZET6Q microcontroller			
Terminal	Terminal name	Port name	Function	Alternate function	Board modifications for enabling Motor Control
1	Emergency Stop	PB6	TIM8_BKIN2		Close SB15 Remove SB17 (Touch button)
2	GND		GND		
3	PWM_1H	PC6	TIM8_CH1		Close SB11 Remove SB12 (Touch button)
4	GND		GND		
5	PWM_1L	PA7	TIM8_CH1N		Close SB79 Remove R198 (OCTOSPI)
6	GND		GND		
7	PWM_2H	PC7	TIM8_CH2		Close SB2 Open SB3 DFSDM STMOD+ Open SB5 (Touch button)
8	GND		GND		
9	PWM_2L	PB0	TIM8_CH2N		Close SB76 Remove R195 OCTOSPI
10	GND		GND		
11	PWM_3H	PC8	TIM8_CH3		Close SB57 Open SB56 (SDIO)
12	GND		GND		
13	PWM_3L	PB1	TIM8_CH3N		Close SB74 Remove R194 (OCTOSPI)
14	Bus Voltage	PA4	ADC12_IN9		Close SB122 Open SB107 UCPD Open SB108 STMOD+ or no daughter board Open SB124 or no ADC/DAC on CN12
15	PhaseA current+	PC0	ADC12_IN1		Close SB90 Remove R209 OCTOSPI
16	PhaseA current-		GND		
17	PhaseB current+	PC1	ADC12_IN2		Close SB91 Remove R215 OCTOSPI
18	PhaseB current-		GND		
19	PhaseC current+	PC2	ADC12_IN3		Close SB94 Remove R214 OCTOSPI
20	PhaseC current-		GND		
21	ICL Shutout	PG9	GPIO		Close SB85 Open SB87: MFX Open SB81 STMOD+
22	GND		GND		
23	Dissipative Brake	PB2	GPIO		Close SB70 Remove R189 OCTOSPI
24	PFC ind. curr.	PC3	ADC12_IN4		Close SB100

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					Remove R218 OCTOSPI
25	5V		5V		
26	Heatsink Temp.	PA3	ADC12_IN8		Close SB86 Removed R206 OCTOSPI Open SB84 OPAMP
27	PFC Sync	PF9	TIM15_CH1		Close SB95 Open SB98 Audio SAI
28	3V3		3V3		
29	PFC PWM	PF10	TIM15_CH2		Close SB97 Open SB96 Audio DFSDM
30	PFC Shutdown	PA9	TIM15_BKIN		Close SB60 Open SB65 SmartCard
31	Encoder A	PA0	TIM2_CH1	ADC12_IN5	Close SB117 Open SB118 MFX Open SB116 OPAMP Open SB115 STMOD+
32	PFC Vac	PA6	ADC12_IN1 1		Close SB80 Remove R204 OCTOSPI
33	Encoder B	PA1	TIM2_CH2	ADC12_IN6	Close SB113 Open SB114 TAMPER KEY Open SB111 OPAMP Open SB112 STMOD+
34	Encoder Index	PA2	TIM2_CH3	ADC12_IN7	Close SB88 Removed R208 OCTOSPI

Figure 26 shows the Motor control connector pinout CN2.

Figure 26. Motor control connector pinout CN2.

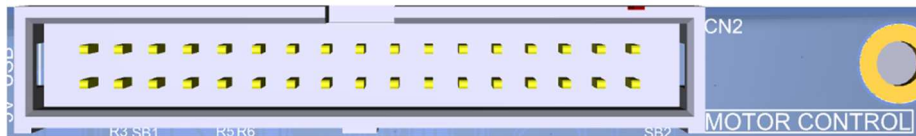


Table 51 describe the Motor control connector pinout CN2

Table 51. Motor Control connector pinout CN2.

STM32 pin	Signal name	Pin	Pin	Signal name	STM32 pin
PB6	Emergency STOP	1	2	GND	-
PC6	PWM_1H	3	4	GND	-
PA7	PWM_1L	5	6	GND	-
PC7	PWM_2H	7	8	GND	-
PB0	PWM_2L	9	10	GND	-
PC8	PWM_3H	11	12	GND	-
PB1	PWM_3L	13	14	BUS VOLTAGE	PA4
PC0	CURRENT A	15	16	GND	-
PC1	CURRENT B	17	18	GND	-
PC2	CURRENT C	19	20	GND	-
PG9	ICL Shutout	21	22	GND	-
PB2	DISSIPATIVE BRAKE	23	24	PCD Ind. Current	PC3
-	+5V power	25	26	Heatsink temperature	PA3
PF9	PFC SYNC	27	28	3.3V power	-
PF10	PFC PWM	29	30	PFC Shut Down	PA9
PA0	Encoder A	31	32	PFC Vac	PA6
PA1	Encoder B	33	34	Encoder Index	PA2

2.26.2 Board modifications to enable motor control

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Figure 5 (top side) and Figure 6 (bottom side) illustrate the board modifications listed in Table 40, required for the operation of motor control. Red color denotes a component to be removed. Green color denotes a component to be fitted.

Figure 27. STM32L552E-EVAL Top side Motor control hardware update.

Figure 28. STM32L552E-EVAL Top side Motor control hardware update.

2.26.3 Limitations

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the Motor control features:

The Motor control cannot be operated simultaneously with Touch sensing Button function

The Motor control cannot be operated simultaneously with OCTOSPI function

The Motor control cannot be operated simultaneously with STMOD+ function

The Motor control cannot be operated simultaneously with SDIO function

The Motor control cannot be operated simultaneously with UCPD function

The Motor control cannot be operated simultaneously with ADC/DAC function

The Motor control cannot be operated simultaneously with MFX function

The Motor control cannot be operated simultaneously with OPAMP function

The Motor control cannot be operated simultaneously with AUDIO function

The Motor control cannot be operated simultaneously with SMARTCARD function

The Motor control cannot be operated simultaneously with TAMPER KEY function

Figure x. PCB top side rework for moto control

Figure x. PCB underside rework for moto control

2.27 Extension connectors CN5, CN6, CN8 and CN9

The CN5, CN6, CN8 and CN9 headers complement to give access to all GPIOs of the STM32L552ZET6Q microcontroller. In addition to GPIOs, the following signals and power supply lines are also routed on these connectors:

- GND
- 5V
- 3V3
- 5V_DC
- VDD
- RESET#
- Clock terminals PC14-OSC32_IN, PC15-OSC32_OUT, PH0-OSC_IN, PH1-OSC_OUT

CN5 and CN6 has two rows header of 19 pins, with 1.27 mm pitch and 2.54 mm row spacing.

CN8 and CN9 has two rows header of 17 pins, with 1.27 mm pitch and 2.54 mm row spacing. Mainly used for FMC interface access.

For extension modules, SAMTEC RSM-series and SAMTEC SMS-series can be recommended as SMD and through-hole receptacles, respectively.

Figure 29 shows the CN5/CN6 connector pinout.

Figure 29. CN5/CN6 connector pinout.

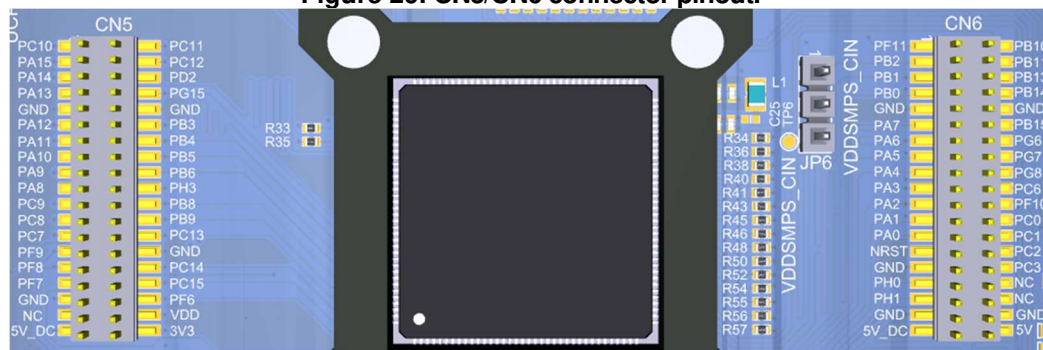


Table 52 describe the CN5 connector pinout

Table 52. CN5 connector pinout.

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
PC10	SDIO, Trace	1	2	SDIO	PC11
PA15	UCPD, Trace	3	4	SDIO, SPI, Trace	PC12
PA14	SWD	5	6	SDIO	PD2
PA13	SWD	7	8	LCD INT	PG15
GND	power	9	10	power	GND
PA12	USB_FS_P	11	12	LED, JTAG	PB3
PA11	USB_FS_N	13	14	JTAG, COMP, STMOD+	PB4
PA10	Audio SAI	15	16	UCPD, COMP, STMOD+	PB5
PA9	Smartcard, Motor control	17	18	Touch key, Motor control	PB6
PA8	Smartcard,	19	20	BOOT0	PH3
PC9	SDIO, Trace	21	22	FDCAN	PB8

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PC8	SDIO, Motor control	23	24	FDCAN	PB9
PC7	Touch key, DFSDM, Motor control	25	26	Wake-up key	PC13
PF9	Audio SAI, Motor control	27	28	power	GND
PF8	Audio SAI	29	30	OSC32-IN	PC14
PF7	Audio SAI	31	32	OSC32_OUT	PC15
GND	power	33	34	Audio SAI	PF6
NC	NC	35	36	Power	VDD
5V_DC	Power	37	38	power	3V3

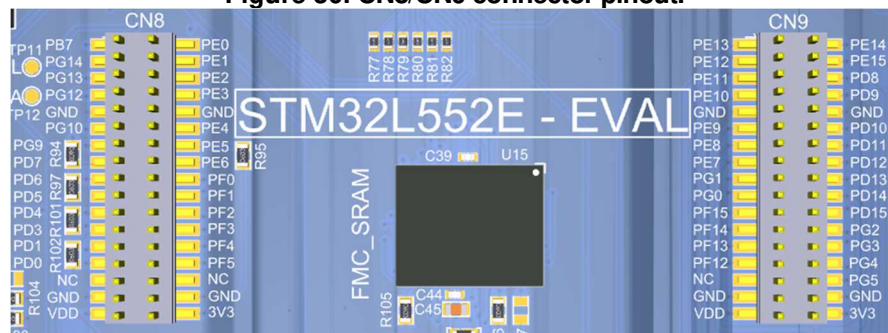
Table 53 describe the CN6 connector pinout

Table 53. CN6 connector pinout.

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
PF11	Octospi	1	2	USART VCP, RS232	PB10
PB2	Octospi, Motor control	3	4	USART VCP, RS232	PB11
PB1	Octospi, Motor control	5	6	LPUART	PB13
PB0	Octospi, Motor control	7	8	UCPD	PB14
GND	power	9	10	Power	GND
PA7	Octospi, Motor control	11	12	UCPD	PB15
PA6	Octospi, Motor control	13	14	LPUART	PG6
PA5	LCD_BL, STMOD+	15	16	LPUART VCP, RS232	PG7
PA4	UCPD, STMOD+, ADC/DAC, Motor control	17	18	LPUART VCP, RS232	PG8
PA3	Octospi, OPAMP, Motor control	19	20	Touch key, Motor control	PC6
PA2	Octospi, Motor control	21	22	DFSDM, Motor control	PF10
PA1	Tamper key, OPAMP, STMOD+, Motor control	23	24	Octospi, Motor control	PC0
PA0	MFX, OPAMP, STMOD+, Motor control	25	26	Octospi, Motor control	PC1
NRST	RESET	27	28	Octospi, Motor control	PC2
GND	Power	29	30	Octospi, Motor control	PC3
PH0	OSC-IN	31	32	NC	NC
PH1	OSC_OUT	33	34	NC	NC
GND	power	35	36	power	GND
5V_DC	power	37	38	power	5V

Figure 30 shows the CN8/CN9 connector pinout.

Figure 30. CN8/CN9 connector pinout.



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Table 54 describe the CN8 connector pinout

Table 54. CN8 connector pinout.

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
PB7	Touch key	1	2	SRAM-FMC	PE0
PG14	I2C	3	4	SRAM-FMC	PE1
PG13	I2C	5	6	Trace	PE2
PG12	LCD-FMC	7	8	SRAM-FMC	PE3
GND	Power	9	10	Power	GND
PG10	SDIO, STMOD+	11	12	SRAM-FMC	PE4
PG9	MFx, STMOD+, Motor control	13	14	Trace	PE5
PD7	SRAM-FMC	15	16	LCD-FMC	PE6
PD6	DFSDM	17	18	SRAM-FMC	PF0
PD5	LCD-SRAM-FMC	19	20	SRAM-FMC	PF1
PD4	LCD-SRAM-FMC	21	22	SRAM-FMC	PF2
PD3	LED	23	24	SRAM-FMC	PF3
PD1	LCD-SRAM-FMC	25	26	SRAM-FMC	PF4
PD0	LCD-SRAM-FMC	27	28	SRAM-FMC	PF5
NC	NC	29	30	NC	NC
GND	power	31	32	power	GND
VDD	power	33	34	power	3V3

Table 55 describe the CN9 connector pinout

Table 55. CN9 connector pinout.

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
PE13	LCD-SRAM-FMC	1	2	LCD-SRAM-FMC	PE14
PE12	LCD-SRAM-FMC	3	4	LCD-SRAM-FMC	PE15
PE11	LCD-SRAM-FMC	5	6	LCD-SRAM-FMC	PD8
PE10	LCD-SRAM-FMC	7	8	LCD-SRAM-FMC	PD9
GND	power	9	10	power	GND
PE9	LCD-SRAM-FMC	11	12	LCD-SRAM-FMC	PD10
PE8	LCD-SRAM-FMC	13	14	SRAM-FMC	PD11
PE7	LCD-SRAM-FMC	15	16	SRAM-FMC	PD12
PG1	SRAM-FMC	17	18	SRAM-FMC	PD13
PG0	SRAM-FMC	19	20	LCD-SRAM-FMC	PD14
PF15	SRAM-FMC	21	22	LCD-SRAM-FMC	PD15
PF14	SRAM-FMC	23	24	SRAM-FMC	PG2
PF13	SRAM-FMC	25	26	SRAM-FMC	PG3
PF12	SRAM-FMC	27	28	SRAM-FMC	PG4
NC	NC	29	30	SRAM-FMC	PG5
GND	power	31	32	power	GND
VDD	power	33	34	power	3V3

2.28 TFT LCD

The 34pins 2.54mm pitch female connector CN18 is designed to connect TFT LCD daughter board MB989 supported FMC interface.

The LCD module is composed of the TFT LCD module MRE028-8347I-51P-TP-A with a LCD driver HX8347I. The LCD support a resolution of 240(RGB) x 320 dots 262K color.

The touch panel feature is drive by a Resistive Touch Screen controller: U34 STMPE811QTR.

2.28.1 Operating voltage

By design MB989 is only compatible for a voltage range 2V5 to 3V3. So LCD is not compatible with the MCU low voltage range 1V8.

2.28.2 LCD interface.

Table 56 describe the HW configuration for the LCD interface.

Table 56. HW configuration for the LCD interface.

IO	HW	Setting	Configuration
PG12	R231	ON	PG12 is used as LCD_CSn_FMC_NE4 and connected to LCD
PD5	R239	ON	PD5 is used as FMC_NWE and connected to LCD and SRAM
PD4	R101	ON	PD4 is used as FMC_NOE and connected to LCD and SRAM
PE6	R236	ON	PE6 is used as LCD_RS_FMC_A22 and connected to LCD
MFx-IO12	-	ON	MFx_IO12 is used as LCD_RESET and connected to LCD
PD14	R23	ON	PD14 is used as FMC_D0 and connected to SRAM and LCD
PD15	R22	ON	PD15 is used as FMC_D1 and connected to SRAM and LCD
PD0	R33	ON	PD0 is used as FMC_D2 and connected to SRAM and LCD
PD1	R35	ON	PD1 is used as FMC_D3 and connected to SRAM and LCD
PE7	R48	ON	PE7 is used as FMC_D4 and connected to SRAM and LCD
PE8	R46	ON	PE8 is used as FMC_D5 and connected to SRAM and LCD
PE9	R45	ON	PE9 is used as FMC_D6 and connected to SRAM and LCD
PE10	R43	ON	PE10 is used as FMC_D7 and connected to SRAM and LCD
PE11	R41	ON	PE11 is used as FMC_D8 and connected to SRAM and LCD
PE12	R40	ON	PE12 is used as FMC_D9 and connected to SRAM and LCD
PE13	R38	ON	PE13 is used as FMC_D10 and connected to SRAM and LCD
PE14	R36	ON	PE14 is used as FMC_D11 and connected to SRAM and LCD
PE15	R34	ON	PE15 is used as FMC_D12 and connected to SRAM and LCD
PD8	R29	ON	PD8 is used as FMC_D13 and connected to SRAM and LCD
PD9	R28	ON	PD9 is used as FMC_D14 and connected to SRAM and LCD
PD10	R27	ON	PD10 is used as FMC_D15 and connected to SRAM and LCD
PA5	SB106	ON	PA5 is used as LCD_BL_CTRL
	SB106	OFF	PA5 is not used as LCD_BL_CTRL PA5 can be used for STMOD+ (SB105 ON)
PG15	R191	ON	PG15 is sued as LCD_INT for Touch panel
PG13	R232	ON	PG13 is used as I2C1_SDA to interface the audio codec and it is shared with MFx, LCD, Ext_I2C, EEPROM, STMOD+
PG14	R228	ON	PG14 is used as I2C1_SCL to interface the audio codec and it is shared with MFx, LCD, Ext_I2C, EEPROM, STMOD+

(Default configuration is shown in bold.)

Figure 31 shows the LCD connector pinout CN18.

Figure 31. LCD connector pinout CN18.



Table 57 describe the LCD interface and connector pinout CN18

Table 57. LCD connector pinout CN18.

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
PG12	LCD_CSn_FMC_NE4	1	2	LCD_RS_FMC_A22	PE6
PD5	FMC_NWE	3	4	FMC_NOE	PD4
MFX_IO12	LCD_RESET	5	6	D0	PD14
PD15	D1	7	8	D2	PD0
PD1	D3	9	10	D4	PE7
PE8	D5	11	12	D5	PE9
PE10	D7	13	14	D8	PE11
PE12	D9	15	16	D10	PE13
PE14	D11	17	18	D12	PE15
PD8	D13	19	20	D14	PD9
PD10	D15	21	22	BLGND	-
PA5	BL_CTRL	23	24	VDD_LCD	-
-	VDD_LCD	25	26	GND	-
-	GND	27	28	VDD_BL	-
-	-	29	30	GND	-
-	TSC_XL	31	32	TSC_XR	-
-	TSC_YD	33	34	TSC_YU	-

2.28.3 Limitations

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the Touch Sensing Button features:

The LCD BL_CTRL cannot be operated simultaneously with STMOD+ function. In this case LCD backlight is force to ON

FMC interface is shared with LCD.

2.29 PMOD connector

The standard PMOD connector P1 is available on STM32L552E-EVAL board to support flexibility in small form factor application. The PMOD connector is implemented the PMOD type 2A & 4A on STM32L552E-EVAL board.

Table 58 describe the HW configuration for the PMOD interface.

Table 58. HW configuration for the PMOD interface.

IO	HW	Setting	Configuration
PA4	SB108/SB6	ON/ON	PA4 is used as SPI_NSS on PMOD
		ON/OFF	PA4 is Not used as SPI_NSS on PMOD PA4 can be used for STMOD+ or USB or Motor control or ADC/DAC
PC12	SB62/SB46	ON/ON	PC12 is used as SPI3_MOSI on PMOD
		ON/OFF	PC12 is Not used as SPI3_MOSI on PMOD PC12 can be used for STMOD+ or SDIO or TRACE
PG10	SB52/SB8	ON/ON	PG10 is used as SPI3_MISO on PMOD
		ON/OFF	PG10 is Not used as SPI3_MISO on PMOD PG10 can be used for STMOD+ or SDIO
PG9	SB81/SB44	ON/ON	PG9 is used as SPI3_SCK on PMOD
		ON/OFF	PG9 is Not used as SPI3_SCK on PMOD PG9 can be used for STMOD+ or MFX or Motor control
PB13	R190/SB7	ON/ON	PB13 is used as LPUART1_CTS on PMOD
		ON/OFF	PB13 is Not used as LPUART1_CTS on PMOD PB13 can be used for STMOD+ or RS232
PG7	SB49/SB45	ON/ON	PG7 is used as LPUART1_TX on PMOD
		ON/OFF	PG7 is Not used as LPUART1_TX on PMOD PG7 can be used for STMOD+ or T_VCP
PG8	SB51/SB9	ON/ON	PG8 is used as LPUART1_RX on PMOD
		ON/OFF	PG8 is Not used as LPUART1_RX on PMOD PG8 can be used for STMOD+ or T_VCP
PG6	R203	ON	PG6 is used as LPUART1_RTS on PMOD or for RS232
PA1	SB112/R186	ON/ON	PA1 is used as PMOD_INT on PMOD shared with STMOD+
		ON/OFF	PA1 is Not used as PMOD_INT on PMOD PA1 can be used for STMOD+ or TamperKey, or OPAMP, or Motor control
MFX_IO14	R185	ON	MFX_IO14 is used as PMOD_RST on PMOD shared with STMOD+

(Default configuration is shown in bold.)

Figure 32 shows the PMOD connector pinout P1.

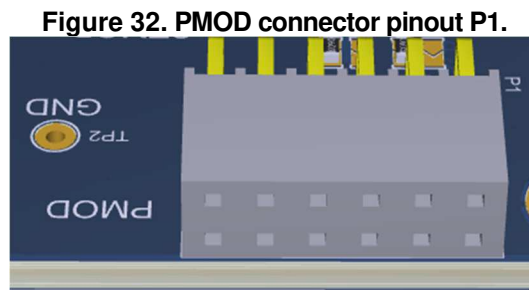


Table 59 describe the PMOD interface and connector pinout P1

Table 59. PMOD connector pinout P1.

Function	STM32 pin	Signal name	Pin names	Pin	Pin	Pin names	Signal name	STM32 pin	Function
SPI3 LPUART1	PA4 PB13	SPI_NSS LPUART1_CTS	1	1	7	7	PMOD_INT	PA1	INT1
SPI3 LPUART1	PC12 PG7	SPI3_MOSI UART_TX	2	2	8	8	PMOD_RST	MFX_IO14	Reset
SPI3 LPUART1	PG10 PG8	SPI3_MISO UART_RX	3	3	9	9	NC	NC	NC
SPI3 LPUART1	PG10 PG8	SPI3_SCK LPUART1_RTS	4	4	10	10	NC	NC	NC
GND	-	GND	5	5	11	11	GND	-	GND
Power	-	VDD	6	6	12	12	VDD	-	Power

2.29.1 Limitations

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the PMOD features:

The PMOD cannot be operated simultaneously with STMOD+ function

The PMOD cannot be operated simultaneously with UCPD function

The PMOD cannot be operated simultaneously with ADC/DAC function

The PMOD cannot be operated simultaneously with Motor control function

The PMOD cannot be operated simultaneously with TRACE function

The PMOD cannot be operated simultaneously with SDIO function

The PMOD cannot be operated simultaneously with MFX function

The PMOD cannot be operated simultaneously with RS-232 function

The PMOD cannot be operated simultaneously with TAMPER KEY function

The PMOD cannot be operated simultaneously with OPAMP function

2.30 STMOD+ connector

The standard STMOD+ connector P2 is available on STM32L552E-EVAL board to support flexibility in small form factor application.

Table 60 describe the HW configuration for the STMOD+ interface.

Table 60. HW configuration for the STMOD+ interface.

IO	HW	Setting	Configuration
PA4	SB108/SB16	ON/ON	PA4 is used as SPI_NSS on STMOD+
		ON/OFF	PA4 is Not used as SPI_NSS on STMOD+ PA4 can be used for PMOD or USB or Motor control or ADC/DAC
PC12	SB62/SB47	ON/ON	PC12 is used as SPI3_MOSI on STMOD+
		ON/OFF	PC12 is Not used as SPI3_MOSI on STMOD+ PC12 can be used for PMOD or SDIO or TRACE
PG10	SB52/SB19	ON/ON	PG10 is used as SPI3_MISO on STMOD+
		ON/OFF	PG10 is Not used as SPI3_MISO on STMOD+ PG10 can be used for PMOD or SDIO
PG9	SB81/SB69	ON/ON	PG9 is used as SPI3_SCK on STMOD+
		ON/OFF	PG9 is Not used as SPI3_SCK on STMOD+ PG9 can be used for PMOD or MFX or Motor control
PB13	R190/SB14	ON/ON	PB13 is used as LPUART1_CTS on STMOD+
		ON/OFF	PB13 is Not used as LPUART1_CTS on STMOD+ PB13 can be used for PMOD or RS232
PG7	SB49/SB64	ON/ON	PG7 is used as LPUART1_TX on STMOD+
		ON/OFF	PG7 is Not used as LPUART1_TX on STMOD+ PG7 can be used for PMOD or T_VCP
PG8	SB51/SB9	ON/ON	PG8 is used as LPUART1_RX on STMOD+
		ON/OFF	PG8 is Not used as LPUART1_RX on STMOD+ PG8 can be used for PMOD or T_VCP
PG6	R203	ON	PG6 is used as LPUART1_RTS on STMOD+ or for RS232
PB5	SB99	ON	PB5 is used as SPI3_MOSI2 on STMOD+
		OFF	PB5 is Not used as SPI3_MOSI2 on STMOD+ PB5 can be used for USB or COMP
PB4	SB89	ON	PB4 is used as SPI3_MISO2 on STMOD+
PB5 PG13	SB99 R232	OFF	PB4 is Not used as SPI3_MISO2 on STMOD+ PB4 can be used for JTAG or SDIO
		ON	PG13 is used as I2C1_SDA to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+
PG14 PA1	R228 SB112/R186	ON	PG14 is used as I2C1_SCL to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+
		ON/ON	PA1 is used as STMOD+_INT on STMOD+ shared with PMOD
		ON/OFF	PA1 is Not used as PMOD_INT on PMOD PA1 can be used for STMOD+ or TamperKey, or OPAMP, or Motor control
MFX_IO14	R185	ON	MFX_IO14 is used as PMOD_RST on PMOD shared with STMOD+
PA0	SB115	ON	PA0 is used as ADC on STMOD+
		OFF	PA0 is Not used as ADC on STMOD+ PA0 can be used for MFX, OPAMP or Motor control
PA5	SB105	ON	PA5 is used as PWM on STMOD+
		OFF	PA5 is Not used as PWM on STMOD+ PA5 can be used for LCD_BL_CTRL
PD6	R97	ON	PD6 is used as DFSDM_DATIN1 on STMOD+ shared with on board MEMS
PF10	SB96	ON	PF10 is used as DFSDM_CKOUT on STMOD+ shared with on board MEMS
		OFF	PF10 is Not used as DFSDM_CKOUT on STMOD+ PF10 can be used for Motor control

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PC7	SB3	ON	PC7 is used as DFSDM_DATIN3 on STMOD+ shared with on board MEMS
		OFF	PC7 is Not used as DFSDM_DATIN3 on STMOD+ PC7 can be used for Touch-Key or Motor control

(Default configuration is shown in bold.)

Figure 33 shows the STMOD+ connector pinout.

Figure 33. STMOD+ connector pinout.

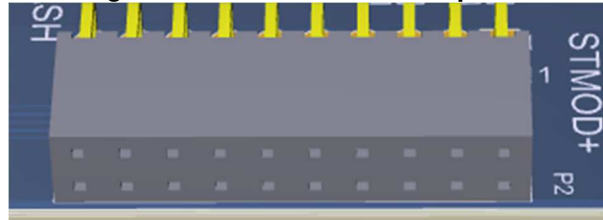


Table 61 describe the STMOD+ interface and connector pinout

Table 61. STMOD+ interface and connector pinout.

MCU Function	STM32 pin	Signal name	Pin names	Pin	Pin	Pin names	Signal name	STM32 pin	MCU Function
SPI3 LPUART1	PA4 PB13	SPI_NSS LPUART1_CTS	1	1	11	11	PMOD_INT	PA1	INT1
SPI3 LPUART1	PC12 PG7	SPI3_MOSI UART_TX	2	2	12	12	PMOD_RST	MFX_IO 14	Reset
SPI3 LPUART1	PG10 PG8	SPI3_MISO UART_RX	3	3	13	13	STMOD+_ADC	PA0	ADC
SPI3 LPUART1	PG10 PG8	SPI3_SCK LPUART1_RTS	4	4	14	14	STMOD+_PWM	PA5	PWM
GND	-	GND	5	5	15	15	5V	-	Power
Power	-	5V	6	6	16	16	GND	-	GND
I2C1	PG14	I2C1_SCL	7	7	17	17	DFSDM1_DATIN1	PD6	DFSDM
SPI3	PB5	SPI3_MOSI2	8	8	18	18	DFSDM1_CKOUT	PF10	DFSDM
SPI3	PB4	SPI3_MISO2	9	9	19	19	DFSDM1_CKOUT	PC7	DFSDM
I2C1	PG13	I2C1_SDA	10	10	20	20	DFSDM1_CKOUT	PF10	DFSDM

2.30.1 Limitations

Due to the share of some IO of STM32L552ZET6Q by multiple peripherals, the following limitations apply in using the STMOD+ features:

The STMOD+ cannot be operated simultaneously with PMOD function

The STMOD+ cannot be operated simultaneously with UCPD function

The STMOD+ cannot be operated simultaneously with ADC/DAC function

The STMOD+ cannot be operated simultaneously with Motor control function

The STMOD+ cannot be operated simultaneously with TRACE function

The STMOD+ cannot be operated simultaneously with SDIO function

The STMOD+ cannot be operated simultaneously with MFX function

The STMOD+ cannot be operated simultaneously with RS-232 function

The STMOD+ cannot be operated simultaneously with TAMPER KEY function

The STMOD+ cannot be operated simultaneously with OPAMP function

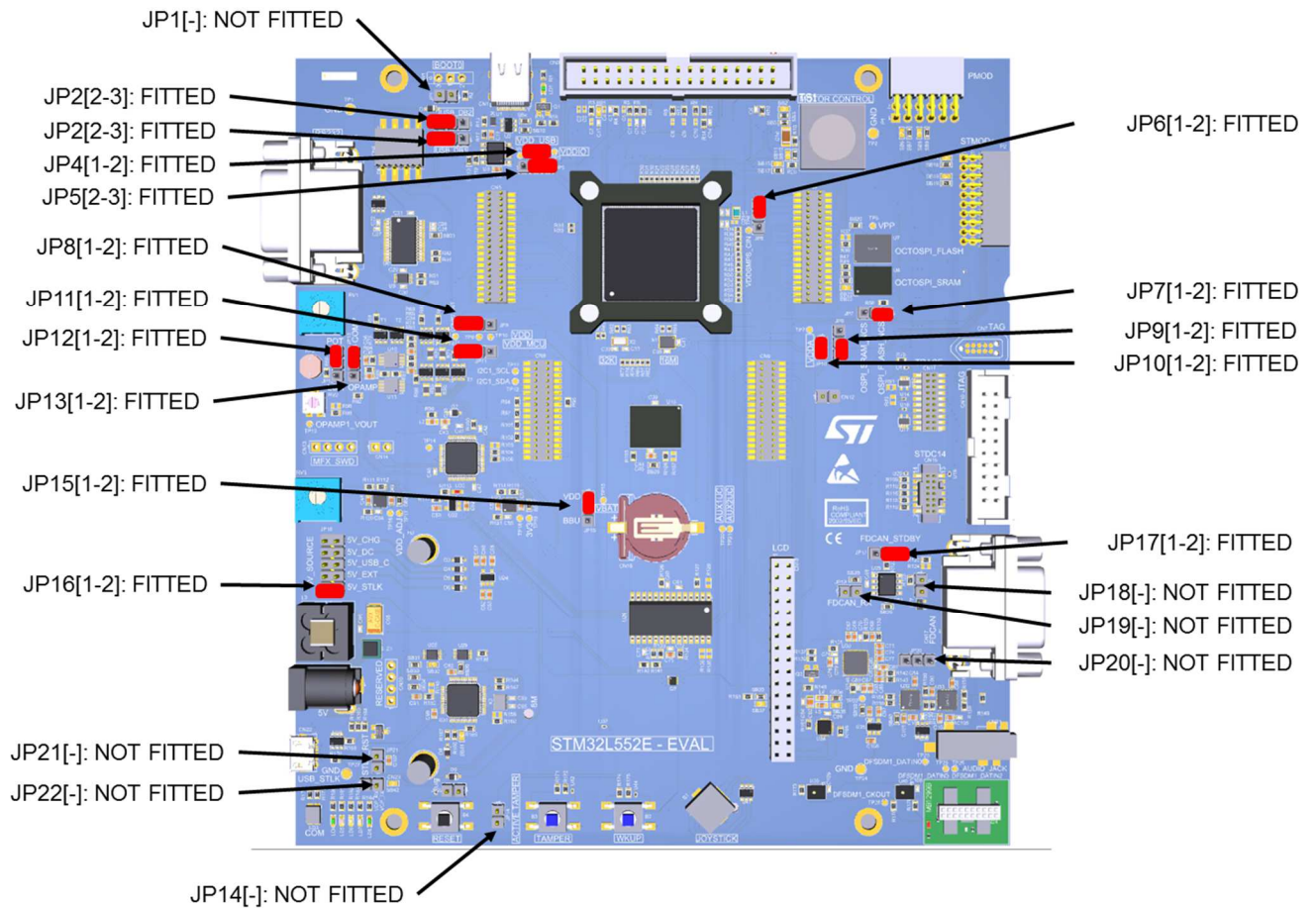
The STMOD+ cannot be operated simultaneously with LCD BL CTRL function

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1 Appendix A STM32L552E-EVAL Jumper summary

Figure 34 summarize the jumper default setting of the STM32L552E-EVAL.

Figure 34. jumper default setting of the STM32L552E-EVAL.



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2 Appendix B STM32L552E-EVAL IO Assignment

LQFP144 Pinout	Pin Name	Main function Pinout assignment	Optional function Pinout assignment	Motor Control connector
1	PE2	TRACE_CLK	-	-
2	PE3	SRAM-FMC_A19	-	-
3	PE4	SRAM-FMC_A20	-	-
4	PE5	TRACE_D2	-	-
5	PE6	LCD_RS_FMC_A22	TRACE_D3	-
6	VBAT	POWER	-	-
7	PC13	User Button WKUP2	TAMPER KEY	-
8	PC14	OSC32_IN	-	-
9	PC15	OSC32_OUT	-	-
10	PF0	SRAM-FMC_A0	-	-
11	PF1	SRAM-FMC_A1	-	-
12	PF2	SRAM-FMC_A2	-	-
13	PF3	SRAM-FMC_A3	-	-
14	PF4	SRAM-FMC_A4	-	-
15	PF5	SRAM-FMC_A5	-	-
16	VSS	POWER	-	-
17	VDD	POWER	-	-
18	PF6	Audio SAI1_SD_B	-	-
19	PF7	Audio SAI1_MCLK_B	-	-
20	PF8	Audio SAI1_SCK_B	-	-
21	PF9	Audio SAI1_FS_B	-	TIM15_CH1
22	PF10	DFSDM1_CKOUT	STMOD+ DFSDM	TIM15_CH2
23	PH0	OSC_IN	-	-
24	PH1	OSC_OUT	-	-
25	NRST	NRST	-	-
26	PC0	OCTOSPI_IO7	-	ADC12_IN1
27	PC1	OCTOSPI_IO4	-	ADC12_IN2
28	PC2	OCTOSPI_IO5	-	ADC12_IN3
29	PC3	OCTOSPI_IO6	-	ADC12_IN4
30	VSSA	POWER	-	-
31	VREFP	POWER	-	-
32	VDDA	POWER	-	-
33	PA0	MFX_IRQ_OUT	OPAMP1_VINP, STMOD+ ADC12_IN5	ADC12_IN5 TIM2_CH1
34	PA1	TAMPER KEY	OPAMP1_VINM STMOD+ PMOD_INT	ADC12_IN6 TIM2_CH2
35	PA2	OCTOSPI_NCS	-	ADC12_IN7 TIM2_CH3
36	PA3	OCTOSPI_CLK	OPAMP1_VOUT	ADC12_IN8
37	VSS	POWER	-	-
38	VDD	POWER	-	-
39	PA4	UCPD_ADC12_IN9	ADC12_IN9/DAC1_OUT1 STMOD+ SPI3_NSS	ADC12_IN9

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			PMOD_SPI3_NSS	
40	PA5	LCD_BL_CTRL_TIM2_CH1	STMOD+_TIM2_CH1	
41	PA6	OCTOSPI_IO3	-	ADC12_IN11
42	PA7	OCTOSPI_IO2	-	TIM8_CH1N
43	PB0	OCTOSPI_IO1	-	TIM8_CH2N
44	PB1	OCTOSPI_IO0	-	TIM8_CH3N
45	PB2	OCTOSPI_DQS	-	IO
46	PF11	OCTOSPI_NCLK	-	-
47	PF12	SRAM-FMC_A6	-	-
48	VSS	POWER	-	-
49	VDD	POWER	-	-
50	PF13	SRAM-FMC_A7	-	-
51	PF14	SRAM-FMC_A8	-	-
52	PF15	SRAM-FMC_A9	-	-
53	PG0	SRAM-FMC_A10	-	-
54	PG1	SRAM-FMC_A11	-	-
55	PE7	LCD-SRAM-FMC_D4	-	-
56	PE8	LCD-SRAM-FMC_D5	-	-
57	PE9	LCD-SRAM-FMC_D6	-	-
58	VSS	POWER	-	-
59	VDD	POWER	-	-
60	PE10	LCD-SRAM-FMC_D7	-	-
61	PE11	LCD-SRAM-FMC_D8	-	-
62	PE12	LCD-SRAM-FMC_D9	-	-
63	PE13	LCD-SRAM-FMC_D10	-	-
64	PE14	LCD-SRAM-FMC_D11	-	-
65	PE15	LCD-SRAM-FMC_D12	-	-
66	PB10	VCP_USART3_TX	RS-232_UART_TX STMOD+ _UART_TX PMOD_UART_TX	-
67	PB11	VCP_USART3_RX	RS-232_UART_RX STMOD+ _UART_RX PMOD_UART_RX	-
68	VDD_SMPS	POWER	-	-
69	VLX	POWER	-	-
70	VSS_SMPS	POWER	-	-
71	VSS	POWER	-	-
72	V15	POWER	-	-
73	VDD	POWER	-	-
74	PB13	RS232_LPUART1_CTS	STMOD+_LPUART1_CTS PMOD_LPUART1_CTS	
75	PB14	UCPD_DB2	-	-
76	PB15	UCPD_CC2	-	-
77	PD8	LCD-SRAM-FMC_D13	-	-
78	PD9	LCD-SRAM-FMC_D14	-	-
79	PD10	LCD-SRAM-FMC_D15	-	-

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80	PD11	SRAM-FMC_A16	-	-
81	PD12	SRAM-FMC_A17	-	-
82	PD13	SRAM-FMC_A18	-	-
83	VSS	POWER	-	-
84	VDD	POWER	-	-
85	PD14	LCD-SRAM-FMC_D0	-	-
86	PD15	LCD-SRAM-FMC_D1	-	-
87	PG2	SRAM-FMC_A12	-	-
88	PG3	SRAM-FMC_A13	-	-
89	PG4	SRAM-FMC_A14	-	-
90	PG5	SRAM-FMC_A15	-	-
91	PG6	RS232 LPUART1_RTS	STMOD+_LPUART1_RTS PMOD_LPUART1_RTS	-
92	PG7	RS232 LPUART1_TX	STMOD+_LPUART1_TX PMOD_LPUART1_TX VCP_LPUART1_TX	-
93	PG8	RS232 LPUART1_RX	STMOD+_LPUART1_RX PMOD_LPUART1_RX VCP_LPUART1_RX	-
94	VSS	POWER	-	-
95	VDD	POWER	-	-
96	PC6		Touch key	TIM8_CH1
97	PC7	DFSDM1_DATIN3	Touch key	TIM8_CH2
98	PC8	SDIO1_D0	-	TIM8_CH3
99	PC9	SDIO1_D1	TRACE_D0	-
100	PA8	SmartCard USART1_CK	-	-
101	PA9	SmartCard USART1_TX	-	TIM1_CH2
102	PA10	Audio SAI1_SD_A	-	-
103	PA11	USB_DM	-	-
104	PA12	USB_DP	-	-
105	PA13	SWDIO	JTAG_JTMS	-
106	VDDUSB	POWER	-	-
107	VSS	POWER	-	-
108	VDD	POWER	-	-
109	PA14	SWCLK	JTAG_JTCK	-
110	PA15	UCPD_CC	JTAG_JTDI	-
111	PC10	SDIO_D2	TRACE_D1	-
112	PC11	SDIO_D3	-	-
113	PC12	SDIO1_CK	STMOD+_SPI3_MOSI PMOD_SPI3_MOSI	-
114	PD0	LCD-SRAM-FMC_D2	-	-
115	PD1	LCD-SRAM-FMC_D3	-	-
116	PD2	SDIO1_CMD	-	-
117	PD3	LED_RED	-	-
118	PD4	LCD-SRAM-FMC_NOE	-	-
119	PD5	LCD-SRAM-FMC_NWE	-	-
120	VSS	POWER	-	-

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121	VDD	POWER	-	-
122	PD6	DFSDM1_DATIN1	STMOD+_DFSDM1_DATIN1	-
123	PD7	SRAM-FMC_NE1	-	-
124	PG9	MFX_WAKE-UP	STMOD+_SPI3_SCK PMOD_SPI3_SCK	IO
125	PG10	SDCARD_DETECT	STMOD+_SPI3_MISO PMOD_SPI3_MISO	-
126	PG12	LCD_CS _n _FMC_NE4	-	-
127	PG13	I2C1_SDA	-	-
128	PG14	I2C1_SCL	-	-
129	VSS	POWER	-	-
130	VDD	POWER	-	-
131	PG15	LCD_CTP_INT	-	-
132	PB3	LED_GREEN	JTAG_JTDO_SWO	-
133	PB4		JTAG_NJTRST COMP2_INP STMOD+_SPI3_MISO2	-
134	PB5	UCPD_DB1	COMP2_OUT STMOD+_SPI3_MOSI2	-
135	PB6		Touch key	TIM8_BKIN2
136	PB7		Touch key	-
137	PH3	BOOT0	-	-
138	PB8	FDCAN1_RX	-	-
139	PB9	FDCAN1_TX	-	-
140	PE0	SRAM_FMC_NBL0	-	-
141	PE1	SRAM_FMC_NBL1	-	-
142	VSS	POWER	-	-
143	V15	POWER	-	-
144	VDD	POWER	-	-

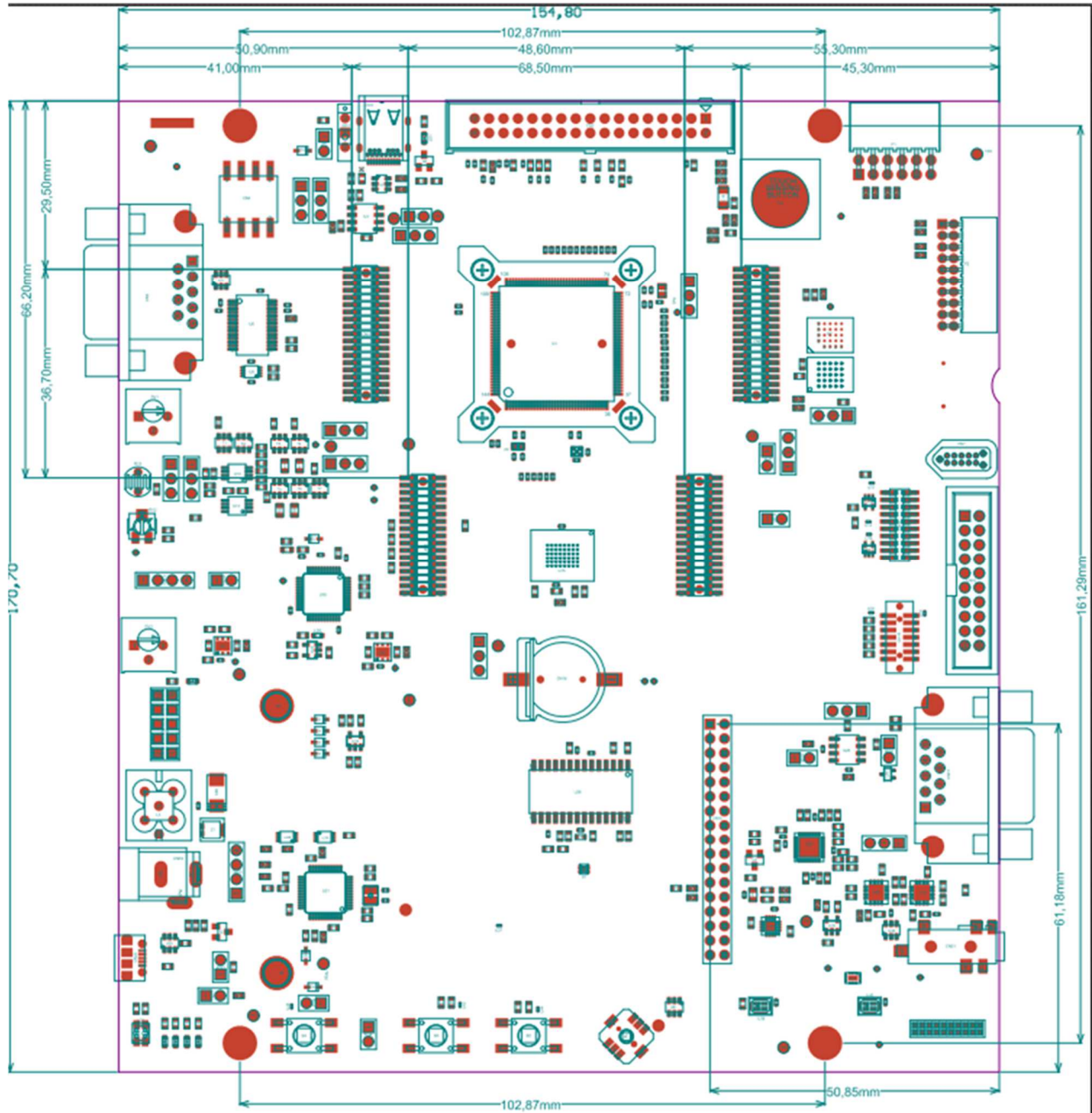
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3 Appendix C Mechanical Dimensions

MB1372 STM32L552E-EVAL board:



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4 Appendix C Document Revision History

Table 39. Document Revision History

Date	Version	Revision Details
5,Jun. 2017	0.1	Initial Version

DRAFT

Appendix A Federal Communications Commission (FCC) and Industry Canada (IC) Compliance

A.1: FCC Compliance Statement

A.1.1: Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

A.1.2: Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

A.1.3: Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

A.2: IC Compliance Statement

This device complies with FCC and Industry Canada RF radiation exposure limits set forth for general population for mobile application (uncontrolled exposure). This device must not be collocated or operating in conjunction with any other antenna or transmitter.

A.2.1: Compliance Statement

Notice: This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Industry Canada ICES-003 Compliance Label: CAN ICES-3 (A)/NMB-3(A)

A.2.2: Déclaration de conformité

Avis: Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement

Étiquette de conformité à la NMB-003 d'Industrie Canada : CAN ICES-3 (A)/NMB-3(A)

Appendix B: CISPR32

B.1: Warning

Warning: This device is compliant with Class A of CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement: Cet équipement est conforme à la Classe A de la CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.