

MIMXRT1050-EVK

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Revision History

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1. Unless Otherwise Specified:


All resistors are in ohms, 1/16 Watt, 0402
All capacitors are in uF, 0402
All voltages are DC
All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

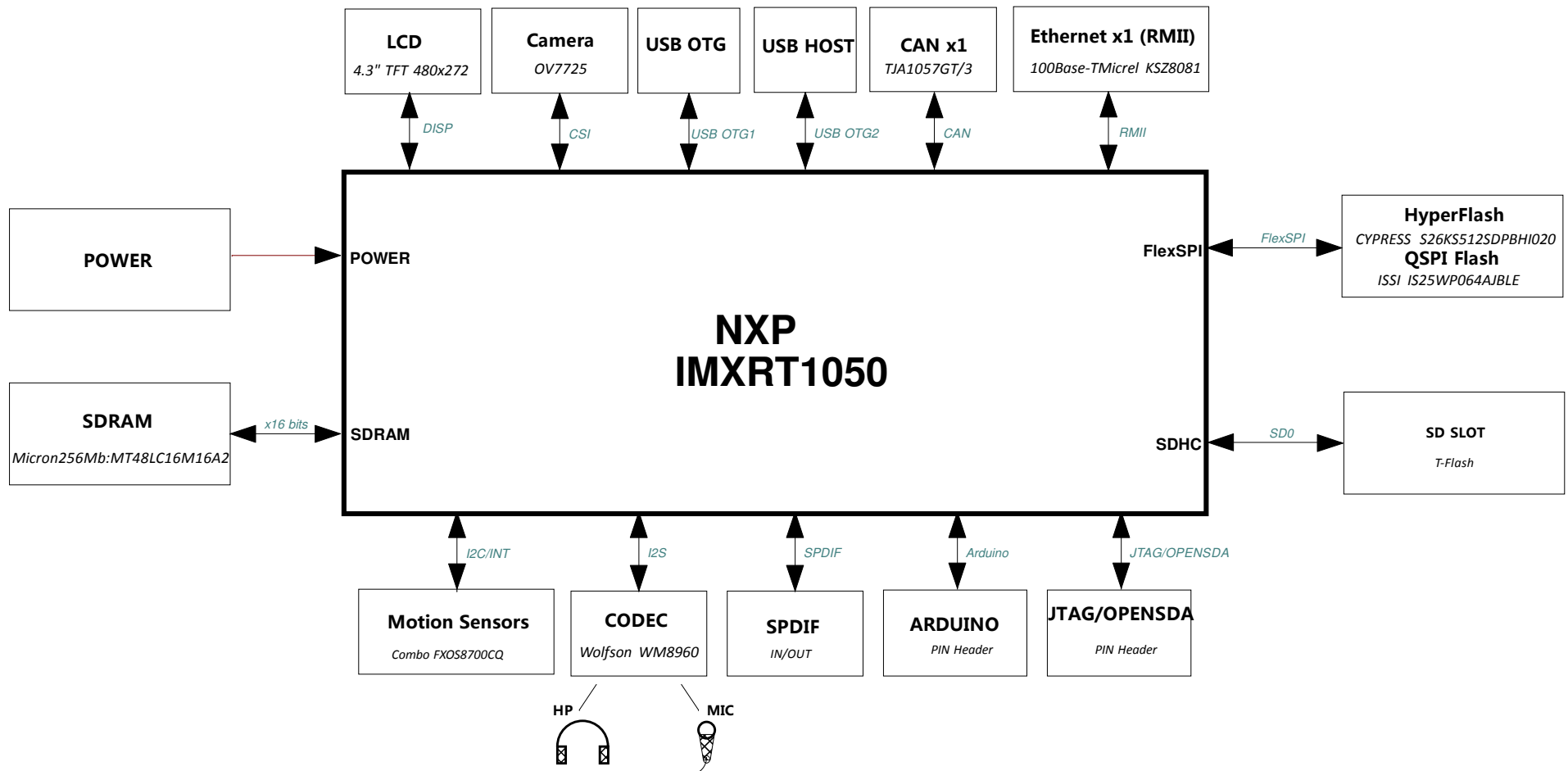
3. Device type number is for reference only. The number varies with the manufacturer.

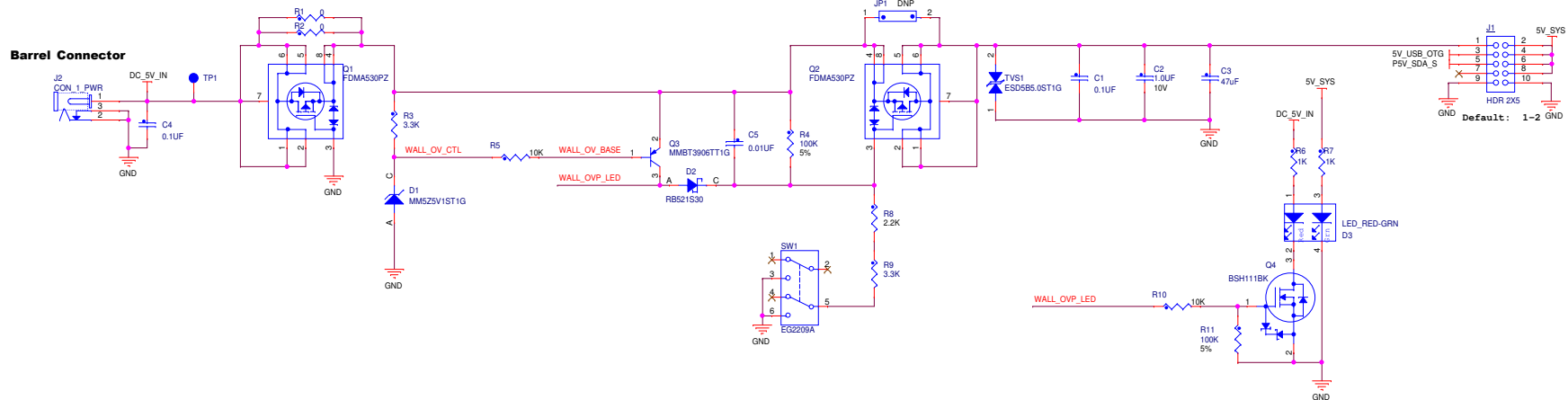
4. Special signal usage:
 _B Denotes - Active-Low Signal
 <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

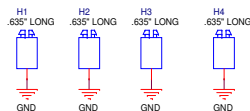
				
ICAP Classification: CP: _____ IJO: X PUBI: _____				
Drawing Title: MIMXRT1050-EVK				
Page Title: COVER				
Size C	Document Number SCH-29538, PDF: SPF-29538	Rev A5		
Date: Monday, October 30, 2017	Sheet 1	of 17		

MIMXRT1050-EVK

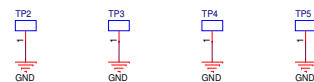




Board Mounting Holes



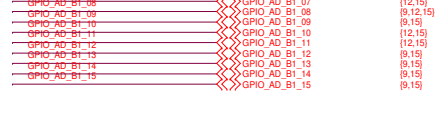
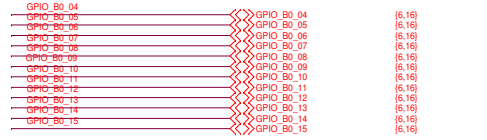
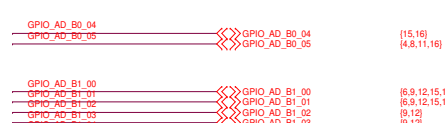
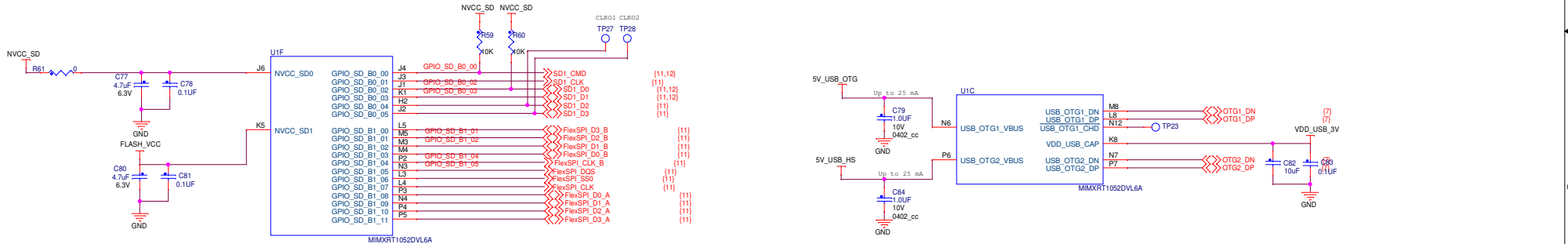
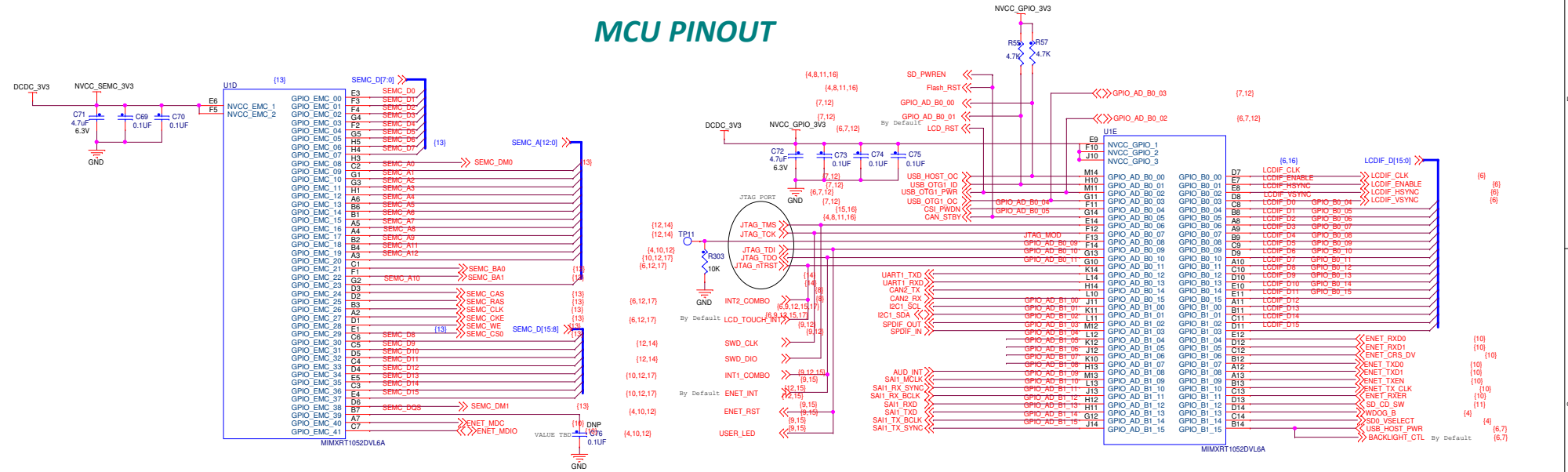
Ground TPs



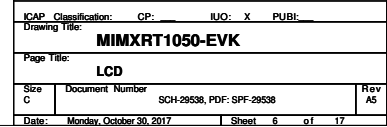
Layout Note: Place Ground TPs to assist signal measurement.



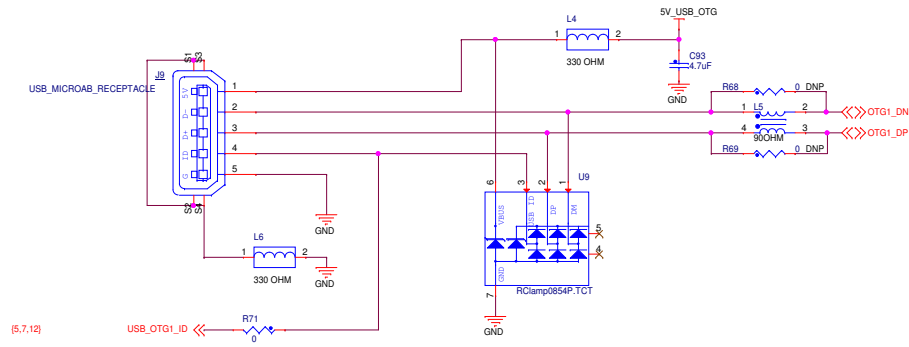
MCU PINOUT



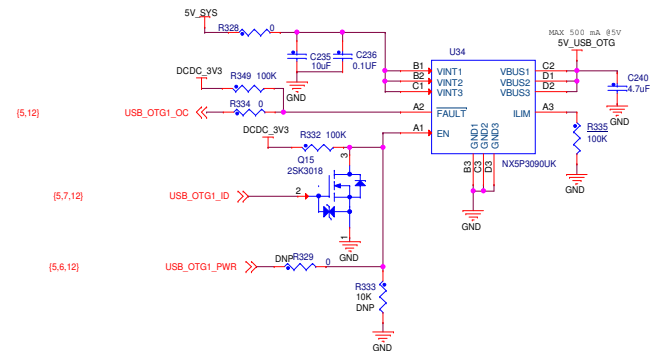
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Drawing Title: MIMXRT1050-EVK			
Page Title: MIMXRT1052DVL6A			
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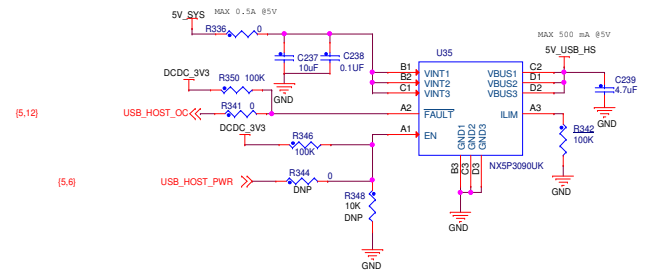
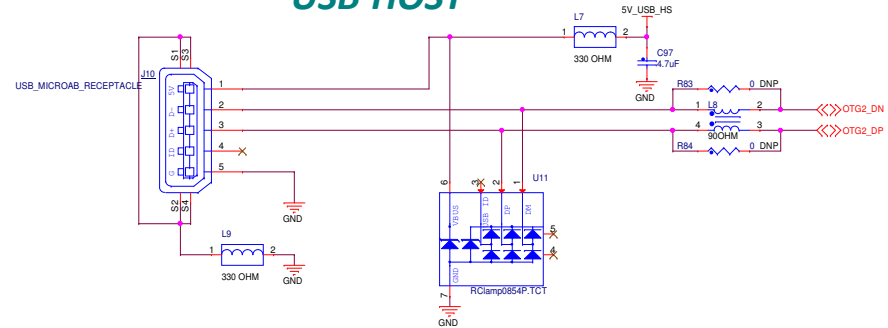
USB OTG



USB POWER

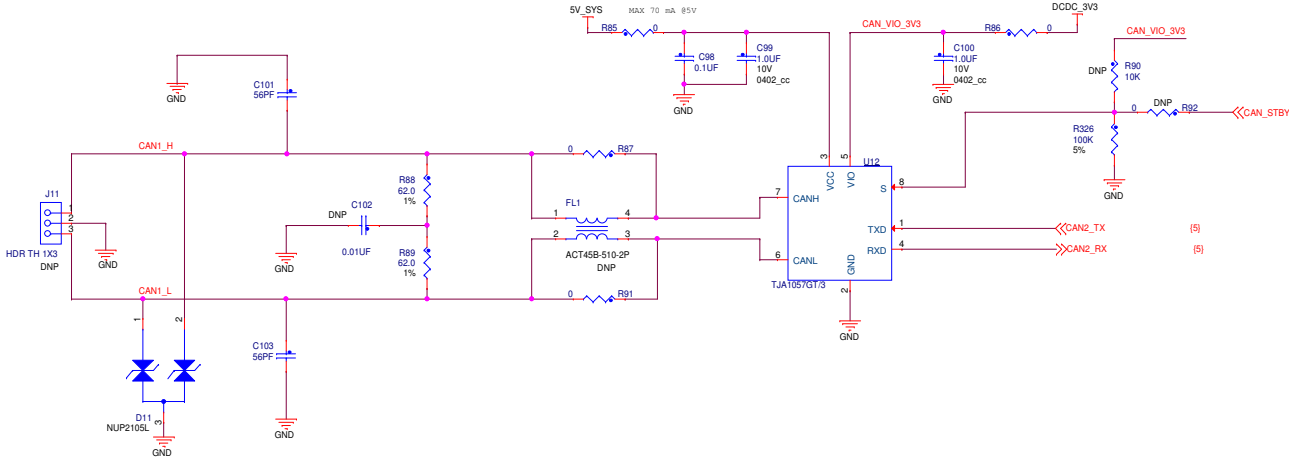


USB HOST

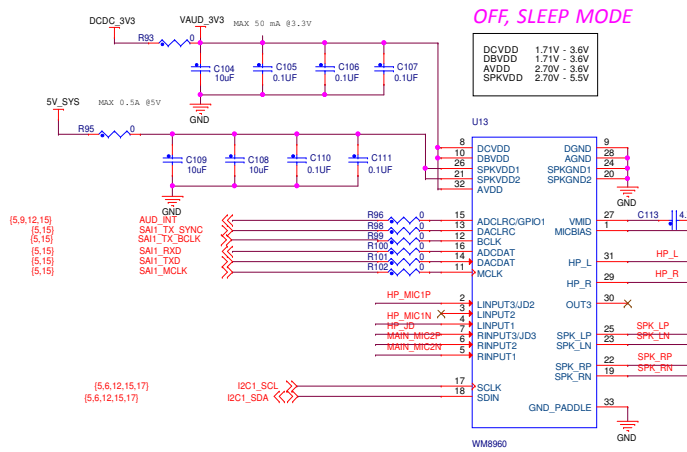


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Page Title: USB			
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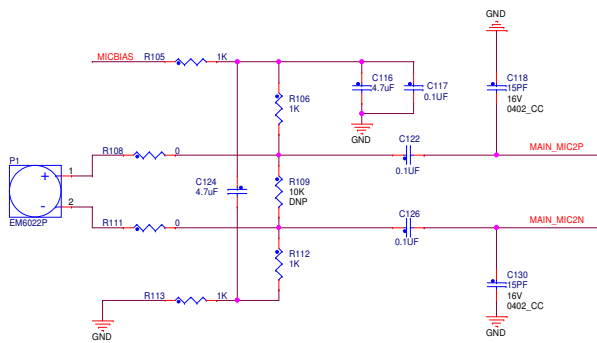
CAN BUS



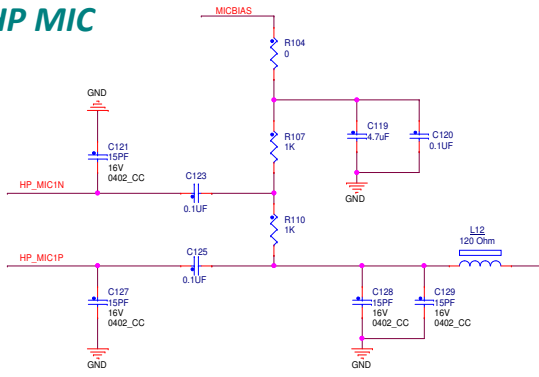
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Drawing Title:					
MIMXRT1050-EVK					
Page Title:					
CAN					
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Main Board MIC

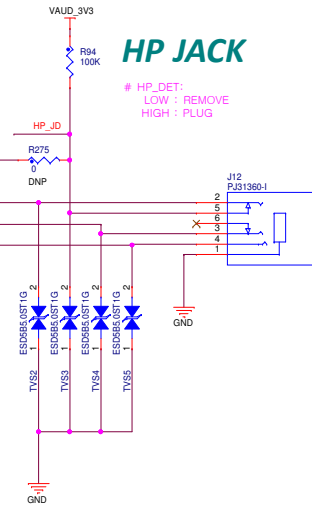


HP MIC

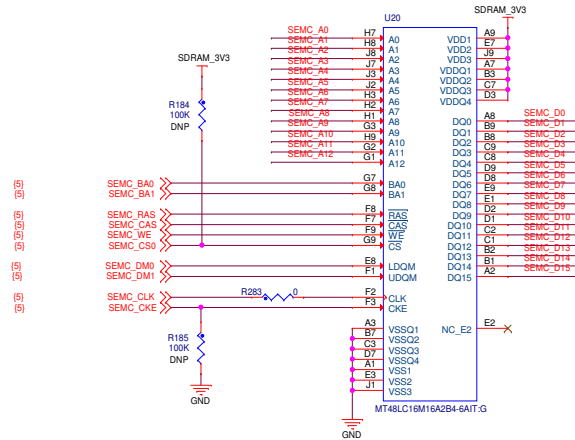
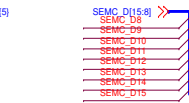
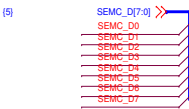
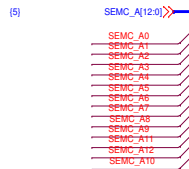
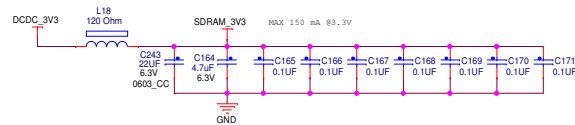


HP JACK

HP_DET:
LOW : REMOVE
HIGH : PLUG

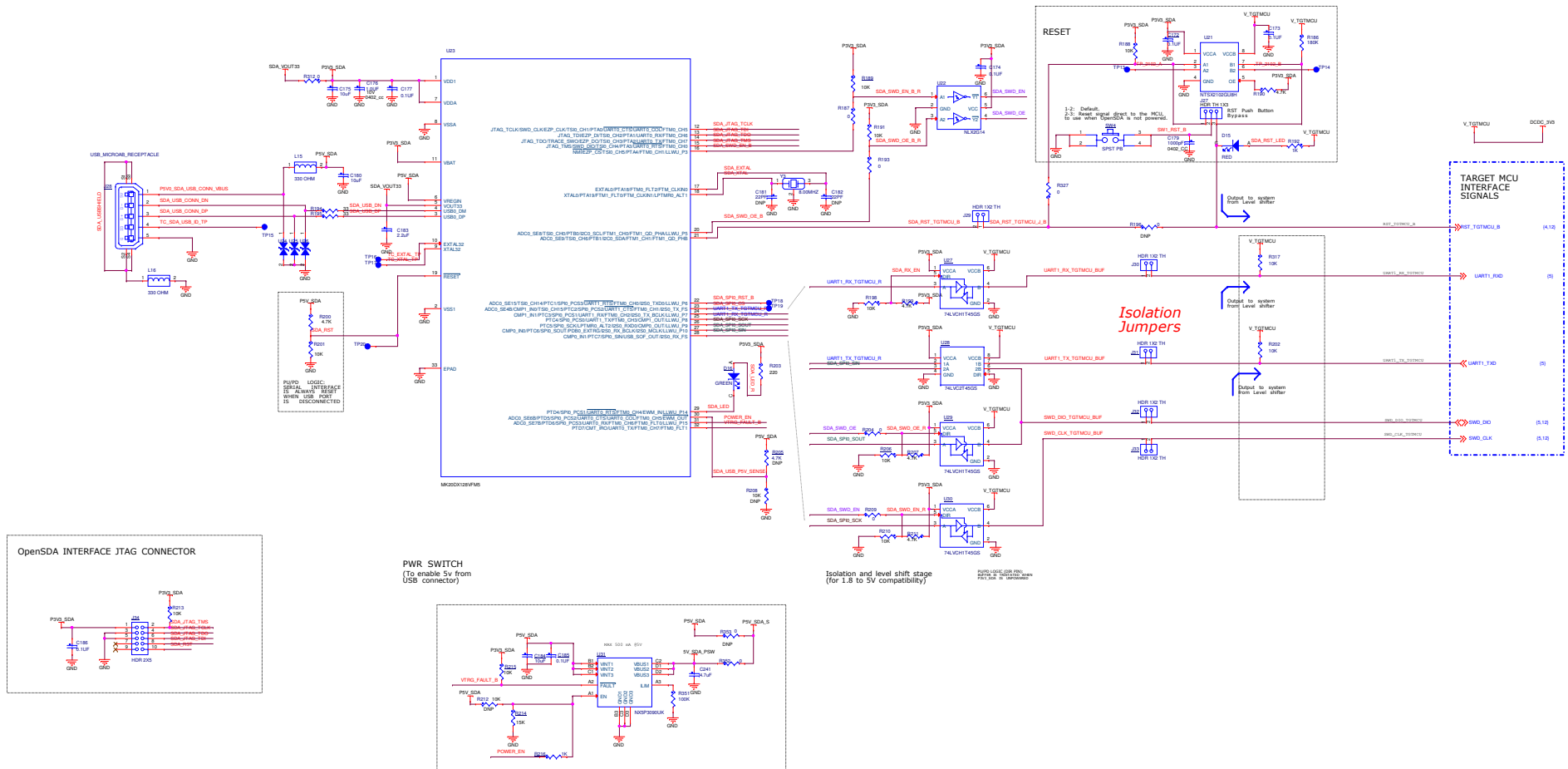


SDRAM



ICAP Classification: GP: IUG: X PUBI:			
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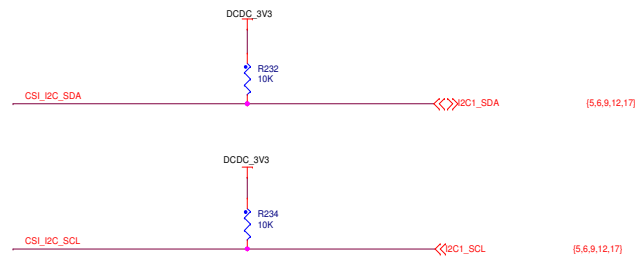
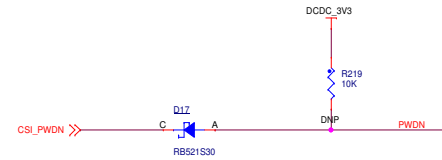
OpenSDA Interface



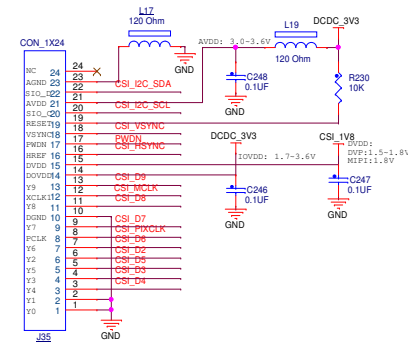
Camera Signals



(5,16)

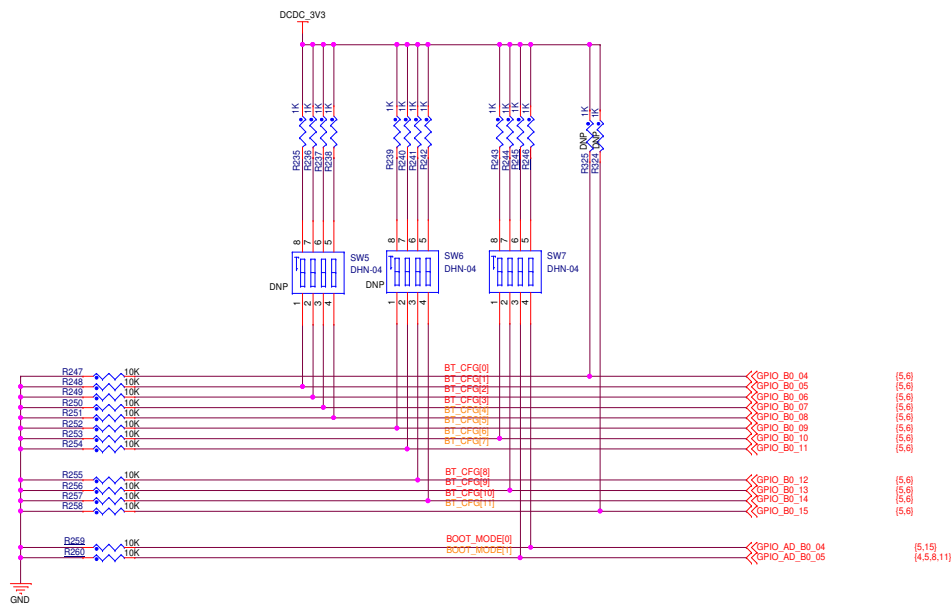


FPC FOR OV7725 MODULE

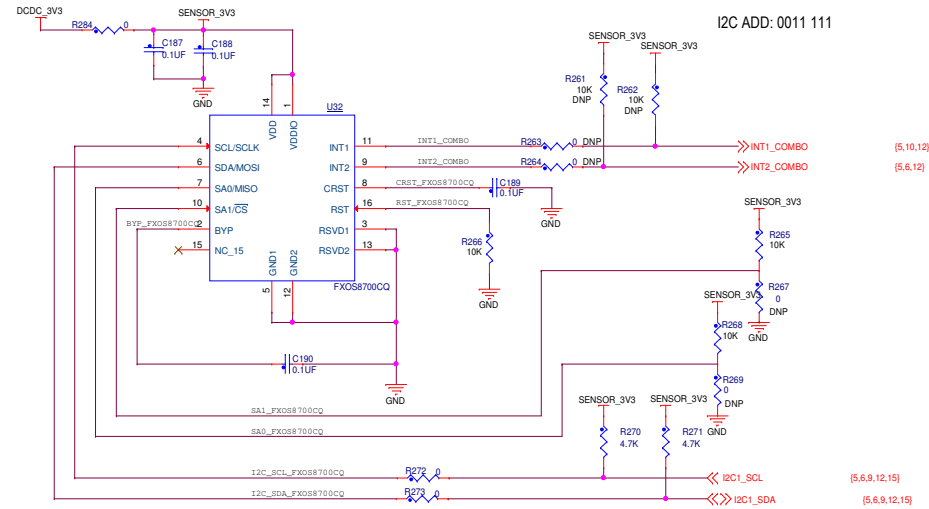


FUSE MAP

USE MAP												
	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
TYPE	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
FlexSPI1 - Serial NOR	Infi nit-Loop (Debug USE only) 0 - Disable 1- Enable	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR				0	0	0	0	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms	EncryptedXIP 0 - Disabled 1- Enabled	Reserved
SD	Infi nit-Loop (Debug USE only) 0 - Disable 1- Enable	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V	0	1	SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable: '0'- No power cycle '1'- Enabled via USDHC_RST pad	SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct	Port Select: 0 - eSDHC1 1 - eSDHC2	Fast Boot: 0 - Regular 1 - Fast Boot



COMBO SENSOR



FXOS8700CQ COMBO SENSOR

